COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JANUARY 1978

VIRTUAL MEMORY DESIGN REDUCES PROGRAM COMPLEXITY

HANDLING MULTILEVEL SUBROUTINES AND INTERRUPTS IN MICROCOMPUTERS

DMA CONTROLLER CAPITALIZES ON CLOCK CYCLES TO BYPASS CPU

Now you can see what's happening on the IEEE-488 bus.

This new adapter and HP's general-purpose Logic State Analyzer give you a clear view of instrument-bus activity for faster design and troubleshooting.

You simply plug the 10050A/10051A Adapter/Test Assembly between the HP-IB** interface and the 1602A Logic State Analyzer. The 10050A/10051A indicates protocol violations and the 1602A can then trigger on the violation for quick identification of the source. In addition, the 1602A can trigger on specific bus signals or data you specify for analysis of any bus transactions. With the real-time view provided by the 1602A, you can quickly locate the problem and identify the equipment at fault in nearly any instrument system based on HP-IB** specifications.

Priced at $1800*, the 1602A is also an ideal Logic State Analyzer for production testing or field troubleshooting of digital equipment. Find out how this versatile Logic State Analyzer and the optional Adapter/Test Assembly, priced at $185*, can help lower your testing and troubleshooting costs whether you're designing and building instrument systems or testing and servicing digital equipment. Get all the details from your HP field engineer.

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** HP's implementation of IEEE Standard 488-1975

088/1

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CIRCLE 1 ON INQUIRY CARD

Models 9100/9300 Vacuum Column Tape Transports. We didn't have to make them this good.

Kennedy vacuum column digital tape transports have been the standard of the industry from their introduction. Some companies would have stopped and relaxed. We didn't. We added features such as our capacitive tape-location detector, for improved tape life; air bearings and tribaloy coated read-after-write heads to reduce tape wear and improve data integrity, and we've achieved the lowest noise level in the industry.

Performance is just as impressive, with tape speeds to 125 ips (75 ips on Model 9100) and operating features such as crystal controlled timing, read threshold scanning, read-after-write shortened skew gate, front-accessible test panel, quick-release hubs and simplified tape loading.

Data densities are 200/556 cpi or 556/800 on our 7-track unit and 800 cpi, 1600 cpi or 800/1600 cpi on the 9-track transport. The format is NRZI/PE.

We could have eliminated some of the features of Models 9100/9300, and still have a transport as good as the best. But we didn't. It's a Kennedy product and it has to be this good.

KENNEDY CO.

540 W. WOODBURY RD., ALTADENA, CALIF. 91001
(213) 798-0953

KENNEDY- QUALITY- COUNT ON IT

CIRCLE 2 ON INQUIRY CARD

Tally reliability. As good as gold.

Tally reliability is unmatched in the printer industry. The value to you is a 100% duty cycle, 200 line per minute printer that costs far less to own. Less than any other printer around.

You can run the T-2000 as long and as hard as you want without the frustration of downtime and costly repairs. Plus, preventive maintenance is unnecessary. Sliding bearings, pivots and lubrication points are eliminated. There are no electronic timing or hammer flight time adjustments. In short, there's nothing to adjust.

The reason behind this unparalleled reliability is the patented Tally print comb mechanism. It uses a unique flexure technology that's impervious to wear and designed for unlimited life. While other printers like to talk about calculated MTBF, Tally points to field proven MTBF. Most of the Tally printers that have been in the field, including those in operation for over four years, have never required adjustment or repair to the print mechanism. In fact, many have experienced no malfunction at all! No one else can safely make that statement. And Tally backs every T-2000 with a full year print mechanism warranty.

The gold printer above is Tally's commemorative unit marking 10,000 machines delivered. The noteworthy statistic is that 99 per cent plus have never had a mechanism failure.

Find out all the facts on this proven performer and call your nearest Tally sales office, or write or call Tally Corporation, 8301 S. 180th Street, Kent, WA 98031. Phone (206) 251-5524.

TALLY **OEM Sales Offices:** Los Angeles (213) 378-0805 • San Antonio (512) 733-8153 • New York (516) 694-8444
Boston (617) 272-8070 • Chicago (312) 325-9788 • Miami (305) 665-5751
Washington, D.C. (703) 471-1145 • Seattle (206) 251-6730 • Business Systems (415) 254-8350

COMPUTER DESIGN

JANUARY 1978

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BPA **CIRCULATION OVER 58,000 (JUNE 1977)**

Publisher's statement of qualified circulation—67,000 since July 1977

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DMA CONTROLLER CAPITALIZES ON CLOCK CYCLES TO BYPASS CPU 117
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CONFERENCES

COMPCON 78 SPRING 66
COMPCON 78 Spring, in 31 sessions on computer technology, will feature areas such as distributed processing and computing, microprogramming techniques, microprocessor developments, high level system languages, LSI testing, and office systems word processing

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In 27 sessions, ISSCC 78 will offer presentations encompassing current and suggested future solid-state circuitry technology on subjects including digital ICs; charge-coupled imagers; static, nonvolatile, and high density memories; and PCM telecommunications

STAFF

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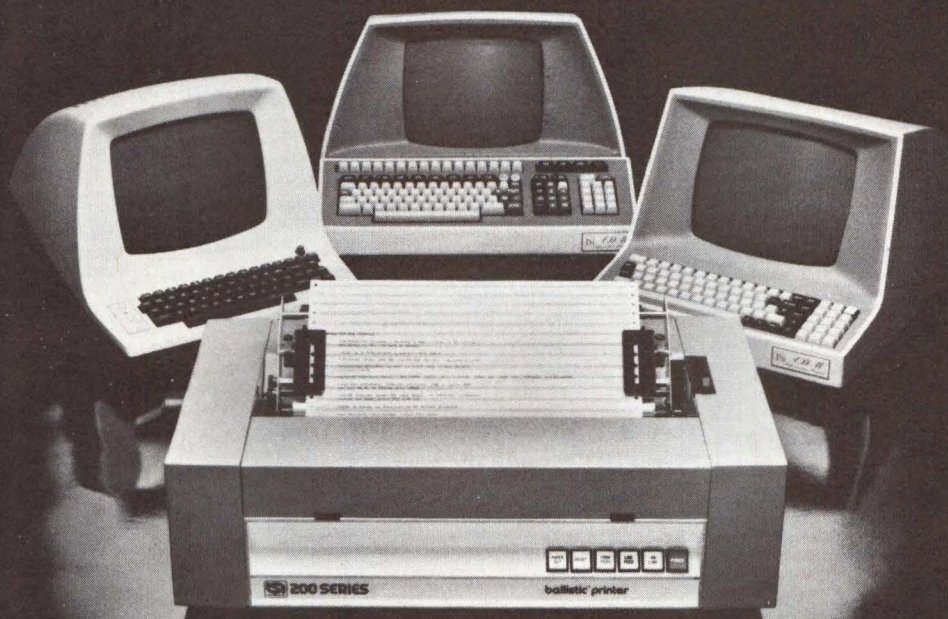
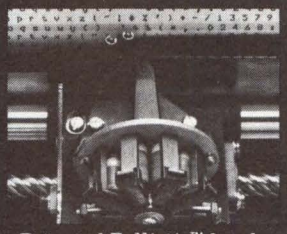
Introducing Lear Siegler's Theory of Relativity.



What goes in must come out.

Lear Siegler, the manufacturer of world famous Video Display Terminals, now gives you hard-copy. The proven dependability in the Dumb Terminal™ and his Smarter Brothers is built into the newest family member – the Ballistic™ Printer.



Patented Ballistic™ head.

Its reliability lies in the simplicity of its patented Ballistic™ head, which has no moving cores attached to the wires. Instead, it uses small "swatters" that propel the matrix wires. And it's designed in such a way as to eliminate tube clogging with inks, dust, and paper fibers. Even wire tip wear is substantially reduced.

The Ballistic Printer prints bi-directionally, at 180 cps, using a lead screw drive – direct, simple, positive, and very accurate. Gone are clutches, gears, belts, return springs and dashpots, along with the possibility of their malfunction or failure. Instead, a servo motor is used to move the head, providing substantially longer printer life.

Add to this such features as fully buffered input. Optional interfaces: serial, RS232, Parallel, and Current Loop. And you can see why we believe our Ballistic Printer is one of the most versatile printers you can buy.

And, of course, the Ballistic Printer plays well with Lear Siegler's entire line of Video Display Terminals.

So if you require a matrix printer with reliability, you should take a close look at ours.

You see, at Lear Siegler, we believe you should get out of your computer what you put into it. Relatively speaking, that is.

Ballistic™ Printer.
Because what goes in, must come out.

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ELECTRONIC INSTRUMENTATION DIVISION
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CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

FEB 2 and MAR 2—Invitational Computer Conf, Pier 66 Hotel & Marina, Ft Lauderdale, Fla; and Breckenridge Inn, St Louis, Mo. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

FEB 6-9—Network-Based Systems Conf and Design Workshop, Ambassador West Hotel, Chicago, Ill. INFORMATION: American Institute of Industrial Engineers (AIIE) Seminars, Dept PR, PO Box 3727, Santa Monica, CA 90403. Tel: (213) 450-0500

FEB 7-10—World Fair for Tech Exchange, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: Dr Dvorkovitz & Associates, PO Box 1748, Ormond Beach, FL 32074. Tel: (904) 677-7033

FEB 8-10—Conf on Word/Text Processing: Problems and Solutions, Jack Tar Hotel, San Francisco, Calif. INFORMATION: American Institute of Industrial Engineers (AIIE) Seminars, Dept PR, PO Box 3727, Santa Monica, CA 90403. Tel: (213) 450-0500

FEB 13-15—WINCON '78 (Winter Conv on Aerospace Electronic Systems), Sheraton Universal Hotel, North Hollywood, Calif. INFORMATION: WINCON '78, 1 Space Pk, Bldg E2/9080, Redondo Beach, CA 90278. Tel: (213) 536-3680

Feb 15-16—6th Annual Midwest Digital Equipment Exhibit, Hopkins House, Minneapolis, Minn. INFORMATION: Clarence K. Peterson, Deerland Distributors, Inc, Hennepin Sq Bldg, Minneapolis, MN 55413. Tel: (612) 331-6433

FEB 15-17—IEEE Internat'l Solid-State Circuits Conf (ISSCC), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 152 W 42d St, New York, NY 10036. Tel: (212) 279-3125

FEB 21-23—ACM Computer Science Conf, Detroit Plaza Hotel, Renaissance Ctr, Detroit, Mich. INFORMATION: Seymour J. Wolfson, Wayne State U, Detroit, MI 48202

FEB 21-23—Datacomm '78, Sheraton Park Hotel, Washington, DC. INFORMATION: Ed Bride, The Conference Co, 60 Austin St, Newton, MA 02160. Tel: (617) 964-4550

FEB 28-MAR 2—COMPCON Spring '78, San Francisco, Calif. INFORMATION: COMPCON Spring '78, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAR 1-3—Control of Power Systems Conf and Exposition, Lincoln Plaza Hotel, Oklahoma City, Okla. INFORMATION: Dr M. E. Council, OG & E Prof, School of Electrical Engineering and Computing Science, U of Oklahoma, Norman, OK 73019. Tel: (405) 325-4721

MAR 5-8—TAPPI Internat'l Pulp and Paper Industry Exhibit, Conrad Hilton Hotel, Chicago, Ill. INFORMATION: Wayne Gross, c/o TAPPI, 1 Dunwoody Pk, Atlanta, GA 30341. Tel: (404) 394-6130

MAR 13-17—IEA/ELECTREX (Internat'l Electrical, Electronic, and Instrument Exhibition), Nat'l Exhibition Ctr, Birmingham, England. INFORMATION: Industrial and Trade Fair Ltd, Radcliffe House, Blenheim Ct, Solihull, West Midlands BN91 2BG, England

MAR 20-22—IECI '78 Industrial Applications of Microprocessors, Sheraton Hotel, Philadelphia, Pa. INFORMATION: Dr S. J. Vahaviolos, Engineering Research Ctr, Western Electric, PO Box 900, Princeton, NJ 08540

MAR 22-24—Internat'l Topical Conf on the Physics of SiO_2 and Its Interfaces, IBM Thomas J. Watson Research Ctr, Yorktown Heights, NY. INFORMATION: Dr Sokrates T. Pantelides, Conf Chm, IBM Thomas J. Watson Research Ctr, PO Box 218, Yorktown Heights, NY 10598. Tel: (914) 945-1207 or 945-3000

MAR 27-31—Automated Business and Banking Equipment Exhibition, U.S. Internat'l Mktg Ctr, Singapore. INFORMATION: George I. Middleton, U.S. Dept of Commerce, DIBA/BIC/OIM, Rm 4126, Washington, DC 20230. Tel: (202) 377-2471

APR 17-20—Design Engineering Show, McCormick Pl, Chicago, Ill. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10017. Tel: (212) 661-8410

APR 18-20—The Society for Information Display Internat'l Sym, Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: Lewis Winner, 152 W 42nd St, New York, NY 10036. Tel: (212) 279-3125

APR 24-26—28th Electronic Components Conf, Disneyland Hotel, Anaheim, Calif. INFORMATION: J. A. Bruorton, Mktg Administration Dept, Union Carbide Corp, PO Box 5928, Greenville, SC 29606. Tel: (803) 963-6348

APR 25-26—26th Annual National Relay Conf, Oklahoma State U, Stillwater, Okla. INFORMATION: School of Electrical Engineering, Engineering Ext 301 EN, Oklahoma State U, Stillwater, OK 74074

APR 28-30—PERCOMP '78, Long Beach Conv Ctr, Long Beach, Calif. INFORMATION: Royal Exposition Mgmt Corp, 1833 E 17th St, Suite 108, Santa Ana, CA 92701. Tel: (714) 973-0880

MAY 9-12—Internat'l Magnetics (INTERMAG) Conf, Palazzo Dei Congressi, Florence, Italy. INFORMATION: E. Della Torre, Dept of Electrical Engineering, McMaster U, Hamilton, Ontario L8S 4L7, Canada

MAY 29-JUNE 7—INTERNEPCON MOSCOW '78 (Internat'l Electronics Production Conf), Expo-Ctr, Pavilion 1, Krasnaja Presnaja Pk, Moscow. INFORMATION: Harry Lepinske, Industrial & Scientific Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

JUNE 12-15—MIMI '78 (4th Internat'l Sym and Exhibition of Mini and Microcomputers and their Applications), Zurich, Switzerland. INFORMATION: Secretariat MIMI '78, Interconvention, c/o Swissair Postfach, 8058 Zurich, Switzerland

JUNE 12-16—7th Triennial IFAC World Congress, Helsinki, Finland. INFORMATION: IFAC '78 Secretariat, POB 192, 00101 Helsinki 10, Finland

SEMINARS

JAN 23-25, FEB 22-24, and MAR 13-15—Minicomputers and Distributed Processing, Atlanta, Ga; Los Angeles, Calif; and New York, NY. INFORMATION: Heidi E. Kaplan, Dept 14NR, New York Mgmt Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

FEB 22-24—Queueing Systems; MAR 6-8—Satellite Data Communications; and MAR 13-15—Experts on Networks, San Francisco, Calif; San Francisco, Calif; and Washington, DC. INFORMATION: Technology Transfer Inc, PO Box 49765, Los Angeles, CA 90049. Tel: (213) 476-1331

MAR 13-15—Computer-Communication Network Design and Analysis, Columbia U, New York, NY. INFORMATION: Heidi E. Kaplan, Dept 14NR, New York Mgmt Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

SHORT COURSES

JAN 30-31 and FEB 1-2—Digital Signal Processing and Digital Filtering with Applications, Kona Kai Club, San Diego, Calif. INFORMATION: Dr Donald J. Rauch, Evolving Technology Seminars, 3720 Jennings St, San Diego, CA 92106. Tel: (714) 224-3780

FEB 27-MAR 3—Data Communications Systems and Networks; and Communications Systems Engineering, Biscayne College, Miami, Fla; and George Washington U, Washington, DC. INFORMATION: Martha Augustin, Continuing Engineering Education; George Washington U, Washington, DC 20052. Tel: (202) 676-6106

We introduced over 100 microcomputer system components in 1977.

Motorola Microcomputers

Motorola now provides

1977 MPU family introductions

- MC3870P — One-Chip Microcomputer
- MC3870CP — One-Chip Microcomputer
- MC3870L — One-Chip Microcomputer
- MC3870CL — One-Chip Microcomputer
- MC6800P — Microprocessor
- MC6800CP — Microprocessor
- MC6800BQCS — Microprocessor
- MC6800CQCS — Microprocessor
- MC68A00P — Microprocessor
- MC68A00L — Microprocessor
- MC68B00P — Microprocessor
- MC68B00L — Microprocessor
- MC6802P — Microprocessor + RAM & Clock
- MC6802CP — Microprocessor + RAM & Clock
- MC6802L — Microprocessor + RAM & Clock
- MC6802CL — Microprocessor + RAM & Clock
- MC6802BQCS — Microprocessor + RAM & Clock
- MC6802CQCS — Microprocessor + RAM & Clock
- MCM6810P — Byte-Organized RAM
- MCM6810CP — Byte-Organized RAM
- MCM6810BJCS — Byte-Organized RAM
- MCM6810CJCS — Byte-Organized RAM
- MCM68A10P — Byte-Organized RAM
- MCM68A10L — Byte-Organized RAM
- MCM68B10P — Byte-Organized RAM
- MCM68B10L — Byte-Organized RAM
- MC6821P — Peripheral Interface Adapter
- MC6821CP — Peripheral Interface Adapter
- MC6821L — Peripheral Interface Adapter
- MC6821CL — Peripheral Interface Adapter
- MC6821BQCS — Peripheral Interface Adapter
- MC6821CQCS — Peripheral Interface Adapter
- MC68A21P — Peripheral Interface Adapter
- MC68A21L — Peripheral Interface Adapter
- MC68B21P — Peripheral Interface Adapter
- MC68B21L — Peripheral Interface Adapter
- MC6840P — Programmable Timer
- MC6840CP — Programmable Timer
- MC6840L — Programmable Timer
- MC6840CL — Programmable Timer
- MC6840BTCS — Programmable Timer
- MC6840CTCS — Programmable Timer
- MC68A40P — Programmable Timer
- MC68A40L — Programmable Timer
- MC68B40P — Programmable Timer
- MC68B40L — Programmable Timer
- MC6843P — Floppy Disk Controller
- MC6843L — Floppy Disk Controller
- MC6844P — DMA Controller
- MC6844L — DMA Controller
- MC6845P — CRT Controller
- MC6845L — CRT Controller
- MC6846P — MC6802 Combo
- MC6846CP — MC6802 Combo
- MC6846L — MC6802 Combo
- MC6846CL — MC6802 Combo
- MC6846BQCS — MC6802 Combo
- MC6846CQCS — MC6802 Combo
- MC6850P — Asynch. Comm. Interface Adapter
- MC6850CP — Asynch. Comm. Interface Adapter
- MC6850BJCS — Asynch. Comm. Interface Adapter
- MC6850CJCS — Asynch. Comm. Interface Adapter
- MC68A50P — Asynch. Comm. Interface Adapter
- MC68A50L — Asynch. Comm. Interface Adapter
- MC68B50P — Asynch. Comm. Interface Adapter
- MC68B50L — Asynch. Comm. Interface Adapter
- MC6852P — Synchronous Serial Data Adapter
- MC6852CP — Synchronous Serial Data Adapter
- MC6852BJCS — Synchronous Serial Data Adapter
- MC6852CJCS — Synchronous Serial Data Adapter
- MC68A52P — Synchronous Serial Data Adapter
- MC68A52L — Synchronous Serial Data Adapter
- MC6854P — Advanced Data Link Controller
- MC6854CP — Advanced Data Link Controller
- MC6854L — Advanced Data Link Controller
- MC6854CL — Advanced Data Link Controller
- MC6854BTCS — Advanced Data Link Controller
- MC6854CTCS — Advanced Data Link Controller
- MC68A54P — Advanced Data Link Controller
- MC68A54L — Advanced Data Link Controller
- MC68B54P — Advanced Data Link Controller
- MC68B54L — Advanced Data Link Controller
- MC6860P — 0—600 bps Modem
- MC6860BJCS — 0—600 bps Modem
- MC6860CJCS — 0—600 bps Modem
- MC6862P — 2400 bps Modem
- MC6862BJCS — 2400 bps Modem
- MC6862CJCS — 2400 bps Modem
- MC6875P — Clock Oscillator/Driver
- MC6875L — Clock Oscillator/Driver
- MC68488P — General-Purpose Interface Adapter
- MC68488CP — General-Purpose Interface Adapter
- MC68488L — General-Purpose Interface Adapter
- MC68488CL — General-Purpose Interface Adapter
- MC68A488P — General-Purpose Interface Adapter
- MC68A488L — General-Purpose Interface Adapter
- MC68B488P — General-Purpose Interface Adapter
- MC68B488L — General-Purpose Interface Adapter
- MCM6830AP — 1K ROM
- MCM6830ACL — 1K ROM
- MCM68A30AP — 1K ROM
- MCM68A30AL — 1K ROM
- MCM68B30AP — 1K ROM
- MCM68B30AL — 1K ROM
- MCM68308P — 8K ROM
- MCM68308L — 8K ROM
- MCM68308CL — 8K ROM
- MCM68A308P — 8K ROM
- MCM68A308L — 8K ROM
- MCM68316AP — 16K ROM
- MCM68316AL — 16K ROM
- MCM68316EP — 16K ROM
- MCM68316EL — 16K ROM
- MCM68316EBJCS — 2048 x 8 ROM
- MCM68316ECJCS — 2048 x 8 ROM
- MCM68A316EL — 16K ROM
- MCM68708L — 8K EPROM
- MCM68708BJCS — 8K EPROM
- MCM68708CJCS — 1024 x 8 EPROM
- MCM68A708L — 8K EPROM
- MCM68332P — 32K ROM
- MCM68322L — 32K ROM
- MCM68A332P — 32K ROM
- MCM68A322L — 32K ROM

2nd Quarter, 1978

- MC6801 — Microprocessor

3rd Quarter, 1978

- MC6809 — Microprocessor

Introduced
Introducing Now
To Be Introduced

Frequency Range
MC68XX = 1.0 MHz
MC68AXX = 1.5 MHz
MC68BXX = 2.0 MHz

Temperature
MC68XX = 0°C to +70°C
MC68XXC = -40°C to +85°C

Package
MC68XXP = Plastic
MC68XXL = Ceramic

Pin-Out Variations
Suffix A, Suffix E

MC68XXBXCS and MC68XXCXCS = Screened to MIL-STD-883 Class B and C

149 devices for 8-bit microcomputer systems

Here's the solid foundation we built on.

Pre '77 M6800 Family

- MC6800L Microprocessor
- MC6800CL Microprocessor
- MC6820P Peripheral Interface Adapter
- MC6820L Peripheral Interface Adapter
- MC6828L Priority Interrupt Controller
- MC6828P Priority Interrupt Controller
- MC6850L Asynch. Comm. Interface Adapter
- MC6850CL Asynch. Comm. Interface Adapter
- MC6852L Synchronous Serial Data Adapter
- MC6852CL Synchronous Serial Data Adapter
- MC6860L 0–600 bps MODEM
- MC6860CL 0–600 bps MODEM
- MC6862L 2400 bps MODEM
- MC6862CL 2400 bps MODEM
- MC6880P Bidirectional Bus Extender
- MC6880L Bidirectional Bus Extender
- MC6881P Bidirectional Bus Switch
- MC6881L Bidirectional Bus Switch
- MC6885-88P Hex Address Bus Extenders
- MC6885-88L Hex Address Bus Extenders
- MC6889P Quad Data Bus Extender
- MC6889L Quad Data Bus Extender
- MCM6810L 1K Static RAM
- MCM6830AL 8K ROM
- MCM6832L 16K ROM

Introduction of 30 more M6800 Family devices pushes the number of Motorola microcomputer system components added in 1977 to 124. The M6800 Family now offers 145 fully-compatible components ranging over 26 system functions in a variety of performance and package options.

Then, of course, there's the completely supported low-cost, low-end MC3870 single-chip microcomputer we introduced recently.

Motorola now provides a complement of 8-bit system components that's virtually unsurpassed in completeness and flexibility. Taken all together, this is the kind of product offering we believe industry has a right to expect from Motorola. It's a reflection of Motorola's massive worldwide commitment to serve industry's microcomputer requirements.

Looking ahead to just two of the major near term products, the single-chip MC6801 and advanced MC6809 microprocessor are an affirmation that our commitment is a continuing one.

Peripheral controllers give year big finish.

All year, significant new products have been making their first appearances, and in December we see several of the most eagerly awaited and most interesting debuts.

The MC6843 is a versatile controller for performing the microprocessor-to-Floppy disk interface. The MC6844 is a Direct memory Access Controller designed to work with a clock pulse generator and I/O Device controller. A third new peripheral controller is the MC6845 for the microprocessor-to-CRT interface. Also worthy of special notice is the MC6875 Clock Oscillator/Driver, the latest bipolar member of the M6800 Family.

Let us demonstrate the desirability of Motorola components for your systems. You won't be disappointed. Use the coupon today for a fast, personalized response.

CD124

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Motorola Microproducts, 3501 Ed Bluestein Blvd., Austin, Texas 78721

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The mind to imagine... the skill to do.

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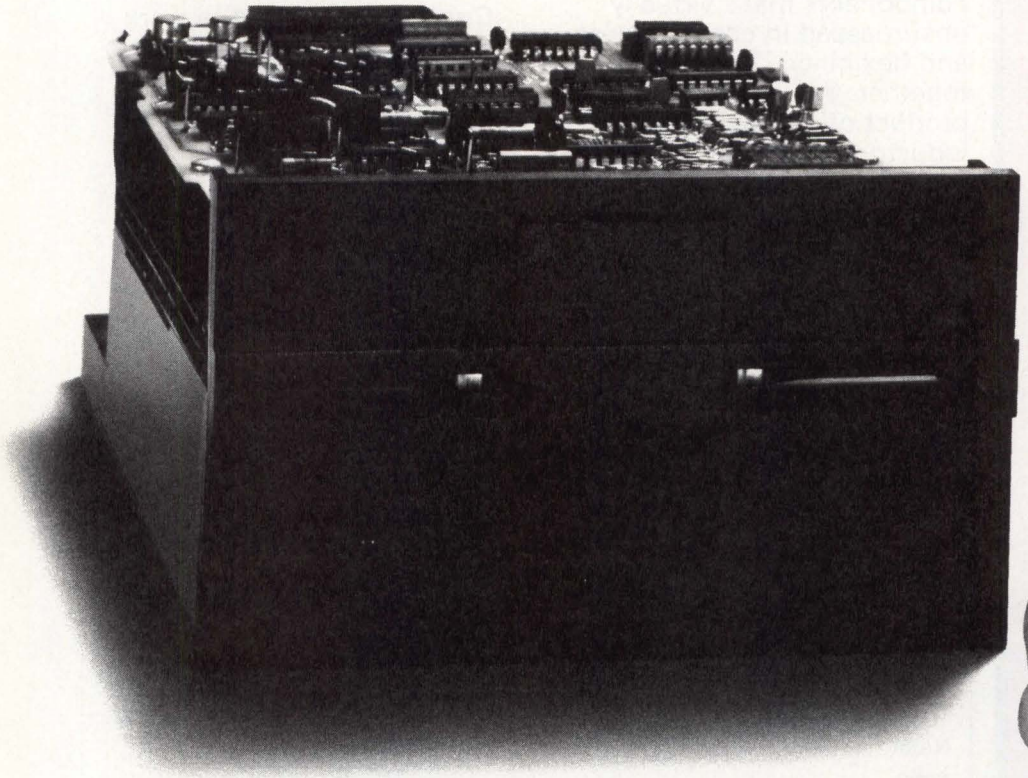
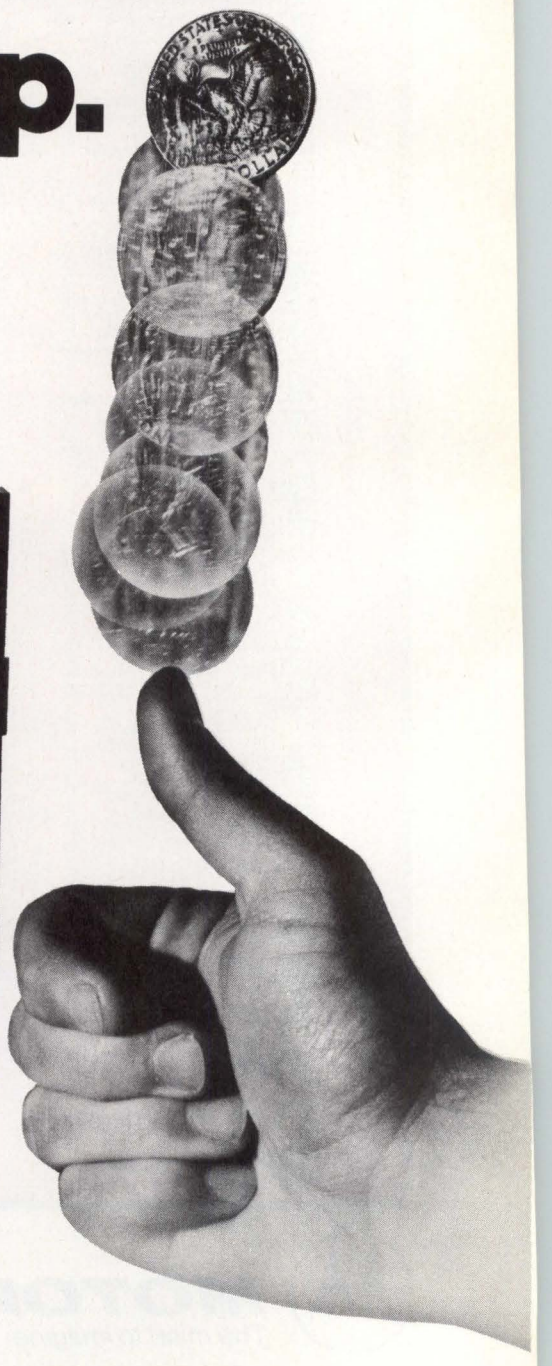
440 Kbytes on-line without a flip.

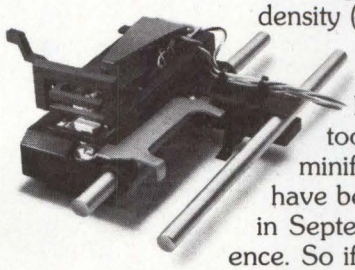


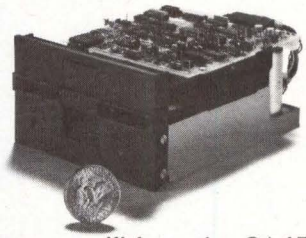


from number 1

Introducing Shugart's SA450 double-sided minifloppy.®

Why flip? Nobody delivers this much *on-line* data storage from a single minifloppy disk drive with total compatibility. Nobody but Shugart offers a complete family of minifloppy disk products. Now a single minidiskette™ can carry operating system software, application programs or about 220 pages of text. All avaliable on-line. Reach 440 Kbytes (unformatted) with random access speed. Without flipping media. **Two heads are better than one.** The proprietary Shugart head design allows you to read and write both sides of the minidiskette. So you can write and read larger data files without the delays and risks that come from additional diskette handling. **We promised. We delivered.** The SA450 delivers true upward expansion based upon the industry standard 35 track format. This proven *Format With a Future* allows you to use single or double-sided minidiskettes without sacrificing the margin that you've come to expect with the minifloppy. **Proven technology—single or double density.** The Shugart SA450 minifloppy disk drive has the same compact size and low weight as the original minifloppy—the Shugart SA400. And it's electrically, mechanically, and media compatible. Double density (MFM/M²FM) is standard, but you can also operate single density on one side or two. **There's more.** The unique direct-drive spiral cam actuator.





Low heat dissipation, write protect, activity light, die cast base plate, and DC drive motor, too. But you get the idea. Nobody makes more minifloppy disk drives than Shugart. Over 25,000 have been installed since we introduced the little guy in September 1976. Nobody can claim more experience. So if you want 440 Kbytes of on-line storage, big drive data integrity, with proven reliability—and you're into word processing, intelligent terminals, small business systems or home computing—you'll love the SA450. Why flip? You can have the real double-sided minifloppy from the people who started the minifloppy revolution. Shugart.

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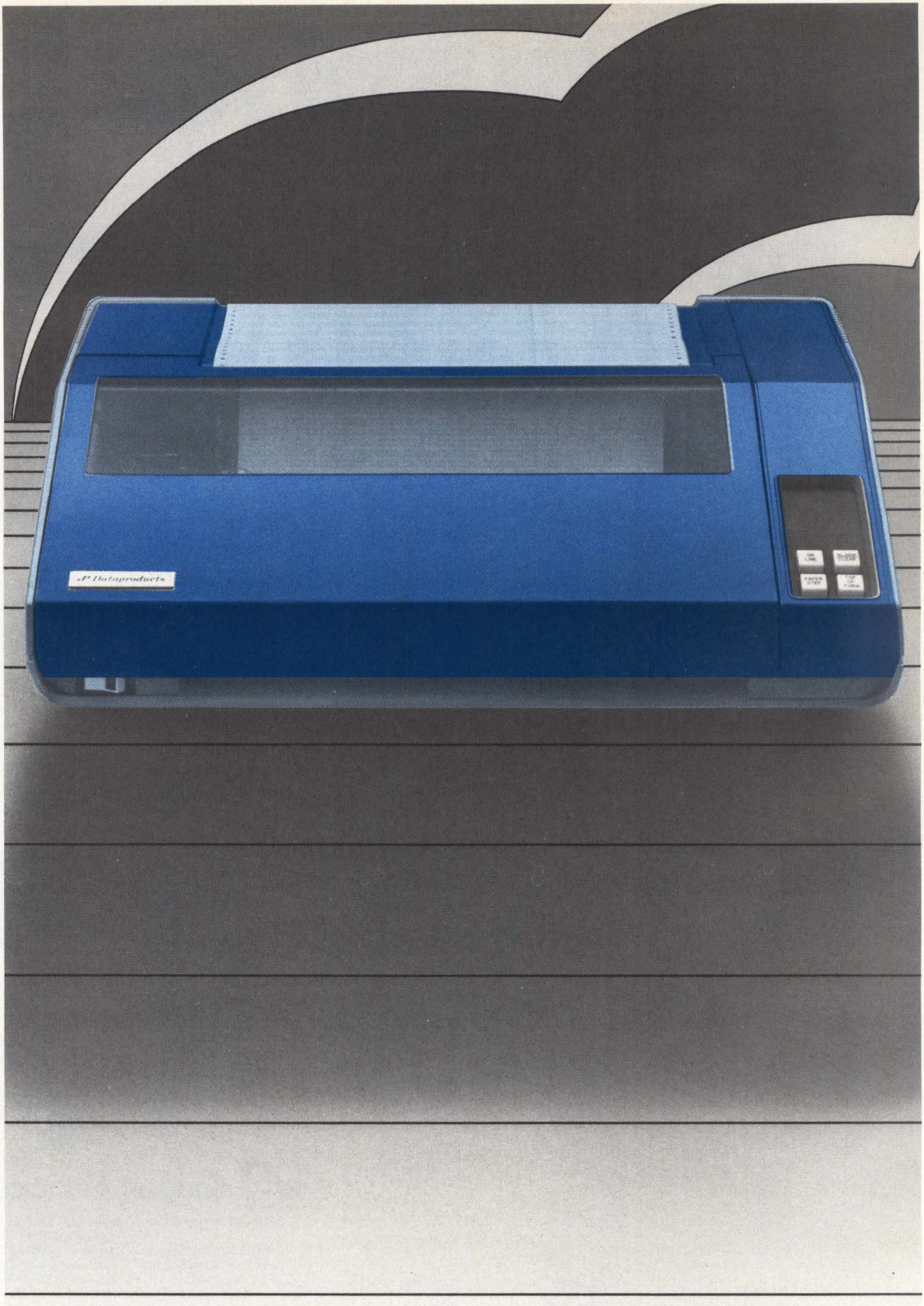
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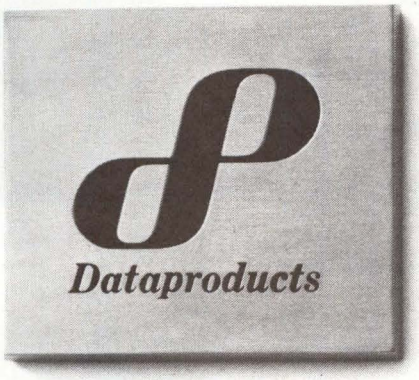

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LOCAL MODEMS

John E. Buckley

Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

Data communications systems have traditionally used modulating/demodulating equipment to convert information signals from the digital domain of data processing to the analog environment of the telephone network. In order to transmit information between two locations it has been necessary to convert digital information into a form that exhibits the same characteristics as human voice. Since the telephone system was originally conceived and developed for voice transmission, it was data communications systems that always had to compromise their signal characteristics. Only with the recent advent and projections of digital transmission systems could elimination of modulator-demodulators (modems) be envisioned. The universal application of digital transmission also is recognized as a distant possibility rather than a short-term probability.

For those applications with data terminals located within a few miles of their central processing center, the existence of local modems, also referred to as short-distance or short-range modems, can provide both economic and operational benefits. These devices do not utilize typical modulation/demodulation techniques that characterize normal modems used in data communications systems. Primarily line drivers, they require a wide frequency spectrum from the interconnecting communications facility. As a result, the normal carrier-derived voice grade channel cannot be used. Telephone company supplied local exchange loops or an unloaded cable is required. In effect, the necessary communications channel must be a 4-wire metallic circuit.

Local modems have been used extensively in applications with a number of remote data terminals or input/output peripherals located in the same building complex as the data processing center. However, these same types of modems now are being installed for data communications use in situations where the data terminals are in the geographical vicinity of the intended processing center rather than in the same building complex.

As with most innovative steps in this technology, not all components advance at the same rate. Local modems are presently being marketed by a number of manufacturers, but not all telephone companies have a tariff to provide the required communications facility. Prospective users of these modems could encounter a lack of understanding or responsiveness when they approach the local telephone company for the required facility. Fortunately, the Bell System has a technical reference manual (PUB 43401) that defines operating specifications that must be met by these local modems. Using this publication and describing the intended application will enhance the probability of the user's obtaining the proper communications channel.

The local modem with a 4-wire metallic connection having a wide operating bandwidth is able to avoid limited bandwidth characteristics of the typical type 3002

Data Transmission Rates of Local Modems In Relation to Cable Gauge of Metallic Circuit

Data Rate (bits/s)	Range In Feet (Kilometers)			
	No 19 Wire	No 22 Wire	No 24 Wire	No 26 Wire
1800	100,000 (30.5)	80,000 (24.4)	60,000 (18.3)	48,000 (14.6)
2400	100,000 (30.5)	80,000 (24.4)	60,000 (18.3)	45,000 (13.7)
4800	80,000 (24.4)	60,000 (18.3)	45,000 (13.7)	30,000 (9.1)
7200	75,000 (22.9)	45,000 (13.7)	35,000 (10.7)	25,000 (7.6)
9600	70,000 (21.3)	44,000 (13.4)	30,000 (9.1)	22,000 (6.7)
19,200	53,000 (16.2)	22,000 (6.7)	22,000 (6.7)	15,000 (4.6)

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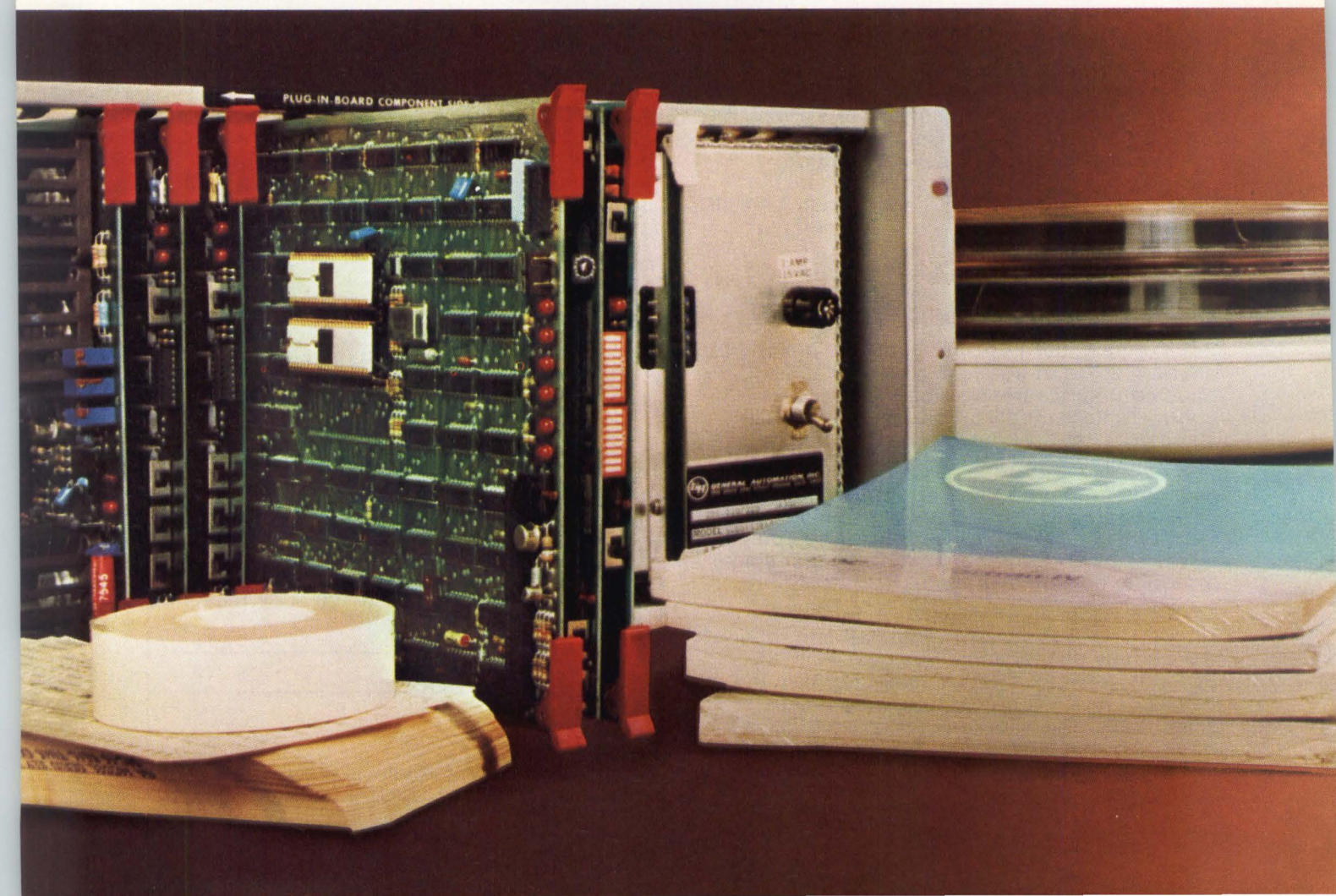
data channel. This channel usually has an operating frequency spectrum from 700 to 3100 Hz. Channel conditioning coupled with the associated modem's operating characteristics may tend to modify the exact quantified operating spectrum of a type 3002 data channel. Traditional modems operating at 2400 bits/s and above must manipulate the actual digital bit stream at the EIA interface to create a minimum number of transmission samples or states in a unit of time. The 2400-bit/s modem (Bell 201 series) actually modulates the communications channel (type 3002) at 1200 baud. Each transmission state represents the value of two adjacent digital bits; thus, the 201 family is referred to as "dibit" modems. Even higher speed modems operate on the basis of 3- or 4-bit bytes represented by a single transmission or modulation state. These higher speed modems are classified as "tribit" and "quadrabit" modems. Their primary purpose is to force-fit a high speed digital bit stream into the bandwidth constraints of a carrier-derived voice grade channel.

The local modem concept assumes that the inherent bandwidth of an all metallic circuit is not limited by the channelization of a carrier system and is strictly a function of the impedance of the metallic circuit and any components used to configure that circuit. Telephone companies that provide channels for local modems become very concerned about the local modem's transmit levels. Any bandwidth limitation of a metallic circuit can be overcome by merely increasing the output power of the local modem; this would easily create a broadcasting situation as the metallic circuit continued to radiate the majority of the local modem's output power. If the metallic circuit can be established as an unloaded circuit, the upper bandwidth frequency limitation would be sufficient to permit only a low output power, such as 40 to 50 mW, from the local modem to achieve reliable data transmission. Unfortunately, local telephone exchange loops are usually loaded circuits, commonly used in order to reach extreme points in a telephone office's typical exchange areas. The telephone company introduces inductance into the local loop to reduce the signal attenuation that normally occurs over 8 to 10 miles (13 to 16 km) in channel length, thereby improving attenuation while significantly impacting bandwidth. Since the bandwidth parameter is the most important criterion as well as the least adjustable by the local modem, an unloaded metallic circuit must be installed.

A wide spectrum of data transmission rates are provided by these modems depending on the actual gauge of the cable that comprises the metallic circuit. As shown in the Table, a representative local modem can provide essentially wide-band transmission data rates on local metallic circuit. It is extremely important to note that the distance specified in this table refers to circuit distance and not the actual direct distance between the two points to be connected. Telephone companies normally do not specify actual circuit mileage. Since a local modem's successful operation is dependent on actual circuit distance, this parameter must be precisely assessed within an acceptable range of accuracy.

Local modems are available in both asynchronous and synchronous models. The purchase price difference between the two types—approximately $300 for the asynchronous and $900 for the synchronous—is sufficient to lead prospective users to select an asynchronous model; and



as if to further mislead them both versions specify essentially the same data rate capabilities. The basic difference is that the synchronous model provides the transmit and receive clock or timing source. In addition, this timing source is complemented with the necessary circuitry to maintain both local modems at each end of the metallic circuit in bit timing synchronization. The asynchronous model depends on the occurrence and recognition of a start and stop bit time associated with each data byte to reset and synchronize the data timing clocking sources.

The economics applicable with local modems are the primary incentive for this approach. System cost savings can be readily recognized when a proposed 4800-bit/s data communications application is considered. Synchronous modems such as the Bell 208 series conventionally would be utilized with a type 3002 data channel. These modems from the local telephone company would require a monthly rental payment of approximately $100 each; a local synchronous modem could be leased for approximately $25/month each. Assuming that the type 3002 data channel and 4-wire metallic circuit are equivalent in price, the pair of local modems would cost only $50 as opposed to $200 for the Bell 208 modems. This is a monthly savings of 75%.

In addition to economic advantages, the resulting data reliability can also be expected to improve. The traditional modem previously discussed must modify the digital bit stream to construct and transmit samples or states whose maximum rate of change does not exceed the available frequency bandpass of the channel. This data compression procedure requires that the traditional synchronous modem interpret and reconstruct the digital bit stream. The conversion is dependent on the timing accuracy as well as the demodulator's signal recovery capabilities. Many so-called transmission data errors can be traced to the fact that the transmitted signal has been distorted beyond the limits of its capability in the associated demodulator. The local modem transmits a single state for each digital bit value; the value of bits per second is equal to the value of baud. Since the usual complex and error prone conversion is no longer required, the resulting data transmission can be expected to be more accurate with respect to these factors.

Both system economy and accuracy are stimulating this interest in local modems; the Bell System has indicated that a local modem product is soon to be included in their data communications product line. These advantages are realized by adding the new requirement of physical circuit criteria with respect to circuit distance, and actual cable wire gauge and loading components. Most telephone companies have noted that if certain output power limits are adhered to by the local modem, a metallic circuit can be configured and installed; virtually all the telephone companies, however, disavow any assurance that the metallic circuit will meet all circuit design parameters. The basic attitude is that a metallic circuit will be installed, but successful operation can only be determined by initial tests. Ordering of any local modems from a manufacturer on a lease or purchase basis must always reserve finalization of the purchase until the actual metallic circuit is tested. If successful, data communications system users will obtain more economical and reliable methods of data communications.

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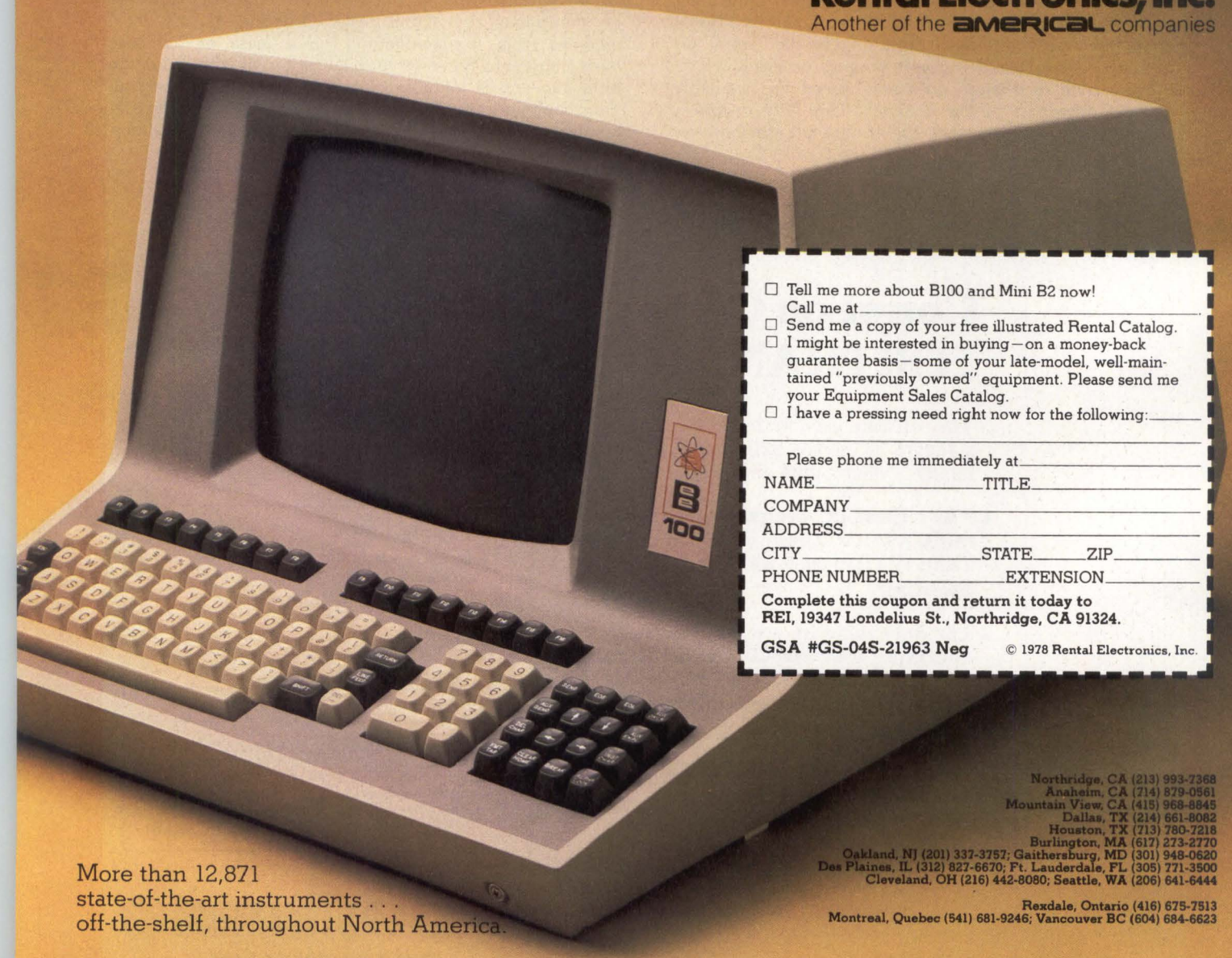

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CIRCLE 10 ON INQUIRY CARD

Direct Connection Modem Automatically Recognizes and Communicates With VA3400/103/212 Modems

Time-sharing organizations with data communications networks having different, noncompatible type modems at remote sites will benefit from the VA3467 answer-only modem. It automatically recognizes and communicates with Vadic VA3400 (1200 bits/s, full duplex), Bell 103 (300 bits/s, full duplex), and Bell 212 (1200 bits/s, full duplex) modems without changing interface protocol. Located at central computer sites, the unit serves to advance full duplex asynchronous data communications.

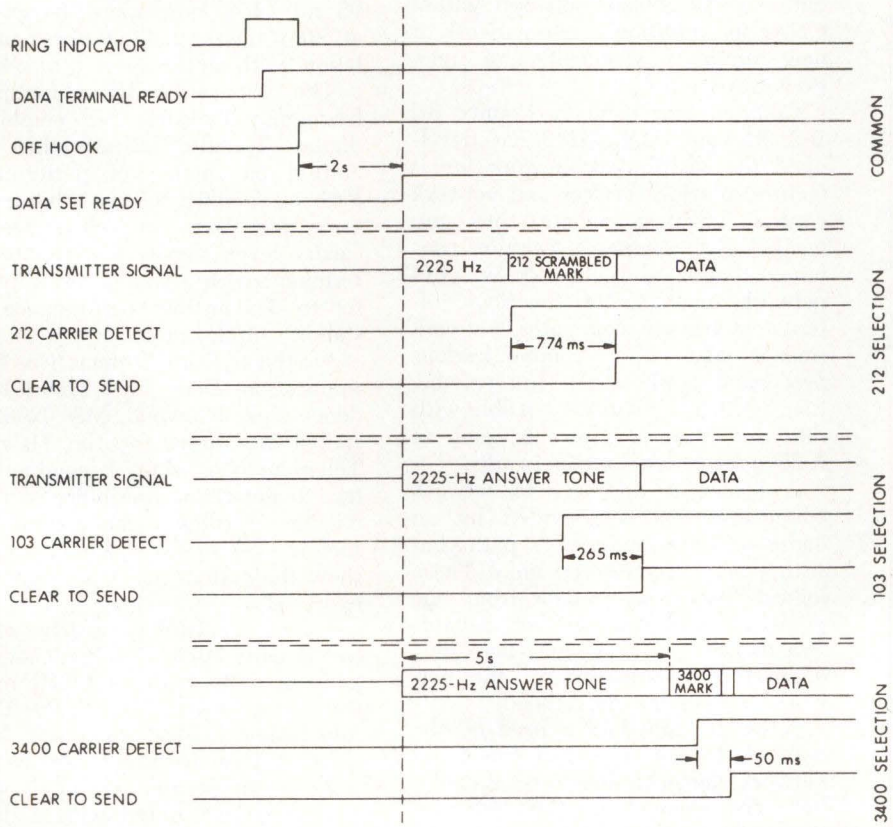
Complying with FCC requirements, the compact package has all components needed to connect directly to switched telephone lines through a telephone company supplied data jack, eliminating the need to rent DAAs from the phone company. Different cables are provided to accommodate other line configurations, including connection to a Bell CBS or CBT DAA. This direct connection eliminates split rotors, and enables one phone number to suffice for all asynchronous ports.

Vadic Corp, 222 Caspian Dr, Sunnyvale, CA 94086 designed the modem around a microprocessor that handles all control and various data processing functions. The microprocessor software and specialized analog circuits are integrated, performing several functions. The modem occupies two card slots in the standard VA1616 or 1601 chassis; eight modems can be housed in 7" (11 cm) of rack height. Other components include an Intel 8035 microprocessor, 2708 1k x 8 EPROM, and 8243 I/O expander.

The automatic recognition sequence identifies the calling modem (if it is a 3400, 103, or 212) without disturbing normal connect protocols. A ring signal passed to the terminal, together with Data Terminal Ready back from the terminal, causes the modem to go off-hook, answering the call. After a 2-s delay to protect telephone company billing equipment, the modem turns on Data Set Ready and initiates the select sequence by first sending a 2225-Hz answer tone, then looking for a 212 or 103 mark carrier (212 carrier is scrambled).

Finding one triggers an appropriate Clear To Send delay; the VA3467 locks into the correct mode until disconnected. If neither one is detected during the first 5 s, the modem switches the transmit signal to the VA3400 low band mark carrier (2025 Hz) for 3 to 6 s, then looks for a high band response from the remote VA3400 or acoustic coupler. Remote VA3400s in the originate mode will not send a carrier until a carrier is detected from the answering modem.

If the VA3467 finds this carrier, it locks into the VA3400 mode until disconnect. If a VA3400 carrier is not found, the VA3467 starts the se-



Initiating modem select sequence as diagrammed, VA3467 modem first sends 2225-Hz answer tone, looking for either a 212 (scrambled) or 103 mark carrier. Finding either triggers appropriate clear-to-send delay which locks unit into correct mode until disconnected. If neither is detected during first 5 s, modem switches transmit signal to 3400 low band carrier, looking for 3400 high band receive carrier. Finding the carrier, it locks into 3400 mode; otherwise modem starts complete sequence again, repeating process until it is disconnected or mode is correctly established

quence again, repeating the process until it is disconnected or a mode is correctly established. Both terminal controlled and automatic disconnect are included in the modem.

Terminal interface operation is transparent to the actual modem used. A single telephone line can be used to support three different types of calling modems, without amending software or establishing new connect procedures for remote terminals.

Full user diagnostics include analog loopback/busy out, digital loopback, and transmit reversals. A continuous self-test capability of the modem turns on its transmitter, switches the receiver to the same carrier, and sends a scrambled mark into the transmitter. If the receiver does not obtain a steady mark after descrambling, or if microprocessor memory or I/O fail, a status light flashes to indicate that there is a problem.

Other configurations of the modem are available. Model VA3427 combines a VA3400 and Bell 212; VA3437 supports 3400 and 103 operation; and VA3447 communicates with the 3400 only. Single unit price of the VA3467 is $850.

Circle 400 on Inquiry Card

Facsimile Service Transmits Messages Quickly, At Lower Cost

A tariff for a facsimile transmission service, which can send a 1-page message from California to New York in 1 min for 20 cents or less, has been approved by the FCC. Controlled by computerized switches and capable of speeds up to 9600 bits/s over dial-up digital channels, the Speedfax service has been introduced by Southern Pacific Communications Co, One Adrian Ct, Burlingame, CA 94010 for business and government users of SPC private line communications network.

A moderate volume of facsimile messages can be transmitted inexpensively at speeds of from 1 to 6 min/page; transmissions of higher volumes at faster speeds are also possible. Rates for the service are based on volume—price per page decreases with increased use. Customers may furnish their own terminal equipment, or the company will furnish both slower and faster terminals.

Circle 401 on Inquiry Card

Flexible Communications Network Architecture Adapts to Changes

Developed to ensure consistent, cost-effective processing systems for data communications networks both now and in the future, the Communications Network Architecture (CNA) provides a greater level of capability, configurability, and network independence. It is fully compatible with all IBM host processors, terminals, and teleprocessing access methods, as well as the company's other communications products and software.

Users can combine IBM's Emulation Processing and System Network Architecture functions into a single communications network that provides for implementation of networks that do not depend on host processors for network control functions. The network allows preservation of present investment in terminals, host computer systems, and software; consolidation of all present networks within CNA; and addition to the network of new terminals, protocols, and functions as required.

Comten, Inc, 1950 W County Rd B-2, St Paul, MN 55113 has developed the distributed network architecture, placing services and network control functions where they are needed in the network. Features contained within the network are full network management functions, alternative transmission paths, network transparency, and communications processing applications. Interconnection to other networks is possible with differing interface protocols, such as X.25 packet switching networks.

A structured approach to network communications is provided by an end-to-end communications path consisting of interconnected links. These logical links convey data from one point (or node) to another, regardless of the specific circuit, line, link, or protocol characteristics; the network resolves the differences.

A set of guidelines is used by the network to define logical functional network elements, and to set up rules for using elements in the design of communications processing systems. CNA defines layered network structures—elements are organized into logically-related layers with rules governing their communication. This localizes effects of system changes and facilitates development of compatible systems. Supporting multilevel network structures—networks of networks—allow the merging of different systems in the same physical network; thus older functions are blended with newer ones.

The network is viewed as an independent entity that provides and maintains communication between end users, freeing them from constraints of host processors. The processor is thereby freed for more effective applications processing. Network independence also promotes distributed processing, since the network accommodates multiple host processors and physical separation of applications programs.

Circle 402 on Inquiry Card

Test Studies 98-Mile Digital Radio Link Between Hawaiian Islands

The RDS model 6200 microwave radio system, a 1344-channel, 6-GHz digital radio link, is operating between mountaintop sites on the Hawaiian islands of Oahu and Kauai, 98 mi (158 km) apart. It operates at 90M bits/s, using 8-phase modulation, with efficiency of 3 bits/Hz.

The system is configured for space/frequency diversity, and employs a digital diversity "hitless switch" operating on quality of performance. Path availability to any arbitrary bit error rate (BER) as well as receiver carrier levels versus BER can be determined with a BER availability test set to demonstrate performance and stability of the radio.

Raytheon Data Systems Co, Communications Dept, 1415 Boston-Providence Tpk, Norwood, MA 02062 installed the units for the Hawaiian Telephone Co, which is conducting a test to determine feasibility of transmission of digital modulation over such a long path. Preliminary results show the system to be performing as expected.

Upon successful completion of the test in early 1978, the telephone company plans to install a 6-GHz microwave radio system to link the Honolulu Bishop Central office to its Kauai office. T-1 carrier trunks between the islands will permit all-digital operation when integrated with a digital switching system scheduled to be installed in the Honolulu office in 1979.

Circle 403 on Inquiry Card

The PerSci generation of Diskette Mass Storage Systems Smarter, Faster, Smaller.

A new generation of advances in diskette drive technology comes together in PerSci Mass Storage Systems, the first diskette subsystems to provide large storage capacity, intelligence and high speed in as little as 4½" of space.

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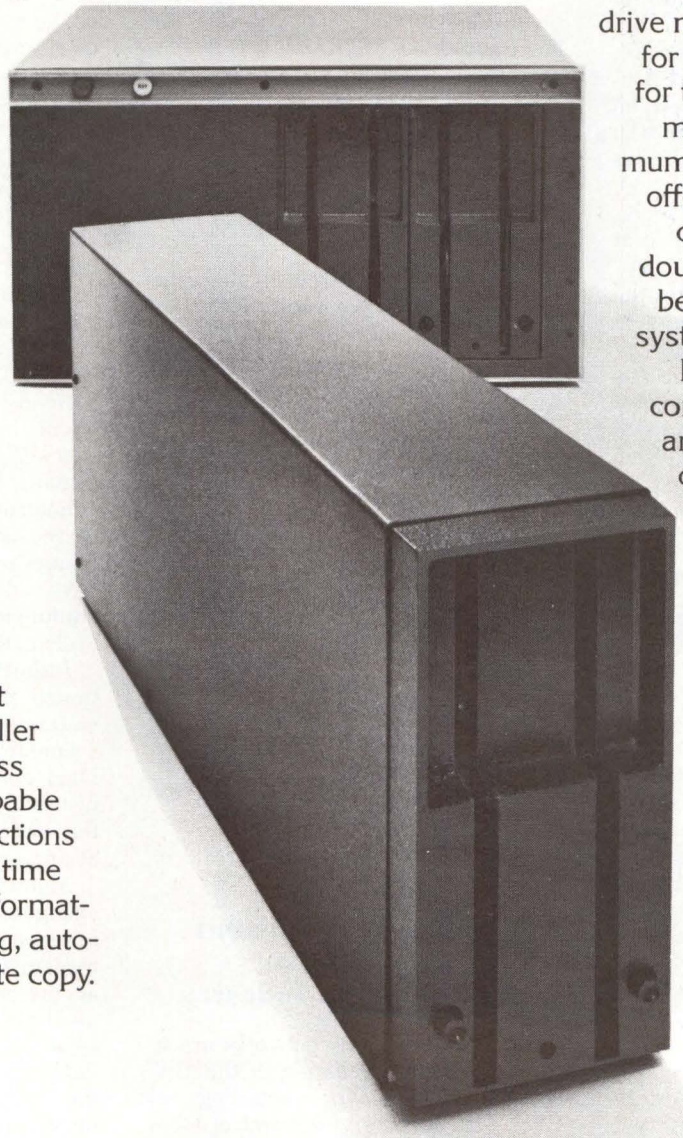

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CIRCLE 36 ON INQUIRY CARD

Approved Tariff Revisions Reduce Many Network Prices

Revisions to Tymnet's Tariff No. 1 have been approved, thus matching prices for its public packet network interface equipment more closely to users' actual requirements as measured by the number of terminals requiring simultaneous support. Under terms of the tariff, 1200-baud service for up to eight terminals meeting simultaneous support is priced at $1250/month, $1750 for up to 16 terminals, and $2450 for up to 30 terminals. The 62-terminal capability price of $2750 remains unchanged.

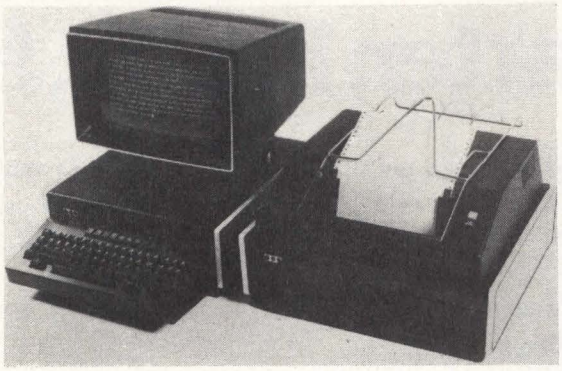
Tymnet, Inc, 10261 Bubb Rd, Cupertino, CA 95014 has included an option in the tariff for users of the 110- to 300-baud service, which was offered at increments of up to 8, 30, and 62 terminals. The added increment supports up to 16 terminals at a monthly price of $1500.

An economic backup line to the network is also available to users of synchronous host interfaces. This optional service is $250 more than the cost of single access line service, plus the company's actual cost of providing the backup line obtained from other carriers.

2-Buffer Display Station Accommodates Interactive Communications Systems

Extending the synchronous Dataspeed® 40/4 data communications terminal series, the single display station is particularly suited to remote or branch office locations requiring a single keyboard display and printer. American Telephone and Telegraph Co, 195 Broadway, New York, NY 10007 has designed the arrangement for low cost use in highly interactive communications private line systems using binary-synchronous protocol in a wide range of industries.

With an integrated controller, the display includes two 1920-char buffers —one for display and the other to accommodate an optional printer. This allows a message to be prepared on the display while a second message is received on the printer. Printer performs local printing under operator control, as well as remotely from a computer.



For implementation with private line systems using binary-synchronous protocol, AT&T's Dataspeed 40/4 single display station features keyboard display with two buffers—one for display and one for optional printer that performs local as well as remote printing

Tariffs for the station are expected to be filed in some states during the first quarter of 1978. Service availability will depend upon effectiveness of the tariffs.

Circle 404 on Inquiry Card

Data Services With Speeds Above 150 Bits/s Offer Low Speed Prices

A spectrum of data transmission services to replace the series 1000 services, which range up to 150 bits/s, are the Private Wire 75, 150, and 300, available to 360 direct-access cities, and the 600/1200, available in 127 of those same cities. The 2-way service of Western Union Telegraph Co, Upper Saddle River, NJ 07458 and price structure are based on the subdivision of an ordinary voice-grade circuit into several data channels; average cost for current customers is expected to decrease slightly.

The tariff filed with the FCC also established a separate rate schedule for 1-way transmission channels up to 300 bits/s, available through 112 cities combined into six regional networks. Subject to FCC approval, the schedules are effective Jan 12.

Continuing Development Is Foreseen In Data Communications Industry

Vast communications networks are in the process of developing in the U.S. and internationally, according to Charles P. Johnson, president of General DataComm Industries, Inc, 131 Danbury Rd, Wilton, CT 06897, which specializes in manufacturing data transmission equipment for the common carrier, end-user, and international markets. Addressing the Boston Stockbrokers Club, he observed that growth factors have occurred in the data communications industry, which includes a wide spectrum of companies such as those offering computers, minicomputers, terminals, and communications, as well as IBM and AT&T.

Market forecasts continue to show a steady rise in the number of telephone installations. By 1987, one in every 15 business telephones will have a data termination representing an annualized growth rate of about 24%. At the same time, the number of telephones used for business purposes will have doubled. Data transmission equipment will be required to make each data termination effective.

Industry surveys also show continued growth patterns for modems, increasing 250% from 1976 to 1981; a similar trend is seen for multiplexers. Data communications, as one of the fastest developing major industries of the nation, should continue to grow at an annual rate of 25%.

Manufacturers must be alert to changes in the marketplace—changes in legislation affecting standards, and in data transmission methods, as well as those dictated by users. Government agencies, here and overseas, will establish rigid operating standards for data communications equipment during the next few years, which manufacturers will be required to meet. During the 1980s, factors such as proven performance, size of the customer base, service capability, and manufacturing will become more important than individual product innovation.

Introducing Micro-2 from Digital Systems

You might find or put together another computer system with the same capability as Digital Systems' new Micro-2. But it would probably cost you a lot more than $5,000. At $4,995 the Micro-2 is a completely assembled, compact, high-performance microcomputer system with Shugart dual-drive, double density floppy disks. Its single computer board includes a Z-80 CPU, 32K of RAM, four RS-232 serial interfaces, 16 bits of parallel I/O, and a real-time clock. And on the same board you have the option of 64K of RAM.

The single disk controller board uses either the standard IBM 3740 format or a double density format of 571K bytes per diskette. Optional double-sided drives increase storage to 2.3 Megabytes. And since the controller can support another two drives, the storage capacity of the Micro-2 can be increased even more.

The simple bus and two-board design of the Micro-2 means greater inherent system reliability. A short cable interconnects the computer and controller boards, providing a high-speed DMA interface. On the computer board there's access to the internal bus connector and a wire-wrap area for custom logic.

With the Micro-2, you get the comprehensive CP/M disk operating system, disk BASIC, and complete hardware diagnostics. (For the past three years CP/M has been field-proven in other Digital Systems' hardware.) What's more, extensive accounting software packages and high-level languages, such as CBASIC and FORTRAN, are available.

So if you're interested in a low-cost, high performance microcomputer system, you can begin and end with the Micro-2. Write or call us today about the new Micro-2 or our other disk-based systems. OEM and dealer discounts are available.

Digital Systems, 6017 Margarido Drive, Oakland, California 94618; (415) 428-0950.

The Computer System That Begins Where Others End.

We'd like to show you around the MSC 8001 Z80/MULTIBUS Single Board Computer

Take the MULTIBUS.™ The MSC 8001 is fully hardware and software compatible with the industry standard SBC 80™ MULTIBUS. Use with any of the wide variety of SBC 80 compatible components to shorten product development cycles. No need to spend extra time and money on basic software development, either. The 8080's software will work just fine.

See the Z80™ perform. Our star attraction is the Z80 CPU, with its expanded instruction set and high speed program execution. The built in eight levels of priority interrupt are at your disposal and more! The Z80 has a non-maskable interrupt you can use to implement power-fail recognition or to assist in debugging.

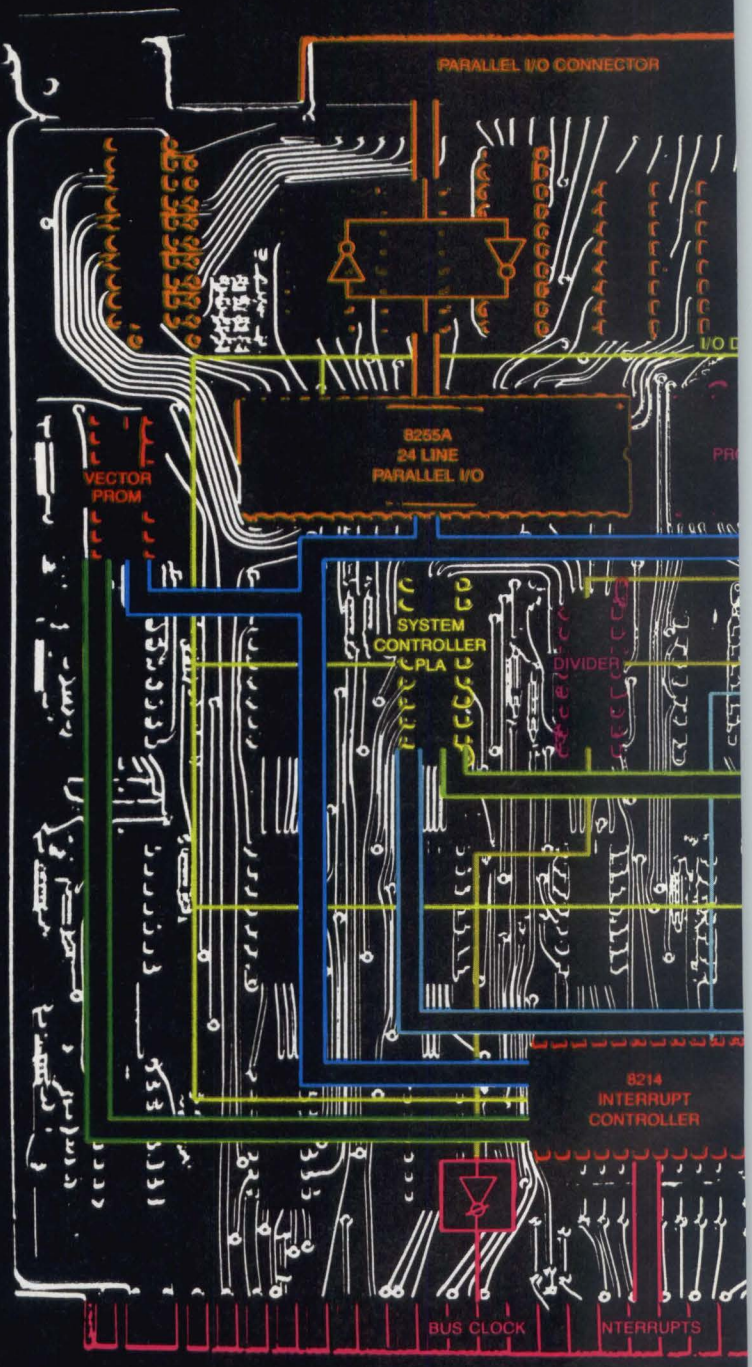
Remembering the way. Our memory gives you up to 8K RAM and up to 16K ROM on board! The need for costly additional memory has now been eliminated in many applications.

Mix and match. You can install identical or completely different 8 bit EPROMs, ROMs or PROMs. Now store commonly used subroutines in ROMs in one or two sockets, and your own applications programs in EPROMs in the others. Using 4K elements you can have up to 16K bytes.

Got a transfer? During Direct Memory Access transfers, the MULTIBUS can access all of our on-board memory. Use the RAM for intermediate storage for a high speed video display or floppy disk controller.

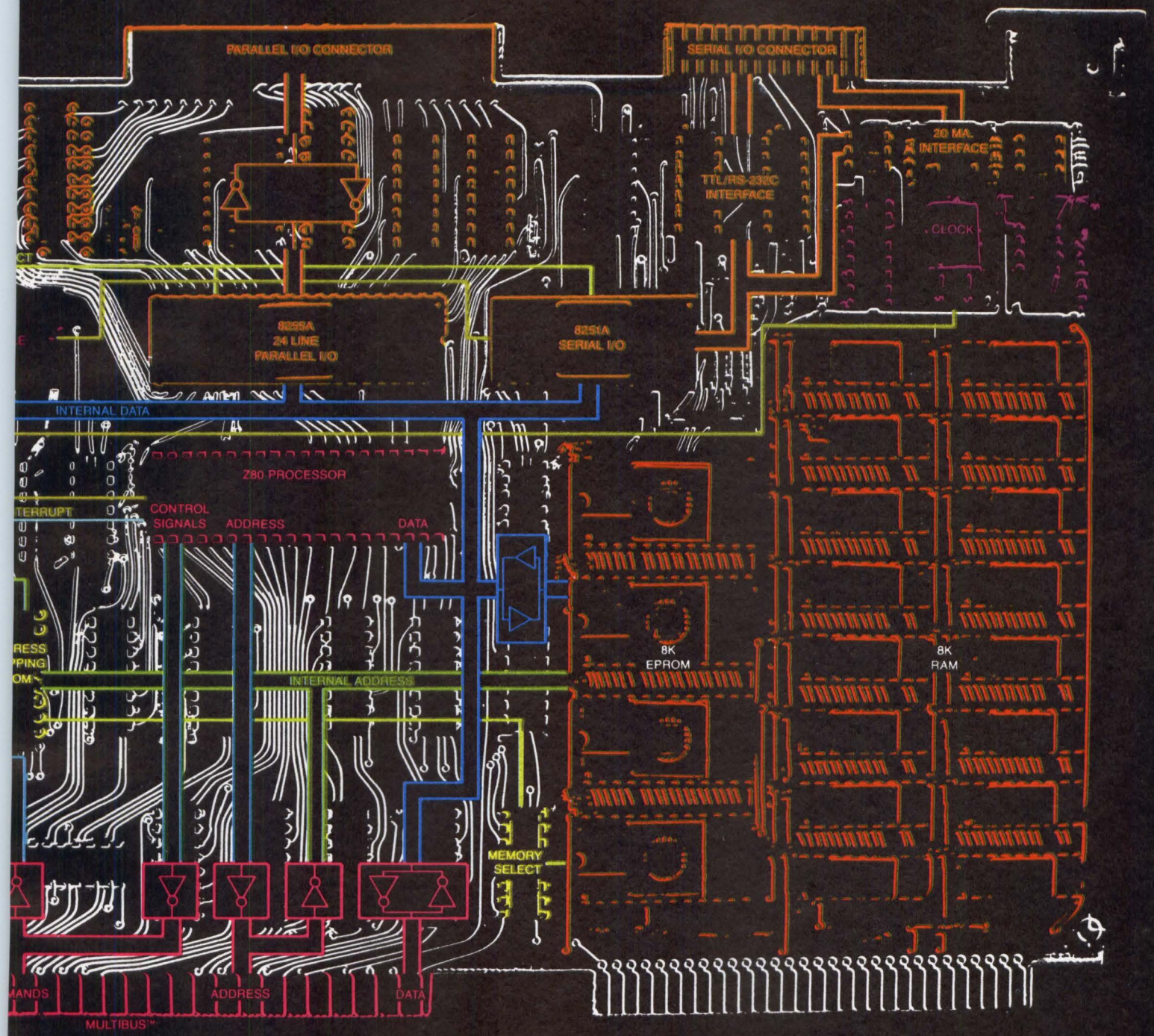
Along the serial way. Programmable serial I/O interfacing for asynchronous and synchronous terminal devices is provided by the MSC 8001. Whether you require TTL, or optically isolated 20mA current loop, it's all on the board. With us you won't need any external converters to handle your Teletype.®

Parallel ins and outs. Two programmable ports offer 48 lines of parallel I/O. Inverted and upright signals can be generated and sensed. All of our I/O lines are buffered inbound and outbound for safety and reliability.



Powering up. The MSC 8001 will operate on a single +5 VDC power source in most system applications.

Going further. Our complete 16 page, full color tour guide to the MSC 8001 Single Board Computer is available by contacting Monolithic Systems Corp., 14 Inverness Drive East, Englewood, CO 80110. 303/770-7400. Telex: 45-4498



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A Half Million Word Computer

THE ROLM 1666. Memory expansion to 576K words. Transparent mapping into 64K blocks for six users. Four-way memory protection. Privileged instructions with I/O allocation & protection.

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CIRCLE 14 ON INQUIRY CARD

COMMUNICATION CHANNEL

Switch Adds Digital Time-Division Approach To Tandem Networks

High performance data and voice circuit switching are provided by the digital tandem switch (DTS) using stored program common control and solid-state digital time-division techniques developed by Rockwell International Corp's Collins Commercial Telecommunications Group, Dallas, TX 75207 for its automatic call distribution systems. The switching system is compatible with digital switching and transmission systems as well as analog circuits and switches. Analog voice signals from subscriber lines are changed by commercially available PCM channel bank equipment to digital form; for network transmission media employing digital carrier equipment such as T-1, the trunk connects directly to the switch.

Communications trunks can be dynamically reassigned by the system supervisor to meet traffic load variations or special situations. As a management information system, the unit computes and displays operating information for the system supervisor. Data are collected in reporting groups related to trunk assignments.

Dual control computers protect against system outage through equipment failure; backup power sources with automatic switchover are available for operation independent of commercial power. Modular systems can be expanded with additional units, without disrupting existing facilities.

Circle 405 on Inquiry Card

Locations For Ground Communication Satellite Facilities Are Selected

An application has been filed with the FCC by Communications Satellite Corp (COMSAT), 950 L'Enfant Plaza, SW, Washington, DC 20024, as manager for the joint owners of the Etam, West Virginia earth station, to construct new earth station facilities at Etam and Lenox, W Va for commercial satellite communications. The $13.4M investment by American Telephone and Telegraph Co, ITT World Communications, Inc, RCA Global Communications, Inc, Western Union International, Inc, and COMSAT will consist of a dish-shaped antenna, approximately 56 ft (17 m) in diameter at both sites, related electronic equipment, and a 2-hop microwave diversity interconnection link to connect the two sites.

The equipment should be completed and ready to operate in early 1980, to work with the 12,200-circuit Intelsat V communications satellite to be launched in late 1979. The Intelsat V operates at higher frequencies of 14 and 11 GHz, which are subject to interference during periods of heavy rain. To minimize this, a diversity site will be constructed at Lenox, approximately 22 miles from the primary site at Etam. □

Handheld Electronic Voice Systems Turn Keyboard Input to Speech

Called the Phonic Mirror® Handi-Voice™, a handheld battery-operated electronic voice system can simulate the human voice, produce complete sentences, and articulate virtually every word in the English language. Based on a speech synthesizer, which electronically simulates the human voice, the units allow vocally impaired individuals to communicate verbally.

The electronic voice synthesizer, developed by Votrax®, div of Federal Screw Works, Troy, MI 48084, converts the output of a digital device into electronically synthesized human speech. This conversion is accomplished through a patented electronic design that uses phonemes (basic sound elements) as building blocks to produce words and phrases. The system produces the phonemes and integrates them with inflection to produce smooth intelligible speech.

In the model HC 110, which consists of a direct selection display board, containing the phoneme-based speech synthesizer, rechargeable battery, and speaker, there is a preprogrammed vocabulary of 393 words, 16 phrases, 45 phonemes, 26 letters, and 13 morphemes (word suffixes/prefixes). The touch-sensitive display board has 128 stations that may be represented as words, pictures or symbols, or controls. Each vocabulary selection occupies a position on the keypad. Four color-coded changeable overlays distinguish between four different vocabulary levels.

Individual sensors under the board respond to touch, allowing words or phrases to be entered. As they are entered these words or phrases are held in memory, allowing a message containing up to 40 selections to be formulated. This message is held until the "talk" station is touched, causing the message to be spoken.

Words that have not been prestored in the vocabulary can be constructed by selecting the letters needed to spell the word, through combining words existing in the vocabulary to form a new word, or by combining existing words with prefixes, suffixes, or isolated sounds to create a new word. Another technique is to create words phonetically by determining the speech sounds (phonemes) required to pronounce the word, and entering sound selections through the display board.

The model 120, which looks and operates like a calculator, is preprogrammed with 893 words, 45 phonemes, 26 letters, 13 morphemes, and 16 short phrases. Selections are made using a 3-digit numeric code. A liquid crystal display window located above the numeric keyboard visually displays the vocabulary codes.

Handheld electronic device capable of producing audible human speech from keyboard inputs is based on speech synthesizer and related computer interfacing devices, developed by Votrax, that enable it to simulate human voice and articulate most English language words

Words not in the vocabulary can be formed using the same techniques described for use with the model 110.

Developed and manufactured by Votrax div of Federal Screw Works, the devices are available through HC Electronics Inc, a subsidiary of American Hospital Supply Corp, 250 Camino Alto, Mill Valley, CA 94941.
Circle 140 on Inquiry Card

Minifloppy Disc Drive Records Double-Density on Double-Sided Media

The SA450 double-sided, double-density, double-headed minifloppy drive can read and write on both sides of a diskette without removing it from the drive. Using double-density (MFM/M²FM) recording, the unit can store 440k bytes of data (unformatted)—up to four times the capacity of the SA400 minifloppy—in the same size package.

Introduced by Shugart Associates, 415 Oakmead Pkwy, Sunnyvale, CA 94086, the SA450 consists of read/write and control electronics, drive mechanism, read/write head, and precision track-positioning mechanism. The proprietary read/write heads are single element glass-bonded ferrite ceramic devices with straddle erase elements to provide erased areas between data tracks. This prevents normal interchange tolerances between media and drives from degrading the signal-to-noise ratio and provides diskette interchangeability.

The two read/write heads are mounted in a stainless steel flexure that loads onto the minidiskette media when in operation. Read/write assembly is accurately positioned through use of a precision spiral cam. This cam has a V-groove with a ball bearing follower that is attached to the head carriage assembly. Driven by a stepping motor, the cam rotates in precise increments to the assigned track location on the minidiskette.

The unit is designed for low heat dissipation, and offers positive media insertion to prevent damage from the door closing on the diskette. Its

DO YOU QUALIFY?

OUR PRODUCT WAS DESIGNED FOR THE VANGUARD OF THE COMPUTER INDUSTRY. SOPHISTICATED USERS RECOGNIZE THE VERSATILITY OF OUR MACHINE AND HAVE BEATEN A PATH TO OUR DOOR.

We've installed our revolutionary computer system, the QM-1, in Fortune 500 aerospace corporations, universities, the military, major system houses and in a giant computer manufacturer.

QM-1: THE MOST VERSATILE YET!

They purchased our system because:

- The QM-1 was specifically designed to enable you to emulate any computer or, for that matter, any peripheral or digital device.
- When an emulator is running, the QM-1 architecture is transparent to the user. Software developed on the QM-1 will run on the machine which has been emulated. The opposite is also true; application and system software from the "real" machine will run unchanged on the QM-1.
- QM-1 customers have emulated commercial, militarized, avionic and special purpose computers. They range from micros to fourth generation Large Scale General Purpose Systems.
- Users are not limited to one system identity; they can emulate as many kinds of computers as they like, even run multiple emulations of different systems concurrently.
- The QM-1 allows you to control and monitor the emulated system, even primitives like gates, data busses and registers. You can use it to design new computers.

Here's what QM-1 users have found to be true:

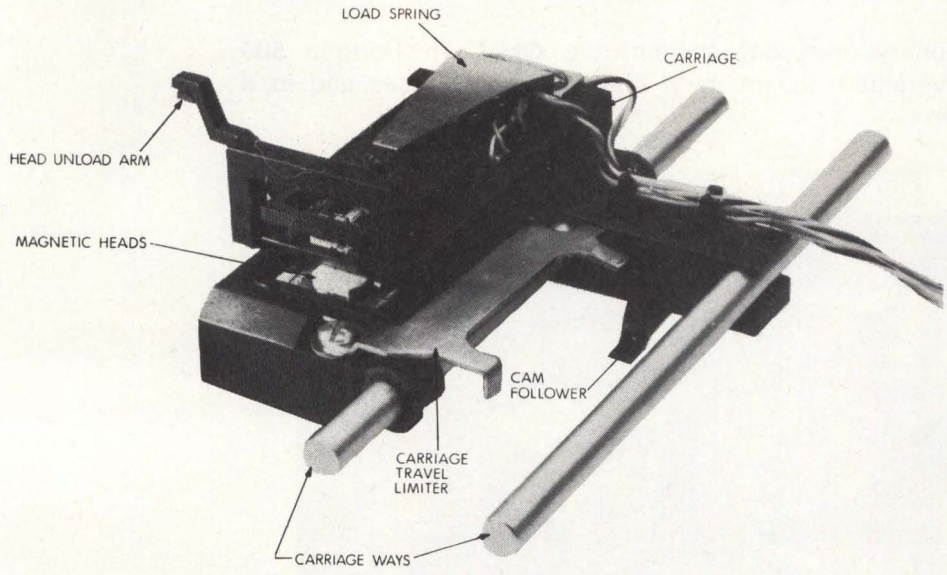
- Emulators on the QM-1 are running one hundred times faster than simulators on more expensive systems.
- The QM-1 is an easily modified, reusable breadboard to verify and validate device design.
- The QM-1 is without equal as a software development tool for any computer. It will also protect investments in software running on destandardized machines.
- The QM-1 is an excellent design tool for analyzing software structure, system composition and hardware/software trade offs.
- The QM-1 is ideal in a computer science environment for instruction and research into hardware and software architecture.

Prices range from $190K for a minimum system configuration, capable of running Nanodata supplied software, to upwards of $700K for a multiprocessor. A "typical" customer configuration sells for $280K and includes emulators of the PDP 11, Data General NOVA, IBM 360, etc.

Do you qualify as a prospective user? If you do, then write for additional information or, better still, call Michael Senft, Director of Marketing.

NANODATA CORPORATION

2457 Wehrle Drive • Williamsville, N.Y. 14221 • (716) 631-5880



Capable of double-density recording on both sides of minidiskette, Shugart's SA450 minifloppy drive uses two read/write heads. Heads are mounted on carriage which moves on precision carriage ways. Diskette is held perpendicular to heads by platen on base casting. Both heads are loaded against diskette by load solenoid

measurements are 3.25 x 5.75 x 8.0" (8.26 x 14.61 x 20.3 cm). Specifications for single-density recording include capacity for 109.4k bytes/surface unformatted, average latency of 100 ms, average access time of 298 ms, and transfer rate of 125k bits/s. Using double-density capability, the unit records 218.8k bytes/surface unformatted and transfers data at 250k bits/s.

Double-sided 5.25" (13.34-cm) minidiskette media for the drive are available in SA154 (soft-sectored), SA155 (hard-sectored, 16 hole), or SA157 (hard-sectored, 10 hole). Packaged in boxes of 10, diskettes will cost approximately $65/box. The drive is priced at $450 (1-24) or $290 in 250-499 quantities.

Circle 141 on Inquiry Card

Cluster Terminal System Allows Local Terminals Access to Data Base

A cluster terminal computer system, the 6500 offers up to 1.5M bytes of storage, IBM 3780 compatibility, and FORTRAN programming. Providing storage and immediate access to local data bases in either standalone or distributed processing environments, the system allows up to eight terminals to share access to a processor, communications port, and storage, minimizing the need for computer time where immediate access to the data base is necessary.

System components include a processor with up to 64k bytes of programmable memory, IBM 3780 compatible bisynchronous communications interface, printer, and floppy disc interface. The system's peripheral interface processor permits interconnection of up to 12 RS-232-compatible devices at communications speeds to 9600 baud. These devices may include a maximum of eight 4000 series video display terminals, two printers, floppy disc, and host processor port. The floppy disc unit accommodates up to six drives, each with 242,900-char capacity. For remote batch processing, the system communications interface operates by performing an IBM 3780 remote batch emulation or using a teleprinter protocol. The asynchronous communications interface is compatible with most minicomputers and mainframes.

Available for the system, from Delta Data Systems Corp, Woodhaven Industrial Pk, Cornwells Heights, PA 19020, is a 3-level software package, which includes operating system, file management system, and program development system. The operating system controls operation and interaction of all system components in complex multistation applications. Through it, system hardware may be operated concurrent with batch or online processing. File management system provides the operator or application program with ability to create, retrieve, and edit information on diskette files. The program development system provides utility and language processors for modifying the system to handle information retrieval requirements or special applications.

Circle 142 on Inquiry Card

Microcomputer-Based Color Graphics System Displays Arabic/Farsi

An Arabic/Farsi color graphics system, the A8051/F8051 is programmable in either assembly or BASIC language with all I/O in Arabic. Developed by Intelligent Systems Corp, 5965 Peachtree Corners E, Norcross,

We've combined refresh with storage in a new modular graphics display.

You build from there.

Suddenly state-of-the-art display technology comes built for the OEM.
Tektronix' new GMA display modules let you integrate into your system our most impressive display capabilities ever. Including refresh and storage graphics in one tube. Complete character and vector generators. Big 19" screen and fine resolution.

It's exactly what you need, because you can specify exactly what you want. Order CRT and power supply only, or select from a range of performance and packaging options in our extensive product line.

You can integrate other products from our graphics family, like hard copy modules. Or talk to us about other special product configurations, like our 11" storage-only components.

No other package lets you pick such comprehensive graphic display capability at anywhere near the price.
It figures, because Tektronix has been the worldwide low-cost graphics leader for years. No matter what unique and unusual systems you're working with, we can help with manufacturing flexibility, engineeering assistance, and a passion for excellence.

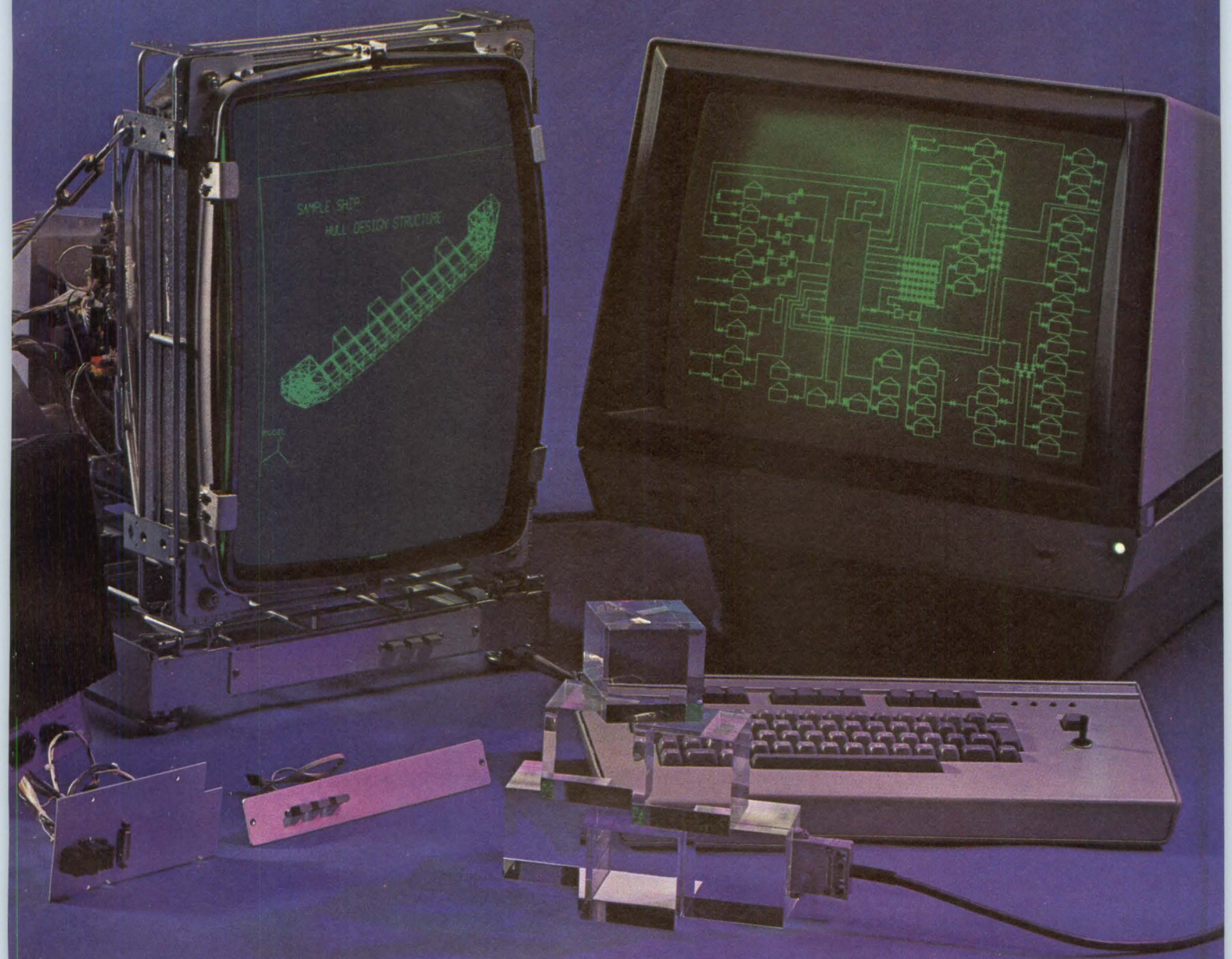
Get capability you can build with. From a supplier you can work with. Get your Tektronix OEM Sales Engineer on the phone today. Or write us for more information.

Tektronix, Inc.
Information Display Group
OEM Components
P.O. Box 500
Beaverton, OR 97077

CIRCLE 19 ON INQUIRY CARD

Tektronix OEM components: the perfect fit.

Tektronix®
COMMITTED TO EXCELLENCE



"Ship hull display courtesy of University of Arizona"

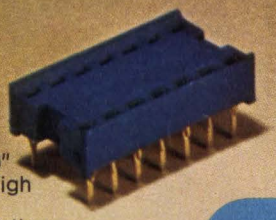
Whatever you need in an IC socket...

RN has 'em all!

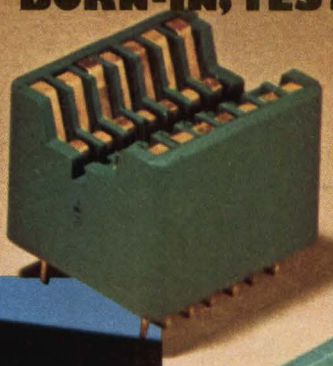
—and with "side wipe" reliability

PRODUCTION SOCKETS

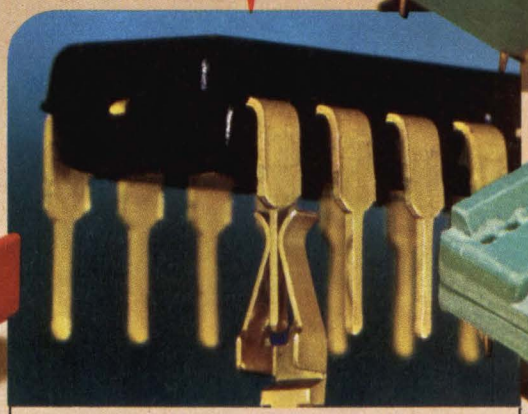
BURN-IN, TEST SOCKETS



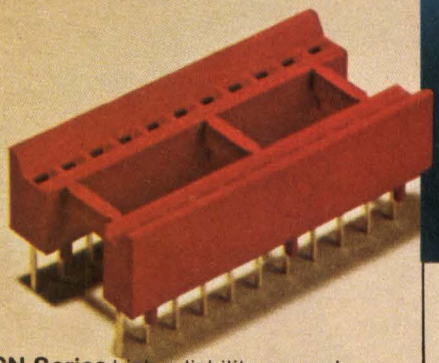
NEW! ICL Series
26% lower profile—.150" Ideal for high density, high volume configurations, provides maximum vibration resistance. Solder type, single leaf "side-wipe" contacts. 8 to 40 contacts.



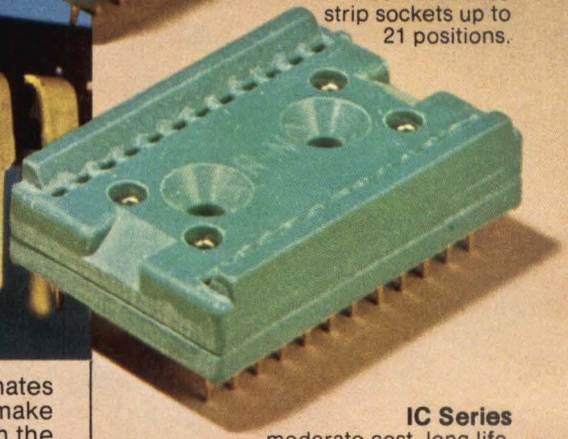
TS Series
very long contact life. Very low insertion force. Ideal for incoming inspection. With 14 to 40 contacts. Also strip sockets up to 21 positions.



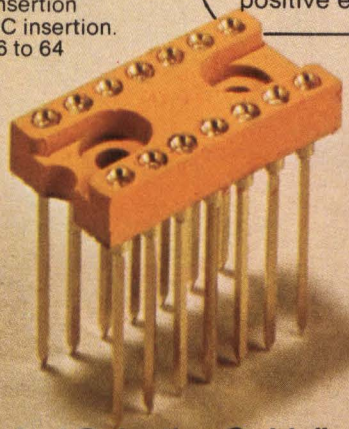
RN HIGH RELIABILITY eliminates trouble. "Side-wipe" contacts make 100% greater surface contact with the wide, flat sides of your IC leads for positive electrical connection.



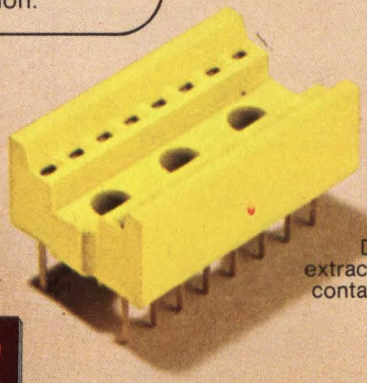
ICN Series high reliability general-purpose sockets. Low insertion force allows automatic IC insertion. In solder or wire-wrap. 6 to 64 contacts. Dual leaf "side-wipe" contacts.



IC Series
moderate cost, long life. Designed for general test and burn-in up to 350°C. With 14 to 40 contacts.



ICA Series
high reliability pin socket contacts. Low profile in solder or wire-wrap. 8 to 40 contacts.



ICN/S2 Series
lowest cost burn-in socket available. Designed to accept IC extraction tool. With 8 to 40 contacts, with strip sockets up to 25 positions.

WRITE TODAY for New RN "Product Selection Guide"...

.... and informative book "What to Look for in IC Interconnects." Free from RN—the people who make more kinds of high reliability sockets than anyone.

RN® ROBINSON NUGENT, INC.

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CIRCLE 20 ON INQUIRY CARD

Intelligent Systems' microcomputer-based, 8051 intelligent terminal is capable of displaying Arabic/Farsi and English language characters in eight colors. Graphics capability is available as option

GA 30071, the system incorporates a 19" (48-cm) dual language intelligent terminal with Arabic/Farsi keyboard operating system, provides selectable baud rates from 110 to 9600, and includes complete graphic hardware and software for drawing vectors, bar graphs and lines, and for point plotting.

Highly legible Farsi characters are generated using a method of splitting characters. This allows both proportional and variable length letters, and simplifies the task of the keyboard operating system in recognizing the type and modifying it accordingly. Character splits are transparent to user, but can be accessed individually.

The terminal automatically accounts for the shape of characters entered in Arabic or Farsi. In English mode, lower case keys are Farsi or Arabic, and whenever they are entered, the characters are right shifted so that they are read from right to left. In Farsi/Arabic mode, the cursor moves from right to left, but numbers and English characters are entered in insert mode so that they are read from left to right. The cursor is automatically moved to the left of the line.

Insert/delete, page roll-up, cursor addressing, two sizes of characters, and background and foreground color selection in eight colors are provided. A graphics option allows up to 30,720 points to be addressed in a 160 x 192 grid. XY point plot, horizontal bar graphs, vertical bar graphs, vector plotting, and character plotting utility programs are available with this option. All routines can be called through keyboard or programs. The called routine will automatically request appropriate coordinates continuously until the exit code is supplied. Multicolor graphics are achieved by user specification of background and foreground colors.

Transmission is line by line, allowing editing and alteration before data are sent to a computer. A character transmission look-up table allows the type of binary code (ie, ASCII, EBCDIC) to be transmitted to be specified.

Standard memory consists of 4k of refresh RAM on 25-line units; 8k is standard on 48-line units. 24k bytes of RAM can be added in 8k increments. One card can contain 24k of ROM/EPROM. Utility programs are in 8080 assembly language. An 8080 assembler, p/ROM programmer, and peripherals are available for program development.

Circle 143 on Inquiry Card

1370 Family Processors Improve Performance Without Adding Capacity

Two additions to the System/370 computer family, 3031 and 3032 processors allow intermediate and large system users to improve their level of performance without having to jump to the top-of-the line processor. Announced by International Business Machines Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604, the 3031 processor has internal operating speeds 2 to 2.5 times those of a System/370 model 148 processor, while the 3032 operates at 2.5 to 3 times the rate of a model 158-3.

Basic machine cycle time for the 3031 is 115 ns. The processor has from 3M to 6M bytes of main storage, available in 1M-byte increments. Processor storage is 4-way interleaved, enabling the unit to handle significantly faster data rates. 32,768 bytes of high speed buffer store make data available to the processor rapidly. Internal organization of the processor allows several instructions to be prefetched while one is being executed.

The 3032 processor has a basic cycle time of 80 ns and is organized to provide separate instruction preprocessing and execution functions which contribute to improved performance by allowing one or more instructions to be prepared while another is being executed. Main memory is available with 2M-, 4M-, or 6M-byte capacity, with a 32k-byte buffer store.

One group of six physically integrated, but functionally independent channels provides for transfer of data; 12 channels are available on the 3032. Each group consists of one byte-multiplexer channel, which operates in the 40k- to 75k-byte/s range, and five block-multiplexer channels, which are capable of data

transfer rates up to 1.5M bytes/s. An optional channel-to-channel adapter allows data communication between channels on different processors, establishing a loosely coupled multiprocessor system.

Both processor complexes include a 3036 console containing two console processors, which improve system availability and serviceability. Each console features dedicated display, keyboard, diskette drive, and I/O channel connection.

Support for both units is provided by MVS, OS/VS 1, single virtual storage, and virtual machine facility. Customer shipments are scheduled to begin in first quarter 1978. Lease price for a 3031 with 2M-byte memory will be $25,000/mo; the 3032 with 2M-byte memory leases for $43,740/mo.
Circle 144 on Inquiry Card

Desktop Computers Configured for Various Applications

Series 625 computers incorporate 65k bytes of addressable semiconductor memory, 630k bytes of diskette storage, CRT display, 40-column alphanumeric printer, full ASCII keyboard, and provision for interfaces in a single enclosure small enough to be used on a desktop. Manufactured by Compucorp, 1901 S Bundy Dr, Los Angeles, CA 90025, and claimed to be the most cost-effective units available, the series includes the 625 computer, 625A data acquisition system, 625B business computer system, and 625C intelligent terminal.

Desk-top computer from Compucorp has 65k bytes of addressable memory, 630k bytes of disc memory, 40-column alphanumeric journal printer, and full ASCII keyboard with user-definable function keys

Data acquisition system includes all features of the computer plus special modules and interfaces for A-D and D-A conversion, multi-unit parallel and serial instrument control, external high speed printer, and XY plotter operation. The business system is configured with a combination of hardware, systems software, and applications software to meet general business application needs. Applications software is designed for modular enhancement to incorporate order entry, inventory, and management information functions. For distributed processing applications, the intelligent terminal combines bulk storage, CRT display, auxiliary journal printer, and full ASCII keyboard with the ability to communicate with host computer and other terminals.

All machines are furnished with the company's extended BASIC compiler, file management system, assembler, and text editor. Programs written in BASIC work with little or no modification.
Circle 145 on Inquiry Card

Business Computer Family Protects Software and Offers Upgradeability

Royale™ interactive computer systems feature firmware, architecture, and memory options that combine to provide economical planned systems growth. Microdata Corp, 17481 Red Hill Ave, Irvine, CA 92714 is offering the transaction-oriented, data-base management system in configurations with from 16k to 128k of memory and from 10M to 600M bytes of disc storage. Virtual memory and direct access file structure avoid problems of file or program size.

Among the system features are an architecture using an I/O processor, main core memory expansion to 128k, a task priority scheduler, firmware diagnostics, cassette tape drive, and disc drive. Software includes a DATA/BASIC™ debugger, a firmware implementation of DATA/BASIC for increased speed, and enhanced procedural language capabilities to allow interactive control of complex job sequences.

Identified as series A, B, C, and D, the family members handle from one to 32 I/O devices. Series A consists of various configurations supporting simultaneous operation of from one to six CRT or keyboard entry devices with from 16k to 64k bytes of central core memory. A typical system could include cartridge disc drive and matrix printer.

For applications requiring six to ten simultaneous operations, series B is recommended. Series C handles the need for 10 to 20 simultaneous applications and series D controls simultaneous performance of up to 32 tasks.
Circle 146 on Inquiry Card

Graphics Processor Enhances Performance of Automated Design System

A comprehensive graphics processing computer designed to enhance the performance of automated design and manufacturing systems, CGP-100™ (Computervision Graphics Processor) increases speed and productivity up to 500% and supports twice as many user terminals. Intended only as a component for the Designer series of interactive graphics systems from Computervision Corp, 201 Burlington Rd, Bedford, MA 01730, the processor is designed with a microprogrammed architecture for efficient implementation of instructions and is field expandable to 512k words of 16-bit memory.

Claimed to be the first central processing unit developed exclusively for use in computer-aided design, the microprogrammed processor provides 30% faster cycle time and allows enhancement of the instruction set at minimum cost to prevent system obsolesence. Built-in diagnostics with program microstep assure data integrity and machine reliability, and offer easy access for servicing. An optional high accuracy hardware floating-point multiply/divide capability dramatically increases speed on the compute-bound tasks associated with graphics applications. Pushbutton automatic program load capability automatically initiates diagnostic procedures to ensure data integrity each time the system is brought up.

One 15 x 15" (37.5 x 37.5-cm) PC board houses 32k words of memory; expansion to 512k words by addition of memory boards allows the system to accommodate eight or more

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users. A memory management unit provides 1M bytes of main memory capacity.

Configurations incorporating the processor can include multiple interactive CRT terminals, cassette tape units, 7- or 9-track magnetic tape units, disc drives, and a variety of digitizing and plotting devices.

Circle 147 on Inquiry Card

Business Computers Offer Multiterminal COBOL At Minicomputer Prices

The 440 Data Series, a family of multiuser COBOL business information systems, combines the high performance 128k-byte GA-16/440 minicomputer with large data base handling technology and interactive multiterminal COBOL capability. Claimed by General Automation, Inc, 1055 S East St, Anaheim, CA 92803 to provide the best price/performance package available, the series is intended for use in data/distributive processing applications in online and batch modes.

Powerful ANSI COBOL software compiles at up to 10 times the speed of an IBM 370/145 and requires minimal conversion efforts to run existing COBOL programs. In addition, compilations can be made from any number of the system's 16 terminals while other operations proceed simultaneously. Tests made on various configurations of hardware and software to determine the system's performance in real operating environments indicate that a 16-terminal system with 160M-bytes of disc storage will respond to data entry operations in less than 1 s, while performing online COBOL compilations at two terminals.

System efficiency is derived from concurrent batch and online processing capabilities. Full terminal oriented COBOL and full ISAM/PSAM file management increase programming, processing, and file storage flexibility. In addition, full password and privileged user provisions ensure total system security and integrity.

Configurations, in rack-mounted or office packages, are available with optional peripherals and software, which includes CONTROL III foreground/background real-time operating system, multiterminal timesharing system, COBOL compiler, and file management system. Peripherals include up to two 10M- or 80M-byte disc drives, 200- or 600-line/min printers, 400- or 1000-card/min readers, up to 16 video display terminals, and 25- or 75-in/s magnetic tape systems.

Circle 148 on Inquiry Card

Business Computer System Uses Microcomputer to Cut Hardware Costs

ADVENT 1000, a microcomputer-based system, offers the same performance and capability of a minicomputer-based system at significantly less cost because of savings in basic hardware costs. Priced under $10,000, the system, designed by Applied Data Communications, 1509 E McFadden Ave, Santa Ana, CA 92705, features a fully implemented microcomputer on one board, IBM-compatible floppy disc, and CRT; and supports 64k RAM, floppy and cartridge disc drives, and printers. Asynchronous communications can occur at 9600 baud; synchronous at 19,200 bits/s.

MICRODOS/BASIC operating software combines the power of ANSI COBOL file processing with the flexibility of a multi-user operating system and the simplicity of the BASIC language. The system includes a comprehensive file and data base management system, and interactive multi-user operating system.

Powerful string handling capability, string match, and variable length strings and string arrays are among the system's features. There are sequential, relative, and indexed-sequential files, as well as a COBOL-style format and edit control. Decimal accuracy is 9 or 15 digits. Also provided are binary integer capability, complete system commands and procedures, and expanded relational and logical capabilities. Efficiency is enhanced through queried I/O, multi-user file protection, and an external subroutine capability. □

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Intecolor 8031
Unretouched photo of screen.

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Take a look at the Intecolor 8031. A compact 13-inch 8-color CRT, it comes complete with graphics hardware and software, a built-in mini disk drive for extra storage, plus "File Handling BASIC" which lets you create, delete, and retrieve program segments from storage, by name.

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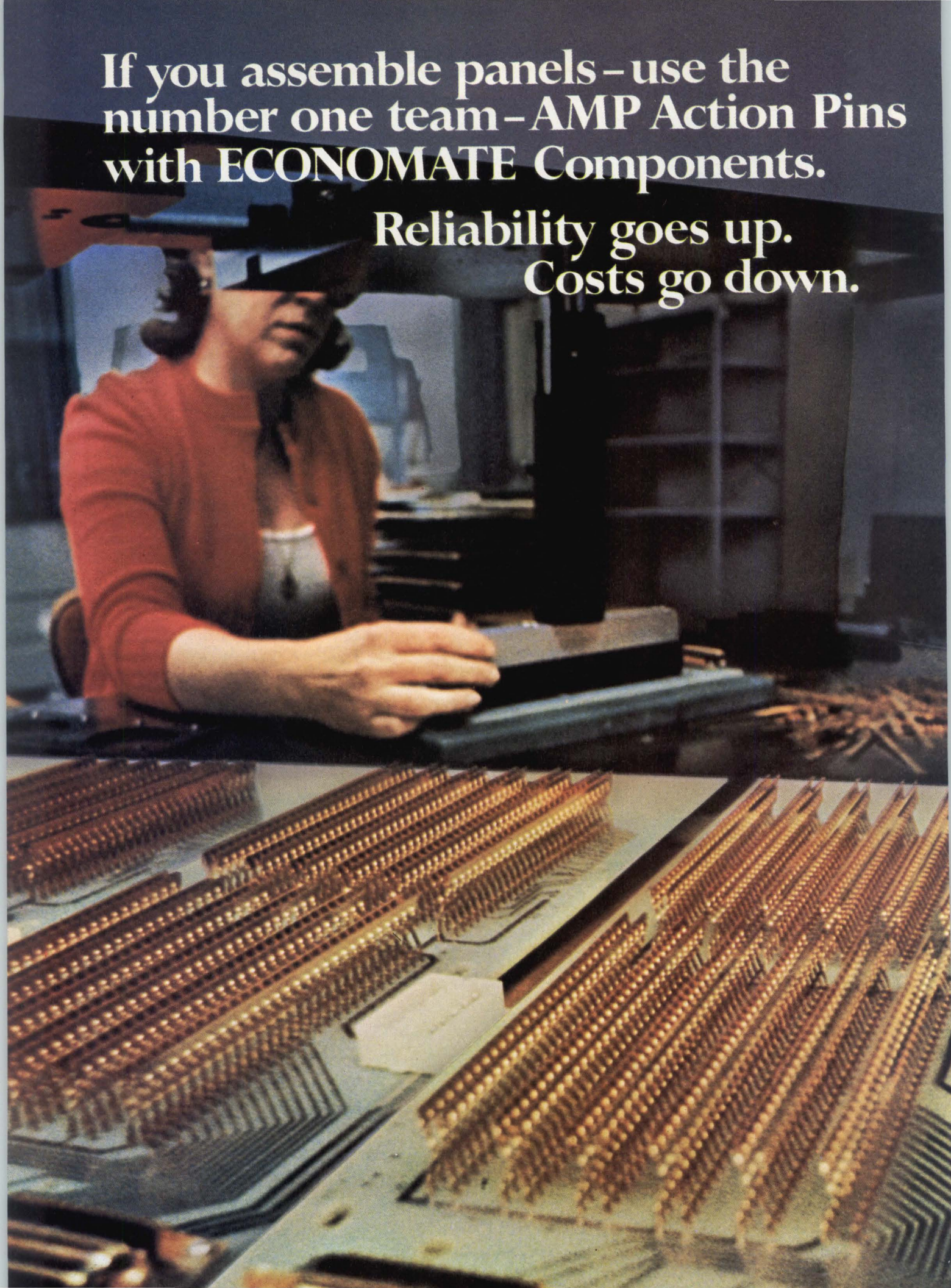
Intecolor 8051
Unretouched photo of screen.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Reliability goes up.
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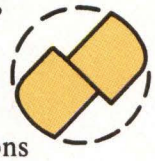
Because the AMP Action Pin has a spring-section concept which eliminates broaching, rupturing, distortion, tearing, and damage to plated-thru walls.



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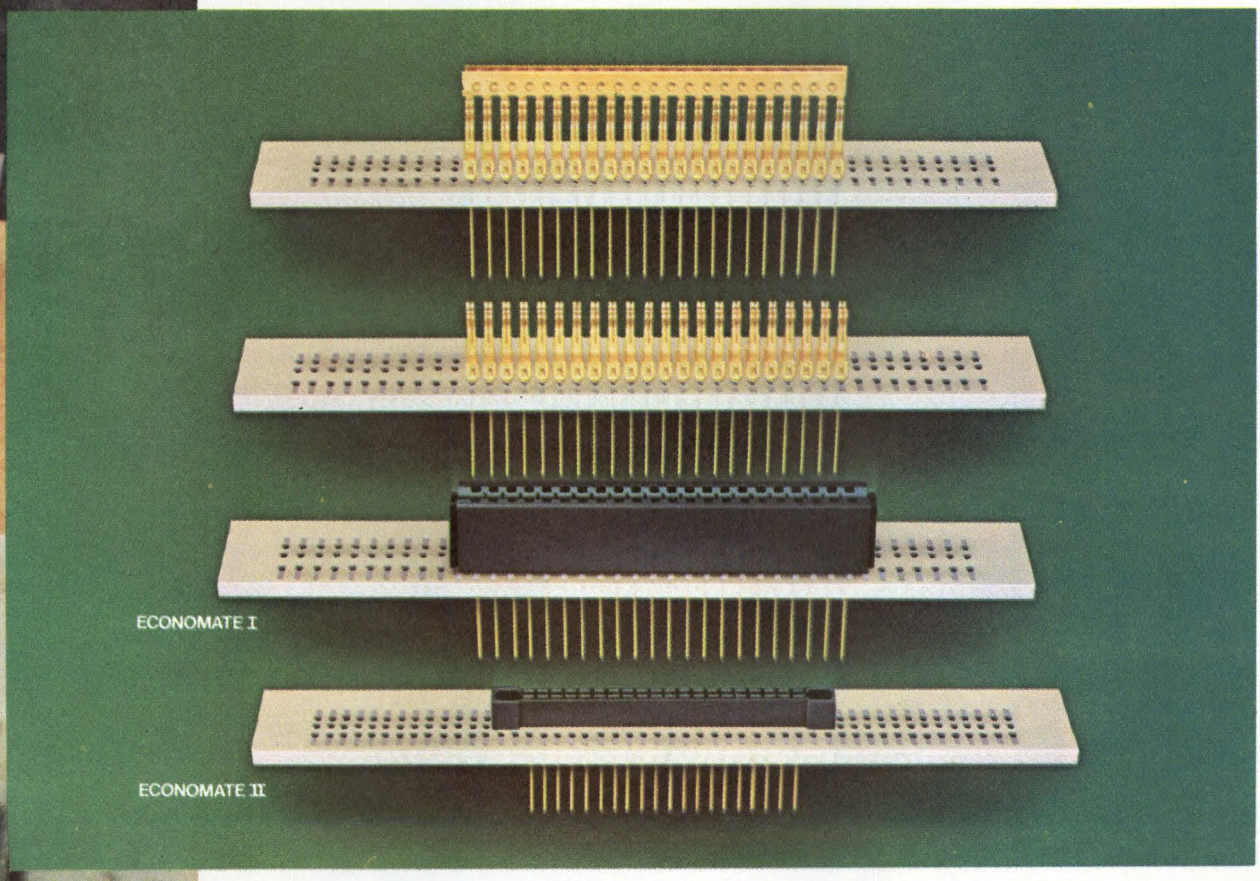

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Digital Technology Enables Robots To "See"

Sydney F. Shapiro
Managing Editor

Robots—covering an extremely wide range of sophistication—have existed for many years. Some have never left the laboratory environment; potential or practicability indicated in the research atmosphere has not always been proven practical for development into real-life systems. Yet, many true robots—maintaining at least some degree of sophistication—have been put to work.

Depending on configuration and design concept, robots are capable of performing diversified tasks—from the manipulation of small, delicate components in fabricating alternators or electric motors to moving heavy automotive engines into various positions for assembly. As sophistication increased, computers began to play larger and larger roles—and not just for programming or massaging data concerning the robots. The availability of high capacity but inexpensive minicomputers enabled the dedication of individual computers to control the actions of single robots. Carrying this dedication concept even further, microcomputers now are assigned to the control of individual joints in robotic arms.

One key capability, however, has generally not been available: vision. Over the past several years, many research facilities have been attempting to develop practical techniques for providing vision to robots, to enable those robots to search for and recognize specific parts, and then do something with those parts. Some laboratory success has been indicated; yet practical systems have been relatively rare. Although the following discussion, of necessity, covers only a very small portion of the overall subject, it serves as an introduction to the technology.

Robot Configurations

In spite of the mentioned wide range of sophistication, all robots are made up of the same basic components: manipulator, controller, and power supply.[1] A summary of those components and a review of other general robotic capabilities aids in an understanding of the place for vision in the hierarchy of robotic functions.

Manipulators consist of mechanical linkages and joints that can move in various directions as driven directly or indirectly by actuators (Fig 1). Feedback data, in either digital or analog form, are transmitted to the controller from sensing devices that monitor positions of the linkages and joints.

Mechanical configurations for manipulators are commonly based on cylindrical, spherical, or jointed-spherical coordinate systems. A cylindrical coordinate robot is basically a horizontal arm mounted on a vertical column which is in turn mounted on a rotating base. The arm moves in and out as it moves up and down on the column; both arm and column rotate as a unit on the base. Work area or envelope of motion configuration is a portion of a cylinder.

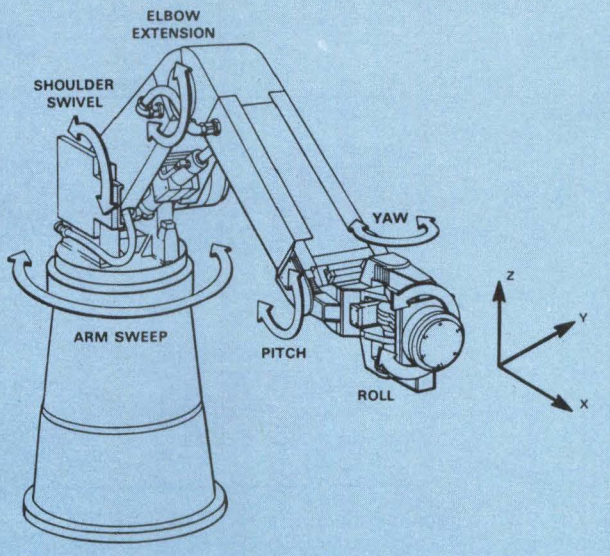

Fig 1 Jointed-arm mechanical configuration and coordinate system for robot with six axes of motion.[2] In this example, each axis is driven by individual hydraulic actuator. Feedback signals representing change in angular position and velocity of the axis are sent to control system. Many robots have far less sophistication since each axis shown here represents a considerable cost from both mechanical and digital control aspects

(*Continued on p 44*)

Robots with a spherical coordinate system can be related to the turret of a tank, with an arm that moves in and out, pivots in a vertical plane, and rotates in a horizontal plane about the base. Work envelope configuration is a portion of a sphere.

A jointed-spherical (or jointed-arm) coordinate system robot comprises a base or trunk plus an upper arm and forearm which move in a vertical plane through the trunk. It includes a shoulder joint between upper arm and trunk, and an elbow joint between upper arm and forearm. Horizontal plane rotary motion is also provided at the shoulder joint. Work envelope configuration for this system is a portion of a sphere.

For some robots a wrist joint can provide up to three additional movements: roll or rotation in a plane perpendicular to the end of the arm, pitch or rotation in a vertical plane through the arm, and yaw or rotation in a horizontal plane through the arm. In addition, the robot can be mounted on an X-Y table or track for two more axes of motion.

Controllers initiate and terminate manipulator motions in chosen sequences and at specified points, store position and sequence data in memory, and communicate with ancillary devices such as printers for management information reports. They vary in complexity and capability from simple step sequencers to minicomputers, or may be memory devices that are preprogrammed for specific robot duties. Each controller initiates and terminates manipulator motion after interpreting information received from the sensors.

Energy for the actuators is provided by the third component, the power supply. That energy may be electrical, hydraulic, or pneumatic, depending on the robot's design.

Computer Control

A must in the programming of any robot is that the controller know the exact position of all robot joints at all times and be able to take decisive action as the result of foreseeable but random occurrences.[2] Use of

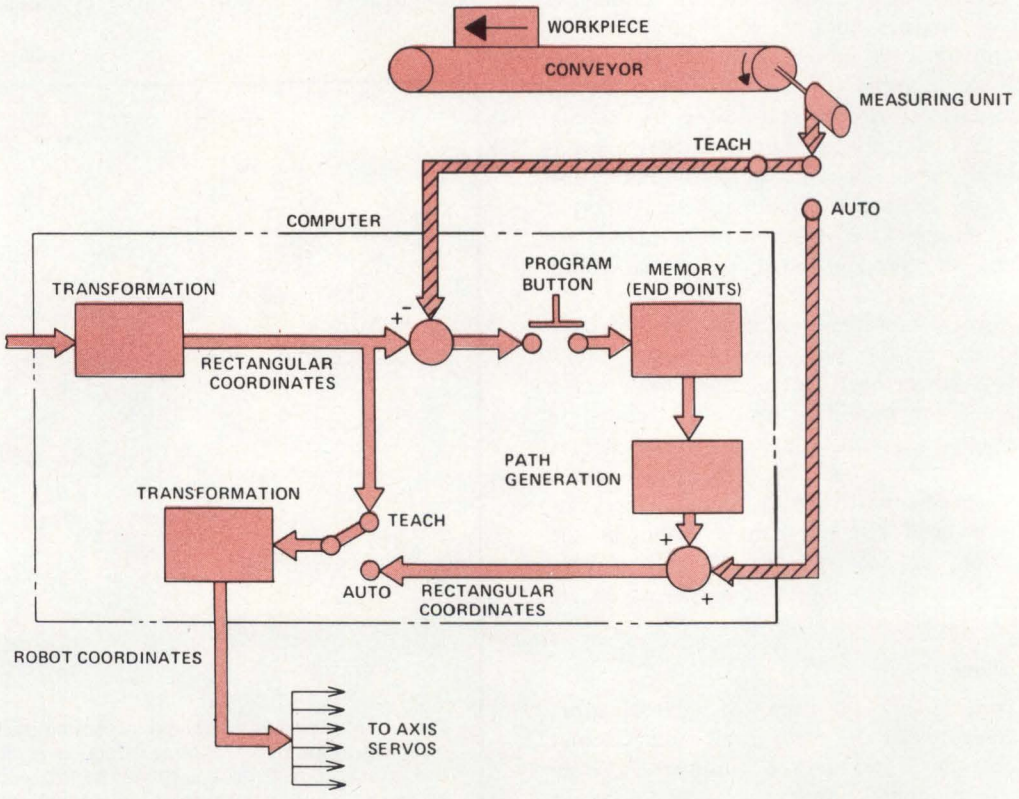

Fig 2 Block diagram of computer control system for stationary base industrial robot.[2] Position sensor interfaces to computer, with robot placed such that X-, Y-, or Z-axis is parallel to moving line. However, greatest robot utilization in terms of tracking range is made when Y-axis is parallel to line

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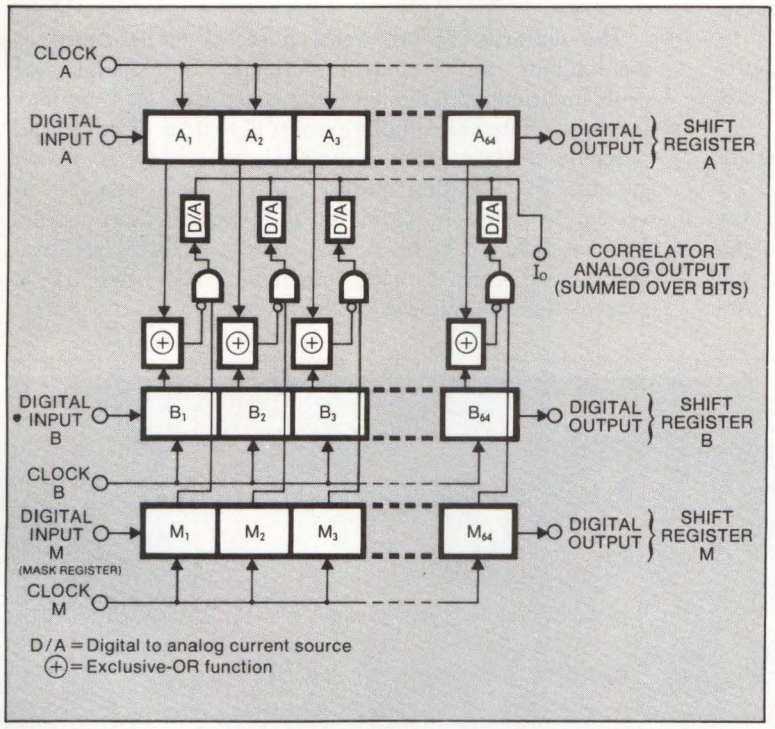

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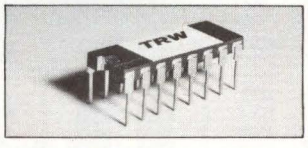
The TRW TDC-1004J is a 64-bit digital correlator capable of operating at 15 MHz with analog correlation output. Digital parallel correlation is a signal processing technique used for bit synchronization, bit detection, error correction coding, pulse compression and other applications. Correlation takes place when two binary words are serially shifted into two independently clocked shift registers. The two words are continually compared bit-for-bit by exclusive-OR circuits.

Each exclusive-OR circuit controls a current source D/A. The current outputs of the D/A circuits are summed to produce the correlation function.

The mask register allows the user to selectively choose "no-compare" bit positions.

For detailed data and prices, contact your local TRW sales office or call (213) 535-1831 or write TRW LSI Products, An Electronics Components Division of TRW, Inc., P.O. Box 1125, Redondo Beach, California 90278.



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a computer as the controlling element provides the flexibility necessary to carry out such actions easily.

Fundamental application of any robot is to move a manipulator from one programmed point to another and then to carry out a desired action. The computer's capabilities provide coordinated control of predetermined actions within a set coordinate system.

An example of a computer control system is provided in Fig 2. This diagram indicates the flow of information through the system during both teach and automatic modes of operation.

During teach mode, the part is positioned at a convenient location in front of the robot. Points are taught as normal but each coordinate in the direction of the line is modified by an amount equal to the current position sensor reading, prior to being stored in memory. Stored data, therefore, are referenced to the start point of tracking. If more convenient, the part may be repositioned at any time during this teaching operation.

In automatic mode, the stored points are used to generate the desired paths, which are then modified by the current position sensor reading. In this way, the control changes the coordinates of taught points in the tracking direction by an amount equivalent to the distance between the position of the part at which the point was taught and the position of the part at which the point is replayed.

Because point coordinates are stored as rectangular and orientation coordinates in space, only the translational coordinate in the direction of the moving line needs to be modified. Since all other coordinates remain the same, the three coordinates representing the orientation of the end effector relative to the part do not change during automatic operation. The end effector, therefore, always replays a programmed point with the same orientation relative to the part as was taught. If the robot was programmed to avoid an obstacle in a certain way during the teaching operation, for example, it will avoid that same obstacle in the same manner during automatic operation.

A great deal of research activity is currently underway towards development of both greater robot capability and more sophisticated computer control. Some of the U.S. research, particularly at universities and laboratories, is federally sponsored although evidently not to the extent that this occurs in several foreign countries.

The majority of the research seems to be aimed at manipulator path control systems, development of problem-oriented languages for programs, and sensory feedback systems. Although control systems for feeding parts do not yet exist, research is underway on vision systems for locating parts, and at least one vision system is being used on a "production" line (as described later). A brief summary of three research studies (abstracted with comments from Ref 3) is presented in the following paragraphs.

Work is being conducted at SRI International in sensory feedback control systems, manipulator path control, and training aids. This approach consists of modular control system components that configure into an overall system. Hardware interfaces have been developed between the computer systems and the manipulators, and the sensors can be usefully transplanted, given the same CPU type. Vision system software is less transferable than path control software.

The vision system utilizes main memory to store prototype models of assembly parts. Usefulness of path control software to assembly systems will largely be determined by the manipulator duty cycle time requirements. If the duty cycle is short and the path to be executed is sufficiently complex, with tool changing and sensory feedback being utilized at several points in the path, the computational time required to transform coordinates, interpolate between boundary points on the path, and compute arm solutions may be excessive.

By using reflected light and placing the parts on a background that provides good contrast, features based on the geometry of the part's outline and the number, size, and location of contrasting features within the parts can be used for recognition and inspection purposes. The company has also developed use of vision for servoing a manipulator arm during an assembly operation. This technique which utilizes an "eye-in-the-hand" approach could be used for monitoring operations during automated assembly.

Studies underway at the Charles Stark Draper Laboratory concern passive compliance, force feedback control, and overall control strategies. Passive compliance provides an open-loop solution for insertion. Work on force feedback has established a sound theoretical basis (with open-loop validation of analytical models) from which to proceed to real-time, closed-loop control experimentation. Software development is required before their force feedback concepts can be applied usefully.

Concepts developed at the University of Rhode Island on visual point-to-point instruction and on orienting workpieces acquired by a manipulator hand may be useful to the development of programmable assembly systems where there is uncertainty in the position of a part in a gripper. Researchers are attempting to solve the problems related to the visual identification of parts in a "heap," and the acquisition of a recognized part from the heap. Binary image processing is currently being used, and utilization of vision to orient a part that has been acquired by a manipulator arm has been demonstrated. The technique may be useful where the stable state of a part is not identifiable in the part's presentation equipment.

Vision Systems

Computer control has increased the sophistication of robots to the point that delicate as well as brute-force tasks can be performed. Robots can assemble automotive motors, spot weld, spray paint, load and unload, and move material. Yet until very recently, they performed those operations blindly. They could not "see." Actions were synchronized through touch or proximity sensors, but not through visual initiators.

(*Continued on p 52*)

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Rather than passively watching system operation, the μScope 820 console lets you execute application programs or diagnostics you develop, in real time or single steps. And it provides full breakpoint capability and a large trace memory.

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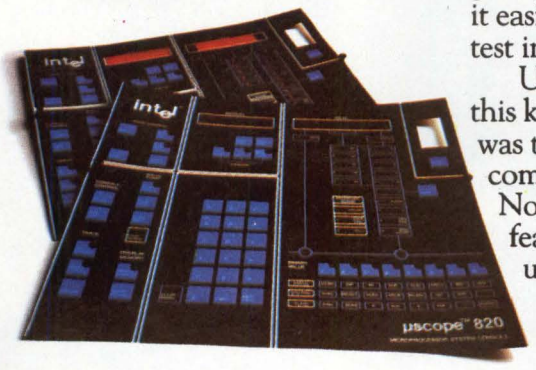

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CIRCLE 29 ON INQUIRY CARD

Now, however, studies such as those at SRI International and the University of Rhode Island, as well as at a number of industrial organizations here and abroad, have resulted in at least a degree of vision. Initial application is expected to be in the recognition of parts and their orientation, inspecting parts for defects, and monitoring assembly processes.

Robot hands are not as sensitive as human hands; they cannot measure workpiece slippage or determine attitude of a piece by feel. Therefore, a robot might not properly align a piece or might collide with an unexpected obstacle while moving the part.

At the University of Rhode Island,[4] in a research project partially supported by the National Science Foundation, two TV cameras are used. An algorithm developed as part of the project computes arm joint values needed to compensate for the misalignment of workpieces in relation to a robot hand. This algorithm relates changes in the features of images from the cameras to changes in the position and orientation of a workpiece.

When each workpiece is brought to a visual check station, the TV cameras extract image feature values from the pair of images. Image features such as the center of gravity and direction of the minimum moment of inertia axis, extracted from the binary image of the workpiece, are compared with those expected. If feature variations are within a small range of acceptable misalignment, the workpiece can be moved to the fixture. However, if the misalignment is too great, the workpiece's position must be corrected before it can be transported to the fixture.

Robots with "vision" were introduced as standard products by Auto-Place Inc in 1976.[5] This capability, called Opto-Sense, is based on use of a solid-state video camera to convert optical information to electrical data which can be processed by a microcomputer. Decisions are made by the microcomputer, based on programmed parameters of the application, and sent to the robot as program changes.

The imaging device contains an X-Y array of 188 horizontal by 244 vertical picture elements or pixels (a total of 45,872) in a 1.15 x 0.87-cm area. Each light sensitive pixel provides an output based on whether the light measured is above or below an adjustable threshold. Below the threshold, the pixel registers white; above, black. The entire array is scanned in 16 ms.

Output signals from the microcomputer are converted through standard solenoid valves to air signals that cause the motions of the robots to be altered. Thereby, robots linked with video cameras can look at, inspect, and classify various industrial parts. Parts with a large number of holes, assemblies with critical parts, critical sizing of part configuration, and scratches or defects in parts can be inspected by measurement of light and dark areas. Where required, backlighting can easily be provided to define light and dark areas better.

In a current industrial application, a robot automatically inspects transmission separator plates for missing holes and sorts them into one of four model classifications. The robot loads a part into the inspection station, where approximately 100 small holes in the separator plate are analyzed for presence. A microprocessor output signal determines the motions of the robot in placing the part into one of four model stacks or a reject station.

Instead of the "white or black" sensing technique, two approaches being researched at General Motors Corp are based on multiple intensities of gray levels. In each, data on the item being analyzed are obtained by digitizing the sampled output from a TV camera.[6] The digital picture is normally stored as a 2-dimensional array of integers, in which the value of each array element corresponds to the average light intensity of one small area of the picture being represented (a pixel). Precision is based on spatial resolution (the camera's sampling density) and gray level resolution (the number of distinct levels into which the range of analog light intensity values are quantized).

For each approach, data on all pixels of each array are relayed to the related computer, but at that point the two methods diverge. One approach can rapidly and reliably find nonoverlapping parts even on visually confusing surfaces which tend to camouflage outlines—such as conveyer belts.[7-9] The other vision system can recognize and determine the position of several parts in the same scene, even if they are overlapping and partially obscured.[10-12]

A system based on the first of these approaches—finding nonoverlapping parts—has been online at GM's Delco Electronics Div in Kokomo, Ind since January 1977. SIGHT-I is said to be the first industrial computer-vision system of its kind to go to work on a U.S. automotive production line. The product of a cooperative effort by three GM groups—Research Laboratories, Manufacturing Development, and Delco—the computer-camera system locates and calculates the position of transistor chips during processing for use in car and truck high energy ignition systems. It also checks each chip for structural integrity and rejects any defective one.

The part to be inspected consists of a Darlington power transistor-pair 5.26 x 5.26-mm IC chip bonded to the surface of an 8.99 x 12.70-mm heat sink, with a weld cup on one corner of the heat sink. Assemblies are mounted firmly on fixtures and fed automatically onto a rotating table.[7]

In manual inspection systems, position and orientation of the chip is determined visually by a human operator who then inspects the chip for gross defects and manually manipulates test probes over the base and emitter areas of the chip. For the automated system, operator, viewing device, and position manipulators have been replaced by a solid-state camera that interfaces to a minicomputer for sensing the assembly at the stage before electrical test.

Using digitized data from the camera, the computer works through a sequence of image enhancement operations to silhouette the part and emphasize its outline. First the computer increases the intensity of the tiny squares along the boundaries (edges) of the

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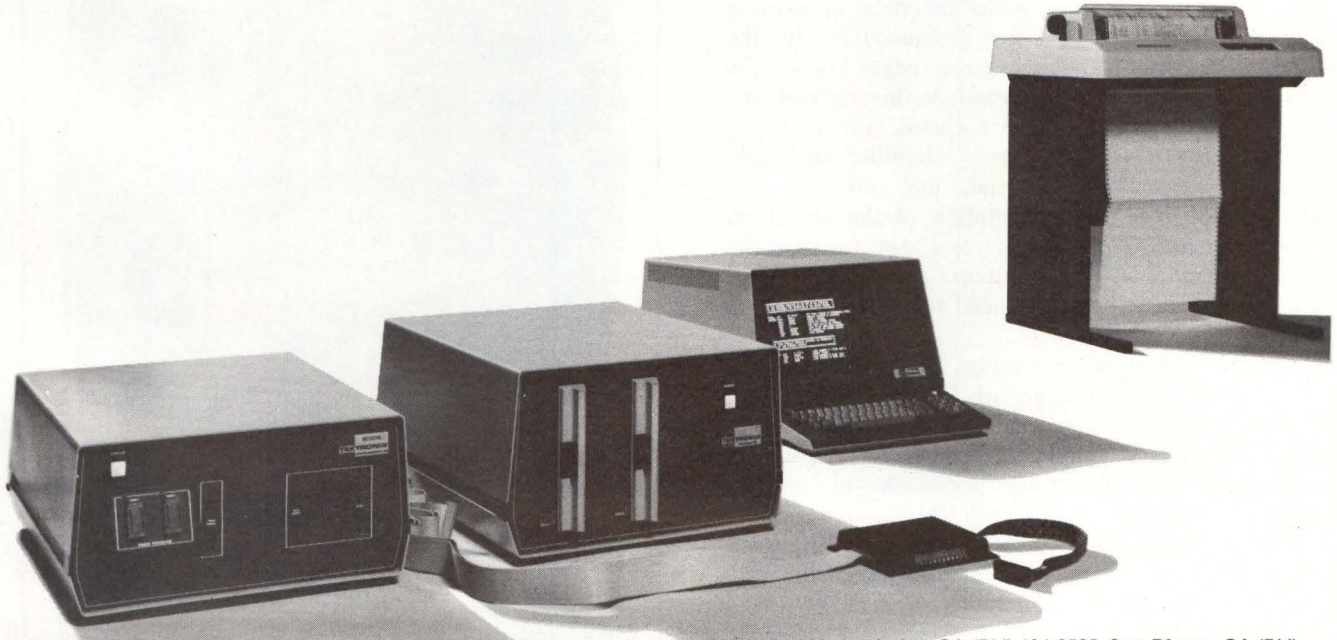

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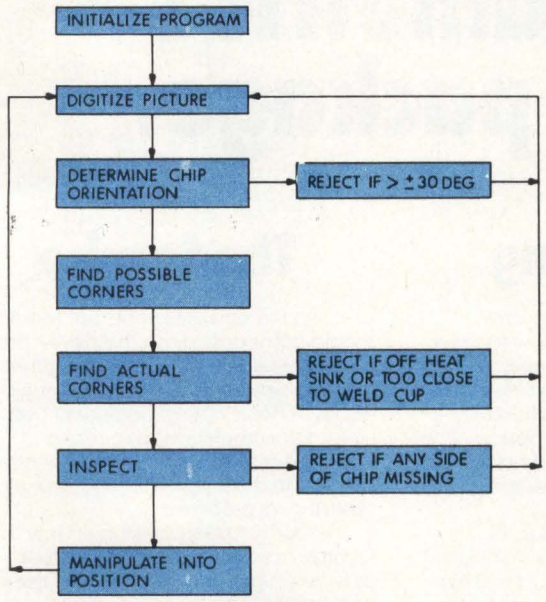


Fig 3 Program logic flow chart of automated "vision" IC chip inspection[8]

objects (Fig 3). Then it smooths the data by erasing isolated false edges caused by irregularities in the background and by inserting more edges along the object boundaries. Further operations insure that the boundaries of all the objects are closed, and that any "holes" inside the connected parts are filled in. From the well-defined outline obtained, the computer can calculate the position and orientation of the object on the conveyor belt. This system does not use specific mathematical models. The computer just locates and emphasizes edges; it does not need to know what it is looking for.

In typical industrial assembly line environments, however, simple thresholding of a gray-level image is not adequate in distinguishing objects from background. To solve this, another research project is underway at GM—using the same approach—to provide vision to an industrial robot such that it can rapidly and reliably determine locations of nonoverlapping parts placed on conveyor belts.[9] Potentially, this system will operate under minicomputer control at typical production line cycle times of 1 to 5 s.

Objects are extracted visually from conveyor belt backgrounds through a sequence of image enhancement operations involving edge detection, smoothing, automatic threshold selection, gap filling, connectivity analysis, and hole filling. Resultant silhouette images of the objects contain sufficient information to locate the parts by determining orientation, without observation of internal features.

The second approach also uses a TV camera to pick up images which are digitized into gray-scale pixels and relayed to the computer. However, it can recognize and determine the position of several parts in the same scene—even if they are overlapping and partially obscured.[10-12]

Image data obtained from a 256 x 256 array are first transformed into edge-point (or gradient) data. Then the edge points are connected into chains (ordered sets of linked edge points), and finally the chains are transformed into ordered sets of connected curves (straight lines and circular arcs) which have the appearance of a line drawing (Fig 4).

Objects that the computer is to recognize are "shown" to the computer in turn under good lighting conditions. The computer analyzes each part, computes geometric properties of the part's boundaries and any internal holes, forms a model, and commits that model to memory.

Then the computer matches characteristics of objects on the conveyor belt as seen by the camera against

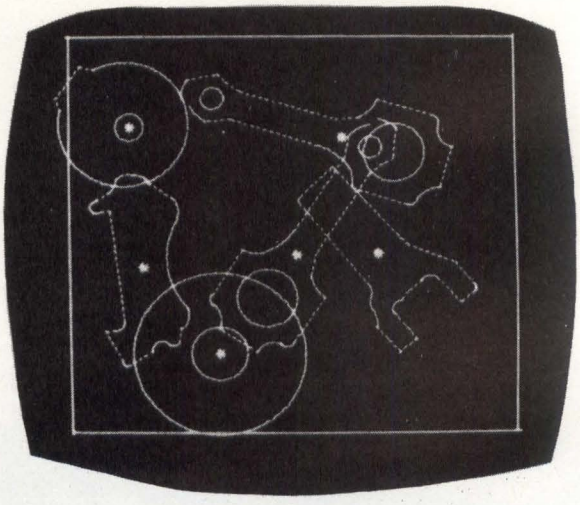
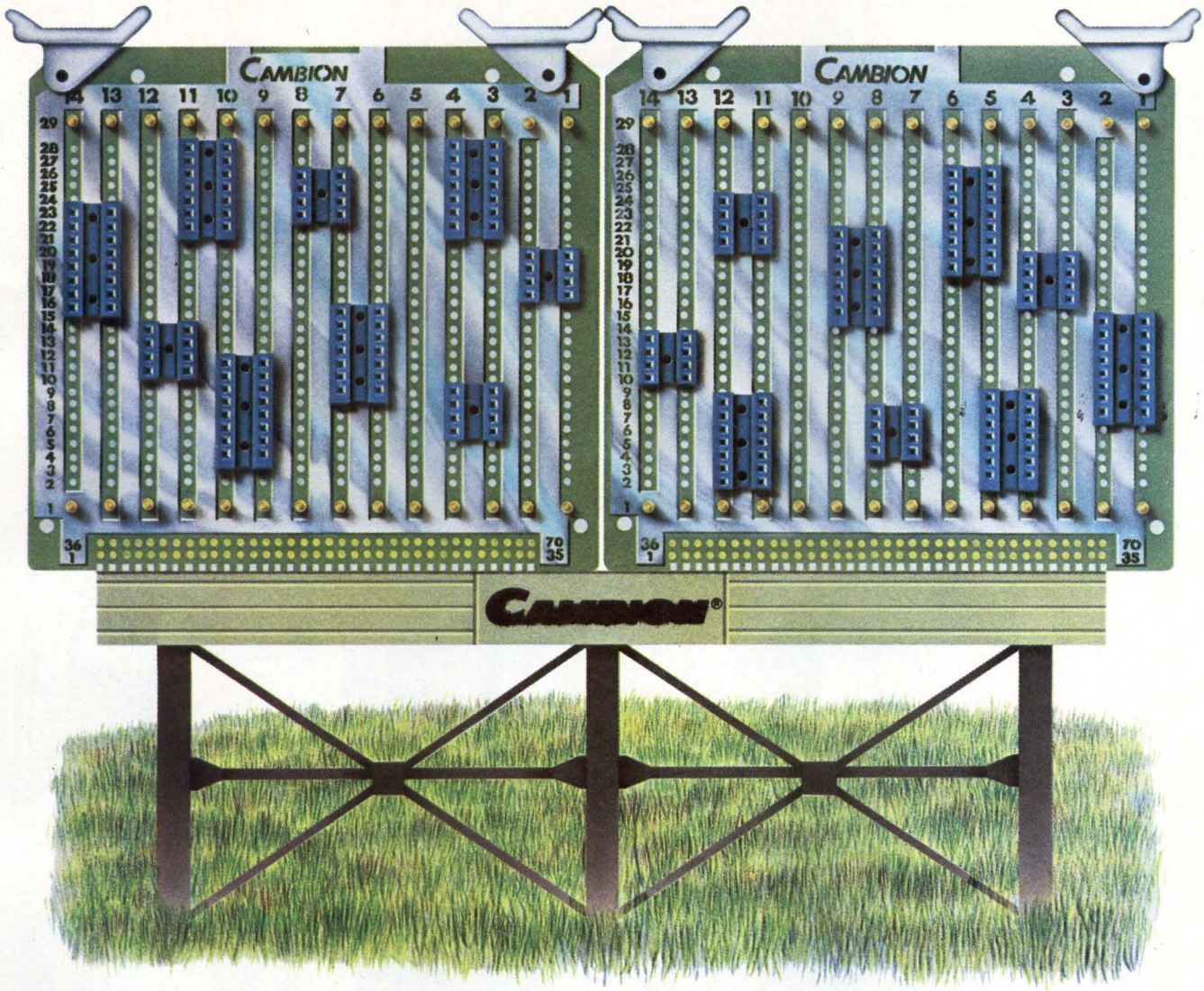


Fig 4 "Line drawing" view of computer vision system that can distinguish overlapping or partially obscured parts. Locating these six parts required 31.6 s of CPU time (25.4 s for image analysis, 6.2 s for matching).[11] Computer analyzes each part, computes geometric properties, forms and memorizes models, and then finds parts by matching what it sees with models and recognizing those that are similar



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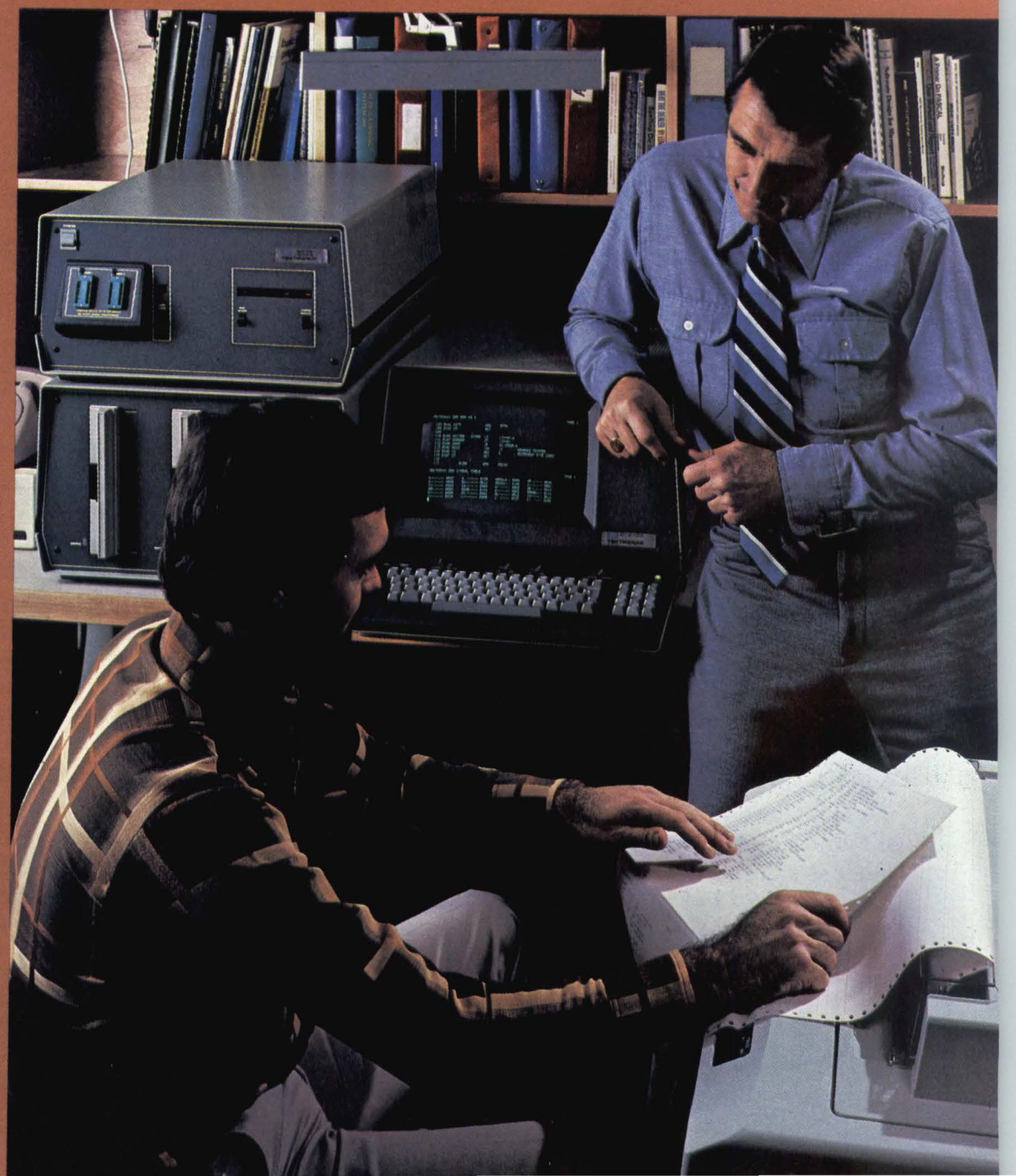

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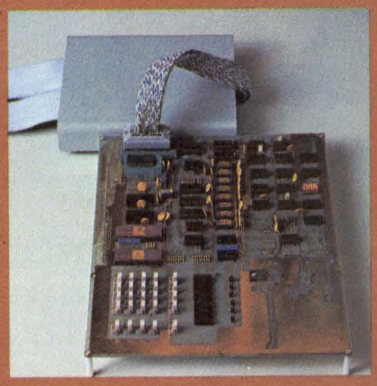

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the models. It is able to recognize those parts that are similar to the models even if it can see only parts of them or if the light is poor. Once a desired part is located, the computer determines its position and orientation.

Both of these approaches are still in the research stage—even though SIGHT-I is based in part on one of them. Drs Michael L. Baird and Walton A. Perkins of GM's Warren, Mich Technical Center have reportedly made progress,[7-12] but a major step is involved in coupling one of the computerized vision system with a robot arm or manipulator. Further study to accomplish this coupling—which will enable the robot to do something with what it sees—is underway at GM's Research Laboratories as well as other facilities in the U.S. and several foreign countries.

Summary

Eventually robots will be able to locate parts, inspect them, turn them over if necessary, and align them for assembly. These and other tasks which robots can accomplish only with "sight" are now within reason.

The overall subject of robots, of course, is truly immense. A great deal of information is available for those readers who care to learn more about general robotics and vision capabilities—and about the overlying influence of digital electronics.

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Microcomputers In Three Cities Maintain Vehicle-Actuated Traffic Control

Continuing its implementation of microprocessors for highway traffic control (*Computer Design*, Jan 1977, p 58; Feb 1977, p 57), Philips Telecommunicatie Industrie B V, Hilversum, The Netherlands has installed or has contracted to design similar systems in two cities in Ireland and one city in Iraq. Prior to this, the company had installed control equipment at 125 traffic intersections in Ireland.

The latest system involves O'Connell St in Dublin, where automotive vehicles enter a section of this arterial highway less than half a mile long from 14 secondary roads. In addition, this street is a shopping center with heavy pedestrian traffic.

To help solve this problem, which traffic police found very difficult to handle, an offline evaluation technique called Transit V was used. A central processor selected optional traffic control programs based on both vehicular and pedestrian traffic measurements. This offline evaluation resulted in a reduction of installation time, and minimal traffic disruption, since the entire configuration had a complete trial run before leaving the factory.

For Cork, Ireland's second largest city, with narrow streets that are easily jammed by traffic, a control system is being designed for installation in two stages. The first will cover 13 intersections and was scheduled for commissioning by late 1977; the second, involving an additional 26 intersections, will be operational early this year.

Central control for this system is based on two microcomputers, fed by information from 22 detectors at strategic highway locations. Programming will allow for four traffic control plans: the usual manual control and clock control plus programs best suited to traffic situations as chosen by a traffic/detector actuated selector. In addition, special control plans will be included for emergency east/west traffic between an industrial site and the hospital, traffic from a sports center, fire fighting vehicles, and police road blocks.

Baghdad, Iraq will have a hierarchical microcomputer-based traffic control system for the busy central city. Controllers will be installed initially at 28 intersections, with microcomputers at the most vital. These intersections will be arranged in two groups, with each group coordinated by a higher-order microcomputer. Top control of the hierarchy will be a central computer that will coordinate the entire area.

Also tied to the system will be closed circuit TV for visual monitoring of key spots and a wall map that will display the current state of traffic. All information from the detectors will be processed for statistical as well as control purposes.

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DC&AS BRIEF

Computer Converts Metric Specifications to American Standards Over Phone Line

When American Motors Corp (AMC) purchased a complete engine manufacturing plant from VW-Audi in West Germany, it found that all of the facility's machinery and assembly/operation drawings were set up to metric standards. In addition, the machinery operated on European electrical current levels.

To convert drawings and assembly specifications to those applicable for U.S. operations, AMC personnel developed a computer program for use on a mainframe computer system based in a Detroit data center—a dual model 66/60 from Honeywell Information Systems, 200 Smith St, Waltham, MA 02154. Engineers at the Richmond, Ind location of the plant where the equipment is being installed interface to the computer over a dial-up, 1200-baud, asynchronous line with synchronous modems at both ends.

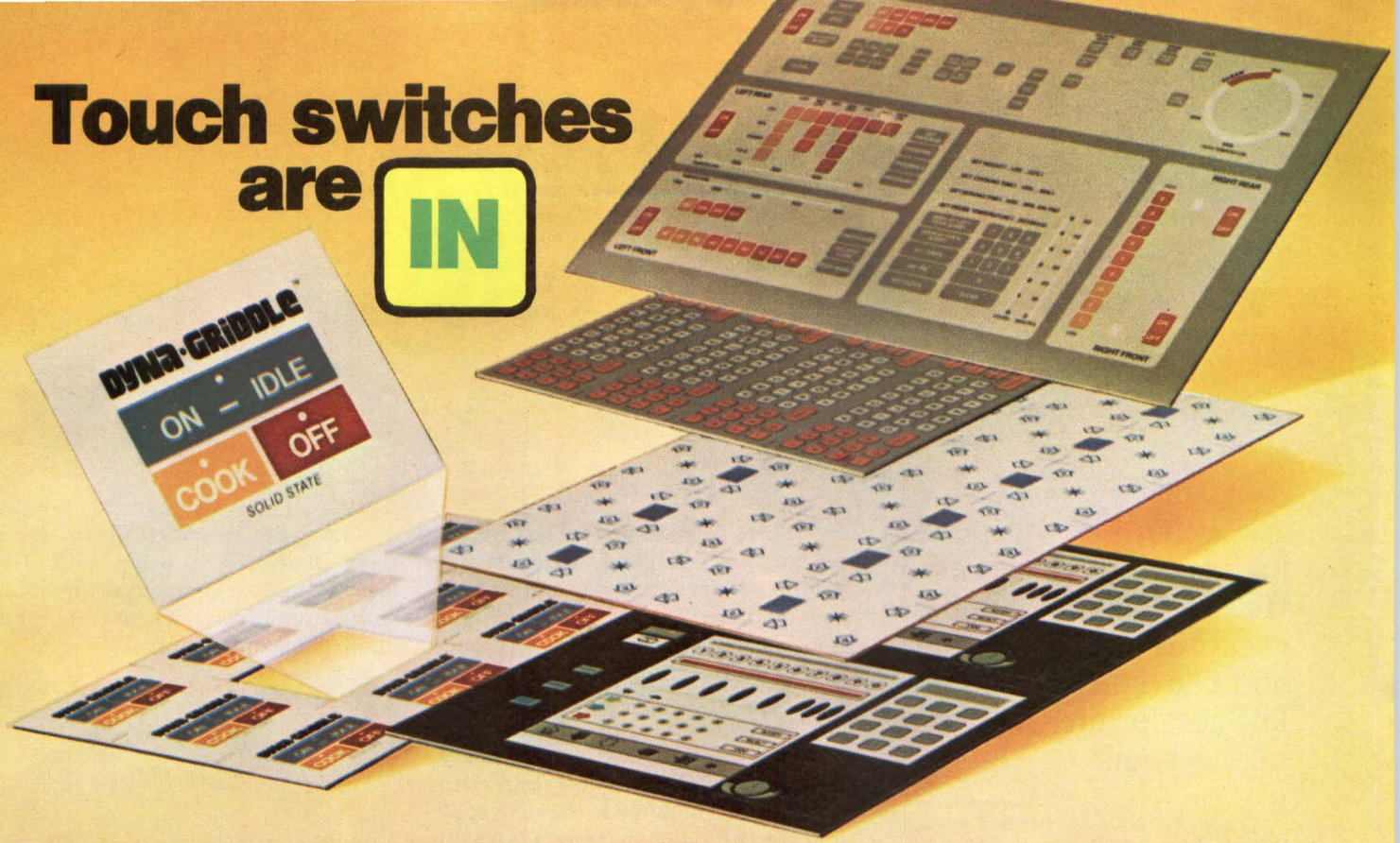
Using a Tektronix video display terminal, the engineer creates a file on a particular part or circuit using one of 60 electrical symbols stored in the host computer's 512k words of main memory. Another symbol indicates whether the circuit is in series or parallel. In the data center a Calcomp 936 printer produces a rewired schematic complete with interconnections and parts cross references.

As parts and specifications are added to the data base, a tape is produced and the plotter prepares the finished drawing which is then available for recall, update, or reference whenever needed. Finished drawings are relayed to Richmond in 1-h turnaround.

Single-Control Input to Rolling Mill Replaces Several Panels of Switches

Unlike more common computer-controlled steel rolling mills where changes in presettings are made manually, with a series of individual controls to adjust speed, pressure, and other variables for each of several positions, a 79″ (200-cm) hot strip rolling mill at Bethlehem Steel Corp's Lackawanna, NY plant functions on a single control. The mill operator can simultaneously feed adjustment information to all of the computer-controlled positions throughout the plant. □

Touch switches are IN



...and CENTRALAB has them NOW

When Centralab introduces touch switches you can be sure they're "In". Backed by 40 years of switch know-how, and after years of intensive research and testing, Centralab is now delivering, in batch-process volume, a complete touch switch system. We call it MONOPANEL.

MONOPANEL is a thin, light, flat, front panel subassembly containing micro-motion touch switches already mounted and interconnected . . . with LED's, nomenclature, graphics and colors to meet your functional and aesthetic requirements.

Batch-Processed For Economy With Quality

MONOPANELS are batch-processed as 11" X 17" master panels only .075" thick, each containing up to 700 switches. Every Monopanel is a complete, 100% pre-tested subassembly containing switches, front panel and graphics.

60,000,000 Cycles Without Failure!

The basic MONOPANEL switch has been operated for sixty million switching cycles without mechanical or electrical failure. And MONOPANEL has been tested and proven against 22 separate mechanical, electrical and environmental standards.

Custom Designed For Your Application

On each 11" X 17" panel you can custom-design individual boards to meet your front panel needs. The illustration above shows just a few of the almost endless variations possible from each master panel.

Unlimited Graphics Available

The flat, smooth, front panel surface permits unlimited choice of graphics. Functions may be grouped by color, with 480 colors available. Thirty choices of type style and size. And whatever visual symbols meet your specific needs.

THIS IS MONOPANEL:

- A complete touch switch subassembly, ready to mount.
- All switches and graphics on a .075" thin panel.
- Flat, spill-proof surface wipes clean.
- Noiseless.
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- Operating current: 100 mA max.
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CIRCLE 37 ON INQUIRY CARD

Hard copy made easy.

With the help of a high-speed microprocessor, Hewlett-Packard combines exceptional performance and convenience in a new low-cost printer and printing terminal.

The HP 2631A printer and HP 2635A printing terminal with alphanumeric keyboard are the first members of a new Hewlett-Packard family of hard copy terminals.

Each machine was designed to give you a number of high-performance features. And both can support a variety of interfaces, including RS232 and CCITT.V24, to fit into systems made by HP and other manufacturers.

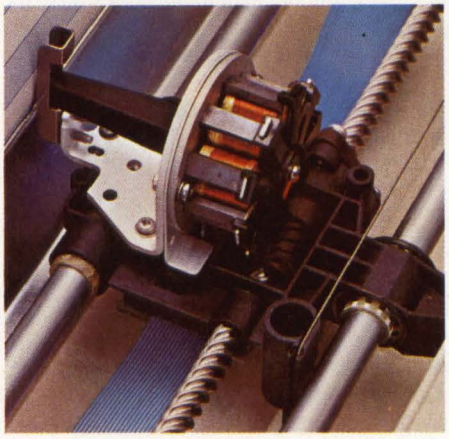
Bi-directional printing increases throughput. Both printers zip along at 180 cps in both directions, depending on your line layout. The microprocessor chooses the quickest path, and increases the speed even more by suppressing leading and trailing blanks.

High-speed slew for columnar data. When the microprocessor senses more than ten blanks in a row, it slews the print head at 45 inches per second to the next print position.

Three ways to print. The Character Compress/Expand Modes let you print more data on a page and emphasize points with headlines and titles. You can get as many as 132 characters on an 8-inch line, or 227 on a 14-inch line.

High-quality print, with six copy resolution. A 7 x 9 dot matrix (versus the usual 7 x 7) gives you clear, crisp printouts, right down to the sixth copy and meets the 128-character USASCII standard. And the extra two dot rows allow true underlining and descenders without character blurring.

Programmably interchangeable character sets. The HP 2631 can be made to print alternate character sets without reconfiguring the printer.



Long lasting, quick change print head saves service calls. The 9 wire print head is conservatively rated at a 100 million character life-span. It's also self-aligning. When you finally replace the head, you can do it yourself in a couple of minutes.

Long-life cartridge ribbon for a clean change. With a life span of at least 10 million characters, this innovative drop-in cartridge takes the mess and trouble out of ribbon changes.

Self-test for quick status checks. One key tells you if the printer is ready to go. If it isn't, the self-test feature helps you isolate the problem, reducing the time and cost for repairs.

Run everything under program control. All the features described and more can be programmably controlled. The software can take you in and out of the various modes. Or you can make a change yourself using one of the front panel switches or keys.

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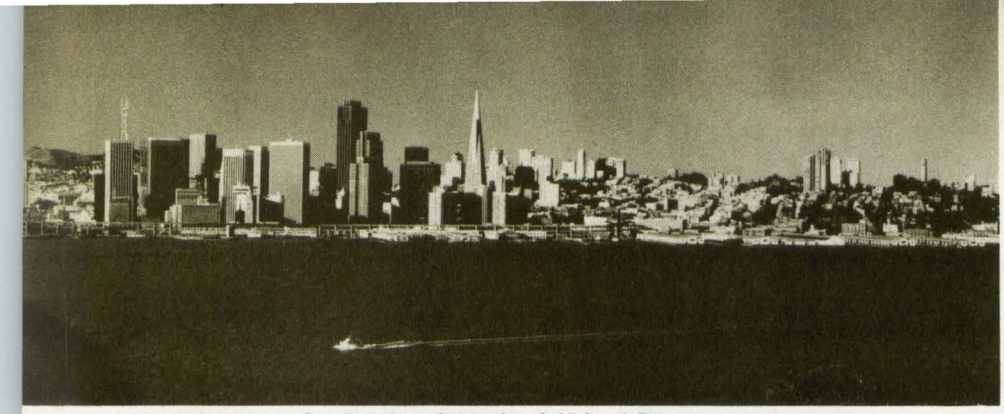

Photo courtesy of San Francisco Convention & Visitors' Bureau

Donald E. Rosenheim
General Chairman

Dean Brown
Program Chairman

Seymour R. Cray
Keynote Speaker

February 27-March 2
Jack Tar Hotel, San Francisco, California

COMPCON 78 Spring
Sixteenth IEEE Computer Society International Conference

"Computer Technology: Status, Limits, Alternatives," will be the theme of COMPCON 78 Spring. This conference will be officially opened at 9:30 am on Tuesday, February 28 by Donald E. Rosenheim, general chairman; Dean Brown, program chairman; and Merlin Smith, president of IEEE Computer Society, with a welcome and presentations of awards. Seymour R. Cray of Cray Research, Inc, will then present the keynote address that questions "Why bother with large computers?"

In 31 technical program sessions, the conference will cover areas such as distributed processing and computing, microprogramming techniques, microprocessor developments, high level system languages, LSI testing, and office systems word processing. For the first time, several program sessions will cover Personal Computing and special exhibits on that subject will be available from 5 to 10 pm on Monday through Wednesday.

An all-day tutorial entitled "Limitations and Alternatives in Future Silicon LSI Technology," led by James M. Early of Fairchild Camera and Instrument Corp, will be presented on Monday, February 27, as a lead-in for COMPCON. Tutorial topics will include n-Channel Memories, CCD Memory, Bipolar and Related Memories, and Microprocessors and Up. The day will conclude with a period of questions and answers; extensive notes documenting each talk will be provided.

On Wednesday morning, recent works and applications will be reported in 5-minute presentations. Informal discussions will follow, with Professor Martin Graham presiding. A special meeting on microcomputer standards on Wednesday evening will feature Dr Robert Stewart presenting a status report on the efforts to develop standards relating to microprocessor software and hardware.

Advance registration fees (prior to February 13) will be $50/$65 (IEEE-CS member/non-member) for COMPCON only or Tutorial only and $100/$130 for both. Advance session chairman and speaker fees are $20, $50, and $70, respectively; and advance student member fees are $15, $25, and $40, respectively. (A current student-body card is required to qualify for the student member fee.)

Registration fees after February 13 for the above respective items are $60/$75 and $120/$150; $20, $60, and $80; and $15; $30, and $45. All these fees include a copy of the COMPCON Proceedings and/or a copy of the tutorial text. Registration fee for only the Personal Computing sessions will be $5 for all.

Advance registrations should be mailed to Jean Sherman, COMPCON 78 Spring, IBM Corp G32/006, 5600 Cottle Rd, San Jose, CA 95193. Those who cannot attend COMPCON 78 Spring may obtain the digest of papers by mailing a check for $15/$20 (member/non-member) to IEEE Computer Society, 5855 Naples Plaza, Suite 301, Long Beach, CA 90803.

The following excerpts from COMPCON 78 Spring technical program include information available at press time.

TECHNICAL PROGRAM

Tuesday Afternoon

Session 3 1:30-5 pm

Distributed Processing and Data Bases

Co-chairmen: Professor Wesley Chu, University of California, Los Angeles; Robert Thomas, Bolt, Beranek & Newman; Mike Hammer, Massachusetts Institute of Technology; and Robert Millstein, Massachusetts Computer Associates

Session 4 1:30-5 pm

High Level System Programming Languages

Chairman: John Couch, Hewlett-Packard Co

Session 5 1:30-5 pm

Small Business Machines

Chairman: Bill Thomas, Four-Phase Systems

Session 6 1:30-5 pm

Design and Development Methodology

Chairman: Ed Porter, Microtechnology Corp

"A Digital Interface Description," Alice C. Parker, Carnegie-Mellon University

Session 7 1:30-5 pm

Microprogramming Techniques

Chairman: Robert Schopmeyer, Advanced Micro Devices

Wednesday Morning

Session 9 9 am-12 noon

Computer-Aided Design

Chairman: Dave Gibson, Intel Corp

"Computer Verification of Large-Scale Integrated Circuit Maps," B. J. Crawford, American Microsystems, Inc

"Planar Layout Systems," Bala Daram, Xerox Corp

"A Structured Design Standard Environment for Digital Systems," W. M. Cleemput, Stanford University

Session 10 9 am-12 noon

Emerging Storage Technology

Chairman: Leonard Laub, Xerox Electro-Optical Systems

"High Density Silicon CCDs and RAMs," Dileep Bhandorkar and John Hewkin, Texas Instruments, Inc

"Bubble Memories," Hung Liang Hu, IBM Corp

"Electron Beam Addressable Memories," Donald O. Smith, Microbit

"The Optical Video Disc for Digital Mass Memory Applications," Richard F. Kenville, RCA Corp

Session 11 9 am-12 noon

Diagnostic Testing of LSI Logic

Chairman: Tudor Finch, Bell Telephone Laboratories

"LSI Test Overview," C. B. Stieglitz, IBM Corp

"Impact of LSI On Logic Simulations," Y. H. Levendel and W. C. Schwartz, Bell Telephone Laboratories

"Logic Structure for LSI Testability," T. W. Williams, IBM Corp

"Technology Dependent Logic Faults," R. L. Wadsack, Tennessee State University

Session 12 9 am-12 noon

High Order Languages for Microprocessors

Chairman: Gary Kildall, *Digital Design*

Session 13 9 am-12 noon

Communications

Chairman: Don Nielson, Stanford Research Institute

"Ethernet Packet Transport for Distributed Computing," David Boggs and Robert Metcalfe, Xerox Palo Alto Research Center

"Packet and Circuit Integration in the Tram Data Network," Mario Gerla and Don Mueller, Computer Transmission Corp

"ARPA Packet Radio Experimental Network," Ron Kunzelman and Don Nielson, Stanford Research Institute

"A Real-Time Truck Dispatching System," Rolf A. Feitle, System Control, Inc

Session 14 9 am-12 noon

Universal Cross Software for Microprocessors

Chairman: Mike Faiman, University of Illinois

Wednesday Afternoon

Session 15 1:30-5 pm

Real-Time Computations

Chairman: Bob Larson, System Control, Inc

"Reconfigurable System Design Facility: An Architecture Emulation and Measurement Concept," Kenneth J. Thurber, Donald R. Anderson, and Larry D. Anderson, Sperry Univac

"Real-Time Software for Ballistic Systems Defense Systems," Charles R. Vick, Ballistic Missile Defense Advanced Technology Center

"Extended Real-Time Analysis for Electric Power Energy Control Centers," Norris M. Peterson, System Control Inc; and Robert F. Bisbhke, Wisconsin Electric Power

Session 16 1:30-5 pm

Operating Systems for Microprocessors

Chairman: William Dejka, Navy Ocean Systems Center

Session 17 1:30-5 pm

Office Systems/Word Processing

Chairman: Larry Little, Lawrence Livermore Laboratory

"Records Processing—An Alternative," Sam J. Kalow, IBM Corp

"Ink Jet Printer Technology," IBM Corp

"The Minifloppy Disc Drive Reaches Maturity," George H. Sollman, Shugart Associates

"Printer Goals in the Development of Word Processing," Robert A. Greene, Wang Laboratories

Session 18 1:30-5 pm

Very Large-Scale Integration

Chairman: Lew Terman, IBM Corp

"VLSI and Mainframe Computers," Lin Wu, Amdahl Corp

"VLSI and Minicomputers"

"VLSI and Microcomputers"

Session 19 1:30-5 pm

Recent Developments in Small Devices

Chairman: Hannon Yourke, IBM Corp

"Developments in Subnanosecond Logic LSIs," A. Anzai, T. Hirai, R. Takagi, and T. Nitta, Computer Development Laboratories VLSI Technical Research Assoc, Japan

"Status and Limits of Miniaturized FETs," Robert H. Dennard, IBM Corp

"Impact of Semiconductor Microelectronics," Sol Triebwasser, IBM Corp; Richard Eden, Rockwell International; and Gill Varnell, Texas Instruments, Inc

Session 20 1:30-5 pm

Computer Simulation, Model Prediction, and Real World Results

Chairman: N. F. Schneidewind, Naval Postgraduate School

"Some Unique Aspects of Computer Simulation in Bio-Medicine —Blood Sugar Regulation: A Case Study," Ivan Nelson, Loma Linda University

"Team Architecture Real-Time Computing System for General Aviation," Thomas McCalla, Jr, Southern Illinois University

"Comparison of Simulator Predicted Operating System Performance With Actual Performance," N. F. Schneidewind and E. Fiegel, Naval Postgraduate School

Thursday Morning

Session 22 9 am-12 noon

Economic Modeling

Chairman: Carl Noble, On Line Decisions

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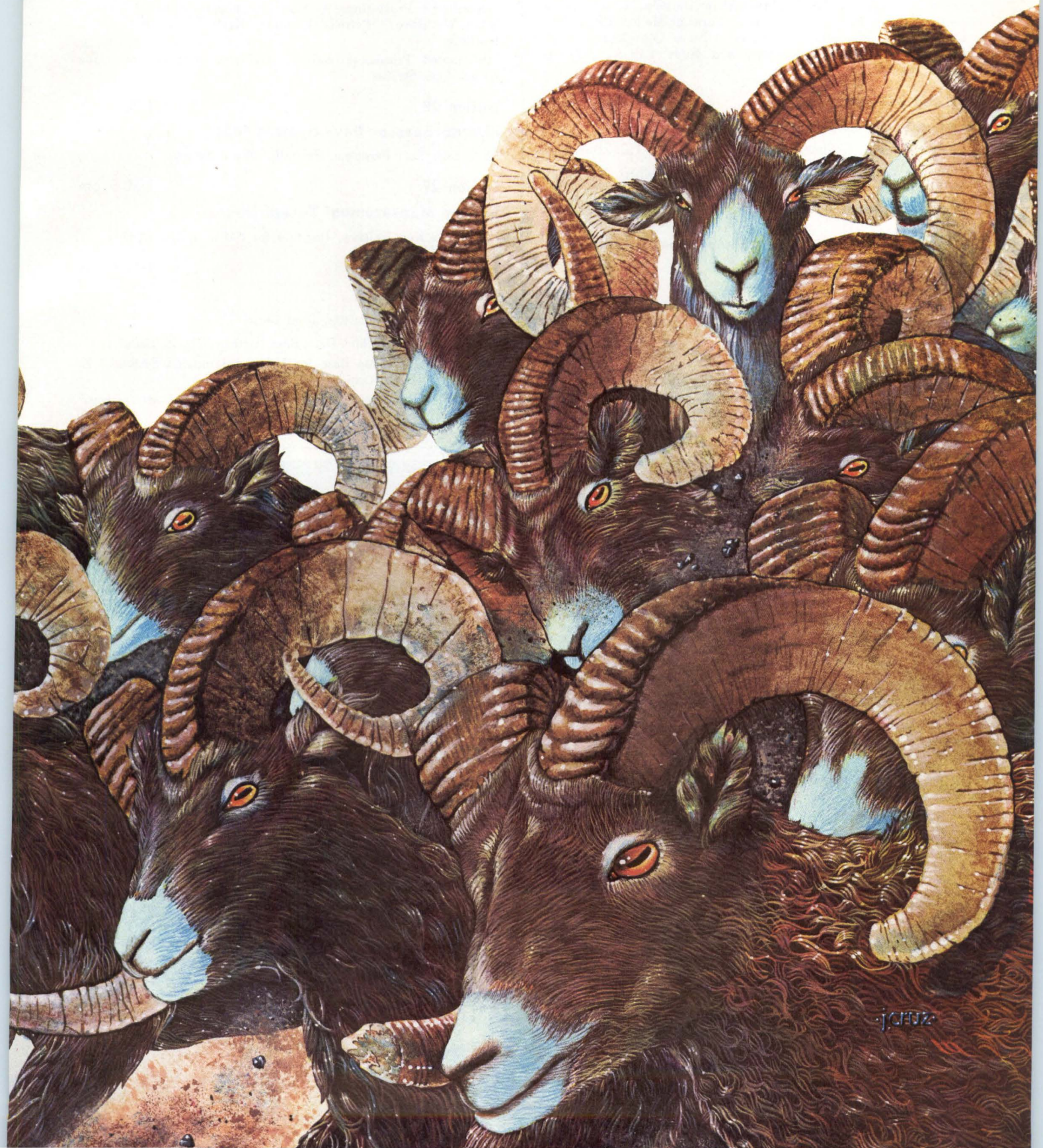
DYNAMIC RAMS.



"The Manager's Role in Economic Modeling—What Should He Know?" Elwood Buffa, University of California, Los Angeles

"A Modeling Prospective," Carl Noble, On Line Decisions

"Corporate Financial Models—Real World," Burt Blewitt, Public Service Electric & Gas

Session 23 9 am-12 noon

New Microprocessor Architectures

Chairman: Bernard Peuto, Zilog, Inc

Panel Members: Forrest Baskett, Los Alamos Scientific Laboratory and Stanford University; Alvin Despain, University of California, Berkeley; L. J. Shustek, Carnegie-Mellon University; Skip Stritter, Motorola Inc; Denis Allison, Consultant; Geene Ogden, Texas Instruments, Inc; and Rudy Langer, National Semiconductor Corp

Session 24 9 am-12 noon

Large-Scale Scientific Computation

Chairman: Jack Worlton, Los Alamos Scientific Laboratory

"Physical Limits on Computer Devices," Dr Robert W. Keyes, IBM Corp

"Computers in the 1980s—And Beyond," Dr Rein Turn, TRW, Inc

"Computational Limits on Scientific Applications," F. W. Bailey, NASA Ames Research Center

Session 25 9 am-12 noon

Microprocessor Developments

Chairman: Peter Alfke

Session 26 9 am-12 noon

Software Development Specificatoins and Requirements

Chairman: Charles R. Vick, Ballistic Missile Defense Advanced Technology Center

Thursday Afternoon

Session 27 1:30-5 pm

Distributed Computing

Chairman: Karl Drexhage, Karl Drexhage Associates

"Consolidated Reporting in a Distributed Environment," Robert S. Drake, Bank of America

"Distributed Processing: A Mature Concept, or Do We Know What We Have?" Patricia Whiting-O'Keefe, Stanford Research Institute

"Distributed Processing and the Corporate Commitment," Joe Reuss, Levi Strauss

Session 28 1:30-5 pm

Microprocessor Development Aids

Chairman: Earl Ferguson, Scientific Micro Systems

Session 29 1:30-5 pm

System Measurement Techniques

Chairman: Ken Kolence, Institute for Software Engineering

Session 30 1:30-5 pm

Data Base Design

Chairman: Stuart Schuster, Intel Corp

"Semantic Integrity and Data Base Systems," D. Z. Badal

"A Longitudinal Data Base for Urban Information Systems," K. Sam and S. Lammugan

"Data Base Processors: Benefits and Architectural Alternatives," Owen H. Bray □

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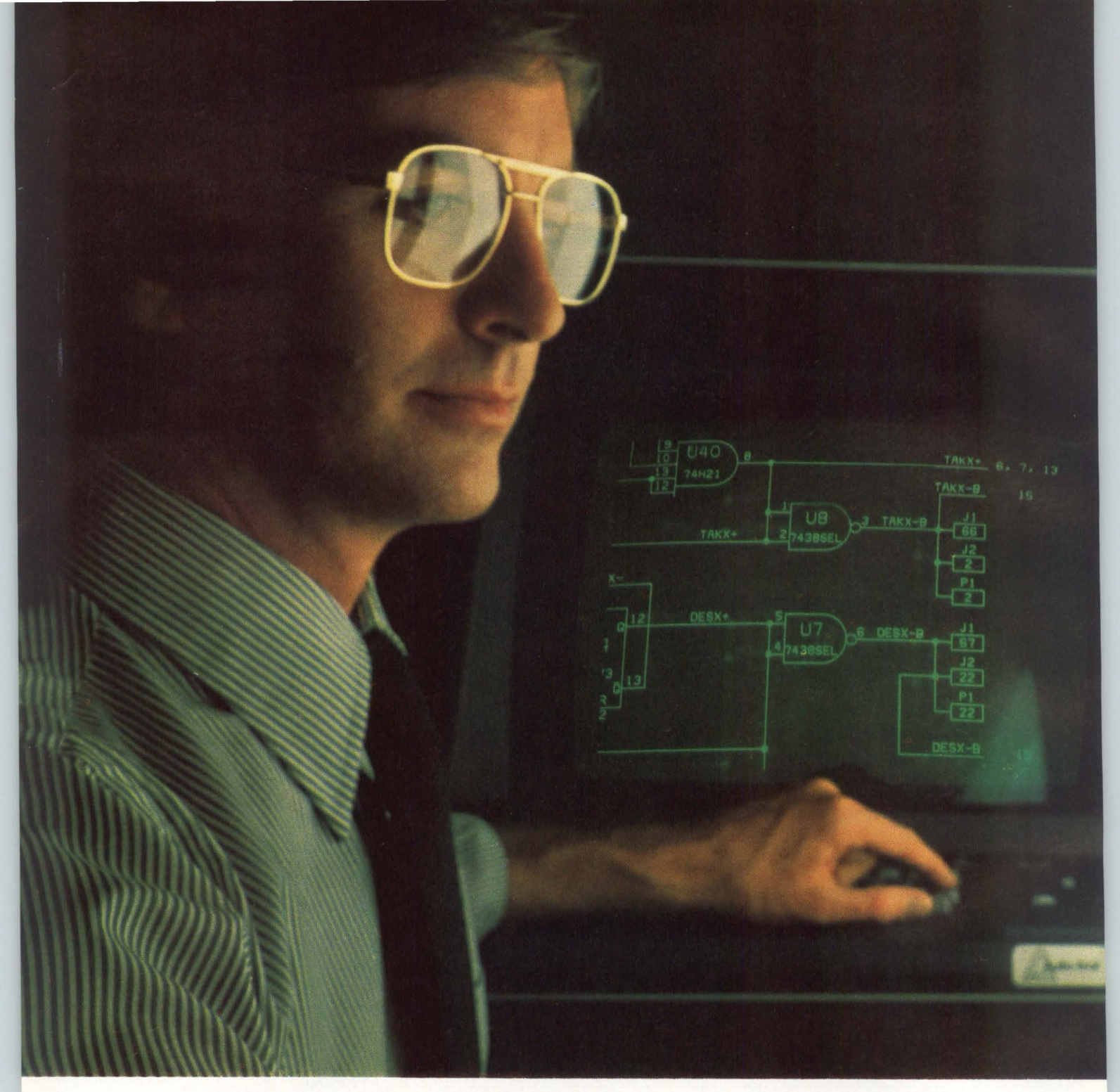

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CIRCLE 42 ON INQUIRY CARD

IEEE International Solid-State Circuits Conference

February 15-17

San Francisco Hilton Hotel
San Francisco, California

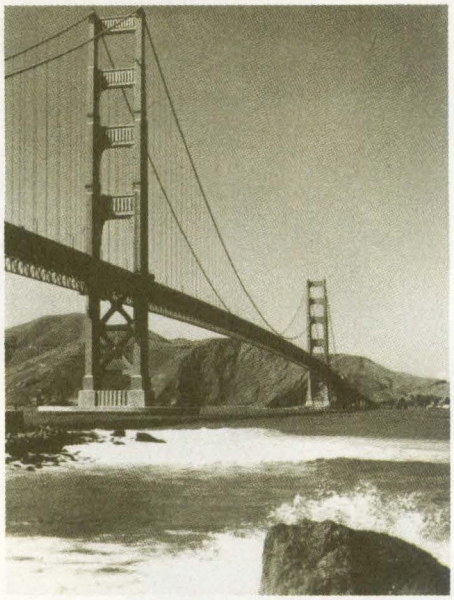


Photo courtesy of San Francisco Convention & Visitors' Bureau

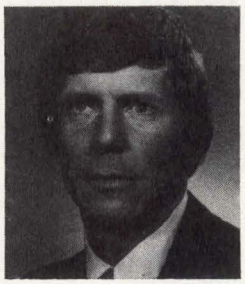
During its silver anniversary celebration in San Francisco, under the counsel of David Hodges, conference chairman, and John Heightley, program chairman, ISSCC 78 will assess current and suggested future technology in solid-state circuitry. Twenty-seven sessions will highlight speakers from Germany, England, Italy, Belgium, Holland, Switzerland, Japan, and the U.S. Those speakers will offer papers in a broad range of subjects that includes digital IC technology, charge-coupled imagers, high speed technology, static and nonvolatile memories, high density memories, and pulse code modulation telecommunications.

Formal opening of the conference, by D. Hodges, University of California, and J. Raper, General Electric Co, will occur in the Continental Ballroom on Wednesday at 1:30 pm. The welcome will include traditional presentation of best-paper awards along with two new awards, the IEEE Cledo Brunetti Award for outstanding contributions in the field of miniaturization in the electronic arts, and the ISSCC Beatrice Winner Award for editorial excellence.

Of special interest will be a keynote address by Dr I. M. Mackintosh, president of a consulting company in England, who will deliver a prognosis on the intercontinental LSI battle. His discussion will include a survey of the strategic, economic, technological, and demographic factors that have affected the worldwide pace and direction in research, development, and design by industry, universities, and government.

The annual informal post-conference get-togethers, when speakers explain design features through operational lab/prototype models, will again afford attendees an opportunity to discuss the papers presented during that day. In addition, subsequent sessions will feature invited talks on the current status and future of magnetic bubbles.

David A. Hodges
Conference Chairman



John D. Heightley
Program Chairman

Informal Discussions

Evening sessions will focus on a wide range of topics and consist of informal discussions with a moderator and panel members. Specifically, the sessions will begin on Wednesday evening with an overview on recent advances in telecommunications and the data acquisition and conversion systems, both key product areas for A-D LSI. Accented will be the questions involved and the problems that arise between MOS and bipolar IIL, as well as technology trends of the future. Further discussion will revolve around fiber optics, including circuit techniques for transmission of digital and analog signals.

Problems with high end microprocessors and an assessment of LSI technology and its impact on advanced system features will be highlighted also. Then, the varied alternative semiconductor technologies as well as conventional bipolar structures will be compared and contrasted, and their merits considered during the final Wednesday evening discussion.

With topics including viability of various design approaches, system applications, testing, specification problems, and reliability, the first Thursday evening session will center around IC CODECs. One discussion will involve how packaging technology influences the performance and cost of current and future computers, with a comparison of alternative packaging designs considered. Accenting approaches to testing and testability of custom LSI, another session will discuss the usefulness of computer aids and the merits of rigorous design philosophies that guarantee testability. The last evening discussion topic will be the urgent need for standardization and better software support in the semiconductor industry.

Registration

Each registrant will receive a copy of the anniversary issue of the annual *Digest of Technical Papers,* which

Designing a measurement and control system takes courage. It can be downright terrifying. Take the case of Design Engineer XG. He innocently listened to the humbuggery of the hooded rascal shown here. Too bad.

The Pip insists that you should be overly concerned with the bits and bytes of your computer. Further, he slyly suggests that if you ignore all this technical trivia, your mind may go into a nucleoid spasm, and even worse—you could lose your job.

Baloney, says Computer Products. Bring PROCOM II into the tussle and the bits, bytes and other ballyhoo will take care of themselves.

PROCOM II is a low-cost microcomputer designed to get computer-directed systems up and running quicker and cheaper than you can imagine.

For more information on how PROCOM II helps you defeat the denizens of destruction and win the measurement and control war, just get in touch with our RTP sales department. We'll send you the whole set of battle plans.

Computer Products, inc.

1400 N.W. 70th Street
Fort Lauderdale, Florida 33309
(305) 974-5500

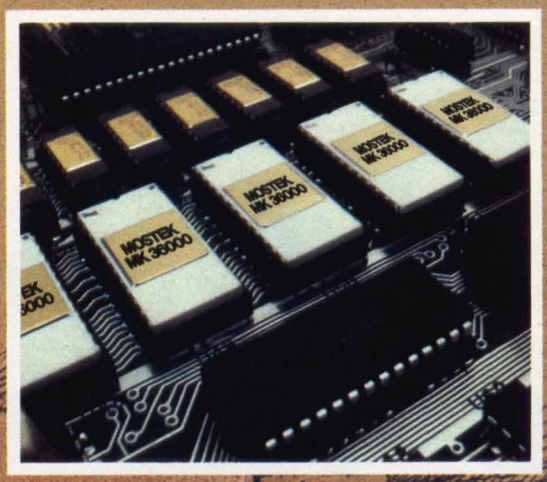
CIRCLE 43 ON INQUIRY CARD

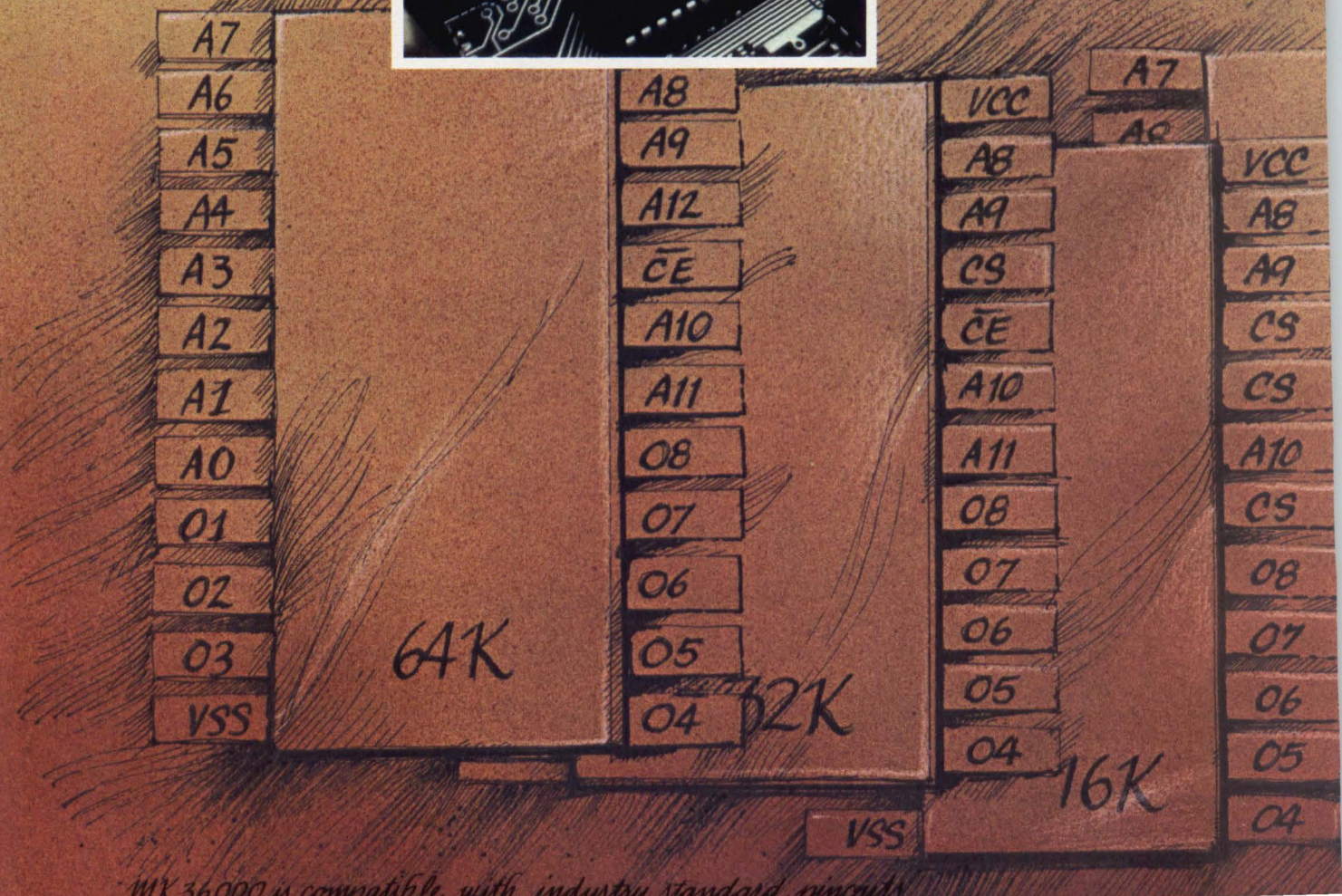
The Pressurized Punctilious Pip.

A fuss-budgeted evildoer who wants to bury you under bits, bytes and buffers.

Mostek's 64K ROM sets new standards for speed and power.

Pin compatibility, from 8K to 64K, means easy system upgrade in density and performance.

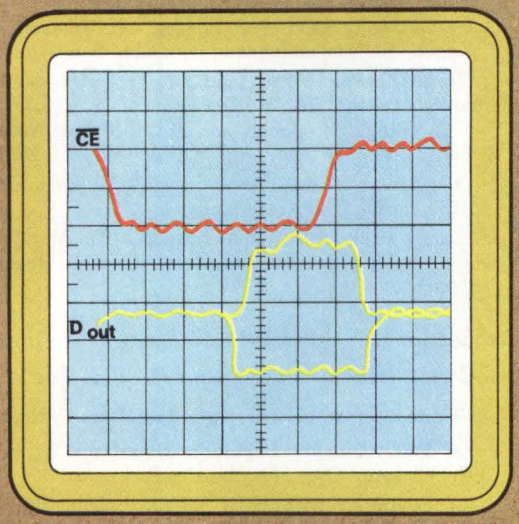




MK 36000 is compatible with industry standard pinouts

Mostek's newest ROM was developed by a design and process team with years of experience in dynamic RAMs. Their goal was to produce the industry's highest density ROM with all the features you expect in Mostek RAMs.

They met that goal with the MK36000 65,536-bit Read-Only Memory. It sets new standards with the industry's highest density, fastest access, and lowest power.



Speed and power. Mostek's MK 36000-4 offers 250 ns access time max! It's ideal for fast microprocessor applications like Mostek's 4MHz Z80, as well as storage for higher level languages. With speeds like this you might expect a sacrifice in power. Not from Mostek. The MK 36000-4 requires only 200 mW active power max. Automatic standby power is just 25 mW typical.

Greater system performance and efficiency. Mostek's ROM family now includes 8K, 16K, and 64K organizations. All are pin-for-pin compatible so you can easily upgrade your existing designs in both density and performance. (With each increase in bit density a chip select input is replaced by the necessary address pin.) The 36000 is pin-compatible with existing EPROMs also allowing upgrades to higher density at much lower costs.

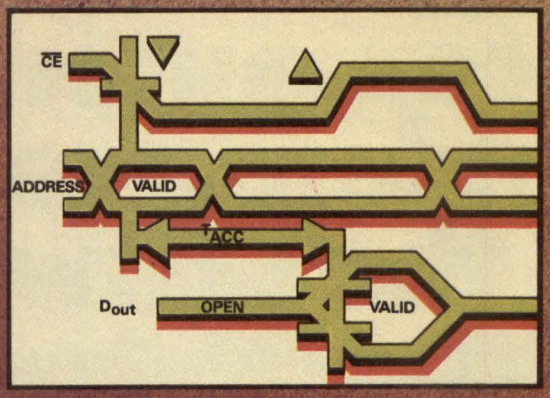
Mostek's Edge-Activated™ design concept provides many other features including +5V only power with ±10% tolerance, on-chip address latches, totally static operation and direct TTL compatibility with common I/O.

In applications with Mostek's Z80 microcomputer and Mostek 4K static RAMs you can activate the entire system with one common timing signal achieving a 75% reduction in device operating power for an automatic standby power mode.

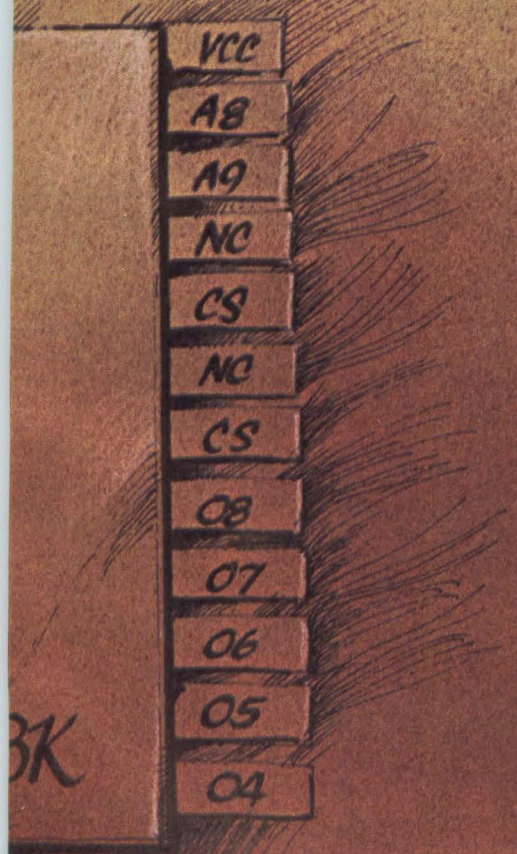
Proven technology for lower cost, greater reliability. The proven technology for high performance and volume production is N-Channel, Silicon Gate MOS. Mostek's years of experience with Poly I™ process allow confident planning of next-generation products like the 36000. Now, Mostek process engineers can quickly move these designs from R&D to full production with proven reliability in millions of circuits.

There's more information on Mostek ROMs. Contact your nearest field sales representative or Mostek Corporation, 1215 W. Crosby Road; Carrollton, Texas 75006, (214) 242-0444. In Europe contact Mostek GmbH.West Germany; Telephone, (0711) 701096

More fast ROMs from Mostek at ISSCC.



MOSTEK



CIRCLE 44 ON INQUIRY CARD

will include a commemorative section with illustrated cameo reports, over 500 diagrams and photos, and 260 pages of edited 800- to 1000-word invited/contributed/keynote condensations. Introductory overview editorials summarizing the contents of day and evening sessions will also be featured. Prices for additional copies are $20 (members), $30 (nonmembers), and $10 (students). Advance registration fees for members are $45 and for nonmembers, $55; at-conference fees are set at $60 and $70, respectively.

Programs with registration forms can be obtained from the IEEE, 345 East 47th St, New York, NY 10017; Philadelphia Section/IEEE, The Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, PA 19104; San Francisco Bay Area Council/IEEE, 701 Welch Rd, Palo Alto, CA 94303; or Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134.

Technical Program Excerpts

Wednesday Morning

Session 1 9-11:45 am Continental Ballroom (4-5)

Digital LSI Technologies

Chairman: H. DeMan, Catholic University, Leuven, Belgium

"Buried Injector Logic: Second Generation I²L Performance," A. A. Yiannoulos, Bell Laboratories

"FET Logic Configuration," E. M. Blaser and D. A. Conrad, IBM Corp

"Dynamic Depletion Mode: An E/D MOSFET Circuit Method," R. W. Knepper, IBM Corp

"Bipolar ICs for Industrial Fiber Optic Data Links," W. Brown, D. Hanson, and T. Hornak, Hewlett-Packard Labs

"Punch-Through Cell for Dense Bipolar ROMs," J. Lohstroh and A. Slob, Phillips Research Laboratories

"Punch-Through MOSFET for High Speed Logic," T. Nakamura, M. Yamamoto, H. Ishikawa, and M. Shinoda, Fujitsu Laboratories, Japan

Session 2 9-11:45 am Continental Ballroom (6)

Advances in Charge-Coupled Imagers

Chairman: W. F. Kosonocky, RCA Laboratories

"A Zigzag-Transfer CCD Imager," H. Matsumoto, T. Ando, Y. Kanoh, S. Yamanaka, and S. Ochi, Sony Corp, Japan

"Buried-Channel CCD Imaging Arrays with Tin-Oxide Transparent Gates," D. H. McCann, A. P. Turley, J. M. Walker, J. A. Hall, R. A. Tracy, and M. H. White, Westinghouse Electric Corp; and L. Thompson, NASA Goddard Space Flight Center

"Resistive Gate CTD Area Sensor," H. Heijns, Philips Research Laboratories, The Netherlands

"Large High-Density CID Imagers," D. M. Brown, M. Ghezzo, and P. L. Sargent, General Electric Research/Development Center

Session 3 9-11:45 am Imperial Ballroom

Compatible Analog and Digital Technology

Chairman: J. A. Schoeff, Advanced Micro Devices

"A Fully Integrated Motion Detector," W. S. Gontowski and R. W. Lutz, Sprague Electric Co

"A Controller with High Speed I²L and High Voltage Analog Circuits," T. Okabe, T. Watanabe, and M. Nagata, Hitachi Central Research Laboratories, Japan

"A Monolithic Speed Control System for Automotive Applications," R. B. Jarrett, Motorola, Inc

"A CMOS Reference Voltage Source," Y. P. Tsividis, Columbia University; R. W. Ulmer, Motorola, Inc

"An n-MOS Voltage Reference," R. A. Blauschild, P. Tucci, D. Muller, and R. G. Meyer, Signetics Corp

Wednesday Afternoon

Session 5 2:15-3 pm Continental Ballroom

Keynote Address

Chairman: D. A. Hodges, University of California

"A Prognosis of the Intercontinental LSI Battle," I. M. Mackintosh, Mackintosh Consultants Co, Ltd, England

Session 6 3:15-6 pm Continental Ballroom (4-5)

High Speed Technologies

Chairman: P. A. Buffet, Digital Equipment Corp

"Model for a 15-ns 16k RAM with Josephson Junctions," P. Gueret, W. Kotyczka, Th. O. Mohr, A. Moser, A. Oosenbrug, and P. Wolf, IBM Research Laboratory, Switzerland

"Sub-100-ps Experimental Josephson Interferometer Logic," M. Klein, D. J. Herrell, and A. Davidson, IBM Research Center

"A 920-Gate Masterslice," T. Nakano, O. Tomisawa, K. Anami, M. Ohmori, I. Ohkura, and M. Nakaya, Mitsubishi Electric Corp, Japan

"A Monolithic Serial Multiplier," D. C. Rollenhagen and N. R. Wild, General Electric Co

"Low Power GaAs Digital ICs Using Schottky Diode-FET Logic," R. C. Eden, B. M. Welch, and R. Zucca, Rockwell International

Session 8 3:15-6 pm Imperial Ballroom

Fully Integrated Analog Filters

Chairman: A. S. Sedra, University of Toronto, Canada

"High Order Monolithic Analog Filters Using Bipolar/JFET Technology," K. S. Tan and P. R. Gray, University of California

"Fully-Integrated High Order n-MOS Sampled Data Ladder Filters," D. J. Allstot, R. W. Brodersen, and P. R. Gray, University of California

"Fully-Integrated CTD Filter with Output Sensing," G. P. Weckler and H. Tseng, Reticon Corp; and R. W. Brodersen, University of California

"A Fully-Integrated 32-Point Chirp Z-Transform IC," W. L. Eversole, D. J. Mayer, P. W. Bosshart, M. deWit, C. R. Hewes, and D. D. Buss, Texas Instruments, Inc

"An Integrated Dual-Tone Multi-frequency Decoder," M. J. Callahan, Jr and H. L. Davis, Mostek Corp

Wednesday Evening

WE 1 8 pm Continental Ballroom (4)

The Future of Analog/Digital LSI

Moderator: A. B. Grebene, Exar Integrated Systems, Inc

Panel Members: A. P. Brokaw, Analog Devices Semiconductor, Inc; H. DeMan, Catholic University of Leuven, Belgium; P. R. Gray, University of California; M. J. Callahan, Jr, Mostek Corp; B. Gilbert, Tektronix; and J. A. Schoeff, Advanced Micro Devices

WE 2 8 pm Continental Ballroom (5)

Fiber Optic Links— A New Application for Solid-State Circuits

Moderator: T. Hornak, Hewlett-Packard Laboratories

Panel Members: J. R. Biard, Spectronics, Inc; J. E. Goell, ITT; W. H. Hackett, Jr, Bell Laboratories; D. Hanson, Hewlett-Packard Co; F. R. McDevitt, Harris Corp; and J. Straus, Bell Northern Research, Ltd, Canada

---

THE GUTS OF A WINNER:

Not just the first 24 MB disk drive —but every inch a champion.

Leading the field in the stretch to 24 MB disk storage: Pertec's D3400 Series. The first cartridge disk drives to double traditional 3-12 MB capacities... without handicapping OEMs.

Meaning: we're not about to boost your data payload by burdening you with expensive penalties—in hard currency, or harder work. Like controller redesign. Like interface snafu's. Like requiring special pre-recorded media. No way.

Familiar technology. D3400 drives fit neatly into Pertec's most advanced disk product line, D3000—as members of a fast-access family you've been living with right along. And completely interface compatible with standard industry configurations. Ours *and* other manufacturers.

One unit: four platters. Available in front or top load models, D3400 expands to 24 MB through 3 fixed and 1 standard media-interchangeable cartridges. All with independent write protection.

Easy installation and maintenance. This 24 MB disk drive looks just like any 3-12 MB unit: same size, same rack space. And the same exclusive Pertec hinge-mounting of PCBAs—simplifies access to the electronics, reducing operational and service costs.

Champs in reliability. Each D3400 cartridge disk drive has to meet the same tough criteria—in production and on-line—that protects every Pertec product, and every OEM investment.

In short, we're producing a bigger storage appetite, but assuring you the same pre-tested, high performance, field-proven drives that have made Pertec the odds-on favorite with OEMs for years.

No-compromise service. One out of five people in Pertec Computer Corporation is a full-time contributor to the most comprehensive OEM-support organization in the field today.

Sales service that expands and cost-optimizes your configuration options: we'll help you target in on the D3000 system that precisely meets your specs—pick from 3 MB to 24 MB on cartridge disk. And the same support goes for our fixed and flexible disk drives—just ask.

Field service facilities are strategically located throughout the world. Trouble-shooting is as close as our toll-free 800 line—open for business around the clock.

And it's that kind of commitment that ranks us today as the world's largest independent manufacturer of peripheral equipment.

☐ Please rush full information on Pertec's 24 MB cartridge disk drives.
☐ Send pricing information based on RFQ below, without obligation or cost.

Request for Quote

Cartridge Type	Capacity (Megabytes)	Platter Configuration	Bit Density (bpi)	Speed (rpm)	Model Number	Quantity Required	Date Wanted	Send Specs Only
5440 Top Load	24.0	QUAD	2200	1500	D3461			
				2400	D3462			
2315 Front Load	24.0	QUAD	2200	1500	D3481			
				2400	D3482			

Name_____

Title_____ Phone_____ Ext_____

Please attach coupon/RFQ to company letterhead and return to Pertec, 9600 Irondale Avenue, Chatsworth, CA 91311.

For immediate requirements, call your nearest Pertec regional sales office: Los Angeles (213) 996-1333. Ann Arbor, Michigan (313) 668-7980. Hudson, New Hampshire (603) 883-2100. England (Reading) 582115.

PCC PERTEC
a division of Pertec Computer Corporation

CIRCLE 46 ON INQUIRY CARD

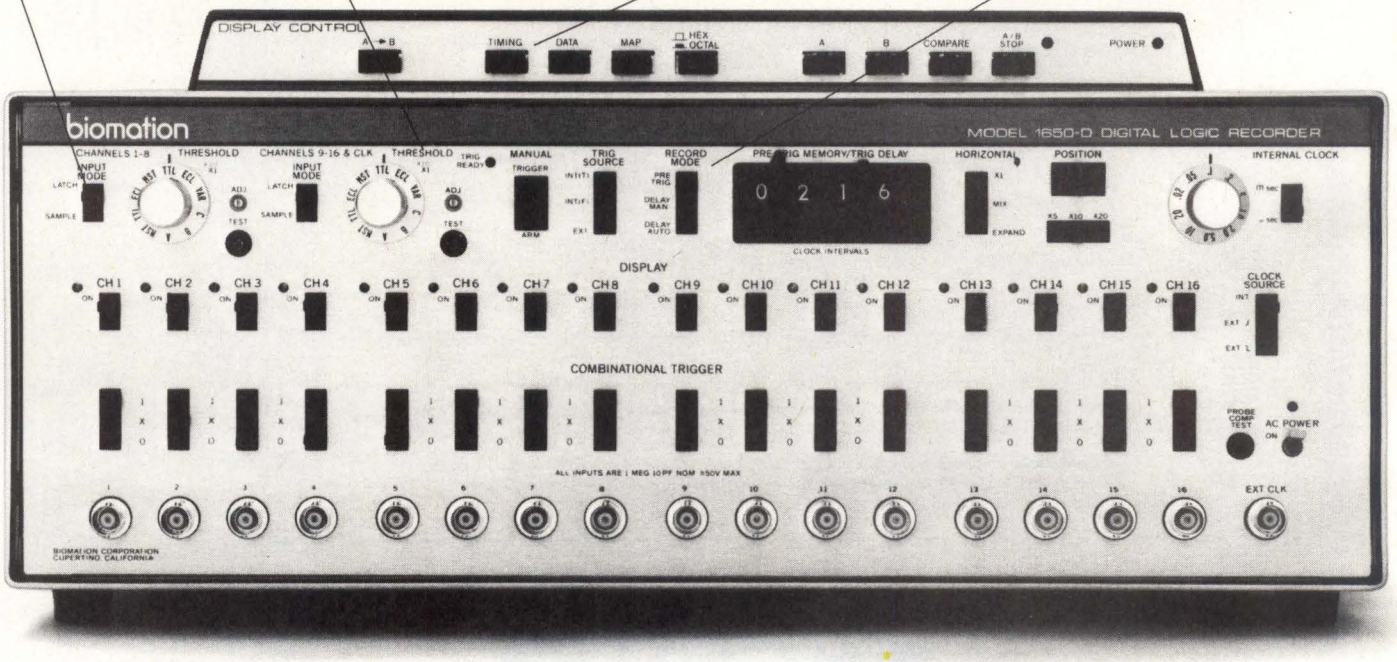
How 36 trigger points can simplify analysis of your microprocessor-based systems.

5ns Glitch Capture.
Latch mode for glitch detection, or sample mode, can be independently selected for channels 1-8 and 9-16. Wide bandwidth BNC input allows capture of pulses as narrow as 5ns.

Mixed Logic Thresholds.
Select one threshold voltage for channels 1-8, another for 9-16. Dial in ECL, TTL, MST, any of three user-preset values or continuously variable level.

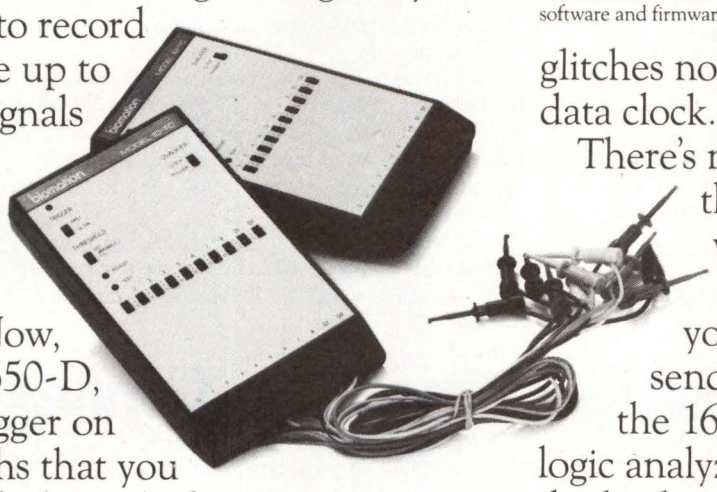
Display Control. Select timing diagram, data domain logic state display or map mode dot pattern of system operation, using the accessory 116 Display Control. Memory feature permits comparison of current and stored system characteristics.

Precise Memory Control.
Pretrigger recording enables you to split the 512-word memory to capture data on both sides of the trigger event. Or, with Delay Mode, start of recording can be delayed as long as 9999 clock intervals after the trigger.

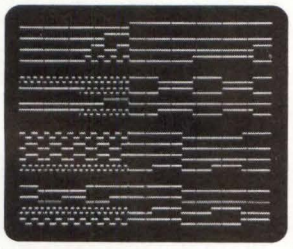


Designing a microprocessor-based system? There's no better way to get a precise, detailed look at both 8-bit and 16-bit microprocessor system operation than our 16-channel, 50 MHz logic analyzer.

Plug in two of our 10-TC active probe pods and the 1650-D's combinational trigger capability is expanded to trigger on words up to 36 bits long. That gives you the power to record and analyze up to 16 digital signals triggering from up to 20 additional locations. Now, with the 1650-D, you can trigger on word lengths that you just couldn't detect before.

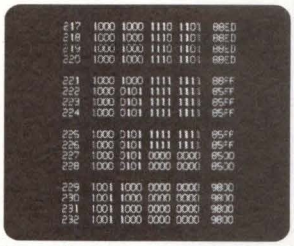


Versatility is the key to the 1650-D's popularity with designers working on microprocessor system development, instrumentation interfacing or analysis of real-time digital circuits. With the 116 Display Control, the 1650-D gives you the capability to analyze both timing and logic state displays. That's the key to simplified hardware/software debugging and integration.



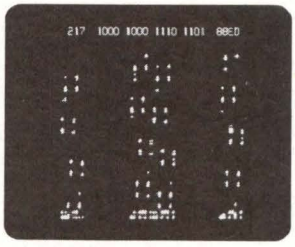
Time Domain. Timing diagram lets you see the sequential and simultaneous relationship between digital signals, to simplify hardware troubleshooting.

A Latch Mode on the input signal enables the 1650-D to detect and record glitches or pulses as narrow as 5ns — vital information when troubleshooting the operation of digital circuits. Or, for data analysis, Sample Mode ignores synchronous glitches not coincident with the data clock.



Data Domain. Display logic states (1's and 0's) with hex or octal translation. That's essential information for troubleshooting software and firmware.

There's not space here to give you all the details on how our 1650-D, with 10-TC probe pods and 36-bit trigger, can simplify your task. But we'll gladly send you detailed information on the 1650-D and our entire line of logic analyzers, from the budget-priced 920-D to the ultra-fast, 200 MHz 8200. And, at your convenience, we'll arrange a demonstration of Biomation's logic analyzers in your lab, capturing and displaying the data you work with.



Map Mode. Each digital word can be translated into a singularly positioned dot in this graphic representation of recorded data. Especially useful for spotting illogical or illegal memory addresses.

Write, call or use the reader service card. Biomation, 10411 Bubb Road, Cupertino, CA 95014. (408) 255-9500. TWX: 910-338-0226.

biomation

WE 3 8 pm Continental Ballroom (6)

High End Microprocessors

Moderator: W. W. Lattin, Intel Corp

Panel Members: L. Thomas, Bell Laboratories; C. Mead, California Institute of Technology; S. Teicher, Digital Equipment Corp; C. Crook, Motorola, Inc; L. Loop, Hewlett-Packard Co; and W. Pohlman, Intel Corp

WE 5 8 pm Imperial Ballroom

Competing High Speed/High Density Technologies

Moderator: L. M. Terman, IBM Corp

Panel Members: T. J. Rodgers, AMI; P. W. J. Verhofstadt, Fairchild Camera and Instrument Corp; R. D. Pashley, Intel Corp; J. Borel, CEN/LETI, France; T. Nakano, Mitsubishi Electric Corp, Japan; A. G. Dingwell, RCA; W. G. Howard, Motorola, Inc; and S. K. Wiedmann, IBM Corp

Thursday Morning

Session 9 9 am-12:15 pm Continental Ballroom (4-5)

Static and Nonvolatile Memories

Chairman: K. D. Wise, University of Michigan

"A High Speed, Low Power 4096 x 1-Bit Bipolar RAM," A. Hotta, Y. Kato, K. Yamaguchi, N. Honma, and M. Inadachi, Hitachi, Ltd, Japan

"A 4k Static Bipolar TTL RAM," K. Okada, K. Aomura, J. Nokubo, and H. Shiba, Nippon Electric Co, Ltd

"A Four-Device Bipolar Memory Cell," R. A. Heald, Signetics Corp

"A 1k x 8-Bit 5-V-Only Static RAM," G. S. Leach, J. M. Hartman, K. L. Clark, and T. R. O'Connell, EMM-SEMI, Inc

"A 4k CMOS Erasable p/ROM," Y. F. Chan, Intersil, Inc

"A 256-Bit Nonvolatile Static RAM," E. Harari, L. Schmitz, B. Troutman, and S. T. Wang, Hughes Aircraft Co

Session 11 9 am-12:15 pm Imperial Ballroom

A-D and D-A Conversion Techniques

Chairman: W. J. Lillis, Motorola, Inc

"A Microprocessor-Compatible High Speed 8-Bit DAC," J. A. Schoeff, Advanced Micro Devices

"A Single-Chip C^2MOS A-D Converter for Microprocessor Systems," E. Masuda, T. Iida, C. Sato, Y. Suzuki, Y. Agawa, and T. Shima, Tokyo Shibaura Electric Co, Ltd, Japan

"A Precision Voltage-to-Frequency Converter," J. C. Schmoock, Raytheon Co

"A 10-Bit Monolithic Tracking A-D Converter," P. H. Saul and J. A. Jenkins, Ferranti, Ltd, England

"A Monolithic 10-Bit A-D Using I^2L and LWT Thin-Film Resistors," A. P. Brokaw, Analog Devices Semiconductor, Inc

Thursday Afternoon

Session 12 1:30-5 pm Continental Ballroom (4-5)

High Density Memories

Chairman: V. A. Dhaka, Xerox Corp

"Magnetic Bubbles—Status and Future," E. W. Pugh, IBM Research Center

"A 64k-Bit MOS RAM," H. Yoshimura, M. Hirai, T. Asaoka, and H. Toyoda, Nippon Tel-Tel Public Corp, Japan

"A 64k-Bit CCD Memory," R. C. Varshney and K. Venkateswaran, Fairchild Camera and Instrument Corp

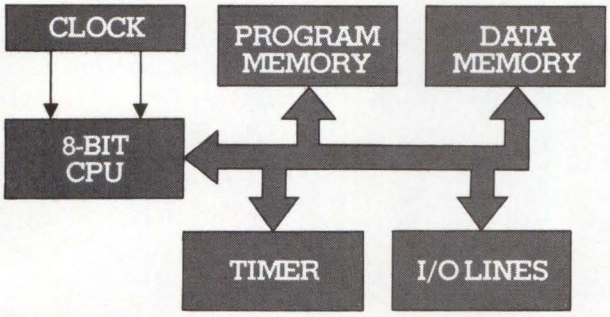
"A 100-ns 150-mW 64k-Bit ROM," D. R. Wilson and P. R. Schroeder, Mostek Corp

"A 16k x 1 I^2L Dynamic RAM," J. M. Early, P. M. Quinn, and T. A. Longo, Fairchild Camera and Instrument Corp

"VMOS Dynamic RAM," K. Hoffmann, R. Losehand, and K. Zapf, Siemens AG, Germany

Introducing the first Intelligent keyboard.

It thinks like you do.



Designing a full-function keyboard for your system used to have a major problem. A full-function price.

MICRO SWITCH has changed all that with the intelligent keyboard. It's the first microcomputer-based keyboard. Ever.

Which means when you equip it with virtually every function you can think of, it still comes in for the price of a simple encoded keyboard. Because all the functions that used to require extra components are now available on a single microcomputer chip.

Besides traditional encoder functions, the chip can handle many others, such as parallel or serial data, multi-character storage and tri-stated outputs for direct data bus compatibility without using expensive I/O ports.

The intelligent keyboard can perform more functions more efficiently because less hardware is needed. You get lower total system cost. Pin for pin compatible EPROM for faster design turnaround. Plus greater reliability since there are fewer components.

Just let us know what your particular needs are. And through MICRO SWITCH Value Engineering we'll work with you closely to create a cost effective solution that interfaces with your total system.

For more information about the intelligent keyboard, call 815/235-6600. It could be the smartest call you've ever made.

MICRO SWITCH

FREEPORT, ILLINOIS 61032

A DIVISION OF HONEYWELL

In Europe MICRO SWITCH has keyboard application engineers in Germany, England, France and Sweden.

Circle 52 for data.

After you've checked double-sided floppy, the best-designed.

Introducing the simple, versatile MFE 700/750.

We took a whole new look at floppy disc technology. And came up with a whole new kind of flexible disc drive.

The MFE 700/750 is the smallest full-sized floppy around, which gives you extra design flexibility.

And because we designed from scratch — not from an existing model — we were able to provide state-of-the-art features throughout. For example:

Our floppy uses a fast, precise HELI-BAND™ positioning system instead of the less-accurate lead screw.

In addition to our AC motor, we offer a unique brushless DC motor which cuts power consumption in half and won't add to your heat problem.

Our twin ceramic heads act as nearly frictionless load pads. They actually help extend media life.

Our IBM compatibility is true compatibility, including track 43 write-current switching, tunnel erase for sharper trim and less fringing, and a data separator that can handle either a missing-clock or a non-missing-clock scheme.

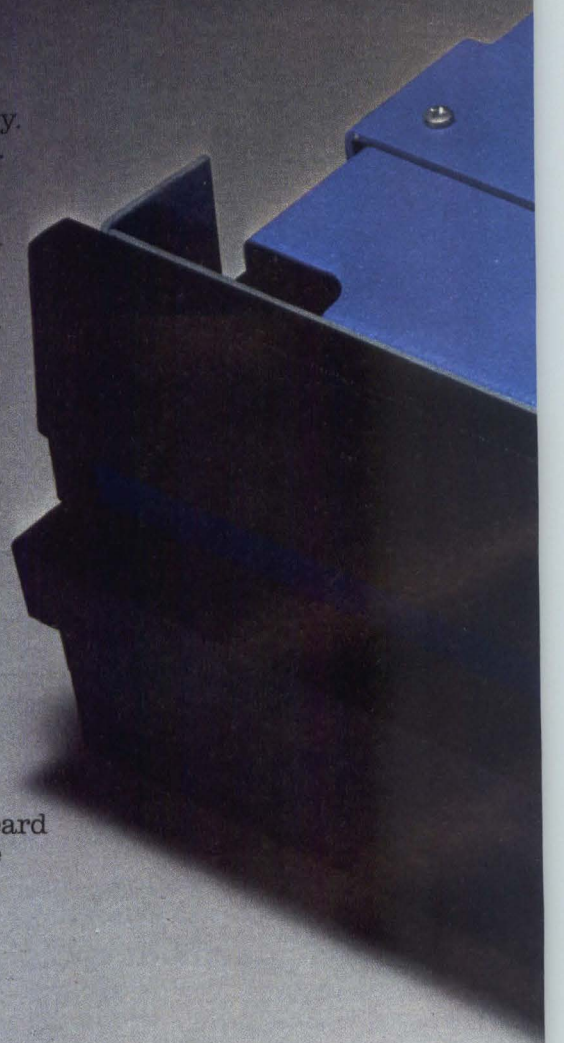
Standard features include data transfer rates of 250/500K bits/sec. and a packing density of 3400/6800bpi. And our standard option list is the longest in the industry. We can tailor a unit to your exact needs.

Naturally, we offer single-sided models, too.

Once you've talked to the company everybody's heard of, talk to us. We'll show you why the best design is more important than the biggest name.

For details, contact MFE, Keewaydin Drive, Salem, New Hampshire 03079, Tel. 603-893-1921/TWX 710-366-1887/TELEX 94-7477.

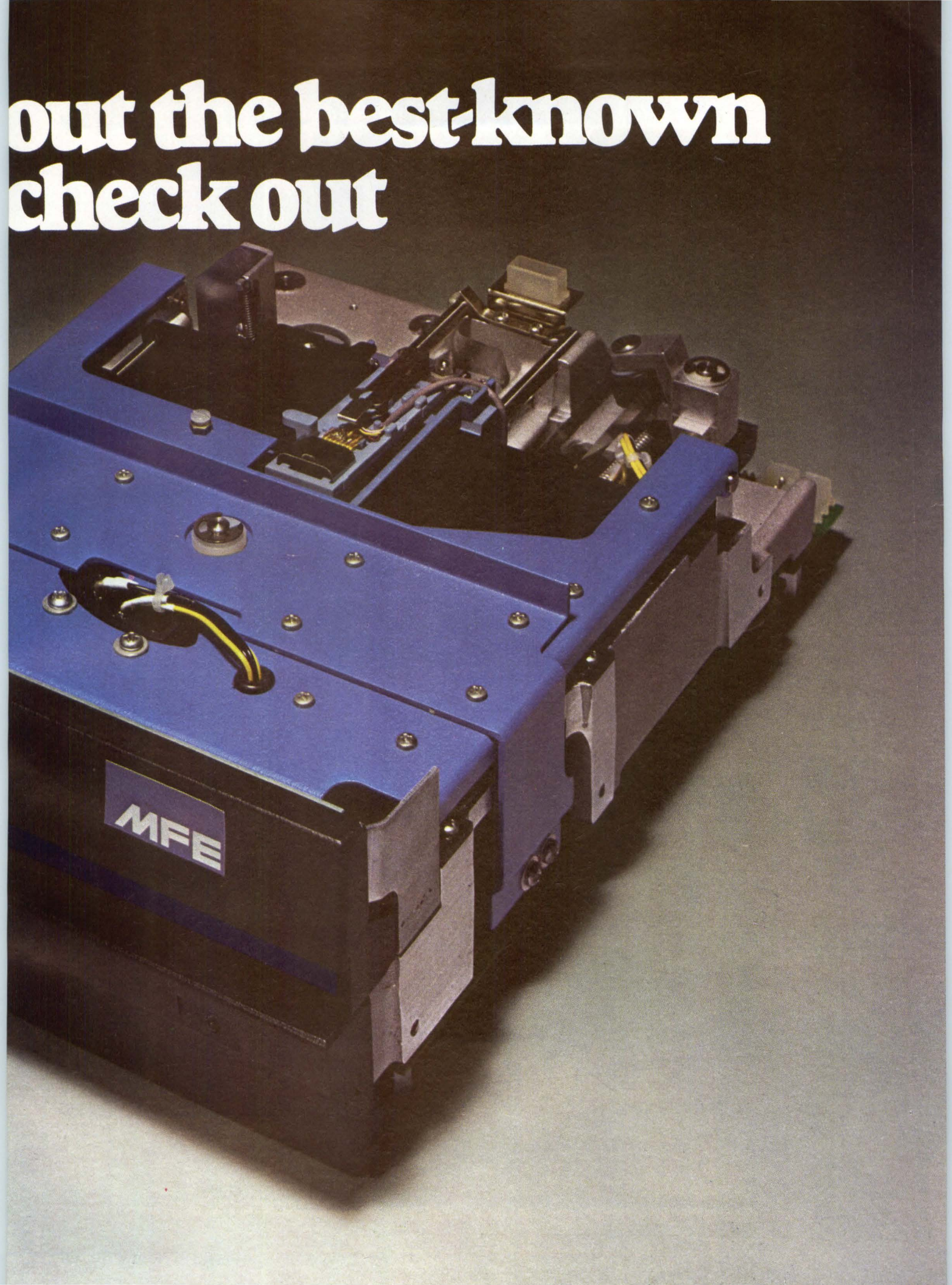
Europe: MFE Products SA, Vevey, Switzerland, Tel. 021 52.80.40/TELEX 26238.



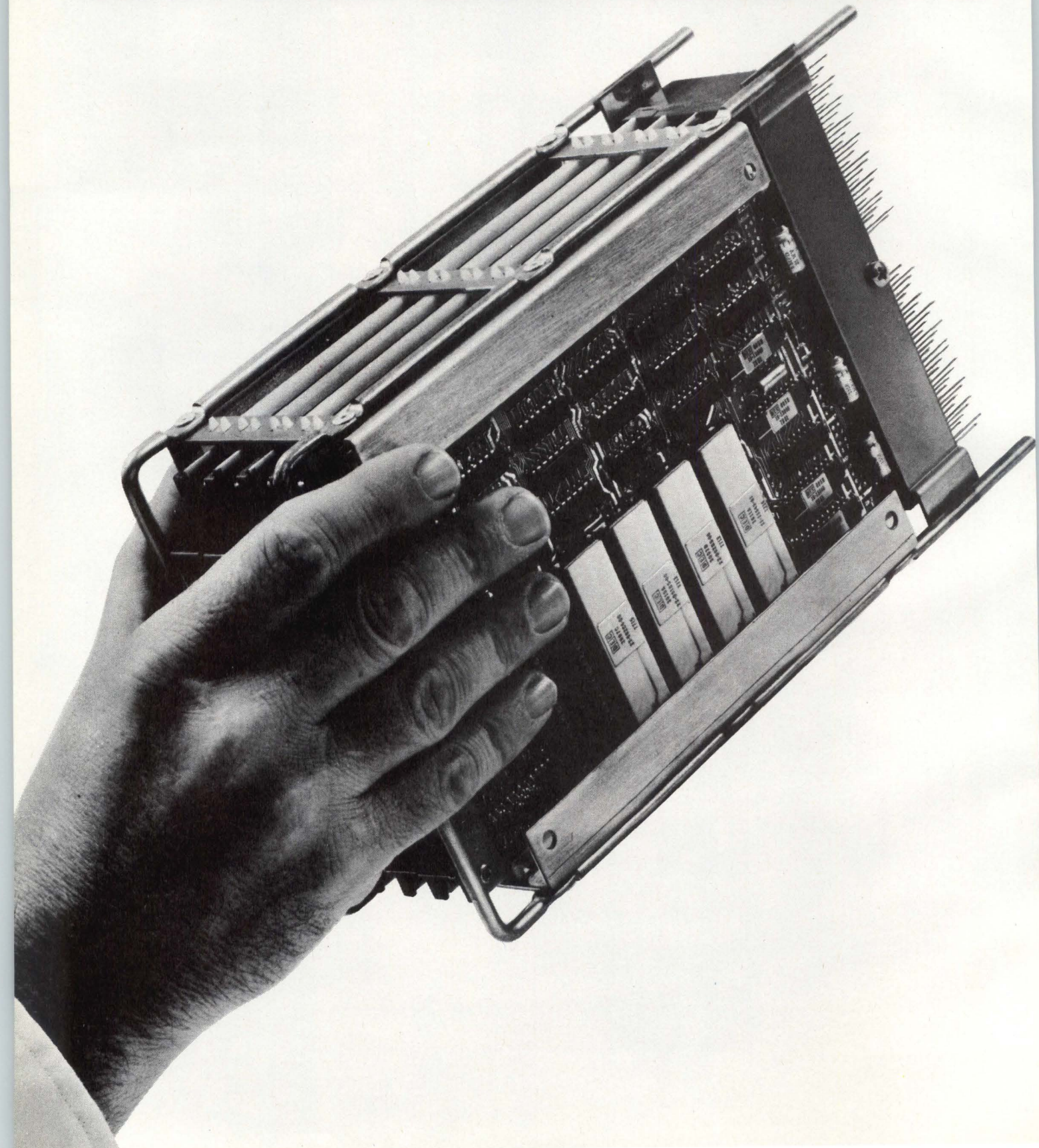
MFE

CIRCLE 53 ON INQUIRY CARD

out the best-known check out



THE WORLD'S MOST POWERFUL 16-BIT MICROCOMPUTER HAS A WHOLE NEW DIMENSION.



Introducing the LSI-11/2.

We've divided our LSI-11 board down the middle, so that CPU and memory are on separate, half-sized boards. What this gives you is a greatly improved form factor, for a new range of design flexibility.

And size is just the start.

Your cost savings can be up to 40%, depending on configuration. And power consumption has been lowered, too.

We're also extending our half-size format to a whole new family of microcomputer options, including memories and interfaces.

Imagine: With just two 5"X 8½" boards in our new microbackplane, you can have a 16-bit system with up to 32K words of RAM, and room left over for your own electronics. That's a 67% reduction in space. And all for less than $1650*.

Naturally, our entire half-size family is compatible with our previous products, to expand your options even further.

The LSI-11/2.

Full PDP-11 power—backed by over 50,000 installations—at a price and size that are both easier to handle.

To explore the possibilities, call toll-free 800-225-9220 (in Mass. 617-481-7400, Ext. 5144), or write Digital Equipment Corporation, One Iron Way, Marlborough, MA 01752.

*Quantity 50

digital
COMPONENTS
GROUP

CIRCLE 54 ON INQUIRY CARD

Session 14 1:30-5 pm Imperial Ballroom

Per-Channel CODECs for PCM Telecommunications

Chairman: G. L. Baldwin, Bell Laboratories

"A Two-Chip PCM CODEC for Per-Channel Applications," J. Cecil, E. Chow, J. Flink, and J. Solomon, National Semiconductor Corp; T. Svensson, Ellemtel, Sweden; and G. Svalla, North Electric Co

"A Single-Chip n-MOS PCM CODEC for Voice," J. Huggins, M. Hoff, and B. Warren, Intel Corp

"A Two-Chip CMOS CODEC," G. F. Landsburg, Siliconix, Inc; and G. Smarandoiu, ICCE, Romania

"A PCM Voice CODEC with Onchip Filters," J. T. Caves, C. H. Chan, S. D. Rosenbaum, L. Sellers, and J. Terry, Bell-Northern Research, Ltd, Canada

"An Integrated PCM Encoder Using Interpolation," J. L. Henry and B. A. Wooley, Bell Laboratories

"A Companding D-A Converter for a Dual-Channel PCM CODEC," E. Pfrenger, P. Picard, and F. von Sichart, Siemens AG, Germany

Thursday Evening

THE 6 8 pm Continental Ballroom (4)

Integrated Circuits for PCM Telecommunications

Moderator: J. E. Solomon, National Semiconductor Corp

Panel Members: C. N. Berglund, Bell-Northern Research, Ltd, Canada; J. Kasson, Rolm Corp; G. Landsburg, Siliconix, Inc; B. Warren, Intel Corp; H. Lie, Bell Laboratories; S. Patroda, Wescom, Inc; and K. Goser, Siemens AG, Germany

THE 7 8 pm Continental Ballroom (5)

Packaging for High Performance Computers

Moderator: W. E. Harding, IBM Corp

Panel Members: R. C. Doane, Digital Equipment Corp; E. A. Wilson, Honeywell Information Systems, Inc; L. C. Wu, Amdahl Corp; A. J. Blodgett, Jr, IBM Corp; and S. S. Roy, International Computers, Ltd, England

THE 8 8 pm Continental Ballroom (6)

Aids to Developing Testable Custom ICs

Moderator: D. M. Caughey, Bell-Northern Research, Ltd, Canada

Panel Members: K. Andres, Hewlett-Packard Co; A. Feller, RCA Corp; J. G. M. Klomp, N. V. Philips, The Netherlands; E. Kozemchak, Bell Laboratories; R. Kusik, Digital Equipment Corp; J. J. Thomas, Digitest Corp; and T. Williams, IBM Corp

THE 10 8 pm Imperial Ballroom

Single-Chip Microcomputers and Their Applications

Moderator: B. T. Murphy, Bell Laboratories

Panel Members: T. A. Longo, Fairchild Camera and Instrument Corp; J. Cyprus, Texas Instruments, Inc; A. Osborne, Adam Osborne and Associates; R. B. Rubinstein, Intel Corp; and J. C. Murphy, Electronic Engineering Co

Friday Morning

Session 15 9 am-12:15 pm Continental Ballroom (4-5)

LSI Applications

Chairman: P. Verhofstadt, Fairchild Camera and Instrument Corp

"E^2-p/ROM Based TV Synthesizer," G. Ferla, V. Daniele, and F. Berenga, SGS-ATES Electronic Components, Italy; and W. Minner, I. Haraszti, and P. Sieber, Telefunken AEG, Germany

"Molybdenum Gate MOS LSI for FM/AM Digital Frequency Synthesizer Receiver," T. Ohgishi, T. Akiyama, and N. Enomoto, Sanyo Electric Co, Ltd, Japan

"High Speed n-MOS Circuits for ROM Accumulator and Multiplier-Type Digital Filters," H. DeMan, C. Vandenbulcke, and M. Van Cappelen, Catholic University of Leuven, Belgium

"A Capacitive Keyboard Interface Chip," G. Katz, L. Baker, and G. Tu, Xerox Corp

"A Single-Chip Sequential Logic Element," R. C. Cline, Signetics Corp

"A High Speed n-MOS/CMOS Single-Chip 16-Bit Microprocessor," M. Suzuki, K. Matsumoto, E. Sugimoto, K. Takemae, and H. Yamamoto, Nippon Electric Co, Japan

Session 16 9 am-12:15 pm Continental Ballroom (6)

LSI Design, Testing, and Interfacing

Chairman: R. C. Joy, IBM Corp

"CAD VLSI Design Techniques and Microprocessor Application," A. Feller, S. E. Ozga, and T. J. Lombardi, RCA Advanced Technology Laboratories

"Pseudo Statistical Analysis of LSI Circuits," F. Y. Chang, IBM Corp

"LSI Chip Design for Testability," S. DasGupta, E. B. Eichelberger, and T. W. Williams, IBM Corp

"Onchip Monitors for System Fault Isolation," F. P. D'Ambra, M. A. Menezes, H. H. Muller, H. Stopper, and R. C. Yuen, Burroughs Corp

"A Miniature Integrated Circuit Accelerometer," L. M. Roylance, Hewlett-Packard Laboratories; and J. B. Angell, Stanford University

"A MOS-Controlled Triac Device," B. W. Scharf and J. D. Plummer, Stanford University □

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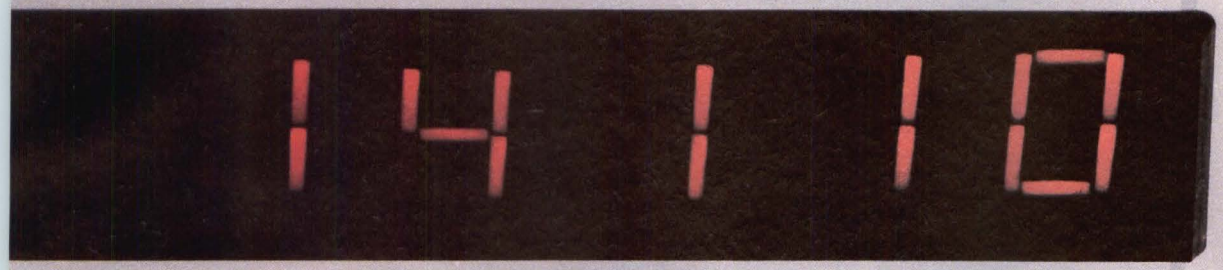

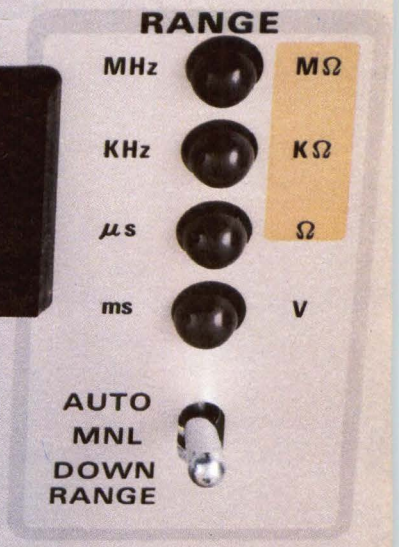

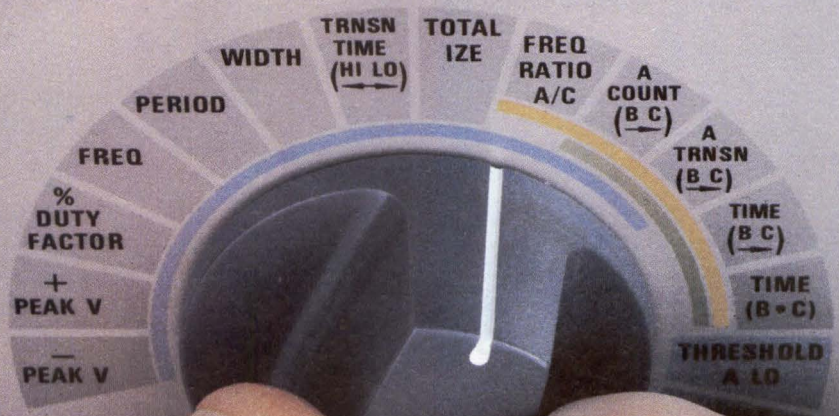

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COURSE OUTLINE. ***First Session (Sunday).*** Introduction to and history of microcomputers. Assignment of laboratory breadboarding station and microcomputer. Distribution of course literature.

Second Session. Review of basic digital electronic and microcomputer interfacing/programming concepts. Experiments involving the breadboarding of interface circuits to the laboratory 8080A microcomputer.

Third Session. Experiments and lectures on interrupt servicing and programmable interface chips, including the 8255 programmable peripheral interface, the 8253 interval timer, and the 8251 USART.

Fourth Session. Assembly language subroutines for the 8080A/8085. Multi-precision arithmetic routines, I/O routines for teletypes and CRTs, sorting, list searches, hashing, tables, etc. Resident interpretive debuggers and editor/assemblers.

Fifth Session. Experiments and lectures on interfacing analog-to-digital converters, digital-to-analog converters, sample-and-hold devices, analog multiplexers, and digital panel meters.

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EDUCATIONAL MATERIAL. Six (6) texts and/or laboratory workbooks in the popular Bugbook series written by the course instructors and their colleagues, as well as some hand-out material, will be used during the course and retained by the participants. Approximately 1850 pages of text material on 8080A/8085 based systems will be provided.

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Questions should be addressed directly to the course instructors, David G. Larsen (703) 951-6478, Dr. Peter R. Rony (703) 951-6370 or Dr. Paul E. Field, (703) 951-5376.

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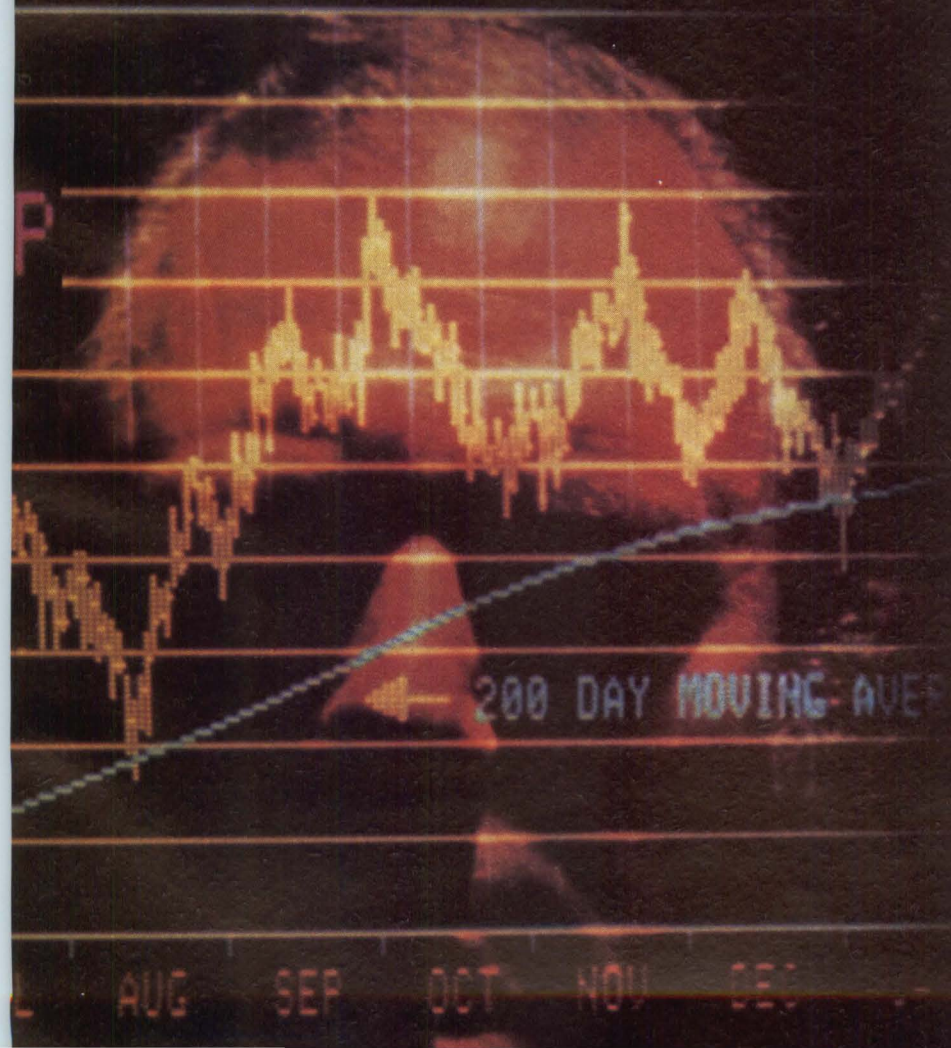

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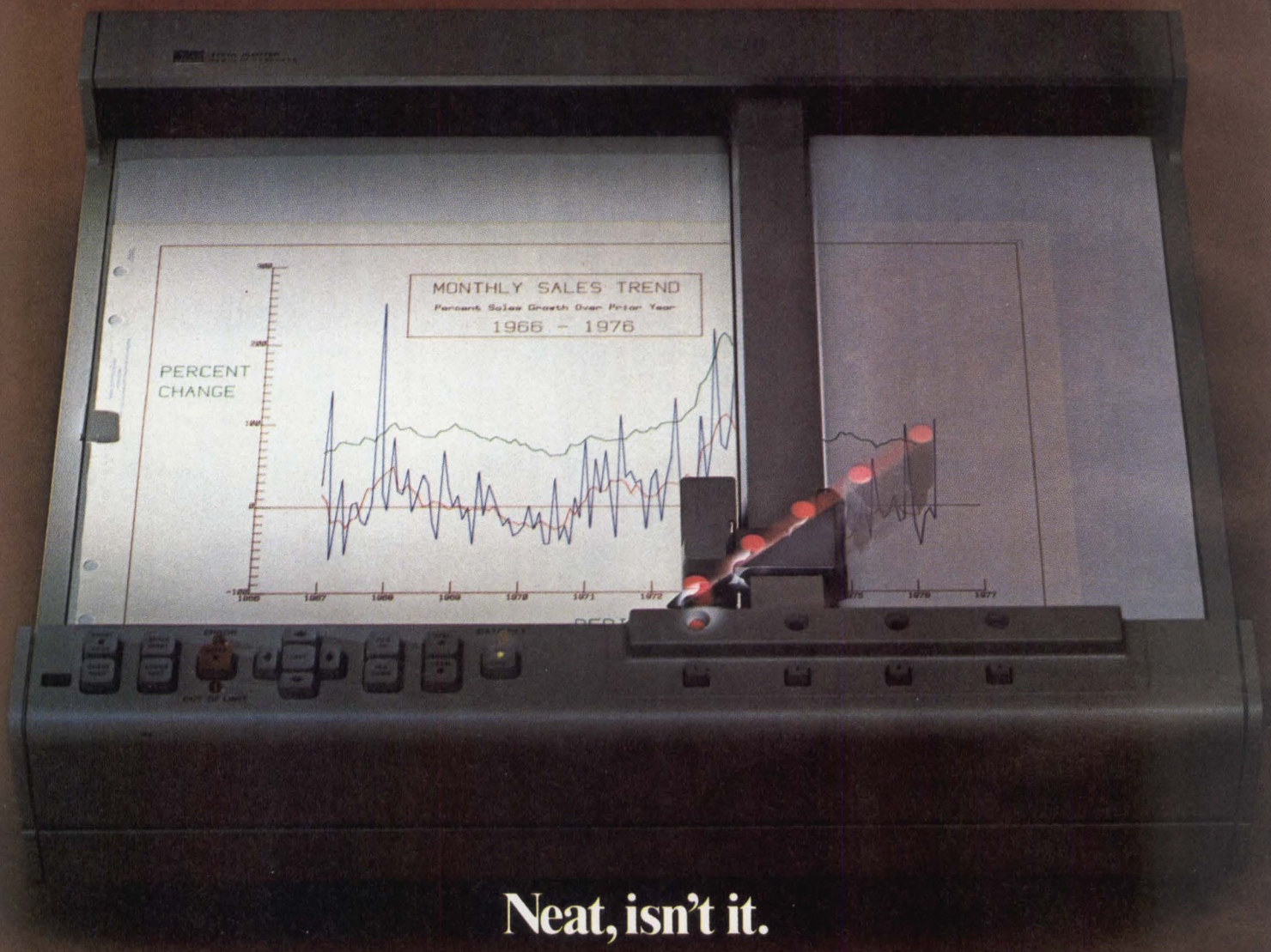

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VIRTUAL MEMORY DESIGN REDUCES PROGRAM COMPLEXITY

Reconfiguring the existing CDC STAR-100 hardware to obtain a true multilevel memory storage hierarchy for automatic memory allocation and I/O transfers should improve the software operating system, maintenance, and cost of an enhanced virtual memory design

Joseph E. Requa Lawrence Livermore Laboratory, Livermore, California

A large virtual memory can be used by the operating system to eliminate an application program's need for conventional input/output, thereby decreasing the cost and complexity of application program development. The price to be paid for the advantages thus attained, however, is reflected in increased operating system overhead, the possibility of central processor idle time, and the increased complexity and thereby increased costs of developing and maintaining the system software. These considerations coupled with increasing software costs and decreasing hardware costs provide an economic incentive for greater hardware participation in the handling of virtual memory.

Since the virtual memory system discussed here is based on the premise that only pages required by a program at a given time reside in memory at that time, and since its operating system is responsible for transferring pages to and from memory, the most logical step in the evolution of virtual memory is to provide hardware handling of page replacement. This requires a page replacement strategy (ie, when memory is full, a procedure for selecting a page to be removed to provide space for a new page), which can be economically implemented in hardware and which will perform efficiently. A second requirement is that the hardware must be given sufficient information to locate pages in external storage.

To detail the proposed automatic hardware control, the concept of virtual memory used in the discussions is first defined and a general approach to implementation of the two most prevalent virtual memory structures is described. Then the virtual memory implementation used in the Control Data STAR-100 (Fig 1) is discussed in detail to supply the background necessary to develop the proposed enhancements. These enhancements will provide for automatic hardware control of page transfers between memory and external storage.

Mapping Functions

A computer that provides any form of mapping other than the identity map between central processing unit (CPU) generated addresses and physical memory addresses satisfies the most general definition of virtual memory. Consider a 3-part computer system consisting of CPU, address translation mechanism, and physical memory. Addresses generated by the CPU are termed virtual addresses. The single-valued time-dependent mapping function, $P = f(V, t)$, in the address translation mechanism generates a physical address, P, by which memory is accessed to satisfy memory request V made by the CPU. The mapping function, $P = V + C(t)$, where C is a constant that is set by operating system software, does not really qualify as providing a virtual memory. Therefore, the set of mapping functions that provide true virtual memory must be restricted. Primary requirement for a virtual memory

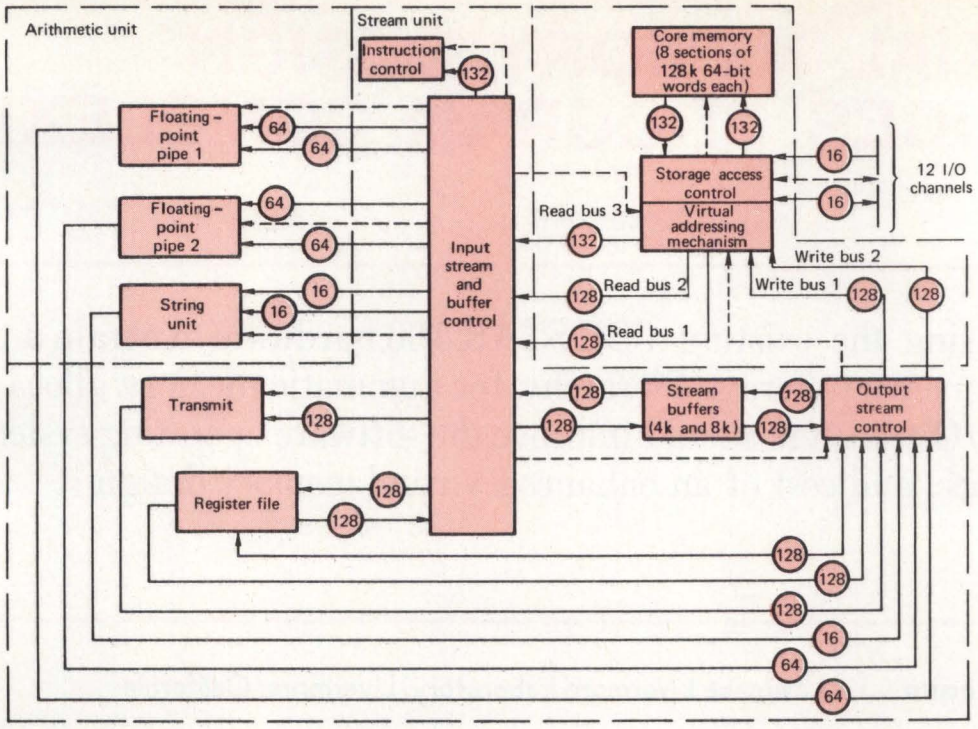

Fig 1 STAR-100 computer system. System consists of 1M 64-bit words with a 1.2-μs memory cycle time and core memory as main storage. Storage access control provides virtual address translation, and access to core memory by CPU and I/O subsystem. CPU consists of stream unit, two floating-point arithmetic units, and string unit. Stream unit provides 256-word general-purpose register file, instruction decoding, control of remaining units of CPU, and buffering and address control for vector operations. Floating-point pipes perform half- and full-word scalar and vector operation. String unit provides bit, decimal, and byte operations

mapping function is that it allow a finite set of discontinuities in the mapping function. The corollary of this restriction is that a contiguous set of virtual addresses may reside in a discontiguous set of physical addresses.

Given an appropriate mapping function to be categorized as a virtual memory mapping function, a few hardware and software pragmatics must be considered. In the case where mapping an address in the range of allowed virtual addresses does not generate

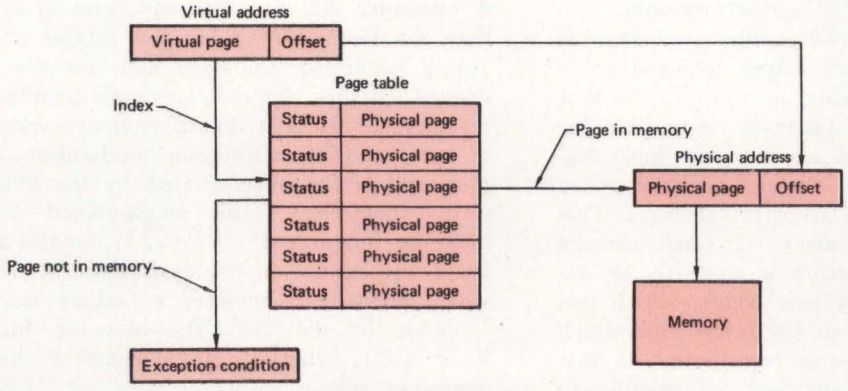

Fig 2 Typical paging mechanism. Virtual page portion of virtual address is used as index into page table. If status indicates that page is in memory, physical page number from page table replaces virtual page portion of virtual address, generating physical address to be sent to memory; otherwise, exception condition occurs, which must be handled by system software

an address in the physical address domain, either hardware or software must alter the mapping function so that the address causes a valid mapping. Without such an alteration, a valid virtual memory mapping function becomes merely a memory protection mechanism. Virtual memory, then, consists of a set of hardware that provides an appropriate mapping function and a combined hardware/software system that resolves failures of the hardware to obtain a physical address for a valid virtual address.

Given the set of acceptable mapping functions, two classes of functions have been implemented in hardware: the set that provides a fixed set of periodic discontinuities and the set that provides a variable number of aperiodic discontinuities. The former class provides a paged virtual memory and the latter a segmented virtual memory.

Paged Virtual Memories

In a paged virtual memory, a physical memory of N words is divided into M pieces, called page frames, where $M < N$. For simplicity of implementation, M and N are chosen to be integer powers of 2 so that a physical address may be divided into two parts, a page frame number and an offset within the page, without the necessity of computation. Let $\log_2 N = C$, $\log_2 M = A$, and $\log_2 (N - M) = B$. A physical address of C bits may be thought of as A bits defining the page frame followed by B bits defining the offset within the page frame. Given a virtual address range that is also a power of 2, a virtual address can be divided in the same manner as a physical address. Note that there is no requirement that virtual and physical address ranges be the same size, but that a physical page frame and a virtual page must be the same size.

Consider the problem of associating a physical page frame number with a virtual page number. One implementation of a paged virtual memory (Fig 2) is to provide a table, called a page table, whose contents are under control of system software and are not modifiable by user software.

This is usually accomplished by providing two states for the CPU: a system state and a user state. In system state, the virtual memory mapping function used is the identity map, and instructions allowing access to the page table and external input and output (I/O) devices are enabled. In user state, the hardware-provided mapping function is used, and instructions allowing access to the page table and external I/O devices are disabled. Associated with user state is a block of information, called the state vector, which is stored by hardware when changing from user mode to system mode and is reloaded by hardware when changing from system to user mode. The state vector contains the state of internal CPU registers, such as the program counter, which must be preserved in order to restart a job after the CPU has been switched to system mode.

There is one entry in the page table for each page of allowed virtual space. Each entry contains, as a minimum, a physical page frame number and an indicator to specify whether or not the page frame contains a virtual page. It may also contain status bits (eg, a bit to indicate that a page has been modified while in memory) and/or control bits (eg, a bit to indicate whether or not modification is allowed). When a virtual address is generated and sent to the address translator, the virtual page number is stripped off and is used as an index into the page table to obtain the physical page frame number. If the page frame contains a virtual page, and the attempted access is legal, the virtual page number portion of the virtual address is replaced by the physical page frame number from the page table and the resultant physical address is sent to memory. If either the page frame does not contain a virtual page or the attempted access is illegal, the CPU is switched to system mode and the operating system is left to cope with the problem.

If hardware cost is to be minimized without regard to performance, the page table is kept in memory and a pointer to it is held in a register that is saved and reloaded as a part of the CPU state vector when

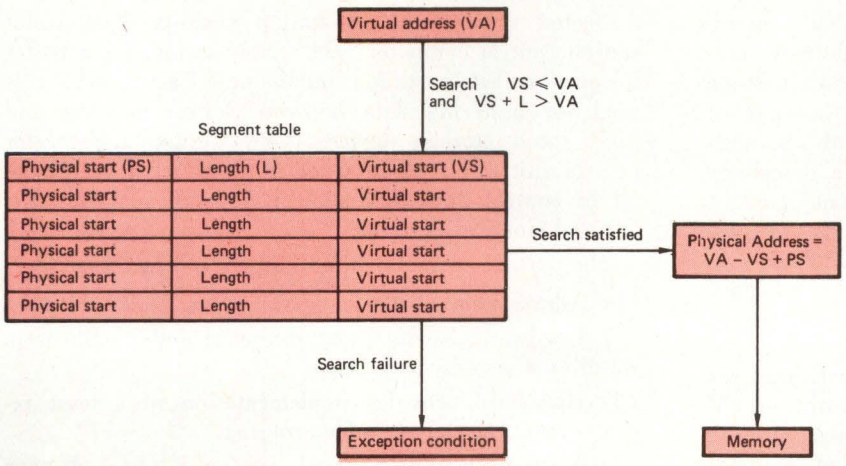

Fig 3 Typical segmentation mechanism. When virtual address is generated, segment table is searched for entry which has virtual starting address less than, or equal to, required virtual address, and virtual starting address plus length greater than required virtual address. If such entry is found, physical address is calculated by subtracting virtual starting address of segment from required virtual address, then adding physical starting address of segment to obtain physical address to send to memory. If entry is not found, exception condition occurs, which must be handled by system software

a CPU mode change occurs. This structure requires a double reference to memory for each address. The alternative is to hold the page table in a set of registers, thereby eliminating the extra memory fetch. The middle ground is to provide a set (typically four to 16) of registers that hold the set of most recently referenced page table entries and can be searched in parallel at high speed. Double memory references are required only for access to pages whose page table entries are not in the registers.

Segmented Virtual Memories

A segmented virtual memory (Fig 3) is somewhat more difficult to implement because of the variable positions of discontinuities in the mapping function. To implement a segmented memory, it is necessary to replace the page table with a segment table and the simple table lookup mechanism with a search mechanism. The segment table contains the starting virtual address, the starting physical address, and the length of each segment currently in physical memory. It may also contain other control information. When a virtual address is generated, the segment table is searched for the entry containing the address. If such an entry is found and if the attempted access is legal, the virtual starting address of the segment is subtracted from the generated virtual address, the beginning physical address is added to this result, and the resultant physical address is sent to memory. If the address is not found, control is given to system software for resolution.

Again, economics dictate the actual structure of the mechanism for address translation. Since instruction references and data references are separable, usually at least two registers are provided: one to hold the segment table entry for the last instruction reference and one to hold the segment table entry for the last data reference. Since both instructions and data tend to be referenced sequentially, provision of two registers allows a large percentage of virtual addresses to be translated to physical addresses without referencing memory.

Present System Design

The CDC STAR-100 is a large scale, high speed, logical and arithmetic computer. Two capabilities, vector processing and virtual memory, give the machine its individual character. Vector processing consists of performing the same operation on a set of operands called vectors, which are characterized by a descriptor specifying a starting address and an element count.

When in vector mode the stream unit (Fig 1) provides the necessary address control and buffering to allow two 64-bit operands to be fetched from memory and one to be stored in memory during each 40-ns CPU cycle. Storage access control provides virtual to physical address translation, and physical memory accessing. Memory consists of 1M 64-bit words or 8M bytes physically organized into four sections with 16 banks per section. A memory word, called a super word or sword, is 512 bits or eight CPU words wide.

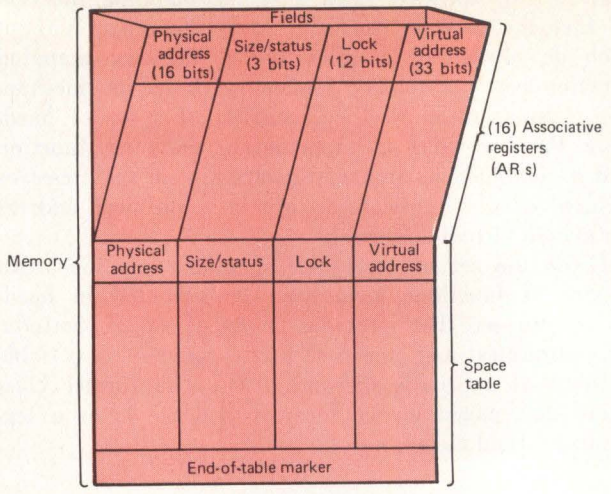

Fig 4 Page table. Table contains one entry for each physical page assigned, giving physical page number, virtual page address, job to which page is assigned in lock field, and size and modification status of page. Page table is held in memory when machine is in system mode. When machine is in user mode, 16 most-recently referenced entries are held in associative registers to speed table searching

Memory cycle time is 1.2 μs. Memory is organized to provide a very high bandwidth for sequential memory references and, hence, is well suited to vector processing. However, the long memory cycle time results in slow random fetching from memory. To alleviate this problem, the stream unit contains a 256-word register file. The 64-bit general-purpose registers in the file have a 40-ns access time and are used as a small fast scalar memory. The arithmetic unit is divided into two segmented functional units, each capable of accepting input(s), performing one step of an operation, and generating output(s) during each CPU cycle. Since data flows through the units in a manner analogous to water flowing through a pipe, the units are called pipes. The string unit provides bit-vector and byte-vector operations.

The system is a local network consisting of the STAR computer and a set of independent I/O processing computers called stations, each controlling a set of dedicated I/O devices. A station consists of a 16-bit station control computer (SCU) and, optionally, a buffer memory called a station buffer unit (SBU), which is used for buffering data between central memory and high speed storage devices. One station, the master control unit (MCU), is attached to the STAR by a special set of control lines that allow it to start and stop the CPU and monitor its status.

The virtual memory is unique in several respects.

(1) Addressable virtual memory space is 2^{48} bits.

(2) Hardware provides CPU reference and modification status on a page-by-page basis.

(3) Hardware provides implementation of a least recently used (LRU) page table ordering.

(4) Virtual memory is cataloged on a physical page basis rather than a virtual page basis.

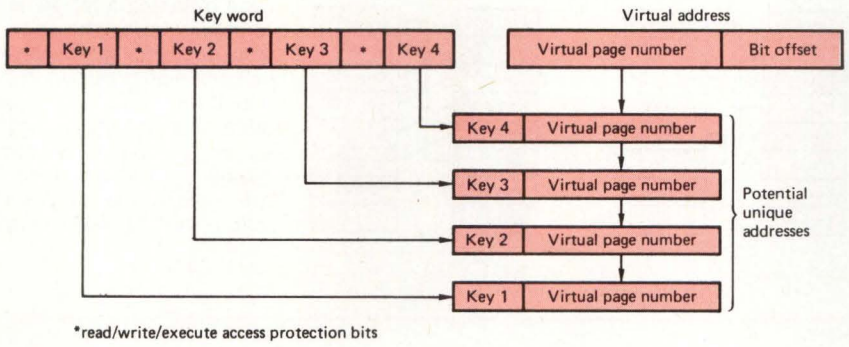

Fig 5 Unique virtual addresses. When job generates virtual address, four potentially unique virtual addresses are generated for comparison with page table unique addresses. Associated with each job is key word containing four unique job identifiers, called keys. Each key has different access protection associated with it. Each potentially unique address is formed by joining one with virtual page number from initial virtual address

(5) Hardware support is provided for two page sizes: a small page of 512 words and a large page of 128 small pages.

Virtual to Physical Page Association

The page table (Fig 4) consists of one 64-bit word per entry. Length of the table is software controlled with a word of 0s indicating the end. An entry is divided into four fields, a 16-bit physical page address, a 3-bit size/modification field, a 12-bit lock field, and a 33-bit virtual page address.

To permit sharing of memory by multiple processes, a lock and key protection mechanism is provided to make addresses generated by a process unique. Consider two processes both active at the same time. Each process might generate address 10000, referencing its own private storage. The lock field in the page table is one-half of the mechanism for resolving such address conflicts; the other half is provided in the state vectors of the processes. The state vector of a process is held in a 16-word block of memory and is called the invisible package. A word within this package, called the key word, contains four 16-bit fields, each divided into 4- and 12-bit subfields. The 12-bit subfields are called keys and the 4-bit subfields contain access protection information.

When a process generates a virtual address, four potentially unique virtual addresses (Fig 5) are generated by joining each of the process's four keys with the virtual page address referenced by the process. A unique virtual address within the page table is defined by joining the lock field and the virtual page address field of a page table entry. When a page table search is initiated, the unique virtual address from each page table entry is compared with each of the potentially unique addresses. A match occurs if one of the potentially unique addresses matches a unique address from the page table. If two matches occur in the search, the mapping function ceases to be single-valued, causing the machine to stop.

Page Table

The page table is divided into two parts, a set of 16 associative registers (ARs) and a memory contained space table. The ARs are loaded and stored, from and to the 16 words of memory immediately preceding the space table, which serves to minimize the time required in page table searching. Page table entries for the most-recently used 16 pages are held in the ARs, which are searched in parallel. The search moves into memory only if a match is not found in the ARs. When a match is found in the ARs, the time required for a memory reference is the same as that required when the machine is in the system mode and virtual addressing is disabled. If the search extends to the space table, it requires 54 cycles to initiate the memory search and to fetch the first space table entry from memory. Thereafter, entries are searched at a rate of 2/cycle.

Search hardware is also used to maintain the page table in least-recently used order (Fig 6). Whenever a match is not found in the ARs—no-match search—contents of the ARs are pushed down one entry, with the last AR's entry being moved to a holding register, and a special marker called a null being inserted in the first AR. Initially, the page table search is in ripple search mode. In this mode, as each entry is read from the page table, it is exchanged with the

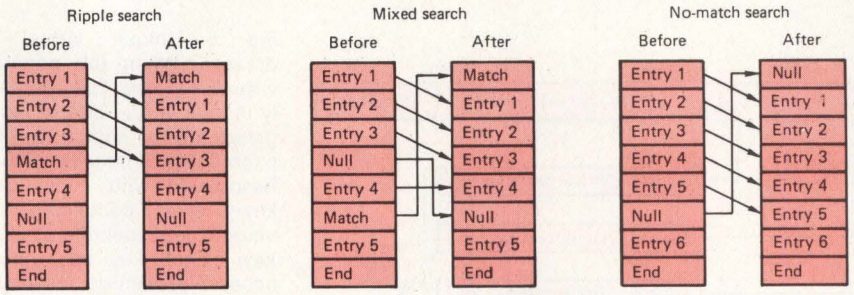

Fig 6 Page table search examples. These examples show how table is maintained in least-recently used order. In ripple search, all entries above matching entry are moved down and match is placed at head of table. In mixed search, entries above the null are moved down, entries between null and match remain in place, match is moved to head of table, and is replaced by null. When no match is present, during no-match search, entire table is moved down and null is left at head of table

entry in the holding register. Thus, the entire page table is pushed down one position in the portion of the table searched. If a match is made while in ripple search mode, the matching entry, which is in the holding register, is transferred to the first AR, replacing the null that was initially inserted.

The search remains in ripple search mode until either a null is encountered or the end of the table is reached. When a null is encountered, the search switches to read-only, or mixed-search mode. The entry in the holding register replaces the null, and entries below the null are read but not moved. If a match is made while in read-only mode, the entry that caused the match is moved to the first AR, replacing the null initially inserted, and is in turn replaced by a null. If one null is placed in the page table initially and the software system neither inserts nor deletes a null, there will be only one null in the table at any time a search is not in progress; furthermore, the hardware will never move the end of table marker.

Handling Page Exceptions

Two types of page exceptions occur. If no match is found in the page table for a requested virtual page, a page fault occurs. If a match is found, but the attempted access is illegal, an access interrupt occurs. In either case, the hardware stores a cause word into the invisible package of the executing process to indicate which exception condition occurred. The cause word contains a 48-bit virtual address field and a set of four cause bits, indicating read-access violation, write-access violation, execute-access violation, and page fault condition. The virtual address field contains the virtual address that caused the exception condition.

In STAR configurations currently in use, no paging store (in the conventional sense of a fast fixed-head rotating device) is provided; hence, all paging activity is between central memory and the file system. The file system consists of rotating moving-head devices attached to buffer controllers, which have access to central memory and provide full I/O support for the system. The file store, as viewed from the CPU, consists of a set of segments on disc. A segment becomes active when a process requests attachment. Therefore, the virtual space known to a process is the set of file segments to which it is attached, with their associated virtual memory correspondence. When a process is initiated it is first attached to two segments: the source file and the drop file. The source file contains the initial image of the process. The drop file is used to contain any pages of read-only files, which are modified in memory so that the initial states of read-only files are preserved. It is also used to contain any virtual space referenced which is not represented in one of the disc segments attached to the process.

When a page exception occurs, software first determines whether it is a page fault or an access violation. In the latter case, if it is a write access violation and if the page involved came from a file whose initial state is to be preserved, the lock associated with the page is changed to the process read-write key, an entry for the page is made in the process's drop file map, and the process is allowed to continue. In all other cases, an access violation is considered to be a fatal error.

When a page fault occurs, the first step in processing is to determine if the required page exists in the file store. The virtual address required is picked up from the cause word, and the drop file map is searched for a matching page address; it must be searched first because a page is allowed to be in both the drop file map and the file segment map. If no match is found in the drop file map, the file segment map is searched. If this search does not find the page, the reference is assumed to be to space not existing in the file store. In this case, a page frame is allocated, an appropriate entry is made in the drop file map and the page table, and the process is allowed to continue. If the page is found in the file store, a page frame is allocated, the page is read from the file store into the page frame, an entry is made in the page table, and the process is allowed to continue.

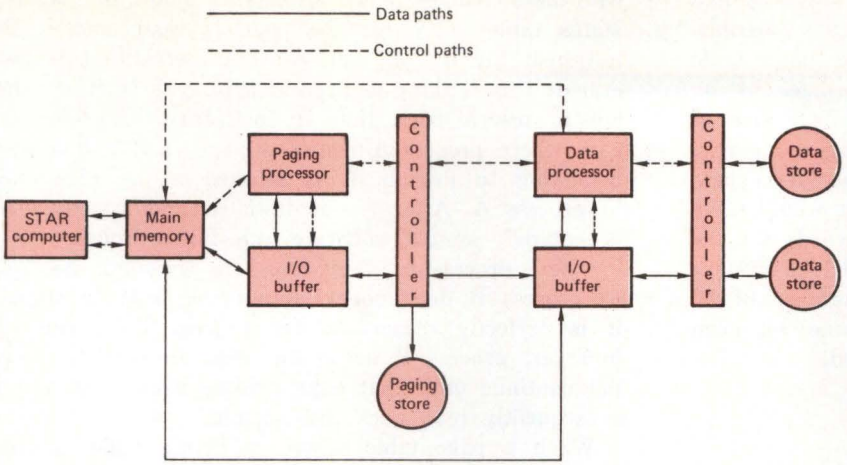

Fig 7 Proposed automatic page allocation. To provide hardware management of page transfers between main memory and paging store, traditional configuration of central processor handling dissimilar I/O devices must be replaced by one providing true hierarchical memory. In this configuration, data processor transfers files between data store and paging store. Paging processor transfers pages between paging store and main memory. All paging activity deals with single uniform level of external storage

Possible Future System

Virtual memory structure of the STAR-100 was designed in the late 1960s for use in the 1970 to 1980 time frame. To redesign for the 1980 to 1990 time frame, a somewhat more complex structure should be provided. When handling faults for small pages, the search mechanism should provide information necessary for page allocation and deallocation, and should automatically initiate the transfers.

The problem of large page allocation does not lend itself to solution utilizing an LRU paging algorithm because there are not enough large pages to provide good statistical behavior. For this reason, handling of large pages should be relegated to system software. A virtual memory upgrade that might be viable in the 1980 to 1990 time frame and can be implemented with current technology is described.

System Configuration

Attempts to implement automatic page allocation are impeded in part by the configuration of most computer systems currently in use. They consist of three levels of memory: main memory, paging store, and data store. All transfers between various levels must be buffered through main memory. An alternate structure (Fig 7) for this 3-level memory hierarchy would provide a processor associated with each level of memory. In this case, the STAR CPU would be associated with main memory. An I/O processor attached to paging store and main memory would be responsible for transfers between them. A second I/O processor attached to paging store and data store would be responsible for transfers between those areas. Each of these I/O processors would have sufficient buffer memory to provide its functions without using central memory buffers.

Natural units of mapping on each level are pages for main memory, segments for paging store, and files for data store. Data flow in the system can then be described in two parts. As files are attached, segments equal to the file sizes are allocated on the paging store, and the files are transferred from data store to paging store. As files with write access on data store are detached, any modified pages in memory are moved to page store; then, any modified pages on the page store are moved back to the file from which they were initially read. The segment table entry is then deleted to release the paging store space. Files without write access on data store have any pages in memory belonging to them deleted, and the appropriate segment table entry removed to free paging store space. As pages not in memory are referenced, they are retrieved from paging store and placed in memory. As pages are removed from main memory, they are returned to their original position in paging store.

From the viewpoint of the STAR CPU, the system configuration appears to be a 2-level memory hierarchy with two exceptions. When a process whose initial image is in data store is initiated, the image must be moved from data store to paging store. When a file is attached or detached from a process, appropriate moves between the second and third level stores must be made. A communication path is provided from CPU to data store I/O processor, and the communication problem is left to system software.

For large page handling, the decision whether large pages should reside in data store or page store depends on relative characteristics of devices used for storage. To allow for the possibility of large pages residing only on data store as well as that of traditional file I/O, the data store buffer memory will have access to main memory as well as to paging store.

Memory Protection

One limitation of the existing virtual memory should be considered before describing the enhanced structure. Current memory protection is on a key rather than a page basis. The current software system allocates one key for read/execute access, one for read/write access, one for globally shared read/execute access, and one for system use. No key remains to allow limited sharing of memory among processes. If memory protection is disassociated from keys and instead is pro-

vided on a page-by-page basis, a private key, a global key, a limited key, and a system key are possible. However, to do this, three bits of the page table entry must be free for access protection usage.

Current experience has shown that a page size of 512 words is too small for existing memory configurations, and any redesign would include a memory expansion of about a factor of 4; therefore, it would seem reasonable to use a page size of 4096 words for the redesigned machine. With this page size, virtual memory can be cataloged with a virtual page number of 30 bits rather than 33. The remaining three bits can then be used as a memory protection field.

Virtual Memory Structure

Since the current page table implementation provides most of the capabilities needed, it should be maintained with only a few changes in operation of the search mechanism. Two hardware defined tables (Fig 8) are added—memory status table and segment table—to provide capability of automatic page allocation and I/O processing.

Memory status table contains a 4-bit entry for each physical page frame in the machine. The first status bit (P) indicates that an entry for the page occurs in the page table, the second bit (T) that a page is in transit between main memory and paging store, the third status bit (S) that the page is in use by the operating system and not available for allocation, and the fourth bit (M) that a paging store address is not available to hardware for that page.

Any page with a zero entry in the memory status table is available for assignment. Any page with only its page table bit set is available for assignment, subject to the constraint that, if its page table entry indicates it has been modified in memory, it must be written to paging store before being reused. Any other "on" bits in the memory status table inhibit assignment of the page.

To catalog segments on paging store, entries in the segment table contain a 22-bit size (length) field, a 12-bit key lock, and a 30-bit virtual page number (starting address) in the first word. The second word contains two 32-bit fields: the first indicates the location in paging store and the second the location in data store. Each field is divided into a 3-bit access indicator, a 5-bit unit number, and a 24-bit page (address) number. Primary purpose of this table is to provide a means of locating a virtual page in paging store when the page is not found in memory. In addition, a register is added to the page table mechanism; called the removal register, it has the same format as a page table entry, and is used to indicate the page to be reassigned. Finally, three base registers are added, one for the starting address of each virtual memory table.

Virtual memory operation will then consist of three searches: search page table, search memory status table, and search segment table (see Fig 9).

Page Table Search

Page table search is performed as described previously, with these changes. When a match is found, the memory status table entry for the page is read, and if the in-transit bit is "on," an exception condition is generated; this is done to prevent a process from attempting to use a page that is in transit. Consider the case where process A causes a page fault and a page belonging to process B is selected to be reassigned to process A. After I/O is initiated and system mode is entered, system software schedules process B as the next process to gain access to the CPU. As long as process B does not reference the page in transit, it is perfectly reasonable for process B to run. If, however, process B needs the page in transit, it can not continue until that page reaches page store and is subsequently read back into memory.

When a page table search is being made, a page should be selected for replacement during the search. Then if the page being searched for is not found (no match is made) and if no free page is available, it is not necessary to search the page table again to find a replacement candidate. This requires that the search algorithm be modified so that as each entry is read from the page table, its associated memory status table entry is also read. If status indicates the page is assignable, the page table entry is moved to the replacement register.

Memory Status Table Search

In parallel with the page table search, the memory status table must be searched for a zero entry. If a page frame with a zero entry is found, at the end of the page table search, the replacement register is cleared, except for the physical address field, which is set to the physical address of the free page frame found. This gives a replacement algorithm that assigns free pages as long as they are available, then switches to an LRU replacement algorithm when no free pages are available.

Segment Table Search

On exit from the page table search with a no-match condition, a page frame to be assigned to the missing page has been selected. Next step is to locate the missing page and the page to be replaced, if modified, in the paging store. To find a virtual address in the segment table, three conditions must be met: the lock in the segment table must match either a key belonging to the faulting user or the lock from the replacement register, the virtual address in the segment table must be less than or equal to the desired virtual address, and the virtual address plus the length in the segment table must be greater than the desired virtual address.

Segment table search hardware must be capable of searching for two virtual addresses simultaneously, since the paging store locations of both the page to be removed and the page to be read must be found, in the case where a modified page is selected for replacement.

All new page table entries, except the modification status, can be constructed using the physical address from the replacement register, the lock from the segment table, the virtual page number from the initial

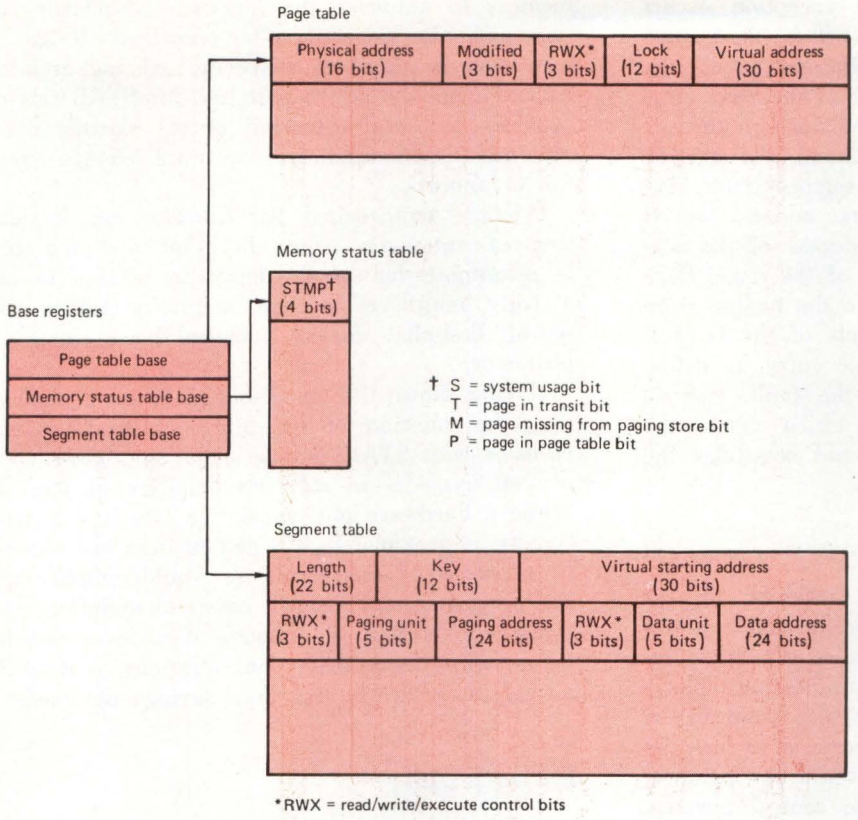

Fig 8 Virtual memory table structure. Configuration consists of set of three base registers specifying location of page table, memory status table, and segment table. Page table contains one entry per assigned physical page defining its virtual address to physical address mapping. Memory status table contains one entry per physical page defining its assignability characteristics. For each segment in paging store, segment table defines virtual address to paging store address mapping

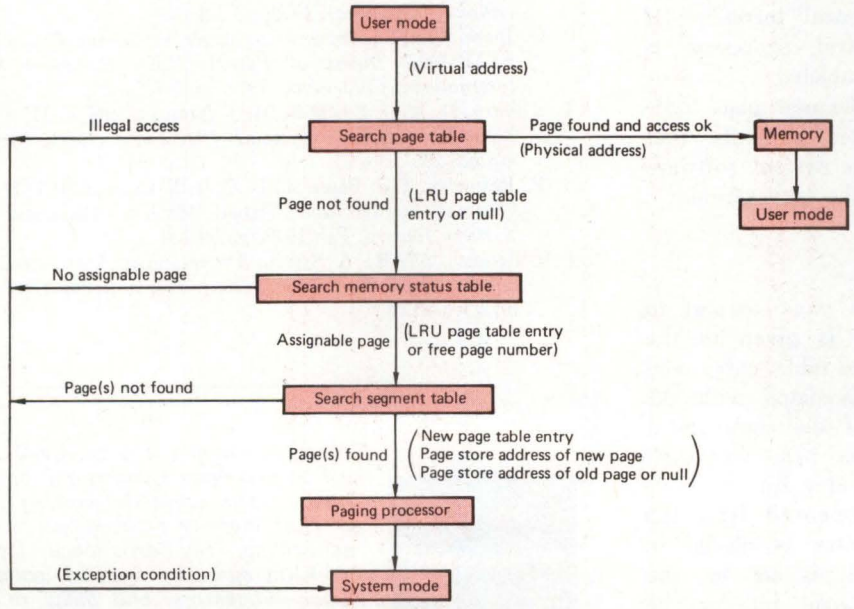

Fig 9 Proposed page table search. When virtual address is generated in user mode, page table is searched for matching address. If match is found, physical address is generated and sent to memory, and machine remains in user mode. If match is not found, least-recently used page, if any, is saved, and memory status table is searched for unassigned page. Segment table is searched next, for paging store address of required page, and, if page to be replaced is modified, for its paging store address as well. Necessary information for I/O processing is sent to paging processor, and system mode is entered to schedule next job

virtual address, and the access bits from the segment table. Modification bits will be set to indicate a small page which has not been referenced by the CPU.

If no segment can be found that matches the required virtual address(es), a page exception occurs and system software takes over. This will be the normal exit for a large page fault. Note that exit on a large page fault is not possible at the end of the page table search because a virtual address does not contain any page size indicator. If a match is found, the starting address on the page store from the segment table plus the difference between the virtual page address faulted for and the starting virtual page address of the segment defines the page store address of the page. Page store address(es) can then be sent to the paging store I/O processor, along with the contents of the replacement register and the new page table entry, to define I/O processing required to satisfy the fault. Control is then given to system software, which marks the faulting process as unable to run and schedules the next process.

Paging Store I/O Processing

When the paging store processor receives an I/O request, it immediately assigns a buffer and initiates a read of the paging store to minimize total time required to satisfy the fault. It then examines the replacement register to determine whether the page to be replaced must be removed from memory or can be simply overlaid. If it must be removed from memory, a second buffer is assigned and the central memory to buffer transfer is done. The paging store write request is then initiated. When the paging store read completes, the appropriate buffer is transferred from the paging processor to central memory. Although slight degradation in performance may result, it is best not to issue a completion response until the page to be removed from memory has been written, if one exists, since this will improve error recovery capability. When transfer of the required page to central memory and transfer of the page from central memory (if required) are completed, the central processor is signaled that the transaction is completed.

Responses to the transaction are the new page table entry, and the replacement register contents that caused the transaction. This provides system software with sufficient information to finish the transaction.

Page Request Post Processing

When a response is received for a page request to the paging store processor, control is given to the operating system, and the new page table entry and the replacement register contents associated with the fault are returned to the system. If the replacement register does not indicate that a free page was used to satisfy the fault, the page table entry for the page frame used to satisfy the fault is removed from the page table. The new page table entry is placed in the page table, the in-page-table bit is set for the page frame assigned, and the in-transit bit for the page frame is turned off. At this point, the operating system marks the faulting process as again able to run, and schedules the next process.

Conclusions

Within the state of current technology, it is possible to provide a hardware implementation of a virtual memory to automate the functions of memory allocation and I/O transfers. The described design implementation is aimed at a specific existing architecture. Although not the only possibility, for STAR this design provides a logical extension of the existing hardware philosophy and minimizes software changes required for its support.

Primary requirement for allowing an implementation of automatic page allocation and I/O transfer is reconfiguration of the hardware system to achieve a truly multilevel storage hierarchy rather than a set of dissimilar devices managed by a single central processor.

Having shown the possibility of such an implementation, the question of feasibility appears. Current experience with STAR indicates that approximately 10% of CPU usage is in software handling of page faults. While a hardware implementation will have some time penalty, approximately 8% of CPU time can conceivably be recovered. Using hardware would simplify the operating system and make it easier to maintain, yielding significant savings in software costs over the life of the system. Given these considerations, cost of implementation is clearly less than savings obtained.

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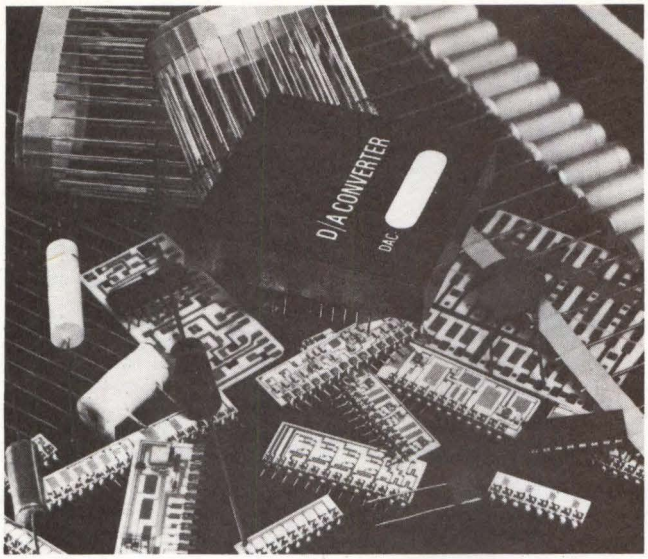

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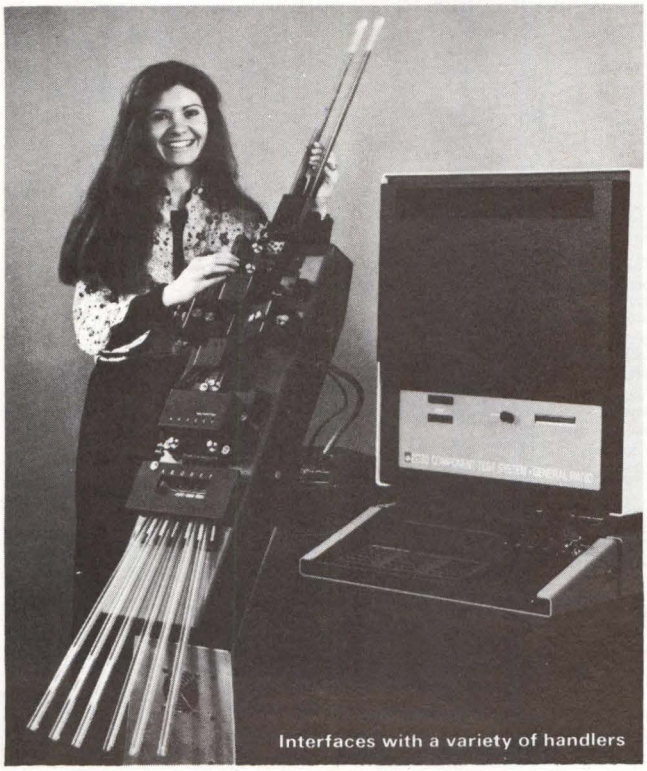
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HANDLING MULTILEVEL SUBROUTINES AND INTERRUPTS IN MICROCOMPUTERS

Programming techniques for implementing multilevel subroutines and interrupts in F8 microcomputer systems are explained in detail for hardware designers with limited software experience

James F. Vittera Mostek Corporation, Carrollton, Texas

The decreasing cost per computer function and reduction in size afforded by advances in metal-oxide semiconductor large-scale integration have brought computer technology and techniques into areas where, until now, mechanical controllers, random logic, and relay logic predominated. Availability of a large number of input/output pins in the single-chip F8 microcomputer (3870) allows its use as a replacement for many previously used control devices. For these applications, software structure relies heavily on the basic concepts of repetitive instructions by several control devices demanding resource priority from the central processing unit. This discussion of the use and implementation of multilevel subroutines and interrupts as they apply to programming an F8-based microcomputer system (Fig 1) is intended to provide the hardware designer not totally familiar with microcomputer programming with the background necessary to construct such software. The computer's instructions are given in the Table.

Subroutines

A subroutine is a sequence of instructions or mnemonics that can be called or used in several portions of the microcomputer program. Its purpose is to reduce the total length of a program by consolidating in one section of the program a sequence of instructions that are repeated in several different areas. When the subroutine is required, the program counter (PO) * contents are replaced with the starting address of the subroutine. At the end of the subroutine, program control is transferred back to the main body of the program.

Fig 2 depicts the main program flow when using subroutines and interrupts. When the main program calls a subroutine, the PO is loaded with the address of the subroutine. The last statement of the subroutine causes a return back to the main program flow by retrieving the saved PO value. The subroutine is called again any place in the main program flow where its sequence of instructions is required. Each time the subroutine is called, a savings in program length and read-only memory (ROM) size results. This savings is equal to the length of the subroutine (minus the four overhead bytes required to call and return), compared with a program that does not use subroutines. Frequently a subroutine will call another subroutine, resulting in what is referred to as nested or multilevel subroutines.

*Early versions of F8 literature labeled the program counter as PC0 and the stack register as PC1.

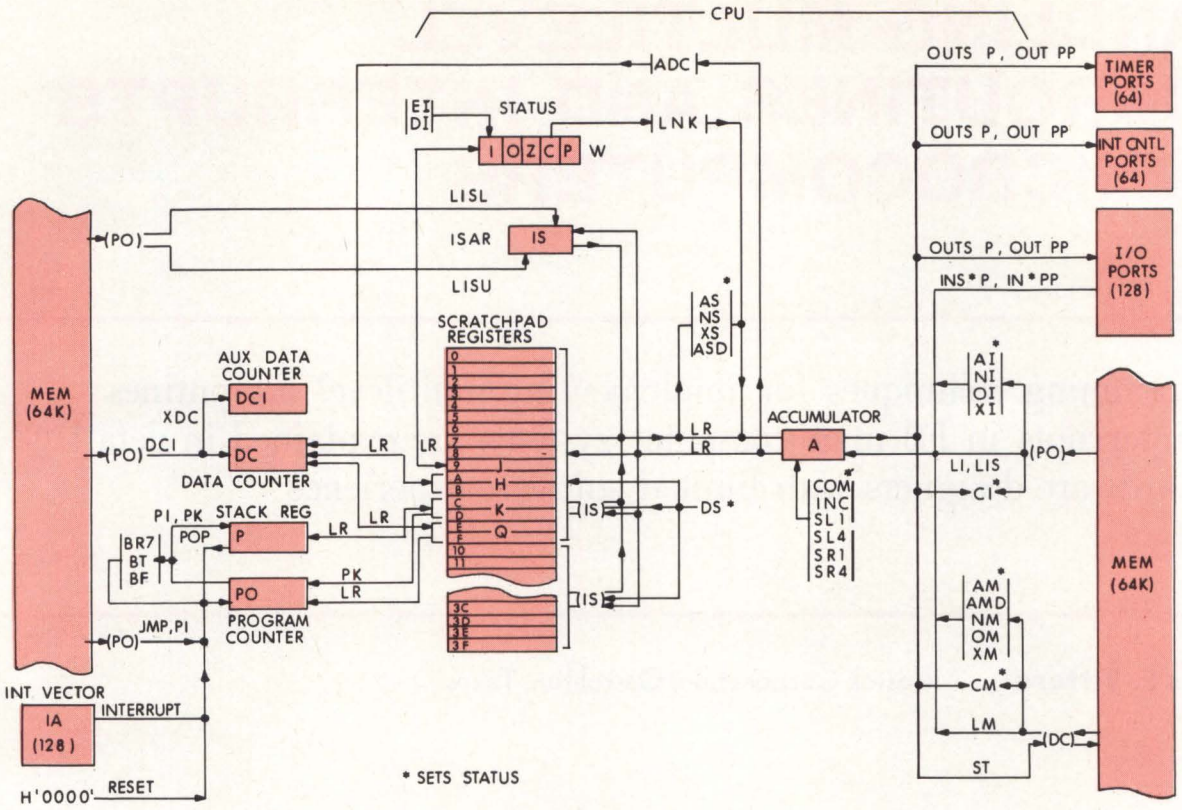

Fig 1 F8 programming model. Register-oriented architecture has 64 internal scratchpad registers, which are used to save return addresses and CPU registers during subroutine calls and interrupt service routines. General architecture can handle 64k bytes of memory and 256 I/O ports while single-chip implementations (3870) use 2k bytes of ROM and six I/O ports.

Interrupts

Interrupts are used in a microcomputer system to make it responsive to the device it is controlling. By interrupting the microcomputer, the input/output (I/O) device can signal its requirement for attention or service by the microcomputer. As in the case of the subroutine, the interrupt can divert the main program flow to a sequence of instructions called the interrupt service routine (Fig 2). This routine either inputs or outputs data to the device being controlled. At the end of this service routine, the PO value at the time of system interrupt is retrieved from a temporary register and is reloaded into the PO to cause a return to the main program flow. Interrupts, like subroutines, can also be nested. An interrupt service routine may be interrupted by a higher priority device, or it may call a subroutine, which in either case causes nesting.

F8 instructions that are used to transfer program flow to or from subroutines or interrupts are shown in Fig 3. The PO holds the address of the next instruction to be executed by the microcomputer, while the stack register (P) acts as a temporary storage location for the PO. In addition, two registers in the scratchpad, designated K and Q, have instructions that link them to PO and P. Major instructions that link and affect these registers are:

Call to Subroutine Immediate (*PI*)—causes the next two 8-bit bytes in the program to be loaded into the PO in order to transfer control to a subroutine, and the old PO value (return address) to be saved in P.

Call to Subroutine (*PK*)—causes the contents of the K register to be loaded into the PO while its current contents are saved in P.

Return from Subroutine (*POP*)—used at the end of a subroutine or interrupt service routine to load contents of P back into the PO in order to return program flow to the main program. Previous value of the PO is overwritten and lost.

Load Register (*LR P,K and LR K,P*)—pair allows transfer of the contents of P to the K register in the scratchpad or vice versa. This switching is useful to save P's contents in preparation for a subroutine or interrupt.

Load Register (*LR PO,Q*)—allows the transfer of the Q register in the scratchpad to the program counter (PO).

The following sections discuss the use of these instructions and registers, as well as the general F8 architecture, to handle subroutines and interrupts, and presents some of the associated tradeoffs.

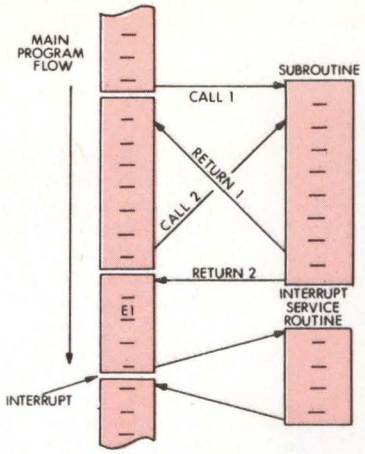

Fig 2 Program flow using subroutines and interrupt service routines. Subroutines can perform same short sequence of computer instructions at different points in main program. Program counter contents must be saved temporarily so that, at conclusion of subroutine, they may be retrieved and reloaded into program counter to cause return to proper place in main program. Similarly, interrupt service routines can divert main program flow to sequence of instructions that service interrupting peripheral and then back again

Subroutines and/or Interrupts Up to Two Levels

Many microcomputer applications can be handled by two levels of subroutines and/or interrupts. Two-level usage means that two return addresses must be saved, easily handled by F8 registers designed for this purpose. Subroutine calling is under full control of the programmer; thus, only return addresses need be saved. Contents of other registers (such as accumulator or status word) can be saved either by the subroutine calling or by the called routines, if these registers are needed by the subroutine. Interrupts are under control of the programmer only to the extent that they can be masked or enabled. Assuming that the interrupts are enabled, upon entry to an interrupt service routine, it may not be known which registers in the central processing unit (CPU) contain data that cannot be overwritten. In this case, the contents of these CPU registers should be stored in the scratchpad during the interrupt service routine and should be restored before exiting this routine. Examples of using the indirect scratchpad address register (ISAR) to store the contents of CPU registers in a push-down stack are given, but in many cases, the programmer will use specific scratchpad registers to save the CPU registers in a given interrupt service routine.

F8 Instructions

ADC	Add data counter with accumulator
AI	Add immediate with accumulator
AM	Add binary accumulator with memory
AMD	Add decimal accumulator with memory
AS	Add binary accumulator with scratch-pad register
ASD	Add decimal accumulator with scratch-pad register
BC	Branch on carry
BF	Branch on false condition
BM	Branch if negative
BNC	Branch if no carry
BNO	Branch if no overflow
BNZ	Branch if no zero
BP	Branch if positive
BR	Absolute branch
BR7	Branch if ISAR is not 7
BT	Branch on true condition
BZ	Branch on zero condition
CI	Compare immediate
CLR	Clear accumulator
CM	Compare with memory
COM	Complement accumulator
DCI	Load data counter immediate
DI	Disable interrupt
DS	Decrement scratchpad register
EI	Enable interrupt
INC	Increment accumulator
IN	Input
INS	Input short
JMP	Jump
LI	Load accumulator immediate
LIS	Load accumulator short
LISL	Load ISAR-lower 3 bits
LISU	Load ISAR-upper 3 bits
LM	Load memory
LNK	Link carry into accumulator
LR	Load register (5 types) Scratchpad Program counter ISAR Status Data counter
NI	Logical AND accumulator immediate
NM	Logical AND memory accumulator
NOP	No operation
NS	Logical AND scratchpad and accumulator
OI	Logical OR immediate
OM	Logical OR memory with accumulator
OUT	Output
OUTS	Output short
PI	Push program counter into stack register Set program counter to new location
PK	Push program counter into stack register Set program counter from scratchpad
POP	Put stack register into program counter
SL	Shift left
SR	Shift right
ST	Store memory
XDC	Exchange data couhters
XI	Exclusive OR immediate
XM	Exclusive OR accumulator with memory
XS	Exclusive OR accumulator with scratchpad

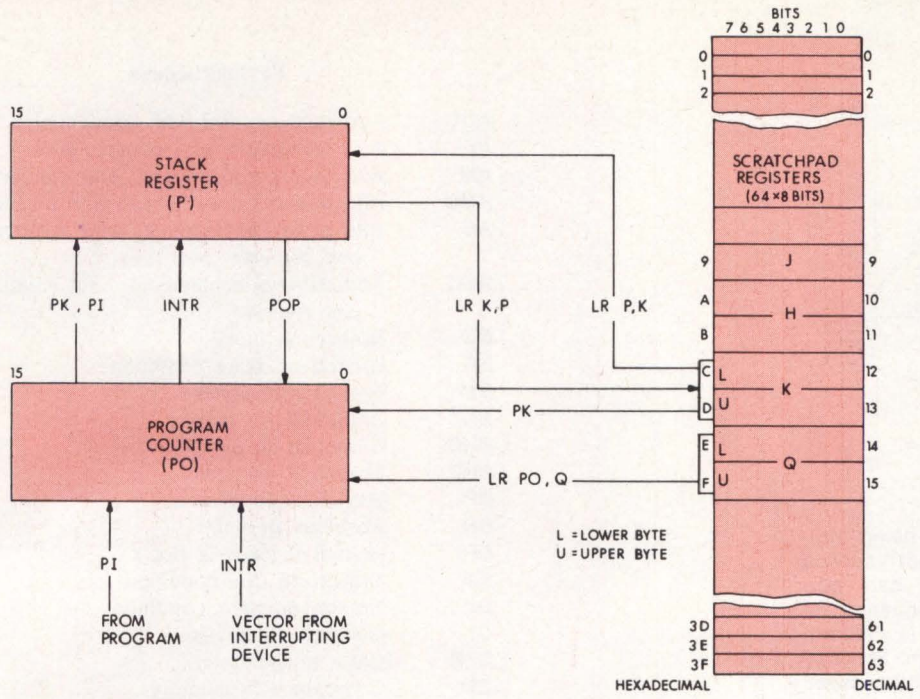

Fig 3 Register architecture. Instructions link 16-bit wide program counter (PO) and stack register (P) with K and Q registers in 64-register scratchpad. PO contains 16-bit address of next instruction to be executed—either subroutine, interrupt service routine, or main program. P acts as temporary storage location for one 16-bit program address, suitable when multilevel nesting is not used. K and Q each comprise upper-order byte (8-bit) register (U) and lower-order byte register (L)

One-Level Subroutine or Interrupt

Instructions normally used to call a subroutine (one level deep) in an F8 microcomputer are given in Fig 4. SUBA1 is the symbolic name of the 2-byte address of the subroutine, and PI causes the return address (XXXX) to be saved in the stack register (P). POP reverses the procedure at the end of the subroutine; thus, the PO is reloaded with the address saved in P, causing program flow to return to the next instruction in the main flow (XXXX). Response to an interrupt from the main flow is similar to this subroutine example, except that the interrupt causes a path to the interrupt service routine with the INTR address (vector) being supplied by the interrupting device and loaded into PO (see Fig 3).

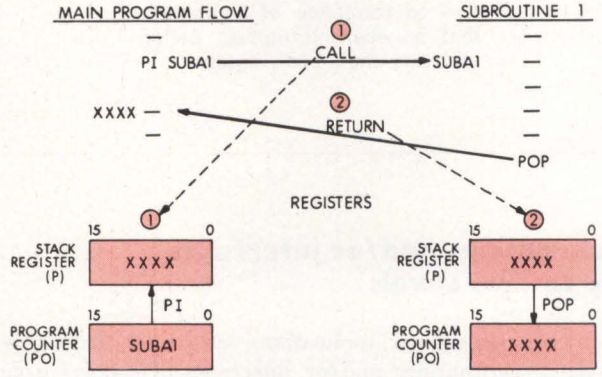

Fig 4 One-level subroutine. During call 1 to subroutine, return address (two 8-bit bytes) is stored in stack register (P). After subroutine execution, POP 2 returns address to program counter (PO) from P

Two-Level Subroutines or Interrupts

Instructions given in Fig 5 can be used to call a second subroutine or to respond to an interrupt from SUBA1. In this case, PI SUBA1 transfers the program flow to SUBA1 while saving the return address (XXXX) in P. Subroutine 1 now transfers the contents of P to K in preparation for another subroutine or an interrupt. Note that, if an interrupt occurs during the PI SUBA1-LR K,P sequence, it will not be serviced until after the LR K,P instruction because PI is privileged (not interruptible). Subroutine 2 is called by PI SUBA2, which saves YYYY in P that was just vacated. Program flow transfers to Subroutine 2, and the POP instruction reloads PO with YYYY from P. At the end of Subroutine 1, the return address is in K, so a PK is used to load XXXX into PO, thereby returning to the main program. Note that LR P,K followed by POP could have been used in place of the PK instruction, but would be one byte longer.

Three-Level Subroutines or Interrupts

Three levels of subroutines or interrupts can be handled by using scratchpad register Q to save a return address. Fig 6 shows programming with three levels of subroutines; two levels of subroutines plus one interrupt would be handled in the same manner. The first subroutine is called from the main program and the return address is saved in P. At the beginning of SUB1, the contents of P are transferred to the K register in preparation for the second subroutine call or interrupt. This second call uses the just vacated P register to store the

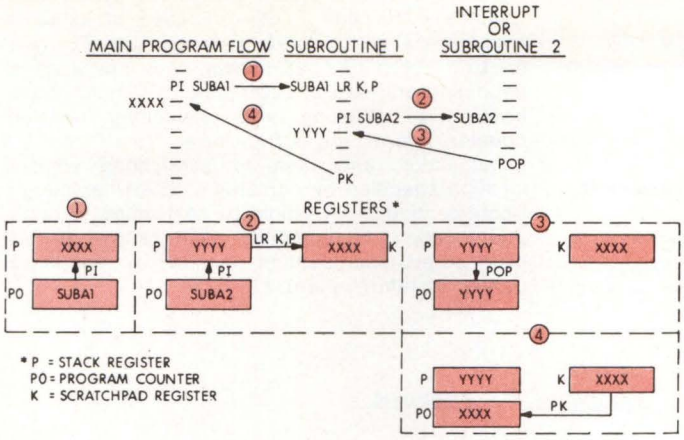

Fig 5 Two-level subroutines. Two levels are handled by storing first-level address (XXXX) initially in stack register (P) and then in scratchpad register K, while second-level address is moved into P. Conversely, main program resumption is achieved by first returning YYYY to PO and then XXXX. Subroutine 1 has 1-byte instruction overhead (LR K, P) to accomplish this 2-level nesting

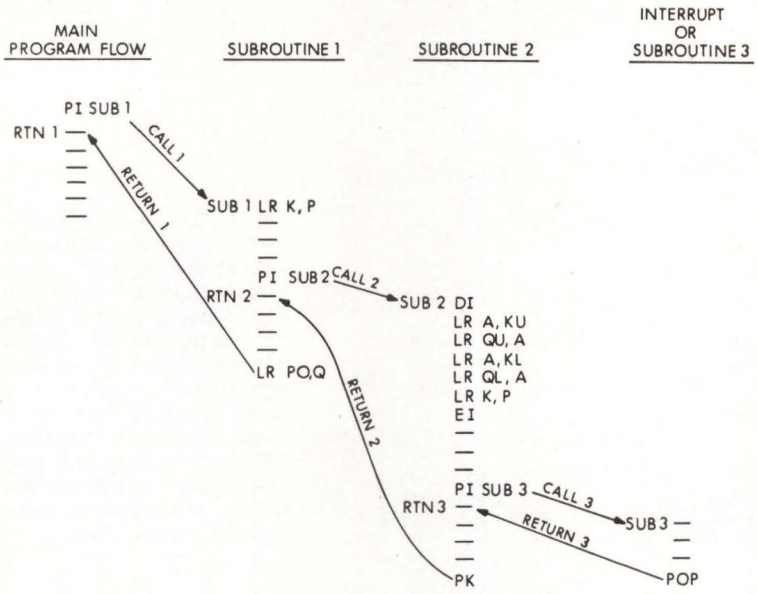

Fig 6 Three-level subroutines. Upper- and lower-byte registers of K and Q are loaded, in turn, via accumulator to hold return addresses for two levels while P holds third. Specialized instructions PK and LR PO,Q reduce overhead instructions involved in restoring return addresses needed to get back to main program

return address to SUB1. Upon entering SUB2, both P and K contain valid return addresses; therefore, interrupts must be disabled while the contents of K are moved to the Q register and the contents of P to K. The disable interrupt (DI) instruction blocks all further interrupts from being recognized, thereby preventing P and K from being overwritten. LR A,KU-LR QU,A instructions move the upper byte of the K register (KU) into the accumulator and then into the upper byte of the Q register (QU). Similarly, the LR A,KL-LR QL,A instructions move the lower byte of the K register (KL) through the accumulator to the QL register; thus, both bytes of K are saved in Q. Then the LR K,P instruction saves the contents of P in scratchpad register K.

Once P is clear, interrupts can be enabled by the EI instruction, allowing a third level of subroutine nesting (as shown in Fig 6) or an interrupt. Return from SUB3 is accomplished by executing the POP instruction, which loads PO with the value RTN3 from P. During the first portion of SUB2, contents of P are moved to K so that a PK instruction will load PO with the return address from SUB2 (RTN2). The return address for SUB1 (RTN1) is moved to the Q register during the first portion of SUB2 and is transferred to PO by execution of the LR PO,Q instruction.

Four or More Multilevel Subroutines or Interrupts

When using the F8 in a system with more than three levels of interrupts or subroutines, a consistent method of placing return addresses into scratchpad registers must be used to allow address recovery. In many cases, it will be desirable to stack registers other than those that already contain the return addresses. Previous examples have shown three levels deep with the three return addresses in the P, K, and Q registers. Since any further nesting would destroy the contents of either P, K, or Q, the technique used is to stack the contents of K onto the automatically expandable scratchpad registers to make room for another level.

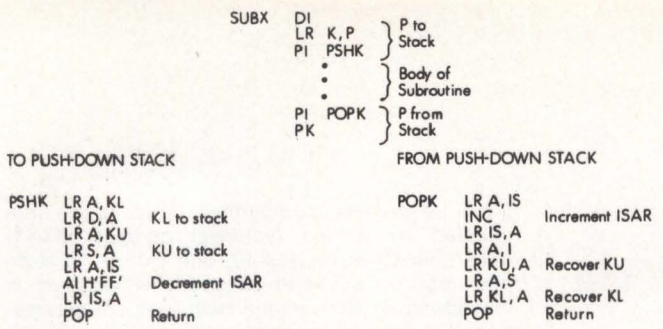

Fig 7 Software program pushdown stack. Subroutines PSHK and POPK are used to establish pushdown stack in scratchpad registers. For generalized subroutine, as shown, they are used at beginning and end of subroutine to handle housekeeping of stacking and unstacking program counter. Information is transferred from P to K via accumulator, and then to scratchpad register location specified by contents of ISAR "pointing". Decrementing ISAR points to next empty scratchpad location; incrementing ISAR returns to last filled scratchpad location on stack to permit recovery of return address

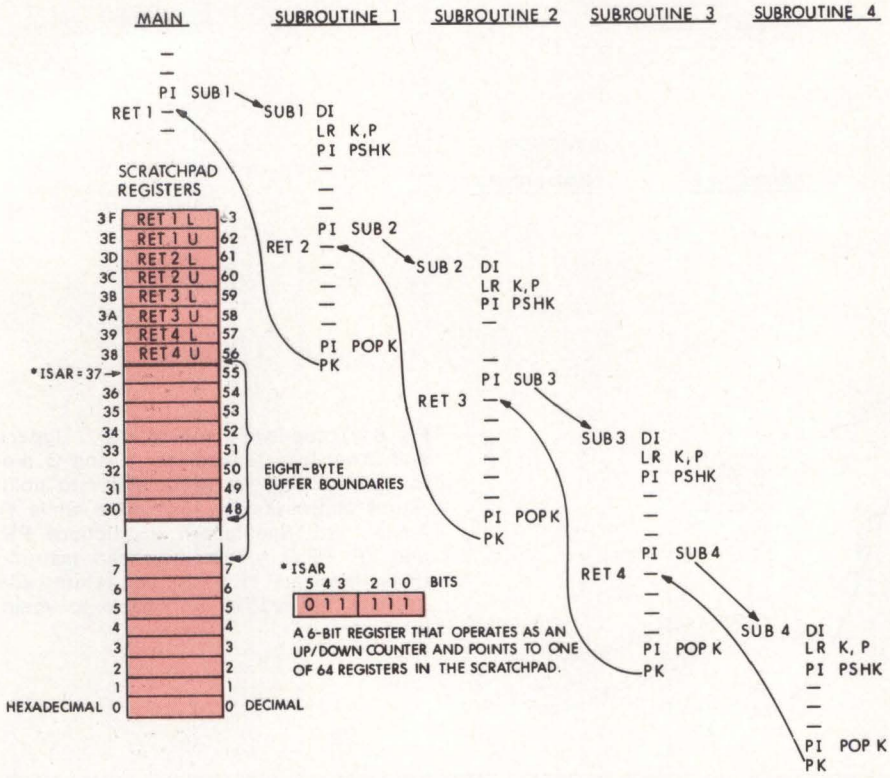

Fig 8 Deeply nested subroutines. Return addresses (RETX) are placed, in turn, on pushdown stack in scratchpad registers, allowing deep nesting limited only by number of available scratchpad registers. In most practical programs, some of these registers will contain other data, and only a few levels of nesting will be needed. ISAR functions as "stack pointer"

A generalized subroutine (shown in Fig 7) automatically transfers the contents of P to a pushdown stack [last-in first-out (LIFO) buffer] in the scratchpad registers. The programs shown in Fig 7 assume that the indirect scratchpad address register (ISAR) is being used as a pointer to the next empty location in the LIFO buffer. In addition, the ISAR must be initialized at an odd register value, probably hexadecimal 3F (or decimal 63), which is the last scratchpad register (see scratchpad register map in Fig 8).

ISAR is a 6-bit register that points to one of the 64 scratchpad registers and is divided into two 3-bit sections: ISAR-upper (bits 5, 4, 3) and ISAR-lower (bits 2, 1, 0). Instructions that use ISAR as a pointer into the scratchpad, such as LR D,A (load accumulator contents into the scratchpad register pointed to by ISAR and then decrement the lower portion of ISAR), have the option to use an auto-incrementing or auto-decrementing mode of operation. In this mode, after ISAR is used to point to the scratchpad register being accessed, the lower 3-bit section of ISAR can be incremented or decremented automatically. Incrementing or decrementing the lower three bits of ISAR produces an 8-byte (2^3) range for ISAR and thus divides the scratchpad into 8-byte segments.

In the PSHK sequence of instructions (Fig 7), use of the auto-increment/decrement feature of the ISAR places the stack register contents onto a pushdown stack. Upon entering routine SUBX by either a subroutine call or an interrupt, the return address is automatically saved in P. The disable interrupt (DI) instruction blocks all further interrupts from being recognized, thereby preventing the P and K registers from being overwritten during this stacking operation. The LR K,P instruction transfers the contents of P into the K register in the scratchpad, and a subroutine call is made to PSHK.

The first instruction executed in the PSHK subroutine loads the lower byte of the K register (KL) into the accumulator (LR A,KL) and then onto the pushdown stack using the LR D,A instruction. It has been assumed

that ISAR is pointing to register H'3F' in Fig 8; therefore, the lower-order byte (L) of RET1 is shown in the upper (last) register (decimal 63). The LR D,A instruction automatically decrements ISAR (lower half), leaving it pointing to the next empty register location in the push-down stack, H'3E' or decimal 62. Instruction pair LR A,KU-LR S,A transfers the upper byte of the K register [RET1 upper (U) byte] into location H'3E' in scratchpad; however, in this case ISAR is not modified. Auto-decrementing is not used in this case because it cannot decrement ISAR across the even buffer boundary at H'38' (outside the 8-byte range); therefore, an alternate method of decrementing ISAR is used. To do a full decrement of ISAR, its contents are loaded into the accumulator (LR A,IS) and a −1 is added to the accumulator (in 2's complement digital coding, −1 is represented by H'FF'). After the subtraction is complete, the accumulator's value is returned to the ISAR (LR IS,A).

Every time another level of subroutine or interrupt is encountered, this movement of return addresses onto the pushdown stack occurs, resulting in the condition shown in Fig 8 while in the fourth level. Note that the ISAR is pointing to the next available register location (H'37') in the pushdown stack, waiting for the next return address to be pushed. When both P and K are cleared (contents saved in the stack) in the body of the subroutine and a call is allowed to another subroutine or interrupt of this format, POPK is called to recover the subroutine return addresses (last-in first-out) from the stack and to return them to the K register. In the case of the POPK routine, the first increment of ISAR may cross an 8-byte boundary (see Fig 8, ISAR from H'37' to H'38'); therefore, its contents are loaded into the accumulator for this addition. LR A,IS-INC and LR IS,A instructions accomplish the addition of one to the ISAR. LR A,I and LR KU,A instructions retrieve the value stored in location ISAR = H'38', return it to the upper byte of the K register (this was the last byte stored), and then autoincrement the ISAR pointer. ISAR now points to register location H'39' and the LR A,S-LR KL,A instructions retrieve RET4L from the stack and place it into the lower portion of the K register. ISAR is not incremented but is left pointing to register location H'39', because this is the first available location in the stack for the next PSHK routine. Should another POPK routine be encountered, the ISAR will move up the scratchpad registers retrieving the saved return addresses.

At the end of each subroutine, PI POPK followed by PK will be executed to unload the stack and return program flow to the correct return address. If the interrupting device service routine needs to call a subroutine, the contents of stack register P must be pushed onto the stack using the methods previously described. Note also that interrupts are allowed at any time except during execution of PSHK and POPK routines, since their return address is stored in P.

In many cases it is desirable to save the major registers within the CPU when an interrupt is serviced. Saving registers on the stack frees all the CPU's computing power for use by the interrupt service routine. Saving the registers on the stack rather than in direct scratchpad locations makes the subroutine or interrupt service routine re-entrant (ie, the routine calls itself without destroying scratchpad register locations).

```
PSHAW   LR D,A      Accm to stack
        LR A,J
        LR S,A      J Reg to stack
        LR J,W      Wreg to Jreg
        LR A,IS     ISAR to A
        AI H'FF'    Decrement A
        LR IS,A     A to ISAR

POPAW   LR A,IS     ISAR to A
        INC         Increment A
        LR IS,A     A to ISAR
        LR W,J      J reg to W
        LR A,I      J from stack
        LR J,A      into J reg
        LR A,S      Accm from stack
        POP         Return to caller
```

Fig 9 Stacking other registers. Program techniques described previously can be used to stack other F8 registers, such as accumulator and status word

The same programming technique as described previously can be used to save the contents of the accumulator and the status register on the stack (see Fig 9). Other F8 registers could be saved using this technique; however, they must be pushed in pairs in order to leave ISAR pointing to an odd register location. Since K, DC (data counter) and DC1 (auxiliary data counter) are all 16-bit registers, this should not be a limitation.

Conclusions

Several programming techniques have been described for handling subroutines and interrupts in F8 microcomputer systems. Many applications for which the F8 is suited (programmable controllers) will have minimal subroutines or a minimum number of interrupts so that only the internal P and K registers will be needed to hold return addresses.

In cases where deeply nested subroutines or multiple interrupts must be handled, a pushdown stack can be created in the scratchpad registers or in external memory. Return addresses in this stack, as well as general-purpose registers, can be saved using the software routines that have been described.

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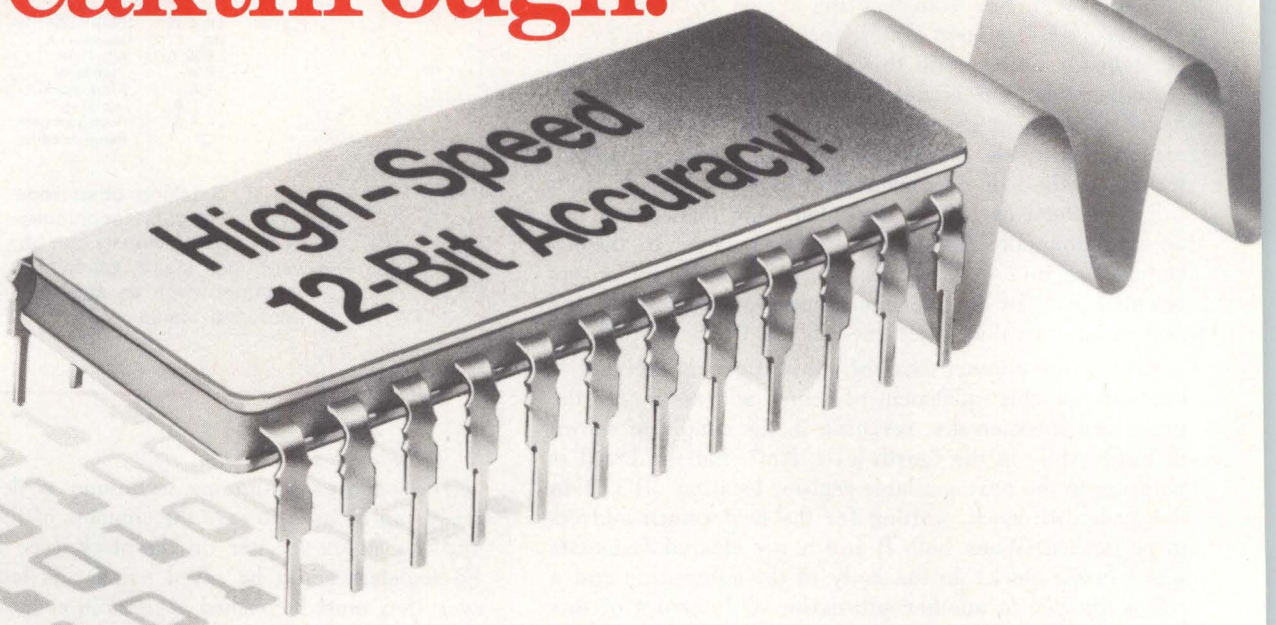

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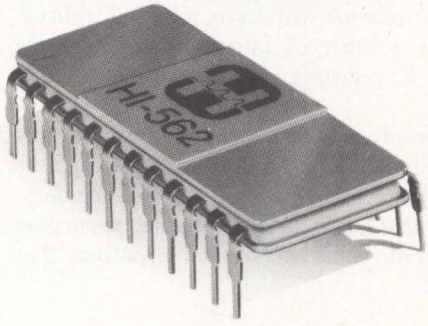

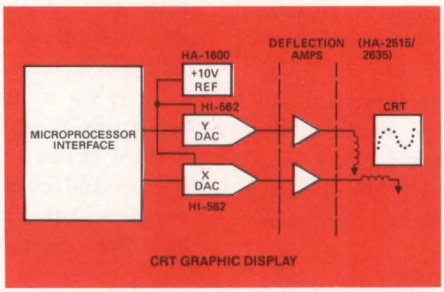

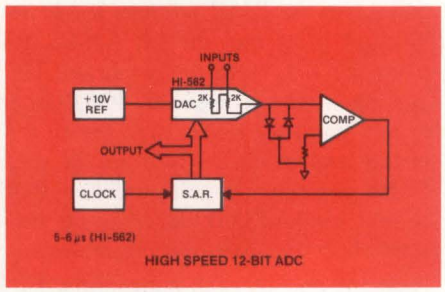

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DMA CONTROLLER CAPITALIZES ON CLOCK CYCLES TO BYPASS CPU

A direct memory access controller can enhance system throughput, especially for large complex microcomputer systems where processing and I/O operations must function at fast rates, by transferring data directly between memory and peripheral devices, effectively bypassing the CPU

Joseph Nissim Rockwell International, Microelectronic Device Division, Anaheim, California

Of the two common methods of transferring input/output data, program controlled and direct memory access, the former is widely known for economy, the latter for speed. Program controlled input/output is particularly useful for low speed interface requirements, as well as for dedicated peripheral applications. However, for microcomputer systems where both processing and input/output operations are required to operate at medium to high speeds, the direct memory access method is preferable, and probably mandatory.

Program controlled (or software) input/output (I/O) refers to the technique of transmitting data to and from memory via the central processing unit (CPU) and the I/O device. To load memory from a peripheral device, for example, data would flow first from I/O device to CPU, then from CPU to memory. This data flow is typically accomplished in software by a read instruction (I/O to CPU) addressing the proper I/O device, followed by a load instruction (CPU to memory) addressing the desired memory location.

In contrast, direct memory access (DMA) I/O refers to a technique by which data are transferred directly between a peripheral and memory, using a DMA controller (DMAC). In other words, data transfer is transparent to the CPU, and thus requires no software.

DMA data transfer, however, affects system operation. The DMAC must first temporarily halt the CPU, and then generate the desired data, address, and control signals required to transfer the data directly to memory. Halting the CPU allows the DMAC to assume control of driving the buses and some of the control lines.

Several DMA transfer methods exist, such as the halt method, the multiplex DMA/CPU method, and the "cycle steal" method. The halt method is simplest: the CPU is shut down while DMA transfer occurs. Its disadvantage is the relatively long time it takes to switch the CPU on and off the bus.

The multiplex DMA/CPU method works by splitting each memory cycle time (clock time) into two time slots: one for the CPU and the other for DMA. This method results in the highest transfer rate as well as the highest CPU execution rate when compared with the other methods. However, it requires high speed memories to accomplish these results.

For applications considered in this article, such as floppy discs, cassettes, cathode-ray tube (CRT) peripherals, and point-of-sale (POS) systems, the cycle steal method is considered best on a cost/performance basis. In conjunction with a DMAC, this method is also particularly useful when DMA transfer requires a fast response. Cycle stealing refers to obtaining CPU clock cycles for DMA transfer without disrupting CPU program execution. In applications where the CPU uses the entire memory bandwidth, DMA would cause CPU performance degradation, unless restricted to a data rate significantly lower than

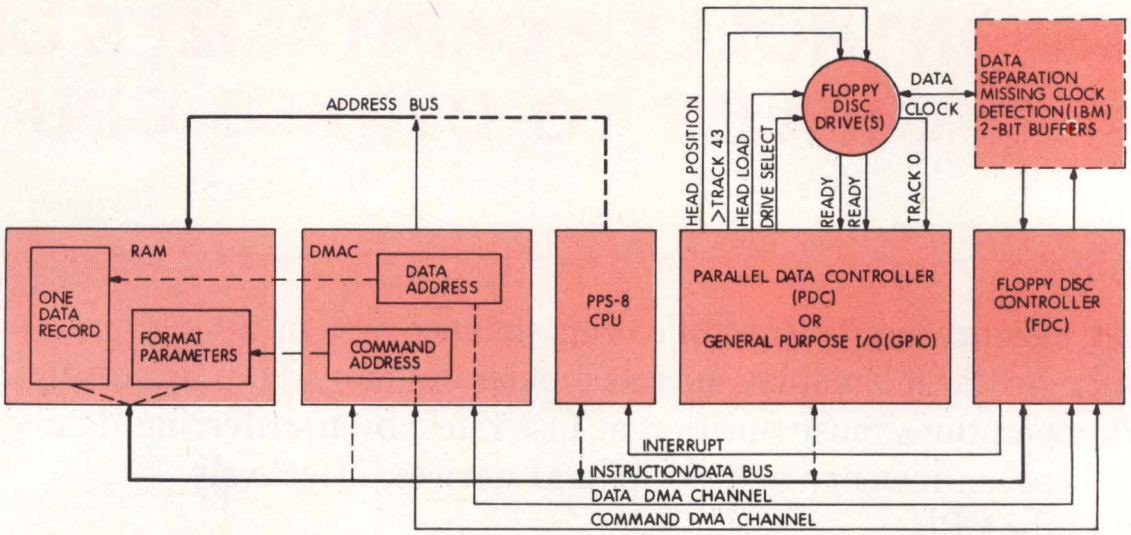

Fig 1 Typical DMA I/O operation. Block diagram illustrates interface between PPS-8 microcomputer system and floppy disc system. In addition to DMA controller, other intelligent I/O devices, such as floppy disc controller (FDC) and parallel data controller (PDC) or general-purpose I/O device (GPIO), aid in transfer of data

that of the CPU. For instance, a DMAC interfaced with a PPS-8 microcomputer can transfer data within 1½ clock cycles after setting the required CPU control line (DMRA—direct memory request/acknowledge). Data transfer can then proceed at the clock rate (250 kHz) when operating in burst mode. (This mode refers to a string of data moving at the highest possible rate—the clock rate.) Initial delay to DMA access may be incurred if the highest priority interrupt is pending, or the CPU is executing I/O instructions. A block diagram of a typical DMAC I/O operation, a floppy disc interface to a microcomputer, is shown in Fig 1.

The advantages of using a DMAC, together with other intelligent I/O devices such as a floppy disc controller (FDC), can result in significant enhancement of system throughput, especially for large complex microcomputer systems. Capabilities of a special DMA controller, its organization, operations, timing, and other characteristics, will be discussed, and a comparison made between CPU program control and DMA control methods.

CPU Program Control

Due to the high rates associated with floppy discs, the CPU program control approach requires total microcomputer dedication during data handling. This dedication means that other microcomputer peripherals can not be serviced while in a disc read or write operation. Consequently, interrupts generated by other system elements must be disabled during these operations.

In designing such a system, allowances must then be made to permit 100% system dedication to the floppy disc during read and write operations. This can be accomplished in the following ways.

(1) If desired, the system can be designed so that other peripherals will not need service during a floppy disc data transfer. Such a design, however, becomes a disadvantage in a multiperipheral real-time environment, because dedication is needed and the other peripherals cannot be serviced. However, for a small peripheral-oriented system, such an approach would be most cost-effective.

(2) One microcomputer can be dedicated to the disc while another handles peripherals that would never interface with disc operations. The second microcomputer could be a peripheral control processor that is subservient to an executive processor. The executive processor could be another microcomputer, a minicomputer, or a large computer. Such a setup would be advantageous for real-time, high throughput system requirements. Its disadvantage, of course, would be the high cost of the various computers needed.

(3) A microcomputer can be dedicated to the disc subsystem. This middle-of-the-line technique is used to "offload" the throughput requirements for the disc subsystem. Its cost-effectiveness is higher than that of the first method discussed but lower than that of the second.

DMA Control

By using direct memory access and CPU cycle stealing techniques, a DMAC considerably improves the data transfer rate of the floppy disc system interface. For instance, only about 1% of system resources would be tied up during a sector address search. This search time is required to transfer the 16 format control block parameters, once for each sector, under DMA control (see Fig 2).

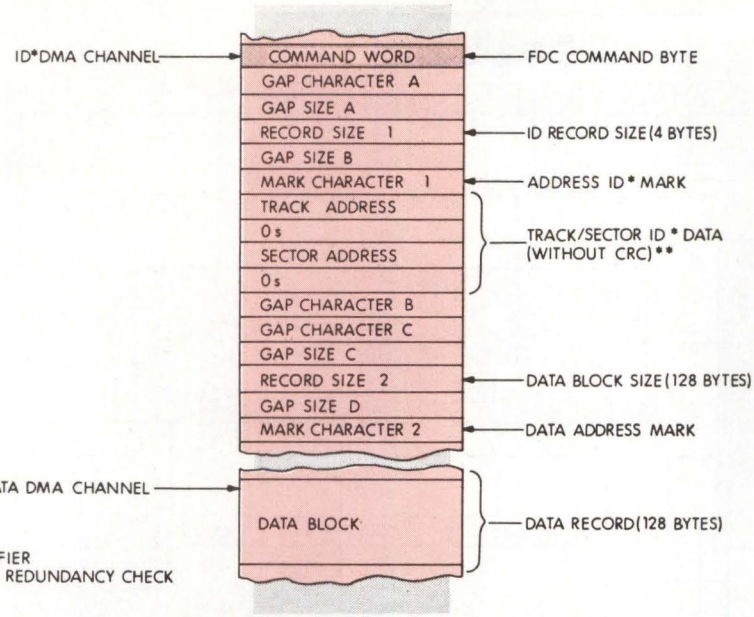

Fig 2 Format parameters. In floppy disc search procedures, up to 32 sectors (IBM compatible) comprise each track. Every sector has identifier (ID) preceding it which denotes track and sector addresses. Sixteen parameters shown make up preamble which precisely identifies proper sector

During data sector transfers (for standard disc density recording at 250 kHz), 12.5% of the system resources would be activated. Once each 32 μs, a data byte (8 bits) must be transferred into or out of random-access memory (RAM) via DMA control. This amounts to one clock cycle of system time (4 μs).

Data operations are full sector transfers under DMA control. When the FDC assembles a byte of data during a read operation, a DMA request is made and the data byte is stored in the RAM data buffer. When the complete sector has been read, verified for accuracy, and placed in RAM, the FDC interrupts the CPU, indicating that the sector addressed has been placed in the RAM data buffer.

DMA Organization

Eight DMA request/acknowledge lines (DMA0 through DMA7) provide bidirectional communication between the I/O devices and the DMAC (see Fig 3). Each bidirectional DMA line connects to a specific I/O peripheral, meaning that an I/O request for DMA service goes directly to the DMAC, and an acknowledge pulse returns directly along the same line to the I/O device. This bidirectional communication over a single line is accomplished through the use of time-multiplexing and pulse-coding techniques. Time-multiplexing permits a single line to be shared by two different functions at separate times; pulse coding refers to notifying the I/O device on a time-multiplex line by means of a serial string of data (ie, three bits coded in binary) that end of block (EOB) has been reached.

Each DMA line (or channel) has a fixed position in a priority structure used to resolve simultaneous requests. The channels are numbered in order of priority, with DMA0 having the highest priority. An additional DMA request/acknowledge line (DMRA) provides bidirectional communication between DMAC and CPU.

Eight 14-bit address registers and eight 8-bit record length registers are included in the DMAC. Individual address registers are pointers to data memory for each of the eight channels used by the different I/O peripherals for data transfer. Record length registers are used to denote the record data length associated with a particular channel (eg, 128 bytes/record for IBM compatibility). One address register and one record length register are associated with each of the eight DMA channels. Each register can be loaded under CPU program control.

Two additional control bits are provided for each of the DMA lines. One specifies whether the RAM is to read or write when a DMA request occurs on the associated DMA line; the other is used to select a special record cycle mode (described later).

A holding register, associated with the record length registers, allows the CPU to sample the contents of any record length register. When any record length register is loaded by the CPU, the previous contents of that register are transferred to the holding register. Contents of the holding register may be read under CPU program control.

DMA Operations

Fig 4 shows a typical DMAC configuration. For simplicity, only a single I/O device, a parallel data controller (PDC), is shown connected to the DMAC. When the PDC requires DMA service, it transmits a pulsed DMA request over DMA0. The DMAC forwards the DMA request

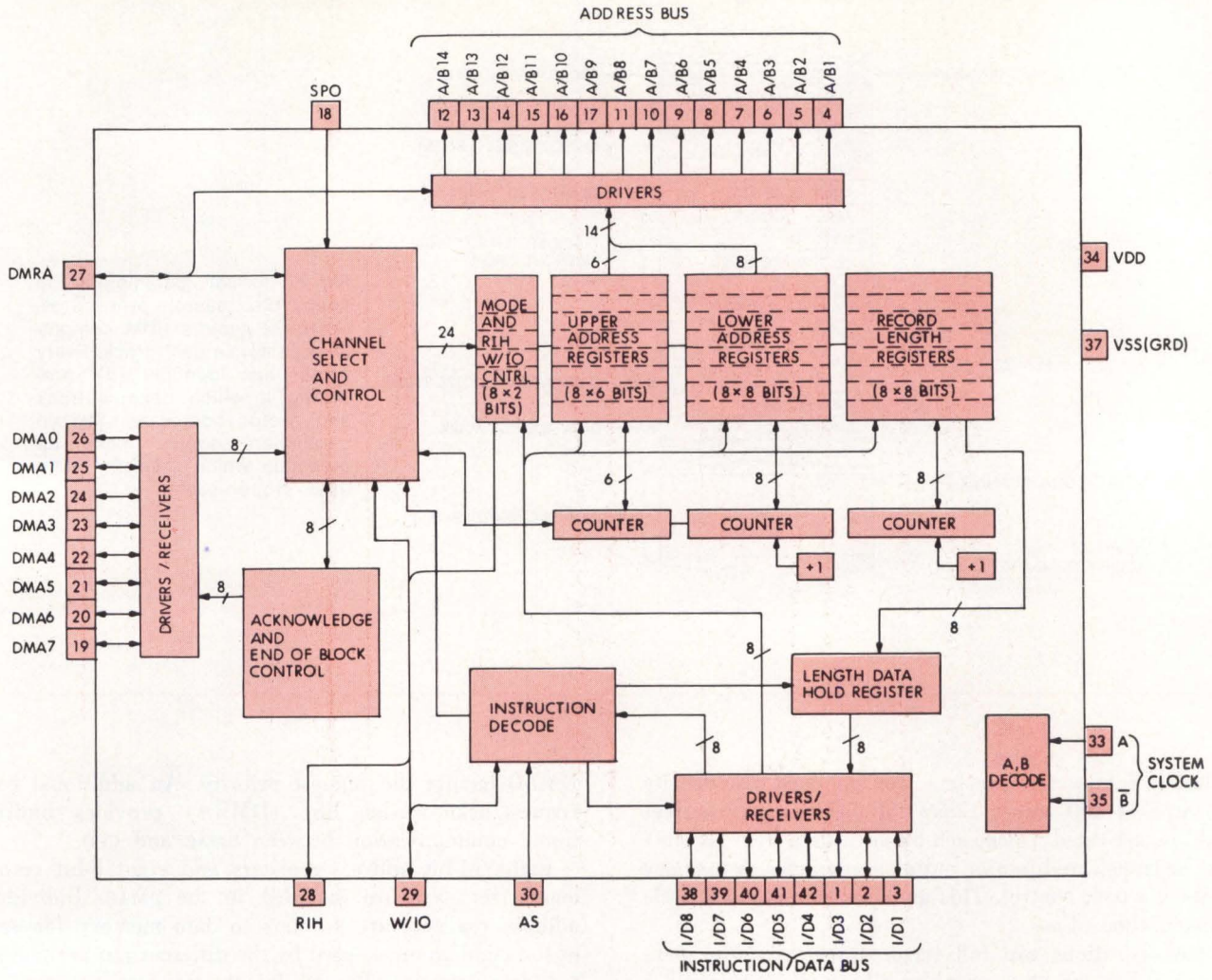

Fig 3 Direct memory access controller. Eight DMA request/acknowledge lines (DMA0 through DMA7) provide bidirectional communication between I/O devices and DMAC. Eight 14-bit (upper plus lower) address registers and eight 8-bit record length registers are associated with eight DMA channels. Holding register allows CPU to sample contents of any record length register. Instruction/data bus lines (I/D1 through I/D8) are bidirectional, while address bus lines (A/B1 through A/B14) are unidirectional

to the CPU over the DMRA line. The CPU acknowledges the DMA request, and enters a "wait" mode.

PPS-8/DMAC operations (summarized in Fig 5) begin when CPU software loads the starting address and length of the data block into the DMAC, and resumes normal program execution. When necessary, the I/O device requests DMA service from DMAC, which requests DMA action from the CPU. The CPU completes the current instruction, acknowledges the DMAC request, isolates (floats) data and address bus drivers, and "waits." (If the instruction being executed is an I/O instruction, the CPU continues program execution until it encounters a non-I/O instruction; then acknowledges the DMA request.) After acknowledging the highest priority DMA request, the DMAC drives the address bus with the contents of the appropriate address register. It also drives read inhibit control (RIH) and enable I/O device control (W/IO) false or true, depending on whether the address RAM is to read or write.

The data byte is transferred between the I/O device and RAM either onto or from the data bus, and the CPU resumes program execution. After each byte is transferred, the DMAC increments the appropriate address register and record length register. DMA operations continue until one of the following events occurs: (1) I/O device ceases to request DMA service; (2) record length register makes a transition from 255 to 0; (3) lower address register makes a transition from all 1s to all 0s; (4) interrupt 0 (INT0) triggers CPU; or (5) DMAC receives a request on a higher priority channel than that currently being serviced.

When the I/O device ceases to request DMA service, the DMAC, in turn, drops its request to the CPU (provided that no other DMA requests are present), and the

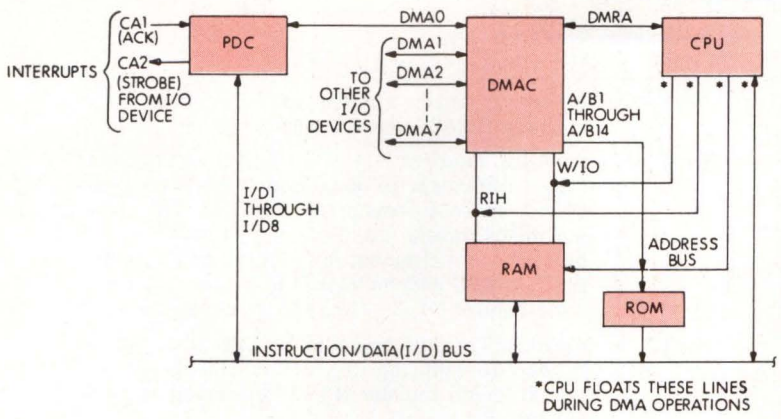

Fig 4 Typical DMAC configuration. Bidirectional line (DMA0) interfaces parallel data controller (PDC) to DMAC. DMAC forwards single I/O device request to CPU over DMRA line, and CPU acknowledges DMA request at completion of current non-I/O instruction. If instruction is I/O type, CPU continues program execution until it has completed non-I/O instruction

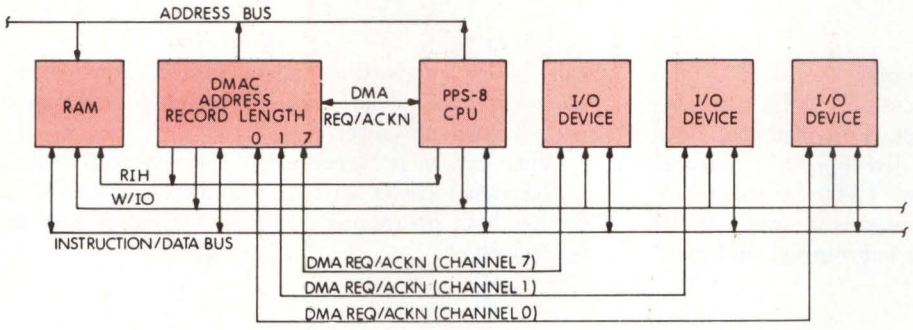

Fig 5 PPS-8/DMAC operations. On receiving CPU acknowledge signal, the DMAC (1) drives acknowledge signal over highest priority line currently requesting service, (2) drives address bus with contents of appropriate address register, and (3) drives RIH and W/IO false or true, depending on whether addressed RAM is to read or write. I/O device either drives data onto, or samples data from, instruction/data (I/D) bus

CPU resumes program execution. If additional DMA requests are present, the DMAC maintains its request to the CPU and automatically switches to the highest priority channel requesting service.

When the record length register makes the transition from 255 to 0, the requesting I/O device is informed of the end-of-block (EOB) condition (via a pulse-coded signal transmitted over the DMA line), and the DMAC drops its request to the CPU, allowing resumption of CPU program execution. If the I/O device continues to request DMA service after being informed of the EOB condition, the DMAC delays for three clock cycles and then again requests DMA service from the CPU. Thus, when the record length register makes the transition from 255 to 0, the CPU is allowed to execute instructions for a minimum of three clock cycles before the DMA request is again honored. The CPU will not honor the DMA request at the completion of the current instruction if that instruction is an I/O command; ie, the CPU will continue to execute instructions until it has executed a non-I/O command, at which time it will honor the request.

When the lower address register makes a transition from all 1s to all 0s, a carry is propagated through the lower address register and into the upper address register; ie, the upper address register is incremented by one. Each time this operation occurs, the DMAC drops the acknowledge signal to the I/O device and the request signal to the CPU. Two clock cycles later (assuming that only the initial I/O device is still requesting DMA service), the DMAC again requests DMA service from the CPU.

When CPU Interrupt 0 (INT0) is triggered, the DMAC is allowed to complete the byte transfer currently in

CPU Instructions to DMAC

Command (Mnemonic)	Op Code Address (4 Bits)	Op Code Command (4 Bits)	Function
Load address register, lower (LARL)	XXXX	0101	A→ARL. Transfer contents of CPU accumulator to lower DMAC address register N
Load address register, upper (LARU)	XXXX	0110	A→ARU. Transfer contents of CPU accumulator (bits 1 through 6) to corresponding bits of upper DMAC address register N. Bit 7 of CPU accumulator is transferred to channel N mode control bit (1 = normal mode; 0 = record cycle mode). Bit 8 in CPU accumulator is transferred to read/write control bit (0 = read; 1 = write)
Load record length register (LRLR)	XXXX	0111	A→RLR. Transfer contents of CPU accumulator to record length register N. Previous contents of record length register N are transferred to holding register
Read holding register (RHR)	XXXX	1111	HR→A. Transfer contents of record length holding register to CPU accumulator

Notes: N = Where N is number coded in lower 3 bits of instruction address field.
A = CPU Accumulator
AR = Address Register
RLR = Record Length Register
HR = Holding Register
Suffix U = Upper portion of register
Suffix L = Lower portion of register
Prefix L = Load
Prefix R = Read

progress. Thereafter, the CPU ignores the state of the DMRA and resumes program execution. INT0 can also be used as a power-fail interrupt. For instance, in a cash register application, upon detection of a power failure by hardware circuitry, an INT0 is generated. The CPU will recognize this interrupt with minimal delay, branch out to the power-fail subroutine, and typically store all pertinent data into a nonvolatile type memory (core memory, for example) for reconstruction upon return of power.

When power is turned on, the synchronized power-on signal (SPO) clears all DMA acknowledge signals and no further DMA operations occur until another DMA request is received.

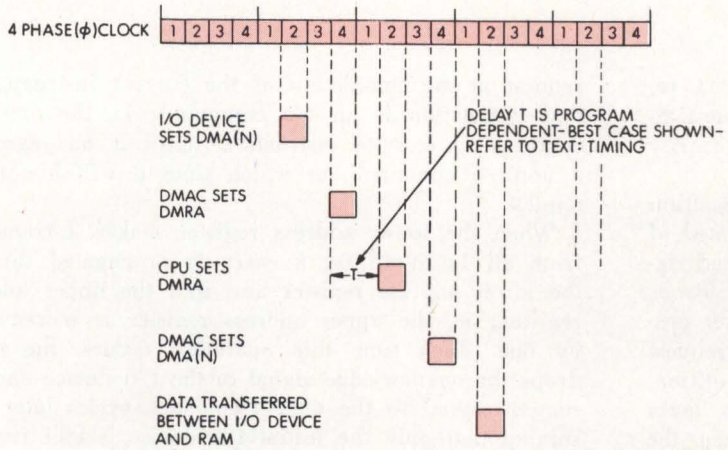

Fig 6 General DMA timing diagram. A one-half cycle delay exists from time the DMAC receives request from I/O device until it, in turn, requests service from CPU. Best case occurs when CPU is executing a non-I/O instruction; then, there is one-half clock cycle delay until CPU sends acknowledge pulse to DMAC. In worst case, CPU is executing one (or more) of series of I/O commands; then, maximum delay could be 4½ clock cycles

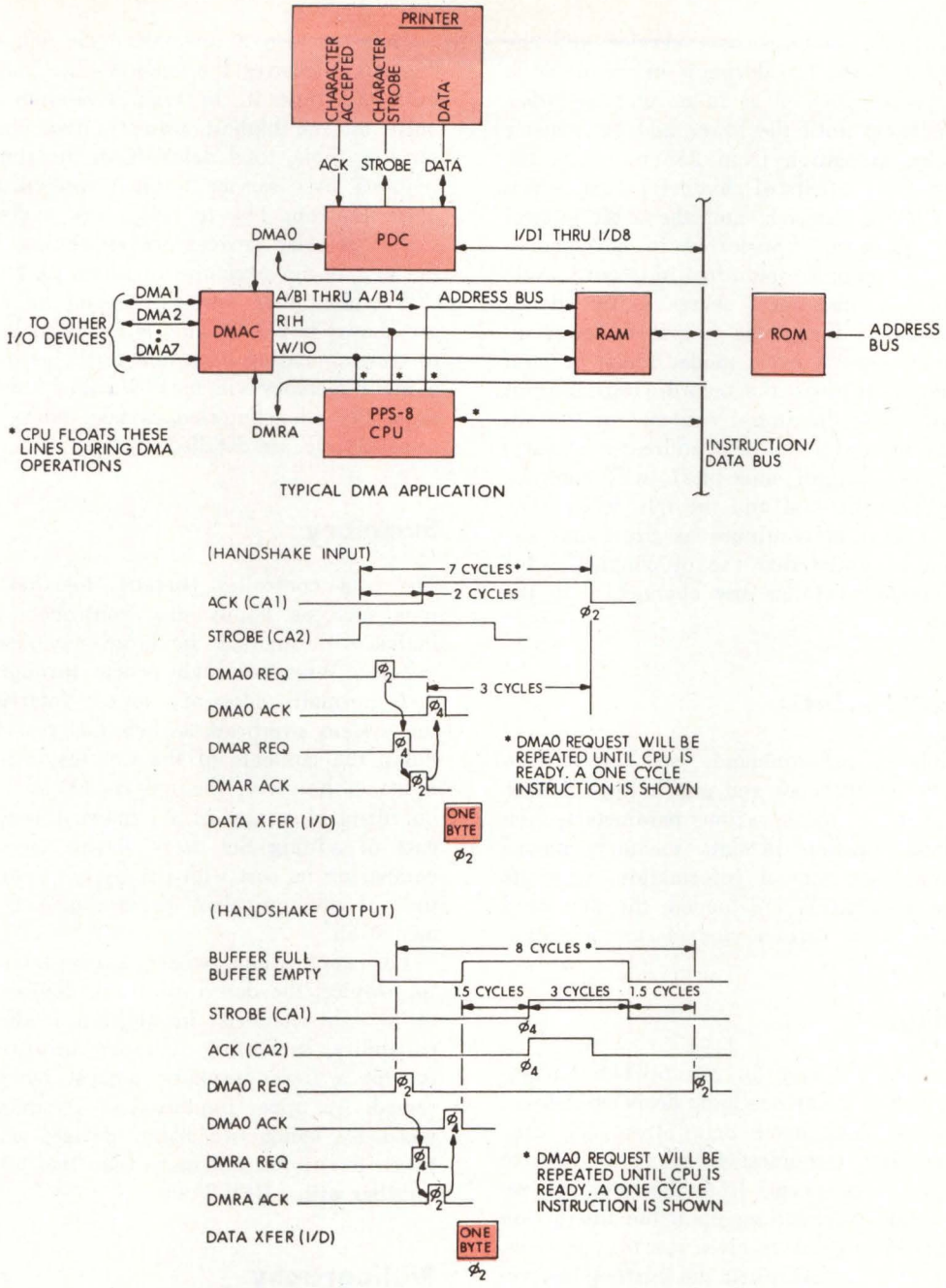

Fig 7 Typical DMA application. Handshake method of input/output communication between peripheral, printer, and main memory via DMAC is depicted. Various time slots in which requests and acknowledges take place, as well as data transfer time, are shown

When the DMAC receives a DMA request on a higher priority DMA channel than that currently being serviced, it completes the byte transfer currently in progress and drops the acknowledge signal on the original (lower priority) channel. The DMAC automatically switches to the higher priority channel and continues the DMA operation.

Record Cycle Mode

A control bit associated with each of the address registers commands a special record cycle mode, which is available for any of the first seven channels (0 through 6). When this control bit (loaded from the CPU) is set at one, normal operation occurs; when it is reset to zero, record cycle mode is commanded.

When an I/O device requests DMA service and the channel associated with the I/O device is in record cycle mode, the bytes are transferred as in normal operation to the channel registers until the lower address register (8 bits) makes the transition from 255 to 0. At the time of transition, the contents of channel 7 (the record length register, address register, and the 2-bit control register) are automatically transferred to corresponding registers of the channel operating in record cycle mode. In other words, channel 7 serves as the identifier (ID) channel and is designated to refresh the channel operating in the record cycle mode. Thus, as long as the DMA request is present, the record (beginning at the address specified by the initial contents of the address register and ending at the next address boundary, within 256 address location multiples) will continue to be transferred between RAM and the I/O device. The rest of the DMA operation continues as previously described. It should be noted that use of channel 7 for DMA service is precluded when any channel is in the record cycle mode.

DMAC Instruction Set

The DMAC responds to four commands (see Table) from the PPS-8 CPU: three out types and one in type. Under program control, the CPU loads various parameters, such as starting address location in data memory, record length information, and control information, into the DMAC. Once these parameters are loaded, the CPU need not intervene again until further changes are required.

General Timing

General DMAC timing is given in Fig 6. The 4-phase clock allows time slots for various logic decision-making. There is a one-half clock cycle delay from the time that the DMAC receives a request from an I/O device until it, in turn, requests service from the CPU. CPU response time is variable, depending upon the instruction being executed at the time it receives the DMA request. The best-case condition exists when the current instruction is a non-I/O type whose execution will be completed during the clock cycle following the one in which the request is received. In this case, there is also a one-half clock cycle delay from the time the CPU receives the request until it sends an acknowledge pulse to the DMAC.

The worst-case condition exists when the CPU is executing one or a series of I/O commands. The CPU will continue program execution until it has executed a non-I/O instruction before it will acknowledge the DMA request. Completion of the I/O command may take one or two clock cycles; execution of the next instruction may require one, two, or three cycles. Thus, if the CPU is executing an I/O command at the time that it receives the DMA request, the maximum delay before it acknowledges the request will be 4½ clock cycles (assuming the command following the I/O command is a non-I/O type).

There is also a one-half cycle delay from the time the DMAC receives the acknowledge pulse from the CPU until the time it, in turn, transmits an acknowledge pulse on the highest priority DMA channel requesting service. Thus, total delay from the time an I/O device requests DMA service until it receives an acknowledge pulse is from 1½ to 5½ clock cycles (assuming no higher priority devices are requesting DMA service and the CPU is not executing a series of I/O commands).

A typical DMA application and its associated timing are shown in Fig 7. This is a typical handshake method of communicating back and forth between a printer and a main memory via DMA. Various time slots in which requests and acknowledges take place, as well as data transfer time, are detailed.

Summary

The DMA controller (DMAC), together with intelligent I/Os such as floppy disc controller, can significantly increase throughput in large complex microcomputer systems. Wherever high system throughput is required, it is normally necessary to use interrupts that add to the system overhead, switch the CPU in and out, and dump the contents of the CPU-resident registers. Using a DMAC, however, the CPU is halted temporarily without disturbing any of its internal registers. Additional cost of adding the DMAC device can be justified, by comparing its cost with the overall system cost and with that of an equivalent programmed I/O system implementation.

For applications where many I/O devices compete for service, the described DMAC device gives priority to up to eight channels; in addition, it allows for a nesting capability. In nesting, a higher priority request can interrupt a lower priority request currently being processed. An upper limitation of 16 channels can be serviced by using two DMAC devices and switching between them; but not more than two DMACs can be used together with a PPS-8 CPU.

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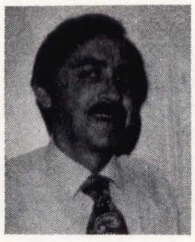

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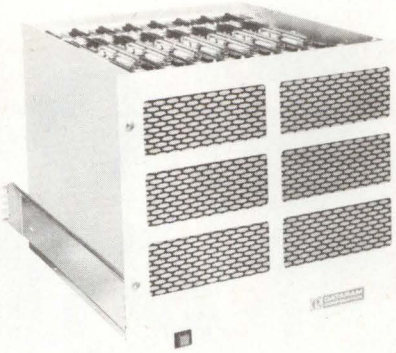

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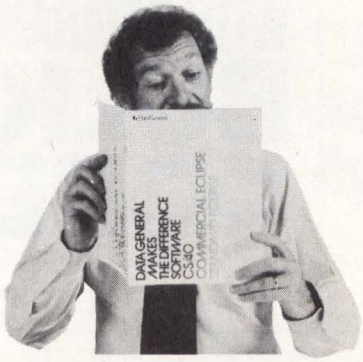

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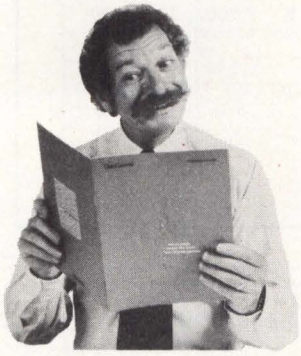

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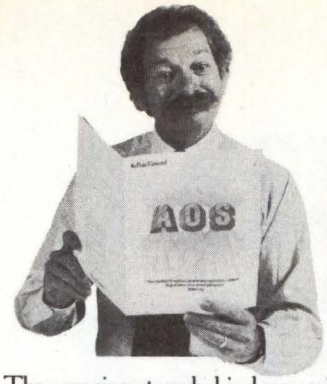

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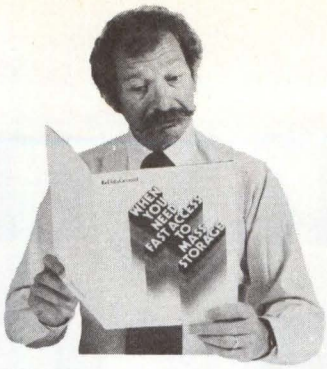

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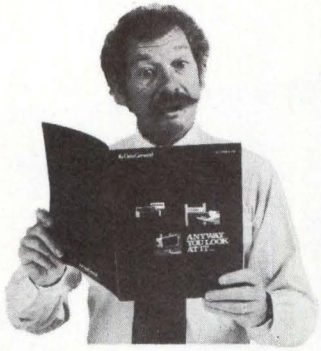

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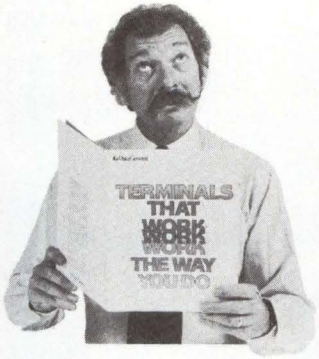

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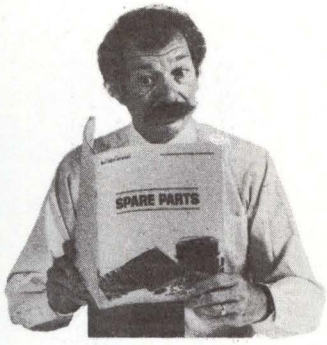

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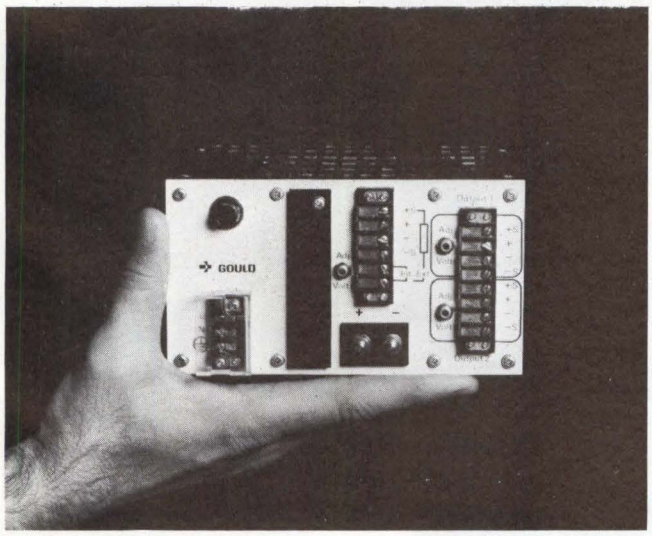

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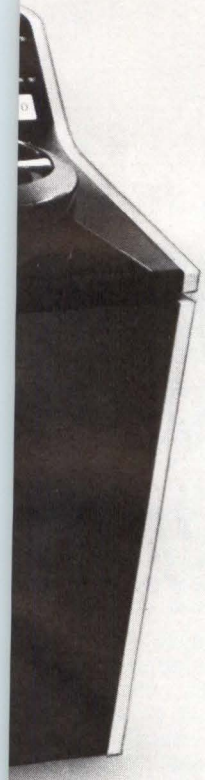

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MICROCOMPUTER INTERFACING: ANALOG MULTIPLEXERS

Jonathan A. Titus and Christopher Titus
Tychon, Inc

Peter R. Rony and David G. Larsen
Virginia Polytechnic Institute & State University

In many analog-to-digital converter applications, it is too expensive to dedicate one converter to each sensor.[1] An alternate approach is to share one converter among several sensors, which constitutes multiplexing, since many signal sources share a common transmission path to a single receiving device, in this case, the analog-to-digital converter.

A multiplexer may be a rotary switch having multiple taps, or positions (Fig 1); a small-signal reed relay available in a dual inline package (DIP) the size of a 14- or 16-pin integrated circuit (IC) device; a semiconductor switching device based upon complementary metal-oxide semiconductor (CMOS) or metal-oxide field-effect transistor (MOSFET) technology; or a complex communication device used by telephone companies. Various features of semiconductor switches make them practical for multiplexers. Some advantages are small size, ie, housed in a standard DIP; direct compatibility with transistor-transistor logic (TTL) signals; built-in onboard digital decoders for channel select; positive and negative signal inputs, ie, bipolar operation; high speed switching; long life (no mechanical wear); low contact resistance of less than 100 Ω; and high off-state resistance of 10^9 Ω typical. Important concepts related to multiplexers are detailed in the listing of Terminology.

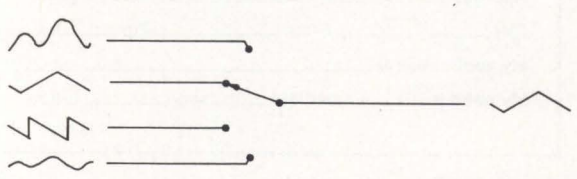


Fig 1 Simple rotary switch multiplexer showing four possible inputs

Terminology for Semiconductor Analog Multiplexers

Bandwidth	Ability of the multiplexer to pass a signal at a particular frequency once it is turned on. Bandwidth is the −3-dB point; it is equivalent to small signal bandwidth associated with sample-and-hold (S/H) devices.
Crosstalk	A measure of the amount of signal input to an "off" channel that appears at the output of the multiplexer, superimposed upon the signal passed through the "on" channel. This is a direct function of the frequency of the signals, since semiconductor switches are capacitively coupled within the IC chip. The higher the frequency, the greater the crosstalk. This phenomenon is similar to the feedthrough problem of S/H devices.
Settling Time	Time necessary for the multiplexer's output to be within a certain error percentage of the input signal once the channel is selected, or turned on. It may be specified as either the semiconductor switch's switching time plus analog output settling time, or as analog output settling time alone.
Switching Transients	Transient voltage spikes that appear at a multiplexer's output when the multiplexer is switched from one channel to another and one of the switches is turned off. Such spikes may cause inaccurate measurements if output is sampled, digitized, or integrated during this time.
Throughput Rate	A measure of the fastest channel-to-channel switch rate that may be used if rated accuracy, generally 0.01%, is to be achieved.

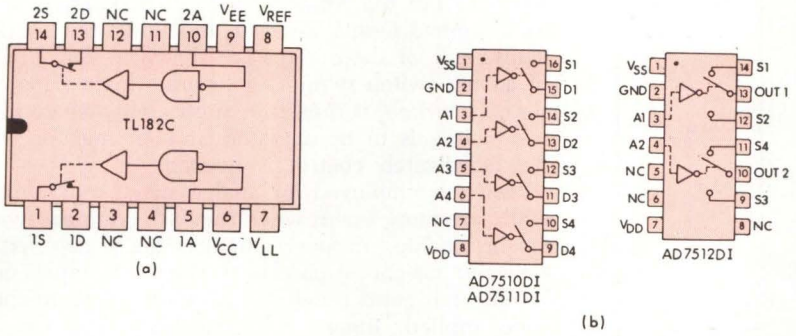
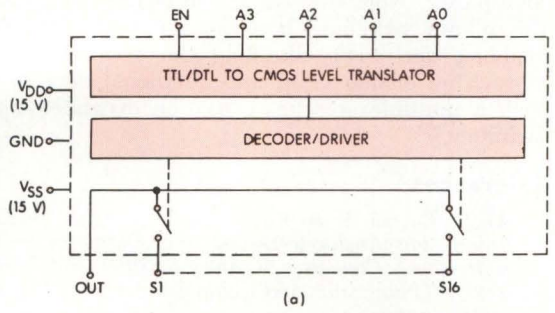
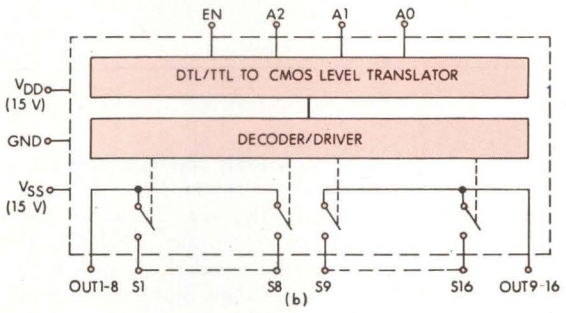


Fig 2 Pin configurations of typical multiplexers that do not have decoding logic. Top view of Texas Instruments TL182C (a) and Analog Devices 7510, 7511, and 7512 (b) are shown (Courtesy of Texas Instruments and Analog Devices, Inc; All rights reserved)





AD7506					
A_3	A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	NONE

AD7507				
A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	NONE

Fig 3 Block diagrams of typical multiplexers with onchip decoders. Functional diagrams and truth tables of Analog Devices 7506 (a) and 7507 (b) devices are shown (Courtesy of Analog Devices, Inc; All rights reserved)

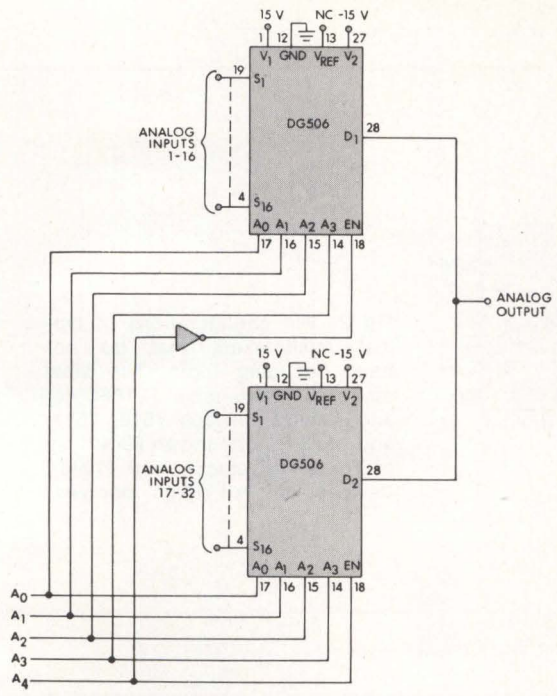


Fig 4 Block diagram illustrates 32-channel analog multiplexer using Siliconix DG506 16-channel multiplexer chips (Courtesy of Siliconix, Inc; All rights reserved)

Semiconductor switches are not ideal devices, and they too have some limitations or constraints that must be considered prior to their use in multiplexer circuits. Almost all such switches require two power supplies, typically 15 and —15 V. Signal inputs cannot exceed these potentials without damaging the device. Most semiconductor switching devices, particularly CMOS and MOSFET, are easily damaged by static electrical discharges such as those produced by synthetic fabrics and rugs. Newer designs incorporate static protection devices within the multiplexer IC device. Early semiconductor switches also were susceptible to a problem called latch-up, which caused them to act as though they were silicon-controlled rectifiers. Once they were turned on to pass a signal, they refused to turn off until the input signal reached 0 V.

A variety of signal sources can provide outputs to be multiplexed. These outputs can include low level thermocouple signals, high level pressure transducer outputs, dc and ac outputs, and high and low frequency outputs. These types of signals may all be multiplexed successfully, although some pre- and post-multiplexer signal conditioning may be required. As an example, low level signals may require amplification before they are input to a multiplexer since transient signals may be large enough to cause significant errors in the low level multiplexer output. If necessary, the resulting amplified and multiplexed signal may be attenuated after being multiplexed. Alternatively, a post-multiplexer filter could be used to remove unwanted noise generated by the switching transients.

Analog switches may be used in almost any circuit that requires a voltage switch. Typical applications are in digital-to-analog converters, programmable gain amplifiers, filters, and integrators. Main interest in these switching devices centers around their use in analog multiplexers, which switch multiple signal inputs to a common point for amplification and digitization. Two types of switching devices to be considered are those with and those without decoders.

Some analog switches, such as the Texas Instruments TL182C and the Analog Devices 7510, 7511, and 7512, have control inputs for each individual switch. Pin configurations for these chips are shown in Fig 2. This type of analog switch requires a separate logic signal to actuate each switch; it is used in applications where more than one switch is to be actuated at one time, or where individual switch control is needed.

Switches employed for analog signal multiplexing generally are more useful when they are equipped with built-in, or onchip, decoder circuits. Such decoder circuits typically accept a parallel binary TTL input and then actuate the correct switch that corresponds to the binary code applied. Binary code can only represent a single binary value at one time, so only one switch at a time is actuated. Block diagrams and truth tables for the Analog Devices 7506 and 7507 analog multiplexers are shown in Fig 3.

When using analog multiplexers with onchip decoders, it is the user's responsibility to provide the correct code of the channel required. Many decoder chips also contain an enable input, which permits multiplexer schemes to be expanded to include a larger number of selectable channels. A typical example is the 32-channel multiplexer circuit shown in Fig 4, which uses a Siliconix DG506 multiplexer. Note the use of the enable input at pin 18; this allows switching between the two multiplexers by enabling one while disabling the other. With the aid of such an enable input and additional decoder circuits, such a multiplexer scheme can be expanded almost indefinitely.[2,3]

References

1. D. G. Larsen, P. R. Rony, and J. A. Titus, *Bugbook VII. Interfacing Analog-to-Digital and Digital-to-Analog Converters and Converter Modules to 8080A/8085 Microcomputers* (Publication forthcoming; adapted with permission of the authors)
2. D. B. Bruck, *Data Conversion Handbook*, Hybrid Systems Corp, Burlington, Mass, 1974
3. *Analog Switches and Their Applications*, Siliconix, Inc, Santa Clara, Calif, 1976

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

NOTE: A 5-day hands-on "Advanced Microcomputer Interfacing and Programming Workshop" for 8080 and 8085 microprocessors is to be held onboard the TSS Carnivale in the Carribean, June 17 to 24. The course will encompass programmable interface chips, data acquisition modules, programming techniques, and future trends, with Dr Peter R. Rony, Dr Paul E. Field, and David G. Larsen as directors. Registration deadline is April 15. Further information may be obtained from Dr Norris Bell, Virginia Polytechnic Institute and State University Continuing Education Center, Blacksburg, VA 24061, tel: (703) 951-6208.

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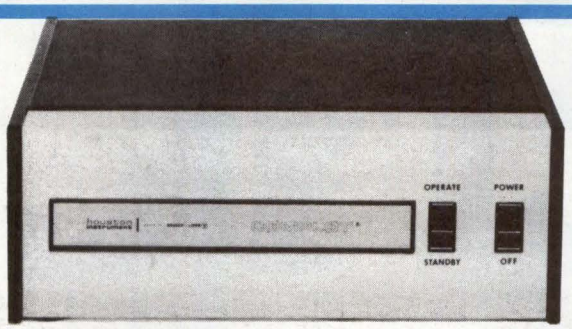

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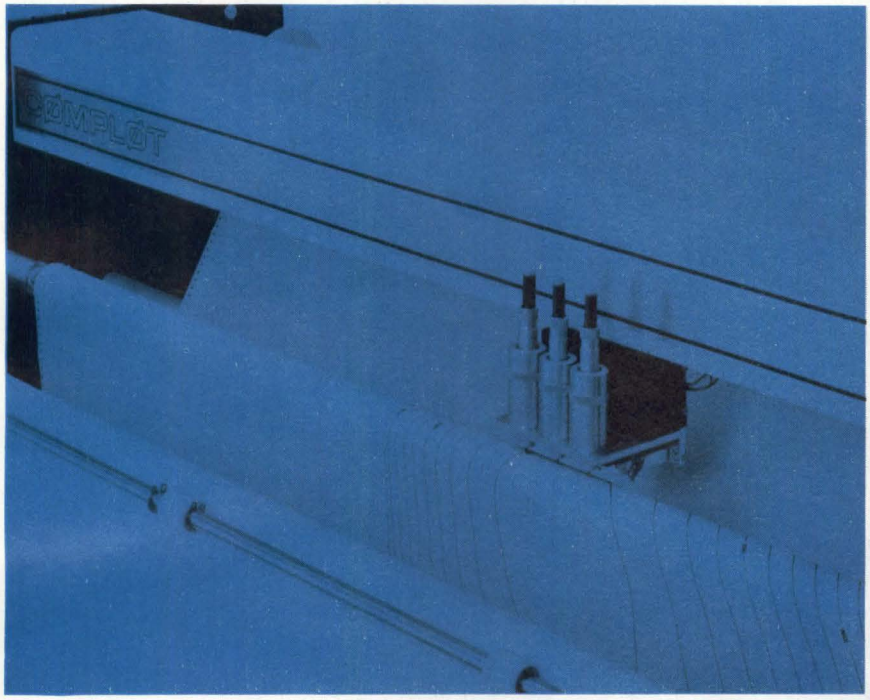

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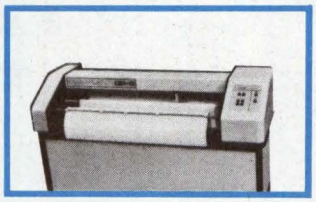

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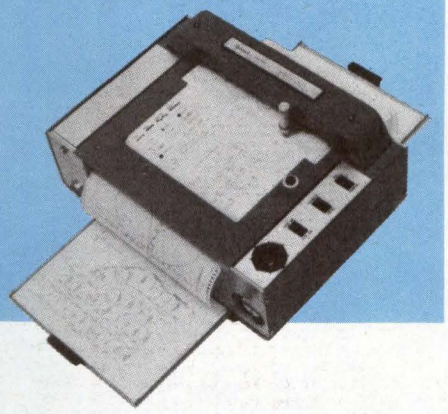

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A general-purpose, single-chip microcomputer aimed at high volume control applications has been designed by Intel Corp, Microcomputer Div, 3065 Bowers Ave, Santa Clara, CA 95051 to reduce both chip and overall system costs. The 8021 chip, at the low end of the MCS-48 microcomputer product line, features a small die and 28-pin package. Priced at $3 each in large OEM quantities, it will be in full production in April.

All functions necessary for digital processing and control are provided. The standalone system contains an 8-bit CPU with a 10-μs instruction cycle time, 64 bytes of R/W data memory, 1024 bytes of program storage in ROM, 21 I/O lines, and other functions which include a programmable interval timer/event counter, and cost-effective onchip system clock and oscillator. The chip executes over 60 instructions, a subset of the 8048 instruction set, with no instruction requiring more than two cycles to execute. The microprocessor is designed to be an efficient controller and arithmetic processor. The chip has bit handling capabilities as well as facilities for binary and BCD arithmetic.

Most of the components are programmable. The RAM consists of eight addressable registers, another 16 locations that serve as program stack or data memory, and 40 remaining bytes used only for data memory. I/O configuration and other functions, such as directions of I/O lines, and number of data memory bytes used as address, stack, and timing intervals between I/O servicing operations, are software programmable.

The I/O lines are organized as two 8-bit ports, one 4-bit port, and a single test/counter input. All lines can individually serve as input or output lines. The counter counts up to a designated programmed count, and then indicates completion to the CPU; it can also be programmed to count an externally occurring event, eliminating software timing loops.

Each of two I/O lines can drive a 7-mA load or the two can be paralleled to drive a single 14-mA load. Options permit certain I/O lines to directly interface to analog circuitry or keyboards while all remaining lines are TTL-compatible.

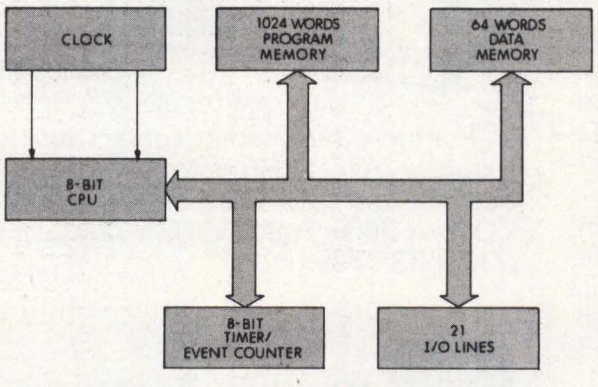
The accurate onchip oscillator can be externally synchronized with a crystal or TTL-level clock signal. It can also produce onchip timing using a single external resistor or inductor.

The chip operates on a single 5-V supply which can vary from 4.5 to 6.5 V. A zero-cross detection feature allows the device to control 60-Hz power and to generate accurate time-of-day and timing control functions.

Programs, which are stored in masked ROM as part of the chip fabrication process, are developed, however, with EPROM. This expedites development and avoids repetitious masking changes and turnaround delays.

Design development and prototyping are facilitated by the MCS-48 family support and the EMB-21™ Emulator Board along with the ICE-48™ In-Circuit Emulator to debug hardware and software before a program is committed to masked ROM. The portable emulator board contains an 8748, which is a 1k-byte EPROM version of the 8048, as well as discrete logic to emulate the 8021's I/O features.

Circle 170 on Inquiry Card



Single component 8-bit microcomputer is fabricated of n-MOS process. Features of Intel's 8021 include subset of the 8048 for low cost, high volume applications, plus additional I/O flexibility and power. Contained on chip are 1k x 8 program memory, 64 x 8 data memory, 21 I/O lines, and 8-bit timer/event counter, in addition to on-board oscillator and clock circuits

Computer-On-A-Chip uProcessor Helps To Cut Application Costs

Designed to be used by manufacturers in various applications to achieve low product prices, the 4-bit S2000 microcomputer reduces parts count and cost by combining 8192 bits (1k 8-bit words) of ROM, 256 bits (64 4-bit words) of RAM, I/O, and a clock oscillator on one chip. The TTL compatible device includes 13 outputs, eight inputs, and eight bidirectional 3-state I/O lines onchip. Input sensing lines have TouchControl™ compatibility, enabling interfacing to capacitive switch devices.

The 40-pin plastic or ceramic packages also include a 7-segment display decoder and LED drivers. A second version is available that will direct drive vacuum fluorescent displays.

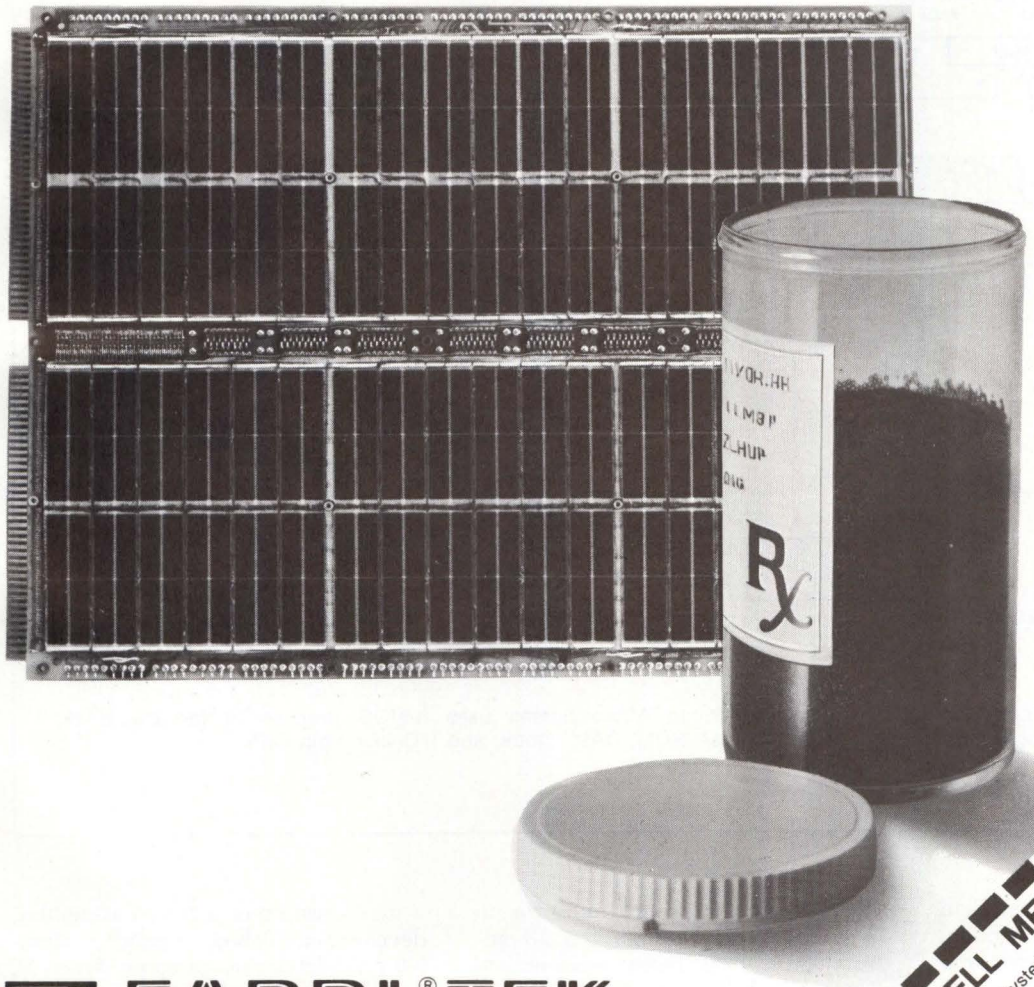
(Continued on p 140)

Suffering from temporary loss of memory?

Try the Fabri-Tek core remedy.

If you're like some people who've been on a straight semiconductor memory diet, you've probably been experiencing severe complications. Loss of memory when power is removed. "Soft" random errors that can't be diagnosed. Temperature sensitivity. Added cost and complexity of error detection and correction schemes and battery back up.

For no added cost, core memories provide greater reliability, maintainability, non-volatility and 20 years of proven technology. They're relied upon in process control and a lot of other demanding applications where a failure could be catastrophic. Take our Model 698: 64K bytes of 650 nsec cycle time and 250 nsec access time. You can build a system up to 512K bytes. (Micro 3000 compatible, too). Maybe its time you kicked the semiconductor habit. We're ready to help.



TELL ME MORE

☐ Model 698-32K X18 System ☐ Model 696-16K X18 System ☐ Future requirement
☐ Bulk Core Systems ☐ 30-90 day requirement ☐ Send literature
☐ Special memory needs ☐ Have salesman call

Name and Title

Company

Address

City, State, Zip

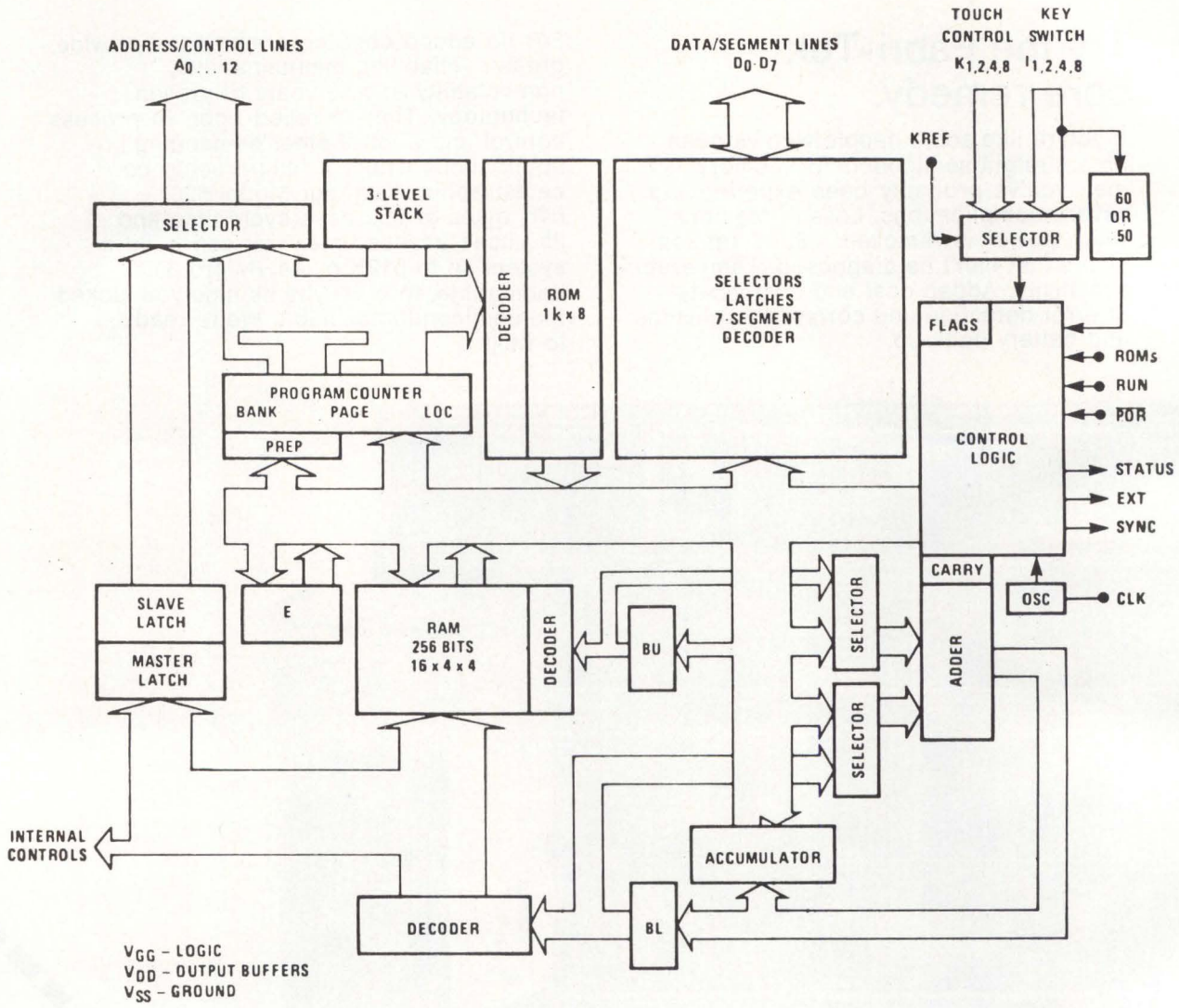
Phone

FABRI-TEK INC.
COMPUTER SYSTEMS

5901 South County Road 18 • Minneapolis, MN 55436 • (612) 935-8811

Boston, MA (617) 969-5077	Hawthorne, CA (213) 973-0484	Dallas, TX (214) 234-8438	Newark, NJ (201) 774-5654
Chicago, IL (312) 437-4116	San Jose, CA (406) 246-8391	Houston, TX (713) 467-4373	United Kingdom Maidenhead 37321-4

CIRCLE 72 ON INQUIRY CARD



To achieve speed and circuit density advantages, American Microsystems uses n-MOS process in fabricating its S2000 microcomputer. Single-chip architecture combines ROM, RAM, clock, and I/O in 40-pin DIPs

The microcomputer also has an arithmetic logic unit, control section, and three registers for addresses and intermediate values. Execution cycle time is 4 μs. Unit operates with a 9-Vdc power supply or dual supplies of 5 and 9 Vdc. Typical power dissipation is 360 mW.

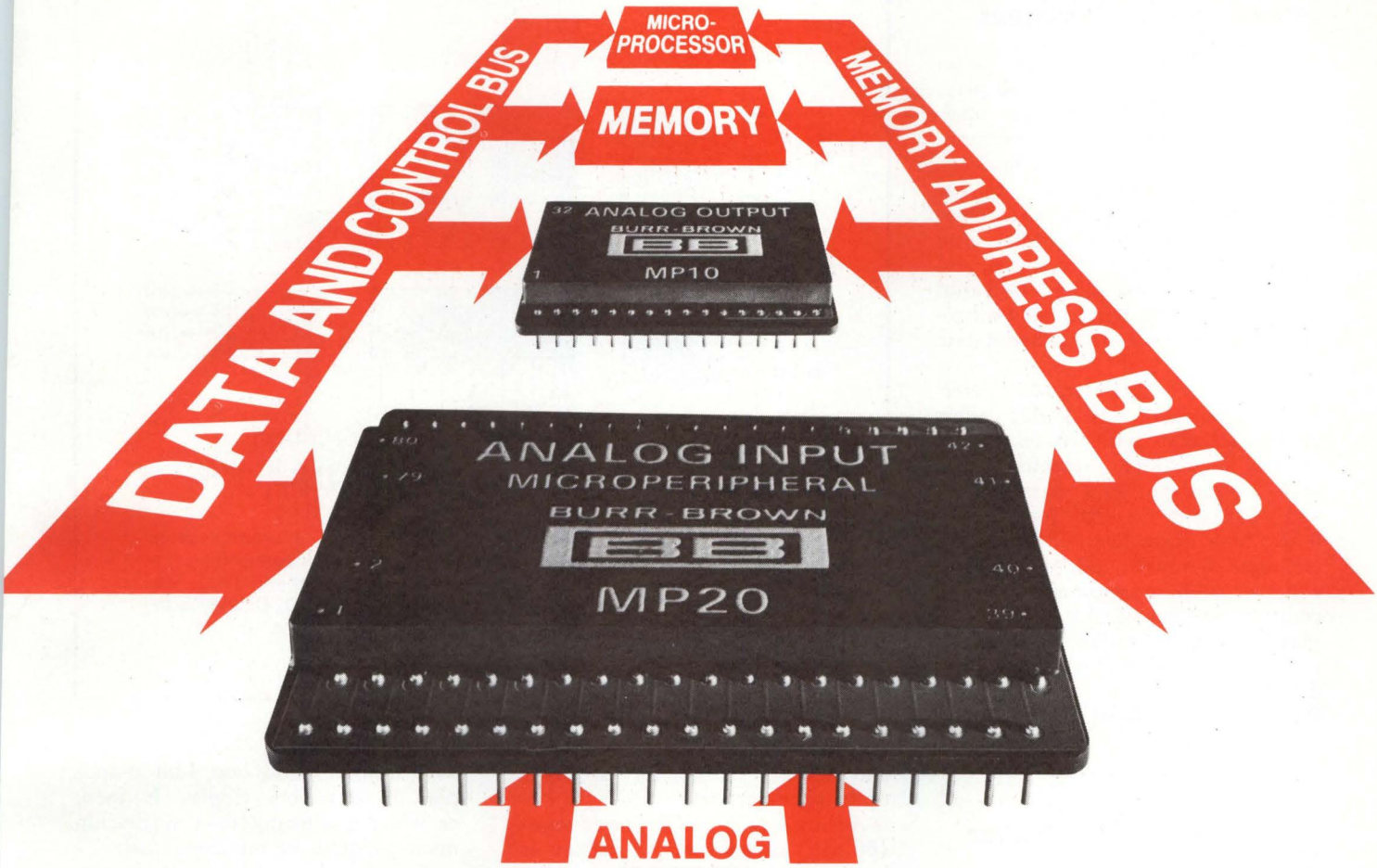
To simplify debugging and device testing, the microprocessor provides access to internal registers and memory. Externally, the computer addresses up to 7168 more words of ROM (which stores programs up to 1k words long) through the 13 address lines; RAM holds intermediate values during processing.

Firmware consists of 51 instruction codes. This instruction set shortens program development time, condenses programs more easily for internal ROM, and simplifies learning to program the device.

American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 provides program development software consisting of a macro assembler, development/debug module, simulator to determine program function, and text editor. User programs can be loaded into p/ROMs from the Microprocessor Development Center's (MDC) RAM for prototype hardware tests; the MDC also loads programs onto diskette for incorporation with S2000 microprocessors fabricated for a user.

Circle 171 on Inquiry Card

Analog input...analog output. Now they're both just this simple.

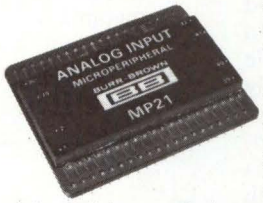


Meet the 16-channel MP20 and MP21 Analog Input Systems. They join our previously introduced MP10 and MP11 Analog Output Systems to give you a complete analog interface solution for your microprocessor based designs.

Now, instead of designing a complete data acquisition system, you simply plug in one of these units as if it were memory. That means big savings in design costs, and faster product introduction too.

For 8080A and SC/MP and Z80 type microprocessors, you need our new MP20. And for 6800, 650X and F-8 types, our MP21. Both of these bus-compatible Analog Input Microperipherals are self contained, requiring no external components.

Since these systems are treated as memory by your CPU, software implementation is simple too. Just assign one 8-bit memory location per channel, and use any memory reference instruction to access data. For example, one LDA instruction will acquire a channel of information when used with the 8080A. Alternatively, the units can be interfaced as an I/O port or on an interrupt basis.



Both the MP20 and MP21 have resistor programmable input ranges of ±10mV to ±5V full scale allowing you to handle low-level signals directly. They provide 8-bit resolution and throughput accuracy better than ±0.4% of full scale on the ±5V range.

With a price of just $140 (100's), it just doesn't make sense to design your own analog input solution. For complete details, write or call Burr-Brown, International Airport Industrial Park, Tucson, Arizona 85734. Phone (602) 294-1431.

CIRCLE 73 ON INQUIRY CARD

BURR-BROWN

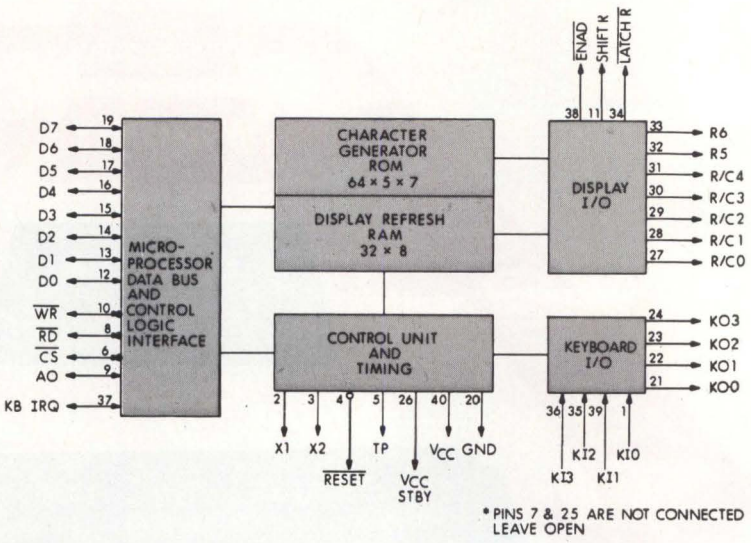
Leaders in microcomputer I/O.

Alphanumeric Displays Satisfy Requirements of µComputer Environment

Three models of the DE/200 series of intelligent, random-access displays are alphanumeric, single line modules featuring low power consumption, vacuum fluorescent technology. The output device contains an onboard microprocessor with a character generator, display buffer, and refresh circuitry. Interface, drive, and refresh electronics offer universal compatibility with bus-oriented microprocessor systems and with serial data devices.

Digital Electronics Corp, 415 Peterson St, Oakland, CA 94601 offers models DE/210 with 10 char positions of 8-mm high characters; /220 with 20 char positions, 9 mm high; and /232 with 32 char positions of 6-mm high characters. Character set includes numbers and upper case alphabet with or without period or comma; 14-segment character design permits clear readable messages, even under high ambient light conditions.

Circle 172 on Inquiry Card



Monolithic n-MOS single-chip interface for 8-bit microprocessors interfaces to CPU via microprocessor data bus. Incorporating intelligent commands for display and keyboard manipulation, Matrox's controller works with any 5 x 7 dot matrix LED. Display contains up to 32 char; keyboard can have up to 64 keys

Alphanumeric Controller Display/Keyboard Functions Are On One Chip

Users of most 8-bit microprocessors now have available a single-chip, general-purpose programmable alphanumeric display and keyboard interface device enabling them to replace a 7-segment display at little or no extra cost. It interfaces directly to address, data, and control buses on the input side. The display controller portion of the MTX-Al (alpha chip) provides all timing and refresh signals to drive up to 32 5 x 7 dot matrix LED displays; keyboard portion provides all scanning signals to debounce and decode any keyboard of up to 64 keys, with a debounce time of 16 ms. Single-pole and ASCII keyboards can be used.

Matrox Electronic Systems, PO Box 56, Ahuntsic Stn, Montreal, Quebec H3L 3N5, Canada has incorporated virtually all functions on one chip. It has a 32 x 8 display refresh RAM built in, as well as a 64 x 5 x 7 ASCII character generator ROM. The chip internally generates all timing and refresh signals for display of up to 32 characters.

A single 5-V ±10% power supply (60 mA) is required. All display and keyboard I/O pins are TTL compatible. Display and keyboard parameters are fully programmable.

The device interfaces directly to any TTL, CMOS, or n-MOS microprocessor through an I/O port or bus. Memory mapped I/O is the simplest; interfacing can also be through one 8-bit I/O bidirectional port (for data transfer) and one 4-bit output port if a remote display is used, or when interfacing to a single-chip microcomputer or minicomputer.

Available in a 40-pin plastic DIP, the chip has a temperature range of 0 to 70°C. Production quantities of the $39 (single unit) device will be available in the first quarter of 1978. Versions for 14-segment displays and units with different character fonts are also planned.

Circle 173 on Inquiry Card

Three Static Memory Modules Are Announced for 12-Bit µComputer

Three static memory modules have been introduced by Pacific Cyber/Metrix, Inc, 3120 Crow Canyon Rd, San Ramon, CA 94583 for use with its PCM-12 microcomputer system (see *Computer Design*, May 1976, p 210). Basic system module, the 12020A, is a 4k-word by 12-bit memory constituting one full field of memory for the computer, which can hold up to eight boards. Each board carries 59 ICs and all necessary bus interfacing logic.

A combination of EPROM and RAM devices, the 12160 holds 1.5k 12-bit words of UV-erasable ROM in the highest pages of its field, and 512 12-bit words of n-channel RAM in its lowest pages. Two boards fill any 4k field of memory with 3k words of EPROM and 1k words of RAM when used with the 12040A memory extender module.

The third module is a nonvolatile memory organized as 4096 12-bit words, with 48 1k CMOS RAMs with

You tell us what your data collection requirements are. We've added more data collection building blocks to satisfy them.

EPIC DATA's Model 1647 data collection terminals and Model 1648 system control units (SCUs), let you configure exactly the data collection system you need. These "building blocks," based on microprocessor architecture and modularity, provide you with simple, practical and flexible terminals or systems for virtually any combination of requirements you may have.

simple. Building blocks can be combined to enable collection of information from a wide variety of pre-prepared and variable data with resulting improved efficiency and reduced errors. No computer knowledge is required for operation. Terminals can be programmed to: provide customized input, output and processing of data; prompt the user through entry steps and validating of data; and enable off-line or on-line operation.

EPIC DATA terminals are rugged, compact and lightweight. They can be wall-mounted or placed on a desk and are easily exchanged during maintenance.

practical. Environmental tests conducted in conformity with MIL-STD-810 plus in-depth, on-site testing assure reliable operation over a broad spectrum of hostile, industrial environments. Simple design and rigorous testing have resulted in an impressive MTBF.

flexible. EPIC DATA terminals can optically read punched badges and 80-column ANSI cards. User-defined keys are available for inputting variable data. Key entry data or time of day is displayed and LEDs are available for prompting.

Terminals can be configured to scan bar codes and magnetic stripes or accommodate other peripherals through RS232 ports. Display options include additional numeric displays, up to 15 LEDs for prompting and a 32-character alpha/numeric display. Serial asynchronous or synchronous communications ports with either RS232 or line driver I/O and a low speed modem may be added. Parallel communications ports are also available. Both PROM and RAM memories are expandable.

Newest Building Block: More to Come in Next Few Months

A self-contained cassette tape recorder providing up to 2.88 megabits of storage for transaction logging or store-and-forward applications is now available. The modular reel-drive tape recorder, like the rest of the building blocks, features high reliability and ease of maintenance. There is no pinch-roller or capstan to wear tape; only the head touches the tape.

SCUs. Model 1648 SCUs can be configured to poll up to 100 terminals, assemble transactions, format data, append time and date, and store or forward collected data to the host.

Tell us what your data collection requirements are. We'll supply the parts. Contact your EPIC DATA representative today or write:

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Representatives: ARIZONA BFA Corporation (602) 994-5400 • CALIFORNIA Moxon Electronics (714) 635-7600 • FLORIDA COL-INS-CO (305) 423-7615 • ILLINOIS Systems Marketing Corp. (312) 593-6220 • KANSAS/MISSOURI Digital Systems Sales (816) 765-3337 • MARYLAND Electronic Marketing Associates (301) 881-5300 • MASSACHUSETTS J & J Associates (617) 272-2606 • MICHIGAN/OHIO WKM Associates, Inc. (313) 588-2300, (216) 267-0445 • NEW YORK Cane Technical Sales (914) 698-4411 • NEW YORK Ossmann Instruments (315) 437-6666 • PENNSYLVANIA WKM Associates (412) 892-2953 • TEXAS DMA (713) 780-2511 • WASHINGTON DPM Associates (206) 453-9082 • MEXICO Electronica Hemisferica, S.A. Mexico City (905) 2-50-60-11 • UNITED KINGDOM Sintrom Ellinor Ltd. Reading (0734) 85464

automatic recharge battery backup. Containing all TTL for interfacing with the microcomputer's system bus, the 12210 retains its memory contents for up to 30 days with system power turned off. When used with the 12230 power-fail module, the system becomes transparent to ac line power failures in general.
Circle 174 on Inquiry Card

Microcomputer System Provides Quick, Basic µProcessor Experience

Aimed primarily at engineers, students, and hobbyists wishing to understand and use microprocessors, the COSMAC Microtutor II (CDP18-S012) is a basic microcomputer system for easy hands-on operating and programming experience. Preassembled and containing its own regulated power supply, it is based on the company's CDP1802 CMOS 8-bit microprocessor, and supercedes the original Microtutor (CDP18S011).

RCA Solid State Div, Box 3200, Somerville, NJ 08876 has equipped the microcomputer with eight binary toggle switches for input and two 7-segment LED hexadecimal digit displays plus a Q LED for output. Additional toggles provide controls to examine and alter memory locations and to initiate program execution.

Components include a crystal clock for stabilized timing applications and a memory protect switch that inhibits the memory write operation. Programs are loaded via the onchip DMA facility, eliminating the bootstrap routine.
Circle 175 on Inquiry Card

Low Cost Microcomputer Uses Double-Density Floppy Discs

Engineered with only two boards—the computer and controller, the Micro-2 microcomputer system is housed in a single cabinet with two Shugart dual-drive, double-density floppy discs. The computer board features a Z80 CPU, 32k or 64k RAM, four RS-232 serial interfaces, and real-time clock.

The controller handles data transfers for sector R/W through a DMA interface, permitting concurrent processor execution. Either IBM 3740 format or double-density format of 571k bytes/diskette can be used by the disc controller. With optional double-sided drives, the system can store up to 2.3M bytes.

Assembled and tested, the high performance system with 32k of memory and two single-sided drives is selling for $4995; the system is complete with comprehensive CP/M disc operating system and hardware diagnostics. Digital Systems, 6017 Margarido Dr, Oakland, CA 94618 supplies extensive accounting software, together with CBASIC, BASIC-E, and FORTRAN.
Circle 176 on Inquiry Card

Board Enables µComputer to Support Four Simultaneous Users

Any Southwest Technical Products 6800 microcomputer (or similar SS-50 bus system) can be turned into a full computer timesharing system with the addition of the multi-user system from Technical Systems Consultants, Inc, PO Box 2574, West Lafayette, IN 47906. The board plugs into a memory slot on the bus, without modifications, to support up to four independent users. For most uses, speed reduction is negligible.

Kit includes plated through-hole PC board, IC sockets, components, diagnostic programs, and user's manual. Multi-user Micro BASIC Plus is contained on a cassette tape; the interpreter resides in less than 4k of RAM. Options include cassette interfaces, floppy disc drives, printer, and two versions of 8k Multi-user BASIC. Besides the microcomputer and system board, system requirements also necessitate a serial interface board for each user, at least 12k of memory, and one terminal for each user.
Circle 177 on Inquiry Card

LSI-11 Compatible Add-In Memory Fits 32k On Single Width Board

A high density add-in memory expansion card requiring only a single peripheral option slot for 32k words of storage using 16k dynamic RAMs, the CDM-77/03 memory for DEC LSI-11 and PDP-11/03 computers is completely hardware and software compatible with the LSI-11. Memory is addressable as a contiguous block in 2k word increments, with address selection accomplished via an onboard DIP switch.

Cyberchron Corp, 5768 Mosholu Ave, Riverdale, NY 10471 has designed the card to function with either burst (CPU) or distributed (DMA) refresh under the control of the processor microcode or REV-11 refresh option. Specs include an access time of 350 ns and cycle time of 525 ns. Calculated MTBF exceeds 100k hours.
Circle 178 on Inquiry Card

Multibus™ Compatible Computer Is Built Around Z80 Microprocessor

An Intel SBC-80 Multibus™ compatible single-board computer featuring 8k static RAM and 8k EPROM sockets is designed around the Zilog Z80 processor with up to 4-MHz clock speed. The MSC 8001 is electrically and mechanically compatible with SBC-80 systems, and operates as a master module in the Multibus scheme.

Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80110 uses the Z80 to provide 158 instructions. A dual set of registers improves multiprocessing capability. Two parallel I/O ports consist of parallel peripheral interface circuits with buffers and terminators to protect internal MOS circuitry; the serial I/O port supports RS-232-C, TTL, or current-loop compatible serial I/O devices with programmable baud rate. Asynchronous and synchronous data formats can be programmed.

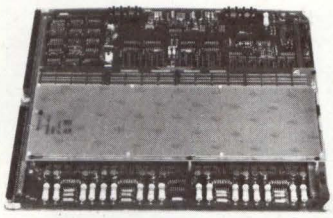
The computer, priced at $845, provides real-time processing with the 8253 interval timer, and eight levels of fully vectored priority interrupts. There are also simpler interrupt modes for SBC 80/10 compatibility.
Circle 179 on Inquiry Card

Prototyping Package Speeds Design of Custom Interface Systems

A prototyping package, designed to complement the BLC 80/10 Board Level Computer and Series/80 family of boards, allows designers to quickly construct and debug custom interface systems. The BLC 80P consists of a BLC 80/10 computer board with 1k words of RAM and 2k words of blank

Contact us for memory that puts your mind at ease

Nerves shot trying to pinpoint "soft" random errors in your semiconductor memory? Feeling tense since your add-on memory still hasn't arrived? Or maybe you're just a little anxious because you'd like to upgrade your system, but aren't sure it's in your budget?



The PINCOMM I System is a high quality 3 wire-3D core memory add-on or replacement for the INTERDATA processors.

Relax! Standard Memories has a line of core memory that will put your mind at ease. None of the usual worries that go along with semiconductor memory, like power failure and complex error detection. And among current core memory manufacturers, Standard Memories stands out as a recognized leader you can depend on. Greater reliability. Lower cost. Fast delivery.

PINCOMM® A gives you the best, low cost core memory for General Automation SPC-16, SPC 18/30 and the GA 16/440. PINCOMM I is the perfect add-on or replacement memory system for INTERDATA Models 50, 55, 70, 74, 7/16, 7/32 & 8/32. PINCOMM N is the ideal Form, Fit and Function replacement for the NOVA 2, 3 & 1200 Series. BUSCOMM® R-11 provides a totally compatible memory to upgrade your DEC PDP-11. And ECOM® 70 is the answer to greater flexibility for the DEC PDP-11/70.

Let us know what's on your mind about add-on or replacement memory. Send the coupon below or call one of our toll free numbers.

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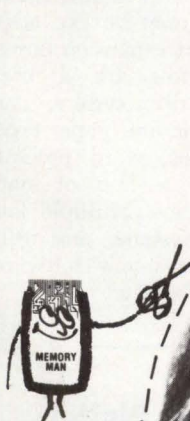
CIRCLE 75 ON INQUIRY CARD



For an instant quotation call The Memory Man toll free: (800) 854-3792, (in California) (800) 432-7271.

I'm thinking about adding memory to the following computer(s):

☐ GENERAL AUTOMATION Model _____ ☐ DATA GENERAL Model _____

☐ INTERDATA Model _____ ☐ DEC Model _____

Name/Title _____

Company _____

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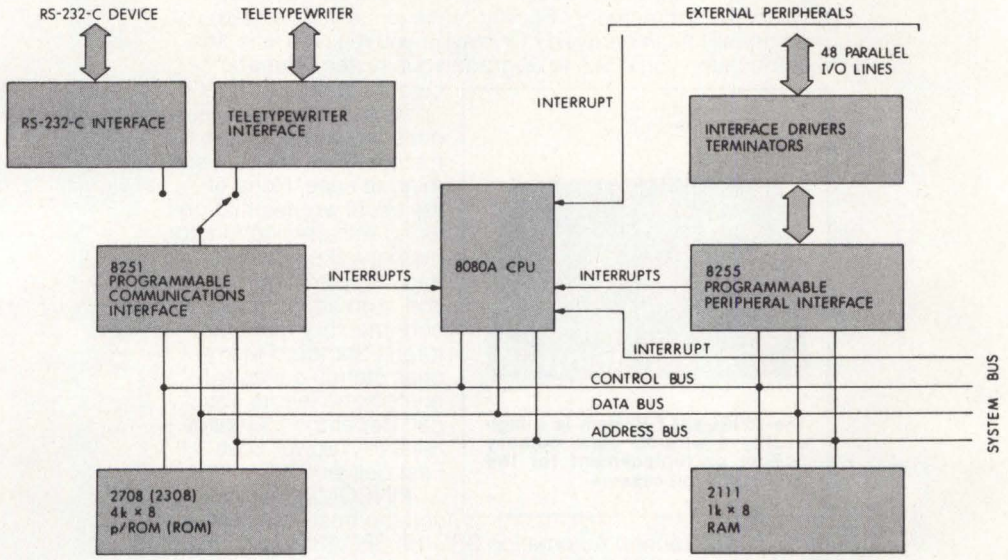
City/State/Zip _____



National Semiconductor's BLC 80P prototyping package is complete system for OEM development and applications. 80/10 PC board holds programmable parallel and serial I/O lines, 1k bytes of RAM and sockets for up to 4k bytes of p/ROM, and CPU circuitry; serial I/O can be used in RS-232-C or teletypewriter current-loop modes

programmable ROM. An additional 2k words of p/ROM contain the system monitor, which offers facilities to load, execute, and debug 80/10 related programs.

The 48 socketed, programmable parallel I/O lines accommodate interchangeable line drivers and terminators. Included in the package are 10 DM 7437 open-collector line drivers, 10 BLC 902 1-kΩ terminating resistor networks, and 10 BLC 901 220/330-Ω terminating resistor networks.

Space for 114 16-pin sockets or the equivalent mix of 14-, 16-, 18-, 22-, 24-, 28-, and 40-pin sockets is available on the universal prototype board to aid in developing custom interface circuits. The 6.25 x 12" (15.88 x 30-cm) CPU and prototype boards are housed in the BLC 604 card cage that can handle two other Series/80 boards. The CPU is complemented with such circuitry as a multisource, single level interrupt network, and bus drivers for memory and I/O expansion.

The cage also serves as a backplane, providing power busing and access to system bus signals. Two power cables and two 50-conductor ribbon cables for interconnection to external circuits are supplied by the Microcomputer Systems Group of National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Jumper selected options give RS-232-C or current-loop mode; cables are supplied for a CRT terminal and for a teletypewriter. With hardware and software documentation, the package sells for $878.

Multi-Configuration Microcomputer System Is Expandable

Model RD-11A, a DEC LSI-11 based computer, is configured on a nine quad-slot backplane, which allows adequate expansion capability. Housing is a DEC H909-C enclosure modified to accept the system power supply, control logic, and frontpanel switches and indicators; it may be either rackmounted or used as a desktop unit.

RDA, Inc, 5012 Herzel Pl, Beltsville, MD 20705 allows a wide variety of memory, peripheral, and software choices. Memories include dynamic and static RAM, core RAM, EPROM, and p/ROM. The system offers 62k bytes of addressable memory; core memory may be expanded to 56k bytes without expansion boxes.

Various peripherals are a DMA interfaced floppy disc system, cartridge disc, magnetic and paper tape, card reader/punches, word processing printers, and a line of data acquisition subsystems. Multiple languages, operating systems, and utilities comprise the system's software.

Circle 180 on Inquiry Card

Microcomputer Digital Input System Serves Industrial Control Market

Twenty-four digital input channels that electrically and mechanically

$44.95 KNOW-IT-ALL

CSC's multi-family Logic Probe 1 with memory. Already the industry standard for performance and value.

This compact, enormously versatile test and trouble-shooting aid is like a pencil-sized scope at your fingertips. Simply connect its clip leads to the circuit's power supply, set a switch to the proper logic family, and touch the probe tip to the node under test.

LP-1's unique circuitry does the work of a level detector, pulse detector, pulse stretcher and memory. HI LED indicates logic "1," LO LED, logic "0," and all pulse transitions—positive *and* negative, as narrow as 50 nanoseconds—are stretched to 1/3 second and displayed on the PULSE LED. One-shot, low-rep-rate narrow pulses—nearly impossible to see even with a fast scope, are easily detectable and visible. And you can indefinitely store single-shot as well as low-rep-rate events.

At frequencies above 1 MHz, there is an additional indication with unsymmetrical pulses: duty cycles of less than 30%, light the LO LED; over 70%, the HI LED. In all modes and circuit states, LP-1's high input impedance virtually eliminates loading problems. The unit also features over-voltage and reverse-polarity protection, interchangeable probe tips, power cables and other optional accessories.

See your CSC dealer today. Or call (203) 624-3103 (East Coast) or (415) 421-8872 (West Coast) for the name of your local stocking distributor and a full-line catalog.

Specifications

Input impedance: 100,000Ω

Thresholds (switch selectable)	**DTL/TTL**	**HTL/CMOS**
logic "1" thresholds (HI-LED)	2.25V ± .15V	70% Vcc ± 10%
logic "0" thresholds (LO-LED)	0.80V ± .10V	30% Vcc ± 10%

Min. detectable pulse width 50nsec. guaranteed

Pulse detector (PULSE LED) in PULSE position of PULSE/MEMORY switch, ⅓-sec. pulse stretcher makes high-speed pulse train or single events (+ or − transitions) visible; in MEMORY position, first transition lights and latches LED

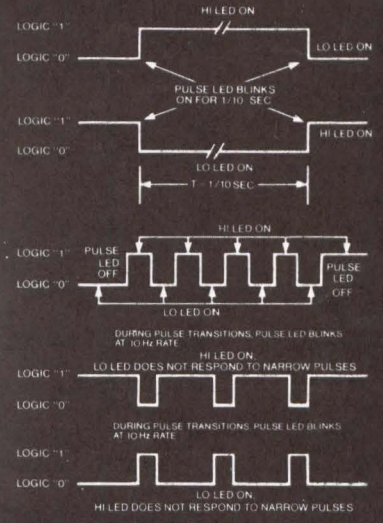
Operating temperature 0-50°C

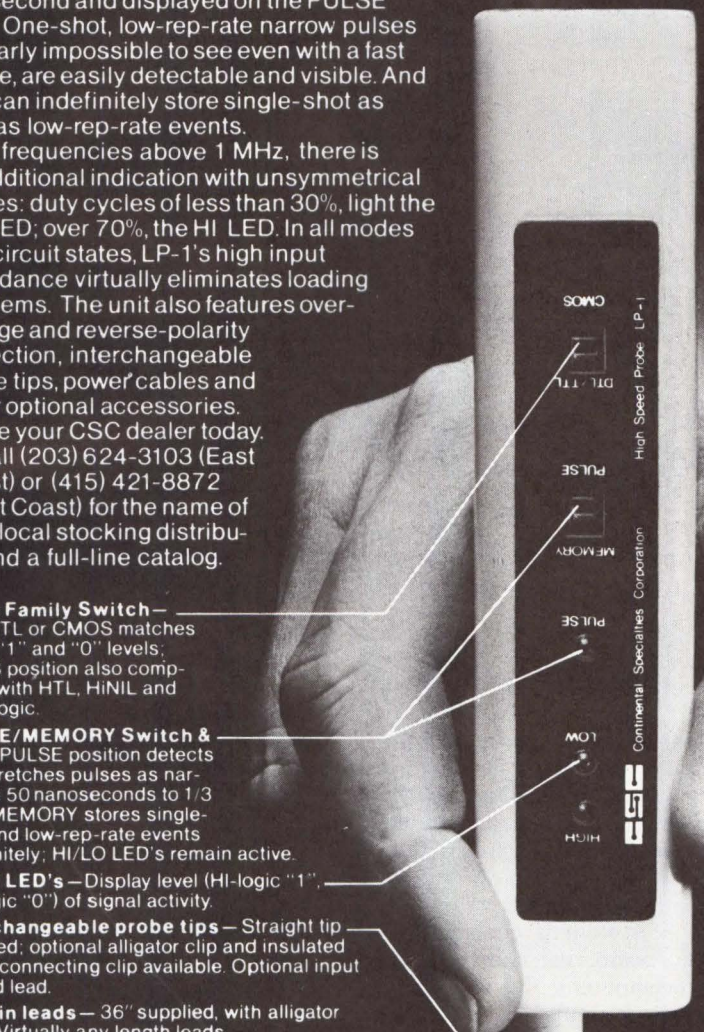
Physical size (l x w x d)
5.8 x 1.0 x 0.7" (147 x 25.4 x 17.8mm)

Weight 3oz. (.085Kg)

Power leads removable 36" (914mm) with color-coded insulated clips; others available

Input protection overload, + 500V continuous; 117 VAC for less than 15 sec.; reverse polarity, 50V; power leads reverse-voltage protected.





Logic Family Switch—TTL/DTL or CMOS matches Logic "1" and "0" levels; CMOS position also compatible with HTL, HiNIL and MOS logic.

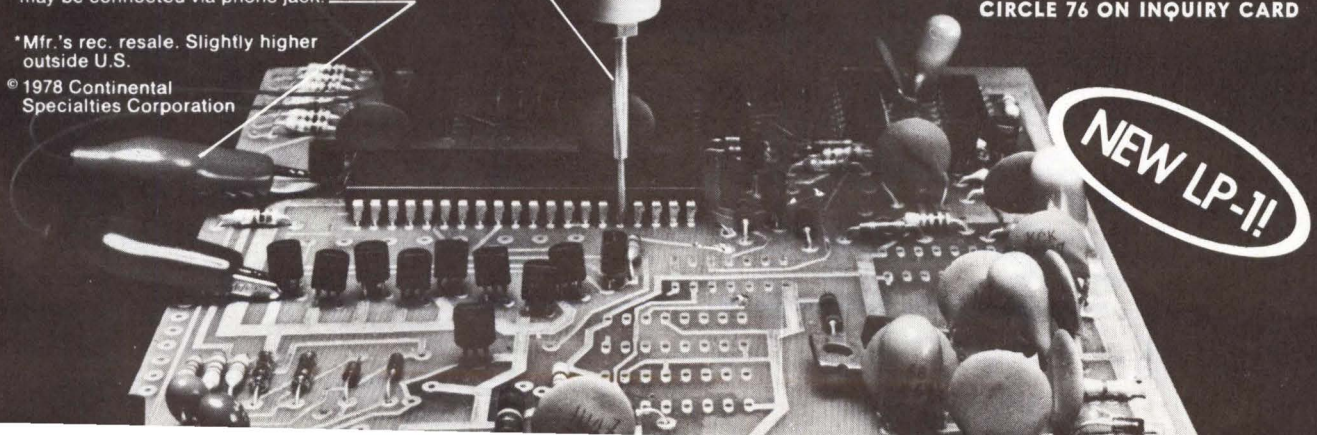
PULSE/MEMORY Switch & LED—PULSE position detects and stretches pulses as narrow as 50 nanoseconds to 1/3 sec.; MEMORY stores single-shot and low-rep-rate events indefinitely; HI/LO LED's remain active.

HI/LO LED's—Display level (HI-logic "1", LO-logic "0") of signal activity.

Interchangeable probe tips—Straight tip supplied; optional alligator clip and insulated quick-connecting clip available. Optional input ground lead.

Plug-in leads—36" supplied, with alligator clips. Virtually any length leads may be connected via phono jack.

*Mfr.'s rec. resale. Slightly higher outside U.S.



NEW LP-1!

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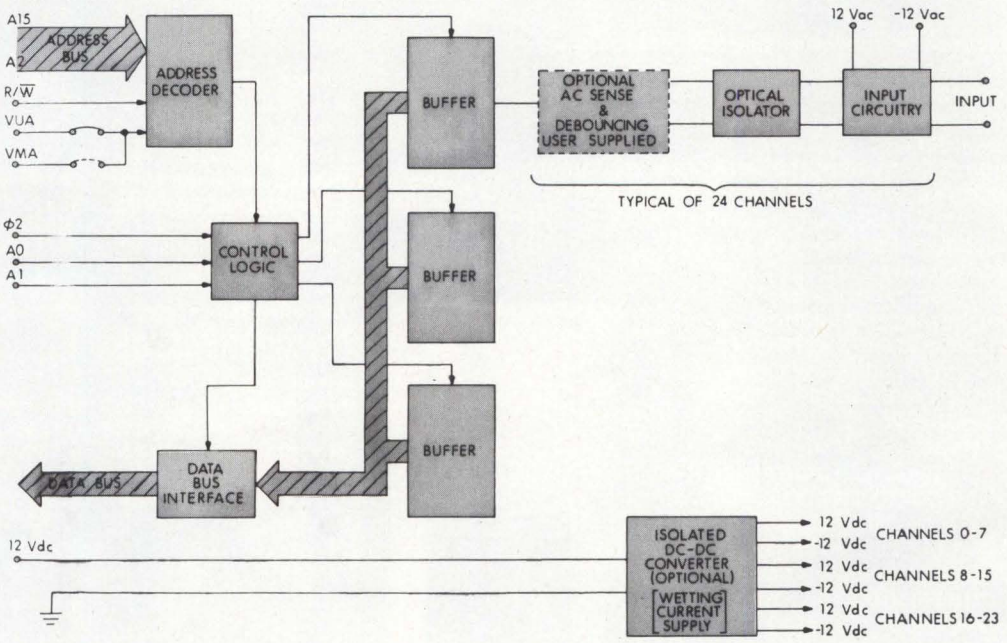
CIRCLE 76 ON INQUIRY CARD



Layout illustrates single-board 24-channel digital input system (MP710). Providing isolation from computer bus and channel-to-channel, Burr-Brown's system is plug-compatible with the Micromodule and EXORciser, and operates from computer's 5-Vdc power supply. Two versions enable operation with both dry and wet relay contacts

interface with Motorola Micromodule[R] and EXORciser[R] microcomputers are provided on the MP710 microperipheral board. Burr-Brown, Tucson, AZ 85734 has designed the system with such features as isolation from the computer bus and channel-to-channel, and contact closures or voltage input. The board is intended to reduce system development time, while accommodating differences in ground levels between inputs, operating with contact closures—wet or dry, and operating in applications (such as industrial control) where isolation protects the microcomputer from voltage transients, lightning, and malfunctions.

Each input can read a contact closure. Either version—MP710 for dry relay contacts, and MP710-NS which operates with voltage inputs (wet relay contacts)—may be modified by jumper selection to operate with voltage or contact closure inputs, or a mixture of both.

Inputs are arranged in groups of eight, with each group isolated from other groups and from the computer bus up to 600 Vdc. Isolation between inputs is 300 Vdc (for the MP710-NS model).

Since each input is isolated, voltage switched by each line is not critical, and ground loops are avoided. Varistors protect each relay contact by suppressing high voltage transients, as for example those encountered in inductive circuits.

The input system is contained on a single PC board that operates from the microcomputer's 5-Vdc power supply. Digital inputs enter through a card edge connector located opposite the bus connector. The user may add an ac sense and debouncing circuit to each channel.

The boards are programmed as memory locations; each input is one memory bit and any read command may be used. Logic 0 represents an open contact (low voltage), and logic 1, a closed contact (high voltage) when the board is read. Each read command inputs the status of eight channels. Address bits A0 and A1 select the set of outputs to be read. The remainder of the address lines are used to select the board itself. The address block that each board occupies is selectable, and is locatable anywhere in memory.

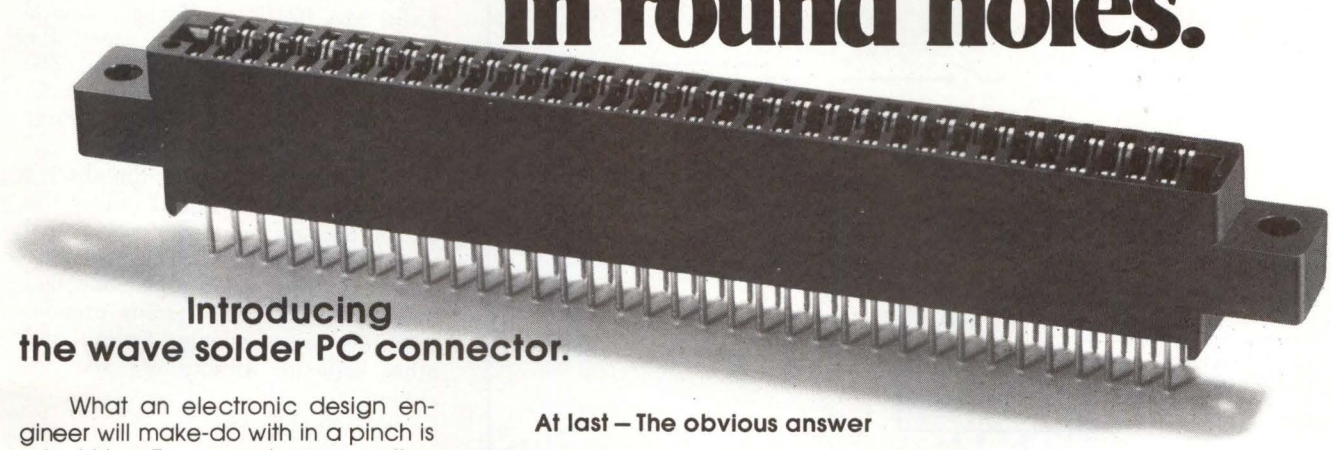
Circle 181 on Inquiry Card

CMOS RAM Module Simulates ROM for Prototyping Purposes

A 1k x 12 CMOS RAM module has been added by Cybertek, Inc, 222 150th Ave, Madeira Beach, FL 33708 to fill the role of a general-purpose RAM board in the LP-12 CMOS family, as well as to simulate the 6312 ROM for prototyping. The LP-12D module can accomplish this, since it can be strapped for address block recognition and RAM select signal generation.

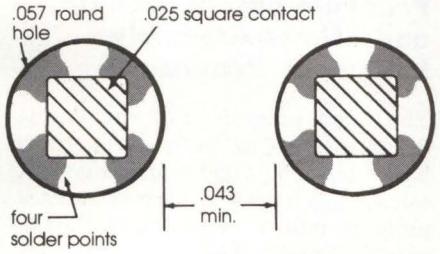
Features of the board, which connects directly to the LP-12 microcom-

No more square tails in round holes.



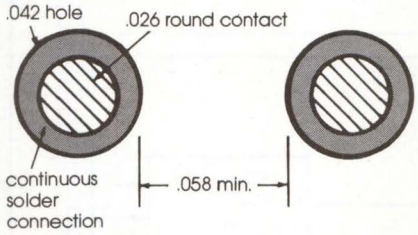
Introducing the wave solder PC connector.

What an electronic design engineer will make-do with in a pinch is astonishing. For example – converting wire wrap* PC connectors to wave solder.



How it's done: you saw off the square .025" tail and push it through a .057" round hole in the PC board. You get only 4 contact points for solder. And there's room for only one tracing between holes. But, so what...it works.

At last – The obvious answer



Our own design engineers, not afraid of doing the obvious and simple thing, have done just that. They've taken a series of our PC wire wrap connectors – and given them .026" round tails. Everything else stays the same: the insulator, semi-bellows contacts, pin and row spacing.

So what?

So – the .026" round pin slips into a .042" round hole in your PC board for an excellent solder connection. So – you can now get multiple tracings between rows.

We have two tail lengths: a .200" short one and a .250" longer one to take the AS400 Solderpak** System. These are available in connectors with contacts on .100", .125" and .156" centers, and in layouts from 6 to 50 positions.

Use our coupon and we'll send you all the details.

There's more. There are some things we haven't told you – including materials and other details you need to know. Ask us for the literature.

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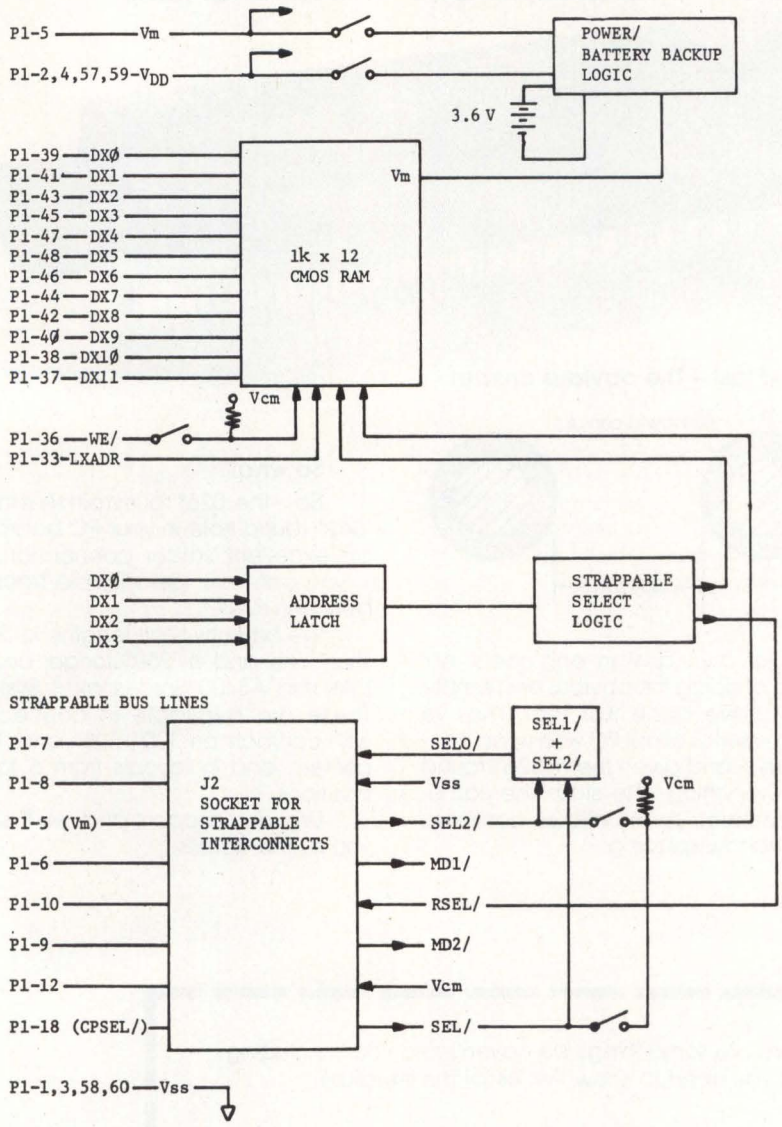
CIRCLE 77 ON INQUIRY CARD



Added to Cybertek's LP-12 family of low power OEM microcomputer boards is 4 x 5" (10.2 x 12.7 cm) 1k x 12 RAM module. Offering CMOS-compatible address, data, and control signals; battery backup option of 3.6-V rechargeable battery pack for data retention; and 750-ns access time at 5 V, LP-12D functions as general-purpose RAM board and as 6312 ROM simulator for prototyping

puter bus, include low power dissipation, write-protect capability, and optional onboard batteries for nonvolatility. It is jumper selectable for address assignment, and can be used for main memory, control panel memory, or both.

Circle 182 on Inquiry Card

Operating System Has Edit, Assemble, and Debug Capabilities

A Z80 assembler, text editor, in-memory file system, and labeled cassette tape storage system with full cyclic redundancy checks on all tape operations are integrated in the ZAPS cassette operating system. It is resident in 14k of memory, including all buffers and 1k bytes of symbol table space. Distributed by Algorithmics, Inc, Box 56, Newton Upper Falls, MA 02164 on Tarbell, Digital Group, or TDL standard tapes, the system runs on most 8080 and Z80 processors. ZAPS architecture is easily adaptable to many microprocessor I/O devices.

Similar to those for timesharing systems, the full context editor requires no line numbers; only actual data bytes are stored. The assembler processes the Zilog recommended form of mnemonics; various pseudo-operands are available. Debug and other software utilities are also included.

Circle 183 on Inquiry Card

Program Enters, Debugs, and Stores Assembly Language Programs

The DBUG program with supporting documentation is an aid for those who develop 8080 microcomputer software, allowing a user to enter a program into memory and to single-step it through. Developed by J. A. and C. Titus, DBUG: *An 8080 Interpretive Debugger* is available as a 100-page paperback for $5 from E & L Instruments, Inc, 61 First St, Derby, CT 06418, as the first of the BUGBOOK application series on assembly language programming. Written for paper tape use, the program can accommodate mag tape cassettes or CRT terminals.

Circle 184 on Inquiry Card

Self-Instruction Course Teaches Microprocessor Operation/Application

Individualized learning techniques instruct the user of the ET-3400/EE-3401 microprocessor learning system in microprocessor operation and design, applications, machine language programming, hardware, and I/O interfacing. Offered by Heath Co, Benton Harbor, MI 49022, the 3400 trainer features the 6800 microprocessor, 256 bytes of RAM (expandable to 512), a 1k ROM monitor, and 6-digit hexadecimal display and keyboard. Hardware/software experiments provide hands-on experience.

Circle 185 on Inquiry Card

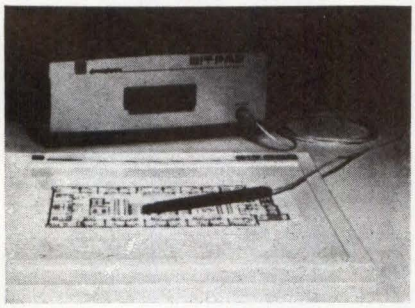
IBM Selectric Printer Is Approved For Microcomputer Output

Selecterm, an IBM Selectric II typewriter that is fully converted to a printer, has been announced by Micro Computer Devices, 960 E Orangethorpe, Bldg F, Anaheim, CA 92801. It may be directly connected to a parallel or serial port of any microcomputer, with all inputs at standard TTL level. All logic is in internal P/ROM so that no additional software is required.

Components include tab command, backspace, vertical tab, and bell. A special typing element produces all ASCII and full upper/lower case alphanumeric characters. All electronics and cable sets are provided along with documentation. Special features such as dual pitch, correcting, pin feed platen in 13 sizes, and noise reduction may be ordered. The $1650 printer may still be used as a typewriter, with the typewriter warranty remaining active since IBM has approved the unit.

Circle 186 on Inquiry Card

Flexible Input Peripheral Facilitates Digitizing For Small System Users



Designed to give fast, low cost data collection of X-Y values, the Bit Pad input device is a full capability digitizer permitting easy entry of positional information. Summagraphics Corp, 35 Brentwood Ave, Fairfield, CT 06430 has equipped each 11 x 11" (28 x 28 cm) unit with a byte-oriented 8-bit parallel output for simple interfacing to any microcomputer. The input device suits numerous applications, particularly those involving small systems.

Circle 187 on Inquiry Card

Z80-Based CPU Board Operates with 8080A General-Purpose Modules

Based on the POLY-BUSS™ structure, which allows either a Z80 or 8080A CPU board to be utilized with the same memory and I/O support boards, the MM1-ZCPU application system contains a Zilog Z80 microprocessor and is compatible with the company's MM1 modular support boards developed for the Intel 8080A. The board has a capacity for 4k of EPROM plus 1k of RAM; it operates at a clock rate of 2 MHz.

Control Logic, Inc, 9 Tech Circle, Natick, MA 01760 offers various memory and I/O boards for support, along with micrologic cards that may be used for special interface requirements. Software development is supported by the company's Microcomputer Development System.

Circle 188 on Inquiry Card

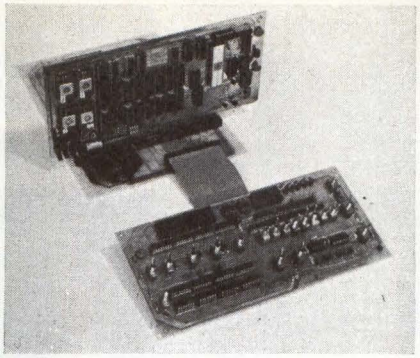
Two Support Circuits Operate With High Speed uProcessor

A high speed clock generator (Am8224-4) and 8-bit, bidirectional bus driver (8238-4) are both offered in ceramic hermetic DIPS by Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086 for operation with the high speed, 250-ns clock period version of the Am9080A-4 MOS microprocessor. The clock generator contains a crystal-controlled oscillator, divide-by-nine counter, high level drivers, and auxiliary logic functions. Buffering the Am9080A/8080A data bus from memory and I/O devices, the driver is controlled by signals from a gating array for proper bus flow and output control.

Circle 189 on Inquiry Card

S-100 Bus Compatible Microcomputer System Is Expandable To Many Levels

The Microputer 6000 is a microcomputer card for the S-100 bus structure, designed by CGRS Microtech, PO Box 368, Southampton, PA 18966 to perform both basic and more demanding functions with the addition of other cards. The 6000 card contains 4k of EPROM and 2k of RAM, with the 6502 microprocessor and TTL support logic. Support products include a front panel, I/O cards, packaging, and software.



Introductory level II microcomputer system from CGRS Microtech consists of level II MPU board and front panel, with motherboard 4, forming basis of powerful unit. Combination provides microprocessor with support circuitry, 2048 bytes of R/W memory, program storage memory, and frontpanel diagnostic system

Level II MPU board, containing microprocessor, clock, R/W memory, and program storage memory on one card, combines with the DMA type level II front control panel, with 16-bit address display, 8-bit data display, and multimode program execution control, to form the basis of a powerful microcomputer development system.

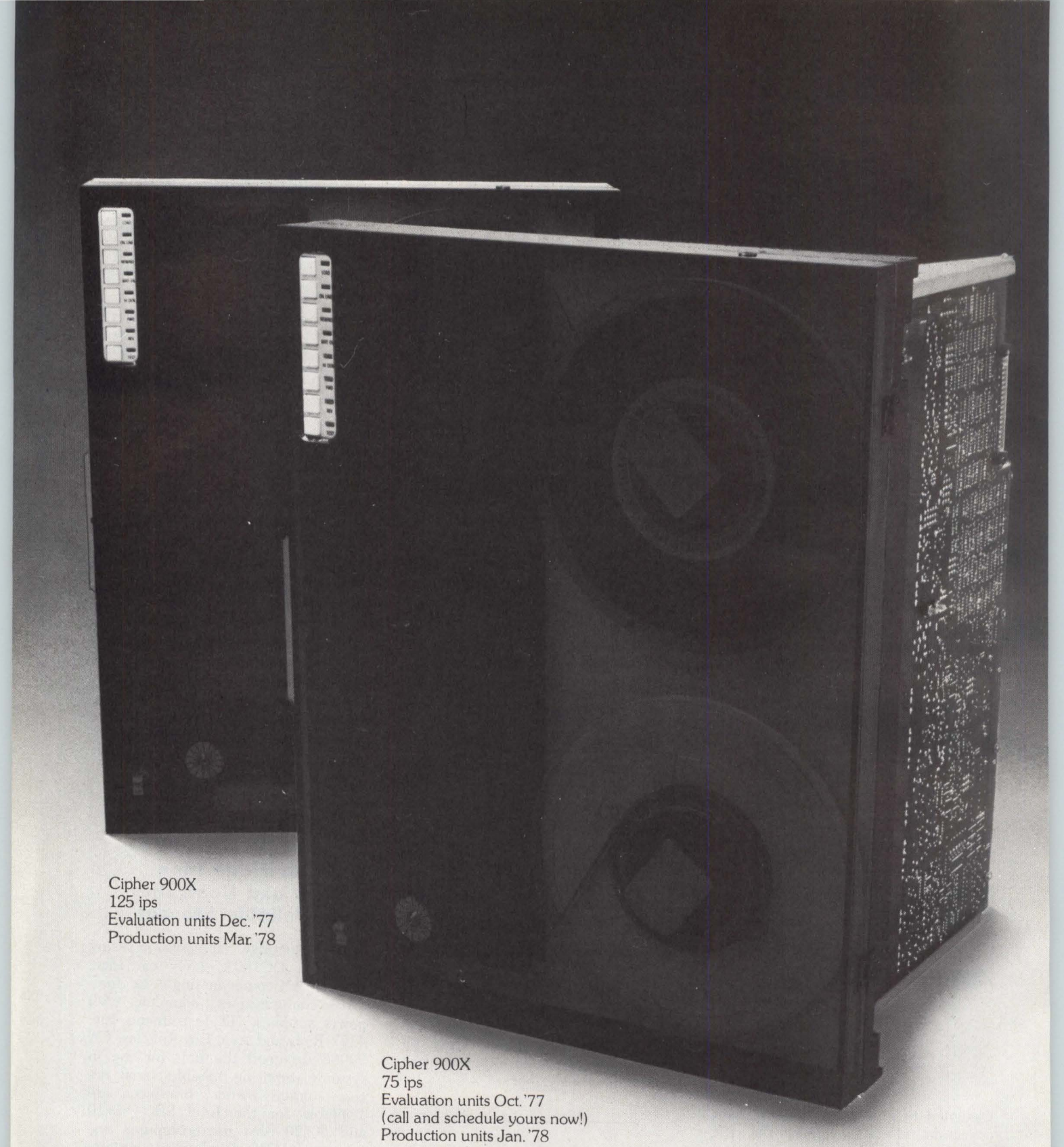
Circle 190 on Inquiry Card

Mini-Cartridge Tape System and Controller Give Reliable Storage

A mini-cartridge tape system using the 3M DC100A tape cartridge, DATAMAX comes in single- or dual-drive configurations, complete with power supplies. HT Instruments Inc, 4121 Redwood Ave, Los Angeles, CA 90066 designed the unit for use in systems requiring reliable serial access storage media. Interfaces are available for the Intel SBC 80/10 and 80/20 OEM microcomputer systems and MDS development system.

Also available is a mini-cartridge tape controller for the SBC 80 OEM microcomputer and MDS development system, which is used with the 3M DCD-1 mini-cartridge drive or DATAMAX. Common features of both units are low error rate, capacity of 100k bytes, easy handling and storage of media, and high transfer rate of 2530 bytes/s. □

Circle 191 on Inquiry Card



Cipher 900X
125 ips
Evaluation units Dec. '77
Production units Mar. '78

Cipher 900X
75 ips
Evaluation units Oct. '77
(call and schedule yours now!)
Production units Jan. '78

Cipher delivers a quiet blow to the competition.

Quiet as a whisper, the 75 and 125 ips Cipher vacuum tape transports simply obsolete every other vacuum drive on the market today.

By design and construction, the Cipher 900X vacuum tape drives are simply the best, most reliable tape transports on the market today. Bar none.

It starts with complete microprocessor control of all of the transport's functions, including complete self-test/diagnostics and a full measure of protection for the tape and an extraordinary reduction of maintenance problems.

In conjunction with our switched linear servo electronics, the microprocessor maintains total servo control during critical load and unload or power fail sequences. It's the smoothest tape handling you've ever seen; there is no possibility of tape damage even if a power failure should occur during high speed rewind.

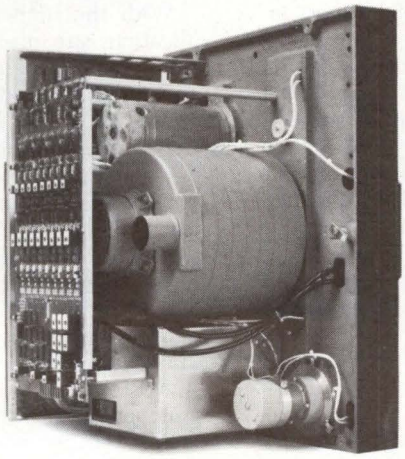
Power wise. The Cipher 900X series is the lowest power user of all vacuum tape transports. Averaging 300 to 350 Watts with a worst case 450 Watts Continuous Power Dissipation, the 900X series uses roughly half the 650 to over 1,000 Watts used by other vacuum tape transports.

You won't believe the quiet. Thanks to the Cipher 900X's multistage low speed vacuum pump, we use a much smaller motor. At 3400 rpms, our motor is substantially quieter than the competition's 10,000 rpm motors. A whisper instead of a high-pitched whine. And we've reduced more than noise. We've also knocked out 50% of the maintenance requirements found in traditional vacuum tape drives by eliminating belt drives.

No relays. Because the Cipher 900X incorporates opto-isolators to drive the blower motor and switch the high voltage AC components at the zero crossing line, transient generated line RFI is minimized. Power usage is drastically reduced. So is maintenance.

No incandescents. Light Emitting Diodes are used in place of incandescents in the 900X. With the field-proven reliability of solid state electronics, the unpredictable behavior of incandescents is eliminated.

Improved tape path. Only the long life sapphire cleaner and the chrome head (guaranteed for 5,000 working hours) come in contact with the tape. Air entering the tape path is filtered and the tape path itself is under a low positive pressure to prevent accidental ingestion of particular contaminants. No guesswork loading, since servos and transducers under control of the microprocessor automatically feed the column during load and unload. Servo controlled shutdown power fails protect the tape since, in the event of a brown out or failure, energy stored in the servos is utilized to effect a controlled power down.



Easiest to maintain and repair. Our exclusive Optical Sensing File Protect replaces troublesome switches, solenoids and trouble-prone mechanisms. And because the Cipher 900X has internally generated sequences of diagnostic and alignment tests, the MTTR is cut a good 30% by immediately locating the problem area. All mechanical and electronic assemblies in the 900X are modular. No special tools or fixtures are required; all critical tolerances are machined in.

The only thing missing are the problems: No belts, no hoses, no relays, no solenoids, no incandescents, no cooling fans, no power surges, no contaminants, no noise problems, no maintenance problems, no special tools or fixtures, no false EOT/BOT detection, no tape problems—no load snap, no whip, no shredding, no special precautions, no guesswork, and best of all—no price premium. None.

With design simplicity and the use of advanced solid state electronic components, the Cipher 900X series provides unparalleled performance, reliability and serviceability. At low cost. And quietly, too.

For further information and specifications, contact Cipher Data Products, 5630 Kearny Mesa Road, San Diego, California 92111. Headquarters: (714) 279-6550. TWX: 910-335-1251. Eastern Region: (617) 449-3182. Central Region: (312) 296-7250. Or contact your Cipher representative.

Cipher Data Products

CIRCLE 78 ON INQUIRY CARD

CHARGE-TRANSFER DEVICES—PART 3: DIVERSE USES OF CTDs FOR ANALOG, DIGITAL, AND OPTICAL APPLICATIONS

Eric R. Garen
Integrated Computer Systems, Inc
Culver City, California

Part 1 of this 3-part series compared the basic technologies of charge-transfer devices while Part 2 described the current status of charge-coupled device digital memories. This final part presents a potpourri of other charge-transfer devices and their applications, including devices for analog signal processing, digital logic, and optical image sensors.

A major use for charge-transfer devices (CTDs) is to delay analog signals, a requirement of many signal processing applications. This delay can be accomplished by sampling the incoming waveform and storing, in an analog shift register, charges that are linearly related to the sampled input voltage. The storage mechanism can be either a bucket-brigade device (BBD) or a charge-coupled device (CCD) shift register memory. (Both Reticon Corp and Fairchild Semiconductor have developed a wide range of these devices.) As described in Part 1 of this series, BBDs are typically slower and have lower dynamic range than CCDs, so that they are often used in audio applications.

A fine application for CTDs in recording motion picture optical soundtracks, for example, was developed by Nuoptix Inc. Optical soundtracks are clear stripes printed in a black background along the edge of the film. Sound is recorded by amplitude-modulating the width of the stripe; thus the stripe must have a nominal width that can be modulated both positive and negative [see Fig 1(a)].

However, during intervals with no sound, any dirt or scratches in the film will be heard as pops and crackles. To eliminate this problem the sound-stripe width is kept very narrow during periods of no sound, and opened to the nominal recording width only when sound is present [Fig 1(b)]. However, opening and closing the width must be done slowly, at a rate below the lowest audio frequency (about 30 ms); otherwise the opening would be heard as an audio tone such as a loud "pop."

This requirement leads to the problem solved by the analog delay line. If the stripe is opened slowly when each sound begins, the first cycles of the sound will be clipped, causing a muffled, distorted sound [Fig 1(c)]. In turn, this problem is solved by "anticipating" the audio signal and opening the stripe "ahead of time" [Fig 1(d)]. Actually this is accomplished by delaying the audio signal 30 ms with a CTD analog delay line prior to recording.

Whenever an incoming signal is detected, the stripe is gradually widened to just the width necessary to record the delayed audio signal (Fig 2). Initially the Reticon SAD 1024, a dual 256-sample BBD, was used; however, recently the company switched to the Reticon R5101, a 2000-sample CCD, to achieve better signal-to-noise performance and to provide the potential for a quadrupled delay period. While the BBD-based design provided 65 to 70 dB signal-to-noise ratios, the CCD models have been tested at 70 to 80 dB. The recording industry is rapidly accepting this device, made possible by CTD technology, because the resulting soundtracks are significantly better than any previously produced.

With the higher speed CCD analog devices, video applications are also feasible. For example, on video tape playback, the signals must be corrected for mechanical speed variation in the tape recorder. Even small fluctuations can cause large problems due to both phase and frequency distortion. This problem is solved by a "time-base corrector," a device that essentially clocks the playback signal into a CCD memory at the nonuniform rate defined by the clock track on the video tape. The signal is then read out of the CCD buffer at a uniform rate provided by an accurate system clock. Although actually a slight oversimplification, this illustrates the use of CCD memories as analog variable rate data buffers in video processing.

A European video application for analog CCDs has been announced by Philips, which is working on a "ghost-eliminator" for home receivers. The received video signal is stored in a CCD. Delay from the CCD device is adjustable to match the delay of the "ghost" image (caused by a secondary reflection that arrives by a longer path and is therefore delayed relative to the direct transmitted signal). The amplitude of the delayed signal is

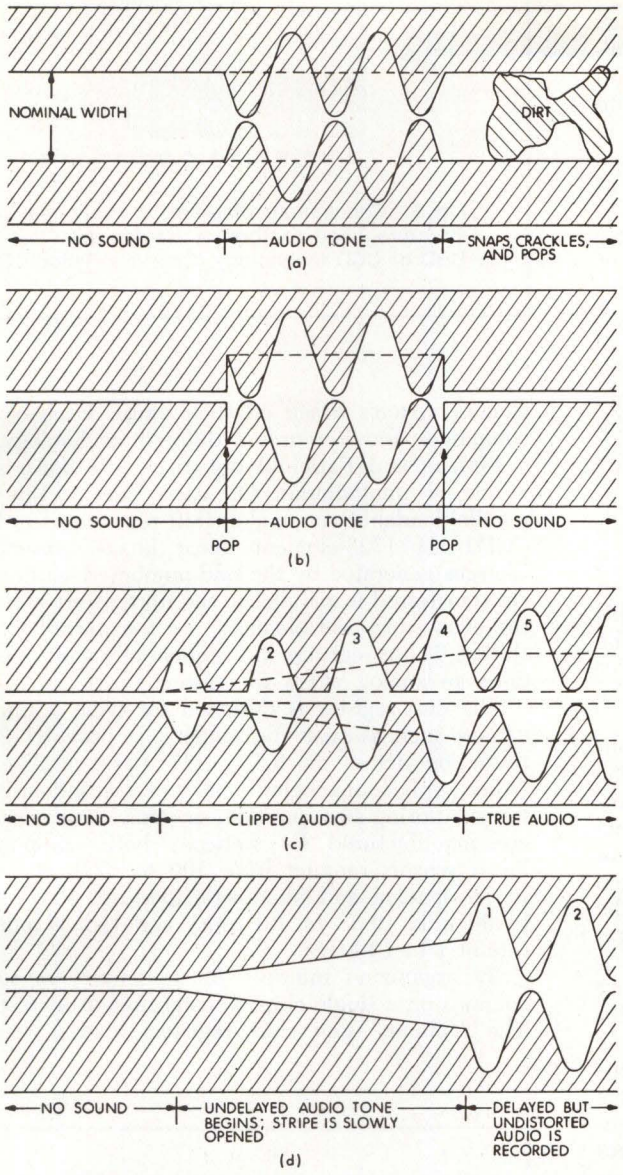


Fig 1 CTD application for motion picture optical soundtrack. (a) Generalized amplitude-modulation technique; dirt or scratches on film cause noise during intervals with no sound. (b) Narrow width sound stripe eliminates noise shown in (a) but fast opening and closing cause audible "pops." (c) Slowly opening stripe when tone first begins clips first three cycles; higher frequencies would have many cycles clipped. (d) Recording a signal delayed with CTDs allows sound stripe to be opened in "advance" of delayed signal

adjusted and subtracted from the original signal to cancel the ghost.

In the previous examples, the CTDs were simply serial-in serial-out analog shift register memories. By tapping intermediate storage cells to make available outputs at varying delays from the input, a multitude of signal processing applications become possible.

Transversal filters are formed from both BBDs and CCDs by using split electrodes to form capacitors whose size is related to the desired tap weight function. As the sampled signal moves down the line, it induces current in these capacitors that is proportional to the product of the tap weight and the signal amplitude. All the signals from each half of the electrodes are summed together and then both sides are subtracted in a differential amplifier. The weighting functions are programmed onto the device during fabrication by a pattern

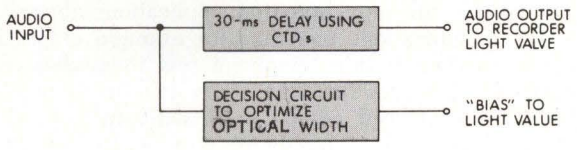


Fig 2 Simplified diagram of delay scheme to "anticipate" signal and open stripe prior to first sound cycles

on the processing mask. A standard family of low pass, band pass, and chirped filters as well as custom devices to meet individual requirements are available from Reticon (Fig 3).

R5602 mask programmed filters are a family of 64-stage BBDs available with various filter functions. In general, these filters can be made with linear phase and with skirts greater than 100 dB/octave. They will operate to sampling rates of 1 MHz and have ultimate rejection in the stop band of typically 50 dB. The end of the pass band for low pass filters and the center frequency for band pass filters will be a function of the input clock. Varying the clock frequency gives easily tuneable filter characteristics.

Complexity of onchip CCD processing is rapidly increasing as evidenced by Reticon's R5601, which performs the convolution portion of the chirp Z algorithm to perform either a discrete Fourier transform or the power spectral density of the input signal. The basic algorithm requires the input signal to be multiplied by a linear fm signal (a chirp), then to convolve the product with another chirp waveform, and finally to post-multiply the output with the same fm waveform of the pre-multiplier. There are then two outputs, the real and the imaginary parts.

Two device types are available: the R5601-1, which has the linear chirped waveforms, and the -2 with this function multiplied by a Hanning window function. The -1 can do either the total discrete Fourier transform or the power spectral density while the -2 can do only the power spectral density.

Each of the R5601 devices contains four 512-tap split electrode transversal filters, two sine and two cosine chirps. The device takes in 512 time samples and outputs 512 coefficients. It is capable of sampling the input signal at rates up to 2 MHz. Fig 4 shows the block diagram of the power spectral density function; the portion within the dotted block indicates the function contained on the device. Reticon also has circuit boards that perform the entire fast Fourier transform function.

CCD technology is not restricted to processing analog signals. TRW is pursuing the development of CCDs for digital logic. While CCDs are slower for even simple arithmetic functions than any conventional digital circuitry, they require less than half the chip area and have 20 times less power consumption than equivalent n-channel MOS devices. For example a 16-bit adder requires only 6.19 mm^2 for CCD logic compared with 16.5 mm^2 for standard n-channel MOS technology. Thus the CCD technology appears to be extremely promising for high volume, low speed applications where chip size and power dissipation are critical. For example, they could be used in appliance controllers which must minimize chip area to minimize cost.

Furthermore, since the technology can easily accommodate both digital and linear circuitry on the same chip, such functions as analog temperature control as well as digital sequence timing could easily be accomplished by one package. Still more potential applications abound in the telecommunications industry; for example chips that perform functions within telephone sets themselves (eg, repertory dialing) require low power to run on the line current, and also need not be particularly fast. To date, TRW has developed a family of basic arithmetic units including adders and multipliers and is currently developing a fully CCD arithmetic-logic unit.

Perhaps the most successful commercial application of CCDs to date has been for solid-state image sensors for TV cameras and facsimile equipment. Reticon, Fairchild, and General Electric have developed both linear and area-array sensors using CTD technology as well as complete

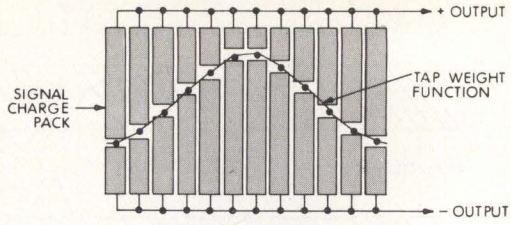


Fig 3 Conceptual diagram of split electrode structure used to form a transversal filter with BBD or CCD technology (Courtesy Reticon Corp)

camera systems based on their chips. Each of the three companies however uses a different technology.

Reticon and Fairchild organize their linear sensors as a line of photodiodes. On each side of this line is a parallel-loadable CCD analog shift register, as in Fairchild's CCD121H 1728-element linear image sensor (Fig 5). Charges generated by the odd-numbered sensing elements are transferred in parallel to the upper shift register, while the even-numbered elements are transferred to the lower shifter. These registers are sequentially shifted out to produce an analog video waveform.

The CCD register is designed for page scanning applications such as facsimile readers. It provides 200-line/in resolution across an 8.5 x 11" (21.6 x 28-cm) page. Other applications include many uses in industrial cameras for monitoring size, position, or gaps. Similar sensor chips are manufactured by Reticon; both companies make linear sensors ranging from 100 to 1728 elements, with sensor spacing and photo-site apertures varying from 15 to 50 mils (0.38 to 1.3 mm) and typical output clock rate of 1 to 10 MHz.

By organizing multiple linear sensors as side-by-side columns on a single chip, a raster area-array is developed. The "column" CCD shift registers load a single "row"

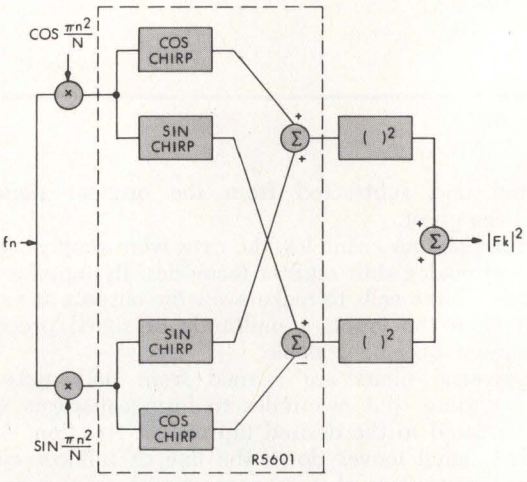


Fig 4 Block diagram of CZT algorithm implemented with Reticon's RS601 quad chirp-Z transversal filter CCD chip (Courtesy Reticon Corp)

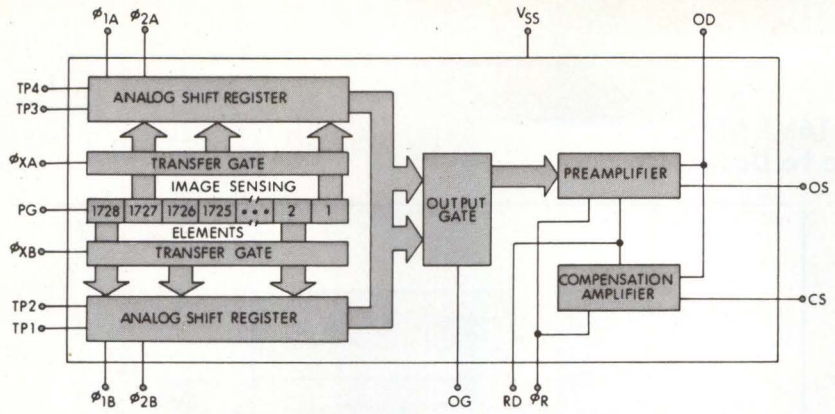


Fig 5 Block diagram of Fairchild CCD121H linear image sensor. 1728 image sensing elements are parallel-loaded through transfer gates into two CCD analog shift registers which are then output serially (Courtesy Fairchild Camera and Instrument Corp)

register to shift out the information on a row-by-row basis. Fairchild offers both a 100 x 100 element and a 244 x 190 element sensor. Reticon manufactures 32 x 32, 50 x 50, and 100 x 100 element arrays.

These devices have found wide applications in industrial automation and military cameras. For example Fairchild Imaging Systems manufactures an MV-201 camera based on the 240 x 190 Fairchild sensor. The MV-201 has been used almost exclusively in military applications and offers significant benefits over a conventional vidicon in size, weight, and power consumption—the entire camera less lens is 2 x 2.5 x 3.75″ (5 x 6.35 x 9.5 cm).

Its main military-application advantage is ruggedness. In one surveillance application this camera is literally shot from a cannon, and then transmits reconnaisance information as it parachutes back to earth. Needless to say, the launch is rough on the camera (20,000 G is not usually acceptable to a normal vidicon).

Reliability and maintenance-free operation are other inherent advantages. A normal vidicon requires constant alignment of the focus coils. In addition, the vidicon's high voltage supply is a source of trouble, and vidicons are susceptible to burn spots (a camera aimed at the sun will destroy its vidicon). All of these problems are circumvented with solid-state cameras. The only disadvantage of the CCD camera is its present resolution of 250 x 250 elements, half the linear resolution required for broadcast TV. With present progress in CCD technology, however, full TV resolution should soon be available.

Fairchild, Reticon, and General Electric manufacture solid-state cameras for industrial applications. The General Electric camera, however, uses a different sensor technology. The TM2200 series of automation cameras utilize arrays as large as a 244 x 248 element charge-injection device (CID). (Its principle of operation was described in the first part of this series.) The most appealing attribute of these cameras is their exceptionally low cost for high reliability. The camera itself costs less than $1000 (only $1200 including drive electronics with power supply and timing circuitry).

These devices have already been widely applied in industrial automation. For example the cameras permit nontactile measurement to an accuracy of 0.002″ (0.05 mm). Applications in quality control, monitoring of machine operation, and sorting of parts are typical.

The charge-transfer device applications described in this series are extremely broad because of CTD's applicability to digital as well as analog techniques. CCD digital memories will compete with magnetic bubbles in the rotating memory replacement market as well as a replacement for mass RAM. Meanwhile CCD technology will also expand its use in low cost digital controller applications and in analog audio and video signal processing. Finally, the use of solid-state cameras is already significant in automation and may soon replace conventional vidicons in broadcast television as resolution increases. The range of applications today is limited more by the reluctance of engineers to try this new technology than by the technology itself.

Second Family of Production 16k RAMs Provide Highest Performance to Date

A family of "second generation" 16k-bit RAMs, offered as direct replacements for "first generation" devices, are claimed to provide "the highest performance achieved to date in production" devices of this type and capacity. For example, one member of the family—the 2117-2, a 150-ns maximum access time device—has a cycle time of 320 ns, at least 55 ns faster than earlier 16k RAMs with that access time. There is also a 300-mV additional noise margin over competitive 16k RAMs.

Read/modify/write cycle time for the -2 is 375 ns. Family members -3 and -4, respectively, have maximum access times of 200 and 250 ns, read or write cycle times of 375 and 410 ns, and read/modify/write cycle times of 375 and 515 ns. All timing characteristics are guaranteed over a ±10% tolerance on all three power supplies (5, 12, and −5 V) and 0 to 70°C operating temperature range.

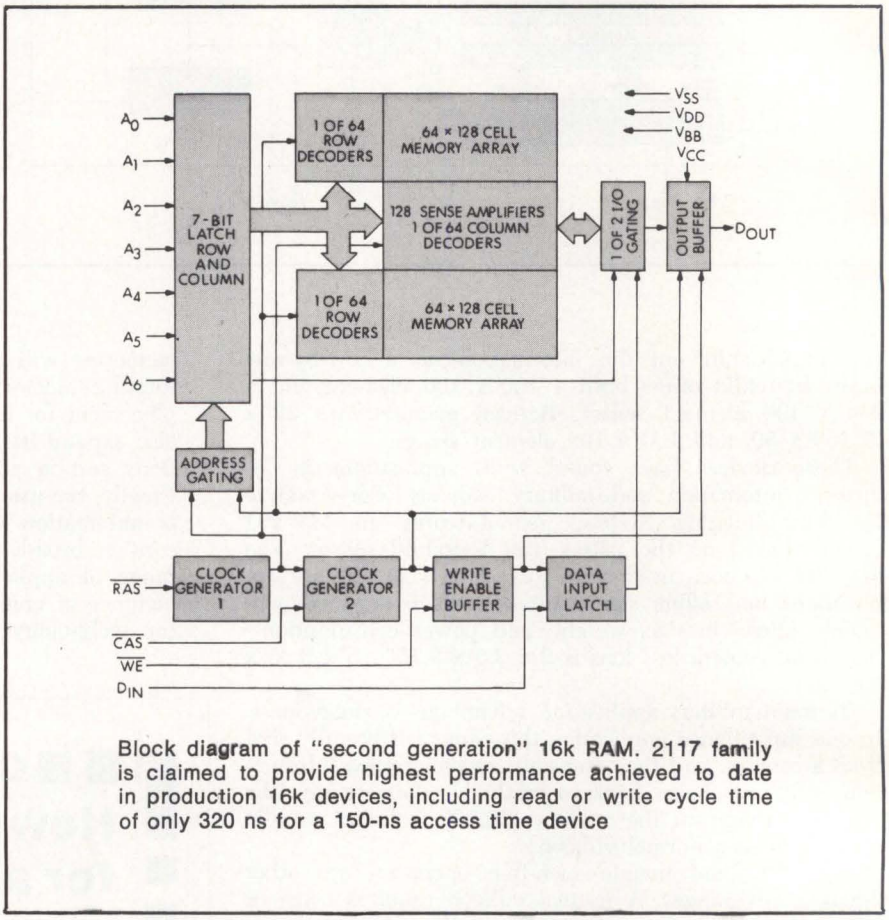
Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 has based design of this chip family on the same 2-layer polysilicon n-channel MOS technology used to produce the 2116 and other high density memory components. However, the 2117 chip design provides improved performance.

For instance, maximum power dissipation for all members of the family is 465 mW in active operation, 20 mW standby. Maximum average operating current is 35 mA, but drops to 1.5 mA when column address select (CAS) and row address select (RAS) are high. All inputs have 400 mV noise margin. Output drive is 4.1 mA when low and −5 mA when high (read or hidden refresh cycles only). Current spiking, which generates system power line noise, has been cut in half—to 110 mA.

These devices normally operate as unlatched-output RAMs, with conventional multiplexed address inputs (RAS and CAS). Since strobe timings are not critical, high performance is maintained at the system level.

Onchip latches are provided for address and data inputs. The output is 3-state. All inputs, including clocks, and the output are TTL-compatible. Refresh is 128 cycles at 2-ms refresh intervals.

A CAS-controlled output latching function increases applications range. The CAS strobe may be used independently of the RAS strobe to keep the data output valid instead of allowing it to return to the high impedance state. As a result, the RAM can emulate latched-output functions, including hidden refresh. Hidden refresh allows a refresh cycle to be performed without disturbing the data output state.



Block diagram of "second generation" 16k RAM. 2117 family is claimed to provide highest performance achieved to date in production 16k devices, including read or write cycle time of only 320 ns for a 150-ns access time device

Minor changes in clock system timing are required to use this mode. To emulate the normal latched output operation of such RAMs as the 2104A and 2116, the 2117 clocks can be used to hold the CAS clock low and allow the RAS clock to go high. This reduces power dissipation and keeps data output valid through an ensuing refresh cycle. The output returns to the normal high impedance state when CAS goes high.

With the normally latched devices, hidden refresh is implemented by running a RAS-only refresh cycle after a RAS/CAS read cycle. With the 2117, RAS is clocked as before but CAS is held low continuously, thus maintaining valid output data from the read cycle through the refresh cycle.

Circle 350 on Inquiry Card

CMOS Generators Provide As Many As 15 Programmable Bit Rates

Clock signals required for digital data transmission systems are provided by HD-4702 and -6405 CMOS programmable bit rate generators. The -4702 can be programmed to provide any of 13 commonly used bit rates, has onchip input TTL-compatible pull-up circuitry, and dissipates 4.5 mW. It is pin-out/specification identical to 34702 devices. -6405 can be pro-

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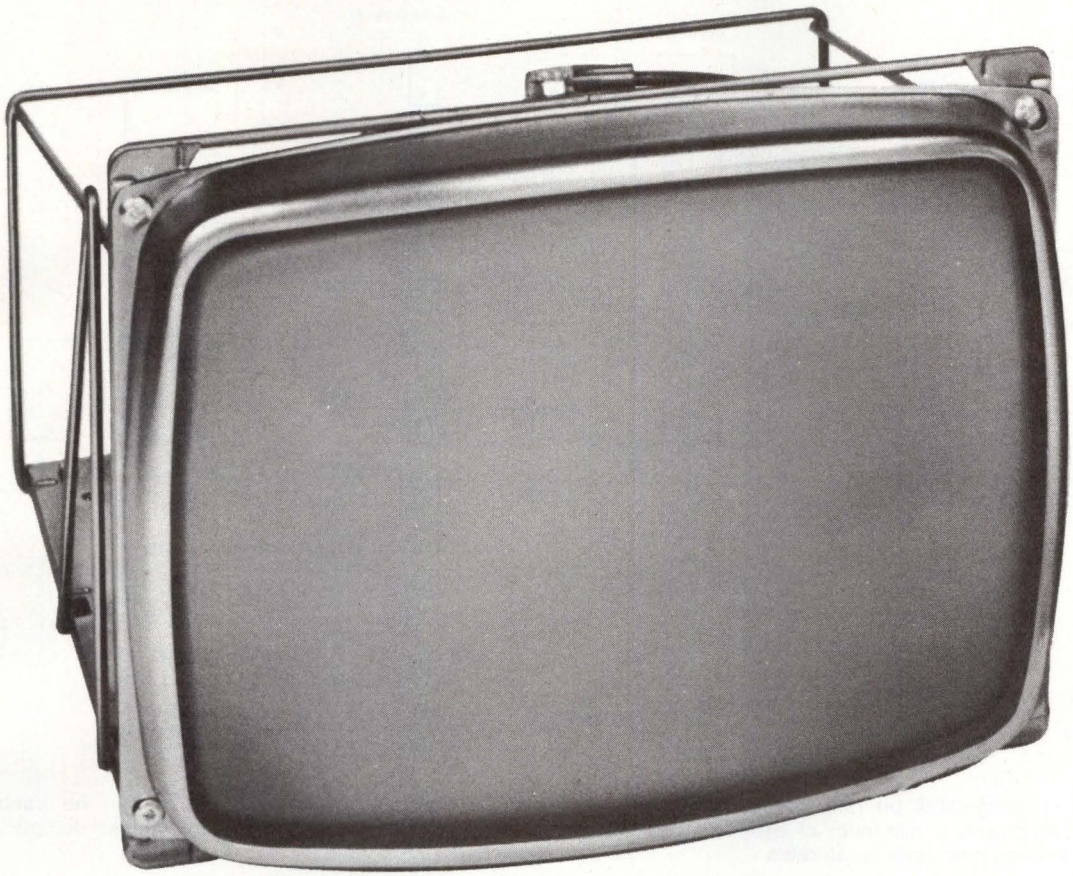

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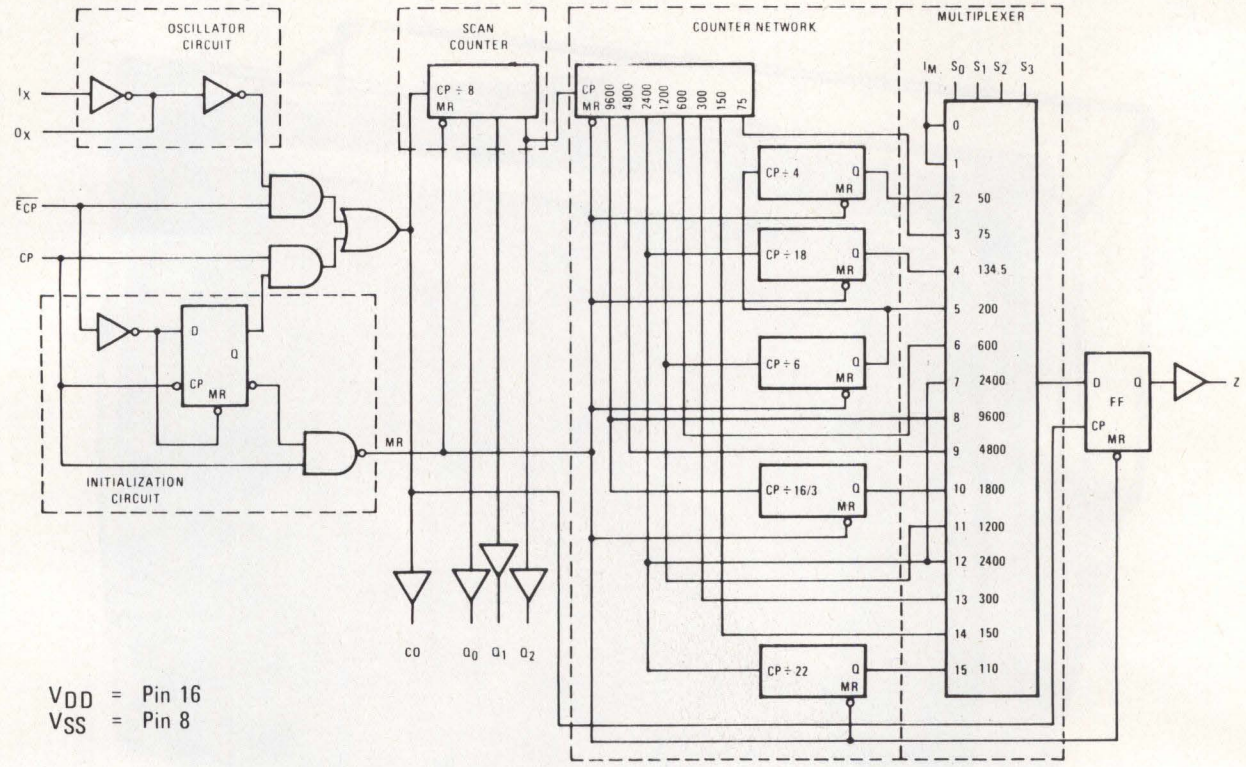

HD-4702 programmable bit rate generator block diagram. Up to eight transmission channels can be controlled in large systems with a minimum of external logic. Any one of 13 bit rates is program selectable; companion 6405 device provides two additional rates

grammed to 15 selectable rates, has no pull-up circuitry, offers standard high impedance CMOS inputs, and dissipates 4 mW.

Both devices operate at 2.4576 MHz and have onchip oscillator circuits which are controlled from external crystal or clock sources. A buffered input clock on each device, operating at the oscillator frequency, can be used to operate the company's HM-6100 CMOS microprocessor system. Operating voltage maximum range is 4 to 7 V.

Multichannel operation can be provided with a minimum of external logic by having the clock frequency (CO) and ÷8 prescaler outputs (Q_0, Q_1, and Q_2) (see diagram) available externally. All signals have a 50% duty cycle except 1800 and 2000 baud, which have less than 0.39% distortion, and 3600 baud, which has less than 0.78%.

Bit rate at the output (Z) depends on choice of the four rate select inputs (S_0 to S_3). Two of the 16 for the -4702 and one of the 16 for the -6405 select an input into which the user can feed either a different frequency or a static level to generate "zero baud," rather than selecting an internally generated frequency.

An initialization circuit generates a common master reset for all flip-flops (FF). This signal is derived from a digital differentiator which senses the first high level on the CP input after $\overline{E_{CP}}$ goes low. When $\overline{E_{CP}}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

Harris Semiconductor, PO Box 883, Melbourne, FL 32901 supplies both devices in 16-pin plastic or ceramic DIPs in either −40 to 85°C or −55 to 125°C temperature ranges for industrial or military applications. Storage temperature range is −65 to 150°C.

Circle 351 on Inquiry Card

Chip Set Reduces Remote Control Part Count

As many as 31 commands can be provided for remote control of equipment via radio frequency, infrared, ultrasonic, or hardwire transmission with a chip set introduced by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051.

(Continued on p 162)

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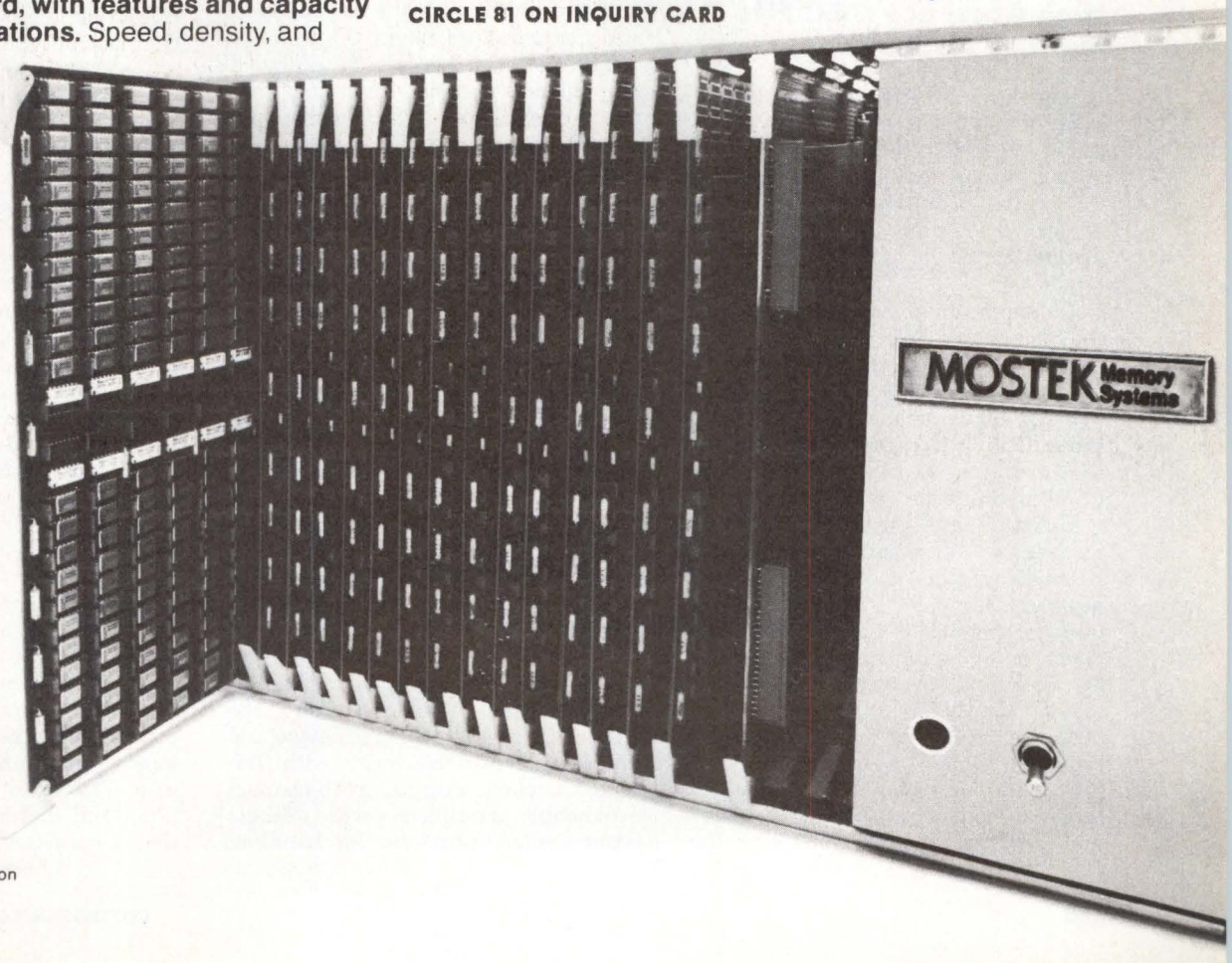
Call now for the complete story. Either the Eastern office 201/842-5110, Western office 408/287-5081, or Memory Systems Marketing at 214/242-0444 extension 2554, Mostek Corporation, 1215 W. Crosby Road, Carrollton, Texas 75006.

MOSTEK Memory Systems

CIRCLE 81 ON INQUIRY CARD



This set, consisting of an S2600 transmitter and S2601 receiver, includes onboard keyboard inputs, oscillators, and both analog and digital receiver outputs.

There is no need for external crystals; only a resistor and a capacitor are required externally for a frequency reference. The receiver has a very high immunity to noise or spurious commands and will operate with up to ±24% difference in timing frequency.

Spurious command rejection has been achieved through a 5-bit command code system which requires that identical, proper commands be transmitted twice in succession before the receiver issues an output. In addition, a correct 5-bit fixed (mask-programmable) preamble code must be received.

The receiver is a p-channel MOS chip with onchip oscillator, five keyboard inputs, 40-kHz signal input, decoding logic, and 11 outputs (six digital, three analog, a pulse train, and an on/off). Onchip memory saves received commands and the logic compares them with later receptions. If the codes do not match, the receiver saves the last code received for its next comparison try. When two successive identical codes are received, a valid output is issued.

Five binary outputs present the 5-bit command code received; the sixth digital output is a "data valid" signal. The pulse train is useful for indexing a stepping switch, such as for industrial controls, while the on/off output can be used to kill and restore the main power supply. Analog outputs can independently provide up to 64 distinct dc levels for controlling motor speed, volume, brightness, or similar electronic settings; one of these analog outputs is mutable.

The transmitter is a low power drain CMOS chip (dissipating only 20 mW) with an onchip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and control logic. Its output is a 40-kHz square wave which is pulse code modulated. A 12-bit message including sync frame, preamble, 5-bit command code, and end of message bits can be transmitted every 38.4 ms.

Circle 352 on Inquiry Card

High Accuracy DAC Fits Military Applications

A monolithic 8-bit D-A converter with a maximum relative accuracy within ±0.1%, the SE/NE5009 features an output current that settles typically in 60 ns and a full-scale current drift of just ±10 ppm/°C. It interfaces directly to TTL, ECL, HTL, and CMOS families.

Although functionally equivalent to the company's NE/SE5007/8 series of D-A converters, this device offers twice the level of accuracy. Signetics, PO Box 9052, Sunnyvale, CA 94086 states that it is equal or superior to the Precision Monolithic DAC-08A in all parameters.

Using three of the new devices, an inexpensive 3-digit BCD converter can be configured that will provide ±0.1% accuracy. Input for the BCD converter uses the popular 8-4-2-1 coding.

Operating temperature range for the 16-pin military version DIP is —55 to 125°C. Maximum supply voltage rating is 36 V. Power dissipation is typically 33 mW at ±5 V and 135 mW in ±15-V supplies. Accuracy differential nonlinearity (±0.19% max) and settling time specified for the unit are valid over the entire operating temperature range.

The device is specifically designed for military systems, precision process control systems for industry, and other high accuracy applications that require analog output from a digital source. It is suited for fast 8-bit converters, variable gain amplifiers, waveform generators, 3-digit BCD converters, and programmable power supplies.

Circle 353 on Inquiry Card

All Data Acquisition System Functions Combined on Single Chip

A 28,000-mil² CMOS chip produced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 is claimed to be the industry's first single-chip data acquisition system. Included on the ADC0816 (MM74C948) device are a true 8-bit A-D converter with Tri-State® latched outputs, a 16-channel expandable multiplexer with address input latches, provision for handling external signal conditioning, and control logic for interfacing the chip to all standard microcomputers.

Operation of the device is said to be virtually adjustment free. Linearity and accuracy are equal to that of most hybrid and discrete implementations and are better than that of most monolithic A-D chips. Linearity, zero error, and full scale error at 25°C are no more than ±½ LSB each. Total unadjusted error, the sum of all errors, is ±¼ LSB typically and ±½ LSB maximum. Absolute accuracy, the sum of total unadjusted error and the quantization error, is guaranteed to be less than 1 LSB.

The A-D converter is partitioned into three major sections: high impedance chopper-stabilized comparator, 256-resistor ladder network with analog switch tree, and successive approximation register. Most important section is the comparator, which is responsible for the ultimate accuracy of the entire converter. Any drift in this section has greatest influence on device accuracy.

A dc input signal is converted by the comparator to an ac signal which is then fed through a high gain ac amplifier and its dc level is restored. Since drift is a dc component, which is not passed by the ac filter, this technique limits the amplifier's drift component, and makes the entire A-D converter insensitive to temperature, long term drift, and input offset errors.

Inherent monotonicity of the resistor ladder network prevents oscillations that could be catastrophic in closed-loop feedback control systems and does not cause load variations on the reference voltage. In this approach, with unequal or shorted resistors, the slope of the output transfer function cannot differ from the slope of the analog input.

The multiplexer directly accesses any one of 16 single-ended analog signals. A particular input channel is selected by using the address decoder. The address is latched into the decoder on the low-to-high transition of the address latch enable signal. A start convert signal can also be used as the address latch enable signal.

Additional single-ended analog signals can be multiplexed to the A-D converter by disabling all multiplexer inputs. The additional external signals are connected to the comparator input and the device ground. Further signal conditioning, such as prescal-

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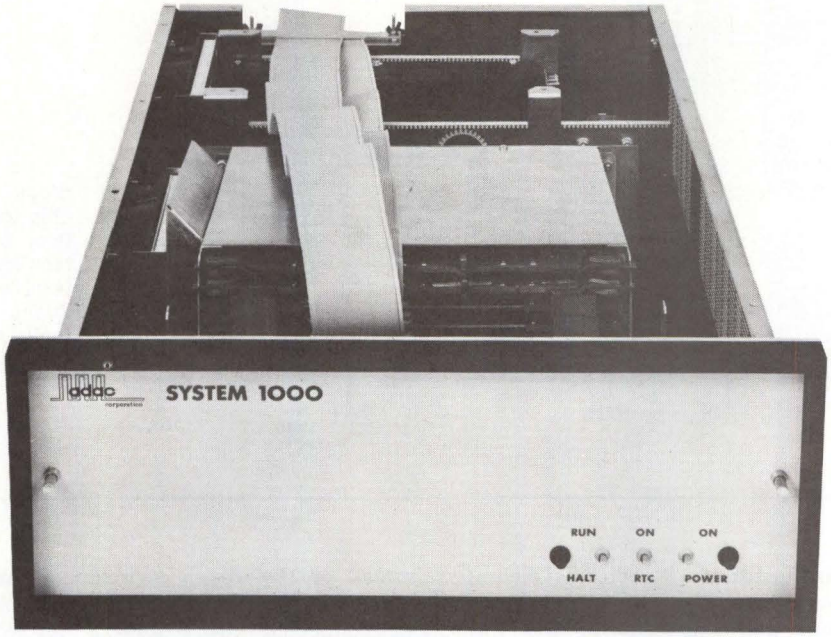

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A single System 1000 can provide up to 700 high level analog input channels, or 128 analog low level input channels, or 700 digital I/O functions. For even greater capacity, a Model 1950 Bus repeater card allows additional 1000 Systems to accommodate as many analog or digital I/O modules as desired.

System 1000 in the stand-alone configuration comes with minimum memory of 4K RAM with up to 24K of additional memory possible in both RAM and ROM. The LSI-11 16 bit resident computer can communicate with any of the extensive library of Adac analog and digital I/O modules or other LSI-11 compatible modules. Applications include digitizing outputs of thermocouples, strain gages, isolation amplifiers, LVDT, RTD, photomultipliers, potentiometers, optical scanners, or giving outputs to scopes, pen recorders and actuators.

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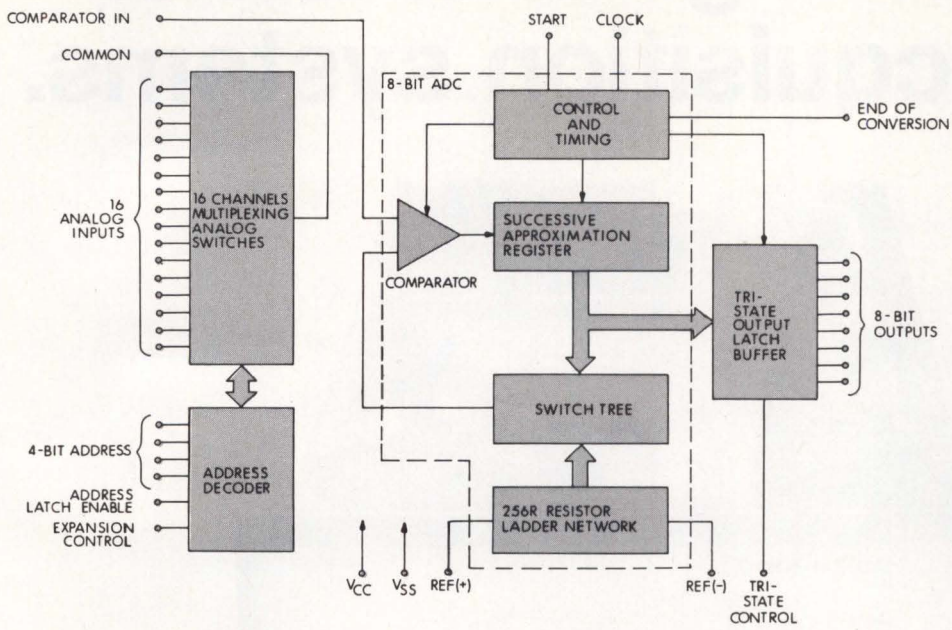

Block diagram of single-chip data acquisition system. Device relieves interface and compatibility problems of multichip configurations at one-fifth to one-tenth the cost of multiple boards

ing, sample and hold, and instrumentation amplification, can also be added between analog input signal and comparator input.

Because of the CMOS circuitry—despite the high level of integration and the wide variety of functions performed—the chip consumes only 15 mW of power. It operates from a single 5-V supply. Absolute operating temperature range is —40 to 85°C, storage range is —65 to 150°C. Operating input voltage (V_{cc}) range is 4.5 to 6 V; absolute maximum V_{cc} is 6.5 V.

Typical conversion time for the device is 100 μs; however the device can operate at 50 μs without degradation. Clock frequency is 50 kHz minimum, 640 kHz maximum.

By attaining the structure of a data acquisition system on a single chip, the user is relieved of multichip interface and compatibility problems. In addition, the patented A-D conversion technique guarantees that the chip will have no missing codes and be monotonic. There is no need for external zero and full scale adjustments. Simple microprocessor interfacing is provided by latched and decoded address inputs and latched Tri-State outputs.

The device is capable of performing without external components in ratiometric sensing applications. Because in such systems the change in parameter is measured instead of the absolute value, the device can operate with the transducer connected directly to the multiplexer inputs, but without an external voltage reference. However, a commercially available voltage reference is required for applications that require an absolute measurement.

Two versions of the chip are being produced: the ADC0816, with an absolute accuracy of ±½ LSB, is priced at $19.95 in 100-unit quantities; and the ADC0817, with an accuracy of ±1 LSB, sells for $17.95 in the same quantities. Each is said to replace $100 to $200 worth of hybrid and discrete component analog boards.

8-Bit DACs Feature 85-ns Settling Time

High speed current steering switches on the model DAC-08BC D-A converter, a 16-pin plastic DIP for 0 to 70°C operation, and the -08BM, a ceramic device for —55 to 125°C military range operation, achieve 85-ns settling time with low glitch full scale changes. Nonlinearity is held to less than 0.19% or ½ LSB.

Each D-A converter from Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 is made up of eight fast switching current sources, a diffused R-2R ladder network, a bias circuit, and a reference control amplifier. The R-2R ladder network gives excellent temperature tracking and results in a gain temperature coefficient of 10 ppm/°C. Monolithic fabrication results in excellent linearity and temperature coefficient in addition to fast settling time and low cost.

An external reference current programs the scale factor. This current can be varied for 1- or 2-quadrant multiplying operation. The output current has a high voltage compliance of —10 to 18 V, allowing direct current to voltage conversion with just an output resistor.

Power supply requirement is 4.5 to 18 V at 3.8 mA and —4.5 to —18 V at 7.8 mA. The devices interface directly to a variety of logic families such as TTL, DTL, CMOS, and HNIL.

Circle 354 on Inquiry Card

Quad Plasma Display Drivers Fit Varied Terminal Applications

Two ac plasma display drivers, the SN75426 and 75427, announced by Texas Instruments, Inc, PO Box 5012, Dallas, TX 75222 feature 90-V output

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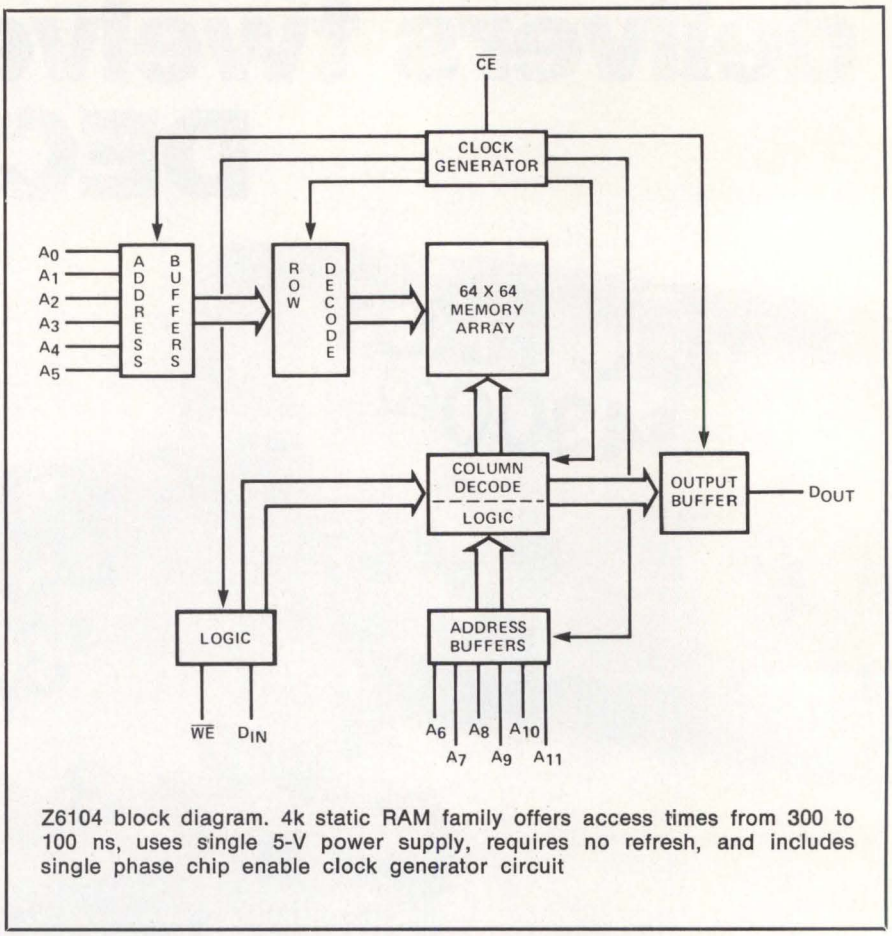
swing, CMOS-compatible inputs, 1-MΩ typical data input impedance, and 30-mA clamp diodes on the output. Independent addressing of each gate enables serial or parallel use. The quad devices are said to be suited for such applications as information display point-of-sale, financial transaction, and text editing terminals.

Logic of the two drivers is complementary to permit controlled writing or erasing at a specified point on the display. Output of the 75426 noninverting pulser is normally near ground potential and is pulsed to near V_{cc2}; output of the 75427 inverting pulser is normally near V_{cc2} potential and is pulsed to near ground.

The devices require two power supplies: one for the logic section and one for the high voltage outputs. Both drivers are characterized for operation from 0 to 70°C.

Circle 355 on Inquiry Card



Z6104 block diagram. 4k static RAM family offers access times from 300 to 100 ns, uses single 5-V power supply, requires no refresh, and includes single phase chip enable clock generator circuit

4k RAM Family Usable With Full Range of Computer Types

Production of a 4096 x 1 static RAM for use with microcomputers as well as mainframes has begun by Zilog, 10460 Bubb Rd, Cupertino, CA 95014. One of the first two memory products made by this company, the Z6104 is available in five access speeds from 300 to 100 ns, enabling the wide range of application. The -1 has 100-ns access time/170-ns cycle time and 550-mW operating power. Respective specifications for the other family devices are: 150/250 ns, 440 mW for the -2; 200/340 ns, 385 mW for the -3; 250/380 ns, 220 mW for the -4; and 300/440 ns, 220 mW for the -5.

All 12 TTL-compatible address input pins (see diagram) are used to select a cell within the 64 x 64 memory array. Address inputs are strobed into the RAM with the chip enable ($\overline{CE}$) high-to-low edge. Chip enable is used as a clock input which triggers the movement of data throughout the RAM. Since the RAM is a static device, $\overline{CE}$ may be halted at any time without the loss of data. The $\overline{CE}$ input during its high-to-low transition is used as the edge for internal data movement. A $\overline{CE}$ "1" input (logic level high) forces the RAM into a non-selected precharge mode. In this mode the power dissipation is reduced.

Write enable ($\overline{WE}$) input controls the chip read/write functions. A $\overline{WE}$ "1" (input high) is the signal for a read cycle. Data appearing at the output during the read cycle are at the same logic level that was written into the RAM cell. A $\overline{WE}$ "0" (input active low) is the signal for a write. Information at the data input (D_{IN}) pin is written to the selected memory location at this time.

In the read cycle, with the $\overline{WE}$ input high, $\overline{CE}$'s high-to-low transition will cause the data at the location specified by the address inputs to appear at the output pin, D_{OUT}. D_{OUT} goes from a high impedance (inactive) mode to the low impedance (active) mode after the access time. When $\overline{CE}$ goes back high, D_{OUT} returns inactive.

In write cycle, data to be written into the chip from D_{IN} are loaded into the selected location on the later occurring edge of $\overline{CE}$ or $\overline{WE}$. The data must remain stable for the required setup and hold times about either $\overline{WE}$ or $\overline{CE}$ edge, whichever occurs first. When writing, D_{OUT} goes active, indicating the logic state of the addressed cell until $\overline{CE}$ returns high.

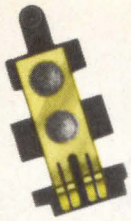
The read/modify/write cycle is an extension of the read and write cycles. Data are read after an access time and in the same cycle are modified with a write operation. For this cycle D_{OUT} starts inactive, and goes active after the write. At the end of the cycle, signified by $\overline{CE}$'s positive edge, D_{OUT} becomes inactive.

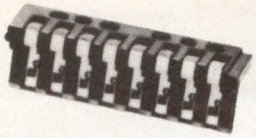
The output (D_{OUT}) is capable of driving two TTL loads or up to eight TTL low-power Schottky loads. Output voltage levels are: $V_{OH} = 2.4$ V min and $V_{OL} = 0.4$ V max.

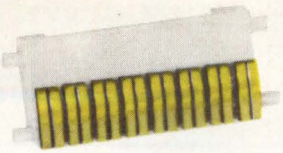
Circle 356 on Inquiry Card

Plastic p/ROM Replaces More Expensive EPROM

A silicon gate, 8k electrically programmable ROM (p/ROM) that is not reprogrammable, the MCM2708P is







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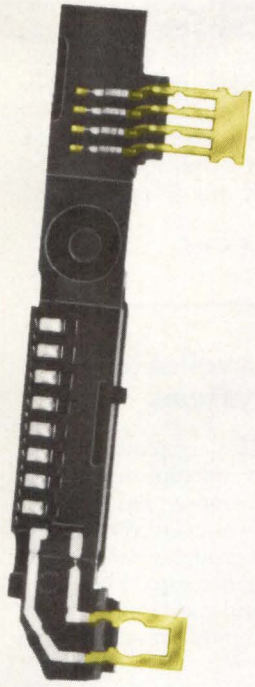

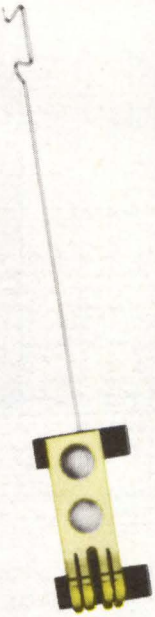

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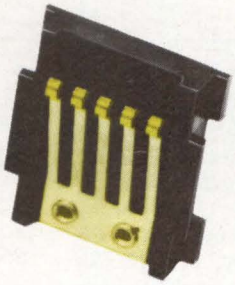
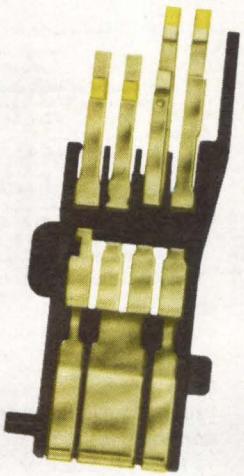
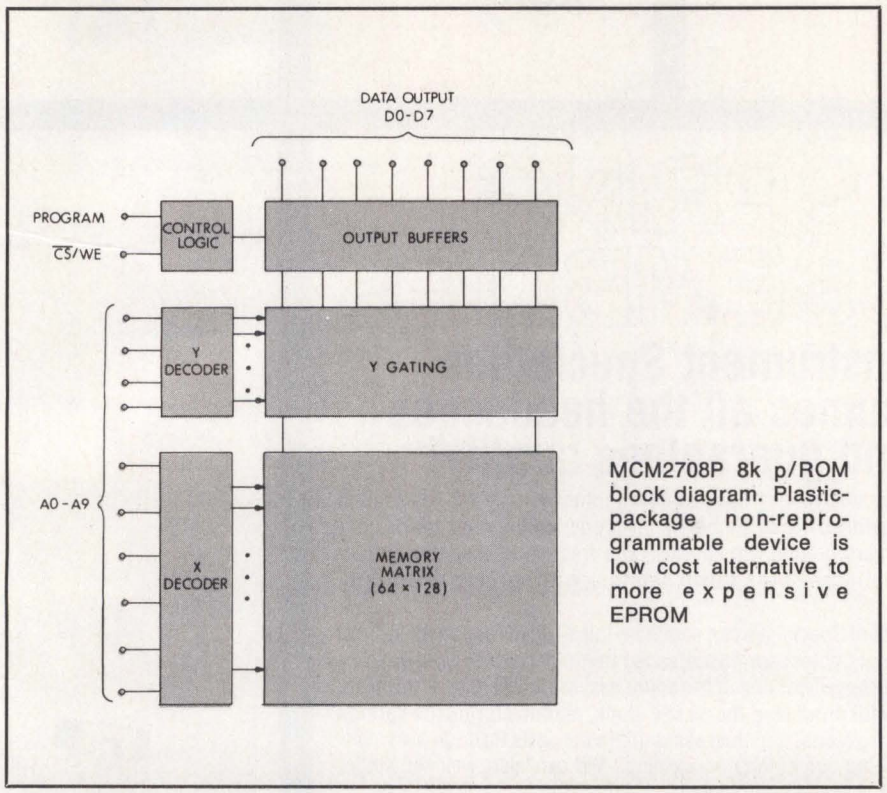






MCM2708P 8k p/ROM block diagram. Plastic-package non-reprogrammable device is low cost alternative to more expensive EPROM

a low cost alternative for compatible ultraviolet-light erasable p/ROMs (EPROMs) such as the MCM2708L. The plastic-package is also pin-compatible with MCM65308, 68308, and 2308 mask-programmable ROMs. It is organized as 1024 bytes x 8 bits.

Maximum access time is 450 ns; nominal power supplies are 12, 5, and −5 V; and total power dissipation is 800 mW. Read operation dc characteristics include 1-μA type, 10-μA max address and chip select input sink current as well as output leakage current; 50-mA typ, 65-mA max V_{DD} supply current; 6-mA typ, 10-mA max V_{CC} supply current; 30-mA typ, 45-mA max V_{BB} supply current; 0.45-V max output low voltage; and 3.7-V and 2.4-V min output high voltages. Absolute maximum ratings include 0 to 70°C operating temperature and −65 to 125°C storage temperature.

The 24-pin 2708P DIPs are available from Motorola Integrated Circuit Div, 3501 Ed Bluestein Blvd, Austin, TX 78721 at suggested pricing of $9.95 each in 100- to 999-unit quantities. (Comparable quantities of the 2708L are $21 each.)

Circle 357 on Inquiry Card

Faster 8k ROMs Are Drop-In Replacements

A series of 1024 x 8 bipolar ROMs rated at 55-ns address access time for commercial grades and 70 ns for military temperature grades has been introduced by Monolithic Memories, Inc, 1165 E Arques Ave, Sunnyvale, CA 94086. The 20-, 22-, and 24-pin packages (6289-2, 6286-2, and 6280-2, respectively) are designed to be pin-compatible replacements for slower ROMs produced by other vendors; the 22- and 24-pin DIPs are also compatible with the company's bipolar p/ROMs.

Circle 359 on Inquiry Card

12-Bit DAC Available For ±12-V Systems

Designers of ±12-V systems, such as those including microprocessors or semiconductor memory, are now offered a 12-bit D-A converter that operates at that voltage range. The DAC80Z is pin-compatible with DAC80 family and meets all its specs with power supplies ranging from ±11.4 to ±16.0 V.

Other characteristics of the DAC80 family, manufactured by Burr-Brown, PO Box 11400, Tucson, AZ 85734, are unaffected. The Z version converter offers 12-bit resolution, ±½ LSB maximum nonlinearity, and a settling time of 300 ns to ±0.01% (current output model), and contains an internal reference. The only performance consideration when operating it from ±12-V supplies is that the ±5-V output voltage range is the maximum useful range.

Circle 360 on Inquiry Card

Dual Power Driver Interfaces Low and High Power Devices

DI-446 is a dual channel version of the -445 power driver used in telecommunications and industrial control systems. It provides interfacing between low power logic and higher power system elements such as relays and control actuators.

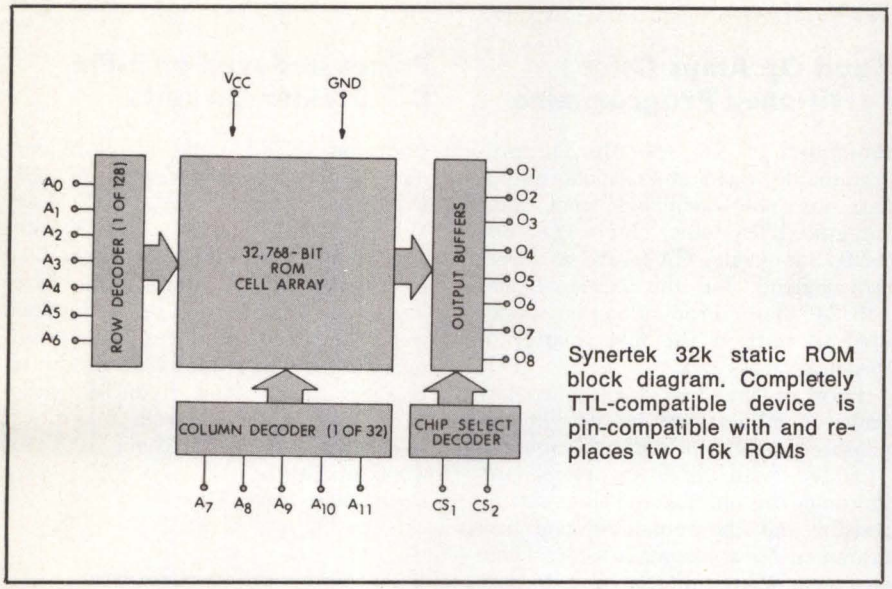
Input circuitry enables operation with either positive or negative true inputs from all logic systems. Logic threshold voltage can be adjusted to provide noise immunity for input signals with absolute levels between 40 and −40 V.

Available from Dionics, Inc, 65 Rushmore St, Westbury, NY 11590, the 16-pin DIP universal dual high voltage, high current device operates at up to 80 V and 300 mA peak. A fully isolated high current diode suppresses transients when the device is driving an inductive load.

Circle 358 on Inquiry Card

32k Static ROM Available As EPROM Replacement

SY2332, an n-channel silicon gate 32k ROM featuring a maximum address access time of 450 ns, is compatible with all popular microprocessors and similar applications. It is designed to replace two 2716 pin-compatible 16k EPROMs, and can eliminate the need to redesign PC boards for volume mask-programmed ROMs after prototyping with EPROMs.



Synertek 32k static ROM block diagram. Completely TTL-compatible device is pin-compatible with and replaces two 16k ROMs

Claimed by Synertek, PO Box 552, 3050 Coronado Dr, Santa Clara, CA 95052 to be the "first" of its type to be "truly available in the marketplace," the device is organized as 4096 x 8 bits, requires only a single 5-V supply, and offers TTL input and output levels with a minimum of 0.4-V noise immunity. Operation is totally asynchronous. No clock input is required. Two programmable chip select inputs allow four 32k ROMs to be OR-tied without external decoding. Three-state outputs enable wire-OR memory expansion.

Absolute maximum ratings for the device, which should not be maintained for extended periods, include 0 to 70°C ambient operating temperature; —65 to 150°C storage temperature; —0.5- to 7-V supply to ground potential, applied output voltage, and applied input voltage; and 1-W power dissipation. Dc characteristics under test conditions include 2.4-V min, 4.75-V max output high voltage; 0.4-V max output low voltage; 2-V min, 5-V max input high voltage; —0.5-V min, 0.8-V max input low voltage; 10-μA max input load and output leakage currents; and 120-mA power supply current. Ac characteristics include 150-ns max chip select and deselect times.

The device is available in either ceramic or plastic 24-pin packages. A one-time tooling fee of $750 to $1000 is charged in addition to the price of $35 each in 100- to 999-part quantities. A turnaround time of three weeks for initial parts is provided by custom contact mask-programming of inventoried wafers.

Circle 361 on Inquiry Card

Op Amps and Comparators Housed in Quad Package

Rather than containing four identical circuits, the MC3405/3505 quad-function linear package combines two different functions: a pair of operational amplifiers, similar to type MC3403/3503, and a pair of dc comparators, similar to type LM339/139. Both functions are capable of common-mode inputs down to the negative supply and operate from a single 3- to 36-V supply or dual ±1.5- to ±18-V supplies.

Available from Motorola Semiconductor Products, Inc, PO Box 20912, Phoenix, AZ 85036, the MC3405 has a specified operating ambient temperature of 0 to 70°C, while the MC3505 operates from —55 to 125°C. Both are in plastic or ceramic 14-pin DIPs. Application is expected to be in linear subsystems which require an operational amplifier's internally compensated, linear input and output characteristics in a circuit area adjacent to the switching speed and logic-compatible output of a comparator.

Circle 362 on Inquiry Card

Quad Op Amps Offer Partitioned Programming

Prototypes of XR 146/246/346 programmable quad operational amplifiers are now available from Exar Integrated Systems, Inc, PO Box 6229, Sunnyvale, CA 94088 as direct replacements for the National LM 146/246/346. Production is scheduled to start in the first quarter of this year.

Four independent high gain, low power amplifiers are internally compensated. Partitioned programming is provided with three op amps programmed by one external bias setting resistor and the remaining one programmed by a second resistor. These two resistors permit the user to program gain bandwidth product, supply current, input bias current, input offset current, input noise, and slew rate. The user therefore can trade off bandwidth for supply current or optimize the noise figure for a given source resistance.

Circle 363 on Inquiry Card

Adjustment-Free DACs Have ±½ LSB Linearity

Completely adjustment-free operation is promised for 8- and 10-bit versions of the DAC337 series of D-A converters. Direct plug-in replacements for MN3000 series DACs, all models are housed in hermetically-sealed 14- or 16-pin DIPs and require only a ±15-V power supply.

Each of the models introduced by Hybrid Systems Corp, Crosby Dr, Bedford, MA 01730 incorporates a precision reference, highly stable, thin-film nichrome resistor network, output amplifier, and switches. Linearity of ±½ LSB is achieved without use of an external zero or gain adjustment. Each version is offered with choice of three output voltage ranges: 0 to 10 (unipolar), and ±5 and ±10 V (bipolar).

Versions processed to "C" option grade for commercial applications operate over the 0 to 70°C range; military grade "B" option versions are processed to meet MIL-STD-883A, Class B and operate over the −55 to 125°C range.

Circle 364 on Inquiry Card

Prices Reduced on 8-Pin DIP Divider Circuits

Prices on RED 5/6 and 50/60 divider circuits have been reduced by LSI Computer Systems, Inc, 1235 Walt Whitman Rd, Melville, NY 11746. The dividers operate with either 50- or 60-Hz signal inputs. They are available in 8-pin mini-DIP configuration. The 5/6 produces one pulse every 0.1 s while the 50/60 produces one pulse per second. Reduced prices vary from $3.75 each in quantities lower than 25 to $1.75 for 1000 to 4999 quantities.

Circle 365 on Inquiry Card

Internal Gain Setting Resistors Improve Amplifier Accuracy

Claimed by the manufacturer to be the first dual inline instrumentation amplifier to incorporate internal gain setting resistors and an optional 2-pole Butterworth filter, the M2200 includes internal laser-trimmed thin film resistors to provide user-selectable gains of 1, 10, 100, and 1000. This is said to provide better accuracy over temperature than conventional designs which require external gain setting resistors. (For applications requiring gains between the standard ones, a single external resistor will provide the proper adjustment.)

Two external capacitors can be used to set the breakpoint of the low-pass Butterworth filter from full bandwidth to below 1 Hz. In many applications this will eliminate the need for an additional filter stage.

Typical input offset voltage at 25°C is ±100 μV, adjustable to 0 with an external trimpot. Input offset voltage drift with temperature is 3 μV/°C at a gain of 1 and less than 0.5 μV/°C at a gain of 1000. Full power bandwidth is 7 kHz, input impedance is 1 GΩ, and input bias current is ±5 nA. Standard operating temperature range is −25 to 85°C but processing to MIL-STD-883 Class B is available. The device is available from Micro Networks Corp, 324 Clark St, Worcester, MA 01606 in an 18-pin, hermetic DIP. □

Circle 366 on Inquiry Card

Looking for reel-to-reel MIL recorder performance but cartridge compactness?

The only way to go — Genisco ECR.

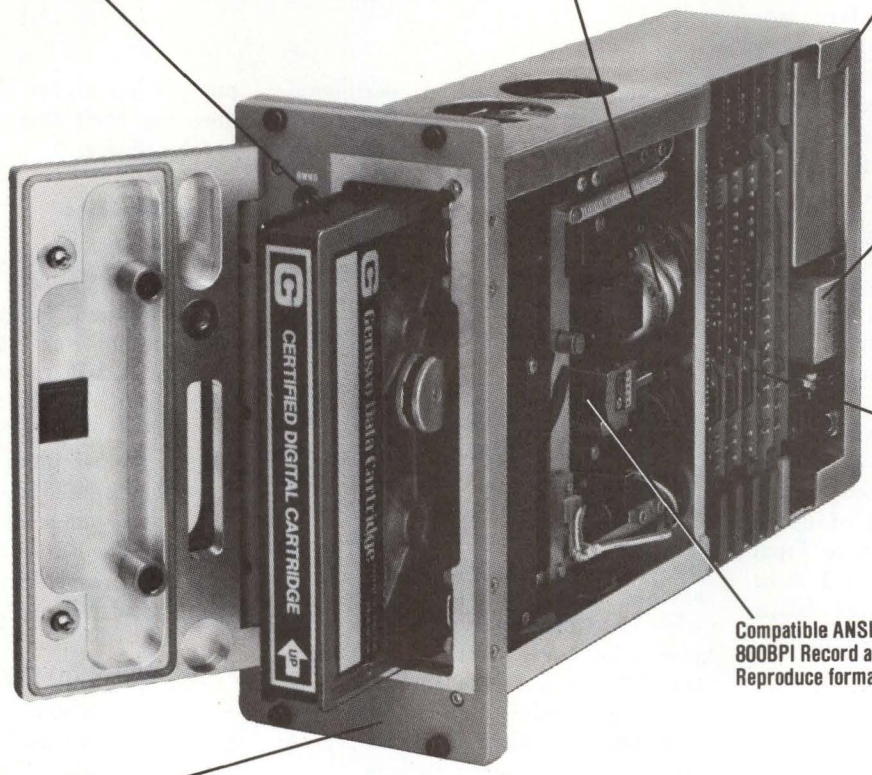
Reel-to-reel performance. Emulating reel-to-reel machines, the Genisco ECR cartridge recorder stores up to 35 megabits and transfers data at a rate of 160K bits/second — at a tape speed of 25 ips.

Compact. Lightweight. You can put eight ECR's in the same space you'd need for a single equivalent performance reel-to-reel unit. And, an ECR weighs just 14 lbs.

Use existing software and controllers. The ECR is compatible with standard ANSI 9-track formatting, so you don't have to make expensive software changes. What's more, your present controllers can be interfaced with only simple modifications.

Proven rugged-environment performance. All this, and the ECR is a prestigious performer, having passed and been qualified to the toughest criteria as set down in MIL-E-5400. Over 200 units already in use in such major programs as the AN/TSQ-73 Missile Minder and the AN/TTC-39 Tri-Tac attest to the ECR's reliable-performance worthiness under critical conditions.

So, since we can only give you a briefing of their benefits, here, contact us for the complete rundown.



Precision Self-Tensioning Cartridge contains 450 feet of 1/2-inch wide tape (stores up to 35 megabits)

Tape Deck is vibration/shock mounted to provide MIL-E-5400 performance.

Meets stringent power requirements (28Vdc) — to MIL-STD-704 specs.

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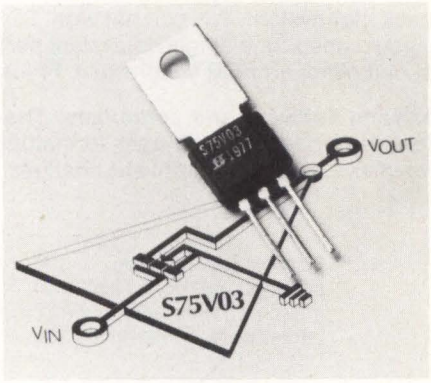
CIRCLE 87 ON INQUIRY CARD

PRODUCT FEATURE

VMOS Power Peripheral Driver Simplifies Low/High Current Interfacing



Vertical metal oxide semiconductor field effect transistor technology, when applied to fabrication of a power peripheral driver, provides the key elements of complementary metal oxide semiconductor and transistor-transistor logic compatibility in addition to several other advantages. These include minimum propagation delays (<10 ns), freedom from failure caused by secondary breakdown and thermal runaway, and no need for standby power (no power supply connection is required). The single semiconductor element is said to satisfy the designer's need for a universal interface device between low current computer logic inputs and high current inductive actuators.

The S75V03 VMOS power peripheral driver is essentially a logic switch with higher current and power handling capability than standard MOS FETs. Because it is a majority carrier device, it is more than an order of magnitude faster than a comparable bipolar device, which is a minority carrier that cannot turn off until its output base region is free of charge.

This VMOS device interfaces directly to CMOS, TTL, DTL, and MOS families. The internal mechanism is basically that of a standard VMOS FET gate controlling the resistance of the channel through which output current is able to flow.

Input current is less than 100 nA and threshold voltage is 0.8 to 2.0 V. A 5-V logic pulse supplied to the input results in an output of up to 600 mA; a 10-V logic pulse input causes the device to conduct 1 A or more. Maintaining the input below 0.8 V permits a 1-mA maximum leakage at a 25-V output.

Applications

In digital circuits this VMOS device can be treated as a logic gate (ie, it will turn on and drive the load whenever the logic operating the driver gate makes a low to high transition). It can serve as a logic output device in microprocessor-based peripheral devices such as terminals; in microprocessor-based process control systems where low logic level inputs must interface to the high currents necessary to drive solenoids, motors, or relays; and in telecommunication systems where logic level inputs drive high current displays or relays.

Unlike bipolar circuits, the VMOS power driver requires no input current limiting, biasing, leakage compensation networks, or switching time speed-up components. In addition, no input resistors, current buffers, or preamplifier stages are needed. Parts savings range from two components when a VMOS driver is used as a replacement for a Darlington bipolar transistor in a simple application, to five or more when used in more commonplace applications—and even more in very complex circuits.

Because the VMOS driver is a voltage controlled device (ie, a drive current is not needed to switch a large amount of current to the load driver or to control the current output), it has higher gain. Driver gain does not limit stage gain as with a bipolar device.

Specifications

Absolute maximum ratings for the S75V03 include 60-V output voltage, 2-A continuous output current, 3-A peak output current, ±30-V input voltage, 12.5-W power dissipation at 25°C, 10°C/W linear derating factor, and −40 to 150°C operating and storage temperatures. Electrical characteristics (at 25°C) include logical "1" input voltage of 2 to 6.5 V typ, logical "0", 1.2 to 0.8 V typ; and logical "1" input current of 0.01 μA typ, logical "0", −0.01 μA.

Price and Delivery

S75V03 VMOS power peripheral drivers will be priced at $0.99 each in 100-up quantities. Samples will be available this month; production quantities will be available in 30 to 60 days. Siliconix inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Tel: (408) 246-8000.

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CIRCLE 88 ON INQUIRY CARD

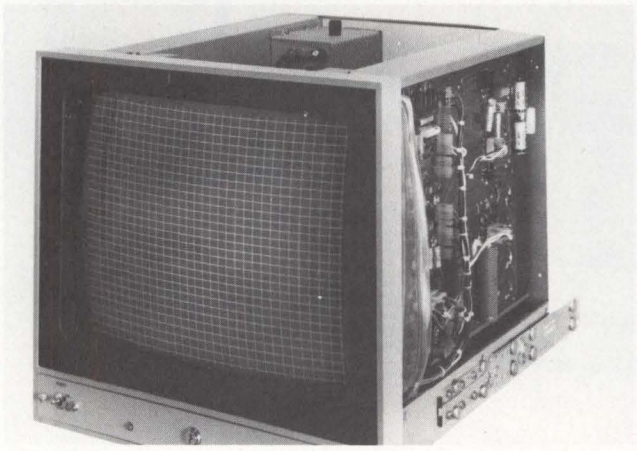
PRODUCTS

Communications Terminal Printer Replacement Operates at Up to 1200-Baud Data Rate

Circle 200 on Inquiry Card

Although it is compatible with the IBM 2741 printer terminal, the model 1641 includes as many as 20 additional features. The desktop keyboard, send and receive, daisy-print mechanism communications terminal features a microprocessor controller. It operates at data rates from 134.5 to 1200 baud, on both half- and full-duplex lines, under IBM Correspondence and P77C/EBCD protocols and the ASCII protocol used in HyTerm terminals. In addition, it can be used in APL terminal applications, communicates via RS-232-C interface, and is compatible with Bell-type 103A, 113A, and 212 modems. Print speed is 45 char/s—three times that of the 2741. An optional Hyplot software package permits high density plotting in increments of 0.0083″ (0.02 cm) horizontally and 0.02″ (0.053 cm) vertically. Users can plot curves, triangles, bar graphs, special symbols, and headers at speeds up to 45 char/s in densities up to 5760 points/in^2 (893/cm^2). Automatic diagnostic and test features such as odd, even, mark, and "none" parity detect as well as self-diagnosis checks are incorporated. **Diablo Systems Inc,** 545 Oakmead Pkwy, Sunnyvale, CA 94086.

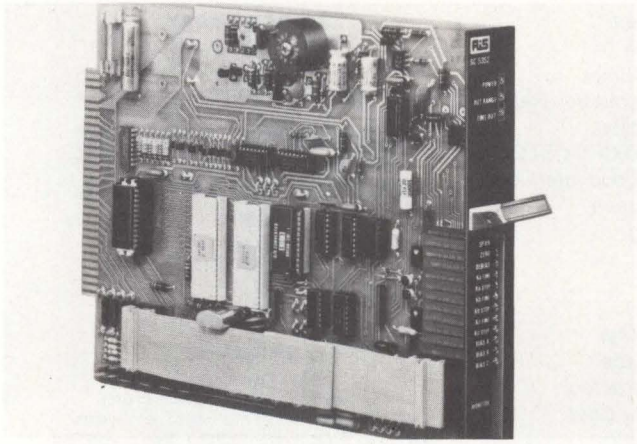
Color CRT Provides High Resolution Display of Computer Graphics



Circle 201 on Inquiry Card

Computer graphics data can be displayed on the model 374 color CRT at a level approaching the CRT's resolution capability. Color-dot triad spacing of only 0.31 mm provides resolution of over 800 lines. The display can operate at horizontal rates up to 34k scans/s, allowing a display of up to 1024 x 512 pixel graphics at a nonflicker, 60-Hz refresh rate; or an ultra high 1024 x 1024 resolution at 30-Hz with 2:1 interlace. Video bandwidth is more than 30 MHz. Separate TTL compatible red, green, and blue inputs are provided. Optional RS-170 and -343 compatible 1-V pk-pk inputs can be provided with keyed black level circuits on each of the three inputs to assure proper color tracking at all brightness settings and at any avg picture level. Analog computing circuits calculate convergence, dynamic blue lateral, pincushion linearity, and dynamic focus waveforms. External effects such as power line changes are compensated for by current feedback dynamic convergence amplifiers. A built-in convergence test pattern as shown on the photo simplifies routine maintenance. **Systems Research Laboratories, Inc,** 2800 Indian Ripple Rd, Dayton, OH 45440.

Interchangeable p/ROMs Enable Field Reassignment of Instrument Functions

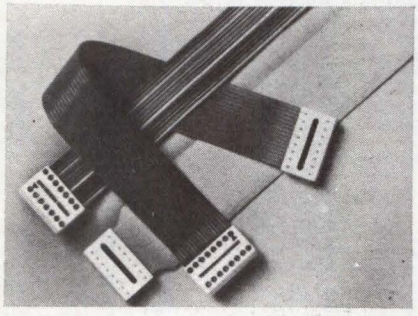


Circle 202 on Inquiry Card

As many as 40 signals can be manipulated from a std 1-slot, 19″ (48-cm) relay-rack mounting chassis when using microprocessor-based, universal module (UNIMOD) instruments. Specific signal assignments are determined by choice of p/ROM and can be changed simply by replacing interchangeable p/ROMs—without further alteration to any module. Whereas conventional instruments are dedicated to discrete functions, the universal module instruments can be assigned to a computational function such as square root extraction, linear integration, addition/subtraction, multiplication/division, tracking/holding, and square root integration by choice of a field-changeable, plug-in, nonvolatile p/ROM that provides the executive routine for manipulating inputs and outputs as well as the instructions for the specific instrument functions. Each module can handle four inputs and outputs and contains 10 separate adjustment potentiometers that can be used as needed. Instrument faceplates and p/ROMs are supplied in kits and are coded to each other by model and function. **Rochester Instrument Systems, Inc,** 255 N Union St, Rochester, NY 14605.

PRODUCTS

DIP JUMPER CABLES



Used for jumpering within a PC board; interconnecting between PC boards, backplanes, and mother boards; and interfacing I/O signals, DIP Jumpers are available in 14-, 16-, 24-, and 40-pin single- or double-ended assemblies. Jumpers, in std lengths of 6, 12, 24, and 36" (15.2, 30.5, 60.9, and 91.4 cm), mate with std IC sockets and feature molded-on strain relief. Contacts are noncorrosive copper alloy 770 spring temper, and insulator is white polyester thermoplastic. **AP Products Inc,** Box 110, 72 Corwin Dr, Painesville, OH 44077.
Circle 203 on Inquiry Card

CORE MEMORY SYSTEM

Meeting environmental and operational requirements of aerospace, shipboard, and severe industrial applications, SEMS-16 is a compact core memory system with 32k x 18 capacity. High performance and reliability are achieved by using a 13-mil low drive wide temperature range core, and by minimizing overall memory power. Operating speeds include access time of 350 ns and cycle time of 900 ns. **Electronic Memories & Magnetics Corp, Severe Environmental Products Div,** 20630 Plummer St, Chatsworth, CA 91311.
Circle 204 on Inquiry Card

PDP-11 ADD-ON PARITY MEMORY

Providing 32k to 128k words of add-on memory for DEC PDP-11 computers having a UNIBUS structure, ARM-1100P expands memory from any 8k boundary in 32k increments to the max of 128k words. It uses only one CPU slot and requires one UNIBUS load. Each unit is supplied complete with wired card rack, power supply, interface, parity control, cooling fans, and interconnecting cables. Access time is 375 ns and full cycle time is 700 ns. **Ampex Corp,** 200 W Nash St, El Segundo, CA 90245.
Circle 205 on Inquiry Card

COMMUNICATIONS BUFFER

CB-1 is a baud rate converter installed between computer terminals and modems conforming to EIA RS-232-C, asynchronous bit serial data transfer, to make them compatible in speed of input or output. With a conversion range of 10 to 960 char/s, buffer is capable of storing 2048 char. Unit equipment includes an overflow alarm and indicator light. Unit measures 16 x 16 x 5.5" (40.6 x 40.6 x 13.9 cm). **Triformation Systems, Inc,** 3132 SE Jay St, Stuart, FL 33494.
Circle 206 on Inquiry Card

CUSTOM OPTICAL READ HEADS

Due to hybrid technology allowing miniaturization of signal conditioning circuitry, complete multichannel custom heads with integrated electronics and logic compatible outputs are now offered. Custom head features a patented arrangement utilizing a microminiature GaAs emitter and Si detector as one integral package. Target may be as close as desired to the sensor, with field of vision at ±5 deg and no focal point or "blind spot" as with conventional configurations. **Ultra Sensors Inc,** 3415 48th Ave N, Minneapolis, MN 55429.
Circle 207 on Inquiry Card

INTEGRATED COMPUTER SYSTEMS, INC.

MICROPROCESSO

LOS ANGELES	HOUSTON	DETROIT	DENVER	BOSTON
January 16-20	January 23-27	February 6-10	February 13-17	March 6-

Similar courses being offered in EUROPE. Write or Call:
Integrated Computer Systems Publishing Co., Inc.
Boulevard Louis Schmidt 84, Bte 6
1040 Brussels, Belgium
Telephone: (02) 735 60 03 Telex: 62473

3 or 4 Day Enginee

2 Day Project Management Series

COURSE 111: One Day–MONDAY

Microprocessor Project Management

From design through manufacture, QA and field service

MICROPROCESSORS: HOW CAN YOU GO WRONG???
WHAT ABOUT . . . ?

Underestimating software costs and time?
Inadequate software documentation?
Selecting the wrong microprocessor?
Software development equipment($14000!)?
Manufacturing problems? Hardware/software testing? Reliability? Obsolescence? . . .

A microprocessor project is different from anything you've managed before. This one efficient day of organized, expert guidance will save you literally months of wasted time, re-invented wheels, and costly oversights.

This unique course synthesizes the experience of hundreds of project managers (who learned the hard way) into a practical field-proven methodology for managing all phases of a microprocessor application. The course emphasizes high-risk, high-cost and time-critical problems unique to microprocessors. Concrete real-world case studies illustrate the methods presented, and these step-by-step methods can be immediately applied to your own project.

This course will benefit every manager and engineer concerned with microprocessors. Teams from engineering, manufacturing, QA, and field service are encouraged to attend (team discounts available).

KEY TOPICS

1. **Fundamental concepts, definitions and jargon.**
2. **Avoiding pitfalls and "technical tunnel-vision."**
3. **Planning and specifying the project – the PERT/flowchart.**
4. **How to select personnel and evaluate performance.**
5. **How to select the right microprocessor – what's really important?**
6. **Software development and test equipment – what's really needed?**
7. **How to estimate overall project costs and schedule.**
8. **How to manage software design and development.**
9. **Software documentation – a practical methodology.**
10. **Verifying that the software works.**
11. **Manufacturing, testing and QA – both software and hardware.**
12. **Component & product reliability – planning μP field service.**
13. **How to prepare for the future today . . . and avoid obsolescence tomorrow.**

SPECIAL LATE-AFTERNOON WORKSHOP

A unique opportunity to discuss your application-oriented problems in a productive shirtsleeves atmosphere. Immediately after Course 111 from 4:30 until 6:00pm with snacks and refreshments.

COURSE 102s: One Day–TUESDAY

Microprocessors and Microcomputers:

A Comprehensive Technical Introduction and Survey

This course provides a comprehensive unbiased introduction to microcomputer hardware/software development and integration. The course emphasizes the factors affecting key design and development decisions including: processor selection, I/O and software design, software implementation steps, development and test equipment, and most important pitfalls to be avoided when getting started. Throughout the course, applications examples provide concrete illustrations of concepts presented and are drawn from the following application areas: military, communications, consumer, instrumentation, industrial control, and biomedical systems.

This course is *vital* (1) to all engineers and managers who want a quick, unbiased, cost-effective introduction to microprocessors (2) to those engineers attending this as the first day of the "Engineering Design" series (Course 102s, 125A and 136) and (3) to managers attending this course as the second day of "Project Management" series (Course 111 and 102s).

COURSE OUTLINE

1. **INTRODUCTION**
   • What is a microprocessor (μp)? a microcomputer (μc)? • Identifying suitable and unsuitable applications
2. **FUNDAMENTAL MICROCOMPUTER CONCEPTS**
   • Terminology • Software (SW) – how it works; how it's developed • Hardware (HW) – Basic μc configurations • The μc design cycle
3. **THE HARDWARE**
   • μp architectures (4, 8, 16-Bit and slices) • Memory systems design – ROM, PROM, RAM, CORE • Input/output organization (programmable I/O, interrupts, DMA) • Build or buy?
4. **INTERFACING TO THE EXTERNAL WORLD**
   • I/O port design • Programmable LSI I/O chips • Interfacing to: analog devices, keyboards, displays, cassettes, etc.
5. **SOFTWARE DESIGN & IMPLEMENTATION**
   • Four implementation methods • Editors, assemblers, compilers • Assembly vs. high level languages (FORTRAN, BASIC, PL/M)
6. **INTEGRATING AND TESTING THE HW AND SW**
   • What really useful tools are available? • What tools should you build yourself? • Isolating and fixing HW and SW bugs
7. **TECHNICAL SURVEY OF μP'S AND μC'S**
   • Intel, Fairchild, Motorola, National, Rockwell, Signetics, Texas Instruments, Zilog, and others including the new LSI minicomputers • Board-level μc systems – PROLOG, PCS, CONTROL LOGIC, WARNER/SWASEY, and others • A systematic, application-oriented approach to selecting the right microprocessor family.
8. **UTILIZING DEVELOPMENT AND TEST EQUIPMENT**
   • Logic analyzers • SW simulators • Specialized μc debugging equipment • μc development systems • Peripherals to buy
9. **HOW TO GET STARTED**
   • What equipment to buy first • Pitfalls to avoid • Good information sources

EDUCATION

SAN DIEGO
March 13-17

OTTAWA, CANADA
April 3-7

Design Series

COURSE 125A: Two Days – WEDNESDAY & THURSDAY

Hands-On Microcomputer Programming Workshop (for the beginner)

LEARN-BY-DOING
EACH STUDENT
RECEIVES A
COMPLETE 8080
MICROCOMPUTER
SYSTEM FOR HIS
PERSONAL USE
THROUGHOUT
THE COURSE.

This highly efficient, intensive short-course combines expert teachers and detailed course materials with the unique opportunity to learn by *immediately* implementing on *your personal microcomputer* each new programming concept as it is developed by the instructor.

COURSE OUTLINE [with exercises in brackets]

1. **INTRODUCTION TO THE ICS 8080 μC TRAINING SYSTEM**
   • Hardware configuration • How to use the keyboard/display and built-in commands • [Loading and executing a simple program]
2. **SOFTWARE FUNDAMENTALS AND BASIC TECHNIQUES**
   • CPU Register Instructions [Counting] • Memory Instructions [Storing & Retrieving Data] • Basic I/O [Controlling LED segments] • Jumps and Loops [Time delay program] • Bit Testing [Binary Decoding] • Subroutines & Stacks [Keyboard Input]
3. **ADVANCED PROGRAMMING TECHNIQUES**
   • Arithmetic [A multi-precision calculator] • Data Organization [Table Look-up] • Block I/O Transfers [Real-Time I/O] • Controller Programs [Traffic Control]
4. **PROGRAM DESIGN METHODOLOGY**
   • Systems analysis • Specifying the program • Design approaches (top-down, structured programming, modular design)

OPTIONS: KEEP THE MICROCOMPUTER SYSTEM

Course 125B: Includes 125A PLUS a microcomputer & an additional 650-page Self-Study Text to take home.
Course 125C: Includes 125A PLUS microcomputer to take home.

NEW! NEW! NEW!

COURSE 136: One Day – FRIDAY

Hands-On Interfacing Workshop

(Limited to current or former attendees of Course 125.)

Utilizing the ICS training microcomputers and additional Interfacing hardware, students will learn both software and hardware for interfacing to the real-world.

In-Class Projects include:
1. Real-Time Interrupt programming (w/Intel 8253 timer)
2. A/D Conversion – A Digital Thermometer
3. DC Motor Control (Open and closed loop)
4. Other (student-option) Interfacing projects

COURSE ENROLLMENT FORM

COURSE HOURS:
Registration: 8:15am
Course Lecture: 9:00am–4:30pm
Special Events: 4:30–6:00pm

In addition to the extensive hands-on exercises of Course 125A and 136, informal microcomputer hardware activities are organized at every course for valuable hands-on experience.

COURSE FEE:
Management Series: (2 days: 111 + 102s)–**$390**
3-day Design Series: (102s + 125A)–**$495***
4-day Design Series: (102s + 125A + 136)–**$595***
Complete Series: (111 + 102s + 125A + 136)–**$695***
Individual Courses: 111 or 102s or 136 –**$195**; 125A–**$395***
*Option 125B–add **$445**; Option 125C–add **$350**

Course Fee Includes: lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.
Team/Group Discounts: 10% reduction for three or more participants from the same organization, if invoiced at the same time.

TO ENROLL:
Please fill out, detach and return coupon. A confirmation with complete course details will be forwarded to you.

MAIL TO: **Integrated Computer Systems, Inc.**
3304 Pico Blvd., Second Floor
Santa Monica, California 90405

For immediate confirmation, CALL: **(213) 450-2060**

☐ PLEASE ENROLL ME in the following courses:

	2 Day Project Management Series		3 or 4 Day Engineering Design Series	
COURSE	111	102s	125A	136
LOS ANGELES	☐ Jan 16	☐ Jan 17	☐ Jan 18-19	☐ Jan 20
HOUSTON	☐ Jan 23	☐ Jan 24	☐ Jan 25-26	☐ Jan 27
DETROIT	☐ Feb 6	☐ Feb 7	☐ Feb 8-9	☐ Feb 10
DENVER	☐ Feb 13	☐ Feb 14	☐ Feb 15-16	☐ Feb 17
BOSTON	☐ March 6	☐ March 7	☐ March 8-9	☐ March 10
SAN DIEGO	☐ March 13	☐ March 14	☐ March 15-16	☐ March 17
OTTAWA, CANADA	☐ April 3	☐ April 4	☐ April 5-6	☐ April 7

NAME _____

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STATE _____ ZIP CODE _____

TELEPHONE (___) _____ Ext _____

PAYMENT: Please indicate method of payment.
☐ Check/M.O. enclosed ☐ P.O. included ☐ Please invoice me

☐ Please put me on your mailing list to receive future Course Schedules.

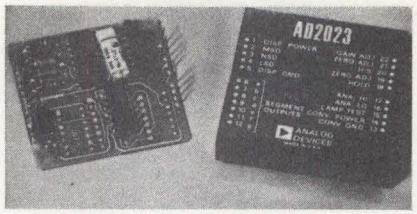
☐ Please send information on ICS Self-Study Courses.

☐ Please contact me with regard to On-Site Courses.

CIRCLE 90 ON INQUIRY CARD

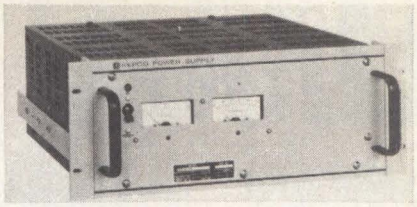
PRODUCTS

3-DIGIT DPM MODULE



Offering an alternative to designing with component ICs or buying a complete DPM with readouts, the AD2023 2 x 2 x 0.4" (5 x 5 x 1-cm) module has all electronics necessary to construct a 3-digit panel meter with designer's choice of external displays. Both 7-segment and BCD output versions use an IIL LSI IC. Requiring a single 5-V supply, units accept input voltages between −99 and 999 mV, with automatic polarity indication. Power requirements are 0.1 W at 5 V. **Analog Devices, Inc, Instruments and Systems Group,** Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062.
Circle 208 on Inquiry Card

KILOWATT POWER SUPPLY

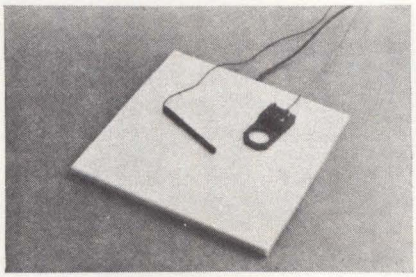


The series PRR kilowatt power supply achieves 70 to 80% efficiency without employing high frequency switching. Four dc outputs offer 12 V at 77 A, 24 V at 42 A, 38 V at 36 A, and 48 V at 22 A. A ferroresonant stabilization technique is used to stabilize voltage; reliability results from the small parts count. Features include automatic current limiting, brownout protection, isolation, built-in blower, and recessed metering. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352.
Circle 209 on Inquiry Card

AC PLASMA PANEL TERMINALS

A family of commercial, militarized, and ruggedized intelligent Plasmascope® display terminals are available with optional programmable microprocessor and up to 64k bits of RAM for local editing and data processing. An ac plasma panel, acting as the display medium, uses a gas discharge principle to produce an array of luminescent, 10-mil (0.025-cm) spots which are individually energized and addressed. Panels have a viewable area of 7.2 x 2.4 and 8.6 x 8.6 in (18.3 x 6 and 21.8 x 21.8 cm) with up to 420 and 5120 char, respectively. **SAI Technology Co,** 4060 Sorrento Valley Blvd, San Diego, CA 92121.
Circle 210 on Inquiry Card

HIGH RESOLUTION DIGITIZING TABLET



For use in conjunction with a cursor and electronic controller, tablet converts graphic data into digital format for computer processing. Graphic data input function similar to a keyboard function for alphanumeric data input is provided. As an alternative to light pens and joysticks, digitizer is characterized by a 0.001" (0.00254 cm) resolution and offscreen hardcopy input capability. **GTCO Corp,** 1055 First St, Rockville, MD 20850.
Circle 211 on Inquiry Card

REMOTE COMMUNICATIONS PRINTER

Available in speeds from 125 to 300 lines/min, printers employ a microprocessor-based communications controller that acts as the interface to communications lines supporting Honeywell VIP 7700; IBM 2780, 3780, 3270, and PARS 2946; and Xerox SDS 7670 protocols. Controller operates with any RS-232-C compatible data set in multi-drop or switched line applications, and offers buffer sizes of 1024 and 2048 char, auto-answer, reverse channel, synchronous or asynchronous operation, and automatic sign-on. **Data 100 Corp,** 6110 Blue Circle Dr, Minneapolis, MN 55435.

Circle 212 on Inquiry Card

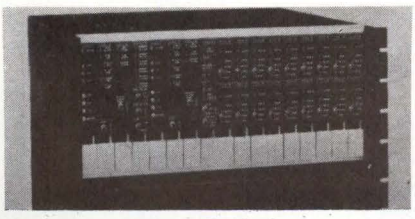
DATA BUFFER

This solid-state digital storage unit consists of a 2048-char memory for a variety of store and forward applications. Operating features of the 4.5-lb (2-kg) model 300 data buffer include RS-232 plug compatibility, switch selectable baud rates of 110 and 300, on/offline capability, and manual or remote control. Interfaces may be to any ASCII datalogger, terminal, programmable calculator, or minicomputer. **Techtran Industries, Inc,** 200 Commerce Dr, Rochester, NY 14623.

Circle 213 on Inquiry Card

INTELLIGENT TIME DIVISION MULTIPLEXER

Timeline 780 SUPERMUX, affecting users of 3270, 2780, 3780, and 360/20 RJE HASP binary synchronous terminals, accepts dial-up, dedicated, synchronous, and asynchronous inputs. Under microprocessor control, device uses statistical techniques to transmit active data inputs, conserving bandwidth to allow for a throughput double or better that of conventional multiplexers. Bisync transmission code may be EBCDIC or ASCII, with or without transparency. **Infotron Systems Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.



Circle 214 on Inquiry Card

PRODUCTS

GRAPHIC DISPLAY UNIT

Integrating hardware and software for interactive process monitoring and control, the 3977 graphic display unit enables curves, graphics, and texts to be displayed simultaneously in eight colors on up to four freely addressable monitors. The minicomputer based controller permits interactive communication with a double computer system and features a rolling map system with joystick, virtual keyboard with light pen, loadable symbol repertoire, switch-selectable symbol format, and connection facilities for hardcopy devices. Screen formats are 24, 32, or 48 lines with 80 col, and 32 lines with 64 col. **Siemens AG,** Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany.

Circle 215 on Inquiry Card

MODEM EMULATOR

Permitting direct connection between terminals and computers located within 100 ft (30 m) of each other, thereby replacing two modems usually hooked up in a back-to-back mode, unit runs asynchronously at speeds up to 40k bits/s, or synchronously at 2400, 3600, 4800, 7200, 9600, 14,400, or 19,200 bits/s. Speed selection, on both stand-alone and rackmount configurations, is made by switches on the circuit card. **Astrocom Corp,** 15012 Minnetonka Industrial Rd, Minnetonka, MN 55343.

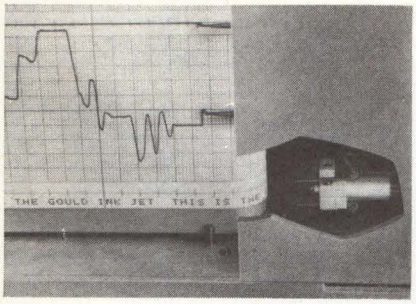
Circle 216 on Inquiry Card

PROTOTYPE BOARDS

Multipurpose Before Boards™ for hobbyists have solder plated through holes, are suitable for analog or digital circuits, and can be handwired or wire-wrapped. The S-100 compatible board is supplied with a 50-pin dual edge connector and can accommodate either 50 or 56 IC packages; the S-100x board is similar but does not have the 50-pin gold-plated connector or regulated power supply circuit. The 6800 bus compatible board is designed to be used with 50-pin Molex type connectors; the identical 6800x version does not contain the power supply circuit. **Multi-Tek, Inc,** PO Box 201, Union Sq, Milford, NH 03055.

Circle 217 on Inquiry Card

INK JET RECORDER ANNOTATION DEVICE



Available as a factory installed option on the company's 2000 series and model 200 recorders, device prints ASCII alphanumeric char in a 5 x 7 matrix along edge of moving chart paper at all speeds. Annotations up to 256 char long may be entered on optional keyboard or obtained from external source. Device permits recorder to be used on an exception basis; printing and recording can be operator, event, or computer-initiated. **Gould Inc, Instrument Systems Div,** 3631 Perkins Ave, Cleveland, OH 44114.
Circle 218 on Inquiry Card

2-POLE AC SYNCHRONOUS MOTORS

Offering synchronous speeds of 3600 rpm for 60 Hz and 3000 rpm for 50 Hz, motors are also available with gear heads for lower speed applications. Series M features a pull-out torque up to 7 oz-in (0.05 N•m) max, and employs a special rotor design in field-proven shaded pole motor. Electrical specs include std 120 V, 60 Hz, and a range of 12 to 240 V, 50 or 60 Hz. **Brevel Motors, a McGraw-Edison Co Div,** 203 Broad St, Carlstadt, NJ 07072.
Circle 219 on Inquiry Card

FRICTION-FEED MATRIX TELEPRINTER

Send-receive terminal version of the 30-char/s model 43 matrix teleprinter prints 10 char/in on a 72- or 80-char line and provides original and one copy using std roll paper. Basic features include upper/lower case printing, 10- or 30-char/s operation, half- or full-duplex mode, built-in test capabilities, and modular design. Interfaces include std EIA RS-232, TTL, or integrated 103-type data set. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60076.
Circle 220 on Inquiry Card

PRODUCTS

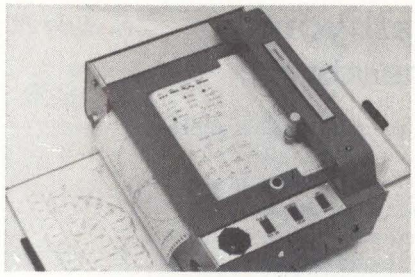
COM SCANNER

Consisting of a rotating drum system that produces output on 9-track, 800-bit/in (315/cm) mag tape in a format suitable for use with graphic COM systems, the Pagitron/COM scanner directly converts engineering drawings without retracing with bolder lines. Because all graphics are converted to digital form, the artwork can become part of a computer data base, capable of being revised and manipulated. Format enables single drawings up to 17 x 22″ (43 x 56 cm) to be scanned in one pass for greater resolution; larger sizes are available. **Optronics International, Inc,** 7 Stuart Rd, Chelmsford, MA 01824.
Circle 221 on Inquiry Card

SYNCHRO/RESOLVER TO DIGITAL CONVERTERS

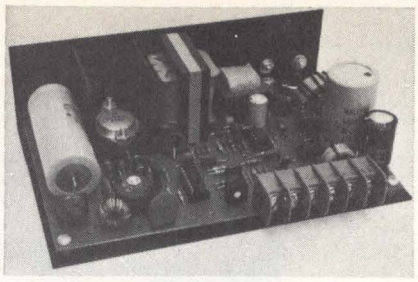
Available in either module or single PC board configurations, the VSDH 400/600 series of solid-state tracking converters accepts either 3-wire synchro or 4-wire resolver inputs of 11.8 or 90 V at 380 to 1200 Hz, or 90 V at 50 to 440 Hz. Specs include 14-bit parallel binary DTL or TTL compatible outputs to an accuracy of ±4 min of arc or ±1.0 LSB. CMOS outputs are available. Reference and synchro inputs are transformer isolated to eliminate loading errors. **Vernitron Corp, Vernitech Div,** 300 Marcus Blvd, Deer Park, NY 11729.
Circle 222 on Inquiry Card

DIGITAL PLOTTER



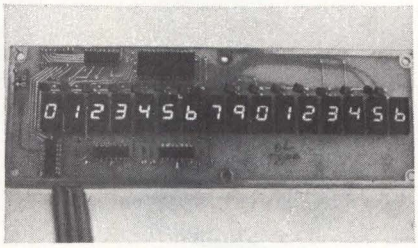
The Microdrive™ technique is used in the DP-11 digital plotter to achieve stop/start plotting rates of up to 4000 increments/s. This method for driving the stepper motors in the plotter allows the step size of the plotter to be altered by a simple electronic change. Audible noise generated by the plotter is also reduced. The device is compatible with most minicomputer plotter interfaces in addition to many of the company's controllers. **Houston Instrument, div of Bausch & Lomb,** One Houston Sq, Austin, TX 78753.
Circle 223 on Inquiry Card

SWITCHING POWER SUPPLIES



Linear replacement open frame regulated supplies include 75-W 1-, 3-, and 4-output units. LR7500, -7700, and -7800 lines offer outputs of 5 V at 15 A, 12 V at 6.5 A, or 15 V at 5 A; a 7500 main supply and two auxiliaries of 5, 12, and 15 V at up to 15 W each; and an additional fourth auxiliary, respectively. Units protect against transient loss of input voltage and brownout conditions down to 92 Vac. Heat dissipation is one-third that of a series regulated supply; efficiency is 70% on multiple-output models. **California DC,** 2348 Towngate Rd, Westlake Village, CA 91361.
Circle 224 on Inquiry Card

16-DIGIT PROCESSOR PANEL DISPLAY



DMO-16 provides 16, 0.3″ (0.76-cm) LED 7-segment numeric display char and drive electronics for easy interfacing to an 8-bit TTL processor output port. Software scanning accomplishes multiplexing; for systems using hardware multiplexing, a 16 x 4 RAM is provided. Display may be cut to length from 8 to 16 digits, has a DIP socket for all I/O connections, and requires 5 V, 350 mA max. **Telesis Laboratory,** Chillicothe, OH 45601.
Circle 225 on Inquiry Card

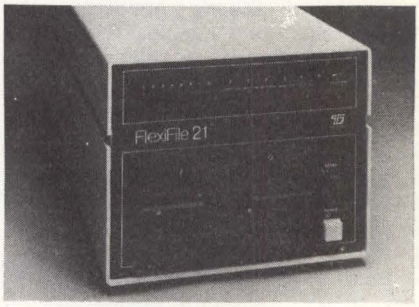
BRUSHLESS DC MOTOR

BM-3201, developed specifically for use in computer peripherals, is a brushless dc motor with samarium cobalt magnets. Motor retains linear speed-torque characteristics of a true dc servomotor. Transient and short-circuit protection is inherent in magnets which, because they cannot be demagnetized, are well suited for dynamic braking. Magnets offer superior magnetic and electrical characteristics and minimize weight and size. **Inland Motor Div, Kollmorgen Corp,** Radford, VA 24141.
Circle 226 on Inquiry Card

AC-DC POWER SUPPLIES

Series EPM ac-dc power supplies are available in eight dual-output models delivering outputs of ±12 or ±15 Vdc at 60, 100, 200, or 300 mA. Std output tolerance is ±2%, and regulation for line and load is 0.02% max. Supplies incorporate stable references and high gain, low phase shift, broadband regulator circuits. Series pass elements are selected for worst case conditions of line, load, and amb temp. All thermal factors are closely controlled. **Intronics, Inc,** 57 Chapel St, Newton, MA 02158.
Circle 227 on Inquiry Card

FLEXIBLE DISC SYSTEM



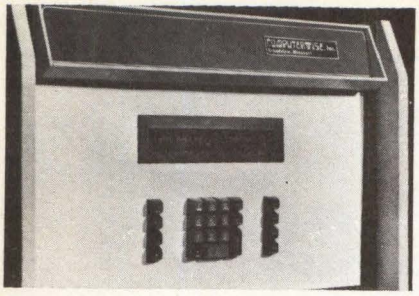
FlexiFile 21, a microprocessor-controlled flexible mini-disc system for data processing and communications applications, is fully user programmable and controlled via its front panel. Eight indicator lamps and six mode select switches enhance capabilities. Utilizing a Shugart mini-floppy drive, the unit contains an Intel 8080 microprocessor, built-in controller, RS-232 and/or current-loop interface, 8-bit parallel bus interface, electronics, and power supply. **Tri-Data,** 800 Maude Ave, Mountain View, CA 94043.
Circle 228 on Inquiry Card

12-BIT MULTIPLYING DAC

Hermetically sealed in a std, 18-pin DIP, series 7521M offers 12-bit accuracy and resolution over the full −55 to 125°C temp range. Performance competitive and pin-for-pin compatible with Analog Devices' 12-bit AD-7521, which is limited to 10-bit accuracy, the device is compatible with TTL and CMOS logic. The converters operate from 5- to 15-V power supplies and consume only 20 mW of power. ±¼ LSB linearity is guaranteed over the specified temp range. **Beckman Instruments Inc,** 2500 Harbor Blvd, Box 3100, Fullerton, CA 92634.

Circle 229 on Inquiry Card

RACK-MOUNTABLE KEYBOARD/DISPLAY UNIT



Unit, attachable to any computer or microprocessor using an asynchronous RS-232 or 20-mA current loop I/O port, mounts in a std 19″ (48-cm) side equipment rack and requires 10.5″ (26.7 cm) panel height. 110- to 9600-baud rate, full- or half-duplex, even, odd, or no parity, 5 or 8 data bits, and 1 or 2 stop bits are switch-selectable. Gas discharge display provides a single line of up to 32 alphanumeric char. **Computerwise, Inc,** 4006 E 137th Terrace, Grandview, MO 64030.
Circle 230 on Inquiry Card

RASTER-SCAN VIDEO IMAGING SYSTEM

A full refresh raster-scan video imaging system, which stands alone or interfaces with most minicomputers, features a dedicated minicomputer and bipolar microprocessor to provide a wide intensity spectrum and high resolution display. Programmable on both processor levels, the system 6400 video image processor stores 5.24M bits of data and can be expanded. Color, gray scale, and b/w processing are available. Resolution is up to 1280 x 1024 pixels. Alphanumerics may be superimposed over image display. **Lexidata Corp,** 215 Middlesex Tpk, Burlington, MA 01803.
Circle 231 on Inquiry Card

TELEPRINTER WITH CASSETTE BUFFER

EDT 1232 teleprinter, equipped with a magnetic tape cassette buffer, offers print quality, heavy-duty use, 120-char/s throughput, 132 print positions, and both front and rear loading of paper. With a storage capacity in excess of 50,000 char, cassette buffer writes, reads, rewinds, and edits under remote computer or local control. Forward-skip and back-skip controls facilitate high speed data search, and backspacing permits error correction. **Western Union Data Services,** 70 McKee Dr, Mahwah, NJ 07430.
Circle 232 on Inquiry Card

COMPUTER-CONTROLLED WIRING ANALYZER

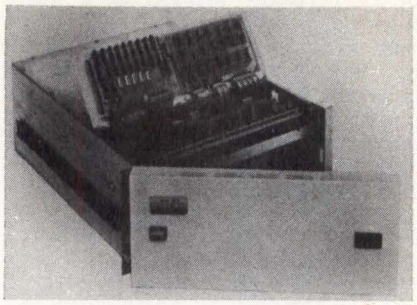
OmniTester 2000A, a series of computer-controlled wiring analyzers, tests complex cables, harnesses, and wired or multilayer backplanes. Operator interface to the microprocessor-controlled system occurs through a CRT terminal. Configuration with several customer-selected I/O peripherals is possible. Features include automatic self-programming, user's product nomenclature printout, and "test from memory" capability. **Automatic Production Systems, Inc,** 351 New Albany Rd, Moorestown, NJ 08057.
Circle 233 on Inquiry Card

COOLING FANS

Designed to cool heat-generating elements in electronic data processing equipment and business machines, two tubeaxial fans, which are 1.5″ (3.8 cm) deep, fit std rack hardware and may be mounted from either face. Model TA300 offers an air flow rate of 27 ft^3 (0.764 m^3)/min at a static pressure of 0.10 in of water (0.254 g/cm^2) and input power of <9W at 60 Hz. By reducing rotational speed to about 2000 r/min, the overall sound power level of the model TA300S is decreased approx 7 dB. **Torin Corp,** Torrington, CT 06829.
Circle 234 on Inquiry Card

PRODUCTS

HEAD-PER-TRACK DISC MEMORY SYSTEM



Patented, automatic recording-head lifter in model 80 series disc memories literally locks up the heads when equipment is not operating, substantially increasing equipment reliability by allowing it to survive the critical phases of transportation, installation, and handling without damage. Ability to withstand shock during operation is assured by high pressure air bearings for the recording heads which are sealed in an environment proof, shock-mounted disc/head chamber. **Alpha Data Inc,** 20750 Marilla St, Chatsworth, CA 91311.
Circle 235 on Inquiry Card

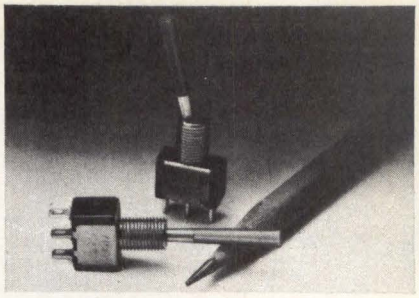
INTERACTIVE TERMINAL FOR DATA LINKS

PIX-II VDU-77, an IBM 3277 equivalent, communicates with IBM 360/370 host mainframes on attention interrupt basis without requiring polling messages. It is designed for use in small clustered applications with PIX-II virtual data links. Systems consist of minicomputer-based local and remote control units that extend mainframe multiplexer channels to allow remote peripheral devices to operate as if they were local. Terminal features a 12″ (30.5-cm) nonglare screen. **Paradyne Corp,** 8550 Ulmerton Rd, Largo, FL 33541.
Circle 236 on Inquiry Card

SMALL BUSINESS COMPUTER SYSTEM MODULES

For disc-oriented systems using high level, modified BASIC programming language, series 1000 includes CPU with front panel switches, real-time clock, 64k bytes of addressable memory, disc controller, line printer controller, and 4-channel multiplexer. Series 2000 includes the same CPU, a storage module controller capable of handling up to two or four drives, and a full 8-channel multiplexer with TTY channel. Two printers can be controlled. **Bytronix Corp,** 2751 E Chapman Ave, Fullerton, CA 92631.
Circle 237 on Inquiry Card

LONG HANDLE SUBMINIATURE TOGGLE SWITCH

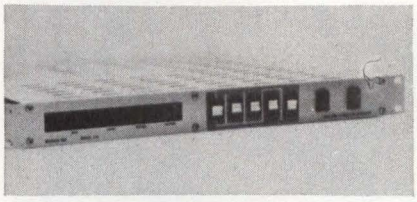


To eliminate electrostatic discharge between operator and switch handle, the model L3 subminiature toggle switch uses plastic (nylon) handles. Available in a choice of nine colors, the units come in spdt, dpdt, 3pdt, and 4pdt configurations. Insulation strength is 1000 MΩ min and dielectric strength is 1000 V rms at sea level. Overall toggle length is 21.34 mm, with plastic portion measuring 16.38 mm; toggle diam is 3.280 mm. **C&K Components, Inc,** 103 Morse St, Watertown, MA 02172.
Circle 238 on Inquiry Card

12-BIT CURRENT-LOOP DAC

The modular MP1480 12-bit current-loop DAC with built-in storage register acts as a digitally controlled current valve for std 4- to 20-mA or other customer-selectable current ranges, or as a voltage output DAC. Specifically designed for application in industrial process control systems, it satisfies ISA Std S50.1 for 4-wire transmitters. Conversion accuracy is within ±0.012% FSR, settling time is within ±½ LSB in <10 μs for a full-scale input, and slew rate is 2 mA/μs. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 239 on Inquiry Card

MODULAR TIMING SYSTEM

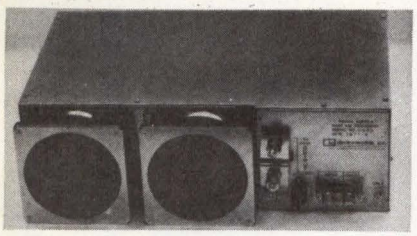


Model 175 timing instruments feature std modular function circuits that permit over 900 timing unit configurations. Complete 1.75″ (4.4-cm) high units include one or more functions providing time code generation and translation, parallel BCD, slow codes, pulse rates, and days display. With any device containing a generator or translator function, the user has a choice of std time codes. Selectable internal/external clock and high intensity 0.6″ (1.5-cm) LED display are std features. **Moxon, Inc, Timing Div,** 2222 Michelson Dr, Irvine, CA 92715.
Circle 240 on Inquiry Card

CACHE BUFFER FOR PDP-11 SERIES

Using bipolar technology, model 920/981 buffer provides 2048 bytes of memory on two PC cards, forming a single plug-in module measuring 8.25 x 5.2 x 2″ (20.96 x 13.2 x 5.1 cm). In PDP-11/35 and /40 computers, cache buffer replaces the M981 UNIBUS terminator module; whereas in PDP-11/34 and other -11 series processors, M920 UNIBUS jumper module is replaced. Although performance is software dependent, average processor throughput increase of 22% is achieved. Model 920/981 buffers entire CPU main memory. **Fabri-Tek Inc,** 5901 South County Rd 18, Minneapolis, MN 55436.
Circle 241 on Inquiry Card

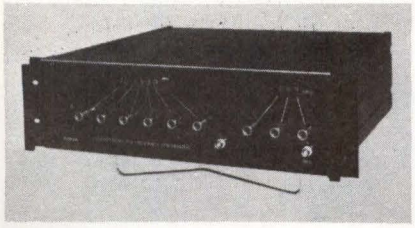
SWITCHING POWER SUPPLY



PEX 058-00 provides high current capacity in the low voltage ranges. Key specs include single adjustable output, 4.75 to 5.25 V; input voltage, 115/230 Vac single-phase; and output ripple and noise (max), 2% pk-pk, 0.5 rms. Transient response time is 0.5 ms. Unit is current limit and overvoltage protected and operates over the 0 to 60°C temp range. Packaged in steel cases, the supplies are virtually immune to accidental rough handling. **Electro-Module, Inc,** 2855 Metropolitan Pl, Pomona, CA 91767.
Circle 242 on Inquiry Card

FREQUENCY SYNTHESIZER INTERFACE BUS OPTION

An IEEE-488 interface bus option (option 003) is available for the model 1013 LED display frequency synthesizer. The unit covers the 0.1-Hz to 13-MHz frequency range with 5-digit resolution. It features leveled output up to 3 V rms with optional amplitude programming in 0.1-dB steps, a square wave output to drive 50 Ω, and TTL. Display indicates frequency and permits operator to monitor output during remote operation. **Comstron Corp,** 200 E Sunrise Hwy, Freeport, NY 11520.



Circle 243 on Inquiry Card

HANDHELD SCANNER

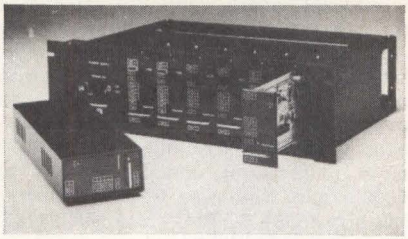
Model 4600 consists of scanning pen connected to decoding/logic unit by a coil cord. Decoding unit uses a microprocessor chip and a buffer memory for 256 8-bit words which permits multidrop data line use. The unit reads a variety of code patterns including 2 of 5, alphameric, Codabar™, UPC, and DCI. Available in both serial and parallel outputs, unit also features alphameric display and NEMA 12 enclosures. Scanner is programmable to provide command output for machinery control. **Accu-Sort Systems, Inc,** Sellersville, PA 18960.
Circle 244 on Inquiry Card

SERVOMOTORS

A300 series 1.5″ (3.8-cm) diam direct replacement permanent magnet motors feature a 9-slot armature, specially skewed with small slot openings. This provides lowest cogging for use on equipment where very low reluctance torques are required. Features include adjustable brush rigging for optimum performance and min bidirectional error, plus self-aligning bearings to dampen shock and vibration. The motors deliver high power outputs of up to 3 oz-in (0.02 N•m) continuous duty at 7000 r/min. **Hathaway Instruments, Inc,** PO Box 45381 SE Sta, Tulsa, OK 74145.
Circle 245 on Inquiry Card

PRODUCTS

MODEM INTERFACE ADAPTERS



EIA modem interfaces are able to operate in V.35 and 300-series circuits with two interface adapters. IFA-2 allows connection of an EIA RS-232/V.24 modem interface to a 303 business-machine cable; IFA-4 operates from the same EIA interface, but outputs V.35 (CCITT) compatible signals on a Bell DDS-configured pinout. Built-in diagnostics, slot transparency, and modularity are common to both. Plug-in units measure 2 x 4 x 7.5" (5 x 10 x 19 cm), and each has a standardized rear-mounted connector. **Prentice Corp,** 795 San Antonio Rd, Palo Alto, CA 94303.

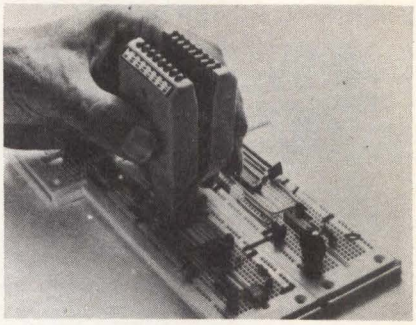
Circle 246 on Inquiry Card

TEXT EDITOR PRINTER

Output speed of the company's std keyboard printers is doubled with the Q-Pak printer that is available for all Redactor[R] I editing and communicating typewriters. Existing word processing systems can be retrofit with the printer, or dual card or tape systems may be ordered with the higher speed printer. Information is transmitted from a computer or another printer directly to this printer at 30 char/s. Features include a microprocessor that provides built-in 31-char memory, daisy wheel printing element, and 10 and/or 12 pitch. **Redactron Corp,** 100 Parkway Dr S, Hauppauge, NY 11787.

Circle 247 on Inquiry Card

DIP LOGIC MONITORS



By monitoring an entire 14- or 16-pin DIP at once, the 16-channel clip-on logic monitors reveal the action of the package as a whole; the state of the pin is indicated by an LED. Model LM-1 tests DTL, TTL, HTL, and CMOS families, automatically seeking out the highest pos and lowest neg voltage levels. Model LM-2 includes a fully isolated line-operated power supply to eliminate test circuit loading. A switch selects RTL, DTL, TTL, HTL, or CMOS operation. **Continental Specialties Corp,** 70 Fulton Terr, New Haven, CT 06509.

Circle 248 on Inquiry Card

FREQUENCY SYNTHESIZER

The SI-160 frequency synthesizer is an advanced 5-digit unit providing ECL signals into a 50-Ω load over the range of 20 to 160 MHz, with a resolution of 1 kHz. Utilizing all solid-state circuitry and a single, phase locked loop, this laboratory instrument has a temp stability guaranteed to ±1 ppm over the range of 0 to 50°C. Enclosure measures 8.5 x 3.2 x 9.0" (21.6 x 8.1 x 22.9 cm). Power is either 115 or 230 Vac, 50 or 60 Hz at 8 W. Various options are available. **Syntest Corp,** 169 Millham St, Marlboro, MA 01752.

Circle 249 on Inquiry Card

DATA LINE MONITOR

TT-101 operates as monitor, trap, exerciser, display, data storage unit, and electronic strip/logic recorder, allowing users to monitor and display all data flow through a communications link. Autopoll and response interrogation capabilities simulate operations such as telecommunications control unit polling sequence, and monitor the response, storing positive responses in memory. Std display system consists of 256-char CRT and rotary display control. Using the control, 16 segments of 256-char pages of memory may be individually displayed in hex, ASCII, EBCDIC, EBCD, or correspondence code. Display function shows transmit characters. Sequences of characters and transmissions are stored in 4k memory, which is also available to the user. **Eotec Corp,** 2595 Martin Ave, Santa Clara, CA 95050.

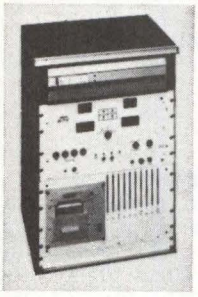
Circle 250 on Inquiry Card

DESKTOP ENCRYPTION UNIT

A portable self-contained unit, DC-26 has a full size keyboard and thermal page printer and provides rapid data entry plus hardcopy output when used as a central or base-station encryption unit. As the message is typed, characters appear on a 5-char LED display. By continued typing, characters are shifted successively off the display, enciphered, and printed. To decipher, scrambled characters are entered in groups of five, with characters being successively shifted off the display, deciphered, and printed after the sixth character is entered. Display is a 16-segment LED alphanumeric type. The thermal 5 x 7 dot matrix printer has max line length of 80 char and prints at 30 char/s. **Datotek, Inc,** 13740 Midway Rd, Dallas, TX 75240.

Circle 251 on Inquiry Card

BACKPLANE INTEGRATED TEST SYSTEMS



Rack-mounted units feature a magnetic tape deck (for endless cartridges) that records a verified prototype assembly for comparison with each production assembly. Tapes can be changed in seconds to match any number of products being tested. BITS test system checks each point for a connection or open to all other points and can cover 1000 points in <10 s. Record and test times are approximately the same. Testing for shorts and opens simultaneously, the unit prints out the error and its correction on paper tape, providing the operator with the information necessary to correct the error. Capacities are 1k, 2k, 5k, and 10k inputs. Base capacity of 99 points is expandable in groups of 100 by adding connectors and I/O boards. **Addison, Div of Muirhead,** 1101 Bristol Rd, Mountainside, NJ 07092.

Circle 252 on Inquiry Card

MICROPROCESSOR-BASED LABORATORY PERIPHERAL CONTROLLER

LPA11-K controller utilizes FORTRAN calls, and transfers analog data at an aggregate rate of up to 150,000 samples/s. Use of DMA enables a 60 to 80% reduction in CPU overhead rates as compared to previous techniques. The unit operates under the RSX-11M operating system on all PDP-11 computers with UNIBUS I/O. Single user mode achieves high throughput rates; multiuser mode allows up to eight users to control experiments and processes simultaneously. Two microprocessors control data and command transfers between laboratory peripherals and the CPU. The device's I/O bus is designed to accommodate std LDP UNIBUS interfaces without modification. The device plugs into one UNIBUS slot, enabling field upgrade of systems. **Digital Equipment Corp,** Laboratory Data Products Group, Marlborough, MA.

Circle 253 on Inquiry Card

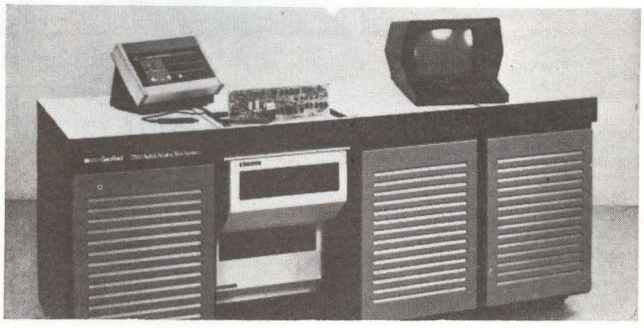
PROGRAMMABLE DATA COMMUNICATIONS TEST SYSTEM

Addition of the Inter-Key keyboard to the Intershake II test system forms a versatile programmable/diagnostic test system. Keyboard simplifies programming and adds capability for entering programs in clear text or hex, or for loading them directly from a tape cassette. Programs may be sent from one system to another, to a printer for program listing, or to tape cassette for bulk storage. Std keyboard and symbols simplify operation. In addition, the combination can act like an asynchronous terminal in conversational mode, at speeds up to 9600 baud with full-duplex transmit and receive capability. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.

Circle 254 on Inquiry Card

PC BOARD TESTER

The 1799 is a fully integrated digital/analog test system that is available with either single- or dual-cartridge disc drives, or dual floppy disc drives for random-access mass storage. A high performance universal pin-scanner matrix allows every pin on the interface shelf to be programmed as a digital driver, a digital sensor, an analog source, or an analog measurement pin. Std measurement capability includes precision dc voltage/current measurement module with integrate, low pass filter, peak-detector, and track and hold mode. A precision resistance measurement unit, high compliance current source, ac voltmeter, and frequency measurement unit are included. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.

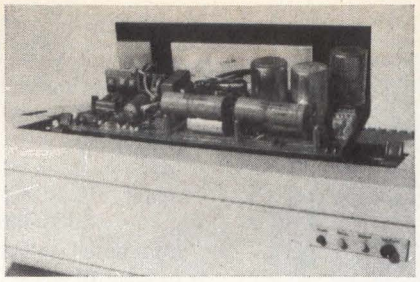


Circle 255 on Inquiry Card

PRODUCTS

SWITCHING REGULATED PRINTER POWER SUPPLIES

ES series multiple output dc power supplies for Diablo and Qume printer applications offer an efficiency rating of 75% and compact size. ES-155E delivers 5 V at 10 A, and ±15 V at 4 A; and handles peak transient loads up to 14 A in 200-W package, with proportional ratings available in 100- and 300-W packages. LSI circuitry features



foldback current limit and overvoltage protection on 5-V outputs. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.
Circle 256 on Inquiry Card

SWITCHING POWER SUPPLIES

Available in three to five outputs, supplies are designed to UL specs and are packaged on a 5 x 9" (12.7 x 22.9-cm) PC board with an edge card output connector and separate 3-pin input connector. Max component height is 2" (5 cm). Outputs available include primary output of 5 V at up to 6 A; second output, 12 to 15 V at up to 9 W; third, −12 to −15 V at up to 9 W; fourth, 5 to 15 V (either polarity) at up to 18 W; and fifth, substrate bias at up to 0.25 W. **Etatech, Inc,** 187-M W Orangethorpe, Placentia, CA 92670.
Circle 257 on Inquiry Card

BAR CODE READER

Model 9200, a code reader on a card, includes a handheld RUBY WAND™ light pen. Complete except for enclosure and power supply, with all needed programming for normal operation on the card, the unit reads all popular bar codes including UPC, Codabar, and code 39. A bar code tag or label can be bidirectionally scanned at 3 to 5 in/s (8 to 13 cm/s) with the light pen reading variable length messages up to 32 char. Std features include ASCII code transmission and RS-232 interface. **Interface Mechanisms, Inc,** 5503-232nd St SW, Mountlake Terrace, WA 98043.
Circle 258 on Inquiry Card

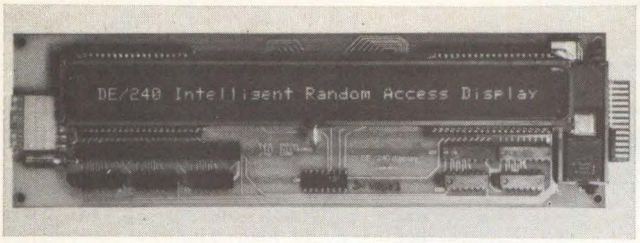
2-SPEED, 20-BIT S-D CONVERTER

Two-speed 20-bit synchro-to-digital conversion is available in a single std module with the 2SD412, which measures 2.6 x 3.6 x 0.8" (6.6 x 9.1 x 2 cm) and weighs <10 oz (283 g). It is available with both TTL and low power TTL outputs at power consumptions of 3.5 and 2 W, respectively. Power supply requirements are 5 and 15 V. Unit offers both binary and nonbinary ratios between the fine and coarse stepping synchros. Accuracy is 0.001 deg at a speed ratio of 36 to 1. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.
Circle 259 on Inquiry Card

LOGIC PROBE

Catch-a-Pulse-Experimentor uses a pulse accumulator to gather multiple pulses into pulse trains for frequency response >40 MHz or to respond to single pulses up to 20 μs. It is compatible with RTL, DTL, TTL, CMOS, MOS, and microprocessors using a 3.5- to 15-V power supply. Thresholds are automatically programmed. No adjustments are required. Visual indication of logic levels is given by LEDs to show hi, lo, bad level, or open circuit logic and pulses. **AVR Electronics,** Box 19299, San Diego, CA 92119.
Circle 260 on Inquiry Card

INTELLIGENT RANDOM-ACCESS DISPLAY



DE/240 is a 40-char/col, dot matrix, vacuum fluorescent microdisplay which features a full ASCII character set and an onboard microprocessor that incorporates character generator, display buffer, refresh, and control logic. Both parallel and serial (1200-baud) interfaces are included to offer universal compatibility with bus-oriented systems and with serial data devices. Three software-selectable end-of-line modes allow editing of 40-char messages. Since all character positions are uniquely addressable, the display can be selectively updated in accordance with the host system's requirements. Display changes are instantaneous, with no distracting line shift effect. **Digital Electronics Corp,** 415 Peterson St, Oakland, CA 94601.

Circle 261 on Inquiry Card

TELEPRINTER/TERMINAL CONVERTER KIT

To convert a DEC LA36 300-baud teleprinter into a 1200-baud interactive terminal, the DS120 card contains a microprocessor which provides necessary control logic. The 9 x 10" (23 x 25 cm) card replaces the standard LA36 card and is plug-compatible with existing electronics. Conversion can be made in minutes with a screwdriver. The microprocessor allows bidirectional printing at 165-char/s, and optimizes carriage movement to automatically tab over white space and print in reverse. It also controls features for forms handling and interactive communications. Std features are EIA interface, horizontal and vertical tabs, top-of-form, Bell 202 compatibility, 100- to 9600-baud line operation, parity selection and error detection, and self-test. **Datasouth Computer Corp,** 122 W Woodlawn Rd, Charlotte, NC 28210.

Circle 262 on Inquiry Card

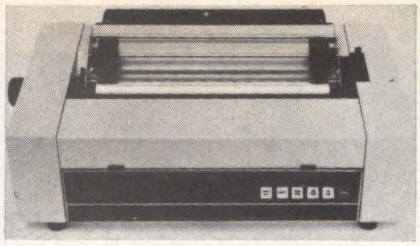
TAPE CASSETTE OPTION FOR DATA COLLECTION TERMINALS

Providing up to 2.88M bits of storage for transaction logging or store-and-forward applications with 1647 series fixed data collection terminals, modular self-contained drive uses industry std cassette tape with biphase level recording. Cassettes meet ANSI, ECMA, and ISO stds. Drives feature a reel-to-reel tape drive system with no pinch rollers or capstans. To maximize data integrity, only the head touches the recording surface. Std speeds include read/write at 10 in/s (25.4 cm/s), fast forward/rewind at 80 in/s (203 cm/s), and search speeds of 40 to 80 in/s (101 to 203 cm/s). Density is 800 bit/in (315/cm) with std data transfer rate of 8000 bits/s. MTBF of the drive, excluding head, is 15,000 h. **Epic Data Corp,** 6350 LBJ Freeway, Dallas, TX 75240.

Circle 263 on Inquiry Card

BIDIRECTIONAL MATRIX PRINTERS

A matrix printer and receive-only communications terminal with Ballistic™ printheads are designed for continuous printing applications. Respectively, the model 201 comes with a std 36-pin parallel interface, while the model 210 is equipped with RS-232 and CCITT current-loop interfaces. Throughput



capacity of both is 75 lines/min for 132-char lines, 120 lines/min for 80-char lines, and >900 lines/min for 1-char lines. **Lear Siegler Inc, Electronic Instrumentation Div,** 714 N Brookhurst St, Anaheim, CA 92803.
Circle 264 on Inquiry Card

NOVA ADD-IN MEMORY

Hardware and software compatible with Data General Nova™ systems 800, 820, 830, 840, 1200, 1210, and 1220, the 3401 add-in memory is expandable in 4k increments to 32k words. Designed around the Burroughs pinout 4k x 1 n-MOS static RAM, it is configured in 16-bit words. The nonvolatile memory has an access time of 240 ns, with 800-ns cycle time. Memory addressing is programmable in contiguous 4k increments. Operating on a single 5 Vdc, the memory has a power dissipation of 11.5 W max operating. **Monolithic Systems Corp,** 14 Inverness Dr E, Englewood, CO 80110.
Circle 265 on Inquiry Card

MODEM ELIMINATOR/DRIVER

Switch-selectable data rates of 2400, 4800, 9600, or 19,200 bits/s of model 300 permit direct connection between terminals and computers while providing the drive capability to operate over distances up to 400 ft (121 m) with std EIA RS-232 interface. Handshaking transpositions are accomplished internal to the unit, since input connectors appear to data terminal equipment as modems. All input signals from one terminal are regenerated by line receivers and drivers before being transmitted to the other terminal. **Avanti Communications Corp,** Box 205, Broadway Station, Newport, RI 02840.
Circle 266 on Inquiry Card

GRAPHIC TV DISPLAY SYSTEM

Modular GMR-27 system comes in three basic configurations: black and white or color graphics and alphanumerics, gray scale and pseudocolor imaging, and full color image processing. Unit has plug compatible interfaces for most computers, and uses high speed 4k MOS random-access display memories. Memory capacities of up to 27 512 x 512 resolution planes are available. Std are alphanumerics and a complete graphics package; image scrolling, byte unpacking, memory readback, and diagnostic self test. **Grinnell Systems Corp,** 2986 Scott Blvd, Santa Clara, CA 95050.
Circle 267 on Inquiry Card

ROTARY SWITCH KITS

All necessary components for assembling A, F, or JKN type switches are included in kits. Stators, clips, eyelets, rotor blades, shafts, indexing blades, and all mounting hardware are in individual jars to prevent silver tarnishing. With exception of shaft and starwheel assembly and, in some cases, the rotor blade, kit items are ready for direct assembly without performing additional operations. **Oak Industries Inc, Switch Div,** Crystal Lake, IL 60014.
Circle 268 on Inquiry Card

For immediate need, circle 100 on Inquiry Card.
For information only, circle 110 on Inquiry Card.

RESPONSE TIME MONITOR

Connected to asynchronous or bisynchronous multidrop terminal networks by optical coupler or RS-232-C bridge, model 300 maintains a running average of response time; and displays number of transactions as well as min, max, and last transaction response times. A 4-digit LED displays the category with name indicated on an alphanumeric LED display. In asynchronous mode, with the RS-232-C connection, timing is initiated by any user settable character five to eight bits long. In bisynchronous mode, control unit and device addresses are switch-settable into the monitor, and response timing information is obtained by observing data flow on communications link. **Questronics, Inc,** 3565 S W Temple #5, Salt Lake City, UT 84115.

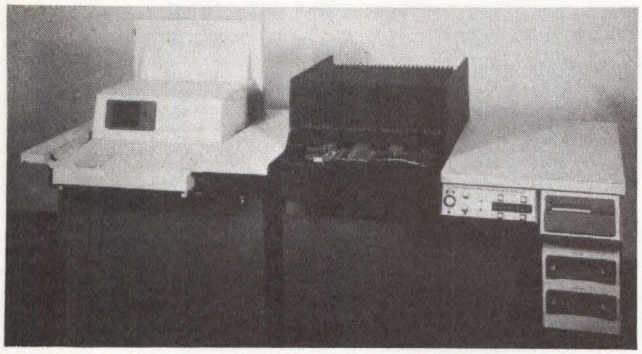
Circle 269 on Inquiry Card

MICROPROCESSOR-CONTROLLED FLAT PANEL DISPLAYS

In addition to providing improved packaging and operating flexibility for the Self-Scan® II line of gas plasma displays, an internal microprocessor controller reduces by 95% the time necessary to design and build frontend control circuitry. To operate the panel, all that is necessary is to feed in appropriate 8-bit signals for char to be displayed. Displays include editing and control routines for insertion, deletion, or blinking of letters, words or lines, increasing or decreasing brightness, and right-to-left data entry. Display subsystem operates off an 8-bit bidirectional or TTL bus. In DMA mode, data can be entered at a rate up to 1 MHz. Other features include shock/vibration resistance, low power, and 2" (5-cm) cross-section. **Burroughs Corp, Electronic Components Div,** PO Box 1226, Plainfield, NJ 07061.

Circle 270 on Inquiry Card

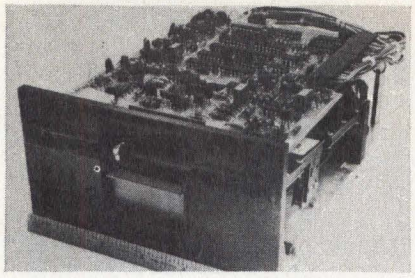
IN-CIRCUIT TESTER



Locating assembly and component faults on analog, hybrid, and digital PC boards, the L529 assembly inspection system prescreens boards prior to functional board test. Microprocessor-controlled tester includes operator's test station, board handler, and programming console. Test station includes control panel for directing all system functions, two tape drives, and strip printer for generating diagnostic error messages. Programmer's console contains an interactive keyboard and CRT. With a sampling of good boards and the system's self-learn capability, a technician can program a complex board in a few hours. Board handler uses weighted rods for applying the contacting force to boards under test. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111.

Circle 271 on Inquiry Card

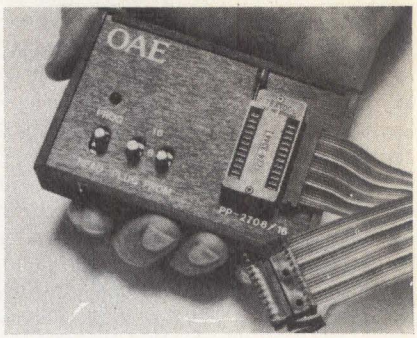
HIGH CAPACITY 5¼" FLOPPY DISC DRIVE



Designated the 1015, the 5¼" (13.3-cm) floppy disc drive is available in either 35- or 77-track models, with single or double density, to a total max storage of 480k bytes/drive. A built-in all-steel head positioner system, using a precision-ground, stainless steel lead screw with steel follower helps assure accurate R/W. Other features are all dc motors, disc-insertion interlock preventing the drive door from closing unless the diskette is properly inserted, and hardware file protect. **Micropolis Corp,** 7959 Deering Ave, Canoga Park, CA 91304.
Circle 272 on Inquiry Card

p/ROM PROGRAMMER

Contained in the series of piggyback p/ROM programmers is the PP-2708/16 which plugs directly into any 2708 or TMS-2716 memory socket. The p/ROM to be programmed is placed in the zero insertion force socket and data are dumped over the eight lower address lines using the company's proprietary interface technique. No additional power supplies are required, and all timing and control sequences are handled by the programmer. **Oliver Audio Engineering, Inc,** 676 W Wilson Ave, Glendale, CA 91203.



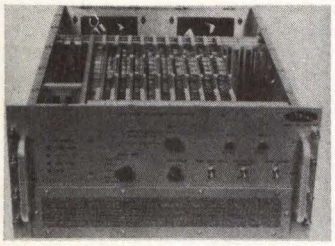
Circle 273 on Inquiry Card

EDP EQUIPMENT TESTER/EXERCISER

A portable and programmable instrument, useful in troubleshooting, tests and exercises any output, input, or communications device, serial or parallel, without tying up a computer or communications line. I/O Donkey features total selectivity for isolating specific problems, 64 stored programs, manual program edit and entry, parity checking, single-step operation, scratch-pad memory, external condition sensing, variable length records, and ASCII ripple generator. **Sorbus Inc, an MAI co,** 150 Allendale Rd, King of Prussia, PA 19406.
Circle 274 on Inquiry Card

COMPUTER RECORDER INTERFACE

Series CRI interface is a high speed, self-contained, multi-megaword data buffer designed to allow efficient computer analysis of wideband signals. Featuring a std digitizing rate of up to 20 MHz and std memory capacity of 1.44M words, the interface accepts output of any wideband receiver or tape recorder and delivers a lower rate digital output to any computer or minicomputer. It is also capable of delivering output to any digital tape transport or disc where the application requires remote processing. Four LEDs indicate the unit's operating state. Separate read and write enable controls are provided for manual operation. Five data block sizes from 64 words to full memory size are operator selectable. **American Electronic Laboratories, Inc,** PO Box 552, Lansdale, PA 19446.



Circle 275 on Inquiry Card

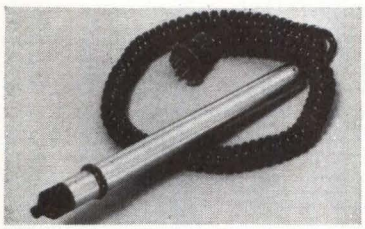
MICROPROCESSOR-BASED IEEE-488 COMPATIBLE SWITCHES

For use in the company's computer-based automatic test systems, switches solve problems associated with connecting UUT to test system. A single 9411A switch controller provides microprocessor control of up to eight switch mainframes, and allows self-test and isolation of faulty signal relays in the switching units. The 9412A modular switch provides high density multifunction switching of signals up to 10 MHz; a built-in 1768 pin interface panel improves signal performance and eliminates spider web cabling. 9413A VHF switch provides flexible high frequency switching of pulse and video signals up to 500 MHz, accommodating up to 12 coaxial switch modules of two types. 9414A, a 16-input matrix switch, switches signals up to 10 MHz. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 276 on Inquiry Card

LIGHT PENS

LP-210/211 offer ease of operation, high sensitivity and fast response times, and simple system interfacing for interactive CRT systems. Luminous sensitivity is 2.1 ftL for both models. Response time is <300 ns—10 times faster than comparable models. LP-210 features patented Touch-Sense™ actuator tip, which is activated by touching the operator's index finger to the pen's barrel when a hit is desired; -211 is identical except that it is fitted with a push-actuation tip that is enabled by pushing against the CRT faceplate. Both versions provide spectral response from 4200 to 11,000 Å; min vector speed of 20 cm/ms; and min input separation of 20 μs. **Information Control Corp,** 9610 Bellanca Ave, Los Angeles, CA 90045.



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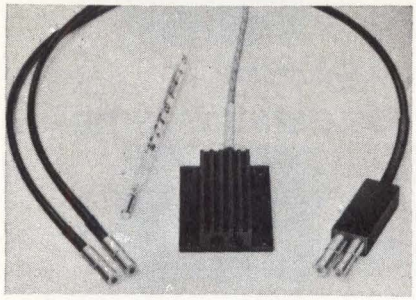
PRODUCTS

FIBER OPTIC SCANNER



A coaxial scanner with sensing tip is designed to operate at a temp of 100°C, suiting it to conditions of severe shock and vibration. A glass fiber optic cable and separate scanner body containing a light source and phototransistor comprise the S17103/F17306 Enviro-Skan. Reflective scanner can be converted to a throughbeam by removing the single cable and reinserting two fiber optic cables. Both cables are available in lengths of 12, 24, and 36" (30, 61, and 91 cm), with ferrule or threaded tip. **Skan-A-Matic Corp,** PO Box S, Elbridge, NY 13060.
Circle 278 on Inquiry Card

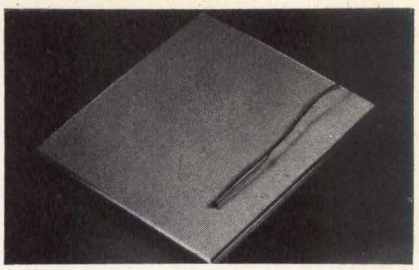
AUTOMATIC SEMICONDUCTOR TEST SYSTEM

Handling devices with up to 120 I/O pins, Sentry™ VIII solves very-large-scale integration test problems. It will also handle microprocessors, peripheral chips, bit slices, phase lock loops, RAMs, ROMs, shift registers, UARTs, and digital hybrids in n-MOS, CMOS, SOS, ECL, DTL, TTL, and IIL technologies. Features include 16 timing generators, expanded waveform generation, and 160-ps timing resolutions. **Fairchild Camera and Instrument Corp, Systems Technology Div,** 1725 Technology Dr, San Jose, CA 95110.
Circle 279 on Inquiry Card

PROGRAMMABLE SEQUENCE CONTROLLER

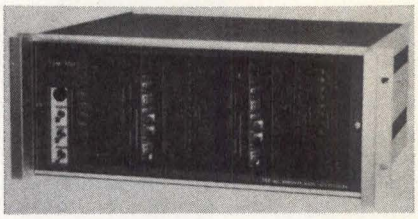
Controller, modularly designed for sequential programming of automation control functions, is capable of logical and monitoring operations as an integral system. For programming of control sequences with fail-safe operation, system incorporates LSI microprocessor and expandable memory modules. Controller offers full expansion capabilities for control logic and sequence timing/counting or arithmetic/computation applications. **Applied Systems Corp,** 26401 Harper Ave, St Clair Shores, MI 48081.
Circle 280 on Inquiry Card

DIGITIZER



Aimed at replacing joysticks, light pens, and trackballs for CRT cursors, while providing precision graphics capability for interactive systems, the self-contained Simple One™ digitizer employs an 11 x 11" (28 x 28-cm) active surface area. Features of source data entry, menu selection, and display manipulation are combined with precise graphic data input. Resolution is 200 lines/in (79/cm) with ±0.02" (±0.05-cm) accuracy. Output is 16-bit parallel binary (bisequential); RS-232-C is optional. **Talos Systems, Inc,** 7419 E Helm Dr, Scottsdale, AZ 85260.
Circle 281 on Inquiry Card

DATA MULTIPLEXER



Remote processes are controlled and monitored by the TDM-100 telemetry data multiplexer, which accurately transmits the data over voice-grade telephone lines. The modular data communication terminal has an active filter and error lockout circuit that provides transmission accuracy to within ±0.5%. Its capacity is 240 command and 240 status channels over a 2-wire circuit using combined frequency and time division multiplexing. **Telemetry Systems Engineering, Inc,** York and Haverhill St, Andover, MA 01810.
Circle 282 on Inquiry Card

MILITARIZED MINICOMPUTER

The PDP-11/70M, a militarized, hardware and software compatible version of DEC's PDP-11, fills the need for a powerful, high performance minicomputer that supports large data bases as well as heavy computational applications in the military market. Providing all features of the commercial model including memory storage of 2M words and cache memory, the computer operates in severe environments. Basic unit is packaged in three full air transport rack chassis, containing the CPU modules, memory I/O interfaces, and power supplies. **Norden div of United Technologies Corp,** Norwalk, CT 06856.
Circle 283 on Inquiry Card

LITERATURE

Stepping Motors

Bibliography of papers and patents covering electromagnetic, hydraulic, and electromechanical stepping motors gives chronological references, listing of patents, stds, national recommendations, and abstracts. Price is $43.50, plus $5.74 for postage and handling. **Publication Sales Dept, ERA Limited,** Cleeve Rd, Leatherhead, Surrey KT22 7SA, England.

Data Communications Networks

"Smart/Network Book," including descriptions of port and equipment tables, and cost summary for network design, enables readers to calculate data communications and networking needs. **Digital Communications Associates, Inc,** Norcross, Ga.
Circle 320 on Inquiry Card

Shaft Position Encoders

Dimensional drawings, photos, application information, and electrical specs comprise 20-page catalog on high resolution, absolute, and incremental rotary optical encoders. **Litton Systems, Inc, Encoder Div,** Chatsworth, Calif.
Circle 321 on Inquiry Card

Network Control Systems

Through use of diagrams and step-by-step explanations, booklet discusses centralized monitoring, and testing and restoring capabilities of System 180 and 200 network diagnostic control equipment. **Racal-Milgo, Inc,** Miami, Fla.
Circle 322 on Inquiry Card

Power Supplies

Bulletin provides technical information on various applications by enumerating power requirements such as specific designations in voltage, current, and overvoltage protection. **Standard Power, Inc,** Santa Ana, Calif.
Circle 323 on Inquiry Card

Primary Power Receptacles

Including dimensional diagrams and material specs, product bulletin describes ac power receptacles which meet connector requirements for U.S., Canadian, and European electrical/electronic equipment. **Switchcraft, Inc,** Chicago, Ill.
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Power Supply Modules

Catalog furnishes complete electrical specs, operating parameters, and dimensional charts for std power supply modules. **Abbott Transistor Laboratories, Inc,** Los Angeles, Calif.
Circle 325 on Inquiry Card

Electrical and Electronic Equipment

In five sections covering tapes, resins, flexible insulation and tubing, equipment, and special services, digest details products and services for electrical and electronic industries. **3M Co,** St Paul, Minn.
Circle 326 on Inquiry Card

Ferrite Toroids

Std sizes, materials, magnetic and electrical properties, and performance and parameter curves are highlighted in catalog containing design and applications guidelines for ferrite users. **Ferronics, Inc, Ferrite Div,** East Rochester, NY.
Circle 327 on Inquiry Card

Permanent Magnet Motors

Catalog offers motor parameters, dimensions, and performance data with curve charts on permanent magnet motors and integral motor tachometers. **Indiana General, Motor Products, a div of Electronic Memories & Magnetics Corp,** El Paso, Tex.
Circle 328 on Inquiry Card

Digital and Analog Electronics

ADDbook ONE, a 400-page tutorial and experimental manual based on the ADD 8000 modular electronics laboratory, provides text, diagrams, and definitions of terms for instruction and reference. Price is $17. **E & L Instruments, Inc,** 61 First St, Derby, CT 06418.

p/ROM Programmers/ Microprocessors

Short-form catalog of p/ROM programmers, microprocessor systems and analyzers, support hardware, and design courses is presented with product photographs and selection charts. **Pro-Log Corp,** Monterey, Calif.
Circle 329 on Inquiry Card

Digital Panel Instruments

Photos, features, applications, and diagrams for selecting and understanding line- or logic-powered digital panel meters and instruments are presented in 80-page catalog. **Analog Devices, Inc,** Norwood, Mass.
Circle 330 on Inquiry Card

Minicomputers

Brochure lists capabilities, capacities, disc drives, and std and optional peripheral equipment to explain family of George™ minicomputers. **Cincinnati Milacron, Electronic Systems Div,** Lebanon, Ohio.
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Vertical Cabinets

Brochure details and illustrates features of 71 accent vertical cabinets that are available in four panel heights and two depths. **Scientific-Atlanta, Inc, Optima Div,** Tucker, Ga.
Circle 332 on Inquiry Card

Modular Power Supplies

Catalog discusses encapsulated modular power supplies by furnishing dimensional diagrams together with power supply and electrical specs. **Calex Mfg Co, Inc,** Pleasant Hill, Calif.
Circle 333 on Inquiry Card

Disc Drives

Detailed bulletin describes design features, operating benefits, specs, and interfaces of 3300 series fixed-media, moving-head disc drives. **Okidata Corp,** Mt Laurel, NJ.
Circle 334 on Inquiry Card

Isolation Techniques

Included in brochure are block diagrams and specific application techniques to point out general isolation problems, objectives, and approaches. **Dynamic Measurements Corp,** Winchester, Mass.
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Power Resistors and Terminations

Data sheet presents specs and material descriptions of resistors and terminations, with outline drawings of four power ratings. **KDI Pyrofilm Corp,** Whippany, NJ.
Circle 336 on Inquiry Card

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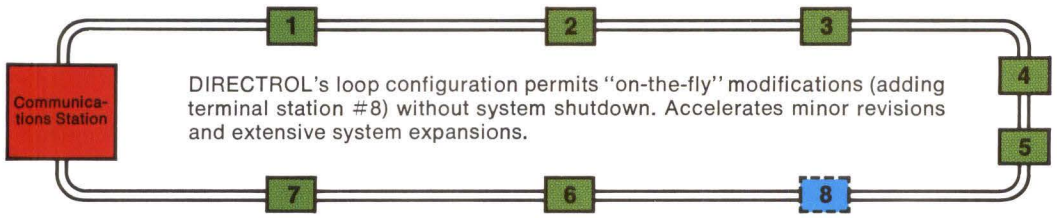

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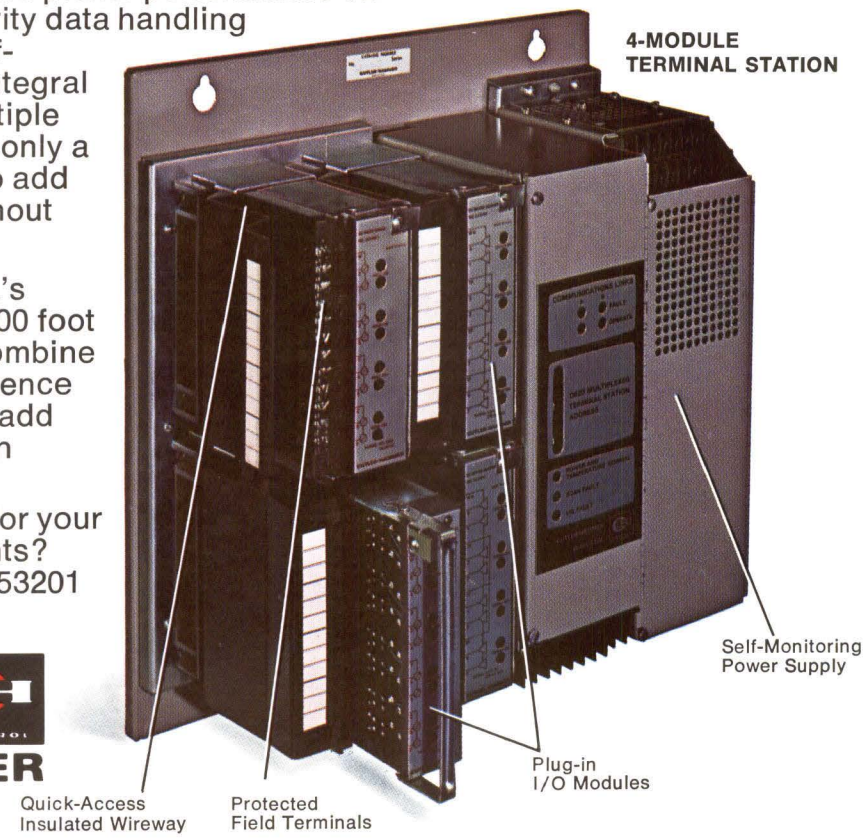

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