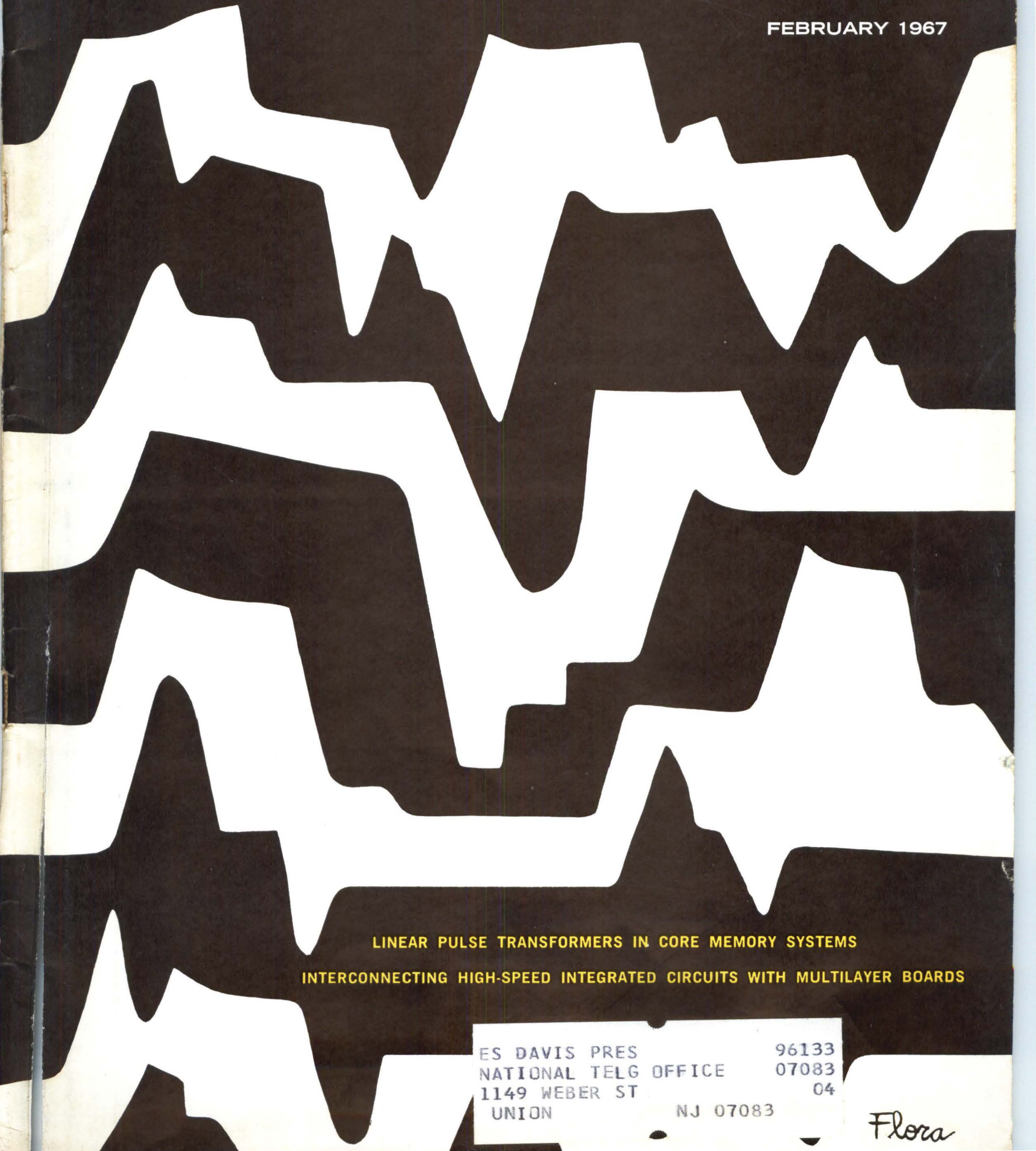
COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

FEBRUARY 1967



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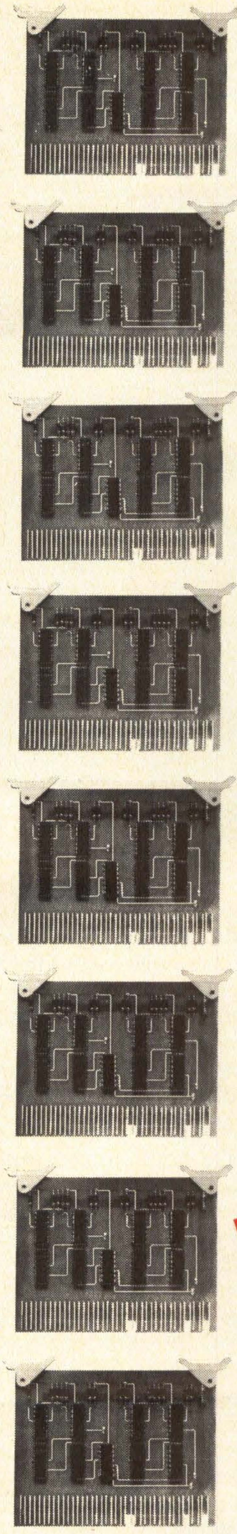

FEBRUARY 1967 • VOLUME 6 • NUMBER 2

FOR ENGINEERING PERSONNEL RESPONSIBLE FOR THE DESIGN & APPLICATION OF DIGITAL CIRCUITS, EQUIPMENT, AND SYSTEMS IN COMPUTING, DATA PROCESSING, CONTROL AND COMMUNICATIONS.

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COMPUTER DESIGN

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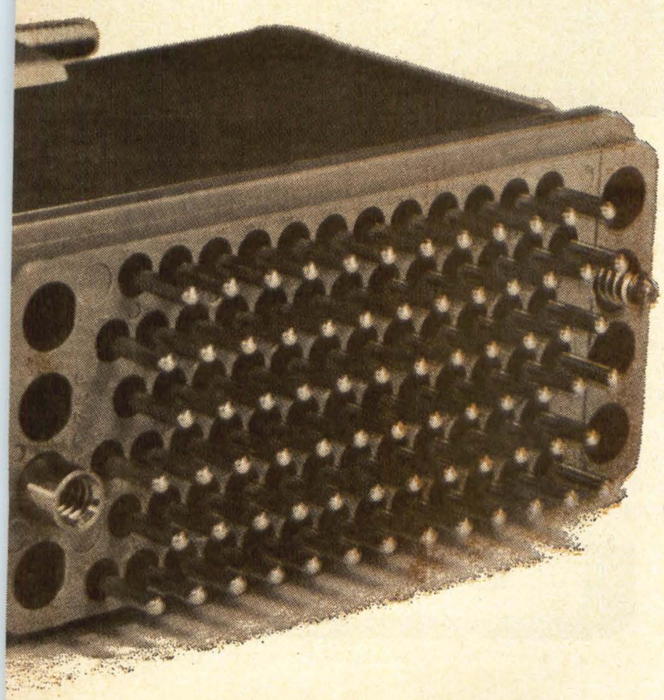

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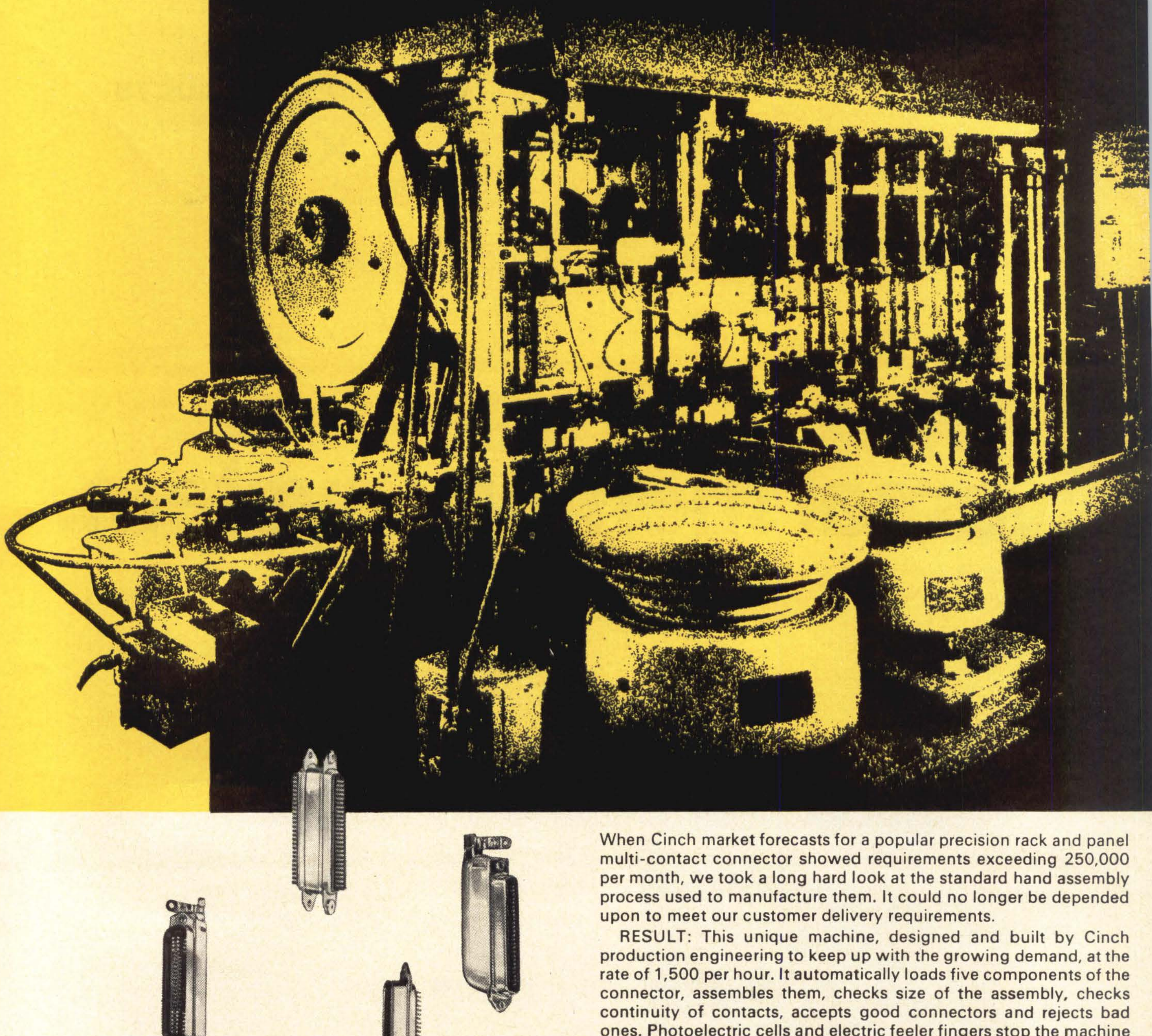

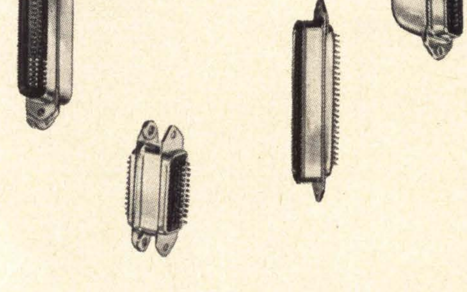

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CIRCLE NO. 5 ON INQUIRY CARD

Letters to the editor

IC LOGIC CARDS

To The Editor:

I enjoyed reading your article in the November 1966 issue of **COMPUTER DESIGN** magazine, as it documented some of the many advantages, to the user, that are available by selecting a well-designed commercial logic family. I am disturbed however, at the omission of the CSC product line from consideration in the survey, as we presently enjoy a position among the top 5 producers of IC logic modules. We are also the only supplier who offers a complete IC line to the government user via a GSA contract. This omission is partially our fault, since CSC has not heavily advertised its product line.

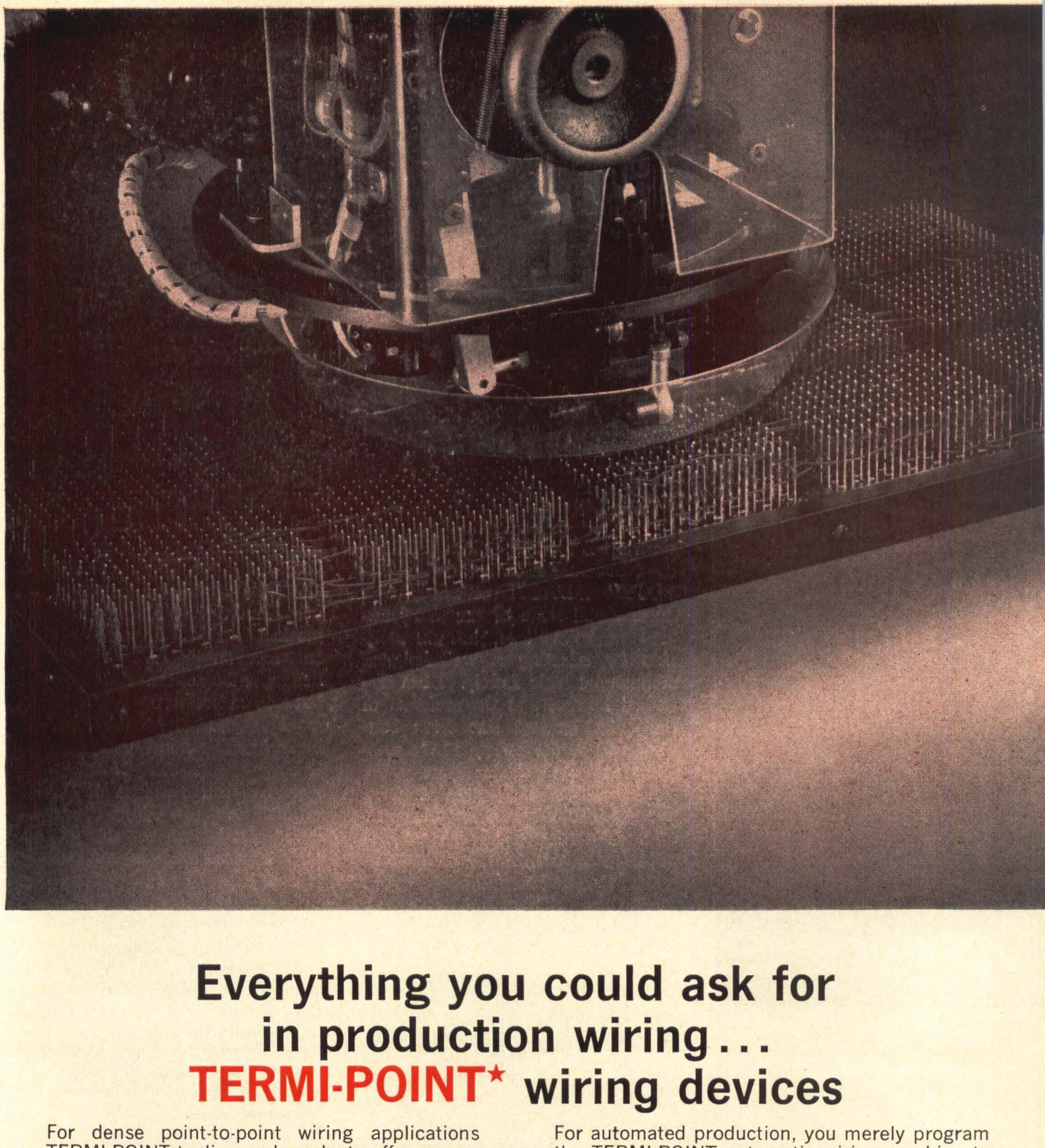
The CSC product line of DTL logic cards was first introduced in January 1965 and has since grown to over 200 items, which are targeted at military and "hi-rel" commercial applications. CSC is the only company which offers a full range military (−55 to +125°C) module line. CSC cards are also offered in 0 to 70°C temperature range. We use Fairchild 930 Series DTL logic but purchase identical components from Stewart-Warner, and Philco. CSC offers 9 basic logic modules, 22 functional modules, and 35 miscellaneous modules, in both temperature ranges, along with accessories. Module interconnections may be made by solder, wire-wrap, taper pin, or "mother boards."

We disagree with your statement that a large broad-based system manufacturer may find the "do-it-yourself" approach optimum. An efficiently run, medium-sized company, organized around a specialty product which requires significant customer service, special handling, design, and a continued flow of new, but related products can always save money, time, and talent for the broad-based systems user and still enjoy a reasonable profit. In a specialty firm such as CSC, QC methods and procedures, documentation, production control, purchasing standards, administration, and personnel are carefully directed towards production of one basic product line. In a diversified systems house the top talent, professional and managerial, will invariably be devoted to project and program tasks rather than to optimizing a commercial logic module line.

Conrad H. Koning, President,
California Systems Components, Inc.
Northridge, Cal.

Editor's Reply: *Our editorial staff apologizes for overlooking this line of modules. For readers who would like to add CSC's literature to their Product Reference File:*

Circle No. 100 on Inquiry Card



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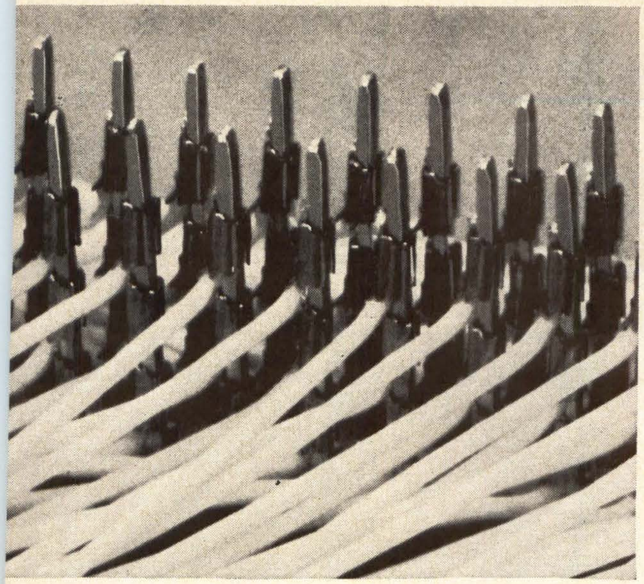
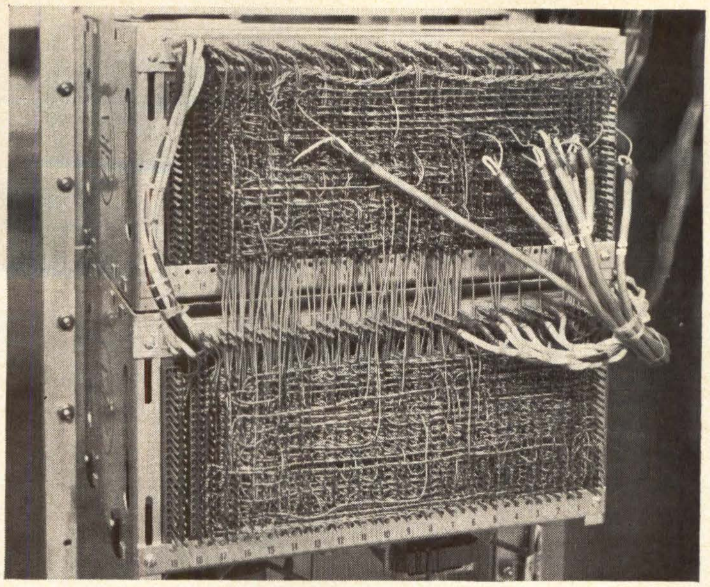
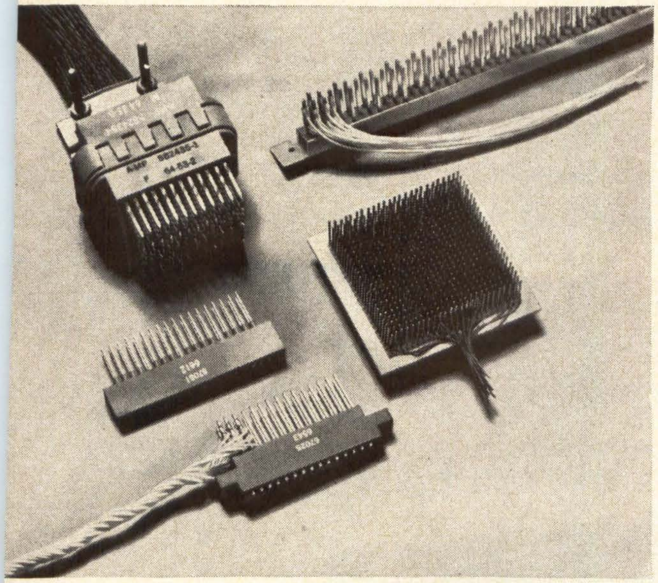
The complete line of TERMI-POINT products includes printed circuit connectors, transition

CIRCLE NO. 6 ON INQUIRY CARD







blocks, bus bars, cable connectors, junction blocks, relay blocks, and other devices. Furthermore, large-scale wiring of these products may be accomplished by mounting them on a panel and programming the TERMI-POINT machine for high-speed automatic wiring.

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No other wiring method offers this combination of advantages!

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If you plan to enlarge or improve your present wiring facilities, we suggest a comparative study of this new technique at your earliest convenience. Write or call today for a demonstration; or ask for information about the TERMI-POINT products which interest you most. Find out how this versatile new method can boost your future production!

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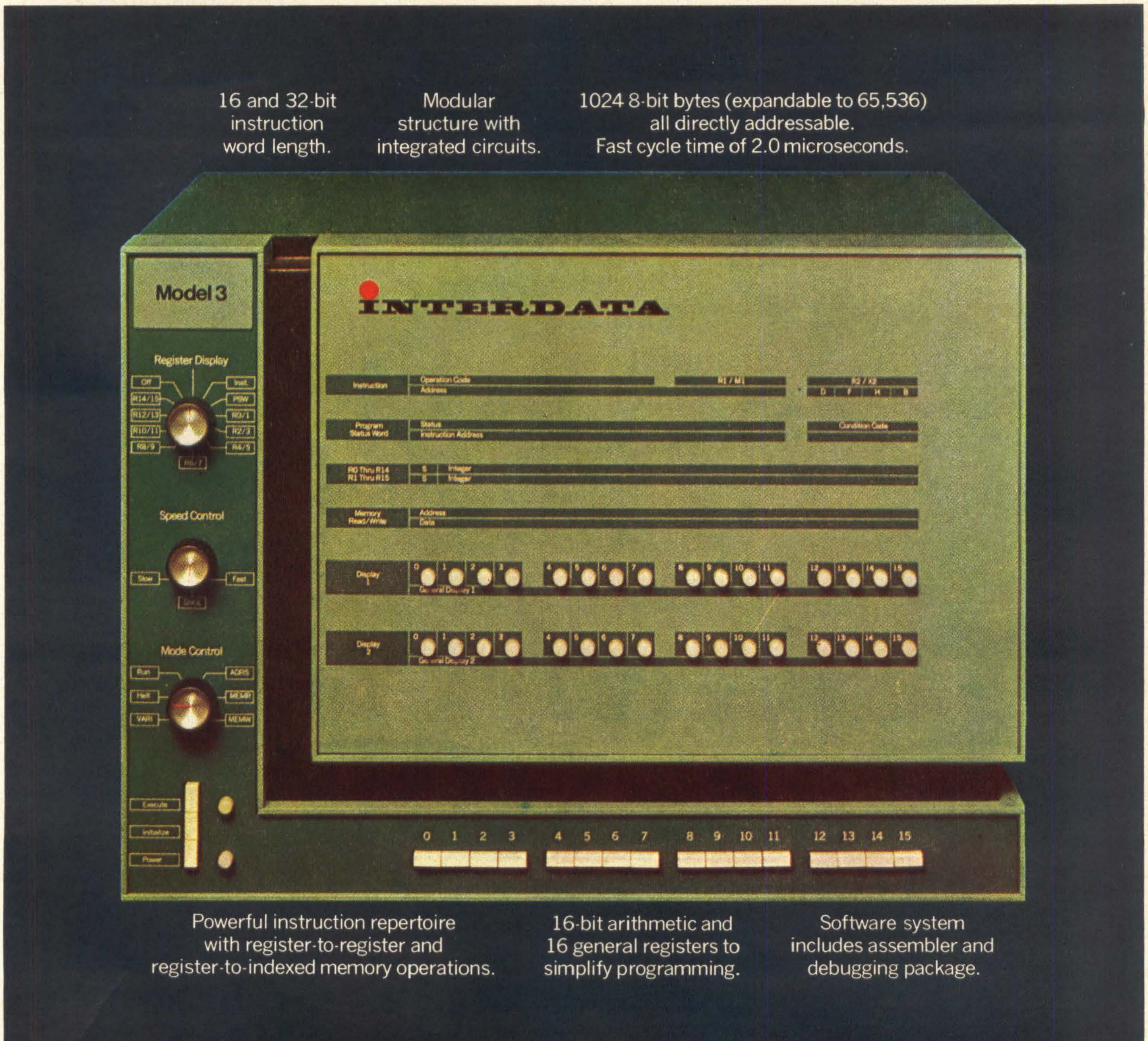

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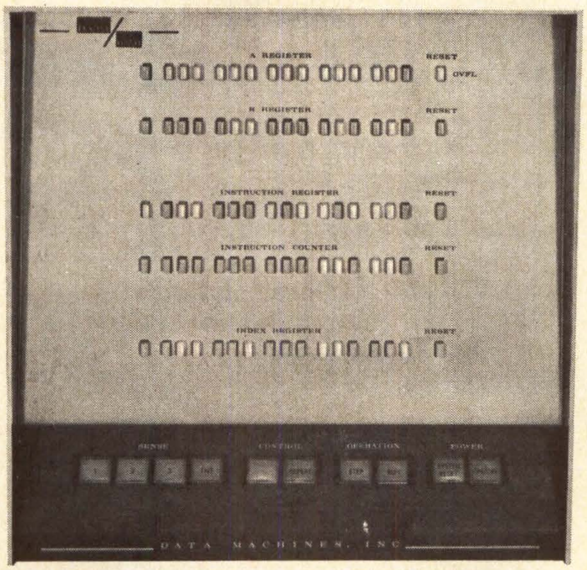

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A Page from the Vermont Research MEMORY FACT BOOK

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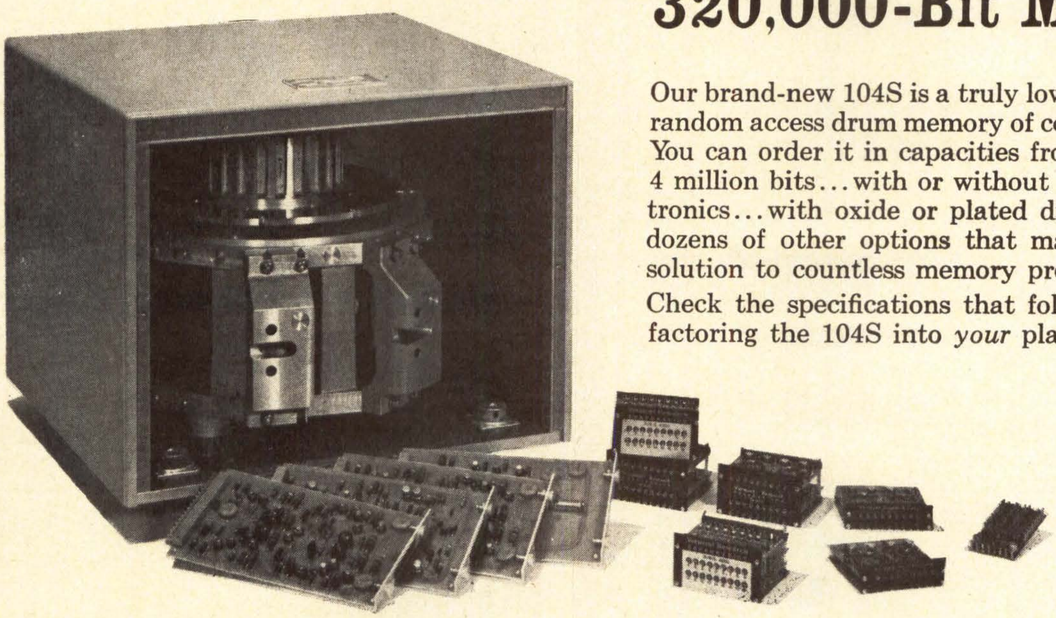

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CIRCLE NO. 19 ON INQUIRY CARD

commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

LARGE SCALE INTEGRATION – PROBLEMS AND POSSIBILITIES

DONALD E. MARSHALL, JR.

Large scale integration may be defined as the technique of placing on a single silicon chip a large number of simple logic elements to perform a system function. LSI usually involves monolithic components, although thick- and thin-film circuitry may also qualify.

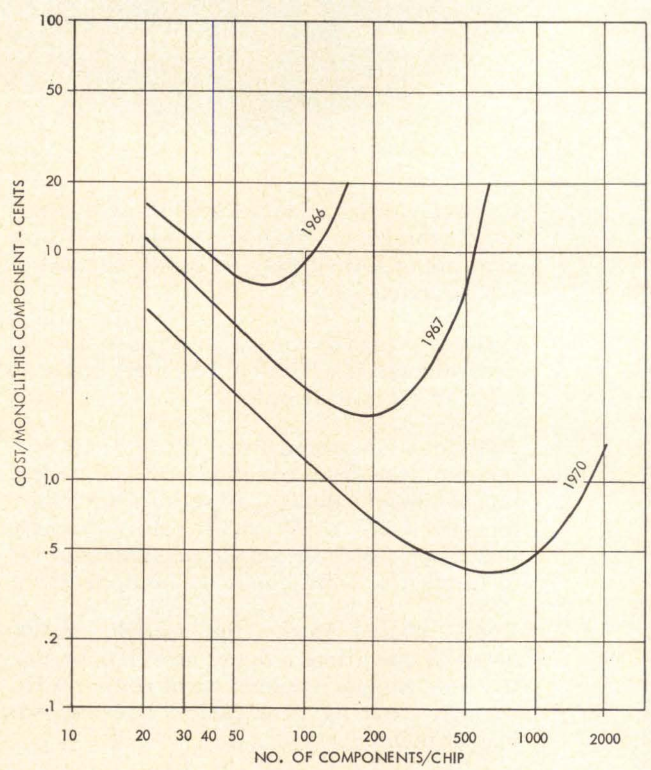
The interest of the computer industry in LSI is understandable. The implications in placing a complete central processing unit, for instance, on a single one-square-inch silicon slice are impossible to ignore. Cost is a major criterion for the broad use of any new technology. However, large scale integration is also expected to improve significantly the performance of computing systems. Few engineers, knowledgeable in integrated circuit technology, doubt that this fascinating concept will ultimately become a reality, but the "how and when" are subjects for much conjecture.

At the present time, we are still a long way from LSI as it is ultimately envisioned. High development and fabrication costs, imperfect fabrication techniques, involved design and development procedures, the complexity of testing, and the problem of system maintenance are among the factors that mitigate against early adoption of LSI for either military or commercial hardware.

Rate of Development

Based on present production yields and costs, the minimum cost per monolithic component is reached at a circuit complexity of 60 components. A larger number of components per chip makes the number of chips per slice too small and increases the probability of a major defect. A smaller chip with fewer components makes the cost of handling, packaging, and testing too high for the logical capability of the circuit.

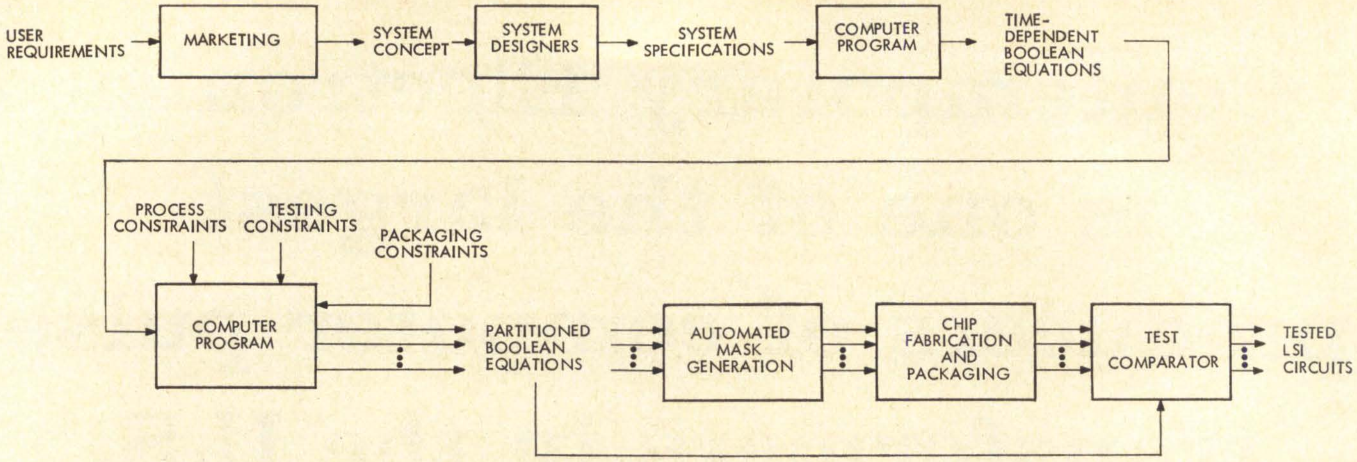
Sixty components is equivalent to about six bi-



OPTIMUM COST/COMPONENT DENSITY

polar transistor NAND gates. At the existing rate of improvement in fabrication technology, optimum chip complexity will double in 1967 and is expected

The author of this month's CD Commentary, Mr. Marshall, is Manager of the Advanced Development Department at the CCD division of Honeywell. In this position, he has the circuit design responsibility in converting the needs of CCD's computer and modular product lines into integrated circuitry purchased from the major integrated circuit manufacturers.



COMPUTER-AUTOMATED DESIGN OF LSI

to exceed 100 gates in 1970. That is, the fabrication cost-per-gate of a 100-gate chip in 1970 will be considerably less than the cost-per-gate of a six-gate chip today. A 4¢-per-gate function cost for a 100-gate chip is quite reasonable, based on anticipated yields and material and labor costs.

One integrated-circuit manufacturer is attempting to beat the yield game by fabricating chips with several hundred gates, testing to find the good ones, and interconnecting these to produce logic functions with a resultant complexity proportional to the process yields at any given time. If this technique can be effectively automated, the above timetable will be considerably accelerated.

An additional accelerating factor for some applications will be the availability of MOS transistor circuitry. Having been proved feasible, the appeal of this component is in its simpler fabrication process, which will ultimately result in very high yields, and in its small dimensions, which may result in about an order of magnitude of improvement in chip complexity over the conventional bipolar transistor approach. However, the comparatively low speed of the MOS transistor may limit its general use to low- or moderate-speed computer applications, such as peripheral equipment, fixed-program memories, or low-speed bulk storage.

Technical Considerations

At the level of complexity envisioned, that is, several hundred gates per device, the system designer is very likely to want a complex function which is optimized for his particular system. In fact, the ability of a computer manufacturer to provide a family of systems with widely-varying pricing and performance characteristics may necessitate individually-designed LSI devices for each member of his family. Therefore, the initial design costs become highly significant as higher functional complexity and specialized application reduces volume usage.

Integrated-circuit development costs typically run about $25,000 for a custom design today, and will increase as device complexity increases using present design techniques. With one device per system and a 25-system requirement, the development cost adds $1,000 to the cost of each system. Clearly, this would be intolerable in many applications, and force the integrated-circuit manufacturer to lower development cost — presumably through design automation. Lagging advances in this area may persuade a number of computer houses to design and fabricate their own LSI chips to minimize the development cost.

An IC facility of even limited capability requires between $250,000 and $750,000 in capital investment. It also requires highly-skilled personnel. One approach is in-house prototype fabrication capability. This limited facility minimizes investment, but provides the necessary design capability.

The classical approach to computer design in which cost, software capability, and computation speed and accuracy are defined, based on a known set of electronic circuits, will require major revision if LSI is to provide economic and performance advantages. The additional constraints placed on system organization result from limitations in the areas of chip density, test and evaluation, spare-parts cost, and partitioning.

In existing bipolar transistor integrated circuitry, the ratio of chip area devoted to active components is about one-half to two-thirds of the total substrate area. The rest is required for component interconnections. In existing MOS transistor circuits, about 80 to 90 percent of the chip area is required for interconnection. The development of a multilayer interconnection capability will improve the ratio of active component area to interconnection area by perhaps two- or three-to-one but each multilayer crossover will have a defect rate associated with it. Since the yield loss will still be dependent on the number of interconnections which, in turn, is related to the ratio of serial-to-parallel data-flow paths, the basic serial-parallel organization decisions, based on cost-speed criteria, will still hold but in manner difficult to relate to the system designer. In fact the design criteria will vary from one IC manufacturer to another.

The complexity of testing an LSI chip approaches the complexity of present day final system testing, in which it is occasionally possible to find logic errors in the field after an extensive final test. Access to each individual functional elements on the chip is prohibited by the high ratio of elements to chip connections, thus forcing a complete functional test.

Consider an LSI chip on which an output state is defined by the states of 20 inputs. At a rate of one Mhz, it takes one second to cycle through all possible combinations of input states. If the chip contains storage or delay elements so that the output state is sensitive to sequences of input states taken two at a time, the test time increases to 14 hours, and for sequences of three, to about 400 years. Testing time can be reduced to within reason by eliminating the test redundancy in the above approach, but the judicious selection of tests which provides full confidence in an error-free chip while minimizing test time will often be beyond the ability of the system designer.

The spares problem is obvious. If the system consists of a few dissimilar integral parts, the system must be virtually duplicated in spare parts. On the assumption that LSI will be in wide use before the cost of the chip approaches the cost of a present-day printed circuit module, the LSI system user will have to give careful consideration to his ability to afford repairs, and must be convinced that part replacement cost will be offset by the improved reliability of the LSI system.

LSI will improve the reliability of electronic systems in approximate proportion to its reduction in the number of external inter-connects per gating function, provided that the LSI chip does not produce any additional environmental stresses on the monolithic components. In order for LSI to be maximally effective, the number of external connections to the complex chip should be minimized but for most useful logic functions it will be about equal to the square root of the number of gates on the chip.

Of major importance is the reduced capacitive loading and length of chip interconnections compared to printed-circuit and connector-plane interconnections. This will reduce propagation delays and thus increase computer speed. But of even greater significance will be the reduction in system noise, making larger and faster computers possible.

The Ultimate Solution

When the application of LSI to future systems is looked at in perspective, the magnitude, diversity, and interrelationships of the numerous problems are seen as difficult to organize effectively. The major stumbling block is the broad range of professional disciplines required of the personnel used in the design of LSI devices. However, there is an ultimate solution to the design problem and that is design automation.

Computer-automated design is playing a major role in LSI development now and will continue to do so in the future. However, the system and process engineers will still have to establish the constraints and write the programs for the computer.

CD Refresher Series

MATHEMATICS REVISITED

Selected Topics in Probability and Statistics

Dan M. Bowers, Contributing Editor

PART 8 – DESCRIPTIVE STATISTICS

In turning our attention to the subject of Statistics, we shall find that although the terminology and emphasis are different from those used in the Probability discussions of the previous seven articles, the underlying principles and techniques will be very familiar. Initially, we shall discuss Descriptive Statistics through which data is gathered and presented so as to convey the maximum information; then, through Inductive Statistics, we shall describe techniques for reaching general conclusions and making predictions from the observed Descriptive Statistics.

As an example of the kind of data in which Descriptive Statistics deals, Table 1 lists the closing prices for 188 mutual investment funds on a recent Friday. A look at this data tells us that to obtain any information from the raw data will make a hard day's night, and that there is no particular value to any graphical presentation of these 188 raw numbers. One concludes that grouping of the data will result in the only kind of meaningful graphical presentation to be had, and further, that intelligent grouping will not destroy the meaningfulness of the information contained in the data. There exist sophisticated methods for determining how to group the data (e.g., Sturge's rule): we shall choose (using the seat-of-the-pants rule) to divide this data into groups (known as a **class**) each having a $4.00 span (known as the **class interval**). This yields Table 2, which presents the data as a **frequency distribution of grouped data,** and begins to display the data in a more meaningful form. The graphical presentation of such a distribution, known as a **histogram,** is probably the most popular form of a statistical presentation; the histogram of this data is shown in Fig. 1.

A presentation sometimes used to smooth the histogram is the **frequency polygon,** in which the frequency of each class is plotted at the center point of the class (called the **class mark**), as shown in Fig. 2. Another useful presentation is the **ogive,** which is a cumulative presentation of the data. The ogive for the mutual fund data is arrived at by reorganizing the data listed above, using the upper boundary of each class as a datum point, as shown in Table 3. The ogive is plotted from these data as shown in Fig. 3; it is effectively the integral of the frequency distribution, and is therefore a uniformly increasing function whose maximum value is the total number of data points. To assist in deriving data, the ogive has also been scaled in percentage of the total data.

From the histogram and the ogive we can directly glean some facts about the prices of the mutual funds which were included in this sampling at the time of the samples:

- More mutual funds sell for about $10.00 than for any other price range.
- 93.7% of the funds sell for $20.00 or less.
- 93.6% of the funds sell for more than $4.00.

Before calling our stockbroker, we shall need to investigate the techniques by which more quantitative descriptions of a statistical presentation may be calculated.

Parameters of Statistical Data — Location

The reader will have noted the parallels between the statistical presentation above and the probability distributions studied in past months. The histogram and the frequency polygon are analogous to the probability density function, and the ogive is the analog to the distribution function. Further, the principal quantitative parameters of these observed data are identical with those useful in probability distribution: the mean and standard deviation.

The **mean** is a fancy name for the simple arithmetic average of the data values. In our example, one arrives at the mean by adding all 188 data values and dividing by 188, a process which, after approximately 20 minutes of dog-work (not including re-work for errors) yields the mean (or average)

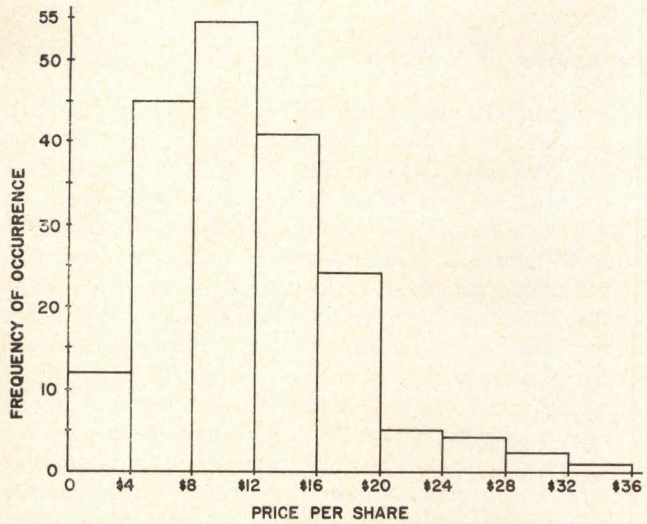


Fig. 1. Histogram for the Distribution of Mutual Fund Prices.

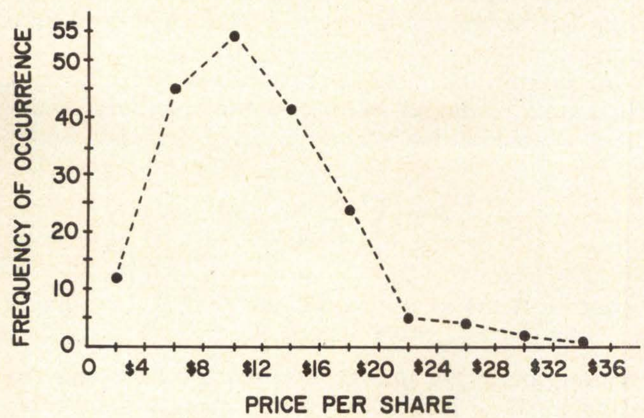


Fig. 2. Frequency Polygon for the Distribution of Mutual Fund Prices.

Table 1

MUTUAL FUND PRICES

2.91	6.11	2.17	1.69	12.46	14.45	2.76
8.63	17.77	17.15	1.77	16.39	15.70	7.43
8.92	12.95	8.81	10.60	13.56	18.98	3.25
4.07	6.35	8.69	9.64	9.80	30.49	11.12
7.31	9.56	2.95	10.36	3.67	9.37	12.47
10.24	15.24	16.74	10.00	26.05	5.75	6.91
7.43	9.52	2.67	4.52	16.17	11.01	14.71
1.72	18.28	1.58	8.88	14.31	6.58	10.24
6.91	8.77	13.07	12.90	10.63	5.68	15.64
7.25	11.54	15.56	17.80	10.56	13.67	26.05
10.48	13.63	14.19	6.65	15.73	7.55	5.47
19.50	17.75	21.62	17.00	9.25	4.46	11.30
14.66	11.00	6.77	10.75	11.10	18.22	11.43
18.40	9.69	16.68	7.25	11.92	5.81	6.85
23.58	6.96	7.54	5.34	9.93	17.20	11.58
24.01	23.79	10.04	29.73	9.59	2.76	6.53
11.31	13.84	18.27	4.78	7.60	11.17	12.87
12.42	15.09	15.17	15.14	8.08	16.18	11.47
11.64	19.35	24.82	15.44	13.47	12.32	5.19
12.16	9.45	21.31	14.76	15.22	13.52	5.79
11.90	16.64	6.13	13.74	5.61	5.86	18.14
5.39	7.57	13.88	5.14	10.10	5.83	11.02
14.09	8.14	9.94	18.85	12.12	7.52	14.23
16.48	9.80	5.60	8.28	12.91	5.56	13.31
11.61	20.86	10.04	6.90	18.33	5.10	7.29
6.27	8.79	7.12	18.77	11.32	14.67	
32.69	15.47	10.29	15.83	7.52	8.75	10.99

Table 2

FREQUENCY DISTRIBUTION OF MUTUAL FUND PRICES

CLASS INTERVAL	FREQUENCY OF OCCURRENCE
$00.01-$04.00	12
$04.01-$08.00	45
$08.01-$12.00	54
$12.01-$16.00	41
$16.01-$20.00	24
$20.01-$24.00	5
$24.01-$28.00	4
$28.01-$32.00	2
$32.01-$36.00	1
	188

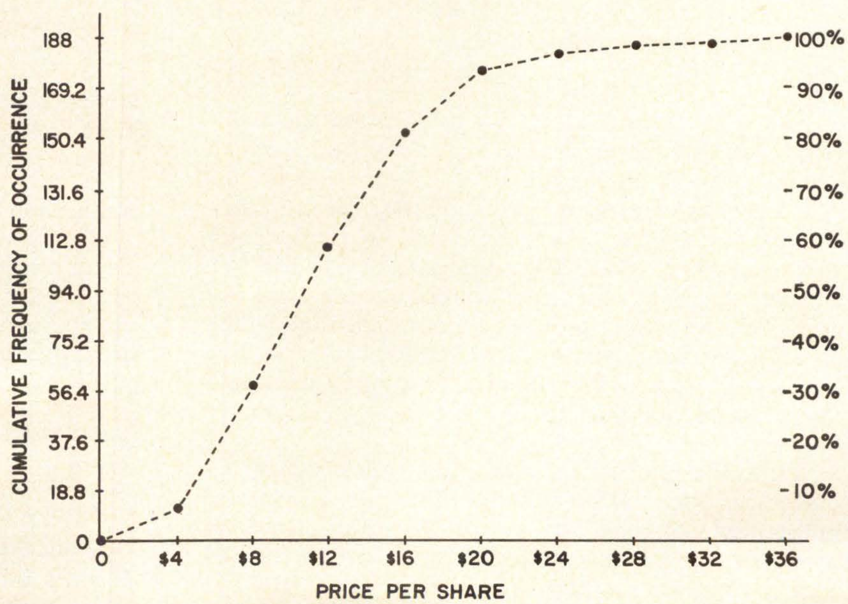


Fig. 3. Ogive for the Distribution of Mutual Fund Prices.

Table 3

CUMULATIVE FREQUENCY DISTRIBUTION OF MUTUAL FUND PRICES

BOUNDARY	CUMULATIVE FREQUENCY	% OF TOTAL
$4.00 or less	12	6.4
$8.00 or less	57	30.3
$12.00 or less	111	59.0
$16.00 or less	152	80.9
$20.00 or less	176	93.7
$24.00 or less	181	96.2
$28.00 or less	185	98.5
$32.00 or less	187	99.5
$36.00 or less	188	100.0

price of a mutual fund on this list, which is $11.48. However, having grouped the data into classes, we should like to work with the grouped data and, further, we should expect grouping to make the calculation simpler. To do so, we assume that every datum in a class has the value of the class mark. Therefore, the mean can be arrived at by multiplying the frequency of each class by the class mark, summing over all classes, and dividing by the total frequency of 188. Using this process, and after only 5 minutes of dog-work, we arrive at a mean of $11.43. This illustrates the significant point that intelligent grouping of statistical data does not appreciably deteriorate the basic values of the data. (We shall see in a later article that one may very closely approximate such parameters as the mean by calculations with only a relative few of the data points, chosen at random from the full list.)

Note the identity of the formula for obtaining the mean of grouped statistical data with that (in Part 5, August issue) for the mean of a discrete probability distribution:

$$\text{Mean (grouped data)} = \frac{\sum\limits_{\text{all } i} x_i f_i}{\sum\limits_{\text{all } i} f_i}$$

where x_i is equivalent to the class mark of the i^{th} class and where f_i is equivalent to the frequency of occurrence of the i^{th} class.

The **median** of a set of statistical data is the value of the middle item, when the data are numerically ordered, which is $10.99½ (the average of the two middle items) for the raw mutual fund data. For grouped data, the median is a vertical line which divides the histogram into two equal areas, in this case $10.74. The median has the frequently-desirable characteristic of not being drastically affected by extreme values, as is the mean.

The mode of a set of data is the value which occurs most often. Note that the mode is valueless in an example such as the raw mutual fund data, since without grouping the mode can exist only if a price chances to appear more than once. For grouped data, one refers to the **modal class**, in this case the class having a class mark of $10.00.

Quartiles are three numbers which divide the area of the histogram into four equal parts. Similarly, **deciles** and **percentiles** are nine and 99 numbers, respectively, which divide the histogram into ten and one hundred equal parts.

Parameters of Variation

The measures of central location provide us with one number which is descriptive of the data for many purposes. We might, for example, speak of the mean annual rainfall, median intelligence, or the modal cause of business failure. As we have seen in probability distributions, however, the variation or dispersion of data about the center is generally of equal importance. The common measures of variation are the range, the average deviation, and the standard deviation. The **range** of a set of data is the difference between the largest and smallest data points. It is not particularly descriptive of the general tendency of the data to disperse, but does communicate some information. **Interquartile ranges** are also used. The **average deviation** (also known as the **mean deviation**) is the sum of the absolute values of the deviations of each datum from the mean, divided by the total number of data points.

As before, the most-used measure of variation is the **standard deviation**, or **root-mean-square deviation**, which can be expressed as:

$$\sigma = \frac{\sqrt{\sum\limits_{i=1}^{n} (x_i - \mu)^2}}{n}$$

where σ is the standard deviation; n is the number of data points, $n = \sum\limits_{\text{all } i} f_i$; μ is the mean; and x_i is a datum point. For grouped data, all data points are considered to fall at the class mark of their class, and the standard deviation becomes:

$$\sigma = \frac{\sqrt{\sum\limits_{j=1}^{k} (x_j - \mu)^2 f_j}}{n}$$

where k is the number of classes; x_j is the class mark; and f_j is the class frequency.

Application of Statistical Data

Using these parameters, we may draw the following two statistical pictures of the mutual fund market as represented by the 188-price sample, in its grouped form.

- Picture A

Mean price: $11.43
Standard deviation: $5.85

- Picture B

First decile: $4.61
Second decile: $6.28
Third decile: $7.95

Fourth decile: $9.35
Fifth decile: $10.74
Sixth decile: $12.17
Seventh decile: $14.01
Eighth decile: $15.84
Ninth decile: $18.87

If we purchase shares of the mutual fund selling at $21.31 on the day of this sample, we can describe our fund with respect to the mutual market as:

- 1.7 standard deviations higher than the mean (picture A);
- Above the ninth decile (picture B).

At a future date we may then rate the growth of our shares in relation to the growth of the market. For example, if the new mean and standard deviation are $14.05 and $6.20, respectively, and the new price of our shares is $23.00, we can see that our share price is now only 1.4 standard deviations above the mean, indicating that it is not growing as fast as the general mutual fund market.

Successive analyses of the same phenomenon can yield information about past trends which might be useful in predicting future action. Such applications are found in population statistics, weather data, and economic statistics such as the Dow-Jones index and the Gross National Product. Next month we shall explore some of the features of these indices and trend indicators, and discuss how correlation studies may establish a cause-and-effect relationship between statistical trends and other observable phenomena.

GOVERNMENT REPORTS ★★

HIGH DENSITY DIGITAL RECORDING ON MAGNETIC TAPE

Report discusses the problems encountered in high area density digital recording on magnetic tape. It examines some aspects of the process of pulse recording and applies findings to the methods of digital recording in common use. Describes a system which offers advantages at high packing densities.

Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. AD-464-392. Price: $2.00.

LAMINATED FERRITE MEMORY, PHASE I

Report describes development of fabrication techniques to permit the assembly of a laminated ferrite stack of 4096 x 64 bits. For the assembled stack a density in excess of 10^5 bits per cubic inch was demonstrated. Additional test data on individual arrays and results of nuclear radiation studies are included.

Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. N66-19518. Price: $3.00.

what do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

LOGIC SYMBOLS STANDARDS

EDITOR'S NOTE: *Last month the CD Readers' Forum summarized its activity and intentions in the arena of Logic Symbols Standards. One of the points made was that only one strong advocate of the ASA Y32.14 standard had been heard from. This month we present a letter from just such a strong advocate, Mr. Thomas H. Mott, who is Chairman of ASA Y32.14, and thus is intimately involved in the controversy. We believe that our readers will find his unexpurgated views to be very enlightening. Again, we invite your comments.*

TO CD READERS' FORUM:

I am led to believe that your magazine is badly misinformed concerning the complete state of developments in this area of standardization. There has been some slow but hard-won progress made in this area at the conference table, where standards should be sought; and the standardization field itself stands to be the major loser should this gain be wiped out by the misguided efforts of a magazine bent on conducting a popularity poll among its readership. You apparently have not even informed your readers of the existence of two conflicting military standards in this area, thus creating false impression that there is but a single military standard.

Your efforts are further misguided in that you have chosen to work outside the framework of ASA Y32.14, thus ignoring literally man-years of standardization effort by the only duly Federal authorized task group in this area and the only task group truly representative of of the whole of the industry.

Standards should come into existence as the result of a consensus of developing opinion, as did ASA Y32.14 — they should not be legislated into being by arbitrary fiat of a selected few individuals, as was MIL STD 806. The chief architects of MIL STD 806 participated in the development of ASA Y32.14 and were given every opportunity to structure the standard in accordance with their way of thinking. In the end they encountered extensive opposition from adherents within industry of the uniform shape symbology. However, they also encountered opposition from within the military itself, which has led to the promulgation of two separate military standards: (1) MIL STD 00806C (Navy) which is fully compatible with the distinctive shape symbology of ASA Y32.14 and permits use of the uniform shape symbology of ASA Y32.14 for experimental and non-service applications, and (2) MIL STD 806B (Air Force).

There is a long-standing policy within the military of not "legislating" standards when industry standards already exist. Owing to the existence of ASA Y32.14, the Navy Department invoked this policy and adopted the distinctive shape symbology of ASA Y32.14 as MIL STD 00806C. MIL STD 806B thus remains chiefly an Air Force standard.

Since, as a practical matter, standards are not formulated by readers writing letters to the editor of a magazine, I should think that your worthy efforts in the interest of standardization could be spent in more fruitful ways. Specifically, I propose that you use the pages of your magazine to try and resolve the conflict between MIL STD 806B (Air Force) and MIL STD 00806C (Navy). Over a year ago ASA once again invited the military to abandon their position of privileged sanction and move to the conference table to argue the merits of MIL STD 806B vs. ASA Y32.14 in free and open discussion, provided that the ASA task group and the military would be bound by the decisions reached at the conference table. The architects of MIL STD 806B accepted the invitation but reneged (for a second time) on the decisions reached by the conference. The Navy Department had the courage to accept and act on the decisions, resulting in the promulgation of MIL STD 00806C.

There can be no further progress in logic diagram standardization until the impasse concerning these two competing philosophies of the distinctive shape symbology has been resolved at the conference table. Only then can we move to the larger question of uniform vs. distinctive shape symbology.

Thomas H. Mott, Jr.
Dir. and Prof. of Computer Sciences
Rutgers, The State University,
New Brunswick, N. J.

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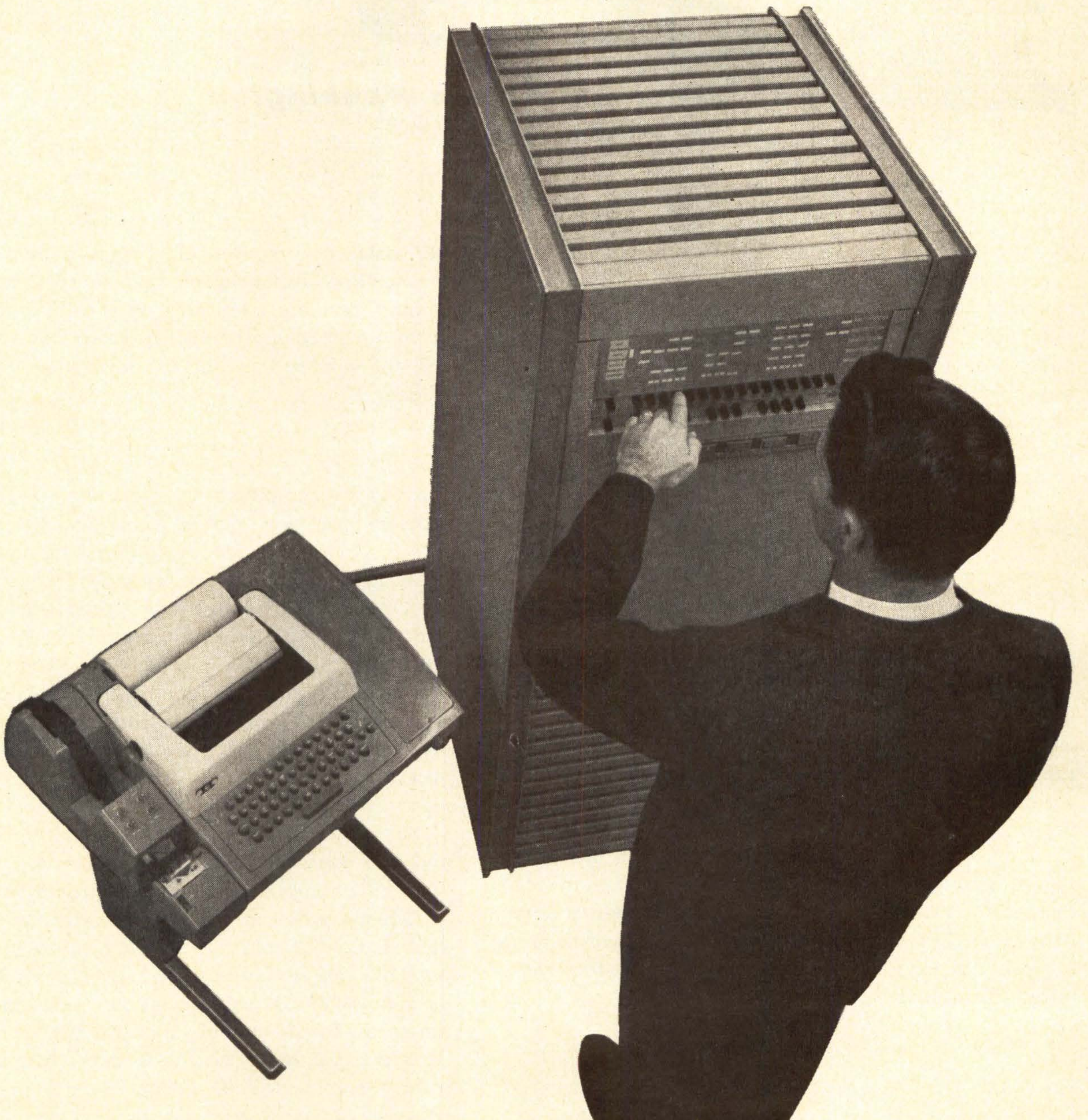

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Systems Engineering Laboratories

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from our man in Washington

Western Europe's present 6,000 computer installations should jump to 18,000 by 1970 — a $3.3 billion increase in value, forecasts S. A. Gee-Smyth, writer for "The Economist," in a recent publication of the European Economic Community. Europe stands on the threshold of a snowballing technology, he believes, with Eastern Europe anxious to buy all types of computers from the West. Other rich pastures for computers are South America and Australia.

A new, simplified, plain language, TRANSIM, for computer simulation in the transportation industry, requires "no glossary, no special vocabulary, no list of definitions, no abstract language, and no short courses" for its operators. Developed by the Commerce Department, the standardized computer program can be used, without modification, from problem to problem. There is no fixed, built-in computer program logic relating to individual, specific transportation problems. It is inexpensive and fast to use. Because new programming is not required and because the simplified input data format is designed for maximum use of readily available data sources, problem turnaround (from formulation to solution) can be accomplished in a small fraction of the time and cost required with other approaches.

The computer is matching jobs for jobless in the District of Columbia's poverty program. The computer program, financed by an $82,000 grant from the Office of Economic Opportunity, prints lists of job openings daily for local manpower centers. USES counselors working at neighborhood centers contact the unemployed matched by the computer and arrange interviews.

Nearly 500 of the Air Force's C-130 propjet transports forming the backbone of the airlift capability in Southeast Asia are being fitted with a tiny built-in weight and balance computer to reduce loading and turnaround time. Input signals from sensors located in the landing gear are integrated by a solid-state computer in the cargo compartment that reads out gross weight and the aircraft's center of gravity as the cargo is loaded.

The use of computers to overcome the information problem gap was played down by Budget Bureau Director Charles L. Schultz during hearings on a proposal by Senator Edward Kennedy (D. Mass.) to have the Advisory Committee on Intergovernmental Relations carry out a study on the possible use of EDP for better coordination of information on Federal aid programs. According to Schultz, much of the needed services for informing state and local officials can be provided by a good up-to-date catalog and does not necessarily require a highly sophisticated, computerized information system. Schultz stated that "information systems in various program fields need to be improved and tied together as a first step, instead of starting with the assumption that computerized systems are the key to the whole problem." Secretary of Commerce John T. Connor told the Senate hearing that it is evident the needed information was not available in an up-to-date, easily accessible form. He questioned if the study should not be done by the Commerce Department. He reminded the Senators that it had been given the responsibility to provide scientific and technological advisory services relating to EDP and related systems and to establish a uniform Federal EDP standard. If the resolution is adopted the Bureau of Standard's services should be utilized, he believes.

Recent Government Contract

GARRETT CORP., Torrance, Cal., has received a $2,732,116 contract order for production of (FSC-6610) computer components for F-4 series aircraft. Work will be done at Los Angeles. The contract order is being issued by the Oklahoma City Air Materiel Area (Air Force Logistics Command), Tinker AFB, Okla.

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INDUSTRY NEWS

COMPUTERS ARE CREATING A WIDENING GAP BETWEEN MANAGEMENT AND EMPLOYEES THAT WILL RESULT IN SERIOUS PERSONNEL PROBLEMS IF NOT PROPERLY RECOGNIZED, says George S. Conomikes, director of Business Forum, Chicago-based business education firm. With the aid of computers, management is able to make improvements in work systems and actually "try them out" before they are installed. This means that management decisions which affect work procedures can be made on the basis of figures rather than human relation. There is an accelerating trend toward this type of remote management, Conomikes pointed out, and the company of tomorrow may well be run by a management that has less and less direct contact with production or office procedures. What does this mean? It means that employees will be told to change the way they are doing things, or to do different types of work, without any understanding of the reasons for the changes. The ultimate result of this according to Conomikes, is a loss of employee "esprit de corps" and it could mean that the "dedicated employee" becomes a vanishing breed. It will be a costly mistake if the human element is neglected in our computerized, systematized, mathematized world of tomorrow, Conomikes stressed. In this future world, there will be a communications gap between the problem-solvers and the people who are affected and who may not fully comprehend the reasons for changes in their systems or work environment. Management had better start looking for the best way to fill this gap if it wants operations to continue at optimum efficiency. The answer, according to Conomikes, is to provide a liaison between management and employees. Someone who will translate management's decisions to the workers involved. Logically, this responsibility should be assumed by the personnel manager.

WESTINGHOUSE ELECTRIC COMPANY HAS ORDERED $5-MILLION OF SIGMA COMPUTERS and related equipment to be purchased from Scientific Data Systems, it was announced by SDS Pres., Max Palevsky.

THE COMPUTER INDUSTRY MUST DEVELOP A NEW YARDSTICK TO MEASURE THE VALUE OF THE COMPUTER-BASED MANAGEMENT SYSTEMS NOW COMING INTO BEING, according to Robert V. Head, Computer Sciences Corp.'s manager of management information technology. He noted that heretofore the measure of a computer's worth has been the savings it has achieved. Few companies have installed computers "unless there was an off-setting cost benefit" that could be clearly demonstrated, Head asserted. Writing in the Dutch technical publication "Informatie", Head explained that the advanced systems now being developed offer intangible benefits that cannot be measured in terms of dollars saved. The Computer Sciences executive singled out the investment banking field to illustrate his point. In deciding whether to install a management information system, Head said, the question an investment banker should consider is not how much it is worth to "update the portfolios and manage the paper work." Rather, he asserted, the question such a firm should ask itself is, "What is it worth to us to be able to make a better or more judicious selection of an investment portfolio?" Head defined a management information system briefly as a "tool that can be used in organizing information and in presenting information to management." Whereas computers initially were used for routine tasks such as record maintenance, they are now being employed increasingly in "more imaginative and ambitious applications," the CSC executive said.

LOCKHEED MISSILES AND SPACE COMPANY, SUNNYVALE, CAL. HAS ORDERED 15 COMPUTER SYSTEMS FROM THE COMPUTER DIVISION, ELECTRO-MECHANICAL RESEARCH, INC., MINNEAPOLIS, MINN. The multi-million dollar order consists of two EMR ADVANCE 6040 computers serving as masters to ADVANCE 6020 machines. They will be used for checkout of the Poseidon missile. Each 6020 computer will communicate with a number of cathode-ray tube visual display units at testing locations. CRT test stand operators will request test programs to check each corresponding subassembly, assembly, and system during the Poseidon prototype, manufacture, and preflight operations.

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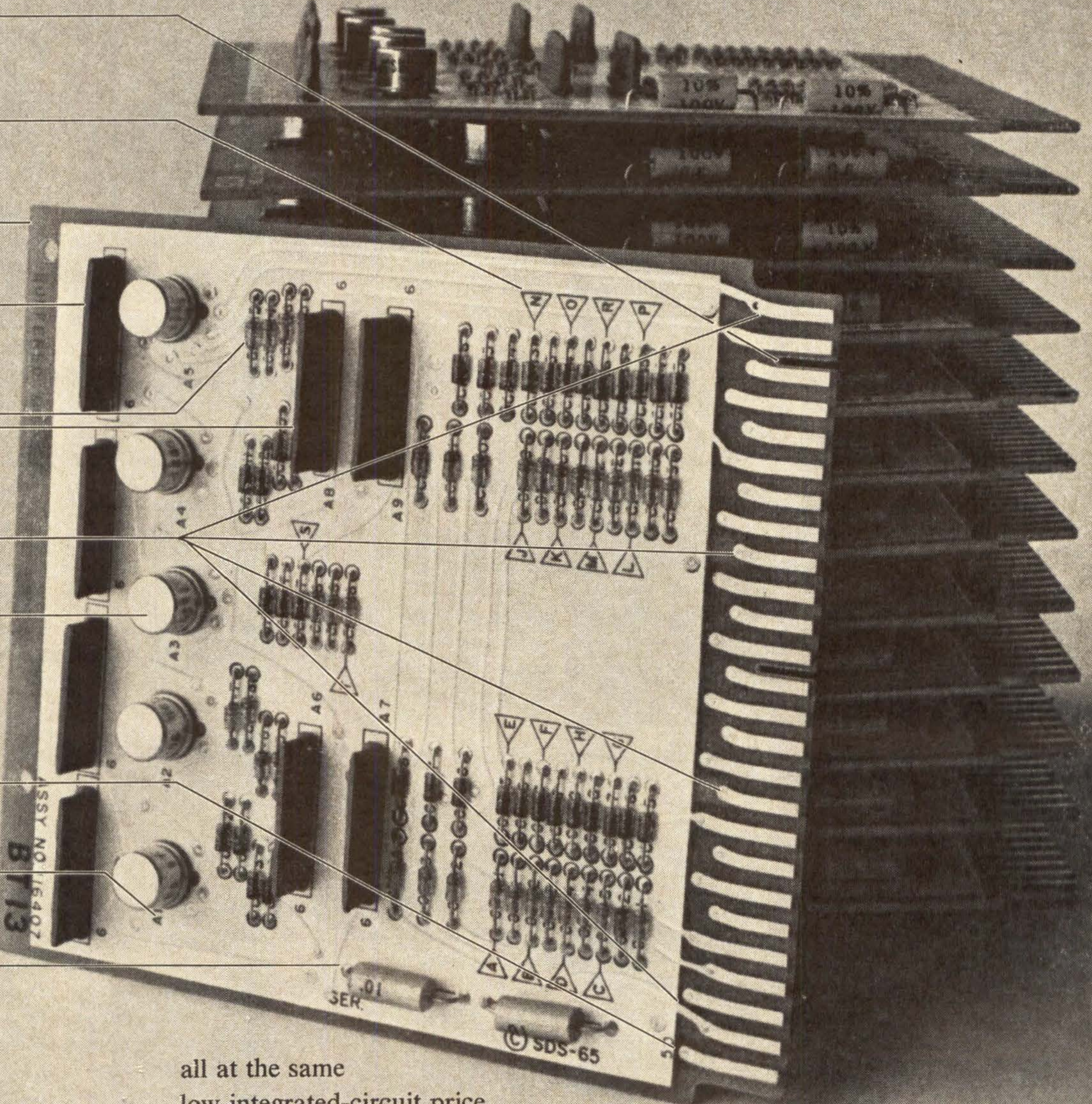

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INDUSTRY NEWS

A BOOKLET BREAKING DOWN THE WORKINGS OF ELECTRONIC COMPUTERS INTO SIMPLIFIED TERMS AND DIAGRAMS IS NOW BEING DISTRIBUTED by the U. S. Atomic Energy Commission. The 56-page publication, "Computers," tells how wires and transistors plus human ingenuity are combined to produce complex machines. It covers the binary counting system, basic electronics, differences between digital and analog computers, and programming. Single copies of "Computers" are available without charge from AEC's Division of Technical Information Extension, P. O. Box 62, Oak Ridge, Tenn. 37830.

LIGHTWEIGHT, AIRBORNE DIGITAL COMPUTERS DEVELOPED FOR DETACHMENT 1 OF THE AIR FORCE AVIONICS LABORATORY BY NORTHROP CORP'S NORTRONICS DIVISION HAVE SATISFACTORILY COMPLETED ACCEPTANCE AND ENVIRONMENTAL TESTS and are currently being integrated into the Holloman low-cost aircraft inertial navigation (locating) system. Nortronics delivered their 3 NDC-1050A integrated circuit computers and control units and displays under an Air Force contract. The NDC-1050A is a low-cost airborne computer, featuring conductive cooling and a random access 2,048-word memory with transient protection to meet requirements of MIL-STD-704 (power input). The computer also is designed to MIL-E-5400 (airborne equipment) specifications. The NDC-1050A contains only two full-sized integrated circuit data registers but it utilizes the first 10 addresses of the main core memory for the accumulator and 12 other working registers. The register contents are made available to the arithmetic and control units during each operation cycle. Input-output data is transferred in a serial mode with word assembly accomplished in the computer program, rather than complex buffering equipment. Nortronics engineers said the economies of serial arithmetic were employed in the computer because of the low cost requisites. This resulted in a 268 KC machine with an add time of 89.5 microseconds, and a multiply time of 835 ms.

GOVERNMENT REPORTS ★★

BREADBOARD MECHANICAL SCANNER

The use of a coherent light to generate a small optical spot for data extraction from a transparency is announced in a report from CBS Laboratories. Using the scanner, a capability of distinguishing 256 lp/mm and 30 shades of grey from light to dark was demonstrated by the developers. The system consists of a laser light source, a beam expander, a beam normalizer, a rotating optical scanning system to cover a 2-inch wide transparency, a transparency holder, a light collector, and a photomultiplier assembly including video amplifier and high-voltage power supply. CBS says these system components are basically off-the-shelf items.

Order from Clearinghouse, U. S. Dept. of Commerce, Springfield, Va. 22151. Order No. AD-628588. Price: $3.00.

ON THE DESIGN AND TESTING OF SELF DIAGNOSABLE COMPUTERS

Study investigates new approach for deriving self-diagnosis programs for digital computers based on only a micro-order description of the computer to be tested without detailed logic information. Approach is made possible by standardizing computer realization techniques by means of a set of design principles which guarantees the existence of a relationship between the behavior of a computer under a large number of failures and alterations of the micro-order specification for that computer. Procedure can be programmed so that the diagnostic programs can be generated by a computer.

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TECHNOLOGY FOR PNP INTEGRATED CIRCUITS

Report describes integrated circuits that are intended for use in code converters for data processing. These PNP integrated circuits are a three-input NOR gate and a flip-flop. During the initial phase of the work, three-input NOR gates were successfully diffused, but rigorous electrical testing disclosed a softening of the collector diodes — believed due to a surface inversion phenomenon within the collector region between the base-collector junction edge and the top-collector contact. A new design was therefore adopted which incorporates a guard ring within the collection ring and which by virtue of its high boron concentration prevents the formation of leakage channels by eliminating surface inversion.

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STANDARDIZATION OF TYPEWRITER FONTS

General Precision's Link Group has completed a program that provides engineering data in support of standardization of typewriter fonts and related features for optical scanning application. Primary emphasis in this program was placed on investigation and evaluation of existing typewriter fonts and includes an evaluation of a type font developed by Subcommittee X3.1 on Character Recognition Under American Standards Association Section Committee X3. Investigations were by computer programmed assessment of each font using a technique developed partly under Air Force contract and partly under continuing Link sponsored character recognition efforts. Evaluations were accomplished by extending the vocabulary capacity of a Link Multifont Page Reader to permit machine reading of a significant volume of typewriter-prepared documents. Reject and error rates were determined in this manner for each of several type styles considered.

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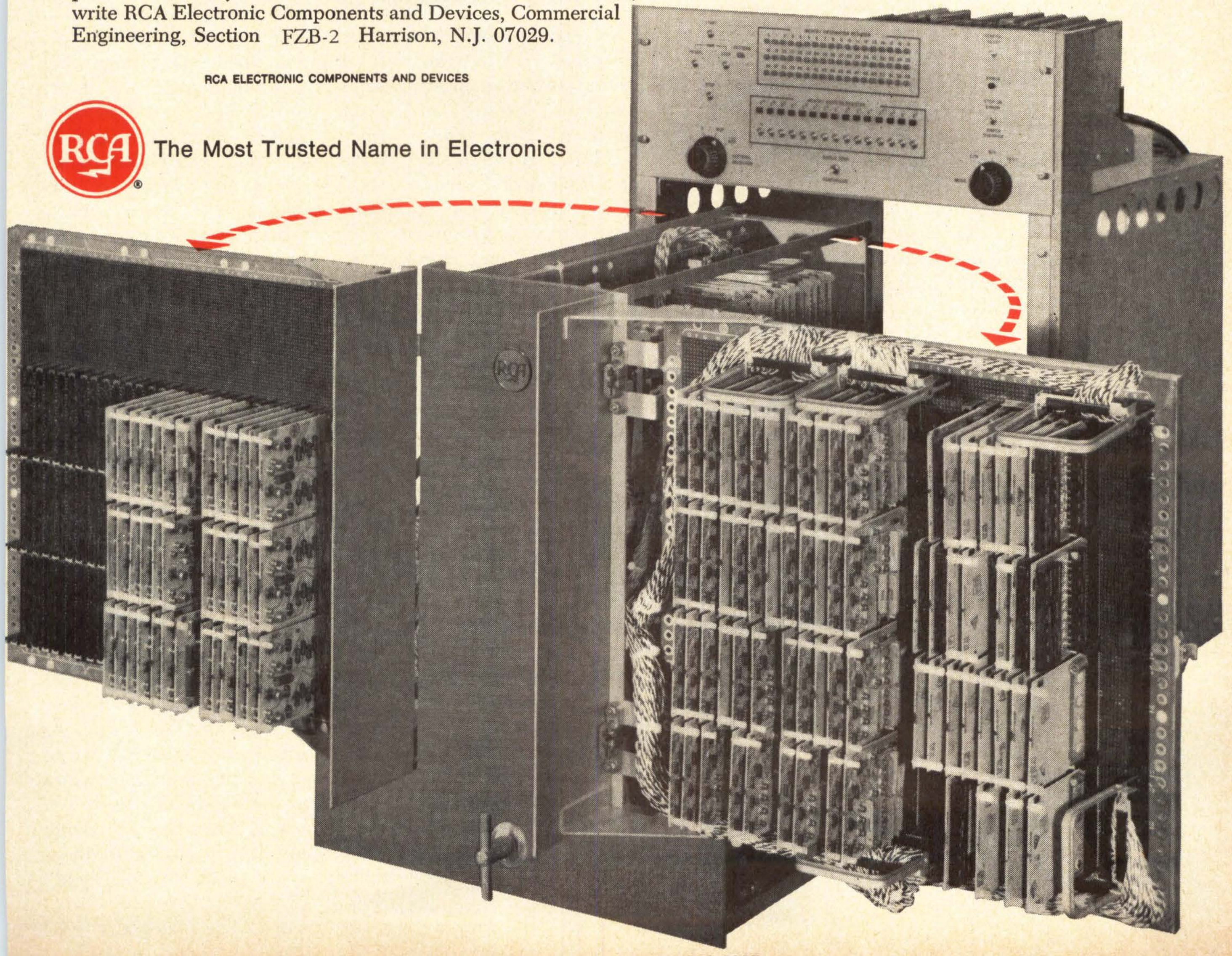


NEW DISPLAY MODULE

Decode and Display Unit Accepts 4-Wire BCD Inputs from Integrated Circuit Logic

A new kind of readout module for displaying 0-9 numerals in response to coded electrical input signals has been developed by Numex, Inc. of Waltham, Mass. The new readout, which has the inherent ability to accept and decode BCD input signals, can be supplied in side-by-side assemblies complete with bezel, frame, and common electronic circuits, to make multi-decade readouts for digital instruments, systems, computers, etc. The first commercial line offered by the company is the R-100 Series, which is designed specifically to display low-signal-level data from integrated circuit systems. Model R-100 averages $50 per decade in sample quantities for 4 decode assemblies. This price is said to compare favorably with other displays designed to read out BCD data from integrated circuits.

New Projection Principles

The NUMEX is a projection readout, and harnesses the image projection principles used in ordinary movie projectors. That is, the image of the numeral to be displayed is mechanically positioned at the focal point of an optical system, which then projects an enlarged view of the numeral onto the viewing screen. The NUMEX is said to differ radically from conventional projection readouts in the method of selecting the image to be displayed. Many conventional projection readouts use a separate light bulb and lens-system for every numeral, and have images of appropriate numerals positioned at the focal-point of every lens. Numeral selection is accomplished by energizing the bulb associated with the desired numeral; the selected bulb then projects the image of the numeral onto the viewing screen. In contrast, the NUMEX uses just one light bulb for all numerals and projects all numerals through a common optical system based on a single high-quality compound lens. A one-inch diameter stainless steel disk, bearing stamped-out numerals 0-9 around its periphery, is mounted so that its edge intercepts the light beam at the focal point of the optical system. Thus, by rotating the disk, numerals 0-9 are brought sequentially to the focal point of the lens causing enlarged numerals to be projected one-after-the-other onto the viewing screen.

The image-bearing disk is actually mounted onto the shaft of a peanut-sized electronically-driven stepping motor which spins the disk until the desired numeral is displayed. Numerals are selected by driving the motor until it has positioned the disk in accordance with the BCD input commands.

The NUMEX readout requires only one power drive circuit (for stepping the motor), whereas most conventional readouts require a power driver for every bulb. Furthermore, the NUMEX drive circuit is active only for a brief period when the display is being updated. Once the correct numeral is in view, motor-drive-pulses are gated off and the motor's magnetic detent action holds the shaft (and numeral-disk) in position.

Another important advantage of the new readout arises from the total absence of bulb-switching. A very large filament, high-power lamp can be used at a low operating temperature. The result is said to be a very long life combined with sufficient brightness to make the readout visible in direct sunlight. If the high current required for these benefits were to be switched, the cost of the ten drivers would be exorbitant, according to the company.

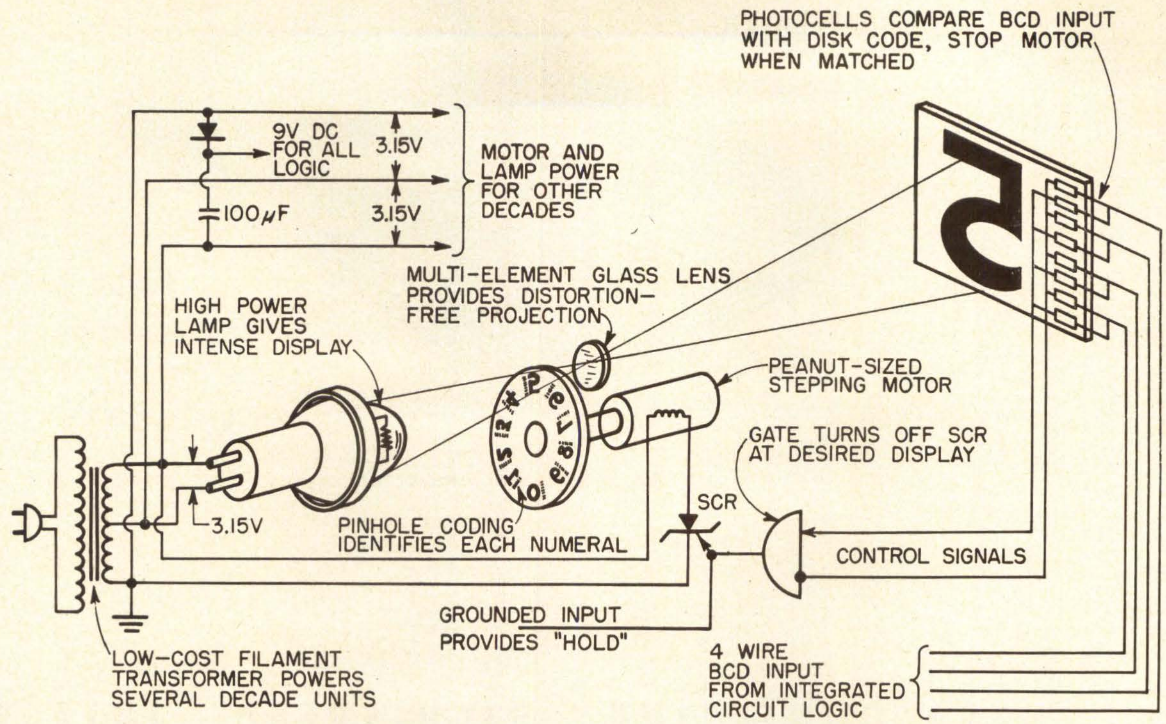
Although not particularly relevant to the Model R-100 readout unit, it is important to note that the use of a stepping motor for numeral control provides the basis for using the NUMEX principle in counting instruments. That is, the motor can be stepped around in accordance with pulses developed by event-monitoring transducers. By equipping every decade with "carry" output pulses, complete multi-decade counters and totalizers can be realized with very little additional hardware.

The decoding principle of the NUMEX operation is that of a digital servo. The stepping motor is pulsed continually when a fresh numeral is called for and, in this way, "tries different numerals for size" until the right one is found. Photocells are used to stop the motor when the displayed numeral matches the numeral specified by the BCD data-input. (This is the null-seeking process upon which all servos are based.)

Key to the NUMEX decoding simplicity is the method of feeding back information about the disk position so as to stop the motor at the correct numeral. Instead of using arrays of silicon diodes in a conventional binary-to-decimal conversion circuit, the NUMEX uses arrays of tiny holes punched in coded patterns alongside the numerals on the image disk. These holes are punched in BCD 8-4-2-1 pattern (other codes are easily substituted) and each set of holes represents, in BCD form, the value of the adjacent decimal numeral.

Light passing through the set of coded holes is projected, along with the numeral image, onto the back of the viewing screen. However, unlike the numeral image, the coded light pattern is not seen by the viewer but, instead, falls onto an array of strategically-placed photocells. The photocells recognize the hole pattern and develop corresponding BCD-coded output signals.

By feeding the coded photocells signals to the NUMEX's internal comparison circuit, the photocell code, representing "what is", can be compared with the input code which represents "what should be." The comparison circuit keeps the motor running until the input and feedback signals are identical, at which point,



further pulses to the stepping motor are shut off. The stepping motor then stops with its detent holding the desired numeral in view until a further updating is required.

No regulated DC power supplies are required by the NUMEX. Instead, one of its very economical features is the ability to operate from a center-tapped 6.3 volt transformer (a mass-produced filament transformer, for example). Drive power for the stepper, bulb power, and supplies for the comparison circuits are all derived from the 6.3 volt input.

According to the company, the fundamental economy of the NUMEX R-100 Series comes from the design principle of literally replacing arrays of silicon decoding diodes with arrays of coded holes punched in the motor-driven disk. Besides eliminating diode costs, the NUMEX principle eliminates the assembly and wiring costs, too. Although the NUMEX does use photocells for reading the optically-encoded disk angles, only 8 photocells are needed for recognizing all BCD codes.

When the NUMEX is used for displaying digital data from high-speed digital computers and other fast logic circuits, an intermediate memory can be built into the NUMEX to avoid tying-up the computer for the 300-millisecond updating period. The auxiliary memory acquires the BCD command in less than 50 ns, frees the computer, and allows the motor to take its own time to reach the new position.

For more information on these new display units:

Circle No. 104 on Inquiry Card.

STANDARD INDUSTRIAL MEMORY SYSTEMS

Three new versions of a standard, low-cost, 10-microsecond memory system include a new hardware design that permits the addition of power supply, counters, level shifters and/or logic modules. Designed for industrial/commercial control data storage applications the 3 versions of the 512 word by 8-bit unit are a half-cycle system, a wired program system, and a BCD addressable system. According to the manufacturer, each of the new systems was designed with a specific application in mind. For example, the half-cycle system, the FX-12/B, offers the advantage of a higher readout or transfer rate making it ideal for pure buffer applications such as data transfer from punched card to magnetic tape. It can also be used in split cycle operations (read-modify-write) thereby reducing the amount of electronics required for counting and signal averaging applications. The FX-12/B is available in three sizes: 512 words by 8 bits, 256 words by 8 bits, and 128 words by 8 bits. Prices range from $1190 for the small size to $1390 for the larger version. The FX-12/W or wired program unit is specifically designed for such applications as code conversion, table look-up, computer programming, machine tool control, and industrial and utility programming. The FX-12/D, claimed to be the first BCD addressable core memory ever offered on the market, is expected to find use wherever interface with decimally-oriented devices is required. All FX-12 Systems include complete timing circuitry, interfacing data registers, sense amplifiers and x, y, and inhibit drivers in addition to the control core matrix. Ferroxcube Corp., Saugerties, N. Y.

Circle No. 260 on Inquiry Card

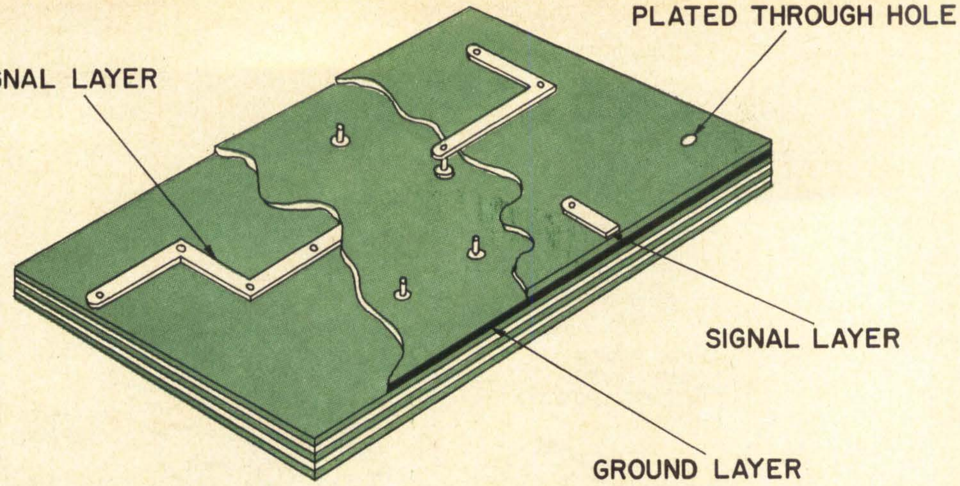


Fig. 1 Sectional view of multilayer PC board

INTERCONNECTING HIGH-SPEED INTEGRATE

A multilayer printed circuit board is described as the state-of-the-art method of achieving dense interconnections of integrated circuits. Electrical considerations involved in the design of multilayer boards are discussed and the effects of these considerations upon critical dimensions of the boards are quantitatively presented.

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Advisory Engineer,
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Bethesda, Maryland

Contemporary integrated circuits provide the user with a relatively high circuit density at the first level package. Typically, three logic circuits are contained in commercially available 14-lead flat packs measuring approximately 0.250 x 0.250 x 0.100 inches. The integrated circuits presently available exhibit raw logic circuit turn ON and turn OFF delays of as little as two to three nanoseconds. These attributes provide the user with the capability of designing a high-speed system, provided he can develop a second level package which will interconnect first level packages with minimal line lengths and with minimal signal distortion.

One of the most attractive means of providing high density interconnections is the multilayer printed circuit board. This consists of several layers of epoxy glass insulation clad with copper on both sides. The copper is etched to provide the desired networks on each side. The resulting etched boards are then combined with insulating layers, and laminated with a bonding agent to form the multilayered printed circuit board. Connections between layers are achieved by drilling holes through the laminated board and electroplating the inside of the holes with copper. Contact is then made with copper lines that have been exposed to the plating material. See Figs. 1 and 2.

The multilayer printed circuit board provides interconnecting lines which are dimensionally well controlled within a homogeneous medium. A signal line on one layer and a parallel return on another layer constitute a transmission system with fairly well defined characteristics,

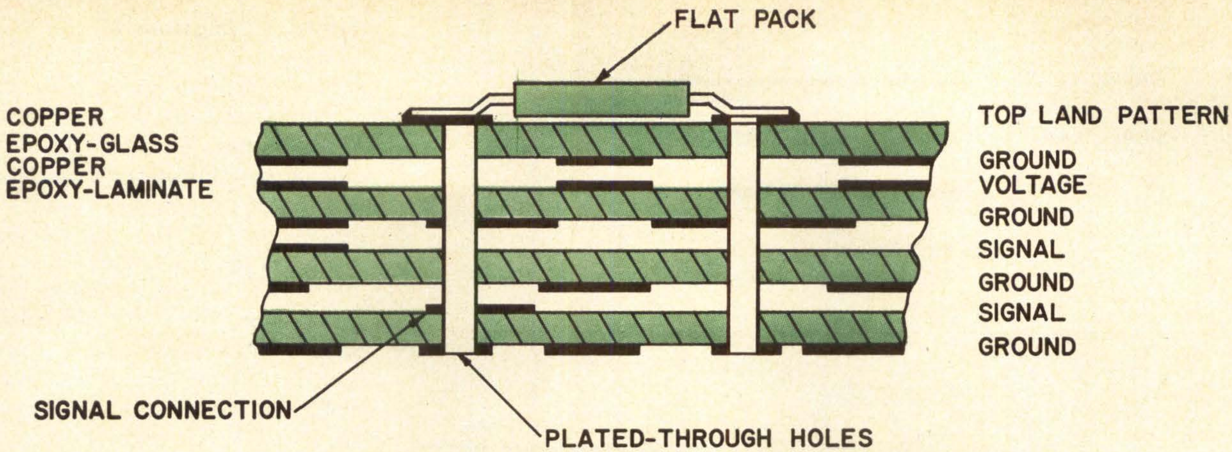

Fig. 2 Cross-sectional view of multilayer PC board

IRCUITS WITH MULTILAYER BOARDS

and it is possible to predict the electrical properties of this system. The remainder of this article describes the considerations involved in choosing the electrical characteristics of the interconnections in terms of the properties of the integrated circuits to be interconnected, and the ease with which the multilayer printed circuit board may be manufactured.

Assignment of Layers

The multilayer printed circuit board provides several stacked layers of copper separated by insulating material. These layers may be etched to form signal lines or they may be left mostly intact to provide a copper plane. Copper planes provide an excellent means of distributing power supply voltages to the integrated circuits through a low impedance path from the power supply terminals or decoupling capacitors; they may also be used as intervening shields between signal layers.

An example of a multilayer board with layer assignments is given in Fig. 2. The top surface provides interconnection between the flat pack leads and the plated-through holes. The second, third, and fourth layers are copper planes which provide low impedance paths for distributing the power supply voltage and ground to the integrated circuits. Also, noise that may appear on the voltage plane due to imperfect decoupling is isolated from the signal layers by the adjacent ground planes. The fifth, sixth, seventh, and eighth layers are alternate signal and ground layers. Notice that the signal lines which are contained within the bottom layers are of triplate construction; i.e., the lines are sandwiched equidistant between two ground planes. The ground planes shield signal lines on different layers from cross-coupling. They also insure uniform electrical characteristics of the individual lines so that they act as transmission lines with a characteristic impedance, Zo.

Characteristic Impedance

The characteristic impedance (Zo) of a transmission line is best determined by measurement.[1] However, the Zo of lines with negligible losses may be expressed in terms of the dielectric constant of the insulation and the capacitance per unit length:[2]

$$Zo = \sqrt{\frac{L}{C}} = \frac{1}{Cv} = \sqrt{\frac{Kr}{cC}} \qquad (1)$$

where L = inductance per unit length, C = capacitance per unit length, v = velocity of propagation, c = velocity of light, and Kr = relative dielectric constant of the insulation.

The problem of determining Zo therefore reduces to one of calculating the capacitance per unit length of signal line, given the cross-sectional dimensions of the multilayer boards. The cross-section of Fig. 3 is a simplified illustration of a tri-plate conductor configuration which occurs in practice. For example, if copper is used for the conductor, the edges will not be square but tapered in from the top; also, the conductor may not be placed exactly in the center between the two ground planes. However, the configuration of Fig. 3 can provide a sufficiently accurate illustration for studying the tradeoffs involved in the selection of Zo versus the board dimensions.

The capacitance, in picofarads per inch, of the signal line of Fig. 3 may be calculated by modifying the width of the conductor to take into account the fringing of the field at the edges, and then determining the parallel plate capacitance of the conductor of modified width. The width of the conductor is increased by an amount determined from the following equation:[3]

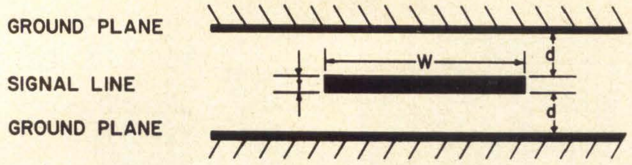

Fig. 3 Tri-plate construction

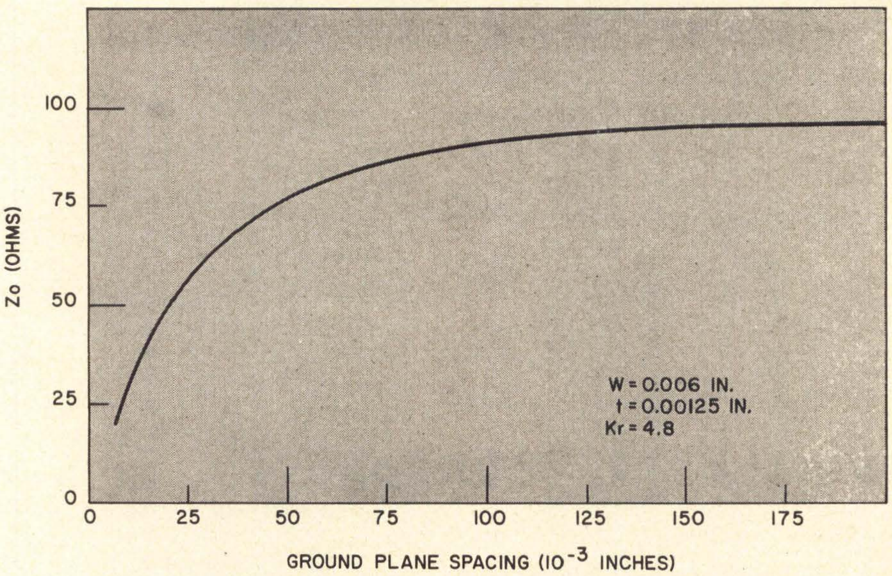

Fig. 4 Zo vs. ground plane spacing

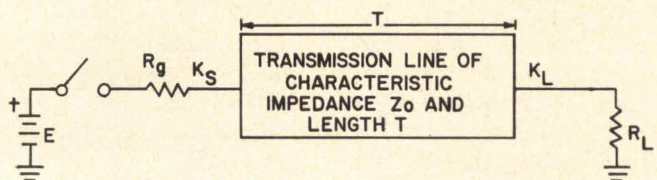

Fig. 5 Equivalent circuit

$$\Delta W = \frac{4}{\pi}\left[(d + t/2)\ \ln \frac{2d + t/2}{d} - \frac{t}{2} \ln \frac{(t/2)\ (2d + t/2)^{1/2}}{d}\right] \quad (2)$$

and the capacitance in picofarads per inch is then determined by:

$$C = \frac{Kr}{4.45}\ \frac{(W + \Delta W)}{d} \quad (3)$$

where the variables are as shown in Fig. 2.

In practice, minimum line width and thickness are limited by physical considerations. For example, epoxy glass laminates clad with one ounce (0.00125 inch thick) electrolytic copper is commonly used as the base laminate of the multilayer board. The copper may be reliably etched to form a minimum line width of 0.006 inch. The base laminate is available in a wide variety of thicknesses, the thinnest being 0.002 inch. The relative dielectric constant of epoxy glass laminates and bonding agents is approximately 4.8. Zo is shown in Fig. 4 as a function of ground plane spacing (2d + t in Fig. 3) for W = 0.006 inch, t = 0.00125 inch, and Kr = 4.8. Note that a Zo above approximately 80 ohms becomes dimensionally unattractive. For example, the multilayer board of Fig. 2 would be approximately 0.044 inches thick if 36 ohm lines were used, but 0.289 inches thick if 80 ohm lines were used.

Signal Propagation

The propagation delay between two computer circuits will be determined by the output impedance of the driving circuit, the input impedance of the load circuit, the characteristic impedance of the interconnecting line, and the line length. The circuit of Fig. 5 is representative of the equivalent circuit for a source and load interconnected by a transmission line. Once the switch closes the voltage at any time, at either the load end or the source end of the line, may be determined by adding the reflections which have occurred up to that time. The delay of the line (T) is simply the length of the line divided by the velocity of propagation of a wavefront along the line; this delay is often referred to as the electrical length of the line. The velocity of propagation is the velocity of light divided by the square root of the relative dielectric constant of the insulating medium $(c/\sqrt{Kr})$, as implied by Eq. (1). The magnitude of the reflections at the source and load ends of the line are dependent upon the mismatch of the source and load impedances with respect to Zo, as described by the reflection coefficients at the source and load, K_S and K_L. The reflection coefficients are determined from the following equations:

$$K_L = \frac{R_L - Zo}{R_L + Zo} \quad (4)$$

$$K_S = \frac{R_g - Zo}{R_g + Zo} \quad (5)$$

Initially, as the switch is closed, the source sees a load of Zo, and the initial voltage at the source is:

$$Vi = E\,\frac{Zo}{Zo + R_g} \quad (6)$$

Until time 1T, the load does not know that the voltage at the source has changed, and the output will remain at 0V. At 1T the load receives the incident wave which is acted upon by the reflection coefficient K_L to produce a voltage at the load of $Vi + K_LVi$. The reflected portion of the incident wave (K_LVi) is then transmitted back to the source where at time 2T the source voltage will change to $Vi + K_LVi + K_SK_LVi$. The reflected portion (K_SK_LVi) is then transmitted back to the load and at time 3T the load voltage becomes $Vi + K_LVi + K_SK_LVi +$

$K_S K_L^2 Vi$. This process keeps repeating until the steady state voltage of ER_L / $(R_g + R_L)$ appears at both ends of the line.

The following four examples illustrate possible waveforms. For further examples, see reference 4. All of the following four examples assume a unit step function input from the battery and switch in Fig. 5, and Zo is 50 ohms. For the first example, $R_g = 0$ and $R_L = \infty$, yielding $K_L = +1$ and $K_S = -1$. The resulting source and load waveforms are shown in Fig. 6. In the second example (Fig. 7) $R_g = 0$ as in the first example, but the line is matched at the load end (R_L = 50 ohms) yielding $K_L = 0$ and $K_S = -1$. In the third example (Fig. 8) the line is matched at the source end (R_g = 50 ohms) but $R_L = \infty$, yielding $K_S = 0$ and $K_L = 1$. The final example illustrates the case where the source impedance is much larger than Zo. In this example (Fig. 9) R_g = 500 ohms, $R_L = \infty$, yielding $K_S = 0.818$ and $K_L = 1$.

The steady state voltage at both the source and load ends of the line is one volt in all of the above examples. The waveforms of Fig. 9, however, very closely approximate an exponential function of the form $e/E = 1 - \exp(t/\tau)$, if τ is replaced by 10T, and E = 1V. The example of Fig. 9, therefore shows that if the impedance of the source is much greater than the characteristic impedance of the line, the waveforms at both ends of the line may be approximated by an exponential function with a time constant $\tau = R_g Ct$. If the Zo of the line is known, Ct may be determined by multiplying the capacitance per unit length of the line by the length of line. The line, therefore, appears as a lumped capacitance load of Ct at the generator output. The lumped capacitance approximation is not applicable to the first three examples where the generator is capable of driving the characteristic impedance of the line beyond 10% of the signal swing; i.e, Vi is much greater than 0.1E.

Review of Reflection Conditions

If the output impedance of the logic circuit is comparable to the characteristic impedance of the interconnections, and if the unloaded rise

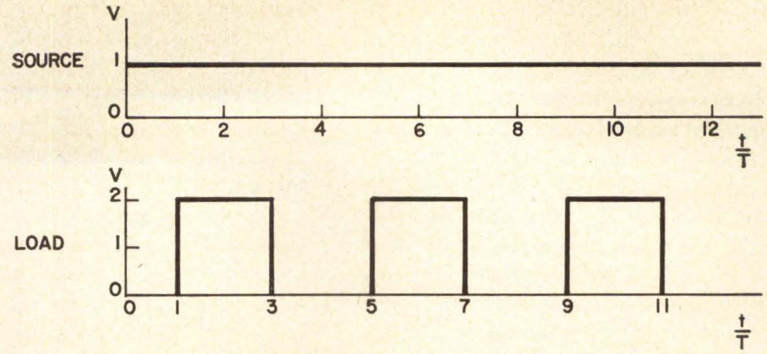

Fig. 6 Zero-impedance step-function generator driving an unterminated line

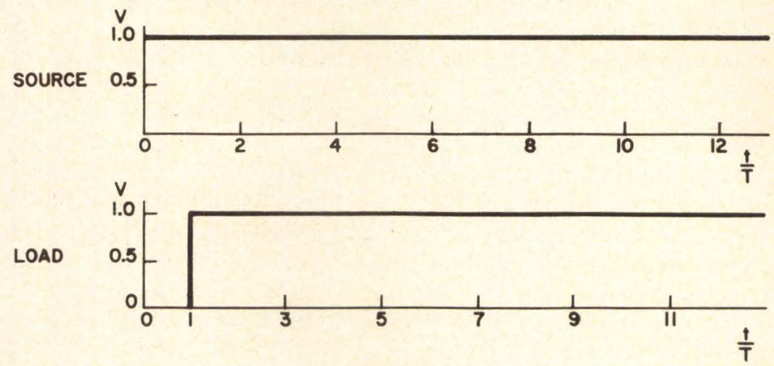

Fig. 7 Zero-impedance step-function generator driving a line terminated in Zo

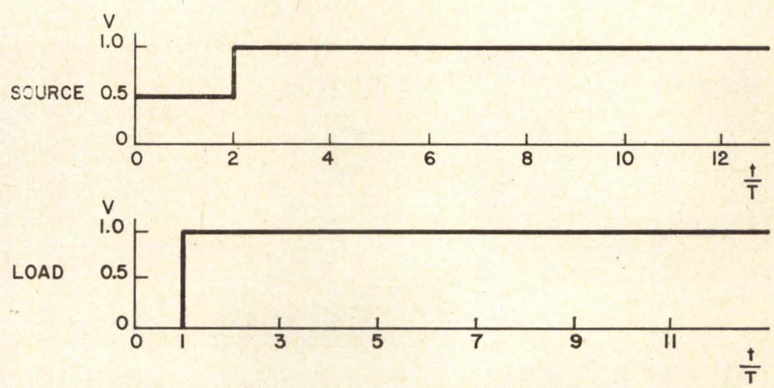

Fig. 8 Step-function generator of impedance Zo driving an unterminated line

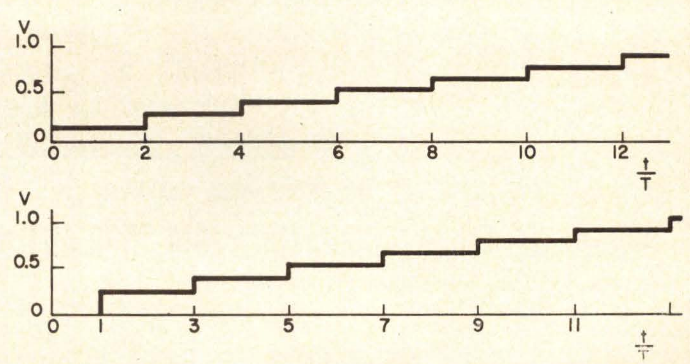

Fig. 9 Step-function generator with source impedance of 500 ohms driving an unterminated line

time of the circuit is less than or comparable to the electrical length of probable interconnecting lines, the circuit waveforms become very dependent upon proper line terminations. If the line is terminated at the load end in a value higher than Zo, and if the source impedance is lower than Zo, a waveform similar to that of Fig. 6 will result. Assuming that $0 < R_g < 50$ ohms and $50 < R_L < \infty$ ohms, the oscillations at the load will eventually diminish to zero. However, it may take several oscillation periods (depending upon the degree of mismatch) before the load waveform has stabilized sufficiently to hold the receiver circuit at the desired state. Thus, the resulting propagation delay may be many times the electrical length of the line.

In the second example (Fig. 7), the source has the capability of developing the full required signal swing across the characteristic impedance of the line. Also, the line is properly terminated such that no reflections occur at the load end of the line. This network provides the least delay between source and load. The voltage source with $R_g = 0$ may be replaced by its Norton Equivalent of a current generator capable of furnishing 20 ma, and the waveforms at the source and load would remain the same.

The waveform of example three (Fig. 8) is identical to that of example two at the load end of the line. However, the source end does not reach steady-state until a time equal to twice the electrical length of the line. This would cause added delay to any circuits that happened to be connected near the source.

Choosing Zo

If one concludes that proper termination is required at the load end of the line in order to realize the potential of high-speed integrated circuits, he must then select a Zo which results in the best compromise between ease of fabrication and circuit requirements. Obviously, the power required of the circuit to drive a terminated line is proportional to the square of the signal swing and inversely proportional to Zo. Therefore, the circuit should be designed with the least possible signal swing which will result in reliable operation. Also, from a power standpoint, Zo should be selected as high as possible. However, there are some pitfalls in choosing Zo too high.

Consider, first of all, the effect of terminating the transmission line in an impedance somewhat higher than Zo. For example, if a logic circuit were available with a one volt signal swing and 10% noise margin, the reflected signal at the load could dip to 0.9V without a deleterious effect upon the operation of the load circuit. A value for the terminating resistor, R_L, which would result in a maximum of 10% undershoot in the output waveform may be determined by allowing the load voltage on the line from time 3T to 5T to be 0.9V and solving for K_L.

For example:

$$0.9 = (1 + K_L + K_L K_S + K_L^2 K_S) V_i \qquad (7)$$

Given that $R_g = 0$ and $Zo = 50$ ohms and the signal swing is 1V, $K_S = -1$ and K_L, as determined from Eq. (7), is ± 0.316. Since the positive value for K_L is of interest, R_L may be determined from Eq. (4) to be 96.5 ohms. Thus, the output waveform is satisfactory for reliable switching of the load circuit even if the line is terminated in almost twice the characteristic impedance of the line. An additional bonus may be derived from the overshoot of the incident wave, which will initially overdrive the load circuit.

Another consideration in selecting the Zo of interconnecting lines is the loading effects of integrated circuits distributed along the line. Up to this point, we have been concerned with just one source and one load. However, in a practical system, the source must be capable of fanning out to more than one load. Although the DC input resistance of a logic circuit may be high in comparison to Zo, the capacitance at the input terminals to the integrated logic circuit may be comparable to the capacitance of an inch or more of line. The net effect of distributing loads along the line is to decrease the characteristic impedance of the line. This presents an argument for keeping logic circuit input capacitance as low as possible and also for selecting a

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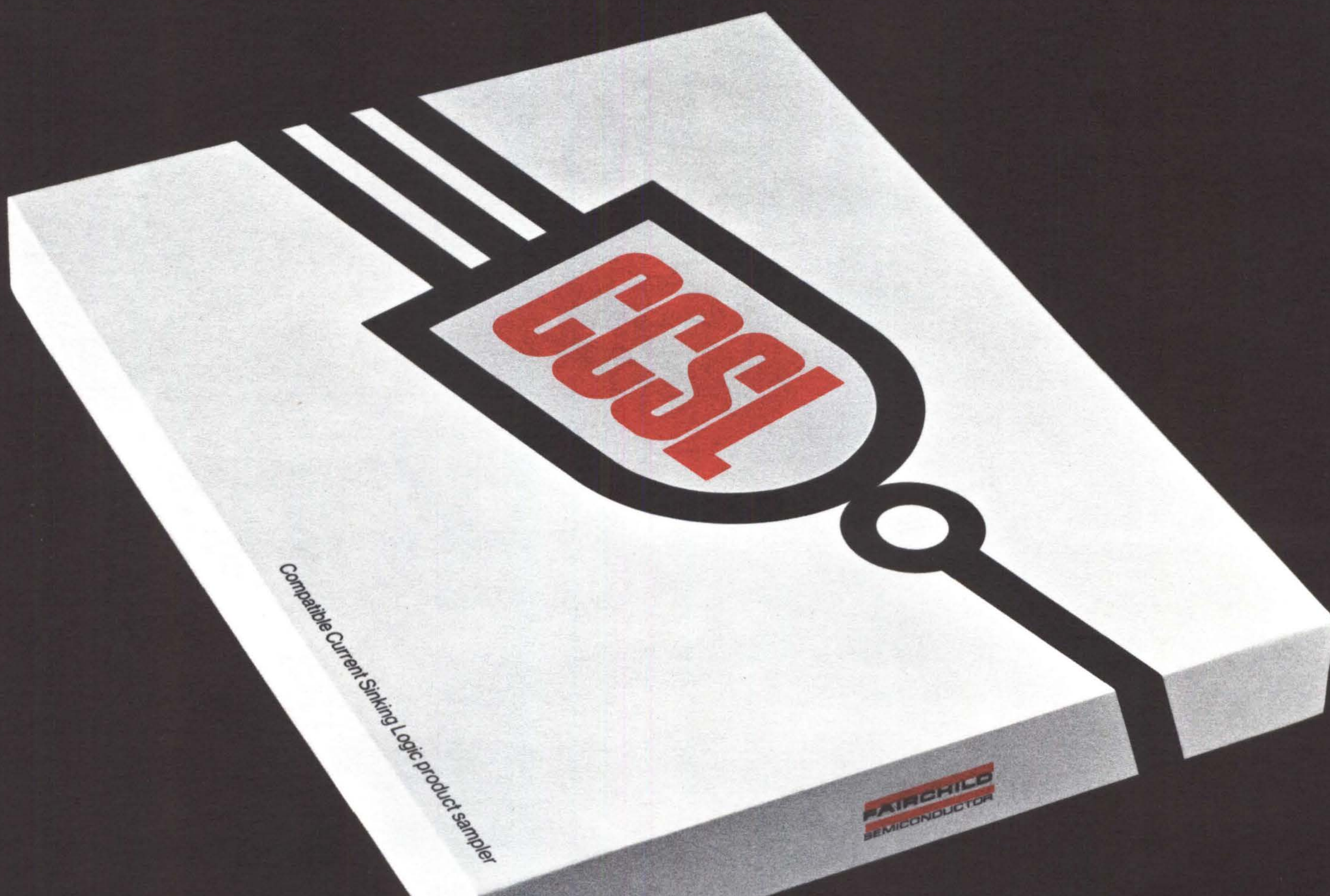

Integrated circuits are conventionally classified by family, and within each family by function. This method of classification restricts you to a single family within a system. Now Fairchild allows you to cross family boundaries and to design by function, selecting circuits from compatible logic families. This permits you to choose the best circuit for each function, and to optimize the system as a whole.

What is compatible logic? Fairchild classifies all digital integrated circuits into compatible logic groups: current sinking logic, current sourcing logic, and current mode logic. A current sinking logic gate (for example, a DTL gate) draws current into its output ("sinks" current) when in the low state, and draws virtually no current when in the high state. A current sourcing gate (for example, an RTL gate) drives current out of its output in the high state and, except for minor leakage, drives no current in the low state. Current mode logic can draw or drive current.

Compatible current sinking logic: There are three families within the Fairchild current sinking group: TTμL (Transistor-transistor Micrologic), DTμL (Diode-transistor Micrologic®) and LPDTμL (Low-power diode-transistor Micrologic) integrated circuits. By crossing family boundaries within the compatible logic group, you can optimize your system design. Here's how:

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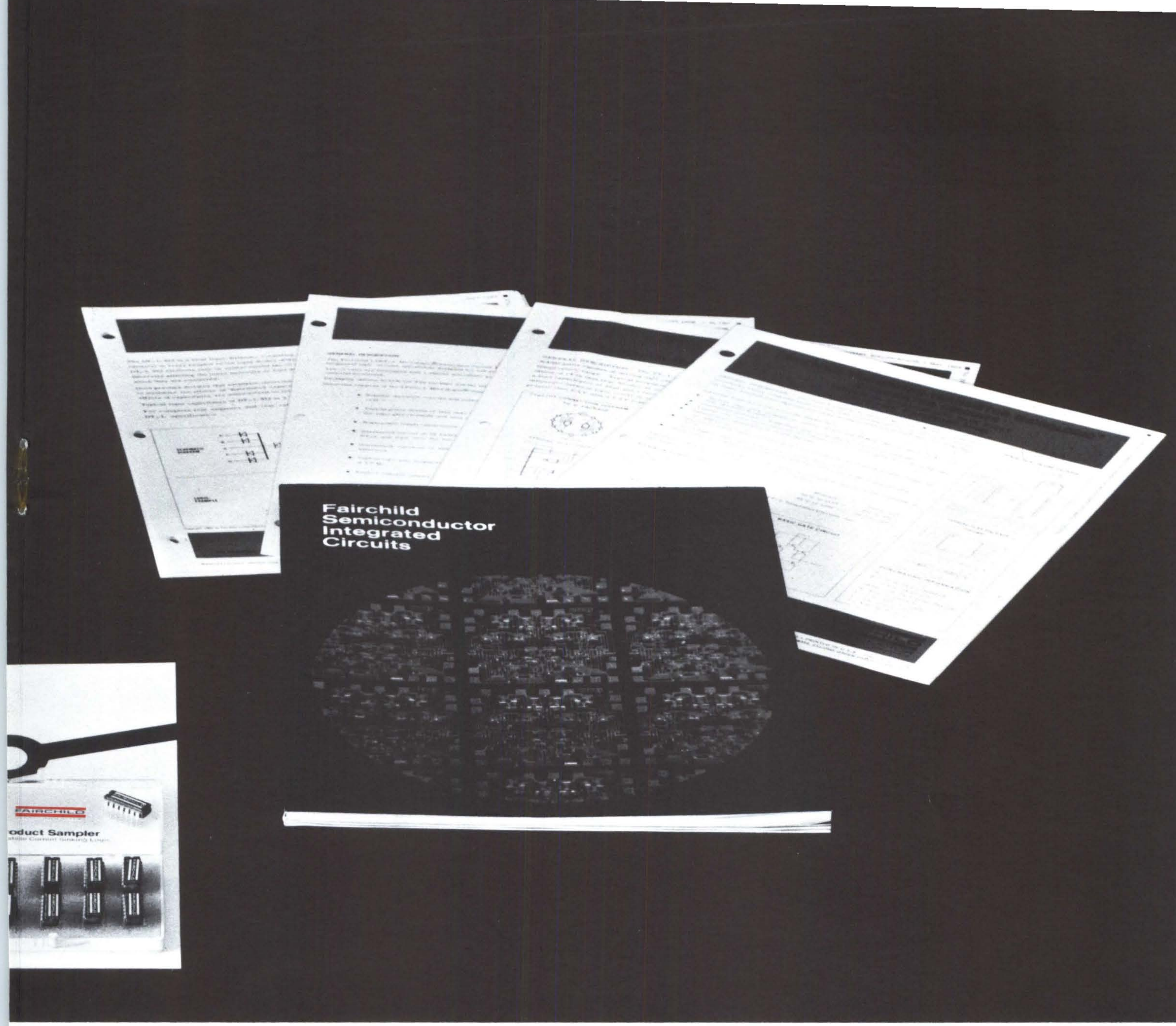
What we mean by compatibility: All three families use NAND logic, and all basic NAND logic functions are available in any of the three forms. All three families use a single 5V



power supply, and all three are guaranteed to perform compatibly when the specified fan-out and fan-in rules for inter-connecting between logic forms are observed. Pin configurations for the same functions are the same, and all three families come in the same two package configurations (maximum-density ¼" x ¼" Flatpak, and easy-to-handle Dual in-line). Finally, all three families are manufactured using the same technology, so that within the same working environment they will maintain a uniform stability over a period of time.

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Compatible Current Sinking NAND Logic Summary

Number and function	Typical Specifications at 25°C Free Air Temperature			
	Noise Immunity	Propagation Delay	Power Dissipation	Fan-out
TTμL				
9000 Clock-gated J-K flip-flop	1 volt	25nsec.	45mW	10
9001 Clock-gated J-K flip-flop	1 volt	25nsec.	45mW	10
9002 Quad 2-input gate	1 volt	10nsec.	12mW	12
9003 Triple 3-input gate	1 volt	10nsec.	12mW	12
9004 Dual 4-input gate	1 volt	10nsec.	12mW	12
9005 Dual AND/OR/NOT gate	1 volt	12nsec.	12mW	12
9006 Dual 4-input extender		4nsec.		
9007 8-input gate	1 volt	10nsec.	12mW	12
9008 Quad 2-input AND/NOR gate	1 volt	12nsec.	12mW	12
9009 Dual 4-input buffer	1 volt	15nsec.	22mW	30
DTμL				
9111 Parallel-gated clocked flip-flop	1 volt	40nsec.	48mW	8
9930 Dual 4-input gate	1 volt	25nsec.	8mW	8
9931 Clock-gated flip-flop	1 volt	50nsec.	20mW	7
9932 Dual 4-input buffer	1 volt	35nsec.	35mW	25
9933 Dual 4-input extender				
9936 Hex inverter	1 volt	25nsec.	48mW	8
9937 Hex inverter	1 volt	20nsec.	72mW	6
9941 Monostable multivibrator	1 volt	25nsec.	35mW	10
9944 Dual 4-input power gate	1 volt	40nsec.	20mW	27
9945 Clock-gated flip-flop	1 volt	50nsec.	42mW	9
9946 Quad 2-input gate	1 volt	25nsec.	32mW	9
9948 Clock-gated flip-flop	1 volt	40nsec.	48mW	8
9949 Quad 2-input gate	1 volt	20nsec.	48mW	5
9950 High speed gated flip-flop	1 volt	20nsec.	50mW	10
9951 2-input monostable multivibrator	1 volt	25nsec.	35mW	10
9961 Dual 4-input gate w/extender	1 volt	20nsec.	24mW	6
9962 Triple 3-input gate	1 volt	25nsec.	24mW	8
9963 Triple 3-input gate	1 volt	20nsec.	36mW	6
LPDTμL				
9040 Clocked flip-flop	1 volt	180nsec. (Output going positive) 90nsec. (Output going negative)	4mW	10
9041 Dual 3-input gate	1 volt	65nsec.	2mW	10
9042 Dual 3-input gate	1 volt	65nsec.	2mW	10
9043 Three and 4-input gate w/extender	1 volt	65nsec.	2mW	10
9044 Dual 4-input gate w/extender	1 volt	65nsec.	2mW	10
9046 Quad 2-input gate	1 volt	65nsec.	2mW	10
9047 Triple 3-input gate	1 volt	65nsec.	2mW	10

Contents of Sampler Kit

Qty.	PART No.	Description	PRICE 1-99 each
4	9000	J-K flip-flop	$ 5.10
2	9002	Quad 2-input gate	$ 3.65
2	9946	Quad 2-input gate	$ 3.65
2	9046	Quad 2-input gate	$20.00

These products are in the industrial temperature range.

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low Zo such that the line with distributed loads does not significantly differ in Zo as compared to a line loaded at just the receiving and/or sending ends.

The last consideration in selecting Zo is the cross-coupling between parallel signal lines within the same plane. In order to achieve the highest possible wiring density, it would be desirable to allow parallel lines to be as closely spaced as physically possible. However, for a given maximum coupling between adjacent parallel lines, the allowable conductor spacing will be a function of the distance between ground-planes of the triplate structure, or the Zo of the lines.

Fig. 10 shows the relationship of Zo, conductor edge-to-edge spacing, and cross-coupling between parallel signal lines. For any given Zo in Fig. 10, conductor spacings less than the one given by the curve will result in greater than 1% maximum coupling between parallel lines. The results of Fig. 10 were calculated for line widths of 0.006 inch etched from one ounce copper of 0.00125 inch thickness with epoxy glass insulation with a relative dielectric constant of 4.8. These calculations are based upon Reference 5, Eq. (22), which is based upon lines of infinitesimal thickness correction for lines of finite thickness was approximated by adjusting for the ground plane spacing of Fig. 4 for a given Zo. Therefore, for a given Zo, the ground plane spacing may be determined from Fig. 4 and the spacing of parallel conductors from Fig. 10. Review of Figs. 4 and 10 demonstrates that large values of Zo not only increase the volume of the multilayer board in the vertical direction but also horizontally.

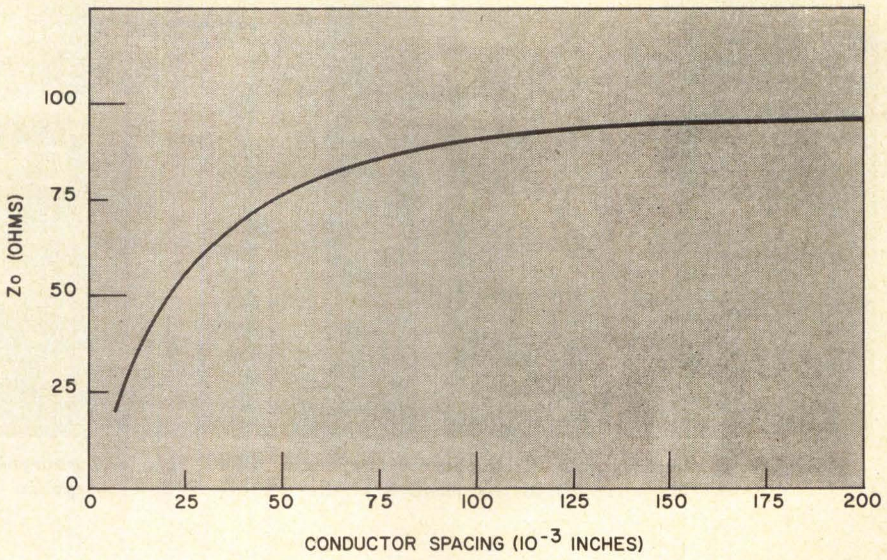

Fig. 10 Zo vs. conductor spacing for 1% cross-coupling

Summary

As computer circuit delays approach 5ns and under, more attention must be given to the method of interconnection. A multilayer printed circuit board has been briefly described as the state-of-the-art approach to integrated computer circuit interconnection. Electrical properties of the multilayer board have been defined in terms of materials in common use today. Also, evaluation of these electrical properties has yielded some conclusions concerning circuit properties necessary to obtain small circuit delays when applied to the system.

To obtain the density of interconnection which is compatible with the circuit density available at the integrated circuit flat-pack level, characteristic impedances of 20 to 50 ohms are realistic. Impedances within the above range result in a thickness of the triplate structure of 0.020 inch or less, so that many of these may be stacked to obtain enough signal layers to insure containment of all nets within a board thickness of less than 0.100 inch — a reasonable design goal. Also, parallel conductors within one plane may be separated by 0.020 inch with less than 1% cross-coupling between lines. This would allow up to 38 channels for signal lines, per inch of board.

High speed computer circuits, therefore, should be designed with 20 to 50 ohm impedance interconnecting lines in mind. This means that driver circuits should be available for driving all lines which are longer than the limit set by the logic circuits, e.g., 2 feet for a 10ns circuit. A driver circuit is practical for the 10ns range logic circuit family because only a few lines would extend over 2 feet in length. However, 5ns circuits would require termination of lines 1 foot or longer, and six inches would look like a long line to a 2ns circuit. In the sub-5ns-delay range, it becomes very desirable to design the capability to drive terminated lines into the basic logic circuit. In order to design this capability into the circuit without creating problems of high power density, circuits with small signal swings are necessary.

Multilayer printed circuit board technology offers the possibility of well-controlled signal transmission, but requires the electrical designer to work within the constraints of the mechanical technology. Ultimately, it is left to the individual designer to choose his own compromise between signal swing, power dissipation, propagation delay, noise tolerance, signal cross-coupling, and packing density.

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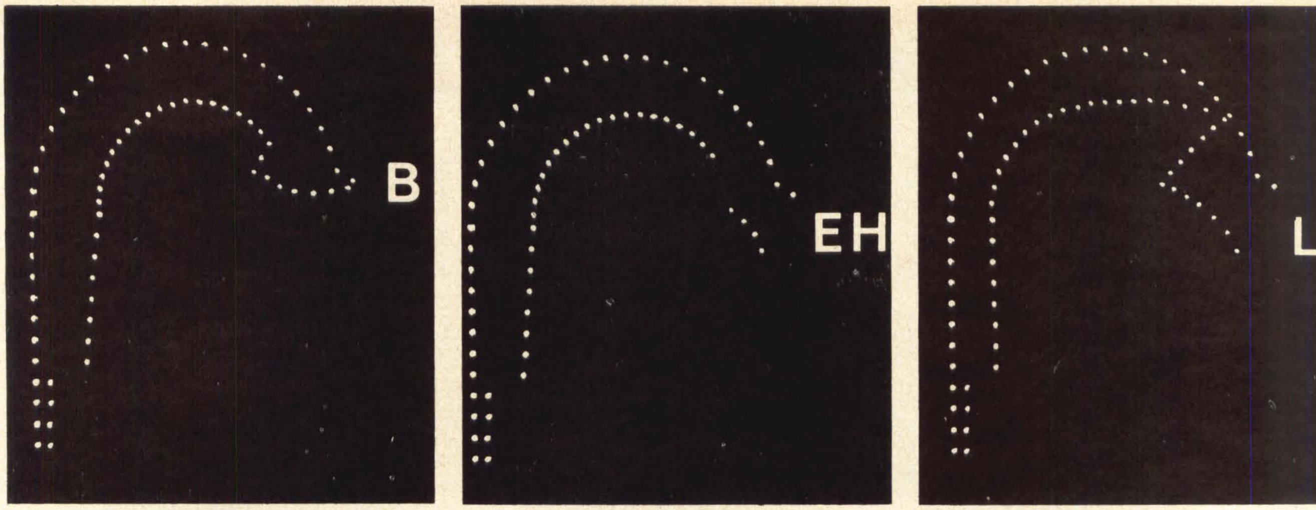

A computer-generated display of the vocal tract shows the changes in the position of the tongue, lips, and pharynx on an oscilloscope as the word "Bell" is spoken.

R & D Reports

A SOUND COMPUTER

Computer-generated Model Creates Speech Sounds

Accurate synthetic speech is now being produced with the aid of a controllable, computer-generated model of the vocal tract developed at Bell Telephone Laboratories. The model, stored in a computer, is actually a geometric description of vocal tract areas as they are shaped to produce various sounds. When synthesizing speech, a researcher can see an outline of the vocal tract displayed on an oscilloscope and, at the same time, hear the sound which corresponds to the displayed shape. By flicking switches and turning knobs at a computer console, the researcher can change the shape and sound simultaneously. Thus, synthetic speech can be improved with both visual and aural aids.

In order to synthesize whole words or syllables realistically, transitions are needed between basic sounds. Shapes corresponding to basic sounds are defined by the researcher at the console. The computer then can automatically interpolate sequences of transitional shapes between one basic shape and another. These sequences correspond to the motions of the human vocal tract when full words are produced. Because the model is similar to the vocal tract, more realistic sounds can now be made with a comparatively simple set of transition rules. Previously, synthesis of transitions was more complicated.

Research of this type is conducted at Bell Laboratories to obtain basic information about speech sounds. Eventually this information may be useful in devising a more efficient means of encoding speech signals and transmitting them over communications lines. It also may help in the development of a practical speaking machine for reading-out data stored-in, or generated by, computers.

In the new vocal tract model, a computer calculates the transmission characteristics of the displayed vocal tract shape and supplies signals corresponding to these characteristics to a speech synthesizer — a device which converts the signals into sound.

The model was designed to fit previously-available data on the areas of the human vocal tract. This data was obtained from X-rays of individuals uttering basic sounds. Vocal tract areas are described in the computer program by five variables. The tongue is represented by a simple arc. Two parameters indicate the position of the tongue (up-down and forward-backward) within a larger, fixed outer arc representing the palate and pharyngeal wall. A third variable indicates the position of the tongue tip — either raised (as it would be when pronouncing "L") or tucked (as it would be when prouncing "Ah").

Area measurement of the lower part of the pharynx (represented by straight lines connected to the bottom of the arcs depicting the tongue and palate) is related directly to the tongue position and is not included as an independent variable. The fourth and fifth parameters are taken from the extent of opening and protrusion of the lips.

Details of the new technique were revealed recently by Dr. C. H. Coker of Bell Laboratories, Murray Hill. New Jersey, at a meeting of the Acoustical Society of America in Los Angeles. The paper was co-authored by Professor O. Fujimura of the University of Tokyo who had worked on the model as a consultant to Bell Laboratories. END

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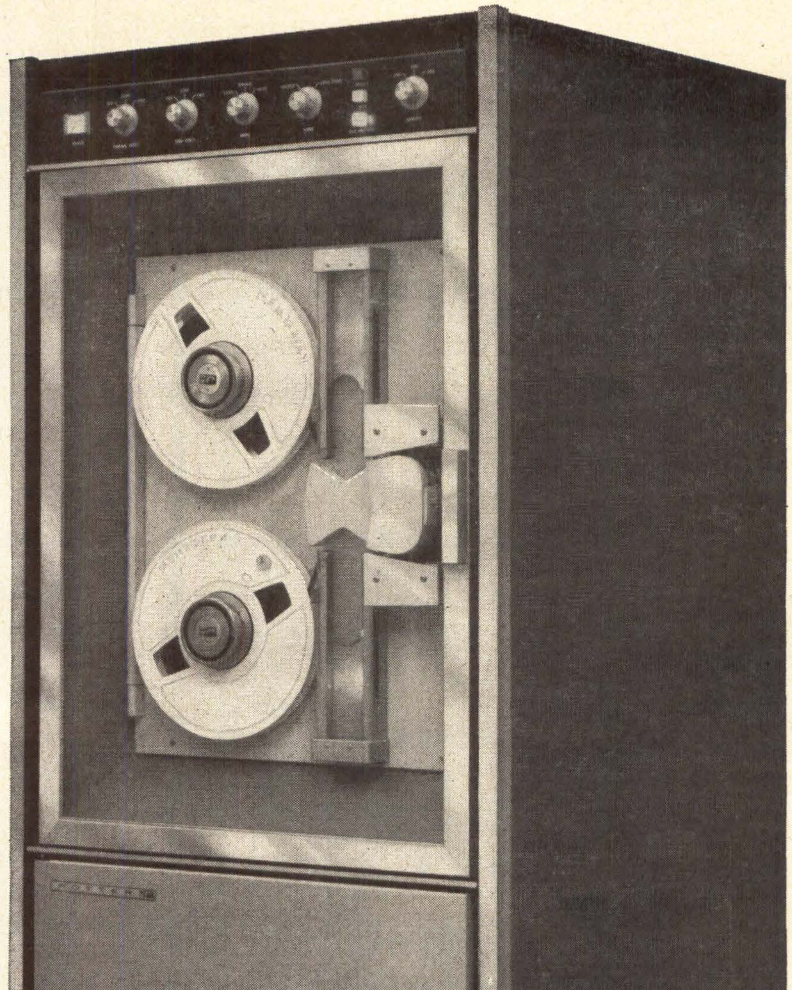

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CIRCLE NO. 27 ON INQUIRY CARD

LINEAR PULSE TRANSFORMERS IN CORE MEMORY SYSTEMS

This survey of the application of pulse transformers in memory systems discusses the major design problems in four types of memory configurations.

WILLIAM G. RUMBLE,
Advanced Development, Lockheed Electronics Co., Los Angeles, Cal.

In recent years, pulse transformers have found increasing use in core memory systems. They possess properties which make them ideally suited for memory applications, and perform functions possible with no other passive device. These properties include common mode isolation, inversion, voltage step-up, and voltage step-down. These properties are combined in an inherently simple and reliable device, which dissipates no standby power. On the minus side of the ledger, pulse transformers tend to be bulky and expensive by today's standards (perhaps an average cost ratio of two transistors per transformer). Furthermore, pulse transformers are not amenable to integrated circuit techniques. For many memory applications, however, the advantages greatly outweigh the disadvantages.

It is the purpose of this article to present a survey of pulse transformers in memories and to discuss some of the design problems. Because of the broad nature of the topic, the finer details of circuit design will not be covered. Most examples will be discussed from the point of view of the ferrite core memory, however, the applicability to other magnetic memories, where similar problems exist, will be apparent. In the interests of keeping the presentation to manageable proportions, only linear transformers, i.e., those with reasonably constant primary inductance, will be covered here.

This presentation includes the form and construction of pulse transformers, equivalent circuits, and core memory organization and circuit problems.

Device Characteristics

Basically, a pulse transformer is a passive coupling element consisting of primary and secondary circuits coupled by a mutual inductance. Multiple primary or secondary circuits are frequently used. Usually a core of magnetic material serves as the source of most of the mutual inductance and as a mechanical support for the primary and secondary windings. The core is commonly a toroid or cup core of ferrite with a linear hysteresis curve. For high frequency applications, when the required primary inductance is small, air-core transformers may be used. The core with the required windings is normally mounted on some kind of header with lead-off wires and then potted.

The transformer can be considered a band-pass filter where the high frequency characteristics determine the pulse rise time response, and the low frequency characteristics determine the pulse flat-top response and maximum pulse width.

A complete equivalent circuit is quite complex and presents severe mathematical difficulties.[1] Fortunately, in most design problems, simplifying assumptions can be made so that the analysis is not too bad. Fig. 1 is a simplified equivalent circuit for a pulse transformer of primary-to-secondary turns ratio of 1:n. For the voltage step-up case, $n > 1$, and for the voltage step-down case $n < 1$.

Let us now consider some of the pulse transformer parameters which are directly measurable. The most important of these are:

- L_P — Primary (Magnetizing) Inductance (effective primary inductance measured with secondary open-circuit)
- L_L — Total Leakage Inductance (effective primary inductance measured with secondary short-circuited)
- C_D — Total Effective Distributed Capacitance (effective distributed capacitance in parallel with L_P,

measured with secondary open-circuit and one side referenced to ac ground)

- C_i — Interwinding Capacitance (total capacitance between primary and secondary windings)

- Φ_s — Saturation Flux Rating (the maximum level of flux available in the transformer core before L_P starts to become seriously non-linear)

These quantities can be combined in simplified equivalent circuits for the step-up and step-down cases. From Fig. 1, it is obvious that for $n > 1$ (step-up), the effects of $(1/n^2)L_{LS}$ become small with respect to L_{LP}, and C_P small with respect to n^2C_S. By combining the effects of L_{LP} and $(1/n^2)\ L_{LS}$ into one lumped inductance, L_L in series with the primary circuit, and combining n^2C_S, C', and C_P into one lumped capacitance in parallel with the secondary circuit, one obtains the equivalent circuit for the step-up transformer (Fig. 2a). Conversely, for the step-down case where $n < 1$, $(1/n^2)L_{LS}$ is large compared with L_{LP}, and C_P is large compared with n^2C_S, and the equivalent circuit of Fig. 2b results. The question arises as to which circuit to use for values of n equal to or near 1. The choice of Fig. 2a or 2b depends on the particular design task.

Pulse transformer circuit analysis is normally carried out by the methods of transient analysis. To achieve mathematical simplicity, the problem is handled in steps, as shown in Fig. 3. This "piece-wise" analysis treats the rise, top, fall, and backswing periods separately, each with different simplifications of the circuits of Fig. 2.

For the rise period, one is mainly interested in the high frequency response. Here, the effects of L_P may be neglected, and the circuit of Fig. 4 results. During the top period of the pulse, the low frequency response is of primary importance, therefore, L_L and C_D may be neglected, leaving the circuit of Fig. 5. The analysis of the fall period and backswing depends a great deal on the primary and secondary circuits. If the primary source impedance remains constant, and the load impedance is relatively unchanged, then the fall period can be analyzed with the same circuit as the rise period (Fig. 4), and the backswing with the same circuit as the top period (Fig. 5).

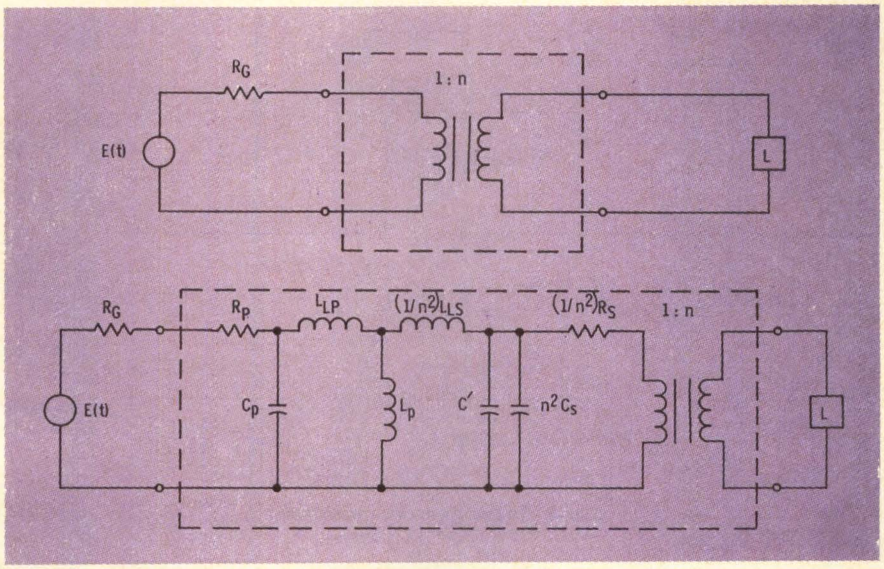


Fig. 1 Pulse transformer and general equivalent circuit.

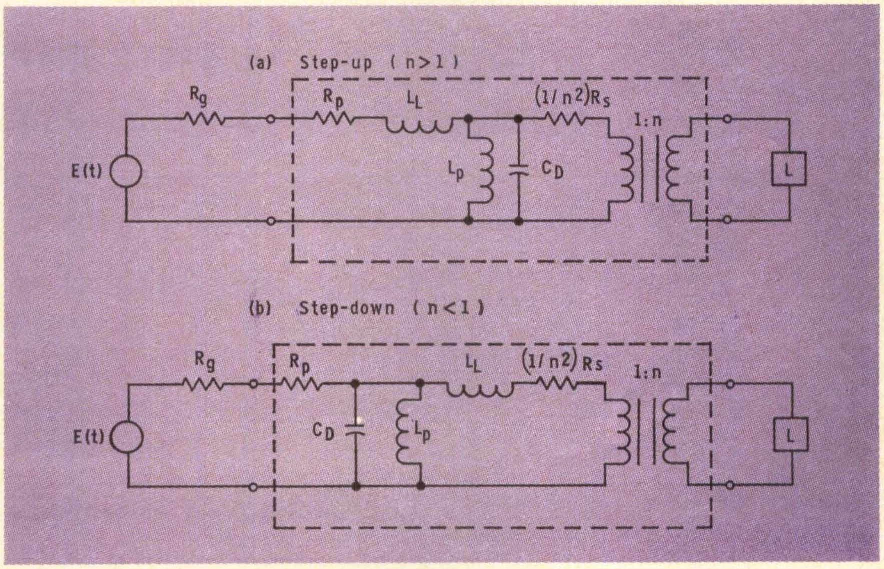


Fig. 2 Simplified equivalent circuits for step-up and step-down cases.

Often, however, the primary will open-circuit on the trailing edge (e.g., as driven from a transistor switch). Here, the magnetizing current, I_m, stored in the primary inductance, L_P, becomes the source for the overshoot and must be included in the analysis. Fig. 6 shows the equivalent circuit for this case. V_{CO} represents the voltage across C_D at the beginning of the fall period. Of course, the load impedance is the primary factor in the fall response in this case.

An important principle, which is of great assistance in transformer analysis, should be mentioned here. It is sometimes referred to as the "Equal Area Theorem," and states that over a period of time, long compared with the transformer decay rate, the area under the voltage waveform across any winding must average zero.[2] This principle is illustrated in Fig. 7. It is derived from the fact that:

$$\Phi = \frac{1}{n_i} \int V_i \, dt$$

where V_i is the voltage across a winding with turns n_i, and where

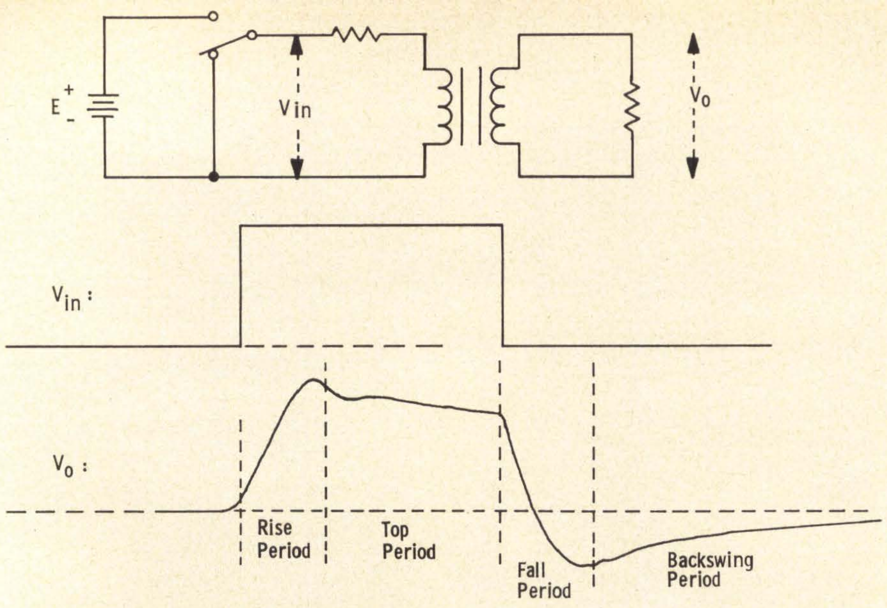


Fig. 3 Pulse response analysis.

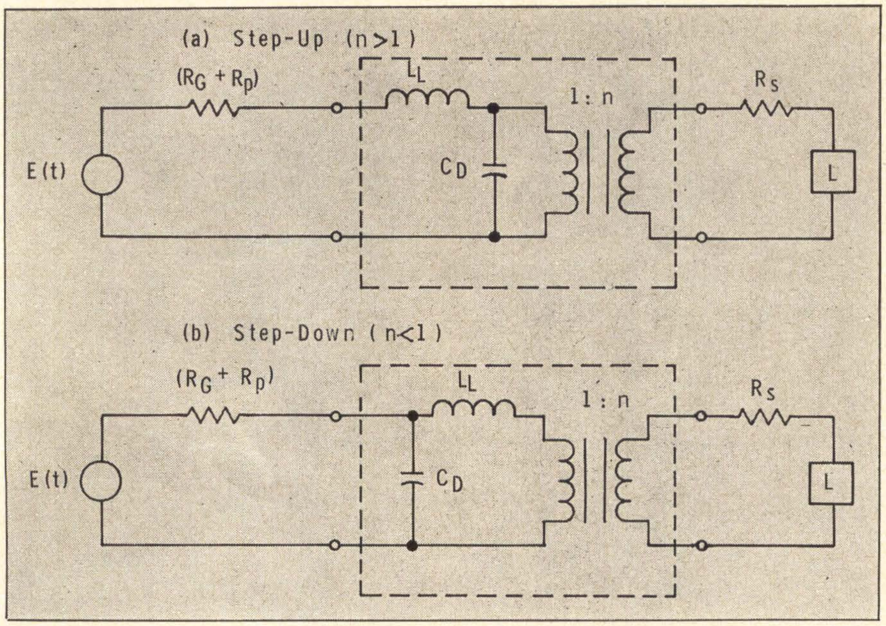


Fig. 4 High-frequency equivalent circuit (rise and fall periods).

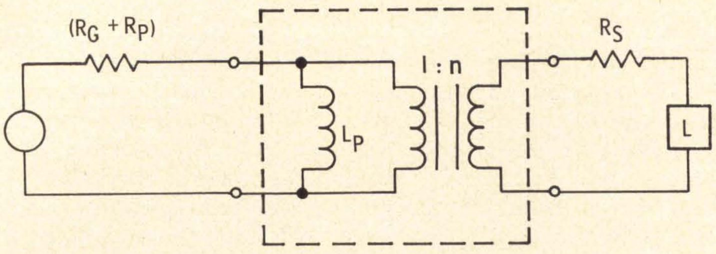


Fig. 5 Low-frequency equivalent circuit (flat-top period).

Φ is sharply limited by the saturation flux Φ_s (i.e., $\Phi \leq \Phi_s$ for nonsaturation of core).

Core Memory Operation

A brief review of core memory operation is in order. Information is stored in "square-loop" ferrite cores by magnetizing them to saturation, or nearly so, in one of two possible directions. A hysteresis loop representing the ONE and ZERO storage states is shown in Fig. 8. The core is switched from one state to another by the sum of two half-select current pulses (X and Y). The cores are arranged in a rectangular plane as shown in Fig. 8. Thus, only one core is acted on or switched in the plane at a time. The selected core lies at the intersection of the selected X, Y line pair.

Information is read from the plane by applying simultaneously half-read pulses on the X, Y line pair. If the core stores a ONE, the core will be switched to the ZERO state, producing a change in flux and voltage readout signal on the sense line. If the core stores a ZERO, the core will not switch and no readout signal will occur. Thus, information is extracted from the memory and destroyed in the process. To restore the information, or to write new information in the core, half-write pulses (opposite in polarity to the read) are applied to the selected X, Y line pair. The action of the write is to switch the core back to the ONE state. If a ZERO is to be written, an inhibit pulse is applied to a separate winding coincident with the write. The inhibit current is the same polarity as the read, and prohibits the core from switching to the ONE state. Thus, a ZERO is written.

In a coincident current memory system, the plane of Fig. 8 represents one bit of each memory word. Multiple planes are stacked as shown in Fig. 9 to provide memory words. For words of N bits each, N frames are required, and the same bit of each plane is driven in parallel.

The organization of a coincident current core memory system is shown in Fig. 10. In the memory cycle, the following essential operations must be performed.

- Select and drive one out-of-m X-drive lines with half-read and write currents. In modern systems, this is performed with a diode matrix and two levels of floating switches designated A and B. By selecting one out-of-c A-switches and one out-of-d B-switches, a unique selection of one out-of-m X-lines results.

- Select and drive one out-of-n Y-drive lines. This is performed in the same manner as for X.

- Gate each inhibit driver as required so that inhibit current is applied to only those planes where a ZERO is to be written.

- Amplify the output of each sense winding and discriminate between a ONE and a ZERO. Transfer the information to the output register.

Pulse transformers can be of assistance in performing all of these functions.

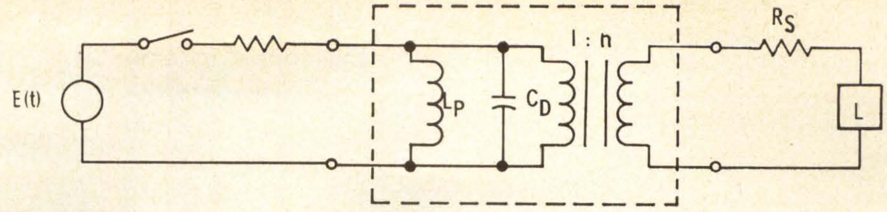
Transformer-Coupled Floating Switch

Fig. 11 is used to illustrate the concept of the floating switch. This is a commonly-used matrix configuration employing two diodes for each output drive line. The current to be switched through the selected drive line (for both read and write pulses) is derived from a single source. The switches are arranged in pairs and in two levels. In each level a switch pair is selected, uniquely selecting one output drive line. The read switches when selected cause current to flow in one direction in the output drive line, and the write switches in the opposite direction.

Since the drive lines are inductive, there will be a substantial voltage drop across the selected drive line during the rise of the current pulse. The potential of the switch output, therefore, must move to accommodate this load back-voltage. Hence, the term "floating switch." The characteristics desired in this circuit are as follows.

- It must present a high impedance in the OFF state, and a low impedance in the ON state.
- It must be able to operate over a wide range of output voltage without affecting circuit performance.
- Current waveshape integrity must be preserved, i.e., the output current should equal the input current.

The transformer-coupled floating switch meets these requirements perfectly. The circuit configuration is shown in Fig. 12. Two types of drive are considered: voltage drive and current drive. The two configurations are really not different in essence, only in the method of controlling the transistor base current. In the voltage-driven switch (Fig. 12) the voltage applied across the transformer primary is approximately equal to the source voltage,



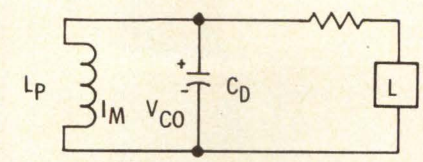


Fig. 6 Fall and backswing equivalent circuit (primary open-circuit).

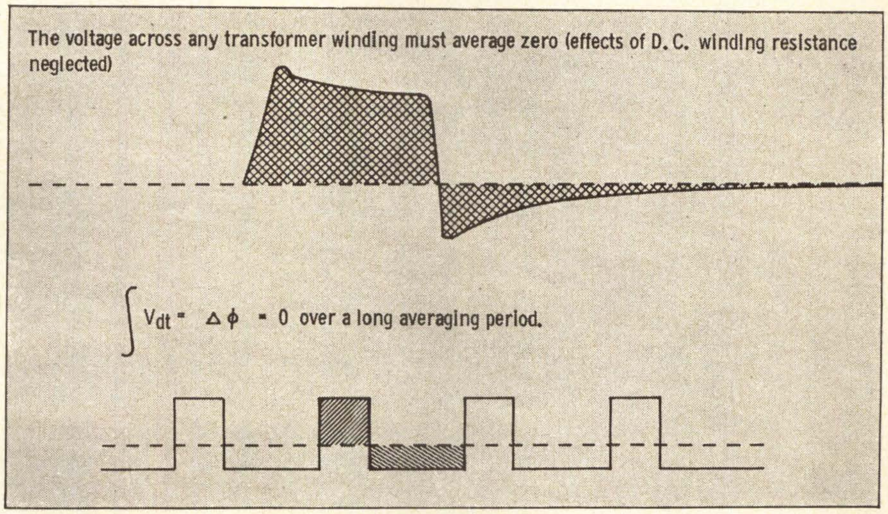


Fig. 7 Equal area theorem.

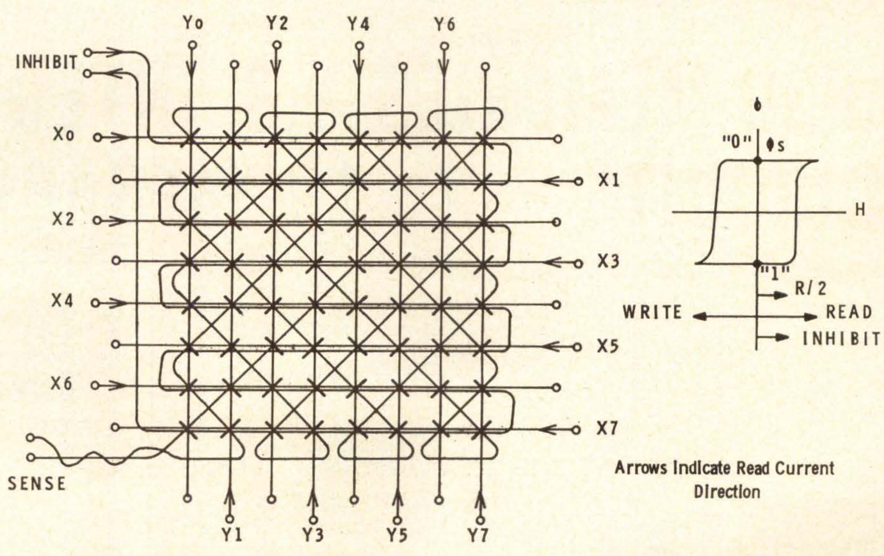
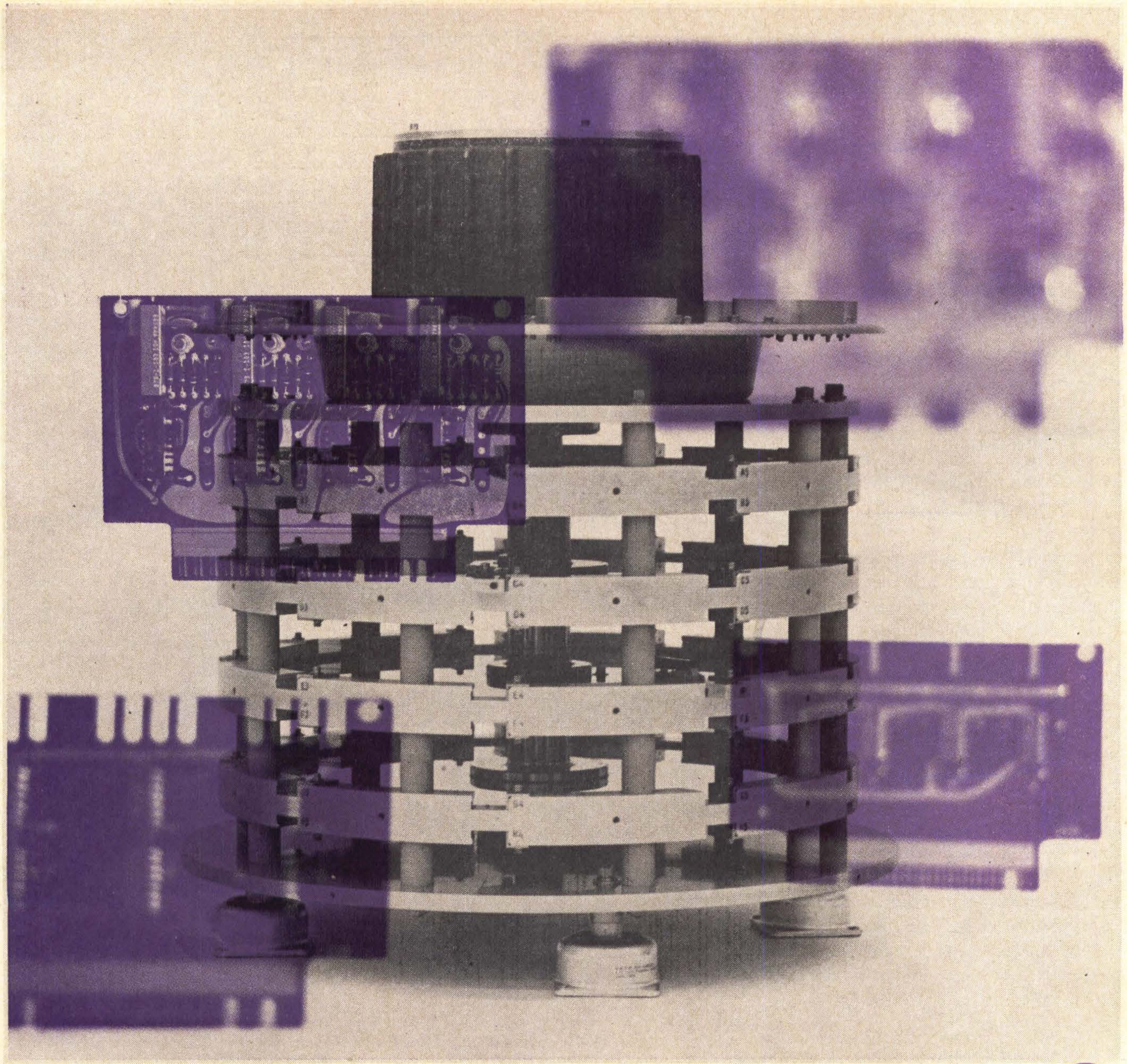


Fig. 8 Coincident-current plane wiring configuration.



E (i.e., the source impedance is small). The transistor base current is controlled mainly by the secondary voltage and R_2. In the current-driven switch (Fig. 13b), the primary voltage is small enough, so that the primary current is mainly controlled by R_1. The transformer acts as a current transformer, so that the transistor base current is $1/nI_p$. R_1, therefore, controls the transistor base current. In both these configurations, a turns ratio of $n \leq 1$ is generally chosen so that the primary current is kept as low as possible. The advantages of the transformer-driven floating switch configuration can be summarized as follows.

- Current waveform integrity is preserved; output current equals input current.
- A true floating switch configuration; common-mode isolation except for interwinding capacitance.
- Standby power is zero.
- Transformer primary is ideally-suited to being driven from a diode matrix.
- Transformer backswing can be designed to turn-off, effectively, a saturated transistor switch.
- Because of the capability of inversion, either NPN or PNP switches can be driven from the same input circuit.

Voltage-Driven Switch

The equivalent circuits for the voltage-driven switch are shown in Fig. 13. Fig. 13b is used for the rise period. R_2 includes R'_2 and the effective transistor input resistance, R_E, in series is referred to the primary. E_2 represents the transistor V_{BE} threshold referred to the primary circuit. The diode in series with R_2 and E_2 is an ideal one, with no forward drop. During the initial portion of the secondary voltage rise, the diode is reverse biased, and the secondary circuit is effectively open. The circuit reduces to R_1 in series with C_D, and the secondary voltage rise is given by the exponential form:

$$V_0 = nE_1\left[1 - \exp.\left(-\frac{t}{R_1C_D}\right)\right]$$

When the diode becomes forward biased, the secondary circuit becomes L_L in series with R_2. The differen-

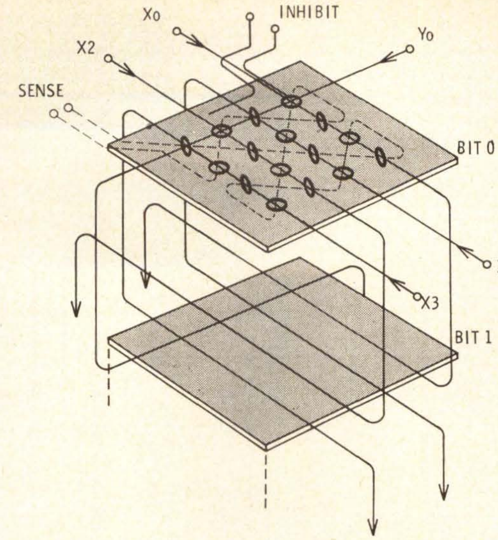


Fig. 9 Coincident-current stack wiring configuration.

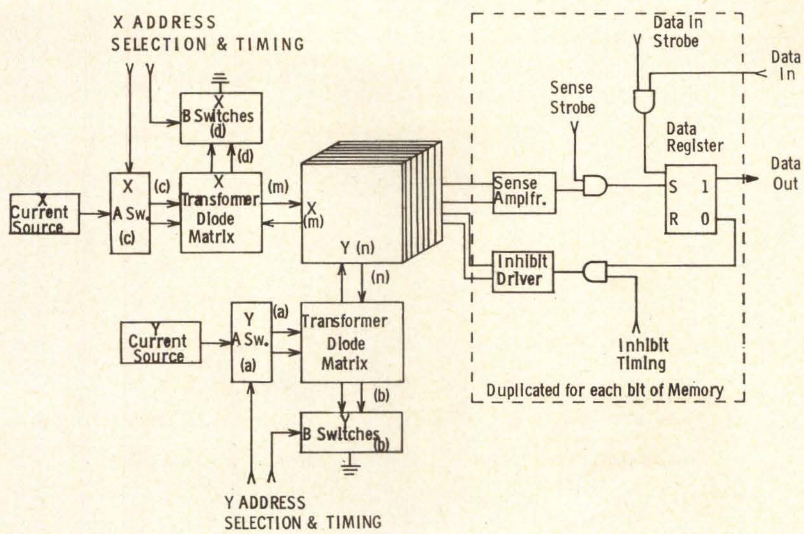


Fig. 10 Coincident-current memory system.

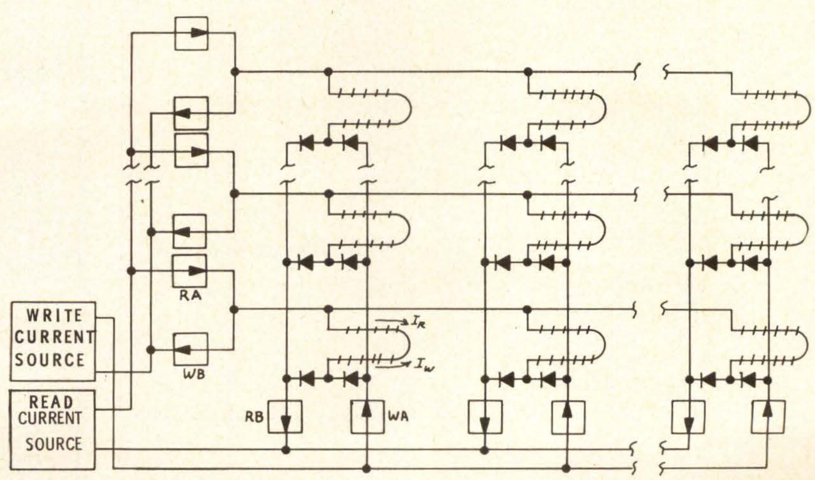


Fig. 11 Diode matrix with floating switches.

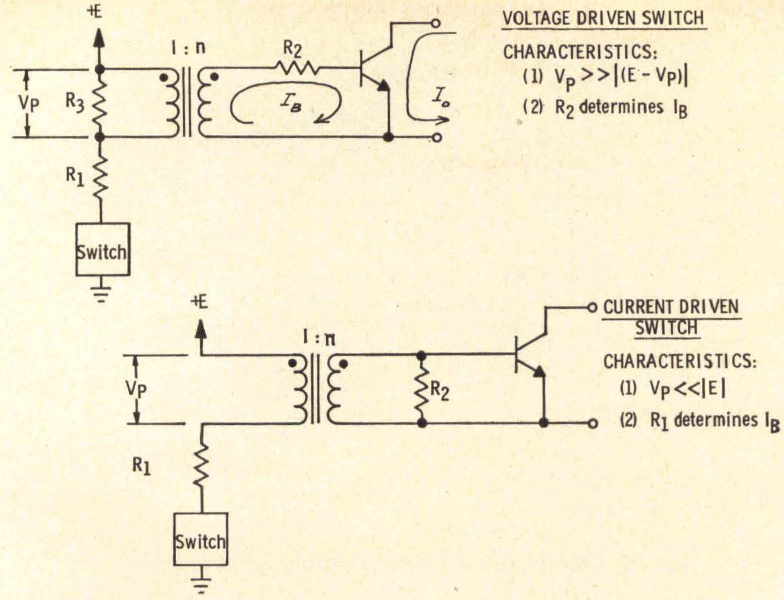


Fig. 12 Voltage- and current-driven switches.

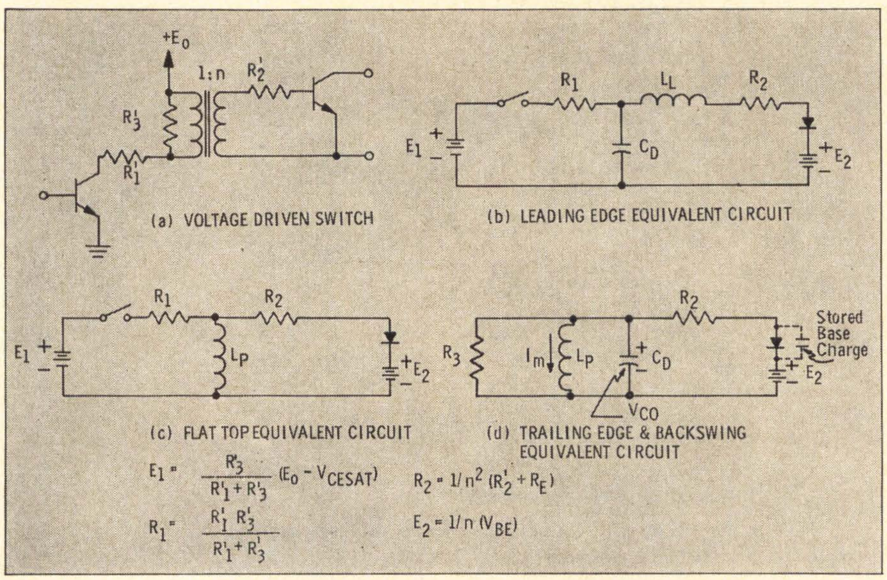


Fig. 13 Voltage-driven switch analysis.

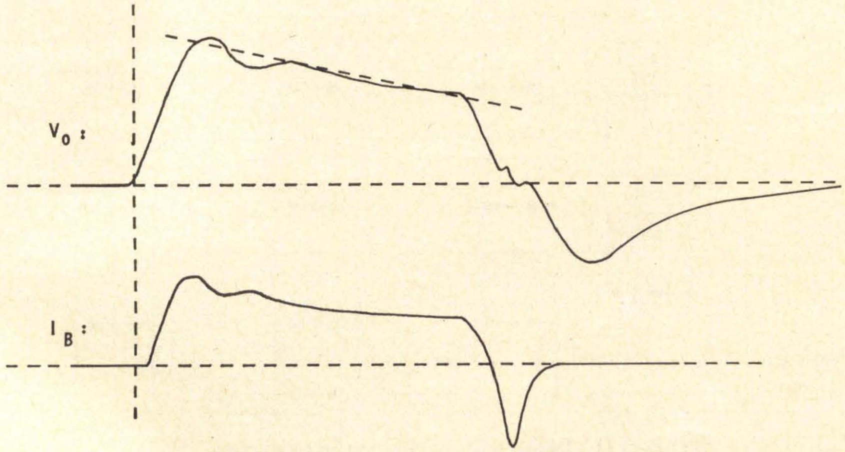


Fig. 14 Voltage-driven switch secondary response.

tial equation for the circuit in terms of the secondary voltage is the familiar form of the damped oscillator:

$$\frac{d^2V_0}{dt^2} + \left(\frac{R_2}{L_L} + \frac{1}{R_1C_D}\right)\frac{dV_0}{dt} + \left(\frac{R_1 + R_2}{L_LC_DR_1}\right) V_0 = \text{Constant}$$

if:

$$\left(\frac{R_2}{L_L} + \frac{1}{R_1C_D}\right) = 2\alpha$$

and:

$$\left(\frac{R_1 + R_2}{L_LC_DR_1}\right) = W_a^{\,2}$$

then critical damping results when:

$$K = \frac{\alpha}{W_a} = 1$$

When $K > 1$, the circuit is overdamped, and when $K < 1$, the circuit is underdamped. A representative secondary voltage waveform for the slightly underdamped case is shown in Fig. 14.

The flat-top period equivalent circuit consists of R_1, R_2, and L_P in parallel. The secondary voltage waveform decays exponentially during this period, with time constant of:

$$\frac{L_P\,(R_1 + R_2)}{R_1R_2}$$

The fractional droop during this period is:

$$D = 1 - \exp.\left[-\frac{R_1R_2t}{L_P\,(R_1 + R_2)}\right]$$

The rate of buildup of magnetizing current in the primary magnetizing inductance, L_P, is V_P/L_P, and the magnetizing current as a function of time is given by:

$$I_m = \frac{E_1}{R_1}\left[1 - \exp.\left(-\frac{R_1R_2t}{L_P\,(R_1 + R_2)}\right)\right]$$

The fall period and backswing equivalent circuit is shown in Fig. 13d. For a short time after the diode becomes reversed biased, it will conduct current in the reverse direction. This represents the stored charge in the transistor base circuit. Until this time, R_2 and R_3 are effectively in parallel, and the equation is:

$$\frac{d^2V_0}{dt^2} + \left(\frac{R_2 + R_3}{R_2R_3C_D}\right)\frac{dV_0}{dt} + \left(\frac{1}{L_PC_D}\right) V_0 = 0$$

After the diode is reversed biased

and the base stored charge is dissipated, the equation is:

$$\frac{d^2V_0}{dt^2} + \left(\frac{1}{R_3C_D}\right)\frac{dV_0}{dt} + \left(\frac{1}{L_PC_D}\right)V_0 = 0$$

The first condition is normally overdamped, while the second is slightly underdamped. Care must be taken so that the underdamped oscillations are not large enough to turn the transistor back on. The method of design has been only roughly outlined here. For a complete discussion, see Grossner[3] or Lee.[4]

There is no need to keep the transistor base current constant, in fact a large droop is helpful. The transistor is overdriven on the rise of the pulse, yielding fast turn-on. By the trailing edge, the base current has decayed to a nominal value, and a large magnetizing current is available to turn the transistor off. A bypass capacitor across R'_2 is useful in providing fast turn-off for the transistor. The waveforms of Fig. 14 show this reverse current flow.

Current-Driven Switch

The current-driven switch equivalent circuits are shown in Fig. 15, and representative secondary response waveforms in Fig. 16. As in the case of the voltage-driven switch, a step-down transformer is assumed. The secondary circuit consists only of the transistor emitter base and the parallel damping resistance, R_T. If n is not to small, R_2 can be safely ignored, and the secondary voltage is constant and equal to E_2. In this case, the magnetizing current builds up linearly at a rate equal to E_2/L_P. The fall and backswing is handled as in the voltage switch. The current available to turn off the transistor is essentially the magnetizing current, I_m. R_T controls the backswing and recovery time.

If the control of the secondary current rise and fall times is critical, a voltage step-up (current step-down) transformer may be used. The advantages of this circuit are apparent from the step-up equivalent circuit which was shown in Fig. 4(a). Since the primary impedance is high L_L can usually be neglected. Also, since the secondary voltage is low (sharply limited by V_{BE}), C_D is not too critical. Turning off the

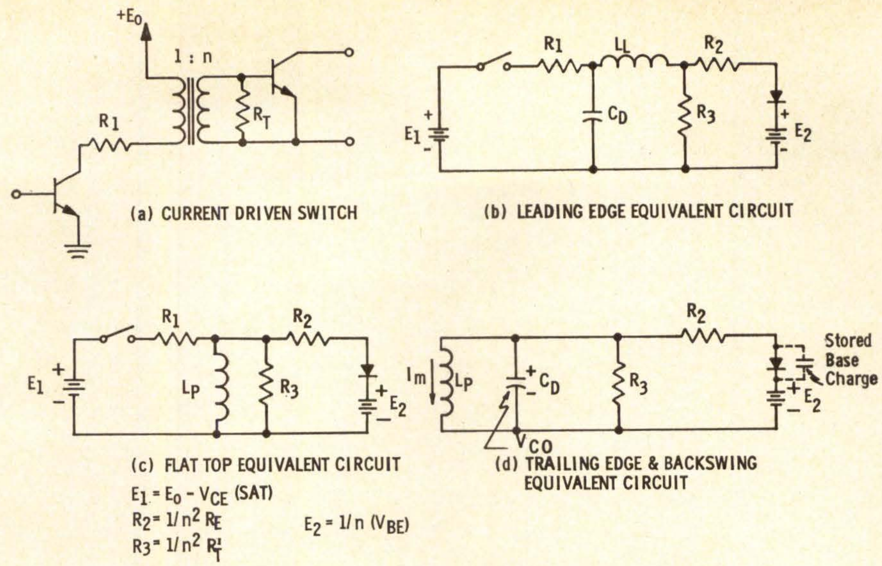


Fig. 15 Current-driven switch analysis.

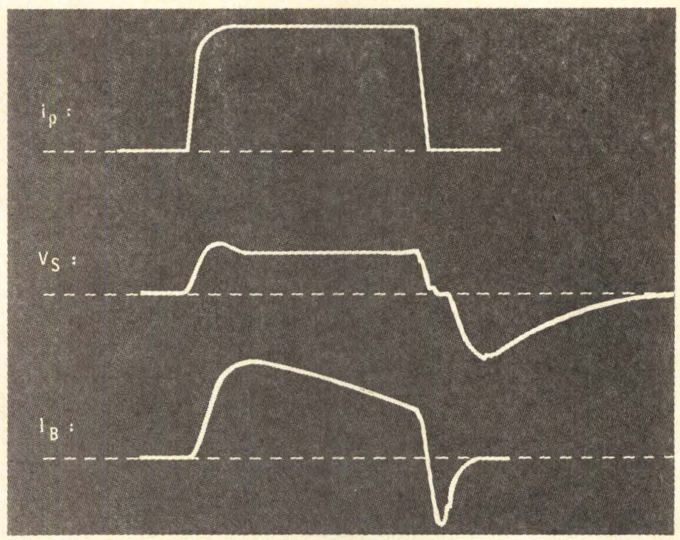


Fig. 16 Current-driven switch secondary response.

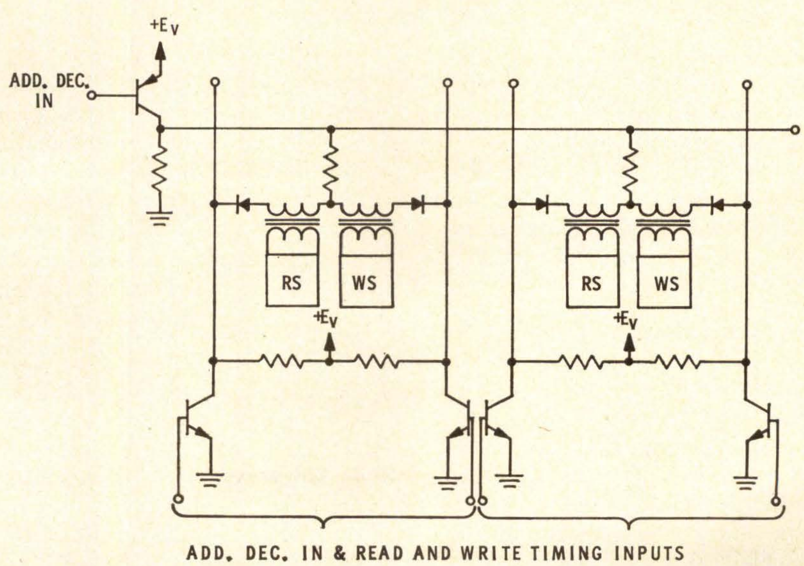


Fig. 17 Example of voltage-driven switch, driven from matrix.

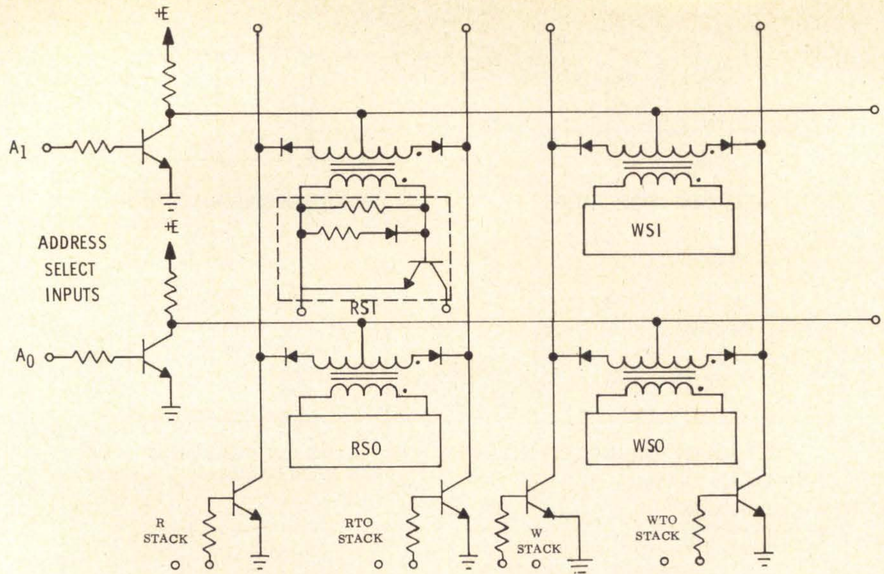


Fig. 18 Current-driven switch with turn-off drive.

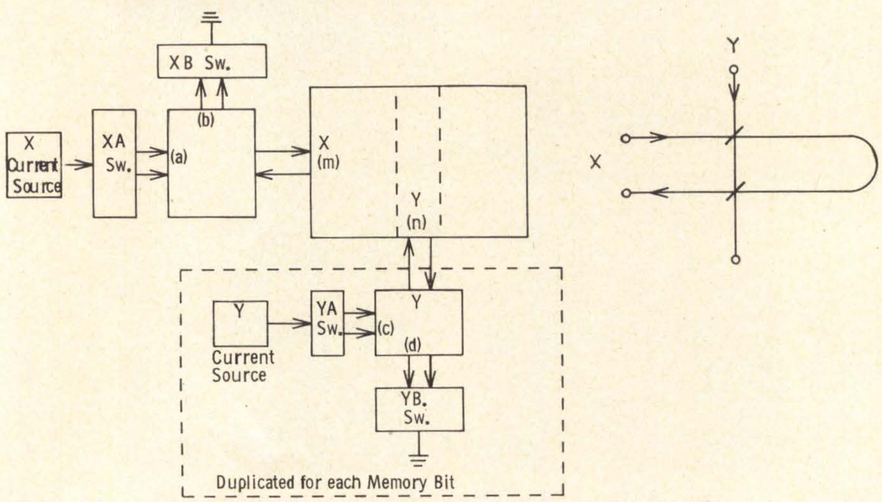


Fig. 19 2½D memory organization.

switch rapidly by driving a second primary winding with current in the opposite sense is another useful technique. This is shown in Fig. 18. Now the turn-off current is relatively independent of the magnetizing current, and L_P is no longer critical.

Switch Applications

One attractive feature of the transformer-coupled switch is the possibility of driving the transformer primaries from a diode matrix. This technique is especially attractive in large memory systems with multiple stacks. Figs. 17 and 18 are examples in which the matrix inputs at the left hand side represent the m address decoder outputs corresponding to the m switches in the group. The inputs at the bottom are the n address decode outputs corresponding to the n stacks in the system. For example, in a memory system consisting of 8 stacks of 4,096 words each, such a matrix would drive the eight XA-switches in each stack, and would have the dimensions 8 x 8. A great reduction in hardware and decoding complexity is thus realized.

2½D Organization

Within the past year or so, a relatively new method of organizing core memories has come into favor.[5] Dubbed 2½D, it is effectively midway between the more commonly-known linear select (2D) and coincident-current (3D) organizations. Instead of the 4-wires per core in the standard CCM, only 3 wires are required. The 2½D memory may be thought of as a 4-wire CCM in which the inhibit wires have been removed and the digit-write function taken over by the Y lines. The price paid for the magnetics simplification is that now the Y-drive circuits must be duplicated for each bit of the memory word. The 2½D organization is shown in Fig. 19. Since the Y diode matrix is duplicated on a per-bit basis, the same switch selection will occur in each matrix. It is advantageous to design a multi-pole switch, i.e., a switch with a single input, but with multiple outputs designed to perform a switching function in multiple diode matrices. The modifications of the voltage- and current-driven switches shown in Fig. 20 are designed for this purpose. In Fig. 20(a), multiple secondaries drive switches in parallel. A step-down transformer is used to minimize primary current. In Fig. 20(b), multiple transformers are used with the primaries series-connected. Here, a step-up configuration is optimum to minimize total primary voltage. As previously mentioned, this also gives better secondary current control.

Transformer Drive Line Coupling

At relatively-slow memory cycle times, for example, 4.0 microseconds and longer, or in systems with short drive lines, diode matrix configurations, such as shown in Fig. 11, are quite adequate. However, for very short cycle times, or for long drive lines, transformer coupling of each individual drive line to the diode matrix and switches becomes extremely desirable. A great improvement in drive current rise time and wave shape, and sense line noise, can be realized with this technique.

The function served by individually transformer-coupling each drive line is the common mode isolation of each line from other lines and from the diode matrix and driving circuits. The problem solved by this common mode isolation can best be understood by referring back to Fig. 11. It is seen that the drive lines are tied together in groups. The diode matrix is represented as a rectangular array, with one end of each drive line connected together in horizontal rows, and other end connected through a diode pair to vertical columns. Thus, when a line is selected and driven, the back voltage from the current rise in the selected line is coupled to many unselected lines as well. These unselected lines present a substantial distributed capacitance because of their proximity to other wires in the stack (e.g., sense and inhibit) and possibly ground planes. This capacitance appears in parallel with the inductance of the selected line during the current rise. The result is to slow the current rise in the selected line and to produce overshoot and oscillations in the wave shape.

A number of unfortunate results are also produced on the sense winding output. The large voltage excursions on the unselected drive lines are capacitance-coupled to the sense line as a large common mode signal. Unless the sense line itself and the impedance of the sense amplifier differential input are exactly balanced, which is rarely the case, some of the common mode voltage will be converted into a differential noise signal. In practice, there will always be some unbalance in the impedance seen at the two ends of the sense winding making it desirable to minimize the sense winding common mode signal. A second source of sense winding noise arises because of the displacement currents flowing in the unselected lines undergoing voltage excursions. These displacement currents are coupled to the sense line via the unselected cores. The unselected cores act essentially as transformers, coupling energy from the drive lines to the sense lines. It should be mentioned that the conventional sense winding pattern cancels out this coupling to a first order approximation. Under worst pattern conditions, however, the core delta noise gives rise to a significant net coupling, which can definitely cause trouble. One very common form of oscillation or ringing found on the sense winding output is caused when the capacitance of the drive lines and the inductance of the return path to ac ground (i.e., the path to ac ground consisting of the selected switches, diode matrix, and wiring leads) form a resonant circuit. The ringing produced is coupled to the

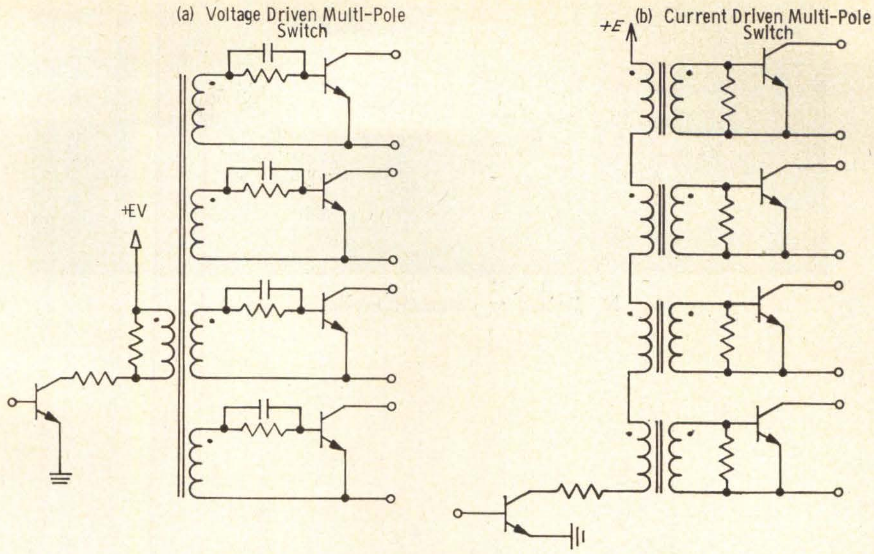


Fig. 20 Multi-pole switch configurations.

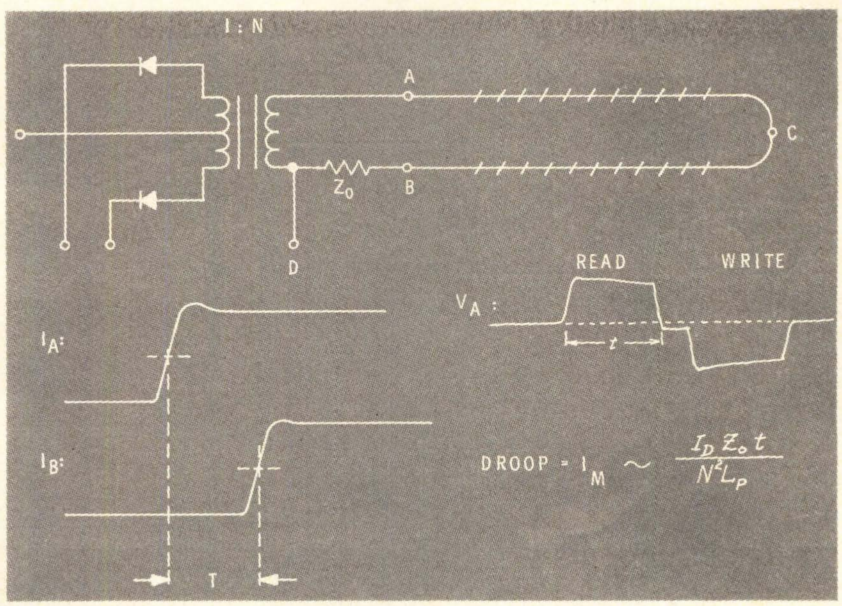


Fig. 21 Series line termination.

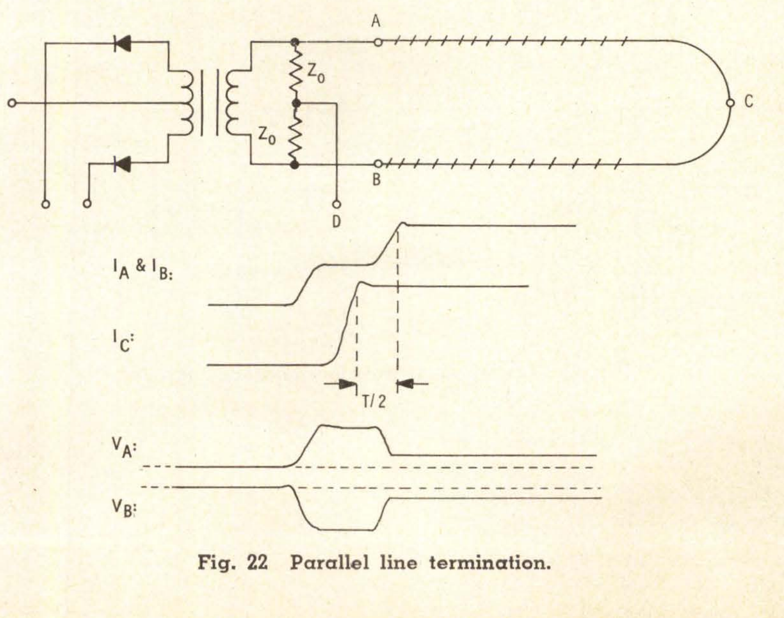


Fig. 22 Parallel line termination.

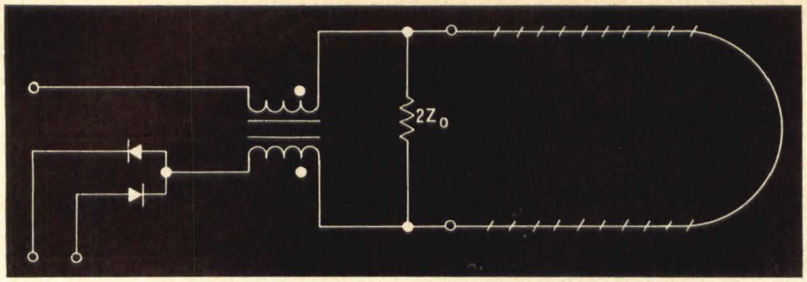


Fig. 23 Balun or common mode line coupling.

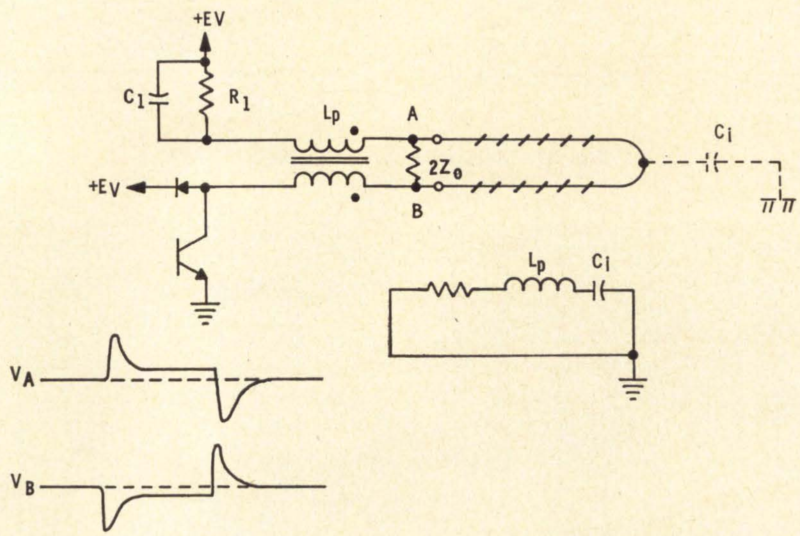


Fig. 24 Inhibit line coupling.

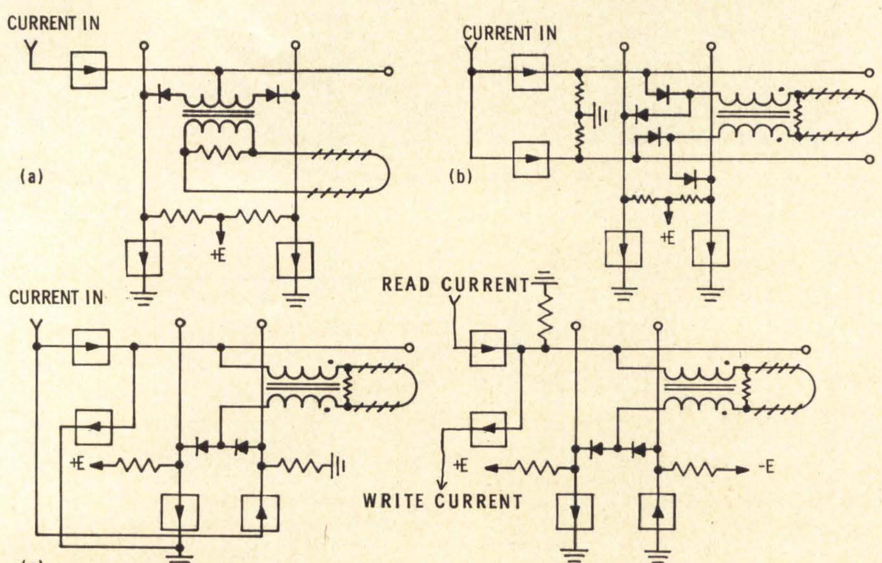


Fig. 25 Examples of transformer-diode matrices.

sense line by both the electrostatic and electromagnetic modes described above. The most effective method of correcting this problem is to break the resonant circuit by isolating the line capacitance with a large series common mode impedance. This, of course, is one of the benefits of individually transformer-coupling each drive line.

If the drive lines are transformer coupled, the above difficulties are avoided. Each line and its distributed capacitance is isolated from the selected line and from each other. Since the unselected line capacitance is blocked, the drive current waveshape is relatively clean and undistorted. Voltage excursions and displacement currents in unselected lines are greatly attenuated, and the amount of energy coupled to the sense line is greatly reduced.

A drive line in a memory stack possesses the properties of a "lossy" transmission line. The distributed inductance of the wire, the lumped inductances of the cores, and the distributed capacitance of the wire to the surrounding wires in the array, give rise to transmission line properties, including a propagation velocity and a characteristic impedance. In most memories, some attempt is made to terminate the drive lines in their characteristic impedance in order to minimize distortion, to absorb energy in the stack, and recover to a low-noise condition rapidly. Characteristic impedances of 100 to 200 ohms are common in today's memory stacks utilizing 0.022"O.D. and 0.030"O.D. ferrite cores. It should be emphasized that the line impedances can vary depending on the exact method of terminating the drive, sense, and inhibit lines, and on the state of the cores. Therefore, in specifying line impedance, care must be taken to define the exact termination on each line, and measurement method.

Two basic methods of transformer coupling the drive lines will be mentioned here: ac transformer coupling, and balun or common mode coupling. Fig. 21 illustrates ac coupling to a series-terminated line. The termination resistor approximately matches the impedance of the line, and the pulse travels from A to B, with a time delay, T, the propagation time of the line. A step-up transformer is desirable for this configuration to minimize primary voltage and to obtain a fast secondary current rise. This is essentially the method of Allen, Bruce, and Councill,[6] except that their system was driven from a load-sharing matrix switch. Because of the ac coupling, there will be some droop for a constant-current primary drive given approximately by the expression:

$$(I_D Z_o t)/(n^2 L_P)$$

where I_D is the drive current in the line, Z_o is the line characteristic impedance, t is the pulse width, n is the transformer turns ratio, and L_P is the primary magnetizing inductance. To recover the transformer, the read current pulse must be followed by an opposite polarity "write" pulse of equal volt-time integral. Half-cycles (e.g., read-only) are therefore not possible with this method.

An ac-coupled parallel terminated line configuration is shown in Fig. 22. Also shown is an exaggerated drawing of the line response to a fast rise current pulse. An attempt is made to indicate the fact that the pulse propagates from both ends of the line. Thus, the current pulse rise at point C is fast and uniform, since the pulses propagating from the ends of the line reach this point simultaneously. The current rise at A and B, the ends of the line, occurs in two steps separated by a duration equal to the propagation time of the line. With this configuration, the line is terminated exactly only for an infinite source impedance, but in practice, it works quite well with considerable mismatch.

Less skew, i.e., the maximum separation in time at which the current reaches full value for two points on the line, is obtained with the parallel termination since the current pulse propagates from both ends of the line. In practice, rise times of about three times the line propagation time, or greater, are used. The power dissipation in the parallel termination resistors is, of course, much less than the series termination. The termination resistors can be connected to ac ground at point D in order to reference the potential of all drive lines and reduce drive line voltage excursions.

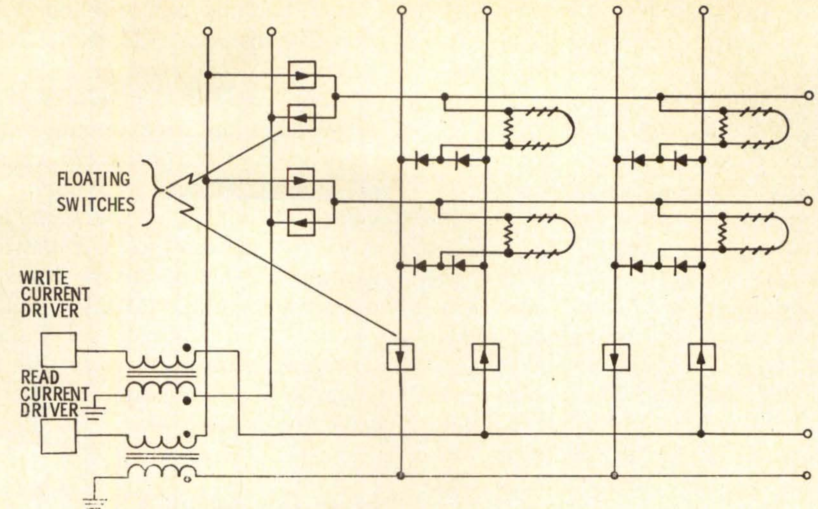


Fig. 26 Balun or common mode transformer used in current source and return circuit.

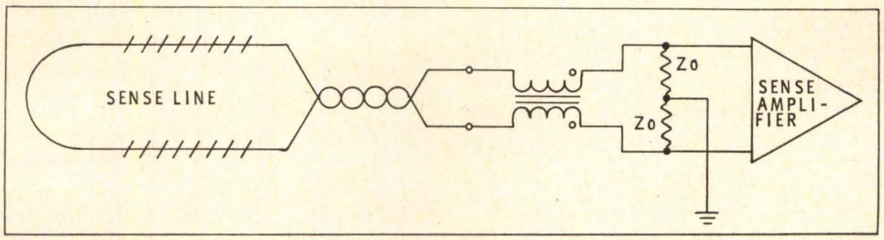


Fig. 27 Balun coupled sense line.

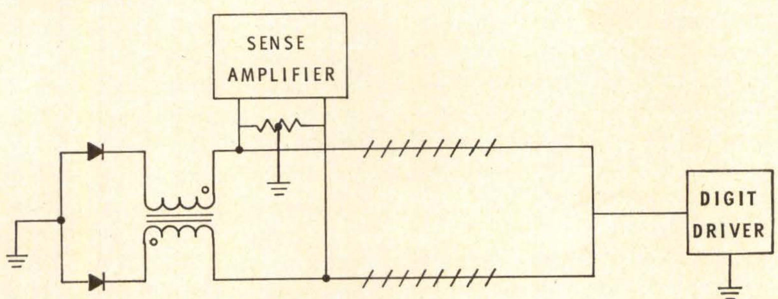


Fig. 28 Common sense-digit line with current splitting transformer.

Balun or Common Mode Line Coupling

The second type of transformer-drive line coupling to be described here is balun or common mode line coupling. Shown in Fig. 23, this configuration is basically a dc-coupled arrangement, where isolation is obtained by placing a large common mode inductance in series with the line. The source of this inductance is a 1:1 transformer, usually designed for high magnetizing inductance and low leakage inductance. This is normally accomplished by a very tightly-coupled bifilar winding. The balun coupling then, presents a low-differential impedance (transformer leakage inductance plus dc winding resistance), and a high common mode impedance (transformer magnetizing inductance). Balun line coupling is used with a parallel termination resistor which is twice the characteristic impedance of the line (Fig. 23). The chief advantage of this configuration is that dc coupling is maintained, and, consequently, droop and transformer recovery are no longer a problem. Half cycles are therefore possible. As with the ac-coupled parallel terminated case, the drive current propagates from both ends of the line.

A balun coupling to the inhibit line is shown in Fig. 24. This inhibit line coupling scheme has a number of advantages: (1) oscillation of the inhibit winding capacitance with the ac ground return circuit inductance is blocked by the large common mode impedance, greatly speeding recovery of the sense winding after pulsing the inhibit winding, and (2) the inhibit current propagates from both ends of the line thus reducing skew. One characteristic of the balun coupled line is for the transformer L_m to oscillate with the line capacitance. Since L_P is large, the amplitude and frequency are both relatively low. The oscillation is typically less than 1% of the drive current and 200 KC or greater, and does no particular harm in the system. It can be damped with a resistor in parallel with L_P, either across one of the windings or across a third winding. Balun coupling, in this writer's opinion, represents the optimum type of transformer drive line coupling for memory stacks.

Four commonly-used transformer-diode matrix configurations are shown in Fig. 25. Lockheed Electronics Co. is currently using the configuration of Fig. 25(b) in their 1.0 microsecond cycle memory system. One system, currently being produced is coincident-current, and the magnetics is organized in 8 stacks, each 4096 words x 74 bits. Ferrite cores with 0.022"O.D. are used. The balun coupling transformers are approximately 3.0 mH magnetizing inductance, have a maximum dc winding resistance of 1.0 ohm for each winding, and have a maximum leakage inductance of 0.7 μH. The line termination resistors are 300 ohms, approximately twice the line impedance.

In practice, the magnetizing inductance of the transformers is non-critical and L_m of 1.0 millihenry or more is quite effective. The minimization of leakage inductance is more important since it represents added inductive load in series with the drive line. A very tightly coupled bifilar winding is thus the optimum transformer design.

Another method of blocking the oscillations of the drive line capacitance and return path lead inductance is with the circuit of Fig. 26. This configuration is useful in driving smaller stacks where the presence of the unselected line capacitance can be tolerated and still achieve an adequate rise time. Here the balun transformer is inserted in series with the current source, and both levels of switches are free to move with the load reactive voltage. This method is most effective in reducing oscillations coupled to the sense line. Also, the matrix shown is basically asymmetrical (i.e., driving from the diode side presents a larger capacitive load than from the other side). The balun transformer corrects this asymmetry by isolating the matrix from ground.

Sense Line Coupling

Two applications involving coupling to the sense line with pulse transformers will be described briefly here. The first of these is a balun-coupled sense line illustrated in Fig. 27. The principle is basically the same as the balun-coupled drive line, i.e., common mode isolation. By inserting a large common mode inductance in series with the line, the common mode signal on the sense winding is greatly attenuated, so that the generation of differential noise signal, due to impedance unbalance, is blocked. The line may be parallel terminated with $2Z_0$ at the sense amplifier input, and referenced to a dc voltage, e.g., ground, as shown in Fig. 27. As with the drive line balun transformer, the transformer L_m is relatively non-critical, values of 1.0 millihenry and up being quite effective. It should be pointed out that there are only minor recovery problems associated with the balun transformer in this configuration. The only source of transformer-magnetizing current, and, hence, recovery problems, is common mode signal, and since the sense line is floating, this must average zero. The line capacitance will absorb some ac common mode signal, or will oscillate with the L_m of the transformer, but the amplitude is small enough to ignore in most cases. In general, the higher the line capacitance, the larger L_m should be.

Fig. 28 illustrates the use of a transformer as a current-splitting device in a common digit-sense line configuration. The common digit-sense line is divided into two segments, which are driven in parallel from a single digit driver. The transformer is connected in an anti-balun configuration, i.e., so that it presents a large differential impedance and a small common mode impedance. Thus, the current is split equally in the two lines. The sense amplifier is connected differentially across the two lines. The diodes present a high-impedance for small differential signals in the transformer, causing rapid recovery from differential signals caused by line impedance unbalance and the digit current. Since the sense amplifier end of the lines is referenced to ground, the sense amplifier is protected against large signals during the digit current.

Conclusions

A survey has been made of the more common uses of pulse transformers in core memories. Four classes of applications have been described and examples given of each. It is clear that pulse transformers are being used in memories more than ever before and that this use is likely to increase in the near future. At this point in time, the major drawback would seem to be that transformers cannot be integrated. This author feels, however, that a great deal can still be done in improving the present pulse transformer technology by reducing the size and cost of units. An approach which deserves intensive development is that of packaging multiple transformer arrays including diodes and termination resistors in single module units.

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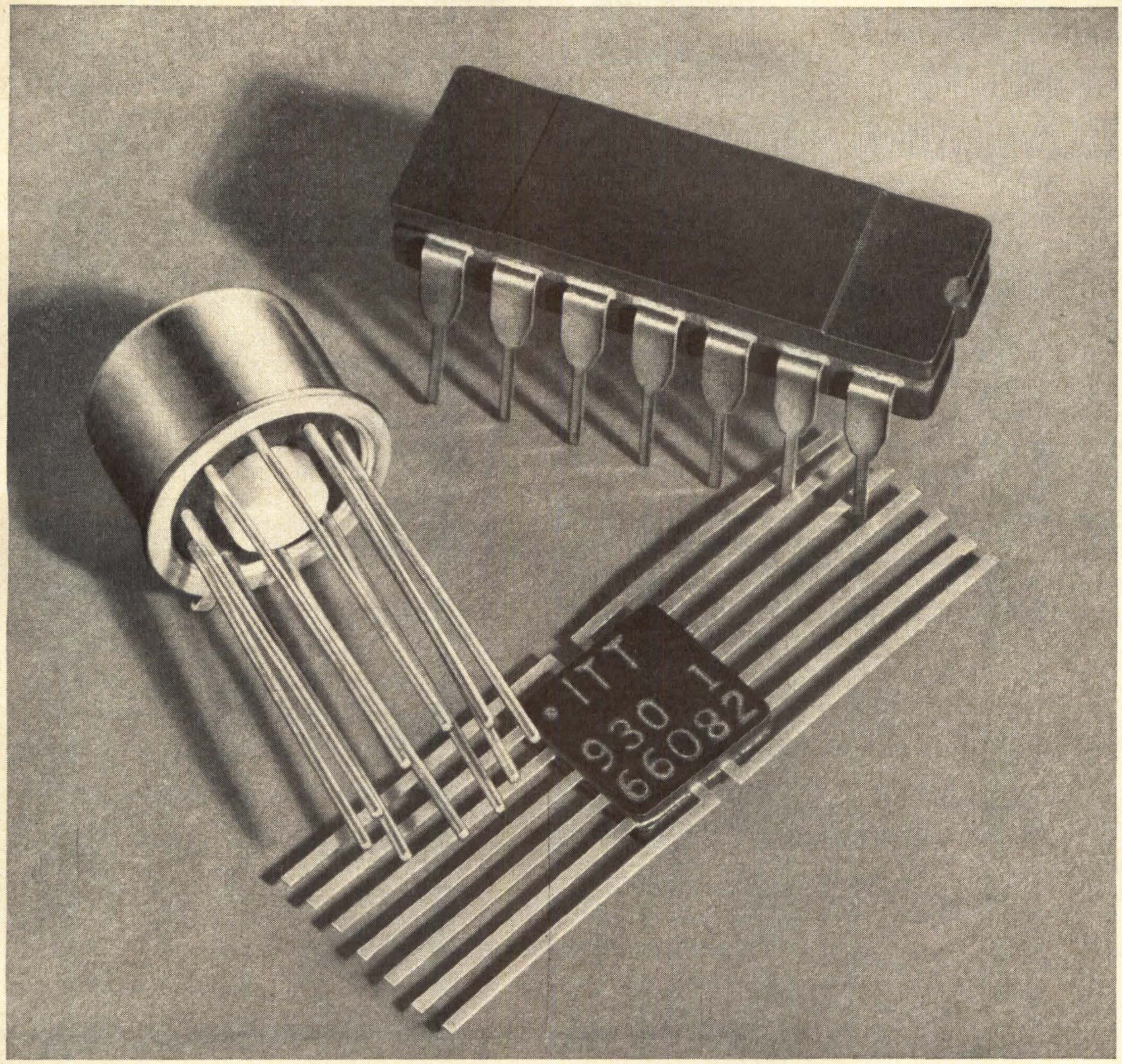

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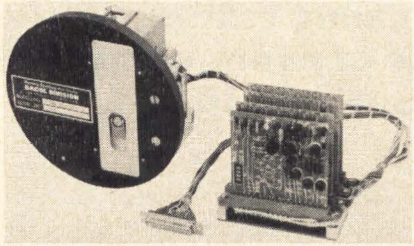

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COMPUTER TRAINER

A dynamic classroom display is featured in a digital computer trainer developed to accelerate training of computer technicians, operators, and programmers. The basic system is composed of a four-by-six foot dynamic display, a general-purpose computer, and an input/output Teletype unit. The 16-bit, 4096-word (or 8192-word) computer can be used to demonstrate operations of business and scientific applications. Its use in the trainer system does not interfere with its capabilities as a working tool. Controls and indicators on the front panel are grouped logically, and contents of all registers are displayed. Indicator lights are also push-buttons with which contents of the registers may be altered, with visible results. An internal maintenance panel makes the data bus and critical timing and control signals available for observation on an oscilloscope. The large display panel contains a color-coded computer organization diagram. As each instruction is executed the display shows with lighted areas, the register contents, information flow, and the cycle, phase, and mode of the operation. Standard operations that can be demonstrated include program interrupt applications and common addressing modes including direct, indirect, immediate, indexing, and relative addressing. Data Machines, Inc., Newport Beach, Cal.

Circle No. 250 on Inquiry Card

IC MEMORY SYSTEM

New one microsecond integrated circuit memory system has a 16,384 word, 18-bits-per-word storage capacity. It can be expanded to 32,768-words at 36-bits-per-word. Features of the system are said to include field-proven circuit modules to assure high reliability, complete front-panel accessibility (panels slide out and open like a book) and maximum flexibility with such options as a self-tester, read/modify/write operation, and easy interfacing with most data processing equipment. RCA Commercial Engineering & Components Div., Harrison, N. J.

Circle No. 216 on Inquiry Card

NEW PRODUCTS

LINE PRINTER

Line printer offers RFI shielding as an option. The specially-designed RFI cabinet totally encloses the printer, and is electrically and mechanically sealed to preclude emission of radiated frequencies. Line filters are provided for reduction in conducted signals. RFI screening is incorporated in glass observation panels and other openings, with wave guide filters for air inlets and outlets. RFI gasking is provided at all joints within the cabinet. While intended primarily for security purposes, the RFI cabinets provide additional noise reduction, and greater protection from environmental extremes. Data Products Corporation, Culver City, Cal.

Circle No. 257 on Inquiry Card

1/2-RACK POWER SUPPLIES

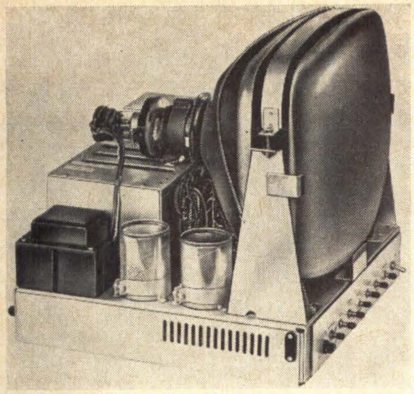
A new series of convection-cooled, all-silicon regulated power supplies offers voltages up to 36 VDC with current ratings up to 13.5 amps. Suitable for rack or bench mounting, these power supplies, designated the LK Series, have multiple current ratings based on ambient temperatures of 40C, 50C, 60C, and 71C for maximum application flexibility. One model is said to offer the highest current available in a half-rack unit. Adjustable, automatic electronic current limiting circuit limits the output current to the preset value upon external overloads including direct short, thereby providing protection for load as well as for power supply. Line regulation is 0.015% or 1 mv, whichever is greater for no-load-to-full load or full-load-to-no load. Lambda Electronics Corp., Melville, L. I., N. Y.

Circle No. 229 on Inquiry Card

NEW STEPPING MOTOR

Compact stepping motor, operating on a new principle, is a simple and accurate device for converting electrical pulses into a continuous rotary output of 10 discrete increments per revolution. Because of its 10-step operation, the motor is said to be ideally suited for use in visual readout counters, rotary switches, and other light-duty decimal applications. Gearing can be provided to give counts in units other than 10. To that end, a 12-step motor is already under development. The new stepping motor, trade-marked Roto-Netic consists of a linear solenoid, a spring-loaded plunger-type armature, and a ratchet-and-pawl actuator on the end of the plunger that turns the output shaft. When the solenoid is energized by a pulse, the plunger is drawn into the coil against the tension of the spring. When de-energized, the spring forces the plunger back into the rest position, driving the actuator against a 10-tooth starwheel, and producing rotation corresponding to one tooth or 36°. The actuator prevents the starwheel from rotating more than 36°, and a pawl prevents reverse rotation. The output element is on the same shaft as the starwheel. Each step is precisely the same as all others. Because the power stroke occurs on de-energization, the last pulse is always recorded, even if power is lost. The Roto-Netic design offers a high torque to size ratio. The unit measures approximately 2" x 1-13/32" x 1⅝" overall and weighs just 6 oz, but continuous-duty starting torque is 0.1 in-lb. Roto-Netic motors are said to eliminate two problems of many stepping motor designs. First, there is no possibility of rotor overshoot (there's no wound rotor), and, hence, there's no need for overshoot compensation. Second, there is no need for lateral shaft movement compensation because there is no axial thrust motion (the output shaft simply turns on its axis). Operation is unidirectional, with clockwise or counterclockwise rotation available from a double-ended output shaft. The stepping speed is a nominal 600 operations per minute at rated voltage. Operation in the range of intermittent rotation to 800 per minute is possible. Life expectancy of the unit is several million operations. Heinemann Electric Co., Trenton, N. J.

Circle No. 241 on Inquiry Card



CRT DISPLAY

A real-time X-Y CRT display unit which will sell for about $500 in production quantities presents a dynamic CRT display of computer or other digital outputs when driven by a character generator. In addition to alphanumerics, the display can handle a number of computer graphics functions. A plug-in modular construction is used to permit the use of a common chassis for the greatest possible number of computer interface requirements. The electronics are all solid-state with the exception of a single high voltage rectifier tube. Integrated circuits are used in the Z-axis amplifier. Conrac Div., Giannini Controls Corp., Duarte, Cal.

Circle No. 273 on Inquiry Card

CARD READER

A new card reader for economical commercial applications senses all 960 holes of a standard 80-column card. Model 2981, designed for behind-panel installation with either vertical or horizontal card aperture, measures only 2⅝ x 7 x 9½" and requires a panel opening of ½ x 4¼". The low profile is said to make it ideally suited to multiple installations in rack or panel applications. Partially inserting the card, then rotating the handle on the front panel, causes the card to move into position and close the contacts. The card is ejected when the handle is rotated in the opposite direction. The 960 normally-open contact pairs are available with individual solder-cup outputs, bussed rows, bussed half-columns, or bussed column pairs. Amp, Inc., Harrisburg, Pa.

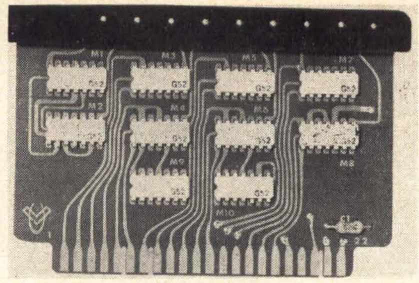
Circle No. 265 on Inquiry Card

NEW PRODUCTS

PC BOARD RACK

Close tolerances and rugged construction of a new type of printed circuit board are said to make it especially suited to mother-board high-density applications. The Series 55 Universal PCB rack is modular in design, and a variety of configurations and board spacings can be assembled with the pre-designed card guides, spacers, connector brackets, and end plates. Card guides are available insulated or non insulated. Structural components are steel, affording high strength over long spans. All parts are temperature-stable; close tolerances are maintained under varying temperature conditions, eliminating stresses on the mother-board. Birtcher Corp., Industrial Div., Monterey Park, Cal.

Circle No. 261 on Inquiry Card



20MC LOGIC CARDS

Complete family of IC logic cards for counting, shifting, and control functions provide input or clock rates from dc to 20mc. Eight different card types include multiple flip-flops and gate cards, an 8-stage shift register, and a crystal-controlled clock unit which supplies a 5mc to 20mc source. A line driver card provides amplifiers for twisted pair or coaxial line distribution of clock or interface signals. The new cards are compatible with company's 5mc cards. Control Logic, Inc., Natick, Mass.

Circle No. 252 on Inquiry Card

VOLTAGE REFERENCE

A new dialable voltage supply features $\pm 0.0025\%$ accuracy from 1 microvolt to 10 volts in an easily transportable case. The unit combines a dial-a-volt reference with a chopper stabilized operational amplifier providing totally isolated voltages. Remote sensing allows the calibrated voltages across the actual load at points distant from the output terminals. IR drops in interconnecting harnesses are automatically compensated insuring specified performance at the load. This unique feature is said to eliminate the primary source of interface errors in calibration consoles and systems. General Resistance, Inc., Bronx, N. Y.

Circle No. 266 on Inquiry Card

FREE RTL CIRCUITS

For evaluation, RTL integrated circuits are offered free to potential customers. Company believes that RTL can fill most industrial and commercial applications. Furthermore, it is said to be attractively priced for these markets. Samples of the complete RTL line, in military, industrial, and commercial grades, are available in both TO-5 type and flat packages. Sperry Semiconductor, Norwalk, Conn.

Circle No. 230 on Inquiry Card

HIGH VOLTAGE POWER

A series of fully-regulated high voltage power supply modules is for use with CRT's image pick-up tubes, photo multiplier tubes, and neon readouts. The series is line operated and covers voltage requirements from 200 to 2500 volts at 20 ma to 2 ma. The units are packaged in MIL-T-27 HA cases and feature independent line and load regulation and short-circuit protection with automatic recovery. The dc output is floating and adjustable. Important features include regulation at high voltage, self-recovering short-circuit protection at high voltage, completely silicon solid-state at high voltage, and unit is designed to be used as a component. High Voltage Power Supply Co., Van Nuys, Cal.

Circle No. 253 on Inquiry Card

TIME CODE READER

Time code reader is said to be a flexible and low-cost device for reading serial NASA and IRIG time codes. It accepts either NASA 36 bit or IRIG B serial, amplitude-modulated, carrier time code formats; converts the time code for decimal display of time; and provides parallel outputs, both decimal and BCD, for driving remote display units or for parallel entry into a digital data system, recorder, or computer. The unit can be used to read serial time codes from magnetic tape, data transmission terminals, or time code generators. High reliability at low cost is said to be achieved by extensive use of integrated circuits in modular building block form. Dynalectron Corp., Data Sciences Div., Silver Spring, Md.

Circle No. 204 on Inquiry Card

COMPUTER CAPACITORS

Computer grade electrolytics designed to cover all computer circuit requirements are said to make ideal selections for input filters on computer cards, translator assemblies, memory decoders, and storage and addressing assemblies. They feature cold-welded anode foil connections coupled with an all-welded design. Cornell-Dubilier Electronics, Newark, N. J.

Circle No. 237 on Inquiry Card

PROGRAM BOARD KITS

New matrix program board kits consist of one 10 x 10, two-level (X-Y), bussed contact switching matrix with screened panel, ten shorting pins, and ten diode pins. The diode pins may be supplied with or without the diode installed. Kit components may be purchased separately for applications where other amounts of pins or matrices are required. These kits may be used for such applications as cordless patch panels, programmable diode matrices, memories, function generators, circuit selectors, numeric control boards, and variable process programmers. Co-Ord Switch, Corona, N. Y.

Circle No. 222 on Inquiry Card

STEP-SERVO MOTOR

Said to be ideally-suited for computer, X-Y plotter, and similar digital systems applications, one of three new step-servo motors, a permanent magnet motor is only 1.434 in. long and weighs 4.0 oz. This 4-phase, bi-directional unit responds at rates to 120 pps in consistent 90 degree increments and delivers 0.6 oz-in running tourque and 1.2 oz-in stall torque on 5.2 watts power input. The second of the new motors, a 3-phase variable reluctance stepper motor responds at rates to 600 pps bi-directionally in accurate 15 degree increments. It operates efficiently on only 4.9 watts power input. Its small size (3/4 inch dia.), light weight (50 grams), and high speed are to make it suitable for a wide variety of computer, integrator, tape recorder, or digital control systems applications. The third unit, a variable reluctance motor, combines high speed, bi-directional response (900 pps, in precise 15 degree steps), with powerful (2.2 oz-in running torque, 6.0 oz-in stall torque) operation. IMC Magnetics Corp., Westbury, N. Y.

Circle No. 248 on Inquiry Card

INCREMENTAL ROTARY ENCODER

Precision optical shaft angle encoder is 1.375 in O.D. and weighs, with its integral electronic package, 3¼ oz. Two integrated circuit amplifiers are located on the back case. The 6-volt outputs may be fed directly into counters or other devices. The encoder can be used to measure or control speed of machine tools, tape transports, computer drums, and other equipment requiring a precision electronic tachometer. Standard pulse rates available "off-the-shelf" are: 1, 10, 30, 36, 50, 100, 120, 360, 500, 1000, and 1024 pulses per revolution. Virtually any other pulse pattern up to 1024 can be supplied to order. W. & L. E. Gurley, Troy, N. Y.

Circle No. 203 on Inquiry Card

SUBMINIATURE REED RELAY

Two new subminiature sealed-contact reed relays offer high switching capacity for printed circuit board application. The new modules provide for one through five Form A contacts, and occupy a maximum of 0.406 cubic inches for five contacts. Both relays offer a maximum current rating from low level to 750 ma and max voltage rating of 200 vdc, 110 vac max. Maximum load is 10 va; initial resistance is 100 milliohm max. Coil voltages range from 6 to 48 vdc. Inherent advantages of sealed-contact reed relays are said to include isolated coil and contacts that are insensitive to transients, and maintenance-free sealed-in-glass contacts that are not affected by contaminating environments and do not require adjustment. C. P. Clare & Co., Chicago, Ill.

Circle No. 233 on Inquiry Card

COMPUTER COAXIAL CABLE

A sub-miniature coaxial cable small enough to thread through the eye of a needle was designed for use in high-density circuits, particularly in the computer field, where complete RF shielding is mandatory. The 50-ohm cable has a solid jacket of precision-drawn copper tubing — 0.008" diameter and flexible enough to bend on a 1/16" radius. This jacket, combined with a 0.0020" solid copper center conductor and insulation of Teflon, forms a cable product that has accurately measurable mechanical and electrical properties. Its light weight and small size are added advantages for subminiature circuitry. MicroDelay Div., Uniform Tubes, Inc., Collegeville, Pa.

Circle No. 268 on Inquiry Card

IC MEMORY

New integrated circuit core memory is said to offer the features of both "off-the-shelf" and custom designed systems. Designated the CE-100, the memory system has a one-microsecond cycle time and is expandable to 4096 words by 36 bits in 4-bit increments. Expansion is accomplished by the addition of bit-oriented, plug-in logic boards and selection of magnetic modules. The user may custom design his system by selecting any portion of the pre-wired 4096 word by 36 bit capacity. However, he can change his design after the system is in use by specifying additional modules or stacks. The system requires seven inches of standard cabinet rack space, and the optional power supply requires another 5¼". The CE-100 uses integrated circuits in all but the high current circuits. Lockheed Electronics Co., Los Angeles, Cal.

Circle No. 210 on Inquiry Card

PAPER TAPE EDITOR

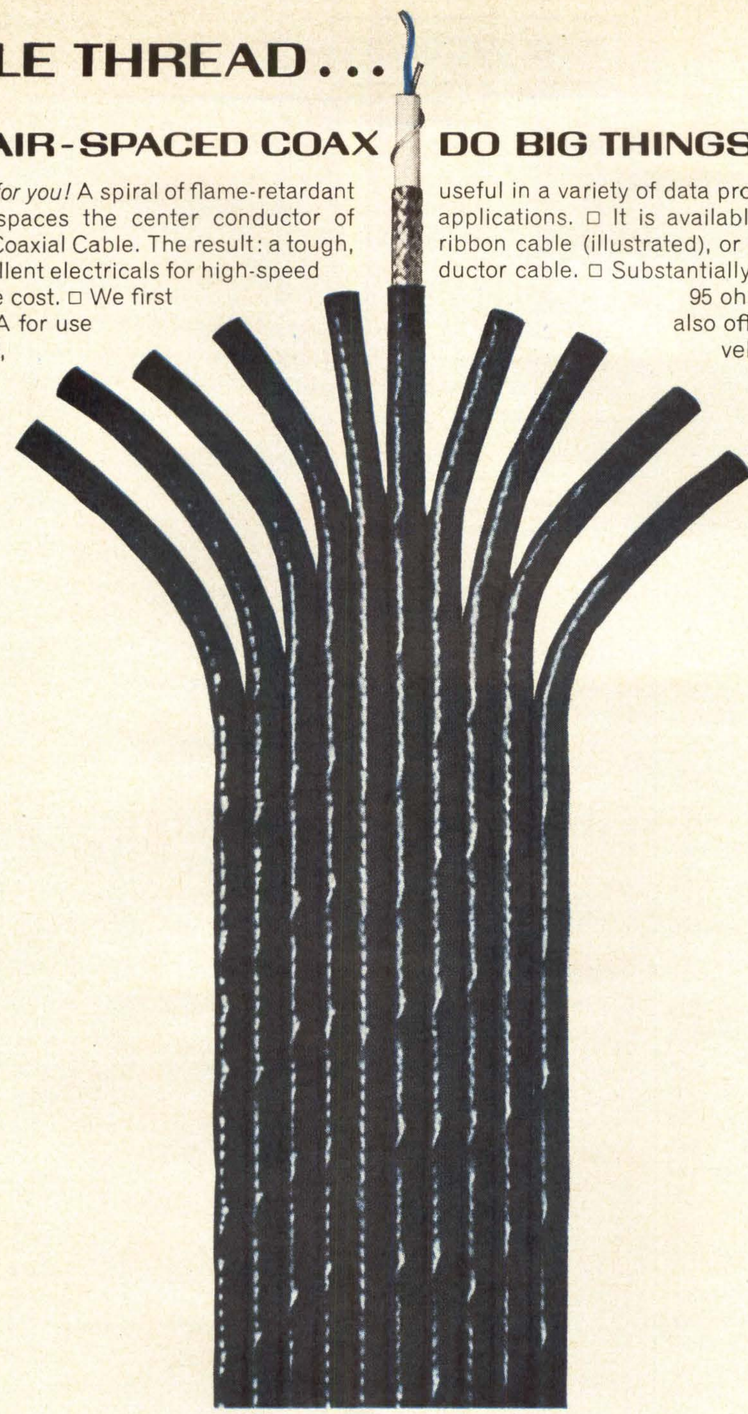
A new approach for the visual interpretation of paper tape messages and programs is said to be offered by a new paper tape editor. It contains a high-speed block reader which scans a 16-character segment of the tape and it immediately decodes each character and projects the appropriate alphanumeric symbol in proper sequence on a cathode ray tube. The message field on the screen remains stationary or travels in either direction as the tape is moved. The unit operates as simply as viewers that are commonly used in the editing of the motion picture films. It improves operator efficiency by eliminating the need for line printer or teletypewriter print-out for inspection of paper tape programs or messages. Since the display is "soft copy," no expandable paper or ribbon supply is required. The display is generated in a scan mode at the operator's desired rate, stopping only at message segments of interest. The unit is adaptable to 5-, 7-, or 8-level chad tape and reads all conventional paper tape materials, colors, and thicknesses. Data-Vox Corp., Sarasota, Fla.

Circle No. 236 on Inquiry Card

THIS LITTLE THREAD...

HELPS OUR AIR-SPACED COAX DO BIG THINGS FOR IBM

Our coax can do the same for you! A spiral of flame-retardant polyethylene thread air-spaces the center conductor of Brand-Rex Turbo® 209A Coaxial Cable. The result: a tough, miniature coax, with excellent electricals for high-speed transmission, at moderate cost. □ We first developed the Turbo 209A for use in the IBM Computer/360, but you may find this space-saving performer useful in a variety of data processing and communications applications. □ It is available as single cable, cemented ribbon cable (illustrated), or conventional round multiconductor cable. □ Substantially lower in price than standard 95 ohm High Temperature types, it also offers lower attenuation; higher velocity of propagation. A spiral drain wire under the shield simplifies termination.



Check the specs. Sound good? Write for full information.
Brand-Rex Turbo 209A Coax U.L. Approvals. Style 1354 (single), Styles 2384, 2385, 2386, 2387, 2388 (cable).
Nominal voltage: 600 volts rms.
Nominal impedance: 95 ohms, +6 −4.
Nominal capacitance: 13.5 pf/ft.
Max. attenuation: 14 db/100 ft at 400 Mc.
Velocity of propagation: 80%.
Inner conductor: #29 AWG silver-coated Turballoy C.
Cable core: Air-spaced, flame-retardant polyethylene. 0.072/0.078″ O.D.
Drain wire: #29 AWG silver-coated Turballoy C spirally applied for flexibility and fatigue resistance.
Shield: #38 AWG tinned copper braid, providing 90% min coverage.
Jacket: High-density vinyl, 0.112″ nom. O.D.; 0.122″ max O.D. at drain wire points.

CIRCLE NO. 36 ON INQUIRY CARD

AMERICAN ENKA CORPORATION
BRAND-REX DIVISION
Willimantic, Connecticut 06226
Phone: (203) 423-7771

NEW PRODUCTS

IC BREADBOARD

New integrated circuit breadboard was designed for use with 14-pin, dual in-line plastic packages. Designated XC73, the 16-socket breadboard permits rapid designing and evaluation of integrated circuits or complete logic designs without damaging individual integrated circuits. Little or no soldering is required, and breadboards may be interconnected to design and test complex systems. Continuous voltage planes on each side of the board provide even voltage distribution and reduce signal crosstalk for operation at high frequencies. Eleven BNC coaxial connectors and one 22-pin edge connector are provided for applying input and output signals. Motorola Semiconductor Prods, Inc., Phoenix, Ariz.

Circle No. 272 on Inquiry Card

PLATED-WIRE MEMORY

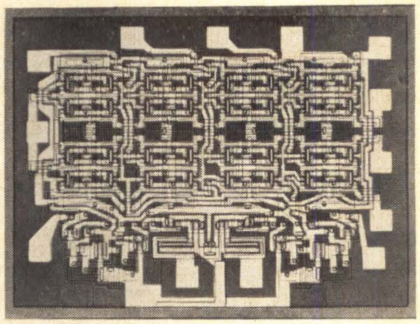
A new electronic memory that is woven automatically on a loom is available as a production item. The new memory, called Woven Plated-Wire Memory (WPWM), offers an access speed of less than 100 nanoseconds. In addition, the memory is said to provide significant savings in space, weight, and power. It can be used in computers, telemetry systems, control systems, and other advanced systems in either nondestructive readout (NDRO) or destructive readout (DRO) configurations. The basic elements of the new memory system are copper wires with a thin-film magnetic coating which are interwoven with epoxy-insulated wire. Memory elements are formed at intersections. The plated wires form the digit/sense lines and storage medium, while the insulated wires form the word lines. The weaving process, according to the company, provides better coupling of digit lines and word lines than is possible with nonwoven plated-wire memories, so that considerably lower word drive currents are required. General Precision, Inc., Librascope Group, Glendale, Cal.

Circle No. 269 on Inquiry Card

IC MODULES

A complete family of general-purpose integrated circuit logic modules features operation to 5 MHz with low power consumption and high immunity to noise. All modules are epoxy glass printed circuit boards 3.5" x 5.75" x 0.062" and have all outputs and inputs available at the pins of a high density 72 pin connector. Monolithic silicon integrated circuits are used for the basic logic functions and high quality discrete components and silicon semiconductors are used where better performance may be obtained through the use of hybrid circuits. A line of short-circuit +5 VDC power supplies providing currents from 2 to 25 amps is available for use with the modules. Information Control Corp., Abacus Div., El Segundo, Cal.

Circle No. 226 on Inquiry Card



16-BIT MEMORY CELL

Integrated circuit flip-flop memory cell is rated for −55C to +125C operation. Each memory element consists of 16 two-transistor flip-flops, arranged in a 4 x 4 matrix, which provides the information storage. Two write and two sense amplifiers are also built into the element. Both data and data complement are available at the sensing outputs, which can be paralleled for use in larger arrays. Addressing, read and write levels are compatible with other high level TTL circuitry. IC memory design results in a non-destructive readout element exhibiting delay of 20 nsec between addressing and read or write. All memory elements are available in 14-lead flat packages or 14-lead dual in-line (plug-in) packages. Transitron Electronic Corp., Wakefield, Mass.

Circle No. 231 on Inquiry Card

BUFFER MEMORIES

A new line of flexible low-cost data storage units are aimed, initially, at applications in time buffering such as block formatting from random rate inputs into synchronous systems, specifically magnetic tapes and other serial mediums, and non-competitive input-output channels. First units will have a capacity of up to 24 bits and up to 4,000 words. Tentative specifications for the first buffer memory call for a full cycle time of 1.6 microseconds buffer or half-cycle time, and random, sequential, and sequential interlace modes of operation. Proposed pricing will parallel main frame storage costs per bit. Fairchild Memory Products, Mountain View, Cal.

Circle No. 227 on Inquiry Card

LOW-COST COMPUTER

A low-cost, high-speed digital computer was designed principally for the control field. It has definite applications for process control, real-time counting, sequence control, and data acquisition. The same unit with a different display panel can be used in the education field for teaching computer usage, mathematics, physics, logic, and programming. The general-purpose computer for control is a 16-bit unit selling for $6,000, while the education unit sells for $6,700. Interdata, Farmingdale, New Jersey.

Circle No. 221 on Inquiry Card

CABLE STRAPS

Two new solid head cable straps accommodate several methods of mounting. These nylon cable straps can be drilled for any size mounting screw or they can be drilled to accept inserts and bushings. Each has a bundle range from 1/16" to 1¾". They have been designed to provide a simple method for tying and clamping wire bundles, harnesses, conduit runs, etc. The strap is fastened around the wire bundle, and using the head which can be adapted to the desired mounting method, the unit is fastened to the structure. The Thomas & Betts Co., Elizabeth, N. J.

Circle No. 251 on Inquiry Card

NEW PRODUCTS

NEW WIRING SYSTEM

A new wiring system consisting of convoluted tubing and specially designed end fittings to terminate the tubing directly to electrical connectors is currently offered in Teflon tubing with aluminum end fittings to accommodate all circular connectors conforming to MIL-C-5015, MIL-C-26842, MIL-C-26500, and NAS-1599. Fittings are also available to accommodate rectangular rack and panel type connectors such as DPX, DPA, and D-submarine. Called the Conflex system, it is said to offer all the advantages of a closed, sealed system, yet end fittings can be uncoupled for termination inspection or modifications. Additional conductors may be added and the entire system resealed by recoupling end fittings to the connectors. Significant space and weight savings are also claimed through deletion of connector end bells and potting, and reduction of insulation on wiring within the Conflex conduit. Conflex tubing is extremely flexible and can withstand continuous flexing. Long conductor life during flexing can be expected since the individual wires are free to find their own positions of minimum stress. Terminations of the tubing are made with a set of simple, lightweight aluminum fittings which form a tight mechanical seal. Panel and connector adapters screw into basic fittings as required, and special locking devices can be specified when vibration is a critical consideration. Included in the range of fittings are units which allow for the termination of a small wire bundle to a larger connector shell size. Icore Electro-Plastics, Sunnyvale, Cal.

Circle No. 254 on Inquiry Card

ECONOMIC IC TESTER

A new integrated-circuit test system, designed to reduce testing costs for semiconductor manufacturers and users, is suitable for measurements as basic as slice probing or as complex as device evaluation in system designs. Designated the Model 668 Test System, it features high-speed testing, simplified low-cost programming, small size, and versatile operation. The unit performs dc and diagnostic tests for the production, quality-control, inspection, and probing functions. The system also accommodates device evaluation tests on individual ICs and special tests on modules and arrays. Standard eight-level EIA code is used in programming the system. With a variable word-length format, virtually unlimited data may be entered serially (by means of a tape reader or from a 100 KHz character-rate computer). Normal tests are performed in 8 msec; longer test times (to 100 msec) as well as a programmable "hold" are available. Any test can be repeated continuously, or the system can be manually stepped through a series of tests one-at-a-time. New tests and/or modifications are easily programmed manually via front-panel controls. Texas Instruments, Industrial Products Group, Houston, Texas.

Circle No. 211 on Inquiry Card

HYSTERESIS MOTORS

A variety of "inside-out" hysteresis synchronous motors are available for applications in business machines, memory drum drives, radar scanners, antenna drives, printers, and capstan drives. Motors with up to 12 poles and with pull-out torques up to 200 ounce-inches can be supplied in diameters up to 5.5 inches. Advantages of these inverted hysteresis synchronous motors, according to the manufacturer, are that their rotors have inherently higher inertia than the conventional designs, and that they lend themselves to economies in manufacture which lower the cost for the user. Speed constancy is excellent because the stored energy in the high-inertia rotor reduces "hunting" and flutter. The ½ horsepower model provides a pull-out torque of 100 ounce-inches, although stack length is only ⅝". The Singer Company, Diehl Div., Somerville, N. J.

Circle No. 213 on Inquiry Card

DIGITAL-ANALOG MULTIPLIER

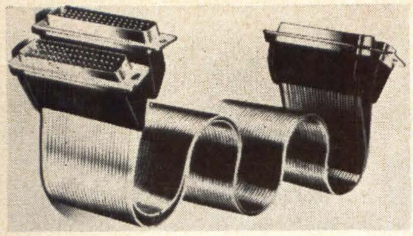
New hybrid multiplier system contains up to 8 D-A multiplier channels in a single rack-mountable housing. The system provides an economical data link between analog and digital computers. It operates directly with analog variables up to ±150 volts and accepts parallel 14-bit digital variable at 500KC rate. The system performs with an operational error of less than 0.01% of full scale and operates directly upon an analog input up to ±150 volts without preliminary scaling. Digital representation of negative signed-data is accepted in either one's complement or two's complement format. Digital input buffer registers are available in single rank or double rank models. Second rank storage allows for random acquisition of data which is to be held until required for simultaneous transfer to first rank storage for next computation. Lancer Electronics Corp., Norristown, Pa.

Circle No. 214 on Inquiry Card

STATIC CARD READER

Weighing only 12.5 pounds (wired complete with 1-foot lengths of wire), a new static card reader is suitable for use on portable equipment. The high-impact plastic dust cover extends only 2¾" above the mounting surface. Protective circuitry senses full insertion and proper orientation of the card. Further protection is provided by an auxiliary safety switch which closes after all the reader switches are operated on card insertion, and (on card withdrawal) opens before any card reader switch operates. The 960 switches can be normally open or normally closed, and are rated at 0.5 ampere (each) with a 28 volt dc resistive load. Contact resistance is less than 100 milliohms at 100 milliamperes, and contact insulation is over 750 megohms at 500 volts. AMP Inc., Harrisburg, Pa.

Circle No. 224 on Inquiry Card



FLAT-CABLE ASSEMBLIES

Flat-cable assemblies consist of multiple ribbons of flat copper conductors uniformly spaced and laminated between Mylar or Teflon insulation, straight or corrugated. The flat cable can be terminated to itself or welded to any connector type using a reliable all-welded technique. Since welding is performed through the insulation, stripping of the cable to make the termination is eliminated. To prevent stress concentration where the change in cross-section occurs in the termination area, flexible potting around the welded junction is standard. The result is a durable termination which matches the flex-life of the flat cable. These assemblies are said to offer up to a 50% combined size and weight reduction over comparable round-wire cable assemblies. ITT Cannon Electric, Los Angeles, Cal.

Circle No. 256 on Inquiry Card

PANEL INDICATORS

A new modular panel indicator features a fast, versatile, snap-together assembly technique. Up to ten or more of these modules may be locked together merely by snapping one module into another and a mounting bracket onto either end of the assembly. The indicator lamps are accessible from the front panel. Using this system, any indicator requirement may be made up from one basic component plus mounting brackets and lenses. Each individual module measures 0.43″ sq. and is 1.4″ deep. The lamp socket accepts a standard T-5.5 miniature lamp (6 to 60 V). Either round or square lenses are available in several colors. Typical price for a 10-module indicator assembly is $5.45 in 100 quantity. International Electro Exchange Corp., Minn., Minn.

Circle No. 274 on Inquiry Card

NEW PRODUCTS

PC CONNECTOR

Printed circuit board connectors with selectively gold-plated contacts and 0.045" square tail wire wrap terminations are currently available as 15, 22, and 36 position units. These new connectors, with 0.156" centers, are said to combine the contact reliability of a heavily gold-plated flexing bifurcated contact with the stability of a rigid 0.045" square tail termination. This combination is achieved by using the appropriate flexible contact material required for the bifurcated contact section and forming it around a wire core to make the termination section of the contact. The 0.045" square tail connector thus formed has the extremely sharp corners necessary for reliable wire wrap attachment. The contacts in these connectors use a selective gold plating process which reduces gold requirements over 60% while maintaining contact reliability and durability of electrical performance. By this technique, a 50 microinch gold plating can be applied to the contact mating surface area only, while 10 microinches of gold is applied to the remainder of the contact. Cinch Manufacturing Co., Chicago, Ill.

Circle No. 244 on Inquiry Card

CURRENT DRIVERS

New current driver has been designed to deliver dual current pulses identical in rise time, fall time, pulse delay, and pulse width. In many memory test applications employing coincident current storage techniques, this one driver can serve effectively as two individual drivers. Output A can drive an X-axis line while output B drives a Y-axis line. Since the current pulse parameters of both outputs are adjusted coincidentally with a single set of controls, the dual output design is said to diminish test set-up time. Current amplitudes of the output pulses can be adjusted independent of one another over a continuous range of from 50 ma to 600 ma. The full rated 1 amp output of the driver can be achieved by throwing a front panel switch which busses the two outputs together internally. The Model 1720 is also a true bi-polar current driver, developing positive or negative pulses dc referenced to ground by the simple flick of a front panel polarity switch. The output voltage rating is 60 volts, positive or negative, and the driver is capable of withstanding a back emf of the same magnitude without damage. The 60 volt output coupled with a low output capacitance of 40 pf (worst case), combine to equip the driver with the ability to drive large inductive loads. Pulse width is variable from 10 ns and pulse delay from 0 to 10 ms. Computer Test Corp., Cherry Hill, N. J.

Circle No. 271 on Inquiry Card

VERSATILE OSCILLOSCOPE

Designated the Model 802 "Memo-Scope" storage oscilloscope and the Model 831 standard oscilloscope, both instruments offer single-switch selection of seven operating modes which provide single channel operation, A or B channel at 5MHz and 20mv/div sensitivity; dual channel operation chopped or alternate; A and B added algebraically; X-Y operation fully-calibrated in both A(y) and B(x) axis; and high gain differential with 2 mv/div sensitivity, 1000:1 common mode rejection and 600 kHz selectable bandpass. The 802 and 831 scopes are said to feature a new, highly-reliable triggering system that not only provides stable triggering far beyond the bandpass of the scope, but also exceptional single shot triggering for storing single shot phenomenon. No stability control is required. A new internal packaging scheme is used that arranges circuit boards radially around the CRT shield. This is designed to simplify calibration and service, and improve cooling. Commenting on the absence of plug-ins in both of the new scopes, the manufacturer stated that by building-in broad capabilities and eliminating the plug-ins, many problems are eliminated such as time lost changing plug-ins, recalibrating, warmup time, and overdesign to accommodate differing plug-in requirements. Storage specifications claimed for the 802 unit include a typical writing speed of 5,000,000 cm/sec and 20 foot-lamberts brightness for stored traces. Stored information can be retained for many hours until intentionally erased. Hughes Instruments, Oceanside, Cal.

Circle No. 235 on Inquiry Card

IC BOARDS

Printed circuit boards for permanent mounting of TO-5 cans have been added to a line of general-purpose computer components and accessories. These printed circuit boards are said to incorporate features which permit circuit interconnection flexibility and to lend themselves to all stages of digital equipment development from breadboard to final production. A large 4.50″ by 9.25″ size mounts up to 16 cans with 8-pin configuration while a smaller 4.50″ by 6.06″ board accepts 8 cans. Circuit functions may be jumpered or permanently wired in numerous ways. Jack-jack or terminal configurations are available on each card size to facilitate the engineer's choice of connection. All jacks are sized for 0.040″ patch cord plugs. Cambridge Thermionic Corporation, Cambridge, Mass.

Circle No. 249 on Inquiry Card

PORTABLE COMPUTING SYSTEM

General-purpose data acquisition and on-line computing system completely self-contained in a portable cabinet, can scan and digitize up to 10 analog signals, perform computations on the input data, and provide output records in typewritten and punched tape form. Input instructions may be entered through either the computer or the Teletype keyboard. Programmed instructions are read from dual card readers having a total capacity of 160 instructions, or punched tape with an unlimited program capacity. A 3-reel tape handler is built in. The system includes a total of 16, 10-digit and 10, 4-digit storage registers. Wang Laboratories, Incorporated, Tewksbury, Mass.

Circle No. 207 on Inquiry Card

ANALOG MEMORY

New analog memory, a hybrid of digital and analog circuitry, is a unity gain track and hold amplifier with high input impedance, high frequency response in the track mode, and zero decay in the hold mode. Track mode small signal bandwidth extends from dc to 150KHz. Hold mode accuracy is better than ±0.05% of full scale for an infinite time period. Aperture error is less than 100 nanoseconds after an acquisition time of 6 microseconds. In the track mode, the unit's digital circuitry is disabled and the instrument functions as a tracking amplifier with linearity of ±0.01% of full scale. In hold mode, the circuitry becomes hybrid and consists of a memory capacitor, recharge circuit, digital clock, and output buffer amplifier. It can retain sampled voltage in an analog state for thousands of hours with a long-term drift of less than ±0.05% of full scale (non-cumulative). The unit's modular construction allows the user to obtain the precise number of channels for initial requirements and easily expand later to meet growing system needs. La Jolla Div., Control Data Corp., La Jolla, Cal.

Circle No. 201 on Inquiry Card

NEW PRODUCTS

POSITIVE THERMISTORS

New thermistors exhibit an increase in resistance (as opposed to the conventional "negative," thermistors decrease in resistance) with increasing temperature up to 50% of instantaneous value per degree centigrade. Made from doped barium titanate, these devices, called Positemp, may be used at temperatures at 170C. Useful for temperature stabilization, temperature control, and temperature reference, the thermistors can also be used as current limiters and liquid and air flow detectors. Utilizing the Curie point change in the materials from which the devices are made, the switching point of the devices — defined as that point which is five times the nominal room temperature resistance value — is a function of the materials and does not change with time. This ensures repeatable and reliable performance of the devices throughout their life. Positemp thermistors with switching temperatures in ten degree increments are currently available in the range from 55C to 165C. Repeatability of device behavior at switch point is $\pm$1C. Pennsylvania Electronics Technology, Inc., Pittsburgh, Pa.

Circle No. 228 on Inquiry Card

SUPERVISORY CONTROL

An advanced, high-speed, supervisory control system is capable of automatically controlling electric utility plants, pipeline systems, water and sewage systems, industrial processes, traffic systems, and railroads. It utilizes standard communications facilities, such as telephone lines and microwave channels. Control signals, and other data pertinent to supervising a specific operation, are exchanged between a central master station and remote stations by means of frequency shift tones. The solid-state logic and automatic address verification ability of the control system enable it to scan up to 180 points per second automatically, acquire analog and digital data from a large number of remote locations, log remote and local data, and read telemetric measurements. The status of a typical remote station can be updated and recorded every 24 milliseconds. Standard interface modules make it possible for the system users to integrate most computers into their equipment. Thus, the new control system, in conjunction with a high-speed digital computer, is said to be suited to on-line, real-time control applications. An important feature of the control system is its economy. It requires but one communication channel to handle all control, supervision, telemetering, and data logging functions, thereby eliminating the expense of multiple communication channels. Floor space required for the system has been minimized by mounting all circuit components on swinging panels, allowing cabinets to be placed permanently against the wall. Control Corp., Minneapolis, Minn.

Circle No. 246 on Inquiry Card

METAL SUBSTRATE PC BOARDS

Insulated metal substrate printed wiring boards are said to be far superior in most respects to conventional printed circuit boards. In the boards the insulation resistance of the coating exceeds 500 megohms at 95% R.H. and 95C. The circuitry is applied by flame spray and is not dependent on organic adhesive for its bond and peel strength. The metal substrate can be utilized not only as a structural member but also as a thermal dissipator as well. These boards are available to customer specifications in single-sided, two-sided, and multi-layer boards. Integronics, Inc., Subs. of Solitron Devices, Inc., Tappan, N.Y.

Circle No. 212 on Inquiry Card

FREQUENCY TOTALIZER

A new line of solid-state totalizers featuring a 1¾″-high front panel with 3 to 6 decades is said to be especially designed for those applications where panel space is a premium and economy is a factor. Input is square wave or positive pulse with amplitude 6 volt pk-pk. Rise time is 1 microsecond maximum and duration is 4 microseconds minimum. Frequency range is 0 to 200 KC. Options available include digital printer output, a 6-digit mechanical totalizer, a pre-amp to provide 10 mv sensitivity and +12 vdc level gating, or another pre-amp to provide 10 mv sensitivity and 2-line pulse gating. Anadex Instruments, Inc., Van Nuys, Cal.

Circle No. 209 on Inquiry Card

CARD-COOLING BLOWER

Heat removal from groups of solid-state cards closely confined in compact enclosures is said to be easy and economical with a new 290 cfn blower. Units take up minimal rack space (3½″ or 5½″) and are available with 4 choices of air discharge. Each unit contains a motor guaranteed for thousands of hours of uninterrupted service-life. McLean Engineering Laboratories, Princeton Junction, N. J.

Circle No. 220 on Inquiry Card

LITERATURE

PC Board Packaging

A new 8-page catalog covers a low-cost printed circuit board packaging system. Comprised of detailed exploded-view drawings, performance charts, specifications, and descriptive information, the publication explains the system's highly reliable, versatile, and economical features. The system is designed to accommodate up to ten two-sided printed boards in card sizes of 4″ x 5″ through 12″ x 15″. By employing low-cost two-sided boards, connections can be made economically by wave or flow soldering. Significantly, the system has been specially designed for cam-actuation of contacts, providing zero mating and unmating forces capabilities. This special feature eliminates PC pad damage during insertion or withdrawal of the PC boards. The packaging system also features all-aluminum construction and high-speed logic capabilities due to minimum length circuit paths. For use with discrete components or integrated circuits with flat or right angle leads, the system is said to be ideally suited for packaging digital logic circuitry employing dual-in-line or similar integrated circuits. ITT Cannon Electric, L. A., Cal.

Circle No. 308 on Inquiry Card

Lacing Tapes

Brochure covers quality control methods and laboratory testing routines applied to the manufacture of electronic lacing tapes. Twenty pages are devoted to the various phases of laboratory control over raw materials and manufacturing processes. Illustrations show the types of test equipment employed. The descriptions of test procedures can be a guide to purchasers of the lacing tapes in setting up their own testing methods. Gudebrod Bros. Silk Co., Inc., Phila., Pa.

Circle No. 316 on Inquiry Card

Control Modules

Performance-proved control module boards for use in digital control systems are described in a new 4-page folder. The modules are comprised of NPE relays mounted on printed circuit boards. The NPE units are produced with either miniature or standard-size switch contacts for maximum design compatibility of space and load handling requirements. Descriptions of the functions performed by the modules — decimal counting, binary counting, logic, and selection — are included. Wabash Magnetics, Incorporated, Wabash, Ind.

Circle No. 319 on Inquiry Card

Special-Purpose Computers

Instrumentation and methods for on-line reduction of random data are described in a set of data sheets. Among the techniques discussed are signal averaging, autocorrelation and crosscorrelation, time and amplitude density computations, digital integration, and expansion and contraction of the time base of electrical signals. The set of seven data sheets also contains complete specifications for a "computer of average transients" series and for compatible analog and digital readout devices. Technical Measurement Corporation, North Haven, Conn.

Circle No. 310 on Inquiry Card

PC Connectors

New catalog, 20 pages in length, contains photographs, descriptions, ratings, and engineering drawings of a full line of printed circuit connectors and fork contacts. Application data is provided with complete industrial and military specifications. Methode Electronics, Inc., Chicago, Ill.

Circle No. 307 on Inquiry Card

Power Supply Catalog

Catalog purchasing guide presents a complete range of power supplies including ac to dc, dc to ac, ac to ac, dc to dc models for industrial and military use. The catalog lists full data, drawings, block diagrams, price and photos of certified mil spec dc modules (with certification details), industrial type modules, unregulated modules, variable supplies, inverters, frequency changers, and high-voltage supplies. Electronic Research Associates, Incorporated, Cedar Grove, N. J.

Circle No. 313 on Inquiry Card

Thumbwheel Switches

A new line of economical rotary thumbwheel switches is described in a new 4-page brochure which contains "how to use" instructions that take the purchaser from switch type to price list information in six steps. The 1100 Series requires only ½" of panel width and is approximately 2" high and 2⅝" deep behind the panel. A termination table provides cross reference between switch model, circuit board details, and terminal identifications. Engineered Electronics Co., Santa Ana, Cal.

Circle No. 321 on Inquiry Card

Function Generator

A 4-page engineering data sheet discusses two card-programmed diode function generators that minimize set-up time for analog or hybrid facilities. These units are designed to cut problem turnaround time, particularly for computer operations involving commonly-used functions, often-repeated problems, and multishift scheduling. The technical data sheet provides a complete description of the units, how they generate 10 or 20-segment functions or are slaved to a single variable, and complete operating specifications. Also included is the punched card layout, and a description of the software available to prepare the generator card from input raw data automatically. Electronic Associates, Inc., West Long Branch, N.J.

Circle No. 318 on Inquiry Card

3C offers, to its customers, a total digital capability; to our professional engineers we offer a dramatic, dynamic growth potential. Continued market acceptance of our new DDP-516, DDP-416 and DDP-124 computers, I/C logic modules and core memory systems has created key opportunities for professional design engineers with experience in integrated circuits, high speed switching circuits and A/D-D/A circuitry to work on our next generation of digital equipment.

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CIRCLE NO. 902 ON INQUIRY CARD

LITERATURE

Numeric Keyboard ASR

How rapid digital data communications can be accomplished by means of the Teletype Model 33 ASR (automatic send-receive) set with numeric keyboard is described in a new brochure. With the exception of the keyboard, the unit is identical to the standard Teletype Model 33 ASR set featuring page printing and paper tape punching and reading capabilities. Besides the numerals 0 through 9, the keyboard contains 4 alphabetical characters (A through D) to multiply the range of possible code combinations. Remaining keys control non-printing machine functions. Although the keyboard transmits only numerics and the four letters, the set can receive the entire range of alphanumerics in either page copy or punched paper tape form. Described in the brochure are illustrations of how the machine can be used in a variety of applications, including super-markets, department stores, banks, and industrial firms. The numeric keyboard is most effective when a number of stations periodically report large quantities of digital data to, or repeatedly order merchandise from a centralized location. Teletype Corp., Skokie, Ill.

Circle No. 306 on Inquiry Card

2½D Core Memory

New 4-page brochure describes a 2½D core memory stack with cycle times of 650 or 900 nanoseconds. The logical organization of a 2½D array, the detail wiring of one bit, and the overall construction of a typical 16,384 word, 18 bit are explained. Physical dimensions, number of words and bit lengths of standard types are given. The advantages of 2½D organization, including higher speeds, wider operating margins, lower supply voltages, and improved reliability are outlined. Electronic Memories, Hawthorne, Cal.

Circle No. 309 on Inquiry Card

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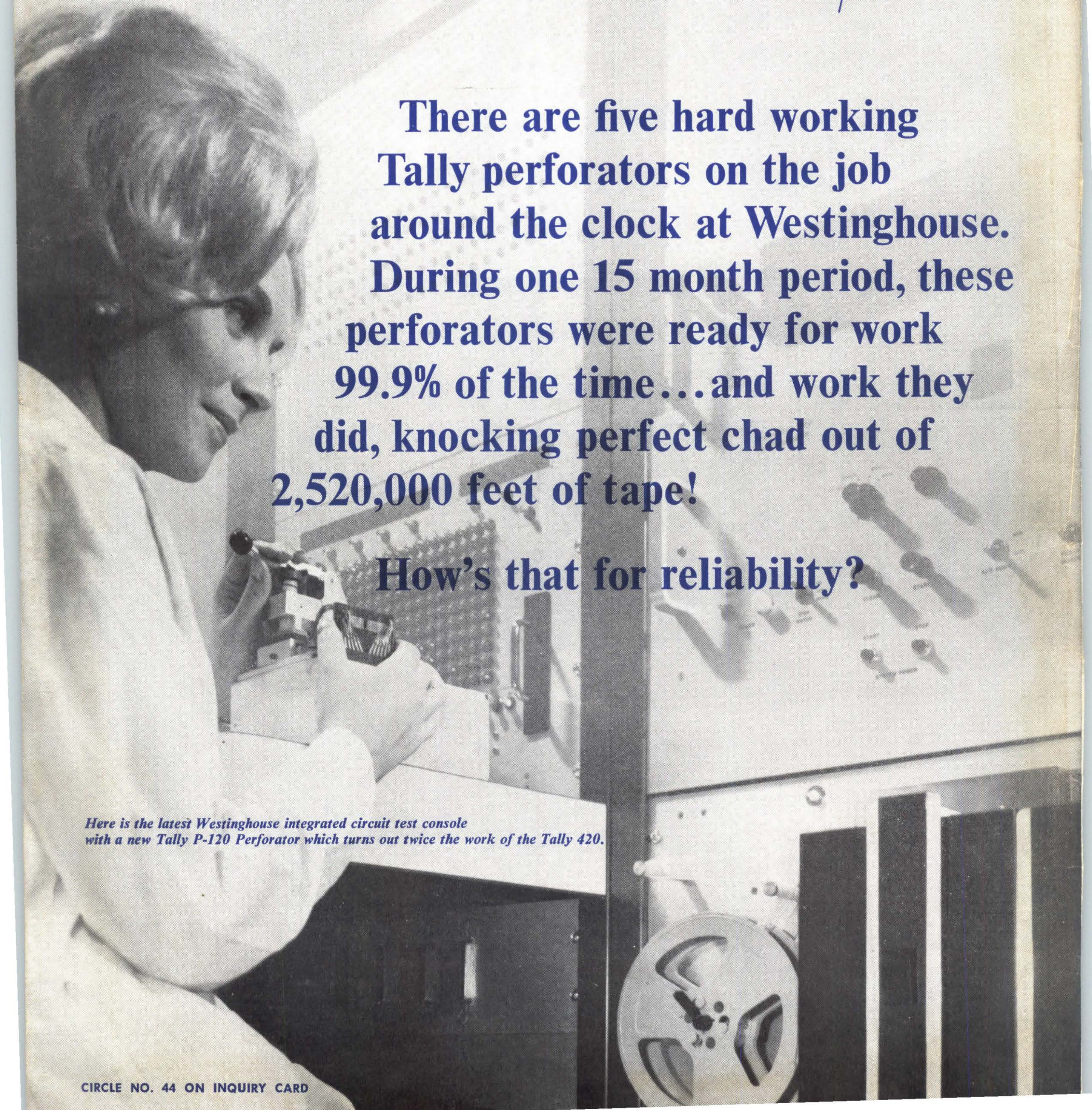
ADVERTISERS' INDEX

Testing integrated circuits is a key step in their production. At the Molecular Electronics Division of Westinghouse Electric Corporation, Tally perforators are used to log data as each module is run through a series of parameter checks. Data logged on the tape is then analyzed by computer.

According to W. DeLauder, Foreman of the Instrumentation Section at Westinghouse, the five Tally Model 420 perforators worked extremely well during a fifteen month period just ended. Fewer than eight calls per perforator were made to keep all five perforators on duty over the entire period. The average time per call was 2.23 hours with an average cost for parts of $3.05.

During the fifteen month period, the five perforators punched with precision over 478 miles of tape. There are a lot of good solid engineering reasons why Tally perforators are extraordinarily reliable. For all of them, please address Ken Crawford, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. In the U.K. and Europe, address Tally Europe, Ltd., Radnor House, 1272 London Road, London, S. W. 16, England.

TALLY



There are five hard working Tally perforators on the job around the clock at Westinghouse. During one 15 month period, these perforators were ready for work 99.9% of the time...and work they did, knocking perfect chad out of 2,520,000 feet of tape!

How's that for reliability?

Here is the latest Westinghouse integrated circuit test console with a new Tally P-120 Perforator which turns out twice the work of the Tally 420.

CIRCLE NO. 44 ON INQUIRY CARD