1. Introduction

CH384 is a PCI-Express bus converter chip, which converts PCIE bus to Quad serial ports and printer port, including four asynchronous serial ports compatible with 16C550 or 16C750, and one EPP/ECP enhanced bidirectional parallel port. CH438 chip can be added to extend 24 serial ports to the maximum. The asynchronous serial port provides a transceiver with independent 256-byte FIFO buffer, supports IrDA infrared encoding and decoding, supports communication baud rate up to 8Mbps and can be used for RS232 serial port expansion of PCIE bus, PCIE high-speed serial port with automatic hardware flow control, serial ports networking, RS485 communication, IrDA communication, parallel/printer port expansion, etc.

The figure below shows its general application block diagram.

2. Features

2.1. Overview

- The same chip can be configured as a four-channel serial ports and a parallel port/printer port or four-channel serial ports and extended multiple serial ports of PCIE Bus.
- Provides two-wire serial host interface, and EEPROM device similar to 24C0X which can be connected to store non-volatile data.
- The device identification (Vendor ID, Device ID, Class Code, etc.) of the PCIE board can be set in the EEPROM device.
- 3.3V power supply, I/O pins supports 5V withstand voltage, serial ports support low-power sleep
mode.
- The chip function is equivalent to CH367 with CH438, providing such application solutions as 8 serial ports, 16 serial ports and 28 serial ports.

2.2. Serial Port
- 4 fully independent asynchronous serial ports, compatible with 16C550, 16C552, 16C554 and 16C750 and enhanced.
- Supports 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Supports odd, even, mark, space and no parity.
- Programmable communication baud rate, supports communication baud rate of 115200bps and up to 8Mbps.
- Internal 256-byte FIFO buffer, supports four FIFO trigger levels.
- Supports MODEM interface signals CTS, DSR, RI, DCD, DTR and RTS, which can be converted to RS232 signals.
- Supports automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Supports serial port frame error detection and Break line interval detection.
- Supports full-duplex and half-duplex UART communication.
- Internal SIR infrared codec of serial port 0, supports IrDA infrared communication with baud rate from 2400bps to 115200bps.
- Supports to connect to external CH438 chips to expand another 8 to 24 asynchronous serial ports to realize 8 to 28 serial ports of PCIE.

2.3. Parallel Port
- Supports SPP, Nibble, Byte, PS/2, EPP, ECP and other IEEE1284 parallel port/printer port working modes.
- Supports bidirectional-data transmission and a transmission speed of up to 1M byte/s.

3. Package

<table>
<thead>
<tr>
<th>Package</th>
<th>Width of Plastic</th>
<th>Pitch of Pin</th>
<th>Instruction of Package</th>
<th>Ordering Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>LQFP-100</td>
<td>14mm x 14mm</td>
<td>0.5mm</td>
<td>Standard LQFP 100</td>
<td>CH384L</td>
</tr>
</tbody>
</table>

4. Configuration

4.1. Global Function Configuration
CH384 has two main hardware function modes: 4 serial ports and parallel port function mode, 4 serial ports and extended multiple serial ports function mode. The pin definitions are different in two function modes, and this manual only covers the former. Please refer to Datasheet (II) CH384DS0_2.PDF for the latter.

4S1P# pin of CH384 is used to select the software recognition mode:
- 4S1P# is connected to VCC33 or suspended, that is, when 4S1P#=1, it is 4 serial ports mode (parallel port/printer port is not used);
- 4S1P# is connected to GND, that is, when 4S1P#=0, it is 4 serial ports and printer port mode.

CKSEL pin of CH384 is used to select the clock frequency of the internal 4 serial ports:
- CKSEL is connected to VCC33 or suspended, i.e. when CKSEL=1, the clock is input from XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient is 1/12 frequency
division by default, and frequency doubling can be selected through CK2X or CKnS;

CKSEL is connected to GND, that is, when CKSEL=0, the clock is input from XO pin. The frequency is determined by the external crystal, and the internal frequency coefficient is always forced to be frequency doubling;

CKSEL is connected to PERST# pin, that is, when CKSEL=R, the internal crystal oscillator is disabled, the internal PLL provides the clock with a frequency of 125MHz, and the internal frequency coefficient is 1/68 frequency division by default, and supported to select no frequency division through CK2X or CKnS.

4.2. External Configuration Chip

CH384 will check the data in the external 24CXX configuration chip after each power-on or PCIE Bus reset. If the configuration chip is connected and the data is valid, it will be automatically loaded into CH384 to replace the default PCIE identification information.

The following table shows the data definition in the configuration chip 24CXX.

<table>
<thead>
<tr>
<th>Byte address</th>
<th>Abbreviation</th>
<th>Description of Chip Configuration Data Area</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>CFG</td>
<td>The valid flag of the external configuration chip, must be 54H</td>
<td>54H</td>
</tr>
<tr>
<td>01H</td>
<td>FREQ</td>
<td>Bit 3 to bit 0 are respectively used to select the internal frequency coefficient of serial port 3 to port 0</td>
<td>0FFH</td>
</tr>
<tr>
<td>03H-02H</td>
<td>RSVD</td>
<td>(Reserved)</td>
<td>0000H</td>
</tr>
<tr>
<td>05H-04H</td>
<td>VID</td>
<td>Vendor ID</td>
<td>Customize</td>
</tr>
<tr>
<td>07H-06H</td>
<td>DID</td>
<td>Device ID</td>
<td>Customize</td>
</tr>
<tr>
<td>08H</td>
<td>RID</td>
<td>Chip version: Revision ID</td>
<td>Customize</td>
</tr>
<tr>
<td>0BH-09H</td>
<td>CLS</td>
<td>Device type code: Class Code</td>
<td>070005H</td>
</tr>
<tr>
<td>0DH-0CH</td>
<td>SVID</td>
<td>Subsystem Vendor ID</td>
<td>Customize</td>
</tr>
<tr>
<td>0FH-0EH</td>
<td>SID</td>
<td>Subsystem ID</td>
<td>Customize</td>
</tr>
<tr>
<td>1FH-10H</td>
<td>RSVD</td>
<td>(Reserved)</td>
<td>00H or FFH</td>
</tr>
<tr>
<td>Other address</td>
<td>APP</td>
<td>User or application program custom unit</td>
<td></td>
</tr>
</tbody>
</table>

5. Applications

5.1. Quad Serial Ports + Parallel Port (Figure below)

This is the basic circuit for PCIE quad serial ports + parallel/printer port based on CH384. The figure does not include RS232 voltage conversion chip.

U3 is an optional external configuration chip, and the online configuration tool software for Windows system is available on the website.

IEEE1284 requires the printer port signals to keep impedance matching. Therefore, the parallel data signals of the printer port may be connected to resistors in series and capacitors in parallel, which can also be eliminated when the requirement is not high.

Crystal X1, capacitors C23 and C24 are used in the clock oscillation circuit. Other capacitors are used for power supply decoupling. The capacitor with a capacity of 10uF is a tantalum capacitor, and the capacitor with a capacity of 0.1uF is a monolithic or high-frequency ceramic capacitor, which are connected in parallel to the power pins of CH384 respectively.

CH384 is a high frequency circuit. Please refer to PCIE Bus specification or PCIE_PCB.PDF document when designing the PCB board.