TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY: TIBPAL20XX-5
DEVICES INCLUDED: TIBPAL20R4-5, TIBPAL20R6-5, TIBPAL20R8-5, TIBPAL20L8-5.

PROGRAMMING PROCEDURE:

Array fuses are programmed by executing the following programming sequence. Each fuse can be opened by selecting the appropriate (1 of 32) Input Line and (1 of 8) Product Line. The levels for selecting Input Lines and Product Lines are shown in Tables 1-2 and 1-3.

Step 1: Raise PGM ENABLE to V_{IHH}.
Step 2: Select an Input Line by applying appropriate levels to PI pins.
Step 3: Select a Product Line group by applying appropriate logic levels to PA pins. The actual product line selected will be determined by the PO pin (described in step 5).
Step 4: Raise /OE to V_{IH}.
Step 5: Raise the selected PO pin to V_{IHH}.
Step 6: Program the fuse by pulsing V_{CC} to V_{IHH}.
Step 7: Remove the output voltage.
Step 8: Lower /OE to V_{IL} to enable device.
Step 9: Pulse PGM VER pin to V_{IH}.
Step 10: Verify the blowing of fuse by checking for a V_{OL} at the selected PO pin.

If the fuse is still intact, steps 1 thru 10 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the Security fuse intact.

Security fuses are provided on each device to discourage the unauthorized copying of fuse patterns. To program the security fuse, follow the steps above omitting steps 2 and 10.

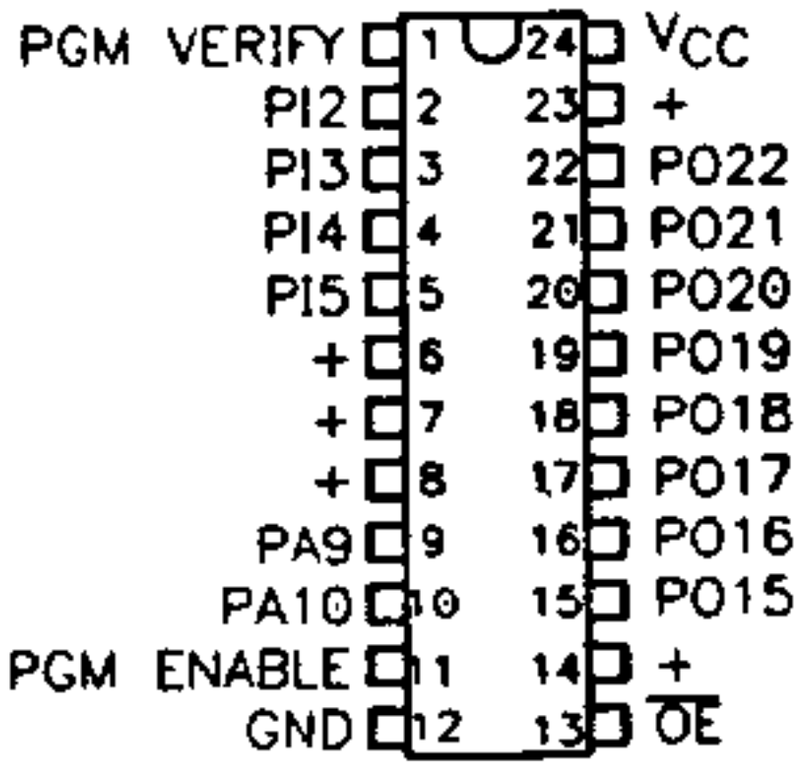
See Tables 1-2 and 1-3 for addressing information.

For programming waveforms, see Figure 1-1.

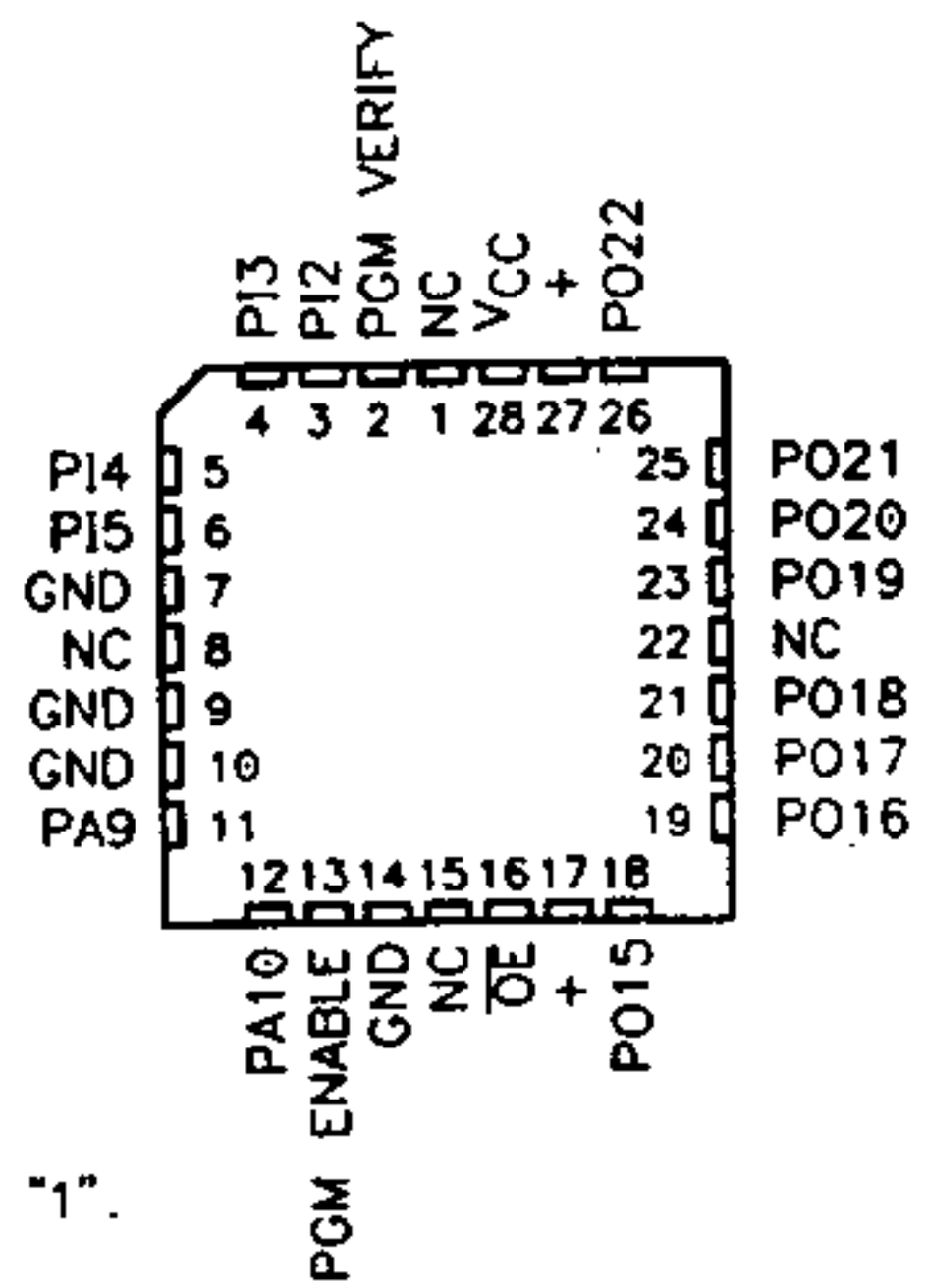
PREPARED BY B. Cole PAL24D-1.DWG DATE 03/24/90	TEXAS INSTRUMENTS			
CHECKED BY DATE 7/17/90	TITLE: ALGORITHM SPECIFICATION TIBPAL20XX-5			
ENGINEER DATE 7/18/90				
APPROVED BY DATE 7/18/90	REVISION B LETTER	A SIZE	PAL24012	SHEET 1 / 10
RELEASED BY DATE / /				

PIN ASSIGNMENTS IN PROGRAMMING MODE

JT or NT PACKAGE
(TOP VIEW)



FN or FK PACKAGE
(TOP VIEW)



+ = Set to logical "1".

TABLE 1–1, PROGRAMMING PARAMETERS, TA = 25°C

PARAM	DESCRIPTION		MIN	NOM	MAX	UNIT
V_{CC}	Verify–level supply voltage		4.75	5.00	5.25	V
V_{IH}	High–Level input voltage		2.40		5.50	V
V_{IL}	Low–level input voltage				0.50	V
V_{IHH}	Program–pulse voltage	PO	10.25	10.50	10.75	V
		PGM ENA	10.25	10.50	10.75	V
		PI, PA	10.25	10.50	10.75	V
		V_{CC}	10.25	10.50	10.75	V
I_{IHH}	Program–pulse current	PO		20	40	ma
		PGM ENA		5	15	ma
		PI, PA		2	10	ma
		I_{CC}			450	ma
t_{w1}	Program–pulse duration at PO		10		50	us
t_{w2}	Pulse duration at PGM VERIFY		100			ns
t_{su}	Set–up time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from /OE low to PGM VERIFY high.		100			ns
t_{d2}	Delay time from PGM VERIFY high to valid output.		100			ns

TABLE 1-2. INPUT LINE SELECT

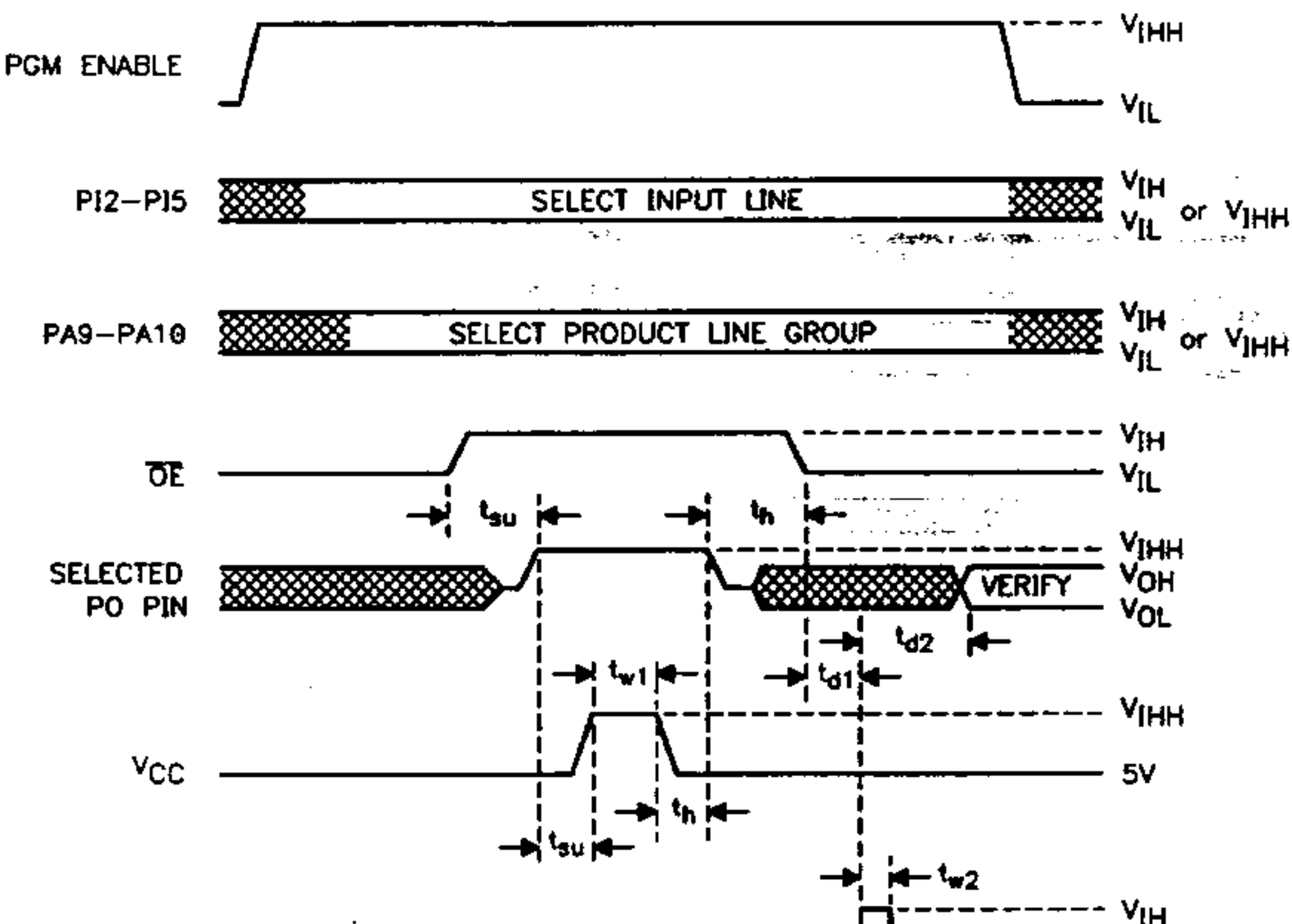
Input Line Number	Input Line Number–Address Pin States			
	PI2	PI3	PI4	PI5
00	L	L	L	L
01	L	L	L	H
02	L	L	L	HH
03	L	L	H	L
04	L	L	H	H
05	L	L	H	HH
06	L	L	HH	L
07	L	L	HH	H
08	L	L	HH	HH
09	L	H	L	L
10	L	H	L	H
11	L	H	L	HH
12	L	H	H	L
13	L	H	H	H
14	L	H	H	HH
15	L	H	HH	L
16	L	H	HH	H
17	L	H	HH	HH
18	L	HH	L	L
19	L	HH	L	H
20	L	HH	L	HH
21	L	HH	H	L
22	L	HH	H	H
23	L	HH	H	HH
24	L	HH	HH	L
25	L	HH	HH	H
26	L	HH	HH	HH
27	H	L	L	L
28	H	L	L	H
29	H	L	L	HH
30	H	L	H	L
31	H	L	H	H
32	H	L	H	HH
33	H	L	HH	L
34	H	L	HH	H
35	H	L	HH	HH
36	H	H	L	L
37	H	H	L	H
38	H	H	L	HH
39	H	H	H	L
SF	X	X	X	X

TABLE 1–3, PRODUCT TERM AND PO SELECTION

PRODUCT TERMS								Address Pin States		
PO22	PO21	PO20	PO19	PO18	PO17	PO16	PO15	PA9	PA10	
00	08	16	24	32	40	48	56	L	L	
01	09	17	25	33	41	49	57	L	H	
02	10	18	26	34	42	50	58	L	HH	
03	11	19	27	35	43	51	59	H	L	
04	12	20	28	36	44	52	60	H	H	
05	13	21	29	37	45	53	61	H	HH	
06	14	22	30	38	46	54	62	HH	L	
07	15	23	31	39	47	55	63	HH	H	
--	--	--	--	--	SF		--	HH	HH	

SF – When programmed, the array will verify as if it were blank.

FIGURE 1–1, PROGRAMMING WAVEFORMS

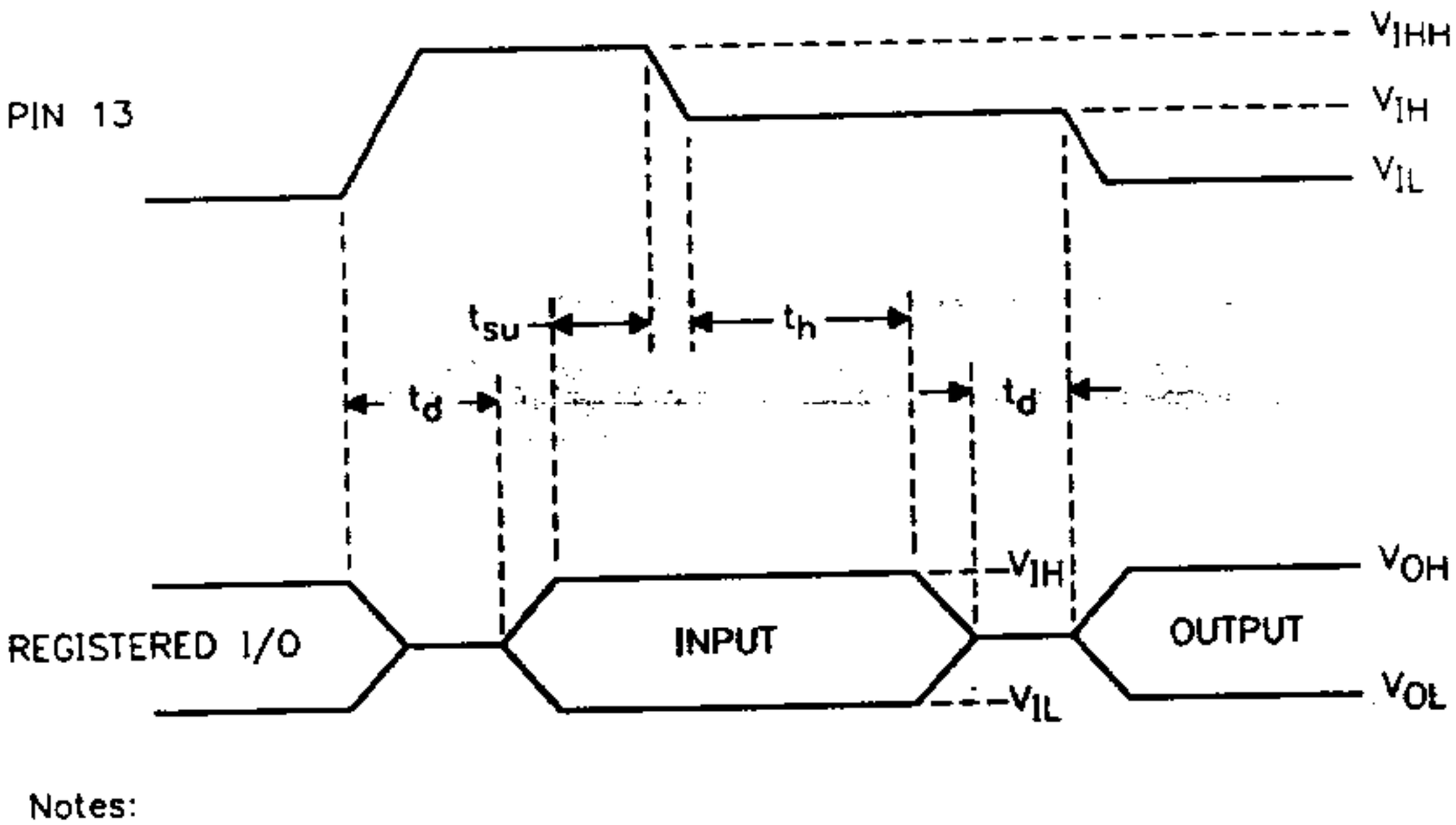


PRELOAD PROCEDURE FOR REGISTERED OUTPUTS (See Note 1)

The output registers of the TIBPAL20XX-5 can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1: With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2: Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3: Lower pin 13 to V_{IH}.
Step 4: Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin. Note that the output inverting buffer will have a low output state corresponding to a preloaded high (applied V_{IH}) register state.

ASYNCHRONOUS PRELOAD WAVEFORMS (See Notes 1 and 2)

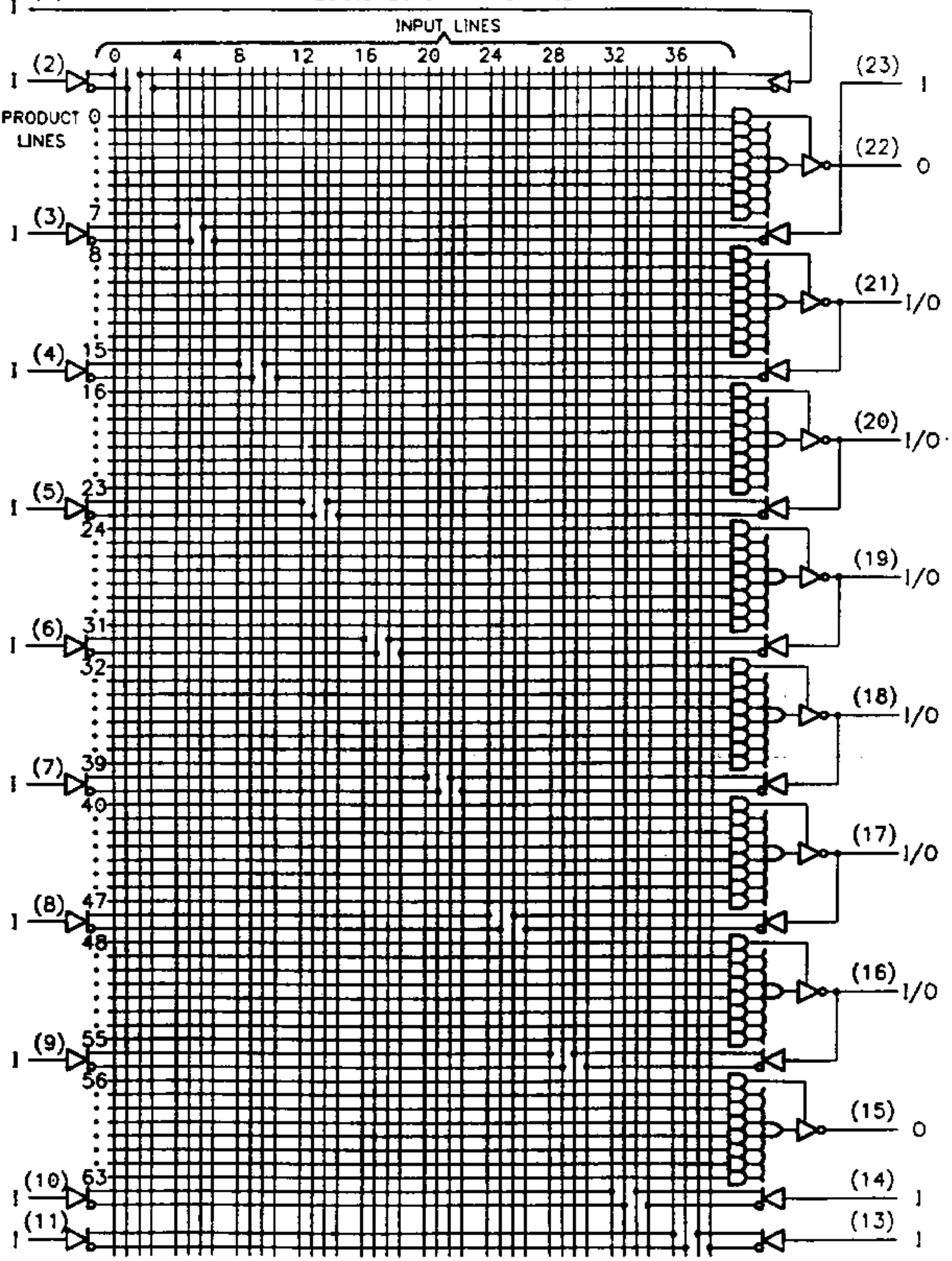


Notes:

1. Pin number shown is for J or N packages only. For FN or FK pacages, pin number must be changed accordingly. (See sheet 2)

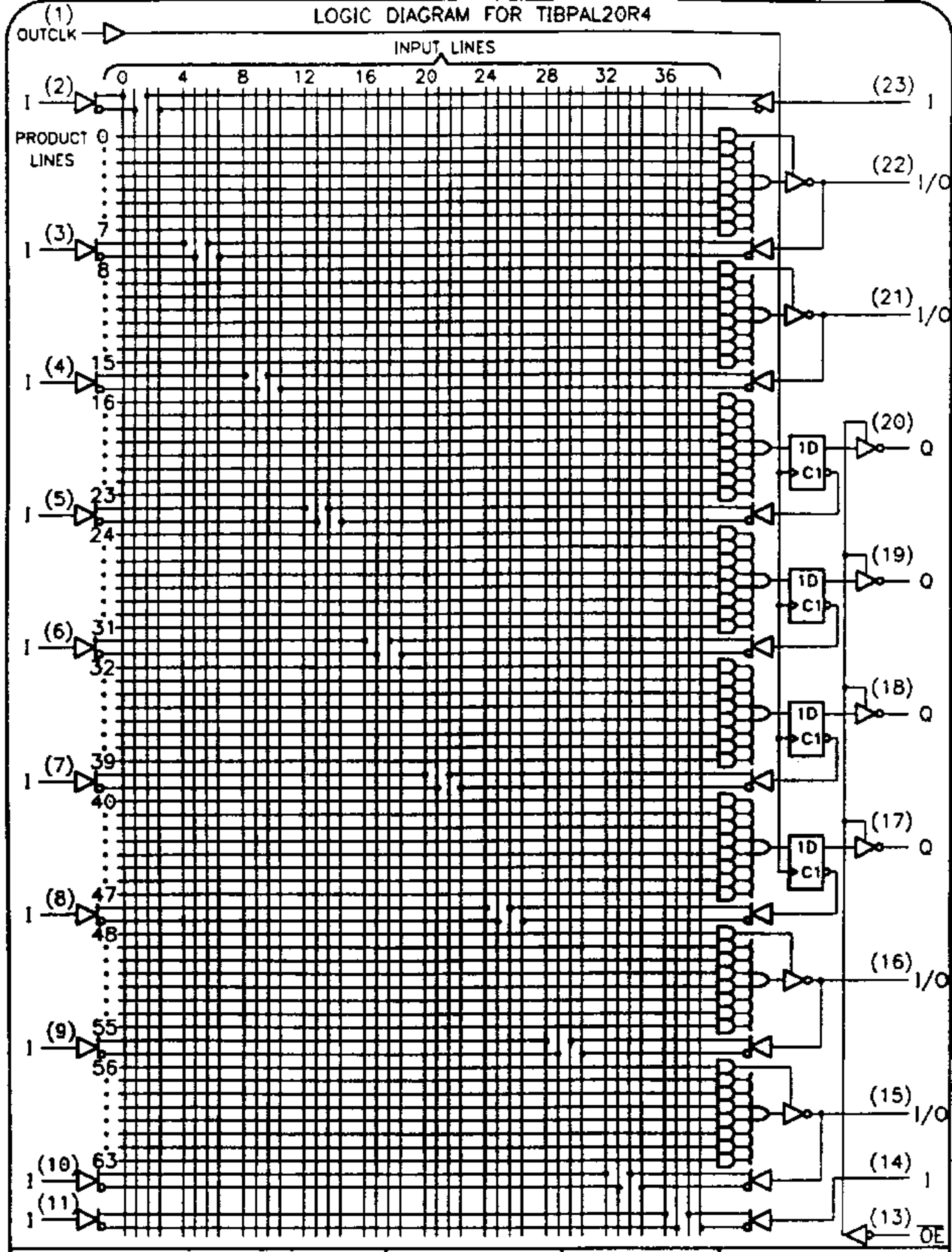
2. $t_d = t_{su} = t_h$ = 100ns to 1000ns.
   V_{IHH} = 10.25 V to 10.75 V.

LOGIC DIAGRAM FOR TIBPAL20L8



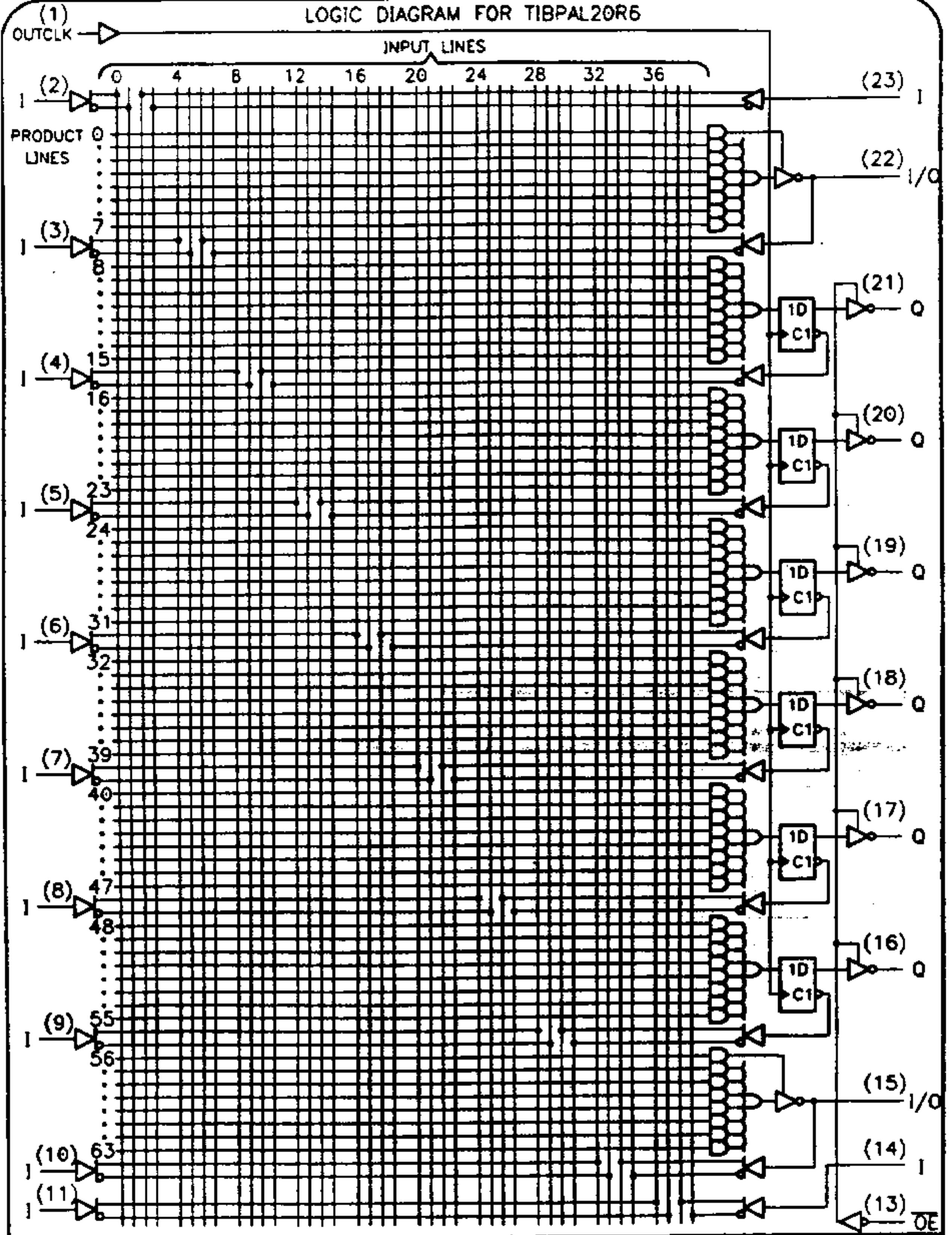
ALGORITHM SPECIFICATION TIBPAL20XX-5	PAL24D-6.DWG	SH 6 of 10	PAL24012

LOGIC DIAGRAM FOR TIBPAL20R4



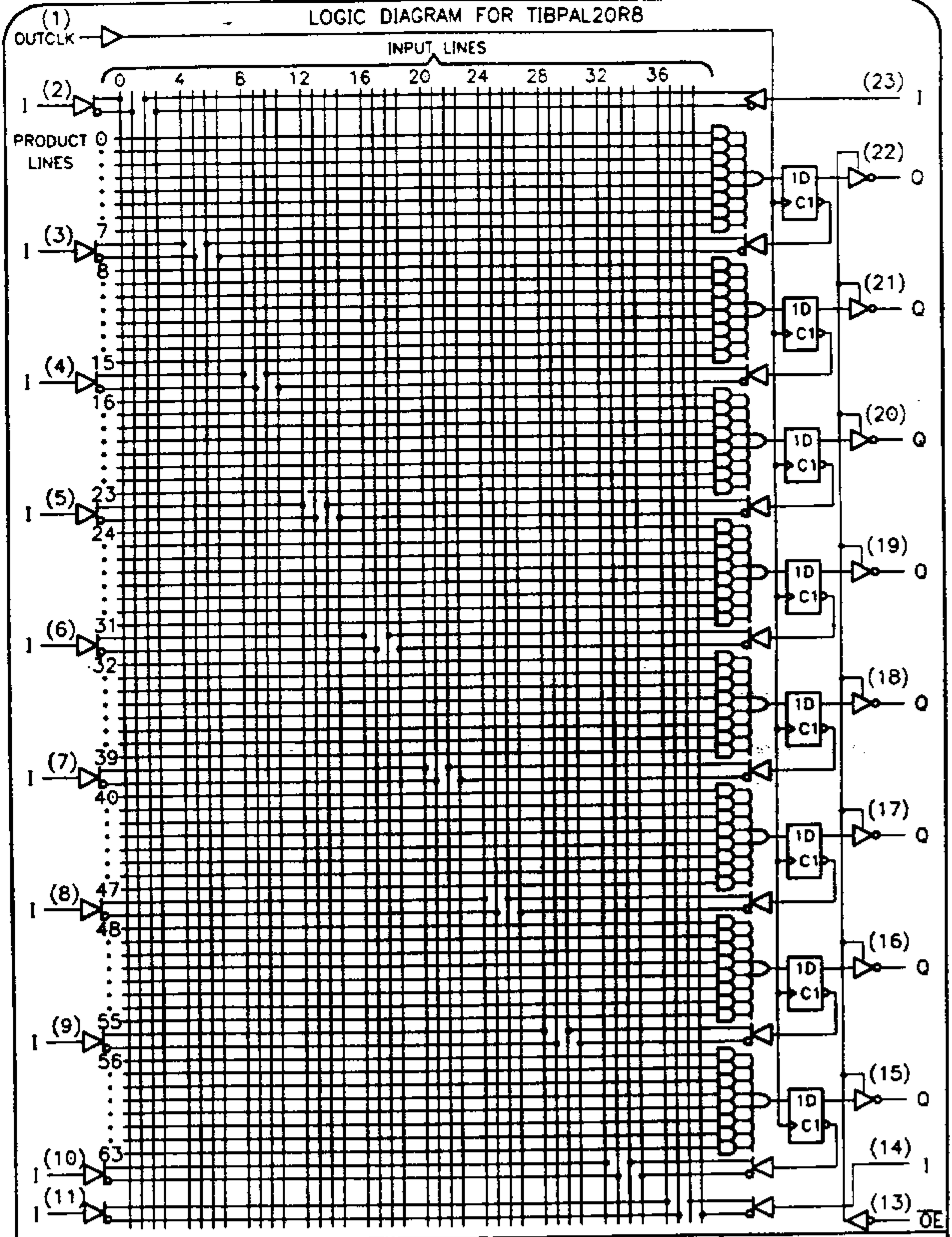
ALGORITHM SPECIFICATION TIBPAL20XX-5	PAL24D-7.DWG	SH 7 of 10	PAL24012

LOGIC DIAGRAM FOR TIBPAL20R6



ALGORITHM SPECIFICATION TIBPAL20XX-5	PAL24D-8.DWG	SH 8 of 10	PAL24012

LOGIC DIAGRAM FOR TIBPAL20R8



ALGORITHM SPECIFICATION TIBPAL20XX-5	PAL24D-9.DWG	SH 9 of 10	PAL24012

REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
A	06-90	Lippens	Sh 2. Removed MAX Spec. from t_{su}, t_h, and t_{d1}. Sh 3. Removed SF1 & changed SF2 to SF. Sh 4. Table 1-3. Removed SF1 and changed SF2 to SF.
B	06-90	Lippens	Sh 5. Changed from: Pin 11 to Pin 13. Sh 2. DIP - Changed pins 14 and 23 from: GND to: +. PLCC - Changed pins 17 and 27 from: GND to: +. Added note: + = Set to logical "1". Table 1-1: Changed units: t_{w1} from: ns to us t_{w2} from: us to ns t_{d2} from: us to ns Sh 5. Added Notes 1 and 2.