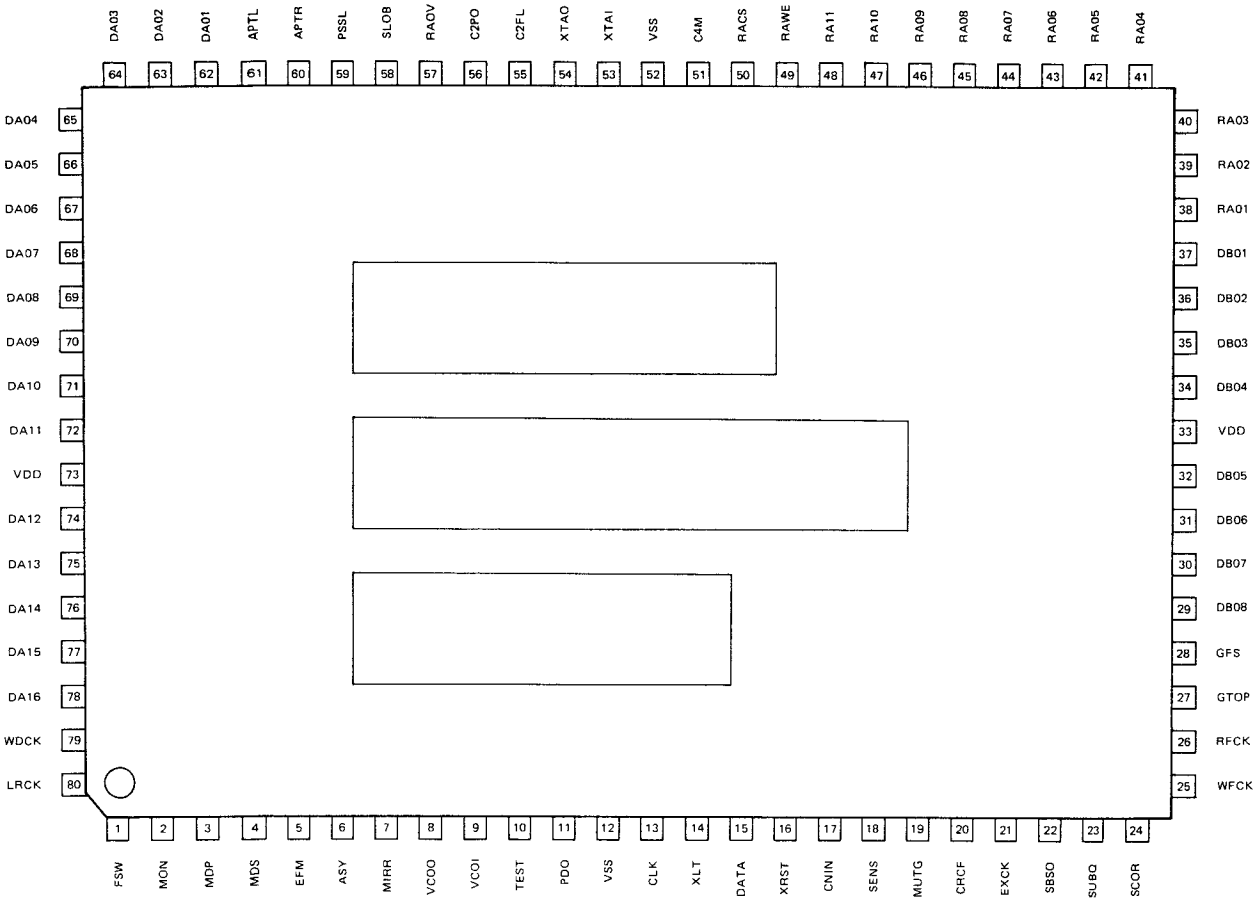
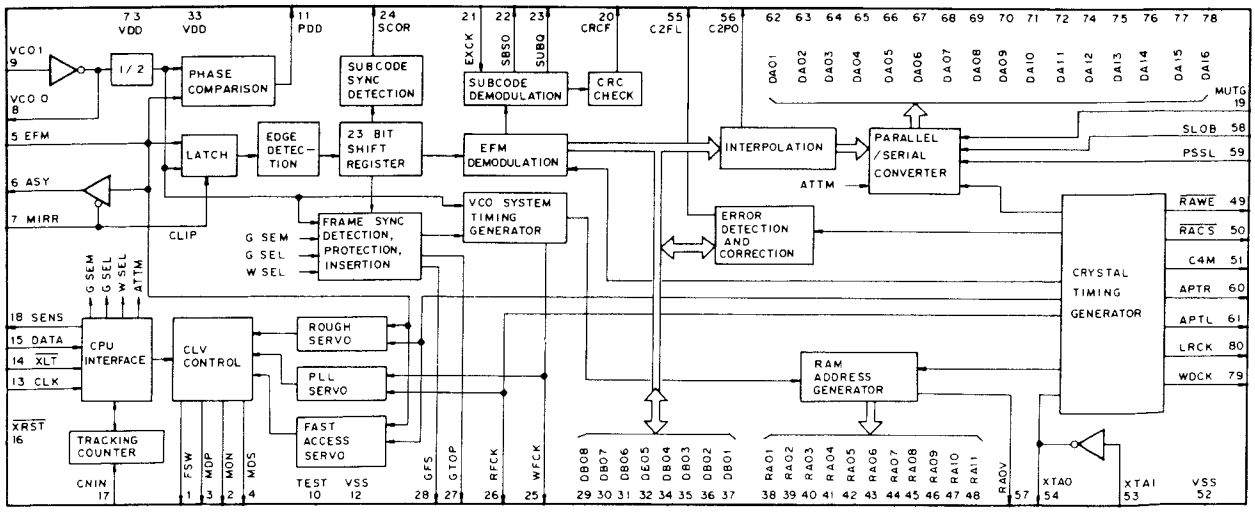
- **CX23035**

- **Pin Name**



- **Block Diagram**



• Pin Functions

Pin No.	Pin name	I/O	Function
1	FSW	O	Spindle motor output filter time constant select output.
2	MON	O	Spindle motor ON/OFF control output.
3	MDP	O	Spindle motor drive output. Rough control during CLV-S mode and phase control during CLV-P mode.
4	MDS	O	Spindle motor drive output. Speed control during CLV-P mode.
5	EFM	I	EFM signal input from RF amp.
6	ASY	O	EFM signal slice level control output.
7	MIRR	I	MIRROR input from RF amp.
8	VCOO	O	VCO output. When locked to EFM signal, f = 8.6432 MHz.
9	VCOI	I	VCO input.
10	TEST	I	(0 V)
11	PDO	O	EFM signal and VCO/2 phase comparison output.
12	VSS	—	GND (0 V)
13	CLK	I	Serial data transfer clock input from CPU. Data latching clock rise edge.
14	XLT	I	Latch input from CPU. Latching 8-bit shift register data (serial data from CPU) to respective registers.
15	DATA	I	Serial data input from CPU.
16	XP.ST	I	System reset input. Reset at L.
17	C_{NIN}	I	Tracking pulse input.
18	SENS	O	Outputting internal state according to address.
19	MUTG	I	Muting input with internal register A ATTM at L, normal state when MUTG is low and no sound when it is high.
20	CRCF	O	Output the CRC result of subcode Q
21	EXCK	I	Clock input for subcode serial output.
22	SBSO	O	Subcode serial output.
23	SUBQ	O	Subcode Q output.
24	SCOR	O	Subcode sync S0 + S1 output.
25	WFCX	O	Write frame clock output. When frame synch is locked, f = 7.35 KHz.
26	RFCX	O	Read frame clock output. Crystal system 7.35 KHz.
27	GTOP	O	Frame sync protection state display output.
28	GFS	O	Frame sync lock state display output.
29	DB08	I/O	External RAM data terminal. DATA8 (MSB)
30	DB07	I/O	External RAM data terminal. DATA7
31	DB06	I/O	External RAM data terminal. DATA6
32	DB05	I/O	External RAM data terminal. DATA5
33	VDD	—	Power supply (+5 V)
34	DB04	I/O	External RAM data terminal. DATA4
35	DB03	I/O	External RAM data terminal. DATA3
36	DB02	I/O	External RAM data terminal. DATA2
37	DB01	I/O	External RAM data terminal. DATA1 (LSB)
38	RA01	O	External RAM address output. ADDR01 (LSB)
39	RA02	O	External RAM address output. ADDR02
40	RA03	O	External RAM address output. ADDR03
41	RA04	O	External RAM address output. ADDR04

Pin No.	Pin name	I/O	Function
42	RA05	O	External RAM address output. ADDR05
43	RA06	O	External RAM address output. ADDR06
44	RA07	O	External RAM address output. ADDR07
45	RA08	O	External RAM address output. ADDR08
46	RA09	O	External RAM address output. ADDR09
47	RA10	O	External RAM address output. ADDR10
48	RA11	O	External RAM address output. ADDR11 (MSB)
49	RAME	O	Write enable signal output to external RAM (active when low).
50	RACS	O	Chip select signal output to external RAM (active when low).
51	C_{AM}	O	Crystal 1/2 frequency division output. f = 4.2336 MHz.
52	V_{SS}	—	GND (0 V)
53	XTAL	I	Crystal oscillation circuit input. f = 8.4672 MHz.
54	XTAO	O	Crystal oscillation circuit output. f = 8.4672 MHz.
55	C2FL	O	Corrects state output. When currently corrected C2 series is incorrectable, it becomes high.
56	C2PO	O	C2 pointer display output. Synchronized to audio data output.
57	RAOV	O	±4 frame jitter absorption RAM overflow and underflow display output.
58	SLOB	I	Audio data output code select input. Two's complement output when low, offset binary output when high.
59	PSSL	I	Audio data output mode select input. Serial output when low, parallel output when high.
60	APTR	O	Aperture compensation control output. High with R-ch.
61	APTL	O	Aperture compensation control output. High with L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL is H. C1F1 output when PSSL is L.
63	DA02	O	DA02 output when PSSL is high, C1F2 output when PSSL is low.
64	DA03	O	DA03 output when PSSL is high, C2F1 output when PSSL is low.
65	DA04	O	DA04 output when PSSL is high, C2F2 output when PSSL is low.
66	DA05	O	DA05 output when PSSL is high, UGFS output when PSSL is low.
67	DA06	O	DA06 output when PSSL is high, WFCK output when PSSL is low.
68	DA07	O	DA07 output when PSSL is high, FCKV output when PSSL is low.
69	DA08	O	DA08 output when PSSL is high, FCKX output when PSSL is low.
70	DA09	O	DA09 output when PSSL is high, PLCK output when PSSL is low.
71	DA10	O	DA10 output when PSSL is high, LRCK output when PSSL is low.
72	DA11	O	DA11 output when PSSL is high, C4LR output when PSSL is low.
73	V_{DD}	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL is high, DENL when PSSL is low.
75	DA13	O	DA13 output when PSSL is high, DENR when PSSL is low.
76	DA14	O	DA14 output when PSSL is high, C210 when PSSL is low.
77	DA15	O	DA15 output when PSSL is high, C210 when PSSL is low.
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL is high, DATA output when PSSL is low.
79	WDCX	O	88.2 KHz strobe signal output.
80	LRCX	O	44.1 KHz strobe signal output.