SIGNETICS
D-MOS
DATA
# SIGNETICS
## D-MOS DATA

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DESCRIPTION
The Signetics D-MOS SD200/201/202/203 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives superior high frequency performance up to 2GHz. A zener diode is connected between the gate and substrate of the SD201 and 203 that bypasses any voltage transient lying outside the range of $-0.3V$ to $+25.0V$. Thus the gates of the SD201 and 203 are protected against damage in all normal handling and operating situations.

All four devices are general purpose transistors especially suited for amplifier designs in the UHF range (500MHz to 2GHz). They have extremely high transconductance, very low input capacitance and extremely low feedback capacitance. The SD200, 201, 202 and 203 combine high gain with low levels of noise, intermodulation distortion and feedback capacitance. These parameters make them ideally suited for critical amplifier applications. These devices are hermetically sealed in modified 4-lead TO-72 packages.

GENERAL FEATURES
- ION-IMPLANTED FOR GREATER CONTROL AND RELIABILITY
- WIDE DYNAMIC RANGE
- POSITIVE BIAS ONLY

SD200/201 FEATURES
- HIGH GAIN THROUGH UHF RANGE – 10dB AT 1GHz
- LOW NOISE THROUGH UHF RANGE:
  SD200 – 4.5dB
  SD201 – 5.0dB
- LOW INPUT CAPACITANCE – 2.4pF
- LOW FEEDBACK CAPACITANCE – 0.20pF
- HIGH DRAIN-TO-SOURCE VOLTAGE – +30V
- HIGH FORWARD TRANSCONDUCTANCE – 15,000 $\mu$hmhos

SD202/203 FEATURES
- HIGH GAIN THROUGH UHF RANGE – 10dB AT 1.5GHz
- LOW NOISE THROUGH UHF RANGE – 3.2dB AT 1.0GHz
- LOW INPUT CAPACITANCE – 3.0pF
- LOW FEEDBACK CAPACITANCE – 0.20pF
- HIGH DRAIN-TO-SOURCE VOLTAGE – +25V
- HIGH FORWARD TRANSCONDUCTANCE – 20,000 $\mu$hmhos
ABSOLUTE MAXIMUM RATINGS

TA = 25°C (Unless Otherwise Noted)

Drain-To-Source Voltage (VDS)
SD200/SD201  +25V
SD202/SD203  +20V

Drain-To-Substrate Voltage (VDB)
SD200/SD201  +25V
SD202/SD203  +20V

DC Gate-To-Substrate Voltage (VGB)
SD200        ±40V
SD201        -0.3V, +10V
SD202        ±40V
SD203        -0.3V, +10V

Drain Current (ID)
50mA

Ambient Temperature Range
Storage       -65°C to +175°C
Operating     -65°C to +125°C

Transistor Dissipation (PT)
At +25°C Case Temperature  1.2W
(Derate linearly to +125°C case temperature at the rate
of 8.0mW/°C.)
At +25°C Free-Air Temperature  300mW
(Derate linearly to +125°C free-air temperature at the
rate of 2.0mW/°C.)

ELECTRICAL CHARACTERISTICS

TA = 25°C
(Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>Drain-To-Source Breakdown</td>
<td>BVDS</td>
<td>Voltage</td>
</tr>
<tr>
<td>Gate Leakage Current</td>
<td>IGSS</td>
<td></td>
</tr>
<tr>
<td>Drain-To-Source Current</td>
<td>ID (OFF)</td>
<td></td>
</tr>
<tr>
<td>Zero Bias Drain Current</td>
<td>IDSS</td>
<td></td>
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<tr>
<td>Threshold Voltage</td>
<td>VT</td>
<td></td>
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<tr>
<td>Forward Transconductance</td>
<td>gfs</td>
<td></td>
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<tr>
<td>Small Signal Short Circuit</td>
<td>Ciss</td>
<td>Input</td>
</tr>
<tr>
<td>Output</td>
<td>COSS</td>
<td></td>
</tr>
<tr>
<td>Reverse Transfer</td>
<td>CRSS</td>
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<tr>
<td>Power Gain*</td>
<td>Gps</td>
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<tr>
<td>Noise Figure*</td>
<td>NF</td>
<td></td>
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<tr>
<td>Drain-To-Source On Resistance</td>
<td>tDS (ON)</td>
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<tr>
<td>Intercept Point</td>
<td>P1</td>
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*Measured in Amplifier Test Fixture.

CHARACTERISTIC CURVES – SD200/201

1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT
<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>SD200</th>
<th>SD201</th>
<th>SD202</th>
<th>SD203</th>
<th>UNIT</th>
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<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
<td>TYP</td>
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<tr>
<td>$V_{GS} = 0V, I_D &lt; 1\mu A$</td>
<td>25</td>
<td>30</td>
<td></td>
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<td></td>
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<tr>
<td>$V_{GS} = \pm 10V, V_{DS} = 0V$</td>
<td></td>
<td></td>
<td>0.1</td>
<td>0.001</td>
<td>1.0</td>
</tr>
<tr>
<td>$V_{GS} = +10V, V_{DS} = 0V$</td>
<td></td>
<td></td>
<td>0.001</td>
<td>1.0</td>
<td>0.001</td>
</tr>
<tr>
<td>$V_{DS} = +15V, V_{GS} = 0V$</td>
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<td></td>
<td>0.001</td>
<td>1.0</td>
<td>0.001</td>
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<tr>
<td>$V_{DS} = V_{GS} = V_T, I_D = 1\mu A$</td>
<td>0.1</td>
<td>1.0</td>
<td>2.0</td>
<td>0.1</td>
<td>1.0</td>
</tr>
<tr>
<td>$V_{DS} = +15V, I_D = 20mA, f = 1kHz$</td>
<td>13.0</td>
<td>15.0</td>
<td>13.0</td>
<td>15.0</td>
<td></td>
</tr>
<tr>
<td>$V_{DS} = +15V, f = 1MHz$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_D = 20mA$</td>
<td>2.4</td>
<td>3.0</td>
<td>2.4</td>
<td>3.0</td>
<td>3.0</td>
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<td>$I_D = 0A$</td>
<td>1.0</td>
<td>1.2</td>
<td>1.0</td>
<td>1.2</td>
<td>1.0</td>
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<td>$V_{DS} = +15V, I_D = 20mA, f = 1GHz$</td>
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<td>$V_{GS} = +4V$</td>
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<td>$V_{GS} = +2.5V$</td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>$V_{DS} = +5V, I_D = 5mA$</td>
<td>50</td>
<td>70</td>
<td>50</td>
<td>70</td>
<td>35</td>
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<tr>
<td>$V_{DS} = +15V, I_D = 20mA, f = 1GHz, f = 2MHz$</td>
<td>29</td>
<td></td>
<td>29</td>
<td></td>
<td>29</td>
</tr>
</tbody>
</table>

**CHARACTERISTIC CURVES — SD200/201 (Continued)**
CHARACTERISTIC CURVES – SD200/201 (Continued)

NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT

OPTIMUM NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY

"S" PARAMETERS

COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE \( T_A \) = 25°C
DRAIN MILLIAMPERES \( I_D \) = 20
DRAIN-TO-SOURCE VOLTS \( V_{DS} \) = +15
COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE ($T_A$) = 25°C

"S" PARAMETERS

DRAIN MILLIAMPERES ($i_D$) = 20
DRAIN-TO-SOURCE VOLTS ($V_{DS}$) = +15

1GHz NOISE FIGURE AND POWER GAIN TEST FIXTURE

DIELECTRIC IS 3/16" TELFLEX FIBERGLASS (DK 8.98 @ 10GHz)
ALL MICROSTRIP WIDTH = 0.175"

NOTE: SHIELD AND 4 TUNABLE CAPACITORS ON GROUND PLANE SIDE OF AMPLIFIER.
DESCRIPTION
The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of -0.3V to +25V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for ±10V switch driver applications. Other characteristics allow them to be used as ±5V switches. The SD214 and 215 are designed to switch signals up to ±10V and the SD212 and 213 are designed to switch signals up to ±5V.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

FEATURES
• LOW FEEDBACK CAPACITANCE – 0.30pF
• LOW DRAIN NODE CAPACITANCE – 1.3pF
• LOW GATE NODE CAPACITANCE – 2.4pF
• LOW FEEDTHROUGH AND FEEDBACK TRANSIENTS
• ION-IMPLANTED FOR GREATER RELIABILITY
• EXCELLENT ISOLATION FROM INPUT TO OUTPUT – 120dB
• 35V DRAIN-TO-SOURCE VOLTAGE FOR SD210/211

APPLICATIONS
SWITCH DRIVER
ANALOG SWITCH
MULTIPLEXERS
DIGITAL SWITCH
SAMPLE AND HOLD
CHOPPERS
A-TO-D CONVERTERS
D-TO-A CONVERTERS

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ$C (Unless Otherwise Noted)

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<thead>
<tr>
<th>PARAMETER</th>
<th>SD210</th>
<th>SD211</th>
<th>SD212</th>
<th>SD213</th>
<th>SD214</th>
<th>SD215</th>
<th>UNITS</th>
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<tr>
<td>$V_{DS}$ Drain-to-Source</td>
<td>+30</td>
<td>+30</td>
<td>+10</td>
<td>+10</td>
<td>+20</td>
<td>+20</td>
<td>Vdc</td>
</tr>
<tr>
<td>$V_{SD}$ Source-to-Drain</td>
<td>+10</td>
<td>+10</td>
<td>+10</td>
<td>+10</td>
<td>+20</td>
<td>+20</td>
<td>Vdc</td>
</tr>
<tr>
<td>$V_{DB}$ Drain-to-Substrate</td>
<td>+15</td>
<td>+15</td>
<td>+15</td>
<td>+15</td>
<td>+25</td>
<td>+25</td>
<td>Vdc</td>
</tr>
<tr>
<td>$V_{SB}$ Source-to-Substrate</td>
<td>+15</td>
<td>+15</td>
<td>+15</td>
<td>+15</td>
<td>+25</td>
<td>+25</td>
<td>Vdc</td>
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<tr>
<td>$V_{GS}$ Gate-to-Source</td>
<td>±40</td>
<td>-15</td>
<td>±40</td>
<td>-15</td>
<td>±40</td>
<td>-25</td>
<td>Vdc</td>
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<tr>
<td>$V_{GB}$ Gate-to-Substrate</td>
<td>±40</td>
<td>-0.3</td>
<td>±40</td>
<td>-0.3</td>
<td>±40</td>
<td>-0.3</td>
<td>Vdc</td>
</tr>
<tr>
<td>$V_{GD}$ Gate-to-Drain</td>
<td>±40</td>
<td>-15</td>
<td>±40</td>
<td>-15</td>
<td>±40</td>
<td>-25</td>
<td>Vdc</td>
</tr>
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</table>
**SIGNETICS D-MOS FET SWITCH – N-CHANNEL ENHANCEMENT • SD210–215**

**ABSOLUTE MAXIMUM RATINGS** (All devices)

- Drain Current ($I_D$) 50mA

**Ambient Temperature Range**
- Storage: -65°C to +175°C
- Operating: -65°C to +125°C

**Transistor Dissipation ($P_T$)**
- At 25°C Case Temperature 1.2W (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)
- At 25°C Free-Air Temperature 300mW (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)

**DISTORTION TEST CIRCUIT**

**NOTE:** All Resistors StandarD and are measured in Ohms.

**CAPACITANCE MODEL**

**ELECTRICAL CHARACTERISTICS**

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<td>Breakdown Voltage</td>
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<td>Drain-To-Source</td>
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<td>$BV_{SD}$</td>
<td>Source-To-Drain</td>
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<tr>
<td>$BV_{DB}$</td>
<td>Drain-To-Substrate</td>
</tr>
<tr>
<td>$BV_{SB}$</td>
<td>Source-To-Substrate</td>
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<tr>
<td>Leakage Current</td>
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<tr>
<td>$I_{DS} , (OFF)$</td>
<td>Drain-To-Source</td>
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<tr>
<td>$I_{SD} , (OFF)$</td>
<td>Source-To-Drain</td>
</tr>
<tr>
<td>$I_{GB}$</td>
<td>Gate</td>
</tr>
<tr>
<td>$V_T$</td>
<td>Threshold Voltage</td>
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<tr>
<td>$gfs$</td>
<td>Forward Transconductance</td>
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<tr>
<td>Small Signal Capacitances</td>
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<td>(See Capacitance Model)</td>
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<tr>
<td>$C_{GD}$</td>
<td>Gate Node</td>
</tr>
<tr>
<td>$C_{GD} + C_{GS}$</td>
<td>Source Node</td>
</tr>
<tr>
<td>$C_{GD} + C_{DB}$</td>
<td>Drain Node</td>
</tr>
<tr>
<td>$r_{DS} , (ON)$</td>
<td>Drain-To-Source Resistance</td>
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**NOTE:** All Resistors Standard and are measured in Ohms.
<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>SD210</th>
<th>SD211</th>
<th>SD212</th>
<th>SD213</th>
<th>SD214</th>
<th>SD215</th>
<th>UNITS</th>
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<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
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<td>VGS = VBS = 0V, IS = 10μA</td>
<td>30</td>
<td>35</td>
<td></td>
<td>30</td>
<td>35</td>
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<td>10</td>
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<tr>
<td>VGS = VBS = -5V, IS = 10nA</td>
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<td>10</td>
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<tr>
<td>VGD = VBD = -5V, ID = 10nA</td>
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<tr>
<td>VGB = 0V, Source OPEN, ID = 10nA</td>
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<td>15</td>
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<tr>
<td>VGB = 0V, Drain OPEN, IS = 10μA</td>
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<tr>
<td>VGS = VBS = -5V</td>
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<td>1</td>
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<td>1</td>
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<td>VDS = +10V</td>
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<tr>
<td>VGD = VBD = -5V</td>
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<td>10</td>
<td></td>
<td>1</td>
<td>10</td>
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<td>1</td>
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<tr>
<td>VSD = +20V</td>
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<td>VDS = VSB = 0V</td>
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<td>VGB = +40V</td>
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<tr>
<td>VGB = +25V</td>
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<tr>
<td>VGB = +30V</td>
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<td></td>
</tr>
<tr>
<td>VDS = VGS = VT, IS = 1μA, VSB = 0V</td>
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<td>0.5</td>
<td>1.0</td>
<td>2.0</td>
<td>0.5</td>
</tr>
<tr>
<td>VDS = 10V, VSB = 0V, ID = 20mA, f = 1kHz</td>
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<tr>
<td>VDS = 10V, f = 1kHz, VGS = VBS = -15V</td>
<td>2.4</td>
<td>3.5</td>
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<td>3.5</td>
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<td>1.3</td>
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<td></td>
<td>3.5</td>
</tr>
<tr>
<td></td>
<td>0.3</td>
<td>0.5</td>
<td>0.3</td>
<td>0.5</td>
<td>0.3</td>
<td>0.5</td>
<td>0.3</td>
</tr>
<tr>
<td>ID = 0.1mA, VSB = 0</td>
<td>50</td>
<td>70</td>
<td></td>
<td>50</td>
<td>70</td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>VGS = +5V</td>
<td>30</td>
<td>45</td>
<td></td>
<td>30</td>
<td>45</td>
<td></td>
<td>30</td>
</tr>
<tr>
<td>VGS = +10V</td>
<td>23</td>
<td></td>
<td></td>
<td>23</td>
<td></td>
<td></td>
<td>23</td>
</tr>
<tr>
<td>VGS = +15V</td>
<td>19</td>
<td></td>
<td></td>
<td>19</td>
<td></td>
<td></td>
<td>19</td>
</tr>
<tr>
<td>VGS = +20V</td>
<td>17</td>
<td></td>
<td></td>
<td>17</td>
<td></td>
<td></td>
<td>17</td>
</tr>
<tr>
<td>VGS = +25V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CHARACTERISTIC CURVES

- **DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE**
- **THRESHOLD VOLTAGE VS SOURCE-TO-SUBSTRATE VOLTAGE**
- **DRAIN TO-SOURCE RESISTANCE VS TEMPERATURE**
- **THRESHOLD VOLTAGE VS TEMPERATURE**

These graphs illustrate various characteristics of a Signetics D-MOS FET switch, focusing on N-Channel Enhancement and specifying parameters such as Drain current, Gate-to-source voltage, Drain-to-source resistance, and Threshold voltage under different conditions.
CHARACTERISTIC CURVES (Continued)

DRAIN-TO-SOURCE RESISTANCE VS GATE-TO-SOURCE VOLTAGE

DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE

DISTORTION VS GATE-TO-SOURCE VOLTAGE

D-MOS DRIVER/SWITCH APPLICATION

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.
TYPICAL WAVEFORMS

SWITCHING CHARACTERISTICS

<table>
<thead>
<tr>
<th>V_{DD}</th>
<th>R_L</th>
<th>t_d (ON) (ns)</th>
<th>t_f (ns)</th>
<th>t_{OFF} (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>680</td>
<td>0.6</td>
<td>1.0</td>
<td>0.7</td>
</tr>
<tr>
<td>10</td>
<td>680</td>
<td>0.7</td>
<td>1.0</td>
<td>0.8</td>
</tr>
<tr>
<td>15</td>
<td>1k</td>
<td>0.9</td>
<td>1.0</td>
<td>1.0</td>
</tr>
</tbody>
</table>

*{t_{OFF}} is dependent on {R_L} and {C_L} and does not depend on the device characteristics.

SWITCHING WAVEFORMS

TEST CIRCUIT

INPUT PULSE

- \( t_d, t_f < 1\,\text{ns} \)
- \( \text{PULSE WIDTH} = 100\,\text{ns} \)
- \( \text{REP RATE} = 1\,\text{MHz} \)

SAMPLING SCOPE

- \( t_f < 360\,\text{ps} \)
- \( R_{IN} = 1\,\text{M}\Omega \)
- \( C_{IN} = 2.0\,\text{pF} \)

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.
DESCRIPTION
The Signetics D-MOS SD300/301/303/304 are silicon, dual-insulated-gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives superior high frequency performance. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +25.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The devices' attributes make them ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure, has made the feedback capacity (Crss) less than 0.02pF. A wide AGC capability plus a significant reduction in cross-modulation distortion is now available because of the inherent linearity of these devices. The SD300, 301, 303 and 304 are hermetically sealed in modified 4-lead TO-72 packages.

GENERAL FEATURES
• LOWER CROSS-MODULATION AND WIDER DYNAMIC RANGE THAN BIPOLAR OR SINGLE GATE FETS
• REVERSE AGC CAPABILITY
• LINEAR MIXING CAPABILITY
• DIODE PROTECTED GATES
• HIGH FORWARD TRANSCONDUCTANCE – gfs = 10,000μmhos
• ION-IMPLANTED
• POSITIVE BIAS ONLY

FEATURES

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SD300</th>
<th>SD301</th>
<th>SD303</th>
<th>SD304</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Gain Through UHF Range</td>
<td>13</td>
<td>14</td>
<td>14</td>
<td>16</td>
<td>dB at 1GHz</td>
</tr>
<tr>
<td>High Gain Through VHF Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB at 500MHz</td>
</tr>
<tr>
<td>Low Noise Through UHF Range</td>
<td>8</td>
<td>6</td>
<td>5.5</td>
<td>5</td>
<td>dB at 1GHz</td>
</tr>
<tr>
<td>Low Noise Through VHF Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB at 500MHz</td>
</tr>
<tr>
<td>Low Input Capacitance</td>
<td>2.0</td>
<td>2.0</td>
<td>3.0</td>
<td>2.5</td>
<td>pF</td>
</tr>
<tr>
<td>Low Feedback Capacitance</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td>0.03</td>
<td>pF</td>
</tr>
<tr>
<td>Low Output Capacitance</td>
<td>1.0</td>
<td>0.6</td>
<td>0.6</td>
<td>1.0</td>
<td>pF</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>SD300</th>
<th>SD301</th>
<th>SD303</th>
<th>SD304</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-To-Source (V_DS)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD300/304</td>
<td>+25V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD301</td>
<td>+20V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Gate No. 1-To-Substrate Voltage (V_G1B)</td>
<td>-0.3V, +10V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Gate No. 2-To-Substrate Voltage (V_G2B)</td>
<td>-0.3V, +15V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain Current (I_D)</td>
<td>50mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Ambient Temperature Range (T_A)

Storage: 65°C to +175°C
Operating: -65°C to +125°C

Transistor Dissipation (P_T)

At +25°C Case Temperature: 1.2W
(Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)

At +25°C Free-Air Temperature: 300mW
(Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)

TEST FIXTURE (1GHz) (Used With SD300, 301, 303)

Electrical Characteristics T_A = +25°C (Unless Otherwise Noted).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>SD300</th>
<th>SD301</th>
<th>SD303</th>
<th>SD304</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_G1S = V_G2S = 0V, I_D = 5μA</td>
<td>25 30</td>
<td>20 25</td>
<td>20 25</td>
<td>25 30</td>
<td>30 30</td>
<td>V</td>
</tr>
<tr>
<td>Gate 1 Leakage Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_G1S = +5V, V_G2S = V_DS = 0V</td>
<td>0.001 0.1</td>
<td>0.001 0.1</td>
<td>0.001 0.1</td>
<td>0.001 0.1</td>
<td>0.001 0.1</td>
<td>μA</td>
</tr>
</tbody>
</table>

Note: Shield and all passive components on ground plane side of amplifier. 1000pF bypasses are: Drain: Cory FT4-01-2 Gate 2: American Technical Ceramics ATC1300B (chip capacitor) Launchers are OSM248-2
<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SD300 MIN</th>
<th>SD300 TYP</th>
<th>SD300 MAX</th>
<th>SD301 MIN</th>
<th>SD301 TYP</th>
<th>SD301 MAX</th>
<th>SD303 MIN</th>
<th>SD303 TYP</th>
<th>SD303 MAX</th>
<th>SD304 MIN</th>
<th>SD304 TYP</th>
<th>SD304 MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_GSS</td>
<td>Gate 2 Leakage Current</td>
<td>V_G2S = +10V, V_G1S = V_D = 0V</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_D (OFF)</td>
<td>Drain-To-Source Leakage Current</td>
<td>V_D = +15V, V_G1S = V_G2S = 0V</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_GSSS</td>
<td>Zero Bias Drain Current</td>
<td>V_G2S = +15V, V_G1S = V_G2S = 0V</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>0.001</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_T1</td>
<td>Gate 1 Threshold Voltage</td>
<td>V_D = +15V, V_G1S = V_T1, V_G2S = +10V, I_D = 1μA 0.10</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_T2</td>
<td>Gate 2 Threshold Voltage</td>
<td>V_D = +15V, V_G2S = V_T2, V_G1S = +4V, I_D = 1μA 0.10</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Small Signal Short Circuit Capacitances</td>
<td>f = 1MHz, Gate 2 AC Grounded</td>
<td>C_iss</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>3.0</td>
<td>3.0</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>gfs</td>
<td>Forward Transconductance</td>
<td>V_D = +15V, V_G1S = 0V, V_G2S = 0V, f = 1kHz 8.0</td>
<td>8.0</td>
<td>8.0</td>
<td>8.0</td>
<td>10.0</td>
<td>10.0</td>
<td>10.0</td>
<td>13.0</td>
<td>15.0</td>
<td>mmhos</td>
<td></td>
<td></td>
<td>mmhos</td>
</tr>
<tr>
<td>NPS</td>
<td>Power Gain</td>
<td>V_D = +15V, V_G1S = +3.5V, V_G2S = +10V, I_D = 18mA, f = 1kHz 9.0</td>
<td>9.0</td>
<td>10.0</td>
<td>10.0</td>
<td>13.0</td>
<td>13.0</td>
<td>16.0</td>
<td>13.0</td>
<td>13.0</td>
<td>dB</td>
<td></td>
<td>dB</td>
<td>dB</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
<td>V_D = +15V, V_G1S = +3.5V, V_G2S = +10V, I_D = 18mA, f = 1kHz 8.0*9.0</td>
<td>8.0*9.0</td>
<td>6.0*7.0</td>
<td>6.0*7.0</td>
<td>8.0</td>
<td>8.0</td>
<td>8.0</td>
<td>5.0</td>
<td>5.0</td>
<td>dB</td>
<td></td>
<td>dB</td>
<td>dB</td>
</tr>
<tr>
<td>E_int</td>
<td>Interfering Signal Level At Gate For 1% Cross-Modulation Distortion, Peak Voltage REFERENCED TO 300Ω System.</td>
<td>V_D = +15V, V_G2S = +10V, I_D = 18mA, Desired Signal f = 1kHz, Undesired Signal f = 500MHz, V_D = +15V, V_G2S = +10V, I_D = 18mA, Desired Signal f = 1kHz, Undesired Signal f = 500MHz, 150</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>150</td>
<td>150</td>
<td>mV</td>
<td></td>
<td>mV</td>
<td>mV</td>
</tr>
<tr>
<td>AGC</td>
<td>Range Of Automatic Gain Control</td>
<td>V_D = +15V, V_G1S = +3.5V, f = 1kHz, V_D = +15V, V_G1S = +3.5V, f = 500MHz</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>dB</td>
<td></td>
<td>dB</td>
<td>dB</td>
</tr>
<tr>
<td>f_Ds (ON)</td>
<td>Drain-To-Source On Resistance</td>
<td>V_G1S = +5V, V_G2S = +10V, I_D = 0.1mA 90</td>
<td>90</td>
<td>130</td>
<td>90</td>
<td>130</td>
<td>65</td>
<td>80</td>
<td>90</td>
<td>130</td>
<td>Ω</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

*Measured in amplifier test fixture.
CHARACTERISTIC CURVES

SD300, 301

S PARAMETERS
AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_DS) = +15

S_11

S_12

S_21

S_22

FREQUENCY (GHz)

FREQUENCY (GHz)
CHARACTERISTIC CURVES (Continued)

**SD300, 301**

**POWER GAIN VS FREQUENCY**

- **Frequency (GHz)**
  - X-axis: 0.1 to 1.0
  - Y-axis: 0.1 to 25

**NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY**

- **Frequency (GHz)**
  - X-axis: 0.1 to 1.0
  - Y-axis: 0.1 to 25

**SD304**

**POWER GAIN VS DRAIN CURRENT**

- **Drain Milliamperes (I_D)**
  - X-axis: 0 to 20
  - Y-axis: 0 to 16

**POWER GAIN VS FREQUENCY**

- **Frequency (GHz)**
  - X-axis: 0.1 to 1.0
  - Y-axis: 0 to 16

CHARACTERISTIC CURVES (Continued)

SD300, 301, 304

DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE

1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE

DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE

AUTOMATIC GAIN CONTROL RANGE AT 500MHz
SIGNETICS D-MOS FET – DUAL GATE ■ SD300, SD301, SD303, SD304

CHARACTERISTIC CURVES (Continued)

SD303

**DRAIN CURRENT VERSUS DRAIN-TO-SOURCE VOLTAGE**

![Graph showing drain current versus drain-to-source voltage for SD303.](image)

**DRAIN CURRENT VERSUS GATE NO. 1-TO-SOURCE VOLTAGE**

![Graph showing drain current versus gate no. 1-to-source voltage for SD303.](image)

**DRAIN CURRENT VERSUS GATE NO. 2-TO-SOURCE VOLTAGE**

![Graph showing drain current versus gate no. 2-to-source voltage for SD303.](image)

**1kHz FORWARD TRANSCONDUCTANCE VERSUS DRAIN CURRENT**

![Graph showing 1kHz forward transconductance versus drain current for SD303.](image)

**POWER GAIN VERSUS FREQUENCY**

![Graph showing power gain versus frequency for SD303.](image)

**POWER GAIN VERSUS DRAIN CURRENT**

![Graph showing power gain versus drain current for SD303.](image)
CHARACTERISTIC CURVES (Continued)

SD303

S PARAMETERS
AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_D) = +15

[Graphs showing S parameters for SD303]
CHARACTERISTIC CURVES (Continued)

SD304

S PARAMETERS
AMBIENT TEMP. (T_A) = 25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_DS) = +15

S11

S12

S21

S22

FREQUENCY (GHz)

FREQUENCY (GHz)
DESCRIPTION
The Signetics D-MOS SD305 and SD306 are silicon, dual-insulated gate, field-effect transistors of the N-channel enhancement mode type. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of \(-0.3\) V to \(+20.0\) V. Thus, the gates are protected against damage in all normal handling and operating situations.

The devices' attributes make them ideally suited for a variety of VHF amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity \((C_{G1D})\) typically less than \(0.03\) pF. A wide AGC capability plus significant reduction in cross modulation distortion is now available because of the inherent linearity of the devices. The SD305 and SD306 are hermetically sealed in a 4-lead TO-72 package.

GENERAL FEATURES
- POSITIVE BIAS ONLY
- LOW GATE VOLTAGES
- ENHANCEMENT MODE OPERATION
- WIDE AGC RANGE - 50dB AT 200MHz
- ZENER DIODE GATE PROTECTION
- ION IMPLANTED FOR GREATER RELIABILITY

FEATURES - SD305 (VHF TV and FM Mixer)
- HIGH CONVERSION GAIN - 17dB AT 200MHz WITH \(V_{G1S} = V_{G2S}\) FOR BIASING SIMPLICITY

FEATURES - SD306 (VHF TV and FM RF Amplifier)
- HIGH POWER GAIN WITHOUT NEUTRALIZATION - 20dB AT 200MHz
- LOW NOISE FIGURE - 1.5dB AT 200MHz
- LOW INPUT AND OUTPUT CAPACITANCE - 3.3pF AND 1.0pF CONSTANT WITH AGC
- LOW FEEDBACK CAPACITANCE - 0.03pF
- SUPERIOR CROSS MODULATION PERFORMANCE
- HIGH TRANSCONDUCTANCE - 15mmhos

ABSOLUTE MAXIMUM RATINGS \(T_A = 25^\circ C\) (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SD305</th>
<th>SD306</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DS}) Drain-To-Source Voltage</td>
<td>+20</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{G1B}) Gate No. 1-To-Substrate Voltage</td>
<td>-0.3 to +20</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>(V_{G2B}) Gate No. 2-To-Substrate Voltage</td>
<td>-0.3 to +20</td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>(I_D) Drain Current</td>
<td>150</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>(T_A) Ambient Temperature Range</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td>-65 to +175</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>(P_T) Transistor Dissipation</td>
<td>1.2</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>At 25(^\circ)C Case Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Derate linearly to 125(^\circ)C case temperature at the rate of 8.0mW/°C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>At 25(^\circ)C Free-Air Temperature</td>
<td>300</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>(Derate linearly to 125(^\circ)C free-air temperature at the rate of 2.0mW/°C)</td>
<td></td>
<td></td>
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### ELECTRICAL CHARACTERISTICS  \( T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SD305</th>
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<td></td>
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<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
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<tr>
<td>OFF Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>( B_{DS} ) Drain-To-Source Breakdown Voltage</td>
<td>( V_{G1S} = V_{G2S} = 0V, I_D = 5\mu A )</td>
<td>20</td>
<td>30</td>
<td></td>
<td>20</td>
<td>25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_D ) (OFF) Drain-To-Source Leakage Current</td>
<td>( V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V )</td>
<td>0.001</td>
<td>1.0</td>
<td></td>
<td>0.001</td>
<td>1.0</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{DSS} ) Zero Bias Drain Current</td>
<td>( V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V )</td>
<td>0.001</td>
<td>1.0</td>
<td></td>
<td>0.001</td>
<td>1.0</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{G1SS} ) Gate No. 1 Leakage Current</td>
<td>( V_{G1S} = +5V, V_{G2S} = V_{DS} = 0V )</td>
<td>0.001</td>
<td>0.1</td>
<td></td>
<td>0.001</td>
<td>0.1</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{G2SS} ) Gate No. 2 Leakage Current</td>
<td>( V_{G2S} = +10V, V_{G1S} = V_{DS} = 0V )</td>
<td>0.001</td>
<td>0.1</td>
<td></td>
<td>0.001</td>
<td>0.1</td>
<td></td>
<td>( \mu A )</td>
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<tr>
<td>ON Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>( V_{T1} ) Gate 1 Threshold Voltage</td>
<td>( V_{DS} = V_{G1S} = V_{T1}, V_{G2S} = +10V, I_D = 1\mu A )</td>
<td>0.1</td>
<td>1.0</td>
<td>2.0</td>
<td>0.1</td>
<td>0.5</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{T2} ) Gate 2 Threshold Voltage</td>
<td>( V_{DS} = V_{G2S} = V_{T2}, V_{G1S} = +5V, I_D = 1\mu A )</td>
<td>0.1</td>
<td>1.0</td>
<td>2.0</td>
<td>0.1</td>
<td>0.5</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>( I_{DS (ON)} ) Drain-To-Source On Resistance</td>
<td>( V_{G1S} = +5V, V_{G2S} = +10V, I_D = 0.1mA )</td>
<td>30</td>
<td>60</td>
<td>65</td>
<td>100</td>
<td></td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Small Signal Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( g_{fs} ) Forward Transconductance</td>
<td>( V_{DS} = +15V, V_{G2S} = +10V, f = 1kHz, I_D = 50mA, I_D = 18mA )</td>
<td>24</td>
<td>27</td>
<td>13</td>
<td>15</td>
<td></td>
<td></td>
<td>mmhos</td>
</tr>
<tr>
<td>( g_{fs (CONV)} ) Conversion Transconductance</td>
<td>( V_{DS} = +15V, V_{G1S} = V_{G2S}, I_D = 8mA, f = 1kHz, E_{LO} (RMS) = 750mV )</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>mmhos</td>
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<tr>
<td>Capacitances</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{G1S} ) Input AC Grounded</td>
<td>( V_{DS} = +15V, V_{G2S} = +10V )</td>
<td>4.0</td>
<td>5.0</td>
<td>3.3</td>
<td>3.6</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>( I_D = 50mA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_D = 18mA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{DS} ) Output</td>
<td>( V_{DS} = +15V, V_{G1S} = V_{G2S}, I_D = 8mA )</td>
<td>4.0</td>
<td>5.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>( V_{DS} = +15V, V_{G1S} = +10V )</td>
<td>1.3</td>
<td>1.7</td>
<td>1.0</td>
<td>1.3</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{G1D} ) Reverse Transfer</td>
<td>( V_{DS} = +15V, V_{G1S} = 0V, V_{G2S} = +10V )</td>
<td>0.03</td>
<td></td>
<td>0.03</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Input Admittance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{Re} \left ( y_{11} \right ) )</td>
<td>( V_{G1S} = V_{G2S}, I_D = 8mA )</td>
<td>1.05</td>
<td></td>
<td></td>
<td></td>
<td>1.11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{Im} \left ( y_{11} \right ) )</td>
<td>( I_D = 18mA )</td>
<td>6.66</td>
<td></td>
<td></td>
<td></td>
<td>4.76</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Admittance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{Re} \left ( y_{22} \right ) )</td>
<td>( f = 200MHz, V_{DS} = +15V )</td>
<td>0.73</td>
<td></td>
<td></td>
<td></td>
<td>1.05</td>
<td></td>
<td>mmhos</td>
</tr>
<tr>
<td>( \text{Im} \left ( y_{22} \right ) )</td>
<td></td>
<td>2.09</td>
<td></td>
<td></td>
<td></td>
<td>1.54</td>
<td></td>
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</table>
### ELECTRICAL CHARACTERISTICS (Continued) \( T_A = 25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SD305</th>
<th>SD306</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Transmittance ( Re (y_{21}) )</td>
<td></td>
<td>4.69</td>
<td>13.23</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( Im (y_{21}) )</td>
<td>-3.01</td>
<td>-5.62</td>
<td>mmhos</td>
</tr>
<tr>
<td>Reverse Transmittance ( Re (y_{12}) )</td>
<td></td>
<td>0.04</td>
<td>0.01</td>
<td>mmhos</td>
</tr>
<tr>
<td></td>
<td>( Im (y_{12}) )</td>
<td>-0.03</td>
<td>-0.04</td>
<td></td>
</tr>
<tr>
<td>( G_{PS} ) Power Gain(^2)</td>
<td>( V_{DS} = +15V, V_{G2S} = +10V, I_D = 18mA, f = 200MHz )</td>
<td></td>
<td>17 20</td>
<td>dB</td>
</tr>
<tr>
<td>( G_{PS (CONV)} ) Conversion Power Gain(^1)</td>
<td>( V_{DS} = +15V, V_{G1S} = V_{G2S}, I_D = 8mA, f = 200MHz, f_{LO} = 245MHz )</td>
<td>14 17</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( NF ) Noise Figure</td>
<td>( V_{DS} = +15V, V_{G2S} = +10V, I_D = 18mA, f = 200MHz )</td>
<td></td>
<td>1.5 2.5</td>
<td>dB</td>
</tr>
<tr>
<td>( AGC_{V_{G2S}} ) Range Of Automatic Gain Control</td>
<td>( V_{DS} = +15V, V_{G1S} = +2.5V, V_{G2S} = +10V \rightarrow 0V, f = 200MHz )</td>
<td></td>
<td>50</td>
<td>dB</td>
</tr>
<tr>
<td>( E_{INT} ) Interfering Signal Level At Gate 1 For 1% Cross Modulation Distortion, Peak Voltage Referenced To 50Ω System(^3)</td>
<td>( V_{DS} = +15V, V_{G2S} = +8V, I_D = 15mA, Wanted signal f = 200MHz, Interfering signal f = 196MHz )</td>
<td></td>
<td>480</td>
<td>mV</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Measured in mixer test fixture.
2. Measured in amplifier test fixture.
3. Measured as shown in block diagram.

### SD305 CHARACTERISTIC CURVES

**DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE**

**DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE**

---

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SD305 CHARACTERISTIC CURVES (Continued)

GATE NO. 1 FORWARD TRANSCONDUCTANCE VS GATE NO. 2-TO-SOURCE VOLTAGE

GATE NO. 2 FORWARD TRANSCONDUCTANCE VS GATE NO. 1-TO-SOURCE VOLTAGE

S PARAMETERS

AMBIENT TEMP. \((T_A) = +25^\circ C\)
DRAIN-TO-SOURCE VOLTS \((V_{DS}) = +15\)

DRAIN MILLIAMPERES \((I_D) = 8\)
GATE NO. 1-TO-SOURCE VOLTS = GATE NO. 2-TO-SOURCE VOLTS

\[ S_{11} \]

\[ S_{12} \]

\[ S_{21} \]

\[ S_{22} \]
CONVERSION GAIN VS DRAIN CURRENT

DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE

GATE NO. 1 FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT

POWER GAIN VS FREQUENCY

POWER GAIN VS DRAIN CURRENT
AUTOMATIC GAIN CONTROL
VS $S_{11}$ AND $S_{22}$

AMBIENT TEMP. ($T_A$) = +25°C
DRAIN-TO-SOURCE VOLTS ($V_{DS}$) = +15

$S_{11}$

$S_{21}$

$S_{22}$

DRAIN MILLIAMPERES ($I_D$) = 50
GATE NO. 1-TO-SOURCE VOLTS = GATE NO. 2-TO-SOURCE VOLTS

S PARAMETERS

GATE NO. 2-TO-SOURCE VOLTS ($V_{G2S}$) = +4
FREQUENCY ($f$) = 200MHz

GATE NO. 1-TO-SOURCE VOLTS ($V_{G1S}$) = +15

FREQUENCY ($f$) = 200MHz

S11 CHARACTERISTIC CURVES (Continued)
SD306 CHARACTERISTIC CURVES

DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE

DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE

1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT

POWER GAIN VS FREQUENCY

POWER GAIN VS DRAIN MILLIAMPERES
SD306 CHARACTERISTIC CURVES (Continued)

**Noise Figure and Available Gain vs Drain Current**

![Graph of Noise Figure and Available Gain vs Drain Current](image)

**Automatic Gain Control Range at 200MHz**

![Graph of Automatic Gain Control Range at 200MHz](image)

**S11 and S22 vs Automatic Gain Control**

![Graph of S11 and S22 vs Automatic Gain Control](image)

**Interfering Signal Level vs Gate No. 2-to-Source Volts**

![Graph of Interfering Signal Level vs Gate No. 2-to-Source Volts](image)

**S Parameters**

- Ambient Temp. ($T_A$) = +25°C
- Drain Milliamperes ($I_D$) = 18
- Drain-to-Source Volts ($V_{DS}$) = 15

![Graph of S Parameters](image)
SD306 CHARACTERISTIC CURVES (Continued)

\[ S_{21} \]

\[ S_{22} \]

TEST CIRCUITS

SD305 200MHz/45MHz MIXER TEST CIRCUIT

SD306 200MHz TEST AMPLIFIER; POWER GAIN, NOISE FIGURE
SD306 TEST PROCEDURE FOR CROSS MODULATION DISTORTION MEASUREMENTS

1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.

2. Generator #2 is set at approximately -15dbm, 200MHz.

3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.

4. Turn off Generator #1 and turn off the modulation on Generator #2.

5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

BLOCK DIAGRAM OF CROSS MODULATION TEST
DESCRIPTION
The Signetics D-MOS SD5000, 5100 and 5200 series are monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enhancement mode technology.

This family of devices is designed to handle a wide variety of analog switching and driver applications. They are capable of high speed operation where excellent transient response, and wide voltage range are required. The SD5000 quad switch array and the SD5100 quad multiplexer can handle high voltage analog signals (±10V), whereas the SD5001 and SD5101 are designed for lower voltage applications. The SD5200 is intended for use as a 30V driver to complement the other switch products.

FEATURES
- LOW INPUT CAPACITANCE – 2.4pF
- LOW FEEDBACK CAPACITANCE – 0.3pF
- LOW OUTPUT CAPACITANCE – 1.3pF
- ±10V ANALOG SIGNAL RANGE
- LOW PROPAGATION DELAY TIME – 600ps
- LOW ON RESISTANCE – 30Ω
- LOW FEEDTHROUGH AND FEEDBACK TRANSIENTS
- ION IMPLANTED FOR GREATER RELIABILITY
- HIGH CHANNEL-TO-CHANNEL ISOLATION – 107dB
- TRANSIENT PROTECTION FOR GATES

SD5000 APPLICATIONS
ANALOG SWITCHING (UP TO VERY HIGH FREQUENCIES)
AUDIO ROUTING
CHOPPERS
CROSSPOINT SWITCHES
SAMPLE AND HOLD

SD5100 APPLICATIONS
MULTIPLEXING
CURRENT SUMMING

SD5200 APPLICATIONS
SWITCH DRIVERS
FUNCTIONAL AND SCHEMATIC DIAGRAMS

ABSOLUTE MAXIMUM RATINGS  \( T_A = 25^\circ C \) (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SD5000</th>
<th>SD5001</th>
<th>SD5100</th>
<th>SD5101</th>
<th>SD5200</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>( V_{DS} )</td>
<td>+20</td>
<td>+10</td>
<td>+30</td>
<td>+15</td>
<td>+30</td>
<td>Vdc</td>
</tr>
<tr>
<td>( V_{SD} )</td>
<td>+20</td>
<td>+10</td>
<td>+.5</td>
<td>+.5</td>
<td>+.5</td>
<td>Vdc</td>
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<tr>
<td>( V_{DB} )</td>
<td>+25</td>
<td>+15</td>
<td>+30</td>
<td>+15</td>
<td>+30</td>
<td>Vdc</td>
</tr>
<tr>
<td>( V_{SB} )</td>
<td>+25</td>
<td>+15</td>
<td>+.5</td>
<td>+.5</td>
<td>+.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>+25</td>
<td>+20</td>
<td>+20</td>
<td>+20</td>
<td>+20</td>
<td>Vdc</td>
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<tr>
<td>( V_{GB} )</td>
<td>-25</td>
<td>-15</td>
<td></td>
<td></td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>( V_{GD} )</td>
<td>+30</td>
<td>+25</td>
<td>+20</td>
<td>+20</td>
<td>+20</td>
<td>Vdc</td>
</tr>
<tr>
<td>( I_D )</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>mA</td>
</tr>
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Ambient Temperature Range

<p>| | | | | | | |</p>
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<tr>
<td>Storage</td>
<td>-55 to +150</td>
<td></td>
<td></td>
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<td>°C</td>
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<tr>
<td>Operating</td>
<td>0 to +85</td>
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Power Dissipation

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<td>Total Package Dissipation*</td>
<td>640</td>
<td></td>
<td></td>
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<tr>
<td>Individual Transistor Dissipation*</td>
<td>300</td>
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<td>mW</td>
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</table>

*Derated 5mW per degree centigrade.
CROSSTALK MEASUREMENT

QUAD SWITCH (SD5000/SD5001)

MULTIPlexer (SD5100/SD5101)

CROSSTALK = 20 Log \( \frac{V_{IN}}{V_{OUT}} \)
WHERE \( V_{IN} \) = 1V RMS AT 3kHz

TEST CIRCUIT NO. 1

TEST CIRCUIT NO. 2

THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of up to ±10 volts for the SD5000 and up to ±5 volts for the SD5001. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (VGS) is zero volts. When VGS exceeds the threshold voltage VT the FET switch starts to turn on. With VGS in excess of +10 volts, a low resistance path (typically 3\( \Omega \)) exists between input and output of the switch. Figure 1 below shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. In this case, the switch is driven by ±10 volts for which the SD5200 could be used as discussed later.

When analog signals are routed from one point to another the important factors are isolation, cross-talk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5000 series offers superior performance in all these areas.

Isolation. ON resistance is typically 30\( \Omega \) and OFF resistance is typically 10\( ^{10} \Omega \), which means the OFF to ON resistance ratio is in excess of 10\(^9\). Isolation from output to input from 3kHz analog signals is ~107dB.

Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example for 600\( \Omega \) source impedance the insertion loss for voice signals (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance the SD5000 switches turn on at sub-nanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB at 1GHz).

The SD5200 is intended as a driver for the SD5000/5001 but is capable of driving any system which requires ±15 volts. Four drivers are in each package and Figure 2 shows how a single driver is biased for ±15 volts. Two external resistors \( R_1 \), \( R_2 \) and a zener diode \( D_1 \) are required per driver. The input is 5V open collector TTL.
The SD5100 series is four channel multiplexers. The SD5100 has 0-30 volts input voltage capability and the SD5101 has 0-15 volts input voltage capability. Each circuit has a common source. The signals at the source are limited to ±200mV and therefore these circuits are used where switching is performed at the virtual ground point of an op amp. In this case, no external driver is required nor are any additional power supplies required. Because the ON resistance of both the SD5000 and SD5001 is very low (30Ω typ) and matched within 5Ω, the need for a compensating FET is minimized and in some cases eliminated. The parts can be driven directly from TTL, either +5 volts or +15 volts open collector.

**ANALOG SWITCH/DRIVER APPLICATION**

The SD5200 operates as an inverting switch capable of driving 30 volts maximum. This wide range capability with high speed fulfills most analog switching applications. Figure 3 demonstrates how the SD5200 drives the SD5000 in a typical analog switching application.

**ANALOG MULTIPLEXER APPLICATION**

The SD5100 series is easy to use as shown in Figure 4. Drive circuitry can be TTL or if very low RON is required (19Ω typ), then TTL open collector logic can drive the SD5100 up to +20 volts. The common source is kept at or near ground and each drain will withstand +30 volts with isolation typically 120dB.

If a compensation transistor is required in series with R2, then the maximum mismatch error for R1 = R2 = 10kΩ would be:

---

**ELECTRICAL CHARACTERISTICS**  \( T_A = +25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown Voltage</td>
</tr>
<tr>
<td>( BV_{DS} )</td>
</tr>
<tr>
<td>( BV_{SD} )</td>
</tr>
<tr>
<td>( BV_{DB} )</td>
</tr>
<tr>
<td>( BV_{SB} )</td>
</tr>
<tr>
<td>Leakage Current</td>
</tr>
<tr>
<td>( I_{DS} ) (OFF)</td>
</tr>
<tr>
<td>( I_{SD} ) (OFF)</td>
</tr>
<tr>
<td>( I_{GS} )</td>
</tr>
<tr>
<td>( I_{GB} )</td>
</tr>
<tr>
<td>( V_T )</td>
</tr>
<tr>
<td>( g_{fs} )</td>
</tr>
<tr>
<td>Small Signal Capacitances</td>
</tr>
<tr>
<td>( C_{IGS} + GD + GB )</td>
</tr>
<tr>
<td>( C_{GD} + DB )</td>
</tr>
<tr>
<td>( C_{IGS} + SB )</td>
</tr>
<tr>
<td>( C_{DG} )</td>
</tr>
<tr>
<td>( C_T )</td>
</tr>
<tr>
<td>( r_{DS} ) (ON)</td>
</tr>
<tr>
<td>( r_{DSM} ) (ON)</td>
</tr>
<tr>
<td>TEST CONDITIONS</td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>$V_{GS} = V_{BS} = -5V, I_S = 10nA$</td>
</tr>
<tr>
<td>$V_{GS} = V_{BS} = 0V, I_S = 1\mu A$</td>
</tr>
<tr>
<td>$V_{GB} = 0V, I_{D} = 1\mu A$</td>
</tr>
<tr>
<td>$V_{GB} = 0V, I_{S} = 10\mu A$</td>
</tr>
<tr>
<td>$V_{GS} = V_{BS} = -5V, I_{S} = 1\mu A$</td>
</tr>
<tr>
<td>$V_{GS} = V_{BS} = 0V, I_{S} = 10nA$</td>
</tr>
<tr>
<td>$V_{GB} = +20V, V_{DS} = +10V$</td>
</tr>
<tr>
<td>$V_{GB} = +25V$</td>
</tr>
<tr>
<td>Drain and Source OPEN</td>
</tr>
<tr>
<td>$V_{DS} = V_{DS}$</td>
</tr>
<tr>
<td>$V_{GS} = V_{T}, I_{S} = 1\mu A, V_{SB} = 0V$</td>
</tr>
<tr>
<td>$V_{DS} = 10V, V_{GS} = 0V, I_{D} = 20mA, f = 1kHz$</td>
</tr>
<tr>
<td>$V_{DS} = 10V, f = 1MHz$</td>
</tr>
<tr>
<td>$V_{GS} = V_{BS} = -15V$</td>
</tr>
</tbody>
</table>

| See Capacitance Model in Figure 1 | 2.4    | 3.5    | 2.4    | 3.5    | 2.4    | 3.5    | 2.4    | 3.5    | 2.4    | 3.5 pF |
| See Test Circuits No. 1 & 2, f = 3kHz | 1.3    | 1.5    | 1.3    | 1.5    | 1.3    | 1.5    | 1.3    | 1.5    | 1.3    | 1.5 pF |
| $I_D = 0.1mA, V_{GB} = 0$ | 0.3    | 0.5    | 0.3    | 0.5    | 0.3    | 0.5    | 0.3    | 0.5    | 0.3    | 0.5 pF |

Without the compensation transistor the error would be:

\[
\text{error} = \frac{R_2 + 65\Omega}{R_1 + 70\Omega} = .05\%
\]

\[
\text{error} = \frac{R_2}{R_1 + 70\Omega} = .7\%
\]
SWITCHING CHARACTERISTICS

<table>
<thead>
<tr>
<th>VDD</th>
<th>R_L</th>
<th>t_d (ON) (ns)</th>
<th>t_r (ns)</th>
<th>t_OFF (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>680</td>
<td>0.6</td>
<td>1.0</td>
<td>9.0</td>
</tr>
<tr>
<td>10</td>
<td>680</td>
<td>0.7</td>
<td>0.8</td>
<td>9.0</td>
</tr>
<tr>
<td>15</td>
<td>1k</td>
<td>0.9</td>
<td>1.0</td>
<td>14.0</td>
</tr>
</tbody>
</table>

* t_OFF is dependent on R_L and C_L and does not depend on the device characteristics.

TEST CIRCUIT

INPUT PULSE
- t_d, t_r < 1ns
- PULSE WIDTH = 100 ns
- REP RATE = 1 MHz
- SAMPLING SCOPE
  - t_r < 350 ps
  - R_L = 1 MΩ
  - C_L = 2.0 µF

CHARACTERISTIC CURVES

MAXIMUM POWER DISSIPATION VS TEMPERATURE

DRAIN-TO-SOURCE RESISTANCE VS SOURCE-TO-SUBSTRATE AND GATE-TO-SOURCE VOLTAGE
CHARACTERISTIC CURVES (Continued)

DRAIN-TO-SOURCE RESISTANCE VS TEMPERATURE

SOURCE-TO-DRAIN LEAKAGE CURRENT VS TEMPERATURE

DRAIN-TO-SOURCE LEAKAGE CURRENT VS TEMPERATURE

SOURCE-TO-SUBSTRATE LEAKAGE CURRENT VS TEMPERATURE

CROSSTALK VS FREQUENCY

GATE LEAKAGE CURRENT VS TEMPERATURE
DESCRIPTION
The Signetics D-MOS SD6000 is an integrated circuit fabricated by the double-diffused process and employing silicon N-channel enhancement mode MOSFETs with dual gates. Zener diodes are connected between all gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations. The use of the dual gate structure plus the incorporation of the drift region has made the feedback capacity (CG1D) typically less than 0.03pF. The attributes of the IC make it ideally suited for FM/VHF RF amplifier and mixer applications. The IC is specifically characterized for incorporation into varactor or conventional FM tuners but the performance guaranteed makes it useful in a wide variety of VHF tuner applications. The power gain at 100MHz is 30dB minimum with a guaranteed noise figure of 3.0dB. A wide AGC capability plus significant reduction in cross modulation is now available because of the inherent linearity of the D-MOS FETs. The SD6000 is packaged in the Signetics 8-pin plastic V package.

GENERAL FEATURES
- POSITIVE BIAS ONLY
- LOW GATE VOLTAGES
- ENHANCEMENT MODE OPERATION
- ZENER DIODE GATE PROTECTION
- ION IMPLANTED FOR GREATER RELIABILITY

FEATURES (RF AMP Section)
- HIGH POWER GAIN WITHOUT NEUTRALIZATION – 25dB AT 100MHz
- LOW NOISE FIGURE – 2.5dB AT 100MHz
- LOW INPUT AND OUTPUT CAPACITANCES CONSTANT WITH AGC – 3.0pF AND 1.0pF
- LOW FEEDBACK CAPACITANCE – 0.025pF
- SUPERIOR CROSS MODULATION PERFORMANCE
- HIGH TRANSCONDUCTANCE – 15mmhos
- WIDE AGC RANGE – 50dB AT 100MHz

FEATURES (Mixer Section)
- HIGH CONVERSION GAIN – 17dB AT 100MHz WITH VG1S = VG2S FOR BIASING SIMPLICITY

ABSOLUTE MAXIMUM RATINGS
T_A = 25°C (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DS</td>
<td>Drain-To-Source Voltage</td>
<td>−0.3</td>
<td>+20V</td>
</tr>
<tr>
<td>V_G1B</td>
<td>Gate No. 1-To-Substrate Voltage</td>
<td>−0.3</td>
<td>+20Vdc</td>
</tr>
<tr>
<td>V_G2B</td>
<td>Gate No. 2-To-Substrate Voltage</td>
<td>−0.3</td>
<td>+20Vdc</td>
</tr>
<tr>
<td>Drain Current</td>
<td></td>
<td>50mA</td>
<td></td>
</tr>
<tr>
<td>T_A</td>
<td>Ambient Temperature Range</td>
<td>−65°C</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage</td>
<td></td>
<td>−65°C</td>
<td>+125°C</td>
</tr>
<tr>
<td>Operating</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_T</td>
<td>Power Dissipation</td>
<td>625mW</td>
<td></td>
</tr>
</tbody>
</table>

At 25°C Case Temperature

Derate at 5.0mW/°C
### ELECTRICAL CHARACTERISTICS  $T_A = 25^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OFF Characteristics — RF Amp and Mixer</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$BV_{DS}$ Drain-To-Source</td>
<td>$V_{G1S} = V_{G2S} = 0V, I_D = 5\mu A$</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{D(OFF)}$ Drain-To-Source</td>
<td>$V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V$</td>
<td>0.001</td>
<td>1.0</td>
</tr>
<tr>
<td>Leakage Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DS}$ Zero Bias Drain Current</td>
<td>$V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V$</td>
<td>0.001</td>
<td>1.0</td>
</tr>
<tr>
<td>$I_{G1SS}$ Gate No. 1 Leakage</td>
<td>$V_{G1S} = +5V, V_{G2S} = V_{DS} = 0V$</td>
<td>0.001</td>
<td>0.1</td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{G2SS}$ Gate No. 2 Leakage</td>
<td>$V_{G2S} = +10V, V_{G1S} = V_{DS} = 0V$</td>
<td>0.001</td>
<td>0.1</td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ON Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{T1}$ Gate 1 Threshold Voltage</td>
<td>$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V, I_D = 1\mu A$</td>
<td>0.1</td>
<td>0.5</td>
</tr>
<tr>
<td>$V_{T2}$ Gate 2 Threshold Voltage</td>
<td>$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V, I_D = 1\mu A$</td>
<td>0.1</td>
<td>0.5</td>
</tr>
<tr>
<td>$r_{DS(ON)}$ Drain-To-Source On Resistance</td>
<td>$V_{G1S} = +5V, V_{G2S} = +10V, I_D = 0.1mA$</td>
<td>65</td>
<td>100</td>
</tr>
<tr>
<td><strong>Small Signal Characteristics — RF Amp</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$g_{fs}$ Forward Transconductance</td>
<td>$V_{DS} = +15V, V_{G2S} = +10V, I_D = 18mA, f = 1kHz$</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>Capacitances</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{G1S}$ Input</td>
<td>$V_{DS} = +15V, V_{G2S} = +10V, I_D = 18mA$</td>
<td>3.0</td>
<td>3.5</td>
</tr>
<tr>
<td>$C_{DS}$ Output</td>
<td>$V_{DS} = +15V, V_{G1S} = 0V, V_{G2S} = 10V$</td>
<td>1.0</td>
<td>1.3</td>
</tr>
<tr>
<td>$C_{G1D}$ Reverse Transfer</td>
<td>$V_{DS} = +15V, V_{G1S} = 0V, V_{G2S} = 10V$</td>
<td>0.025</td>
<td></td>
</tr>
<tr>
<td>Input Admittance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Re (y_{11})$</td>
<td></td>
<td>0.21</td>
<td></td>
</tr>
<tr>
<td>$Im (y_{11})$</td>
<td></td>
<td>2.26</td>
<td></td>
</tr>
<tr>
<td>Output Admittance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Re (y_{22})$</td>
<td></td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>$Im (y_{22})$</td>
<td></td>
<td>0.68</td>
<td></td>
</tr>
<tr>
<td>Forward Transmittance</td>
<td></td>
<td>12.85</td>
<td>-1.50</td>
</tr>
<tr>
<td>$Re (y_{21})$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Im (y_{21})$</td>
<td></td>
<td>0.01</td>
<td>-0.03</td>
</tr>
<tr>
<td>Reverse Transmittance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$G_{ps}$ Power Gain*</td>
<td>$V_{DS} = +15V, V_{G2S} = +10V$</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>$I_D = 18mA, f = 100MHz$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$NF$ Noise Figure*</td>
<td>$V_{DS} = +15V, V_{G2S} = +10V$</td>
<td>2.5</td>
<td>3.0</td>
</tr>
<tr>
<td>$I_D = 18mA, f = 100MHz$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$AGC(V_{G2S})$ Range Of Automatic Gain Control</td>
<td>$V_{DS} = +15V, V_{G1S} = +2.5V, f = 100MHz$</td>
<td>50</td>
<td></td>
</tr>
</tbody>
</table>

43
**ELECTRICAL CHARACTERISTICS (Continued) TA = 25°C**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LIMITS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Small Signal Characteristics — MIXER</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>gfs((CONV) Conversion Transconductance</td>
<td>V_DS = +15V, V_G1S = V_G2S, I_D = 8mA, f = 1kHz, E_LO (RMS) = 750mV</td>
<td>10</td>
<td>mmhos</td>
</tr>
<tr>
<td>Capacitances</td>
<td>f = 1MHz, Gate No. 2 AC Grounded</td>
<td>4.0</td>
<td>4.75 pF</td>
</tr>
<tr>
<td>C_GIS Input</td>
<td>V_DS = +15V, V_G1S = V_G2S, I_D = 8mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_DS Output</td>
<td>V_DS = +15V, V_G1S = 0V</td>
<td>1.1</td>
<td>1.5 pF</td>
</tr>
<tr>
<td>C_G1D Reverse Transfer</td>
<td>V_DS = +15V, V_G1S = 0V</td>
<td>0.030</td>
<td></td>
</tr>
<tr>
<td>Input Admittance</td>
<td>Re (y_{11})</td>
<td>0.21</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Im (y_{11})</td>
<td>2.28</td>
<td></td>
</tr>
<tr>
<td>Output Admittance</td>
<td>Re (y_{22})</td>
<td>0.41</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Im (y_{22})</td>
<td>1.04</td>
<td></td>
</tr>
<tr>
<td>Forward Transmittance</td>
<td>f = 100MHz, V_DS = +15V V_G1S = V_G2S, I_D = 8mA</td>
<td>3.18</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Re (y_{21})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Im (y_{21})</td>
<td>-0.83</td>
<td></td>
</tr>
<tr>
<td>Reverse Transmittance</td>
<td>Re (y_{12})</td>
<td>0.03</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Im (y_{12})</td>
<td>-0.01</td>
<td></td>
</tr>
<tr>
<td>Gps(CONV) Conversion Power Gain**</td>
<td>V_DS = +15V, V_G1S = V_G2S, I_D = 8mA, f_RF = 100MHz, f_LO = 89.3MHz</td>
<td>14</td>
<td>19 dB</td>
</tr>
</tbody>
</table>

*Measured in Amplifier test fixture.

**Measured in MIXER test fixture.

**CHARACTERISTIC CURVES**

**RF AMP SECTION**

**DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE**

**DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE**
CHARACTERISTIC CURVES (Continued)

**RF AMP SECTION**

**DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE**

- Ambient Temp. (T_a) = 25°C
- Drain-to-Source Volts (V_{DS}) = +15

**1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT**

- Ambient Temp. (T_a) = 25°C
- Drain-to-Source Volts (V_{DS}) = +15
- Frequency = 1kHz

**POWER GAIN VS DRAIN CURRENT**

- Ambient Temp. (T_a) = 25°C
- Drain-to-Source Volts (V_{DS}) = +15
- Gate No. 2-to-Source Volts (V_{G2S}) = +10

**NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT**

- Ambient Temp. (T_a) = 25°C
- Drain-to-Source Volts (V_{DS}) = +15
- Gate No. 2-to-Source Volts (V_{G2S}) = +10
- Frequency = 1kHz

**AUTOMATIC GAIN CONTROL RANGE**

- Ambient Temp. (T_a) = 25°C
- Drain-to-Source Volts (V_{DS}) = +15
- Gate No. 2-to-Source Volts (V_{G2S}) = +10
- Frequency = 1kHz
RF AMP SECTION

S11 VS FREQUENCY

S12 VS FREQUENCY

S21 VS FREQUENCY

S22 VS FREQUENCY

MIXER SECTION

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE

DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE
CHARACTERISTIC CURVES (Continued)

GATE NO. 1 FORWARD
TRANS CONDUCTANCE VS
GATE NO. 2-TO-SOURCE VOLTAGE

GATE NO. 1 FORWARD
TRANS CONDUCTANCE VS
DRAIN CURRENT

GATE NO. 2 FORWARD
TRANS CONDUCTANCE VS
GATE NO. 1-TO-SOURCE VOLTAGE

CONVERSION GAIN VS.
DRAIN CURRENT

S₁₁ VS FREQUENCY

S₁₂ VS FREQUENCY
CHARACTERISTIC CURVES (Continued)

MIXER SECTION

S21 VS FREQUENCY

- AMBIENT TEMP: T_A = 25°C
- DRAIN TO SOURCE VOLTS (VDS) = 15
- GATE NO. 1 TO SOURCE VOLTS (VGS1) = GATE NO. 2 TO SOURCE VOLTS (VGS2) = 0
- DRAIN MILLIAMPERES (I_D) = 10

S22 VS FREQUENCY

- AMBIENT TEMP: T_A = 25°C
- DRAIN TO SOURCE VOLTS (VDS) = 15
- GATE NO. 1 TO SOURCE VOLTS (VGS1) = GATE NO. 2 TO SOURCE VOLTS (VGS2) = 0
- DRAIN MILLIAMPERES (I_D) = 10

RF AMP SECTION TEST CIRCUIT

L1-L2: 5 TURN #18 WIRE 3/16" DIA, AIR CORE
TAPPED AT 1 TURN
C1-C2: NP0, ERIE NO. 538-011A-2-8
SIGNETICS D-MOS DUAL DUAL-GATE FETS, N-CHANNEL ENHANCEMENT • SD6000

MIXER SECTION TEST CIRCUIT

![Mixer Section Test Circuit Diagram]

FM TUNER USING SD6000 ELECTRICAL DATA

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td>+12V</td>
</tr>
<tr>
<td>Supply Current</td>
<td></td>
<td>25mA</td>
</tr>
<tr>
<td>Frequency Range</td>
<td></td>
<td>88MHz to 108MHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>RF Amp (-3dB)</td>
<td>2.5MHz</td>
</tr>
<tr>
<td></td>
<td>Mixer (-3dB)</td>
<td>300kHz</td>
</tr>
<tr>
<td>Input Impedance</td>
<td></td>
<td>75Ω</td>
</tr>
<tr>
<td>Output Impedance</td>
<td></td>
<td>50Ω</td>
</tr>
<tr>
<td>IF Output Frequency</td>
<td></td>
<td>10.7MHz</td>
</tr>
<tr>
<td>Oscillator Stability w/respect to Supply Voltage</td>
<td>40kHz/volt</td>
<td></td>
</tr>
<tr>
<td>Oscillator Stability w/respect to Temperature</td>
<td>10kHz/°C</td>
<td></td>
</tr>
<tr>
<td>Power Gain</td>
<td>88MHz to 108MHz</td>
<td>30dB Min</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>@ 100MHz</td>
<td>3.0dB Max</td>
</tr>
</tbody>
</table>
FM TUNER USING SD6000

PARTS LIST

1. Transistors
   - Q1: PNP Silicon, Type 2N4126

2. Integrated Circuits
   - U1: Dual D-MOS FET, Type SD6000V

3. Resistors (All carbon resistors in ohms ±10% tolerance.)
   - R1: 30k
   - R2: 68k
   - R3: 200k
   - R4: 150k
   - R5: 39k
   - R6: 82k
   - R7: 120
   - R8: 6800
   - R9: 13k
   - R10: 3k

4. Capacitors
   - C1: 5-20pF, Type 3 Gang Tuning Capacitor
   - C2: 20pF, Type ±5% NPO

5. Miscellaneous Components
   - T1: IF Transformer, Cambion 533-3652-003
   - Jcore Prim. 30T #26, Sec. 2T #26
   - L1: RF Input Coil, 4 turns #18 on 3/16" dia. Air core - Tap 1 turn from ground side.
   - L2: RF Output Coil, 4 turns #18 on 3/16" dia. air core.
   - L3: Oscillator Coil, 4 turns #18 on 3/16" dia. air core center-tapped.
   - L4: 33µh RF choke
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Signetics International Corp.
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63 Croydon Road
Penge
London SE20 7TW
Phone: 01-659 2111

WEST GERMANY
Signetics G mb H
D-4006 Dusseldorf-Erkath
Rathelbeckerweg 42
Phone: (0211) 244238

Signetics G mb H
D-2 Hamburg 67
Eulenkrugstrasse 81E
Phone: (040) 60-35-242

JAPAN
Asahi Glass Co. Ltd.
1-2 Marunouchi, 2 Chome
Chiyoda-ku, Tokyo
Phone: 218-5536

KOREA
Kumho & Co., Inc.
Dongwha Building
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Seoul
Phone: 28-5271/24-3241/22-0404

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Aberdeen
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Phone: 28-527195/519763

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Asahi Glass Co. Ltd.
1-2 Marunouchi, 2 Chome
Chiyoda-ku, Tokyo
Phone: 218-5536

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Kumho & Co., Inc.
Dongwha Building
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