The SB-1250 is the first MIPS64™ processor to offer the fast-growing networking and communications markets. The SB-1250 is the first MIPS64™ processor to offer the industry-leading performance, high functional integration, and low power levels required by next-generation networking applications. Specifically, the SB-1250 delivers on a single chip:

- Two quad issue, 64-bit, MIPS CPUs running at 600 MHz -1 GHz
- 128 Gbit/sec peak on chip bus bandwidth to enable high-speed packet processing
- 50 Gbit/sec peak memory bandwidth for fast memory accesses with minimal latency
- 25 Gbit/sec total I/O bandwidth for high-speed data transfers
- 8-10W in power consumption, making it the lowest power processor for its performance class

The SB-1250 will be manufactured in TSMC’s 0.15 micron process, and is packaged in a 860 ball BGA package.

**Overview**

SiByte’s first Mercurian™ processor, SB-1250, is a state-of-the-art multi-processor solution targeted at the fast-growing networking and communications markets. The SB-1250 is the first MIPS64™ processor to offer the industry-leading performance, high functional integration, and low power levels required by next-generation networking applications. Specifically, the SB-1250 delivers on a single chip:

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**Implementation of MIPS64 ISA**

The SB-1 CPU core is a high-performance implementation of the standard MIPS64 Instruction Set Architecture (ISA), and incorporates the MIPS-3D and MIPS-MDMX Application Specific Extensions (ASEs). The core supports a 4-issue enhanced skew pipeline and can dispatch up to two memory and two ALU (Integer, Floating Point, MDMX or MIPS-3D) instructions per cycle.

**Key Features**

**Two SB-1 CPUs operating at 600 MHz-1 GHz, each with:**
- Quad-issue in-order pipeline; dual execute, dual memory pipes
- 32K Instruction Cache, 4-way associative
- 32K Data Cache, 2 accesses per cycle, 4-way associative
- Advanced Branch Predictors
- 128 entry TLB

**ZBus:**
- Connects the CPUs, L2 cache, memory and I/O bridges
- Runs at half the CPU core clock; 256-bit wide data bus

**On-Chip L2 Cache:**
- 512K, ECC protected, shared by both CPUs
- Ways can be removed to enable 128KB memory banks

**DDR SDRAM memory controller:**
- Two channels, each with a 64-bit data bus plus ECC
- Runs up to 200 MHz clock, 400 MHz data rate
- Supports up to 8 GB memory systems

**High-Speed Network I/O:**
- Three 10/100/1000 Ethernet MACs; 802.3 compliant
- Option to configure MACs into two 16-bit packet FIFO interfaces to enable full duplex OC-48 data rates

**Standard I/O:**
- PCI: 32-bit, 33/66 MHz
- LDT: 400 MHz clock, peak bandwidth of 6.4 Gbit/sec in each direction

**System I/O:**
- SMBus serial configuration interface
- Two serial interfaces (UART or synchronous)
- PCMCIA control interface
- On-Chip system control and debug
- Generic I/O

**Other Features:**
- DMA controllers for serial and Ethernet ports
- Internal data mover for moving data from any source to any destination address