ST62
GENERAL PURPOSE

DATABOOK

4th EDITION

SGS-THOMSON
MICROELECTRONICS

GENERAL PURPOSE ST62

SGS-THOMSON
MICROELECTRONICS

4661

ST62
GENERAL PURPOSE

DATABOOK

4th EDITION

OCTOBER 1994

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

INTRODUCTION

SGS-THOMSON Microelectronics provides a wide range of microcontroller products to suit all major application environments. From the high level control of systems (ST9, ST10 and ST20 families), through a range of intermediate level products (ST7) to controllers offering the economical solutions to the control of small systems. SGS-THOMSON has introduced the ST6 family, enhanced by the multi-purpose CMOS technology integrating non-volatile EPROM and EEPROM memories, to continue the level of economy initially offered by the COPs family.

The ST6 family has been developped to suit fully flexible control systems, by maximising the features integrated onto the silicon and accordingly minimising the number of external devices required. This brings the benefit of reducing the total system cost, very attractive for high volume control equipment among consumer, industrial and automotive applications.

ST62 OVERVIEW

Devices in the ST62 family are designed to exhibit key benefits for noisy environments, with their excellent EMI characteristics. Built-in hardware features minimise the noise generated by MCU operation and provide a high immunity to external noise.

Generation of noise is kept low by the careful control of the output buffer switching speeds and by employing an internal serial databus that minimises the number of transistors that switch simultaneously. The sensitivity to external noise is minimised by several features including the wide 3 to 6 volt supply voltage range and built-in protection diodes in the I/O ports.

Other major benefits include a full choice of EPROM, OTP and ROM versions to cover all needs from prototyping to high volume production; direct interfacing to analogue sensors, LEDs and power loads such as triacs and relays with the integral A/D converter and the 20mA output buffers. For user input and feedback, ST62 family members also provide efficient keyboard scanning configurations and direct LCD display drive. Several family members offer high reliability EEPROM for parameter storage.

In addition to the EPROM and OTP ROM equivalent parts (for quick preproduction evaluation and test), shortening the critical development phase, reducing the Time to Market is also aided by full-feature development support tools: Assembler and Linker, Software simulator, Real-time Hardware Emulators and production EPROM programmers (see following tables).

Display requirements with LCD displays are easily handled (dot-matrix or static up to 4 way multiplex drive) by the ST62 LCD driver family members ST624x and ST628x. Brief introductions to these ST62 LCD driver MCUs are given in this book, for full information on these products please refer to the ST62 LCD Driver databook 1st edition (reference DBST624xFST/1) or a later edition.

ST62	ROM	RAM	LCD	EEPROM	I/O	A/D	LED	LCD	8bit	AR	SPI	PACKAGE
	K		RAM						TIMER	TIMER		
ST6240	8	192	24	128	16	12	4	4x45	2		1	QFP80
ST6242	8	128	24		10	6	4	4x40	1		1	QFP64
ST6245	4	128	12	64	11	7	4	4x24	2		1	QFP52
ST6280	8	192	128	128	22	12	10	16x48	1	1	1	QFP100
ST6285	8	192	96	-	12	8	4	16x40	1		1	QFP80

LED = Led or TRIAC driving AR TIMER = Auto Reload Timer SPI = Serial Peripheral Interface

Further ST6 family members are dedicated to TV and Satellite tuning control applications (please refer to the SGS-THOMSON Video Products Databook, Volume 1 Signal Processing, for further information on the ST63 dedicated products).

GENERAL PURPOSE ST62 OVERVIEW

The General Purpose members of the ST62 family of microcontrollers are Microcontrollers with "standard" peripherals encompassing most low-end embedded control requirements. It has been seen that nearly all equipments involving a control system, from children's animated toys and novelties to industrial and consumer controllers, have benefited from the use of a microcontroller. Not only from the increased ease of design, but also with the flexibility for change and upgrade, and system redefinition to differentiate between models in a range and against competitors.

The ST62 General Purpose Microcontroller family gives different mixes of I/O lines, timers, analog to digital converters, packages and memory sizes (RAM, ROM/EPROM and EEPROM) to offer a suitable device for your application's needs. To help you in choosing, and to provide a quick route to development, the ST62 Starter Kits are low-cost tools providing program development support, even to the extent of the included programmers for the equivalent EPROM version. With this, prototypes can be made in the correct form factor packaging as the final product, greatly optimising marketing and qualification trials. Thus "General Purpose" means here that there is no dedicated application that the ST6 has been designed for, the choice is fully open for you, so welcome to the world of the ST62 General Purpose Microcontrollers.

ST62	ROM K	RAM	EEPROM	I/O	A/D	LED	8bit TIMER	AR TIMER	SPI	PACKAGE
ST6210B	2	64		12	8	4	1			DIP20/SO20
ST6215B	2	64		20	16	4	1			DIP28/SO28
ST6220B	4	64		12	8	4	1			DIP20/SO20
ST6225B	4	64		20	16	4	1			DIP28/SO28
ST6230*	8	192	128	36						DIP28/SO28
ST6232*	8	192	128	36						DIP42
ST6235*	8	192	128	36						QFP52
ST6260B	4	128	128	13	7	6	1	1	1	DIP20/SO20
ST6265B	4	128	128	21	13	8	1	1	1	DIP28/SO28

AR TIMER = Auto Reload Timer SPI = Serial Peripheral Interface

* Under Development

INTRODUCTION

Tools for ST62xx Family

DEVICES		EMULATOR		
ROM	EPROM/OTP	COMPLETE	DEDICATION BOARD	PROBE
ST621X ST622X ST621XB ST622XB	ST62E1X/T1X ST62E2X/T2X ST62E1XB/T1XB ST62E2XB/T2XB	ST626X-EMU(3/6V)	ST626X-DBE	included in EMU and DBE
ST624X	ST62E4X/T4X	ST624X-EMU (no probe) ST6240-EMU (with probe) ST6242-EMU (with probe) ST6245-EMU (with probe)	ST624X-DBE (no probe)	ST6240-P/QFP ST6242-P/QFP ST6245-P/QFP
ST626X ST629X	ST62E6X/T6X ST62E9X/T9X	ST626X-EMU	ST626X-DBE	included in EMU and DBE
ST628X	ST62E8X/T8X	ST628X-EMU (no probe) ST6280-EMU (with probe) ST6285-EMU (with probe)	ST628X-DBE (no probe)	ST6280-P/QFP ST6285-P/QFP
Software tools		ST6-SW/PC		
ST636X/7X/8X	ST63E85/T85	ST638X-EMU	ST638X-DBE	Included in EMU & DBE
ST6369	ST63E69/T69			
ST631XX	ST63E1XX/T1XX	ST631XX-EMU	ST631XX-DBE	

Tools for ST62xx Family (Continued)

DEVICES		EPROM PROGRAMMER			KIT
ROM	EPROM/OTP	SINGLE EPROM	COMPLETE GANG	GANG ADAPTOR	
ST621X ST622X ST621XB ST622XB	ST62E1X/T1X ST62E2X/T2X ST62E1XB/T1XB ST62E2XB/T2XB	ST62E1X-EPB/220 ST62E1X-EPB/110	ST62E10-GP/DIP ST62E10-GP/SO ST62E15-GP/DIP ST62E15-GP/SO	ST62E10-GPA/DIP ST62E10-GPA/SO ST62E15-GPA/DIP ST62E15-GPA/SO	ST6220-KIT/220 ST6220-KIT/110 ST6220-KIT/UK ST622X-KIT/220 ST622X-KIT/110 ST622X-KIT/UK ST622X-PWRKIT/50 ST622X-PWRKIT/60
ST624X	ST62E4X/T4X	ST62E4X-EPB-PC ST62E4X-EPB/220 ST62E4X-EPB/110	ST62E40-GP/QFP ST62E42-GP/QFP ST62E45-GP/QFP	ST62E40-GPA/QFP ST62E42-GPA/QFP ST62E45-GPA/QFP	ST6240-KIT/220 ST6240-KIT/110 ST6240-KIT/UK
ST626X ST629X	ST62E6X/T6X ST62E9X/T9X	ST62E6X-EPB/220 ST62E6X-EPB/110	ST62E60-GP/DIP ST62E60-GP/SO ST62E65-GP/DIP ST62E65-GP/SO	ST62E60-GPA/DIP ST62E60-GPA/SO ST62E65-GPA/DIP ST62E65-GPA/SO ST62E94-GPA/DIP	ST626X-KIT/220 ST626X-KIT/110 ST626X-KIT/UK
ST628X	ST62E8X/T8X	ST62E8X-EPB/220 ST62E8X-EPB/110	Under development 62E80GP/QFP	Under development 62E80GPA/QFP	
Software tools			ST62E85-GP/QFP	ST62E85-GPA/QFP	ST62-FUZZY/PC
ST636X/7X/8X	ST63E85/T85	ST638X-EMU	ST638X-DBE	Included in EMU & DBE	
ST6369	ST63E69/T69				
ST631XX	ST631XX/T1XX	ST63E1XX-EPB/220			

GENERAL INDEX

GENERAL INDEX

ST621xB DATASHEETS

ST622xB DATASHEET INDEX

Page Number

SGS-THOMSON
MICROELECTRONICS

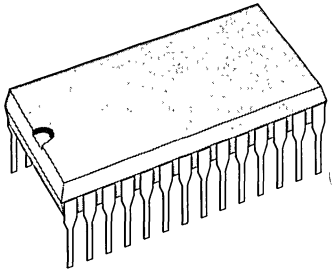
ST6210B-ST6215B
ST6220B-ST6225B

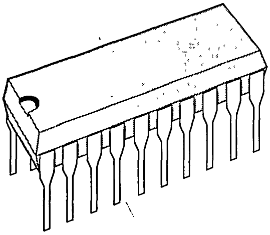
8-BIT HCMOS MCUs WITH A/D CONVERTER

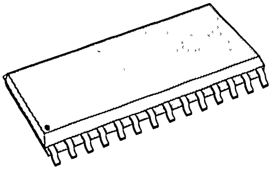
PRELIMINARY DATA

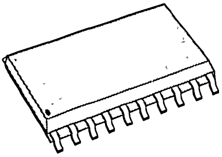
- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait, Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 1828 bytes (ST6210B, 15B)
  3876 bytes (ST6220B, 25B)
- Data ROM: User selectable size
  (in program ROM)
- Data RAM: 64 bytes
- ROM readout Protection
- PDIP20, PSO20 (ST6210B, 20B) packages
- PDIP28, PSO28 (ST6215B, 25B) packages
- 12/20 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler
- Digital Watchdog and Oscillator Safe Guard
- 8 bit A/D Converter with up to 8 (ST6210B, 20B) and up to 16 (ST6215B, 25B) analog inputs
- On-chip clock oscillator driven by Quartz Crystal, Ceramic resonator or RC network
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The development tool of the ST621xB, 2xB microcontrollers consists of the ST626x-EMU emulation and development system connected via an RS232 serial line to an MS-DOS PC

Device Summary page 3/67


PDIP28


PDIP20

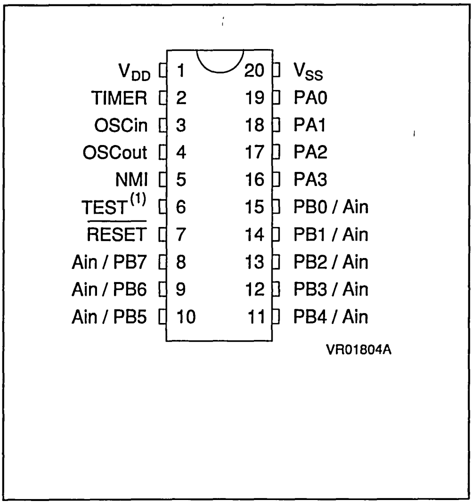

PSO28


PSO20

(Ordering Information at the end of the datasheet)

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. ST6210B, ST6220B Pin Configuration



Note 1. This pin is also the V_{PP} input for EPROM based device.

Figure 2. ST6215B, ST6225B Pin Configuration

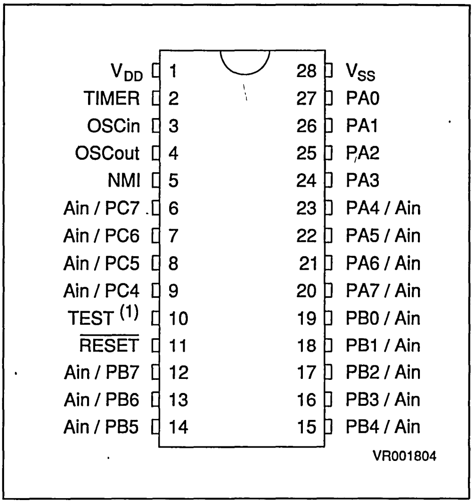
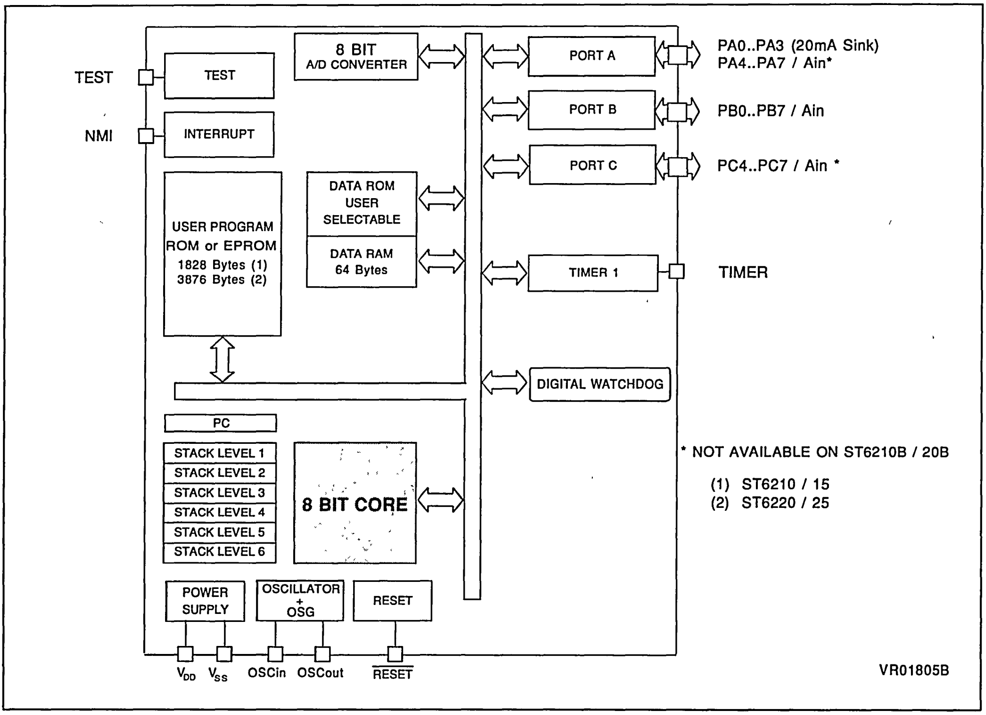


Figure 3. Block Diagram



GENERAL DESCRIPTION

The ST6210B, ST6215B, ST6220B and ST6225B microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).

The macrocells of the ST6210B, 15B, 20B and 25B are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler, the 8-bit A/D Converter with up to 8 (ST6210B, 20B) and up to 16 (ST6215B, 25B) analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD).

The ST621xB, 2xB are upward compatible with the ST621x, 2x. They in addition feature enhanced RC oscillator, Oscillator Safe Guard, Readout Protection against Piracy and a new External STOP Mode Control option to enlarge the range of power consumption/safety trade-offs.

These devices are well suited for automotive, appliance and industrial applications. The ST62E20B and ST62E25B EPROM versions are available for prototypes and low-volume production; also OTP versions are available. The only difference between these devices are program memory size and I/O pin number, following the table below.

DEVICE SUMMARY

Device	ROM (Bytes)	I/O Pins
ST6210B	2K	12
ST6215B	2K	20
ST6220B	4K	12
ST6225B	4K	20

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. When the QUARTZ/CERAMIC RESONATOR mask option is selected, a quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins. When the RC OSCILLATOR mask option is selected, a resistor must be connected between the pin OSCout and the ground. The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to thebeginning of its program.

TEST. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive.
On ST6210B, 15B, 20B, 25B the user can select as ROM mask option the availability of an on-chip pull-up at NMI pin.

TIMER. This is the timer I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time-out occurs.
On ST6210B, 15B, 20B, 25B the user can select as ROM mask option the availability of an on-chip pull-up at TIMER pin.

PA0-PA3,PA4-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs. PA0-PA3 can also sink 20mA for direct LED driving while PA4-PA7 can be programmed as analog inputs for the A/D converter.,
Note. PA4-PA7 are not available on ST6210B, ST6220B.

PB0-PB7. These 8 lines are organized as one I/O port (B). When the External STOP Mode Control option is disabled, each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter. When the External STOP Mode Control option is enabled, PB0 output Mode is forced as open-drain (push-pull output is not possible). The other lines are unchanged.

PC4-PC7. These 4 lines are organized as one I/O port (C). When the External STOP Mode Control option is disabled, each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter. When the External STOP Mode Control is enabled PC7output Mode is forced as open-drain (push-pull output is not possible) . The other lines are unchanged.
Note. PC4-PC7 are not available on ST6210B, ST6220B.

ST62xx CORE

The core of the ST62xx Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in Figure 5; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST62xx Family core has six registers and three pairs of flags available to the programmer. They are shown in Figure 4 and are explained in the following paragraphs.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at address FFh. Accordingly the ST62xx instruction set can use the accumulator as any other register of the data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode. These registers can be

Figure 4. ST62xx Core Programming Model

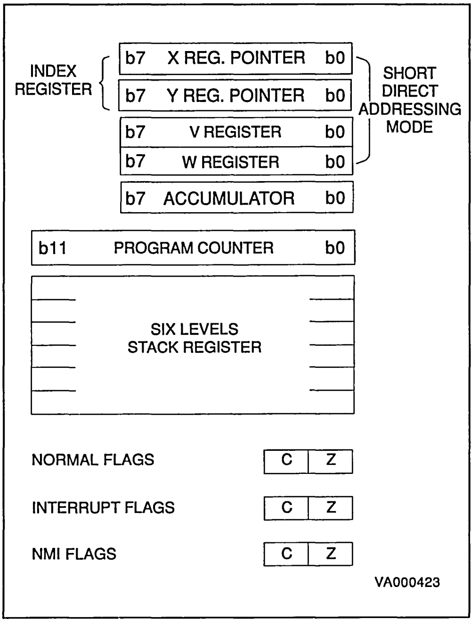
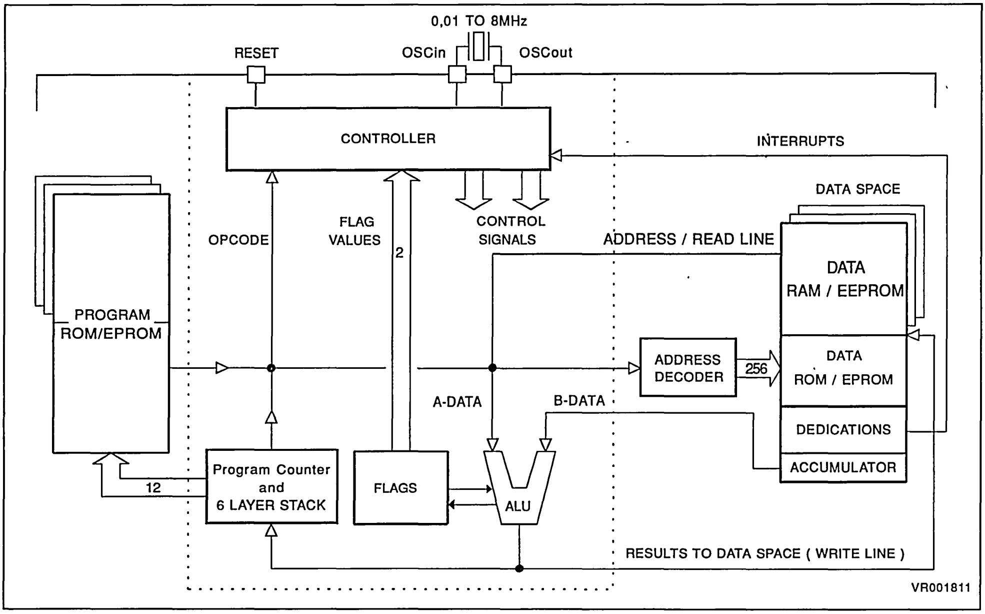


Figure 5. ST62xx Core Block Diagram



ST62xx CORE (Continued)

addressed in the data space as RAM locations at addresses 80h (X) and 81h (Y). They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST62xx instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at addresses 82h (V) and 83h (W). They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST62xx instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. Nevertheless, if the program space contains more than 4096 locations, the further program space can be addressed by using the Program Bank Switch register. The PC value is incremented, after it is read the address of the current instruction. To execute relative jumps the PC and the offset are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

- JP (Jump) instruction . . .	PC= Jump address
- CALL instruction	PC= Call address
- Relative Branch Instructions.	PC= PC± offset
- Interrupt	PC=Interrupt vector
- Reset	PC= Reset vector
- RET & RETI instructions .	PC= Pop (stack)
- Normal instruction	PC= PC + 1

Flags (C, Z)

The ST62xx core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI, ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST62xx core uses the pair of flags that correspond to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST62xx core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. It should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The flags are not cleared during the context switching and so remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

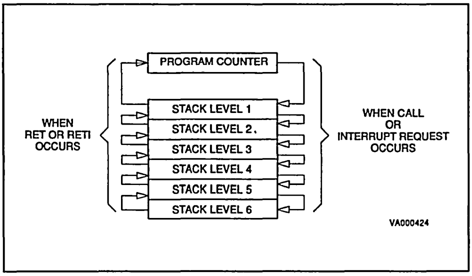
The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

The switching between the three sets of flags is automatically performed when an NMI, an interrupt or a RETI instructions occurs. As the NMI mode is automatically selected after the reset of the MCU, the ST62xx core uses at first the NMI flags.

Stack

The ST62xx core includes true LIFO hardware stack that eliminates the need for a stack pointer. The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When a subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is popped back into the previous level. These two operating modes are described in Figure 6. Since the accumulator, as all other data space registers, is not stored in this stack the handling of these registers should be performed inside the subroutine. The stack pointer will remain in its deepest position if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

Figure 6. Stack Operation



MEMORY SPACES

The MCU operates in three different memory spaces: program space, data space, and stack space. A description of these spaces is shown in the following figures.

Program Space

The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and the user vectors. It is addressed by the 12-bit Program Counter register (PC register) and so the ST62xx core can directly address up to 4K bytes of Program Space. ST62 devices with more than 4K ROM use ROM banked program memory (not available on ST6210B, 15B, 20B, 25B).

Rom Protection

The ST621xB, 2xB program space can be protected against external reading of the ROM contents when the READOUT PROTECTION mask option is selected. If this option is selected, the user can blow a dedicated fuse on the silicon by applying a high voltage at V_{PP} (see detailed information in the "Electrical Specification").

Note:

Once the fuse is blown, it is no longer possible, even for SGS-THOMSON, to gain access to the ROM contents. Returned parts with blown fuse can therefore not be accepted.

Table 1. ST6210B, 15B Program ROM Memory

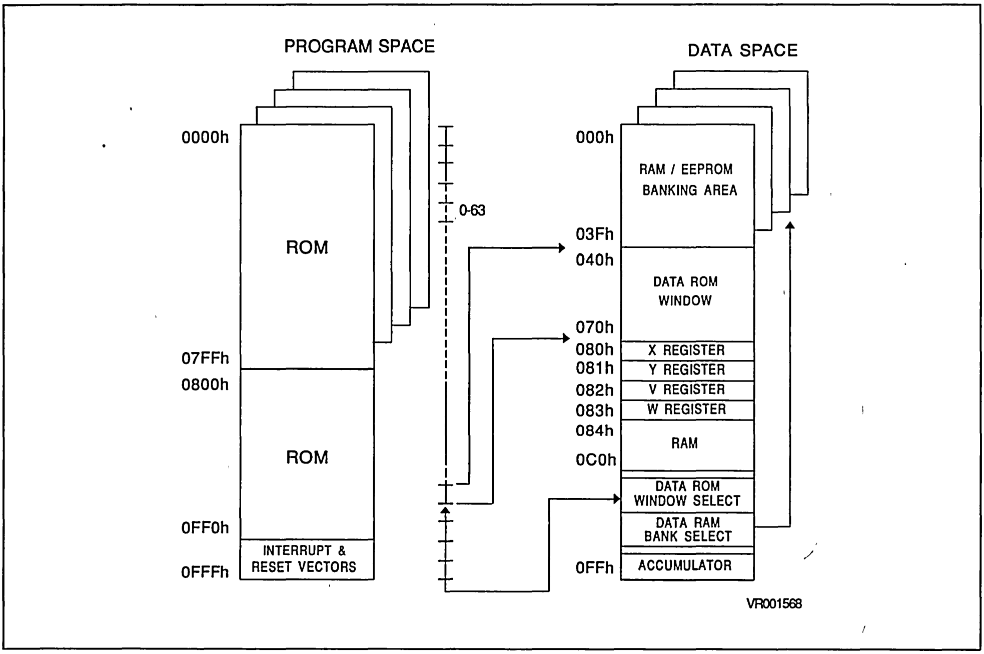
Device Address	Description
0000h-07FFh 0800h-087Fh	Not implemented Reserved
0880h-0F9Fh	User Program ROM 1828 Bytes
0FA0h-0FEFh 0FF0h-0FF7h 0FF8h-0FFBh 0FFCh-0FFDh 0FFEh-0FFFh	Reserved Interrupt Vectors Reserved NMI Vector User Reset Vector

Table 2. ST6220B, 25B Program ROM Memory

Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3872 Bytes
0FA0h-0FEFh 0FF0h-0FF7h 0FF8h-0FFBh 0FFCh-0FFDh 0FFEh-0FFFh	Reserved Interrupt Vectors Reserved NMI Vector User Reset Vector

MEMORY SPACES (Continued)

Figure 7. Memory Addressing Description Diagram



MEMORY SPACES (Continued)

Data Space

The instruction set of the ST62xx core operates on a specific space, named Data Space, that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM, ST62xx core/peripheral registers, and read-only data such as constants and look-up tables.

Data ROM. All the read-only data is physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory contains consequently the program to be executed, the constants and the look-up tables needed for the program.

The locations of Data Space in which the different constants and look-up tables are addressed by the ST62xx core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory.

Data RAM. In the ST6210B, ST6215B, ST6220B and ST6225B products the data space includes 60 bytes of RAM, the accumulator (A), the indirect registers (X), (Y), the short direct registers (V), (W), the I/O port registers, the peripheral data and control registers, the interrupt option register and the Data ROM Window register (DRW register).

As the data space is less than 256 bytes the ST62xx core can directly address this area and the Data Bank Switch register (DRBR) has not been implemented.

Stack Space

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

Figure 8. ST6210B,15B,20B,25B Data Memory Space

NOT IMPLEMENTED	000h 03Fh
DATA ROM WINDOW 64 BYTES	040h 07Fh
X REGISTER	080h
Y REGISTER	081h
V REGISTER	082h
W REGISTER	083h
DATA RAM 60 BYTES	084h 0BFh
PORT A DATA REGISTER	0C0h
PORT B DATA REGISTER	0C1h
PORT C DATA REGISTER	0C2h
RESERVED	0C3h
PORT A DIRECTION REGISTER	0C4h
PORT B DIRECTION REGISTER	0C5h
PORT C DIRECTION REGISTER	0C6h
RESERVED	0C7h
INTERRUPT OPTION REGISTER	0C8h*
DATA ROM WINDOW REGISTER	0C9h*
RESERVED	0CAh 0CBh
PORT A OPTION REGISTER	0CCh
PORT B OPTION REGISTER	0CDh
PORT C OPTION REGISTER	0CEh
RESERVED	0CFh
A/D DATA REGISTER	0D0h
A/D CONTROL REGISTER	0D1h
TIMER PSC REGISTER	0D2h
TIMER DATA REGISTER	0D3h
TIMER TSCR REGISTER	0D4h
RESERVED	0D5h 0D7h
WATCHDOG REGISTER	0D8h
RESERVED	0D9h 0FEh
ACCUMULATOR	0FFh

* WRITE ONLY REGISTER

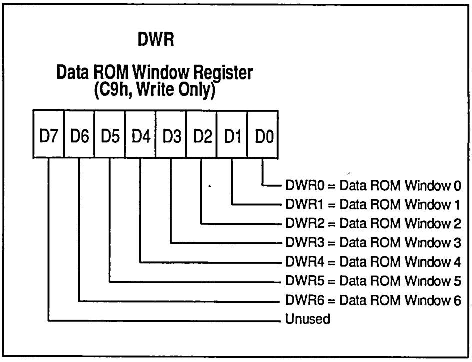
MEMORY SPACES (Continued)

Data Window register (DWR)

The Data ROM window is located from address 040h to address 7Fh in the Data space. It allows the direct reading of 64 consecutive bytes located anywhere in the ROM memory between the addresses 0000h and 1FFFh (if implemented on the particular device). All the bytes of the ROM memory can therefore be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data Window register (DWR register, location C9h).

The DWR register can be addressed like a RAM location in the Data Space at the address C9h, nevertheless it is a write only register that cannot be accessed with single-bit operations. This register is used to move the 64-byte read-only data window (from the 40h address to 7Fh address of the Data Space) up and down the ROM memory of the MCU in steps of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 least significant bits of the register address given in the instruction (as least significant bits) and the content of the DWR register (as most significant bits, see Figure 8). So when addressing location 40h of dataspace, and 0 is loaded in the DWR register, the phisycal addressed location in ROM is 00h. The DWR register is not cleared at reset, therefore it must be written to before the first access to the Data ROM window area.

Figure 10. Data ROM Window Register



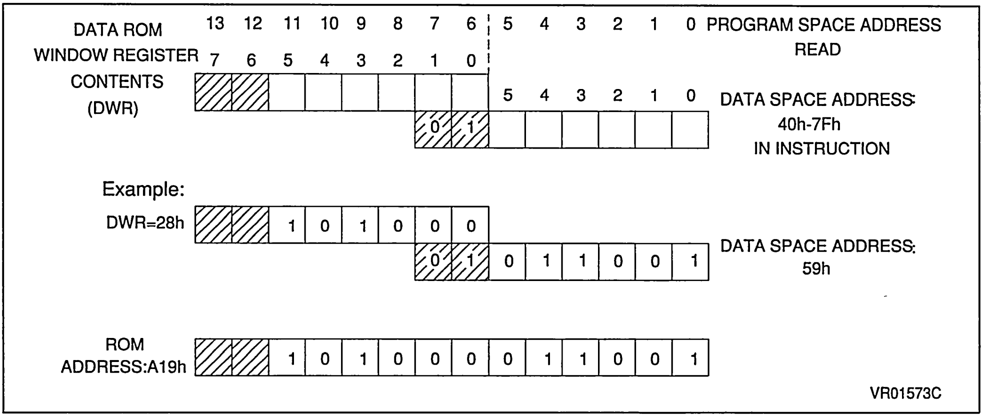
D7. This bit is not used.

DWR6-DWR0. These are the Data ROM Window bits that correspond to the upper bits of the data ROM space.

This register is undefined on reset. Neither read nor single bit instructions may be used to address this register.

Note: Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in the interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to the DWR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR is not affected.

Figure 9. Data ROM Window Memory Addressing



TEST MODE

For normal operation the TEST pin must be held low when reset is active. An on-chip 100kΩ pull-down resistor is internally connected to the TEST pin.

INTERRUPT

The ST62xx core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 1). When a source provides an interrupt request, and the request processing is also enabled by the ST62xx core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction). Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The ST6210B, ST6215B, ST6220B and ST6225B microcontrollers have six different interrupt sources associated to different interrupt vectors as it is described in table below.

Table 3. Interrupt Vector/Source Relationship

Interrupt Source	Associated Vector	Vector Address
NMI pin	Interrupt vector #0 (NMI)	(FFCh, FFDh)
Port A pins	Interrupt vector #1	(FF6h, FF7h)
Port B pins	Interrupt vector #2	(FF4h, FF5h)
Port C pins	Interrupt vector #2	(FF4h, FF5h)
TIMER peripheral	Interrupt vector #3	(FF2h, FF3h)
ADC peripheral	Interrupt vector #4	(FF0h, FF1h)

Interrupt Vectors Description

- The ST62xx core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines in the static page of the Program Space.
- The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at addresses FFCh,FFDh in the Program Space. On ST6210B, ST6215B, ST6220B and ST6225B this vector is associated with the external falling edge sensitive interrupt pin (NMI).
- The interrupt vector located at addresses FF6h, FF7h is named interrupt vector #1. It is associated with Port A pins and can be programmed by software either in the falling edge detection mode or in the low level sensitive detection mode according to the code loaded in the Interrupt Option Register (IOR).
- The interrupt vector located at addresses FF4h, FF5h is named interrupt vector #2. It is associated with Port B and C pins and can be programmed by software either in the falling edge detection mode or in the positive edge detection mode according to the code loaded in the Interrupt Option Register (IOR).
- The two interrupt vectors located respectively at addresses FF2h, FF3h and addresses FF0h, FF1h are respectively named interrupt vector #3 and #4. Vector #3 is associated to the TIMER peripheral and vector #4 to the A/D converter peripheral.

All the on-chip peripherals have an interrupt request flag bit (TMZ for timer, EOC for A/D), that is set to one when the device generates an interrupt request and a mask bit (ETI for timer, EAI for A/D) that must be set to one to allow the transfer of the flag bit to the core.

Interrupt Priority

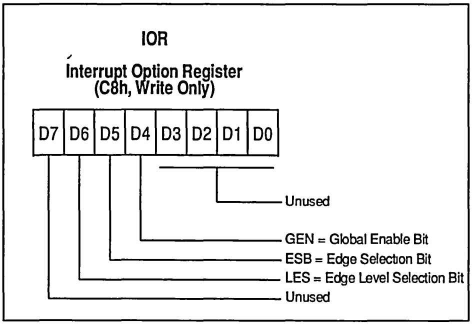
The non-maskable interrupt request has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the four other interrupts can not interrupt each other. If more than one interrupt request are pending, they are processed by the ST62xx core according to their priority level: vector #1 has the higher priority while vector #4 the lower.
The priority of each interrupt source is fixed.

INTERRUPT (Continued)

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8h) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the address C8h, nevertheless it is a write-only register that cannot be accessed with single-bit operations. The operating modes of the external interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 5 and 6 of the IOR register.

Figure 11. Interrupt Option Register



D7. D3-D0 These bits are not used.

LES. Level/Edge Selection Bit. When this bit is set to one, the interrupt #1 (Port A) is low level sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

ESB. Edge Selection Bit. When this bit is set to one, the interrupt #2 (Ports B & C) is positive edge sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

GEN. Global Enable Interrupt. When this bit is set to one, all the interrupts are enabled. When this bit is cleared to zero all the interrupts (excluding NMI) are disabled.

This register is cleared on reset.

Table 4. Interrupt Option Register Description

GEN	SET	Enable all interrupts
	CLEARED	Disable all interrupts
ESB	SET	Rising edge mode on interrupt input #2
	CLEARED	Falling edge mode on interrupt input #2
LES	SET	Level-sensitive mode on interrupt input #1
	CLEARED	Falling edge mode on interrupt input #1
OTHERS	NOT USED	

External Interrupts Operating Modes

The NMI interrupt is associated to the external interrupt pin of the ST6210B, ST6215B, ST6220B and ST6225B devices. This pin is falling edge sensitive and the interrupt pin signal is latched by a flip-flop which is automatically reset by the core at the beginning of the non-maskable interrupt service routine. A Schmitt trigger is present on NMI pin.

The two interrupt sources associated with the falling/rising edge mode of the external interrupt pins (Ports A-vector #1, Ports B and C-vector #2) are connected to two internal latches. Each latch is set when a falling/rising edge occurs during the processing of the first one, will be processed as soon as the first one has been finished (if there is not a higher priority interrupt request). If more than one interrupt occurs during the processing of the first one, these other interrupt requests will be lost.

The storage of the interrupt requests is not available in the level sensitive detection mode. To be taken into account, the low level must be present on the interrupt pin when the core samples the line after the execution of the instructions.

During the end of each instruction the core tests the interrupt lines and if there is an interrupt request the next instruction is not executed and the related interrupt routine is executed.

Note

On ST6210B,15B and ST6220B,25B the user can select the availability of an on-chip pull-up at NMI pin as ROM mask option (see option list at the end of the datasheet).

When GEN bit is low, the NMI interrupt is active but cannot cause a wake up from STOP/WAIT modes.

INTERRUPT (Continued)

Interrupt Procedure. The interrupt procedure is very similar to a call procedure, indeed the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event, the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

The following list summarizes the interrupt procedure:

ST62xx actions

- Interrupt detection
- The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (or the NMI flags)
- The value of the PC is stored in the first level of the stack
- The normal interrupt lines are inhibited (NMI still active)
- First internal latch is cleared
- The related interrupt vector is loaded in the PC.

User actions

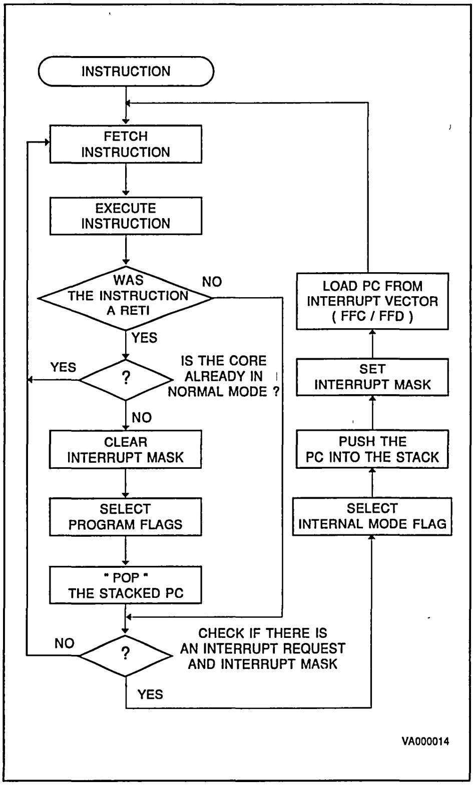
- User selected registers are saved inside the interrupt service routine (normally on a software stack)
- The source of the interrupt is found by polling (if more than one source is associated to the same vector) the interrupt flag of the source.
- Interrupt servicing
- Return from interrupt (RETI)

ST62xx actions

- Automatically the ST62xx core switches back to the normal flags (or the interrupt flags) and pops the previous PC value from the stack

The interrupt routine begins usually by the identification of the device that has generated the interrupt request (by polling). The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack. After the RETI instruction execution, the core carries out the previous actions and the main routine can continue.

Figure 12. Interrupt Processing Flow-Chart

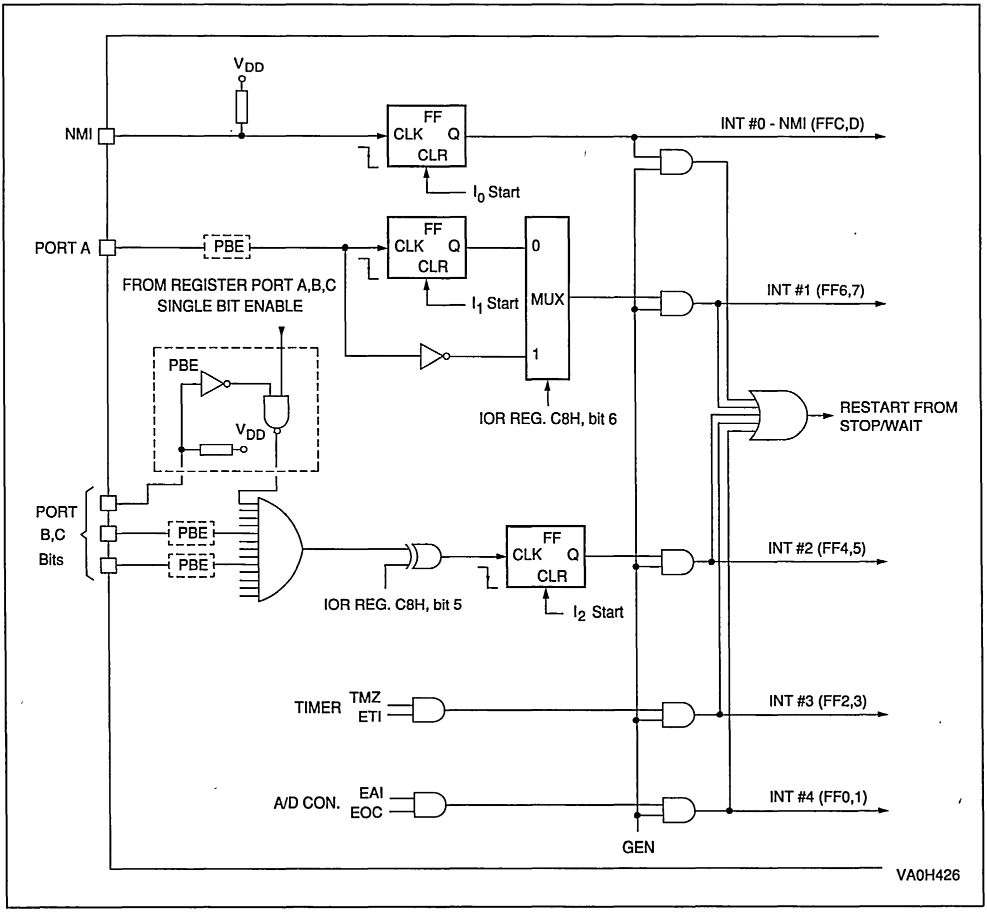

INSTRUCTION
FETCH INSTRUCTION
EXECUTE INSTRUCTION
WAS THE INSTRUCTION A RETI
NO
YES
LOAD PC FROM INTERRUPT VECTOR (FFC / FFD)
YES
?
IS THE CORE ALREADY IN NORMAL MODE ?
SET INTERRUPT MASK
NO
CLEAR INTERRUPT MASK
PUSH THE PC INTO THE STACK
SELECT PROGRAM FLAGS
SELECT INTERNAL MODE FLAG
" POP " THE STACKED PC
NO
?
CHECK IF THERE IS AN INTERRUPT REQUEST AND INTERRUPT MASK
YES
VA000014

INTERRUPT (Continued)

Table 5. Interrupt Requests and Mask Bits

Peripheral	Register	Address Register	Mask bit	Masked Interrupt Source	Interrupt vector
GENERAL	IOR	C8h	GEN	All Interrupts, excluding NMI	
TIMER	TSCR	D4h	ETI	TMZ: TIMER Overflow	Vector 3
A/D Converter	ADCR	D1h	EAI	EOC: End of Conversion	Vector 4
Port PAn	ORPA-DRPA	C4h-CCh	ORPAn-DRPAn	PAn pin	Vector 1
Port PBn	ORPB-DRPB	C5h-CDh	ORPBn-DRPBn	PBn pin	Vector 2
Port PCn	ORPC-DRPC	C6h-CEh	ORPCn-DRPCn	PCn pin	Vector 2

Figure 13. Interrupt Circuit Diagram



RESET

The ST6210B, 15B, 20B, 25B can be reset in three ways: by the external reset input (RESET) tied low, by power-on reset and by the digital Watchdog peripheral.

RESET Input

The $\overline{\text{RESET}}$ pin can be connected to a device of the application board in order to restart the MCU during its operation. The activation of the$\overline{\text{RESET}}$ pin may occur in the RUN, WAIT or STOP mode. This input has to be used to reset the MCU internal state and provide a correct start-up procedure. The pin is active low and has a Schmitt trigger input. The internal reset signal is generated by adding a delay to the external signal. Therefore even short pulses at the $\overline{\text{RESET}}$ are accepted, provided V_{DD} has finished its rising phase and the oscillator is running correctly (normal RUN or WAIT modes). The MCU is kept in the Reset state as long as the $\overline{\text{RESET}}$ pin is held low.

If the $\overline{\text{RESET}}$ activation occurs in the RUN or WAIT mode, the processing of the program is stopped (in RUN mode only), the Input/Outputs are placed in input with pull-up resistors, the Low Frequency Auxiliary Oscillator (LFAO) is stopped and the main Oscillator is restarted. When the level on the RESET pin becomes high, the initialization sequence is executed just after the internal delay.

If a $\overline{\text{RESET}}$ pin activation occurs in the STOP mode, the oscillator starts and all the inputs/outputs are configured in input with pull-up resistors. When the level of the $\overline{\text{RESET}}$ pin becomes high, the initialization sequence is started just after the internal delay.

Power-on Reset

The function of the POR consists in waking up the MCU during the power-on sequence. At the beginning of this sequence, the MCU is configured in the Reset state: every Input/Output port is configured in input with pull-up resistor and no instruction is executed. When the power supply voltage becomes sufficient, the oscillator starts to operate, nevertheless an internal delay is generated to allow the oscillator to be completely stabilized before the execution of the first instruction. The initialization sequence is executed just after the internal delay.

The internal delay is generated by an on-chip counter. The internal reset is released 2048 cycles of the internal frequency after the external reset is released.

Note:

When the OSG is enabled, the first pulses to the on-chip counter generating the internal delay are coming from the Low Frequency Auxilliary Oscillator (LFAO), until the Main Oscillator starts running.

To have a correct start-up, the user should take care that the internal reset is not released before the V_{DD} level is sufficient to allow MCU operation at the chosen frequency (see Recommended Operating Conditions).

A proper reset signal for slow rising V_{DD} can be generally provided by an external RC network connected at pin $\overline{\text{RESET}}$.

RESET (Continued)

Watchdog Reset

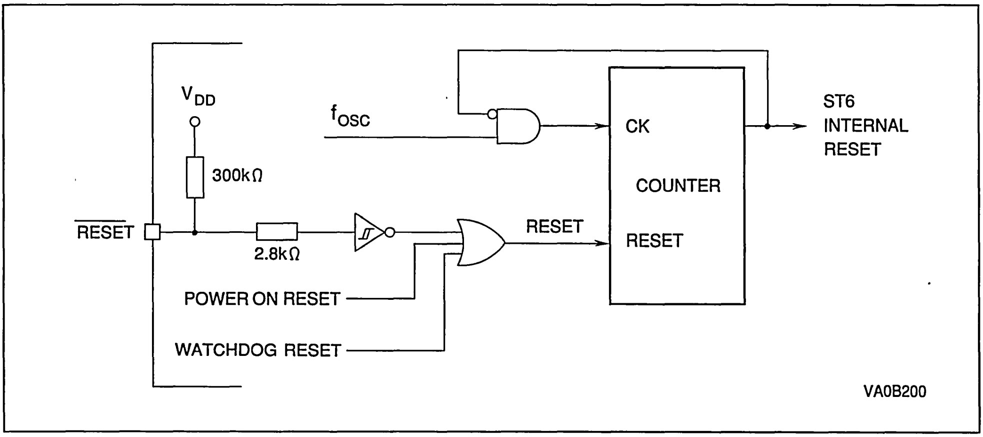
The ST621xB, 2xB provide an on-chip watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed, preventing the end-of-count being reached, the internal reset is activated. This, in particular, resets the watchdog. The MCU restarts as with normal reset from $\overline{\text{RESET}}$ pin including the internal delay.

Application Notes

An external resistor between V_{DD} and reset pin is not required because an internal pull-up device is provided.

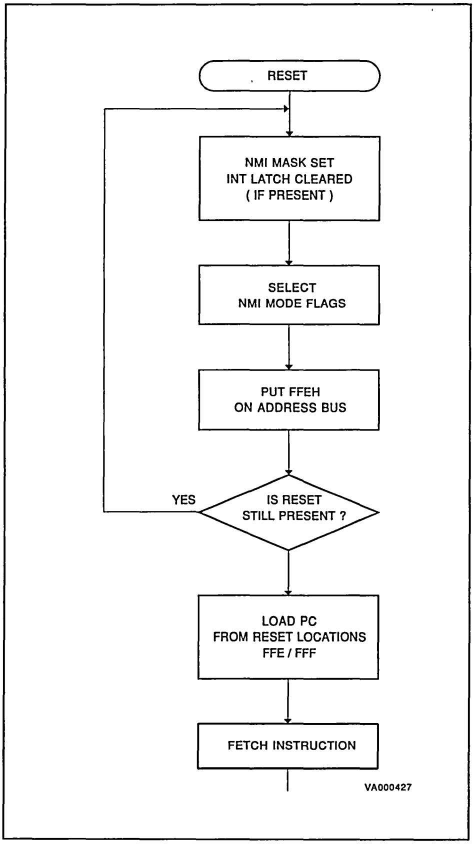
The POR device operates in a dynamic manner in the way that it brings about the initialization of the MCU when it detects a dynamic rising edge of the V_{DD} voltage. The typical detected threshold is about 2 volts, but the actual value of the detected threshold depends on the way in which the V_{DD} voltage rises up. The POR device *DOES NOT* allow the supervision of a static or slowly rising or falling edge of the V_{DD} voltage.

Figure 14. Reset Circuit



RESET (Continued)

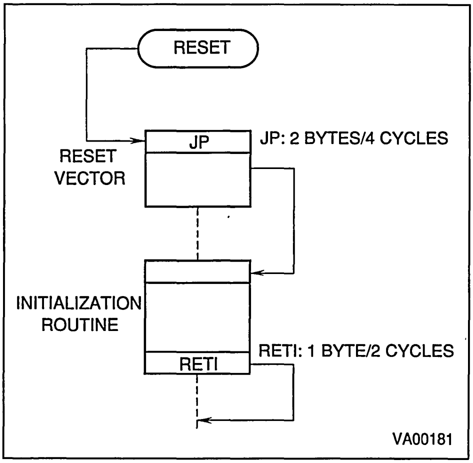
Figure 15. Reset and Interrupt Processing Flow-Chart



MCU Initialization Sequence

When a reset occurs the stack is reset to the program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEh & FFFh). A jump instruction to the beginning of the program has to be written into these locations. After a reset a NMI is automatically activated so that the core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine the ST62xx will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced.

Figure 16. Restart Initialization Program Flow-Chart



RESET (Continued)

Table 6. Reset Value

Register	Address	Value	Comment
Port Data Registers	0C0h to 0C2h	00h	
Port Direction Register	0C4h to 0C6h		I/O are Input with pull-up
Port Option Register	0CCh to 0CEh		I/O are Input with pull-up
Interrupt Option Register	0C8h		Interrupt disabled
Timer Status/Control	0D4h		Timer disabled
X, Y, V, W, Register	080h to 083h	Undefined	As written if programmed
Accumulator	0FFh		
Data RAM	084h to 0BFh		
Data ROM Window Register	0C9h		
A/D Result Register	0D0h		
Timer Counter Register	0D3h	FFh	Max count loaded
Timer Prescaler Register	0D2h	7Fh	
Watchdog Counter Register	0D8h	FEh	
A/D Control Register	0D1h	40h	A/D in Standby, main oscillator ON

WAIT & STOP MODES

The WAIT and STOP modes have been implemented in the ST62xx core in order to reduce the consumption of the product when the latter has no instruction to execute. These two modes are described in the following paragraphs.

In addition, the Low Frequency Auxiliary Oscillator (LFAO) can be used instead of the main oscillator to reduce power consumption in RUN and WAIT mode.

WAIT Mode

The MCU goes into the WAIT mode as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a “software frozen” state where the core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, but where the peripherals are still working.

The WAIT mode can be used when the user wants to reduce the consumption of the MCU when it is idle, while not losing count of time or monitoring of external events. The active oscillator (main oscillator or LFAO) is not stopped in order to provide a clock signal to the peripherals. The Timer counting may be enabled as well as the Timer interrupt before entering the WAIT mode; this allows the WAIT mode to be left when Timer interrupt occurs. The above explanation related to the timers applies also to the A/D converter.

If the power consumption has to be further reduced, the Low Frequency Auxiliary Oscillator (LFAO) can be used (provided the main oscillator has a frequency higher than the LFAO). It must be switched on before entering the WAIT mode.

If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU enters a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behavior depends on the state of the ST62xx core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case is described in the following paragraphs. In any case, the ST62xx core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

If the Watchdog is disabled the STOP mode is available. When in STOP mode the MCU is placed in the lowest power consumption mode. In this operating mode the microcontroller can be considered as being “frozen”, no instruction is executed, the oscillator is stopped, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, and the ST62xx core waits for the occurrence of an external interrupt request or Reset activation to output from the STOP state.

If the exit from the STOP mode is performed with a general RESET (by the activation of the external pin) the MCU will enter a normal reset procedure as described in the RESET chapter. The case of an interrupt depends on the state of the ST62xx core before the initialization of the STOP sequence and also of the kind of the interrupt request that is generated.

WAIT & STOP MODES (Continued)

This case will be described in the following paragraphs. In any case, the ST62xx core generates a delay after the occurrence of the interrupt request in order to wait for the complete stabilization of the oscillator before the execution of the first instruction.

Exit from WAIT and STOP Modes

The following paragraphs describe the output procedure of the ST62xx core from WAIT and STOP modes when an interrupt occurs (not a RESET). It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) before the start of the WAIT or STOP sequence, but also of the type of the interrupt request that is generated.

In any case, interrupts do not affect the oscillator selection. When the LFAO is used, the user program must handle oscillator selection as soon as the RUN mode resumes.

Normal Mode. If the ST62xx core was in the main routine when the WAIT or STOP instruction has been executed, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the STOP or the WAIT instruction is executed if no other interrupts are pending.

Not Maskable Interrupt Mode. If the STOP or WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs: the instruction that follows the STOP or the WAIT instruction is executed and the ST62xx core is still in the non-maskable interrupt mode even if another interrupt has been generated.

Normal Interrupt Mode. If the ST62xx core was in the interrupt mode before the initialization of the STOP or WAIT sequence, it outputs from the stop or wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non-maskable interrupt, the non-maskable routine is processed at first. Then the routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core remains in the normal interrupt mode.

Notes:

To reach the lowest power consumption during RUN or WAIT modes, the user software must take care of:

- configuring unused I/O as input without pull-up with well defined logic levels.
- placing the A/D converter in its power down mode by clearing the PDS bit in the A/D control register before entering the STOP instruction.
- stopping Timer external clock
- selecting the Low Frequency Auxiliary Oscillator (provided the main oscillator runs faster).

When the hardware activated watchdog is selected or the software watchdog enabled, the STOP instruction is deactivated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

If all the interrupt sources are disabled (including NMI if GEN is low), the restart of the MCU can only be done by a Reset activation. The WAIT and STOP instructions are not executed if an enabled interrupt request is pending.

ON-CHIP CLOCK OSCILLATOR

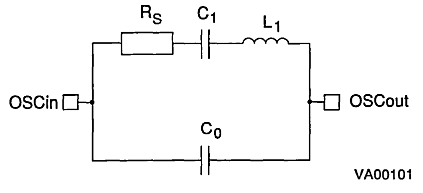
The ST6210B,15B, 20B, 25B provide a Main Oscillator which can be used with an external clock, with crystal or ceramic resonator, with a RC network. In addition, a Low Frequency Auxiliary Oscillator can be switched on for safety reason, to reduce power consumption or to have a fully integrated clock circuitry.

The internal frequency is divided by 12 to produce the Timer, the A/D converter and the Watchdog clock.

With a 8MHz external frequency, the fastest machine cycle is therefore 1.625µs.

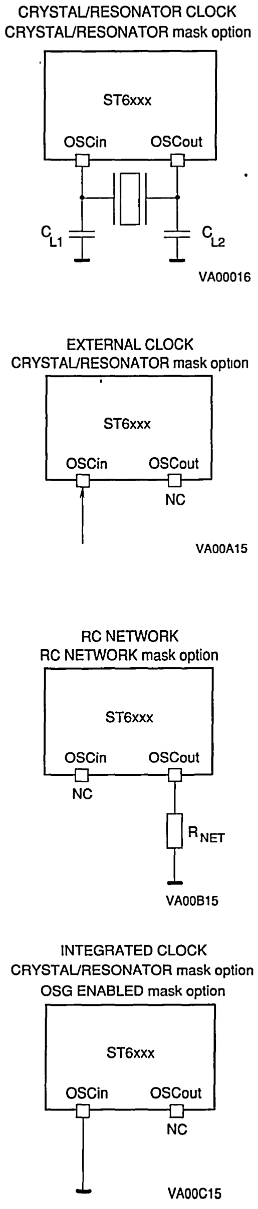
The machine cycle is the smallest unit needed to execute any operation (i.e. increment the program counter). An instruction may need two, four, or five machine cycles to be executed.

Figure 17. Crystal Parameters



Crystal Parameters: AT-cut Parallel Resonance Crystal
C0 = Parallel Resonance Capacitance

Figure 18. Oscillator Connection


CRYSTAL/RESONATOR CLOCK
CRYSTAL/RESONATOR mask option

EXTERNAL CLOCK
CRYSTAL/RESONATOR mask option

RC NETWORK
RC NETWORK mask option

INTEGRATED CLOCK
CRYSTAL/RESONATOR mask option
OSG ENABLED mask option

CL1 = CL2 = 12 to 22pF for a 4/8MHz crystal

ON-CHIP CLOCK OSCILLATOR (Continued)

Main Oscillator

The oscillator is configured through mask option. When the CRYSTAL/RESONATOR option is selected, it must be used with a quartz crystal, a ceramic resonator or an external signal provided on pin OSCin. When the RC NETWORK option is selected, the system clock is generated by a RC network.

The oscillator can be turned off when the OSG ENABLED mask option is selected by setting OSCOFF bit of the ADC Control Register. The Low Frequency Auxiliary Oscillator is automatically started.

Turning on the main oscillator is achieved by a software reset of bit OSCOFF of the A/D Converter Control Register or by resetting the MCU. Restarting the main oscillator takes the oscillator start up time plus possibly the duration of the software instruction at f_{LFAO} low frequency.

Low Frequency Auxiliary Oscillator (LFA0)

The Low Frequency Auxiliary Oscillator has three main purposes. First, it can be used to reduce power consumption in non timing critical routines. Second, it enables to generate a fully integrated system clock, without any external components. Last, it acts as safety oscillator in case of the main oscillator fails.

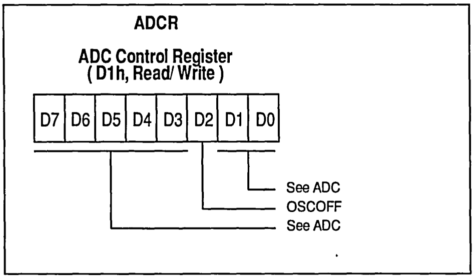
This oscillator is available when the OSG ENABLED mask option is selected. In this case, it automatically starts one of its periods after the first missing edge from the main oscillator, whatever the reason (main oscillator defective, no clock circuitry provided, main oscillator switched off ...).

User program, normally interrupts, WAIT and STOP instructions, is normally processed but at the reduced f_{LFAO} frequency. The A/D converter accuracy is decreased, as the internal frequency is below 1MHz.

At power on, the Low Frequency Auxiliary Oscillator starts faster than the Main Oscillator. It therefore feeds the on-chip counter generating the POR delay until the Main Oscillator runs.

The Low Frequency Auxiliary Oscillator is switched off as soon as the main oscillator starts.

Figure 19.OSCOFF Bit in ADC Control Register



OSCOFF. When low, this bit enables main oscillator to run. The main oscillator is switched off when OSCOFF is high.

Oscillator Safe Guard

The Oscillator Safe Guard (OSG) enables to drastically increase the safety of operation of ST62xx devices. It has three basic functions. It first filters spikes from the oscillator lines which would result in over frequency to the ST62 core. Second, it gives access to the Low Frequency Auxilliary Oscillator (LFAO), used to ensure minimum processing in case of failure of the main oscillator, to reduce power consumption or to provide a fixed frequency low cost oscillator. Last, it automatically limits the internal frequency to ensure correct operation in case the power supply drops.

The OSG is enabled or disabled through the OSG mask option. It can be seen as a filter whose cross over frequency is device dependent.

Spikes on the oscillator lines result in an increased internal frequency. Without the OSG, this may lead to an over frequency at the operating power supply. The OSG filters such spikes (see Figure 20). Anyway, enabling the OSG limits the maximum frequency to f_{OSG}.

When the OSG is enabled, it gives access to the Low Frequency Auxiliary Oscillator. This oscillator starts operating after the first missing edge of the main oscillator (see Figure 21).

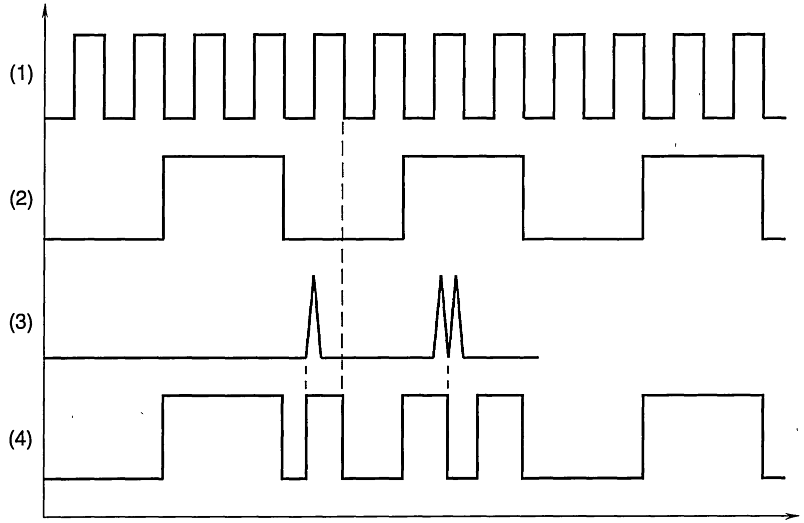
Over frequency at a given power supply is seen by the OSG as spikes. It therefore filters some periods in order that the internal frequency of the device is kept within both the range the particular device can stand (depending on Vdd) and below f_{OSG} , the maximum authorised frequency with OSG enabled.

Notes:

The OSG should be used wherever possible as it provides maximum safety. Care must be taken as it increases power consumption and reduces the maximum authorised frequency down to f_{OSG}.

ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 20. OSG Filtering Principle



(1) Maximum Frequency for the device to work correctly

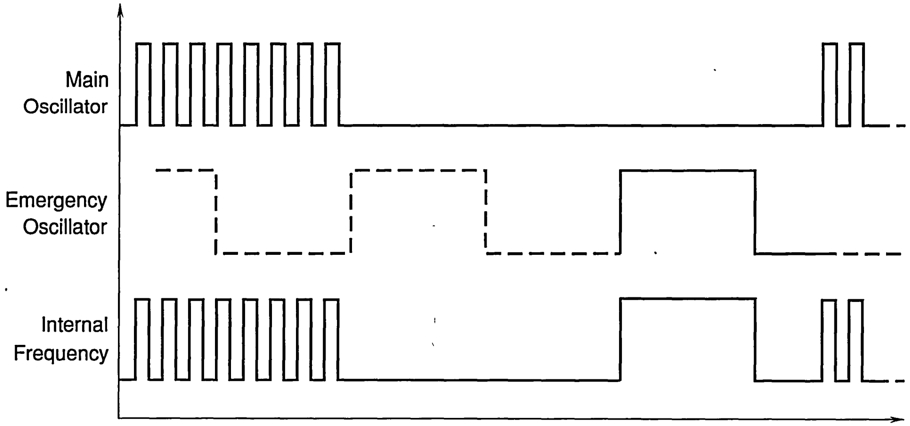
(2) Actual Quartz Crystal Frequency at OSCin pin

(3) Noise from OSCin

(4) Resulting Internal Frequency

VR001932

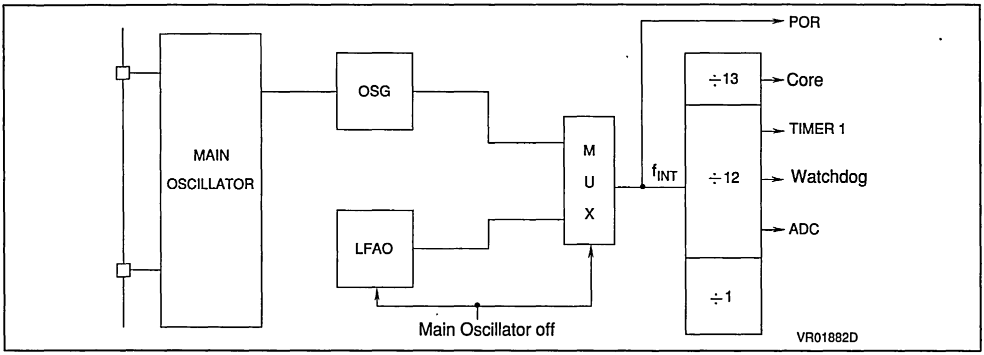
Figure 21. OSG Emergency Oscillator Principle



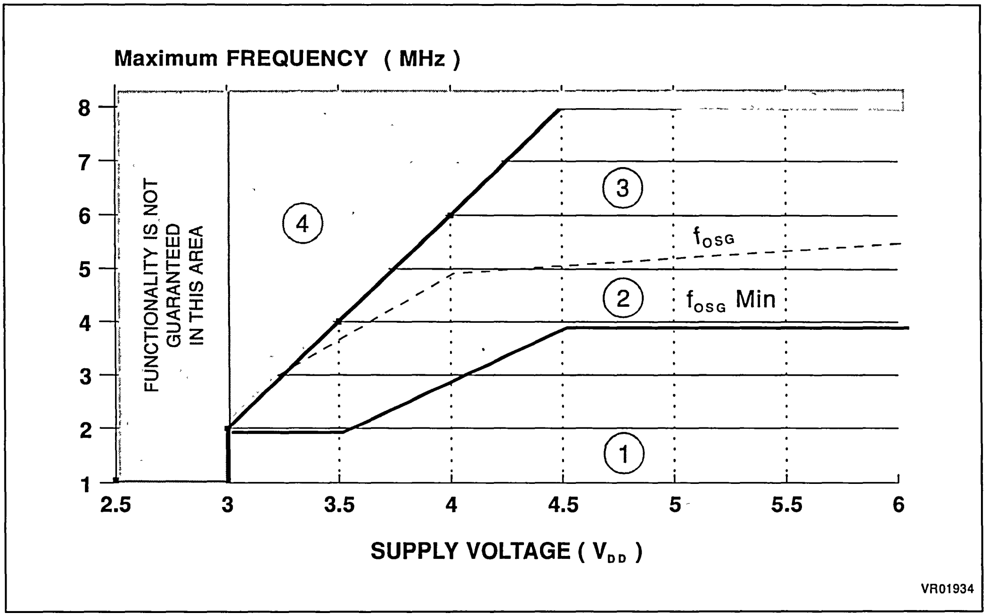
VR001933

ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 22. Clock Circuits Block Diagram



Maximum Operating Frequency (f_{MAX}) versus Supply Voltage (V_{DD})



① In this area, operation is guaranteed at the quartz crystal frequency.

② When the OSG is disabled, operation in this area is guaranteed at the quartz crystal frequency
When the OSG is enabled, operation in this area is guaranteed at a frequency of at leastf_{OSG} min.

③ When the OSG is disabled, operation in this area is guaranteed at the quartz crystal frequency
When the OSG is enabled, access to this area is prevented. The internal frequency is kept atf_{OSG}.

④ When the OSG is disabled, operation in this area is not guaranteed
When the OSG is enabled, access to this area is prevented. The internal frequency is kept atf_{OSG}.

INPUT/OUTPUT PORTS

The ST6210B, ST6215B, ST6220B and ST6225B microcontroller have respectively 12 and 20 Input/Output lines that can be individually programmed either in the input mode or the output mode with the following software selectable options:

- Input without pull-up and without interrupt
- Input with pull-up and with interrupt
- Input with pull-up without interrupt
- Analog inputs (PA4-PA7, PB0-PB7, PC4-PC3)
- Push-pull output
- Standard Open drain output
- 20mA Open drain output

The lines are organized in three Ports (Port A, B and C).

Each port occupies 3 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data, Direction and Option registers are associated with the PA0 line of Port A).

The three DATA registers (DRA, DRB, DRC), are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port data registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related option registers, to select the different input mode options.

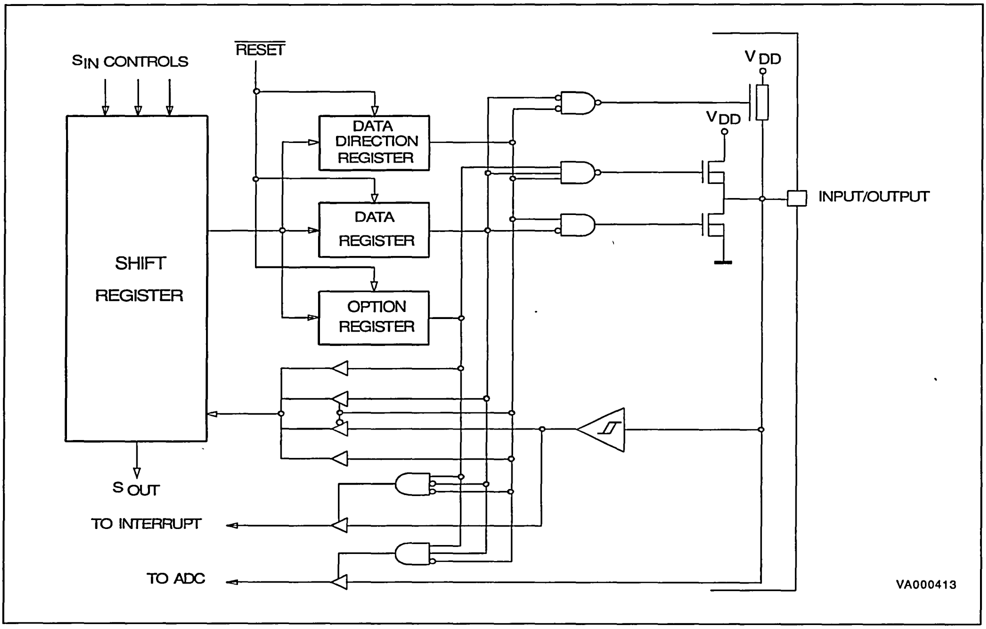
Single-bit operations on I/O registers are possible but care is necessary because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired change of the input configuration.

The three Data Direction registers (DDRA, DDRB and DDRC) allow the selection of the data direction of each pin (input or output).

The three Option registers (ORA, ORB and ORC) are used to select the different port options available both in input and in output mode.

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up/no-interrupt is selected on all the pins, thus avoiding pin conflicts.

Figure 23. I/O Port Block Diagram



INPUT/OUTPUT PORTS (Continued)

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations, except PB0 and PC7 when the External STOP Mode Control option is selected.

This is achieved by writing the relevant bit in the data (DR), data direction register (DDR) and option registers (OR). Table 7 shows all the port configurations that can be selected by user software.

Input Option Description

Pull-up, High Impedance Option. All the input lines can be individually programmed with or without an internal pull-up according to the codes programmed in the OR and DR registers . If the pull-up option is not selected, the input pin is in the high-impedance state.

Interrupt Option. All the input lines can be individually connected by software to the interrupt lines of the ST62xx core according to the codes programmed in the OR and DR registers. The pins of Port A are AND-connected to the interrupt associated to the vector #1. The pins of Port B & C are AND-connected to the interrupt associated to the vector #2. The interrupt modes (falling edge sensitive, rising edge sensitive, low level sensitive) can be selected by software for each port by programming the IOR register.

Analog Input Option. The sixteen PA4-PA7, PB0-PB7, PC4-PC7 pins can be configured to be analog inputs according to the codes programmed in the OR and DR registers. These analog inputs are connected to the on-chip 8-bit Analog to Digital Converter. *ONLY ONE* pin should be programmed as analog input at a time, otherwise the selected inputs will be shorted.

Figure 24. I/O Port Option Registers

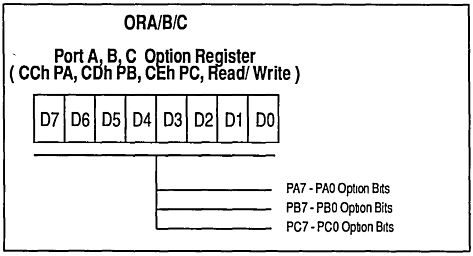


Figure 25. I/O Port Data Direction Registers

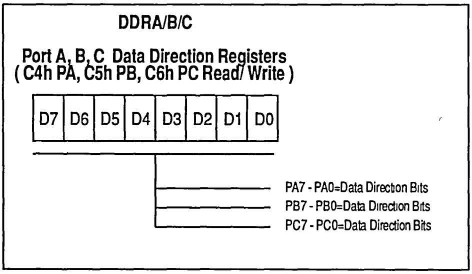
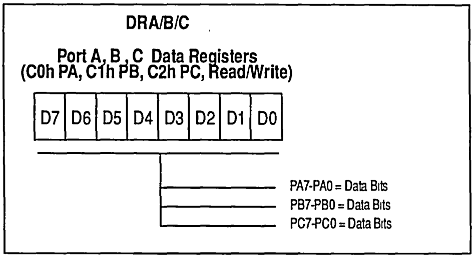

DDRA/B/C
Port A, B, C Data Direction Registers
(C4h PA, C5h PB, C6h PC Read/ Write)
D7
D6
D5
D4
D3
D2
D1
D0
PA7 - PA0=Data Direction Bits
PB7 - PB0=Data Direction Bits
PC7 - PC0=Data Direction Bits

Figure 26. I/O Port Data Registers



Note: For complete coding explanation refer to Table 7

Table 7. I/O Port Options Selection

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt (Reset state)
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up, with interrupt
0	1	1	Input	No pull-up, no interrupt (PA0-PA3 pins)
			Input	Analog input (PA4-PA7, PB0-PB7, PC4-PC7 pins)
1	0	X	Output	20mA sink open-drain output (PA0-PA3 pins)
1	0	X	Output	Standard open-drain output (PA4-PA7, PB0-PB7, PC4-PC7 pins)
1	1	X	Output	20mA sink push-pull output (PA0-PA3 pins)

Notes: X. Means don't care.

INPUT/OUTPUT PORTS (Continued)

Note:

Switching the I/O ports from one state to another should be done in a way that no unwanted side effects can happen. The recommended safe transitions are shown below. All other transitions are risky and should be avoided during change of operation mode as it is most likely that there will be an unwanted side-effect such as interrupt generation or two pins shorted together by the analog input lines.

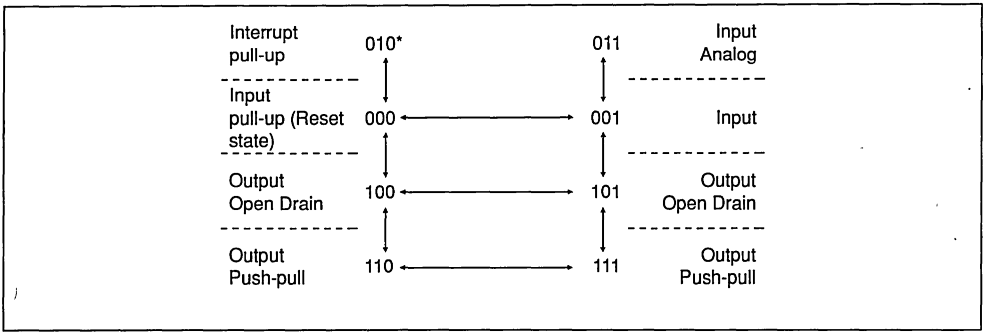
Single bit instructions (SET, RES, INC and DEC) should be used very carefully with Port A, B and C data registers because these instructions make an implicit read and write back of the whole addressed register byte. In port input mode however data register address reads from input pins, not from data register latches and data register information in input mode is used to set characteristics of the input pin (interrupt, pull-up, analog input), therefore these characteristics may be unintentionally reprogrammed depending on the state of input pins. As general rule is better to use single bit instructions on data register only when the whole port is in output mode. If input or mixed configuration is needed it is recommended to keep a copy of the data register in RAM. On this copy it is possible to use single bit instructions, then the copy register could be written into the port data register.

```
SET     bit, datacopy
LD      a, datacopy
LD      DRA, a
```

The WAIT and STOP instructions allow the ST62xx to be used in situations where low power consumption is needed. The lowest power consumption is achieved by configuring I/Os in input mode with well-defined logic levels.

The user has to take care not to switch outputs with heavy loads during the conversion of one of the analog inputs in order to avoid any disturbance in the measurement.

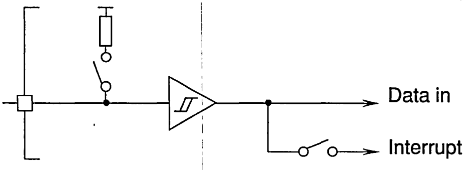
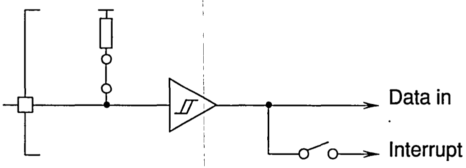
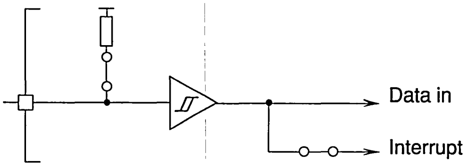
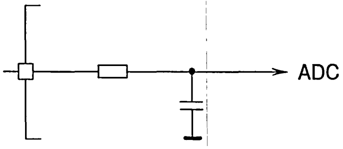
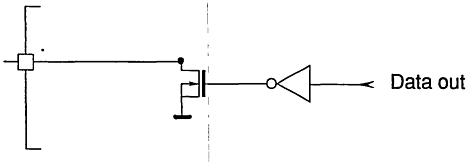
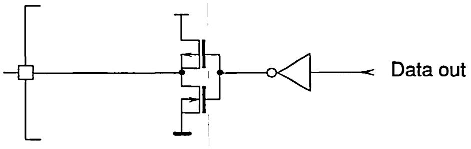
State Transition Diagram for Safe Transitions



Note *. xxx = DDR, OR, DR Bits respectively

INPUT/OUTPUT PORTS (Continued)

Table 8. I/O Port Options Selection

Mode	Available At[1]	Schematic
Input	PA0-PA7 PB0-PB7 PC4-PC7 TIMER	
Input with pull up	PA0-PA7 PB0-PB7 PC4-PC7 TIMER	
Input with pull up with interrupt	PA0-PA7 PB0-PB7 PC4-PC7	
Analog Input	PA4-PA7 PC4-PC7 PB0-PB7	
Open drain output 5mA Open drain output 20mA	PA4-PA7 PB0-PB7 PC4-PC7 PA0-PA3	
Push-pull output 5mA Push-pull output 20mA	PA4-PA7 PB0-PB7 PC4-PC7 PA0-PA3	

Note 1. Provided proper configuration.

TIMER

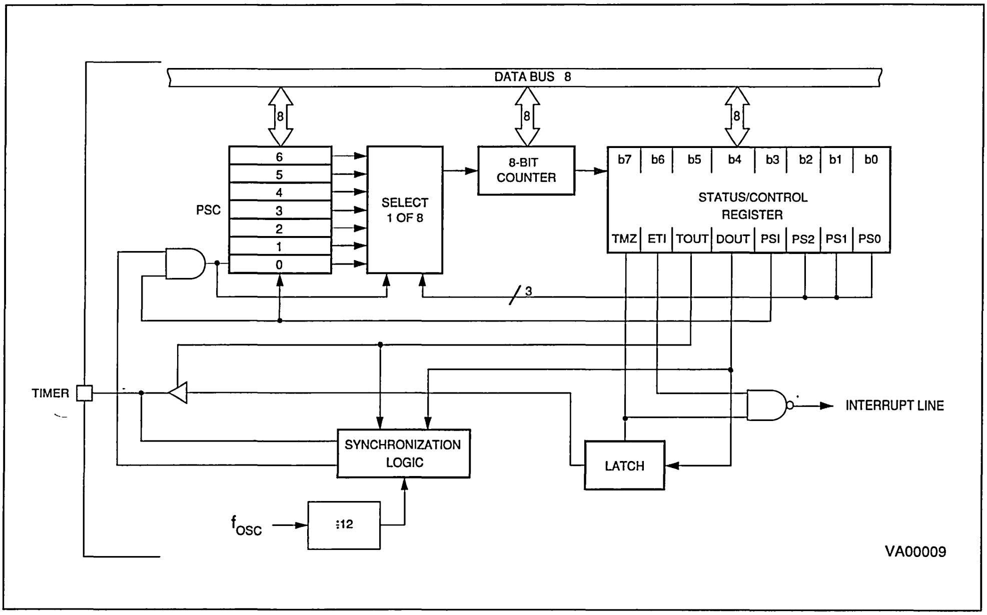
The ST6210B, ST6215B, ST6220B and ST6225B offer one on-chip Timer peripheral consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and control logic that allows configuring the peripheral in three operating modes.

Figure 27 shows the Timer block diagram. This timer has the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as a RAM location at address D3h. The state of the 7-bit prescaler can be read in the PSC register at address D2h. The control logic device is managed in the TSCR register (D4h address) as described in the following paragraphs.

The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (Timer Zero)bit in the TSCR is set to one. If the ETI (Enable Timer Interrupt) bit in the TSCR is also set to one an interrupt request, associated to interrupt vector #3, is generated. The Timer interrupt can be used to exit the MCU from the WAIT mode.

The prescaler input can be the internal frequency divided by 12 or an external clock at TIMER pin. The prescaler decrements on the rising edge. Depending on the division factor programmed by PS2, PS1 and PS0 bits in the TSCR (see table 10), the clock input of the timer/counter register is multiplexed to different sources. On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR. This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC is connected to clock input of TCR, and so on. The prescaler initialize bit PSI in the TSCR register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting. The prescaler can be given any value between 0 and 7Fh by writing to address D2h, if bit PSI in the TSCR register is set to one. The tap of the prescaler is selected using the PS2/PS1/PS0 bits in the control register.
Figure 28 shows the Timer working principle.

Figure 27. Timer Block Diagram



TIMER (Continued)

Timer Operating Modes

There are three operating modes of the Timer peripheral. They are selected by the bits TOUT and DOUT (see TSCR register). These three modes correspond to the two clock frequencies that can be connected on the 7-bit prescaler (f_{INT}÷12 or TIMER pin signal) and to the output mode.

Gated Mode (TOUT = "0", DOUT = "1"). In this mode the prescaler is decremented by the Timer clock input (f_{INT} divided by 12) but ONLY when the signal at TIMER pin is held high (giving a pulse width measurement potential). This mode is selected by the TOUT bit in TSCR register cleared to "0" (i.e. as input) and DOUT bit set to "1".

Clock Input Mode (TOUT = "0", DOUT = "0"). In this mode the TIMER pin is an input and the prescaler is decremented on rising edge. The maximum input frequency that can be applied to the external pin in this mode is 1/4 of the internal frequency when the processor is running but can be higher when the WAIT mode is entered.

Output Mode (TOUT = "1", DOUT = data out). The TIMER pin is connected to the DOUT latch. Therefore the timer prescaler is clocked by the prescaler clock input (f_{INT}÷12).

The user can select the desired prescaler division ratio through the PS2, PS1, PS0 bits. When TCR count reaches 0, it sets the TMZ bit in the TSCR. The TMZ bit can be tested under program control to perform a timer function whenever it goes high. The low-to-high TMZ bit transition is used to latch the DOUT bit of the TSCR and pass it to TIMER pin. This operating mode allows external signal generation on the TIMER pin.

Table 9. Timer Operating Modes

TOUT	DOUT	Timer Pin	Timer Function
0	0	Input	Event Counter
0	1	Input	Input Gated
1	0	Output	Output "0"
1	1	Output	Output "1"

Timer Interrupt

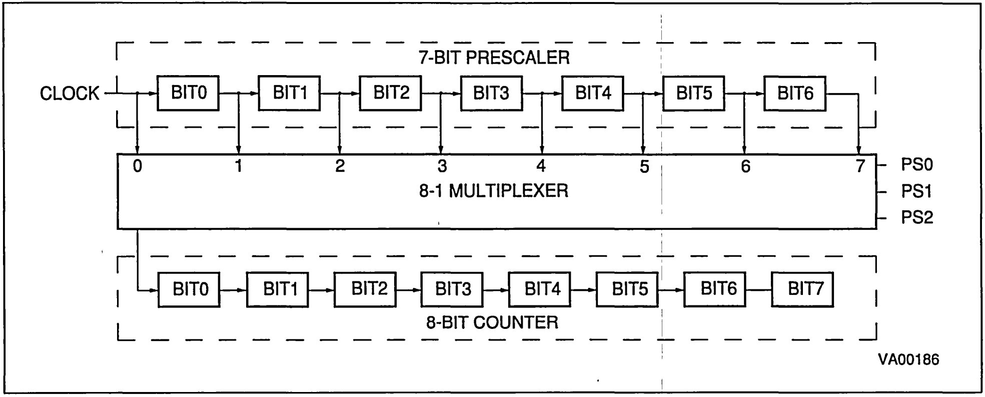
When the counter register decrements to zero and the software controlled ETI (Enable Timer Interrupt) bit is set to one then an interrupt request associated to interrupt vector #3 is generated. When the counter decrements to zero also the TMZ bit in the TSCR register is set to one.

Notes:

On ST6210B,15B, ST6220B, 25B the user can select the availability of an on-chip pull-up at TIMER pin as ROM mask option (see option list at the end of the datasheet).

TMZ is set when the counter reaches 00h ; however, it may be set by writing 00h in the TCR register or setting bit 7 of the TSCR register. TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFh while the 7-bit prescaler is loaded to 7Fh , and the TSCR register is cleared which means that Timer is stopped (PSI="0") and the timer interrupt is disabled.

Figure 28. Timer Working Principle



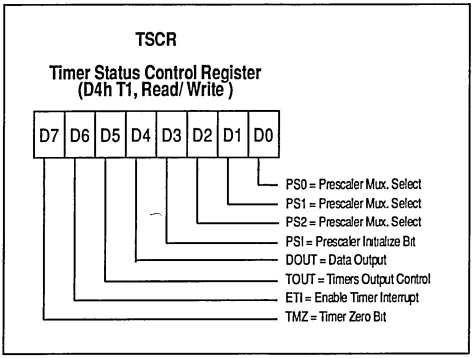
TIMER (Continued)

If the Timer is programmed in output mode, DOUT bit is transferred to the TIMER pin when TMZ is set to one (by software or due to counter decrement). When TMZ is high, the latch is transparent and DOUT is copied to the timer pin. When TMZ goes low, DOUT is latched.

A write to the TCR register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00h again. The values of the TCR and the PSC registers can be read accurately at any time.

Timer Registers

Figure 29. Timer Status Control Register


TSCR
Timer Status Control Register
(D4h T1, Read/ Write)
D7
D6
D5
D4
D3
D2
D1
D0
PS0 = Prescaler Mux. Select
PS1 = Prescaler Mux. Select
PS2 = Prescaler Mux. Select
PSI = Prescaler Initialize Bit
DOUT = Data Output
TOUT = Timers Output Control
ETI = Enable Timer Interrupt
TMZ = Timer Zero Bit

TMZ. Low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before starting with a new count.

ETI. This bit, when set, enables the timer interrupt request (vector #3). If ETI=0 the timer interrupt is disabled. If ETI=1 and TMZ=1 an interrupt request is generated.

TOUT. When low, this bit selects the input mode for the TIMER pin. When high the output mode is selected.

DOUT. Data sent to the timer output when TMZ is set high (output mode only). Input mode selection (input mode only).

PSI. Used to initialize the prescaler and inhibit its counting. When PSI="0" the prescaler is set to 7Fh and the counter is inhibited. When PSI="1" the prescaler is enabled to count downwards. As long as PSI="0" both counter and prescaler are not running.

Table 10. Prescaler Division Factors

PS2	PS1	PS0	Divided by
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Figure 31. Timer Counter Register

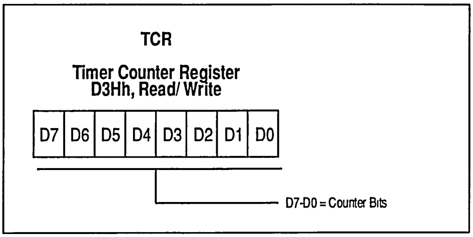
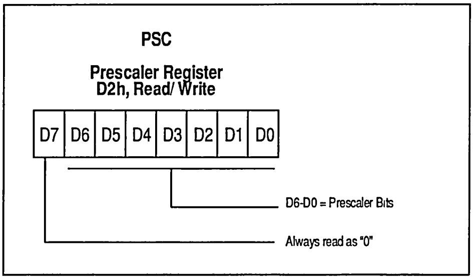


Figure 30. Prescaler Register



PS2, PS1, PS0. These bits select the division ratio of the prescaler register.

DIGITAL WATCHDOG

The digital Watchdog of the ST6210B/15B device consists of a down counter that can be used to provide a controlled recovery from a software upset.

The Watchdog generates a system reset when the counter passes 00h. User software can prevent the reset by reloading the counter. User software should therefore be written in such a way that the counter is regularly reloaded as long as the software runs correctly. In the case of software upset (e.g. infinite loop or power supply fail), user software should not reload the counter so it will pass 00h and reset the MCU.

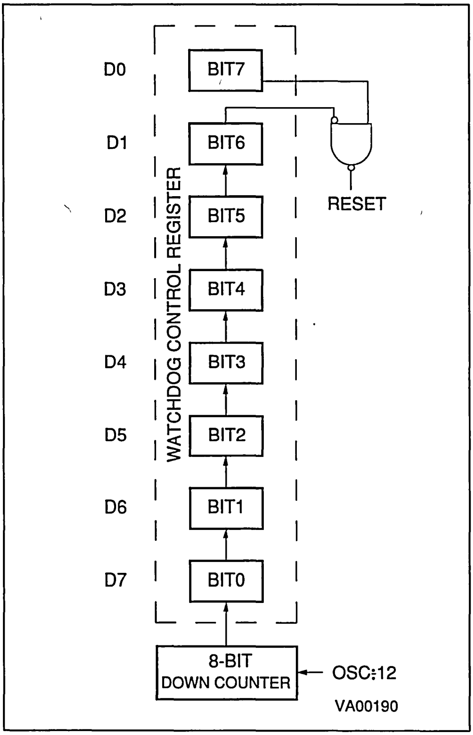
The Watchdog activation (hardware or software) is user selectable by mask option. If the hardware option is selected the Watchdog is automatically initialized after reset so that this function does not need to be activated by the user program.

The Watchdog uses one data space register (DWDR location D8h). The Watchdog register is set to FEh on reset and counts down when activated. The Watchdog time can be adjusted through the value reloaded into the DWDR register. Only the 6 MSbits are significant. This gives the possibility to generate a reset in a time between 3072 to 196608 clock cycles in 64 possible steps (with a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded before bits 2-7 decrement from all zeros to all ones.

The WATCHDOG ACTIVATION can be software (it is launched by software) or hardware (it automatically starts counting down after reset). When the software activation is selected, the watchdog can be launched by setting to 1 bit 0 of the Digital Watchdog Register after bit SR of this register has been set to 1. Once activated, the watchdog cannot be stopped by software: a full external reset is mandatory.

The STOP instruction is inhibited as soon as the watchdog is active. A WAIT instruction is processed instead and the watchdog continues to countdown. The NMI pin allows, in addition to the interrupt generation, to control the execution of the STOP instruction. It is inhibited when NMI is low (a WAIT instruction is processed instead). When NMI is high, a STOP instruction freezes the watchdog counter before entering the STOP mode. When the micro exits from the STOP mode (for example, when an NMI interrupt is generated), the watchdog resumes activity.

Figure 32. Watchdog Working Principle



Note:

When the software activation is selected and the watchdog is not activated, the 7 MSbits of the counter can be used to perform timer functions. Care must be taken as the Watchdog bits are in reverse order.

Bit 1 of the Watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero.

C. This is the Watchdog activation bit. If hardware option is selected, it is forced high and the user cannot change it (the Watchdog is always active). When the software option is selected, the Watchdog function is activated by setting C to 1. It can then be cleared only by a system reset and is not affected by the STOP Mode Control option. When C is kept low the counter can be used as a 7-bit timer.

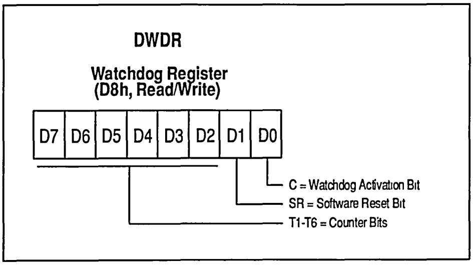
DIGITAL WATCHDOG (Continued)

When cleared to zero it allows the use of the counter as a 7-bit timer. This bit is cleared on reset.

SR. This bit is set to one during the reset and will generate a software reset if cleared to zero. When C = "0" (watchdog disabled) it is the MSB of the 7-bit timer.

T1-T6. These are the watchdog counter bits. It must be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter.

Figure 33. Digital Watchdog Register



Application Notes

The hardware activation option is very useful when the external circuitry may inject noises on the reset pin, where there is an unstable supply voltage, or RF influence or other similar phenomena. If the Watchdog software activation is selected and the Watchdog is not used during power-on reset external noise may cause the undesired activation of the Watchdog with a generation of an unexpected reset. To avoid this risk, two additional instructions, that check the state of the watchdog and eventually reset the chip are neededwithin the first 27 instructions, after the reset. These instructions are:

```
jrx 0, WD, #+3
ldi WD, 0FDH
```

These instructions should be executed at the very beginning of the customer program.

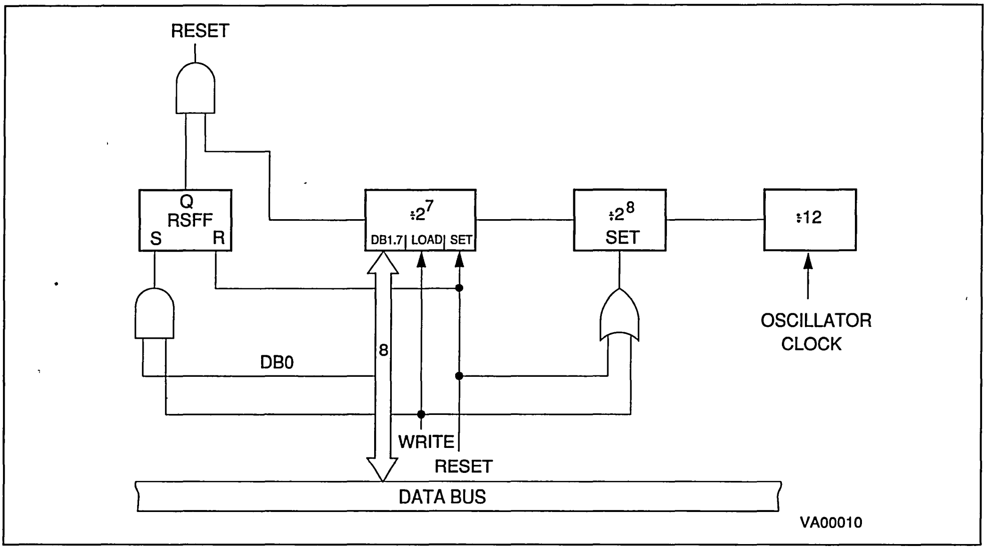
If the Watchdog is used (both hardware or software activated), during power-on reset the Watchdog register may be set to a low value, that could give a reset after 28 instructions earliest. To avoid undesired resets, the Watchdog must be set to the desired value within the first 27 instructions, the best is to put at the very beginning.

Alternatively the normal legal state can be checked with the following short routine:

```
ldi a, 0FEH
and a, WD
cpi a, 0FEH
jrz #+3
ldi WD, 0FDH
```

This sequence is recommended for security applications, where possible stack confusion error loops must be avoided and the Watchdog must only be refreshed after extensive checks.

Figure 34. Digital Watchdog Block Diagram



8-BIT A/D CONVERTER

The A/D converter of ST621xB,2xB devices is an 8-bit analog to digital converter with up to 8 (PB0-PB7 on ST6210B, ST6220B) and up to 16 (PA4-PA7, PB0-PB7, PC4-PC7 on ST6215B, ST6225B) analog inputs (as alternate functions of I/O lines) offering 8-bit resolution with a typical conversion time of 70ms (clock frequency of 8MHz).

The A/D peripheral converts the input voltage by a process of successive approximations using a clock frequency derived from the oscillator with a division factor of twelve. With an oscillator clock frequency less than 1.2MHz, the A/D converter accuracy is decreased.

The selection of the pin signal that has to be converted is done by configuring the related I/O line as analog input through the I/O ports option and data registers (refer to I/O ports description for additional information). Only one I/O line must be configured as analog input at a time. The user must avoid the situation in which more than one I/O pin is selected to be analog input to avoid malfunction of the ST62xx.

The ADC uses two registers in the data space: the ADC data conversion register which stores the conversion result and the ADC control register used to program the ADC functions.

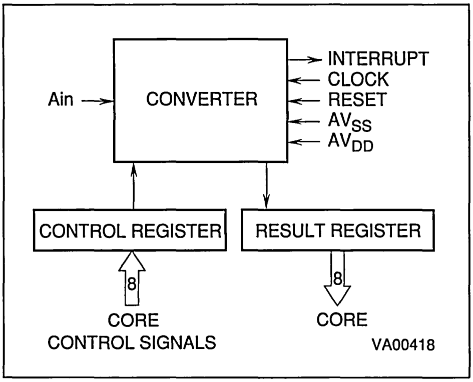
A conversion is started by writing a "1" to the Start bit (STA) in the ADC control register. This automatically clears (resets to "0") the End Of Conversion Bit (EOC). When a conversion has been finished this EOC bit is automatically set to "1" in order to flag that conversion is complete and that the data in the ADC data conversion register is valid. Each conversion has to be separately initiated by writing to the STA bit.

The STA bit is continually being scanned so that if the user sets it to "1" while a previous conversion is in progress then a new conversion is started before the previous one has been completed.The start bit (STA) is a write only bit, any attempt to read it will show a logical "0".

The A/D converter has a maskable interrupt associated to the end of conversion. This interrupt is associated to the interrupt vector #4 and occurs when the EOC bit is set, i.e. when a conversion is completed. The interrupt is masked using the EAI (interrupt mask) bit in the control register.

The power consumption of the device can be reduced by turning off the ADC peripheral. That is achieved when the PDS bit in the ADC control register is cleared to "0". If PDS="1", the A/D is supplied and enabled for conversion. This bit must be set at least one instruction before the beginning of the conversion to allow the stabilization of the A/D converter. This action is needed also before entering the WAIT instruction as the A/D comparator is not automatically disabled by the WAIT mode

Figure 35. A/D Converter Block Diagram



During reset any conversion in progress is stopped, the control register is reset to 40h and the A/D interrupt is masked (EAI=0).

Notes:

The ST62xx A/D converter does not feature a sample and hold. The analog voltage to be measured should therefore be stable during the conversion time. Variation should not exceed±1/2 LSB for the best accuracy in measurement. A low pass filter can be used at the analog input pins to reduce input voltage variation during the conversion.

When selected as an analog channel, the input pin is internally connected to a capacitor Cad of typically 12pF. For maximum accuracy, this capacitor must be fully loaded at conversion start. In the worst case, conversion starts one instruction (6.5 µs) after the channel has been selected. In the worst case conditions, the impedance ASI of the analog voltage source is calculated using the following formula :

$$6.5\mu s = 9 \times Cad \times ASI$$

(capacitor loaded over 99.9%), ie 30 kΩ including 50% guardland. ASI can be higher if Cad has been loaded for a longer time by adding instructions before conversion start (adding more than 26 CPU cycles is meaningless).

Since the ADC is on the same chip as the microprocessor the user should not switch heavily loaded output signals during conversion if high precision is needed. This is because such switching will affect the supply voltages which are used for comparisons.

8-BIT A/D CONVERTER (Continued)

The accuracy of the conversion depends on the quality of the power supply voltages (V_{DD} and V_{SS}). The user must specially take care of applying regulated reference voltage on the V_{DD} and V_{SS} pins (the variation of the power supply voltage must be inferior to 5V/ms). This implies in particular that a suitable decoupling capacitor is used at V_{DD}.

The converter can resolve the input voltage with a resolution of:

$$\frac{V_{DD} - V_{SS}}{256}$$

The Input voltage (Ain) which has to be converted must be constant for 1µs before conversion and remain constant during the conversion.

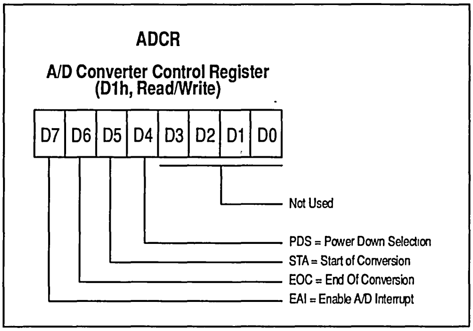
The resolution of the conversion can be improved if the power supply voltage (V_{DD}) of the microcontroller becomes lower.

In order to optimize the resolution of the conversion, the user can configure the microcontroller in the WAIT mode because this mode allows the minimization of the noise disturbances and the variations of the power supply voltages due to the switching of the outputs. Nevertheless, it must be take care of executing the WAIT instruction as soon as possible after the beginning of the conversion because the execution of the WAIT instruction may provide a small variation of the V_{DD} voltage (the negative effect of this variation is minimized at the beginning of the conversion because the latter is less sensitive than the end of the conversion when the less significant bits are determined).

The best configuration from a accuracy point of view is the WAIT mode with the Timer stopped. Indeed, only the ADC peripheral and the oscillator are still working. The MCU has to be wake-up from the WAIT mode by the interrupt of the ADC peripheral at the end of the conversion. It must be noticed that the wake-up of the microcontroller could be done also with the interrupt of the TIMER, but in this case, the Timer is working and some noise could disturb the converter in terms of accuracy.

EAI. If this bit is set to one the A/D interrupt (vector #4) is enabled, when EAI=0 the interrupt is disabled.

Figure 36. A/D Converter Control Register


ADCR
A/D Converter Control Register
(D1h, Read/Write)
D7
D6
D5
D4
D3
D2
D1
D0
Not Used
PDS = Power Down Selection
STA = Start of Conversion
EOC = End Of Conversion
EAI = Enable A/D Interrupt

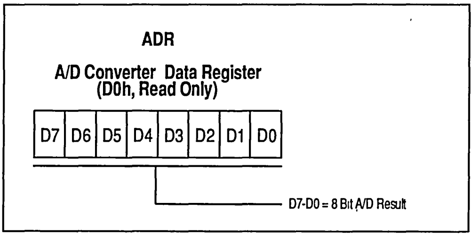
EOC. *Read Only*;This read only bit indicates when a conversion has been completed. This bit is automatically reset to zero when the STA bit is written. If the user is using the interrupt option then this bit can be used as an interrupt pending bit. Data in the data conversion register are valid only when this bit is set to one.

STA. *Write Only*; Writing a “1” in this bit will start a conversion on the selected channel and automatically reset to zero the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

PDS. This bit activates the A/D converter if set to “1”. Writing a zero into this bit will put the ADC in power down mode (idle mode).

D3-D0. Not used

Figure 37. A/D Converter Data Register



SOFTWARE DESCRIPTION

The ST62xx software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST62xx core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

Addressing Modes

The ST62xx core has nine addressing modes which are described in the following paragraphs. The ST62xx core uses three different address spaces : Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X,Y,V and W registers, peripheral and Input/Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct. The core can address the four RAM registers X,Y,V,W (locations 80h, 81h, 82h, 83h) in the short-direct addressing mode . In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch to any address of the 4K bytes Program space.

An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained in adding the three most significant bits that characterize the kind of the test, one bit that determines whether the branch is a forward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0h to Fh) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range of -126 to +129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80h,81h). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST62xx core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types:load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types.

All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes.

For Load Immediate one operand can be any of the 256 data space bytes while the other is always immediate data.

Table 12. Load & Store Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 13. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieve a branch in the program when the selected condition is met.

Bit Manipulation Instructions. These instructions can handle any bit in data space memory. One group either sets or clears. The other group (see Conditional Branch) performs the bit test branch operations.

Control Instructions. The control instructions control the MCU operations during program execution.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space.

Table 14. Conditional Branch Instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b. 3-bit address
e. 5 bit signed displacement in the range -15 to +16
ee. 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ. Affected
*. Not Affected

Table 15. Bit Manipulation Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b. 3-bit address;
rr. Data space register;
*. Not Affected

Table 16. Control Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated and a WAIT is automatically executed instead of a STOP if the watchdog function is selected.
Δ. Affected
*. Not Affected

Table 17. Jump & Call Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc.12-bit address;
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used by ST6

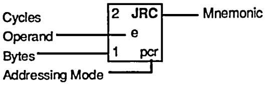
LOW HI	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW HI
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b.d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b.d.	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b.d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b.d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b.d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b.d	2 JRZ e 1 pcr	#	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b.d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b.d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b.d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

Tj = T_A + PD x RthJA

Where :T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = I_{DD} x V_{DD} (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3[1]	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3[1]	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50[2]	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50[2]	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.
- (2) The total current through ports A and B combined may not exceed 50mA. The total current through port C may not exceed 50mA. If the application is designed with care and observing the limits stated above, total current may reach 100mA.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

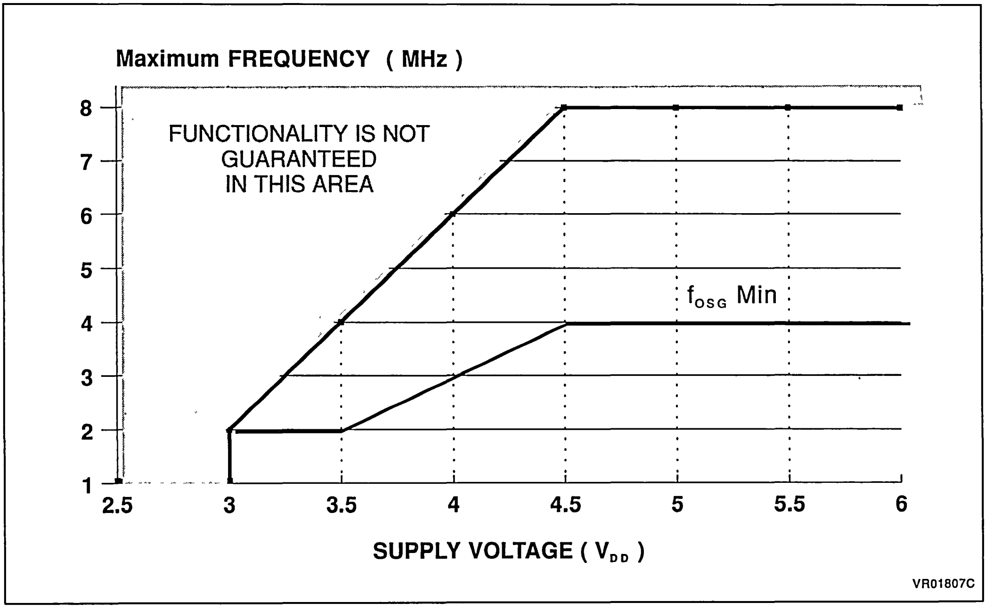
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 2MHz f_{INT} = 2MHz	3.0		6.0	V
		f_{OSC}= 4MHz f_{INT} = 4MHz	3.5		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
f_{INT}	Internal Frequency [3]	V_{DD} = 3V; OSG disabled V_{DD}= 4.5V;OSG disabled	0 0		2.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input [1] Analog Inputs[2]	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input [1] Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An internal frequency above 1MHz is recommended for reliable A/D results.

Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})



The shade area is outside the ST6210B/15B operating range, device functionality is not guaranteed.

DC ELECTRICAL CHARACTERISTICS
(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage TIMER,NMI,RESET pins				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage TIMER,NMI,RESET pins		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage [4] All Inputs	V_{DD}= 5V V_{DD}= 3V		1 0.5		V
V_{OL}	Low Level Output Voltage TIMER pin	I_{OL}= + 5.0mA			0.2 x VDD	V
V_{OH}	High Level Output Voltage TIMER pin	I_{OH} = – 5.0mA	V_{DD} x 0.65			V
R_{PU}	Pull-up TIMER, NMI pins		50	100	200	kΩ
I_{IL} I_{IH}	Input Leakage Current[1] TIMER, NMI pins	V_{IN}= V_{SS} V_{IN}= V_{DD}		0.1	1.0	µA
I_{IL} I_{IH}	Input Leakage Current RESET pin	V_{IN}=V_{DD}; Watchdog Res. V_{IN}=V_{DD}; No Watch. Res. V_{IN}=V_{SS}; External Res.	 -8	 -16	1 10 -30	mA µA µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}= V_{SS} f_{OSC}= 8MHz			3.5	mA
	Supply Current in RUN Mode [2]	V_{DD} = 5.0V f_{INT}=8MHz V_{DD} = 5.0V f_{INT}=f_{LFAO} V_{DD} = 3.0V f_{INT}=2MHz			3.5 TBD TBD	mA
	Supply Current in WAIT Mode [3]	V_{DD}= 5.0V f_{INT}=8MHz V_{DD} = 5.0V f_{INT}=f_{LFAO} V_{DD}= 3.0V f_{INT}=2MHz			1.50 TBD TBD	mA
	Supply Current in STOP Mode [3]	I_{LOAD}= 0mA V_{DD}= 5.0V			10	µA

Notes :
1. Only when pull-ups are not inserted
2. All peripherals running
3. A/D Converter in Stand-by
4. Hysteresis voltage between switching levels

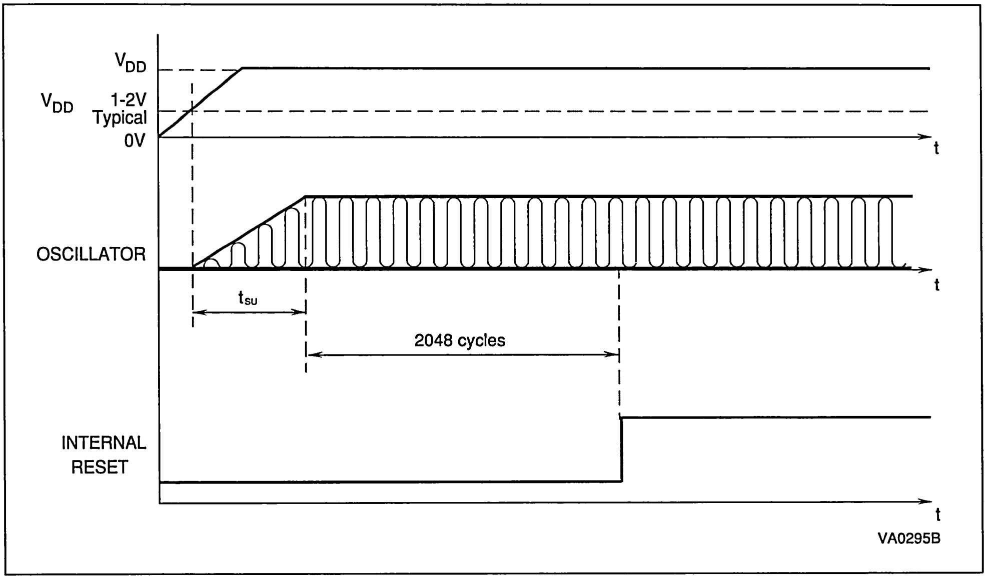
AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

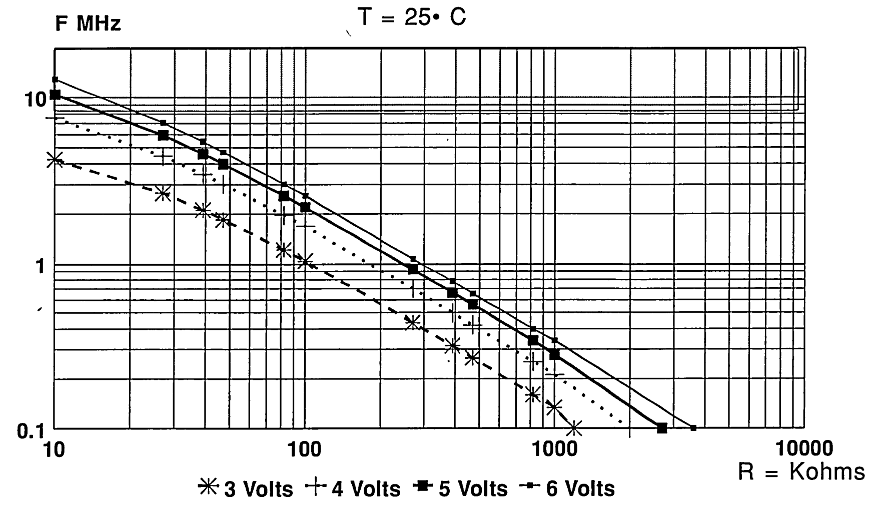
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V; OSG disabled V_{DD} = 4.5V; OSG disabled			2 8	MHz
f_{OSG}	Maximum internal frequency with OSG enabled	VDD = 3.0V V_{DD} = 4.5V	2 4			MHz
f_{LFAO}	Low Frequency Auxiliary Oscillator		200	400	800	kHz
t_{SU}	Oscillator Start-up Time at Power On (2)	Ceramic Resonator $C_{L1} = C_{L2}$ = 22pF		5	100	ms
t_{SUS}	Oscillator STOP mode Recovery Time (2)	8MHz Ceramic Resonator CL1=C_{L2}=22pF		0.2	100	
		8MHz Quartz CL1=C_{L2}=22pF		10	100	
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:
1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.
2. See Figure 38. This value is highly dependent on the Ceramic Resonator or Quartz Crystal used in the application.

Figure 38.Power On Reset



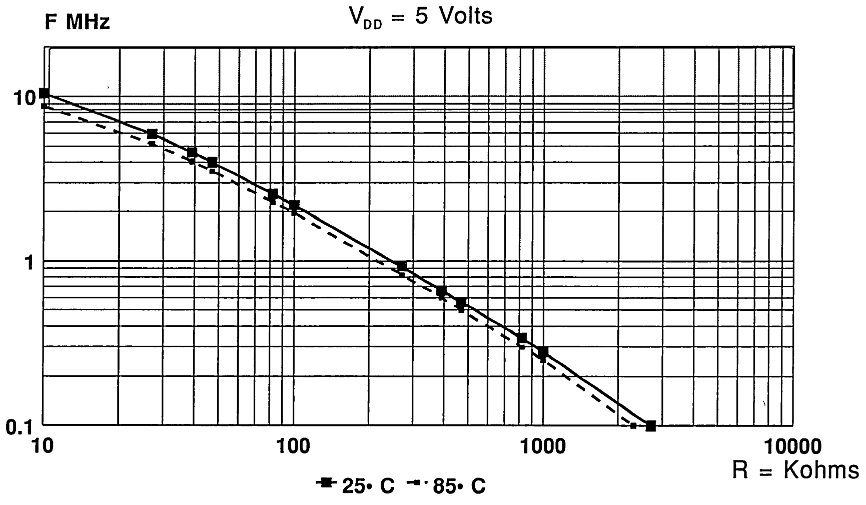
RC Oscillator. fINT versus RNET (Indicative Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

VR01935

RC Oscillator. fINT versus RNET (Indicative Values)

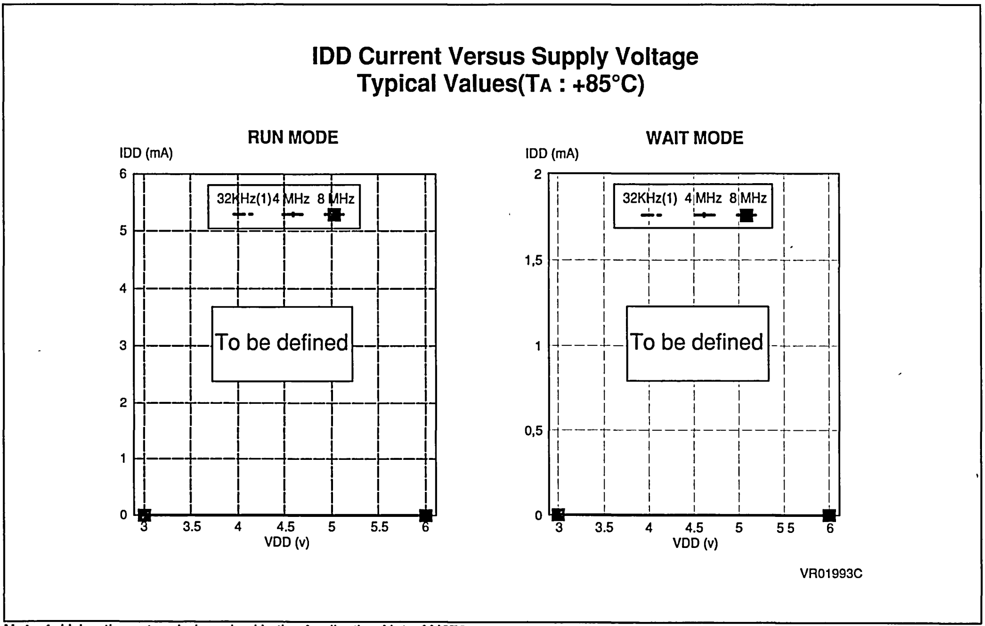


The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

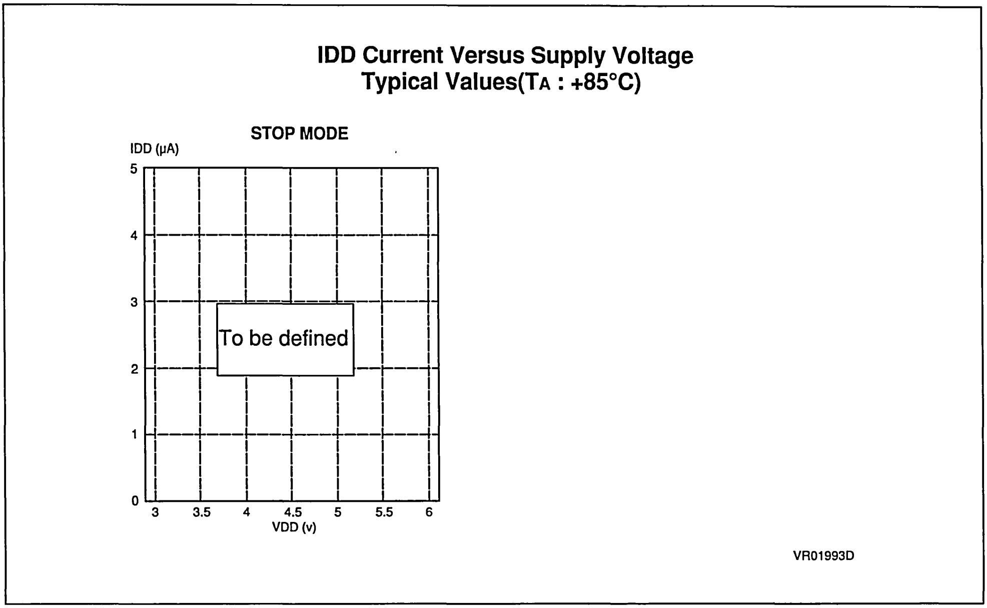
VR01935A

ELECTRICAL CHARACTERISTICS (Continued)

CURRENT CONSUMPTION



Note 1. Using the network described in the Application Note AN673



I/O PORT CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA } PA0-PA3 I_{OL}= 20mA } PA0-PA3			 0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		 0.1 0.1	 1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	kΩ

TIMER CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIMER Pin	Stop Mode Run and Wait Modes			2 $\frac{f_{INT}}{8}$	MHz MHz
t_W	Pulse Width at TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -40 to +85°C unless otherwise specified)

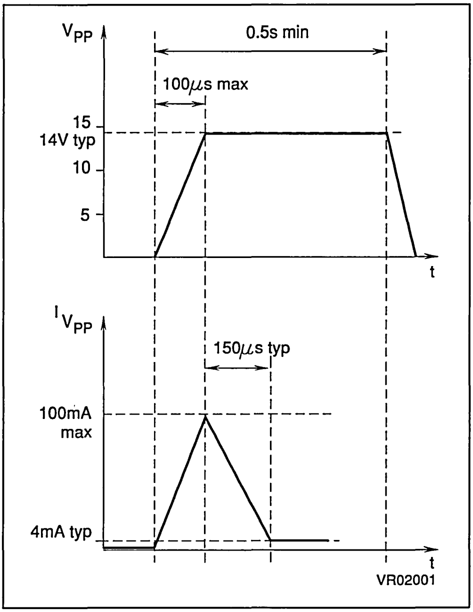
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy [1] [2]	f_{OSC} > 1.2MHz f_{OSC} > 32kHz		±1	±2 ±4	LSB
t_C	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when V_{IN} = V_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when V_{IN} = V_{DD}			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN}[3]	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance	Analog Channel switched just before conversion start [4]			30	kΩ

Notes:

1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

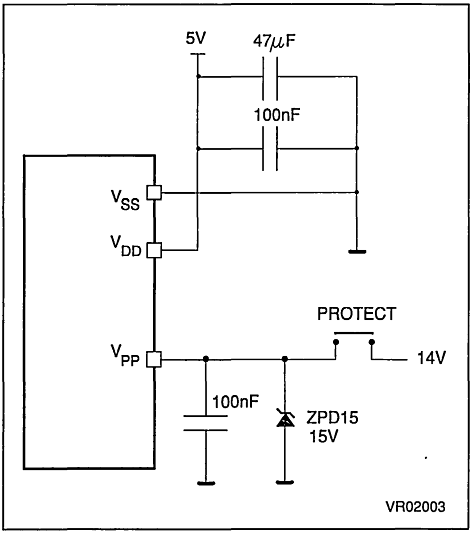
READ PROTECTION FUSE

If the ROM READOUT PROTECTION option is selected as enabled, the following waveform must be applied at the V_{PP} pin for the fuse to be blown:



The following circuit can be used for this purpose:

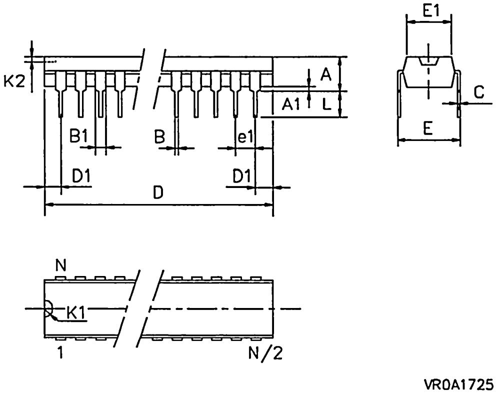
Figure 39. Example of READOUT PROTECTION fuse programming circuit



Note: ZPD15 is used for overvoltage protection

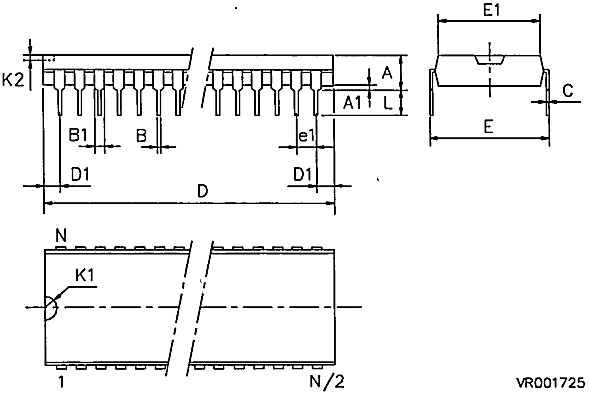
PACKAGE MECHANICAL DATA

Figure 40. 20-Pin Dual in Line Plastic (B), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.93			0.155
A1	0.254			0.010		
B			0.45			0.017
B1	1.39		1.65	0.055		0.065
C			0.25			0.009
D			25.4			1.000
D1			1.34			0.053
E		8.5			0.334	
E1			7.1			0.279
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L		3.30			0.129	
e1		2.54			0.10	
Number of Pins						
N	20					

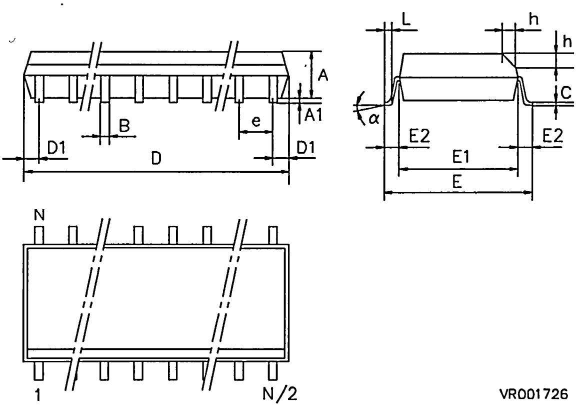
Figure 41. 28-Pin Dual in Line Plastic (B), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9			0.508	
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

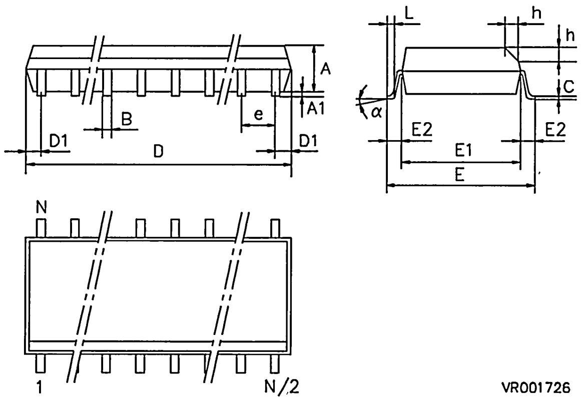
PACKAGES MECHANICAL DATA (Continued)

Figure 42. 20-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	12.6		13.0	.4961		.5118
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	20					

Figure 43. 28-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

ORDERING INFORMATION

The following chapter deals with the procedure for transfer customer codes to SGS-THOMSON.

Communication of the customer code. Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on one diskette with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to SGS-THOMSON using the correctly filled OPTION LIST appended.

Listing Generation & Verification. When SGS-THOMSON receives the diskette, a computer listing is generated from it. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask.

SGS-THOMSON sales organization will provide detailed information on contractual points.

Table 18. ROM Memory Map

ST6210B,ST6215B (2K ROM Devices)

Device Address	**Description**
0000h-087Fh	Reserved [1]
0880h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved [1]
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved [1]
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

ST6220B,ST6225B (4K ROM Devices)

Device Address	Description
0000h-007Fh	Reserved [1]
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved [1]
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved [1]
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Note 1. Reserved Areas should be filled with FFh

ORDERING INFORMATION TABLE

Sales Type	ROM x8	I/O	Additonal Features	Temperature Range	Package
ST6210BB1/XXX ST6210BB6/XXX	2K Bytes	12	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP20
ST6210BM1/XXX ST6210BM6/XXX				0 to +70°C -40 to +85°C	PSO20
ST6215BB1/XXX ST6215BB6/XXX		20	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP28
ST6215BM1/XXX ST6215BM6/XXX				0 to +70°C -40 to +85°C	PSO28
ST6220BB1/XXX ST6220BB6/XXX	4K Bytes	12	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP20
ST6220BM1/XXX ST6220BM6/XXX				0 to +70°C -40 to +85°C	PSO20
ST6225BB1/XXX ST6225BB6/XXX		20	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP28
ST6225BM1/XXX ST6225BM6/XXX				0 to +70°C -40 to +85°C	PSO28

Note: /XXX is a 2-3 alphanumeric character code added to the generic sales type on receipt of a ROM code and valid options.

ST6210B, ST6215B , ST6220B, ST6225B MICROCONTROLLER OPTION LIST

Customer . . . .
Address . . . .
. . . .
Contact . . . .
Phone No . . . .
Reference . . . .

SGS-THOMSON Microelectronics references
Device: [ ] ST6210B [ ] ST6215B [ ] ST6220B [ ] ST6225B

Package: [ ] Dual in Line Plastic [ ] Small Outline Plastic
In this case, select conditioning
[ ] Standard (Stick)
[ ] Tape & Reel

Temperature Range: [ ] 0°C to + 70°C [ ] – 40°C to + 85°C
Special Marking: [ ] No
[ ] Yes "_ _ _ _ _ _ _ _ _ _ _ _ _ _"
Authorized characters are letters, digits, '.', '–', '/' and spaces only.
Maximum character count DIP20 - DIP28: 10
SO20 - SO28:8
Oscillator Source Selection: [ ] Crystal/Resonator
[ ] RC Network
Watchdog Selection: [ ] Software Activation (STOP mode available)
[ ] Hardware Activation (no STOP mode)
OSG: [ ] Enabled
[ ] Disabled
Input pull-up selection on NMI pin : [ ] Yes [ ] No
Input pull-up selection on TIMER pin : [ ] Yes [ ] No
ROM Readout Protection: Please contact your local SGS-THOMSON Sales Office

Comment :
Supply Operating Range in the application: [ ] 3.0V to 6.0V
[ ] 4.5V to 6.0V
Notes . . . .
. . . .
Signature . . . .
Date . . . .

SGS-THOMSON
MICROELECTRONICS

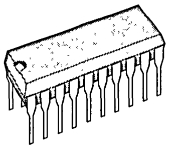
ST62T10B, T15B, E20B
ST62T20B, T25B, E25B

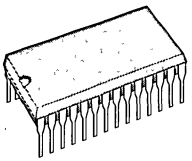
8-BIT OTP/EPROM HCMOS MCUs WITH A/D CONVERTER

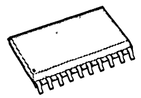
PRELIMINARY DATA

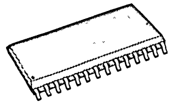
- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM
- User EPROM: 1828 bytes (ST62x10B, x15B)
  3876 bytes (ST62x20B, x25B)
- Data EPROM: User selectable size (in program EPROM)
- Data RAM: 64 bytes
- EPROM readout protection
- PDIP20, PSO20 (ST62T10B,T20B) packages
- PDIP28, PSO28 (ST62T15B,T25B) packages
- FDIP20, CSO20 (ST62E20B) packages
- FDIP28, CSO28 (ST62E25B) packages
- 12/20 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without Pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer)
- Digital Watchdog and Oscillator Safe Guard
- 8 bit A/D Converter with up to 8 (ST62T10B, ST62x20B) and up to 16 (ST62T15B, ST62x25B) analog inputs
- On-chip clock oscillator driven by Quartz Crystal, Ceramic resonator or RC network; Low Frequency Auxiliary Oscillator.
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The ST62E20B, E25B are the EPROM versions, the ST62T10B, T15B, T20B, T25B are the OTP versions, fully compatible with ROM versions ST6210B, 15B, 20B, 25B.

Device Summary page 55/67


PDIP20

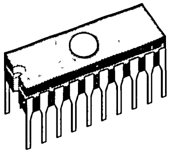

PDIP28

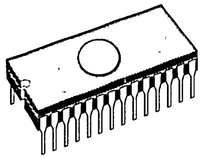

PSO20


PSO28

(Ordering Information at the end of the datasheet)

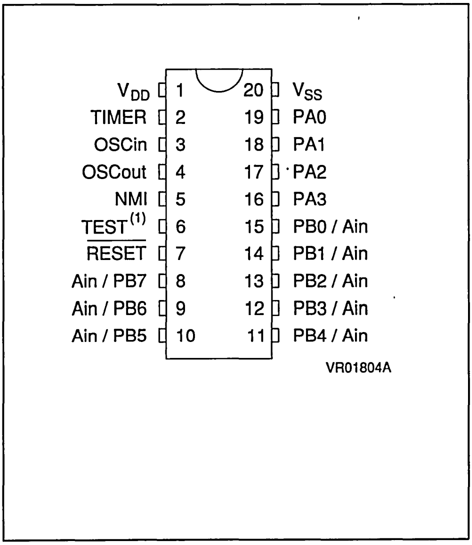
EPROM PACKAGES


FDIP20W


FDIP28W

This is preliminary data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. ST62T10B, T20B, E20B Pin Config.



Note 1. This pin is also the V_{PP} input for EPROM based device

Figure 2. ST62T15B, T25B, E25B Pin Config.

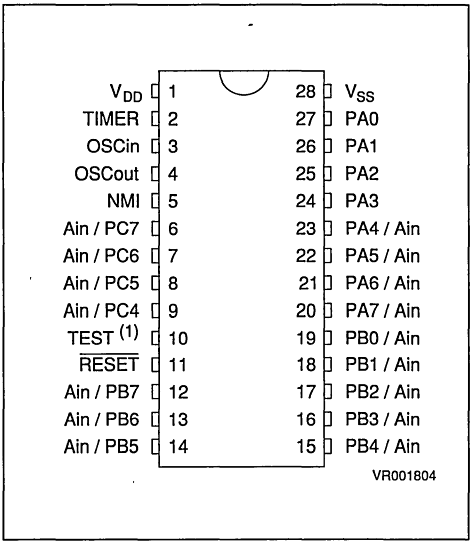
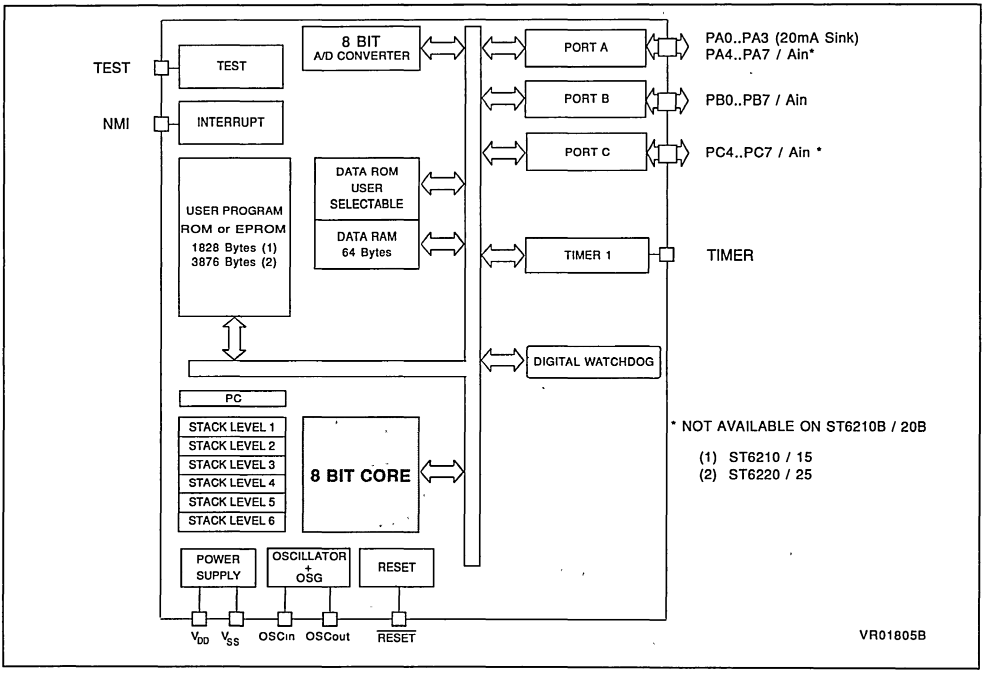


Figure 3. ST62T10B,T15B,T20B,T25B - ST62E20,E25 Block Diagram



GENERAL DESCRIPTION

The ST62T10B, T15B, T20B, T25B, E20B and E25B microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. They are the OTP/EPROM versions of the ST6210B, ST6215B, ST6220B and ST6225B devices respectively.

ST62E20B, E25B are user programmable and erasable devices. They are best suited for development.

ST62T10B, T15B, T20B, T25B are One Time Programmable devices (OTP). These offer the best cost/flexibility trade-off for prototyping and preseries as well as most low to medium volume applications.

All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells).

The macrocells of the ST6210B, 15B, 20B and 25B (available on the EPROM/OTP products) are: The Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler, the digital watchdog (DWD), an 8-bit A/D Converter with up to 8 (ST6210B, 20B) or 16 (ST6215B, 25B) analog inputs.

The ST62T10B, T15B, E20B, T20B, E25B, T25B are upward compatible with the ST62T10, T15, E20, T20, E25, T25. They in addition feature RC network, an External STOP Mode Control enlarging the range of power consumption/safety tradeoffs, an enhanced readout protection mechanism to prevent software piracy and an option byte to select options.

These devices are well suited for automotive, appliance and industrial applications.

DEVICE SUMMARY

Device	UV-EPROM	OTP ROM	I/O Pins	Emulated Device
ST62T10B		2K	12	ST6210B
ST62T15B		2K	20	ST6215B
ST62T20B		4K	12	ST6220B
ST62T25B		4K	20	ST6225B
ST62E20B	4K		12	ST6210B ST6220B
ST62E25B	4K		20	ST6215B ST6225B

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. Depending on the Option Byte, either a quartz crystal, a ceramic resonator, an external clock signal or an RC network can be connected in order to allow the correct operation of the MCU with various stability/cost trade-offs. The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST/V_{PP}. The TEST must be held at V_{SS} for normal operation. If TEST pin is connected to a +12.5V level during the reset phase, the EPROM programming Mode is entered. An internal pulldown resistor selects normal operating mode if the TEST/V_{PP} pin is left unconnected

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. The user can select the availability of an on-chip pull-up at NMI pin through the Option Byte.

TIMER. This is the timer I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a timeout occurs. The user can select the availability of an on-chip pull-up at TIMER pin through the Option Byte.

PA0-PA3,PA4-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs. PA0-PA3 can also sink 20mA for direct led driving while PA4-PA7 can be programmed as analog inputs for the A/D converter. **Note.** PA4-PA7 are not available on ST62T10B, ST62x20B.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter.

PC4-PC7. These 4 lines are organized as one I/O port (C). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter.

Note. PC4-PC7 are not available on ST62T10B, ST62x20B.

THE USER IS ASKED TO REFER TO THE DATASHEET OF THE ST6210B, 15B, 20B, 25B ROM DEVICE FOR FURTHER DETAILS.

EPROM/OTP DESCRIPTION

The ST62E20B, E25B are the EPROM versions of the ST6220B/25B products. They are intended for use during the development of an application and for pre-production and small volume production. ST62T20B/T25B OTP (One Time Programmable) have the same characteristics except that they cannot be erased. They all include EPROM memory instead of the ROM memory of the corresponding ST6220B/25B. User can program these devices using the ST62E2xB EPROM programming tools from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E20B, E25B and ST62T10B, T15B, T20B, T25B products have exactly the same software and hardware features as the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/VPP pin. The programming of the ST62E20B, E25B, T10B, T15B, T20B, T25B is described in the User Manual of the EPROM Programming Board.
Other than this exception, the OTP, EPROM and ROM parts are fully compatible. This datasheet thus provides only information specific to the EPROM based devices.

ROM Option Emulation

The ROM mask options that can be selected by the user in the ROM devices can be selected on the EPROM/OTP devices by an Option Byte that can be programmed with the ST62E2xB EPROM programming tools available from SGS-THOMSON. This Option Byte is automatically read, and the selected options enabled, when the power supply is switched on.
The Option Byte is written during programming either by using the PC menu (PC driven Mode) or automatically (stand-alone mode).

EPROM Programming Mode

An additional mode is used to configure the part for programming of the EPROM. This is set by a 12.5V voltage applied to the TEST/VPP pin. The programming of the ST62E20B, E25B, and ST62T10B, T15B, T20B, T25B is described in the User Manual of the EPROM Programming Board.

EPROM ERASING

The EPROM of the windowed package of the ST62E20B, E25B may be erased by exposure to Ultra Violet light.

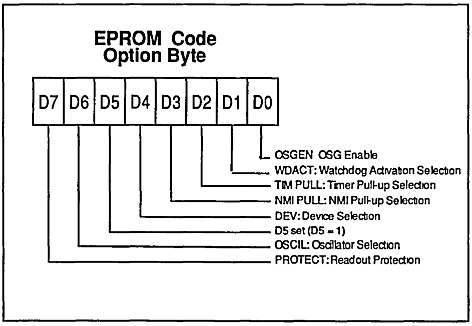
The erasure characteristic of the ST62E20B, E25B is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E20B, E25B packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the ST62E20B, E25B EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-s/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with $12000\mu W/cm^{2}$ power rating. The ST62E20B, E25B should be placed within 2.5cm (1 Inch) of the lamp tubes during erasure.

OPTION BYTE

The Option Byte enables emulation of the mask options of the ROM devices. It can only be accessed during the programming mode. This access is made either automatically (copy from a master device) or by selecting the "OPTION BYTE PROGRAMMING" mode of the programmer. The option byte is located in a non-user map. No address has to be specified.

Figure 4. EPROM Code Option Byte


EPROM Code
Option Byte
D7
D6
D5
D4
D3
D2
D1
D0
OSGEN OSG Enable
WDACT: Watchdog Activation Selection
TIM PULL: Timer Pull-up Selection
NMI PULL: NMI Pull-up Selection
DEV: Device Selection
D5 set (D5 = 1)
OSCIL: Oscillator Selection
PROTECT: Readout Protection

PROTECT. This bit allows the protection of the software contents against piracy. When the bit PROTECT is set high, readout of the EPROM/OTP contents is prevented by hardware. No programming equipment is able to gain access to the user program. When this bit is low, the user program can be read. This bit emulates the READOUT PROTECTION mask option of ROM devices.

OSCIL. When this bit is high, the oscillator must be controlled by a quartz crystal, a ceramic resonator or an external frequency. When it is low, the oscillator must be controlled by an RC network, with only the resistor having to be externally provided. This bit emulates the OSCILLATOR mask option of ROM devices.

DEV. This bit must be set to one on the ST62T15B, T25B and E25B devices. It must be cleared to 0 on the ST62T10B, T20B and E20B. This bit is used to tie I/O pins not connected in the 20 pin packaged devices to V_{DD} in order to avoid unconnected CMOS inputs.

NMI PULL. This bit must be set high to configure the NMI pin with a pull up resistor. When it is low, no pull up is provided. This bit emulates the NMI PIN PULL-UP mask option available in ROM devices.

TIM PULL. This bit must be set high to configure the TIMER pin with a pull up resistor. When it is low, no pull up is provided. This bit emulates the TIMER PIN PULL-UP mask option available in ROM devices.

WDACT. This bit controls the watchdog activation. When it is high, hardware activation is selected. The software activation is selected when WDACT is low.This bit emulates the WATCHDOG ACTIVATION mask option of ROM devices.

OSGEN. This bit must be set high to enable the Oscillator Safe Guard. When this bit is low, the OSG is disabled. This bit emulates the OSG mask option available in ROM devices.

Table 1. OTP Memory Map

ST62T10B, ST62T15B
(2K ROM Devices)

Device Address	Description
0000h-087Fh	Reserved [(1)]
0880h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved [(1)]
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved [(1)]
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Note 1. Reserved Areas should be filled with FFh

ST62T20B, T25B
(4K ROM Devices)

Device Address	Description
0000h-007Fh	Reserved [(1)]
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved [(1)]
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved [(1)]
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Note 1. Reserved Areas should be filled with FFh

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

	Tj =	T_A + PD x RthJA
Where :	T_A =	Ambient Temperature.
	RthJA =	Package thermal resistance (junction-to ambient).
	PD =	Pint + Pport.
	Pint =	I_{DD} x V_{DD} (chip internal power).
	Pport =	Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3[1]	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3[1]	V
V_{PP}	EPROM Programming Voltage	13	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50[2]	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50[2]	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

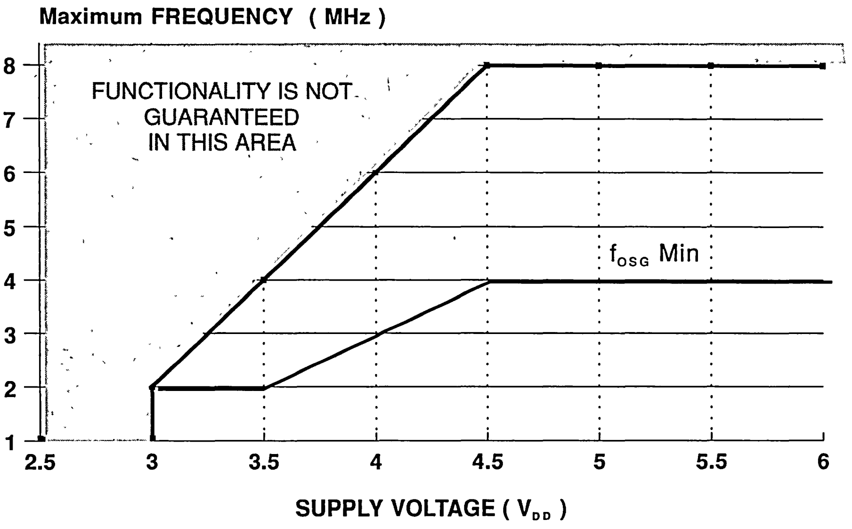
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version	-40		85	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 2MHz f_{INT}= 2MHz	3.0		6.0	V
		f_{OSC}= 4MHz f_{INT}= 4MHz	3.5		6.0	V
		f_{OSC} = 8MHz f_{INT}=8MHz	4.5		6.0	V
f_{INT}	Internal Frequency [(3)]	V_{DD} = 3V;OSG disabled V_{DD} = 4.5V;OSG disabled	0 0		2.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input [(1)] Analog Inputs[(2)]	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input [(1)] Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An internal frequency above 1MHz is recommended for reliable A/D results.

Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})



The shaded area is outside the ST62T10B/T15B operating range, device functionality is not guaranteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage TIMER,NMI,RESET pins				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage TIMER,NMI,RESET pins		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage [4] All Inputs	V_{DD}= 5V V_{DD}= 3V		1 0.5		V
V_{OL}	Low Level Output Voltage TIMER pin	I_{OL} = + 5.0mA			V_{DD} x 0.2	V
V_{OH}	High Level Output Voltage TIMER pin	I_{OH} = – 5.0mA	V_{DD} x 0.65			V
I_{IL} I_{IH}	Input Leakage Current[1] TIMER, NMI pins	V_{IN}= V_{SS} V_{IN}= V_{DD}		0.1	1.0	µA
I_{IL} I_{IH}	Input Leakage Current RESET pin	V_{IN}=V_{DD}; Watchdog Res. V_{IN}=V_{DD}; No Watch. Res. V_{IN}=V_{SS}; External Res.	 -8	 -16	1 10 -30	mA µA µA
R_{PU}	Pull-up TIMER, NMI pins		50	100	200	kΩ
I_{DD}	Supply Current in RESET Mode	V_{RESET}= V_{SS} f_{OSC}= 8MHz			3.5	mA
	Supply Current in RUN Mode [2]	V_{DD} = 5.0V f_{INT}=8MHz V_{DD}= 5.0V f_{INT}=f_{LFAO} V_{DD} = 3.0V f_{INT}=2MHz			3.5 TBD TBD	mA
	Supply Current in WAIT Mode [3]	V_{DD}= 5.0V f_{INT}=8MHz V_{DD}= 5.0V f_{INT}=f_{LFAO} V_{DD}= 3.0V f_{INT}=2MHz			1.50 TBD TBD	mA
	Supply Current in STOP Mode [3]	I_{LOAD}= 0mA V_{DD}= 5.0V			10	µA

Notes :

1. Only when pull-ups are not inserted
2. All peripherals running
3. A/D Converter in Stand-by
4. Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

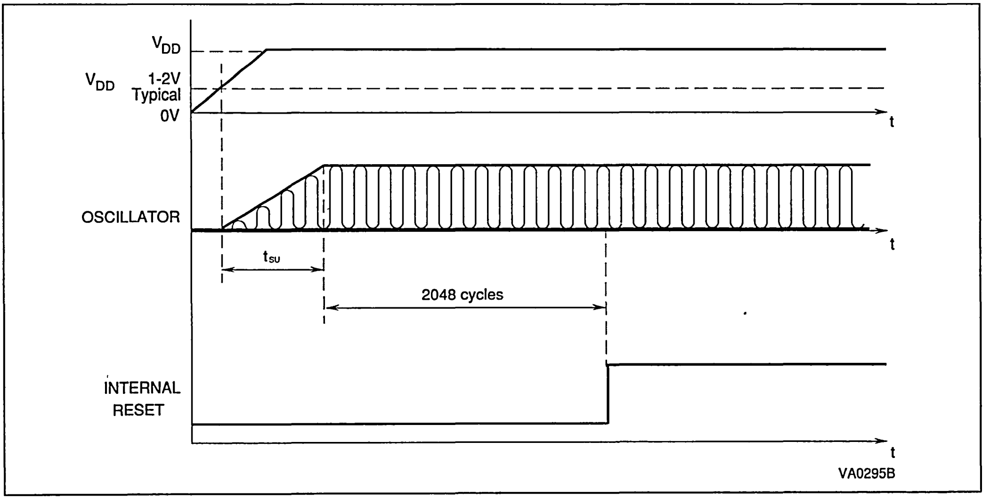
(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V; OSG disabled V_{DD} = 4.0V; OSG disabled V_{DD} = 4.5V; OSG disabled			2 6 8	MHz
f_{OSG}	Maximum internal frequency with OSG enabled	VDD = 3.0V V_{DD} = 4.5V	2 4			MHz
f_{LFAO}	Low Frequency Auxiliary Oscillator frequency		200	400	800	kHz
t_{SU}	Oscillator Start-up Time at Power On [2]	Ceramic Resonator C_{L1} = C_{L2} = 22pF		5	100	ms
t_{SUS}	Oscillator STOP mode Recovery Time [2]	8MHz Ceramic Resonator C_{L1}=C_{L2}=22pF		0.2	100	
		8MHz Quartz C_{L1}=C_{L2}=22pF		10	100	
t_{REC}	Supply Recovery Time [1]		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
Retention	EPROM Data Retention	T_A=55°C	10			Year
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

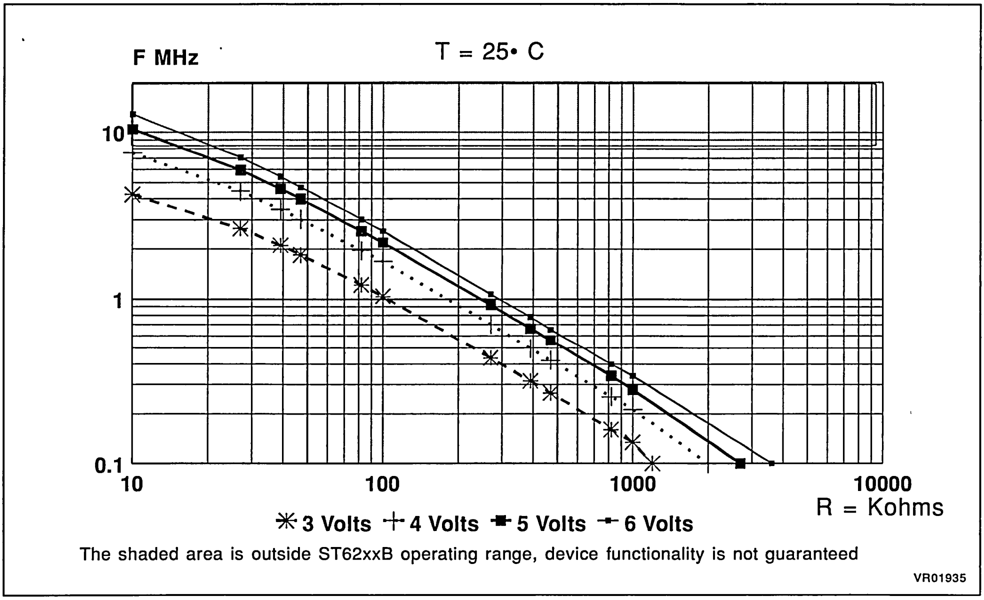
Notes:

1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.
2. See Figure 5. This value is highly dependent on the Ceramic Resonator or Quartz Crystal used in the application.

Figure 5. Power On Reset

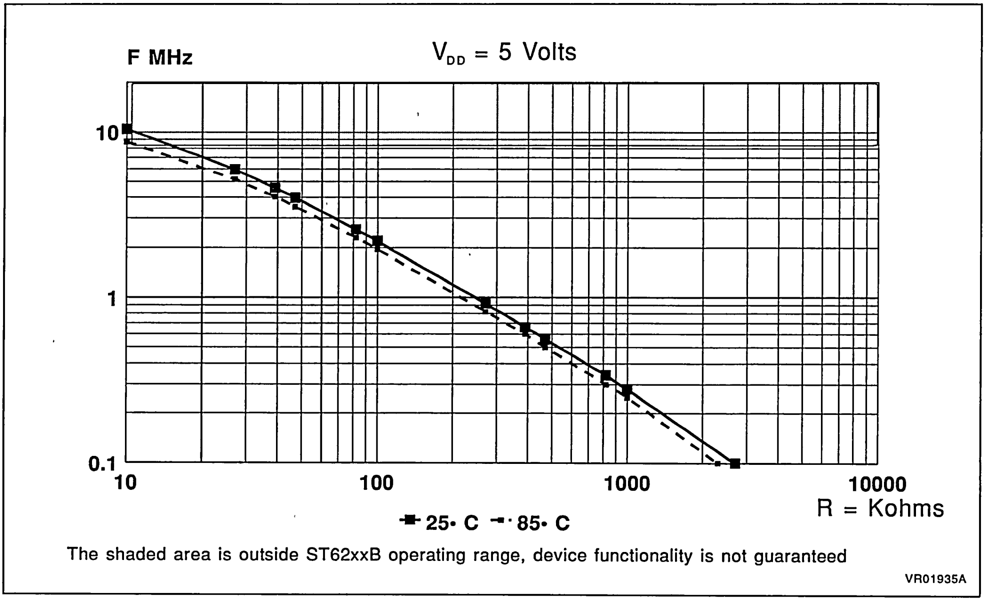


RC Oscillator, fosc Frequency versus RNET (Typical Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

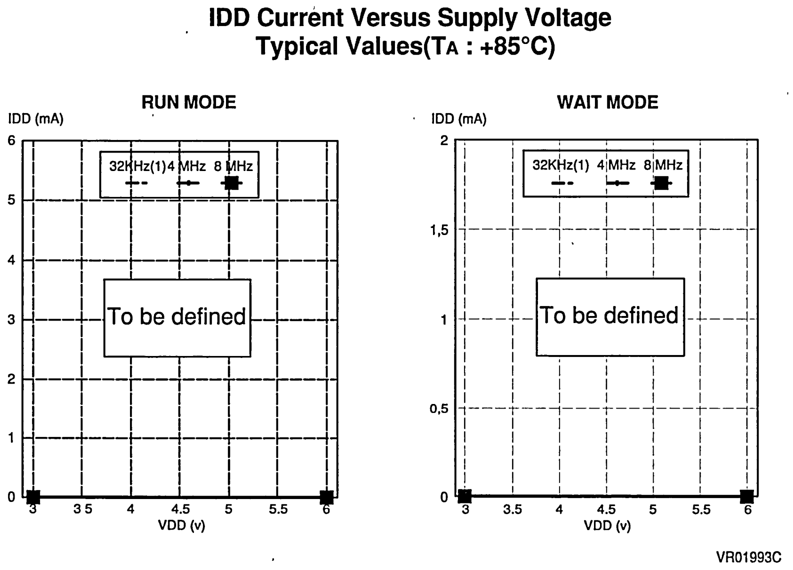
RC Oscillator, fosc Frequency versus RNET (Typical Values)



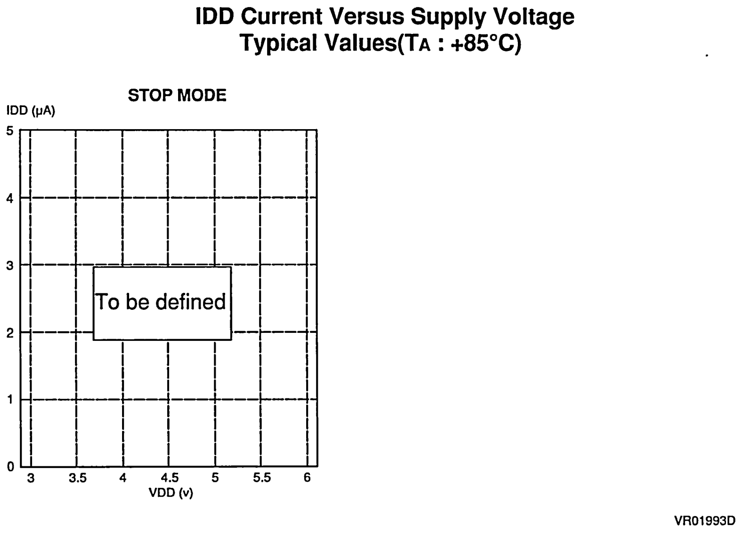
The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

ELECTRICAL CHARACTERISTICS (Continued)

CURRENT CONSUMPTION



Note1. Using the network described in the Application Note AN673



I/O PORT CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA } PA0-PA3 I_{OL}= 20mA } PA0-PA3			 0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		 0.1 0.1	 1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	kΩ

TIMER CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIMER Pin	STOP Mode Run and Wait Modes			2 $\frac{f_{INT}}{8}$	MHz MHz
t_W	Pulse Width at TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -40 to +85°C unless otherwise specified)

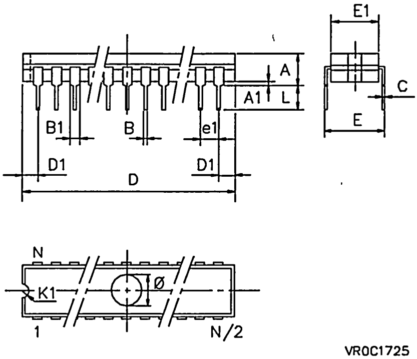
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution [(1)]			8		Bit
A_{TOT}	Total Accuracy [(1)]	f_{OSC} > 1.2MHz f_{OSC} > 32kHz		±1	±2 ±4	LSB
t_C[(2)]	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when Vin = V_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when Vin = V_{DD}			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN}[(3)]	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance				30	kΩ

Notes:

1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

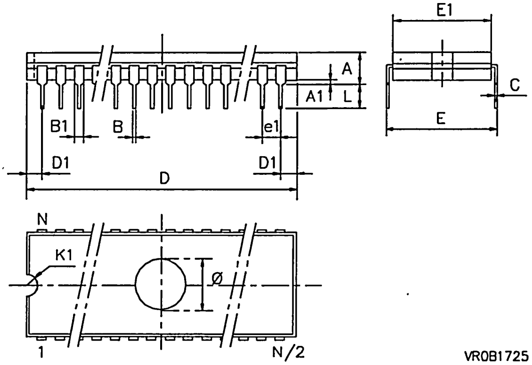
PACKAGE MECHANICAL DATA

20-Lead Frit Seal Ceramic Dual in Line Pàckage, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.27		1.52	0.050		0.060
C	0.22		0.31	0.009		0.012
D			26.92			1.059
D1	0.51		1.27	0.020		0.050
E	–	–	–	–	–	–
E1			7.80			0.307
L	3.40			0.134		
e1	2.29		2.79	0.090		0.110
Ø	4.24		4.39	0.167		0.173
	Number of Pins					
N	20					

28-Lead Frit Seal Ceramic Dual in Line Package, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

ORDERING INFORMATION TABLE

Sales Type	OTP/ EPROM	I/O	Additional Features	Temperature Range	Package
ST62T10BB6	**OTP** 2K Bytes	12	A/D Converter	-40 to +85°C	PDIP20
ST62T10BM6					PSO20
ST62T15BB6		20			PDIP28
ST62T15BM6					PSO28
ST62T20BB6	**OTP** 4K Bytes	12			PDIP20
ST62T20BM6					PSO20
ST62T25BB6		20			PDIP28
ST62T25BM6					PSO28
ST62E20BF1	**EPROM** 4K Bytes	12		0 to +70°C	FDIP20
ST62E25BF1		20			FDIP28

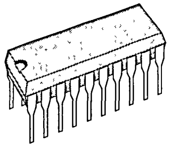
SGS-THOMSON
MICROELECTRONICS

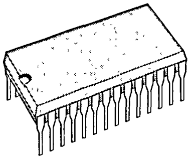
ST62T10-ST62T15
ST62T20,E20-ST62T25,E25

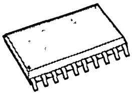
8-BIT OTP/EPROM HCMOS MCUs WITH A/D CONVERTER

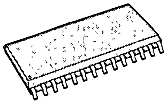
- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM
- User ROM: 1828 bytes (ST62T10, T15)
  3876 bytes (ST62x20, x25)
- Data ROM: User selectable size
  (in program ROM)
- Data RAM: 64 bytes
- PDIP20, PSO20 (ST62T10,T20) packages
- PDIP28, PSO28 (ST62T15,T25) packages
- FDIP20, CSO20 (ST62E20) packages
- FDIP28, CSO28 (ST62E25) packages
- 12/20 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without Pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 8 (ST62T10, ST62x20) and up to 16 (ST62T15, ST62x25) analog inputs
- On-chip clock oscillator
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The ST62E20, E25 are the EPROM versions, the ST62T10, T15, T20, T25 are the OTP versions, fully compatible with ROM versions ST6210, 15, 20, 25.

Device Summary page 3/15


PDIP20

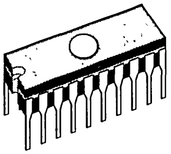

PDIP28

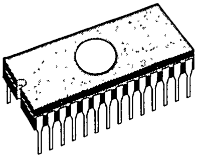

PSO20

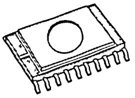

PSO28

(Ordering Information at the end of the datasheet)

EPROM PACKAGES


FDIP20W


FDIP28W


CSO20W

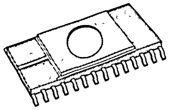

CSO28W

Figure 1: ST62T10,ST62x20 Pin Configuration

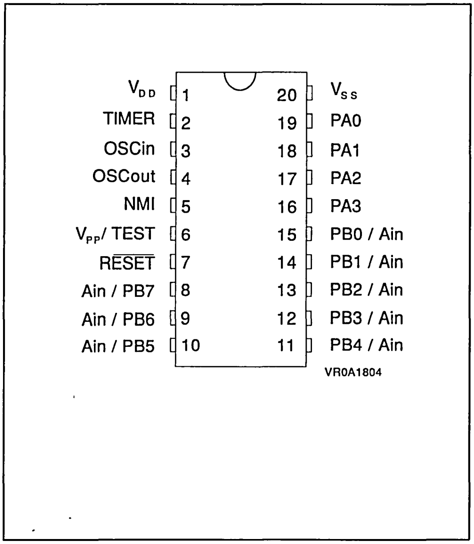


Figure 2. ST62T15,ST62x25 Pin Configuration

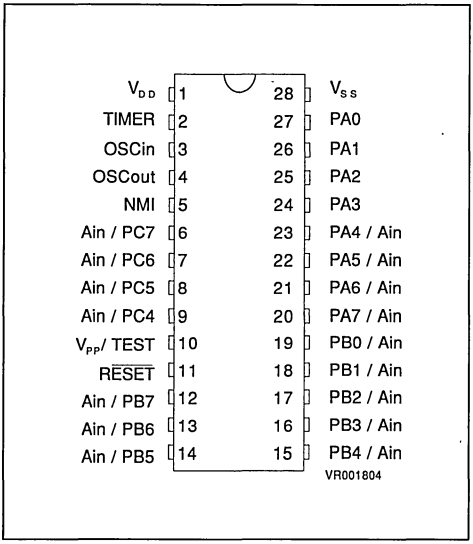
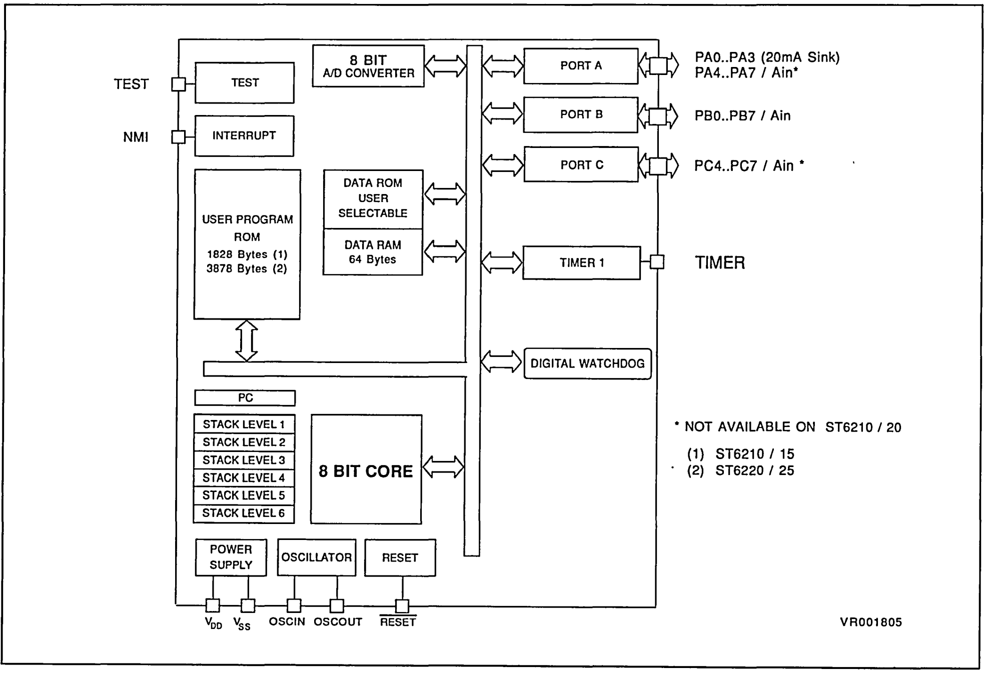


Figure 3. ST62T10,T15,x20,x25 Block Diagram



GENERAL DESCRIPTION

The ST62T10, T15, T20, T25, E20 and E25 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. They are OTP/EPROM versions of the ST6210B, ST6215B, ST6220B and ST6225B devices respectively.

All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6220, E25 and OTP ST62T10, T15, T20, T25 are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler, the digital watchdog (DWD), an 8-bit A/D Converter with up to 8 (ST6210, 20) or 16 (ST6215, 25) analog inputs. Thanks to these peripherals, these devices are well suited for automotive, appliance and industrial applications.

ST62E20, E25 are user programmable and erasable devices. They are best suited for development.
ST62T10,T15,T20,T25 are One Time Programmable devices (OTP). These offer the best cost/flexibility trade-off for prototyping and preseries as well as most low to medium volume applications.

The EPROM ST62E20, E25 and OTP ST62T10, T15, T20, T25 are downward compatible with the ROM ST621XB/2XB. They include the same functionalities and blocks as these ROM devices with the following exceptions: no RC network, no Oscillator Safe Guard (OSG), no external STOP Mode Control, no readout protection and no option byte.

DEVICE SUMMARY

Device	UV-EPROM	OTP ROM	I/O Pins	Emulated Device
ST62T10		2k	12	ST6210
ST62T15		2k	20	ST6215
ST62T20		4k	12	ST6220
ST62T25		4k	20	ST6225
ST62E20	4k		12	ST6210 ST6220
ST62E25	4k		20	ST6215 ST6225

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The OSCIN pin is the input pin, the OSCOUT pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST/V_{PP}. The TEST must be held at V_{SS} for normal operation. If TEST pin is connected to a +12.5V level during the reset phase, the EPROM programming Mode is entered.

NMI. The NMI pin provides the capability for asynchronous applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. NMI pin is not internally connected to an on-chip pull-up resistor which is available as a mask option for ROM devices. The pull-up resistor has to be provided externally.

TIMER. This is the timer I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time-out occurs. TIMER pin is not internally connected to an on-chip pull-up resistor which is available as a mask option for ROM devices. The pull-up resistor has to be provided externally.

PA0-PA3,PA4-PA7(*). These 8 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs. PA0-PA3 can also sink 20mA for direct led driving while PA4-PA7 can be programmed as analog inputs for the A/D converter.
(*) PA4-PA7 are not available on ST62T10, ST62x20.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter.

PC4-PC7(*). These 4 lines are organized as one I/O port (C). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter.
(*) PC4-PC7 are not available on ST62T10, ST62x20.

ST62T10, T15, T20, T25, E20 and E25, OTP/EPROM DESCRIPTION

The ST62E20 EPROM device emulates the ST6210B and ST6220B ROM devices. The ST62E25 EPROM device emulates the ST6215B and ST6225B ROM devices.

Care must be taken when emulating the 2K ROM devices to start the program at the correct address (see Memory Map for 2K Devices)

EPROM parts are programmed using any programming equipment supporting it and validated by SGS-THOMSON. Once erased, the device can be reprogrammed.

The ST62T10, T15, T20, T25 OTP devices are the counterparts of the ST6210B,15B,20B,25B ROM devices. OTP (One Time Programmable) parts are low cost devices which have to be programmed like EPROM devices. Unlike EPROM devices, OTPs cannot be erased once programmed.

From a user point of view, once programmed, these OTP and EPROM products have the same software and hardware features as the ROM ST621XB/2XB versions, except :

- No internal pull-up resistor available on pin NMI
- No internal pull-up resistor available on pin TIMER
- No RC network
- No Oscillator Safe Guard (OSG)
- No External STOP Mode Control
- No Readout protection

Other than these exceptions, ST62T10, T15, T20, T25 and ST62E20, E25 are fully compatible with the ST6210B, 15B, 20B, 25B equivalents, this datasheet thus provides only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6210, 15, 20, 25 ROM DEVICE FOR FURTHER DETAILS.

EPROM Programming Mode

An additional mode is used to configure the part for programming of the EPROM, this is set by a 12.5V voltage applied to the TEST/V$_{PP}$ pin. The programming of the OTP and EPROM parts is described in the User Manual of the EPROM Programming board.

EPROM ERASING

The EPROM of the windowed package of the ST62E20, E25 may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E20, E25 is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E20, E25 packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the ST62E20, E25 EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm2 power rating. The ST62E20, E25 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Table 1. OTP Memory Map

ST62T10, ST62T15 (2K ROM Devices)

Device Address	Description
0000h-087Fh	Reserved [1]
0880h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved [1]
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved [1]
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Notes :

[1] Reserved Areas should be filled with FFh

ST62T20, ST62T25 (4K ROM Devices)

Device Address	Description
0000h-007Fh	Reserved [1]
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved [1]
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved [1]
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Notes :

[1] Reserved Areas should be filled with FFh

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

Tj = T_A + PD x RthJA

Where: T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = I_{DD} x V_{DD} (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
V_{PP}	OTP/EPROM Programming Voltage	13	V
I_O	Current Drain per Pin Excluding V_{DD} & V_{SS}	± 10	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Note : Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	1 Suffix Version 6 Suffix Version	0 -40		70 85	°C
V_{DD}	Operating Supply Voltage		3.0		6.0	V
V_{PP}	Programming Voltage		12	12.5	13	V
F_{OSC}	Oscillator Frequency	$4.5 < V_{DD} < 6.0V$ $V_{DD} = 3.5V$ $V_{DD} = 3.0V$	0.01 0.01 0.01		8.0 4.0 2.0	MHz
AV_{DD} AV_{SS}	Analog Supply Voltage[1]	$V_{SS} \leq AV_{SS} < AV_{DD} \leq V_{DD}$	V_{SS}		V_{DD}	V
I_{INJ+}	Pin Injection Current (positive) Digital Input Analog Inputs [2]	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input Analog Inputs [3]	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :

1.An oscillator frequency above 1MHz is recommended for reliable A/D results.

2.A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.

3.If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.

DC ELECTRICAL CHARACTERISTICS

(T_A = -25 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	RESET Pin				
		V_{DD}=5V			1.6	V
		V_{DD}=3V			1	
V_{IH}	Input High Level Voltage	RESET Pin				
		V_{DD}=5V	3.4			V
		V_{DD}=3V	2			
I_{IL}	Input Leakage Current	RESET Pin				
I_{IH}		V_{IN}=V_{DD} (1)			10	µA
		V_{IN}=V_{DD} (2)			1	mA
		V_{IN}=V_{SS}	-8	-16	-30	µA
V_{IL}	Input Low Level Voltage	NMI,TIMER				
		V_{DD}=5V			0.3xV_{DD}	V
		V_{DD}=3V				
V_{IH}	Input High Level Voltage	NMI,TIMER				
		V_{DD}=5V	0.7xV_{DD}			V
		V_{DD}=3V				
V_{OL}	Low Level Output Voltage	TIMER, IOL=5.0mA V_{DD}=5V			0.2xV_{DD}	V
V_{OH}	High Level Output Voltage	TIMER, I_{OL}=-5.0mA V_{DD}=5V	0.65V_{DD}			V
I_{IL}	Input Leakage Current	TIMER				
I_{IH}		V_{IN}=V_{DD} or V_{SS}				
		V_{IN}=5.0V		0.1	1.0	µA
		V_{IN}=3.9V		0.1	1.0	
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS} f_{OSC}=8MHz			3.5	mA
	Supply Current in RUN Mode	f_{OSC}=8MHz I_{LOAD}=0mA V_{DD}=5.0V			3.5	mA
	Supply Current in WAIT Mode	f_{OSC}=8MHz (4) I_{LOAD}=0mA V_{DD}=5.0V			1.5	mA
	Supply Current in STOP Mode(3)	I_{LOAD}=0mA V_{DD}=5.0V			10	µA

Notes :

1. No Watchdog Reset Actived.
2. Reset generated by Watchdog.
3. When the Watchdog function is activated the STOP instruction is deactivated. WAIT instruction is automatically executed.
4. Timer and A/D in OFF state.

AC ELECTRICAL CHARACTERISTICS

(T_A= – 40 to + 85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	$V_{DD} = 3.0V$ $V_{DD} = 4.5V$ $V_{DD} = 5.5V$	0.01 0.01 0.01		2 8 8	MHz
t_{ILH}	Interrupt Pin Maximum Pulse Widht	$V_{DD} = 3.0V$ $V_{DD} = 4.5V$ $V_{DD} = 5.5V$			no limit	µs
t_{SU}	Oscillator Start-up Time			5	10	ms
t_{SR}	Supply Rise Time		0.01		100	ms
t_{REC}	Supply Recovery Time		100			ms
T_{WNMI}	Minimum Pulse Width	NMI Pin V_{DD}=5V	100			ns
T_{WRES}	Minimum Pulse Width	RESET Pin	100			ns
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All outputs Pins			10	pF

I/O PORTS CHARACTERISTICS

(T_A= – 40 to + 85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA , PA0-PA3 I_{OL}= 20mA , PA0-PA3			 0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		 0.1 0.1	 1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V	50	100	200	KΩ

TIMER CHARACTERISTICS

(T_A= – 40 to + 85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{OSC}}$			second
f_{IN}	Input Frequency on TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V			$\frac{f_{OSC}}{4}$	MHz
t_W	Pulse Width at TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= – 40 to + 85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C(1)	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		AV_{SS}		AV_{DD}	V
ZIR	Zero Input Reading	Conversion result when Vin = AV_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when Vin = AV_{DD}			FF	Hex
AV_{SS}(2) AV_{DD}	Analog Reference		V_{SS}		V_{DD}	V
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN}(3)	Analog Input Capacitance				2	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Reference Supply Impedence				2	KΩ

Notes:

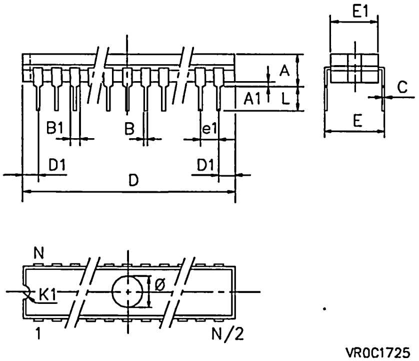
1. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased. It is recommended not to use the A/D with fOSC < 1Mhz.

2. In ST6210, ST6215, ST6220 and ST6225 AVSS and AVDD are internally connected to digital VSS and VDD.

3. Excluding Pad Capacitance.

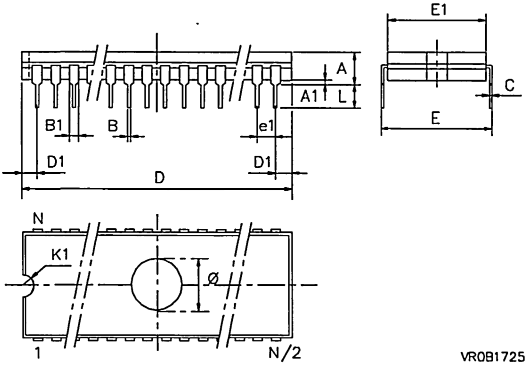
PACKAGE MECHANICAL DATA

20-Lead Frit Seal Ceramic Dual in Line Package, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.27		1.52	0.050		0.060
C	0.22		0.31	0.009		0.012
D			26.92			1.059
D1	0.51		1.27	0.020		0.050
E	–	–	–	–	–	–
E1			7.80			0.307
L	3.40			0.134		
e1	2.29		2.79	0.090		0.110
Ø	4.24		4.39	0.167		0.173
	Number of Pins					
N	20					

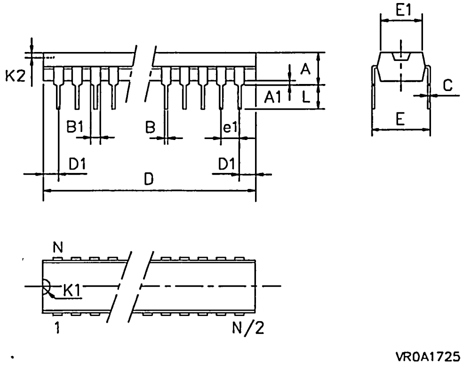
28-Lead Frit Seal Ceramic Dual in Line Package, 600-Mil Widht



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

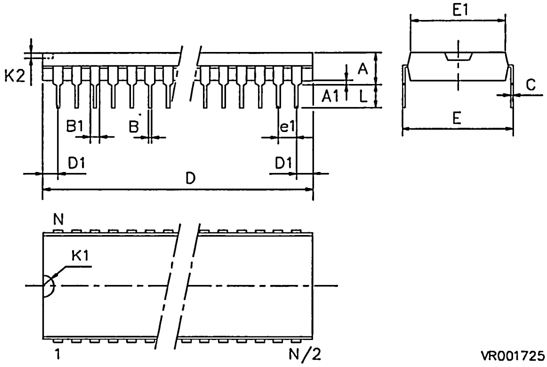
PACKAGE MECHANICAL DATA (Continued)

20-Pin Dual in Line Plastic, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.93			0.155
A1	0.254			0.010		
B			0.45			0.017
B1	1.39		1.65	0.055		0.065
C			0.25			0.009
D			25.4			1.000
D1			1.34			0.053
E		8.5			0.334	
E1			7.1			0.279
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L		3.30			0.129	
e1		2.54			0.10	
	Number of Pins					
N	20					

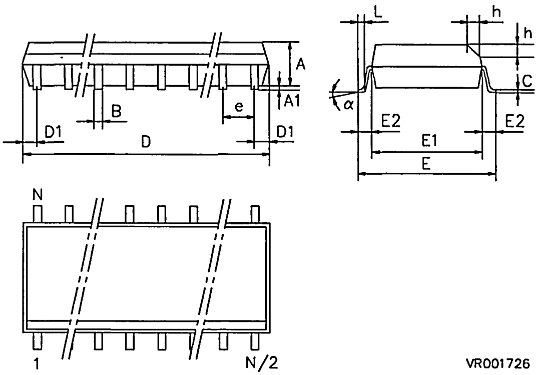
28-Pin Dual in Line Plastic, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4 8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
	Number of Pins					
N	28					

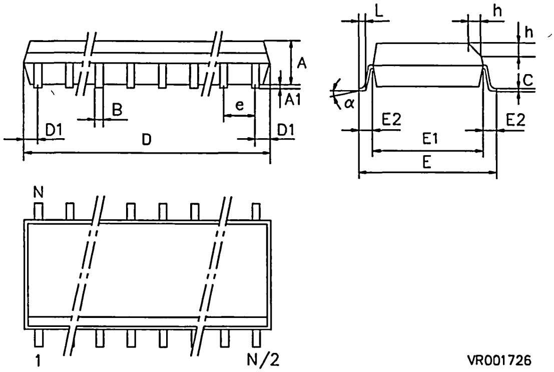
PACKAGES MECHANICAL DATA (Continued)

20-Lead Small Outline Plastic, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	12.6		13.0	.4961		.5118
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	20					

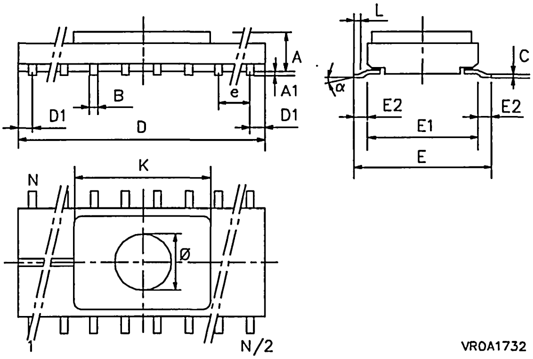
28-Lead Small Outline Plastic, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0 016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

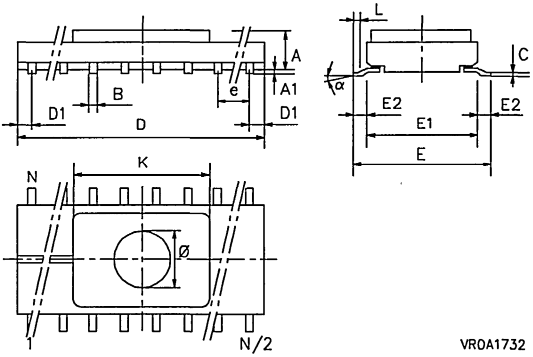
PACKAGES MECHANICAL DATA (Continued)

20-Lead Small Outline Ceramic, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
A1						
B						
C						
D						
D1	–	–	–	–	–	–
E						
E1						
E2	–	–	–	–	–	–
L						
e		1.27			0 05	
α	–	–	–	–	–	–
Number of Pins						
N	20					

28-Lead Small Outline Ceramic, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
A1						
B						
C						
D						
D1	–	–	–	–	–	–
E						
E1						
E2	–	–	–	–	–	–
L						
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

ORDERING INFORMATION TABLE

Sales Type	OTP/ EPROM	I/O	Additional Features	Temperature Range	Package
ST62T10B6/HWD ST62T10B6/SWD	**OTP** 2K Bytes	12	Hardware WatchDog Software WatchDog	-40 to +85°C	PDIP20
ST62T10M6/HWD ST62T10M6/SWD			Hardware WatchDog Software WatchDog		PSO20
ST62T15B6/HWD ST62T15B6/SWD		20	Hardware WatchDog Software WatchDog	-40 to +85°C	PDIP28
ST62T15M6/HWD ST62T15M6/SWD			Hardware WatchDog Software WatchDog		PSO28
ST62T20B6/HWD ST62T20B6/SWD	**OTP** 4K Bytes	12	Hardware WatchDog Software WatchDog	-40 to +85°C	PDIP20
ST62T20M6/HWD ST62T20M6/SWD			Hardware WatchDog Software WatchDog		PSO20
ST62T25B6/HWD ST62T25B6/SWD		20	Hardware WatchDog Software WatchDog	-40 to +85°C	PDIP28
ST62T25M6/HWD ST62T25M6/SWD			Hardware WatchDog Software WatchDog		PSO28
ST62E20F1/HWD ST62E20F1/SWD	**EPROM** 4K Bytes	12	Hardware WatchDog Software WatchDog	0 to +70°C	FDIP20
ST62E20S1/HWD ST62E20S1/SWD			Hardware WatchDog Software WatchDog		CSO20
ST62E25F1/HWD ST62E25F1/SWD		20	Hardware WatchDog Software WatchDog	0 to +70°C	FDIP28
ST62E25S1/HWD ST62E25S1/SWD			Hardware WatchDog Software WatchDog		CSO28

ST626xB DATASHEET

ST626xB DATASHEET INDEX

Page Number

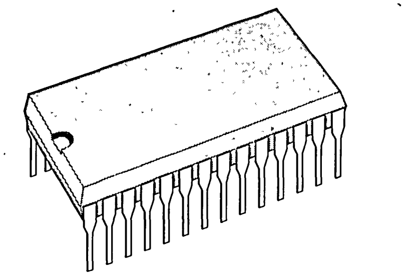
SGS-THOMSON
MICROELECTRONICS

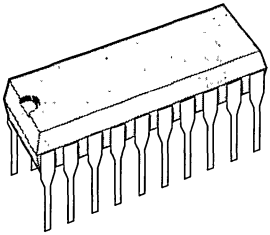
ST6260B
ST6265B

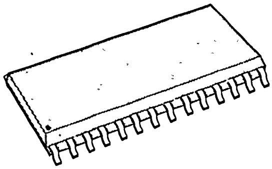
8-BIT HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTO-RELOAD TIMER

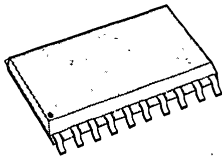
PRELIMINARY DATA

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 3884 bytes
- Data ROM: User selectable size (in program ROM)
- Data RAM: 128 bytes
- EEPROM: 128 bytes
- PDIP20, PSO20 (ST6260B) packages
- PDIP28, PSO28 (ST6265B) packages
- 13/21 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 6/8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (TIMER 1)
- 8 bit Auto-reload Timer with 7-bit programmable prescaler (AR TIMER)
- Digital Watchdog
- 8 bit A/D Converter with up to 7 (ST6260B) and up to 13 (ST6265B) analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator driven by Quartz Crystal, Ceramic resonator or RC network
- User configurable Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The development tool of the ST626xB microcontrollers consists of the ST626xB-EMU emulation and development system connected via a standard RS232 serial line to an MS-DOS Personal Computer


PDIP28


PDIP20


PSO28


PSO20

(Ordering Information at the end of the datasheet)

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. ST6260B Pin Configuration

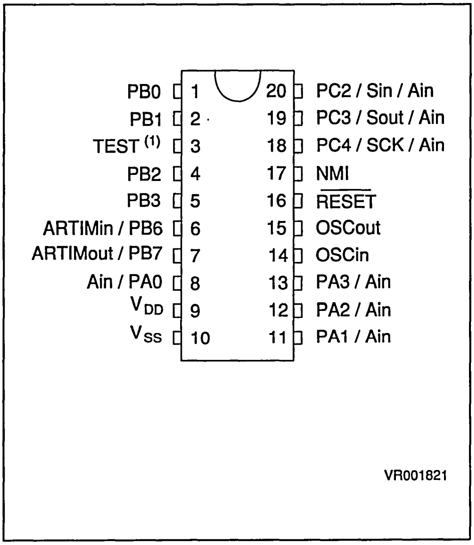
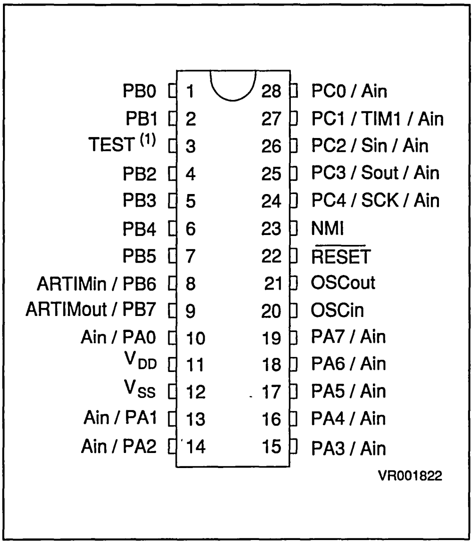
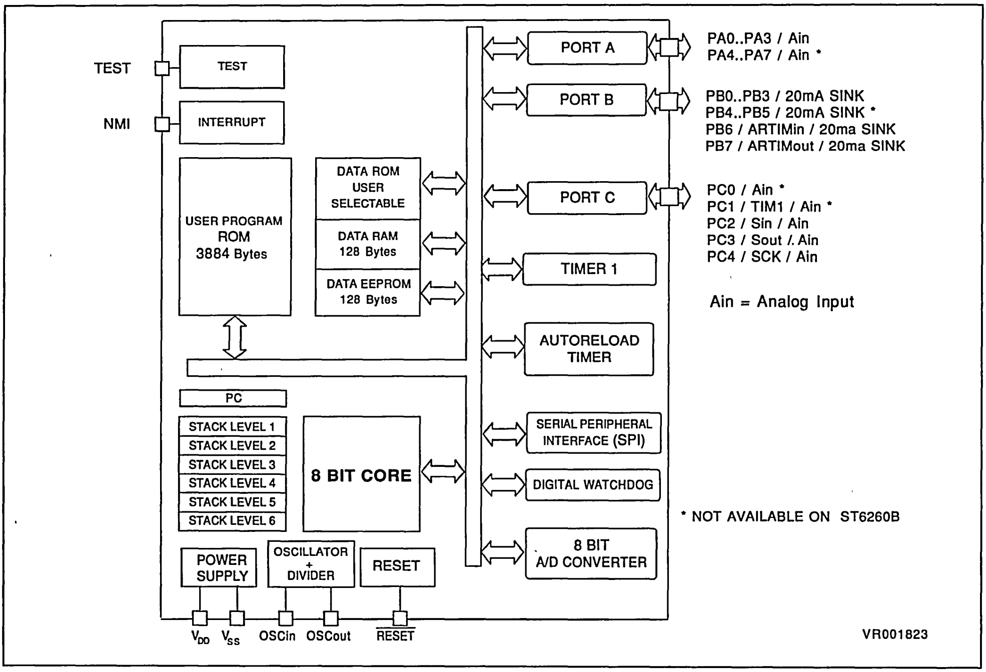


Figure 2. ST6265B Pin Configuration



Note 1: This pin is also the V_{PP} input for EPROM based devices

Figure 3. ST6260B/65B Block Diagram



GENERAL DESCRIPTION

The ST6260B and ST6265B microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells). The macrocells of the ST6260B and ST6265B are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer 1), the 8-bit with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 7 (ST6260B) and up to 13 (ST6265B) analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.

The ST626xB are upward compatible with their ST626x counterparts. They feature in addition to RC network, user configurable Power on Reset delay and an External STOP Mode Control option to enlarge the range of power consumption/safety trade-offs.

ST6260B and ST6265B are well suited for automotive, appliance and industrial applications. The ST62E60 and ST62E65B EPROM versions are available for prototypes and low-volume production; also OTP versions are available.

PIN DESCRIPTION

V$_{DD}$ and V$_{SS}$. Power is supplied to the MCU using these two pins. V$_{DD}$ is power and V$_{SS}$ is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. When the QUARTZ/CERAMIC RESONATOR mask option is selected, a quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins. When the RC OSCILLATOR mask option is selected, a resistor must be connected between the pin OSCout and the ground.The oscillator frequency is internally divided by 1, 2 or 4 by a software controlled divider. The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at V$_{SS}$ for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. It is provided with an on-chip pull-up resistor and Schmitt trigger characteristics.

When the option EXTERNAL STOP MODE CONTROL is enabled the NMI pin, in addition, enables the control of how the STOP instruction is processed.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as 1 I/O pin or as analog input for the on-chip A/D converter. This pin is available only on the ST6265B (28 pin version). If programmed to be the TIMER1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.

To use this pin as TIMER 1 output a dedicated bit in the TIMER1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the . To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). PA4-PA7 are not available on ST6260B (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). PB4, PB5 are available only on the ST6265B (28 pin version). When the External STOP Mode Control is disabled, each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving. When the External STOP Mode Control is enabled, PB0 is forced as open drain output. The other lines are unchanged.

PC0-PC4. These 5 lines are organized as one I/O port (C). PC0 and PC1 are not available on ST6260B (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

ST62xx CORE

The core of the ST62xx Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in Figure 5; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST62xx Family core has six registers and three pairs of flags available to the programmer. They are shown in Figure 4 and are explained in the following paragraphs.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at address FFh. Accordingly the ST62xx instruction set can use the accumulator as any other register of the data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode. These registers can be addressed in the data space as RAM locations at

Figure 4. ST62xx Core Programming Model

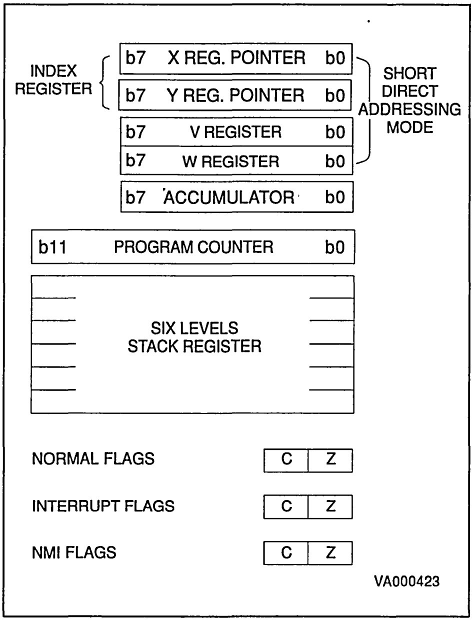
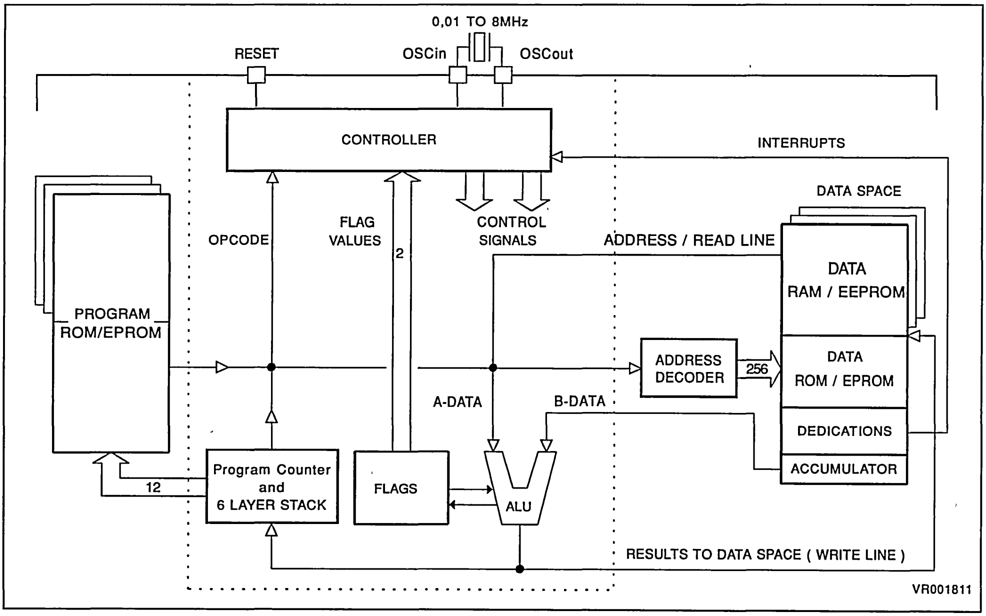


Figure 5. ST62xx Core Block Diagram



ST62xx CORE (Continued)

addresses 80h (X) and 81h (Y). They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST62xx instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at addresses 82h (V) and 83h (W). They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST62xx instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. Nevertheless, if the program space contains more than 4096 locations, the further program space can be addressed by using the Program Bank Switch register.

The PC value is incremented, after it is read the address of the current instruction. To execute relative jumps the PC and the offset are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

- JP (Jump) instruction . . PC= Jump address
- CALL instruction . . . . PC= Call address
- Relative Branch Instructions.PC= PC ± offset
- Interrupt . . . . PC= Interrupt vector
- Reset . . . . PC= Reset vector
- RET & RETI instructions PC= Pop (stack)
- Normal instruction . . . . PC= PC + 1

Flags (C, Z)

The ST62xx core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI, ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST62xx core uses the pair of flags that correspond to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST62xx core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. It should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The flags are not cleared during the context switching and so remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

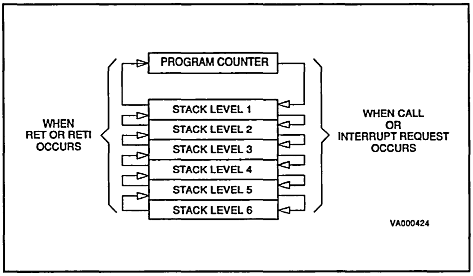
The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

The switching between the three sets of flags is automatically performed when an NMI, an interrupt or a RETI instructions occurs. As the NMI mode is automatically selected after the reset of the MCU, the ST62xx core uses at first the NMI flags.

Stack

The ST62xx core includes true LIFO hardware stack that eliminates the need for a stack pointer. The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When a subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is popped back into the previous level. These two operating modes are described in Figure 6. Since the accumulator, as all other data space registers, is not stored in this stack the handling of these registers should be performed inside the subroutine. The stack pointer will remain in its deepest position if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

Figure 6. Stack Operation



MEMORY SPACES

The MCU operates in three different memory spaces: program space, data space, and stack space. A description of these spaces is shown in the following figures.

Program Space

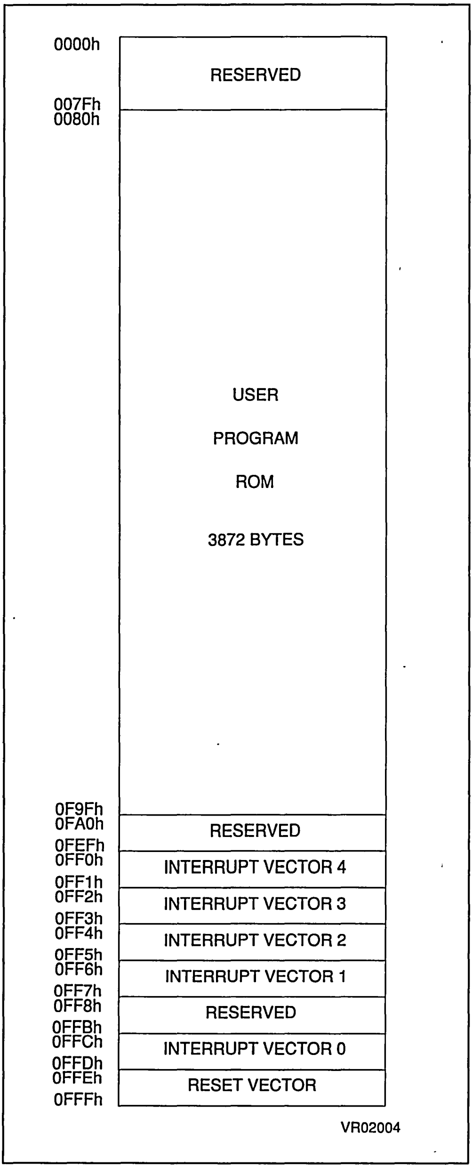
The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and the user vectors. It is addressed by the 12-bit Program Counter register (PC register) and so the ST62xx core can directly address up to 4K bytes of Program Space. ST62 devices with more than 4K ROM use ROM banked program memory (not available on ST6260B, ST6265B).

The ST6260B,65B program space can be protected against external reading of the ROM contents when the READOUT PROTECTION mask option is selected. If this option is selected, the user can blow a dedicated fuse on the silicon by applying a high voltage at V_{PP}, (see detailed information in the "Electrical Specification").

Note:

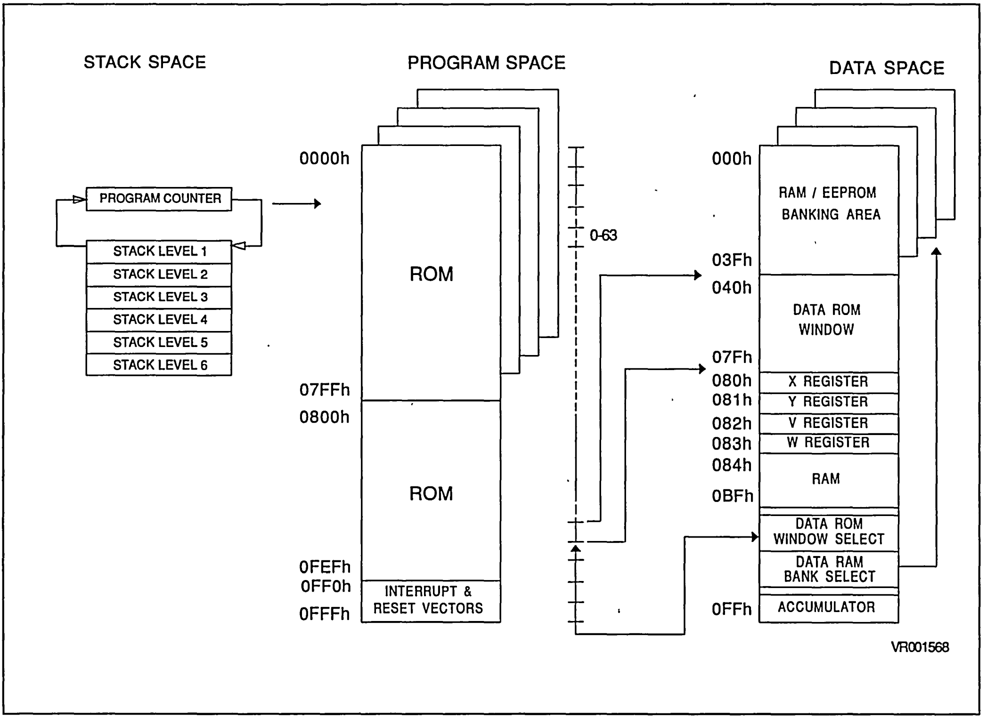
Once the fuse is blown, it is no longer possible, even for SGS-THOMSON, to gain access to the ROM contents. Returned parts with blown fusecan therefore not be accepted.

Figure 7. ST6260B/65B Program ROM Memory Map



MEMORY SPACES (Continued)

Figure 8. Memory Addressing Description Diagram



MEMORY SPACES (Continued)

Data Space

The instruction set of the ST62xx core operates on a specific space, named Data Space, that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM and EEPROM memory, ST62xx core/peripheral registers, and read-only data such as constants and look-up tables.

Data ROM. All the read-only data is physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory contains consequently the program to be executed, the constants and the look-up tables needed for the program.

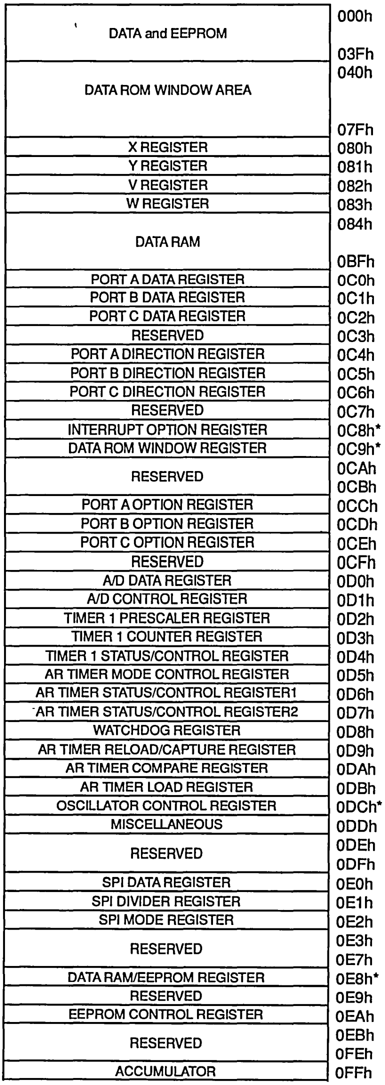
The locations of Data Space in which the different constants and look-up tables are addressed by the ST62xx core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory .

Data RAM/EEPROM. The ST6260B/65B offer 128 bytes of data RAM memory and 128 bytes of EEPROM. 64 bytes of RAM are directly addressed in data space in the range 080h-0BFh (static space). The additional RAM and EEPROM are addressed using the banks of 64 bytes located between addresses 00h and 3Fh.

Stack Space

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

Figure 9. ST6260B/65B Data Memory Space



DATA and EEPROM	000h 03Fh
DATA ROM WINDOW AREA	040h 07Fh
X REGISTER	080h
Y REGISTER	081h
V REGISTER	082h
W REGISTER	083h
DATA RAM	084h 0BFh
PORT A DATA REGISTER	0C0h
PORT B DATA REGISTER	0C1h
PORT C DATA REGISTER	0C2h
RESERVED	0C3h
PORT A DIRECTION REGISTER	0C4h
PORT B DIRECTION REGISTER	0C5h
PORT C DIRECTION REGISTER	0C6h
RESERVED	0C7h
INTERRUPT OPTION REGISTER	0C8h*
DATA ROM WINDOW REGISTER	0C9h*
RESERVED	0CAh 0CBh
PORT A OPTION REGISTER	0CCh
PORT B OPTION REGISTER	0CDh
PORT C OPTION REGISTER	0CEh
RESERVED	0CFh
A/D DATA REGISTER	0D0h
A/D CONTROL REGISTER	0D1h
TIMER 1 PRESCALER REGISTER	0D2h
TIMER 1 COUNTER REGISTER	0D3h
TIMER 1 STATUS/CONTROL REGISTER	0D4h
AR TIMER MODE CONTROL REGISTER	0D5h
AR TIMER STATUS/CONTROL REGISTER1	0D6h
AR TIMER STATUS/CONTROL REGISTER2	0D7h
WATCHDOG REGISTER	0D8h
AR TIMER RELOAD/CAPTURE REGISTER	0D9h
AR TIMER COMPARE REGISTER	0DAh
AR TIMER LOAD REGISTER	0DBh
OSCILLATOR CONTROL REGISTER	0DCh*
MISCELLANEOUS	0DDh
RESERVED	0DEh 0DFh
SPI DATA REGISTER	0E0h
SPI DIVIDER REGISTER	0E1h
SPI MODE REGISTER	0E2h
RESERVED	0E3h 0E7h
DATA RAM/EEPROM REGISTER	0E8h*
RESERVED	0E9h
EEPROM CONTROL REGISTER	0EAh
RESERVED	0EBh 0FEh
ACCUMULATOR	0FFh

* WRITE ONLY REGISTER

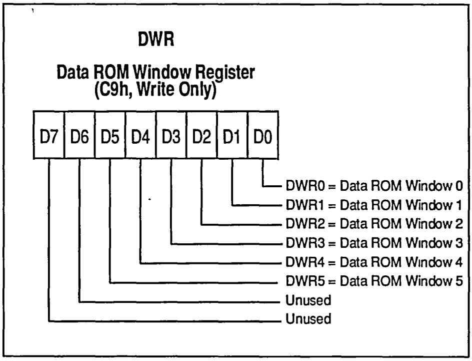
MEMORY SPACES (Continued)

Data Window register (DWR)

The Data ROM window is located from address 040h to address 7Fh in the Data space. It allows the direct reading of 64 consecutive bytes located anywhere in the ROM memory between the addresses 0000h and 0FFFh. All the bytes of the ROM memory can be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data Window register (DWR register, location C9h).

The DWR register can be addressed like a RAM location in the Data Space at the address C9h, nevertheless it is a write only register that cannot be accessed with single-bit operations. This register is used to move the 64-byte read-only data window (from the 40h address to 7Fh address of the Data Space) up and down the ROM memory of the MCU in steps of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 least significant bits of the register address given in the instruction (as least significant bits) and the content of the DWR register (as most significant bits, see Figure 9). So when addressing location 40h of dataspace, and 0 is loaded in the DWR register, the phisycal addressed location in ROM is 00h. The DWR register is not cleared at reset, therefore it must be written to before the first access to the Data ROM window area.

Figure 11. Data ROM Window Register



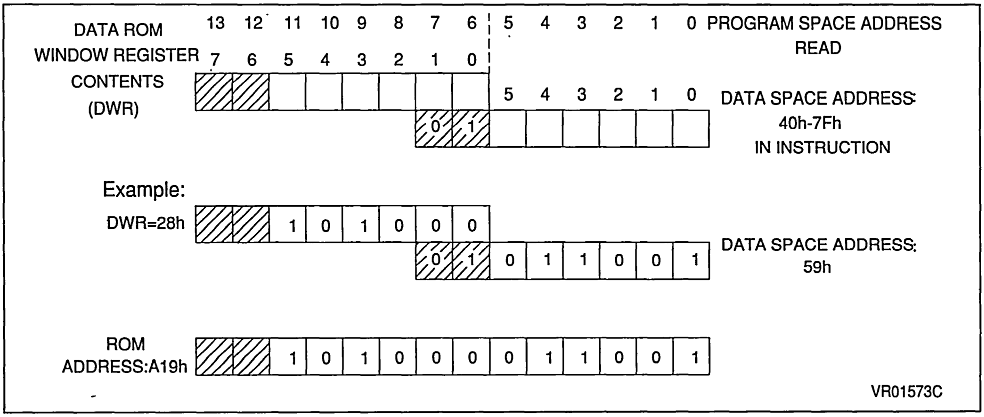
D7-D6. Not used.

DWR5-DWR0. These are the Data ROM Window bits that correspond to the upper bits of the data ROM space.

This register is undefined on reset. Neither read nor single bit instructions may be used to address this register.

Note: Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in the interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to the DWR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR is not affected.

Figure 10. Data ROM Window Memory Addressing



MEMORY SPACES (Continued)

Data RAM/EEPROM Bank Register (DRBR)

The selection of the bank is made by programming the Data RAM Bank Switch register (DRBR register) located at address E8h of the Data Space according to Table 1. No more than one bank should be set at a time.

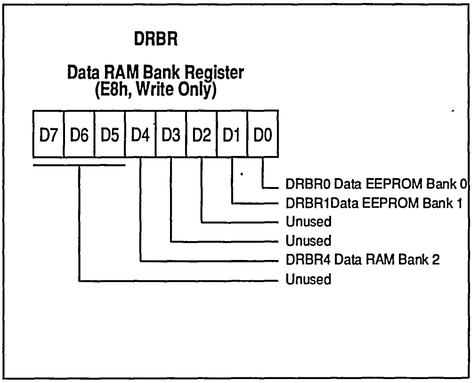
The DRBR register can be addressed like a RAM location in the Data Space at the address E8h; nevertheless it is a write only register that cannot be accessed with single-bit operations. This register is used to select the desired 64-byte RAM/EEPROM bank of the Data Space. The number of bank has to be loaded in the DRBR register and the instruction has to point to the selected location as if it was in bank 0 (from 00h address to 3Fh address).

This register is not cleared during the MCU initialization, therefore it must be written before the first access to the Data Space bank region. Refer to the Data Space description for additional information. The DRBR register is not modified when an interrupt or a subroutine occurs.

Table 1. Data RAM Bank Register Set-up

DRBR Value	Selection
00h	None
01h	EEPROM Page 0
02h	EEPROM Page 1
10h	RAM Page 2
Other	Reserved

Figure 12. Data RAM/EEPROM Bank Register



D7-D5. These bits are not used.

DRBR4. This bit, when set, selects RAM page 2.

D3-D2. These bits are not used.

DRBR1. This bit, when set, selects EEPROM page 1.

DRBR0. This bit, when set, selects EEPROM page 0.

Notes:

Care is required when handling the DRBR register as it is write only. For this reason, it is not allowed to change the DRBR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to DRBR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DRBR is not affected.

In DRBR Register, *only 1 bit must be set.* Otherwise two or more pages are enabled in parallel, producing errors.

MEMORY SPACES (Continued)

EEPROM Description

The data space of ST62xx family from 00h to 3Fh is paged as described in Table 2. The ST6260B/65B has 128 bytes of EEPROM located in two pages of 64 bytes (page 0 and 1).

The EEPROM is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. Once selected through the Data RAM Bank Register, the active EEPROM page is controlled by the EEPROM Control Register (EECTL) located at address EAh. E20FF bit of the EECTL register must be cleared to "0" prior to any write or read access to the EEPROM. If no bank is selected or if E2OFF is set, any access is meaningless.

Programming must be enabled by setting bit E2ENA of register EECTL.

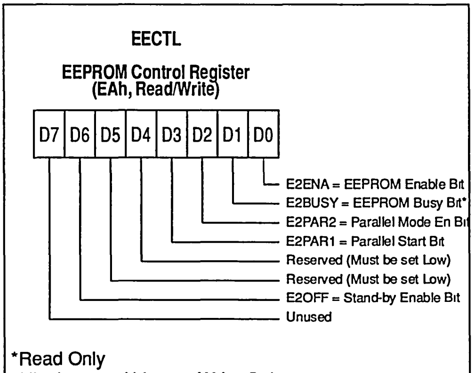
Bit E2BUSY of EECTL register is set to 1 when the EEPROM is performing a programming cycle. Any access to the EEPROM when E2BUSY is set to 1 is meaningless.

Provided E2OFF and E2BUSY are cleared to 0, an EEPROM location is read like any other data location, also in term of access time.

Writing the EEPROM can work in two modes: Byte Mode (BMODE) and Parallel Mode (PMODE). BMODE is the normal way to use the EEPROM and consists in accessing one byte at a time. PMODE consists in simultaneously programing 8 bytes of the same row.

D7. Not Used

Figure 13. EEPROM Control Register


EECTL
EEPROM Control Register
(EAh, Read/Write)
D7
D6
D5
D4
D3
D2
D1
D0
E2ENA = EEPROM Enable Bit
E2BUSY = EEPROM Busy Bit*
E2PAR2 = Parallel Mode En Bi
E2PAR1 = Parallel Start Bit
Reserved (Must be set Low)
Reserved (Must be set Low)
E2OFF = Stand-by Enable Bit
Unused

*Read Only
All other used bits are Write Only

E2OFF. *WRITE ONLY.* If this bit is set the EEPROM is disabled (any access will be meaningless) and the power consumption of the EEPROM is reduced to the lowest values.

D5, D4. Reserved, must be set to zero.

E2PAR1. *WRITE ONLY.* Once in Parallel Mode, as soon as the user software sets the E2PAR1 bit the parallel writing of the 8 adjacent registers will start. It is internally reset at the end of the programming procedure. Note that less than 8 bytes can be written; the undefined bytes are unaffected by the parallel programming.

E2PAR2. *WRITE ONLY.* This bit must be set by the user program in order to perform parallel programming (more than one byte at a time). If E2PAR2 is set and the parallel start bit (E2PAR1) is low, up to 8 adjacent bytes can be written at maximum speed, the contents being stored in volatile registers. These 8 adjacent bytes are considered as a row, whose address lines A7, A6, A5, A4, A3 are fixed while A2, A1 and A0 are the changing bits. E2PAR2 is automatically reset at the end of any parallel programming procedure. It can be reset by the user software before starting the programming procedure, leaving the EEPROM registers unchanged.

E2BUSY. *READ ONLY.* This bit is automatically set by the EEPROM control logic when the EEPROM is in programming mode. The user program should test it before any read or write EEPROM operation; any attempt to access the EEPROM while the busy bit is set will be aborted and the writing procedure in progress completed.

E2ENA. *WRITE ONLY.* This bit enables programming of the EEPROM cells. It must be set to one before any write into the EEPROM register. Any attempt to write to the EEPROM when E2ENA is low is meaningless and will not trigger a write cycle.

This register is cleared at reset.

Notes:

The data to write has to be written directly at the address that it will have inside the EEPROM space. There is no buffer memory between the data RAM and the EEPROM spaces.

When the EEPROM is busy (E2BUSY = "1") EECTL can not be accessed in write mode, it is only possible to read the status of E2BUSY. This implies that as long as the EEPROM is busy, it is not possible to change the status of the EEPROM Control Register. EECTL bits 4 and 5 are reserved and must never be set to "1".

Care is required when handling the EECTL register as some bits are write only. For this reason, it is not allowed to change the EECTL contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in interrupt service routine, an image of this

MEMORY SPACES (Continued)

Table 2. EEPROM Parallel Write Row Structure

Byte	0	1	2	3	4	5	6	7	Dataspace addresses. Banks 0 and 1.
ROW7									38h-3Fh
ROW6									30h-37h
ROW5									28h-2Fh
ROW4									20h-27h
ROW3									18h-1Fh
ROW2									10h-17h
ROW1									08h-0Fh
ROW0									00h-07h

Up to 8 bytes in each row may be programmed at the same time in Parallel Write mode

register must be saved in a RAM location, and each time the program writes to EECTL it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the EECTL is not affected.

Additional Notes on Parallel Mode. If the user wishes to perform parallel programming, the first action should be to set the E2PAR2 bit to one. From this time the EEPROM will be addressed in writing, the ROW address will be latched and it will be possible to change it only at the end of the programming procedure or by resetting E2PAR2 without programming the EEPROM. After the ROW address latching the ST62xx can "see" only one EEPROM row (the selected one) and any attempt to write or read other rows will produce errors. Do not read the EEPROM while E2PAR2 is set.

As soon as E2PAR2 bit is set, the 8 volatile ROW latches are cleared. From this moment the user can load data in the whole ROW or in a subset. Setting E2PAR1 will modify the EEPROM registers corresponding to the ROW latches accessed after E2PAR2. For example, if the software sets E2PAR2 and accesses the EEPROM by writing to addresses 18h, 1Ah, 1Bh and then sets E2PAR1, these three registers will be modified at the same time; the remaining bytes will be unaffected. Note that E2PAR2 is internally reset at the end of the programming procedure. This implies that the user must set E2PAR2 bit between two parallel programming procedures. Note that if the user tries to set E2PAR1 while E2PAR2 is not set there will not be any programming procedure and the E2PAR1 bit will be unaffected. Consequently E2PAR1 bit cannot be set if E2ENA is low. E2PAR1 can be affected by the user to set it, only if E2ENA and E2PAR2 bits are also set to one.

TEST MODE

For normal operation the TEST pin must be held low when reset is active. An on-chip 100kΩ pull-down resistor is internally connected to the TEST pin.

INTERRUPTS

The ST62xx core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 1). When a source provides an interrupt request, and the request processing is also enabled by the ST62xx core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction).
Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The ST6260B and ST6265B microcontrollers have eight different interrupt sources associated to five interrupt vectors as it is described in table below.

Table 3. Interrupt Vector/Source Relationship

Interrupt Source	Vector	Vector Address
NMI	Interrupt vector #0	(FFCh, FFDh)
Port A & B	Interrupt vector #1	(FF6h, FF7h)
Port C & SPI	Interrupt vector #2	(FF4h, FF5h)
AR TIMER	Interrupt vector #3	(FF2h, FF3h)
TIMER1 & ADC	Interrupt vector #4	(FF0h, FF1h)

Interrupt Vectors Description

The ST62xx core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines in the static page of the Program Space.

– The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at addresses FFCh,FFDh in the Program Space. On ST6260B and ST6265B this vector is associated with the external falling edge sensitive interrupt pin (NMI).

– The interrupt vector located at addresses FF6h, FF7h is named interrupt vector #1. It is associated with Port A and Port B pins. It can be programmed by software either in the falling edge detection mode or in the low level sensitive detection mode according to the code loaded in the Interrupt Option Register (IOR).

– The interrupt vector located at addresses FF4h, FF5h is named interrupt vector #2. It is associate with Port C pins and the SPI peripheral can be programmed by software either in the falling edge detection mode or in the positive edge detection mode according to the code loaded in the Interrupt Option Register (IOR).

– The interrupt vector located at addresses FF2h, FF3h is named interrupt vector #3. It is associated with the AR TIMER peripheral.

– The interrrupt vector loaded at address FF0h, FF1h is named interrupt vector #4. It is associated with the TIMER 1 and the A/D converter peripherals.

All the on-chip peripherals have an interrupt request flag bit (TMZ for timer, EOC for A/D), this bit is set to one when the device wants to generate an interrupt request and a mask bit (ETI for timer, EAI for A/D) that must be set to one to allow the transfer of the flag bit to the core.

Interrupt Priority

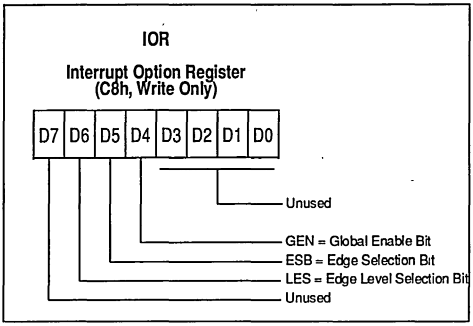
The non-maskable interrupt request NMI has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the four other interrupts can not interrupt each other. If more than one interrupt request are pending, they are processed by the ST62xx core according to their priority level: vector #1 has the higher priority while vector #4 the lower.
The priority of each interrupt source is fixed.

INTERRUPT (Continued)

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8h) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the address C8h, nevertheless it is a write-only register that cannot be accessed with single-bit operations. The operating modes of the external interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 5 and 6 of the IOR register.

Figure 14. Interrupt Option Register



D7. D3-D0 These bits are not used.

LES. Level/Edge Selection Bit. When this bit is set to one, the interrupt #1 (Port A, B lines) is low level sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

ESB. Edge Selection Bit. When this bit is set to one, the interrupt #2 (Port C lines) is positive edge sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

GEN. Global Enable Interrupt. When this bit is set to one, all the interrupts are enabled. When this bit is cleared to zero all the interrupts (excluding NMI) are disabled.

This register is cleared on reset.

Table 4. Interrupt Option Register Description

GEN	SET	Enable all interrupts
	CLEARED	Disable all interrupts
ESB	SET	Rising edge mode on interrupt input #2
	CLEARED	Falling edge mode on interrupt input #2
LES	SET	Level-sensitive mode on interrupt input #1
	CLEARED	Falling edge mode on interrupt input #1
OTHERS	NOT USED	

External Interrupts Operating Modes

The NMI interrupt is associated to the NMI pin of the ST6260B/65B. The interrupt request is generated by a falling edge applied to the NMI pin. The NMI interrupt pin signal is latched and is automatically reset by the core at the beginning of the non-maskable interrupt service routine. An on-chip pull-up resistor and a Schmitt trigger are available at pin NMI.

The two interrupt sources associated with the falling/rising edge mode of the external interrupt pins (Ports A and B vector #1, Ports C vector #2) are connected to two internal latches. Each latch is set when a falling/rising edge occurs and is cleared when the associated interrupt routine is started. So, the occurrence of an external interrupt request is stored: a second interrupt, that occurs during the processing of the first one, will be processed as soon as the first one has been finished (if there is not an higher priority interrupt request). If more than one interrupt occurs during the processing of the first one, these other interrupt requests will be lost.

The storage of the interrupt requests is not available in the level sensitive detection mode. To be taken into account, the low level must be present on the interrupt pin when the core samples the line after the execution of the instructions. At the end of each instruction the core tests the interrupt lines and if there is a pending interrupt request the next instruction is not executed and the related interrupt routine is executed.

Note:

When GEN bit is low, the NMI interrupt is active but cannot cause a wake up from STOP/WAIT modes.

INTERRUPT (Continued)

Interrupt Procedure. The interrupt procedure is very similar to a call procedure, indeed the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event, the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

The following list summarizes the interrupt procedure:

ST62xx actions

- Interrupt detection
- The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (or the NMI flags)
- The value of the PC is stored in the first level of the stack
- The normal interrupt lines are inhibited (NMI still active)
- First internal latch is cleared
- The related interrupt vector is loaded in the PC.

User actions

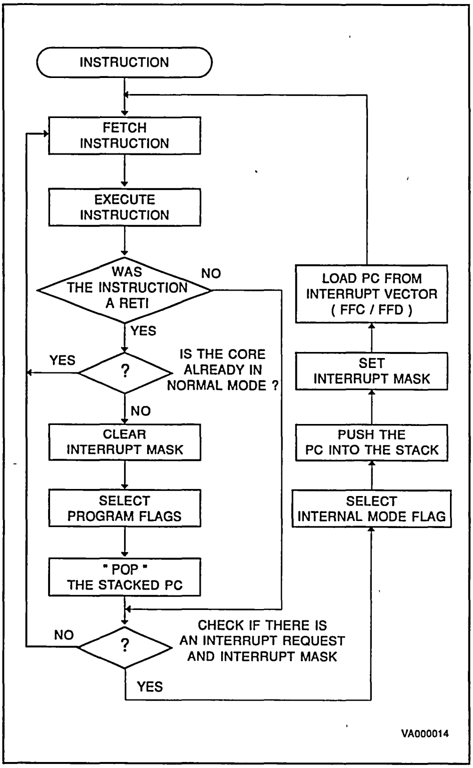
- User selected registers are saved inside the interrupt service routine (normally on a software stack)
- The source of the interrupt is found by polling (if more than one source is associated to the same vector) the interrupt flag of the source.
- Interrupt servicing
- Return from interrupt (RETI)

ST62xx actions

- Automatically the ST62xx core switches back to the normal flags (or the interrupt flags) and pops the previous PC value from the stack

The interrupt routine begins usually by the identification of the device that has generated the interrupt request (by polling). The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack. After the RETI instruction execution, the core carries out the previous actions and the main routine can continue.

Figure 15. Interrupt Processing Flow-Chart


INSTRUCTION
FETCH INSTRUCTION
EXECUTE INSTRUCTION
WAS THE INSTRUCTION A RETI
NO
YES
?
IS THE CORE ALREADY IN NORMAL MODE ?
YES
NO
CLEAR INTERRUPT MASK
SELECT PROGRAM FLAGS
" POP " THE STACKED PC
?
CHECK IF THERE IS AN INTERRUPT REQUEST AND INTERRUPT MASK
NO
YES
LOAD PC FROM INTERRUPT VECTOR (FFC / FFD)
SET INTERRUPT MASK
PUSH THE PC INTO THE STACK
SELECT INTERNAL MODE FLAG
VA000014

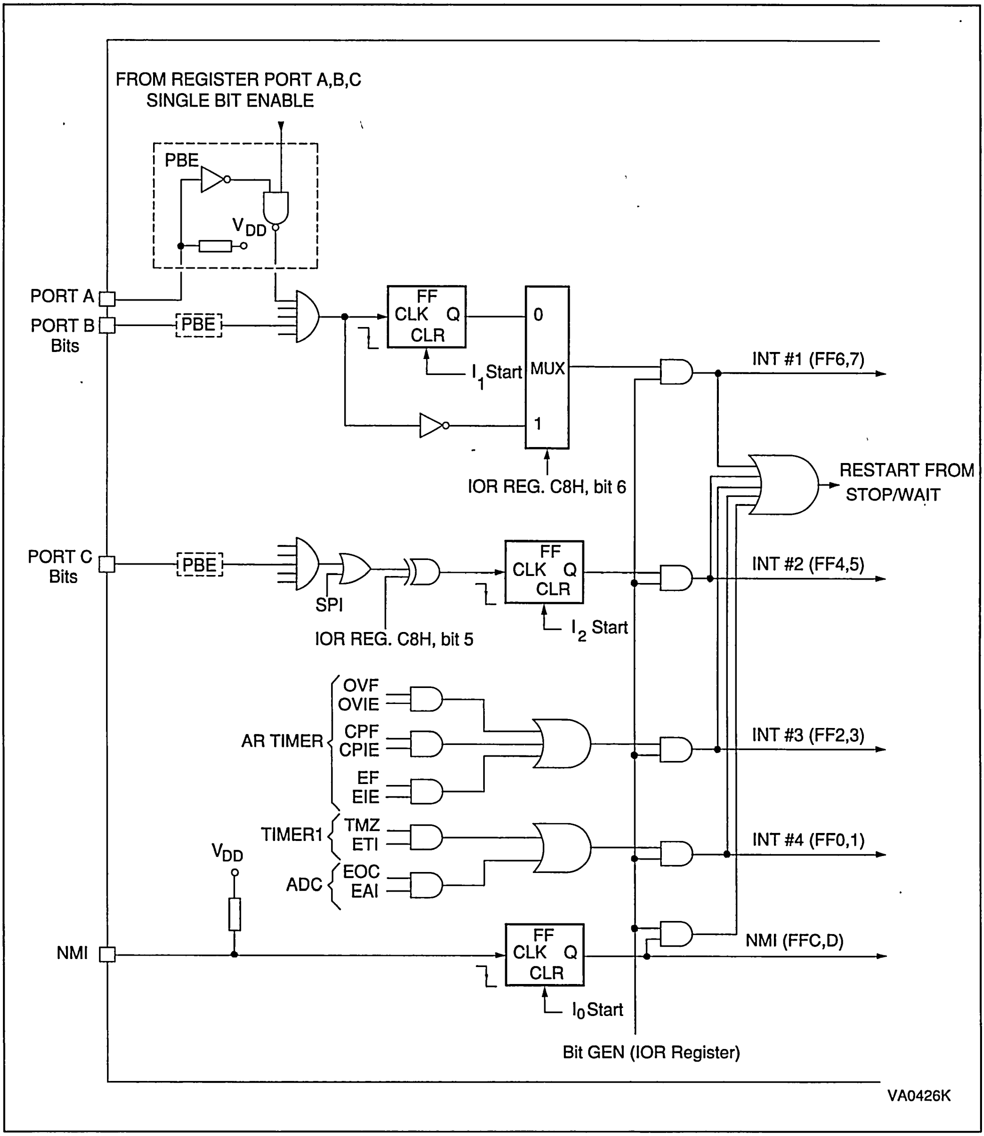
INTERRUPT (Continued)

Table 5. Interrupt Requests and Mask Bits

Peripheral	Register	Register Address	Mask bit	Masked Interrupt Source	Interrupt Vector
GENERAL	IOR	C8h	GEN	All sources, excluding NMI	
TIMER 1	TSCR1	D4h	ETI	TMZ: TIMER 1 Overflow	Vector 4
A/D CONVERTER	ADCR	D1h	EAI	EOC: End of Conversion	Vector 4
AR TIMER	ARMC	D5h	OVIE CPIE EIE	OVF: AR TIMER Overflow CPF: Successful compare EF: Active edge on ARTIMin	Vector 3
SPI	SPIMOD	E2h	SPIE	SPIF: End of Transmission	Vector 2
Port PAn	ORPA-DRPA	C0h-C4h	ORPAn-DRPAn	PAn pin	Vector 1
Port PBn	ORPB-DRPB	C1h-C5h	ORPBn-DRPBn	PBn pin	Vector 1
Port PCn	ORPC-DRPC	C2h-C6h	ORPCn-DRPCn	PCn pin	Vector 2

INTERRUPT (Continued)

Figure 16. Interrupt Circuit Diagram



RESET

The ST6260B/65B can be reset in three ways: by the external reset input ($\overline{\text{RESET}}$) tied low, by power-on reset and by the digital Watchdog peripheral

RESET Input

The $\overline{\text{RESET}}$ pin can be connected to a device of the application board in order to restart the MCU during its operation. The activation of the $\overline{\text{RESET}}$ pin may occur in the RUN, WAIT or STOP mode. This input has to be used to reset the MCU internal state and provide a correct start-up procedure. The pin is active low and has a schmitt trigger input. The internal reset signal is generated by adding a delay to the external signal. Therefore even short pulses at the $\overline{\text{RESET}}$ are accepted, provided V_{DD} has finished its rising phase and the oscillator is running correctly (normal RUN or WAIT modes). The MCU is kept in the Reset state as long as the $\overline{\text{RESET}}$ pin is held low.

If the $\overline{\text{RESET}}$ activation occurs in the RUN or WAIT mode, the processing of the program is stopped (in RUN mode only) and the Input/Outputs are placed in input with pull-up resistors. When the level on the $\overline{\text{RESET}}$ pin becomes high, the initialization sequence is executed just after the internal delay.

If a $\overline{\text{RESET}}$ pin activation occurs in the STOP mode, the oscillator starts and all the inputs/outputs are configured in input with pull-up resistors. When the level of the $\overline{\text{RESET}}$ pin becomes high, the initialization sequence is started just after the internal delay.

Power-on Reset

The function of the POR consists in waking up the MCU during the power-on sequence. At the beginning of this sequence, the MCU is configured in the Reset state: every Input/Output port is configured in input with pull-up resistor and no instruction is executed. When the power supply voltage becomes sufficient, the oscillator starts to operate, nevertheless an internal delay is generated to allow the oscillator to be completely stabilized before the execution of the first instruction. The initialization sequence is executed just after the internal delay.

The internal delay is generated by a mask option configurable on-chip counter. When the 2048 CYCLES DELAY option is selected the internal reset is released 2048 cycles of the oscillator after the external reset is released. When the 32768 CYCLES DELAY option is selected, the delay is 32768 cycles of the oscillator.

Note:

To have a correct start-up, the user should take care that the internal reset is not released before the VDD level is sufficient to allow MCU operation at the chosen frequency (see Recommended Operating Conditions).

A proper reset signal for slow rising V_{DD} can be generally provided by an external RC network connected at pin $\overline{\text{RESET}}$.

RESET (Continued)

Watchdog Reset

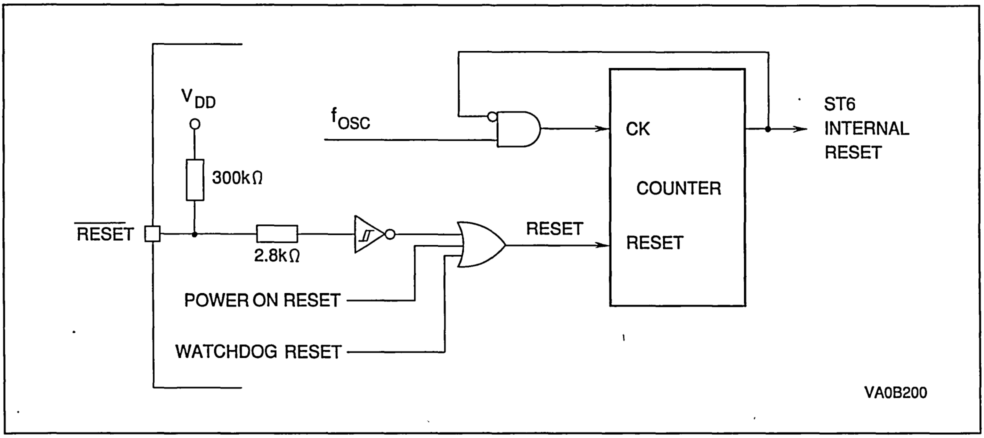
The ST6260B and ST6265B provide an on-chip watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed, preventing the end-of-count being reached, the internal reset is activated. This, in particular, resets the watchdog. The MCU restarts as with normal reset from $\overline{\text{RESET}}$ pin including the internal delay.

Application Notes

An external resistor between V_{DD} and reset pin is not required because an internal pull-up device is provided.

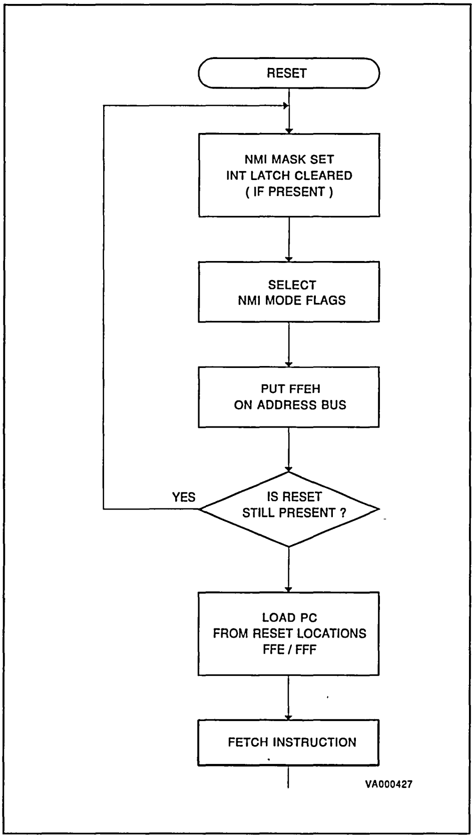
The POR device operates in a dynamic manner in the way that it brings about the initialization of the MCU when it detects a dynamic rising edge of the V_{DD} voltage. The typical detected threshold is about 2 volts, but the actual value of the detected threshold depends on the way in which the V_{DD} voltage rises up. The POR device *DOES NOT* allow the supervision of a static or slowly rising or falling edge of the V_{DD} voltage.

Figure 17. Reset Circuit



RESET (Continued)

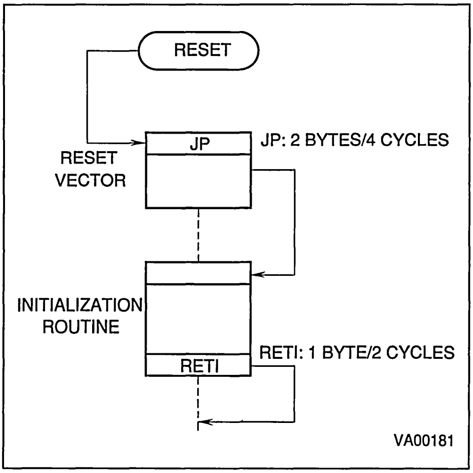
Figure 18. Reset and Interrupt Processing Flow-Chart



MCU Initialization Sequence

When a reset occurs the stack is reset to the program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEh & FFFh). A jump instruction to the beginning of the program has to be written into these locations. After a reset a NMI is automatically activated so that the core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine the ST62xx will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced

Figure 19. Restart Initialisation Program Flow-Chart



RESET (Continued)

Table 6. Reset Value

Register	Address	Value	Comment
Oscillator Control Register	0DCh	00h	$f_{INT} = f_{OSC}$; user must set bit3 to 1
EEPROM Control Register	0EAh		EEPROM disabled
Port Data Registers	0C0h to 0C2h		
Port Direction Register	0C4h to 0C6h		I/O are Input with pull-up
Port Option Register	0CCh to 0CEh		I/O are Input with pull-up
Interrupt Option Register	0C8h		Interrupt disabled
TIMER 1 Status/Control	0D4h		TIMER 1 disabled
AR TIMER Mode Control Register	0D5h		AR TIMER stopped
AR TIMER Status/Control 1 Register	0D6h		
AR TIMER Status/Control 2 Register	0D7h		
AR TIMER Compare Register	0DAh		
Miscellaneous Register	0DDh		SPI output not connected to PC3
SPI Registers	0E0h to 0E2h		SPI disabled
X, Y, V, W, Register	080h to 083h	Undefined	As written if programmed
Accumulator	0FFh		
Data RAM	084h to 0BFh		
Data RAM Page Register	0E8h		
Data ROM Window Register	0C9h		
EEPROM	00h to 03Fh		
A/D Result Register	0D0h		
AR TIMER Load Register	0DBh		
AR TIMER Reload/Capture Register	0D9h		
TIMER 1 Counter Register	0D3h	FFh	
TIMER 1 Prescaler Register	0D2h	7Fh	Max count loaded
Watchdog Counter Register	0D8h	FEh	
A/D Control Register	0D1h	40h	A/D in Standby

WAIT & STOP MODES

The WAIT and STOP modes have been implemented in the ST62xx core in order to reduce the consumption of the product when the latter has no instruction to execute. These two modes are described in the following paragraphs

WAIT Mode

The MCU goes into the WAIT mode as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a "software frozen" state where the core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, but where the peripherals are still working.

The WAIT mode can be used when the user wants to reduce the consumption of the MCU when it is idle, while not losing count of time or monitoring of external events. The oscillator is not stopped in order to provide a clock signal to the peripherals. The TIMER 1 and counting may be enabled as well as both Timer interrupts before entering the WAIT mode; this allows the WAIT mode to be left when timer interrupt occurs. The above explanation related to the timers applies also to the A/D converter and the SPI.

If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU enters a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behavior depends on the state of the ST62xx core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case is described in the following paragraphs. In any case, the ST62xx core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

If the Watchdog is disabled the STOP mode is available. When in STOP mode the MCU is placed in the lowest power consumption mode. In this operating mode the microcontroller can be considered as being "frozen", no instruction is executed, the oscillator is stopped, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, and the ST62xx core waits for the occurrence of an interrupt request or Reset activation to output from the STOP state. The interrupt request can be issued by a pin. or by an externally clocked timer.

If the exit from the STOP mode is performed with a general RESET (by the activation of the external pin) the MCU will enter a normal reset procedure as described in the RESET chapter. The case of an interrupt depends on the state of the ST62xx core before the initialization of the STOP sequence and also of the kind of the interrupt request that is generated.

This case will be described in the following paragraphs. In any case, the ST62xx core generates a delay after the occurrence of the interrupt request in order to wait the complete stabilization of the oscillator before the execution of the first instruction.

Exit from WAIT and STOP Modes

The following paragraphs describe the output procedure of the ST62xx core from WAIT and STOP modes when an interrupt occurs (not a RESET). It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) before the start of the WAIT or STOP sequence, but also of the type of the interrupt request that is generated.

Normal Mode. If the ST62xx core was in the main routine when the WAIT or STOP instruction has been executed, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the STOP or the WAIT instruction is executed if no other interrupts are pending.

Not Maskable Interrupt Mode. If the STOP or WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs: the instruction that follows the STOP or the WAIT instruction is executed and the ST62xx core is still in the non-maskable interrupt mode even if another interrupt has been generated.

WAIT & STOP MODES (Continued)

Normal Interrupt Mode. If the ST62xx core was in the interrupt mode before the initialization of the STOP or WAIT sequence, it outputs from the stop or wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non-maskable interrupt, the non-maskable routine is processed at first. Then the routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core remains in the normal interrupt mode.

Notes:

To reach the lowest power consumption during RUN or WAIT modes, the user software must take care of:

- selecting 4 as ratio of the Oscillator divider.
- configuring unused I/O as input without pull-up with well defined logic levels.
- placing the A/D converter in its power down mode by clearing the PDS bit in the A/D control register before entering the STOP instruction.
- putting the EEPROM on-chip memory in stand-by mode by setting the E2OFF bit in EEPROM Control Register to one.
- setting bit D3 of the Oscillator Control Register to one.
- stopping all external clocks (TIMER 1, AR TIMER and SPI).

When the watchdog is active (independent of its mode), the STOP instruction is deactivated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

If all the interrupt sources are disabled (including NMI if GEN is low), the restart of the MCU can only be done by a Reset activation. The WAIT and STOP instructions are not executed if an enabled interrupt request is pending.

ON-CHIP CLOCK OSCILLATOR

The ST6260B/65B on-chip oscillator has been designed to require a minimum of external components and to reduce the oscillator power consumption.

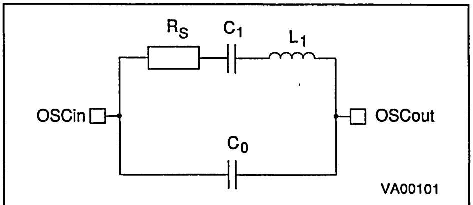
A quartz crystal, a ceramic resonator, an RC network or an external signal may be used to generate a system clock with various stability/cost tradeoffs. The clock generator options connection methods are shown in Figure 22.

The oscillator is configured by mask option. When the CRYSTAL/RESONATOR option is selected, it must be used with a quartz crystal, a ceramic resonator or an external signal. To use the oscillator with an RC network, the RC NETWORK option must be selected.

A programmable divider is provided in order to adjust the internal clock of the micro (core and peripherals) to the best power consumption/performance trade-off. The Division Ratio is selected through the Oscillator Control Register located at address 0DCh.

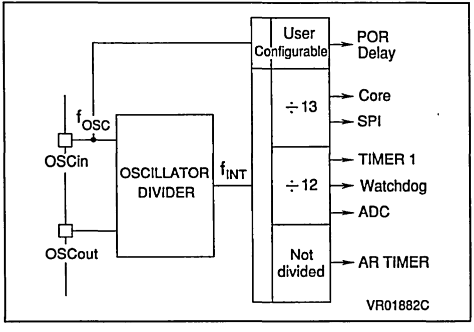
The internal frequency is directly used to clock the AR TIMER. It is further divided by 12 to produce the TIMER 1, the A/D converter and the Watchdog clock and by 13 for the core and SPI clock.

Figure 20. Crystal Parameters



Crystal Parameters: AT-cut Parallel Resonance Crystal
C0 = Parallel Resonance Capacitance

Figure 21. Internal Clock Circuits



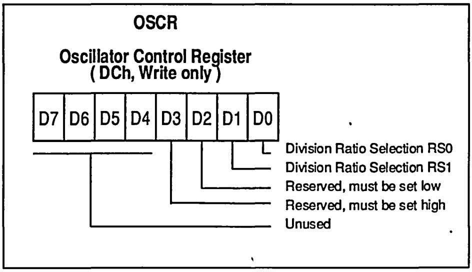
ON-CHIP CLOCK OSCILLATOR (Continued)

With a 8MHz external frequency, the fastest machine cycle is therefore 1.625µs.

The machine cycle is the smallest unit needed to execute any operation (i.e.increment the program counter). An instruction may need two, four, or five machine cycles to be executed.

Oscillator Control Register

Figure 22. Oscillator Control Registers


OSCR
Oscillator Control Register
(DCh, Write only)
D7
D6
D5
D4
D3
D2
D1
D0
Division Ratio Selection RS0
Division Ratio Selection RS1
Reserved, must be set low
Reserved, must be set high
Unused

D7-D4. These bits are not used.

D3. Reserved - Cleared at Reset. THIS BIT MUST BE SET TO 1 BY USER PROGRAM to achieve lowest power consumption.

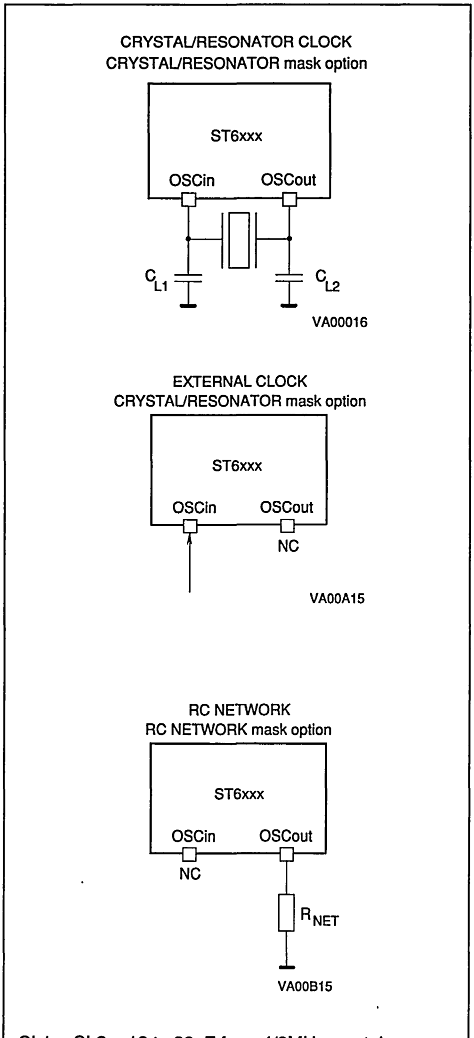
D2. Reserved. Must be kept low.

RS1-RS0. These bits select the division ratio of the Oscillator Divider in order to generate the internal frequency. The following selections are available:

RS1	RS0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	4

Note : Care is required when handling the OSCR register as some bits are write only. For this reason, it is not allowed to change the OSCR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to OSCR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the OSCR is not affected.

Figure 23. Oscillator Connection



CL1 = CL2 = 12 to 22pF for a 4/8MHz crystal

INPUT/OUTPUT PORTS

The ST6260B and ST6265B microcontroller have respectively 13 and 21 Input/Output lines that can be individually programmed either in the input mode or the output mode with the following software selectable options:

- Input without pull-up and without interrupt
- Input with pull-up and with interrupt
- Input with pull-up without interrupt
- Analog inputs (PA0-PA7, PC0-PC4)
- Timer 1 I/O line (PC1, not available on ST6260B)
- AR Timer I/O lines (PB6, PB7)
- SPI control signals (PC2-PC4)
- Push-pull output
- Standard Open drain output
- 20mA Open drain output PB lines.

The lines are organized in three Ports (Port A, B and C).

Each port occupies 3 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data, Direction and Option registers are associated with the PA0 line of Port A).

The three DATA registers (DRA, DRB, DRC), are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port data registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related option registers, to select the different input mode options.

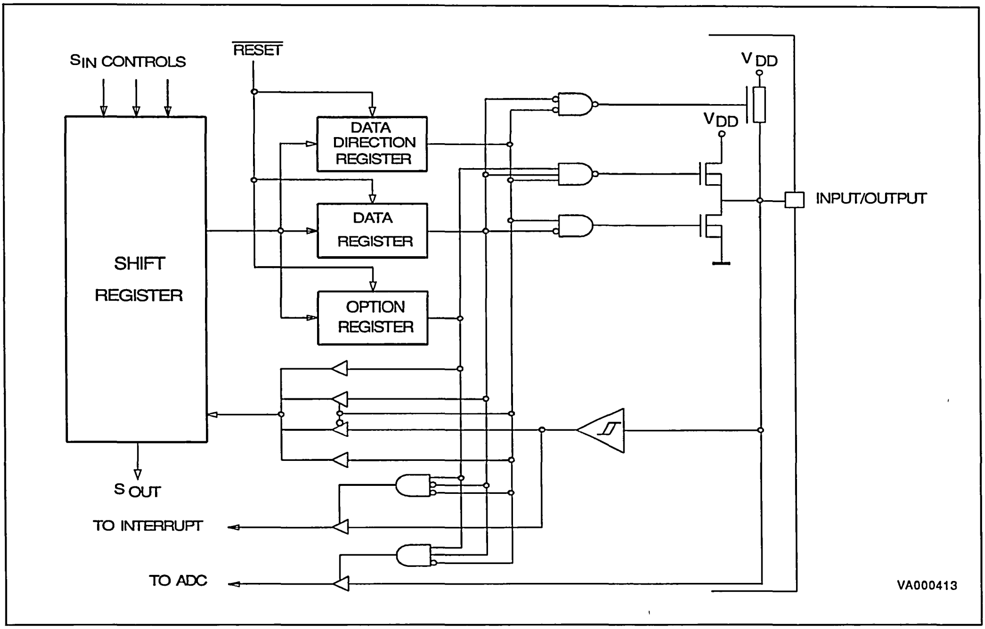
Single-bit operations on I/O registers are possible but care is necessary because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired change of the input configuration.

The three Data Direction registers (DDRA, DDRB and DDRC) allow the selection of the data direction of each pin (input or output).

The three Option registers (ORA, ORB and ORC) are used to select the different port options available both in input and in output mode.

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up/no-interrupt is selected on all the pins, thus avoiding pin conflicts.

Figure 24. I/O Port Block Diagram



INPUT/OUTPUT PORTS (Continued)

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations.

This is achieved by writing the relevant bit in the data (DR), data direction register (DDR) and option registers (OR). Table 7 shows all the port configurations that can be selected by user software.

Input Option Description

Interrupt Option. All the input lines can be individually connected by software to the interrupt lines of the ST62xx core according to the codes programmed in the OR and DR registers. The pins of Port A and B are "ORed" and are connected to the interrupt associated to the vector #1. Pins of ports C are "ORed" with the SPI interrupt line and connected to interrupt vector #2. The interrupt modes (falling edge sensitive, rising edge sensitive) can be selected by software for each port by programming the IOR register.

Analog Input Option. The PA0-PA7 and PC0-PC4 pins can be configured to be analog inputs according to the codes programmed in the OR and DR registers. These analog inputs are connected to the on-chip 8-bit Analog to Digital Converter. *ONLY ONE* pin should be programmed as analog input at a time, otherwise the selected inputs will be shorted.

Figure 25. I/O Port Data Registers

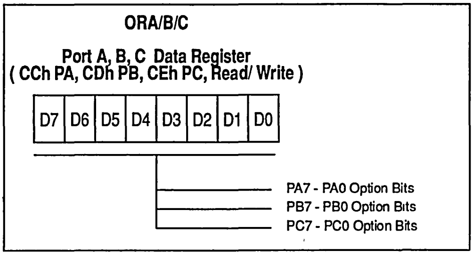


Figure 26. I/O Port Data Direction Registers

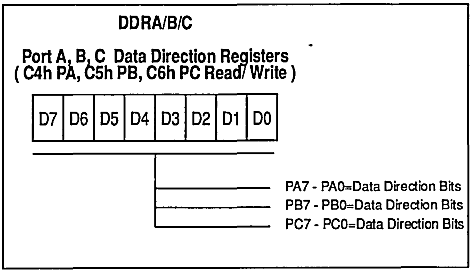
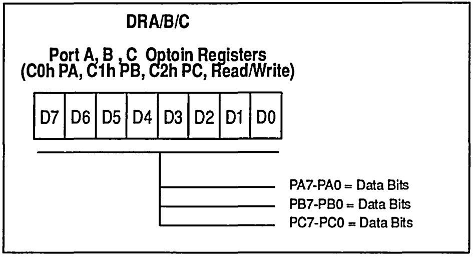

DDRA/B/C
Port A, B, C Data Direction Registers
(C4h PA, C5h PB, C6h PC Read/ Write)
D7
D6
D5
D4
D3
D2
D1
D0
PA7 - PA0=Data Direction Bits
PB7 - PB0=Data Direction Bits
PC7 - PC0=Data Direction Bits

Figure 27. I/O Port Option Registers



Note: For complete coding explanation refer to Table 7

Table 7. I/O Port Options Selection

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt (Reset state)
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up, with interrupt
0	1	1	Input	No pull-up, no interrupt (Port B pins)
			Input	Analog input (Ports A and C pins)
1	0	X	Output	Open-drain output (20mA sink current for Port B pins)
1	1	X	Output	Push-pull output (20mA sink current for Port B pins)

Notes: X. Means don't care.

INPUT/OUTPUT PORTS (Continued)

Timer 1 Alternate function Option.

When bit TOUT of register TSCR1 is low, pin PC1/Timer 1 is configured through the port registers as any standard pin of Port B. It is in addition connected to the Timer 1 input for Gated and Event counter modes. When bit TOUT of register TSCR1 is high, pin PC1/Timer 1 is forced as Timer 1 output, independently of the port registers configuration.

AR Timer Alternate function Option

When bit PWMOE of register ARMC is low, pin ARTIMout/PB7 is configured as any standard pin of port B through the port registers. When PWMOE is high, ARTIMout/PB7 is the PWM output, independently of the port registers configuration.

ARTIMin/PB6 is connected to the AR Timer input. It is configured through the port registers as any standard pin of port B. To use ARTIMin/PB6 as AR Timer input, it must be configured as input through DDRB.

SPI Alternate function Option

PC2/PC4 are used as standard I/O as long as bit SPCLK of the SPI Mode Register is kept low.

When PC2/Sin is configured as input, it is automatically connected to the SPI shift register input, independent of the state at SPCLK.

PC3/SOUT is configured as SPI push-pull output by setting bit 0 of the Miscellaneous Register (address DDh), regardless of the state of Port C registers.

PC4/SCK is configured as push-pull output clock (master mode) by programming it as push-pull output through DDRC register and by setting bit SPCLK of the SPI Mode Register.

PC4/SCK is configured as input clock (slave mode) by programming it as input through DDRC register and by clearing bit SPCLK of the SPI Mode Register. With this configuration, PC4 can simultaneously be used as an input.

Note. Switching the I/O ports from one state to another should be done in a way that no unwanted side effects can happen. The recommended safe transitions are shown below. All other transitions are risky and should be avoided during change of operation mode as it is most likely that there will be an unwanted side-effect such as interrupt generation or two pins shorted together by the analog input lines.

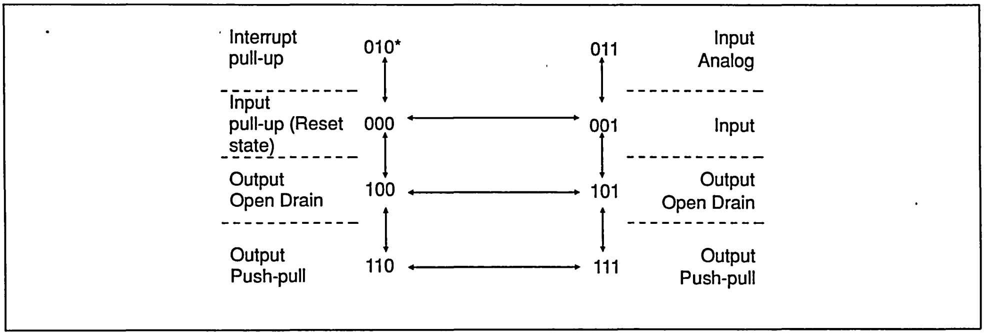
Single bit instructions (SET, RES, JRR and JRS) should be used very carefully with Port A and B data registers because these instructions make an implicit read and write back of the whole addressed register byte. In port input mode however data register address reads from input pins, not from data register latches and data register information in input mode is used to set characteristics of the input pin (interrupt, pull-up, analog input), therefore these characteristics may be unintentionally reprogrammed depending on the state of input pins. As general rule is better to use single bit instructions on data register only when the whole port is in output mode. If input or mixed configuration is needed it is recommended to keep a copy of the data register in RAM. On this copy it is possible to use single bit instructions, then the copy register could be written into the port data register.

```
SET     bit, datacopy
LD      a, datacopy
LD      DRA, a
```

The WAIT and STOP instructions allow the ST62xx to be used in situations where low power consumption is needed. The lowest power consumption is achieved by configuring I/Os in input mode with well-defined logic levels.

The user has to take care not to switch outputs with heavy loads during the conversion of one of the analog inputs in order to avoid any disturbance in the measurement.

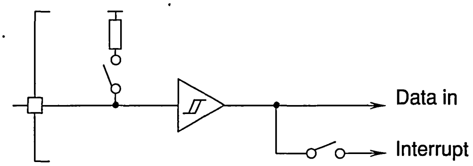
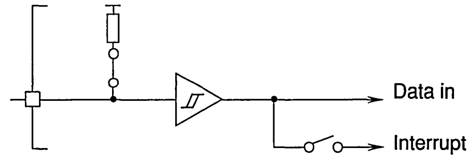
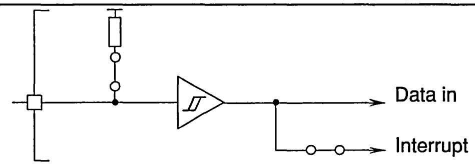
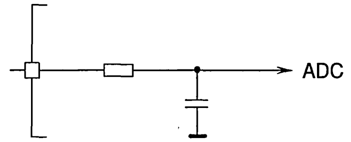
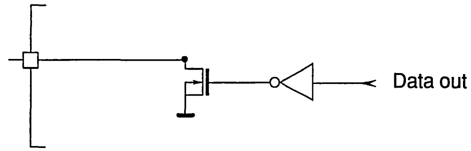
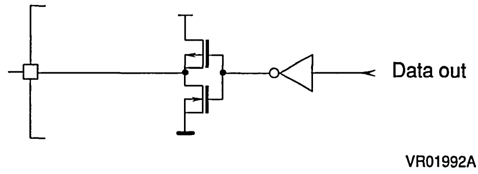
Figure 28. State Transition Diagram for Safe Transitions



Note *. xxx = DDR, OR, DR Bits respectively

INPUT/OUTPUT PORTS (Continued)

Table 8. I/O Port Options Selection

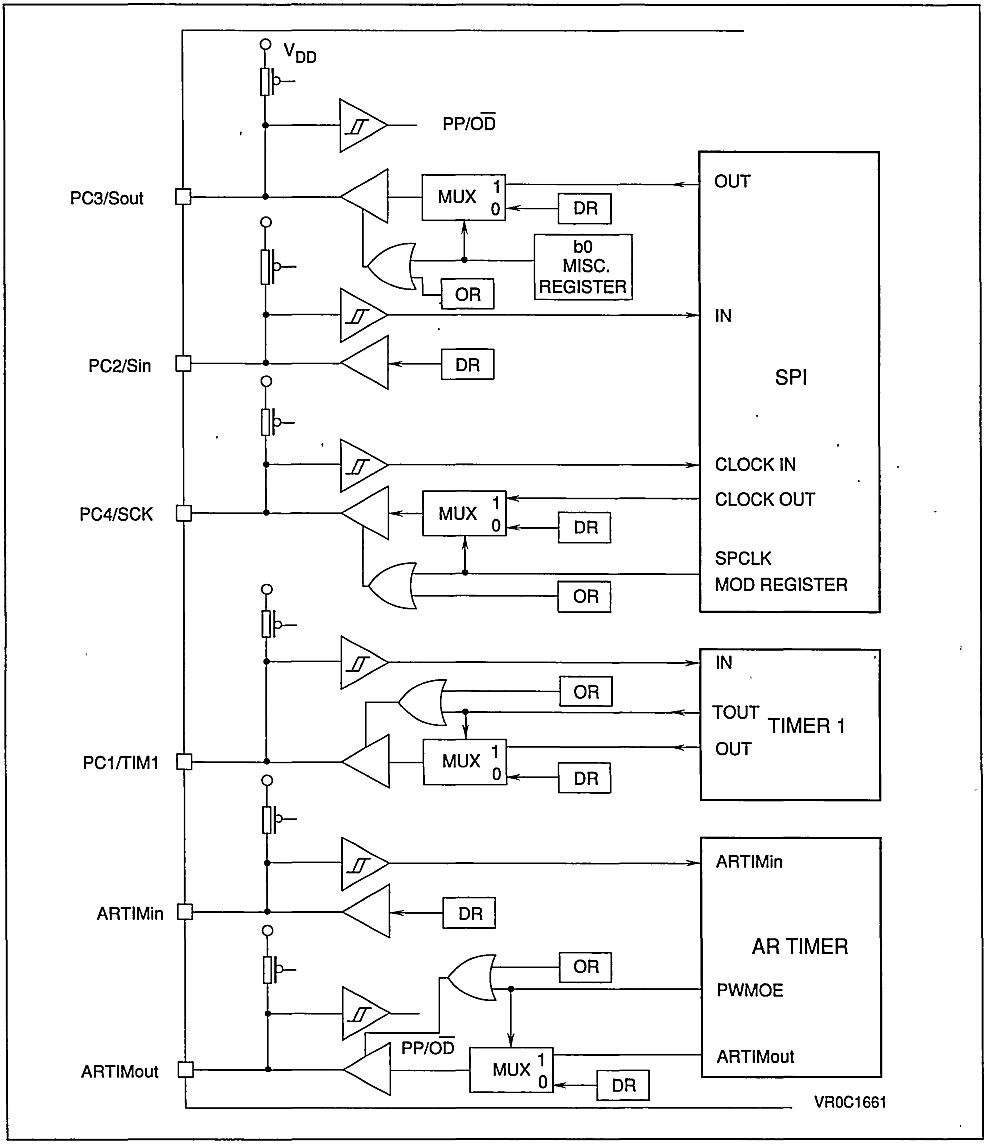
Mode	Available At[1]	Schematic
Input	PA0-PA7 PB0-PB7 PC0-PC4 Sin, SCK ARTIMin, TIM1	
Input with pull up	PA0-PA7 PB0-PB7 PC0-PC4 Sin, SCK ARTIMin, TIM1	
Input with pull up with interrupt	PA0-PA7 PB0-PB7 PC0-PC4 Sin [2], SCK[2] ARTIMin[2], TIM1[2]	
Analog Input	PA0-PA7 PC0-PC4	
Open drain output 5mA Open drain output 20mA	PA0-PA7 PC0-PC4 PB0-PB7	
Push-pull output 5mA Push-pull output 20mA	PA0-PA7 PC0-PC4 TIM1, Sout, SCK PB0-PB7 ARTIMout	

Notes:

1. Provided proper configuration.
2. This configuration is available but should be used with care.

INPUT/OUTPUT PORTS (Continued)

Figure 29. Peripheral Interface Configuration of SPI, Timer 1 and AR Timer



TIMERS

The ST6260B/65B offer two on-chip Timer peripherals named Timer 1 and Auto-reload Timer. Timer 1 consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and control logic that allows configuring the peripheral in three operating modes. The Auto-reload Timer is an 8-bit Timer with Auto-reload, Input Capture and Output Compare capabilities. 4 modes are available for PWM, PLL, time measurement and period measurement.

Timer 1

Figure 30 shows the Timer 1 block diagram. An external Timer pin is available for the user (ST6265B only). The content of the 8-bit counter can be read/written in the Timer/Counter register TCR which is addressed in the data space as a RAM location at addresses D3h. The state of the 7-bit prescaler is read in the PSC register at addresses D2h. The control logic device is managed in the TSCR1 register (addresses D4h) as described in the following paragraphs.

The 8-bit counter is decremented by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (Timer Zero) bit in the TSCR1 is set to one. If the ETI (Enable Timer Interrupt) bit in the TSCR1 is also set to one an interrupt request, associated to interrupt vector #4, is generated. The interrupt service routine then should poll bit TMZ in TSCR1 to determine if the interrupt has been generated by Timer 1 or by the A/D Converter. The Timer 1 interrupt can be used to exit the MCU from the WAIT mode.

The Timer 1 Prescaler input can be the internal clock (after Oscillator Divider) divided by 12 or an external clock at the Timer I/O pin. The prescaler decrements on the rising edge. Depending on the division factor programmed by PS2, PS1 and PS0 bits in TSCR1, the clock input of the timer/counter register is multiplexed to different sources. On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR1. This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC1 is connected to clock input of TCR1, and so on. The prescaler initialize bit PSI in the TSCR1 register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting. The prescaler can be given any value between 0 and 7Fh by writing to addresses D2h, if bit PSI in the TSCR1 register is set to one. The tap of the prescaler is selected using the PS2,PS1,PS0 bits in the control register. Figure 31 shows the Timer 1 working principle.

Timer 1 can be configured in 3 modes using the TOUT and DOUT bits of the TSCR1 register. These modes are Event counter, Gated or Output signal.

The internal Timer I/O can in addition be connected to either the PC1/TIM1 pin or bit DRC1 of the Port C Data Register depending on the configuration of bit DDRC1 of the Port C Data Direction Register. Table 9 summarize the modes of Timer 1.

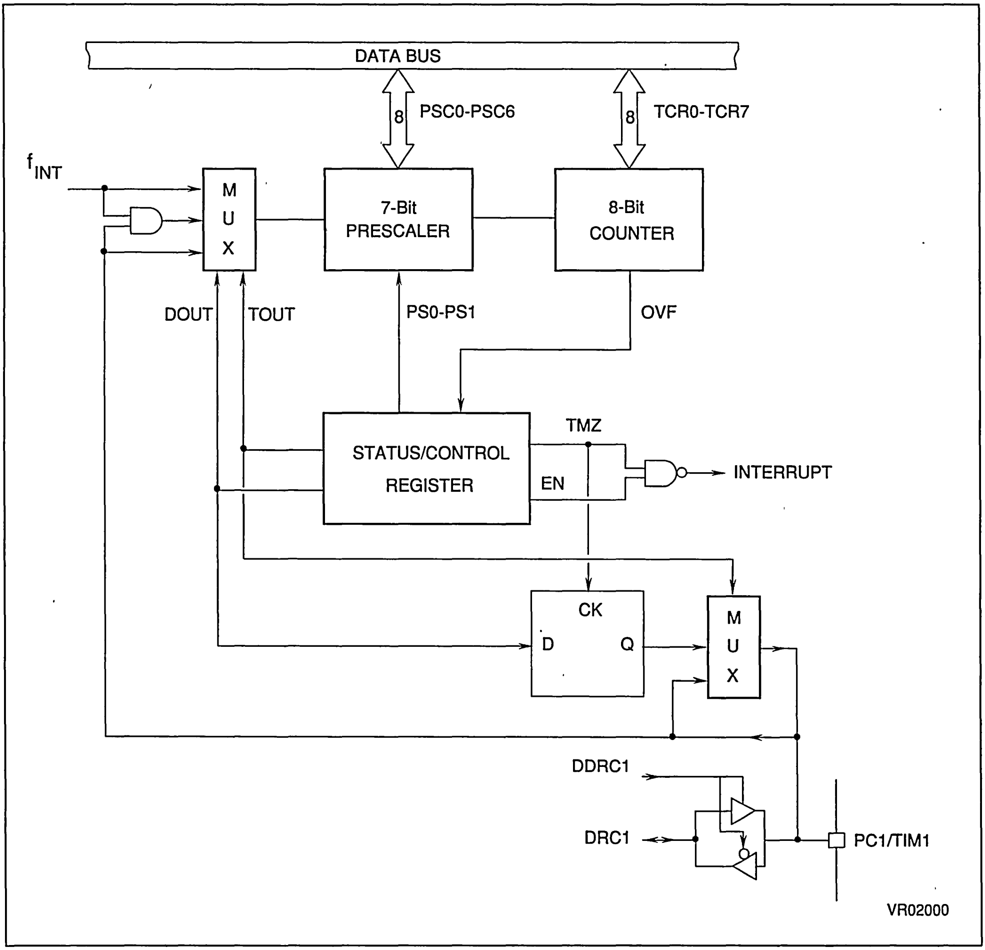
– Event counter: The Prescaler is decremented at each rising edge of the Timer I/O. The Timer I/O is either the PC1/TIM1 pin or the DRC1 bit of the DRC register depending on DDRC1.

– Gated: The Timer 1 is decremented by the Timer clock (f_{INT} divided by 12) when the internal Timer I/O is held high. The Timer I/O is either pin PC1/TIM1 or the DDRC1 bit of register DDRC.

– Output signal: The PC1/TIM1 pin is connected to the DOUT latch and is configured as output regardless of DOUT and DDRC1 bits. The low to high transition of bit TMZ (when counter reaches 00h) is used to latch the data previously stored in DOUT and pass it to the PC1/TIM1 through the Timer I/O. This operating mode allows signal generation.

TIMERS (Continued)

Figure 30. Timer 1 Peripheral Block Diagram



TIMERS (Continued)

Timer 1 Interrupt

If the software controlled ETI (Enable Timer Interrupt) bit is set, when the counter decrements to zero, the TMZ bit in the TSCR register is set to one and an interrupt request associated to interrupt vector #4 is generated.

Since only one interrupt vector is available for both Timer 1 and the A/D Converter, the interrupt service routine should determine from which source the interrupt came by polling the TMZ bit and the EOC bit of the A/D Converter Control Register.

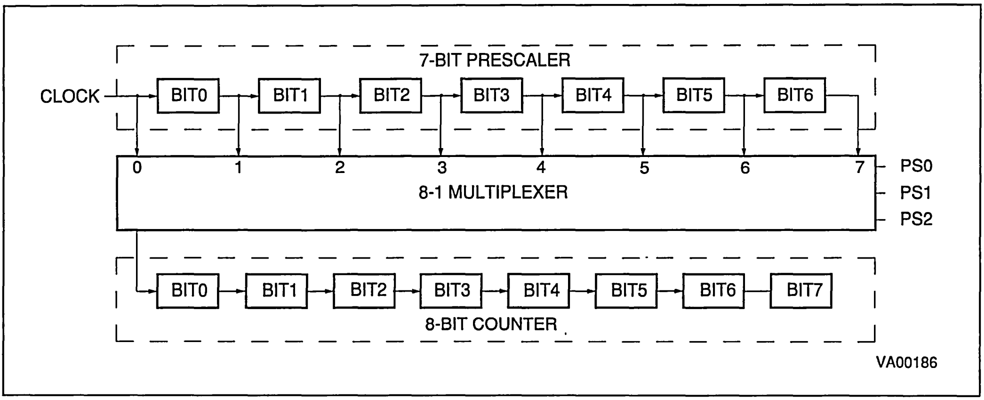
Notes:

TMZ is set when the counter reaches 00h; however, it may be set by writing 00h in the TCR1 register or setting bit 7 of the TSCR1 register. TMZ bit must be cleared by user software when servicing the Timer 1 interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFh while the 7-bit prescaler is loaded to 7Fh , and the TSCR1 register is cleared which means that Timer 1 is stopped and the Timer 1 interrupt is disabled.

If the Timer 1 is programmed in output mode, DOUT bit is transferred to the TIM1 pin when TMZ is set to one (by software or due to counter decrement). When TMZ is high, the latch is transparent and DOUT is copied to the timer pin. When TMZ goes low, DOUT is latched.

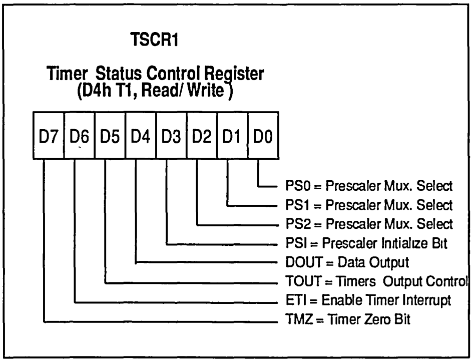
A write to the TCR1 register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR1 register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00h again. The values of the TCR1 and the PSC1 registers can be read accurately at any time.

Figure 31. Timer 1 Working Principle



TIMERS (Continued)

Figure 32. Timer Status Control Register


TSCR1
Timer Status Control Register
(D4h T1, Read/ Write)
D7
D6
D5
D4
D3
D2
D1
D0
PS0 = Prescaler Mux. Select
PS1 = Prescaler Mux. Select
PS2 = Prescaler Mux. Select
PSI = Prescaler Initialize Bit
DOUT = Data Output
TOUT = Timers Output Control
ETI = Enable Timer Interrupt
TMZ = Timer Zero Bit

TMZ. Low-to-high transition indicates that the timer count register has decremented to zero. This bit must be cleared by user software before starting with a new count.

ETI. This bit, when set, enables the timer interrupt request (vector #4). If ETI="0" the timer interrupt is disabled. If ETI="1" and TMZ="1" an interrupt request is generated.

TOUT. When low, this bit selects an input mode for the Timer I/O pin. When high the output mode is selected.

DOUT. If Timer 1 is in Output mode, DOUT is the data sent to the PC1/TIM1 pin when TMZ goes high. DOUT enables discrimination between Event Counter and Gated modes if TOUT is low.

PSI. Used to initialize the prescaler and inhibit its counting. When PSI="0" the prescaler is set to 7Fh and the counter is inhibited. When PSI="1" the prescaler is enabled to count downwards. As long as PSI="0" both counter and prescaler are not running.

PS2, PS1, PS0. These bits select the division ratio of the prescaler register.

Table 9. Prescaler Division Factors

PS2	PS1	PS0	Divided by	PS2	PS1	PS0	Divided by
0	0	0	1	1	0	0	16
0	0	1	2	1	0	1	32
0	1	0	4	1	1	0	64
0	1	1	8	1	1	1	128

Figure 33. Timer Counter Register

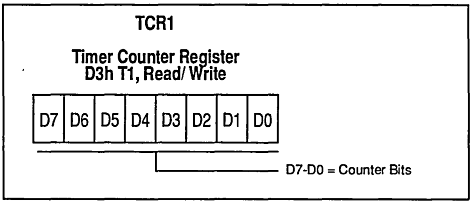


Figure 34. Prescaler Register

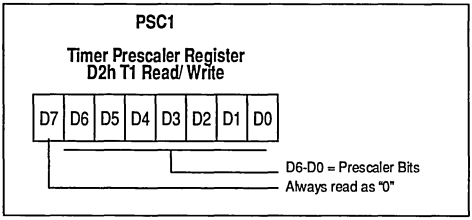


Table 10. Modes of Timer 1

TOUT	DOUT	DDRC1	Mode	Timer I/O
0	0	0	Event Counter	PC1/TIM1
0	0	1	Event Counter	DRC1
0	1	0	Gated	PC1/TIM1
0	1	1	Gated	DRC1
1	X	X	Output	PC1/TIM1

TIMERS (Continued)

Auto-reload Timer

The Auto-reload Timer (AR Timer) on-chip peripheral consists of an 8-bit timer/counter (AR COUNTER) with compare and capture/reload capabilities and a 7-bit prescaler with a clock multiplexer enabling the clock input to be selected as f_{INT}, $f_{INT}/3$ or external clock. One Mode Control Register (AR MODE), two Status Control Registers (ARSC0, ARSC1), an output pin (ARTIMout/PB7) and an input pin (ARTIMin/PB6) allow the Auto-reload Timer to be used in 4 modes:

- Auto-reload (PWM generation),
- Output compare and reload on external event (PLL),
- Input capture and output compare for time measurement.
- Input capture and output compare for period measurement.

The AR Timer can be used to wake the MCU from WAIT mode with either an internal or an external clock. It also can be used to wake the MCU from STOP mode if used with an external clock provided at pin ARTIMin. A Load register allows the program to read and write the counter on the fly.

AR Timer Description

The AR COUNTER is an 8-bit up-counter incremented on the clock input rising edge. It is loaded from the ReLoad/Capture Register REL/CAP (address D9h) for auto-reload or capture operations as well as for initialization. Direct access to the AR COUNTER is not possible, however by reading/writing the Load Register AR LOAD (address DBh) it is possible to read/write the TC counter content.

The AR Timer input clock is either the internal clock (from Oscillator Divider), the internal clock divided by 3 or the ARTIMin pin. Selection between these clock sources is made through the AR Multiplexer by bits CC0-CC1 of Register ARSC1. The output of the AR Multiplexer feeds the AR Prescaler, ARPSC. ARPSC is a software programmable 7-bit prescaler. Programming of ARPSC is performed by the AR Prescaler Multiplexer AR MUX which selects one of the 8 available taps of the prescaler outputs under the control of PSC0-PSC2 in the AR Mode Control Register (address D5h). So the division factor of PSC prescaler can be set to 2^n (where n = 0, 1,..7).

The clock input to the ARTC counter is enabled by bit TEN (Timer Enable) in the AR Mode Control Register. When TEN is cleared to "0" the TC counter is stopped and the prescaler and counter contents are frozen. When the TEN bit is set to "1" the TC counter runs at the rate of the selected clock source. TC is cleared after system reset.

The ARTC counter can also be initialized by writing into the load register ARLR, which causes also the immediate copy of the value into the ARTC counter regardless of whether ARTC is running or not. Initialization of ARTC, in both ways, will also clear the ARPSC in order to start counting from a known state.

Each interrupt generated by the AR Timer operating modes is associated to interrupt vector #3.

Timer Operating Modes

Four different operating modes are available for the AR Timer:

Auto-reload Mode with PWM Generation. This mode allows a Pulse Width Modulated signal to be generated on the ARTIMout output pin with minimum Core processing time used.

ARTC is a free running 8-bit counter fed by the ARPSC prescaler output and is incremented on every rising edge of the clock signal.

When a counter overflow occurs the ARTC counter is automatically reloaded with the contents of the Reload/Capture Register (REL/CAP, address D9h) while ARTIMout is set. When the counter reaches the value contained in the compare register ARCP, ARTIMout is reset.

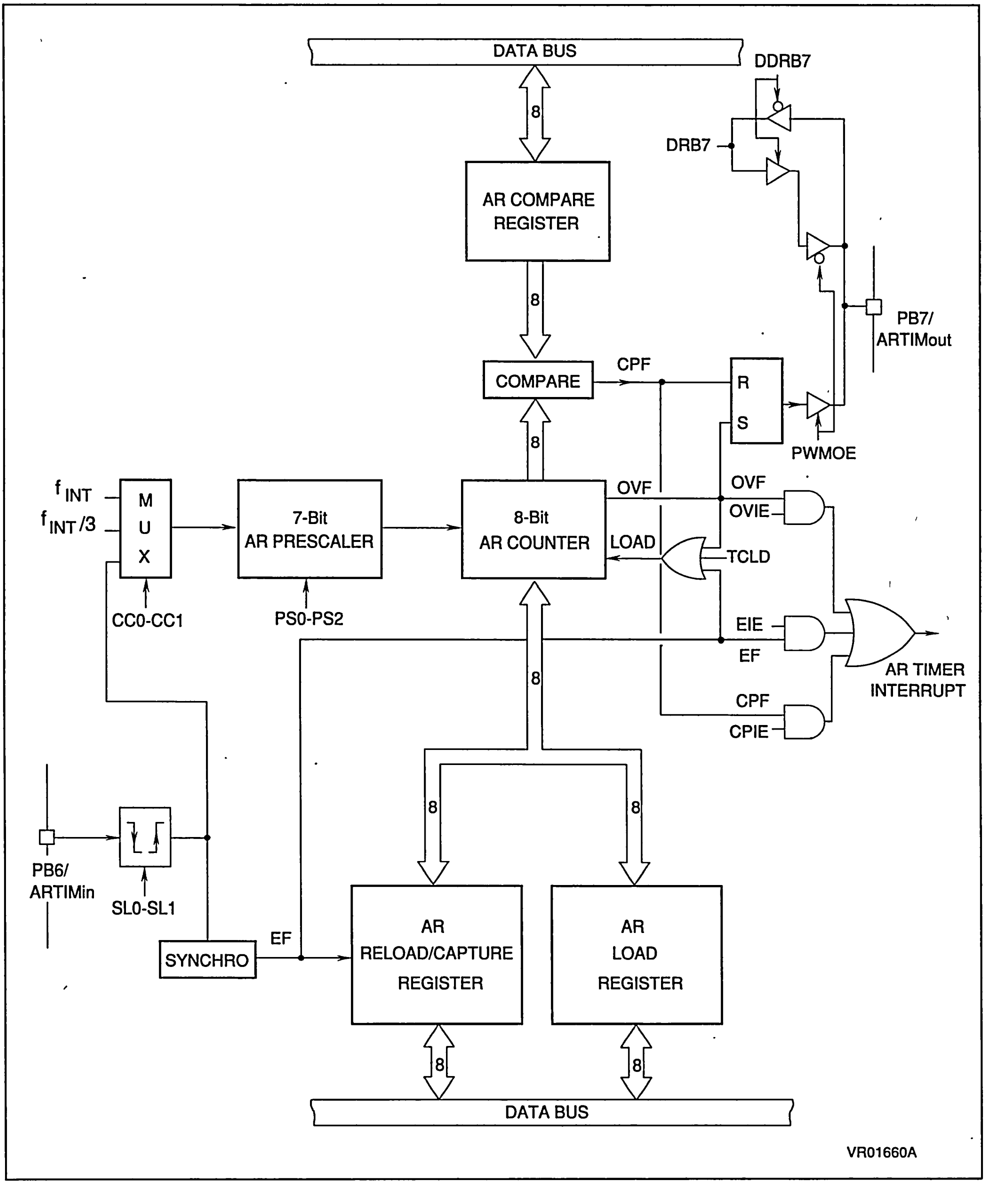
At overflow, the OVF flag of register ARSC0 is set and an overflow interrupt request is generated if the overflow interrupt enable bit, OVIE in the Mode Control Register (ARMC, address D5h), is set to "1". OVF must be reset to zero by the user software.

When the counter reaches the compare value the CPF flag of register ARSC0 is set and a compare interrupt request is generated if the Compare Interrupt enable bit, CPIE, in the Mode Control Register (ARMC, address D5h), is set to one. The interrupt service routine may then adjust the PWM period by loading a new value into ARCP. CPF must be reset to zero by software.

The PWM signal is generated at ARTIMout (refer to block diagram) connected to the ARTIMout output pin. The frequency of this signal is controlled by the prescaler and by the auto-reload value present in the Reload/Capture register ARRC (address D9h). The duty cycle of the PWM signal is controlled by the Compare Register (ARCP, address DAh).

TIMERS (Continued)

Figure 35. AR Timer Block Diagram



TIMERS (Continued)

Note that the reload values will also affect the value and the resolution of the duty cycle of PWM output signal. To achieve a ARTIMout signal the contents of the ARCP register must be greater than the contents of the ARRC register.

The maximum available resolution for the ARTIMout duty cycle is:

Resolution = 1/[255-(ARRC)]

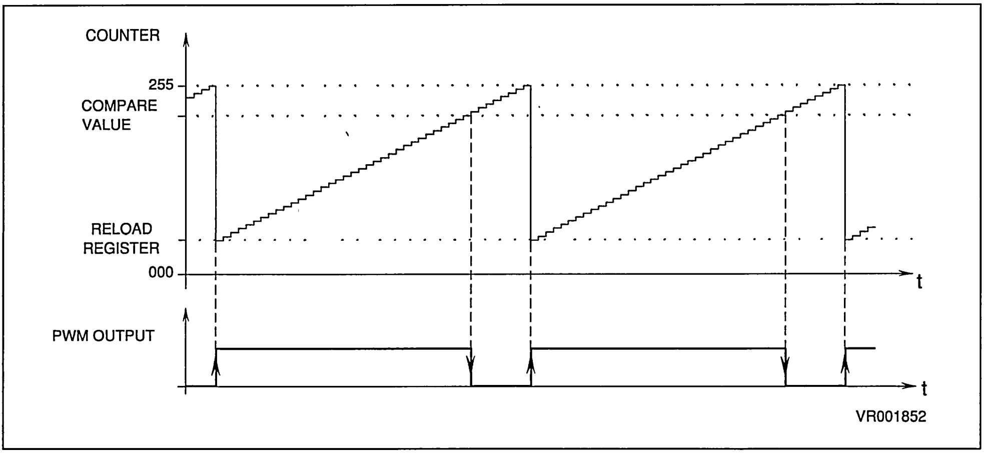
Where ARRC is the content of Reload/Capture register and the compare value loaded in the Compare Register, ARCP, must be in the range from (ARRC) to 255.

The initialization of the ARTC counter is made by writing into the ARRC register, then by setting the TCLD (Timer Load) and the TEN (Timer Clock Enable) bits in the Mode Control register ARMC.

The enable and the selection of clock sources are controlled by CC0, CC1, SL0 and SL1 bits in the Status Control Register ARSC1. The prescaler division ratio is selected by PS0, PS1 and PS2 bits in the ARSC1 Register.

In Auto-reload Mode any clock source can be selected: Internal Clock, Internal Clock divided by 3 or the signal at the ARTIMin input pin.

Figure 36. Auto-reload Timer PWM Function



TIMERS (Continued)

Capture Mode with PWM Generation. In this case, ARTC is a free running 8-bit counter fed by the PSC prescaler output. ARTC is incremented on every clock rising edge.

An 8-bit capture operation from ARTC counter to ARRC register is performed on every active edge at ARTIMin/PC Input pin when enabled by Edge Control bits SL0, SL1 in the ARSC1 register. At the same time the External Flag EF, in the ARSC0 register, is set and an external interrupt request is generated if the External Interrupt Enable bit EIE, in the ARMC register, is set to one. The EF flag must be reset by software.

Each ARTC overflow sets ARTIMout, while a match between ARTC and ARCP (Compare Register) contents resets ARTIMout and sets the compare flag CPF and the compare interrupt request is generated if the related compare interrupt enable bit CPIE is set. A PWM signal is generated at ARTIMout. The CPF flag must be reset by software.

The frequency of this signal is controlled by the prescaler. The duty cycle is controlled by register ARCP from 0-255/256.

Initialization and reading of ARTC counter are made in the same way as in the auto-reload mode (see previous paragraph).

The enable and selection of clock sources is controlled by CC0, CC1 bits in the AR Status Control Register ARSC1.

The prescaler division ratio is selected by PS0, PS1 and PS2 bits in the ARSC1 Register.

In Capture mode the possible clock sources are the internal clock and the internal clock divided by 3; the external ARTIMin input pin should not be used.

Capture Mode with Reset of ARTC, ARPSC and PWM Generation. This mode is identical to the previous one, with the difference that a capture condition also resets the ARTC counter and ARPSC prescaler allowing easy measurement of the time between two captures (for input period measurement on ARTIMin pin).

Load on External Input. ARTC is a free running 8-bit counter fed by the ARPSC prescaler. TC is incremented on every clock rising edge.

Each ARTC overflow sets the ARTIMout. A match between ARTC and ARCP (Compare Register) contents resets the ARTIMout and sets the compare flag CPF and the compare interrupt request is generated if the related compare interrupt enable bit CPIE is set. A PWM signal is generated at ARTIMout. The CPF flag must be reset by software

The initialization of ARTC can be done in the same way as described in the previous paragraph. In addition if the external ARTIMin input is enabled, an active edge on the input pin will copy the contents of the ARRC register into the ARTC counter, whether ARTC is running or not.

Notes:

The allowed AR Timer clock sources are the following:

AR Timer mode	Clock Sources
Auto-reload mode	f_{INT}, f_{INT}/3, ARTIMin
Capture mode	f_{INT}, $f_{INT/3}$
Capture/Reset mode	f_{INT}, $f_{INT/3}$
External Load mode	f_{INT}, $f_{INT/3}$

The timer clock frequency should not be modified while ARTC is counting as the ARTC counter may take an unpredictable value. For example the multiplexer setting should not be modified while ARTC is counting.

Any loading of ARTC (by auto-reload, through ARLR, ARRC or by the Core) resets ARPSC at the same time.

Care should be taken when both the Capture interrupt and the Overflow interrupt are used. The capture and the overflow are asynchronous. If the capture occurs when the Overflow Interrupt Flag (OVF) is high (between counter overflow and the flag being reset by software in the interrupt routine), the External Interrupt Flag (EF) could be cleared simultaneusly without the interrupt being taken into account.

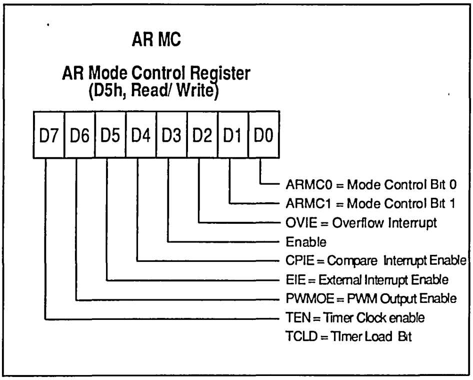
The solution consists in resetting the OVF flag by writing 03h in the ARSC0 register. The value of EF is not affected by this operation. If an interrupt has occured, it will be processed when the micros exits from the interrupt routine (the second interrupt is latched).

TIMERS (Continued)

AR Timer Registers

Mode Control Register ARMC. The AR Mode Control Register ARMC is used to program the different operation modes of AR Timer, to enable the clock of the Timer/Counter and to initialize it. It can be read and written by the Core and it is cleared to zero on system reset (AR Timer is disabled).

Figure 37. AR Mode Control Register


AR MC
AR Mode Control Register
(D5h, Read/ Write)
D7
D6
D5
D4
D3
D2
D1
D0
ARMC0 = Mode Control Bit 0
ARMC1 = Mode Control Bit 1
OVIE = Overflow Interrupt Enable
CPIE = Compare Interrupt Enable
EIE = External Interrupt Enable
PWMOE = PWM Output Enable
TEN = Timer Clock enable
TCLD = Timer Load Bit

TCLD. This bit, when set to one, will cause the contents of ARRC register to be loaded into the ARTC counter and the contents of ARPSC register are cleared in order to initialize the timer before starting to count. This bit is write only and any attempt to read it will show a logical zero.

TEN. This bit, when set to one, will allow the timer to count. When cleared to zero it will stop the timer and freeze the ARPSC and ARTSC values.

PWMOE. This bit, when set, enables the PWM output to be carried on ARTIMout output pin. When cleared to zero the PWM output is disabled.

EIE. This bit, when set, enables the external interrupt request. If EIE = “0” the external interrupt request is masked. If EIE = “1” and the related flag EF in the ARSC0 register is also set an interrupt request is generated.

CPIE. This bit, when set, enables the compare interrupt request. If CPIE = “0” the compare interrupt request is masked. If CPIE = “1” and the related flag CPF into the ARSC0 register is also set an interrupt request is generated.

OVIE. This bit, when set, enables the overflow interrupt request. If OVIE = “0” the compare interrupt request is masked. If OVIE = “1” and the related flag OVF into the ARSC0 register is also set, an interrupt request is generated.

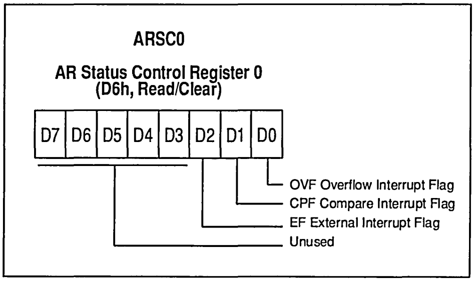
ARMC1, ARMC0. These are the operation mode control bits. The following bit combination will select the different operating modes:

ARMC1	ARMC0	Operating Mode
0	0	Auto-reload Mode
0	1	Capture Mode
1	0	Capture Mode with Reset of ARTC and ARPSC
1	1	Load on External Edge Mode

AR Timer Status/Control Registers ARSC0 & ARSC1. These registers provide the AR Timer status information bits and also allows the programming of clock sources, active edge and prescaler multiplexer programming.

ARSC0 register bits 0,1 and 2 contains the interrupt flags of the AR Timer. These bits are read normally. Each one can be reset by writing a zero. Writing a one does not affect the bit value.

Figure 38. AR Status Control Register 0


ARSC0
AR Status Control Register 0
(D6h, Read/Clear)
D7
D6
D5
D4
D3
D2
D1
D0
OVF Overflow Interrupt Flag
CPF Compare Interrupt Flag
EF External Interrupt Flag
Unused

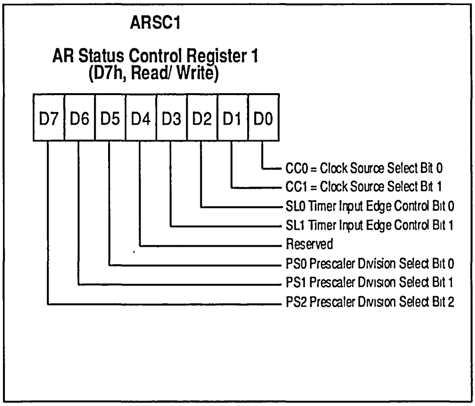
EF. This bit is set to one by any active edge at the external ARTIMin input pin. The flag is cleared by writing a zero in the EF bit.

CPF. This bit is set to one if the contents of ARTC counter and ARCP register are equal. The flag is cleared by writing a zero into CPF bit.

OVF. This bit is set to one by a transition of TC counter from FFh to 00h. The flag is cleared by writing a zero into OVF bit.

TIMERS (Continued)

Figure 39. AR Status Control Register 1


ARSC1
AR Status Control Register 1
(D7h, Read/ Write)
D7
D6
D5
D4
D3
D2
D1
D0
CC0 = Clock Source Select Bit 0
CC1 = Clock Source Select Bit 1
SL0 Timer Input Edge Control Bit 0
SL1 Timer Input Edge Control Bit 1
Reserved
PS0 Prescaler Division Select Bit 0
PS1 Prescaler Division Select Bit 1
PS2 Prescaler Division Select Bit 2

PS2-PS0. These bits control the AR Prescaler division ratio. The prescaler itself is not affected by these bits. The AR PSC division is listed in the following Table 11:

Table 11. Prescaler Division Ratio Selection

PS2	PS1	PS0	ARPSC Division Ratio
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

D4. Reserved. Must be kept to 0.

SL1-SL0. These bits control the edge function on AR Timer input pin for external synchronization. If bit SL0 is cleared to zero the edge detection is disabled, if set to one the edge detection is enabled. If bit SL1 is cleared to zero the AR Timer input pin is rising edge sensitive, if set to one it is falling edge sensitive.

SL1	SL0	Edge Detection
X	0	Disabled
0	1	Rising Edge
1	1	Falling Edge

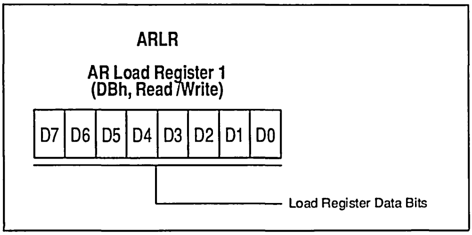
CC1-CC0. These bits select the clock source for the AR Timer through the AR Multiplexer. The programming of the clock sources is explained in the following Table 12:

Table 12. Clock Source Selection

CC1	CC0	Clock Source
0	0	F_{int}
0	1	F_{int} Divided by 3
1	0	ARTIMin Input Clock
1	1	Reserved

AR Load Register ARLR. The ARLR load register is used to read or write "on the fly" the ARTC counter register, while it is counting. ARLR register is not affected by system reset.

Figure 40. AR Load Register

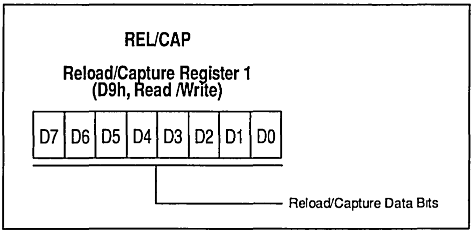


D7-D0. These are the load register data bits.

TIMERS (Continued)

AR Reload/Capture Register. The ARRC reload/capture register is used to hold the auto-reload value that is automatically loaded into ARTC counter from ARRC when overflow occurs.

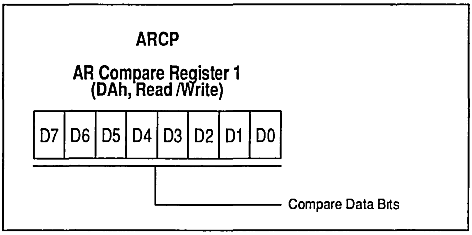
Figure 41. AR Reload/Capture



D7-D0. These are the Reload/Capture register data bits.

AR Compare Register. The CP compare register is used to hold the compare value to perform the compare function with TC counter.

Figure 42. AR Compare Register



D7-D0. These are the Compare register data bits.

DIGITAL WATCHDOG

The digital Watchdog of the ST6260B/65B device consists of a down counter that can be used to provide a controlled recovery from a software upset.

The Watchdog generates a system reset when the counter passes 00h. User software can prevent the reset by reloading the counter. User software should therefore be written in such a way that the counter is regularly reloaded as long as the software runs correctly. In the case of software upset (e.g. infinite loop or power supply fail), user software should not reload the counter so it will pass 00h and reset the MCU.

The Watchdog activation (hardware or software) is user selectable by mask option. If the hardware option is selected the Watchdog is automatically initialized after reset so that this function does not need to be activated by the user program.

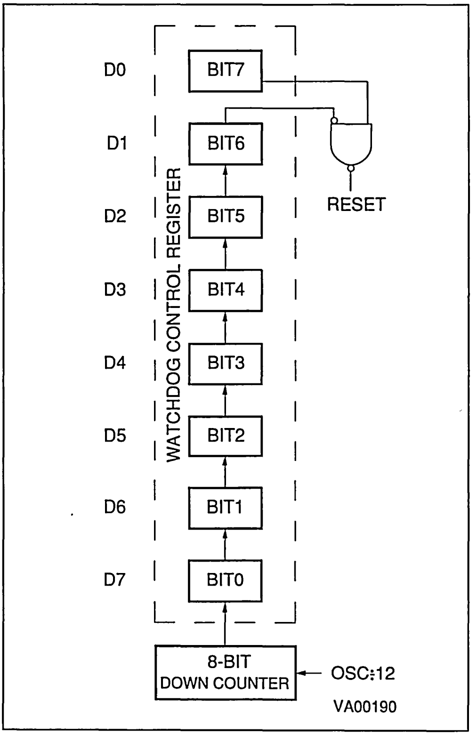
The Watchdog uses one data space register (DWDR location D8h). The Watchdog register is set to FEh on reset and counts down when activated. The Watchdog time can be adjusted through the value reloaded into the DWDR register. Only the 6 MSbits are significant. This gives the possibility to generate a reset in a time between 3072 to 196608 clock cycles in 64 possible steps (with a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded before bits 2-7 decrement from all zeros to all ones.

The actual watchdog behaviour is controlled by two mask options: the WATCHDOG ACTIVATION and the EXTERNAL STOP MODE CONTROL (see Table 13).

The WATCHDOG ACTIVATION can be software (it is launched by software) or hardware (it automatically starts counting down after reset). When the software activation is selected, the watchdog can be launched by setting to 1 bit 0 of the Digital Watchdog Register after bit SR of this register has been set to 1. Once activated, the watchdog cannot be stopped by software: a full external reset is mandatory.

When the EXTERNAL STOP MODE CONTROL is disabled, the STOP instruction is inhibited as soon as the watchdog is active. A WAIT instruction is processed instead and the watchdog continues to countdown. When the EXTERNAL STOP MODE CONTROL is enabled, the NMI pin allows, in addition to the interrupt generation, to control the execution of the STOP instruction. It is inhibited when NMI is low (a WAIT instruction is processed instead). When NMI is high, a STOP instruction freezes the watchdog counter before entering the STOP mode. When the micro exits from the STOP mode (for example, when an NMI interrupt is generated), the watchdog resumes activity. When the EXTERNAL STOP MODE CONTROL is enabled, port PB0 is in addition forced as open drain output.

Figure 43. Watchdog Working Principle



Note:

When the software activation is selected and the watchdog is not activated, the 7 MSbits of the counter can be used to perform timer functions. Care must be taken as the Watchdog bits are in reverse order.

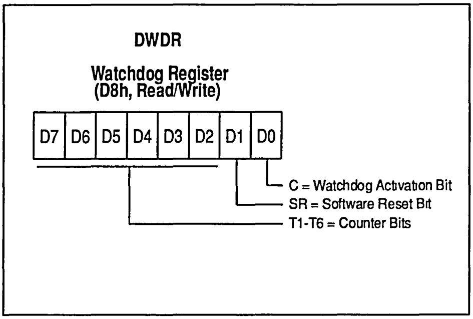
Bit 1 of the Watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero.

DIGITAL WATCHDOG (Continued)

Table 13. Watchdog Activation and External Stop Mode Control

Activation	External Stop Mode Control	NMI	STOP Mode Status
Hardware	Disabled	X	No STOP mode
	Enabled	0	No STOP mode
		1	STOP mode available
Software	Disabled	X	STOP mode available if watchdog not active
	Enabled	0	STOP mode available if watchdog not active
		1	STOP mode available

Figure 44. Digital Watchdog Register



C. This is the Watchdog activation bit. If hardware option is selected, it is forced high and the user cannot change it (the Watchdog is always active). When the software option is selected, the Watchdog function is activated by setting C to 1. It can then be cleared only by a system reset and is not affected by the STOP Mode Control option. When C is kept low the counter can be used as a 7-bit timer.

When cleared to zero it allows the use of the counter as a 7-bit timer. This bit is cleared on reset.

SR. This bit is set to one during the reset and will generate a software reset if cleared to zero. When C = "0" (watchdog disabled) it is the MSB of the 7-bit timer.

T1-T6. These are the watchdog counter bits. It must be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter.

Application note:

The watchdog has an important role in the high noise immunity of the ST62 devices. It should therefore be used wherever possible. The watchdog related options must be selected as a tradeoff between application security and STOP mode availability. When the STOP mode is not required, the hardware activation with External STOP Mode Control disabled should be preferred as it provides maximum security, especially during power on. When the STOP mode is required, the hardware activation with External STOP Mode Control enabled should be chosen. NMI should be high by default to allow the STOP mode to be entered when no specific action is required. When NMI goes low, processing is required, so security becomes important: it is provided by the automatically started watchdog.

Connecting pin NMI to PB0 (see Figure 46) in addition allows a software control of the level at the NMI pin. With PB0 being forced as open drain output, it can then be used to maintain NMI low for as long as maximum security must be guaranteed or to avoid key bounces or noise. When no more processing is required, PB0 must be released and a STOP instruction can be executed for the device returns to the low power consumption mode (provided the NMI signal is high).

DIGITAL WATCHDOG (Continued)

Software activation should be used only when the watchdog counter must be used as timer. To ensure the watchdog has not been unexpectantly turned on, the following instructions should be executed within the first 27 instructions.

```
jrr 0, WD, #+3
ldi WD, 0FDH
```

These instructions test the C bit and reset it (i.e. deactivate the watchdog) if relevant (i.e. if the watchdog is active) by performing a software reset.

With all modes, a minimum of 28 instructions are executed after activation before the watchdog can generate a reset. Consequently, user software must reload the watchdog counter within the first 27 instructions following watchdog activation (software mode) or the first 27 instructions executed after a reset (hardware activation).

Figure 46. Typical circuit to be used when the EXTERNAL STOP MODE CONTROL is enabled

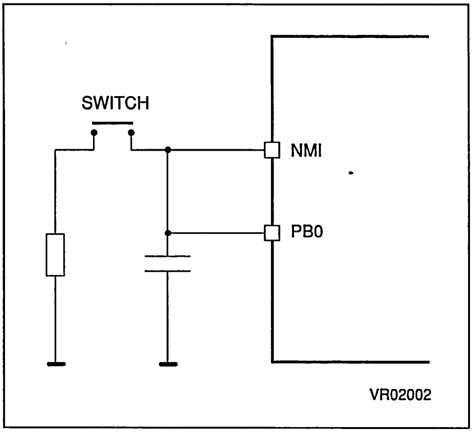
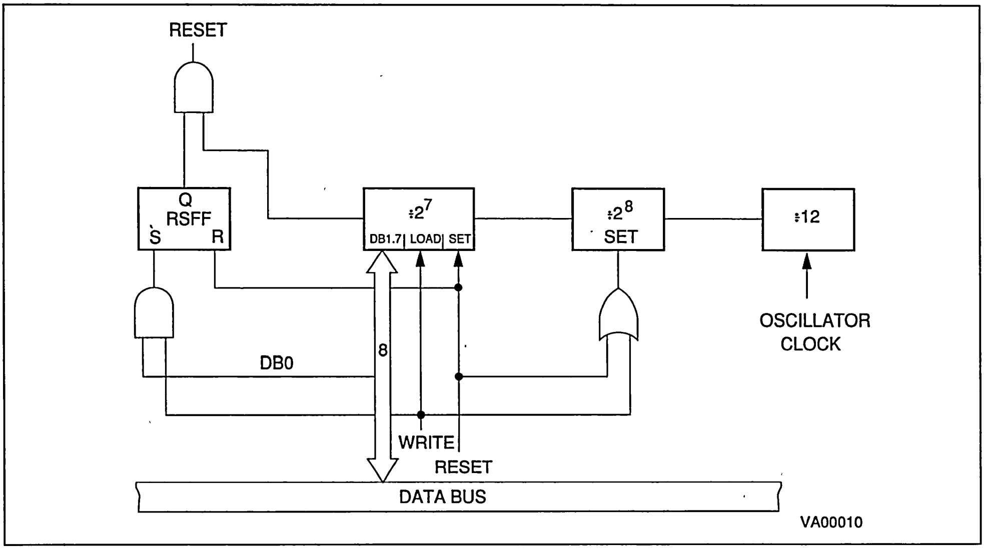


Figure 45. Digital Watchdog Block Diagram



8-BIT A/D CONVERTER

The A/D converter of ST6260B/65B device is an 8-bit analog to digital converter with up to 7 (ST6260B) and up to 13 (ST6265B) analog inputs (as alternate functions of I/O lines PA0-PA7, PC0-PC4) offering 8-bit resolution with total accuracy ±2 LSB and a typical conversion time of 70µs (clock frequency of 8MHz).

The A/D peripheral converts the input voltage by a process of successive approximations using a clock frequency derived from the oscillator with a division factor of twelve. With an oscillator clock frequency less than 1.2MHz, the A/D converter accuracy is decreased.

The selection of the pin signal that has to be converted is done by configuring the related I/O line as analog input through the I/O ports option and data registers (refer to I/O ports description for additional information). Only one I/O line must be configured as analog input at a time. The user must avoid the situation in which more than one I/O pin is selected to be analog input to avoid malfunction of the ST62xx.

The ADC uses two registers in the data space: the ADC data conversion register which stores the conversion result and the ADC control register used to program the ADC functions.

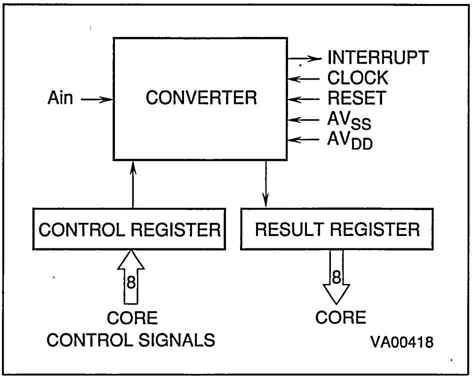
A conversion is started by writing a "1" to the Start bit (STA) in the ADC control register. This automatically clears (resets to "0") the End Of Conversion Bit (EOC). When a conversion has been finished this EOC bit is automatically set to "1" in order to flag that conversion is complete and that the data in the ADC data conversion register is valid. Each conversion has to be separately initiated by writing to the STA bit.

The STA bit is continually being scanned so that if the user sets it to "1" while a previous conversion is in progress then a new conversion is started before the previous one has been completed.The start bit (STA) is a write only bit, any attempt to read it will show a logical "0".

The A/D converter has a maskable interrupt associated to the end of conversion. This interrupt is associated to the interrupt vector #4 and occurs when the EOC bit is set, i.e. when a conversion is completed. The interrupt is masked using the EAI (interrupt mask) bit in the control register.

The power consumption of the device can be reduced by turning off the ADC peripheral. That is achieved when the PDS bit in the ADC control register is cleared to "0". If PDS="1", the A/D is supplied and enabled for conversion. This bit must be set at least one instruction before the beginning of the conversion to allow the stabilization of the A/D converter.*This action is needed also before entering the WAIT instruction as the A/D comparator is not automatically disabled by the WAIT mode*

Figure 47. A/D Converter Block Diagram



During reset any conversion in progress is stopped, the control register is reset to 40h and the A/D interrupt is masked (EAI=0).

Notes:

The ST62xx A/D converter does not feature a sample and hold. The analog voltage to be measured should therefore be stable during the conversion time. Variation should not exceed ±1/2 LSB for the best accuracy in measurement. A low pass filter can be used at the analog input pins to reduce input voltage variation during the conversion.

When selected as an analog channel, the input pin is internally connected to a capacitor Cad of typically 12pF. For maximum accuracy, this capacitor must be fully loaded at conversion start. In the worst case, conversion starts one instruction (6.5 µs) after the channel has been selected. In the worst case conditions, the impedance ASI of the analog voltage source is calculated using the following formula :

$$6.5\ \mu s = 9 \times Cad \times ASI$$

(capacitor loaded over 99.9%), ie 30 kΩ including 50% guardland. ASI can be higher if Cad has been loaded for a longer time by adding instructions before conversion start (adding more than 26 CPU cycles is meaningless).

Since the ADC is on the same chip as the microprocessor the user should not switch heavily loaded output signals during conversion if high precision is needed. This is because such switching will affect the supply voltages which are used for comparisons.

8-BIT A/D CONVERTER (Continued)

The accuracy of the conversion depends on the quality of the power supply voltages (V_{DD} and V_{SS}). The user must specially take care of applying regulated reference voltage on the V_{DD} and V_{SS} pins (the variation of the power supply voltage must be inferior to 5V/ms). This implies in particular that a suitable decoupling capacitor is used at V_{DD}.

The converter can resolve the input voltage with a resolution of:

$$\frac{V_{DD} - V_{SS}}{256}$$

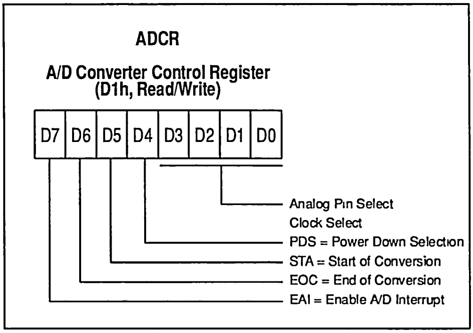
The Input voltage (Ain) which has to be converted must be constant for 1µs before conversion and remain constant during the conversion.

The resolution of the conversion can be improved if the power supply voltage (V_{DD}) of the microcontroller becomes lower.

In order to optimize the resolution of the conversion, the user can configure the microcontroller in the WAIT mode because this mode allows the minimization of the noise disturbances and the variations of the power supply voltages due to the switching of the outputs. Nevertheless, it must be take care of executing the WAIT instruction as soon as possible after the beginning of the conversion because the execution of the WAIT instruction may provide a small variation of the V_{DD} voltage (the negative effect of this variation is minimized at the beginning of the conversion because the latter is less sensitive than the end of the conversion when the less significant bits are determined).

The best configuration from a accuracy point of view is the WAIT mode with the Timer and AR Timer stopped. Indeed, only the ADC peripheral and the oscillator are still working. The MCU has to be wake-up from the WAIT mode by the interrupt of the ADC peripheral at the end of the conversion. It must be noticed that the wake-up of the microcontroller could be done also with the interrupt of the TIMER, but in this case, the Timer is working and some noise could disturb the converter in terms of accuracy.

Figure 48. A/D Converter Control Register


ADCR
A/D Converter Control Register
(D1h, Read/Write)
D7
D6
D5
D4
D3
D2
D1
D0
Analog Pin Select
Clock Select
PDS = Power Down Selection
STA = Start of Conversion
EOC = End of Conversion
EAI = Enable A/D Interrupt

EAI. If this bit is set to one the A/D interrupt (vector #4) is enabled, when EAI=0 the interrupt is disabled.

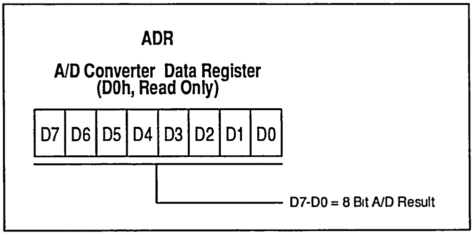
EOC. *Read Only*;This read only bit indicates when a conversion has been completed. This bit is automatically reset to zero when the STA bit is written. If the user is using the interrupt option then this bit can be used as an interrupt pending bit. Data in the data conversion register are valid only when this bit is set to one.

STA. *Write Only*; Writing a "1" in this bit will start a conversion on the selected channel and automatically reset to zero the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

PDS. This bit activates the A/D converter if set to "1". Writing a zero into this bit will put the ADC in power down mode (idle mode).

D3-D0. Not used

Figure 49. A/D Converter Data Register



SERIAL PERIPHERAL INTERFACE SPI

The ST6260B/65B SPI is an optimized synchronous serial interface with programmable transmission modes and master/slave capabilities supporting a wide range of industry standard SPI specifications. The ST6260B/65B SPI is controlled by simple user software to perform serial data exchange with low-cost external memory or serially controlled peripherals for display or driving motors or relays. The peripheral is composed of an 8-bit data/shift register DSR (address E0h), by a Divide register DIV (address E1h) and by a mode control register MOD (address E2h).

The SPI may be used as either a Master or a Slave Unit. The Master is defined by the synchronous serial clock line SCK being supplied by the MCU, while the Slave mode accepts external data with the SCK clock externally supplied. For the Master mode of the SPI, SCK is internally generated with a frequency derived from a programmable division ratio of the Oscillator Clock divided by 13. Input may also be disabled in Master mode for data security.

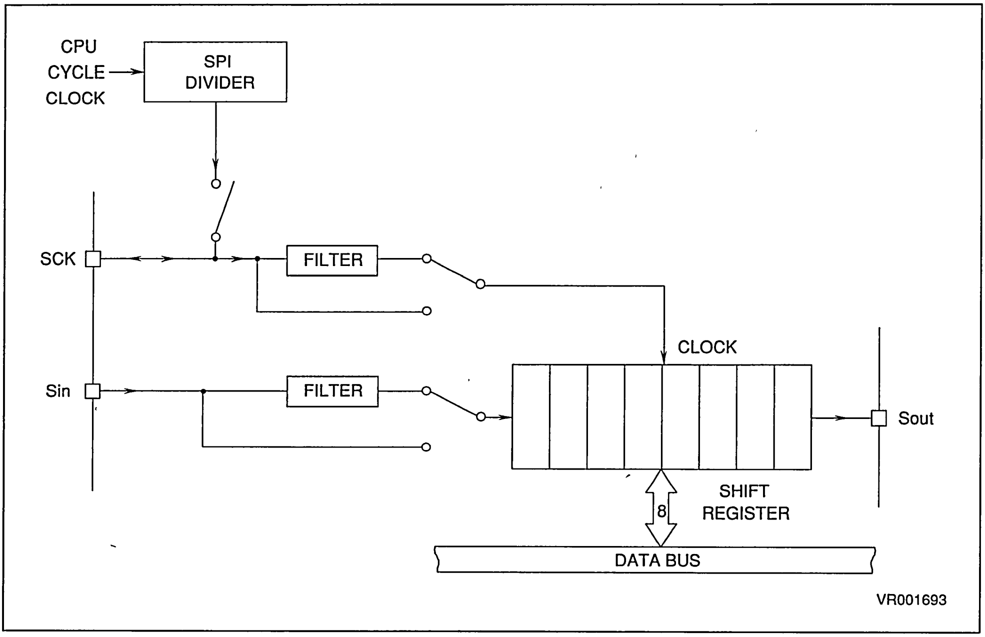
For maximum versatility the SPI can be programmed to sample the data on either the rising or the falling edge of SCK, and with or without a phase shift.

The Sin, Sout and SCK (SPI Data in, Data out and Clock signals respectively) signals are connected, as alternate functions, to I/O pins PC2-PC4. PC2 is connected with the SPI Serial Data Input Sin, PC3 is connected with the SPI Serial Data Output Sout and PC4 is connected with the SPI Clock Input/Output SCK.

For serial input operation PC2/Sin must be configured as input. For serial output operation, PC3/Sout alternate function is selected by programming Bit 0 of Miscellaneous Register (address DDh); writing a zero will set the pin as PC3 I/O line while writing a one will select the SPI Sout functionality. The serial clock Input mode is selected if the PC4 port pin is programmed in input mode and bit SPCLK is cleared. The output mode is selected if PC4 is programmed in output mode and SPCLK is set to 1.

An interrupt request can be associated to the end of transmission. This request is associated to interrupt vector #2 and can be masked by programming bit SPIE of the SPI MOD register. As the SPI interrupt is "ORed" with Port C interrupt source, an interrupt flag bit is available in the DIV register allowing the discrimination of the interrupt request.

Figure 50. SPI Block Diagram



SERIAL PERIPHERAL INTERFACE SPI (Continued)

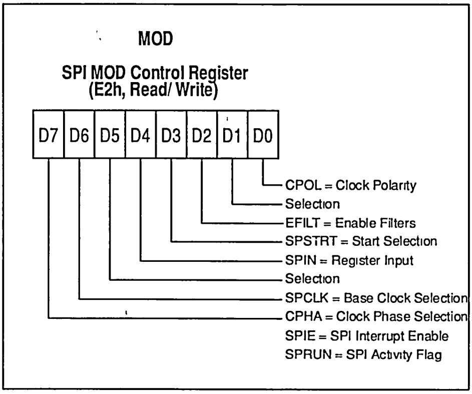
SPI Registers

SPI MODE (SPIMOD) Control Register

The MOD control register defines and controls the transmission modes and characteristics.

This register is read/write and all bits are cleared at reset. The configuration of SPSTRT = 1 and SPIN = 1 is not allowed and must be avoided.

Figure 51. SPI MOD Control Register



SPRUN. This bit is the SPI activity flag. This can be used in either read or write modes; it is automatically cleared by the SPI at the end of a transmission and generates an interrupt request (providing that the SPIE Interrupt Enable bit is set). The Core can stop the running transmission at any time by resetting the SPRUN bit; this will also generate an interrupt request (providing that the SPIE Interrupt enable bit is set). The SPRUN bit can be used as the start bit, in conjunction with the SPSTRT bit, when an external signal is present on the Sin pin.

SPIE. This bit is the SPI Interrupt Enable bit. If this bit is set to one the SPI interrupt (vector #2) is enabled, when SPIE = "0" the interrupt is disabled.

CPHA. This bit selects the clock phase of the clock signal. If this bit is cleared to zero the normal state is selected; in this case Bit 7 of the data frame is present on Sout pin as soon as the SPI Shift Register is loaded. If this bit is set to one the shifted state' is selected; in this case Bit 7 of data frame is present on Sout pin on the first falling edge of Shift Register clock. The polarity relation and the division ratio between Shift Register and SPI base clock are also programmable; refer to DIV register and Timing Diagrams for more information.

SPCLK. This bit selects the SPI base clock source. It is either the core cycle clock (f_{INT}/13) (Master mode) or the signal provided at SCK pin by an external device (slave mode). If SPCLK is low and the SCK pin is configured as input, the slave mode is selected. If SPCLK is high and the SCK pin is configured as output, the master mode is selected. In this case, the phase and polarity of the clock are controlled by CPOL and CPHA.

SPIN. This bit enables the transfer of the data input to the Shift Register in received mode. If this bit is cleared to zero the Shift Register input is 0. If this bit is set to one the Shift Register input corresponds to the input signal present on the Sin pin.

SPSTRT. This bit selects the transmission start mode. If this bit is cleared to zero the internal start condition occurs as soon as the SPRUN bit is enabled (set to one). If this bit is set to one, the internal start signal is the logic "AND" between the SPRUN bit and the external signal present on the Sin pin; in this case transmission will start after the latest of both signals providing that the first signal is still present. After the transmission has been started, it will continue even if the Sin signal is reset.

EFILT. This bit enables/disables the input noise filters on the Sin and SCK inputs. If it is cleared to zero the filters are disabled, if set to one the filters are enabled. These noise filters will eliminate any pulse on Sin and SCK with a pulse width smaller than one to two Core clock periods (depending on the occurrence of the signal edge with respect to the Core clock edge). For example, if the ST6260B/65B runs with an 8MHz crystal, Sin and SCK will be delayed by 125 to 250ns.

CPOL. This bit controls the relationship between the data on the Sin and Sout pins and SCK. The CPOL bit selects the clock edge which captures data and allows it to change state. It has the greatest impact on the first bit transmitted (the MSB) as it does (or does not) allow a clock transition before the first data capture edge.

Refer to the timing diagrams at the end of this section for additional details. These show the relationship between CPOL, CPHA and SCK, and indicate the active clock edges and strobe times.

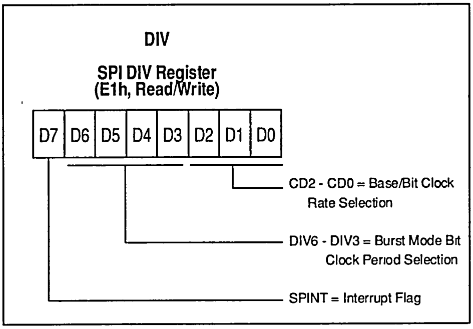
SERIAL PERIPHERAL INTERFACE SPI (Continued)

SPI Divide (SPIDIV) Register

The SPIDIV register defines the SPI transmission rate and frame format. It also contains the interrupt flag bit.

Bits CD0-CD2, DIV3-DIV6 are read/write while SPINT can be read and cleared only. Write access is not allowed if the SPRUN bit of Mode Control register is set to one. All bits are cleared at reset.

Figure 52. SPI DIV Register


DIV
SPI DIV Register
(E1h, Read/Write)
D7
D6
D5
D4
D3
D2
D1
D0
CD2 - CD0 = Base/Bit Clock Rate Selection
DIV6 - DIV3 = Burst Mode Bit Clock Period Selection
SPINT = Interrupt Flag

SPINT/DIV7. This is the SPI interrupt flag bit. It is automatically set to one by the SPI at the end of a transmission and an interrupt request can be generated in accordance with the state of the interrupt mask bit into the MOD control register. This bit is read only and has to be cleared by the user software at the end of the interrupt service routine.

DIV6-DIV3. These bits define the number of shift register bits that are transmitted in a transmission frame. The available selections are listed in Table 14. The normal setting is 8 bits.

CD2-CD0. These bits define the division ratio between the core clock (f_{INT} divided by 13) and clock supplied to the Shift Register in Master mode.

SPI Data Shift (DSR) Register

SPIDSR is the SPI data shift register.

The Shift Register transmits and receives the Most Significant bit as the first bit.

Table 14. Base/Bit Clock Ratio Selection

CD2-CD0	Divide Ratio (decimal)
0 0 0	Divide by 1
0 0 1	Divide by 2
0 1 0	Divide by 4
0 1 1	Divide by 8
1 0 0	Divide by 16
1 0 1	Divide by 32
1 1 0	Divide by 64
1 1 1	Divide by 256

Table 15. Burst Mode Bit Clock Periods

DIV6-DIV3	Number of bits sent
0 0 0 0	Reserved (not to be used)
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	10
1 0 1 1	11
1 1 0 0	12
1 1 0 1	13
1 1 1 0	14
1 1 1 1	15

SPIDSR is read/write, however write access is not allowed if the SPRUN bit of Mode Control register is set to one.

DSR7-DSR0. These are the SPI shift register data bits.

Data is sampled into DSR on the SCK edge determined by the CPOL and CPHA bits. The affect of these setting is shown in the following diagrams.

Figure 53. SPI Data/Shift Register

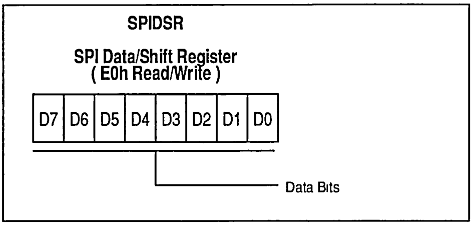
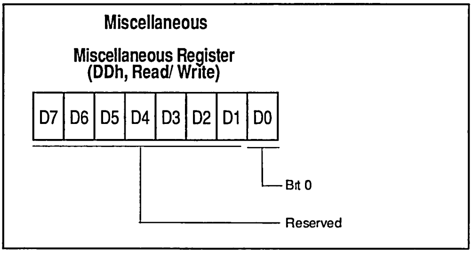


Figure 54. Miscellaneous Register



Bit 0. This bit, when set, selects pin PC3/Sout as the SPI output line. When this bit is cleared to zero, PC3/Sout acts as a standard I/O line.

SERIAL PERIPHERAL INTERFACE (Continued)

SPI Timing Diagrams

Figure 55. CPOL = 0 Clock Polarity Normal, CPHA = 0 Phase Selection Normal

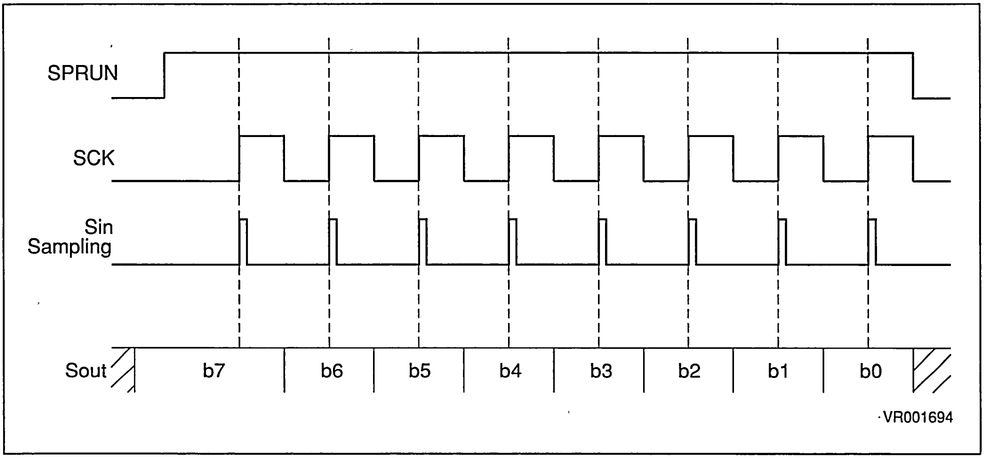


Figure 56. CPOL = 1 Clock Polarity Inverted, CPHA = 0 Phase Selection Normal

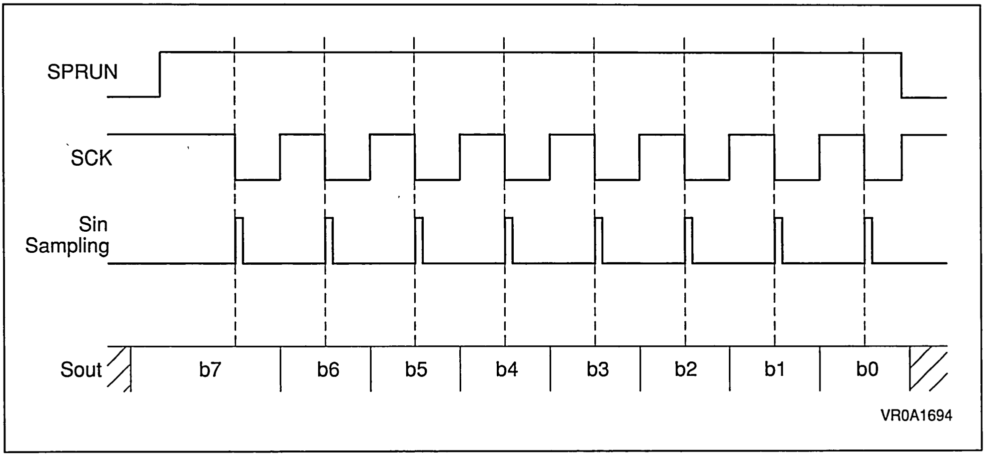


Figure 57. CPOL = 0 Clock Polarity Normal, CPHA = 1 Phase Selection Shifted

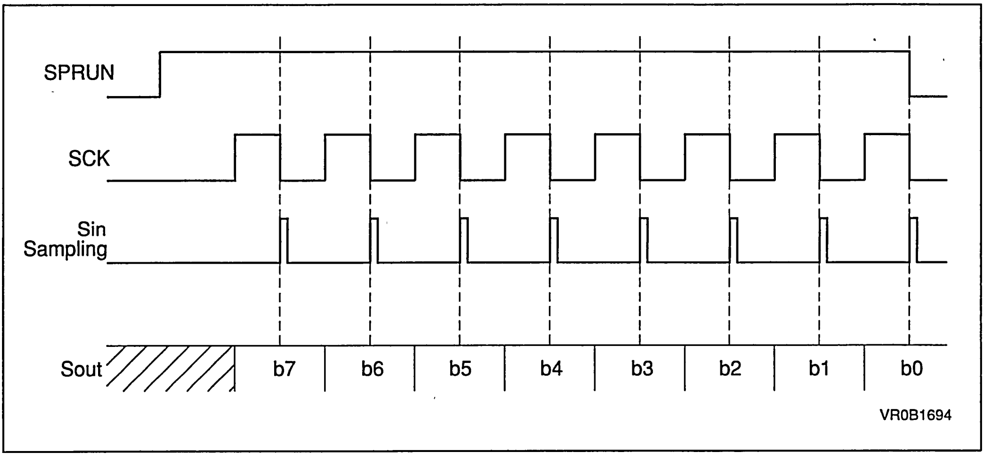
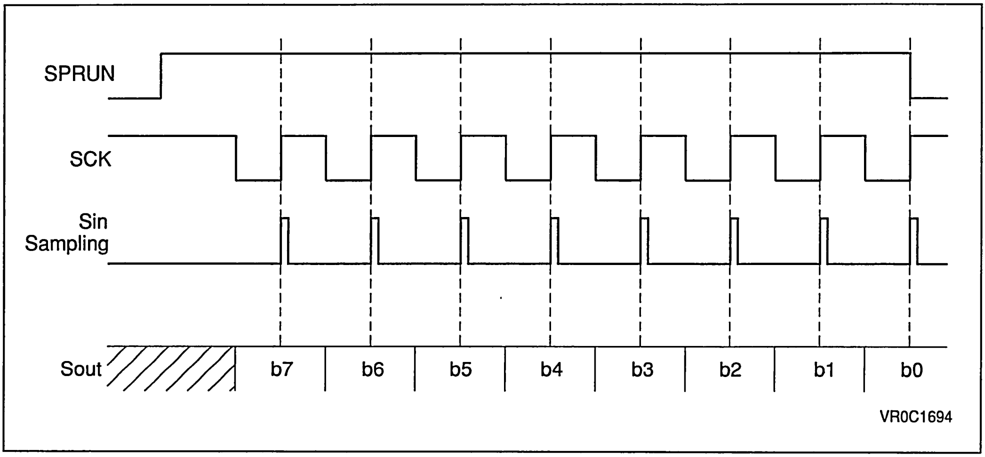


Figure 58. CPOL =1 Clock Polarity Inverted CPHA = 1 Phase Selection Shifted



SOFTWARE DESCRIPTION

The ST62xx software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST62xx core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space.

Addressing Modes

The ST62xx core has nine addressing modes which are described in the following paragraphs. The ST62xx core uses three different address spaces : Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X,Y,V and W registers, peripheral and Input/Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct. The core can address the four RAM registers X,Y,V,W (locations 80h, 81h, 82h, 83h) in the short-direct addressing mode . In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch to any address of the 4K bytes Program space.

An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained in adding the three most significant bits that characterize the kind of the test, one bit that determines whether the branch is a forward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0h to Fh) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range of -126 to +129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80h,81h). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST62xx core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types:load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types.

All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes.

For Load Immediate one operand can be any of the 256 data space bytes while the other is always immediate data.

Table 16. Load & Store Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:

X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 17. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:

X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register

Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieve a branch in the program when the selected condition is met.

Bit Manipulation Instructions. These instructions can handle any bit in data space memory. One group either sets or clears. The other group (see Conditional Branch) performs the bit test branch operations.

Control Instructions. The control instructions control the MCU operations during program execution.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space.

Table 18. Conditional Branch Instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b. 3-bit address
e. 5 bit signed displacement in the range -15 to +16
ee. 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ. Affected
*. Not Affected

Table 19. Bit Manipulation Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b. 3-bit address;
rr. Data space register;
*. Not Affected

Table 20. Control Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated and a WAIT is automatically executed instead of a STOP if the watchdog function is selected.
Δ. Affected
*. Not Affected

Table 21. Jump & Call Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc.12-bit address;
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used by ST6

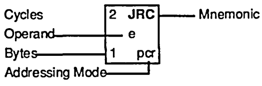
LOW HI	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW HI
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b d.	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b.d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b d	2 JRZ e 1 pcr	#	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b.d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b.d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

	Tj =	T_A + PD x RthJA
Where :	T_A =	Ambient Temperature.
	RthJA =	Package thermal resistance (junction-to ambient).
	PD =	Pint + Pport.
	Pint =	I_{DD} x V_{DD} (chip internal power).
	Pport =	Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3$^{(1)}$	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3$^{(1)}$	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50$^{(2)}$	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guaranteed to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

- (2) The total current through ports A and B combined may not exceed 50 mA. The total current through port C may not exceed 50 mA. If the application is designed with care and observing the limits stated above, total current may reach 100 mA.

THERMAL CHARACTERISTIC

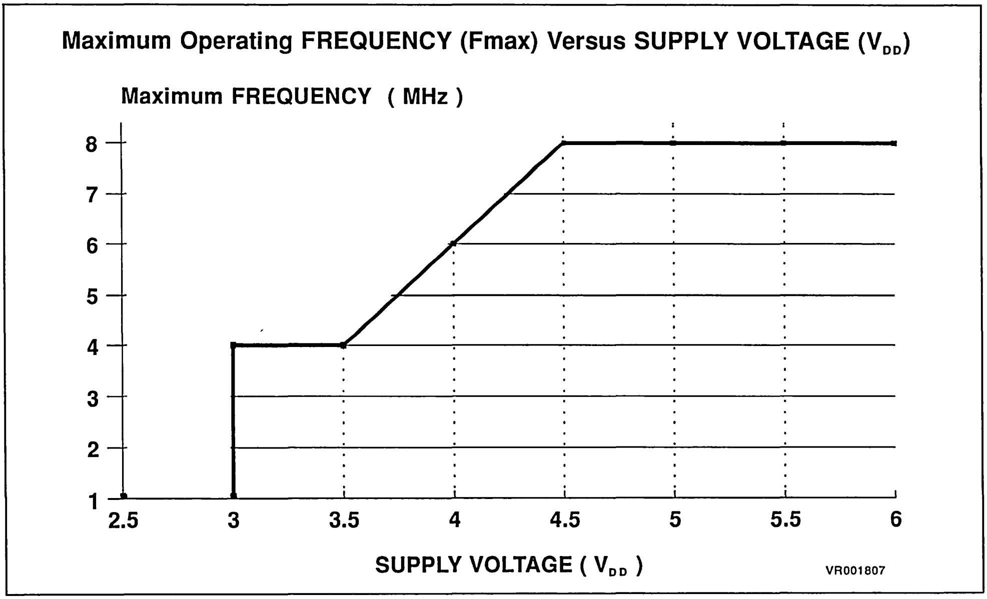
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz	3.0		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
f_{INT}	Internal Frequency [3]	V_{DD} = 3V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input [1] Analog Inputs[2]	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input [1] Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

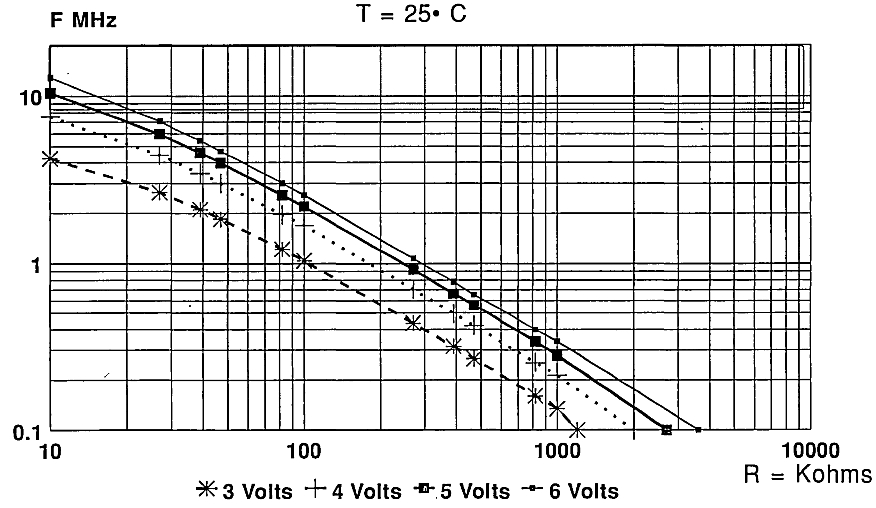
Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An internal frequency above 1MHz is recommended for reliable A/D results.



The shaded area is outside the ST6260B/65B operating range, device functionality is not guaranteed.
The striped area is guaranteed only with the LOW VOLTAGE option.

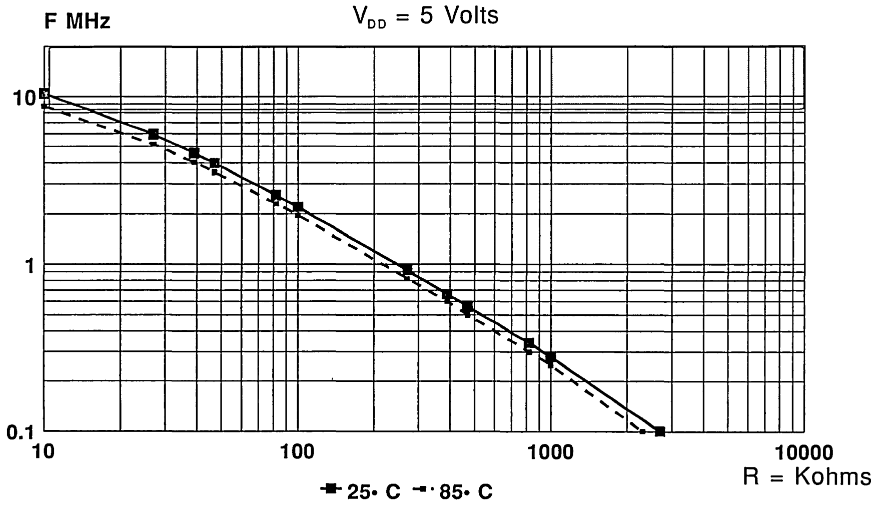
RC Oscillator. fOSC Frequency versus RNET (Typical Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

VR01935

RC Oscillator. fOSC Frequency versus RNET (Typical Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

VR01935A

DC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage [4] All Inputs	V_{DD}=5V V_{DD}=3V	0.2 0.2			V
V_{OL}	Low Level Output Voltage Port A, C	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL} = +5.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OL}	Low Level Output Voltage Port B	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL}=+20.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OH}	High Level Output Voltage Port A, B, C	V_{DD}=4.5V I_{OL} = -1.6mA V_{DD}=4.5V I_{OL} = -5.0mA V_{DD}=3.0V I_{OL} = -0.7mA	4.1 3.5 2.6			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C, NMI	V_{IN} = V_{SS}, V_{DD}=2.5-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS}· f_{OSC}=8MHz			3.5	mA
	Supply Current in RUN Mode [2]	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			6.6 TBD	mA
	Supply Current in WAIT Mode [3]	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			1.50 TBD	mA
	Standard STOP Mode Consumption Option[3]	I_{LOAD}=0mA V_{DD}=6.0V; 70°C			10	µA
	Low STOP Mode Consumption Option[3]	I_{LOAD}=0mA V_{DD}=3.0V; 70°C			2	µA

Notes :

1. Only when pull-ups are not inserted
2. All peripherals running
3. EEPROM and A/D Converter in Stand-by
4. Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

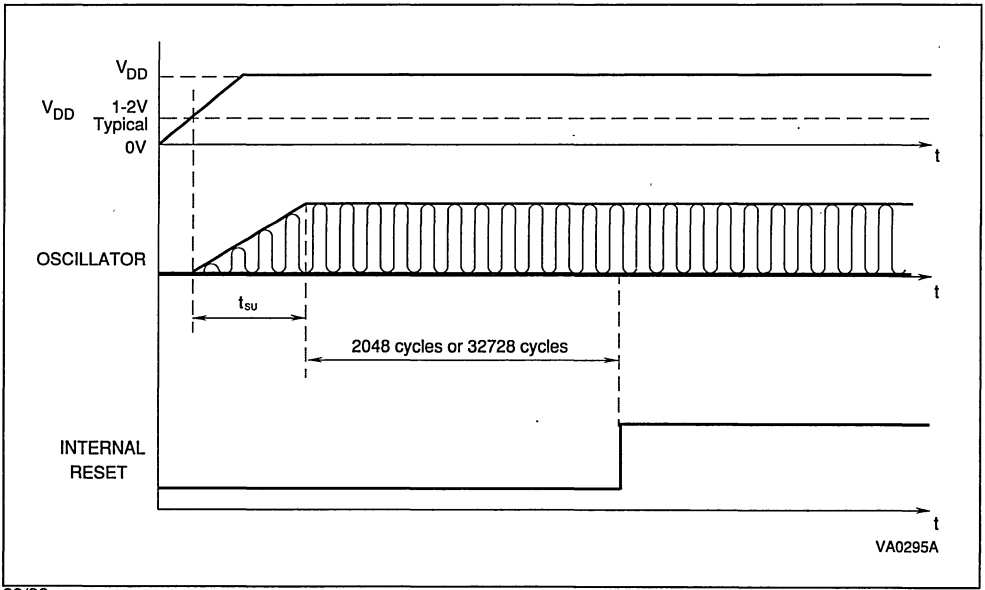
(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V V_{DD} = 4.5V			4 8	MHz
t_{SU}	Oscillator Start-up Time at Power On [2]	Ceramic Resonator C_{L1} = C_{L2} = 22pF		5	100	ms
t_{SUS}	Oscillator STOP mode Recovery Time [2]	8MHz Ceramic Resonator CL1=C_{L2}=22pF		0.2	100	
		8MHz Quartz CL1=C_{L2}=22pF		10	100	
t_{REC}	Supply Recovery Time [1]		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C T_A = 85°C T_A = 125°C		5 10 20	10 20 30	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300,000			cycles
Retention	EEPROM Data Retention	T_A = 25°C	10			years
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:

1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.
2. See Figure 59. This value is highly dependent on the Ceramic Resonator or Quartz Crystal used in the application.

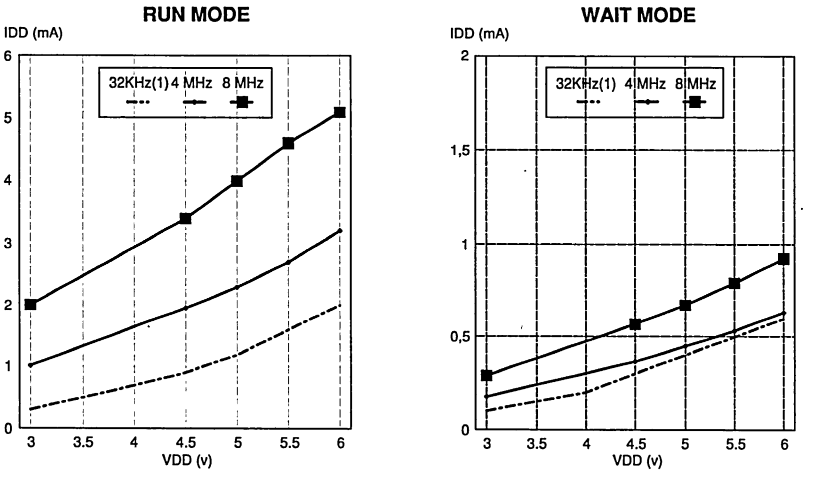
Figure 59. Power On Reset



ELECTRICAL CHARACTERISTICS (Continued)

CURRENT CONSUMPTION

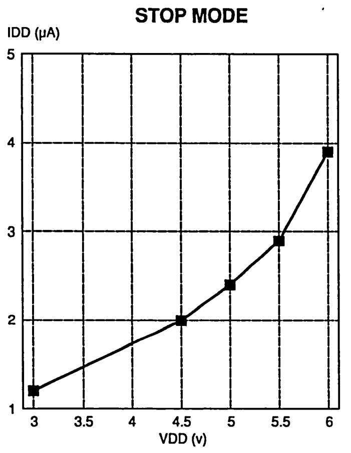
IDD Current Versus Supply Voltage
Typical Values (TA : +85°C)



VR01993A

Note (1) : Using the network described in the Application Note AN673

IDD Current Versus Supply Voltage
Typical Values(TA : +85°C)



VR01993B

I/O PORT CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			 0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		 0.1 0.1	 1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	KΩ

SPI CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note 1. Minimum time 0µs
Maximum time 1 instruction cycle

TIMER1 CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin[1]				$\frac{f_{INT}}{4}$	MHz
t_W	Pulse Width at TIM1 Pin[1]	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

Note :
1. Not available for ST6260B

AR TIMER CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	125 125 125			ns ns ns

A/D CONVERTER CHARACTERISTICS

(T_A= -40 to +85°C unless otherwise specified)

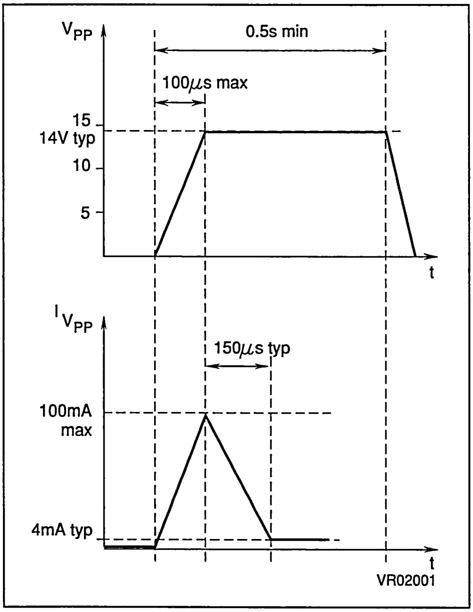
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy [1] [2]	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_{IN} = V_{SS}$	00			Hex
FSR	Full Scale Reading	Conversion result when $V_{IN} = V_{DD}$			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN}[3]	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance	Analog Channel switched just before conversion start [4]			30	kΩ

Notes:

1. Noise at V_{DD}, V_{SS}<10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

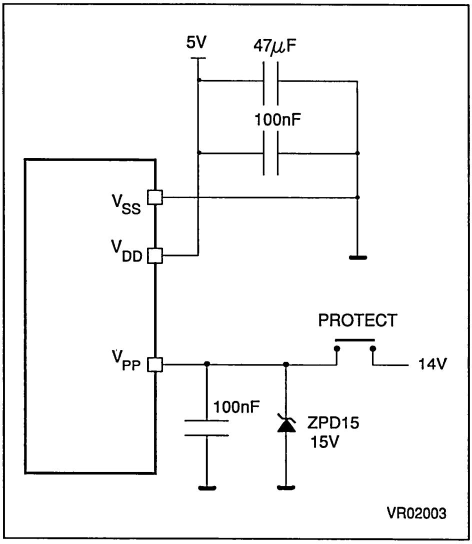
READ PROTECTION FUSE

If the ROM READOUT PROTECTION option is selected as enabled, the following waveform must be applied at the V_{PP} pin for the fuse to be blown:



The following circuit can be used for this purpose:

Figure 60. Example of READOUT PROTECTION Fuse programming circuit



Note: ZPD15 is used for overvoltage protection

ORDERING INFORMATION

The following chapter deals with the procedure for transfer customer codes to SGS-THOMSON.

Communication of the customer code. Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on one diskette with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to SGS-THOMSON using the correctly filled OPTION LIST appended.

Listing Generation & Verification. When SGS-THOMSON receives the diskette, a computer listing is generated from it. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask.

SGS-THOMSON sales organization will provide detailed information on contractual points.

Table 22. ROM Memory Map

Device Address	Description
0000h-007Fh	Reserved [1]
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved [1]
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved [1]
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Notes :
1. Reserved Areas should be filled with FFh

ORDERING INFORMATION TABLE

Sales Type	ROM x8	I/O	Temperature Range	Package
ST6260BB1/XXX ST6260BB6/XXX	4K Bytes	13 13	0 to +70°C -40 to +85°C	PDIP20
ST6260BM1/XXX ST6260BM6/XXX	4K Bytes	13 13	0 to +70°C -40 to +85°C	PSO20
ST6265BB1/XXX ST6265BB6/XXX	4K Bytes	21 21	0 to +70°C -40 to +85°C	PDIP28
ST6265BM1/XXX ST6265BM6/XXX	4K Bytes	21 21	0 to +70°C -40 to +85°C	PSO28

Note: /XXX is a 2-3 alphanumeric character code added to the generic sales type on receipt of a ROM code and valid options.

ST6260B, ST6265B MICROCONTROLLER OPTION LIST

Customer . . . .
Address . . . .
. . . .
Contact . . . .
Phone No . . . .
Reference . . . .

SGS-THOMSON Microelectronics references

Device:
[ ] ST6260B, [ ] ST6265B

Package:
[ ] Dual in Line Plastic [ ] Small Outline Plastic

In this case, select conditioning
[ ] Standard (Stick) [ ] Tape & Reel

Temperature Range:
[ ] 0°C to + 70°C [ ] – 40°C to + 85°C

Special Marking:
[ ] No
[ ] Yes "_ _ _ _ _ _ _ _ _ _ _ _"

Authorized characters are letters, digits, '.', '–', '/' and spaces only.
Maximum character count DIP20 - DIP28: 10
SO20 - SO28: 8.

Oscillator Source Selection :
[ ] Crystal Quartz/Ceramic Resonnator
[ ] RC Network

Power on Reset Delay:
[ ] 32768 cycles.delay
[ ] 2048 cycles delay

Watchdog Selection:
[ ] Software Activation (STOP mode available)
[ ] Hardware Activation (no STOP mode)

External STOP Mode Control:
[ ] Enabled
[ ] Disabled

ROM Readout Protection:
[ ] Disabled

For Enabled option, contact your local SGS-THOMSON office.

STOP Mode Consumption:
[ ] Standard (10µA max)

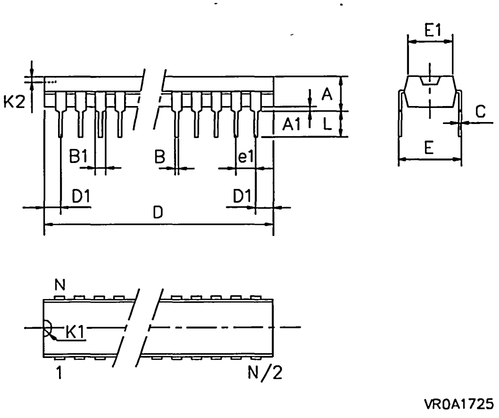
For Low STOP Mode Consumption option contact your local SGS-THOMSON office.

Supply Operating Range: [ ] Standard Range: 3.0V to 6.0V

Notes . . . .
. . . .
Signature . . . .
Date . . . .

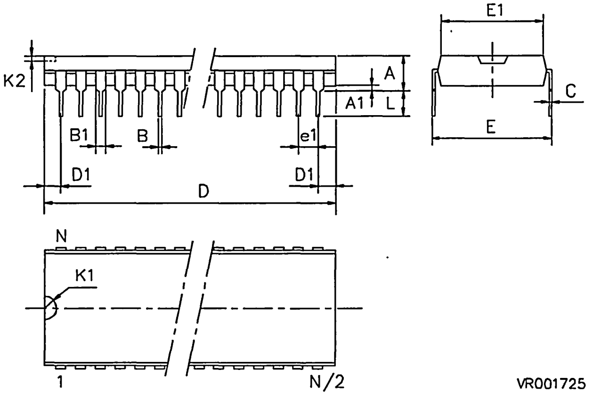
PACKAGE MECHANICAL DATA

Figure 61. 20-Pin Dual in Line Plastic (B), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.93			0.155
A1	0.254			0.010		
B			0.45			0.017
B1	1.39		1.65	0.055		0.065
C			0.25			0 009
D			25.4			1.000
D1			1.34			0 053
E		8.5			0.334	
E1			7.1			0.279
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L		3.30			0.129	
e1		2.54			0.10	
Number of Pins						
N	20					

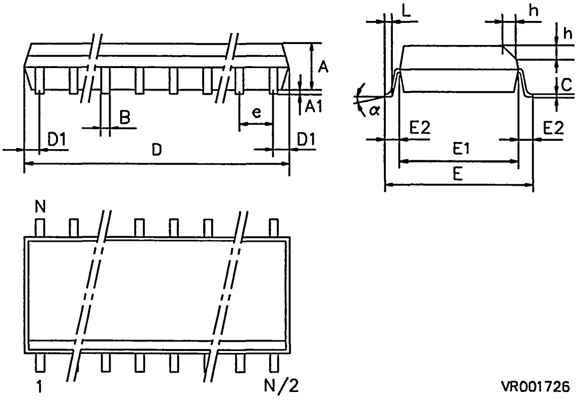
Figure 62. 28-Pin Dual in Line Plastic (B), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0 086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0 2		0.3	0 008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9				0.508
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

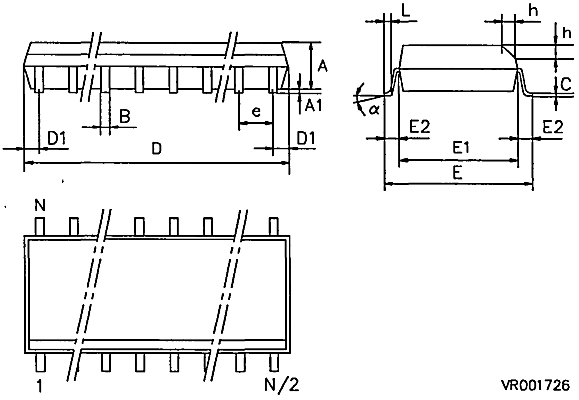
PACKAGES MECHANICAL DATA (Continued)

Figure 63. 20-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	12.6		13.0	.4961		.5118
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	20					

Figure 64. 28-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

NOTES:

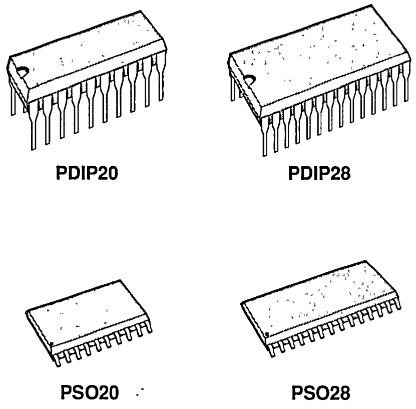
SGS-THOMSON
MICROELECTRONICS

ST62E60B, T60B
ST62E65B, T65B

8-BIT OTP/EPROM HCMOS MCUs WITH A/D CONVERTER, EEPROM & AUTORELOAD TIMER

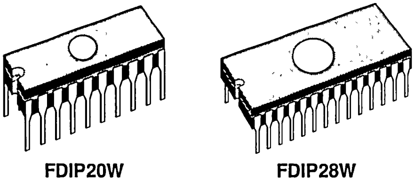
PRELIMINARY DATA

- 3.5 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User EPROM: 3884 bytes
  Data ROM: User selectable size
  (in program EPROM)
  Data RAM: 128 bytes
  EEPROM: 128 bytes
- PDIP20, PSO20 (ST62T60B) packages
- PDIP28, PSO28 (ST62T65B) packages
- FDIP20W (ST62E60B) packages
- FDIP28W (ST62E65B) packages
- 13/21 fully software programmable I/O as:
  – Input with pull-up resistor
  – Input without Pull-up resistor
  – Input with interrupt generation
  – Open-drain or push-pull outputs
  – Analog Inputs
- 6/8 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (Timer1)
- 8 bit Autoreload timer with 7-bit programmable prescaler (AR Timer)
- Digital Watchdog
- 8 bit A/D Converter with up to 7 (ST62E60B,T60B) and up to 13 (ST62E65B,T65B) analog inputs
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator driven by Quartz or Ceramic or RC network
- User configurable Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes



(Ordering Information at the end of the datasheet)

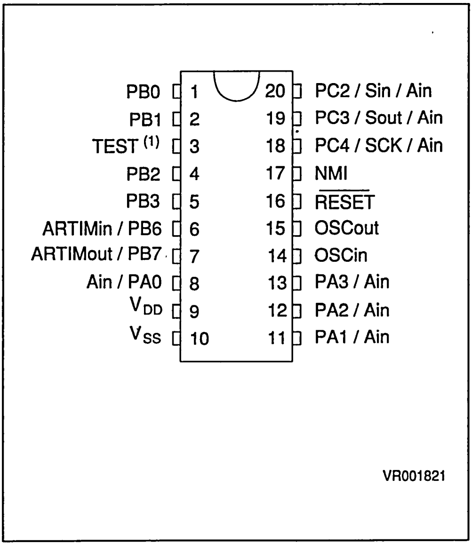
EPROM PACKAGES



The ST62E60B and ST62E65B are the EPROM versions; ST62T60B and ST62T65B are the OTP versions; both are fully compatible with ST6260B and ST6265B ROM resonator versions.

This is preliminary data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. ST62E60B/T60B Pin Configuration



Note 1. This pin is also the V_{PP} input for EPROM based devices

Figure 2. ST62E65B/T65B Pin Configuration

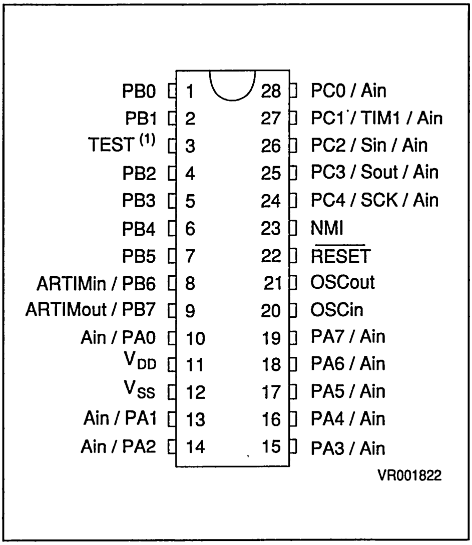
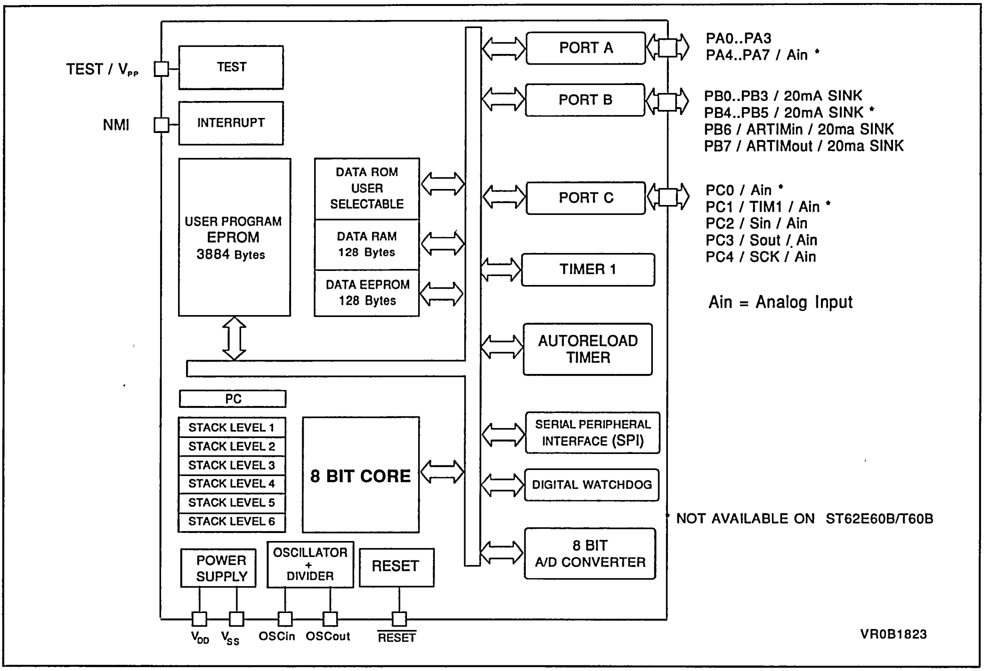


Figure 3. ST62E60B,E65B Block Diagram



GENERAL DESCRIPTION

The ST62E60B,T60B,E65B,T65B microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications.

They are the EPROM and OTP versions of the ST6260B and ST6265B devices. EPROM are suited for development. OTPs are suited for prototyping, preseries, low to mid volume series and inventory optimization for customer having several applications using the same MCU. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).

The macrocells of the ST62E60B, T60B, E65B and T65B are: the timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer1), the 8-bit Auto-reload Timer with 7 bit programmable prescaler (AR Timer), the 8-bit A/D Converter with up to 7 (ST62E60B,T60B) and up to 13 (ST62E65B,T65B) analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD) and an 8-bit Serial synchronous Peripheral Interface (SPI). In addition, these devices offer 128 bytes of EEPROM for non volatile data storage.

The ST62E60B, T60B, E65B and T65B are upward compatible with the ST62E60, T60, E65, T65. They in addition feature RC network, user configurable Power-on Reset Delay and an External STOP Mode Control option to enlarge the range of power consumption/safety trade-offs.

ST62E60B ,T60B, E65B and T65B are well suited for automotive, appliance and industrial applications.

PIN DESCRIPTION

V$_{DD}$ and V$_{SS}$. Power is supplied to the MCU using these two pins. V$_{DD}$ is power and V$_{SS}$ is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. Depending on the Option Byte, either a quartz crystal, a ceramic resonator, an external clock signal or an RC network can be connected in order to allow the correct operation of the MCU with various stability/cost trade-offs. The oscillator frequency is internally divided by 1, 2 or 4 by a software controlled divider.The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST/V$_{PP}$. The TEST must be held at V$_{SS}$ for normal operation. If TEST pin is connected to a +12.5V level during the reset phase, the EPROM programming Mode is entered.

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. It is provided with an on-chip pull-up resistor and Schmitt trigger characteristics.

When the External STOP Mode Control option is enabled, the NMI pin in addition enables a control of the way the STOP instruction is processed.

PC1/TIM1/Ain. This pin can be used as a Port C I/O bit, as Timer 1 I/O pin or as analog input for the on-chip A/D converter. This pin is available only on the ST62E65B and T65B (28 pin version). If programmed to be the Timer 1 pin, in input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time out occurs.
To use this pin as Timer 1 output a dedicated bit in the TIMER 1 Status/Control Register must be set. To use this pin as input pin the I/O pin has to be programmed as input. The analog mode should be programmed to use the line as an analog input.

PB6/ARTIMin, PB7/ARTIMout. These pins are either Port B I/O bits or the Input and Output pins of the Auto-reload Timer. To be used as timer input function PB6 has to be programmed as input with or without pull-up. A dedicated bit in the AR TIMER Mode Control Register sets PB7 as timer output function.

PA0-PA7. These 8 lines are organized as one I/O port (A). PA4-PA7 are not available on ST62E60B and T60B (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input, open-drain or push-pull output.

PB0-PB3, PB4, PB5. These 6 lines are organized as one I/O port (B). PB4, PB5 are available only on the ST62E65B and T65B (28 pin version). When the External STOP Mode Control is disabled, each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED and TRIAC driving. When the External STOP Mode Control is enabled, PB0 is forced as open drain output. The other lines are unchanged.

PC0-PC4. These 5 lines are organized as one I/O port (C). PC0 and PC1 are not available on ST62E60B, T60B (20 pin version). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input for the A/D converter, open-drain or push-pull output. PC2-PC4 can also be used as respectively Data in, Data out and Clock I/O pins for the on-chip SPI to carry the synchronous serial I/O signals.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6260B,65B ROM DEVICE FOR FURTHER DETAILS.

EPROM/OTP DESCRIPTION

The ST62E60B/E65B are the EPROM versions of the ST6260B/65B products. They are intended for use during the development of an application and for pre-production and small volume production. ST62T60B/T65B OTP have the same characteristics. They all include EPROM memory instead of the ROM memory of the corresponding ST6260B/65B, and so the program can be easily modified by the user with the ST62E6xB EPROM programming tools from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E60B/E65B and ST62T60B/T65B products have exactly the same software and hardware features as the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/VPP pin. The programming of the ST62E60B, T60B, E65B, T65B is described in the User Manual of the EPROM Programming Board.

The supply operating range is 3.5V to 6.0Von the OTP and the EPROM parts.
On the ROM version, the supply operating range is 3.0V to 6.0V.

Other than this exception, the OTP, EPROM and ROM parts are fully compatible. This datasheet thus provides only information specific to the EPROM based devices.

Note also the Low STOP mode consumption of ROM devices can not be emulated on EPROM or OTP devices

ROM Option Emulation

The ROM mask options that can be selected by the user in the ROM devices can be selected on the EPROM/OTP devices by an EPROM CODE byte that can be programmed with the ST62E6xB EPROM programming tools available from SGS-THOMSON. This EPROM CODE byte is automatically read, and the selected options enabled, when the chip reset is activated.

The Option byte is written during programming either by using the PC menu (PC driven Mode) or automatically (stand-alone mode).

EPROM Programming Mode

An additional mode is used to configure the part for programming of the EPROM, this is set by a 12.5V voltage applied to the TEST/VPP pin. The programming of the ST62E60B/E65B and ST62T60B/T65B is described in the User Manual of the EPROM Programming board.

EPROM ERASING

The EPROM of the windowed package of the ST62E60B/E65B may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E60B/E65B is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlights and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E60B/E65B packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the ST62E60B/E65B EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537A. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E60B/E65 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Table 1. ST62T60B/T65B OTP Memory Map

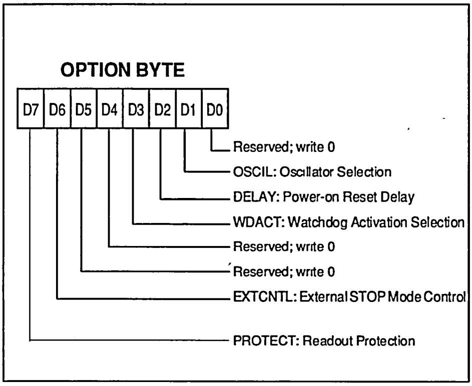
Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3856 Bytes
0FA0h-0FEFh 0FF0h-0FF7h 0FF8h-0FFBh 0FFCh-0FFDh 0FFEh-0FFFh	Reserved Interrupt Vectors Reserved NMI Vector User Reset Vector

Note. Reserved Areas should be filled with FFh

OPTION BYTE

The Option Byte enables emulation of the mask options of the ROM devices. It can only be accessed during the programming mode. This access is made either automatically (copy from a master device) or by selecting the “OPTION BYTE PROGRAMMING” mode of the programmer. The option byte is located in a non-user map. No address has to be specified.

Figure 4. EPROM Code Option Byte


OPTION BYTE
D7
D6
D5
D4
D3
D2
D1
D0
Reserved; write 0
OSCIL: Oscillator Selection
DELAY: Power-on Reset Delay
WDACT: Watchdog Activation Selection
Reserved; write 0
Reserved; write 0
EXTCNTL: External STOP Mode Control
PROTECT: Readout Protection

PROTECT. This bit allows the protection of the software contents against piracy. When the bit PROTECT is set high, readout of the OTP contents is prevented by hardware. No programming equipment is able to gain access to the user program. When this bit is low, the user program can be read. This bit emulates the READOUT PROTECTION mask option of ROM devices.

EXTCNTL. This bit selects the External STOP Mode capability. When EXTCNTL is high, pin NMI controls if the STOP mode can be accessed when the watchdog is active. In addition, PB0 is forced as open drain output. When EXTCNTL is low, the STOP instruction is processed as a WAIT as soon as the watchdog is active. This bit emulates the EXTERNAL STOP MODE CONTROL of ROM devices.

D5-D4. Reserved. Must be cleared to zero.

WDACT. This bit controls the watchdog activation. When it is high, hardware activation is selected. The software activation is selected when WDACT is low.This bit emulates the WATCHDOG ACTIVATION mask option of ROM devices.

DELAY. This bit enables the selection of the delay internally generated after pin RESET is released. When DELAY is low, the delay is 2048 cycles of the oscillator, it is of 32768 cycles when DELAY is high. This bit emulates the POWER ON RESET DELAY mask option of ROM devices.

OSCIL. When this bit is low, the oscillator must be controlled by a quartz crystal, a ceramic resonator or an external frequency. When it is high, the oscillator must be controlled by an RC network, with only the resistor having to be externally provided. This bit emulates the OSCILLATOR mask option of ROM devices.

D0. Reserved. Must be cleared to zero.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

Tj = T_A + PD x RthJA

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = I_{DD} x V_{DD} (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50(2)	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

- (2) The total current through ports A and B combined may not exceed 50 mA. The total current through port C may not exceed 50 mA. If the application is designed with care and observing the limits stated above, total current may reach 100 mA.

THERMAL CHARACTERISTIC

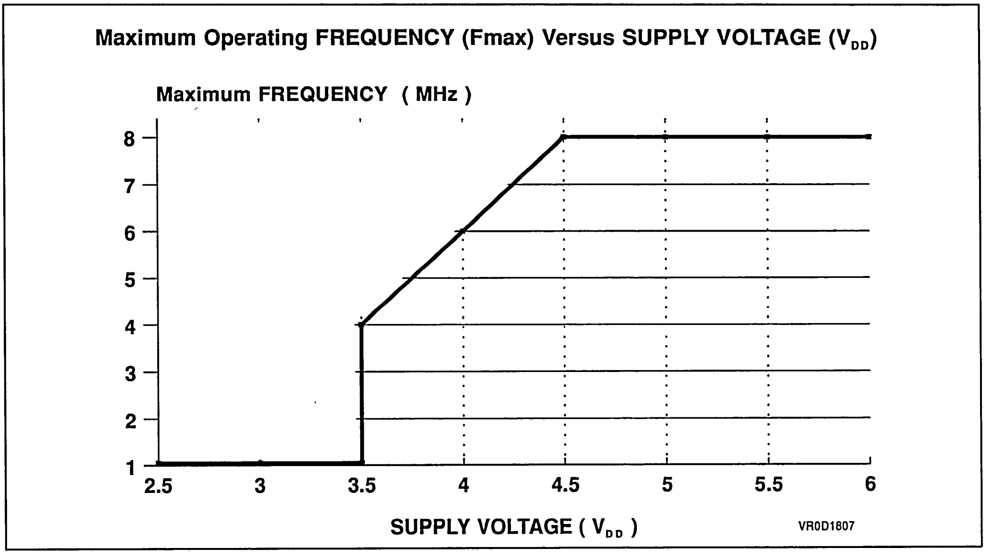
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 4MHz f_{INT} = 4MHz	3.5		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
V_{PP}	EPROM Prog. Voltage		12	12.5	13	V
f_{INT}	Internal Frequency	V_{DD} = 3.5V V_{DD} = 4.5V	0 0		4.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input [(1)] Analog Inputs[(2)]	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input [(1)] Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

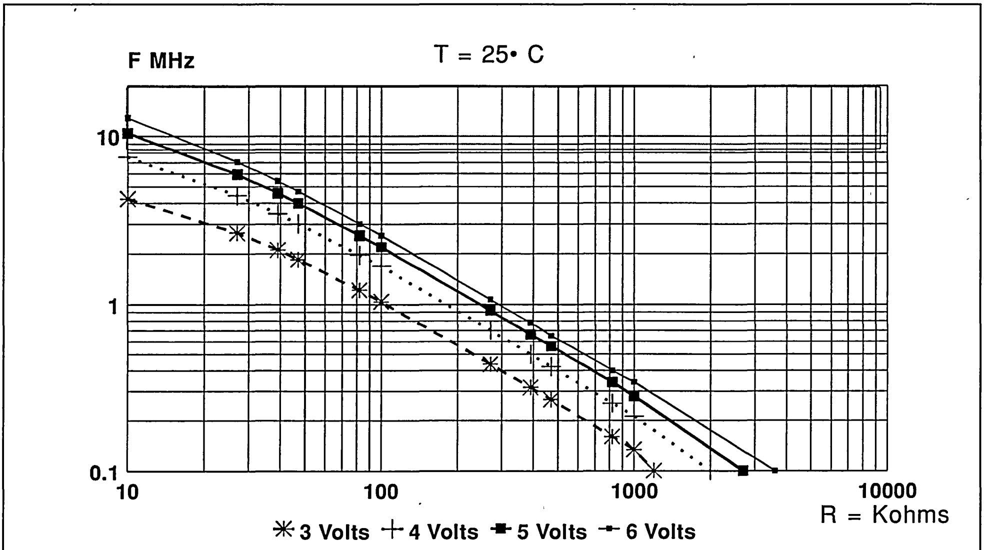
Notes :

1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (~ 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An internal frequency above 1MHz is recommended for reliable A/D results.



The shaded area is outside the device operating range, device functionality is not guaranteed.

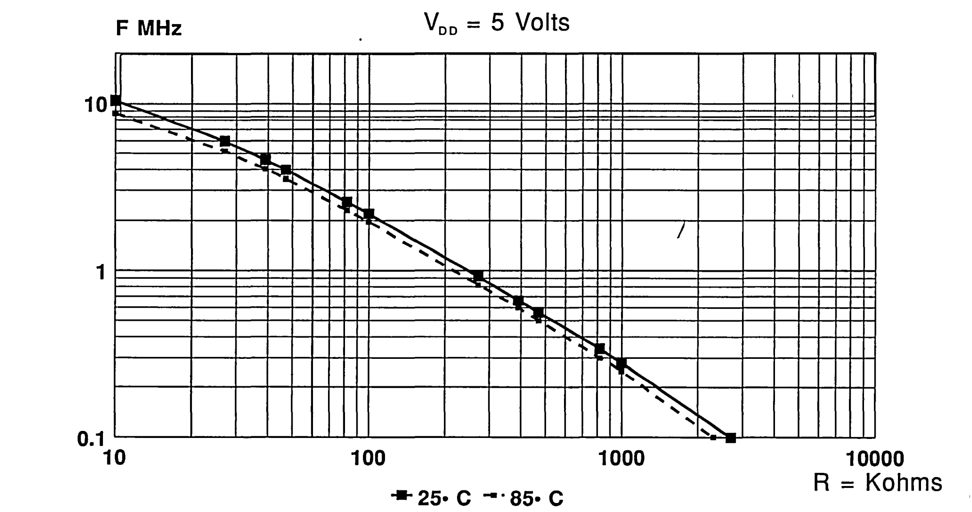
RC Oscillator. fOSC Frequency versus RNET (Typical Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

VR01935

RC Oscillator. fOSC Frequency versus RNET (Typical Values)



The shaded area is outside ST62xxB operating range, device functionality is not guaranteed

VR01935A

DC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage All inputs				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage All inputs		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage [4] All Inputs	V_{DD}=5V V_{DD}=3V	0.2 0.2			V
V_{OL}	Low Level Output Voltage Port A, C	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL} = +5.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OL}	Low Level Output Voltage Port B	V_{DD}=4.5V I_{OL} = +1.6mA V_{DD}=4.5V I_{OL}=+20.0mA V_{DD}=3.0V I_{OL} = +0.7mA			0.4 1.3 0.4	V
V_{OH}	High Level Output Voltage Port A, B, C	V_{DD}=4.5V I_{OL} = -1.6mA V_{DD}=4.5V I_{OL} = -5.0mA V_{DD}=3.0V I_{OL} = -0.7mA	4.1 3.5 2.6			V
I_{PU}	Input Pull-up Current Input Mode with Pull-up Port A, B, C, NMI	V_{IN} = V_{SS}, V_{DD}=3-6V			100	µA
I_{IL} I_{IH}	Input Leakage Current(1)	V_{IN} = V_{SS} V_{IN} = V_{DD}			1.0	µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}=V_{SS} f_{OSC}=8MHz			3.5	mA
	Supply Current in RUN Mode [2]	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			6.6 TBD	mA
	Supply Current in WAIT Mode [3]	V_{DD}=5.0V f_{INT}=8MHz V_{DD}=3.0V f_{INT}=4MHz			1.50 TBD	mA
	Supply Current in STOP Mode[3]	I_{LOAD}=0mA V_{DD}=5.0V			10	µA

Notes :

1.Only when pull-ups are not inserted
2.All peripherals running
3.EEPROM and A/D Converter in Stand-by
4.Hysteresis voltage between switching levels

AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

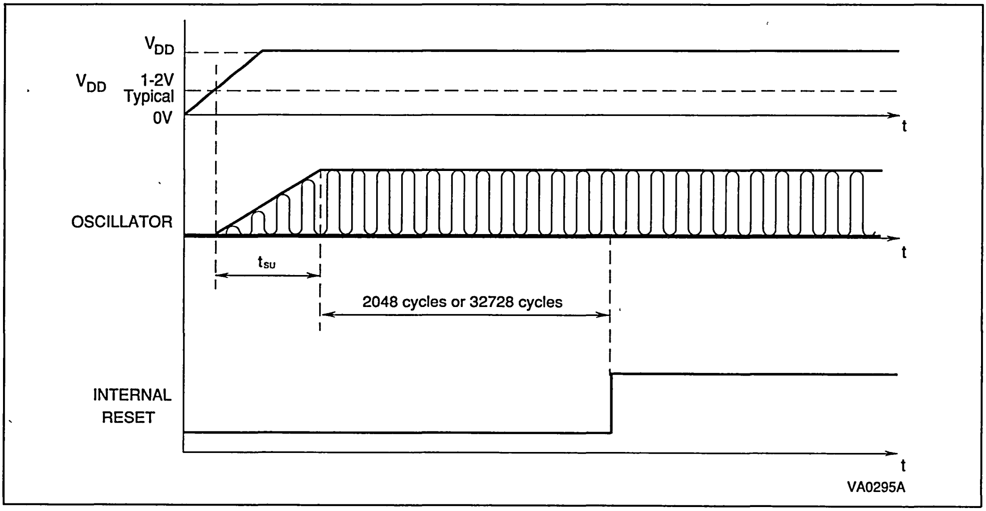
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.5V V_{DD} = 4.0V V_{DD} = 4.5V			4 6 8	MHz
t_{SU}	Oscillator Start-up Time at Power On [2]	Ceramic Resonator $C_{L1} = C_{L2}$ = 22pF		5	100	ms
t_{SUS}	Oscillator STOP mode Recovery Time [2]	8MHz Ceramic Resonator CL1=C_{L2}=22pF		0.2	100	
		8MHz Quartz CL1=C_{L2}=22pF		10	100	
t_{REC}	Supply Recovery Time [1]		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
T_{WEE}	EEPROM Write Time	T_A = 25°C T_A = 85°C T_A = 125°C		5 10 20	10 20 30	ms
Endurance	EEPROM WRITE/ERASE Cycle	Q_A L_{OT} Acceptance	300,000			cycles
Retention	EEPROM Data Retention	T_A = 55°C	10			years
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:

[1] Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.

[2] See Figure 59. This value is highly dependent on the Ceramic Resonator or Quartz Crystal used in the application.

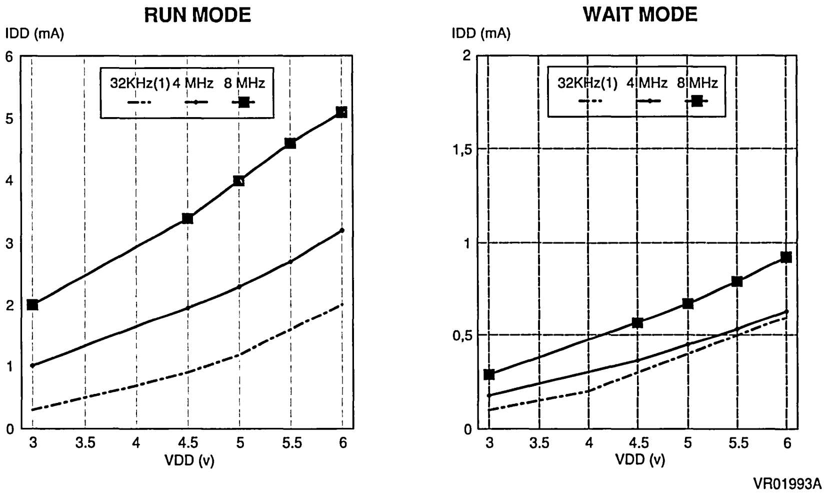
Figure 5. Power On Reset



ELECTRICAL CHARACTERISTICS (Continued)

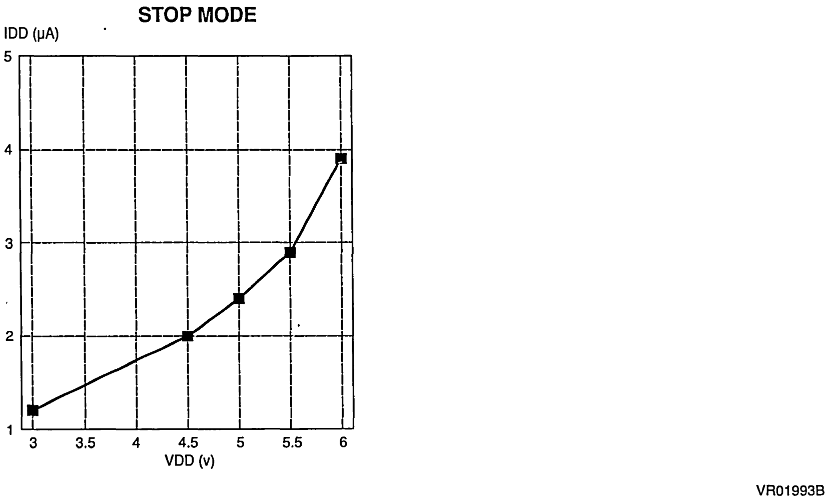
CURRENT CONSUMPTION

IDD Current Versus Supply Voltage Typical Values (TA : +85°C)



Note (1) : Using the network described in the Application Note AN673

IDD Current Versus Supply Voltage Typical Values(TA : +85°C)



I/O PORT CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA , Port B I_{OL}= 20mA , Port B			 0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		 0.1 0.1	 1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	KΩ

SPI CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CL}	Clock Frequency at SCK				500	kHz
t_{SV}	Data Set up time on Sin			TBD		
t_H	Data hold time on Sin			TBD		
t_{TS}	Delay Transmission started on Sin	8MHz	0	Note 1		µs

Note :

1. Minimum time 0µs
Maximum time 1 instruction cycle

TIMER1 CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIM1 Pin(1)				$\frac{f_{INT}}{4}$	MHz
t_W	Pulse Width at TIM1 Pin(1)	V_{DD} = 3.5V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

Note:

1.Not available for ST6260B

AR TIMER CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{1}{f_{INT}}$			s
f_{ARin}	Input Frequency on ARTIMin pin	STOP Mode RUN and WAIT Modes			2 $\frac{f_{INT}}{4}$	MHz MHz
t_W	Pulse Width at ARTIMin Pin	V_{DD} = 3.5V V_{DD} = 4.5V V_{DD} = 5.5V	125 125 125			ns ns ns

A/D CONVERTER CHARACTERISTICS
(T_A= -40 to +85°C unless otherwise specified)

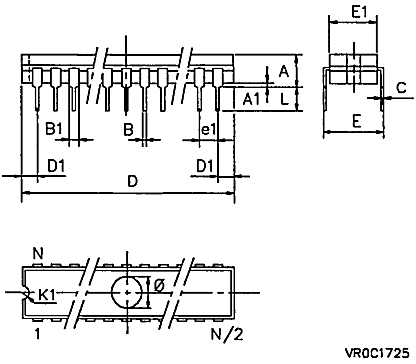
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy [1] [2]	f_{OSC} > 1.2MHz f_{OSC} > 32kHz			±2 ±4	LSB
t_C[2]	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when Vin = V_{SS}	00			Hex
FSR	Full Scale Reading	Conversion result when Vin = V_{DD}			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN}[3]	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance [4]				30	kΩ

Notes:

1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

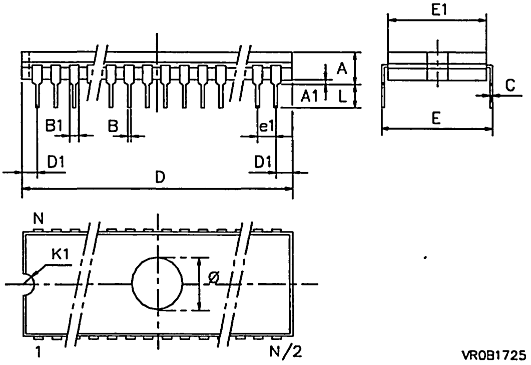
PACKAGE MECHANICAL DATA

Figure 6. 20-Lead Frit Seal Ceramic Dual in Line Package, 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.27		1.52	0.050		0.060
C	0.22		0.31	0.009		0.012
D			26.92			1.059
D1	0.51		1.27	0.020		0.050
E	–	–	–	–	–	–
E1			7.80			0.307
L	3.40			0.134		
e1	2.29		2.79	0.090		0.110
Ø	4.24		4.39	0.167		0.173
	Number of Pins					
N	20					

Figure 7. 28-Lead Frit Seal Ceramic Dual in Line Package, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0 022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3 00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					

ORDERING INFORMATION

ORDERING INFORMATION TABLE

Sales Types	OTP/EPROM	I/O	Temperature Range	Package
ST62T60BB6	OTP 4K Bytes	13	-40°C to 85°C	PDIP20
ST62T60BM6				PSO20
ST62T65BB6		21		PDIP28
ST62T65BM6				PSO28
ST62E60BF1	EPROM 4K Bytes	13	0°C to 70°C	CDIP20
ST62E65BF1		21		CDIP28

ST623x Family
FUNCTIONAL DESCRIPTION

ST623x DATASHEET INDEX

Page Number

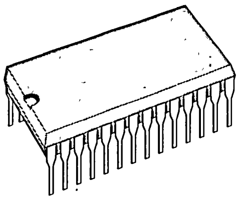
SGS-THOMSON
MICROELECTRONICS

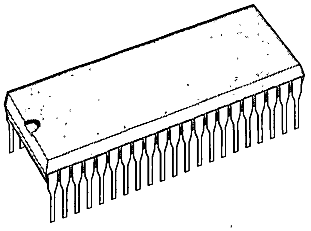
ST623x

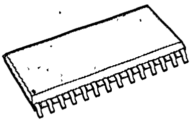
8-BIT HCMOS MCUs WITH A/D CONVERTER, EEPROM, UART & 16-BIT AUTO-RELOAD TIMER

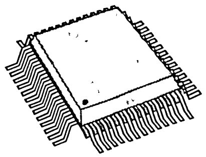
FUNCTIONAL DESCRIPTION

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 8K bytes
- Data ROM: User selectable size (in program ROM)
- Data RAM: 192 bytes
- EEPROM: 128 bytes
- PDIP28, PSO28 package (ST6230)
- SDIP42 package (ST6232)
- PQFP52 package (ST6235)
- Up to 36 fully software programmable I/O as:
  – Input with pull-up resistor
  – Input without pull-up resistor
  – Input with interrupt generation
  – Open-drain or push-pull outputs
  – Analog Inputs
- Up to 12 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (TIMER 1)
- 16 bit Auto-reload Timer (ARTIM16)
- Digital Watchdog
- 8 bit A/D Converter with up to 24 multiplexed analog inputs
- 8 bit Asynchronous Peripheral Interface (UART)
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator driven by Quartz Crystal or Ceramic resonator
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The development tool of the ST623x microcontrollers consists of the ST623x-EMU emulation and development system connected via a standard RS232 serial line to an MS-DOS Personal Computer


PDIP28


PSDIP42


PSO28


PQFP52

(Ordering Information at the end of the datasheet)

This is a functional description Data from SGS-THOMSON. Details are subject to change without notice.

GENERAL DESCRIPTION

The ST623x microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells). The macrocells of the ST623x areas follows:

- the Timer peripheral that includes a 16-bit autoreload timer with compare and capture modes (ARTIMER16) and an 8-bit counter with a 7-bit software programmable prescaler (Timer1)
- the 8-bit A/D Converter with up to 24 multiplexed analog inputs (A/D inputs are alternate functions of I/O pins)
- an 8-bit Serial synchronous Peripheral Interface (SPI)
- a Serial Asynchronous Peripheral (UART)
- a Digital Watchdog (DWD)

In addition these devices offer 128bytes of EEPROM, 192 bytes of RAM and 8K bytes of ROM. ST623x are well suited for automotive, home appliances and industrial applications. The ST62E3x EPROM versions are available for prototypes and field test; also ST62T3x OTP (One Time Programmable) versions are available.

Figure 1. ST623x Block Diagram

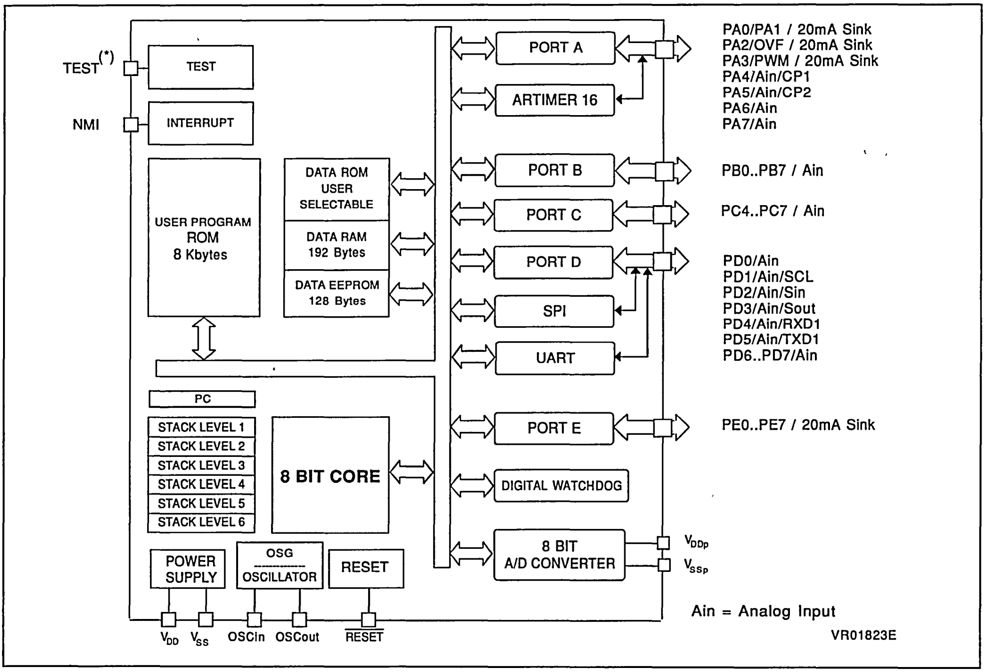
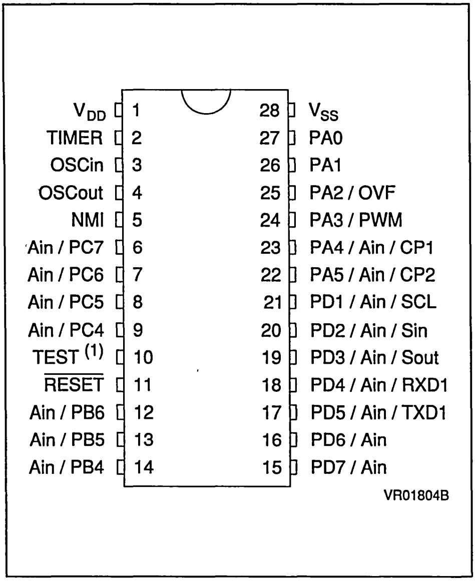


Figure 2. ST6230 Pin Configuration



Note 1: This pin is also the V_{PP} input for EPROM based devices

Figure 3. ST6232 Pin Configuration

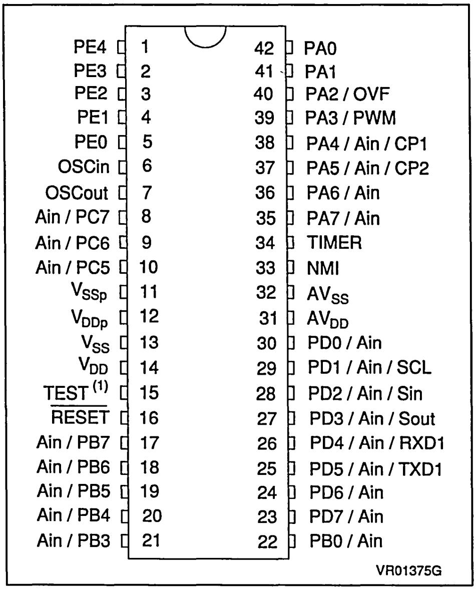
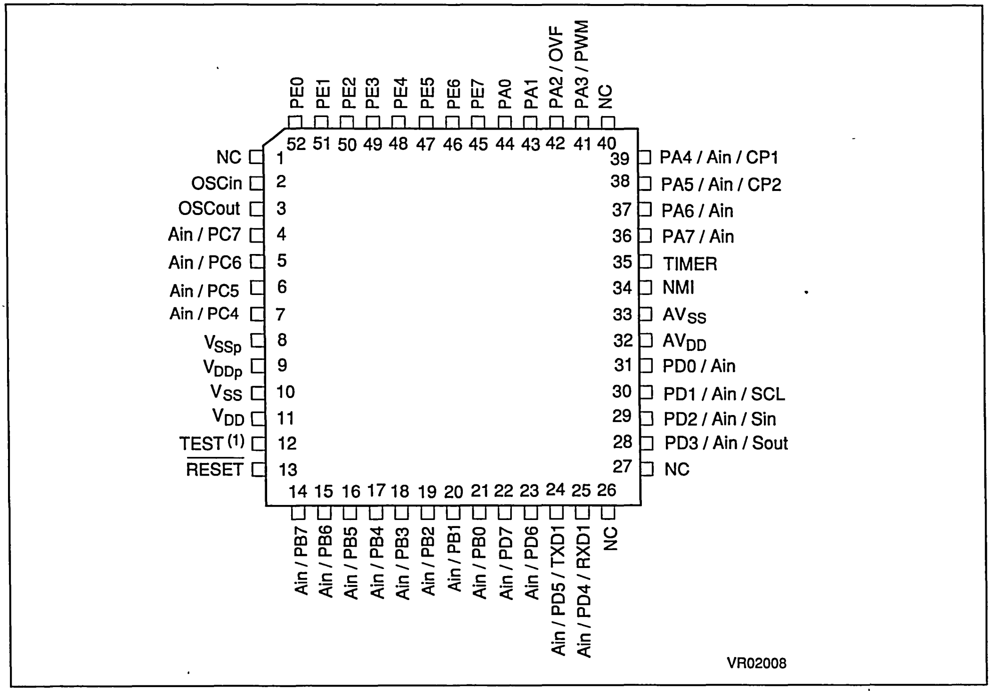


Figure 4. ST6235 Pin Configuration



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU logic (except A/D converter and I/O pins) using these two pins. V_{DD} is power and V_{SS} is the ground connection.

V_{DDp} and V_{SSp}. Power is supplied to the MCU I/Os independently from the rest of the chip using these two pins. These pins have to be connected to the V_{DD} and V_{SS} pins. It is not allowed to leave any of these pins unconnected or to apply different potentials respectively to V_{DD}/V_{DDp} and V_{SS}/V_{SSp}.

AV_{DD} and AV_{SS}. Power is supplied to the MCU A/D converter independently from the rest of the chip using these two pins.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins. Also an external clock signal can be supplied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST pin must be held at Vss for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for an asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive. It is provided with an on-chip pull-up resistor and Schmitt trigger characteristics.
The user can select as Run mask option (see option list at the end of the datasheet) the availability of an on-chip pull-up at this pin. On EPROM/OTP versions the selection is made by EPROM option.

PC4/PC7. These 4 lines are organised as one I/O port (port C). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input open-drain or push-pull output.

PB0/PB7. These 8 lines are organised as one I/O port (port B). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input open-drain or push-pull output.

PD0/PD7. These 8 lines are organised as one I/O port (port D). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, analog input open-drain or push-pull output. In addition, the pins PD5/TXD1 and PD4/RXD1 can be used as UART input (PD5/TXD1) or UART output (PD4/RXD1). The pins PD3/Sout, PD2/Sin and PD1/SCL can also be used respectively as data Out, data In and Clock pins for the on-chip SPI.

TIMER. This is the TIMER 1 I/O pin. In input mode, it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In output mode, the TIMER pin outputs the data bit when a time-out occurs.
The user can select as Run mask option (see option list at the end of the datasheet) the availability of an on-chip pull-up at this pin. On EPROM/OTP versions the selection is made by EPROM option.

PA0/PA7. These 8 lines are organized as one I/O port (port A). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. In addition, the pins PA5/CP2, PA4/CP1, PA3/PWM, PA2/OVF can be used respectively as Compare Inputs, PWM output and Overflow output pins for the on-chip ARTIMER16. PA0/PA3 can sink 20mA in output mode. PA4/PA7 can be configured as analog inputs.

PE0/PE7. These 8 lines are organized as one I/O port (PE). Each line may be configured under software control as input with or without internal pull-up resistor, interrupt generation input with pull-up resistor, open-drain or push-pull output. In output mode, these lines can also sink 20mA for direct LED and TRIAC driving.

MEMORY SPACES

The MCU operates in three different memory spaces: program space, data space, and stack space. A description of these spaces is shown in the following figures.

Program Space

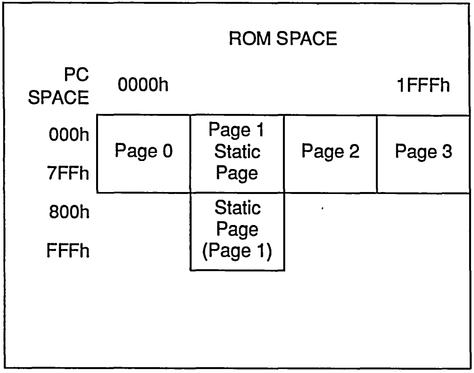
The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and the user vectors. It is addressed by the 12-bit Program Counter register (PC register) and so the ST62xx core can directly address up to 4K bytes of Program Space. Nevertheless, the Program Space can be extended by the addition of 2K byte ROM banks as it is shown in the following figure in which the ST623x 8K byte memory is described.

The ST623x program space can be protected against external reading of the ROM contents when the READOUT PROTECTION mask option is selected. If this option is selected, the user can blow a dedicated fuse on the silicon by applying a high voltage at V_{PP}, (see detailed information in the "Electrical Specification").

Note:

Once the fuse is blown, it is no longer possible, even for SGS-THOMSON, to gain access to the ROM contents. Returned parts with blown fuse can therefore not be accepted.

Figure 5. ST623x 8K bytes Program Space Addressing Description



MEMORY SPACES (Continued)

Data Space

The instruction set of the ST62xx core operates on a specific space, named Data Space, that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM and EEPROM memory, ST62xx core/peripheral registers, and read-only data such as constants and look-up tables.

Data ROM. All the read-only data is physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory contains consequently the program to be executed, the constants and the look-up tables needed for the program.

The locations of Data Space in which the different constants and look-up tables are addressed by the ST62xx core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory .

Data RAM/EEPROM.The ST623x offer 192 bytes of data RAM memory and 128 bytes of EEPROM. 64 bytes of RAM are directly addressed in data space in the range 080h-0BFh (static space). The additional RAM and EEPROM are addressed using the banks of 64 bytes located between addresses 00h and 3Fh.

Stack Space

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

Figure 6. ST623x Data Memory Space

DATA and EEPROM	000h 03Fh
DATA ROM WINDOW AREA	040h 07Fh
X REGISTER	080h
Y REGISTER	081h
V REGISTER	082h
W REGISTER	083h
DATA RAM	084h 0BFh
PORT A DATA REGISTER	0C0h
PORT B DATA REGISTER	0C1h
PORT C DATA REGISTER	0C2h
PORT D DATA REGISTER	0C3h
PORT A DIRECTION REGISTER	0C4h
PORT B DIRECTION REGISTER	0C5h
PORT C DIRECTION REGISTER	0C6h
PORT D DIRECTION REGISTER	0C7h
INTERRUPT OPTION REGISTER	0C8h*
DATA ROM WINDOW REGISTER	0C9h*
ROM BANK SELECT REGISTER	0CAh*
RAM/EEPROM BANK SELECT REGISTER	0CBh*
PORT A OPTION REGISTER	0CCh
PORT B OPTION REGISTER	0CDh
PORT C OPTION REGISTER	0CEh
PORT D OPTION REGISTER	0CFh
A/D DATA REGISTER	0D0h
A/D CONTROL REGISTER	0D1h
TIMER 1 PRESCALER REGISTER	0D2h
TIMER 1 COUNTER REGISTER	0D3h
TIMER 1 STATUS/CONTROL REGISTER	0D4h
RESERVED	0D5h
UART DATA SHIFT REGISTER	0D6h
UART STATUS CONTROL REGISTER	0D7h
WATCHDOG REGISTER	0D8h
RESERVED	0D9h
I/O INTERRUPT POLARITY REGISTER	0DAh
OSG STATUS CONTROL REGISTER	0DBh
SPI INTERRUPT DISABLE REGISTER	0DCh*
SPI DATA REGISTER	0DDh
RESERVED	0DEh
EEPROM CONTROL REGISTER	0DFh
TIM16 COMPARE MASK REGISTER LOW BYTE T16MSKL	0E0h
TIM16 2ND STATUS CONTROL REGISTER T16SCR2	0E1h
TIM16 3RD STATUS CONTROL REGISTER T16SCR3	0E2h
TIM16 4TH STATUS CONTROL REGISTER T16SCR4	0E3h
TIM16 1ST STATUS CONTROL REGISTER T16SCR1	0E8h
TIM16 RELOAD CAPTURE REGISTER HIGH BYTE T16RLCPH	0E9h
TIM16 RELOAD CAPTURE REGISTER LOW BYTE T16RLCPL	0EAh
TIM16 CAPTURE REGISTER HIGH BYTE T16CPH	0EBh
TIM16 CAPTURE REGISTER LOW BYTE T16CPL	0ECh
TIM16 COMPARE VALUE REGISTER HIGH BYTE T16CMPH	0EDh
TIM16 COMPARE VALUE REGISTER LOW BYTE T16CMPL	0EEh
TIM16 COMPARE MASK REGISTER HIGH BYTE T16MSKH	0EFh
RESERVED	0F0h 0FBh
PORT E DATA REGISTER	0FCh
PORT E DIRECTION REGISTER	0FDh
PORT E OPTION REGISTER	0FEh
ACCUMULATOR	0FFh

* WRITE ONLY REGISTER

INTERRUPTS

The ST62xx core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 4). When a source provides an interrupt request, and the request processing is also enabled by the ST62xx core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction).
Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The ST623x microcontrollers have eleven different interrupt sources associated to five interrupt vectors as it is described in table below.

Table 1. Interrupt Vector/Source Relationship

Interrupt Source	Vector	Vector Address
NMI & Port C	Interrupt vector #0	(FFCh, FFDh)
SPI, Port E & A	Interrupt vector #1	(FF6h, FF7h)
Port B & D	Interrupt vector #2	(FF4h, FF5h)
ARTIMER16	Interrupt vector #3	(FF2h, FF3h)
UART, TIMER1 & ADC	Interrupt vector #4	(FF0h, FF1h)

Interrupt Vectors Description

The ST62xx core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines in the static page of the Program Space.

- The interrupt vector associated with the non-maskable interrupt source and Port C is named interrupt vector #0. It is located at addresses FFCh,FFDh in the Program Space. This vector is associated with the external falling edge sensitive interrupt pin (NMI). Port C interrupt can be programmed by software either in falling or rising edge mode according to the code loaded in the I/O Interrupt Polarity Register (IPR).
- The interrupt vector located at addresses FF6h, FF7h is named interrupt vector #1. It is associated with Port E and Port A pins. It can be programmed by software either in the falling or rising edge detection mode or in the low level or high level sensitive detection mode according to the code loaded in the Interrupt Option Register (IOR) and in the I/O Interrupt Polarity Register (IPR). It is also associated to the SPI cell.
- The interrupt vector located at addresses FF4h, FF5h is named interrupt vector #2. It is associated with Port B & D. It can be programmed by software either in the falling edge detection mode or in the positive edge detection mode according to the code loaded in the Interrupt Option Register (IOR) and in the I/O Interrupt Polarity Register (IPR).
- The interrupt vector located at addresses FF2h, FF3h is named interrupt vector #3. It is associated with the ARTIMER16 peripheral.
- The interrrupt vector loaded at address FF0h, FF1h is named interrupt vector #4. It is associated with the TIMER 1, the A/D converter and the UART peripherals.

All the on-chip peripherals have an interrupt request flag bit (TMZ for timer, EOC for A/D). This bit is set to one when the device wants to generate an interrupt request and a mask bit (ETI for timer, EAI for A/D) that must be set to one to allow the transfer of the flag bit to the core.

Interrupt Priority

The non-maskable interrupt request NMI has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the four other interrupts can not interrupt each other. If more than one interrupt request are pending, they are processed by the ST62xx core according to their priority level: vector #1 has the higher priority while vector #4 the lower.
The priority of each interrupt source is fixed.

INPUT/OUTPUT PORTS

The ST623x microcontrollers have up to 36 Input/Output lines that can be individually programmed either in the input mode or the output mode with the following software selectable options:

- Input without pull-up and without interrupt
- Input with pull-up and with interrupt
- Input with pull-up without interrupt
- Analog inputs (PA4-PA7, PB0-PB7, PC4-PC7, PD0-PD7)
- Timer 1 I/O line
- ARTIMER16 I/O lines (PA2-PA5)
- SPI control signals (PD1-PD3)
- Push-pull output
- Standard Open drain output
- 20mA Open drain output (PA0-PA3,PE0-PE7) lines.

The lines are organised in five Ports (Port A, B, C, D and E).

Each port occupies 3 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data, Direction and Option registers are associated with the PA0 line of Port A).

The five DATA registers (DRA, DRB, DRC, DRD and DRE) are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port data registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related option registers, to select the different input mode options.

Single-bit operations on I/O DATA registers are possible but care is necessary because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired change of the input configuration.

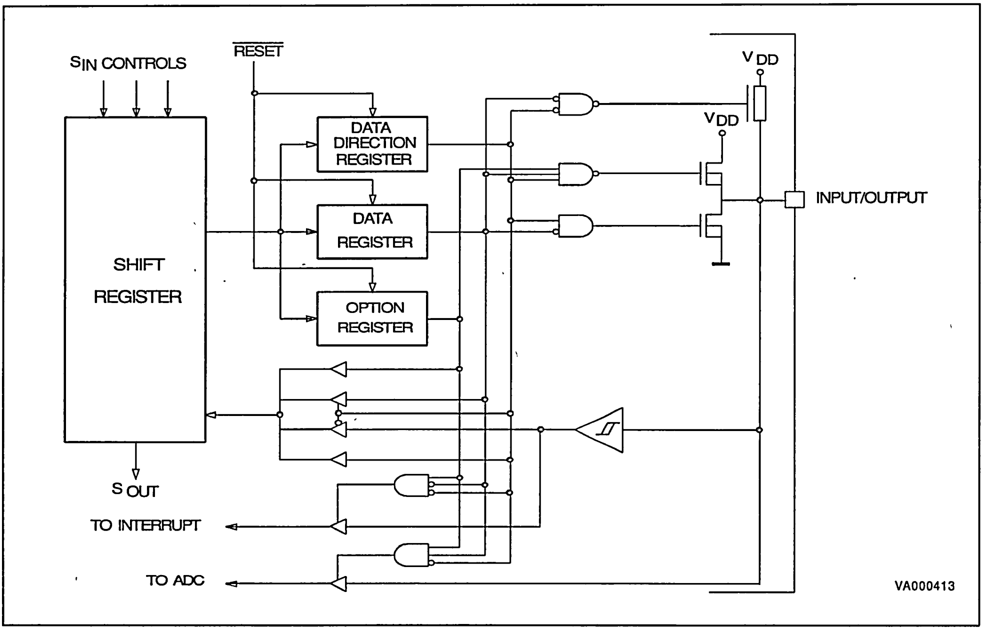
The five Data Direction registers (DDRA, DDRB, DDRC, DDRDand DDRE) allow the selection of the data direction of each pin (input or output).

The five Option registers (ORA, ORB, ORC, ORD and ORE) are used to select the different port options available both in input and in output mode.

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up/no-interrupt is selected on all the pins, thus avoiding pin conflicts, if ROM option 7 is reset to 0.

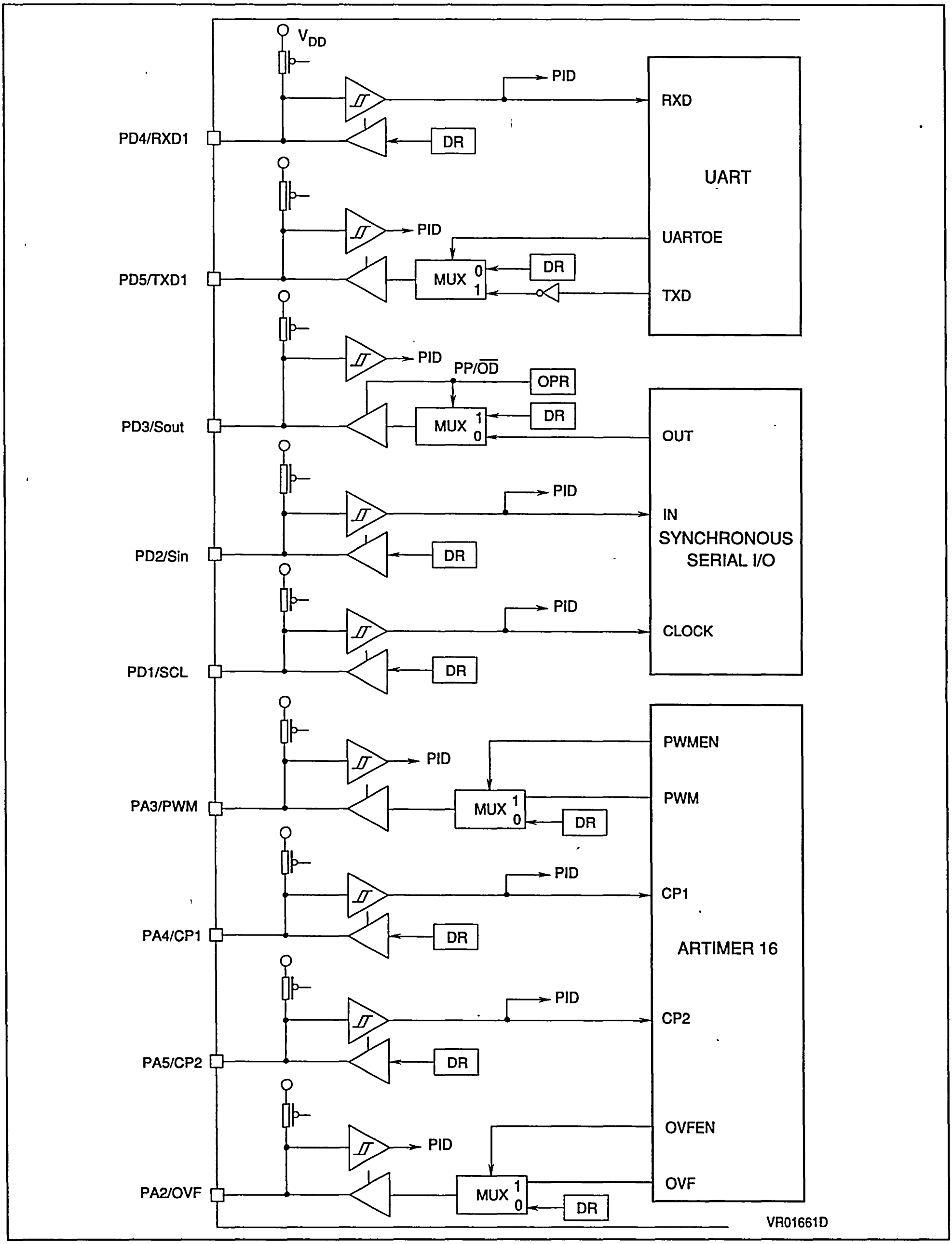
If ROM option 7 is set to 1 I/O data registers are set to FF at reset, selecting input mode without pull-up/no interrupt on all the I/O pins. All I/O pins will float at high impedance in that state.

Figure 7. I/O Port Block Diagram



INPUT/OUTPUT PORTS (Continued)

Figure 8. Peripheral Interface Configuration of SPI, Timer 1 and ARTIMER16



Note : PID means Port Input Data

TIMERS

The ST623x offers two on-chip Timer peripherals named Timer 1 and Auto-reload Timer 16. Timer 1 consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and control logic that allows configuring the peripheral in three operating modes. The Auto-reload Timer is an 16-bit Timer with Auto-reload, Input Capture and Output Compare capabilities. 4 modes are available for PWM, PLL, time measurement and period measurement.

Timer 1

Figure 33 shows the Timer 1 block diagram. An external Timer pin is available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR1 which is addressed in the data space as a RAM location at addresses D3h. The state of the 7-bit prescaler is read in the PSC1 register at address D2h. The control logic device is managed in the TSCR1 register (addresses D4h) as described in the following paragraphs.

The 8-bit counter is decremented by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (Timer Zero) bit in the TSCR1 is set to one. If the ETI (Enable Timer Interrupt) bit in the TSCR1 is also set to one an interrupt request, associated to interrupt vector #4, is generated. The interrupt service routine then should poll bit TMZ in TSCR1 to determine if the interrupt has been generated by UART, Timer 1 or by the A/D Converter. The Timer 1 interrupt can be used to exit the MCU from the WAIT mode.

The Timer 1 Prescaler input can be the internal clock divided by 12 or an external clock at the Timer I/O pin. The prescaler decrements on the rising edge. Depending on the division factor programmed by PS2, PS1 and PS0 bits in TSCR1, the clock input of the timer/counter register is multiplexed to different sources. On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR1. This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC1 is connected to clock input of TCR1, and so on. The prescaler initialize bit PSI in the TSCR1 register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting. The prescaler can be given any value between 0 and 7Fh by writing to addresses D2h, if bit PSI in the TSCR1 register is set to one. The tap of the prescaler is selected using the PS2,PS1,PS0 bits in the control register. Figure 34 shows the Timer 1 working principle.

Timer Operating Modes

There are 3 operating modes of the Timer1 peripheral. They are selected by the bits TOUT and DOUT (see TSCR1 register). These three modes correspond to the two-clock frequencies that can be connected on the 7-bit prescaler (f_{OSC}/12 or TIMER pin signal) and to the output mode.

TIMERS (Continued)

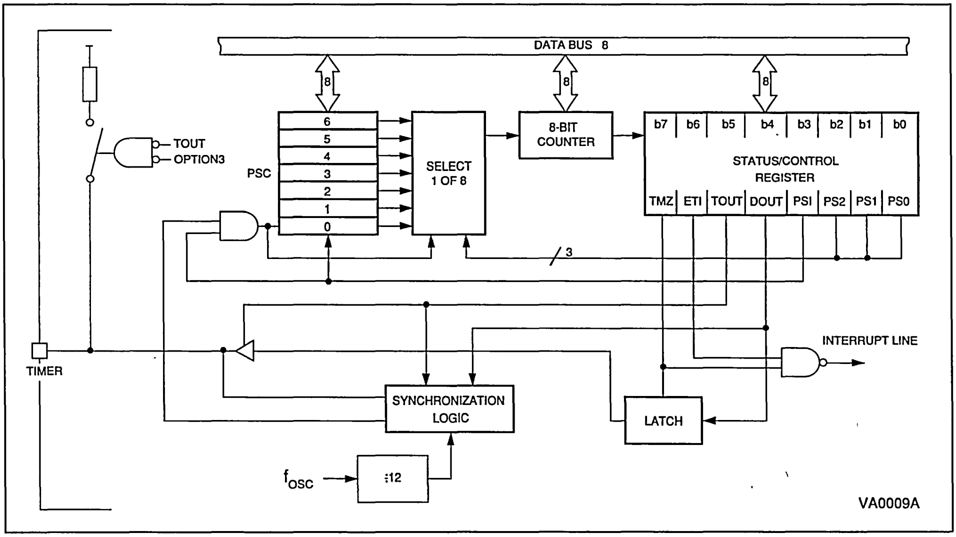
Clock Input Mode (TOUT = "0", DOUT = "0"). In this mode the TIMER pin is an input and the prescaler is decremented on rising edge. The maximum input frequency that can be applied to the external pin in this mode is 1/8 of the oscillator frequency.

Gated Mode (TOUT = "1", DOUT = data out). In this mode the prescaler is decremented by the Timer clock input (oscillator divided by 12) but ONLY when the signal at TIMER pin is held high (giving a pulse width measurement potential). This mode is selected by the TOUT bit in TSCR register cleared to "0" (i.e. as input) and DOUT bit set to "1".

Output Mode (TOUT = "1", DOUT = data out). The TIMER pin is connected to the DOUT latch. Therefore the timer prescaler is clocked by the prescaler clock input (f_{OSC}/12).

In clock input mode and gated mode (TOUT = "0") a pull-up device is connected to TIMER pin if ROM option 3 is set to 0, providing a high level resistance at this pin. If ROM option 3 is set to 1 the pull-up is off and the TIMER pin is floating at high impedance.

Figure 9. Timer 1 Peripheral Block Diagram



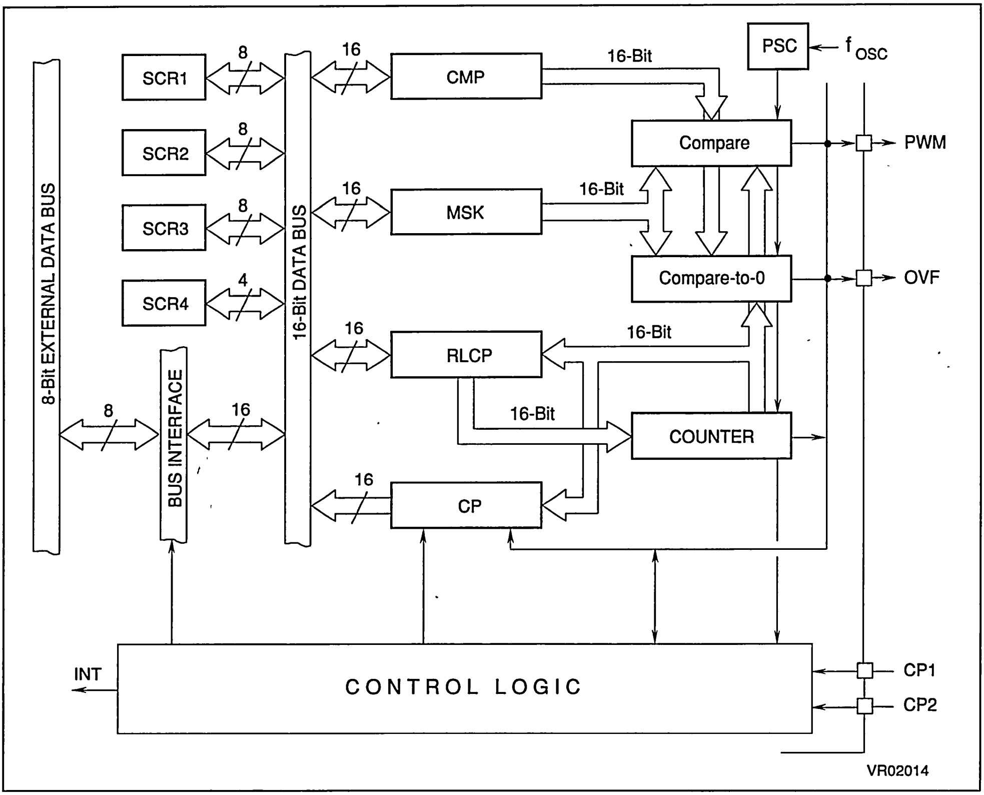
ARTIMER 16

The ARTIMER 16 is a powerful 16-bit timer module. It includes PWM and frequency output modes, with versatile capture and compare modes for resolving many timing requirements. Most of the ARTIMER16 modes can run in parallel with minimum user overhead.

All timer registers in the ARTIMER16 are 16-bit, and are accessed from the 8-bit internal bus. The full 16-bit word is written in two bytes, the high byte first and then the low byte. The high byte is stored in an intermediate register and is written to the target 16-bit register at the same time as the write to the low byte. This high byte will remain constant if further writes are made to the low bytes, until the high byte is changed. Full Read/Write access is available to all registers except where indicated.

The ARTIMER16 includes four 16-bit registers, four 8-bit status/control registers and the associated control logic. Two outputs provide PWM and Overflow (OVF) output signals each with programmable polarity, and two inputs CP1 and CP2 control start-up, capture and/or reload operations on the central counter.

Figure 10. ARTIMER16 Block Diagram



ARTIMER 16 (Continued)

The central counter is a 16-bit synchronous down counter which accepts the buffered Oscillator clock through a prescaler with a programmable division ratio (1/1, 1/4, 1/16). This counter can be Reloaded on an event on the input pins, or on an overflow, and its value can be stored into the Capture registers on an external event.

The value in the counter is continuously compared to the value programmed into the Compare Register, and when a match is made the PWM output bit may be toggled or Set/Reset. When the counter value is zero, the OVF overflow output bit can be set or toggled and, in PWM mode with Set/Reset, the PWM output bit is Reset/Set.

The range of the comparison register can be modified by using the Mask register which offers the capability to reduce the number of bits used in the comparison, thus lowering the period and increasing the frequency.

To allow very low power standby operation, and to allow a synchronous startup, the clock to the counter can be stopped, and the comparisons put on hold. This signal (RUNRES) must be active to use the ARTIMER16.

The operational modes of the ARTIMER16 are:

PWM generation

Frequency Generation

Reload Functions

Capture Functions

DIGITAL WATCHDOG

The digital Watchdog of the ST623x device consists of a down counter that can be used to provide a controlled recovery from a software upset.

The Watchdog generates a system reset when the counter passes 00h. User software can prevent the reset by reloading the counter. User software should therefore be written in such a way that the counter is regularly reloaded as long as the software runs correctly. In the case of software upset (e.g. infinite loop or power supply fail), user software should not reload the counter so it will pass 00h and reset the MCU.

The Watchdog activation (hardware or software) is user selectable by mask option. If the hardware option is selected the Watchdog is automatically initialised after reset so that this function does not need to be activated by the user program.

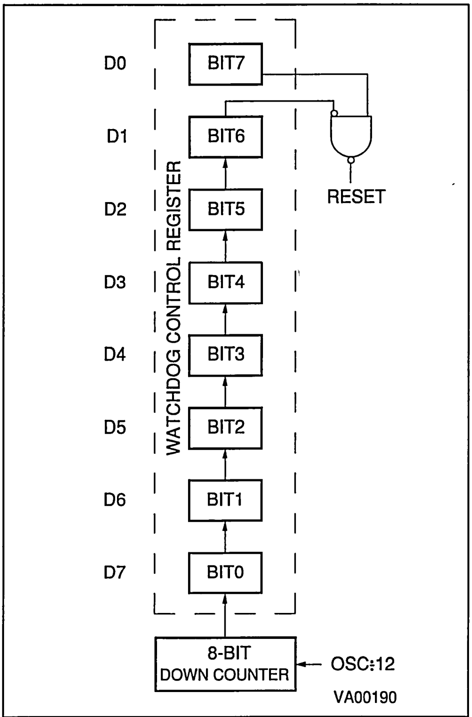
The Watchdog uses one data space register (DWDR location D8h). The Watchdog register is set to FEh on reset and counts down when activated. The Watchdog time can be adjusted through the value reloaded into the DWDR register. Only the 6 MSbits are significant. This gives the possibility to generate a reset in a time between 3072 to 196608 clock cycles in 64 possible steps (with a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded before bits 2-7 decrement from all zeros to all ones.

The actual watchdog behaviour is controlled by two mask options: the WATCHDOG ACTIVATION and the EXTERNAL STOP MODE CONTROL (see Table 13).

The WATCHDOG ACTIVATION can be software (it is launched by software) or hardware (it automatically starts counting down after reset). When the software activation is selected, the watchdog can be launched by setting to 1 bit 0 of the Digital Watchdog Register after bit C of this register has been set to 1. Once activated, the watchdog cannot be stopped by software: a full external reset is mandatory.

When the EXTERNAL STOP MODE CONTROL is disabled, the STOP instruction is inhibited as soon as the watchdog is active. A WAIT instruction is processed instead and the watchdog continues to countdown. When the EXTERNAL STOP MODE CONTROL is enabled, the NMI pin allows, in addition to the interrupt generation, to control the execution of the STOP instruction. It is inhibited when NMI is low (a WAIT instruction is processed instead). When NMI is high, a STOP instruction freezes the watchdog counter before entering the STOP mode. When the micro exits from the STOP mode (for example, when an NMI interrupt is generated), the watchdog resumes activity.

Figure 11. Watchdog Working Principle



Note:

When the software activation is selected and the watchdog is not activated, the 7 MSbits of the counter can be used to perform timer functions. Care must be taken as the Watchdog bits are in reverse order.

Bit 1 of the Watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero.

DIGITAL WATCHDOG (Continued)

Table 2. Watchdog Activation and External STOP Mode Control

Activation	External Stop Mode Control	NMI	STOP Mode Status
Hardware	Disabled	X	No STOP mode
	Enabled	0	No STOP mode
		1	STOP mode available
Software	Disabled	X	STOP mode available if watchdog not active
	Enabled	0	STOP mode available if watchdog not active
		1	STOP mode available

8-BIT A/D CONVERTER

The A/D converter of ST623x devices is an 8-bit analog to digital converter with up to 24 analog inputs (ST6235) as alternate functions of I/O lines. It offers 8-bit resolution with total accuracy ±2LSB and a typical conversion time of 70ms (clock frequency of 8MHz).

The A/D peripheral converts the input voltage by a process of successive approximations using a clock frequency derived from the oscillator with a division factor of twelve. With an oscillator clock frequency less than 1.2MHz, the A/D converter accuracy is decreased.

The selection of the pin signal that has to be converted is done by configuring the related I/O line as analog input through the I/O ports option and data registers (refer to I/O ports description for additional information). Only one I/O line must be configured as analog input at a time. The user must avoid the situation in which more than one I/O pin is selected to be analog input to avoid malfunction of the ST62xx.

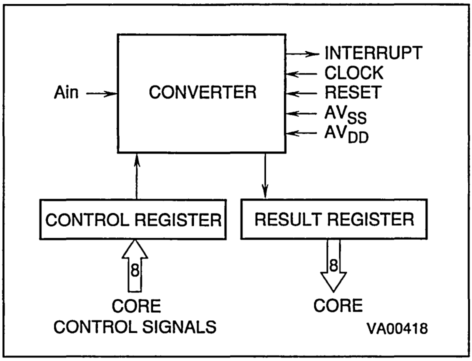
The ADC uses two registers in the data space: the ADC data conversion register which stores the conversion result and the ADC control register used to program the ADC functions.

A conversion is started by writing a “1” to the Start bit (STA) in the ADC control register. This automatically clears (resets to “0”) the End Of Conversion Bit (EOC). When a conversion has been finished this EOC bit is automatically set to “1” in order to flag that conversion is complete and that the data in the ADC data conversion register is valid. Each conversion has to be separately initiated by writing to the STA bit.

The STA bit is continually being scanned so that if the user sets it to “1” while a previous conversion is in progress then a new conversion is started before the previous one has been completed.The start bit (STA) is a write only bit, any attempt to read it will show a logical “0”.

The A/D converter has a maskable interrupt associated to the end of conversion. This interrupt is associated to the interrupt vector #4 and occurs when the EOC bit is set, i.e. when a conversion is completed. The interrupt is masked using the EAI (interrupt mask) bit in the control register.

Figure 12. A/D Converter Block Diagram



The power consumption of the device can be reduced by turning off the ADC peripheral. That is achieved when the PDS bit in the ADC control register is cleared to “0”. If PDS=“1”, the A/D is supplied and enabled for conversion. This bit must be set at least one instruction before the beginning of the conversion to allow the stabilisation of the A/D converter.*This action is needed also before entering the WAIT instruction as the A/D comparator is not automatically disabled by the WAIT mode.*

During reset any conversion in progress is stopped, the control register is reset to 40h and the A/D interrupt is masked (EAI=0).

Notes:

The reference voltage inputs of the A/D converter cell are connected to separate pins AV_{DD} and AV_{SS} (ST6232, ST6235). This offers the following features:

- definition of conversion range independently of the controler supply voltage ($V_{SS} \leq AV_{SS} < AV_{DD} \leq V_{DD}$)
- reduced conversion range for higher accuracy

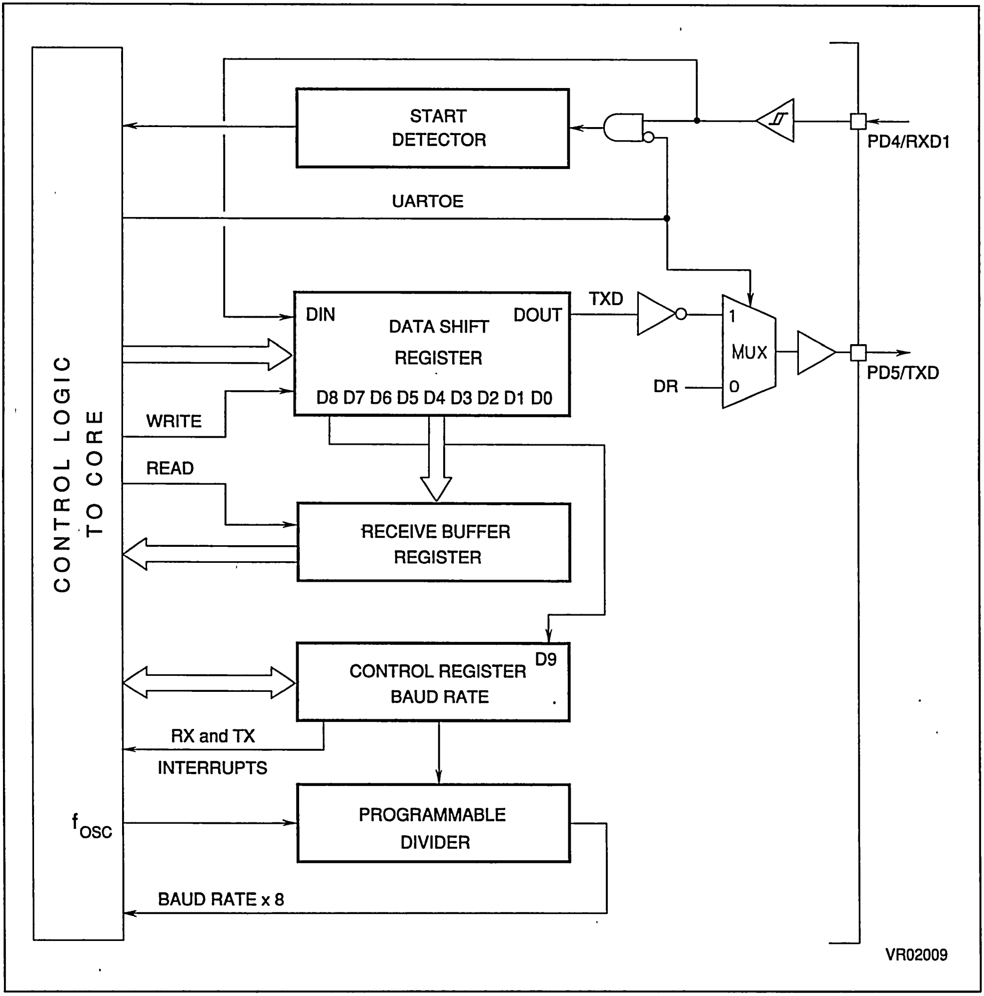
reduced noise due to decoupling independent from the MCU supply.

U.A.R.T.

The UART (Universal Asynchronous Receiver/Transmitter) provides the basic hardware for asynchronous serial communication which, combined with an appropriate software routine, gives a serial interface providing communication with common baud rates (up to 38,400 Baud with an 8MHz external oscillator) and flexible character formats.

Operating in Half-Duplex mode only, the UART uses 11-bit characters comprising 1 start bit, 9 data bits and 1 Stop bit. Parity is supported by software only for transmit and for checking the received parity bit (bit 9). Transmitted data is sent directly, while received data is buffered allowing further data characters to be received while the data is being read out of the receive buffer register. Data transmit has priority over data being received.

Figure 13. UART Block Diagram



SERIAL PERIPHERAL INTERFACE (SPI)

The ST623x SPI is an optimized serial synchronous interface that supports a wide range of industry standard SPI specifications. The ST623x SPI is controlled by small and simple user software to perform serial data exchange. The serial shift clock can be implemented either by software (using the bit-set and bit-reset instructions), with the on-chip Timer 1 by externally connecting the SPI clock pin to the timer pin or by directly applying an external clock to the SPI.

The peripheral is composed by an 8-bit Data/shift Register (address DDh) and a 4-bit binary counter. The SCL, Sin and Sout SPI data and clock signals are connected to the PD1, PD2 and PD3 I/O lines. With the 3 I/O pins, the SPI can operate in the following operating modes: Software SPI, S-BUS, I^{2}C-bus and as a standard serial I/O (clock, data, enable). An interrupt request can be generated after eight clock pulses. Figure 14 shows the SPI block diagram.

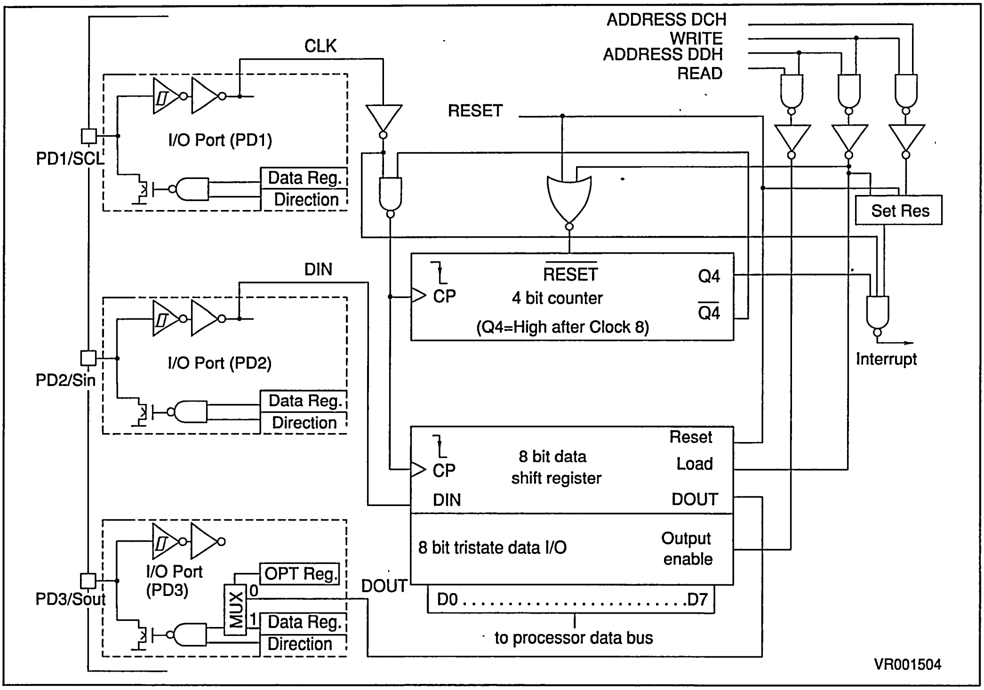
The PD1/SCL line clocks, on the falling edge, the shift register and the counter. To allow SPI operation the PD1/SCL must be programmed as input, an external clock supplied to this pin will drive the SPI peripheral (slave mode).

If PD1/SCL is programmed as output, a clock signal can be generated by software, setting and resetting the port line by software (master mode).

The SCL clock signal is the shift clock for the SPI data/shift register. The PD2/Sin pin is the serial shift input and PD3/Sout is the serial shift output. These two lines can be tied together to implement two wires protocols (I^{2}C-bus, etc). When data is serialized, the MSB is the first bit. PD2/Sin has to be programmed as input. For serial output operation PD3/Sout has to be programmed as open-drain output.

After 8 clock pulses (D7..D0) the output $\overline{Q4}$ of the 4-bit binary counter becomes low, disabling the clock from the counter and the data/shift register. Q4 enables the clock to generate an interrupt on the 8th clock falling edge as long as no reset of the counter (processor write into the 8-bit data/shift register) takes place. After a processor reset the interrupt is disabled. The interrupt is active when writing data in the shift register (DDh) and desactivated when writing any data in the register SPI Interrupt Disable 0DCh.

Figure 14. SPI Block Diagram



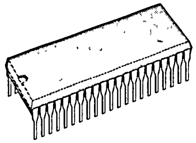
SGS-THOMSON
MICROELECTRONICS

ST62E3x, T3x

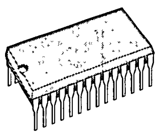
8-BIT OTP/EPROM HCMOS MCUs WITH A/D CONVERTER,EEPROM, UART & 16-BIT AUTO-RELOAD

FUNCTIONAL DESCRIPTION

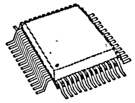
- 4.5 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM
- User EPROM: 8K bytes
- Data EPROM: User selectable size (in program EPROM)
- Data RAM: 192 bytes
- EEPROM: 128 bytes
- CDIP28 package (ST62E30)
- CDIP42 package (ST62E32)
- PDIL28, PSO28 package (ST62T30)
- SDIP42 package (ST62T32)
- PQFP52, CQFP52W package (ST62E35, T35)
- Up to 36 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- Up to 12 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler (TIMER 1)
- 16 bit Auto-reload Timer (ARTIM16)
- Digital Watchdog
- 8 bit A/D Converter with up to 24 multiplexed analog inputs
- 8 bit Asynchronous Peripheral Interface (UART)
- 8 bit Synchronous Peripheral Interface (SPI)
- On-chip clock oscillator driven by Quartz Crystal or Ceramic resonator
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The development tool of the ST623x microcontrollers consists of the ST623x-EMU emulation and development system connected via a standard RS232 serial line to an MS-DOS Personal Computer



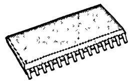
PSDIP42



PDIP28



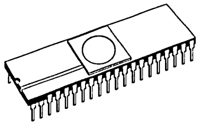
PQFP52



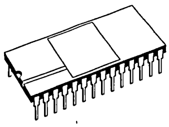
PSO28

(Ordering Information at the end of the datasheet)

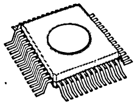
EPROM PACKAGES



CSDIP42W



CDIP28W



CQFP52W

The ST62E3x are the EPROM versions, the ST62T3x are the OTP versions. Both are compatible with the ROM versions.

July 1994

This is a functional description from SGS-THOMSON. Details are subject to change without notice.

GENERAL DESCRIPTION

The ST62E3x, T3x microcontrollers are members of the 8-bit HCMOS ST62XX family, a series of devices oriented to low-medium complexity applications. They are the EPROM and OTP versions of the ST623x devices. EPROM are suited for development. OTP are suited for prototyping, pre-series, low to mid volume series and inventory optimisation for customers having several applications using the same MCU.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST623X ROM DEVICES FOR FURTHER DETAILS.

EPROM/OTP DESCRIPTION

The ST62E3X are the EPROM version of the ST623x products. They can be programmed and erased when submitted to Ultra Violet light. The ST62T3x use the same die as the EPROM version, housed in a plastic package opaque to the UV light.

From the user point of view (with the following exceptions) the ST62E3x and ST62T3x have exactly the same software and hardware features as the ROM versions. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62T3x is described in the User Manual of the EPROM Programming board.

Discrepancies versus ROM

The operating voltage range is from 4.5V to 6.0 V instead of 3.0V to 6.0V for the ROM device.

ROM Option Emulation

The ROM mask options that can be selected by the user in the ROM devices can be selected on the EPROM/OTP devices by an EPROM CODE byte that can be programmed with the ST62E3x EPROM programming tools. This EPROM CODE byte is automatically read, and the selected options enabled when the chip reset is activated.

The Option byte is written during programming either by using the PC menu (PC driven mode) or automatically (stand-alone mode).

EPROM ERASING

The EPROM of the windowed package of the ST62E3x may be erased by the exposure to Ultra Violet light.

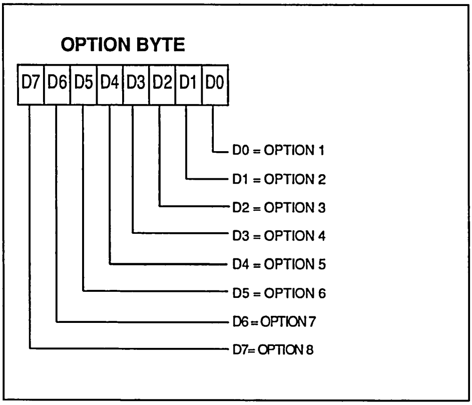
The erasure characteristics of the ST62E3x is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It is thus recommended that the window of the ST62E3x packages be covered by an opaque label to prevent unintentional erasure problems when testing the application.

The recommended erasure procedure of the ST62E3x is the exposure to short wave ultraviolet light which have a wave-length 2537Å. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E3x should be placed within 2.5cm (1inch) of the lamp tubes during erasure.

OPTION BYTE

The Option byte enables emulation of the mask options of the ROM devices. It can only be accessed during the programming mode. This access is made either automatically (copy from master device) or by selecting the "OPTION BYTE PROGRAMMING" mode of the programmer. The Option byte is located in a non-user accessible map. No address has to be specified.

Figure 1. EPROM Code Option Byte



AVAILABLE ROM OPTIONS FOR ST623x

AVAILABLE ROM OPTIONS FOR ST623x	Output Logic State
OPTION 1	Must be set at 1
OPTION 2	0: hardware watchdog 1: software watchdog
OPTION 3	0: Timer pull-up on 1: Timer pull-up off
OPTION 4	0: NMI pull-up on 1: NMI pull-up off
OPTION 5	0: for DIP28, QFP52, PSO28 1: for SDIL42
OPTION 6	0: NMI does not affect STOP instruction if WD is enabled 1: NMI affects STOP instruction if WD is enabled
OPTION 7	0: Port pull-up resistors on at reset 1: Port pull-up resistors off at reset
OPTION 8	0: EPROM read-out protection disabled 1: EPROM read-out protection enabled

ST62 OVERVIEWS

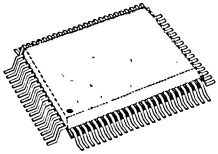
SGS-THOMSON
MICROELECTRONICS

ST6240

8-BIT HCMOS MCU WITH LCD DRIVER, EEPROM AND A/D CONVERTER

PRELIMINARY DATA

- 3 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
User ROM:	7948	bytes
Data RAM:	192	bytes
LCD RAM:	24	bytes
EEPROM:	128	bytes
- PQFP80 package
- 16 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs (12 pins)
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving, and have SPI alternate functions
- Two 8-bit counters with 7-bit programmable prescalers (Timers 1 and 2)
- Software or hardware activated digital watchdog
- 8-bit A/D converter with up to 12 analog inputs
- 8-bit synchronous Serial Peripheral Interface (SPI)
- LCD driver with 45 segment outputs, 4 backplane outputs and selectable duty cycle for up to 180 LCD segments direct driving
- 32kHz oscillator for stand-by LCD operation
- Power Supply Supervisor (PSS)
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E40 is the EPROM version, ST62T40 is the OTP version
- Development tool: ST6240-EMU connected via RS232 to an MS-DOS Personal Computer

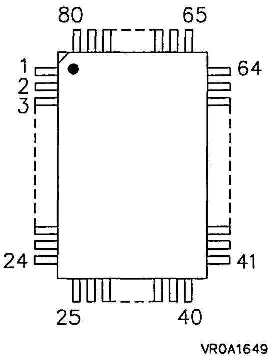


PQFP80

(Ordering Information at the end of the datasheet)

This is Preliminary Data from SGS-THOMSON, details are subject to change without notice.

Figure 1. 80 Pin Quad Flat Pack (QFP) Package Pinout



ST6240 Pin Description

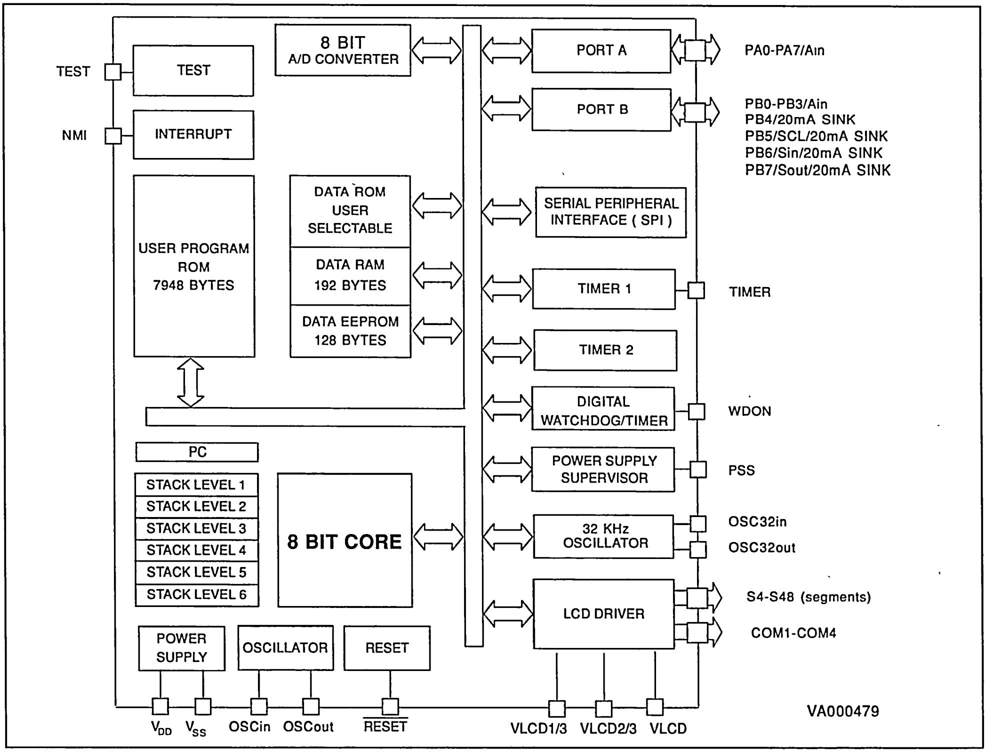
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	S43	25	$\overline{\text{RESET}}$	64	S26	65	S27
2	S44	26	OSCout	63	S25	66	S28
3	S45	27	OSCin	62	S24	67	S29
4	S46	28	WDON	61	S23	68	S30
5	S47	29	NMI	60	S22	69	S31
6	S48	30	TIMER	59	S21	70	S32
7	COM4	31	PB7/Sout [1]	58	S20	71	S33
8	COM3	32	PB6/Sin [1]	57	S19	72	S34
9	COM2	33	PB5/SCL [1]	56	S18	73	S35
10	COM1	34	PB4 [1]	55	S17	74	S36
11	VLCD1/3	35	PB3/Ain	54	S16	75	S37
12	VLCD2/3	36	PB2/Ain	53	S15	76	S38
13	VLCD	37	PB1/Ain	52	S14	77	S39
14	PA7/Ain	38	PB0/Ain	51	S13	78	S40
15	PA6/Ain	39	OSC32out	50	S12	79	S41
16	PA5/Ain	40	OSC32in	49	S11	80	S42
17	PA4/Ain			48	S10		
18	TEST			47	S9		
19	PA3/Ain			46	S8		
20	PA2/Ain			45	S7		
21	PA1/Ain			44	S6		
22	PA0/Ain			43	S5		
23	V$_{DD}$			42	S4		
24	V$_{SS}$			41	PSS		

Note 1: 20mA Sink

GENERAL DESCRIPTION

The ST6240 microcontroller is a member of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6240 are: a high performance LCD controller/driver with 45 segment outputs and 4 backplanes able to drive up to 180 segments, two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), the digital watchdog (DWD), an 8-bit A/D Converter with up to 12 analog inputs, a Power Supply Supervisor and an 8-bit synchronous Serial Peripheral Interface (SPI). In addition these devices offer 128 bytes of EEPROM for storage of non volatile data. Thanks to these peripherals the ST6240 is well suited for general purpose, automotive, security, appliance and industrial applications. The ST62E40 EPROM version is available for prototypes and low-volume production, an OTP version is also available (see separate datasheet).

Figure 2. ST6240 Block Diagram



Note:
Ain= Analog Input

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU.This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TIMER. This is the TIMER 1 I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the TIMER pin outputs the data bit when a time-out occurs.

WDON. This pin selects the watchdog enabling option (hardware or software). A low level selects the hardware activated option (the watchdog is always active), a high level selects the software activated option (the watchdog can be activated by software, deactivated only by reset, thus enabling STOP mode). An internal pull-up resistance selects the software watchdog option if the WDON pin is not connected.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output or as analog input for the A/D converter. Port A has a 5mA drive capability in output mode.

PB0-PB3,PB4-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. PB0-PB3 can be programmed as analog inputs for the A/D converter while PB4-PB7 can also sink 20mA for direct LED driving. PB5-PB7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals.

COM1-COM4. These four pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the 45 LCD lines allowing up to 180 segments to be driven.

S4-S48. These pins are the 45 LCD peripheral driver outputs of ST6240. Segments S1-S3 are not connected to any pin.

VLCD. Display voltage supply. It determines the high voltage level on COM1-COM4 and S4-S48 pins.

VLCD1/3, VLCD2/3. Display supply voltage inputs for determining the display voltage levels on COM1-COM4 and S4-S48 pins during multiplex operation.

PSS. This is the Power Supply Supervisor sensing pin. When the voltage applied to this pin is falling below a software programmed value the highest priority (NMI) interrupt can be generated. This pin has to be connected to the voltage to be supervised.

OSC32in and OSC32out. These pins are internally connected with the on-chip 32kHz oscillator circuit. A 32.768kHz quartz crystal can be connected between these two pins if it is necessary to provide the LCD stand-by clock and real time interrupt. OSC32in is the input pin, OSC32out is the output pin.

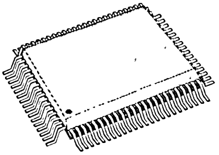
SGS-THOMSON
MICROELECTRONICS

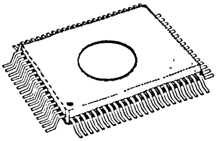
ST62E40
ST62T40

8-BIT OTP/EPROM HCMOS MCUs WITH LCD DRIVER,EEPROM AND A/D CONVERTER

PRELIMINARY DATA

- 3 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM
- User EPROM: 7948 bytes
  Data RAM: 192 bytes
  LCD RAM: 24 bytes
  EEPROM: 128 bytes
- PQFP80 and CQFP80-W packages
- 16 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs (12 pins)
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- Two 8-bit counters and 7-bit programmable prescalers (Timer 1 and 2)
- Software or hardware activated digital watchdog
- 8-bit A/D converter with up to 12 analog inputs
- 8-bit synchronous serial peripheral interface (SPI)
- LCD driver with 45 segment outputs, 4 backplane outputs and selectable duty cycle for up to 180 LCD segments direct driving
- 32kHz oscillator for stand-by LCD operation
- Power Supply Supervisor (PSS)
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E40 is the EPROM version, ST62T40 is the OTP version, fully compatible with ST6240 ROM version.

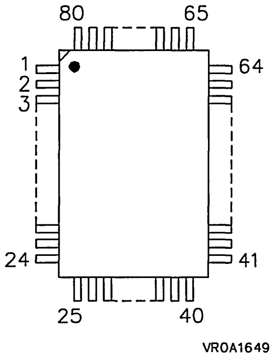

PQFP80


CQFP80-W

(Ordering Information at the end of the datasheet)

This is Preliminary data from SGS-THOMSON, details are subject to change without notice.

Figure 1. 80 Pin Quad Flat Pack (QFP) Package Pinout



ST62E40/T40 Pin Description

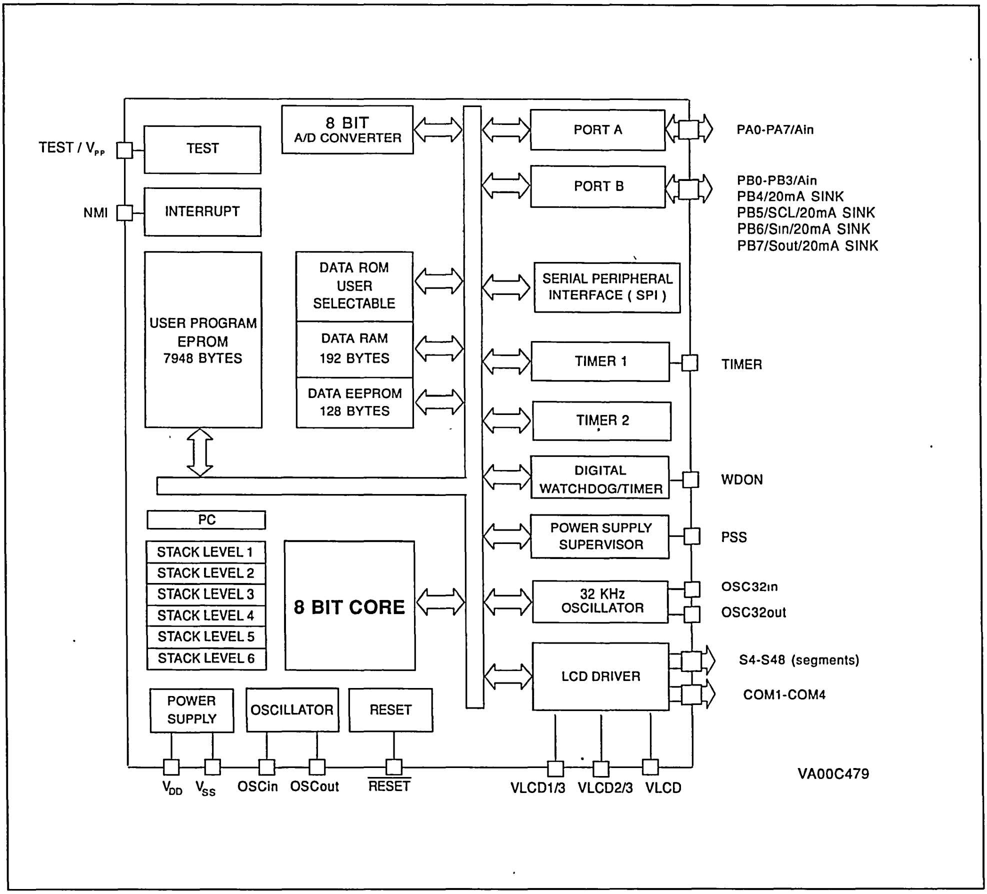
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	S43	25	$\overline{\text{RESET}}$	64	S26	65	S27
2	S44	26	OSCout	63	S25	66	S28
3	S45	27	OSCin	62	S24	67	S29
4	S46	28	WDON	61	S23	68	S30
5	S47	29	NMI	60	S22	69	S31
6	S48	30	TIMER	59	S21	70	S32
7	COM4	31	PB7/Sout (1)	58	S20	71	S33
8	COM3	32	PB6/Sin (1)	57	S19	72	S34
9	COM2	33	PB5/SCL (1)	56	S18	73	S35
10	COM1	34	PB4 (1)	55	S17	74	S36
11	VLCD1/3	35	PB3/Ain	54	S16	75	S37
12	VLCD2/3	36	PB2/Ain	53	S15	76	S38
13	VLCD	37	PB1/Ain	52	S14	77	S39
14	PA7/Ain	38	PB0/Ain	51	S13	78	S40
15	PA6/Ain	39	OSC32out	50	S12	79	S41
16	PA5/Ain	40	OSC32in	49	S11	80	S42
17	PA4/Ain			48	S10		
18	TEST/V_{PP}			47	S9		
19	PA3/Ain			46	S8		
20	PA2/Ain			45	S7		
21	PA1/Ain			44	S6		
22	PA0/Ain			43	S5		
23	V_{DD}			42	S4		
24	V_{SS}			41	PSS		

Note 1: 20mA Sink

GENERAL DESCRIPTION

The ST62E40,T40 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. They are the EPROM/OTP versions of the ST6240 ROM device and are suitable for product prototyping and low volume production. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6240 family are: a high performance LCD controller/driver with 45 segment outputs and 4 backplanes able to drive up to 180 segments, two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), the digital watchdog timer (DWD), an 8-bit A/D Converter with up to 12 analog inputs, a Power Supply Supervisor and an 8-bit synchronous Serial Peripheral Interface (SPI). In addition these devices offer 128 bytes of EEPROM for storage of non volatile data. Thanks to these peripherals the ST6240 family is well suited for general purpose, automotive, security, appliance and industrial applications.

Figure 2. ST62E40 Block Diagram



Note: Ain = Analog Input

PIN DESCRIPTION

V$_{DD}$ and V$_{SS}$. Power is supplied to the MCU using these two pins. V$_{DD}$ is power and V$_{SS}$ is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST/V$_{PP}$. The TEST must be held at V$_{SS}$ for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU.This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TIMER. This is the TIMER 1 I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the TIMER pin outputs the data bit when a time-out occurs.

WDON. This pin selects the watchdog enabling option (hardware or software). A low level selects the hardware activated option (the watchdog is always active), a high level selects the software activated option (the watchdog can be activated by software, deactivated only by reset, thus enabling STOP mode). An internal pull-up resistance selects the software watchdog option if the WDON pin is not connected.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output or as analog input for the A/D converter. Port A has a 5mA drive capability in output mode.

PB0-PB3,PB4-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. PB0-PB3 can be programmed as analog inputs for the A/D converter while PB4-PB7 can also sink 20mA for direct LED driving. PB5-PB7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals.

COM1-COM4. These four pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the 45 LCD lines allowing up to 180 segments to be driven.

S4-S48. These pins are the 45 LCD peripheral driver outputs of ST6240. Segments S1-S3 are not connected to any pin.

VLCD. Display voltage supply. It determines the high voltage level on COM1-COM4 and S4-S48 pins.

VLCD1/3, VLCD2/3. Display supply voltage inputs for determining the display voltage levels on COM1-COM4 and S4-S48 pins during multiplex operation.

PSS. This is the Power Supply Supervisor sensing pin. When the voltage applied to this pin is falling below a software programmed value the highest priority (NMI) interrupt can be generated. This pin has to be connected to the voltage to be supervised.

OSC32in and OSC32out. These pins are internally connected with the on-chip 32kHz oscillator circuit. A 32.768kHz quartz crystal can be connected between these two pins if it is necessary to provide the LCD stand-by clock and real time interrupt. OSC32in is the input pin, OSC32out is the output pin.

ST62E40,T40 EPROM/OTP DESCRIPTION

The ST62E40 is the EPROM version of the ST6240 ROM product. It is intended for use during the development of an application, and for pre-production and small volume production. The ST62T40 OTP has the same characteristics. Both include EPROM memory instead of the ROM memory of the ST6240, and so the program and constants of the program can be easily modified by the user with the ST62E40 EPROM programming board from SGS-THOMSON.

From a user point of view (with the following exception) the ST62E40,T40 products have exactly the same software and hardware features of the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E40,T40 is described in the User Manual of the EPROM Programming board.

On the ST62E40, all the 8192 bytes of PROGRAM memory are available for the user, as all the EPROM memory can be erased by exposure to UV light. On the ST62T40 (OTP) device) a reserved area for test purposes exists, as for the ST6240 ROM device. In order to avoid any discrepancy between program functionality when using the EPROM, OTP and ROM it is recommended not to use these reserved areas, even when using the ST62E40.

Other than this exception, the ST62E40,T40 parts are fully compatible with the ROM ST6240 equivalent, this datasheet thus provides only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6240 ROM-BASED DEVICE FOR FURTHER DETAILS.

EPROM ERASING

The EPROM of the windowed package of the ST62E40 may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E40 EPROM is such that erasure begins when the memory is exposed to light with wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E40 package be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.
The recommended erasure procedure of the ST62E40 EPROM is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E40 should be placed within 2.5 cm (1 inch) of the lamp tubes during erasure.

SGS-THOMSON
MICROELECTRONICS

ST6242

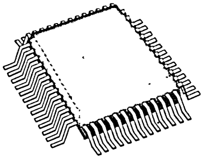
8-BIT HCMOS MCU WITH LCD DRIVER, AND A/D CONVERTER

PRELIMINARY DATA

- 3 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
-

User ROM:	7948 bytes
Data RAM:	128 bytes
LCD RAM:	24 bytes

- PQFP64 package
- 10 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs (6 pins)
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- 8-bit counter with 7-bit programmable prescaler
- Software activated digital watchdog
- 8-bit A/D converter with up to 6 analog inputs
- 8-bit synchronous Serial Peripheral Interface (SPI)
- LCD driver with 40 segment outputs, 4 back-plane outputs and selectable duty cycle for up to 160 LCD segments direct driving
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E42 is the EPROM version, ST62T42 is the OTP version
- Development tool: ST6242-EMU connected via RS232 to an MS-DOS Personal Computer

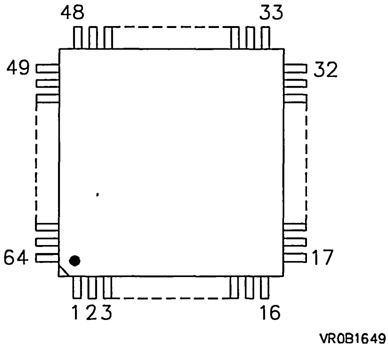


PQFP64

(Ordering Information at the end of the datasheet)

This is Preliminary Data from SGS-THOMSON, details are subject to change without notice.

Figure 3. 64 Pin Quad Flat Pack (QFP) Package Pinout



ST6242 Pin Description

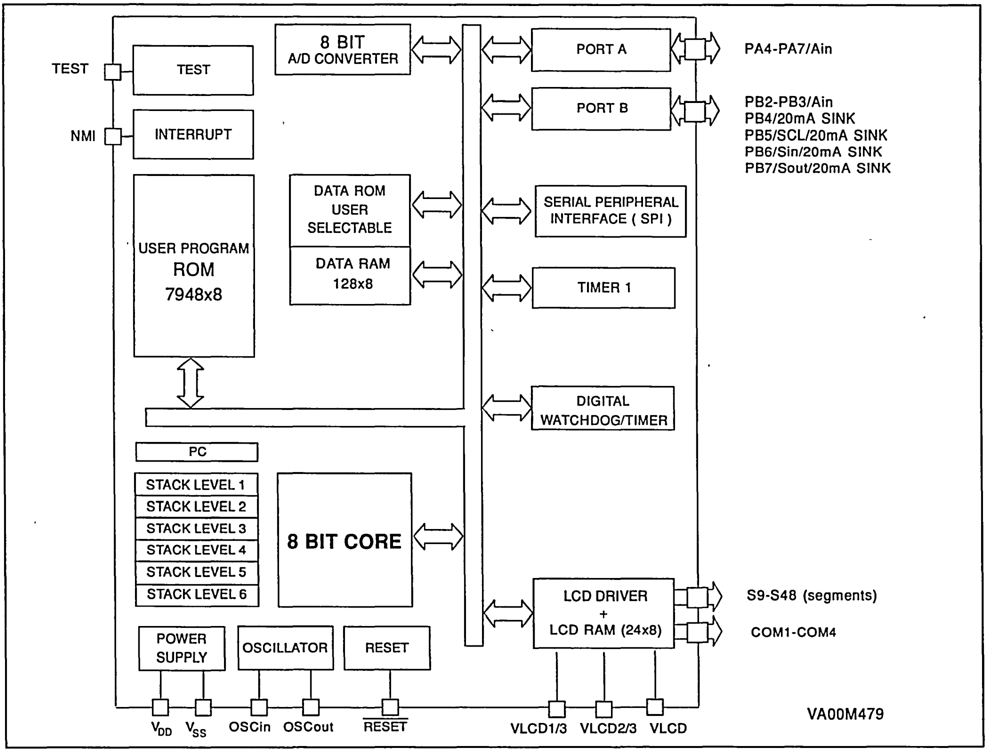
Pin number	Pin name
1	S45
2	S46
3	S47
4	S48
5	COM4
6	COM3
7	COM2
8	COM1
9	VLCD1/3
10	VLCD2/3
11	VLCD
12	PA7/Ain
13	PA6/Ain
14	PA5/Ain
15	PA4/Ain
16	TEST/V_{PP}
17	V_{DD}
18	V_{SS}
19	$\overline{\text{RESET}}$
29	OSCout
21	OSCin
22	NMI
23	PB7/Sout (1)
24	PB6/Sin (1)
25	PB5/SCL (1)
26	PB4 (1)
27	PB3/Ain
28	PB2/Ain
29	S9
30	S10
31	S11
32	S12
33	S13
34	S14
35	S15
36	S16
37	S17
38	S18
39	S19
40	S20
41	S21
42	S22
43	S23
44	S24
45	S25
46	S26
47	S27
48	S28
49	S29
50	S30
51	S31
52	S32
53	S33
54	S34
55	S35
56	S36
57	S37
58	S38
59	S39
60	S40
61	S41
62	S42
63	S43
64	S44

Note 1: 20mA SINK

GENERAL DESCRIPTION

The ST6242 microcontroller is a member of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6242 are: a high performance LCD controller/driver with 40 segment outputs and 4 backplanes able to drive up to 160 segments. A Timer peripheral including an 8-bit counter with a 7-bit software programmable prescaler (Timer), the digital watchdog timer (DWD), an 8-bit A/D Converter with up to 6 analog inputs, a Power Supply Supervisor and an 8-bit synchronous Serial Peripheral Interface (SPI). Thanks to these peripherals the ST6242 is well suited for general purpose, automotive, security, appliance and industrial applications. The ST62E42 EPROM version is available for prototypes and low-volume production, an OTP version is also available (see separate datasheet).

Figure 4. ST6242 Block Diagram



Note: Ain = Analog Input

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU.This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

PA4-PA7. These 4 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output or as analog input for the A/D converter. Port A has a 5mA drive capability in output mode.

PB0-PB3,PB4-PB7. These 6 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. PB2-PB3 can be programmed as analog inputs for the A/D converter while PB4-PB7 can also sink 20mA for direct LED driving. PB5-PB7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals.

COM1-COM4. These 4 pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the 40 LCD lines allowing up to 160 segments to be driven.

S9-S48. These pins are the 40 LCD peripheral driver outputs of ST6242. Segments S1-S8 are not connected to any pin.

VLCD. Display voltage supply. It determines the high voltage level on COM1-COM4 and S9-S48 pins.

VLCD1/3, VLCD2/3. Resistor network nodes for determining the intermediate display voltage levels on COM1-COM4 and S9-S48 pins during multiplex operation.

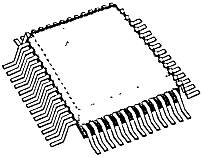
SGS-THOMSON
MICROELECTRONICS

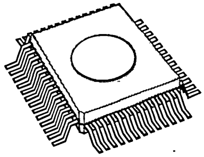
ST62E42
ST62T42

8-BIT OTP/EPROM HCMOS MCUs WITH LCD DRIVER, AND A/D CONVERTER

PRELIMINARY DATA

- 3 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM
- User EPROM: 7948 bytes
  Data RAM: 128 bytes
  LCD RAM: 24 bytes
- PQFP64 and CQFP64-W packages
- 10 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs (6 pins)
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- 8-bit counters and 7-bit programmable prescalers
- Software activated digital watchdog
- 8-bit A/D converter with up to 6 analog inputs
- 8-bit synchronous serial peripheral interface (SPI)
- LCD driver with 40 segment outputs, 4 backplane outputs and selectable duty cycle for up to 160 LCD segments direct driving
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E42 is the EPROM version, ST62T42 is the OTP version, fully compatible with ST6242 ROM version.

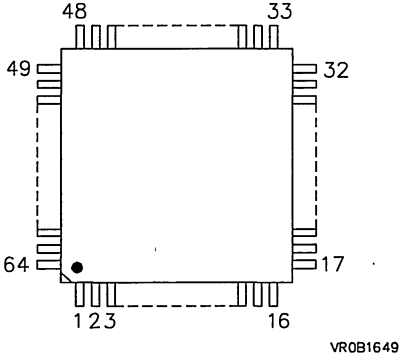

PQFP64


CQFP64-W

(Ordering Information at the end of the datasheet)

This is Preliminary data from SGS-THOMSON, details are subject to change without notice.

Figure 1.Pin Quad Flat Pack (QFP) Package Pinout



ST62E42/T42 Pin Description

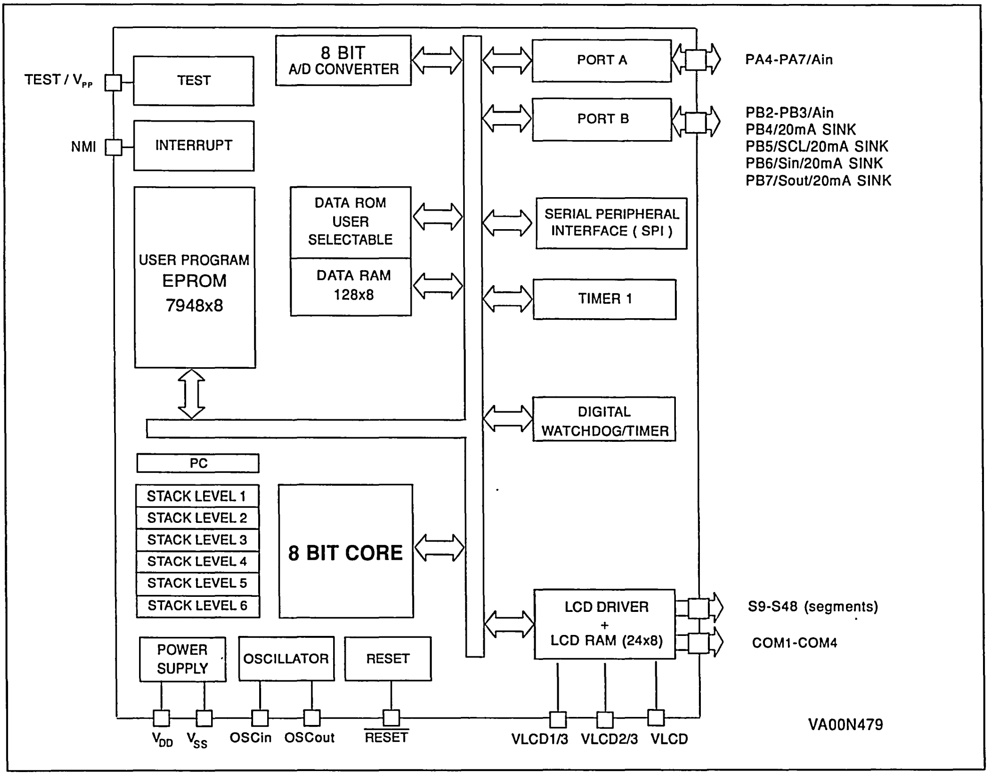
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	S45	17	V_{DD}	33	S13	49	S29
2	S46	18	V_{SS}	34	S14	50	S30
3	S47	19	$\overline{\text{RESET}}$	35	S15	51	S31
4	S48	29	OSCout	36	S16	52	S32
5	COM4	21	OSCin	37	S17	53	S33
6	COM3	22	NMI	38	S18	54	S34
7	COM2	23	PB7/Sout (1)	39	S19	55	S35
8	COM1	24	PB6/Sin (1)	40	S20	56	S36
9	VLCD1/3	25	PB5/SCL (1)	41	S21	57	S37
10	VLCD2/3	26	PB4 (1)	42	S22	58	S38
11	VLCD	27	PB3/Ain	43	S23	59	S39
12	PA7/Ain	28	PB2/Ain	44	S24	60	S40
13	PA6/Ain	29	S9	45	S25	61	S41
14	PA5/Ain	30	S10	46	S26	62	S42
15	PA4/Ain	31	S11	47	S27	63	S43
16	TEST/V_{PP}	32	S12	48	S28	64	S44

Note 1: 20mA SINK

GENERAL DESCRIPTION

The ST62E42,T42 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. They are the EPROM/OTP versions of the ST6242 ROM device and are suitable for product prototyping and low volume production. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6242 family are: a high performance LCD controller/driver with 40 segment outputs and 4 backplanes able to drive up to 160 segments, a Timer peripheral including an 8-bit counter with a 7-bit software programmable prescaler, a digital watchdog timer (DWD), an 8-bit A/D Converter with up to 6 analog inputs and an 8-bit synchronous Serial Peripheral Interface (SPI). Thanks to these peripherals the ST6242 family is well suited for general purpose, automotive, security, appliance and industrial applications.

Figure 2. ST62E42 Block Diagram



Note: Ain = Analog Input

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the ST62E42 using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST/V_{PP}. The TEST pin is used to place the MCU into special operating mode. TEST must be held at V_{SS} for normal operation (an internal pull-down resistor is present to select normal operating mode if TEST pin is not connected). If this pin is connected to a +12.5V level during the reset phase, the EPROM programming mode is entered.

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the ST62E42.This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

PA4-PA7. These 4 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output or as analog input for the A/D converter. Port A has a 5mA drive capability in output mode.

PB2-PB3,PB4-PB7. These 6 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. PB2-PB3 can be programmed as analog inputs for the A/D converter while PB4-PB7 can also sink 20mA for direct LED driving. PB5-PB7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals.

COM1-COM4. These four pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the 40 LCD lines allowing up to 160 segments to be driven.

S9-S48. These pins are the 40 LCD peripheral driver outputs of ST62E42. Segments S1-S8 are not connected to any pin.

VLCD. Display voltage supply. It determines the high voltage level on COM1-COM4 and S9-S48 pins.

VLCD1/3, VLCD2/3. Display supply voltage inputs for determining the display voltage levels on COM1-COM4 and S9-S48 pins during multiplex operation.

ST62E42,T42 EPROM/OTP DESCRIPTION

The ST62E42 is the EPROM version of the ST6242 ROM product. It is intended for use during the development of an application, and for pre-production and small volume production. The ST62T42 OTP has the same characteristics. Both include EPROM memory instead of the ROM memory of the ST6242, and so the program and constants of the program can be easily modified by the user with the ST62E42 EPROM programming board from SGS-THOMSON.

From a user point of view (with the following exception) the ST62E42,T42 products have exactly the same software and hardware features of the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/VPP pin. The programming of the ST62E42,T42 is described in the User Manual of the EPROM Programming board.

On the ST62E42, all the 8192 bytes of PROGRAM memory are available for the user, as all the EPROM memory can be erased by exposure to UV light. On the ST62T42 (OTP) device) a reserved area for test purposes exists, as for the ST6242 ROM device. In order to avoid any discrepancy between program functionality when using the EPROM, OTP and ROM it is recommended not to use these reserved areas, even when using the ST62E42.

Notes on programming:

In order to emulate exactly the ST6242 features with the ST62E42 and ST6242, some software precautions have to be taken:

1. Data RAM: The data entered in the Data RAM bank register (CBh) must be 08h.

2. I/O: To prevent floating input or uncontrolled I/O interrrupt on the EPROM/OTP devices, the port bits PA0-PA3, PB0, PB1 must be programmed as push-pull outputs.

3. Timer: The bit "TOUT" of the Timer status control register (D4h) must be set "1" (timer in output mode).

4. Data Memory Space: Write 40h at the address DFh of the Data Memory Space (desabled EE).

5. When programming for the EPROM/OTP parts, it is suggested that the conditional assembly technique is used for controlling the I/O ports in order to disable the appropriate code for the ROM device.

6. Do not access data space locations D5h, D6h, D7h, DAh, DBh.

Other than this exception, the ST62E42,T42 parts are fully compatible with the ROM ST6242 equivalent, this datasheet thus provides only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6242 ROM-BASED DEVICE FOR FURTHER DETAILS.

EPROM ERASING

The EPROM of the windowed package of the ST62E42 may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E42 EPROM is such that erasure begins when the memory is exposed to light with wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E42 package be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.
The recommended erasure procedure of the ST62E42 EPROM is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E42 should be placed within 2.5 cm (1 inch) of the lamp tubes during erasure.

SGS-THOMSON
MICROELECTRONICS

ST6245

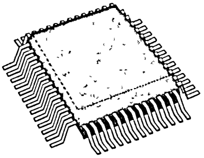
8-BIT HCMOS MCU WITH LCD DRIVER, EEPROM AND A/D CONVERTER

PRELIMINARY DATA

- 3 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
-

User ROM:	3884	bytes
Data RAM:	128	bytes
LCD RAM:	12	bytes
EEPROM:	64	bytes

- PQFP52 package
- 11 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs (7 pins)
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving, and have SPI alternate functions
- Two 8-bit counters with 7-bit programmable prescalers (Timers 1 and 2)
- Software activated digital watchdog
- 8-bit A/D converter with up to 7 analog inputs
- 8-bit synchronous Serial Peripheral Interface (SPI)
- LCD driver with 24 segment outputs, 4 backplane outputs and selectable duty cycle for up to 96 LCD segments direct driving
- 32kHz oscillator for stand-by LCD operation
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E45 is the EPROM version, ST62T45 is the OTP version
- Development tool: ST6245-EMU connected via RS232 to an MS-DOS Personal Computer

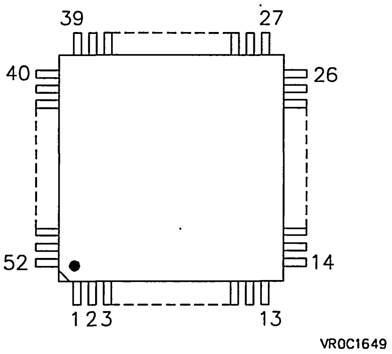


PQFP52

(Ordering Information at the end of the datasheet)

This is Preliminary Data from SGS-THOMSON, details are subject to change without notice.

Figure 4. 52 Pin Quad Flat Pack (QFP) Package Pinout



ST6245 Pin Description

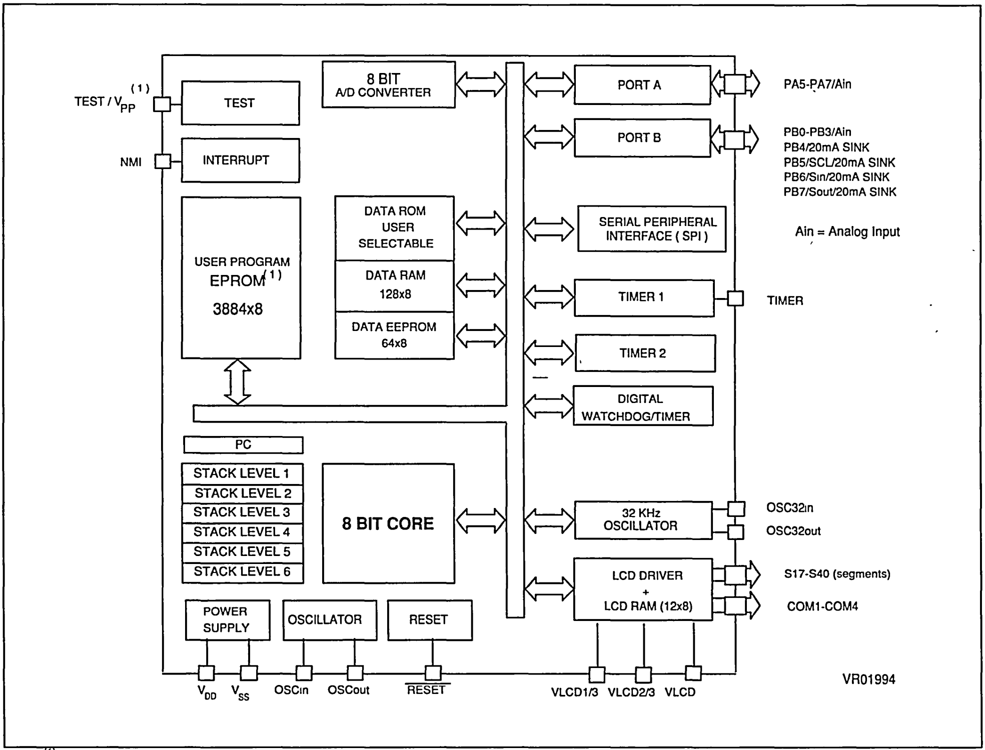
Pin number	Pin name
1	COM4
2	COM3
3	COM2
4	COM1
5	VLCD1/3
6	VLCD2/3
7	VLCD
8	PA7/Ain
9	PA6/Ain
10	PA5/Ain
11	TEST
12	V_{DD}
13	V_{SS}
14	$\overline{\text{RESET}}$
15	OSCout
16	OSCin
17	NMI
18	TIMER
19	PB7/Sout (1)
20	PB6/Sin (1)
21	PB5/SCL (1)
22	PB4 (1)
23	PB3/Ain
24	PB2/Ain
25	PB1/Ain
26	PB0/Ain
27	OSC32out
28	OSC32in
29	S17
30	S18
31	S19
32	S20
33	S21
34	S22
35	S23
36	S24
37	S25
38	S26
39	S27
40	S28
41	S29
42	S30
43	S31
44	S32
45	S33
46	S34
47	S35
48	S36
49	S37
50	S38
51	S39
52	S40

Note 1: 20mA SINK

GENERAL DESCRIPTION

The ST6245 microcontroller is a member of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6245 are: a high performance LCD controller/driver with 24 segment outputs and 4 backplanes able to drive up to 96 segments, two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), the digital watchdog (DWD), an 8-bit A/D Converter with up to 7 analog inputs and an 8-bit synchronous Serial Peripheral Interface (SPI). In addition these devices offer 64 bytes of EEPROM for storage of non volatile data. Thanks to these peripherals the ST6245 is well suited for general purpose, automotive, security, appliance and industrial applications. The ST62E45 EPROM version is available for prototypes and low-volume production, an OTP version is also available (see separate datasheet).

Figure 5. ST6245 Block Diagram



Note [1]**:** VPP only exists in EPROM version

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU.This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TIMER. This is the TIMER 1 I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the TIMER pin outputs the data bit when a time-out occurs.

PA5-PA7. These 3 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output or as analog input for the A/D converter. Port A has a 5mA drive capability in output mode.

PB0-PB3,PB4-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. PB0-PB3 can be programmed as analog inputs for the A/D converter while PB4-PB7 can also sink 20mA for direct LED driving. PB5-PB7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals.

COM1-COM4. These four pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the 24 LCD lines allowing up to 96 segments to be driven.

S17-S40. These pins are the 24 LCD peripheral driver outputs of ST6245. Segments S1-S16 and S41-S48 are not connected to any pin.

VLCD. Display voltage supply. It determines the high voltage level on COM1-COM4 and S1-S24 pins.

VLCD1/3, VLCD2/3. Display supply voltage inputs for determining the display voltage levels on COM1-COM4 and S1-S24 pins during multiplex operation.

OSC32in and OSC32out. These pins are internally connected with the on-chip 32kHz oscillator circuit. A 32.768kHz quartz crystal can be connected between these two pins if it is necessary to provide the LCD stand-by clock and real time interrupt. OSC32in is the input pin, OSC32out is the output pin.

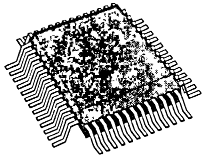
SGS-THOMSON
MICROELECTRONICS

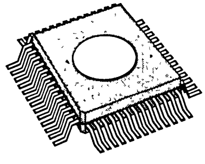
ST62E45
ST62T45

8-BIT OTP/EPROM HCMOS MCUs WITH LCD DRIVER,EEPROM AND A/D CONVERTER

PRELIMINARY DATA

- 3 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM
- User EPROM: 3884 bytes
  Data RAM: 128 bytes
  LCD RAM: 12 bytes
  EEPROM: 64 bytes
- PQFP52 and CQFP52-W packages
- 11 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs (7 pins)
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- Two 8-bit counters and 7-bit programmable prescalers (Timers 1 and 2)
- Software activated digital watchdog
- 8-bit A/D converter with up to 7 analog inputs
- 8-bit synchronous serial peripheral interface (SPI)
- LCD driver with 24 segment outputs, 4 backplane outputs and selectable duty cycle for up to 96 LCD segments direct driving
- 32kHz oscillator for stand-by LCD operation
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E45 is the EPROM version, ST62T45 is the OTP version, fully compatible with ST6245 ROM version.


PQFP52

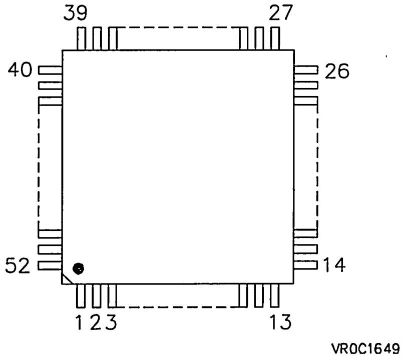

CQFP52-W

(Ordering Information at the end of the datasheet)

December 1993

This is Preliminary Data from SGS-THOMSON, details are subject to change without notice.

Figure 1. 52 Pin Quad Flat Pack (QFP) Package Pinout



ST62E45/T45 Pin Description

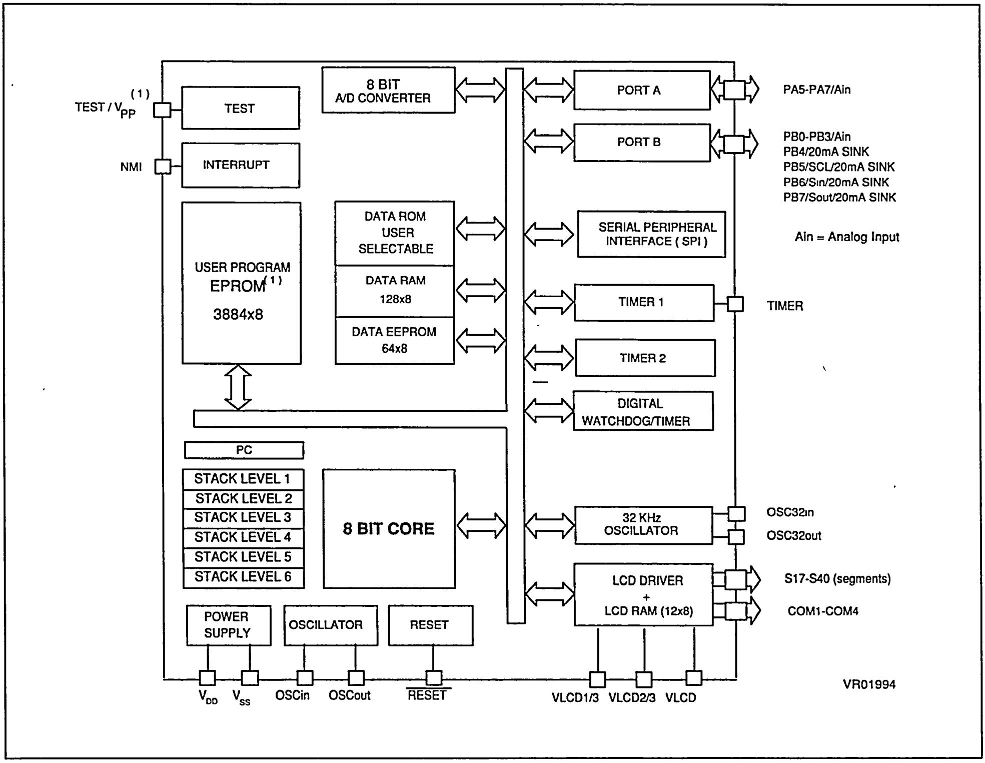
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	COM4	14	$\overline{\text{RESET}}$	27	OSC32out	40	S28
2	COM3	15	OSCout	28	OSC32in	41	S29
3	COM2	16	OSCin	29	S17	42	S30
4	COM1	17	NMI	30	S18	43	S31
5	VLCD1/3	18	TIMER	31	S19	44	S32
6	VLCD2/3	19	PB7/Sout (1)	32	S20	45	S33
7	VLCD	20	PB6/Sin (1)	33	S21	46	S34
8	PA7/Ain	21	PB5/SCL (1)	34	S22	47	S35
9	PA6/Ain	22	PB4 (1)	35	S23	48	S36
10	PA5/Ain	23	PB3/Ain	36	S24	49	S37
11	TEST	24	PB2/Ain	37	S25	50	S38
12	V_{DD}	25	PB1/Ain	38	S26	51	S39
13	V_{SS}	26	PB0/Ain	39	S27	52	S40

Note 1: 20mA SINK

GENERAL DESCRIPTION

The ST62E45,T45 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. They are the EPROM/OTP versions of the ST6245 ROM device and are suitable for product prototyping and low volume production. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6245 family are: a high performance LCD controller/driver with 24 segment outputs and 4 backplanes able to drive up to 96 segments, two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), the digital watchdog timer (DWD), an 8-bit A/D Converter with up to 7 analog inputs and an 8-bit synchronous Serial Peripheral Interface (SPI). In addition these devices offer 64 bytes of EEPROM for storage of non volatile data. Thanks to these peripherals the ST6245 family is well suited for general purpose, automotive, security, appliance and industrial applications.

Figure 2. ST62E45 Block Diagram



Note(1) : VPP only exists in EPROM version

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST/V_{PP}. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU.This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TIMER. This is the TIMER 1 I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the TIMER pin outputs the data bit when a time-out occurs.

PA5-PA7. These 3 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output or as analog input for the A/D converter. Port A has a 5mA drive capability in output mode.

PB0-PB3,PB4-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, interrupt generating input with pull-up resistor, open-drain or push-pull output. PB0-PB3 can be programmed as analog inputs for the A/D converter while PB4-PB7 can also sink 20mA for direct LED driving. PB5-PB7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals.

COM1-COM4. These four pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the 24 LCD lines allowing up to 96 segments to be driven.

S17-S40. These pins are the 24 LCD peripheral driver outputs of ST62E45. Segments S1-S16 and S41-S48 are not connected to any pin.

VLCD. Display voltage supply. It determines the high voltage level on COM1-COM4 and S1-S24 pins.

VLCD1/3, VLCD2/3. Display supply voltage inputs for determining the display voltage levels on COM1-COM4 and S1-S24 pins during multiplex operation.

OSC32in and OSC32out. These pins are internally connected with the on-chip 32kHz oscillator circuit. A 32.768kHz quartz crystal can be connected between these two pins if it is necessary to provide the LCD stand-by clock and real time interrupt. OSC32in is the input pin, OSC32out is the output pin.

ST62E45,T45 EPROM/OTP DESCRIPTION

The ST62E45 is the EPROM version of the ST6245 ROM product. It is intended for use during the development of an application, and for pre-production and small volume production. The ST62T45 OTP has the same characteristics. Both include EPROM memory instead of the ROM memory of the ST6245, and so the program and constants of the program can be easily modified by the user with the ST62E45 EPROM programming board from SGS-THOMSON.

From a user point of view (with the following exception) the ST62E45,T45 products have exactly the same software and hardware features of the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/V_{PP} pin. The programming of the ST62E45,T45 is described in the User Manual of the EPROM Programming board.

On the ST62E45, all the 3884 bytes of PROGRAM memory are available for the user, as all the EPROM memory can be erased by exposure to UV light. On the ST62T45 (OTP) device) a reserved area for test purposes exists, as for the ST6245 ROM device. In order to avoid any discrepancy between program functionality when using the EPROM, OTP and ROM it is recommended not to use these reserved areas, even when using the ST62E45.

Notes on programming:

In order to emulate exactly the ST6245 features with the ST62E45 and ST6245, some software precautions have to be taken:

1. I/O: To prevent floating input or uncontrolled I/O interrrupt on the EPROM/OTP devices, the port bits PA0-PA4 must be programmed as push-pull outputs.

2. When programming for the EPROM/OTP parts, it is suggested that the conditional assembly technique is used for controlling the I/O ports in order to disable the appropriate code for the ROM device.

3. Do not access data space locations CAh, DAh .

Other than this exception, the ST62E45,T45 parts are fully compatible with the ROM ST6245 equivalent, this datasheet thus provides only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6240 ROM-BASED DEVICE FOR FURTHER DETAILS.

EPROM ERASING

The EPROM of the windowed package of the ST62E45 may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E45 EPROM is such that erasure begins when the memory is exposed to light with wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E45 package be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.
The recommended erasure procedure of the ST62E45 EPROM is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E45 should be placed within 2.5 cm (1 inch) of the lamp tubes during erasure.

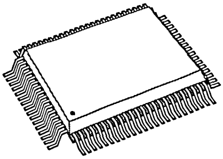
SGS-THOMSON
MICROELECTRONICS

ST6280

8-BIT HCMOS MCU WITH DOT MATRIX LCD DRIVER EEPROM AND A/D CONVERTER

PRELIMINARY DATA

- 4.5 to 6V supply operating range
- 8.4 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 7948 bytes
  Data RAM: 192 bytes
  LCD RAM: 128 bytes
  EEPROM: 128 bytes
- PQFP100 package
- 12 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs
- 10 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- One 8-bit counter with 7-bit programmable prescaler (Timer 1)
- One 8-bit auto-reload timer with 7-bit programmable prescaler (ARTimer)
- Software activated digital watchdog
- 8-bit A/D converter with up to 12 analog inputs
- 8-bit synchronous serial peripheral interface (SPI)
- LCD driver controller with 48 segments outputs, 8 backplane and 8 software selectable segment/backplane outputs able to drive up to 48x16 (768) or 56x8 (448) segments.
- 32kHz oscillator for stand-by LCD operation
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E80 is the EPROM version, ST62T80 is the OTP version
- Development tool: ST628x-EMU connected via a standard RS232 to an MS-DOS Personal Computer

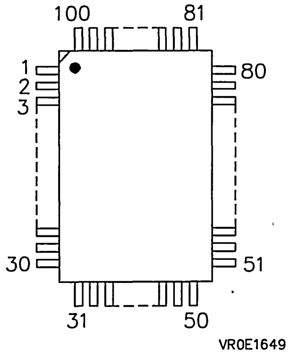


PQFP100

(Ordering information at the end of the datasheet)

This is preliminary data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. 100 Pin Quad Flat Pack (QFP) Package Pinout



ST6280 Pin Description

Pin number	Pin name
1	S39
2	S40
3	S41
4	S42
5	S43
6	S44
7	S45
8	S46
9	S47
10	S48
11	S49
12	S50
13	S51
14	S52
15	S53
16	S54
17	S55
18	S56
19	PB7/ARTIMout /Ain
20	PB6/ARTIMin /Ain
21	PB5/Ain
22	PB4/Ain
23	PB3/Ain
24	PB2/Ain
25	PB1/Ain
26	PB0/Ain
27	TEST
28	OSCout
29	OSCin
30	$\overline{\text{RESET}}$

Pin number	Pin name
31	PC7/Ain
32	PC6/Ain
33	PC5/Ain
34	PC4/Ain
35	PC3 (1)
36	PC2 (1)
37	PC1 (1)
38	PC0 (1)
39	NMI
40	V_{DD}
41	V_{SS}
42	VLCD
43	VLCD4/5
44	VLCD3/5
45	VLCD2/5
46	VLCD1/5
47	PA7/Sout (1)
48	PA6/Sin (1)
49	PA5/SCL (1)
50	PA4/TIM1 (1)

Pin number	Pin name
51	PA3 (1)
52	PA2 (1)
53	OSC32out
54	OSC32in
55	COM1
56	COM2
57	COM3
58	COM4
59	COM5
60	COM6
61	COM7
62	COM8
63	COM9/S1
64	COM10/S2
65	COM11/S3
66	COM12/S4
67	COM13/S5
68	COM14/S6
69	COM15/S7
70	COM16/S8
71	S9
72	S10
73	S11
74	S12
75	S13
76	S14
77	S15
78	S16
79	S17
80	S18

Pin number	Pin name
81	S19
82	S20
83	S21
84	S22
85	S23
86	S24
87	S25
88	S26
89	S27
90	S28
91	S29
92	S30
93	S31
94	S32
95	S33
96	S34
97	S35
98	S36
99	S37
100	S38

Note 1: 20mA SINK

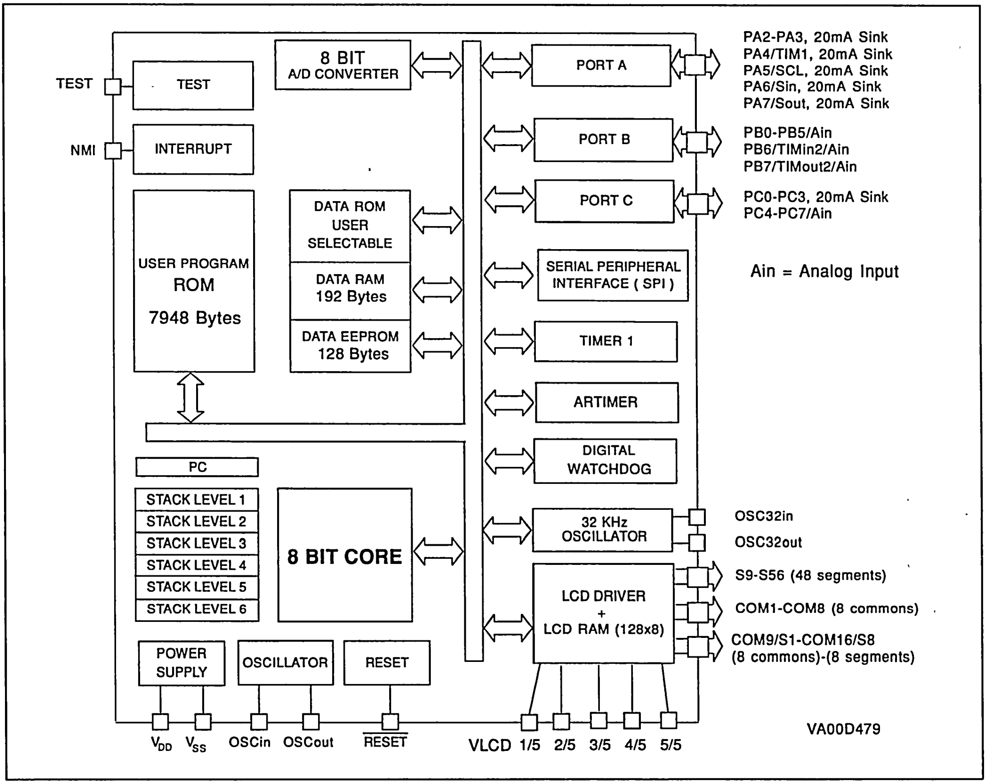
GENERAL DESCRIPTION

The ST6280 microcontrollers is a member of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach:

a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6280 are an advanced LCD driver/controller with 48 segments, 8 backplanes and 8 software selectable segment/backplane outputs able to drive up to 48x16 (768) or 56x8 (448) segments, one 8 bit Autoreload timer with 7 bit programmable prescaler (ARTimer), one 8 bit standard timer/counter with a 7-bit software programmable prescaler (Timer 1), the digital watchdog (DWD), an 8-bit A/D Converter with up to 12 analog inputs, a 32kHz Oscillator, and an 8-bit synchronous serial peripheral interface (SPI). In addition this device offers 128 bytes of EEPROM for storage of non-volatile data.

Thanks to these peripherals the ST6280 is well suited for general purpose, automotive, security, appliance and industrial applications. The ST62E80 EPROM version is available for prototyping and low-volume production, an OTP version is also available (see separate datasheet).

Figure 2. ST6280 Block Diagram



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST. TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU. This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

PA4/TIM1. This pin can be used as Timer 1 I/O pin. In input mode it is connected to the timer prescaler input and acts as the external timer clock or as the control gate for the internal timer clock. In the output mode the timer pin outputs the timer data bit when a time out occurs.
To use this pin as Timer output the I/O pin has to be programmed as open-drain output. To use this pin as Timer input the I/O pin has to be programmed as input.

PB6/TIMIN2, PB7/TIMOUT2. These pins are the Input and Output pins of the Autoreload Timer. The timer input pin ARTIMin is connected to port line PB6. To use the line as timer input function, PB6 has to be programmed as input with or without pull-up. The timer output pin is connected to the port line PB7. A dedicated bit in the ARTIMER mode control register sets the line as timer output function ARTIMout.

PA2-PA7. These 6 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED or triac driving. PA5-PA7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals. PA4 can also be used as the TIMER 1 I/O pin.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, open-drain or push-pull output or as an analog input for the A/D converter. PB6 is also connected to the ARTIMER input function while PB7 can act as the ARTIMER output.

PC0-PC3, PC4-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. PC0-PC3 can also sink 20mA for direct LED or triac driving while PC4-PC7 can be programmed as analog inputs for the A/D converter.

COM1-COM8. These eight pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the LCD segment lines.

S9-S56. These pins are the 48 LCD peripheral driver outputs of the ST6280. Segments S1-S8 are multiplexed with COM9-COM16 and their function is software selectable.

COM9/S1-COM16/S8. These pins are the 8 multiplexed common/segment lines. Under software selected control, they can act as LCD common outputs allowing a 48×16 dot matrix operation, or they can act as segment outputs allowing 56×8 dot matrix operation.

VLCD1/5-VLCD5/5. Resistor network nodes for determining the intermediate LCD voltage levels on COM1-COM8/COM16 and S1/S8-S56 pins during multiplex operation.

OSC32in and OSC32out. These pins are internally connected with the on-chip 32kHz oscillator circuit. A 32.768kHz quartz crystal can be connected between these two pins if it is necessary to provide the LCD stand-by clock and real time interrupt. OSC32in is the input pin, OSC32out is the output pin.

SGS-THOMSON
MICROELECTRONICS

ST62E80
ST62T80

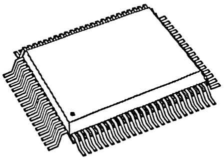
8-BIT EPROM HCMOS MCU WITH DOT MATRIX LCD DRIVER EEPROM AND A/D CONVERTER

PRELIMINARY DATA

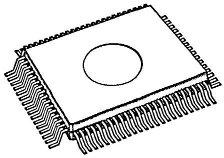
- 4.5 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperture Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM

User EPROM:	8192 bytes
Data RAM:	192 bytes
LCD RAM:	128 bytes
EEPROM:	128 bytes

- PQFP100 and CQFP100-W packages
- 12 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs
- 10 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- One 8-bit counter with 7-bit programmable prescalers (Timer 1)
- One 8-bit auto-reload timer with 7-bit programmable prescaler (Timer 2)
- Software activated digital watchdog
- 8-bit A/D converter with up to 12 analog inputs
- 8-bit synchronous serial peripheral interface (SPI)
- LCD driver with 48 segment outputs, 8 backplane outputs and 8 software selectable segment/backplane outputs able to drive up to 48x16 (768) or 56x8 (448) LCD segments.
- 32kHz oscillator for stand-by LCD operation
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E80 is the EPROM version, ST62T80 is the OTP version, fully compatible with ST6280 ROM version.



PQFP100

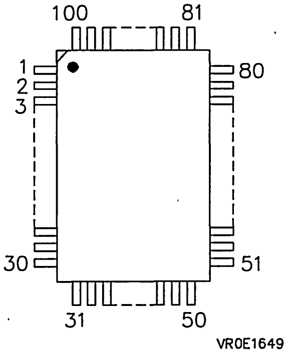


CQFP100-W

(Ordering Information at the end of the datasheet)

This is preliminary data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. 100 Pin Quad Flat Pack (QFP) Package Pinout



ST62E80/T80 Pin Description

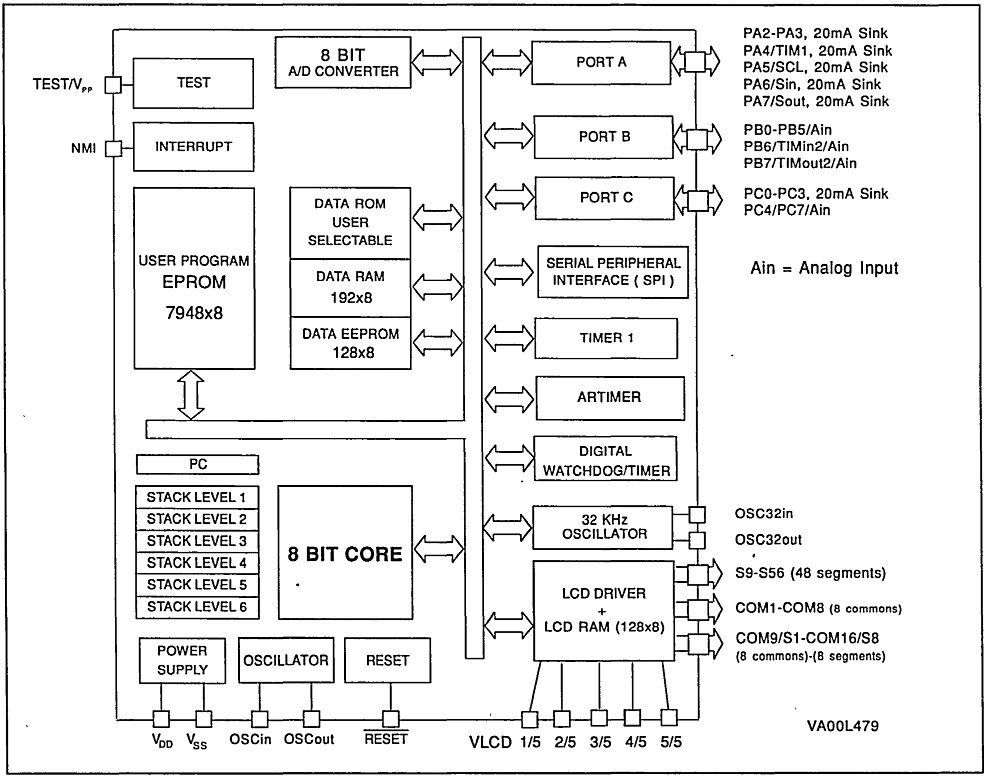
Pin number	Pin name
1	S39
2	S40
3	S41
4	S42
5	S43
6	S44
7	S45
8	S46
9	S47
10	S48
11	S49
12	S50
13	S51
14	S52
15	S53
16	S54
17	S55
18	S56
19	PB7/TIMout2 /Ain
20	PB6/TIMin2 /Ain
21	PB5/Ain
22	PB4/Ain
23	PB3/Ain
24	PB2/Ain
25	PB1/Ain
26	PB0/Ain
27	TEST/V_{PP}
28	OSCout
29	OSCin
30	$\overline{\text{RESET}}$
31	PC7/Ain
32	PC6/Ain
33	PC5/Ain
34	PC4/Ain
35	PC3 [1]
36	PC2 [1]
37	PC1 [1]
38	PC0 [1]
39	NMI
40	V_{DD}
41	V_{SS}
42	VLCD
43	VLCD4/5
44	VLCD3/5
45	VLCD2/5
46	VLCD1/5
47	PA7/Sout [1]
48	PA6/Sin [1]
49	PA5/SCL [1]
50	PA4/TIM1 [1]
51	PA3 [1]
52	PA2 [1]
53	OSC32out
54	OSC32in
55	COM1
56	COM2
57	COM3
58	COM4
59	COM5
60	COM6
61	COM7
62	COM8
63	COM9/S1
64	COM10/S2
65	COM11/S3
66	COM12/S4
67	COM13/S5
68	COM14/S6
69	COM15/S7
70	COM16/S8
71	S9
72	S10
73	S11
74	S12
75	S13
76	S14
77	S15
78	S16
79	S17
80	S18
81	S19
82	S20
83	S21
84	S22
85	S23
86	S24
87	S25
88	S26
89	S27
90	S28
91	S29
92	S30
93	S31
94	S32
95	S33
96	S34
97	S35
98	S36
99	S37
100	S38

Note 1: 20mA SINK

GENERAL DESCRIPTION

The ST62E80, ST62T80 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. They are the EPROM/OTP versions of the ST6280 ROM device and are suitable for prototyping and low-volume production. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6280 family are: an advanced LCD driver/controller with 48 segments, 8 backplanes and 8 software selectable segment/backplane outputs able to drive up to 48x16 (768) or 56x8 (448) segments, one 8 bit reload timer with 7 bit programmable prescaler (Timer 2), one 8 bit standard timer/counter with a 7-bit software programmable prescaler (Timer 1), the digital watchdog timer (DWD), an 8-bit A/D Converter with up to 12 analog inputs, a 32kHz Oscillator, and an 8-bit synchronous serial peripheral interface (SPI). In addition this device offers 128 bytes of EEPROM for storage of non-volatile data. Thanks to these peripherals the ST6280 family is well suited for general purpose, automotive, security, appliance and industrial applications.

Figure 2. ST62E80/T80 Block Diagram



PIN DESCRIPTION

V$_{DD}$ and V$_{SS}$. Power is supplied to the MCU using these two pins. V$_{DD}$ is power and V$_{SS}$ is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST. TEST must be held at V$_{SS}$ for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU. This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

PA4/TIM1. This pin can be used as Timer 1 I/O pin. In input mode it is connected to the timer prescaler input and acts as the external timer clock or as the control gate for the internal timer clock. In the output mode the timer pin outputs the timer data bit when a time out occurs.
To use this pin as Timer output the I/O pin has to be programmed as open-drain output. To use this pin as Timer input the I/O pin has to be programmed as input.

PB6/TIMIN2, PB7/TIMOUT2. These pins are the Input and Output pins of the Autoreload Timer. The timer input pin ARTIMin is connected to port line PB6. To use the line as timer input function, PB6 has to be programmed as input with or without pull-up. The timer output pin is connected to the port line PB7. A dedicated bit in the ARTIMER mode control register sets the line as timer output function ARTIMout.

PA2-PA7. These 6 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED or triac driving. PA5-PA7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals. PA4 can also be used as the TIMER 1 I/O pin.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, open-drain or push-pull output or as an analog input for the A/D converter. PB6 is also connected to the ARTIMER input function while PB7 can act as the ARTIMER output.

PC0-PC3, PC4-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. PC0-PC3 can also sink 20mA for direct LED or triac driving while PC4-PC7 can be programmed as analog inputs for the A/D converter.

COM1-COM8. These eight pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the LCD segment lines.

S9-S56. These pins are the 48 LCD peripheral driver outputs of the ST6280. Segments S1-S8 are multiplexed with COM9-COM16 and their function is software selectable.

COM9/S1-COM16/S8. These pins are the 8 multiplexed common/segment lines. Under software selected control, they can act as LCD common outputs allowing a 48×16 dot matrix operation, or they can act as segment outputs allowing 56×8 dot matrix operation.

VLCD1/5-VLCD5/5. Resistor network nodes for determining the intermediate LCD voltage levels on COM1-COM8/COM16 and S1/S8-S56 pins during multiplex operation.

OSC32in and OSC32out. These pins are internally connected with the on-chip 32kHz oscillator circuit. A 32.768kHz quartz crystal can be connected between these two pins if it is necessary to provide the LCD stand-by clock and real time interrupt. OSC32in is the input pin, OSC32out is the output pin.

ST62E80/ST62T80 EPROM/OTP DESCRIPTION.

The ST62E80 is the EPROM version of the ST6280 ROM product. It is intended for use during the development of an application, and for pre-production and small volume production. The ST62T80 OTP has the same characteristics. They both include EPROM memory instead of the ROM memory of the ST6280, and so the program and constants of the program can be easily modified by the user with the ST62E80 EPROM programming board of from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E80, ST62T80 products have exactly the same software and hardware features of the ROM version.

On the ST62E80, all the 8192 bytes of PROGRAM memory are available for the user, as all the EPROM memory can be erased by exposure to UV light. On the ST62T80 (OTP) device a reserved area for test purposes exists, as for the ST6280 ROM device. In order to avoid any discrepancy between program functionality when using the EPROM, OTP and ROM it is recommended not to use these reserved areas, even when using the ST62E80.

Other than these exceptions, the ST62E80, ST62T80 parts are fully compatible with the ROM ST6280 equivalent; this datasheet thus provides only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6280 ROM-BASED DEVICE FOR FURTHER DETAILS.

EPROM ERASING

The EPROM of the windowed package of the ST62E80 may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E80 EPROM is such that erasure begins when the memory is exposed to light with wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E80 package be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.
The recommended erasure procedure of the ST62E80 EPROM is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E80 should be placed within 2.5 cm (1 inch) of the lamp tubes during erasure.

ST62T80 OTP Memory Map

ROM Page	Device Address	Description
Page 0	0000h-007Fh 0080h-07FFh	Reserved User ROM
Page 1 "STATIC"	0800h-0F9Fh 0FA0h-0FEFh 0FF0h-0FF7h 0FF8h-0FFBh 0FFCh-0FFDh 0FFEh-0FFFh	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
Page 2	0000h-000Fh 0010h-07FFh	Reserved User ROM
Page 3	0000h-000Fh 0010h-07FFh	Reserved User ROM

SGS-THOMSON
MICROELECTRONICS

ST6285

8-BIT HCMOS MCU WITH DOT MATRIX LCD DRIVER AND A/D CONVERTER

PRELIMINARY DATA

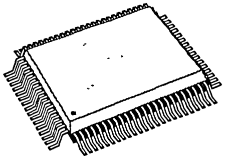
- 4.5 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperture Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM

User EPROM:	8192 bytes
Reserved ROM:	244 bytes
Data RAM:	192 bytes
LCD RAM:	96 bytes

- PQFP80 package
- 8 fully software programmable I/O as:

– Input with/without pull-up resistor
– Input with interrupt generation
– Open-Drain or Push-pull outputs
– Analog Inputs

- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- One 8-bit counter with 7-bit programmable prescalers (Timer 1)
- Software activated digital watchdog
- 8-bit A/D converter with up to 12 analog inputs
- 8-bit synchronous serial peripheral interface (SPI)
- LCD driver with 40 segment outputs, 8 backplane outputs and 8 software selectable segment/backplane outputs able to drive up to 40x16 (640) or 48x8 (384) LCD segments.
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E85 is the EPROM version, ST62T85 is the OTP version, fully compatible with ST6285 ROM version.

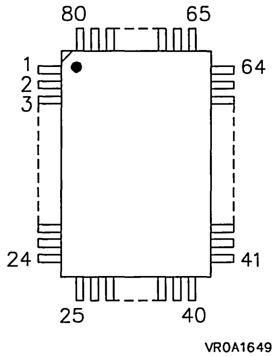


PQFP80

(Ordering Information at the end of the datasheet)

This is preliminary data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. 80 Pin Quad Flat Pack (QFP) Package Pinout



ST6285 Pin Description

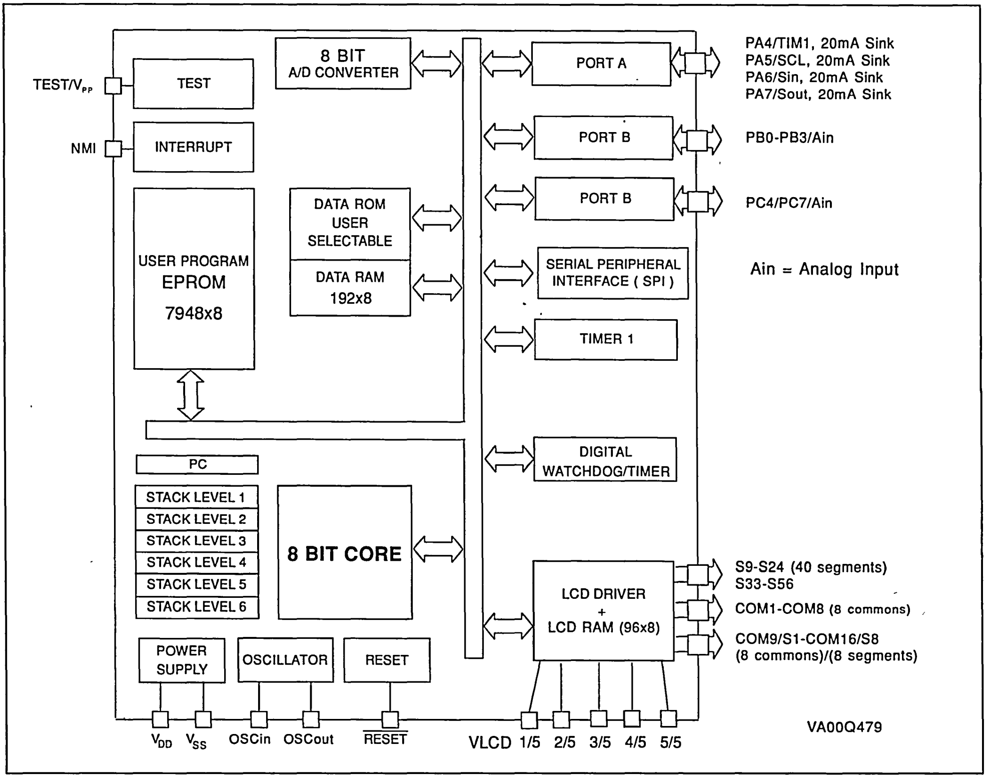
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	S41	25	PC7	41	COM1	65	S17
2	S42	26	PC6	42	COM2	66	S18
3	S43	27	PC5	43	COM3	67	S19
4	S44	28	PC4	44	COM4	68	S20
5	S45	29	NMI	45	COM5	69	S21
6	S46	30	V_{DD}	46	COM6	70	S22
7	S47	31	V_{SS}	47	COM7	71	S23
8	S48	32	VLCD	48	COM8	72	S24
9	S49	33	VLCD4/5	49	COM9/S1	73	S33
10	S50	34	VLCD3/5	50	COM10/S2	74	S34
11	S51	35	VLCD2/5	51	COM11/S3	75	S35
12	S52	36	VLCD1/5	52	COM12/S4	76	S36
13	S53	37	PA7/Sout (1)	53	COM13/S5	77	S37
14	S54	38	PA6/Sin (1)	54	COM14/S6	78	S38
15	S55	39	PA5/SCL (1)	55	COM15/S7	79	S39
16	S56	40	PA4/TIM1 (1)	56	COM16/S8	80	S40
17	PB3			57	S9		
18	PB2			58	S10		
19	PB1			59	S11		
20	PB0			60	S12		
21	TEST/V_{PP}			61	S13		
22	OSCout			62	S14		
23	OSCin			63	S15		
24	$\overline{\text{RESET}}$			64	S16		

Note 1: 20mA SINK

GENERAL DESCRIPTION

The ST6285 microcontroller is a member of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6285 family are: an advanced LCD driver/controller with 40 segments, 8 backplanes and 8 software selectable segment/backplane outputs able to drive up to 40×16 (640) or 48×8 (384) segments, one 8 bit standard timer/counter with a 7-bit software programmable prescaler (Timer 1), the digital watchdog timer (DWD), an 8-bit A/D Converter with up to 12 analog inputs and an 8-bit synchronous serial peripheral interface (SPI). Thanks to these peripherals the ST6285 family is well suited for general purpose, automotive, security, appliance and industrial applications. The ST62E85 EPROM version is available for prototyping and low-volume production, an OTP version is also available.

Figure 2. ST6285 Block Diagram



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST. TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU. This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

PA4/TIM1. This pin can be used as Timer 1 I/O pin. In input mode it is connected to the timer prescaler input and acts as the external timer clock or as the control gate for the internal timer clock. In the output mode the timer pin outputs the timer data bit when a time out occurs.
To use this pin as Timer output the I/O pin has to be programmed as open-drain output. To use this pin as Timer input the I/O pin has to be programmed as input.

PA4-PA7. These 4 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED or triac driving. PA5-PA7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals. PA4 can also be used as the TIMER 1 I/O pin.

PB0-PB3. These 4 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, open-drain or push-pull output or as an analog input for the A/D converter.

PC4-PC7. These 4 lines are organized as one I/O port (C). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. PC4-PC7 can be programmed as analog inputs for the A/D converter. Port C has schmitt trigger inputs and a 5mA drive capability in output mode.

COM1-COM8. These eight pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the LCD segment lines.

S9/S24-S33/S56. These pins are the 40 LCD peripheral driver outputs of the ST62E85, ST62T85. Segments S1-S8 are multiplexed with COM9-COM16 and their function is software selectable.

COM9/S1-COM16/S8. These pins are the 8 multiplexed common/segment lines. Under software selected control, they can act as LCD common outputs allowing a 40×16 dot matrix operation, or they can act as segment outputs allowing 48×8 dot matrix operation.

VLCD1/5-VLCD5/5. Resistor network nodes for determining the intermediate display voltage levels on COM1-COM8/COM16 and S1/S8-S56 pins during multiplex operation.

SGS-THOMSON
MICROELECTRONICS

ST62E85
ST62T85

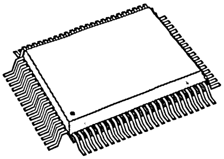
8-BIT EPROM HCMOS MCU WITH DOT MATRIX LCD DRIVER AND A/D CONVERTER

PRELIMINARY DATA

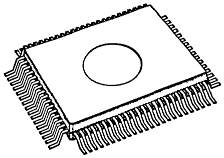
- 4.5 to 6V supply operating range
- 8.4MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperture Range
- Run, Wait & Stop Modes
- 5 different interrupt vectors
- Look-up table capability in EPROM

User EPROM:	8192 bytes
Data RAM:	192 bytes
LCD RAM:	96 bytes

- PQFP80 and CQFP80-W packages
- 8 fully software programmable I/O as:
  - Input with/without pull-up resistor
  - Input with interrupt generation
  - Open-Drain or Push-pull outputs
  - Analog Inputs
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving and have SPI alternate functions
- One 8-bit counter with 7-bit programmable prescalers (Timer 1)
- Software activated digital watchdog
- 8-bit A/D converter with up to 12 analog inputs
- 8-bit synchronous serial peripheral interface (SPI)
- LCD driver with 40 segment outputs, 8 backplane outputs and 8 software selectable segment/backplane outputs able to drive up to 40x16 (640) or 48x8 (384) LCD segments.
- One external not maskable interrupt
- 9 powerful addressing modes
- The accumulator, the X, Y, V & W registers, the port and peripherals data & control registers are addressed in the data space as RAM locations.
- The ST62E85 is the EPROM version, ST62T85 is the OTP version, fully compatible with ST6285 ROM version.



PQFP80

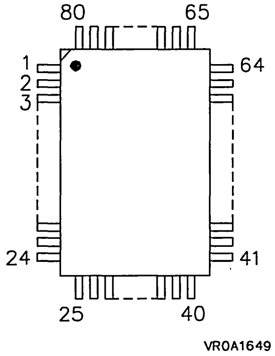


CQFP80-W

(Ordering Information at the end of the datasheet)

This is preliminary data from SGS-THOMSON. Details are subject to change without notice.

Figure 1. 80 Pin Quad Flat Pack (QFP) Package Pinout



ST62E85 Pin Description

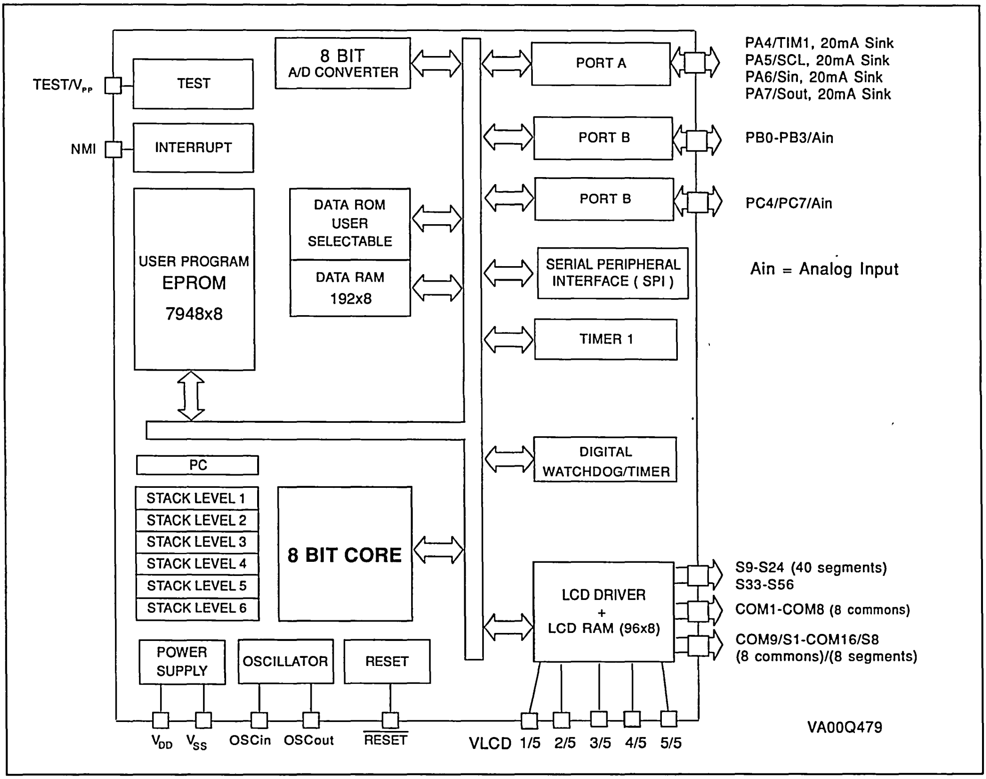
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	S41	25	PC7	41	COM1	65	S17
2	S42	26	PC6	42	COM2	66	S18
3	S43	27	PC5	43	COM3	67	S19
4	S44	28	PC4	44	COM4	68	S20
5	S45	29	NMI	45	COM5	69	S21
6	S46	30	V_{DD}	46	COM6	70	S22
7	S47	31	V_{SS}	47	COM7	71	S23
8	S48	32	VLCD	48	COM8	72	S24
9	S49	33	VLCD4/5	49	COM9/S1	73	S33
10	S50	34	VLCD3/5	50	COM10/S2	74	S34
11	S51	35	VLCD2/5	51	COM11/S3	75	S35
12	S52	36	VLCD1/5	52	COM12/S4	76	S36
13	S53	37	PA7/Sout [1]	53	COM13/S5	77	S37
14	S54	38	PA6/Sin [1]	54	COM14/S6	78	S38
15	S55	39	PA5/SCL [1]	55	COM15/S7	79	S39
16	S56	40	PA4/TIM1 [1]	56	COM16/S8	80	S40
17	PB3			57	S9		
18	PB2			58	S10		
19	PB1			59	S11		
20	PB0			60	S12		
21	TEST/V_{PP}			61	S13		
22	OSCout			62	S14		
23	OSCin			63	S15		
24	$\overline{\text{RESET}}$			64	S16		

Note 1: 20mA SINK

GENERAL DESCRIPTION

The ST62E85, ST62T85 microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. They are the EPROM/OTP versions of the ST6285 ROM device and are suitable for prototyping and low-volume production. All ST62xx members are based on a building block approach: a common core is associated with a combination of on-chip peripherals (macrocells). The macrocells of the ST6285 family are: an advanced LCD driver/controller with 40 segments, 8 backplanes and 8 software selectable segment/backplane outputs able to drive up to 40x16 (640) or 48x8 (384) segments, one 8 bit standard timer/counter with a 7-bit software programmable prescaler (Timer 1), the digital watchdog timer (DWD), an 8-bit A/D Converter with up to 12 analog inputs and an 8-bit synchronous serial peripheral interface (SPI). Thanks to these peripherals the ST6285 family is well suited for general purpose, automotive, security, appliance and industrial applications.

Figure 2. ST62E85/T85 Block Diagram



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. OSCin is the input pin, OSCout is the output pin. An external clock signal can be applied to OSCin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller at the beginning of its program. The $\overline{\text{RESET}}$ pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

TEST/. TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous applying an external top priority interrupt to the MCU. This pin is falling edge sensitive. The NMI pin is provided with an on-chip pull-up resistor and schmitt trigger input characteristics.

PA4/TIM1. This pin can be used as Timer 1 I/O pin. In input mode it is connected to the timer prescaler input and acts as the external timer clock or as the control gate for the internal timer clock. In the output mode the timer pin outputs the timer data bit when a time out occurs.
To use this pin as Timer output the I/O pin has to be programmed as open-drain output. To use this pin as Timer input the I/O pin has to be programmed as input.

PA4-PA7. These 4 lines are organized as one I/O port (A). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. In output mode these lines can also sink 20mA for direct LED or triac driving. PA5-PA7 can also be used as respectively Clock, Data in and Data out pins for the on-chip SPI to carry the synchronous serial I/O signals. PA4 can also be used as the TIMER 1 I/O pin.

PB0-PB3. These 4 lines are organized as one I/O port (B). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, open-drain or push-pull output or as an analog input for the A/D converter.

PC4-PC7. These 4 lines are organized as one I/O port (C). Each line may be configured under software control as an input with or without internal pull-up resistor, an interrupt generating input with pull-up resistor, or an open-drain or push-pull output. PC4-PC7 can be programmed as analog inputs for the A/D converter. Port C has schmitt trigger inputs and a 5mA drive capability in output mode.

COM1-COM8. These eight pins are the LCD peripheral common outputs. They are the outputs of the on-chip backplane voltage generator which is used for multiplexing the LCD segment lines.

S9/S24-S33/S56. These pins are the 40 LCD peripheral driver outputs of the ST62E85, ST62T85. Segments S1-S8 are multiplexed with COM9-COM16 and their function is software selectable.

COM9/S1-COM16/S8. These pins are the 8 multiplexed common/segment lines. Under software selected control, they can act as LCD common outputs allowing a 40x16 dot matrix operation, or they can act as segment outputs allowing 48x8 dot matrix operation.

VLCD1/5-VLCD5/5. Resistor network nodes for determining the intermediate display voltage levels on COM1-COM8/COM16 and S1/S8-S56 pins during multiplex operation.

ST62E85/ST62T85 EPROM/OTP DESCRIPTION.

The ST62E85 is the EPROM version of the ST6285 ROM product. It is intended for use during the development of an application, and for pre-production and small volume production. The ST62T85 OTP has the same characteristics. They both include EPROM memory instead of the ROM memory of the ST6285, and so the program and constants of the program can be easily modified by the user with the ST62E85 EPROM programming board of from SGS-THOMSON.

From a user point of view (with the following exceptions) the ST62E85, ST62T85 products have exactly the same software and hardware features of the ROM version.

On the ST62E85, all the 8192 bytes of PROGRAM memory are available for the user, as all the EPROM memory can be erased by exposure to UV light. On the ST62T85 (OTP) device a reserved area for test purposes exists, as for the ST6285 ROM device. In order to avoid any discrepancy between program functionality when using the EPROM, OTP and ROM it is recommended not to use these reserved areas, even when using the ST62E85.

Notes on programming:

In order to emulate exactly the ST6285 features with the ST62E85 and ST62T85, some software precautions have to be taken:

1. LCD RAM: The accessible segments are segments 9 to 24 and 33 to 56.

2. I/O: To prevent floating input or uncontrolled I/O interrupt, the port bit PA0-PA3, PB4-PB7 must be programmed as push-pull output.

3. Data Memory Space: write 40h at the address DFh of the Data Memory Space (disabled EEPROM).

4. Do not access data space locations: C7, CD, D9, DA, DB, DF, E5 to FE.

Other than these exceptions, the ST62E85, ST62T80 parts are fully compatible with the ROM ST6280 equivalent, this datasheet thus provides only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST6285 ROM-BASED DEVICE FOR FURTHER DETAILS.

EPROM ERASING

The EPROM of the windowed package of the ST62E85 may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST62E85 EPROM is such that erasure begins when the memory is exposed to light with wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST62E85 package be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.
The recommended erasure procedure of the ST62E85 EPROM is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST62E85 should be placed within 2.5 cm (1 inch) of the lamp tubes during erasure.

ST62T80 OTP Memory Map

ROM Page	Device Address	Description
Page 0	0000h-007Fh 0080h-07FFh	Reserved User ROM
Page 1 "STATIC"	0800h-0F9Fh 0FA0h-0FEFh 0FF0h-0FF7h 0FF8h-0FFBh 0FFCh-0FFDh 0FFEh-0FFFh	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
Page 2	0000h-000Fh 0010h-07FFh	Reserved User ROM
Page 3	0000h-000Fh 0010h-07FFh	Reserved User ROM

Note : EPROM addresses are related to the ROM file to be processed.

SGS-THOMSON
MICROELECTRONICS

*fuzzy*TECH™ ST6 Explorer Edition

FUZZY LOGIC DEVELOPMENT TOOL FOR ST6

DESIGN:

- System : up to four inputs and one output
- Variables: up to 7 labels per input/output
- Rules : up to 125 rules

ON-LINE OPTIMISATION:

- Real time visualisation and modification
- Data recording

OFF-LINE OPTIMISATION:

- Transfer plot: redundant or unstable rules
- Debugger: real time treatment from PC
- Time response: time plot of input/output
- Simulation: analysis of a built-in model

CODE GENERATOR:

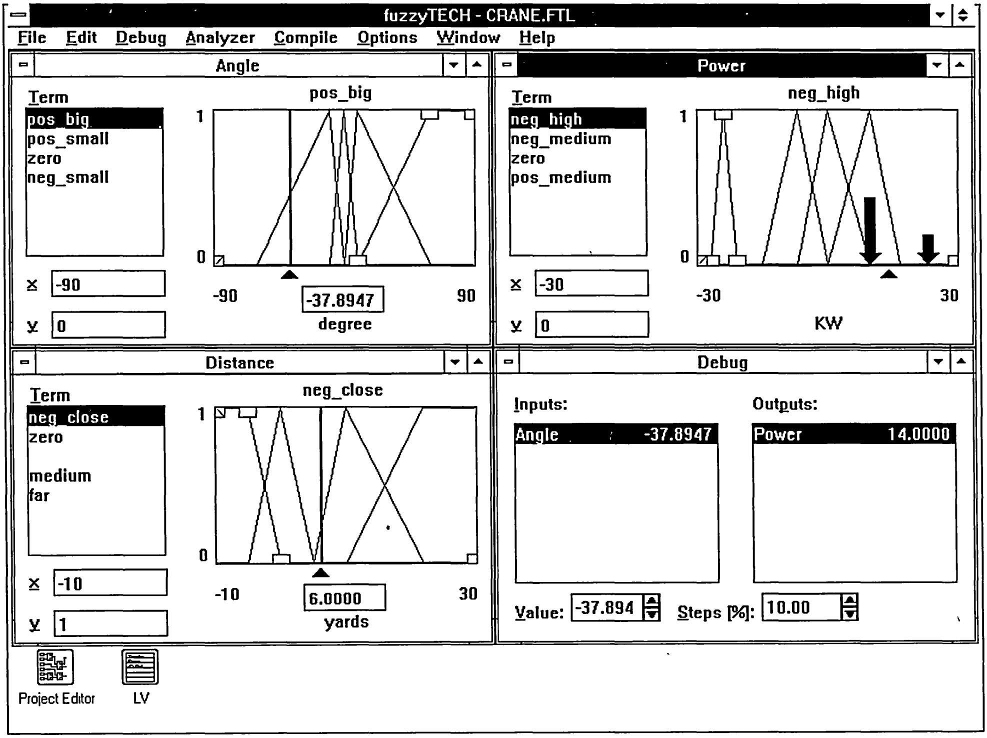
- Optimised ST6 assembly code
- No licence fee

USER INTERFACE:

- "point & click" tools MS-Windows™ compatible

PERFORMANCE (typical) :

- 7 rules / 2 inputs/ 1output 10ms
  580 bytes ROM - 30 bytes RAM
- 20 rules / 2 inputs/ 1output15ms
  670bytes ROM - 34 bytes RAM



Angle — Term: pos_big, pos_small, zero, neg_small
x: -90
y: 0
-37.8947

Power — Term: neg_high, neg_medium, zero, pos_medium
x: -30
y: 0

Distance — Term: neg_close, zero, medium, far
x: -10
y: 1
6.0000

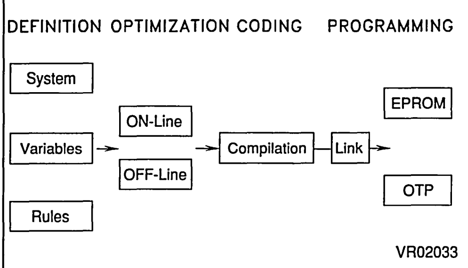
Debug — Inputs: Angle -37.8947 — Outputs: Power 14.0000
Value: -37.894 Steps [%]: 10.00

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

DESCRIPTION

*fuzzy*TECH ST6 Explorer Edition is an easy to use, high level software development tool optimised for the design of fuzzy logic controls with the ST6 microcontroller. It covers all the steps of a fuzzy logic design from the initial concept to the production of optimised ST6 executable code. In addition, its MS-Windows™ based interface takes full advantage of the intuitive approach of fuzzy logic to define and optimise the control with a very friendly approach. These features enable the fast development of optimised control.

Figure 1. A development flow chart



THE GRAPHIC DESIGN EDITORS:

*Fuzzy*TECH ST6 Explorer Edition includes three graphical editors for the definition of the system structure, linguistic variables and rules generation. The resolution is 8-bit for all internal and external data. These editors enable definition of the complete system with graphical tools using a "point & click" approach.

System:

- Up to 4 input variables per module
- 1 output variable per module
- Fast computation fuzzification method

Variables:

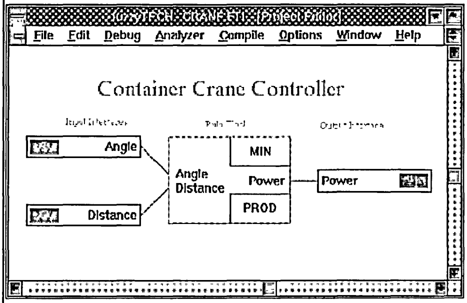
- Up to 7 terms per variable

Rules:

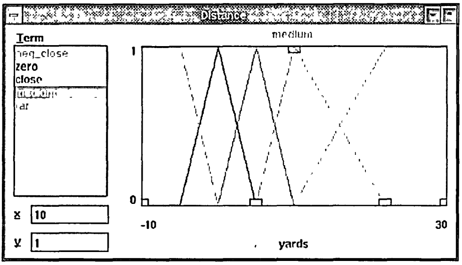
- Allows up to 125 rules
- Full graphical input with matrix or spreadsheet
- Supports standard Max-Min inference method

Figure 2. Design Screen Examples

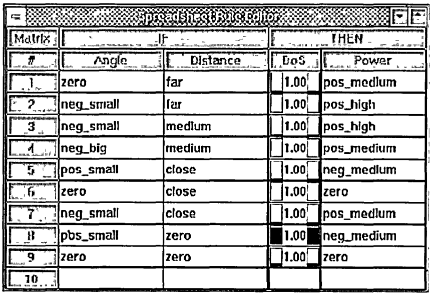
Example of System Architecture



Example of Variable Definition



Example of Rule Generator



Matrix	IF		THEN	
#	Angle	Distance	DoS	Power
1	zero	far	1.00	pos_medium
2	neg_small	far	1.00	pos_high
3	neg_small	medium	1.00	pos_high
4	neg_big	medium	1.00	pos_medium
5	pos_small	close	1.00	neg_medium
6	zero	close	1.00	zero
7	neg_small	close	1.00	pos_medium
8	pbs_small	zero	1.00	neg_medium
9	zero	zero	1.00	zero
10				

THE OPTIMISATION TOOLS:

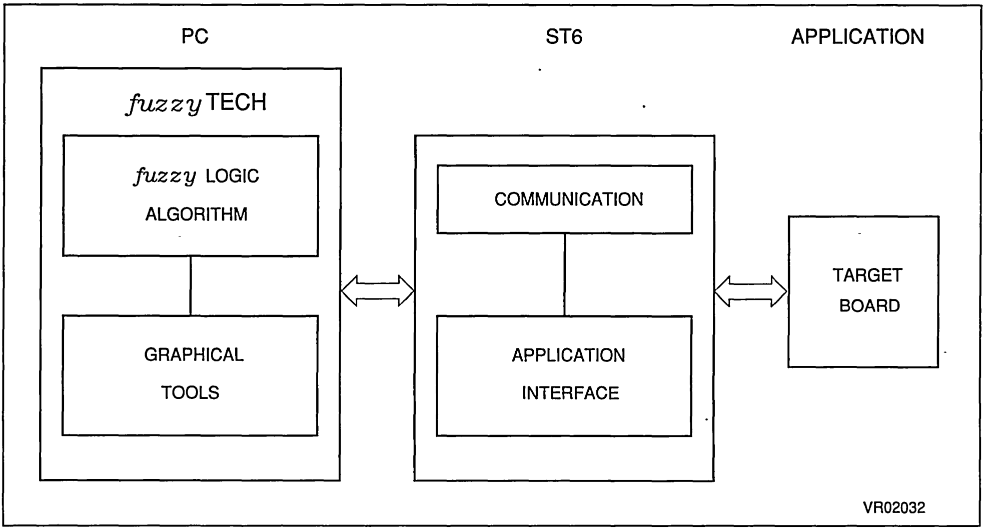
*fuzzy*TECH ST6 Explorer Edition provides several optimisation tools using real time data coming from the application or simulations of the system behaviour. The generated files can be treated with the graphical tools of *fuzzy*TECH or with other software running on a PC.

On-line optimisation:

- Real time visualisation and modification (serial debug mode):

This mode enables the visualisation and modification in real time of the fuzzy logic algorithm configuration from a PC. In this mode, the fuzzy logic algorithm is treated by the PC. The ST62 program includes the application interface and the PC interface protocol. An RS232 link provides the interface between the PC and the ST62. The optimisation tools of *fuzzy*TECH can be used in real time in this mode. This option can be used in applications with a dynamic operation of typically 100ms or slower.

Figure 3. Task sharing of the serial debug mode

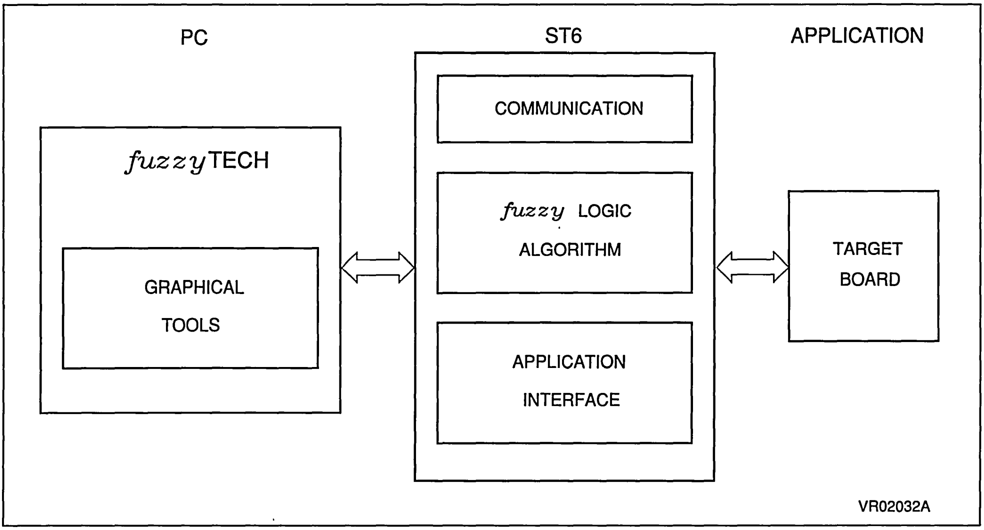


THE OPTIMISATION TOOLS (Continued)

- Data recording (file mode):

This mode enables the recording of input and output data coming from the ST62 in a PC. In this mode, the fuzzy logic algorithm is treated by the ST62 microcontroller. During each fuzzy iteration, the input and output data of the algorithm are sent by serial RS232 or a parallel port to the PC. This data can be used later inside the *fuzzy*TECH program or in any other software to visualise the control performance. This mode can be used in applications requiring a dynamic operation faster than 100ms.

Figure 4. Task sharing of the file mode



THE OPTIMISATION TOOLS (Continued)

Off-line optimisation:

The debugging tool uses files coming from the real application or from simulation. It generates files in the *fuzzy*TECH format which enables the use of the *fuzzy*TECH graphical tools to optimise the control algorithm.

- *fuzzy*TECH Debugger:

Test and verification of the system under design using different debug modes. The entire inference flow can be visualised, including rules and tracing variables.

- *fuzzy*TECH Time Response:

Rules and variable tracing either in real time, on the basis of recorded process data, or using a process simulation.

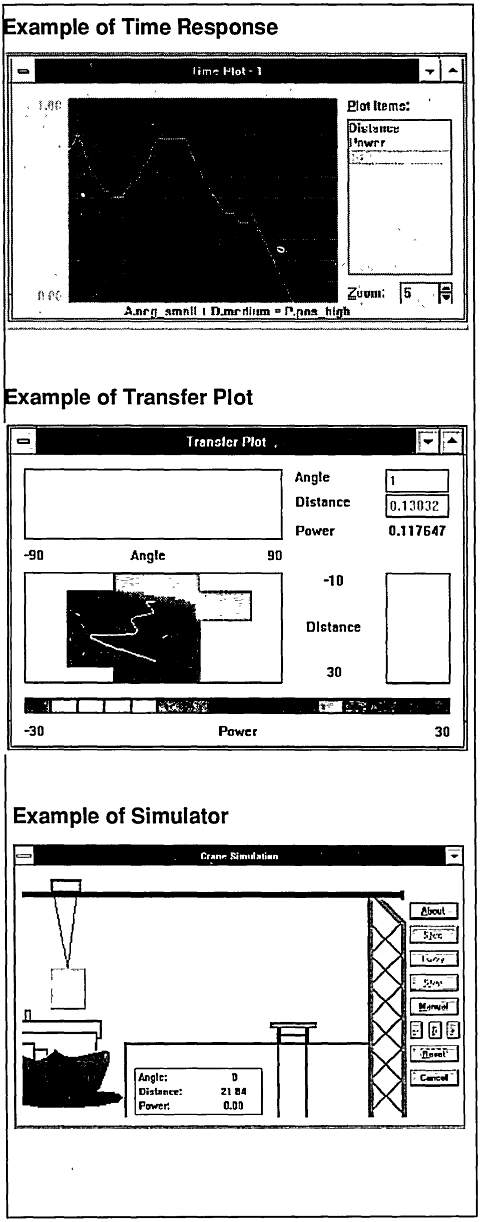
- *fuzzy*TECH Transfer Plot :

Visualisation with surface control of the operative rules to identify redundant rules and regions of instability.

- *fuzzy*TECH Simulator:

To get started right away, an animated simulator of a crane container control is provided. By experimenting how modifications on rules affect the crane performance, the basics of fuzzy logic control can be understood.

Figure 5. Optimisation Screen Examples



Example of Time Response

Example of Transfer Plot

Angle 1
Distance 0.13032
Power 0.117647

Example of Simulator

Angle: 0
Distance: 21 84
Power: 0.00

CODE GENERATOR:

*fuzzy*TECH is a hardware independent object oriented program dedicated to fuzzy logic. Its output has to be compiled and linked to the rest of the application prior to use in the target microcontroller.

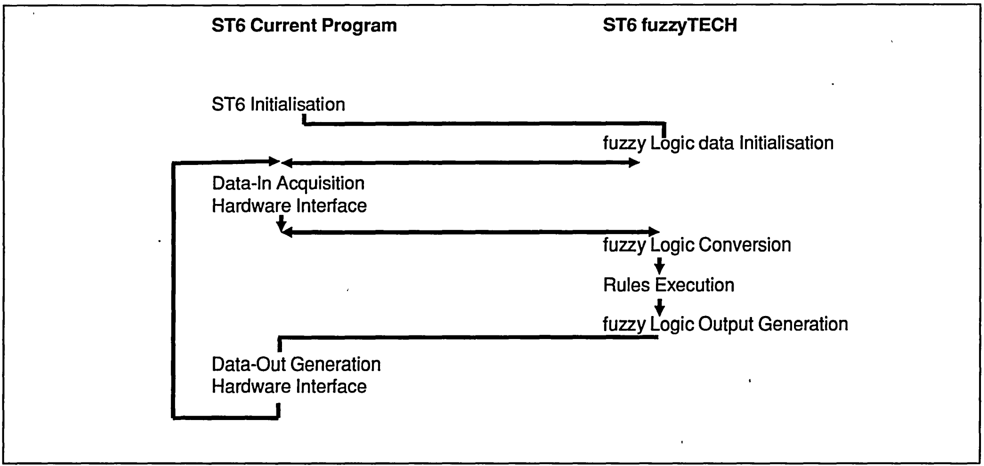
The ST6 code generator is used to produce highly optimised ST6 assembler code which minimises the program size. Data acquisition and data out is made using the conventional peripherals and programming resources of the microcontroller.

The fuzzy logic code is merged with the conventional program using the "link" procedure of the current ST6 programming software. The linked code is loaded into the ST6 EPROM or OTP part using an ST6 programming tool for full product evaluation, test and production.

TYPICAL PROGRAM FLOW CHART

The *fuzzy*TECH ST6 Explorer Edition blocks are called as subroutines of the ST6 application program. A typical flow chart is given here below:

Figure 6. Typical Flow Chart



APPLICATIONS

Fuzzy logic brings computer reasoning closer to the way people think. It suits well applications that are more easy to describe with a linguistic approach than with a mathematical model, especially non-linear systems. It provides also a bridge between the analog and digital world, enabling a designer with a good analog background to develop a microcontroller based control without digital expertise.

*fuzzy*TECH ST6 Explorer Edition is particularly useful in applications which can be defined with few inputs and one output and where a resolution of 8 bits and a dynamic range of around 100ms are sufficient to control the system.

Typical applications are home appliances (washing machine, vacuum cleaner and food processor,...) , temperature control (air conditioning, refrigeration, cooker, oven, central heating, furnace,...), sensor interfaces (InfraRed detector, Alarm, ...), motor control (speed or position), or battery chargers. Being user-friendly, *fuzzy*TECH enables a system expert without microcontroller knowledge to define the control in a short time.

APPLICATION NOTES

Several application notes describe practical systems designed with the *fuzzy*TECH ST6 Explorer Edition. They show how to take advantage of its friendly user interface and debugging facilities to design an optimised control, even for relatively fast "real time" loops, without specific experience on digital control techniques. These notes are enclosed in the *fuzzy*TECH ST6 EXPLORER EDITION documentation.

HARDWARE/SOFTWARE REQUIREMENTS

- A 80386 (or higher) PC with at least 2Mbyte of memory
- MS-Windows 3.1™ or higher and MS-DOS 5.0 or higher
- Hard disk with 5 Mbyte of free space and a 3.5" floppy disk
- VGA monitor supported by Windows

The generated ST6 assembly code runs on every member of the ST6 microcontroller family. For the implementation, ST6 assembler/linker software and a programmer socket are required.

Each *fuzzy*TECH ST6 Explorer Edition set includes a 3.5" floppy disk and two books, one user manual with application notes and one detailed datasheet.

*fuzzy*TECH is a trade mark of Inform Software Corp.

ST6 is a trade mark of SGS-THOMSON Microelectronics.

MS-Windows and MS-DOS are registered trademarks of Microsoft Corp.

ST62 STARTER KITS

SGS-THOMSON MICROELECTRONICS

ST6220-KIT

STARTER KIT FOR ST622x/1x MCU FAMILY

Preliminary Data

- Basic Programmer board enables to program EPROM device
- Power supply and 25 wire flat cable
- ST62E20F1 (20 pins): 2 pieces
  ST62E25F1 (28 pins): 2 pieces
- ST6 Software Tools includes the ST6 Assembler, the ST6 Linker, the ST6 Simulator and the interface to drive the Basic Programmer board.
- Application softwares are documented software modules that you may copy or link in your applications
- Documentation includes Kit Guide, ST621x/2x User Manual and ST62/ST63 Software Development Tools User Manual

DESCRIPTION

The STARTER KIT gives a quick entry to the ST62 world. It provides a basic development system that can be used by every design engineer. It is particularly useful for evaluation of the ST6210/15 and ST6220/25 Microcontrollers as well as for development of simple applications.

SYSTEM REQUIREMENTS

To use the Starter Kit, you must have a PC-AT compatible personnal computer equipped with:

- A hard disk and a 5"1/4 diskette drive
- 640 K of conventional main memory
- One Parallel Centronic compatible port
- MS-DOS version 3.10 or higher

This is Preliminary Data from SGS-THOMSON, details are subject to change without notice.

Using the ST622x STARTER KIT

The ST621x/2x USER MANUAL gives extensive description of the hardware and software aspects of the ST6210, ST6215, ST6220 and ST6225 microcontrollers. It contains all the information design engineers require to design the application hardware and the ST6210/15 source software.

The enclosed ST6 Assembler enables the transformation of the ASCII source file into an executable file. The ST6 Assembler documentation is located in the ST6 SOFTWARE DEVELOPMENT TOOLS USER MANUAL.

Smart programming implies the use of several modules, each of them performing an elementary task. Because each module can be quickly individually tested and debugged, the overall debug time is drastically reduced thus speeding the development of bug free application software. The ST6 Linker is use to make one program out of several modules. The ST6 SOFTWARE DEVELOPMENT TOOLS USER MANUAL also contains the associated documentation.

Each module, and the linked program, may be tested and debugged using the ST6 Simulator, also described in the ST6 SOFTWARE DEVELOPMENT TOOLS USER MANUAL. Once debugged, the application software can then be regarded as functionally working. It can then be programmed into an EPROM device using the BASIC PROGRAMMER described later in this guide.

Once successfully simulated, application software must be tested in circuit in order to check that there are no errors due to differences between the functional description of the environment and the real operating conditions. This test can be made by plugging an EPROM device into the application hardware and performing standard hardware debugging. However, high level applications require a Real Time Development Tools to be used (see data sheet in the ST621x/2x USER MANUAL).

The last step in developping an ST62 application consists of checking the validity of the complete product specification by making prototypes. The One Time Programmable devices (OTP) available in the ST62 family are well suited to such field tests.

The user is then ready to go into production using either the economical ST62T1x/T2x OTPs or masked ROM devices.

ORDERING INFORMATION

Sales Type	Description
ST6220-KIT/220	Complete kit for operation from 220Vac mains
ST6220-KIT/110	Complete kit for operation from 110Vac mains
ST6220-KIT/UK	Complete kit for operation in UK

ST622x-KIT

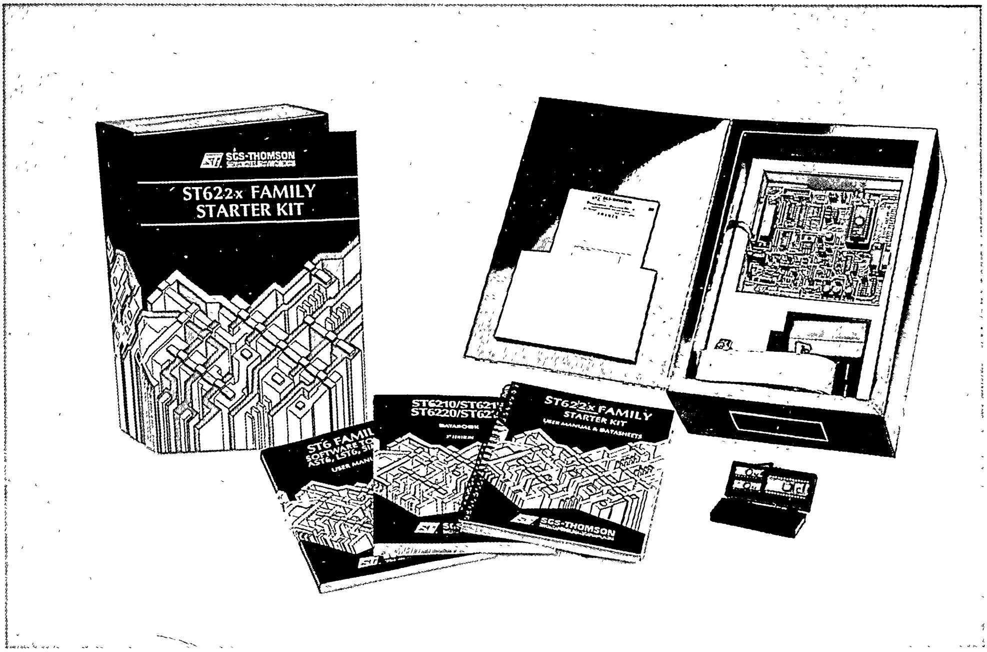
STARTER KIT FOR ST622x MCU FAMILY

HARDWARE FEATURES

- Immediate evaluation of ST62E25 with demonstration examples
- Program debugging by connection of an application environment to the board
- On board programming of ST62E20, ST62T20, ST62E25 and ST62T25
- In-circuit programming of ST62E2x and ST62T2x through the Starter Kit

SOFTWARE FEATURES

- Software simulator including I/O read/write
- Assembler, linker, debugger
- EPROM/OTP programming utilities
- Application examples



August 1994

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

1 DESCRIPTION

The ST622x Starter Kit can be used for evaluation, simulation and emulation purposes. First, it can be used to demonstrate the capabilities of the ST6225. It is only necessary to connect the supply to the board and to load the demonstration software provided with the Kit into the ST62E25 sample.

The same board can be used as a hardware interface to the software simulator when connected to the PC. Analog or digital values from the ST622x I/O pins can also be loaded directly to the simulator.

Once the program is successfully simulated, it can be loaded in a ST62E25 or ST62E20 by using the on-board programmer (DIL packaged devices only). The application environment can be connected to the Starter Kit via the I/O connector to perform a full evaluation of the user application.

In addition, an in-circuit programming facility is provided with the Kit to enable programming, via the Starter Kit board, of any ST62E2x (EPROM) or ST62T2x (OTP) already mounted in the user application board.

Hardware items

The Kit includes 2 samples of ST62E25, 2 samples of ST62E20, an RS232 interface, a temperature control circuit, a trimmer, a set of LED and buttons, all cables plus a power supply. Pins are available for direct connection to an external user application. The board is connected to the PC via the parallel port.

Software items

The diskette provided with this kit includes an enhanced simulator including I/O read/write, assembler, linker, EPROM/OTP ST6 programming facilities and demonstration examples.

Documentation

A full set of documents is provided with the Kit including the ST622x data book, a Kit guide and the ST62/63 Software Development Tools user manual.

System requirement

The ST622x Starter Kit communicates with a PC-AT compatible Personal Computer equipped with a hard disk and a 5 1/4" diskette drive, 640k of conventional memory, one parallel Centronic compatible port and MS-DOS version 3.10 or higher.

Bulletin Board Systems

Upgrades of Software Tools, example code and documentation are available to Registered users through the SGS-THOMSON Bulletin Board Systems (BBSs). These are accessible by Modem at the following numbers:

- *In the USA*:

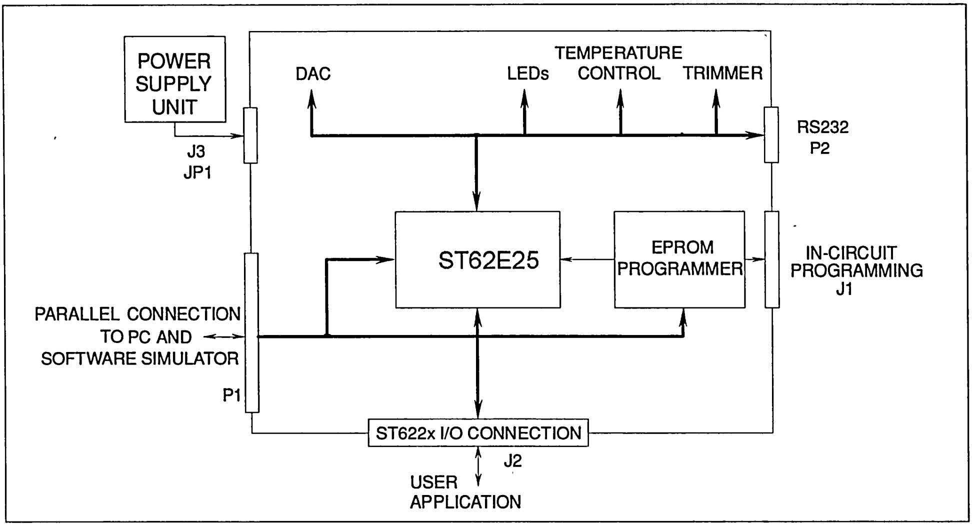
(1) 708 517-1898 2400 baud (V22bis), 8-bits, No Parity, 1 Stop bit (8,N,1)

- *In Europe*:

Micros Technical Support Hotline (France): (+33) 76 48 99 28
9600 baud (V32) and lower, 8,N,1
Microcontroller Support (France): (+33) 42 29 14 16
9600 baud (V32) and lower, 8,N,1

DESCRIPTION (Continued)

Figure 1. Block Diagram of ST622X Starter Kit



Kit Contents

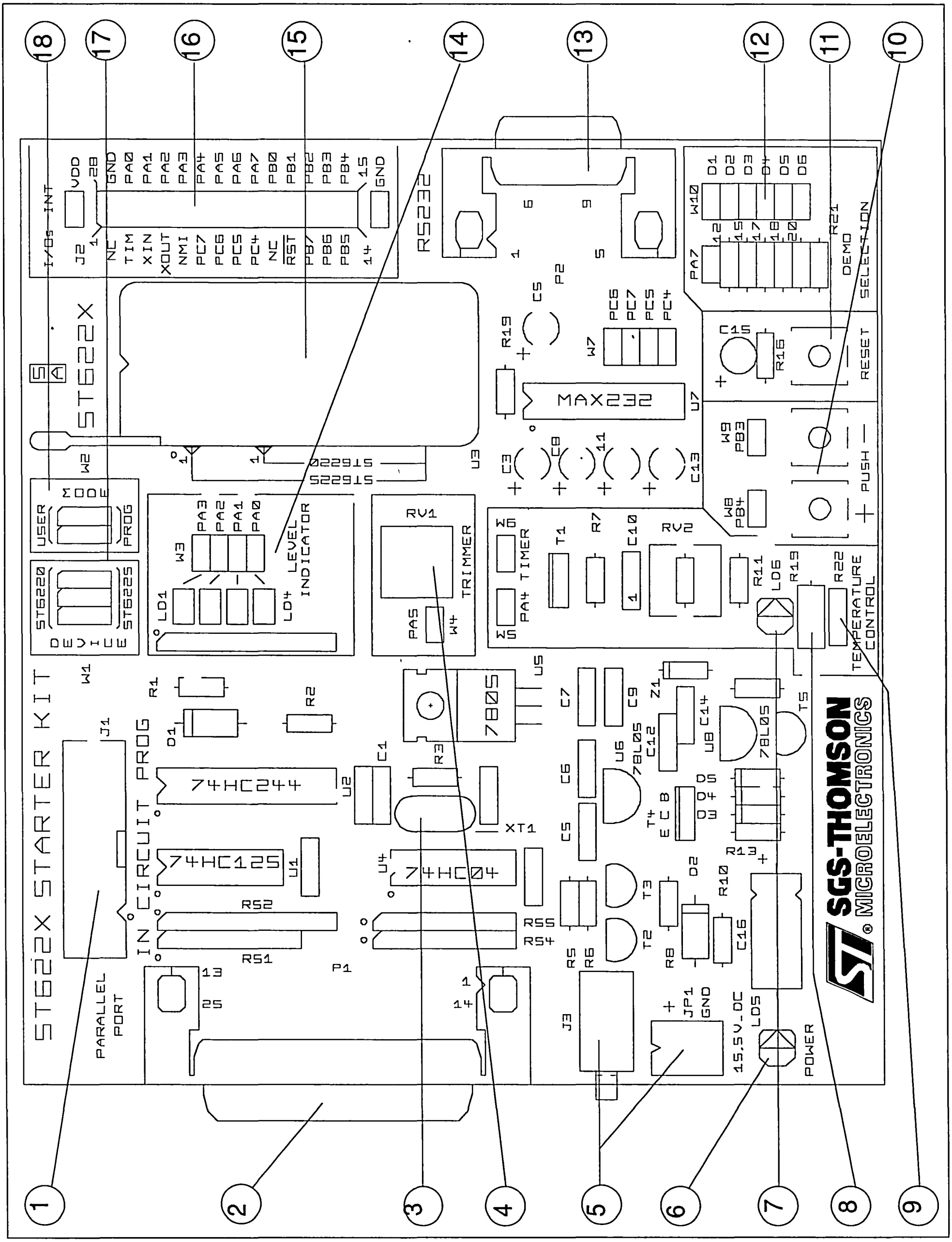
ST622x STARTER KIT Board:	- Typical application board based on ST6225 MCU - MCU Peripherals evaluation/emulation facilities - ST622x EPROM/EEPROM programming functions - "In Situ" connector for any ST622x programming - Power supply and PC-AT connection cable
SOFTWARE TOOLS:	- AST6/LST6 ST6 family assembler/linker - SIMST6 simulator software performing dedicated access to the board MCU peripherals - ST622xPG EPROM/EEPROM programming software
ST622x APPLICATION ROUTINES:	- Demonstration programs - Basic subroutines library
ASSOCIATED DOCUMENTS:	- STARTER KIT GUIDE - ST6 SOFTWARE TOOLS MANUAL (DBST6SOFTOST/1) - ST6 PROGRAMMING MANUAL (DBST6ST/3) - ST622x family DATA BOOK (DBST6ST/3)

2 HARDWARE DESCRIPTION

2.1 Board overview

1 - IN CIRCUIT programming connector J1
2 - PC station connector P1 (for links to simulator and programming softwares)
3 - 8 Mhz crystal oscillator
4 - 10 Kohms trimer including jumper W4-PA5
5 - Power supply JACK connector J3 and JP1 pads
6 - Power supply LED indicator LD1
7 - Heater resistor power LED indicator LD2
8 - Heater resistor circuit including jumper W6-TIMER
9 - Thermistor circuit including jumper W5-PA4
10 - "+" and "-" pushbuttons including jumpers W8-PB4 and W9-PB3
11 - RESET pushbutton
12 - Demonstration routine selector including jumpers W10
13 - RS232 interface circuit and connector including jumpers W7
14 - 4 LEDs Level indicator including jumpers W3
15 - DIL 20-28 MCU socket
16 - User's I/O interface connector J2
17 - "ST6220" or "ST6225" device selection jumpers W1
18 - "Programming" or "User" operating mode selection jumpers W2

Figure 2. Board Overview



ORDERING INFORMATION TABLE

Sales Type	Description
ST6220-KIT/220	Complete kit for operation from 220 Vac mains
ST6220-KIT/110	Complete kit for operation from 110 Vac mains
ST6220-KIT/UK	Complete kit for operation in United Kingdom

SGS-THOMSON MICROELECTRONICS

ST626x-KIT

STARTER KIT FOR ST626x MCU FAMILY

HARDWARE FEATURES

- Immediate evaluation of ST62E65 with demonstration examples
- Program debugging by connection of an application environment to the board
- On board programming of ST62E60, ST62T60, ST62E65 and ST62T65
- In-circuit programming of ST62E6x and ST62T6x through the Starter Kit

SOFTWARE FEATURES

- Software simulator including I/O read/write
- Assembler, linker, debugger
- EPROM/OTP programming utilities
- Application examples

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

1 DESCRIPTION

The ST626x Starter Kit can be used for evaluation, simulation and emulation purposes. First, it can be used to demonstrate the capabilities of the ST6265. It is only necessary to connect the supply to the board and to load the demonstration software provided with the Kit into the ST62E65 sample.

The same board can be used as a hardware interface to the software simulator when connected to the PC. Analog or digital values from the ST626x I/O pins can also be loaded directly to the simulator.

Once the program is successfully simulated, it can be loaded in a ST62E65 or ST62E60 by using the on-board programmer (DIL packaged devices only). The application environment can be connected to the Starter Kit via the I/O connector to perform a full evaluation of the user application.

In addition, an in-circuit programming facility is provided with the Kit to enable programming, via the Starter Kit board, of any ST62E6x (EPROM) or ST62T6x (OTP) already mounted in the user application board.

Hardware items

The Kit includes 2 samples of ST62E65, 2 samples of ST62E60, an audio transducer, an RS232 interface, a thermistor, a trimmer, a set of LED and buttons, all cables plus a power supply. Pins are available for direct connection to an external user application. The board is connected to the PC via the parallel port.

Software items

The diskette provided with this kit includes an enhanced simulator including I/O read/write, assembler, linker, EPROM/OTP ST6 programming facilities and demonstration examples.

Documentation

A full set of documents is provided with the Kit including the ST626x data book, a Kit guide and the ST62/63 Software Development Tools user manual.

System requirement

The ST626x Starter Kit communicates with a PC-AT compatible Personal Computer equipped with a hard disk and a 5 1/4" diskette drive, 640k of conventional memory, one parallel Centronic compatible port and MS-DOS version 3.10 or higher.

Bulletin Board Systems

Upgrades of Software Tools, example code and documentation are available to Registered users through the SGS-THOMSON Bulletin Board Systems (BBSs). These are accessible by Modem at the following numbers:

- *In the USA*:

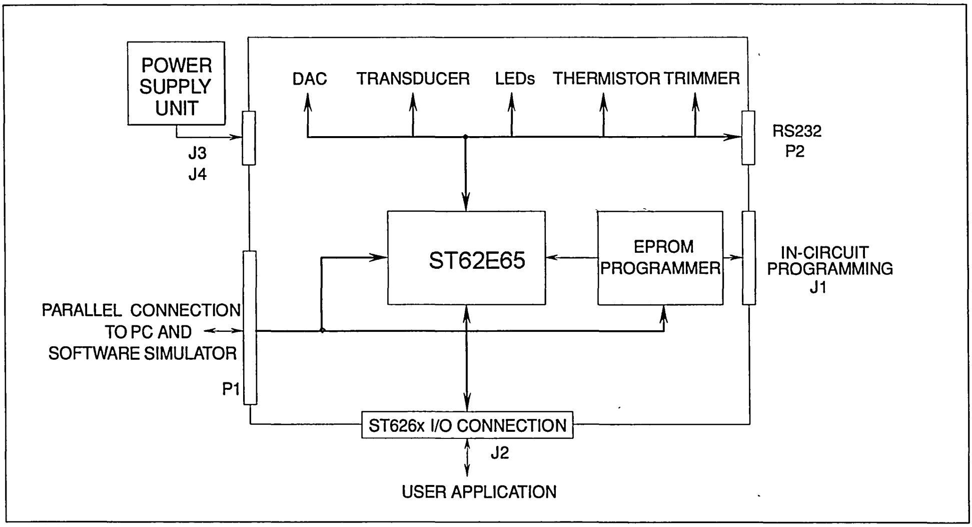
(1) 708 517-1898   2400 baud (V22bis), 8-bits, No Parity, 1 Stop bit (8,N,1)

- *In Europe*:

Micros Technical Support Hotline (France): (+33) 76 48 99 28
    9600 baud (V32) and lower, 8,N,1
Microcontroller Support (France): (+33) 42 29 14 16
    9600 baud (V32) and lower, 8,N,1

DESCRIPTION (Continued)

Figure 1. Block Diagram of ST626X Starter Kit



Kit Contents

ST626x STARTER KIT Board:	- Typical application board based on ST6265 MCU - MCU Peripherals evaluation/emulation facilities - ST626x EPROM/EEPROM programming functions - "In Situ" connector for any ST626x programming - Power supply and PC-AT connection cable
SOFTWARE TOOLS:	- AST6/LST6 ST6 family assembler/linker - SIMST6 simulator software performing dedicated access to the board MCU peripherals - ST626xPG EPROM/EEPROM programming software
ST626x APPLICATION ROUTINES:	- Demonstration programs - Basic subroutines library
ASSOCIATED DOCUMENTS:	- STARTER KIT GUIDE - ST6 SOFTWARE TOOLS MANUAL (DBST6SOFTOST/1) - ST6 PROGRAMMING MANUAL (DBST6ST/3) - ST626x family DATA BOOK (DBST6ST/3)

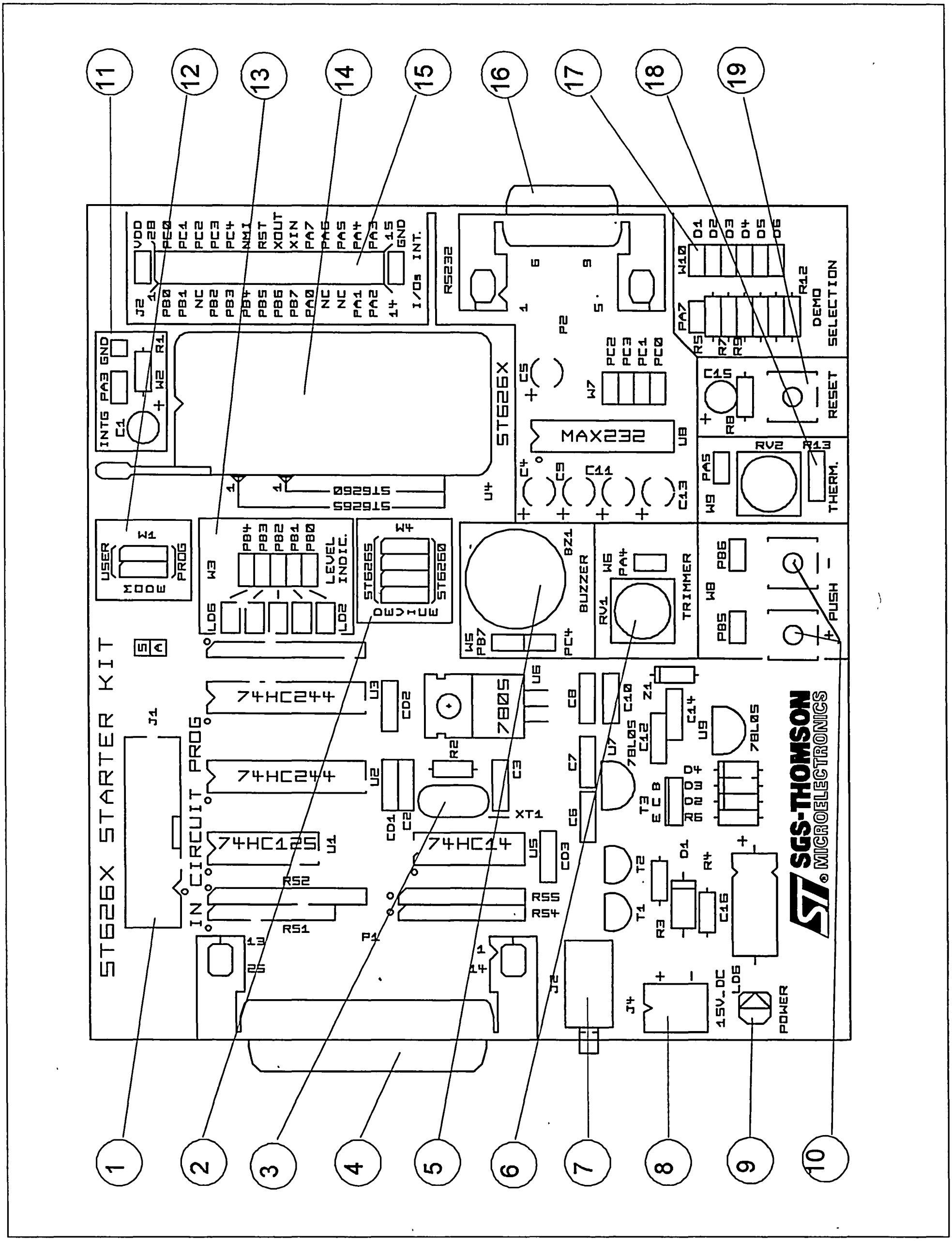
2 HARDWARE DESCRIPTION

2.1 Board overview

1 - IN CIRCUIT programming connector J1
2 - "ST6260" or "ST6265" device selection jumpers W4
3 - 8 Mhz crystal oscillator
4 - PC connector P1 (for links to simulator and programming software)
5 - Audio Transducer circuit (Buzzer) including jumpers W5
6 - 10 Kohm trimmer and jumpers W6
7 - Power supply JACK connector J3
8 - Power supply connector J4
9 - Power supply LED indicator
10 - "+" and "-" pushbuttons and jumpers W8
11 - DAC integrator circuit including jumpers W2
12 - "Programming" or "User" operating mode selection jumpers W1
13 - 5 LED Level indicator including jumpers W3
14 - DIL 20-28 MCU socket
15 - User's I/O interface connector J2
16 - RS232 interface circuit and connector including jumpers W7
17 - Demonstration routine selector (jumpers W10)
18 - Thermistor circuit including jumpers W9
19 - RESET pushbuttons and jumpers W8

Note: DAC is a Digital to Analog Conversion circuit.

Figure 2. Board Overview



ORDERING INFORMATION TABLE

Sales Type	Description
ST6260-KIT/220	Complete kit for operation from 220 Vac mains
ST6260-KIT/110	Complete kit for operation from 110 Vac mains
ST6260-KIT/UK	Complete kit for operation in United Kingdom

SGS-THOMSON
MICROELECTRONICS

ST6240-KIT

STARTER KIT FOR ST624x MCU FAMILY

PRELIMINARY DATA

HARDWARE FEATURES

- Immediate evaluation of ST62E40 with a demonstration examples
- Program debugging by connection of an application environment to the board
- On board programming of ST62E40 and ST62T40
- In-circuit programming of ST62E4x and ST62T4x through the Starter Kit

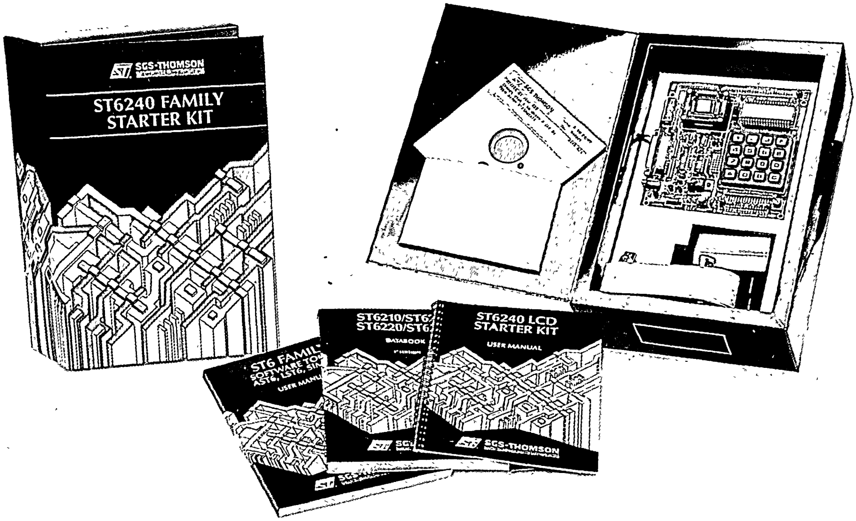
SOFTWARE FEATURES

- Software simulator including LCD display and I/O read/write
- Assembler, linker, debugger
- EPROM/OTP programming utilities
- Application examples

DESCRIPTION

The ST6240 Starter Kit can be used for evaluation, simulation and emulation purposes. First, it can be used to demonstrate the capabilites of the ST6240. It is only necessary to connect the supply to the board and to load the demonstration software provided with the Kit into the ST62E40 sample; LCD and keyboard interfacing can be immediately evaluated.

The same board can be used as a hardware interface to the software simulator when connected to the PC, allowing display values from the simulator to be displayed directly on the LCD. Analog or digital values from the ST624x I/O pins can also be loaded directly to the simulator.


SGS-THOMSON
ST6240 FAMILY STARTER KIT
ST6 FAMILY SOFTWARE TOOLS
ST6210/ST62 ST6220/ST62 DATABOOK
ST6240 LCD STARTER KIT USER MANUAL
SGS-THOMSON

This is preliminary data from SGS-THOMSON, details are subject to change without notice

DESCRIPTION (Continued)

Once the program is successfully simulated, it can be loaded in the ST62E40 sample with the on-board programmer.
The application environment can be connected to the Starter Kit via the I/O connector to perform a full evaluation of the user application.

In addition, since the LCD is connected to the PCB via a socket, it can easily be removed and replaced by a customized LCD.

QFP packages are difficult to handle manually, so an in-circuit programming facility is provided with the Kit to enable programming, via the Starter Kit board, of any ST62E4x (EPROM) or ST62T4x (OTP) already soldered in the user application board.

Hardware items

The Kit PCB includes a QFP80 socket, a 16 key keyboard, a 32 segment x 4 LCD, an ST62E40 and cables plus a power supply.

Pins are available for direct connection to an application.

The board is connected to the PC via the parallel port.

Software items

The diskette provided with this kit includes an enhanced simulator including control of the external LCD display and I/O read/write, assembler, linker, debugger, EPROM/OTP ST6 programming facilities and demonstration examples.

Documentation

A full set of documents is provided with the Kit including the ST62 LCD drive data book, a Kit guide and the ST62/63 Software Development Tools user manual.

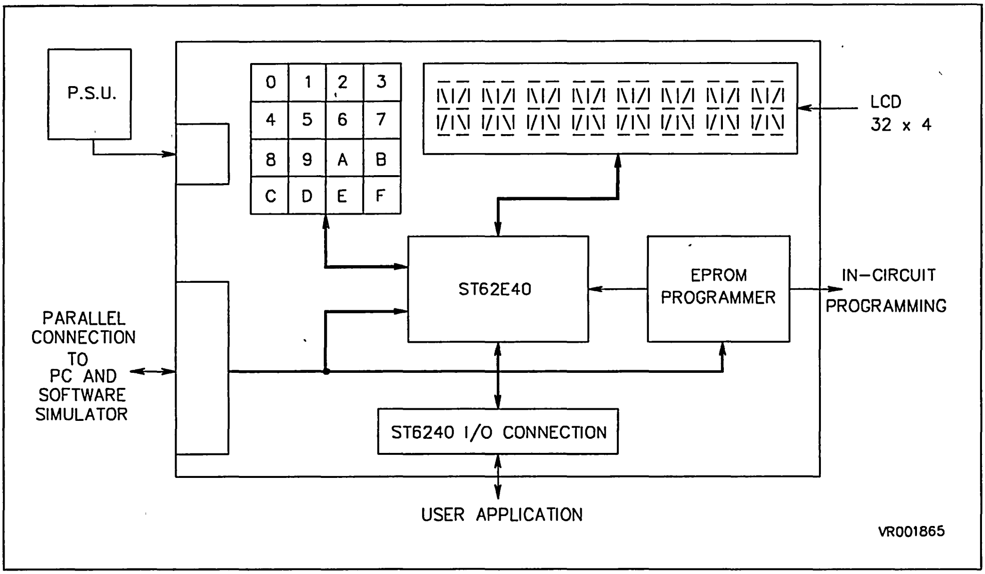
System requirement

The ST624x Starter Kit communicates with a PC-AT compatible Personal Computer equipped with a hard disk and a 5"1/4 diskette drive, 640k of conventional memory, one parallel Centronic port and MS-DOS version 3.10 or higher.

Ordering information

Sales type	Description
ST6240-KIT/220	Complete kit for operation from 220Vac mains
ST6240-KIT/110	Complete kit for operation from 110Vac mains
ST6240-KIT/UK	Complete kit for operation in UK

Block Diagram of ST6240 Starter Kit



DEVELOPMENT TOOLS

SGS-THOMSON
MICROELECTRONICS

ST6-SW

SOFTWARE DEVELOPMENT TOOLS FOR ST6 MCU FAMILY

- Includes:
  - Macro assembler
  - Linker
  - Software simulator
- Runs on MS-DOS systems
- Window based graphic interface
- Extensive symbol manipulation

GENERAL DESCRIPTION

Full software development tools is achieved using the ST6 Software Development Tools consisting of a powerful macro assembler, a linker and a software simulator.

The ST6 Macro assembler accepts a source file written in ST6 assembly language using any text editor package and transforms it in an ST6 executable file.

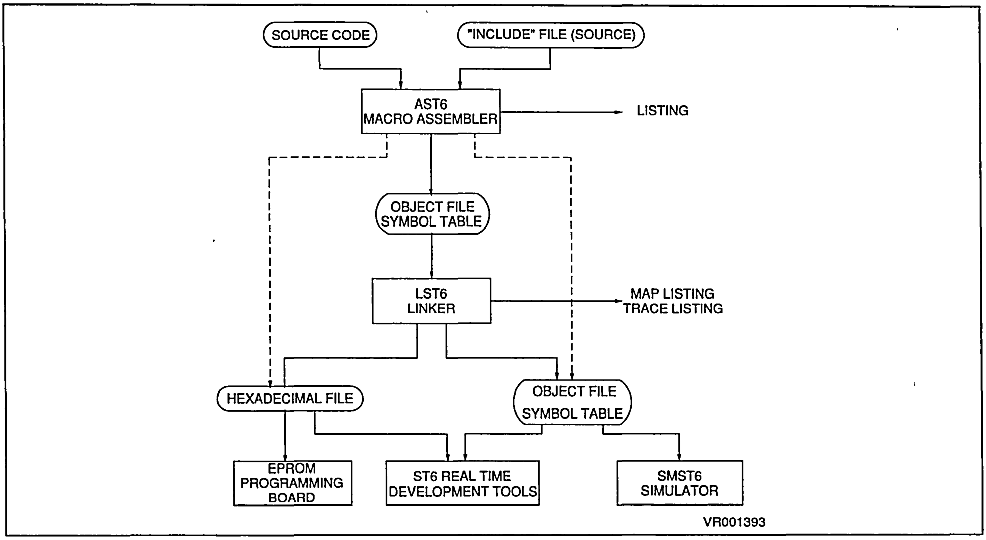
To enable good testability and fast debugging, many application software are made up of several modules, each of them performing an elementary task. Each module is assembled independently of the others, thus producing a number of object files. The ST6 Linker combines these object files into a single executable program. Both object format and hexadecimal format are produced. The hexadecimal file is used to program an EPROM while the object file is used to run the simulator or the debugger.

The ST6 Software Simulator allows the user to debug and execute any executable program written for any member of the ST62/ST63 family of microcontrollers without the aid of additional hardware.

Once debugged with the simulator, the program can be programmed into an EPROM device by using the hexadecimal file and the ST6 programming board. By plugging the EPROM device into the application hardware, simple applications can be debugged without the need of an emulator.

The ST6 Hardware Development Tools are required where high performance debugging is needed.

Figure 1. Development Flow Chart



ST6 ASSEMBLER

- Macro call and conditional assembly
- Extensive symbol manipulation
- Error diagnostics

General Description

The ST6 Macro assembler accepts a source file written in ST6 assembly language and transforms it into an executable file in relocatable object code format. When the whole program is in one file only, the assembler also generates an hexadecimal file (INTEL hex format) ready to be programmed into an EPROM device.

The assembler recognizes the use of section, symbols, macros and conditional assembly directives. In addition, the ST6 Assembler is able to produce detailed assembly listing and symbol cross reference file.

Figure 2. AST6 Directives

.ASCII	Stores in program space a string as a sequence of ASCII codes
.ASCIZ	Same as .ASCII followed by a null character
.BLOCK	Reserves a block of contiguous memory location
.BYTE	Stores successive bytes of data in program space
.DEF	Defines the characteristics of a data space location
.DISPLAY	Displays a string during assembly process
.DP_ON	Segments the data space
.EJECT	Starts a new listing page
.ELSE	Beginning of the alternative part in conditional assembly block
.END	End of source file
.ENDC	End of conditional assembly block
.ENDM	End of a macro definition
.EQU	Assigns the value of an expression to a label
.ERROR	User defined assembly error
.EXTERN	Defines a symbol as external
.IFC	Beginning of conditional assembly block
.INPUT	Includes an additional source file in the present one
.GLOBAL	Defines a symbol as global
.LABEL.W	Initializes Data ROM Window Register
.LABEL.D	Gains access to a label in a Data ROM Window
.LINESIZE	Set listing line length
.LIST	Enables the listing of specified fields of the source file
.MACRO	Beginning of a macro definition
.MEXIT	End of a macro expansion
.NOTRANSMIT	Inhibits symbol transmission to the linker
.ORG	Set current location counter
.PAGE_D	Specifies the page number in data space
.PL	Set listing page length
.PP_ON	Segments the program space in 2K pages
.ROMSIZE	Defines the available ROM size
.SECTION	Provides a logical partitioning of program space
.SET	Same as .EQU, but can be redefined in the source file
.TITLE	Assigns title to the document
.TRANSMIT	Transmits symbol definitions to the linker
.VERS	Defines the target ST6 device
.WARNING	User defined assembly warning
.WINDOW	Defines a continuous relocatable block of program code
.W_ON	Enables the use of the .WINDOW directive
.WORD	Stores successive words of data in program space

ST6 LINKER

- Links up to 32 modules
- Extensive symbol manipulation
- 33 sections (including interrupt vectors)
- Error diagnostics

The ST6 Linker is responsible for combining a number of object files into a single program, associating an absolute address to each section of code, and resolving any external references.

The ST6 Linker produces an hexadecimal file in INTEL format to be down loaded into an EPROM device and an object code file to be used with the simulator. The linker also produces a map file which gives information about the sections, pages, modules and labels. Finally, listing files are produced which update the assembler listings with real addresses of symbols and statements.

This software program allows the user to develop modular programs, which may then be combined and addressed as defined by the user. The flexibility of the ST6 Linker is greatly increased by the use of sections allowing the user to group pieces of software from different modules. The location and the size of each section is user selectable.

ST6 SIMULATOR

- Window based graphic interface
- On line assembler/disassembler
- Supports symbolic debugging
- 128 breakpoints and 128 software traps
- TRACE mode
- I/O and CLOCK simulation

SIMST6 allows the user to debug and execute any program written for any of the current and future members of the ST6 family of microcontrollers, without the aid of additional hardware.

The user specifies the target device, its mapping and the object code file to be used. The simulator functionally duplicates the operation of the ST6 and completely supports the instruction set. I/O channels may be opened, read, and written, in order to simulate the I/O functions of peripherals, while interrupts may be set, and then set pending, in order to simulate the handling of interrupts. The simulator uses the clock frequency assigned by the user, along with the number of clock cycles needed by each instruction to keep track of the real time execution speed.

The ST6 Simulator accepts command lines in both interactive and batch mode.

ORDERING INFORMATION

Sales Type	Description
ST6-SW	ST6 software development tools (includes assembler, linker and emulator)

Note : The ST6 software package is included in all ST6xxx-EMU real time develoment tools.

SGS-THOMSON MICROELECTRONICS

ST6xxx-EMU

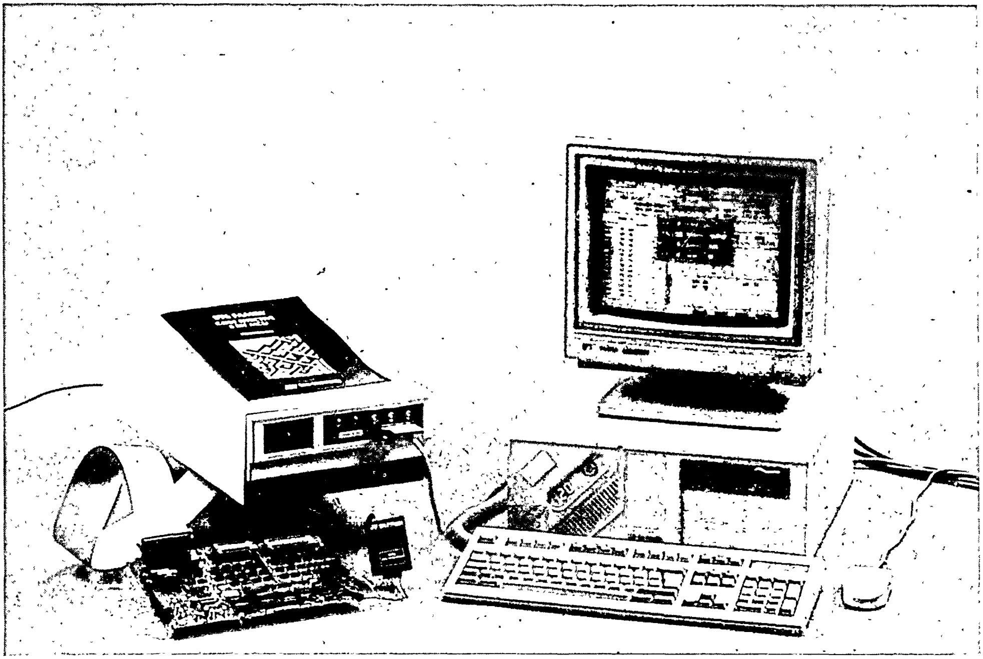
REAL TIME DEVELOPMENT TOOLS FOR ST6 MCU FAMILY

HARDWARE FEATURES

- Supports ST62xx and ST63xx family
- Real time emulation
- 32 KBytes of emulation memory
- Breakpoints on up to 256 events
- Events can be defined on program space, data space and on up to 4 external signals
- 1K of real trace memory
- Tracing of up to 32 bits including 4 external signals

SOFTWARE FEATURES

- Symbolic debugger
- Window based interface
- On line assembler/disassembler
- Log files capable of storing any displayed screen
- Command files able to execute a set of debugger commands



April 1993

GENERAL DESCRIPTION

The ST6 Real Time Development System is an advanced hardware development system designed and configured to provide comprehensive support for the ST6 family of MCU's.

The mainframe consists of a basic part, common to all ST6 devices, and one (ST62 sub family) or two (ST63 sub family) dedicated board depending of specific device to emulate. Only the dedicated boards have to be changed to emulate a new device within the ST62/ST63 subfamilies.

The software part of the real time emulation tool is the symbolic debugger. It can be run on a PC compatible system and is common to all ST62/ST63 devices. It drives the emulator mainframe through an RS232 channel. The debugger uses a windowed menu driven user interface and enables the user to set the configuration of the emulator.

Once assembled and eventually linked and debugged by using the simulator, the application software is ready to be down loaded into the ST6-EMU. The device probe is connected into the application hardware. The development station will perform a real time emulation of the target device, thus allowing high performance test and debugging of both application hardware and software.

The breakpoints allow user to stop the MCU when the application software reaches selected addresses and/or addresses within a selected ranges and/or on data fetch (or read or write or both) cycles. The user is then able to read and modify any register and memory location. An on line assembler/disassembler is also available to ease the debugging.

The logic analyser can be used when real time emulation is needed. It allows to display the last 1024 cycles. The displayed cycles are either fetch cycles only or fetch cycles and data space accesses. Addresses, data, control/status bits and 4 user signals are displayed using mnemonic and user symbols.

Such a powerful tool enables the user to detect and trap any pattern and thus quickly debug the application. The trapping of random patterns is greatly improved by the capability to quit the emulation session while the emulator continue to run the application software. When the user re-enters the debugger, the emulation session resumes and information about any events of interest will be flashed to the screen in the form of a message.

Log files offer the ability to send any screen display to a text file. In particular, log files are very useful to save the contents of the logic analyser and/or the contents of data registers to be analysed or printed.

Command files can be used to execute a set of debugger commands in order to ease and speed up the emulation session.

A powerful help facility can be called at any time to give additional information about the commands, the processor or the emulator.

When the program is fully debugged, the ST6 EPROM remote programming board can be used to program the emulation device with the INTEL hex format file produced by the linker.

Figure 1. SDBST6 Command Summary

ALL	One Line Assembler
BASE	Change base of numbers
BREAK	Display/set breakpoint
CB	Clear breakpoints
CMP	Compare memory
DL	Display memory in listing ASM form
DM	Display/change memory
DOS	Branch to DOS
DR	Display/change registers
DS	Display symbol table
FM	Fill memory with pattern
GO	Start user program
GRAPH	Return to GRAPHIC interface
HELP	Call HELP utility
HWTEST	Execute diagnostic test
LOAD	Load memory from a file
LCONF	Load data pages configuration
MOVE	Move memory block
NEXT	Single/multi step mode
PM	Display/change paged Data ROM locations
QUIT	Abandon the program
RESET	Reset ST6 core dedications
SAVE	Save memory into a file
SB	Set address breakpoints
SCONF	Save data pages configuration
SEARCH	Search pattern in memory
REM	Put comment in a log file
SET	Set system options
SR	Set register
TRACE	Display traced execution
USE	Execute command file
WR	Display current Working Register set
UPLOAD	Copy ROMulator into HOST

ORDERING INFORMATION

Sales Type	Description
ST6240-EMU	Complete emulator package for ST6240 devices (including dedicated board and ST6-SW software package)
ST6242-EMU	Complete emulator package for ST6242 devices (including dedicated board and ST6-SW software package)
ST6245-EMU	Complete emulator package for ST6245 devices (including dedicated board and ST6-SW software package)
ST626X-EMU	Complete emulator package for ST626XB and ST629X devices (including dedicated board and ST6-SW software package)
ST638X-EMU	Complete emulator package for ST636X/7X/8X devices (including dedicated board and ST6-SW software package)
ST631XX-EMU	Complete emulator package for ST631XX devices (including dedicated board and ST6-SW software package)
ST621X-DBE	Separate dedicated board for ST621XB devices
ST624X-DBE	Separate dedicated board for ST624X devices
ST626X-DBE	Separate dedicated board for ST626X and ST629X devices
ST624X-EMU	Emulator package for ST6240 devices without probes (including dedicated board and ST6-SW software packages)
ST624X-EMU	Emulator package for ST6280 devices without probes (including dedicated board and ST6-SW software packages)
ST6240-PQFP	Probe for ST6240
ST6242-PQFP	Probe for ST6242
ST6245-PQFP	Probe for ST6245

Note : The emulator power supply can be adjusted to 220V or 110V.

EPROM PROGRAMMING BOARDS FOR ST62 MCU FAMILY

HARDWARE FEATURES

- Programs the ST62Exx EPROM and OTP MCUs
- Standalone and PC driven modes
- All ST62Exx packages are supported

SOFTWARE FEATURES

- Menu driven software
- S19 or INTEL hex file formats

DESCRIPTION

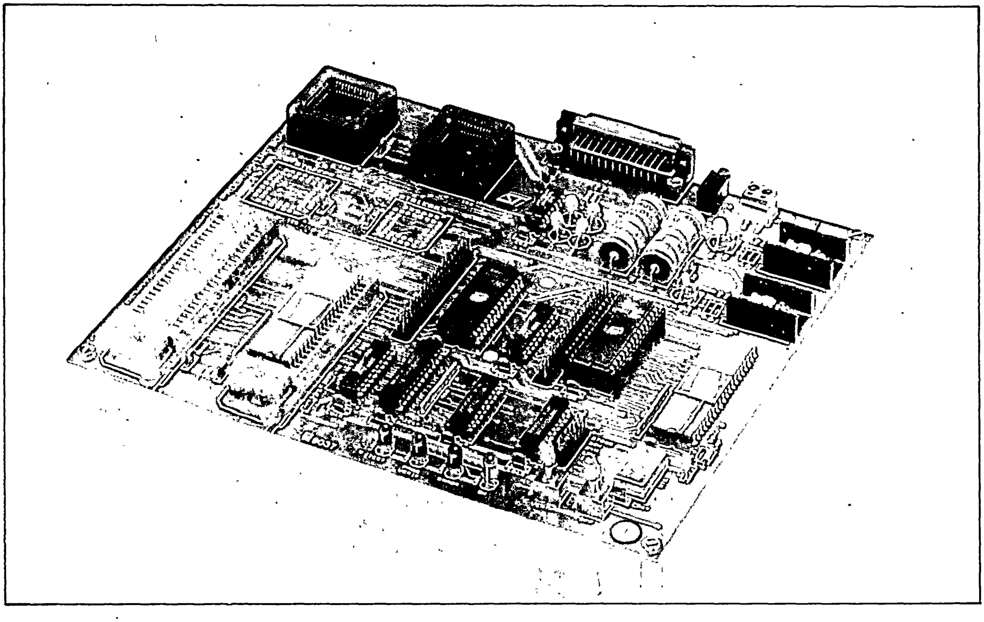
Different programming boards are designed for programming of the various EPROM and OTP devices of the ST62 sub-family. For a particular device, all available packages are supported by the same programming board.

It can run either in standalone or remote mode under control of a DOS compatible PC.

In standalone mode, the microcontrollers can be programmed with a simple key operation directly from a master EPROM device or a master microcontroller. Two colour LEDs indicate the operational pass or fail.

In standalone mode an EPROM memory or a master MCU is plugged into the programming board. The code from the EPROM or the master MCU is read and programmed into the ST62 EPROM or OTP device. Both VERIFY and BLANK CHECK functions are provided.

In remote mode, the programming board is connected to a DOS compatible PC through an RS232 serial channel. Object code in either S19 or INTEL HEX format is read from disk file to program the



ORDERING INFORMATION

Sales Types [1]	Supported Devices	Supported Packages
ST62E1X- EPB/XXX	ST62E10 [2] ST62T10 [2] ST62E15 [2] ST62T15 [2] ST62E20 [2] ST62T20 [2] ST62E25 [2] ST62T25 [2]	DIP20 DIP28 SO20 SO28
ST62E4X-EPB/XXX	ST62E40 ST62E42 ST62E45 ST62T40 ST62T42 ST62T45	QFP52 QFP64 QFP80
ST62E6X-EPB/XXX	ST62E60 ST62E65 ST62T60 ST62T65 ST62E94 ST62T94	DIP20 SO20 DIP28 SO28 DIP20 DIP28
ST62E6X-EPB/XXX	ST6280 ST62E80 ST62T80 ST6285 ST62E85 ST62T85	QFP100 QFP80
ST631XX-EPB/220	ST631XX	DIP40 DIP28

Notes :

1. ST62Exx-EPB/110 : 110V Power Supply
   ST62Exx-EPB/220 : 220V Power Supply
2. Both /HWD and /SWD options are supported

GANG PROGRAMMERS FOR ST62 MCU FAMILY

HARDWARE FEATURES

- Programs simultaneously up to 10 ST62Exx EPROM and OTP MCUs
- Standalone and PC driven modes
- DIP and SO packages supported

SOFTWARE FEATURES

- Menu driven software
- S19 or INTEL hex file format

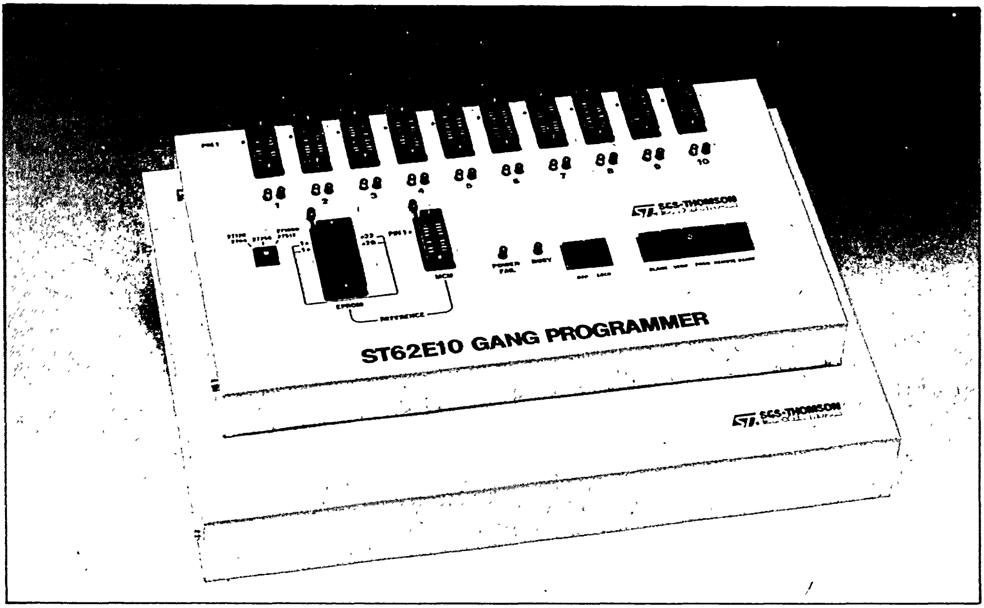
DESCRIPTION

The ST62 gang programmers are designed for programming up to 10 EPROM or OTP devices. It can run either in standalone or remote mode under control of a DOS compatible PC.

In standalone mode, the target ST62 MCUs are programmed with a simple key operation directly from a master EPROM memory or from a master EPROM MCU. Two color LEDs indicate for each target device the operational pass or fail. Both VERIFY and BLANK CHECK functions are provided.

In Remote mode, the gang programmer is connected to a DOS compatible PC through an RS232 serial channel. Object code in either S19 or INTEL HEX format is read from disk files to program the target devices. The menu driven software also offers VERIFY, BLANK CHECK, READ master and other utility functions.

The gang programmer is made up of a two parts, a base unit common to all ST62XX devices and a dedicated package adaptator.



ORDERING INFORMATION

Sales Types	Description	Supported Devices [1]	Supported Packages
ST62E10-GP/DIP	Gang Programmer	ST62E10 ST62T10 ST62E20 ST62T20	DIP20
ST62E10-GP/SO	Gang Programmer	ST62E10 ST62T10 ST62E20 ST62T20	SO20
ST62E15-GP/DIP	Gang Programmer	ST62E15 ST62T15 ST62E25 ST62T25	DIP28
ST62E15-GP/SO	Gang Programmer	ST62E15 ST62T15 ST62E25 ST62T25	SO28
ST62E40-GP/QFP	Gang Programmer	ST62E45 ST62T45	QFP52
ST62E42-GP/QFP	Gang Programmer	ST62E45 ST62T45	QFP52
ST62E45-GP/QFP	Gang Programmer	ST62E45 ST62T45	QFP52
ST62E65-GP/QFP	Gang Programmer	ST62E45 ST62T45	QFP52
ST62E65-GP/QFP	Gang Programmer	ST62E45 ST62T45	QFP52
ST62E80-GP/QFP	Gang Programmer	ST62E80 ST62T80	QFP100
ST62E85-GP/QFP	Gang Programmer	ST62E85 ST62T85	QFP100

Note 1. Both /HWD and /SWD options are supported.

Dedicated Gang Programmers (suffix /GP) are delivered including one dedication module (Suffix /GPA). Alternative device dedication modules are available under the sales types given above, but with /GP replaced by /GPA, allowing the use of another device type or package with the same Programmer.

PROGRAMMING MANUAL

ST62 - ST63

PROGRAMMING MANUAL

INTRODUCTION

This manual deals with the description of the instruction set and addressing modes of ST62,63 microcontroller series. The manual is divided in two main sections. The first one includes, after a general family description, the addressing modes description. The second section includes the detailed description of ST62,63 instruction set. Each instruction is described in detail with the differences between each ST6 series.
ST6 software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability.

Table 1. ST62,63 Series Core Characteristics

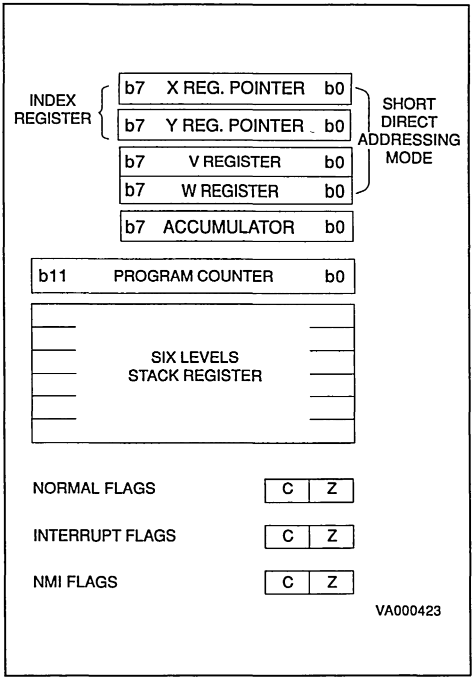
	ST62,63 Series
Stack Levels	6
Interrupt Vectors	5
NMI	YES
Flags Sets	3
Program ROM	2K + 2K• n 20K Max
Data RAM	64 byte • m
Data ROM	64 byte pages in ROM
Carry Flag SUB Instruction	Reset if A > Source
Carry Flag CP Instruction	Set if A < Source

PROGRAMMING MODEL

It is useful at this stage to outline the programming model of the ST62,63 series, by which we mean the available memory spaces, their relation to one another, the interrupt philosophy and so on.

Memory Spaces. The ST6 devices have three different memory spaces: data, program and stack. All addressing modes are memory space specific so there is no need for the user to specify which space is being used as in more complex systems. The stack space, which is used automatically with subroutine and interrupt management for program counter storage, is not accessible to the user.

Figure 1. ST6 Family Programming Model



PROGRAMMING MODEL (Continued)

Figure 2. ST62 Data Space Example

b7 b0	
NOT IMPLEMENTED	000H 03FH
DATA ROM/EPROM WINDOW 64 BYTE	040H 07FH
X REGISTER	080H
Y REGISTER	081H
V REGISTER	082H
W REGISTER	083H
DATA RAM 60 BYTES	084H 0BFH
PORT A DATA REGISTER	0C0H
PORT B DATA REGISTER	0C1H
PORT C DATA REGISTER	0C2H
RESERVED	0C3H
PORT A DIRECTION REGISTER	0C4H
PORT B DIRECTION REGISTER	0C5H
PORT C DIRECTION REGISTER	0C6H
RESERVED	0C7H
INTERRUPT OPTION REGISTER	0C8H
DATA ROM WINDOW REGISTER	0C9H
RESERVED	0CAH 0CBH
PORT A OPTION REGISTER	0CCH
PORT B OPTION REGISTER	0CDH
PORT C OPTION REGISTER	0CEH
RESERVED	0CFH
A/D DATA REGISTER	0D0H
A/D CONTROL REGISTER	0D1H
TIMER PSC REGISTER	0D2H
TIMER DATA REGISTER	0D3H
TIMER TSCR REGISTER	0D4H
RESERVED	0D5H 0D7H
WATCHDOG REGISTER	0D8H
RESERVED	0D9H 0FEH
ACCUMULATOR	0FFH

Figure 3. ST62 Program Memory Example

b7 b0	
NOT IMPLEMENTED	0000H 07FFH
RESERVED	0800H 087FH
USER PROGRAM ROM 1828 BYTES	0880H 0F9FH
RESERVED	0FA0H 0FEFH
INTERRUPT VECTOR #4 A/D INTERRUPT	0FF0H 0FF1H
INTERRUPT VECTOR #3 TIMER INTERRUPT	0FF2H 0FF3H
INTERRUPT VECTOR #2 PORT B & C INTERRUPT	0FF4H 0FF5H
INTERRUPT VECTOR #1 PORT A INTERRUPT	0FF6H 0FF7H
RESERVED	0FF8H 0FFBH
INTERRUPT VECTOR #0 NMI INTERRUPT	0FFCH 0FFDH
USER RESET VECTOR	0FFEH 0FFFH

On EPROM versions there are no reserved areas. These reserved bytes are present on ROM/OTP versions.

Data Memory Space. The following registers in the data space have fixed addresses which are hardware selected so as to decrease access times and reduce addressing requirements and hence program length. The Accumulator is an 8 bit register in location 0FFH. The X, Y, V & W registers have the addresses 80H-83H respectively. These are used for short direct addressing, reducing byte requirements in the program while the first two, X & Y, can also be used as index registers in the indirect addressing mode. These registers are part of the data RAM space. In the ST62 and ST63 for data space ROM a 6 bit (64 bytes addressing) window multiplexing in program ROM is available through a dedicated data ROM banking register.

PROGRAMMING MODEL (Continued)

For data RAM and I/O expansion the lowest 64 bytes of data space (00H-03FH) are paged through a data RAM banking register.

Self-check Interrupt Vector FF8H & FF9H:
jp (self-check interrupt routine)

A jump instruction to the reset and interrupt routines must be written into these locations.

ST62 & ST63 Program Memory Space. The ST62 and ST63 devices can directly address up to 4K bytes (program counter is 12-bit wide). A greater ROM size is obtained by paging the lower 2K of the program ROM through a dedicated banking register located in the data space. The higher 2K of the program ROM can be seen as static and contains the reset, NMI and interrupt vectors at the following fixed locations:

Reset Vector FFEH & FFFH:
jp (reset routine)

NMI Interrupt Vector FFCH & FFDH:
jp (NMI routine)

Non user Vector FFAH & FFBH

Non user Vector FF8H & FF9H

Interrupt #1 Vector FF6H & FF7H jp (Int 1 routine)

Interrupt #2 Vector FF4H & FF5H jp (Int 2 routine)

Interrupt #3 Vector FF2H & FF3H jp (Int 3 routine)

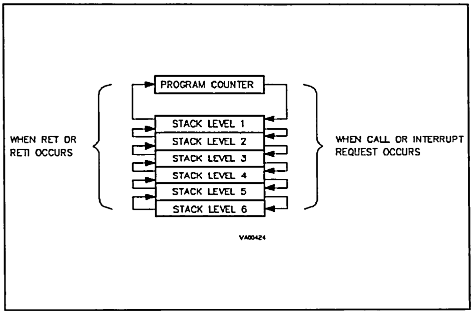
Interrupt #4 Vector FF0H & FF1H jp (Int 4 routine)

Program Counter & Stack Area. The program counter is a twelve bit counter register since it has to cover a direct addressing of 4K byte program memory space. When an interrupt or a subroutine occurs the current PC value is forward "pushed" into a deep LIFO stacking area. On the return from the routine the top (last in) PC value is "popped" out and becomes the current PC value. The ST60/61 series offer a 4-word deep stack for program counter storage during interrupt and sub-routines calls. In the ST62 and ST63 series the stack is 6-word deep.

Status Flags. Three pairs of status flags, each pair consisting of a Zero flag and a Carry flag, are available. In the ST62 and ST63 an additional third set is available. One pair monitors the normal status while the se-cond monitors the state during interrupts; the third flags set monitors the status during Non Maskable interrupt servicing. The switching from one set to another one is automatic as the interrupt requests (or NMI request for ST62,ST63 only) are acknowledged and when the program returns after an interrupt service routine. After reset, NMI set is active, until the first RETI instruction is executed.

ST62 & ST63 Interrupt Description. The ST62 and ST63 devices have 5 user interrupt vectors (plus one vector for testing purposes). Interrupt vector #0 is connected to the not maskable interrupt input of the core. Interrupts from #1 to #4 can be connected to different on-chip and external sources (see individual datasheets for detailed information). All interrupts can be globally disabled through the interrupt option register. After the reset ST62 and ST63 devices are in NMI mode, so no other interrupts can be accepted and the NMI flags set is in use, until the RETI instruction is performed. If an interrupt is detected, a special cycle will be executed, during this cycle the program counter is loaded with the related interrupt vector address. NMI can interrupt other interrupt routines at any time while normal interrupt can't interrupt each other. If more then one interrupt is waiting service, they will be accepted according to their priority. Interrupt #1 has the highest priority while interrupt #4 the lowest. This priority relationship is fixed.

Figure 2. ST62 & ST63 Stack Area

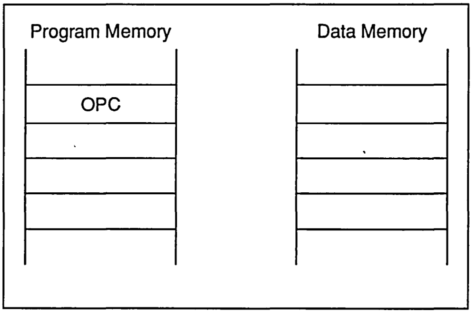


ADDRESSING MODES

The ST6 family gives the user nine addressing modes for access to data locations. Some of these are specifically tailored to particular instruction types or groups while others are designed to reduce program length and operating time by using the hardware facilities such as the X, Y, V & W registers. The data locations can be in either the program memory space or the data memory space when the ST6 is operating due to user software. In addition the ST6 has a stack space for the 12 bit program counter but this is controlled by internal programming and is not accessible by the user. This section will describe all the addressing modes which are provided to the user. The following is the complete list of the ST6 available addressing modes:

- Inherent
- Direct
- Short Direct
- Indirect
- Immediate
- Program Counter Relative
- Extended
- Bit Direct
- Bit Test & Branch

Inherent. For instructions using the inherent addressing mode the opcode contains all the information necessary for execution. All instructions using this mode are **One Byte** instructions.

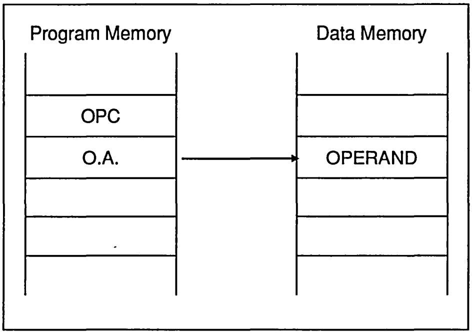


OPC = Opcode

Example:

Instruction	Comments
WAIT	Puts ST6 into the low power WAIT mode
STOP	Puts the ST6 into the lowest power mode
RETI	Returns from interrupt. Pops the PC from the PC stack.Sets the normal set of flags

Direct. In the direct addressing mode the address of the data is given by the program memory byte immediately following the opcode. This data location is in the data memory space. All instructions using this mode are **Two Bytes** instructions, lasting **Four Cycles**.



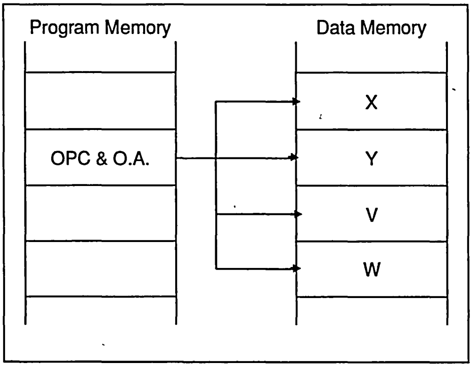
OPC = Opcode
O.A = Operand Address

Example:

Instruction	Comments
LD A,0A3H	Loads the accumulator with the value found in location A3H in the data space.
SUB A,11H	The value found in locations 11H in the data memory is subtracted from the value in the accumulator.

ADDRESSING MODES (Continued)

Short Direct. ST6 core has four fixed location registers in the data space which may be addressed in a short direct manner. The addresses and names of these registers are 80H (X), 81H (Y), 82H (V) and 83H (W). When using this addressing mode the data is in one of these registers and the address is a part of the opcode. All instructions using this mode are **One Byte** instructions, lasting **Four Cycles.**

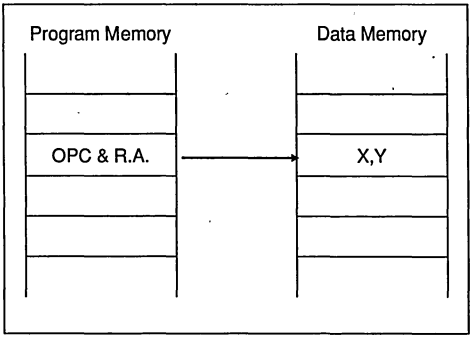


OPC = Opcode
O.A .= Operand Address

Example:

Instruction	Comments
LD A,X	The value of the X register (80H) is loaded into the accumulator.
INC X	The X register is incremented.

Indirect. The indirect mode must use either the X (80H) or Y (81H) register. This register contains the address of the data. The operand is at the data space address pointed to by the content of X or Y registers. All instructions using this mode are **One Byte** instructions, lasting **Four Cycles.**

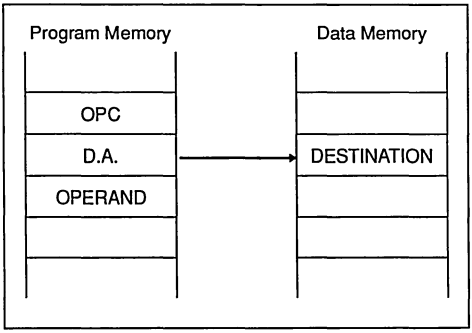


OPC = Opcode
R.A. = Register Address

Example:

Instruction	Comments
LD A,(X)	The value in the registers pointed to by the X register is loaded into the accumulator.
ADD A,(Y)	The value in the register pointed to by the Y register is added to the accumulator value.
INC (Y)	The value in the register pointed to by the Y register is incremented.

Immediate. In the immediate addressing mode the operand is found in the program ROM in a byte which is the last byte of the instruction. This addressing mode can be used for initializing data space registers and supplying constants. Instructions using this mode can be **Two** or **Three Bytes** instructions, lasting **Four Cycles.**



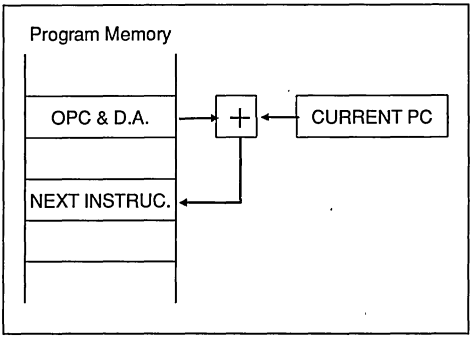
OPC = Opcode
D.A. = Destination Address

ADDRESSING MODES (Continued)

Example:

Instruction	Comments
LDI 34H,DFH	Loads immediate value DFH into data space location 34H.
SUBI A,22H	The immediate value 22H is subtracted from the acc.

Program Counter Relative. This addressing mode is used only with conditional branches within the program. The opcode byte contains the data which is a fixed offset value. This offset is added to the program counter to give the address of the next instruction. The offset can have any value in the range -15 to +16. It is determined by the last five bits of the opcode. All instructions using this mode are **One Byte** Instructions, lasting **Two Cycles**.



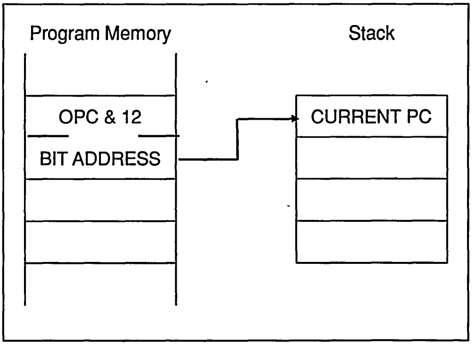
OPC = Opcode
D.A. = Destination Address

Example:

Instruction	Comments
JRC 3	If the carry flag is set then PC = PC+3
JRNZ -7	If the zero flag is not set (i.e the result of a previous instruction is not zero) then PC = PC-7

The relative jump address can be also a label that is automatically handled by the assembler.

Extended. The extended addressing mode is used to make long jumps within the program memory space (4K). The data requires 12 bits and is provided by half of the opcode byte and all of the second byte. All instructions using this mode are **Two Bytes** instructions, lasting **Four Cycles**.



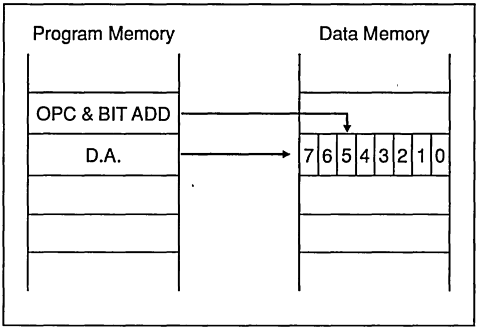
OPC = Opcode

Example:

Instruction	Comments
JP 3FAH	Loads 3FAH into program counter and continues with the instruction at 3FAH.
CALL ROU1	The current PC is pushed onto the stack and PC loaded with the value associated to the ROU1 label

The absolute jump address can be also a label that is automatically handled by the assembler.

Bit Direct. This addressing mode allows the user to set or clear any specified bit in a data memory register. The address of the bit is given in the form: "b,R" where b is the number of the bit and R is the address of the register. The bit is determined by three bits in the opcode and the register address is given by the second byte. All instructions using this mode are **Two Byte** instructions, lasting **Four Cycles**.



OPC = Opcode
D.A. = Destination Address

ADDRESSING MODES (Continued)

Example:

Instruction	**Comments**
SET 4,A	Sets bit 4 of the accumulator to 1.
RES 0,PORT	Clears bit 0 of PORT register

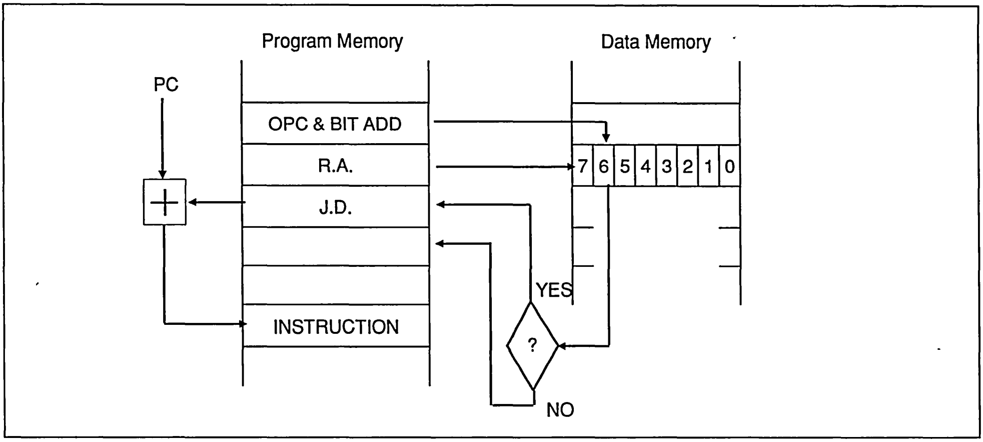
The register address can be associated to a label that is automatically handled by the assembler.

Bit Test & Branch. The bit test addressing mode is used in conditional jump instructions in which the jump depends on the result of a bit test. The opcode specifies the bit to be tested, the byte following the opcode in the register address in data space, and the third byte is the jump displacement, which is in the range -126 to +129. This displacement can be determined using a label, which is converted by the assembler. The state of the tested bit is also copied into the carry flag. All instructions using this mode are **Three Byte** instructions, lasting **Five Cycles.**

Example:

Instruction	**Comments**
JRS 3,PORT,LAB1	If bit three of data memory register associated to PORT label is set then PC=PC+LAB1 (where LAB1 is the jump displacement associated to a label
JRR 0,0AH,-72	If bit 0 of data memory register OAH is reset to 0 then PC=PC-72.

The register address and the jump displacement can be associated to labels that are automatically handled by the assembler.



OPC = Opcode
R.A. = Relative Address
J.D. = Jump Displacement

ST62 & ST63 INSTRUCTION SET

The ST62,63 instructions can be divided functionally into the following seven groups.

- LOAD AND STORE
- ARITHMETIC AND LOGIC
- CONDITIONAL BRANCH
- JUMP AND CALL
- BIT MANIPULATION
- CONTROL
- IMPLIED

The following summary shows the instructions belonging to each group, the number of operands required for each instructions and the number of machine cycles. The flag behaviour is usually the same for both ST62 and ST63. The only difference is present for CP and SUB instructions as specified in the detailed description.

Table 2. Load & Store Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
LD	1	4	Δ	*
LD rr	2	4	Δ	*
LDI A	2	4	Δ	*
LDI	3	4	*	*

Notes: Δ: Affected
*: Not Affected

Table 3. Arithmetic & Logic Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
ADD	2	4	Δ	Δ
ADD (X,Y)	1	4	Δ	D
ADDI	2	4	Δ	D
AND	2	4	Δ	*
AND (X,Y)	1	4	Δ	*
ANDI	2	4	Δ	*
CLR A	2	4	Δ	D
CLR	3	4	*	*
COM	1	4	Δ	D
CP	2	4	Δ	D
CP (X,Y)	1	4	Δ	D
CPI	2	4	Δ	D
DEC	1	4	Δ	*
DEC A/rr	2	4	Δ	*
INC	1	4	Δ	*
INC A/rr	2	4	Δ	*
RLC	1	4	Δ	D
SLA	2	4	Δ	D
SUB	2	4	Δ	D
SUB (X,Y)	1	4	Δ	D
SUBI	2	4	Δ	D

Notes: Δ: Affected
*: Not Affected

Table 4. Conditional Branch Insructions

Instruction	Bytes	Cycles	Flags	
			Z	C
JRC	1	2	*	*
JRNC	1	2	*	*
JRR	3	5	*	Δ
JRS	3	5	*	Δ
JRZ	1	2	*	*
JRNZ	1	2	*	*

Notes: Δ: Affected
*: Not Affected

Table 5. Jump & Call Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
CALL	2	4	*	*
JP	2	4	*	*

Notes: Δ: Affected
*: Not Affected

ST62 & ST63 INSTRUCTION SET (Continued)

Table 6. Bit Manipulation Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
RES	2	4	*	*
SET	2	4	*	*

Notes: Δ: Affected
*: Not Affected

Table 7. Control Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
NOP	1	2	*	*
RET	1	2	*	*
RETI	1	2	Δ	Δ
STOP	1	2	*	*
WAIT	1	2	*	*

Notes: Δ: Affected
*: Not Affected

Table 8. Addressing Modes/Instruction Table

Instruction	Inh	Dir	Sh Dir	Ind	Imm	PCR	Ext	Bit Dir	Bit Test	Flags	
										Z	C
ADD		X	X	X						Δ	Δ
AND		X	X	X						Δ	*
CALL							X			*	*
CLR A		X								Δ	D
CLR		X								*	*
COM	X									Δ	Δ
CP		X		X	X					Δ	Δ
DEC		X	X	X						Δ	*
INC		X	X	X						Δ	*
JP							X			*	*
JRC, JRNC						X				*	*
JRZ, JRNZ						X				*	*
JRR, JRS									X	*	Δ
LD, LDI					X					Δ	*
NOP						X				*	*
RES, SET								X		*	*
RET	X									*	*
RETI	X									Δ	Δ
RLC	X									Δ	Δ
SLA	X									Δ	Δ
STOP, WAIT	X									*	*
SUB		X		X	X					Δ	Δ

Notes:

INH.	Inherent, DIR: Direct, SH.DIR: Short Direct,
IND.	Indirect, IMM: Immediate, PCR: Program Counter Relative
EXT.	Extended, BIT DIR: Bit Direct, BIT TEST.: Bit Test
Δ .	Affected
* .	Not Affected

ST62 & ST63 INSTRUCTION SET (Continued)

Table 9. ST62,63 Opcode Map

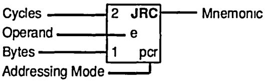
Low Hi	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Low Hi
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b.d.	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b.d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b.d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b d	2 JRZ e 1 pcr	#	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b.d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ST62 & ST63 INSTRUCTION SET (Continued)

Table 10. Instruction Set Cycle-by-Cycle Summary

Instruction	Cycles	Cycles(#)	Address Bus	Data Bus	CPU Activity	Notes
Indirect Addressing Mode						
ADD, AND, CP, DEC, INC, LD, SUB	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Instruction Next Instruction Next Instruction	Decode Opcode Read Operand Address Read Operand Execute Instruction	ROM Data Space not Addressed
ADD, AND, CP, DEC, INC, LD, SUB	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Data Space Rom Add	Opcode (*) Next Instruction Next Instruction Rom Data (#)	Decode Opcode Read Operand Address Read Operand Execute Instruction	ROM Data Space Addressed
Direct Addressing Mode						
ADD, AND, CP, DEC, INC, LD, RES, SET, LSA, SUB, CLR	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 (*) Opcode Address +2	Opcode (*) Operand Address Operand Address(*) Next Instruction	Decode Opcode Address Data Space Read Operand Execute Instruction	ROM Data Space not Addressed
ADD, AND, CP, DEC, INC, LD, RES, SET, LSA, SUB, CLR	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 (*) Data Space Rom Add. (*)	Opcode (*) Operand Address Operand Address(#) Rom Data (#)	Decode Opcode Address Data Space Read Operand Execute Instruction	ROM Data Space Addressed
Immediate Addressing Mode						
ADDI, ANDI, CPI, LDI, SUBI	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1(*) Opcode Address +2(*)	Opcode (*) Immediate Operand Immediate Operand Next Instruction	Decode Opcode Idle Read Operand Execute Instruction	
LDI rr	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +2 Opcode AdDress +3	Opcode (*) Register Address Immediate Operand Next Opcode	Decode Opcode Read Register Address Read Immediate Operand Write Operand To Reg.	ROM Data Space not Addressed
LDI rr	4	1 2 3 4	Opcode Address(*) Opcode Address +1 (*) Opcode Address +2 (#) Data Space Rom Add.	Opcode (*) Register Address Immediate Operand Rom Operand (#)	Decode Opcode Read Register Address Read Immediate Operand Write Operand To Reg.	ROM Data Space Addressed
Short Direct Addressing Mode						
DEC, INC, LD	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Opcode Next Opcode Next Opcode	Decode Opcode Define Data Space Add. Read Operand Execute Instruction	

Notes: *. Valid only at the beginning of the cycle
#. Valid only unti t 18 of the cycle

ST62 & ST63 INSTRUCTION SET (Continued)

Table 10. Instruction Set Cycle-by-Cycle Summary (Continued)

Instruction	Cycles	Cycles(#)	Address Bus	Data Bus	CPU Activity	Notes
Other Instructions						
CALL	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +2(*)	Opcode (*) Subroutine Address Subroutine Address Next Instruction	Decode Opcode Increment Stack Pointer Push Return Address Calculate Subroutine Add.	
COM	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Opcode Next Opcode Next Opcode	Decode Opcode Calculate Acc. Address Read Accumulator Complement Accumulator	
INTERRUPT	1	1	Next opcode address	Next Opcode (*)	Calculate Interrupt Add. Push Return Address Switch Flag Set	Note 1
JP	4	1 2 3 4	Opcode Address(*) opcode Address +1 opcode Address +1 opcode Address +2	Opcode (*) Jump Address Following Instr. Following Instr. (*)	Decode Opcode Idle Read Jump Address Calculate Jump Address	
JRC, JRNC, JRZ, JRNZ	2	1 2	Opcode Address(*) Opcode Address +1	Opcode (*) Following Instr.	Decode Opcode Calculate Offset	
JRR, JRS	5	1 2 3 4 5	Opcode Address(*) Opcode Address +1(*) Opcode Address +2(*) Opcode Address +2(*) Opcode Address +3(*)	Opcode (*) Operand Address (*) Branch Value Branch Value (*) Following Instr.	Decode Opcode Read Operand Test Operand Fetch Branch Value Calculate New Address	ROM Data Space not Addressed
JRR, JRS	5	1 2 3 4 5	Opcode Address(*) Opcode Address +1(*) Data Space Rom Add.(#) Opcode Address +2(*) Data Space Rom Add.(#)	Opcode (*) Operand Address (*) Rom Data (#) Branch Value (*) Rom Data (#)	Decode Opcode Read Operand Test Operand Fetch Branch Value Calculate New Address	ROM Data Space Addressed
RET	2	1 2	Opcode Address(*) Return Address	Opcode (*) Next Opcode	Decode Opcode Pop Return Address	
RETI	2	1 2	Opcode Address(*) Return Address	Opcode (*) Next Opcode	Decode Opcode Pop Return Address Switch Flag Set	
RLC	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Opcode Next Opcode Next Opcode	Decode Opcode Calculate Acc. Address Read Accumulator Shifted	
STOP, WAIT	2	1 2	Opcode Address(*) Opcode Address +1	Opcode (*) Next Opcode	Decode Opcode Stop/Wait the Oscillator	

Notes: *. Valid only at the beginning of the cycle
#. Valid only until t18 of the cycle

1. Add oscillator build up time plus 16 oscillator clocks if a stop instruction has been executed before the interrupt occured

ADD

Addition

Mnemonic: ADD

Function: Addition

Description: The contents of the source byte is added to the accumulator leaving the result in the accumulator. The source register remains unaltered.

Operation: dst ← dst + src

The destination must be the accumulator.

Instruction Format	Opcode (Hex)	Bytes	Cycles	Flags	
ADD dst,src				Z	C
ADD A,A	5F FF	2	4	Δ	Δ
ADD A,X	5F 80	2	4	Δ	D
ADD A,Y	5F 81	2	4	Δ	D
ADD A,V	5F 82	2	4	Δ	D
ADD A,W	5F 83	2	4	Δ	D
ADD A,(X)	47	1	4	Δ	D
ADD A,(Y)	4F	1	4	Δ	D
ADD A,rr	5F rr	2	4	Δ	D

Notes:
rr. 1 Byte dataspace address.
Δ: Z is set if the result is zero. Cleared otherwise.
C is cleared before the operation and than set if there is an overflow from the 8-bit result.

Example: If data space register 22H contains the value 33H and the accumulator holds the value 20H then the instruction,

ADD A,22H

will cause the accumulator to hold 53H (i.e. 33+20).

Addressing Modes: Source: Direct, Indirect

Destination: Accumulator

ADDI

Addition Immediate

Mnemonic: ADDI

Function: Addition Immediate

Description: The immediately addressed data (source) is added to the accumulator leaving the result in the accumulator.

Operation: dst ← dst + src

The destination must be the accumulator.

Instruction Format	Opcode (Hex)	Bytes	Cycles	Flags	
ADDI dst,src				Z	C
ADDI A,nn	57 nn	2	4	Δ	Δ

Notes:
nn. 1 Byte immediate data
Δ: Z is set if result is zero. Cleared otherwise
C is cleared before the operation and than set if there is an overflow from the 8-bit result

Example: If the accumulator holds the value 20H then the instruction,

ADDI A,22H

will cause the accumulator to hold 42H (i.e. 22+20).

Addressing Modes: Source: Immediate
Destination: Accumulator

AND

Logical AND

Mnemonic: AND

Function: Logical AND

Description: This instruction logically ANDs the source register and the accumulator. The result is left in the destination register and the source is unaltered.

Operation: dst ←src AND dst

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
AND dst,src				Z	C
AND A,A	BF FF	2	4	Δ	*
AND A,X	BF 80	2	4	Δ	*
AND A,Y	BF 81	2	4	Δ	*
AND A,V	BF 82	2	4	Δ	*
AND A,W	BF 83	2	4	Δ	*
AND A,(X)	A7	1	4	Δ	*
AND A,(Y)	AF	1	4	Δ	*
AND A,rr	BF rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C is unaffected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If data space register 54H contains the binary value 11110000 and the accumulator contains the binary value 11001100 then the instruction,

AND A,54H

will cause the accumulator to be altered to 11000000.

Addressing Modes: Source: Direct, Indirect.
Destination: Accumulator

ANDI

Logical AND Immediate

Mnemonic: ANDI

Function: Logical AND Immediate

Description: This instruction logically ANDs the immediate data byte and the accumulator. The result is left in the accumulator.

Operation: dst ← src AND dst

The source is immediate data and the destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
ANDI dst,src				Z	C
ANDI A,nn	B7 nn	2	4	Δ	*

Notes:
nn. 1 Byte immediate data
*. C is unaffected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If the accumulator contains the binary value 00001111 then the instruction,

ANDI A,33H

will cause the accumulator to hold the value 00000011.

Addressing Modes: Source: Immediate
Destination: Accumulator

CALL

Call Subroutine

Mnemonic: CALL

Function: Call Subroutine

Description: The CALL instruction is used to call a subroutine. It "pushes" the current contents of the program counter (PC) onto the top of the stack. The specified destination address is then loaded into the PC and points to the first instruction of a procedure. At the end of the procedure a RETurn instruction can be used to return to the original program flow. RET pops the top of the stack back into the PC.
Because the ST6 stack is 4 levels deep (ST60) and 6 levels deep (ST62,ST63), a maximum of four/six calls or interrupts may be nested. If more calls are nested, the PC values stacked latest will be lost. In this case returns will return to the PC values stacked first.

Operation: PC ← dst; Top of stack ← PC

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
CALL dst				Z	C
CALL abc	c0001 ab	2	4	*	*

Notes:
abc. the three half bytes of a twelve bit address, the start location of the subroutine.
*. C,Z not affected

Example: If the current PC is 345H then the instruction,

CALL 8DCH

The current PC 345H is pushed onto the top of the stack and the PC will be loaded with the value 8DCH. The next instruction to be executed will be the instruction at 8DCH, the first instruction of the called subroutine.

Addressing Modes: Extended

CLR

Clear

Mnemonic: CLR

Function: Clear

Description: The destination register is cleared to 00h.

Operation: dst ⟵ 0

Inst. Format	OPCDE (Hex)	Bytes	Cycles	Flags	
CLR dst				Z	C
CLR A	DF FF	2	4	Δ	Δ
CLR X	0D 80 00	3	4	*	*
CLR Y	0D 81 00	3	4	*	*
CLR V	0D 82 00	3	4	*	*
CLR W	0D 83 00	3	4	*	*
CLR rr	0D rr 00	3	4	*	*

Notes:
rr. 1 Byte dataspace address
Δ. Z set, Δ. C reset
*. C,Z unaffected

Example: If data space register 22h contains the value 33h,

CLR 22h

will cause register 22h to hold 00h.

Addressing Modes: Direct

COM

Complement

Mnemonic: COM

Function: Complement

Description: This instruction complements each bit of the accumulator; all bits which are set to 1 are cleared to 0 and vice-versa.

Operation: dst ← NOT dst

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
COM dst				Z	C
COM A	2D	1	4	Δ	Δ

Note :

Δ: Z is set if the result is zero. Cleared otherwise.
C will contain the value of the MSB before the operation.

Example: If the accumulator contains the binary value 10111001 then the instruction

COM A

will cause the accumulator to be changed to 01000110 and the carry flag to be set (since the original MSB was 1).

Addressing Modes: Inherent

CP

Compare

Mnemonic: CP

Function: Compare

Description: This instruction compares the source byte (subtracted from) with the destination byte, which must be the accumulator. The carry and zero flags record the result of this comparison.

Operation: dst - src

The destination must be the accumulator, but it will not be changed.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
CP dst,src				Z	C
CP A,A	3F FF	2	4	Δ	Δ
CP A,X	3F 80	2	4	Δ	Δ
CP A,Y	3F 81	2	4	Δ	Δ
CP A,V	3F 82	2	4	Δ	Δ
CP A,W	3F 83	2	4	Δ	Δ
CP A,(X)	27	1	4	Δ	Δ
CP A,(Y)	2F	1	4	Δ	Δ
CP A,rr	3F rr	2	4	Δ	Δ

Note: rr. 1 Byte dataspace address

ST60 Δ: Z is set if the result is zero. Cleared otherwise.

C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otehrwise.

C is set if Acc < src, cleared if Acc ≥ src.

Example: If the accumulator contains the value 11111000 and the register 34H contains the value 00011100 then the instruction,

CP A,34H

will clear the Zero flag Z and set the Carry flag C, indicating that Acc ≥ src (on ST60)

Addressing Modes: Source: Direct, Indirect

Destination: Accumulator

CPI

Compare Immediate

Mnemonic: CPI

Function: Compare Immediate

Description: This instruction compares the immediately addressed source byte (subtracted from) with the destination byte, which must be the accumulator. The carry and zero flags record the result of this comparison.

Operation: dst-src

The source must be the immediately addressed data and the destination must be the accumulator, that will not be changed.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
CPI dst,src				Z	C
CPI A,nn	37 nn	2	4	Δ	Δ

Note: nn.1 Byte immediate data.

ST60 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc < src, cleared if Acc ≥ src.

Example: If the accumulator contains the value 11111000 then the instruction,

CPI A,00011100B

will clear the Zero flag Z and set the Carry flag C indicating that Acc ≥ src (on ST60).

Addressing Modes: Source: Immediate
Destination: Accumulator

DEC

Decrement

Mnemonica: DEC

Function: Decrement

Description: The destination register's contents are decremented by one.

Operation: dst ← dst-1

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
DEC dst				Z	C
DEC A	FF FF	2	4	Δ	*
DEC X	1D	1	4	Δ	*
DEC Y	5D	1	4	Δ	*
DEC V	9D	1	4	Δ	*
DEC W	DD	1	4	Δ	*
DEC (X)	E7	1	4	Δ	*
DEC (Y)	EF	1	4	Δ	*
DEC rr	FF rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C is unaffected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If the X register contains the value 45H and the data space register 45H contains the value 16H then the instruction,

DEC (X)

will cause data space register 45H to contain the value 15H.

Addressing Modes: Short direct, Direct, Indirect.

INC

Increment

Mnemonic: INC

Function: Increment

Description: The destination register's contents are incremented by one.

Operation: dst ← dst+1

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
INC dst				Z	C
INC A	7F FF	2	4	Δ	*
INC X	15	1	4	Δ	*
INC Y	55	1	4	Δ	*
INC V	95	1	4	Δ	*
INC W	D5	1	4	Δ	*
INC (X)	67	1	4	Δ	*
INC (Y)	6F	1	4	Δ	*
INC rr	7F rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C is unaffected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If the X register contains the value 45H and the data space register 45H contains the value 16H then the instruction

INC (X)

will cause data space register 45H to contain the value 17H.

Addressing Modes: Short direct, Direct, Indirect.

JP

Jump

Mnemonic: JP

Function: Jump (Unconditional)

Description: The JP instruction replaces the PC value with a twelve bit value thus causing a simple jump to another location in the program memory. The previous PC value is lost, not stacked.

Operation: PC ← dst

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
JP dst				**Z**	**C**
JP abc	c1001 ab	2	4	*	*

Notes:
abc. the three half bytes of a twelve bit address.
*. C,Z not affected

Example: The instruction,

JP 5CDH

will cause the PC to be loaded with 5CDH and the program will continue from that location.

Addressing Modes: Extended

JRC

Jump Relative on Carry Flag

Mnemonic: JRC

Function: Jump Relative on Carry Flag

Description: This instruction causes the carry (C) flag to be tested and if this flag is set then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The displacemente is of five bits. If C=0 than the next instruction is executed.

Operation: If C=1, PC ← PC + e

where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRC e	e110	1	2	*	*

Notes:
e. 5 bit displacement in the range –15 to + 16
*. C,Z not affected

Example: If the carry flag is set then the instruction,

JRC + 8

will cause a branch forward to PC+8. The user can use labels as indentifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

JRNC

Jump Relative on Non Carry Flag

Mnemonic: JRNC

Function: Jump Relative on Non Carry Flag

Description: This instruction causes the carry (C) flag to be tested and if this flag is cleared to zero then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The dispacement is of five bits. If C=1 then the next instruction is executed.

Operation: If C=0, PC ← PC + e

where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRNC e	e010	1	2	*	*

Notes:
e: 5 bit displacement in the range -15 to +16
*: C,Z not affected

Example: If the carry flag is cleared then the instruction,

JRNC -5

will cause a branch backward to PC-5. The user can use labels as identifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

JRNZ

Jump Relative on Non Zero Flag

Mnemonic: JRNZ

Function: Jump Relative on Non Zero Flag

Description: This instruction causes the zero (Z) flag to be tested and if this flag is cleared to zero then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The displacement is of five bits. If Z=1 then the next instruction is executed.

Operation: If Z=0, PC ← PC + e

where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRNZ e	e000	1	2	*	*

Notes:
e. 5 bit displacement in the range -15 to +16.
*. C,Z not affected

Example: If the zero flag is cleared then the instruction,

JRNZ -5

will cause a branch backward to PC-5. The user can use labels as identifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

JRR

Jump Relative if Reset

Mnemonic: JRR

Function: Jump Relative if RESET

Description: This instruction causes a specified bit in a given dataspace register to be tested. If this bit is reset (=0) then the PC value will be changed and a relative jump will be performed within the program. The relative jump range is -126 to +129. If the tested bit is not reset then the next instruction is executed.

Operation: If bit=0, PC ← PC + ee

where ee= 8 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRR b,rr,ee	b00011 rr ee	3	5	*	Δ

Notes:
b. 3 bit-address
rr. 1 Byte dataspace address
ee. 8 bit displacement in the range -126 to +129

*. Z is not affected
Δ. The tested bit is shifted into carry.

Example: If bit 4 of dataspace register 70H is reset and the PC=110 then the instruction,

JRR 4, 70H, -20

will cause the PC to be changed to 90 (110-20) and the instruction starting at that address in the program memory to be the next instruction executed.

The user is advised to use labels for conditional jumps. The relative jump will be calculated by the assembler. The jump must be in the range -126 to +129.

Addressing Modes: Bit Test

JRS

Jump Relative if Set

Mnemonic: JRS

Function: Jump Relative if set

Description: This instruction causes a specified bit in a given dataspace register to be tested. If this bit is set (=1) then the PC value will be changed and a relative jump will be performed within the program. The relative jump range is -126 to +129. If the tested bit is not set then the next instruction is executed.

Operation: If bit=1, PC ← PC + ee

where ee= 8 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRS b,rr,ee	b10011 rr ee	3	5	*	Δ

Notes:
b. 3 bit-address
rr. 1 Byte dataspace address
ee. 8 bit displacement in the range -126 to +129

*. Z is not affected
Δ. The tested bit is shifted into carry.

Example: If bit 7 of dataspace register AFH is set and the PC=123 then the instruction,

JRS 7,AFH,+25

will cause the PC to be changed to 148 (123+25) and the instruction starting at that address in the program memory to be the next instruction executed.

The user is advised to use labels for conditional jumps. The relative jump will be calculated by the assembler. The jump must be in the range -126 to +129.

Addressing Modes: Bit Test

JRZ

Jump Relative on Zero Flag

Mnemonic: JRZ

Function: Jump Relative on Zero Flag

Description: This instruction causes the zero (Z) flag to be tested and if this flag is set to one then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The displacement is of five bits.
If Z=0 then next instruction is executed.

Operation: If Z=1, PC ← PC + e

where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRZ e	e100	1	2	*	*

Notes:
e. 5 bit displacement in the range -15 to +16.
*. C,Z not affected

Example: If the zero flag is set then the instruction,

JRZ +8

will cause a branch forward to PC+8. The user can use labels as identifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

LD

Load

Mnemonic: LD

Function: Load

Description: The contents of the source register are loaded into the destination register. The source register remains unaltered and the previous contents of the destination register are lost.

Operation: dst ← src

Either the source or the destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
LD dst,src				Z	C
LD A,X	35	1	4	Δ	*
LD A,Y	75	1	4	Δ	*
LD A,V	B5	1	4	Δ	*
LD A,W	F5	1	4	Δ	*
LD X,A	3D	1	4	Δ	*
LD Y,A	7D	1	4	Δ	*
LD V,A	BD	1	4	Δ	*
LD W,A	FD	1	4	Δ	*
LD A,(X)	07	1	4	Δ	*
LD (X), A	87	1	4	Δ	*
LD A,(Y)	0F	1	4	Δ	*
LD (Y),A	8F	1	4	Δ	*
LD A,rr	1F rr	2	4	Δ	*
LD rr,A	9F rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C not affected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If data space register 34H contains the value 45H then the instruction;

LD A,34H

will cause the accumulator to be loaded with the value 45H. Register 34H will keep the value 45H.

Addressing Modes: Source: Direct, Short Direct, Indirect

Destination: Direct, Short Direct, Indirect

LDI

Load Immediate

Mnemonic: LDI

Function: Load Immediate

Description: The immediately addressed data (source) is loaded into the destination data space register.

Operation: dst ← src

The source is always an immediate data while the destination can be the accumulator, one of the X,Y,V,W registers or one of the available data space registers.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
LDI dst,src				Z	C
LDI A,nn	17 nn	2	4	Δ	*
LDI X,nn	0D 80 nn	3	4	*	*
LDI Y,nn	0D 81 nn	3	4	*	*
LDI V,nn	0D 82 nn	3	4	*	*
LDI W,nn	0D 83 nn	3	4	*	*
LDI rr,nn	0D rr nn	3	4	*	*

Notes:
rr. 1 Byte dataspace address
nn. 1 Byte immediate value

*. Z, C not affected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: The instruction

LDI 34H,45H

will cause the value 45H to be loaded into data register at location 34H.

Addressing Modes: Source: Immediate
Destination: Direct

NOP

No Operation

Mnemonic: NOP

Function: No Operation

Description: No action is performed by this instruction. It is typically used for timing delay.

Operation: No Operation

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
NOP	04	1	2	*	*

Note: *. C,Z not affected

Addressing Modes: Program Counter Relative

RES

Reset Bit

Mnemonic: RES

Function: Reset Bit

Description: The RESET instruction is used to reset a specified bit in a given register in the data space.

Operation: dst (n) $\leftarrow 0, 0 \leq n \leq 7$

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
RES bit,dst				Z	C
RES b,A	b01011 FF	2	4	*	*
RES b,rr	b01011 rr	2	4	*	*

Notes:
b. 3 bit-address
rr. 1 Byte dataspace address
*. C,Z not affected

Example: If register 23H of the dataspace contains 11111111 then the instruction,

RES 4,23H

will cause register 23H to hold 11101111.

Addressing Modes: Bit Direct

RET

Return from Subroutine

Mnemonic: RET

Function: Return From Subroutine

Description: This instruction is normally used at the end of a subroutine to return to the previously executed procedure. The previously stacked program counter (stacked during CALL) is popped back from the stack. The next statement executed is that addressed by the new contents of the PC. If the stack had already reached its highest level (no more PC stacked) before the RET is executed, program execution will be continued at the next instruction after the RET.

Operation: PC ← Stacked PC

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
RET	CD	1	2	*	*

Note: *. C,Z not affected

Example: If the current PC value is 456H and the PC value at the top of the stack is 3DFH then the instruction,

RET

will cause the PC value 456H to be lost and the current PC value to be 3DFH.

Addressing Modes: Inherent

RETI

Return from Interrupt

Mnemonic: RETI

Function: Return from Interrupt

Description: This instruction marks the end of the interrupt service routine and returns the ST60/62/63 to the state it was in before the interrupt. It "pops" the top (last in) PC value from the stack into the current PC. This instruction also causes the ST60/62/63 to switch from the interrupt flags to the normal flags. The RETI instruction also applies to the end of NMI routine for ST62/63 devices; in this case the instruction causes the switch from NMI flags to normal flags (if NMI was acknowledged inside a normal routine) or to standard interrupt flags (if NMI was acknowledged inside a standard interrupt service routine).

In addition the RETI instruction also clears the interrupt mask (also NMI mask for ST62/63) which was set when the interrupt occurred. If the stack had already reached its highest level (no more PC stacked) before the RETI is executed, program execution will be continued with the next instruction after the RETI. Because the ST60 is in interrupt mode after reset (NMI mode for ST62/63), RETI has to be executed to switch to normal flags and enable interrupts at the end of the starting routine. If no call was executed during the starting routine, program execution will continue with the instruction after the RETI (supposed no interrupt is active).

Operation: Actual Flags ← Normal Flags (1)

PC ← Stacked PC

IM ← 0

(1) Standard Interrupt flags if NMI was acknowledged inside a standard interrupt service (ST62/63 only).

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
RETI	4D	1	2	Δ	Δ

Note: Δ C,Z normal flag will be used from now on.

Example: If the current PC value is 456H and the PC value at the top of the stack is 3DFH then the instruction

RETI

will cause the value 456H to be lost and the current PC value to be 3DFH.
The ST6 will switch from interrupt flags to normal flags and the interrupt mask is cleared.

Addressing Modes: Inherent

RLC

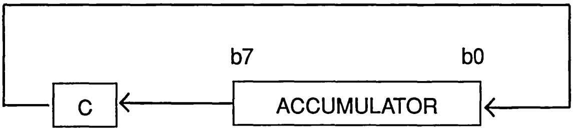
Rotate Left Through Carry

Mnemonic: RLC

Function: Rotate Left through Carry

Description: This instruction moves each bit in the accumulator one place to the left (i.e. towards the MSBit. The MSBit (bit 7) is moved into the carry flag and the carry flag is moved into the LSBit (bit0) of the accumulator.

Operation:



dst(0) ← C

C ←dst(7)

dst(n+1) ← dst(n), 0 ≤ n ≤ 6

This instruction can only be performed on the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
RLC A	AD	1	4	Δ	Δ

Note : Δ: Z is set if the result is zero. Cleared otherwise.
C will contain the value of the MSB before the operation.

Example: If the accumulator contains the binary value 10001001 and the carry flag is set to 0 then the instruction,

RLC A

will cause the accumulator to have the binary value 00010010 and the carry flag to be set to 1.

Addressing Modes: Inherent

SET

Set Bit

Mnemonic: SET

Function: Set Bit

Description: The SET instruction is used to set a specified bit in a given register in the data space.

Operation: dst (n) ← 1, $0 \leq n \leq 7$

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
SET bit,dst				Z	C
SET b,A	b11011 FF	2	4	*	*
SET b,rr	b11011 rr	2	4	*	*

Notes:
b. 3 bit-address
rr. 1 Byte dataspace address
*. C,Z not affected

Example: If register 23H of the dataspace contains 00000000 then the instruction,

SET 4,23H

will cause register 23H to hold 00010000.

Addressing Modes: Bit Direct

SLA

Shift Left Accumulator

Mnemonic: SLA

Function: Shift Left Accumulator

Description: This instruction implements an addition of the accumulator to itself (i.e a doubling of the accumulator) causing an arithmetic left shift of the value in the register.

Operation: ADD A,FFH

This instruction can only be performed on the accumulator.

Inst. Format	OPCPDE (Hex)	Bytes	Cycles	Flags	
				Z	C
SLA A	5F FF	2	4	Δ	Δ

Note: Δ: Z is set if the result is zero. Cleared otherwise.
C will contain the value of the MSB before the operation.

Example: If the accumulator contains the binary value 11001101 then the instruction,

SLA A

will cause the accumulator to have the binary value 10011010 and the carry flag to be set to 1.

Addressing Modes: Inherent

STOP

Stop Operation

Mnemonic: STOP

Function: Stop operation

Description: This instruction is used for putting the ST60/62/63 into a stand-by mode in which the power consumption is reduced to a minimum. All the on-chip peripherals and oscillator are stopped (for some peripherals,A/D for example, it is necessary to individually turn-off the macrocell before entering the STOP instruction). To restart the processor an external interrupt or a reset is needed.

Operation: Stop Processor

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
STOP	6D	1	2	*	*

Note : *: C,Z not affected

Addressing Mode: Inherent

SUB

Subtraction

Mnemonic: SUB

Function: Subtraction

Description: This instruction subtracts the source value from the destination value.

Operation: dst ←dst-src

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
.SUB dst,src				Z	C
SUB A,A	DF FF	2	4	Δ	Δ
SUB A,X	DF 80	2	4	Δ	Δ
SUB A,Y	DF 81	2	4	Δ	Δ
SUB A,V	DF 82	2	4	Δ	Δ
SUB A,W	DF 83	2	4	Δ	Δ
SUB A,(X)	C7	1	4	Δ	Δ
SUB A,(Y)	CF	1	4	Δ	Δ
SUB A,rr	DF rr	2	4	Δ	Δ

Note: rr.1 Byte dataspace address

ST60 Δ: Z is set if the result is zero. Cleared otherwise.

C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otherwise.

C is set if Acc < src, cleared if Acc ≥ src.

Example: If the Y register contains the value 23H, dataspace register 23H contains the value 53H and the accumulator contains the value 78H then the instruction,

SUB A,(Y)

will cause the accumulator to hold the value 25H (i.e. 78-53). The zero flag is cleared and the carry flag is set (on ST60), indicating that result is > 0.

Addressing Modes: Source: Indirect,Direct

Destination: Accumulator

SUBI

Subtraction Immediate

Mnemonic: SUBI

Function: Subtraction Immediate

Description: This instruction causes the immediately addressed source data to be subtracted from the accumulator.

Operation: dst ← dst - src

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
SUBI dst,src				Z	C
SUBI A,nn	D7 nn	2	4	Δ	Δ

Note: nn. 1 Byte of immediate data

ST60 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc < src, cleared if Acc ≥ src.

Example: If the accumulator contains the value 56H then the instruction,

SUBI A,25

will cause the accumulator to contain the value 31H. The zero flag is cleared and the carry flag is set (on ST60), indicating that the result is > 0.

Addressing Modes: Source: Immediate
Destination: Accumulator

WAIT

Wait Processor

Mnemonic: WAIT

Function: Wait Processor

Description: This instruction is used for putting the ST60/62/63 into a stand-by mode in which the power consumption is reduced to a minimum. Instruction execution is stopped, but the oscillator and some on-chip peripherals continue to work. To restart the processor an interrupt from an active on-chip peripheral (eg. timer), an external interrupt or reset is needed. For on-chip peripherals active during wait, see ST60/62/63 data sheets.

Operation: Put ST6 in stand-by mode

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
WAIT	ED	1	2	*	*

Note : *. C,Z not affected

Addressing Modes: Inherent

EUROPE

DENMARK

2730 HERLEV
Herlev Torv, 4
Tel. (45-44) 94.85.33
Telex: 35411
Telefax: (45-44) 948694

FINLAND

LOHJA SF-08150
Ratakatu, 26
Tel. (358-12) 155.11
Telefax. (358-12) 155.66

FRANCE

94253 GENTILLY Cedex
7 - avenue Gallieni - BP. 93
Tel.: (33-1) 47.40.75.75
Telex: 632570 STMHQ
Telefax: (33-1) 47.40.79.10

67000 STRASBOURG
20, Place des Halles
Tel. (33-88) 75.50.66
Telefax: (33-88) 22.29.32

GERMANY

85630 GRASBRUNN
Bretonischer Ring 4
Postfach 1122
Tel.: (49-89) 460060
Telefax: (49-89) 4605454
Teletex: 897107=STDISTR

60327 FRANKFURT
Gutleutstrasse 322
Tel. (49-69) 237492-3
Telefax: (49-69) 231957
Teletex: 6997689=STVBF

30695 HANNOVER 51
Rotenburger Strasse 28A
Tel. (49-511) 615960-3
Teletex: 5118418 CSFBEH
Telefax: (49-511) 6151243

90491 NÜRNBERG 20
Erlenstegenstrasse, 72
Tel.: (49-911) 59893-0
Telefax: (49-911) 5980701

70499 STUTTGART 31
Mittlerer Pfad 2-4
Tel. (49-711) 13968-0
Telefax: (49-711) 8661427

ITALY

20090 ASSAGO (MI)
V.le Milanofiori - Strada 4 - Palazzo A/4/A
Tel. (39-2) 57546.1 (10 linee)
Telex: 330131 - 330141 SGSAGR
Telefax: (39-2) 8250449

40033 CASALECCHIO DI RENO (BO)
Via R. Fucini, 12
Tel. (39-51) 591914
Telex: 512442
Telefax: (39-51) 591305

00161 ROMA
Via A. Torlonia, 15
Tel. (39-6) 8553960
Telex: 620653 SGSATE I
Telefax: (39-6) 8444474

NETHERLANDS

5652 AR EINDHOVEN
Meerenakkerweg 1
Tel.: (31-40) 550015
Telefax: (31-40) 528835

SPAIN

08004 BARCELONA
Calle Gran Via Corts Catalanes, 322
6th Floor, 2th Door
Tel. (34-3) 4251800
Telefax: (34-3) 4253674

28027 MADRID
Calle Albacete, 5
Tel. (34-1) 4051615
Telex: 46033 TCCEE
Telefax: (34-1) 4031134

SWEDEN

S-16421 KISTA
Borgarfjordsgatan, 13 - Box 1094
Tel.: (46-8) 7936920
Telex: 12078 THSWS
Telefax: (46-8) 7504950

SWITZERLAND

1218 GRAND-SACONNEX (GENEVA)
Chemin Francois-Lehmann, 18/A
Tel. (41-22) 9292929
Telex: 415493 STM CH
Telefax: (41-22) 9292900

UNITED KINGDOM and EIRE

MARLOW, BUCKS
Planar House, Parkway
Globe Park
Tel.: (44-628) 890800
Telex: 847458
Telefax: (44-628) 890391

SALES OFFICES

AMERICAS

BRAZIL

05413 SÃO PAULO
R. Henrique Schaumann 286-CJ33
Tel.: (55-11) 883-5455
Telex: (391)11-37988 "UMBR BR"
Telefax : (55-11) 282-2367

CANADA

NEPEAN ONTARIO K2H 9C4
301 Moodie Drive Suite 307
Tel.: (613) 829-9944
Telefax: (613) 829-8998

U.S.A.

NORTH & SOUTH AMERICAN
MARKETING HEADQUARTERS
55 Old Bedford Road
Lincoln, MA 01773
Tel.: (617) 259-0300
Telefax: (617) 259-4421

ALABAMA
Huntsville - Tel.: (205) 533-5995
Fax: (205) 533-9320

ARIZONA
Phoenix - Tel.: (602) 867-6217
Fax: (602) 867-6200

CALIFORNIA
Santa Ana - Tel.: (714) 957-6018
Fax: (714) 957-3281
San Jose - Tel : (408) 452-8585
Fax: (452) 1549

COLORADO
Boulder - Tel.: (303) 449-9000
Fax: (303) 449-9505

FLORIDA
Boca Raton - Tel.: (407) 997-7233
Fax: (407) 997-7554

GEORGIA
Norcross - Tel.: (404) 242-7444
Fax: (404) 368-9439

ILLINOIS
Schaumburg - Tel : (708) 517-1890
Fax: (708) 517-1899

INDIANA
Kokomo - Tel.: (317) 455-3500
Fax: (317) 455-3400
Indianapolis - Tel.: (317) 575-5520
Fax: (317) 575-8211

MICHIGAN
Livonia - Tel.: (313) 953-1700
Fax: (313) 462-4071

MINNESOTA
Bloomington - Tel.: (612) 944-0098
Fax: (612) 944-0133

NORTH CAROLINA
Cary - Tel.: (919) 469-1311
Fax: (919) 469-4515

NEW JERSEY
Voorhees - Tel.: (609) 772-6222
Fax: (609) 772-6037

NEW YORK
Poughkeepsie - Tel.: (914) 454-8813
Fax: (914) 454-1320

OREGON
Lake Oswego - Tel.: (503) 635-7650

TENNESSEE
Knoxville - Tel.: (615) 524-6239

TEXAS
Austin - Tel.· (512) 502-3020
Fax: (512) 346-6260
Carrollton - Tel.: (214) 466-8844
Fax: (214) 466-8130
Houston - Tel.: (713) 376-9936
Fax: (713) 376-9948

FOR RF AND MICROWAVE
POWER TRANSISTORS CONTACT
THE FOLLOWING REGIONAL
OFFICE IN THE U.S.A.

PENNSYLVANIA
Montgomeryville - Tel : (215) 361-6400
Fax: (215) 361-1293

ASIA / PACIFIC

AUSTRALIA

NSW 2220 HURTSVILLE
Suite 3, Level 7, Otis House
43 Bridge Street
Tel. (61-2) 5803811
Telefax: (61-2) 5806440

VICTORIA 3168 NOTTING HILL
11 Business Park Drive
Tel. (61-3) 558 9993
Telefax: (61-3) 558 9997

CHINA

SHANGHAI 200233
1008-10 Astronartics Building
222 Cao Xi Road
Tel. (021) 472-5415
Telefax: (021) 472-6814

SHENZHEN
Flat J, 22/F
38 Dungmen Nanlu
Postal N. 518-001
Tel. (0755) 228-0035
Telefax: (0755) 228-0035

HONG KONG

WANCHAI
22nd Floor - Hopewell centre
183 Queen's Road East
Tel. (852) 8615788
Telex: 60955 ESGIES HX
Telefax: (852) 8656589

INDIA

NEW DELHI 110019
Liaison Office
3rd Floor, F-Block
International Trade Tower
Nehru Place
Tel. (91-11) 644-5928/647-9415
Telex: 031-70193 STMI IN
Telefax: (91-11) 6443054

MALAYSIA

SELANGOR, PETALING JAYA 46200
Unit BM-10
PJ Industrial Park
Jalan Kemajuan 12/18
Tel.: (03) 758 1189
Telefax: (03) 758 1179

PULAU PINANG 10400
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel. (04) 379735
Telefax (04) 379816

KOREA

SEOUL 121
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel. (82-2) 553-0399
Telex: SGSKOR K29998
Telefax: (82-2) 552-1051

TAE-GU
18th Floor Youngnam Tower
111 Shinchun-3 Dong
Tong-Ku
Tel. (053) 756-9583
Telefax: (053) 756-4463

SINGAPORE

SINGAPORE 2056
28 Ang Mo Kio - Industrial Park 2
Tel. (65) 4821411
Telex: RS 55201 ESGIES
Telefax· (65) 4820240

TAIWAN

TAIPEI
11th Floor
105, Section 2 Tun Hua South Road
Tel. (886-2) 755-4111
Telex: 10310 ESGIE TW
Telefax: (886-2) 755-4008

THAILAND

BANGKOK 10110
54 Asoke Road
Sukhumvit 21
Tel : (662) 260 7870
Telefax: (662) 260 7871

JAPAN

TOKYO 108
Nisseki - Takanawa Bld. 4F
2-18-10 Takanawa
Minato-Ku
Tel. (81-3) 3280-4121
Telefax: (81-3) 3280-4131

OSAKA 532
Shin-Osaka Dai 2 Mori Bldg.
3-5-36 Miyahara Yodogawa-Ku
Tel. (81-0) 6397-4130
Telefax: (81-0) 6397-4131

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

SGS-THOMSON Microelectronics GROUP OF COMPANIES
Australia - Brazil - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands -
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

Recycled and chlorine free paper

Recycled and chlorine free paper

ORDER CODE: DBST6ST/4

Eurodis Texim Electronics B.V.
Postbus 172
7480 AD Haaksbergen
Tel. : 05427 33333
Fax : 05427 33888