MEMORY PRODUCTS

SGS-THOMSON MICROELECTRONICS

MEMORY PRODUCTS

DATABOOK

2nd EDITION

DM 25,--

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RYSTON Electronics

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ELECTRONICS
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Na hřebenech II 1062
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SGS-THOMSON
MICROELECTRONICS

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DATABOOK

2nd EDITION

AUGUST 1992

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

SGS-THOMSON Microelectronics manufactures an extensive range of memory products which satisfy the needs of a diverse range of applications. They include,

Non-volatile memories: EPROM, OTP ROM, FLASH MEMORIES and EEPROM.

Static RAMs: Fast SRAM, Cache TAGRAM and Burst SRAM, BiPORT FIFOs.

Zeropower, Timekeeper and Processor Manager specialty memories.

This databook provides comprehensive, technical information on each family of memory products to aid selection for a defined use.

EPROMs (UV eraseable Electrically Programmable Read Only Memories). This family includes EPROMs which can be erased by exposure to Ultra Violet light through a quartz window in the package. Data is provided on EPROMs in two technologies, CMOS and NMOS, and in densities from 16K bits up to 16Megbits. Memory access times for standard products are as fast as 80ns. Programming times have been reduced through the use of specially designed 'margin-mode verify' circuits and new PRESTO programming algorithms. For portable equipment some sizes of EPROM are specified for operation in read mode down to 3V supply.

OTP ROMs (One Time Programmable Read Only Memories). These devices are similar to EPROMs but are packaged in plastic packages, both Dual In Line and surface mounting types. They are not eraseable, but may be programmed one time only using the same programming technique as for EPROMs.

FLASH MEMORIES. (Electrically programmable and Eraseable Memories). The FLASH MEMORY provides a new flexibility for the system designer by implementing both electrical programming, like an EPROM, and electrical erasure. The erasure is either the entire chip or for certain devices by blocks of the memory. This gives the devices additional functionality as they can be erased and reprogrammed in the circuit board for applications where there is a requirement to change the contents of the non-volatile memory. The manufacturing process for FLASH MEMORIES is very similar to that of EPROMs thus ensuring a similar evolution of density, performance and reliability.

EEPROMs. (Electrically Eraseable and Programmable Read Only Memories). Different from the FLASH MEMORY, the EEPROM may be erased and written byte-by-byte. Two types of EEPROM are included: serial access with buses compatible with I^2C or MICROWIRE® standards, and parallel access devices. EEPROMs are widely used for storing equipment parameters or data configurations. The special CMOS technology used by SGS-THOMSON allows a guarantee of over 1,000,000 erase/write cycle endurance and over 10 years data retention. Devices operate down to 2.5V.

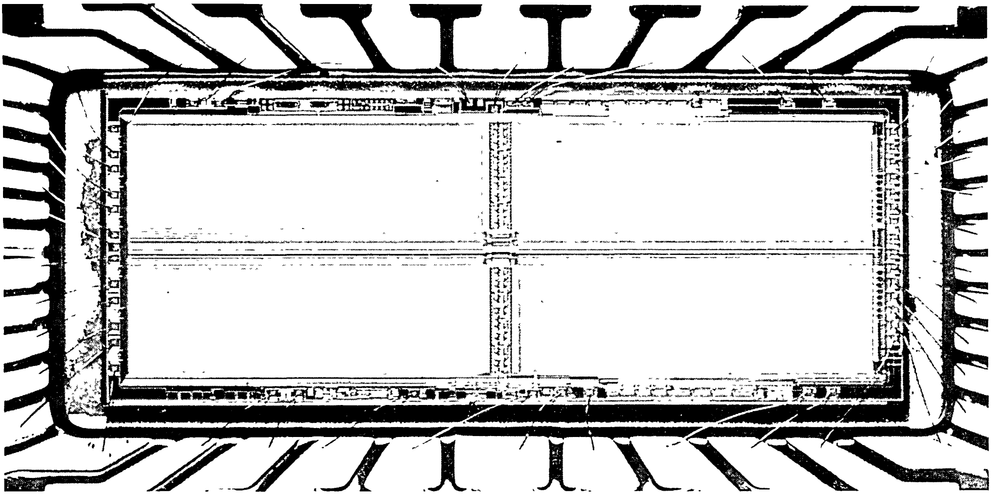
Fast SRAM. Using a new Advanced CMOS process the Fast SRAM products offer access times down to 10ns and are thus suitable for use in high speed applications such as computer cache memory systems. Product sizes range from 64K up to 1Megabit. The memories use a technique known as VBO (Variable Bit Organisation) which establishes the organisation (x1, x4 or x8) at the final metal mask level: this enables a rapid reaction to customer orders for different organisations but still maintains a short production time for the whole family.

Cache TAGRAM™. Computer Cache systems are made using a combination of a memory to store the cache data addresses (the tagram) and the cache data store (a fast SRAM or burst SRAM). The Cache TAGRAM family includes both standard TAGRAMs and the SnoopTAG for multiprocessor/dual bus applications. The burst SRAM (BRAM) products are 32K x 9 fast SRAMs with internal address counters and are designed for use with popular microprocessors.

BiPORT™ FIFOs. The BiPORT FIFO family is a series of FIFO memories based on SRAM technology, with built in address registers for read and write pointers. Sizes vary from 512 bits up to 8K bits. The architecture allows both depth and width exapnsion.

ZEROPOWER™ and **TIMEKEEPER™**. This range of products satisfies a very important sector of applications: they provide fast Read/Write non-volatile memory for use as back-up storage, for example during power down. The basic range of Zeropower products consists of an ultra low power SRAM, with integrated supply voltage detector and a switch-over to battery sustained operation. The packaging includes an integrated lithium battery which has the capacity to maintain memory contents for 10 - 11 years. Timekeeper products include a real time clock which is also powered by the back-up battery during power down.

SGS-THOMSON has an extensive program of both process R & D and product development which results in many new product updates and introductions every year. Please contact your nearest sales office to learn about new products that have been introduced since this data book was published.



The 16 Megabit EPROM developed in 0,6 micron CMOS Technology

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CMOS UV EPROM and OTP ROM

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
64K	M27C64A-15F1	8K x 8	150	5V ± 10%	30mA / 100µA	High Speed	0 to 70	FDIP28W
	M27C64A-20F1	8K x 8	200	5V ± 10%	30mA / 100µA	High Speed	0 to 70	FDIP28W
	TS27C64A-20CQ	8K x 8	200	5V ± 10%	30mA / 100µA	HIgh Speed	0 to 70	FDIP28W
	M27C64A-25F1	8K x 8	250	5V ± 10%	30mA / 100µA	High Speed	0 to 70	FDIP28W
	TS27C64A-25CQ	8K x 8	250	5V ± 10%	30mA / 100µA	HIgh Speed	0 to 70	FDIP28W
	TS27C64A-30CQ	8K x 8	300	5V ± 10%	30mA / 100µA	HIgh Speed	0 to 70	FDIP28W
	M27C64A-20F6	8K x 8	200	5V ± 10%	30mA / 100µA	High Speed	–40 to 85	FDIP28W
	TS27C64A-20VQ	8K x 8	200	5V ± 10%	30mA / 100µA	HIgh Speed	–40 to 85	FDIP28W
	M27C64A-25F6	8K x 8	250	5V ± 10%	30mA / 100µA	High Speed	–40 to 85	FDIP28W
	TS27C64A-25VQ	8K x 8	250	5V ± 10%	30mA / 100µA	HIgh Speed	–40 to 85	FDIP28W
	TS27C64A-30VQ	8K x 8	300	5V ± 10%	30mA / 100µA	HIgh Speed	–40 to 85	FDIP28W
	TS27C64A-20CP	8K x 8	200	5V ± 10%	30mA / 100µA	High Speed	0 to 70	PDIP28
	TS27C64A-25CP	8K x 8	250	5V ± 10%	30mA / 100µA	High Speed	0 to 70	PDIP28
	TS27C64A-20VP	8K x 8	200	5V ± 10%	30mA / 100µA	High Speed	–40 to 85	PDIP28
	TS27C64A-25VP	8K x 8	250	5V ± 10%	30mA / 100µA	High Speed	–40 to 85	PDIP28
	TS27C64A-20CFN	8K x 8	200	5V ± 10%	30mA / 100µA	High Speed	0 to 70	PLCC32
	TS27C64A-25CFN	8K x 8	250	5V ± 10%	30mA / 100µA	High Speed	0 to 70	PLCC32
	TS27C64A-25VFN	8K x 8	200	5V ± 10%	30mA / 100µA	High Speed	–40 to 85	PLCC32
128K	M27C128A-12F1	16K x 8	120	5V ± 10%	30mA / 100µA	PRESTO II, 2 sec.	0 to 70	FDIP28W
	M27C128A-15F1	16K x 8	150	5V ± 10%	30mA / 100µA	PRESTO II, 2 sec	0 to 70	FDIP28W
	M27C128A-20F1	16K x 8	200	5V ± 10%	30mA / 100µA	PRESTO II, 2 sec.	0 to 70	FDIP28W
	M27C128A-20F6	16K x 8	200	5V ± 10%	30mA / 100µA	PRESTO II, 2 sec.	–40 to 85	FDIP28W
256K	M27C256B-80XF1	32K x 8	80	5V ± 5%	30mA / 100µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-10XF1	32K x 8	100	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
256K	M27C256B-12XF1	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-15XF1	32K x 8	150	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-20XF1	32K x 8	200	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-25XF1	32K x 8	250	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-10F1	32K x 8	100	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-12F1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-12F1L	32K x 8	120	5V ± 10%	30mA / 100µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-15F1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-20F1	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-20F1L	32K x 8	200	5V ± 10%	30mA / 100µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-25F1	32K x 8	250	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M27C256B-12XF6	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-15XF6	32K x 8	150	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-20XF6	32K x 8	200	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-25XF6	32K x 8	250	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-12F6	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-15F6	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-20F6	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-20F6L	32K x 8	200	5V ± 10%	30mA / 100µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-25F6	32K x 8	250	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M27C256B-12XB1	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PDIP28
	M27C256B-90B1	32K x 8	90	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PDIP28
	M27C256B-12B1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PDIP28
	M27C256B-15B1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PDIP28

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
256K	M27C256B-20B1	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PDIP28
	M27C256B-15B6	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	PDIP28
	M27C256B-20B6	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	PDIP28
	M27C256B-20B7	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 105	PDIP28
	M27C256B-15B3	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 125	PDIP28
	M27C256B-20B3	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 125	PDIP28
	M27C256B-12XC1	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PLCC32
	M27C256B-15XC1	32K x 8	150	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PLCC32
	M27C256B-12C1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PLCC32
	M27C256B-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PLCC32
	M27C256B-20C1	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PLCC32
	M27C256B-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	PLCC32
	M27C256B-20C6	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	PLCC32
	M27C256B-20C7	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 105	PLCC32
	M27C256B-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 125	PLCC32
	M27C256B-20C3	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 125	PLCC32
	M27C256B-12M1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PSO28
	M27C256B-15M1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PSO28
	M27C256B-20M1	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PSO28
	M27C256B-10N1	32K x 8	100	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PTSO28
	M27C256B-12N1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PTSO28
	M27C256B-15N1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PTSO28
	M87C257-12XF1	32K x 8, Latch	120	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M87C257-20XF1	32K x 8, Latch	200	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
256K	M87C257-12F1	32K x 8, Latch	120	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M87C257-20F1	32K x 8, Latch	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	FDIP28W
	M87C257-15XF6	32K x 8, Latch	150	5V ± 5%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M87C257-15F6	32K x 8, Latch	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	FDIP28W
	M87C257-15C1	32K x 8, Latch	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	0 to 70	PLCC32
	M87C257-20C6	32K x 8, Latch	200	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 85	PLCC32
	M87C257-15C3	32K x 8, Latch	150	5V ± 10%	30mA / 200µA	PRESTO II, 3 sec.	–40 to 125	PLCC32
512K	M27C512-80XF1	64K x 8	80	5V ± 5%	30mA / 100µA	PRESTO II, 7 sec.	0 to 70	FDIP28W
	M27C512-12XF1	64K x 8	120	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	FDIP28W
	M27C512-15XF1	64K x 8	150	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec	0 to 70	FDIP28W
	M27C512-20XF1	64K x 8	200	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec	0 to 70	FDIP28W
	M27C512-25XF1	64K x 8	250	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec	0 to 70	FDIP28W
	M27C512-10F1	64K x 8	100	5V ± 10%	30mA / 100µA	PRESTO II, 7 sec	0 to 70	FDIP28W
	M27C512-12F1	64K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec	0 to 70	FDIP28W
	M27C512-15F1	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	FDIP28W
	M27C512-20F1	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	FDIP28W
	M27C512-20F1L	64K x 8	200	5V ± 10%	30mA / 100µA	PRESTO II, 7 sec	0 to 70	FDIP28W
	M27C512-25F1	64K x 8	250	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec	0 to 70	FDIP28W
	M27C512-12XF6	64K x 8	120	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec	–40 to 85	FDIP28W
	M27C512-15XF6	64K x 8	150	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 85	FDIP28W
	M27C512-20XF6	64K x 8	200	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 85	FDIP28W
	M27C512-25XF6	64K x 8	250	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 85	FDIP28W
	M27C512-15F6	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 85	FDIP28W
	M27C512-20F6	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 85	FDIP28W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
512K	M27C512-20XF3	64K x 8	200	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 125	FDIP28W
	M27C512-10F3	64K x 8	100	5V ± 10%	30mA / 100µA	PRESTO II, 7 sec.	–40 to 125	FDIP28W
	M27C512-15XB1	64K x 8	150	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PDIP28
	M27C512-15B1	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PDIP28
	M27C512-20B1	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PDIP28
	M27C512-20B6	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec	–40 to 85	PDIP28
	M27C512-20B3	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec	–40 to 125	PDIP28
	M27C512-15XC1	64K x 8	150	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec	0 to 70	PLCC32
	M27C512-15C1	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PLCC32
	M27C512-20C1	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PLCC32
	M27C512-20XC6	64K x 8	200	5V ± 5%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 85	PLCC32
	M27C512-20C6	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 85	PLCC32
	M27C512-15C3	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 125	PLCC32
	M27C512-20C3	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	–40 to 125	PLCC32
	M27C512-10N1	64K x 8	100	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PTSO28
	M27C512-12N1	64K x 8	120	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PTSO28
	M27C512-15N1	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PTSO28
	M27V512-200K1	64K x 8	200	3.0 to 5.5V	10mA / 100µA	PRESTO II, 7 sec.	0 to 70	PLCC32
	M27V512-250K1	64K x 8	250	3.0 to 5 5V	10mA / 100µA	PRESTO II, 7 sec	0 to 70	PLCC32
	M27V512-200N1	64K x 8	200	3 0 to 5 5V	10mA / 100µA	PRESTO II, 7 sec.	0 to 70	PTSO28
	M27V512-250N1	64K x 8	250	3.0 to 5.5V	10mA / 100µA	PRESTO II, 7 sec.	0 to 70	PTSO28
	M27C516-20F1	32K x 16	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C516-15C1	32K x 16	150	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PLCC32
	M27C516-20C1	32K x 16	200	5V ± 10%	30mA / 200µA	PRESTO II, 7 sec.	0 to 70	PLCC32

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
1M	M27C1000-12XF1 *	128K x 8	120	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-15XF1 *	128K x 8	150	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-20XF1 *	128K x 8	200	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-25XF1 *	128K x 8	250	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-10F1 *	128K x 8	100	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-12F1 *	128K x 8	120	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-15F1 *	128K x 8	150	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-20F1 *	128K x 8	200	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1000-20B1 *	128K x 8	200	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	PDIP32
	M27C1001-80XF1	128K x 8	80	5V ± 5%	30mA / 100µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-12XF1	128K x 8	120	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-15XF1	128K x 8	150	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-15XF1L	128K x 8	150	5V ± 5%	30mA / 100µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-20XF1	128K x 8	200	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-25XF1	128K x 8	250	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-10F1	128K x 8	100	5V ± 10%	30mA / 100µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-12F1	128K x 8	120	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-15F1	128K x 8	150	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-15F1L	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-20F1	128K x 8	200	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-20F1L	128K x 8	200	5V ± 10%	30mA / 100µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-25F1	128K x 8	250	5V ± 10%	35mA / 200µA	PRESTO II, 13 sec.	0 to 70	FDIP32W
	M27C1001-12XF6	128K x 8	120	5V ± 5%	35mA / 200µA	PRESTO II, 13 sec.	–40 to 85	FDIP32W

* ROM compatible pin-out

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
1M	M27C1001-15XF6	128K x 8	150	5V ± 5%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 85	FDIP32W
	M27C1001-20XF6	128K x 8	200	5V ± 5%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 85	FDIP32W
	M27C1001-15F6	128K x 8	150	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 85	FDIP32W
	M27C1001-15F6L	128K x 8	150	5V ± 10%	35mA / 100μA	PRESTO II, 13 sec.	–40 to 85	FDIP32W
	M27C1001-20F6	128K x 8	200	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 85	FDIP32W
	M27C1001-15B1	128K x 8	150	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	0 to 70	PDIP32
	M27C1001-20B1	128K x 8	200	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	0 to 70	PDIP32
	M27C1001-20B6	128K x 8	200	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 85	PDIP32
	M27C1001-20B3	128K x 8	200	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 125	PDIP32
	M27C1001-12XC1	128K x 8	120	5V ± 5%	35mA / 200μA	PRESTO II, 13 sec.	0 to 70	PLCC32
	M27C1001-15C1	128K x 8	150	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	0 to 70	PLCC32
	M27C1001-20C1	128K x 8	200	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	0 to 70	PLCC32
	M27C1001-15C6	128K x 8	150	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 85	PLCC32
	M27C1001-15C3	128K x 8	150	5V ± 10%	35mA / 200μA	PRESTO II, 13 sec.	–40 to 125	PLCC32
	M27C1001-12L1	128K x 8	120	5V ± 10%	30mA / 100μA	PRESTO II, 13 sec	0 to 70	LCCC32W
	M27V101-250L1	128K x 8	250	3.0 to 5.5V	30mA / 100μA	PRESTO II, 13 sec	0 to 70	LCCC32W
	M27V101-200L6	128K x 8	200	3.2 to 5.5V	35mA / 100μA	PRESTO II, 13 sec.	–40 to 85	LCCC32W
	M27V101-250L6	128K x 8	250	3.2 to 5.5V	35mA / 100μA	PRESTO II, 13 sec.	–40 to 85	LCCC32W
	M27C1024-12XF1	64K x 16	120	5V ± 5%	35mA / 100μA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C1024-15XF1	64K x 16	150	5V ± 5%	35mA / 100μA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C1024-20XF1	64K x 16	200	5V ± 5%	35mA / 100μA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C1024-25XF1	64K x 16	250	5V ± 5%	35mA / 100μA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C1024-12F1	64K x 16	120	5V ± 10%	35mA / 100μA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C1024-15F1	64K x 16	150	5V ± 10%	35mA / 100μA	PRESTO II, 7 sec.	0 to 70	FDIP40W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
1M	M27C1024-20F1	64K x 16	200	5V ± 10%	35mA / 100µA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C1024-25F1	64K x 16	250	5V ± 10%	35mA / 100µA	PRESTO II, 7 sec.	0 to 70	FDIP40W
	M27C1024-12XF6	64K x 16	120	5V ± 5%	35mA / 100µA	PRESTO II, 7 sec.	–40 to 85	FDIP40W
	M27C1024-15C1	64K x 16	150	5V ± 10%	35mA / 100µA	PRESTO II, 7 sec.	0 to 70	PLCC44
	M27C1024-20C1	64K x 16	200	5V ± 10%	35mA / 100µA	PRESTO II, 7 sec.	0 to 70	PLCC44
2M	M27C2001-80XF1	256K x 8	80	5V ± 5%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-15XF1	256K x 8	150	5V ± 5%	35mA / 200µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-20XF1	256K x 8	200	5V ± 5%	35mA / 200µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-25XF1	256K x 8	250	5V ± 5%	35mA / 200µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-10F1	256K x 8	100	5V ± 10%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-12F1	256K x 8	120	5V ± 10%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-15F1	256K x 8	150	5V ± 10%	35mA / 200µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-20F1	256K x 8	200	5V ± 10%	35mA / 200µA	PRESTO II, 26 sec.	0 to 70	FDIP32W
	M27C2001-12F6	256K x 8	120	5V ± 10%	35mA / 100µA	PRESTO II, 26 sec.	–40 to 85	FDIP32W
	M27C2001-20F6	256K x 8	200	5V ± 10%	35mA / 200µA	PRESTO II, 26 sec.	–40 to 85	FDIP32W
	M27C2001-12B1	256K x 8	120	5V ± 10%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	PDIP32
	M27C2001-15B1	256K x 8	150	5V ± 10%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	PDIP32
	M27C2001-10XC1	256K x 8	100	5V ± 5%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	PLCC32
	M27C2001-12C1	256K x 8	120	5V ± 10%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	PLCC32
	M27C2001-15C1	256K x 8	150	5V ± 10%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	PLCC32
	M27C2001-12L1	256K x 8	120	5V ± 10%	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	LCCC32W
	M27V201-250L1	256K x 8	250	3.0 to 5.5V	30mA / 100µA	PRESTO II, 26 sec.	0 to 70	LCCC32W
	M27V201-200L6	256K x 8	200	3.2 to 5.5V	35mA / 100µA	PRESTO II, 26 sec.	–40 to 85	LCCC32W
	M27V201-250L6	256K x 8	250	3.2 to 5.5V	35mA / 100µA	PRESTO II, 26 sec.	–40 to 85	LCCC32W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
4M	M27C4001-80XF1	512K x 8	80	5V ± 5%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	FDIP32W
	M27C4001-10XF1	512K x 8	100	5V ± 5%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	FDIP32W
	M27C4001-10F1	512K x 8	100	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	FDIP32W
	M27C4001-12F1	512K x 8	120	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	FDIP32W
	M27C4001-15F1	512K x 8	150	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	FDIP32W
	M27C4001-12F6	512K x 8	120	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	–40 to 85	FDIP32W
	M27C4001-15F6	512K x 8	150	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	–40 to 85	FDIP32W
	M27C4001-10F2	512K x 8	100	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	–55 to 125	FDIP32W
	M27C4001-12B1	512K x 8	120	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	PDIP32
	M27C4001-15B1	512K x 8	150	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	PDIP32
	M27C4001-10XC1	512K x 8	100	5V ± 5%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	PLCC32
	M27C4001-12C1	512K x 8	120	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	PLCC32
	M27C4001-15C1	512K x 8	150	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	PLCC32
	M27C4001-12L1	512K x 8	120	5V ± 10%	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	LCCC32W
	M27V401-250L1	512K x 8	250	3.0 to 5.5V	50mA / 100µA	PRESTO II, 52 sec.	0 to 70	LCCC32W
	M27V401-200L6	512K x 8	200	3.2 to 5.5V	50mA / 100µA	PRESTO II, 52 sec.	–40 to 85	LCCC32W
	M27V401-250L6	512K x 8	250	3.2 to 5.5V	50mA / 100µA	PRESTO II, 52 sec.	–40 to 85	LCCC32W
	M27C4002-10XF1	256K x 16	100	5V ± 5%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	FDIP40W
	M27C4002-10F1	256K x 16	100	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	FDIP40W
	M27C4002-12F1	256K x 16	120	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	FDIP40W
	M27C4002-15F1	256K x 16	150	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	FDIP40W
	M27C4002-12F6	256K x 16	120	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	–40 to 85	FDIP40W
	M27C4002-15F6	256K x 16	150	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	–40 to 85	FDIP40W
	M27C4002-10F2	256K x 16	100	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	–55 to 125	FDIP40W

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
4M	M27C4002-12J1	256K x 16	120	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	JLCC44W
	M27C4002-12J6	256K x 16	120	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	–40 to 85	JLCC44W
	M27C4002-15B1	256K x 16	150	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	PDIP40
	M27C4002-12XC1	256K x 16	120	5V ± 5%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	PLCC44
	M27C4002-15C1	256K x 16	150	5V ± 10%	50mA / 100µA	PRESTO II, 26 sec.	0 to 70	PLCC44
16M	M27C160-150F1	x8 / x16	150	5V ± 10%	50mA / 100µA	PRESTO II, 10 sec	0 to 70	FDIP42W
	M27C160-200F1	x8 / x16	200	5V ± 10%	50mA / 100µA	PRESTO II, 10 sec	0 to 70	FDIP42W

NMOS UV EPROM

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
16K	M2716F1	2K x 8	450	5V ± 5%	100mA/25mA	Fixed pulse, 100 sec.	0 to 70	FDIP24W
	M2716-1F1	2K x 8	350	5V ± 10%	100mA/25mA	Fixed pulse, 100 sec.	0 to 70	FDIP24W
	M2716-1F6	2K x 8	350	5V ± 10%	100mA/25mA	Fixed pulse, 100 sec.	–40 to 85	FDIP24W
32K	M2732A-2F1	4K x 8	200	5V ± 5%	125mA/35mA	Fixed pulse, 200 sec.	0 to 70	FDIP24W
	M2732AF1	4K x 8	250	5V ± 5%	125mA/35mA	Fixed pulse, 200 sec.	0 to 70	FDIP24W
	M2732A-3F1	4K x 8	300	5V ± 5%	125mA/35mA	Fixed pulse, 200 sec.	0 to 70	FDIP24W
	M2732A-4F1	4K x 8	450	5V ± 5%	125mA/35mA	Fixed pulse, 200 sec.	0 to 70	FDIP24W
	M2732AF6	4K x 8	250	5V ± 5%	125mA/35mA	Fixed pulse, 200 sec.	–40 to 85	FDIP24W
	M2732A-4F6	4K x 8	450	5V ± 5%	125mA/35mA	Fixed pulse, 200 sec.	–40 to 85	FDIP24W

NMOS UV EPROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
64K	M2764A-1F1	8K x 8	180	5V ± 5%	75mA/35mA	Fast, 32 sec.	0 to 70	FDIP28W
	M2764A-2F1	8K x 8	200	5V ± 5%	75mA/35mA	Fast, 32 sec.	0 to 70	FDIP28W
	M2764AF1	8K x 8	250	5V ± 5%	75mA/35mA	Fast, 32 sec.	0 to 70	FDIP28W
	M2764A-3F1	8K x 8	300	5V ± 5%	75mA/35mA	Fast, 32 sec.	0 to 70	FDIP28W
	M2764A-4F1	8K x 8	450	5V ± 5%	75mA/35mA	Fast, 32 sec.	0 to 70	FDIP28W
	M2764A-20F1	8K x 8	200	5V ± 10%	75mA/35mA	Fast, 32 sec.	0 to 70	FDIP28W
	M2764A-25F1	8K x 8	250	5V ± 10%	75mA/35mA	Fast, 32 sec.	0 to 70	FDIP28W
	M2764A-2F6	8K x 8	200	5V ± 5%	75mA/35mA	Fast, 32 sec.	–40 to 85	FDIP28W
	M2764AF6	8K x 8	250	5V ± 5%	75mA/35mA	Fast, 32 sec.	–40 to 85	FDIP28W
	M2764A-4F6	8K x 8	450	5V ± 5%	75mA/35mA	Fast, 32 sec.	–40 to 85	FDIP28W
128K	M27128A-2F1	16K x 8	200	5V ± 5%	85mA/40mA	Fast, 64 sec.	0 to 70	FDIP28W
	M27128AF1	16K x 8	250	5V ± 5%	85mA/40mA	Fast, 64 sec.	0 to 70	FDIP28W
	M27128A-3F1	16K x 8	300	5V ± 5%	85mA/40mA	Fast, 64 sec.	0 to 70	FDIP28W
	M27128A-4F1	16K x 8	450	5V ± 5%	85mA/40mA	Fast, 64 sec.	0 to 70	FDIP28W
	M27128A-20F1	16K x 8	200	5V ± 10%	85mA/40mA	Fast, 64 sec.	0 to 70	FDIP28W
	M27128A-25F1	16K x 8	250	5V ± 10%	85mA/40mA	Fast, 64 sec.	0 to 70	FDIP28W
	M27128A-30F1	16K x 8	300	5V ± 10%	85mA/40mA	Fast, 64 sec.	0 to 70	FDIP28W
	M27128AF6	16K x 8	250	5V ± 5%	85mA/40mA	Fast, 64 sec.	–40 to 85	FDIP28W
256K	M27256-1F1	32K x 8	170	5V ± 5%	100mA/40mA	Fast, 128 sec.	0 to 70	FDIP28W
	M27256-2F1	32K x 8	200	5V ± 5%	100mA/40mA	Fast, 128 sec.	0 to 70	FDIP28W
	M27256F1	32K x 8	250	5V ± 5%	100mA/40mA	Fast, 128 sec.	0 to 70	FDIP28W
	M27256-3F1	32K x 8	300	5V ± 5%	100mA/40mA	Fast, 128 sec.	0 to 70	FDIP28W
	M27256-4F1	32K x 8	450	5V ± 5%	100mA/40mA	Fast, 128 sec.	0 to 70	FDIP28W
	M27256-20F1	32K x 8	200	5V ± 10%	100mA/40mA	Fast, 128 sec.	0 to 70	FDIP28W

NMOS UV EPROM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
256K	M27256-25F1	32K x 8	250	5V ± 10%	100mA/40mA	Fast, 128 sec.	0 to 70	FDIP28W
	M27256F6	32K x 8	250	5V ± 5%	100mA/40mA	Fast. 128 sec.	–40 to 85	FDIP28W
512K	M27512-2F1	32K x 8	200	5V ± 5%	125mA/40mA	PRESTO, 32 sec	0 to 70	FDIP28W
	M27512F1	32K x 8	250	5V ± 5%	125mA/40mA	PRESTO, 32 sec.	0 to 70	FDIP28W
	M27512-3F1	32K x 8	300	5V ± 5%	125mA/40mA	PRESTO, 32 sec.	0 to 70	FDIP28W
	M27512-20F1	32K x 8	200	5V ± 10%	125mA/40mA	PRESTO, 32 sec.	0 to 70	FDIP28W
	M27512-25F1	32K x 8	250	5V ± 10%	125mA/40mA	PRESTO. 32 sec	0 to 70	FDIP28W
	M27512-2F6	32K x 8	200	5V ± 5%	125mA/40mA	PRESTO, 32 sec	–40 to 85	FDIP28W
	M27512F6	32K x 8	250	5V ± 5%	125mA/40mA	PRESTO, 32 sec	–40 to 85	FDIP28W

FLASH MEMORIES

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
256K	M28F256-10XB1	32K x 8	100	5V ±5%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F256A-10XB1	32K x 8	100	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F256-12B1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F256A-12B1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F256-15B1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F256A-15B1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F256A-20B1	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F256A-12XB6	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32

FLASH MEMORIES (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
256K	M28F256-12B6	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F256A-12B6	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F256-15B6	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F256A-15B6	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F256A-12XB3	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PDIP32
	M28F256-15B3	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PDIP32
	M28F256A-15B3	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PDIP32
	M28F256-10XC1	32K x 8	100	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256A-10XC1	32K x 8	100	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256-12C1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256A-12C1	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256A-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256-20C1	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256A-20C1	32K x 8	200	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F256A-12XC6	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F256A-12C6	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F256A-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F256A-12XC3	32K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
	M28F256-12C3	32K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
	M28F256-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
	M28F256A-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
512K	M28F512-10XB1	64K x 8	100	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F512-12B1	64K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32

FLASH MEMORIES (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
512K	M28F512-15B1	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F512-20B1	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F512-12XB6	64K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F512-12B6	64K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F512-15B6	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F512-12XB3	64K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PDIP32
	M28F512-15B3	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PDIP32
	M28F512-10XC1	64K x 8	100	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F512-12C1	64K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F512-15C1	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F512-20C1	64K x 8	200	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F512-12XC6	64K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F512-12C6	64K x 8	120	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F512-15C6	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F512-12XC3	64K x 8	120	5V ± 5%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
	M28F512-15C3	64K x 8	150	5V ± 10%	30mA / 200µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
1M	M28F101-10XP1	128K x 8	100	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F141-10XP1	128K x 8 (4 Blocks)	100	5V ± 5%	30mA / 100µA	PRESTO F, 4 x Block Erase	0 to 70	PDIP32
	M28F101-12XP1	128K x 8	120	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F141-12XP1	128K x 8 (4 Blocks)	120	5V ± 5%	30mA / 100µA	PRESTO F, 4 x Block Erase	0 to 70	PDIP32
	M28F101-15P1	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PDIP32
	M28F141-15P1	128K x 8 (4 Blocks)	150	5V ± 5%	30mA / 100µA	PRESTO F, 4 x Block Erase	0 to 70	PDIP32

FLASH MEMORIES (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
1M	M28F101-12XP6	128K x 8	120	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F101-15P6	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PDIP32
	M28F101-12XP3	128K x 8	120	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PDIP32
	M28F101-15P3	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PDIP32
	M28F101-10XK1	128K x 8	100	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F141-10XK1	128K x 8 (4 Blocks)	100	5V ± 5%	30mA / 100µA	PRESTO F, 4 x Block Erase	0 to 70	PLCC32
	M28F101-12XK1	128K x 8	120	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F141-12XK1	128K x 8 (4 Blocks)	120	5V ± 5%	30mA / 100µA	PRESTO F, 4 x Block Erase	0 to 70	PLCC32
	M28F101-15K1	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PLCC32
	M28F141-15K1	128K x 8 (4 Blocks)	150	5V ± 5%	30mA / 100µA	PRESTO F, 4 x Block Erase	0 to 70	PLCC32
	M28F101-12XK6	128K x 8	120	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F101-15K6	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PLCC32
	M28F101-12XK3	128K x 8	120	5V ± 5%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
	M28F101-15K3	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PLCC32
	M28F101-12N1	128K x 8	120	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PTSO32
	M28F101-15N1	128K x 8	150	5V ± 10%	30mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PTSO32
	M28F102-10XP1	64K x 16	100	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PDIP40
	M28F102-12XP1	64K x 16	120	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PDIP40
	M28F102-15P1	64K x 16	150	5V ± 10%	50mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PDIP40
	M28F102-12XP6	64K x 16	120	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PDIP40
	M28F102-15P6	64K x 16	150	5V ± 10%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PDIP40
	M28F102-12XP3	64K x 16	120	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PDIP40

FLASH MEMORIES (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
1M	M28F102-15P3	64K x 16	150	5V ± 10%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PDIP40
	M28F102-10XK1	64K x 16	100	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PLCC44
	M28F102-12XK1	64K x 16	120	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PLCC44
	M28F102-15K1	64K x 16	150	5V ± 10%	50mA / 100µA	PRESTO F, 12V/10µs	0 to 70	PLCC44
	M28F102-12XK6	64K x 16	120	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PLCC44
	M28F102-15K6	64K x 16	150	5V ± 10%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 85	PLCC44
	M28F102-12XK3	64K x 16	120	5V ± 5%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PLCC44
	M28F102-15K3	64K x 16	150	5V ± 10%	50mA / 100µA	PRESTO F, 12V/10µs	–40 to 125	PLCC44

ROM

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Standby	Temperature Range (°C)	Package
512K	M23C512B1ZZ	64K x 8	100	5V ± 10%	40mA / 20µA	0 to 70	PDIP28
1M	M23C1000B1ZZ	128K x 8	100	5V ± 10%	40mA / 20µA	0 to 70	PDIP28
	M23C1001B1ZZ *	128K x 8	100	5V ± 10%	40mA / 20µA	0 to 70	PDIP32

* EPROM compatible pin-out - ZZ is a code allocated for each ROM content

EEPROM, I^2C and MICROWIRE Serial Access Bus

Size	Part Number	Organisation	Bus Type	Vcc Range	Features	Temperature Range (°C)	Package
1K	ST24C01B1	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	0 to 70	PSDIP8
	ST25C01B1	128 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	0 to 70	PSDIP8
	ST24C01B6	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 85	PSDIP8
	ST25C01B6	128 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	–40 to 85	PSDIP8
	ST24C01B3	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 125	PSDIP8
	ST24C01M1	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	0 to 70	PSO8
	ST24C01M1013TR	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	0 to 70	PSO8TR
	ST25C01M1	128 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	0 to 70	PSO8
	ST25C01M1013TR	128 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	0 to 70	PSO8TR
	ST24C01M6	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 85	PSO8
	ST24C01M6013TR	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 85	PSO8TR
	ST25C01M6	128 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	–40 to 85	PSO8
	ST25C01M6013TR	128 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	–40 to 85	PSO8TR
	ST24C01M3	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 125	PSO8
	ST24C01M3013TR	128 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 125	PSO8TR
2K	ST24C02AB1	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	0 to 70	PSDIP8
	ST24C02AB1/AAB	256 x 8	I^2C	4.5 to 5.5V	Content all 00	0 to 70	PSDIP8
	ST25C02AB1	256 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	0 to 70	PSDIP8
	ST24C02AB6	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 85	PSDIP8
	ST25C02AB6	256 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	–40 to 85	PSDIP8
	ST24C02AB3	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 125	PSDIP8
	ST24C02AM1	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	0 to 70	PSO8
	ST24C02AM1013TR	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	0 to 70	PSO8TR
	ST25C02AM1	256 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	0 to 70	PSO8

EEPROM, I^2C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	Bus Type	Vcc Range	Features	Temperature Range (°C)	Package
2K	ST25C02AM1013TR	256 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	0 to 70	PSO8TR
	ST24C02AM6	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 85	PSO8
	ST24C02AM6013TR	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 85	PSO8TR
	ST25C02AM6	256 x 8	I^2C	2.5 to 5.5V	Byte/Page Write	–40 to 85	PSO8
	ST24C02AM3	256 x 8	I^2C	4.5 to 5.5V	Byte/Page Write	–40 to 125	PSO8
4K	ST24C04B1	512 x 8	I^2C	4.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST25C04B1	512 x 8	I^2C	2.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST24C04B6	512 x 8	I^2C	4.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST25C04B6	512 x 8	I^2C	2.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST24C04B3	512 x 8	I^2C	4.5 to 5.5V	Write Protection	–40 to 125	PSDIP8
	ST25C04B3	512 x 8	I^2C	2.5 to 5.5V	Write Protection	–40 to 125	PSDIP8
	ST24C04ML1	512 x 8	I^2C	4.5 to 5.5V	Write Protection	0 to 70	PSO14
	ST24C04ML1013TR	512 x 8	I^2C	4.5 to 5.5V	Write Protection	0 to 70	PSO14TR
	ST25C04ML1	512 x 8	I^2C	2.5 to 5.5V	Write Protection	0 to 70	PSO14
	ST25C04ML1013TR	512 x 8	I^2C	2.5 to 5.5V	Write Protection	0 to 70	PSO14TR
8K	ST24C08B1	1K x 8	I^2C	4.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST25C08B1	1K x 8	I^2C	2.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST24C08B6	1K x 8	I^2C	4.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST25C08B6	1K x 8	I^2C	2.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
16K	ST24C16CB1	2K x 8	I^2C	4.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST25C16CB1	2K x 8	I^2C	2.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST24C16CB6	2K x 8	I^2C	4.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST25C16CB6	2K x 8	I^2C	2.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
256	ST93C06B1	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSDIP8

EEPROM, I^{2}C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	Bus Type	Vcc Range	Features	Temperature Range (°C)	Package
256	ST93C06B6	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C06B3	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C06M1	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSO8
	ST93C06M1013TR	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSO8TR
	ST93C06M6	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSO8
	ST93C06M6013TR	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSO8TR
	ST93C06M3	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSO8
	ST93C06M3013TR	32x8 or 16x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSO8TR
1K	ST93CS46B1	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST93CS47B1	64 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST93CS46B6	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST93CS47B6	64 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST93CS46B3	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 125	PSDIP8
	ST93CS46M1	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSO8
	ST93CS47M1	64 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	0 to 70	PSO8
	ST93CS46M6	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSO8
	ST93CS47M6	64 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 85	PSO8
	ST93CS46M3	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 125	PSO8
	ST93CS46ML1	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSO14
	ST93CS47ML1	64 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	0 to 70	PSO14
	ST93CS46ML6	64 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSO14
	ST93CS47ML6	64 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 85	PSO14
	ST93C46AB1	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C46AB6	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSDIP8

EEPROM, I^{2}C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	Bus Type	Vcc Range	Features	Temperature Range (°C)	Package
1K	ST93C46AB3	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C46AM1	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSO8
	ST93C46AM1013TR	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSO8TR
	ST93C46TM1	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	90° Turn Pinout	0 to 70	PSO8
	ST93C46TM1013TR	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	90° Turn Pinout	0 to 70	PSO8TR
	ST93C46AM6	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSO8
	ST93C46AM6013TR	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSO8TR
	ST93C46TM6	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	90° Turn Pinout	–40 to 85	PSO8
	ST93C46TM6013TR	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	90° Turn Pinout	–40 to 85	PSO8TR
	ST93C46AM3	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSO8
	ST93C46AM3013TR	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSO8TR
	ST93C46TM3	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	90° Turn Pinout	–40 to 125	PSO8
	ST93C46TM3013TR	128x8 or 64x16	MICROWIRE	4.5 to 5.5V	90° Turn Pinout	–40 to 125	PSO8TR
2K	ST93CS56B1	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST93CS57B1	128 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST93CS56B6	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST93CS57B6	128 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST93CS56B3	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 125	PSDIP8
	ST93CS56M1	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSO8
	ST93CS56M1013TR	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSO8TR
	ST93CS57M1	128 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	0 to 70	PSO8
	ST93CS56M6	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSO8
	ST93CS57M6	128 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 85	PSO8
	ST93CS56M3	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 125	PSO8

EEPROM, I²C and MICROWIRE Serial Access Bus (cont'd)

Size	Part Number	Organisation	Bus Type	Vcc Range	Features	Temperature Range (°C)	Package
2K	ST93CS56ML1	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSO14
	ST93CS57ML1	128 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	0 to 70	PSO14
	ST93CS56ML6	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSO14
	ST93CS57ML6	128 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 85	PSO14
	ST93CS56ML3	128 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 125	PSO14
	ST93C56B1	256x8 or 128x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C56B6	256x8 or 128x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C56B3	256x8 or 128x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C56M1	256x8 or 128x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSO8
	ST93C56M6	256x8 or 128x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSO8
	ST93C56M3	256x8 or 128x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSO8
4K	ST93CS66B1	256 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST93CS67B1	256 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	0 to 70	PSDIP8
	ST93CS66B6	256 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST93CS67B6	256 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 85	PSDIP8
	ST93CS66B3	256 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 125	PSDIP8
	ST93CS67B3	256 x 16	MICROWIRE	2.5 to 5.5V	Write Protection	–40 to 125	PSDIP8
	ST93CS66ML1	256 x 16	MICROWIRE	4.5 to 5.5V	Write Protection	–40 to 85	PSO14
	ST93C66CB1	512x8 or 256x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSDIP8
	ST93C66CB6	512x8 or 256x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSDIP8
	ST93C66CB3	512x8 or 256x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSDIP8
	ST93C66CM1	512x8 or 256x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	0 to 70	PSO8
	ST93C66CM6	512x8 or 256x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 85	PSO8
	ST93C66CM3	512x8 or 256x16	MICROWIRE	4.5 to 5.5V	Dual Org, 1MHz	–40 to 125	PSO8

EEPROM, Parallel Access Bus

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Programming	Temperature Range (°C)	Package
64K	M28C64C-150P1	8K x 8	150	5V ± 10%	30mA / 100µA	5ms	0 to 70	PDIP28
	M28C64C-200P1	8K x 8	200	5V ± 10%	30mA / 100µA	5ms	0 to 70	PDIP28
	M28C64C-150P6	8K x 8	150	5V ± 10%	30mA / 100µA	5ms	–40 to 85	PDIP28
	M28C64C-200P6	8K x 8	200	5V ± 10%	30mA / 100µA	5ms	–40 to 85	PDIP28
	M28C64C-150K1	8K x 8	150	5V ± 10%	30mA / 100µA	5ms	0 to 70	PLCC32
	M28C64C-200K1	8K x 8	200	5V ± 10%	30mA / 100µA	5ms	0 to 70	PLCC32
	M28C64C-150K6	8K x 8	150	5V ± 10%	30mA / 100µA	5ms	–40 to 85	PLCC32
	M28C64C-200K6	8K x 8	200	5V ± 10%	30mA / 100µA	5ms	–40 to 85	PLCC32
	M28C64C-150M1	8K x 8	150	5V ± 10%	30mA / 100µA	5ms	0 to 70	PSO28
	M28C64C-200M1	8K x 8	200	5V ± 10%	30mA / 100µA	5ms	0 to 70	PSO28
	M28C64C-150M6	8K x 8	150	5V ± 10%	30mA / 100µA	5ms	–40 to 85	PSO28
	M28C64C-200M6	8K x 8	200	5V ± 10%	30mA / 100µA	5ms	–40 to 85	PSO28

FAST SRAM

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Features	Temperature Range (°C)	Package
64K	M621064-10PS1	64K x 1	10	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSDIP22
	M621064-12PS1	64K x 1	12	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSDIP22
	M621064-15PS1	64K x 1	15	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSDIP22
	M621064-20PS1	64K x 1	20	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSDIP22
	M621064-10E1	64K x 1	10	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSOJ24
	M621064-12E1	64K x 1	12	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSOJ24
	M621064-15E1	64K x 1	15	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSOJ24
	M621064-20E1	64K x 1	20	5V ± 10%	140mA / 20mA	Separate I/O	0 to 70	PSOJ24
	M624016-10PS1	16K x 4	10	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSDIP22
	M624016-12PS1	16K x 4	12	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSDIP22
	M624016-15PS1	16K x 4	15	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSDIP22
	M624016-20PS1	16K x 4	20	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSDIP22
	M624016-10E1	16K x 4	10	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSOJ24
	M624016-12E1	16K x 4	12	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSOJ24
	M624016-15E1	16K x 4	15	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSOJ24
	M624016-20E1	16K x 4	20	5V ± 10%	140mA / 20mA	Common I/O	0 to 70	PSOJ24
	M624017-10PS1	16K x 4	10	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP24
	M624017-12PS1	16K x 4	12	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP24
	M624017-15PS1	16K x 4	15	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP24
	M624017-20PS1	16K x 4	20	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP24
	M624017-10E1	16K x 4	10	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ24
	M624017-12E1	16K x 4	12	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ24
	M624017-15E1	16K x 4	15	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ24
	M624017-20E1	16K x 4	20	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ24

FAST SRAM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Features	Temperature Range (°C)	Package
64K	M628008-10PS1	8K x 8	10	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP28
	M628008-12PS1	8K x 8	12	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP28
	M628008-15PS1	8K x 8	15	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP28
	M628008-20PS1	8K x 8	20	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSDIP28
	M628008-10E1	8K x 8	10	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ28
	M628008-12E1	8K x 8	12	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ28
	M628008-15E1	8K x 8	15	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ28
	M628008-20E1	8K x 8	20	5V ± 10%	140mA / 20mA	With Output Enable	0 to 70	PSOJ28
256K	M621256-12PS1	256K x 1	12	5V ± 10%	140mA / 1mA	Separate I/O	0 to 70	PSDIP24
	M621256-15PS1	256K x 1	15	5V ± 10%	130mA / 1mA	Separate I/O	0 to 70	PSDIP24
	M621256-20PS1	256K x 1	20	5V ± 10%	120mA / 1mA	Separate I/O	0 to 70	PSDIP24
	M621256-12E1	256K x 1	12	5V ± 10%	140mA / 1mA	Separate I/O	0 to 70	PSOJ24
	M621256-15E1	256K x 1	15	5V ± 10%	130mA / 1mA	Separate I/O	0 to 70	PSOJ24
	M621256-20E1	256K x 1	20	5V ± 10%	120mA / 1mA	Separate I/O	0 to 70	PSOJ24
	M624064-12PS1	64K x 4	12	5V ± 10%	140mA / 1mA	Common I/O	0 to 70	PSDIP24
	M624064-15PS1	64K x 4	15	5V ± 10%	130mA / 1mA	Common I/O	0 to 70	PSDIP24
	M624064-20PS1	64K x 4	20	5V ± 10%	120mA / 1mA	Common I/O	0 to 70	PSDIP24
	M624064-12E1	64K x 4	12	5V ± 10%	140mA / 1mA	Common I/O	0 to 70	PSOJ24
	M624064-15E1	64K x 4	15	5V ± 10%	130mA / 1mA	Common I/O	0 to 70	PSOJ24
	M624064-20E1	64K x 4	20	5V ± 10%	120mA / 1mA	Common I/O	0 to 70	PSOJ24
	M624065-12PS1	64K x 4	12	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSDIP28
	M624065-15PS1	64K x 4	15	5V ± 10%	130mA / 1mA	With Output Enable	0 to 70	PSDIP28
	M624065-20PS1	64K x 4	20	5V ± 10%	120mA / 1mA	With Output Enable	0 to 70	PSDIP28
	M624065-12E1	64K x 4	12	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSOJ28

FAST SRAM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Features	Temperature Range (°C)	Package
256K	M624065-15E1	64K x 4	15	5V ± 10%	130mA / 1mA	With Output Enable	0 to 70	PSOJ28
	M624065-20E1	64K x 4	20	5V ± 10%	120mA / 1mA	With Output Enable	0 to 70	PSOJ28
	M628032-12PS1	32K x 8	12	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSDIP28
	M628032-15PS1	32K x 8	15	5V ± 10%	130mA / 1mA	With Output Enable	0 to 70	PSDIP28
	M628032-20PS1	32K x 8	20	5V ± 10%	120mA / 1mA	With Output Enable	0 to 70	PSDIP28
	M628032-12E1	32K x 8	12	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSOJ28
	M628032-15E1	32K x 8	15	5V ± 10%	130mA / 1mA	With Output Enable	0 to 70	PSOJ28
	M628032-20E1	32K x 8	20	5V ± 10%	120mA / 1mA	With Output Enable	0 to 70	PSOJ28
288K	M629032-12PS1	32K x 9	12	5V ± 10%	160mA / 1mA	With Output Enable	0 to 70	PSDIP32
	M629032-15PS1	32K x 9	15	5V ± 10%	150mA / 1mA	With Output Enable	0 to 70	PSDIP32
	M629032-20PS1	32K x 9	20	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSDIP32
	M629032-12E1	32K x 9	12	5V ± 10%	160mA / 1mA	With Output Enable	0 to 70	PSOJ32
	M629032-15E1	32K x 9	15	5V ± 10%	150mA / 1mA	With Output Enable	0 to 70	PSOJ32
	M629032-20E1	32K x 9	20	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSOJ32
1M	M621100-15E1	1M x 1	15	5V ± 10%	140mA / 1mA	Separate I/O	0 to 70	PSOJ28
	M621100-17E1	1M x 1	17	5V ± 10%	140mA / 1mA	Separate I/O	0 to 70	PSOJ28
	M621100-20E1	1M x 1	20	5V ± 10%	120mA / 1mA	Separate I/O	0 to 70	PSOJ28
	M621100-25E1	1M x 1	25	5V ± 10%	120mA / 1mA	Separate I/O	0 to 70	PSOJ28
	M624256-15E1	256K x 4	15	5V ± 10%	140mA / 1mA	Common I/O	0 to 70	PSOJ28
	M624256-17E1	256K x 4	17	5V ± 10%	140mA / 1mA	Common I/O	0 to 70	PSOJ28
	M624256-20E1	256K x 4	20	5V ± 10%	120mA / 1mA	Common I/O	0 to 70	PSOJ28
	M624256-25E1	256K x 4	25	5V ± 10%	120mA / 1mA	Common I/O	0 to 70	PSOJ28
	M628128-15E1	128K x 8	15	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSOJ32
	M628128-17E1	128K x 8	17	5V ± 10%	140mA / 1mA	With Output Enable	0 to 70	PSOJ32

STATIC RAMs

FAST SRAM (cont'd)

Size	Part Number	Organisation	Speed (ns)	Vcc Range	Active/Stby	Features	Temperature Range (°C)	Package
1M	M628128-20E1	128K x 8	20	5V ± 10%	120mA / 1mA	With Output Enable	0 to 70	PSOJ32
	M628128-25E1	128K x 8	25	5V ± 10%	120mA / 1mA	With Output Enable	0 to 70	PSOJ32

CACHE MEMORIES

Organisation	Part Number	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
4K x 4	MK41S80X10	10	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24
	MK41S80X10/20	10	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24TR
	MK41S80N12	12	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP22
	MK41S80X12	12	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24
	MK41S80X12/20	12	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24TR
	MK41S80N15	15	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP22
	MK41S80X15	15	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24
	MK41S80X15/20	15	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24TR
	MK41S80N20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP22
	MK41S80X20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24
	MK41S80X20/20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24TR
	MK41H80N25	25	Fast TAGRAM	5V ± 10%	0 to 70	PSDIP22
	MK41S80N25	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP22
	MK41S80X25	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24
	MK41S80X25/20	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ24TR

CACHE MEMORIES (cont'd)

Organisation	Part Number	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
4K x 4	MK41H80N35	35	Fast TAGRAM	5V ± 10%	0 to 70	PSDIP22
8K x 8	MK48S80X15	15	Very Fast TAGRAM	5V ± 10%	0 to 70	PSJO28
	MK48S80X15/20	15	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28TR
	MK48S80N17	17	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP28
	MK48S80X17	17	Very Fast TAGRAM	5V ± 10%	0 to 70	PSJO28
	MK48S80X17/20	17	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28TR
	MK48S74N20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP28
	MK48S80N20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP28
	MK48S74X20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28
	MK48S74X20/20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28TR
	MK48S80X20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSJO28
	MK48S80X20/20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28TR
	MK48S74N25	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP28
	MK48S80N25	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP28
	MK48S74X25	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28
	MK48S74X25/20	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28TR
	MK48S80X25	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSJO28
	MK48S80X25/20	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28TR
	MK48S74N35	35	Very Fast TAGRAM	5V ± 10%	0 to 70	PSDIP28
	MK48S74X35	35	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28
	MK48S74X35/20	35	Very Fast TAGRAM	5V ± 10%	0 to 70	PSOJ28TR
32K x 9	MK62486Q19	19	Burst SRAM (BRAM)	5V ± 10%	0 to 70	PLCC44
	MK62940Q19	19	Burst SRAM (BRAM)	5V ± 10%	0 to 70	PLCC44
	MK62486Q24	24	Burst SRAM (BRAM)	5V ± 10%	0 to 70	PLCC44

CACHE MEMORIES (cont'd)

Organisation	Part Number	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
32K x 9	MK62940Q24	24	Burst SRAM (BRAM)	5V ± 10%	0 to 70	PLCC44
4K x10	MK45180Q17	17	SnoopTAG	5V ± 10%	0 to 70	PLCC68
	MK45180Q20	20	SnoopTAG	5V ± 10%	0 to 70	PLCC68
2K x 20	MK4202Q17	17	Very Fast TAGRAM	5V ± 10%	0 to 70	PLCC68
	MK4202Q20	20	Very Fast TAGRAM	5V ± 10%	0 to 70	PLCC68
	MK4202Q25	25	Very Fast TAGRAM	5V ± 10%	0 to 70	PLCC68

BiPORT FIFO

Organisation	Part Numer	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
1K x 5	MK4505MN25	25	Master FIFO	5V ± 10%	0 to 70	PSDIP24
	MK4505MN33	33	Master FIFO	5V ± 10%	0 to 70	PSDIP24
	MK4505MN50	50	Master FIFO	5V ± 10%	0 to 70	PSDIP24
	MK4505SN25	25	Slave FIFO	5V ± 10%	0 to 70	PSDIP20
	MK4505SN33	33	Slave FIFO	5V ± 10%	0 to 70	PSDIP20
	MK4505SN50	50	Slave FIFO	5V ± 10%	0 to 70	PSDIP20
512 x 9	MK45H01N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H01N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H01N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H01N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H01N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28

BiPORT FIFO (cont'd)

Organisation	Part Numer	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
512 x 9	MK45H11N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H11N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H11N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H11N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H11N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H01K25	25	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H01K35	35	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H01K50	50	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H01K65	65	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H01K12	120	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK4501N65	65	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4501N80	80	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4501N10	100	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4501N12	120	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4501N15	150	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4501N20	200	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4501K65	65	Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK4501K80	80	Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK4501K10	100	Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK4501K12	120	Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK4501K15	150	Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK4501K20	200	Fast FIFO	5V ± 10%	0 to 70	PLCC32
1K x 9	MK45H02N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H02N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28

BiPORT FIFO (cont'd)

Organisation	Part Numer	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
1K x 9	MK45H02N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H02N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H02N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H12N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H12N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H12N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H12N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H12N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H02K25	25	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H02K35	35	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H02K50	50	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H02K65	65	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H02K12	120	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
2K x 9	MK45H03N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H03N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H03N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H03N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H03N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H13N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H13N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H13N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H13N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H13N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H03K25	25	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32

BiPORT FIFO (cont'd)

Organisation	Part Numer	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
2K x 9	MK45H03K35	35	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H03K50	50	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H03K65	65	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H03K12	120	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK4503N65	65	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4503N80	80	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4503N10	100	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4503N12	120	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4503N15	150	Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK4503N20	200	Fast FIFO	5V ± 10%	0 to 70	PDIP28
4K x 9	MK45H04N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H04N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H04N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H04N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H04N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H14N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H14N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H14N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H14N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H14N12	120	Very Fast FIFO	5V ± 10%	0 to 70	PSDIP28
	MK45H04K25	25	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H04K35	35	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H04N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
	MK45H04K65	65	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32

BiPORT FIFO (cont'd)

Organisation	Part Numer	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
4K x 9	MK45H04K12	120	Very Fast FIFO	5V ± 10%	0 to 70	PLCC32
8K x 9	MK45H08N25	25	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H08N35	35	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H08N50	50	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H08N65	65	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28
	MK45H08N120	120	Very Fast FIFO	5V ± 10%	0 to 70	PDIP28

ZEROPOWER and TIMEKEEPER

Size	Part Number	Organisation	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
16K	MK48C02AN15	2K x 8	15	ZEROPOWER SRAM w/out Battery	5V +10/–5%	0 to 70	PDIP28
	MK48C02AN20	2K x 8	20	ZEROPOWER SRAM w/out Battery	5V +10/–5%	0 to 70	PDIP28
	MK48C02AN25	2K x 8	25	ZEROPOWER SRAM w/out Battery	5V +10/–5%	0 to 70	PDIP28
	MK48C02AK15	2K x 8	15	ZEROPOWER SRAM w/out Battery	5V +10/–5%	0 to 70	PLCC32
	MK48C02AK20	2K x 8	20	ZEROPOWER SRAM w/out Battery	5V +10/–5%	0 to 70	PLCC32
	MK48C02AK25	2K x 8	25	ZEROPOWER SRAM w/out Battery	5V +10/–5%	0 to 70	PLCC32
	MK48Z02B12	2K x 8	120	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48Z02B15	2K x 8	150	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48Z02B20	2K x 8	200	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48Z02B25	2K x 8	250	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48Z12B12	2K x 8	120	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP24

ZEROPOWER and TIMEKEEPER (cont'd)

Size	Part Number	Organisation	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
16K	MK48Z12B15	2K x 8	150	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP24
	MK48Z12B20	2K x 8	200	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP24
	MK48Z12B25	2K x 8	250	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP24
	MKI48Z02B15	2K x 8	150	ZEROPOWER SRAM	5V +10/–5%	–40 to 85	PHDIP24
	MKI48Z02B20	2K x 8	200	ZEROPOWER SRAM	5V +10/–5%	–40 to 85	PHDIP24
	MKI48Z02B25	2K x 8	250	ZEROPOWER SRAM	5V +10/–5%	–40 to 85	PHDIP24
	MKI48Z12B15	2K x 8	150	ZEROPOWER SRAM	5V ± 10%	–40 to 85	PHDIP24
	MKI48Z12B20	2K x 8	200	ZEROPOWER SRAM	5V ± 10%	–40 to 85	PHDIP24
	MKI48Z12B25	2K x 8	250	ZEROPOWER SRAM	5V ± 10%	–40 to 85	PHDIP24
64K	MK48Z08B70	8K x 8	70	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48Z08B10	8K x 8	100	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48Z09B10	8K x 8	100	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48Z18B10	8K x 8	100	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP28
	MK48Z19B10	8K x 8	100	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP28
	MKI48Z18B10	8K x 8	100	ZEROPOWER SRAM	5V ± 10%	–40 to 85	PHDIP28
256K	MK48Z30B70	32K x 8	70	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48Z30B12	32K x 8	120	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48Z30YB70	32K x 8	70	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP28
	MK48Z30YB12	32K x 8	120	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP28
	MK48Z32B70	32K x 8	70	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48Z32B12	32K x 8	120	ZEROPOWER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48Z32YB70	32K x 8	70	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP28
	MK48Z32YB12	32K x 8	120	ZEROPOWER SRAM	5V ± 10%	0 to 70	PHDIP28

ZEROPOWER and TIMEKEEPER (cont'd)

Size	Part Number	Organisation	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
1M	M48Z128-85PM1	128K x 8	85	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMDIP32
	M48Z128-120PM1	128K x 8	120	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMDIP32
	M48Z128Y-85PM1	128K x 8	85	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMDIP32
	M48Z128Y-120PM1	128K x 8	120	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMDIP32
2M	M46Z128-85PM1	128K x 16	85	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMDIP40
	M46Z128-120PM1	128K x 16	120	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMDIP40
	M46Z128Y-85PM1	128K x 16	85	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMDIP40
	M46Z128Y-120PM1	128K x 16	120	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMDIP40
	M48Z256-85PL1	256K x 8	85	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMLDIP32
	M48Z256-120PL1	256K x 8	120	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMLDIP32
	M48Z256Y-85PL1	256K x 8	85	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMLDIP32
	M48Z256Y-120PL1	256K x 8	120	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMLDIP32
4M	M46Z256-85PM1	256K x 16	85	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMDIP40
	M46Z256-120PM1	256K x 16	120	ZEROPOWER SRAM Module	5V +10/–5%	0 to 70	PMDIP40
	M46Z256Y-85PM1	256K x 16	85	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMDIP40
	M46Z256Y-120PM1	256K x 16	120	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMDIP40
	M48Z512-85PL1	512K x 8	85	ZEROPOWER SRAM Module	5V +10/ –5%	0 to 70	PMLDIP32
	M48Z512-120PL1	512K x 8	120	ZEROPOWER SRAM Module	5V +10/ –5%	0 to 70	PMLDIP32
	M48Z512Y-85PL1	512K x 8	85	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMLDIP32
	M48Z512Y-120PL1	512K x 8	120	ZEROPOWER SRAM Module	5V ± 10%	0 to 70	PMLDIP32
512	MK41T56N00	64 x 8	–	I^{2}C Bus, Real Time Clock	5V ± 10%	0 to 70	PSDIP8
	MK48T85Q24	64 x 8	–	PC Clock, Addr/Data MPX	5V ± 10%	0 to 70	PLCC28
	MK48T87B24	64 x 8	–	PC Clock, Addr/Data MPX	5V ± 10%	0 to 70	PHDIP24
	MK48T87AB24	64 x 8	–	PC Clock, Addr/Data MPX	5V ± 10%	0 to 70	PHDIP24

ZEROPOWER and TIMEKEEPER (cont'd)

Size	Part Number	Organisation	Speed (ns)	Function	Vcc Range	Temperature Range (°C)	Package
16K	MK48T02B12	2K x 8	120	TIMEKEEPER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48T02B15	2K x 8	150	TIMEKEEPER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48T02B20	2K x 8	200	TIMEKEEPER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48T02B25	2K x 8	250	TIMEKEEPER SRAM	5V +10/–5%	0 to 70	PHDIP24
	MK48T12B15	2K x 8	150	TIMEKEEPER SRAM	5V ± 10%	0 to 70	PHDIP24
	MK48T12B20	2K x 8	200	TIMEKEEPER SRAM	5V ± 10%	0 to 70	PHDIP24
	MK48T12B25	2K x 8	250	TIMEKEEPER SRAM	5V ± 10%	0 to 70	PHDIP24
64K	MK48T08B10	8K x 8	100	TIMEKEEPER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48T08B15	8K x 8	150	TIMEKEEPER SRAM	5V +10/–5%	0 to 70	PHDIP28
	MK48T18B10	8K x 8	100	TIMEKEEPER SRAM	5V ± 10%	0 to 70	PHDIP28
	MK48T18B15	8K x 8	150	TIMEKEEPER SRAM	5V ± 10%	0 to 70	PHDIP28
16K	M48C1001-45K1	2K x 8	45	Processor Manager	5V ± 10%	0 to 70	PLCC44
	M48C1002-45K1	2K x 8	45	Processor Manager	5V ± 10%	0 to 70	PLCC28

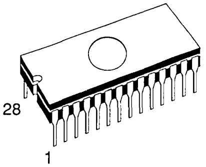
CMOS EPROM

SGS-THOMSON
MICROELECTRONICS

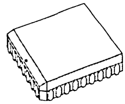
M27C64A

CMOS 64K (8K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 150ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.5V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- HIGH SPEED PROGRAMMING (less than 1 minute)



FDIP28W (F)



PLCC32 (C)

DESCRIPTION

The M27C64A is a high speed 65,536 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 8,192 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C64A is offered in Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

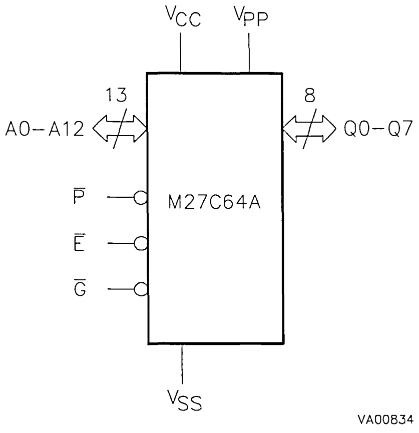
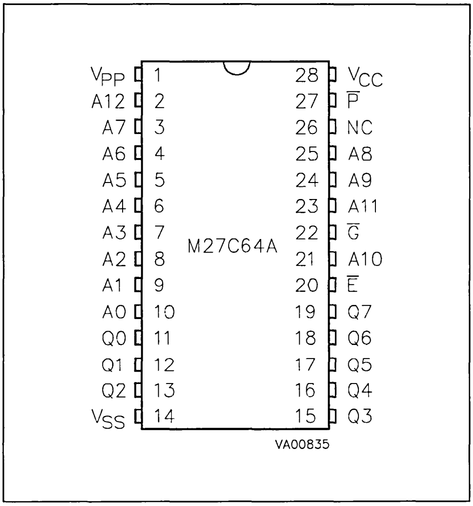
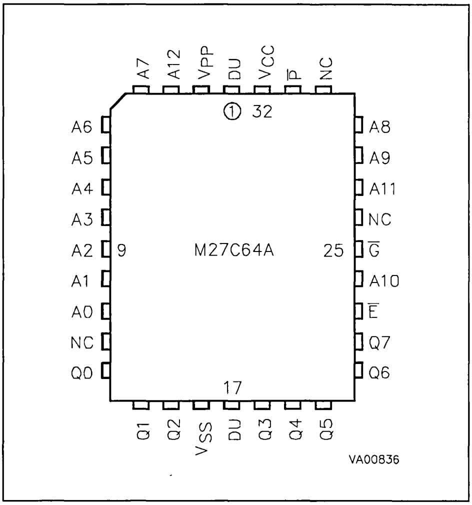


Figure 2A. DIP Pin Connections


VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
VSS 14
28 VCC
27 P̄
26 NC
25 A8
24 A9
23 A11
22 Ḡ
21 A10
20 Ē
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3
M27C64A
VA00835

Warning: NC = No Connection

Figure 2B. LCC Pin Connections


A7
A12
VPP
DU
VCC
P̄
NC
① 32
A6
A5
A4
A3
A2
A1
A0
NC
Q0
9
M27C64A
25
A8
A9
A11
NC
Ḡ
A10
Ē
Q7
Q6
17
Q1
Q2
VSS
DU
Q3
Q4
Q5
VA00836

Warning: NC = No Connection, DU = Don't Use

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature.	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The modes of operation of the M27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs.Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C64A has a standby mode which reduces the active current from 30mA to 100µA. The

DEVICE OPERATION (cont'd)

M27C64A is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C64A is in the programming mode when V_{PP} input is at 12.5V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	1	0	0	1	1	0	1	1	9Bh
Device Code	V_{IH}	0	0	0	0	0	1	0	0	08h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

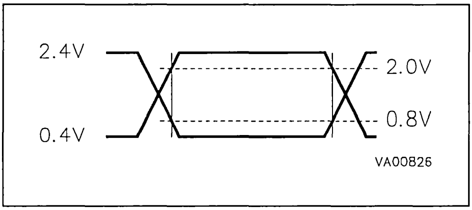

2.4V
0.4V
2.0V
0.8V
VA00826

Figure 4. AC Testing Load Circuit

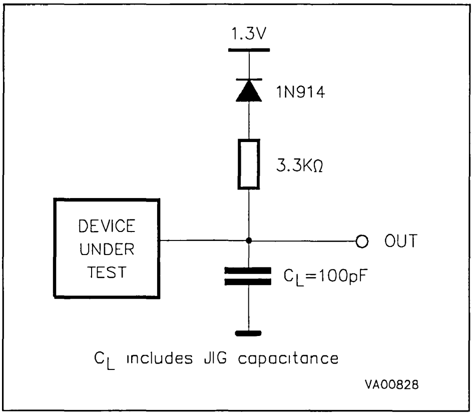

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L=100pF
C_L includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Figure 5. Read Mode AC Waveforms

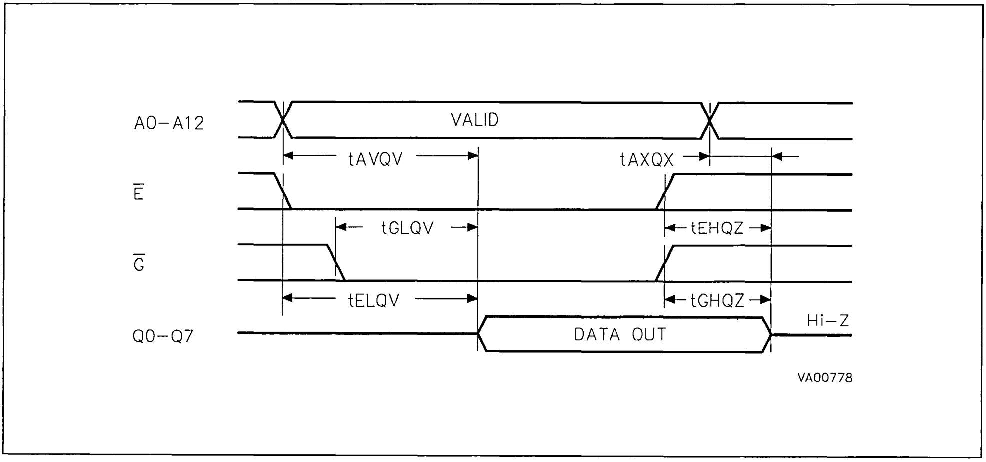

A0–A12
VALID
tAVQV
tAXQX
E
tGLQV
tEHQZ
G
tELQV
tGHQZ
Q0–Q7
DATA OUT
Hi–Z
VA00778

Table 6. Read Mode DC Characteristics [(1)]
(T$_A$ = 0 to 70 °C or –40 to 85 °C: V$_{CC}$ = 5V ± 10%; V$_{PP}$ = V$_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
V_{OH}	Output High Voltage TTL	$I_{OH} = -400\mu A$	2.4		V
	Output High Voltage CMOS	$I_{OH} = -100\mu A$	$V_{CC} - 0.7V$		V

Note: 1. V$_{CC}$ must be applied simultaneously with or before V$_{PP}$ and removed simultaneously with or after V$_{PP}$

Table 7. Read Mode AC Characteristics [(1)]
(T$_A$ = 0 to 70 °C or –40 to 85 °C: V$_{CC}$ = 5V ± 10%; V$_{PP}$ = V$_{CC}$)

Symbol	Alt	Parameter	Test Condition	M27C64A								Unit
				-15		-20		-25		-30		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		65		70		100		120	ns
t_{EHQZ} [(2)]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	0	60	0	105	ns
t_{GHQZ} [(2)]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	0	60	0	105	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1 V$_{CC}$ must be applied simultaneously with or before V$_{PP}$ and removed simultaneously with or after V$_{PP}$
2. This parameter is sampled only and not tested 100%

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			30	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)		0.95	1 05	ms
		Program Pulse Width (Over Program)		2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

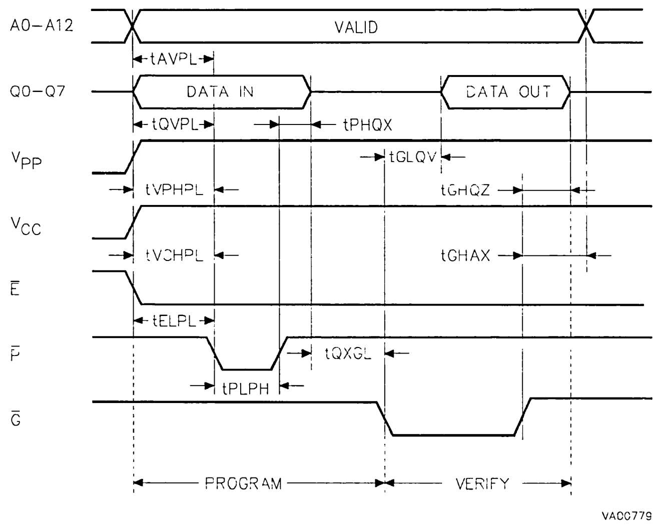
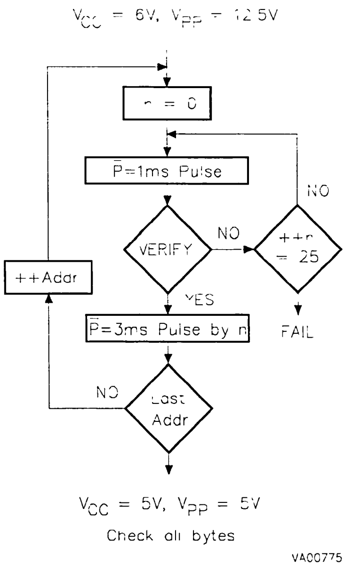

A0–A12
VALID
tAVPL
Q0–Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00779

Figure 7. Programming Flowchart


VCC = 6V, VPP = 12.5V
n = 0
P=1ms Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
P=3ms Pulse by n
NO
Last Addr
VCC = 5V, VPP = 5V
Check all bytes
VA00775

High Speed Programming

The high speed programming algorithm, described in the flowchart, rapidly programs the M27C64A using an efficient and reliable method, particularly suited to the production programming environment. An individual device will take around 1 minute to program.

Program Inhibit

Programming of multiple M27C64A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C64A may be common. A TTL low level pulse applied to a M27C64A $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.5V, will program that M27C64A. A high level $\overline{E}$ input inhibits the other M27C64A from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.5V and V_{CC} at 6V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to

DEVICE OPERATION (cont'd)

automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C64A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C64A, with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C64A, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C64A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C64A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C64A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C64A window to prevent unintentional erasure. The recommended erasure procedure for the M27C64A is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C64A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C64A -15 F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-15	150 ns	blank	± 10%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-20	200 ns			C	PLCC32	6	–40 to 85 °C	TR	Tape & Reel
-25	250 ns								
-30	300 ns								

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

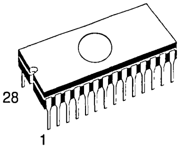
For further information on any aspect of this device, please contact our Sales Office nearest to you.

M27C128A

CMOS 128K (16K x 8) UV EPROM

ADVANCE DATA

- VERY FAST ACCESS TIME: 120ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 2sec. (PRESTO II ALGORITHM)



FDIP28W (F)

DESCRIPTION

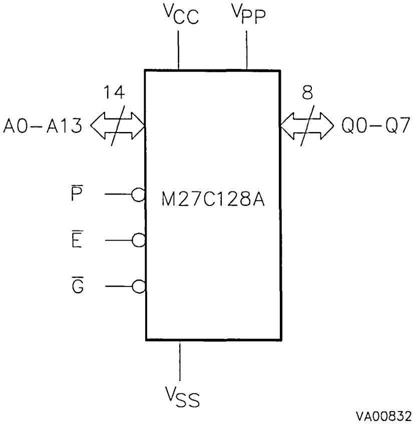
The M27C128A is a high speed 131,072 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 16,384 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A13	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



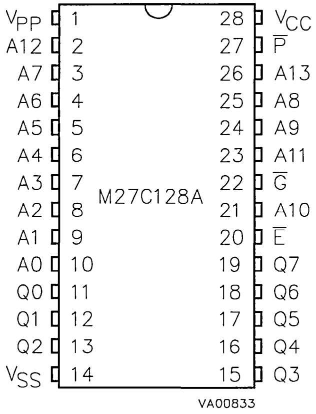
This is advance information on a new product now in development or undergoing evaluation Details are subject to change without notice

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. DIP Pin Connections



DEVICE OPERATION

The modes of operation of the M27C128A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C128A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C128A has a standby mode which reduces the active current from 30mA to 100µA. The M27C128A is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system

DEVICE OPERATION (cont'd)

control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C128A is in the programming mode when V_{pp} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 2 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0 5V.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	0	1	0	0Ah

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

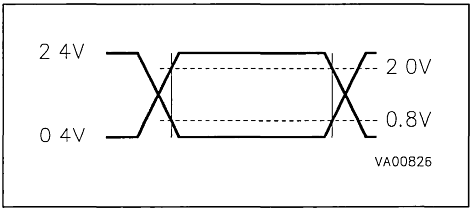

2.4V
0.4V
2.0V
0.8V
VA00826

Figure 4. AC Testing Load Circuit

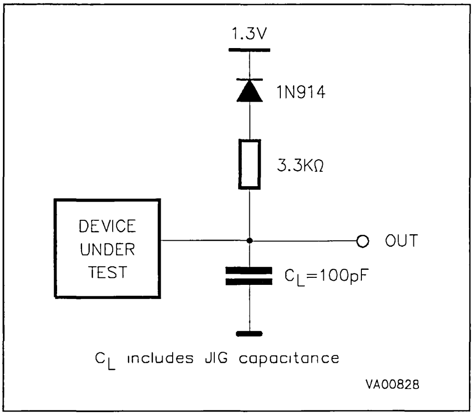

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
CL includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Figure 5. Read Mode AC Waveforms

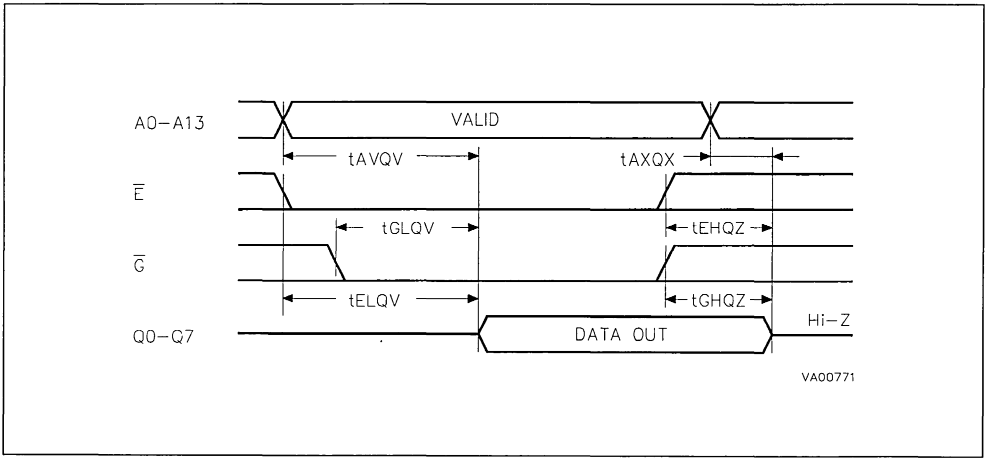

A0–A13
VALID
tAVQV
tAXQX
E̅
tGLQV
tEHQZ
G̅
tELQV
tGHQZ
Q0–Q7
DATA OUT
Hi–Z
VA00771

Table 6. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C128A						Unit
				-12		-15		-20		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		75		80	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	35	0	35	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	35	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			30	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

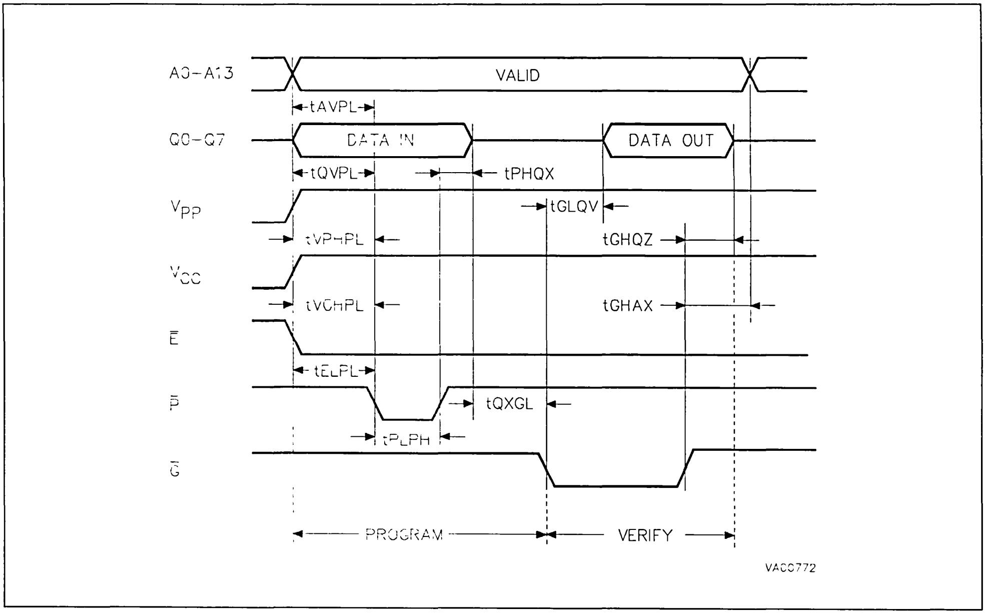
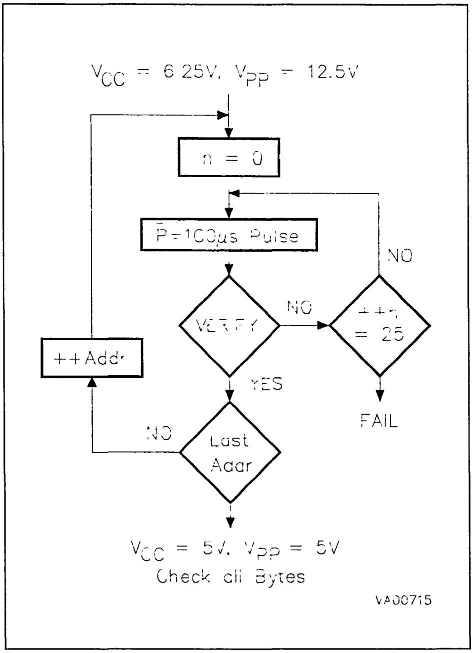

A0-A13
VALID
tAVPL
Q0-Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00772

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
P=100μs Pulse
VERIFY
NO
++n = 25
NO
YES
FAIL
++Addr
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00715

Program Inhibit

Programming of multiple M27C128A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C128A may be common. A TTL low level pulse applied to a M27C128A $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C128A. A high level $\overline{E}$ input inhibits the other M27C128A from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C128A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C128A, with

DEVICE OPERATION (cont'd)

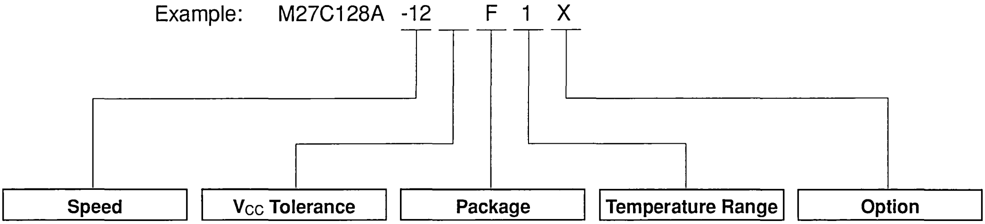
$V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C128A, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C128A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C128A window to prevent unintentional erasure. The recommended erasure procedure for the M27C128A is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C128A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter

ORDERING INFORMATION



Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-12	120 ns	blank	± 10%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-15	150 ns					6	–40 to 85 °C		
-20	200 ns								

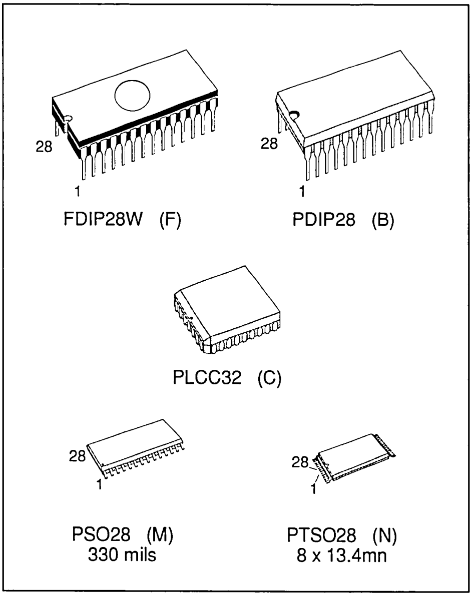
For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M27C256B

CMOS 256K (32K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30 mA
  - Standby Current 100 µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 3sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C256B is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems. It is organized as 32,768 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C256B is offered in Plastic Dual-in-Line, Plastic Leaded Chip Carrier, Plastic Small Outline and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

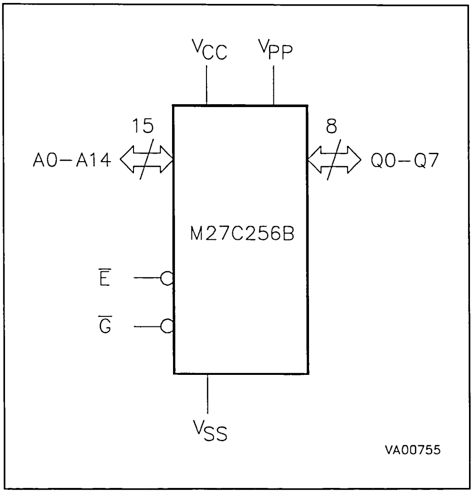


Table 2. Absoulte Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6 grade 7	0 to 70 –40 to 125 –40 to 85 –40 to 105	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13 5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2A. DIP Pin Connections

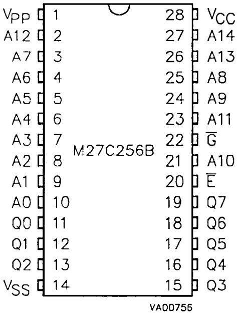

VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
VSS 14
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 G̅
21 A10
20 E̅
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3
M27C256B
VA00756

Figure 2B. SO Pin Connections

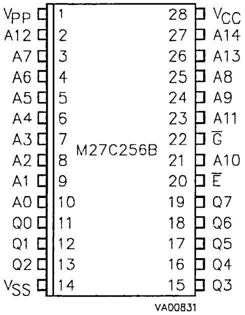

VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
VSS 14
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 G̅
21 A10
20 E̅
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3
M27C256B
VA00831

Figure 2C. LCC Pin Connections

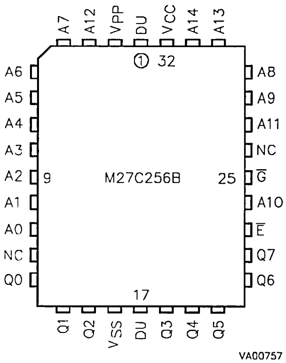
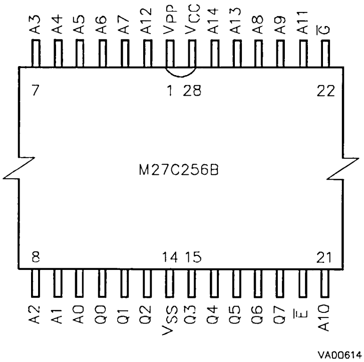

A7
A12
VPP
DU
VCC
A14
A13
① 32
A6
A5
A4
A3
A2 9
A1
A0
NC
Q0
A8
A9
A11
NC
25 G̅
A10
E̅
Q7
Q6
M27C256B
17
Q1
Q2
VSS
DU
Q3
Q4
Q5
VA00757

Figure 2D. PTSO Pin Connections


A3
A4
A5
A6
A7
A12
VPP
VCC
A14
A13
A8
A9
A11
G̅
7
1 28
22
M27C256B
8
14 15
21
A2
A1
A0
Q0
Q1
Q2
VSS
Q3
Q4
Q5
Q6
Q7
E̅
A10
VA00614

Warning: NC = No Connection, DU = Dont't Use.

DEVICE OPERATION

The modes of operation of the M27C256B are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C256B has a standby mode which reduces the active current from 30 mA to 100µA (or 200µA, see Read Mode DC Characteristics Table for details). The M27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Notes. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0 5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	1	0	1	8Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

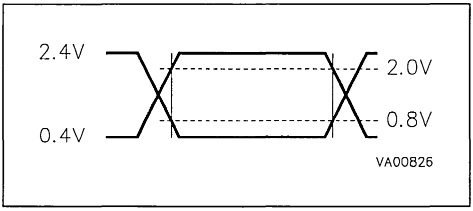


Figure 4. AC Testing Load Circuit

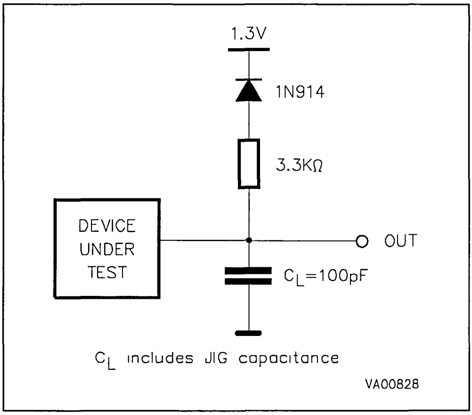


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}(2)	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. For speeds -80, -90 and Option "L" only For other types the maximum I_{CC2} is 200µA

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C256B								Unit
				-80		-90		-10		-12		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		90		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		90		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C256B						Unit
				-15		-20		-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		65		70		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested

Figure 5. Read Mode AC Waveforms

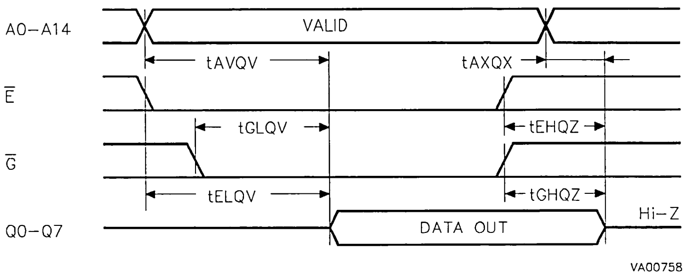


Table 8. Programming Mode DC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 9. Programming Mode AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

DEVICE OPERATION (cont'd)

between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C256B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C256B is in the programming mode when V_{PP} input is at 12.75 V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

Figure 6. Programming and Verify Modes AC Waveforms

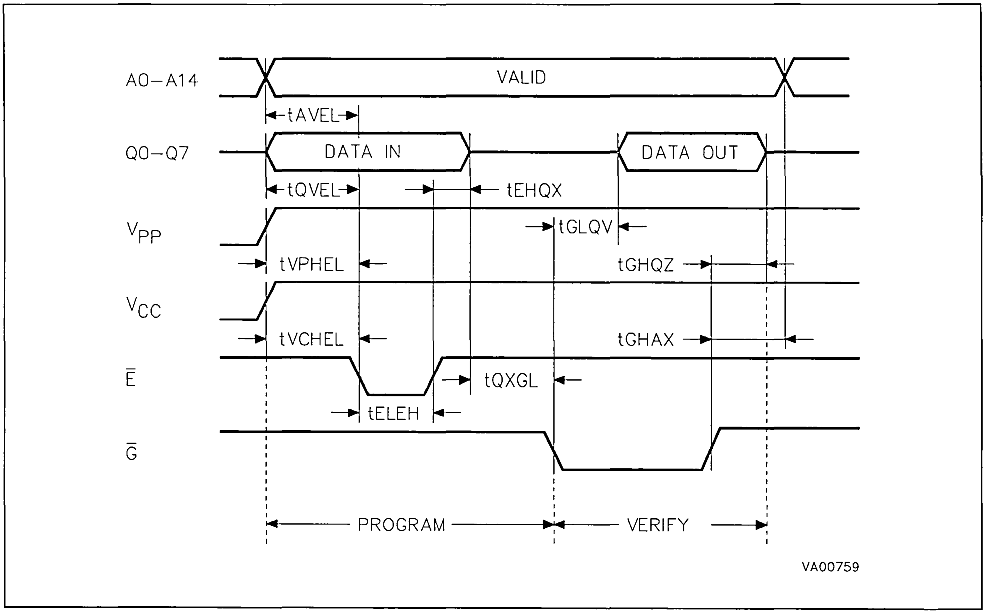
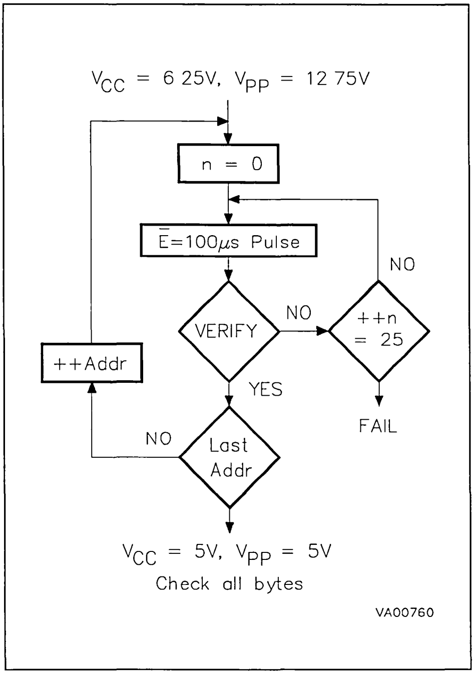

A0–A14
VALID
tAVEL
Q0–Q7
DATA IN
DATA OUT
tQVEL
tEHQX
VPP
tGLQV
tVPHEL
tGHQZ
VCC
tVCHEL
tGHAX
E̅
tQXGL
tELEH
G̅
PROGRAM
VERIFY
VA00759

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.75V
n = 0
E̅=100µs Pulse
VERIFY
NO
++n = 25
NO
YES
FAIL
++Addr
NO
Last Addr
VCC = 5V, VPP = 5V
Check all bytes
VA00760

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of less than 3 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C256Bs in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C256B may be common. A TTL low level pulse applied to a M27C256B's $\overline{E}$ input, with V_{PP} at 12.75 V, will program that M27C256B. A high level $\overline{E}$ input inhibits the other M27C256Bs from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C256B. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C256B, with $V_{CC} = V_{PP} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C256B, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C256B is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C256B in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C256B is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C256B window to prevent unintentional erasure. The recommended erasure procedure for the M27C256B is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M27C256B should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C256B -80 X F 1 L

Speed	
-80	80 ns
-90	90 ns
-10	100 ns
-12	120 ns
-15	150 ns
-20	200 ns
-25	250 ns

V_{CC} Tolerance	
X	± 5%
blank	± 10%

Package	
F	FDIP28W
B	PDIP28
C	PLCC32
M	PSO28 330 mils
N	PTSO28 8 x 13.4mm

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C
7	–40 to 105 °C

Option	
L	Low Power
X	Additional Burn-in
TR	Tape & Reel

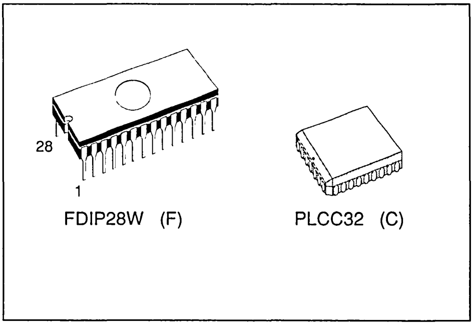
For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M87C257

ADDRESS LATCHED
CMOS 256K (32K x 8) UV EPROM and OTP ROM

- INTEGRATED ADDRESS LATCH
- VERY FAST ACCESS TIME: 100ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 200µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 3sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M87C257 is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM. The M87C257 incorporates latches for all address inputs to minimize chip count, reduce cost, and simplify the design of multiplexed bus systems.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M87C257 is offered in Plastic Leaded Chip Carrier, package.

Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{AS}V_{PP}$	Address Strobe / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

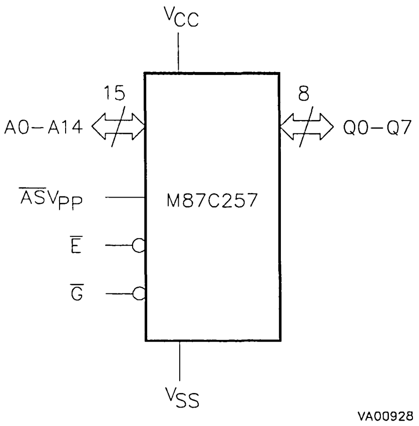


Figure 2A. DIP Pin Connections

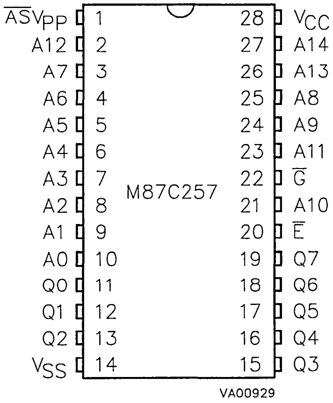
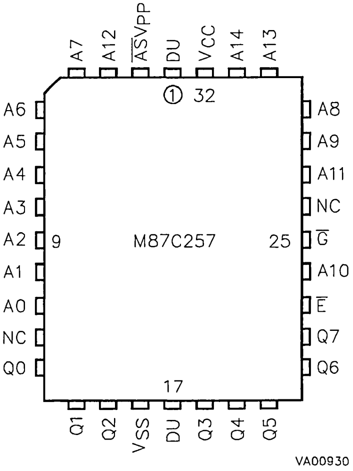

$\overline{AS}V_{PP}$ 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
V_{SS} 14
28 V_{CC}
27 A14
26 A13
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{E}$
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3
M87C257
VA00929

Figure 2C. LCC Pin Connections


A7
A12
$\overline{AS}$VPP
DU
VCC
A14
A13
① 32
A6
A5
A4
A3
A2
A1
A0
NC
Q0
9
M87C257
25
A8
A9
A11
NC
$\overline{G}$
A10
$\overline{E}$
Q7
Q6
17
Q1
Q2
VSS
DU
Q3
Q4
Q5
VA00930

Warning: NC = No Connection, DU = Dont't Use.

Table 2. Absoulte Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6 grade 7	0 to 70 –40 to 125 –40 to 85 –40 to 105	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DEVICE OPERATION

The modes of operation of the M87C257 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M87C257 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should

DEVICE OPERATION (cont'd)

be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable ($\overline{AS}$ = V_{IH}) or latched ($\overline{AS}$ = V_{IL}), the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

The M87C257 reduces the hardware interface in multiplexed address-data bus systems. The processor multiplexed bus (AD0-AD7) may be tied to the M87C257's address and data pins. No separate address latch is needed because the M87C257 latches all address inputs when $\overline{AS}$ is low.

Standby Mode

The M87C257 has a standby mode which reduces the active current from 30mA to 200µA. The M87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	$\overline{AS}V_{PP}$	Q0 - Q7
Read (Latched Address)	V_{IL}	V_{IL}	X	V_{IL}	Data Out
Read (Applied Address)	V_{IL}	V_{IL}	X	V_{IH}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{IL}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

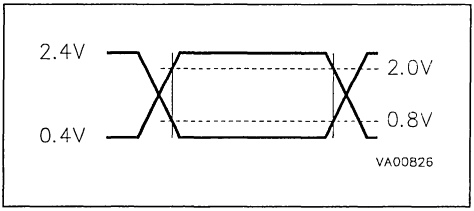

2.4V
0.4V
2.0V
0.8V
VA00826

Figure 4. AC Testing Load Circuit

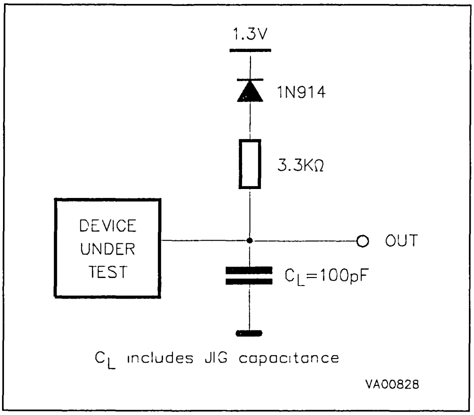

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L=100pF
C_L includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Figure 5. Read Mode AC Waveforms

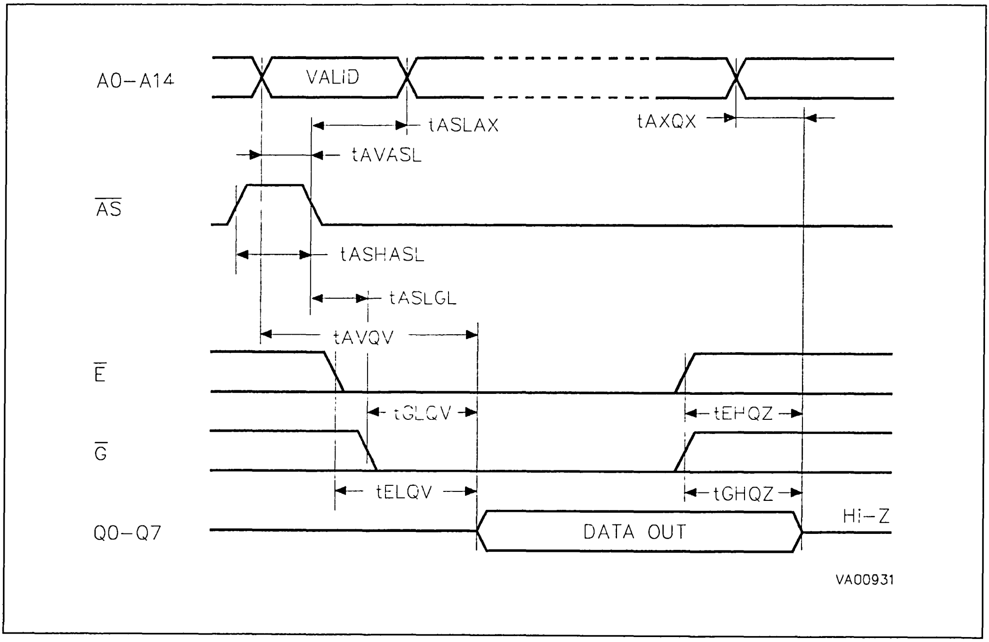

A0–A14
VALID
tASLAX
tAXQX
tAVASL
AS
tASHASL
tASLGL
tAVQV
E
tGLQV
tEHQZ
G
tELQV
tGHQZ
Q0–Q7
DATA OUT
Hi–Z
VA00931

Table 6. Read Mode DC Characteristics [1]

(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		30	mA
I_{CC1} [2]	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2} [2]	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		200	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	V_{CC} – 0.8V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Stable Inputs

Table 7. Read Mode AC Characteristics [1]

(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M87C257								Unit
				-10		-12		-15		-20		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120		150		200	ns
t_{AVASL}	t_{AL}	Address Valid to Address Strobe Low		7		7		7		15		ns
t_{ASHASL}	t_{LL}	Address Strobe High to Address Strobe Low		35		35		35		50		ns
t_{ASLAX}	t_{LA}	Address Strobe Low to Address Transition		20		20		20		30		ns
t_{ASLGL}	t_{LOE}	Address Strobe Low to Output Enable Low		20		20		20		30		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		60		70	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	40	0	40	0	40	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	40	0	40	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	V_{CC} -0.8V		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 6. Programming and Verify Modes AC Waveforms

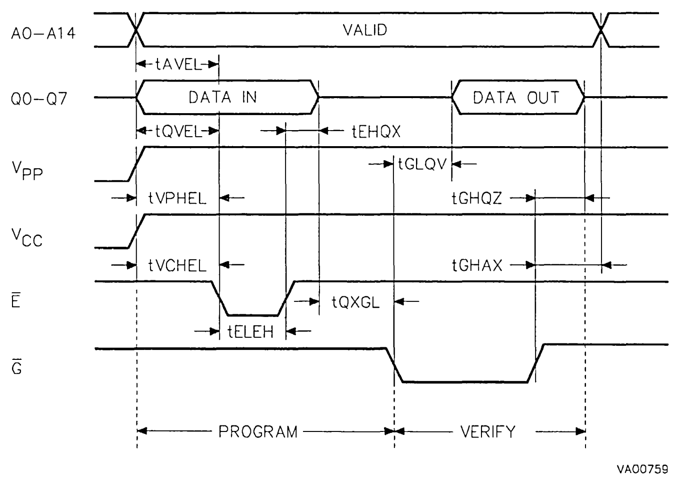
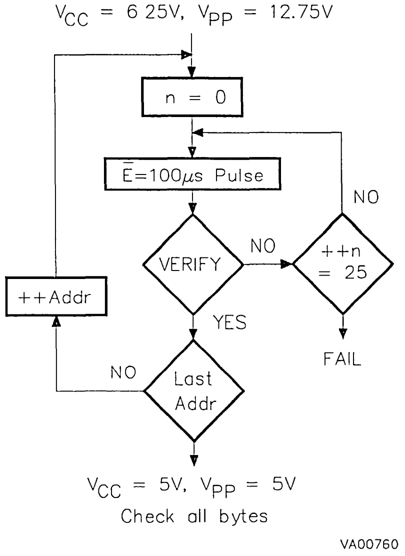

A0–A14
VALID
tAVEL
Q0–Q7
DATA IN
DATA OUT
tQVEL
tEHQX
VPP
tGLQV
tVPHEL
tGHQZ
VCC
tVCHEL
tGHAX
E̅
tQXGL
tELEH
G̅
PROGRAM
VERIFY
VA00759

Figure 7. Programming Flowchart


VCC = 6 25V, VPP = 12.75V
n = 0
E̅=100µs Pulse
VERIFY
NO
++n = 25
NO
YES
FAIL
++Addr
NO
Last Addr
VCC = 5V, VPP = 5V
Check all bytes
VA00760

DEVICE OPERATION (cont'd)

capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M87C257 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M87C257 is in the programming mode when V_{PP} input is at 12.75 V, and E̅ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of less than 3 seconds. Programming with PRESTO II involves the application of a sequence of 100μs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M87C257s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M87C257 may be common. A TTL low level pulse applied to a M87C257's $\overline{E}$ input, with V_{PP} at 12.75 V, will program that M87C257. A high level $\overline{E}$ input inhibits the other M87C257s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

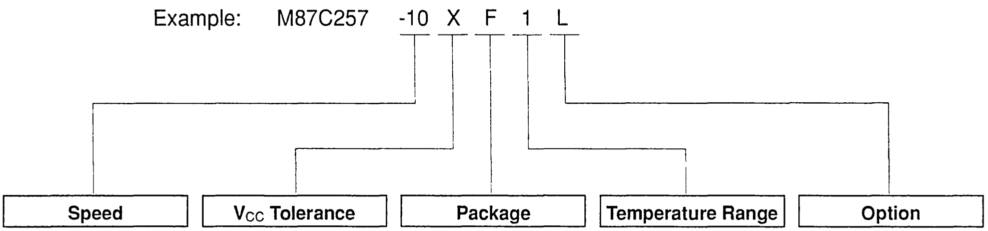
Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M87C257. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M87C257, with $V_{CC} = V_{PP} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. When $A9 = V_{ID}$, $\overline{AS}$ need not be toggled to latch each identifier address. For the SGS-THOMSON M87C257, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M87C257 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M87C257 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M87C257 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M87C257 window to prevent unintentional erasure. The recommended erasure procedure for the M87C257 is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M87C257 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION



Example: M87C257 -10 X F 1 L

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-10	100 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	L	Low Power
-12	120 ns	blank	± 10%	C	PLCC32	3	–40 to 125 °C	X	Additional Burn-in
-15	150 ns					6	–40 to 85 °C	TR	Tape & Reel
-20	200 ns					7	–40 to 105 °C		

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

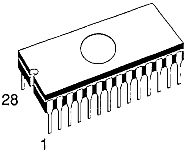
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

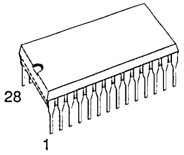
M27C512

CMOS 512K (64K x 8) UV EPROM and OTP ROM

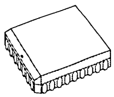
- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE WITH HIGH SPEED MICRO-PROCESSORS, ZERO WAIT STATE
- LOW POWER “CMOS” CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 6sec. (PRESTO IIB ALGORITHM)



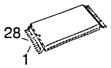
FDIP28W (F)



PDIP28 (B)



PLCC32 (C)



PTSO28 (N)
8 x 13.4mm

DESCRIPTION

The M27C512 is a high speed 524,288 bit UV erasable and electrically programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 65,536 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C512 is offered in Plastic Dual-in-Line, Plastic Thin Small Outline and Plastic Leaded Chip Carrier packages.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

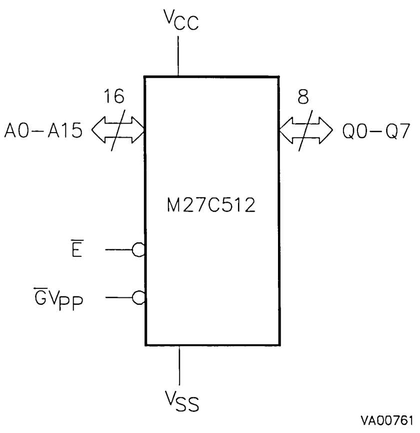


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6 grade 3	0 to 70 –40 to 85 –40 to 125	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2A. DIP Pin Connections

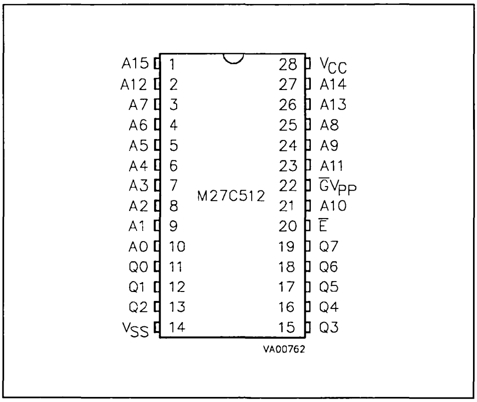
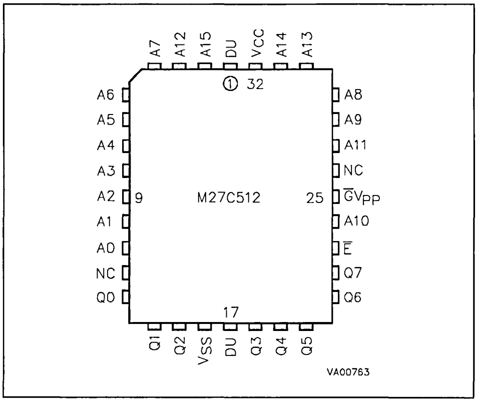
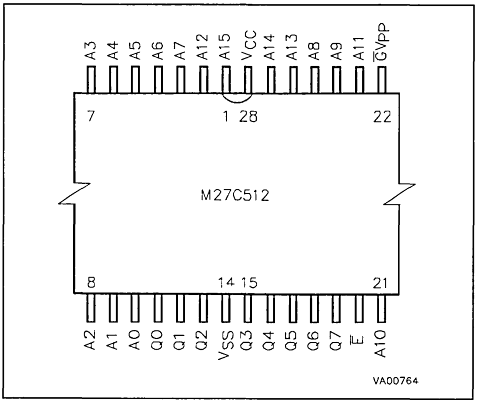

A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
VSS 14
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 GVPP
21 A10
20 E
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3
M27C512
VA00762

Figure 2B. LCC Pin Connections


A7
A12
A15
DU
VCC
A14
A13
① 32
A6
A5
A4
A3
A2 9
A1
A0
NC
Q0
A8
A9
A11
NC
25 GVPP
A10
E
Q7
Q6
M27C512
17
Q1
Q2
VSS
DU
Q3
Q4
Q5
VA00763

Warning: NC = No Connection, DU = Don't Use

Figure 2C. PTSO Pin Connections


A3
A4
A5
A6
A7
A12
A15
VCC
A14
A13
A8
A9
A11
GVPP
7
1 28
22
M27C512
8
14 15
21
A2
A1
A0
Q0
Q1
Q2
VSS
Q3
Q4
Q5
Q6
Q7
E
A10
VA00764

DEVICE OPERATION

The modes of operations of the M27C512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data

DEVICE OPERATION (cont'd)

is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C512 has a standby mode which reduces the active current from 30mA to 100µA (or 200µA, see Read Mode DC Characteristics Table for details). The M27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C512 is in the programming mode when V_{PP} input is at 12.75V and

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

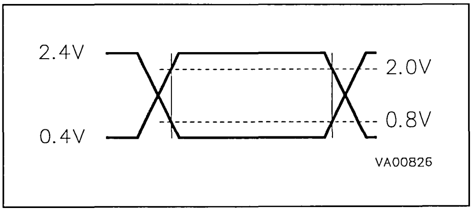


Figure 4. AC Testing Load Circuit

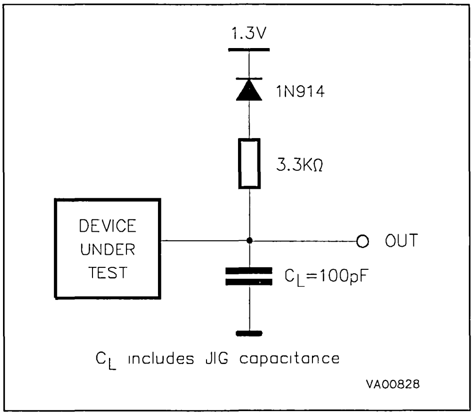


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2 This parameter is sampled only and not tested 100%.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2} (2)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. For speeds -80, -90, -10 and Option "L" only. For other types the maximum I_{CC2} is 200µA.

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C512								Unit
				-80		-90		-10		-12		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		90		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		90		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		40		40		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C512						Unit
				-15		-20		-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		70		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes. 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2 This parameter is sampled only and not 100% tested.

Figure 5. Read Mode AC Waveforms

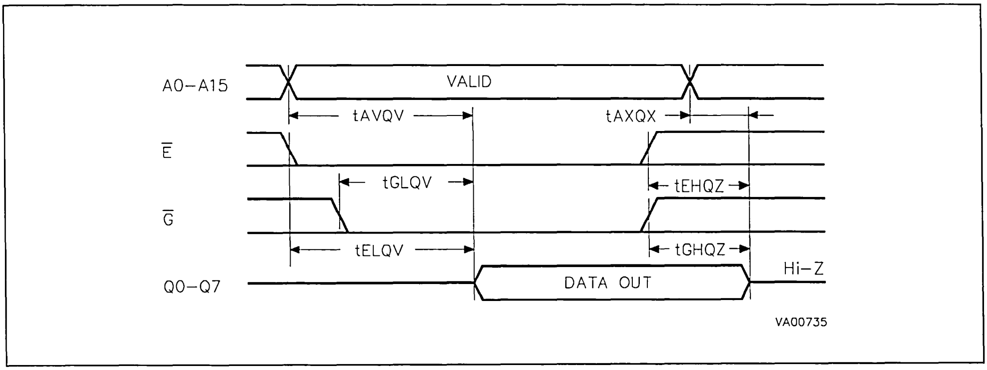


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested.

Figure 6. MARGIN MODE AC Waveforms

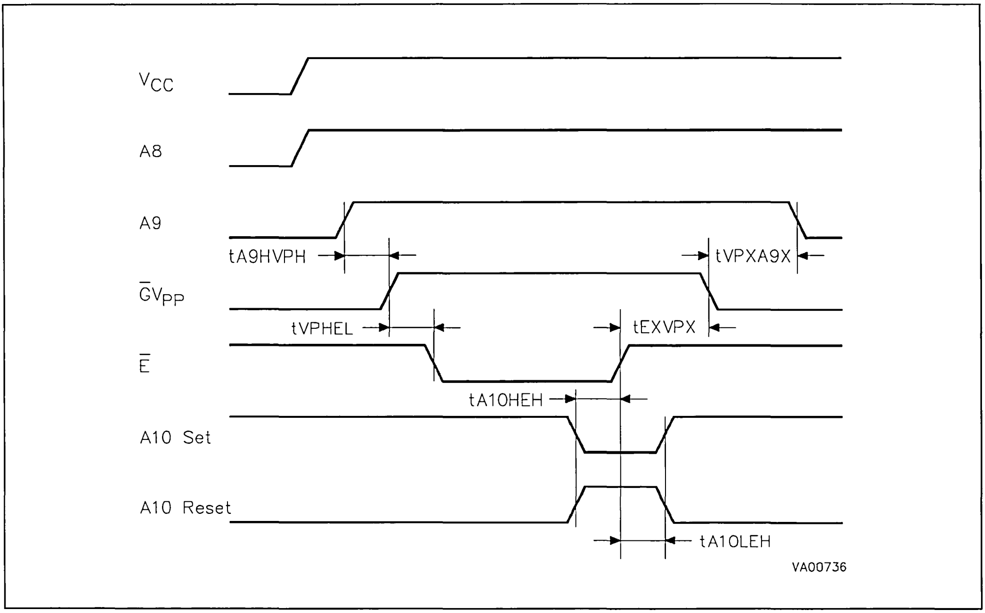

V_{CC}
A8
A9
tA9HVPH
tVPXA9X
$\overline{G}V_{PP}$
tVPHEL
tEXVPX
$\overline{E}$
tA10HEH
A10 Set
A10 Reset
tA10LEH
VA00736

Figure 7. Programming and Verify Modes AC Waveforms

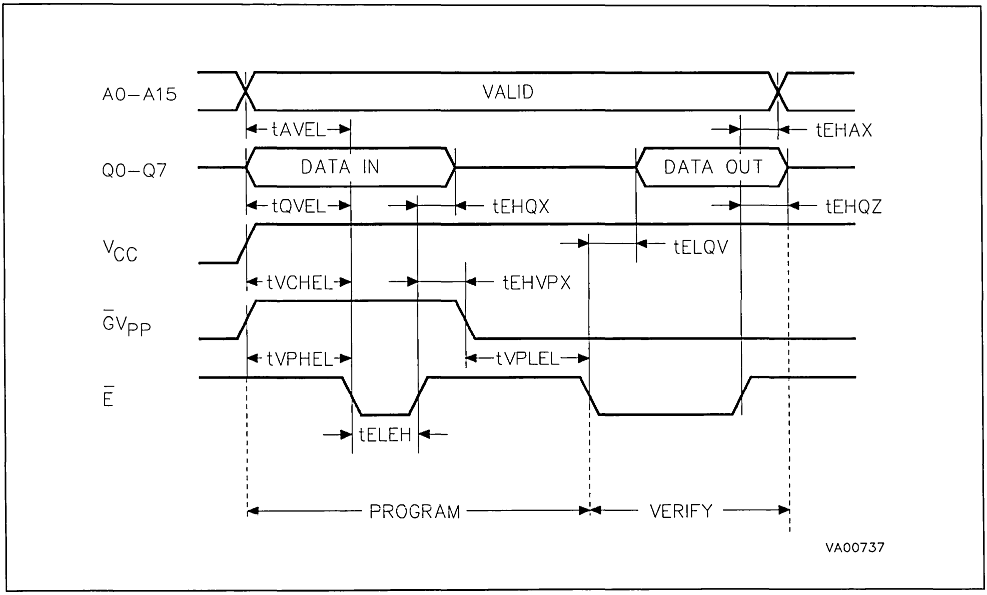
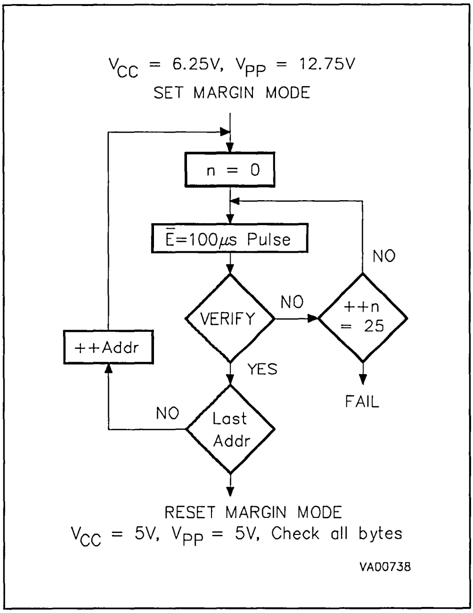

A0–A15
VALID
tAVEL
tEHAX
Q0–Q7
DATA IN
DATA OUT
tQVEL
tEHQX
tEHQZ
V_{CC}
tELQV
tVCHEL
tEHVPX
$\overline{G}V_{PP}$
tVPHEL
tVPLEL
$\overline{E}$
tELEH
PROGRAM
VERIFY
VA00737

Figure 8. Programming Flowchart



DEVICE OPERATION (cont'd)

E̅ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

The M27C512 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 7 seconds. This can be achieved with SGS-THOMSON M27C512 due to several design innovations described in the M27C512 datasheet to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27C512s in parallel with different data is also easily accomplished. Except for E̅, all like inputs including G̅V_{PP} of the parallel M27C512 may be common. A TTL low level pulse applied to a M27C512's E̅ input, with V_{PP} at 12.75V, will program that M27C512. A high level E̅ input inhibits the other M27C512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with G̅ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of E̅.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C512, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range.

ERASURE OPERATION (cont'd)

Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C512 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C512 window to prevent unintentional erasure. The recommended erasure procedure for the M27C512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C512 -80 X F 1 L

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	L	Low Power
-90	90 ns	blank	± 10%	B	PDIP28	3	–40 to 125 °C	X	Additional Burn-in
-10	100 ns			C	PLCC32	6	–40 to 85 °C	TR	Tape & Reel
-12	120 ns			N	PTSO28 8 x 13.4mm				
-15	150 ns								
-20	200 ns								
-25	250 ns								

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

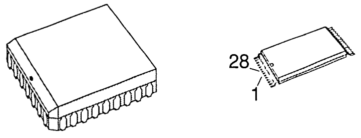
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M27V512

LOW VOLTAGE CMOS 512K (64K x 8) OTP ROM

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V ($T_A = 0$ to 70°C)
  - V_{CC} Range: 3.2V to 5.5V ($T_A = -40$ to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 10mA
  - Standby Current 10µA
- SMALL PACKAGES FOR SURFACE MOUNTING:
  - Plastic: PLCC32
  - Plastic: PTSO28, thin small outline 8 x 13.4mm
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES OF AROUND 6sec. (PRESTO IIB ALGORITHM)
- M27V512 IS PROGRAMMABLE AS M27C512 WITH IDENTICAL SIGNATURE



PLCC32 (K)

PTSO28 (N)
8 x 13.4mm

DESCRIPTION

The M27V512 is a low voltage, low power 512K One Time Programmable ROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 524,288 by 8 bits.

The M27V512 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

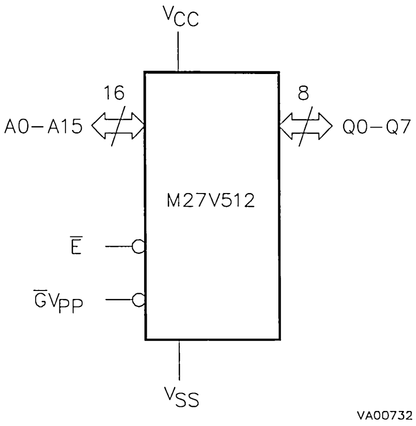
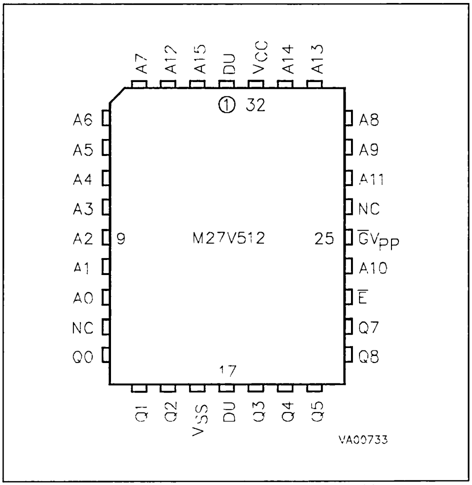


Figure 2A. LCC Pin Connections


A7
A12
A15
DU
VCC
A14
A13
① 32
A6
A5
A4
A3
A2
A1
A0
NC
Q0
9
M27V512
25
A8
A9
A11
NC
$\overline{G}V_{PP}$
A10
$\overline{E}$
Q7
Q8
17
Q1
Q2
VSS
DU
Q3
Q4
Q5
VA00733

Warning: NC = No Connection, DU = Don't Use.

Figure 2B. TSOP Pin Connections

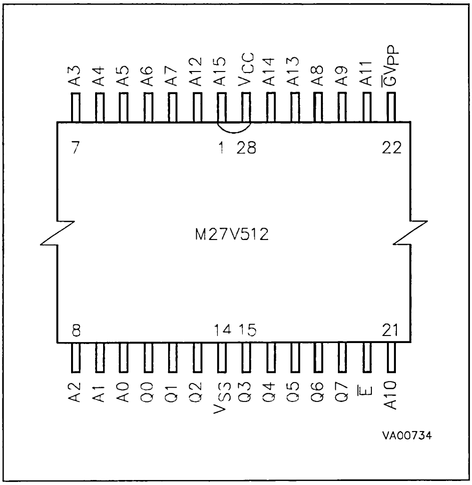

A3
A4
A5
A6
A7
A12
A15
VCC
A14
A13
A8
A9
A11
$\overline{G}V_{PP}$
7
1 28
22
M27V512
8
14 15
21
A2
A1
A0
Q0
Q1
Q2
VSS
Q3
Q4
Q5
Q6
Q7
$\overline{E}$
A10
VA00734

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DESCRIPTION (cont'd)

The M27V512 can also be operated as a standard 512 EPROM (similar to M27C512) with a 5V power supply .

For equipment requiring a surface monted, low profile package, theM27V512 is offered in Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

DEVICE OPERATION

The modes of operations of the M27V512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27V512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power

DEVICE OPERATION (Cont'd)

control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V512 has a standby mode which reduces the active current from 10mA to 10µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because OTP ROMs are often used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

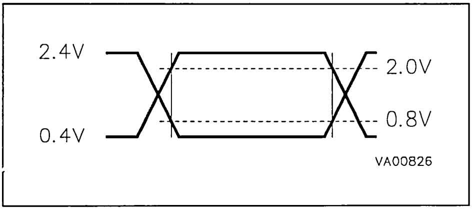


Figure 3. AC Testing Input Output Waveforms

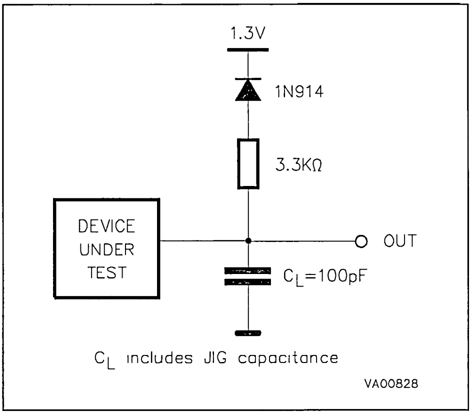


Figure 4. AC Testing Load Circuit

Table 5. Capacitance (T$_A$ = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Table 6. Read Mode DC Characteristics [(1)]

(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz, V_{CC} ≤ 3.2V		10	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		10	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 7. Read Mode AC Characteristics [1]
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V512				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		70		100	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	60	0	60	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested.

Figure 5. Read Mode AC Waveforms

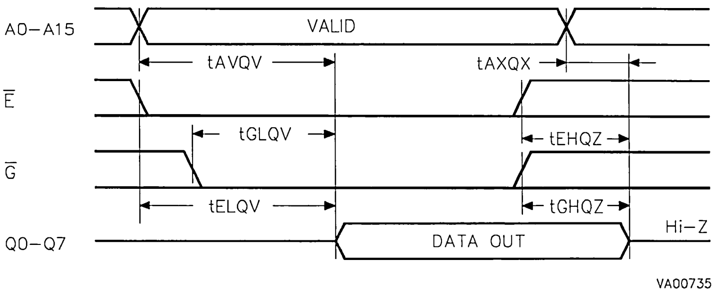


Table 8. Programming Mode DC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Table 9. MARGIN MODE AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

Table 10. Programming Mode AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		0		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

2 This parameter is sampled only and not 100% tested.

Figure 6. MARGIN MODE AC Waveforms

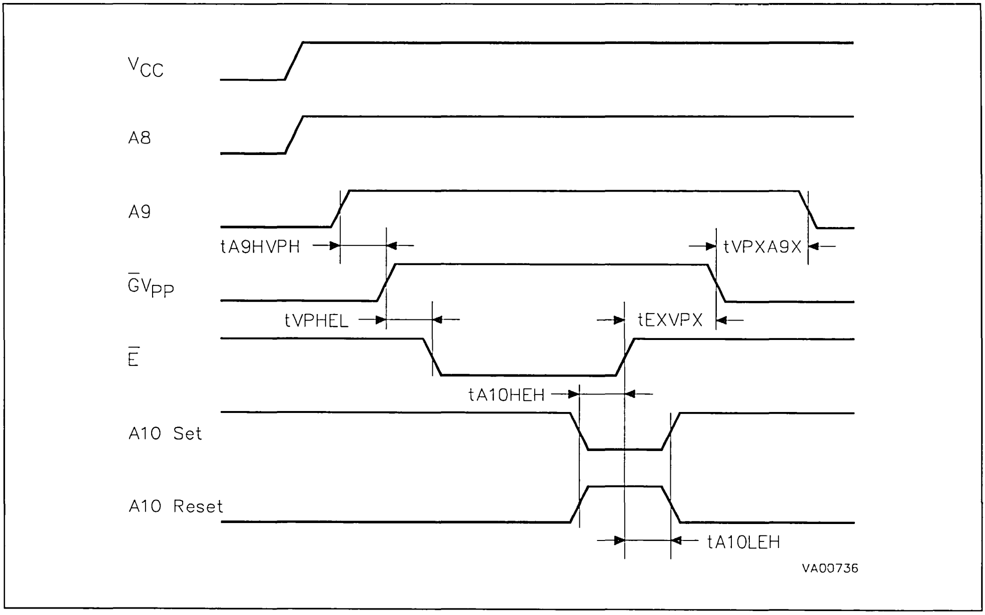

VCC
A8
A9
tA9HVPH
tVPXA9X
GVPP
tVPHEL
tEXVPX
E
tA10HEH
A10 Set
A10 Reset
tA10LEH
VA00736

Figure 7. Programming and Verify Modes AC Waveforms

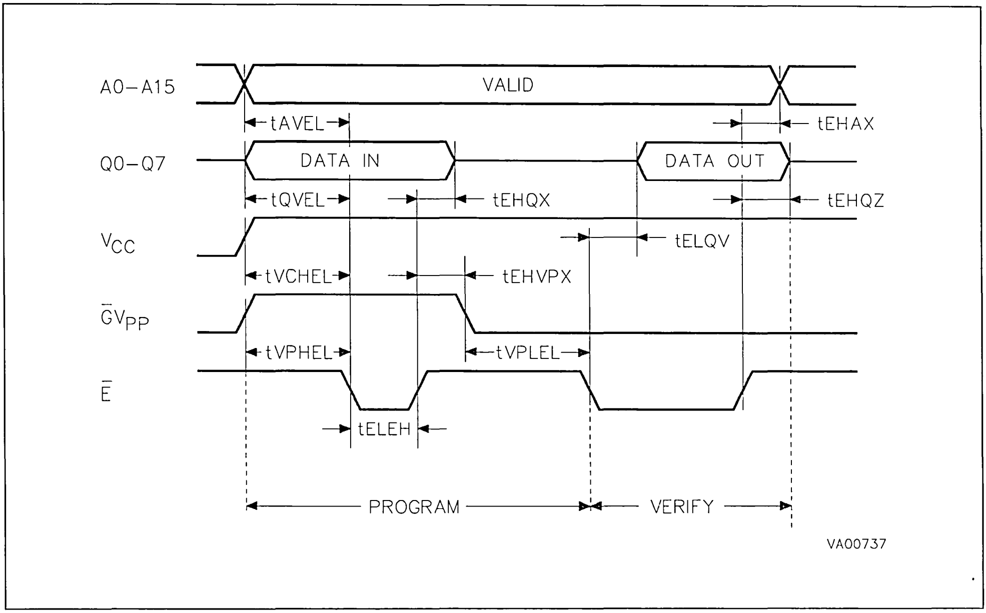
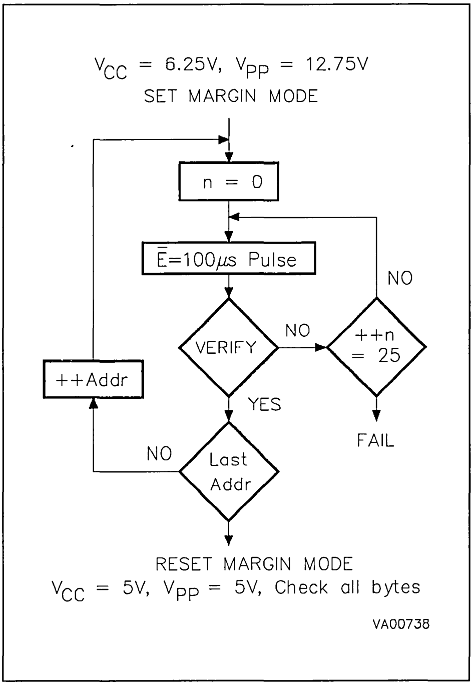

A0-A15
VALID
tAVEL
tEHAX
Q0-Q7
DATA IN
DATA OUT
tQVEL
tEHQX
tEHQZ
VCC
tELQV
tVCHEL
tEHVPX
GVPP
tVPHEL
tVPLEL
E
tELEH
PROGRAM
VERIFY
VA00737

Figure 8. Programming Flowchart



Programming

The M27V512 has been designed to be fully compatible with the M27C512. As a result the M27V512 can be programmed as the M27C512 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V512 has the same electronic signature and uses the same PRESTO IIB algorithm.

When delivered, all bits of the M27V512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27V512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

The M27V512 uses the PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in around 6 seconds. This can be achieved with SGS-THOMSON M27V512 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100μs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27V512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27V512 may be common. A TTL low level pulse applied to a M27V512's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27V512. A high level $\overline{E}$ input inhibits the other M27V512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

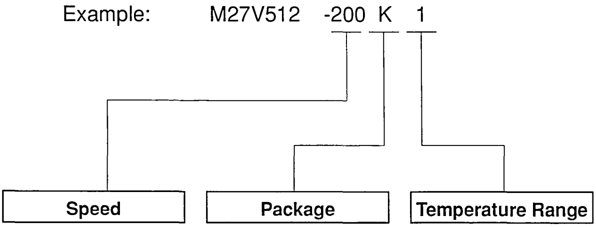
Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V512. To activate this mode, the programming equipment must apply a Supply Voltage V_{CC} of 5V and force 11.5V to 12.5V on address line A9 of the M27V512.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V512, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

Note that the M27V512 and the M27C512 have the same identifier bytes.

ORDERING INFORMATION


Example: M27V512 -200 K 1
Speed
Package
Temperature Range

Speed		Package		Temperature Range	
-200	200 ns	K	PLCC32	1	0 to 70 °C
-250	250 ns	N	PTSO28 8 x 13.4mm	6	–40 to 85 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

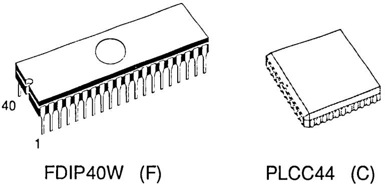
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M27C516

CMOS 512K (32K x 16) UV EPROM and OTP ROM

- FAST ACCESS TIME: 120ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 200µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 3sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C516 is a high speed 512K bit UV erasable and electrically programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 32K by 16 bits.

The 40 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C516 is offered in a Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program Enable
V_{CC}	Supply Voltage
V_{PP}	Program Supply
V_{SS}	Ground

Figure 1. Logic Diagram

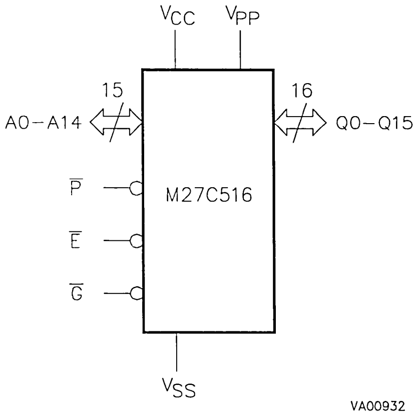


Figure 2A. DIP Pin Connections

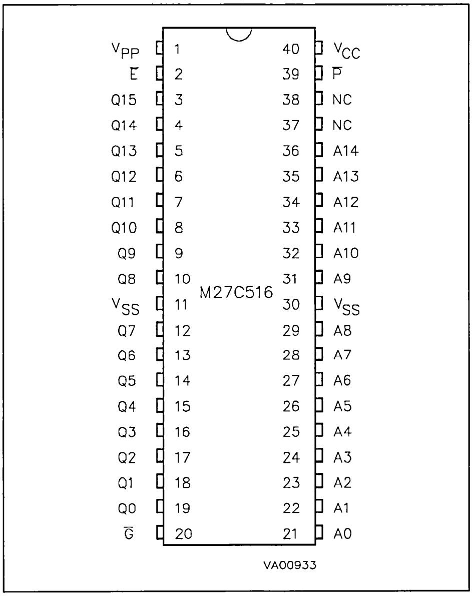
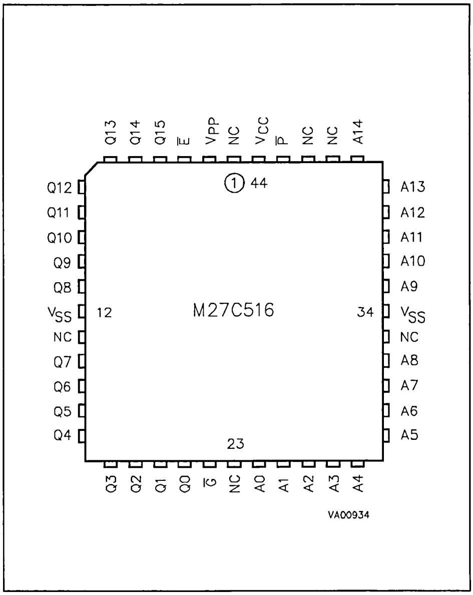

VPP 1
E 2
Q15 3
Q14 4
Q13 5
Q12 6
Q11 7
Q10 8
Q9 9
Q8 10
VSS 11
Q7 12
Q6 13
Q5 14
Q4 15
Q3 16
Q2 17
Q1 18
Q0 19
G 20
40 VCC
39 P
38 NC
37 NC
36 A14
35 A13
34 A12
33 A11
32 A10
31 A9
30 VSS
29 A8
28 A7
27 A6
26 A5
25 A4
24 A3
23 A2
22 A1
21 A0
M27C516
VA00933

Figure 2B. LCC Pin Connections


Q13 Q14 Q15 E VPP NC VCC P NC NC A14
Q12 Q11 Q10 Q9 Q8 VSS NC Q7 Q6 Q5 Q4
A13 A12 A11 A10 A9 VSS NC A8 A7 A6 A5
Q3 Q2 Q1 Q0 G NC A0 A1 A2 A3 A4
1 44
12
34
23
M27C516
VA00934

Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1	0 to 70	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The modes of operations of the M27C516 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27C516 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should

DEVICE OPERATION (cont'd)

be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C516 has a standby mode which reduces the active current from 30mA to 200µA. The M27C516 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Program	V_{IL}	X	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	1	1	1	0Fh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

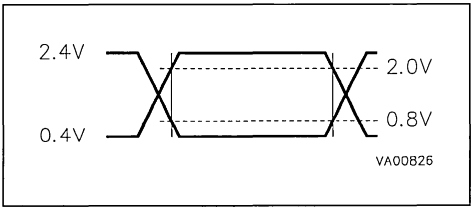


Figure 4. AC Testing Load Circuit

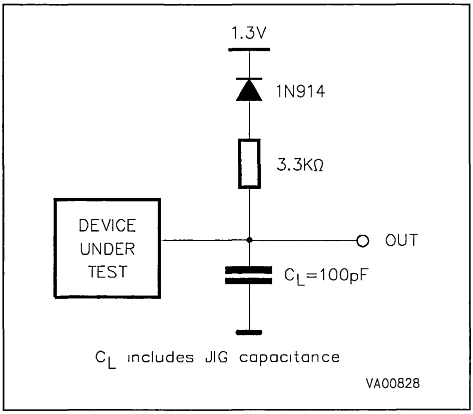


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is sampled only and not tested 100%.

Table 6. Read Mode DC Characteristics [(1)]
(T_A = 0 to 70 °C; V_{CC} = 5V ± 5%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		200	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics [1]

(T_A = 0 to 70 °C; V_{CC} = 5V ± 5%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C516						Unit
				-12		-15		-20		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50		60		70	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	50	0	60	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	40	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested.

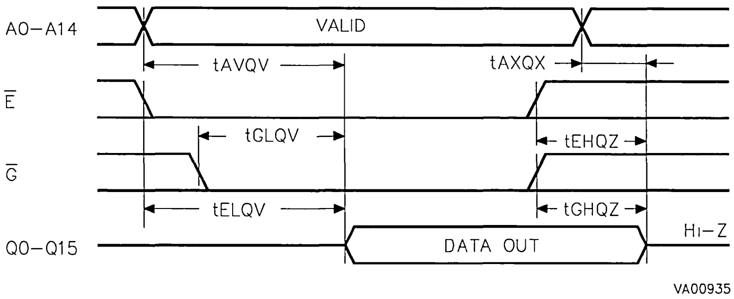


Figure 5. Read Mode AC Waveforms

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C516 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C516 is in -the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ±0.25V.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		µs

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

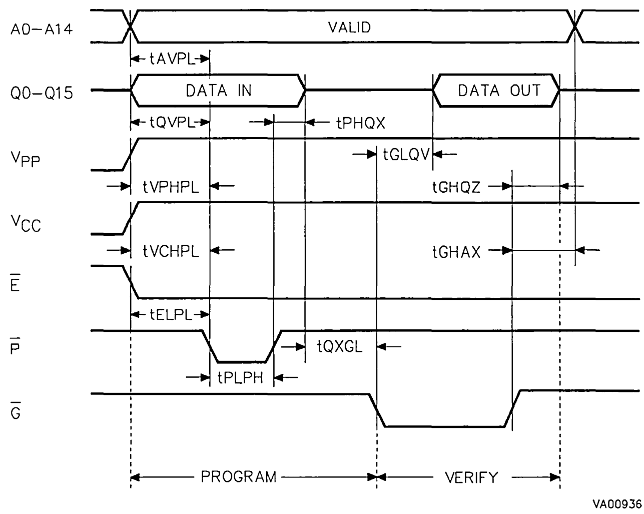
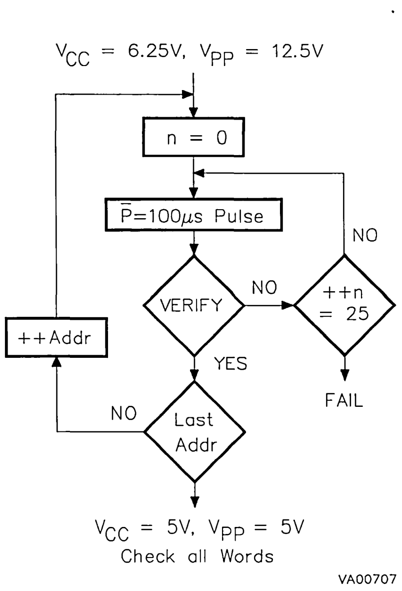

A0–A14
VALID
tAVPL
Q0–Q15
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00936

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
P=100µs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Words
VA00707

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in around 3 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C516s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C516 may be common. A TTL low level pulse applied to a M27C516's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C516. A high level $\overline{E}$ input inhibits the other M27C516s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C516. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C516.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C516, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C516 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C516 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C516 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C516 window to prevent unintentional erasure. The recommended erasure procedure for the M27C516 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C516 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C516 -12 X F 1 L

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-12	120 ns	X	± 5%	F	FDIP40W	1	0 to 70 °C	L	Low Power
-15	150 ns			C	PLCC44			X	Additional Burn-in
-20	200 ns							TR	Tape & Reel

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

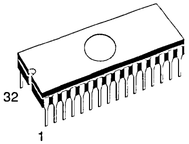
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

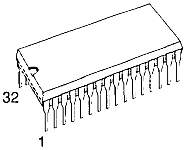
M27C1000

CMOS 1 Megabit (128K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 12sec.(PRESTO II ALGORITHM)



FDIP32W (F)



PDIP32 (B)

DESCRIPTION

The M27C1000 is a high speed 1 Megabit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C1000 is offered in Plastic Dual-in-Line package.

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

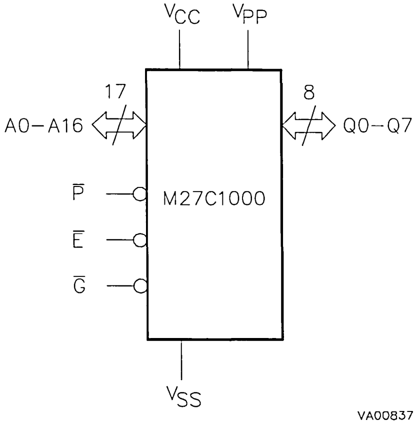
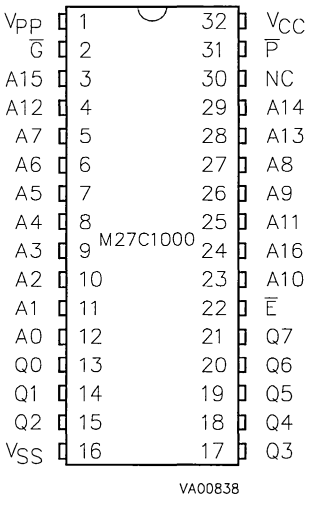


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1	0 to 70	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The modes of operation of the M27C1000 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C1000 has two control functions, both of which must be logically active in order to obtain data at the outputs.Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1000 has a standby mode which reduces the active current from 30mA to 100µA (or 35mA to 200µA, see Read Mode DC Characteristics Table for details). The M27C1000 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary

DEVICE OPERATION (cont'd)

device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1000 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C1000 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 12 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

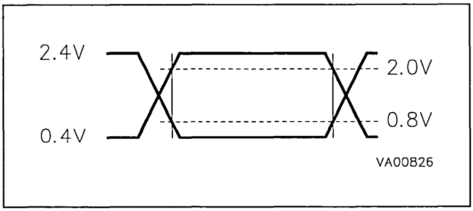


Figure 4. AC Testing Load Circuit

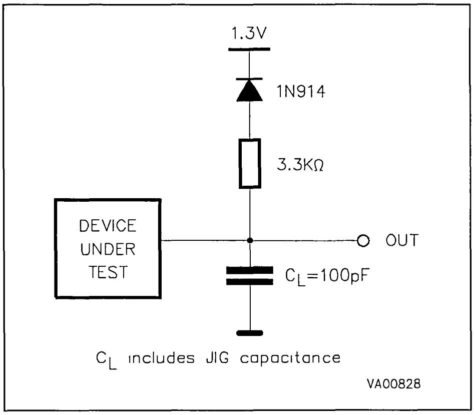


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (2)	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2} (3)	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 For Speeds -80, -10 only. For other types the maximum I_{CC} is 35mA.
3. For Speeds -80, -10 only. For other types the maximum I_{CC2} is 200µA.

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1000						Unit
				-80		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1000						Unit
				-15		-20		-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		65		70		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is sampled only and not 100% tested.

Figure 5. Read Mode AC Waveforms

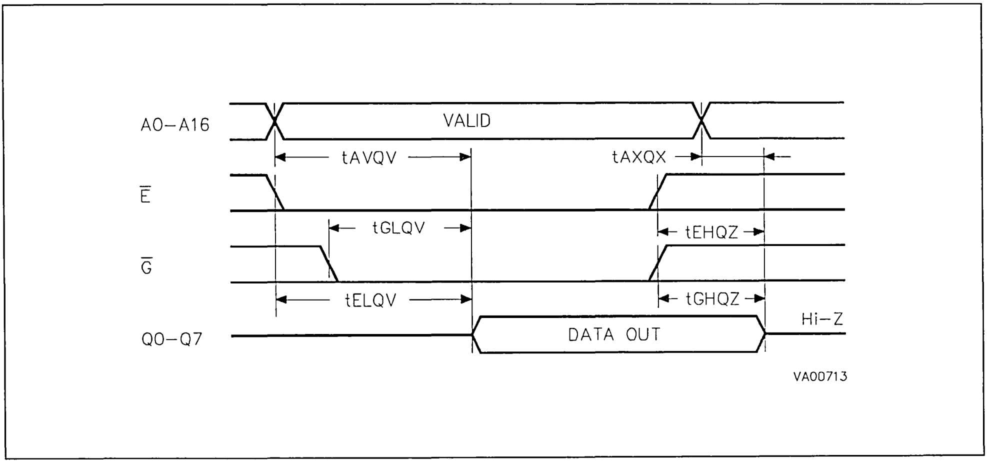


Table 8. Programming Mode DC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is sampled only and not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

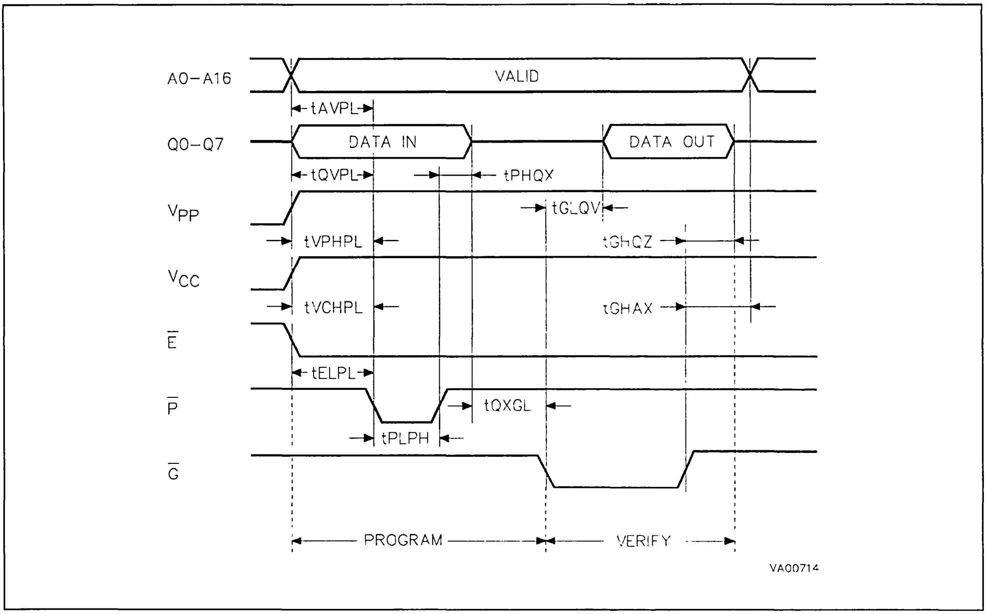
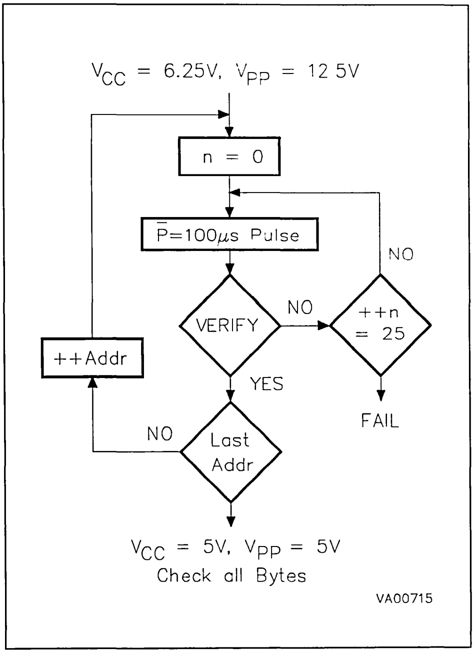

A0–A16
VALID
tAVPL
Q0–Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00714

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
P=100µs Pulse
VERIFY
NO
++n = 25
NO
FAIL
YES
++Addr
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00715

Program Inhibit

Programming of multiple M27C1000s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C1000 may be common. A TTL low level pulse applied to a M27C1000 $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C1000. A high level $\overline{E}$ input inhibits the other M27C1000 from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1000. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1000, with

DEVICE OPERATION (cont'd)

$V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C1000, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1000 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1000 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1000 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1000 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1000 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C1000 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C1000 -80 X F 1

Speed		V_{CC} Tolerance		Package		Temperature Range	
-80	80 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C
-10	100 ns	blank	± 10%	B	PDIP32		
-12	120 ns						
-15	150 ns						
-20	200 ns						
-25	250 ns						

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

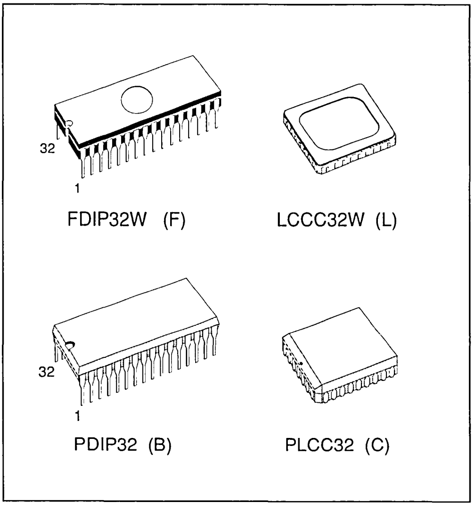
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M27C1001

CMOS 1 Megabit (128K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 12sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C1001 is a high speed 1 Megabit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C1001 is offered in both Plastic Dual-in-Line and Plastic Leaded Chip Carrier packages.

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

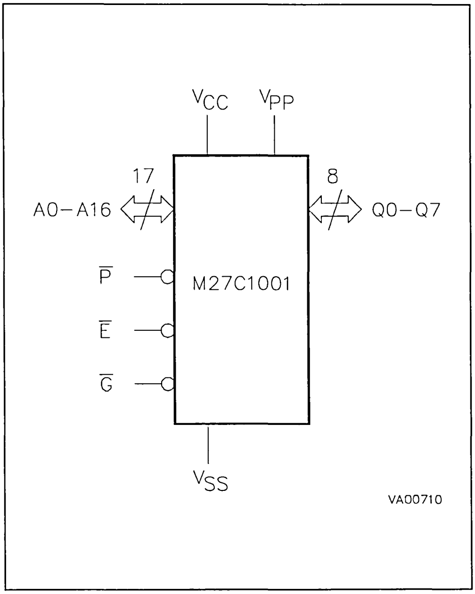
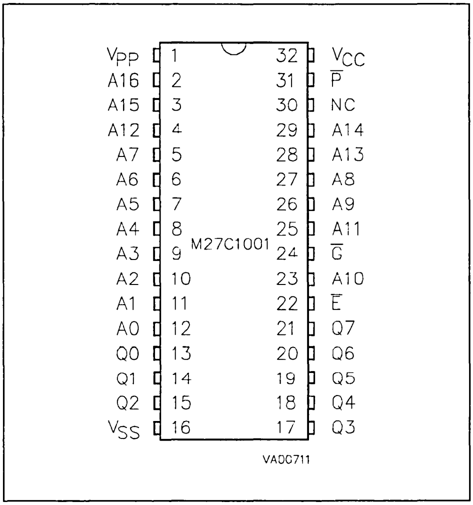


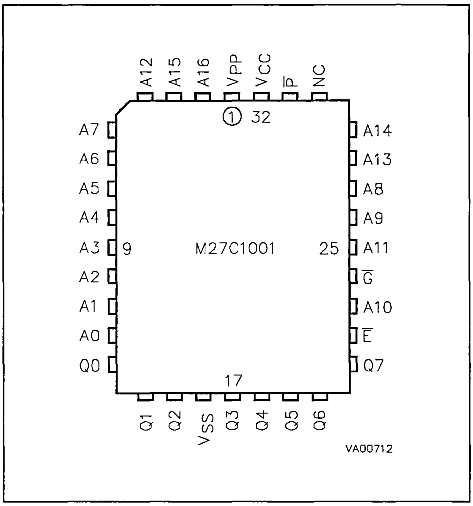
Figure 2A. DIP Pin Connections



V_{PP} 1 32 V_{CC}
A16 2 31 $\overline{P}$
A15 3 30 NC
A12 4 29 A14
A7 5 28 A13
A6 6 27 A8
A5 7 26 A9
A4 8 25 A11
A3 9 24 $\overline{G}$
A2 10 23 A10
A1 11 22 $\overline{E}$
A0 12 21 Q7
Q0 13 20 Q6
Q1 14 19 Q5
Q2 15 18 Q4
V_{SS} 16 17 Q3
M27C1001
VA00711

Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



A12
A15
A16
VPP
VCC
$\overline{P}$
NC
① 32
A7
A6
A5
A4
A3
A2
A1
A0
Q0
9
M27C1001
25
A14
A13
A8
A9
A11
$\overline{G}$
A10
$\overline{E}$
Q7
17
Q1
Q2
VSS
Q3
Q4
Q5
Q6
VA00712

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DEVICE OPERATION

The modes of operation of the M27C1001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1001 has a standby mode which reduces the active current from 30mA to 100µA (or

DEVICE OPERATION (cont'd)

35mA to 200µA, see Read Mode DC Characteristics Table for details). The M27C1001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C1001 is in the programming mode when V_{pp} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

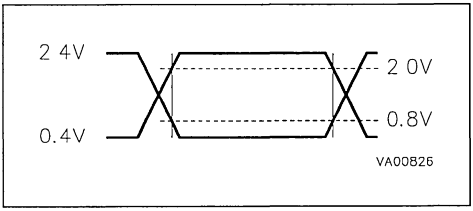


Figure 4. AC Testing Load Circuit

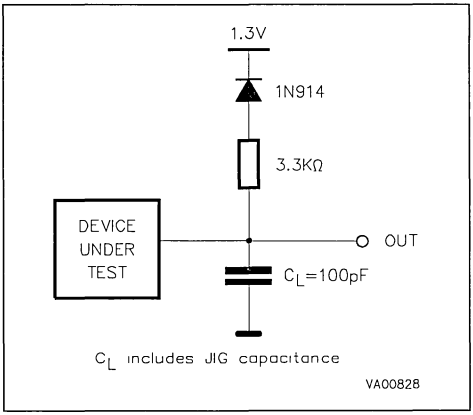


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Table 6. Read Mode DC Characteristics [(1)]
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}[(2)]	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}[(3)]	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 For Speeds -80, -10 and Option "L" at 0 to 70 °C only For other types the maximum I_{CC} is 35mA
3. For Speeds -80, -10 and Option "L" at 0 to 70 °C only. For other types the maximum I_{CC2} is 200µA.

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1001						Unit
				-80		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1001						Unit
				-15		-20		-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		65		70		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

2 This parameter is sampled only and not 100% tested.

Figure 5. Read Mode AC Waveforms

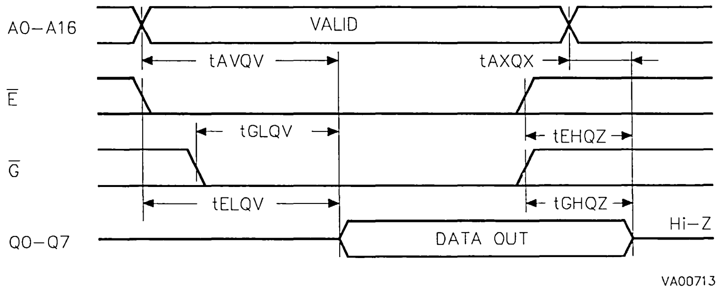


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

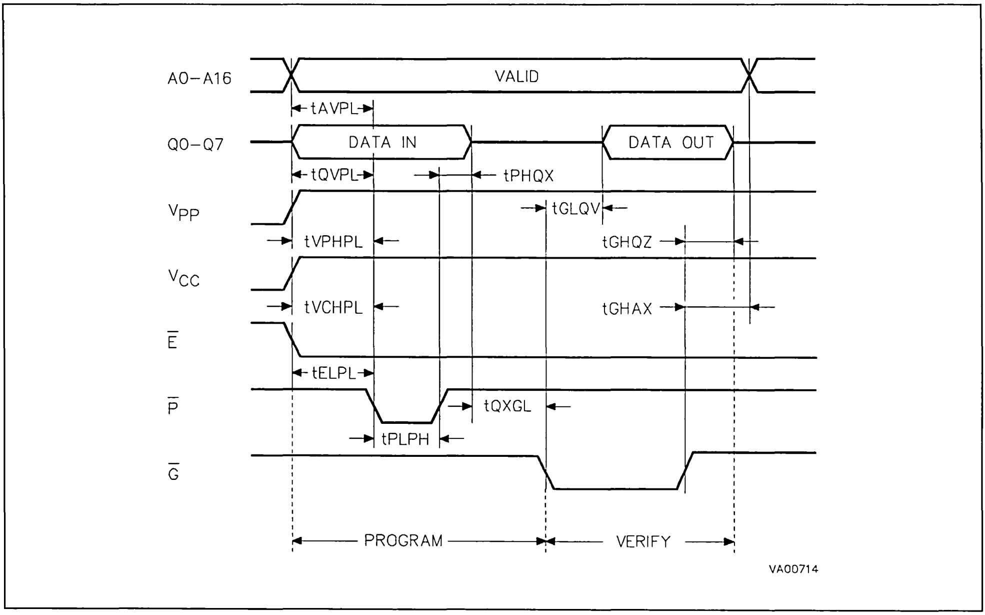
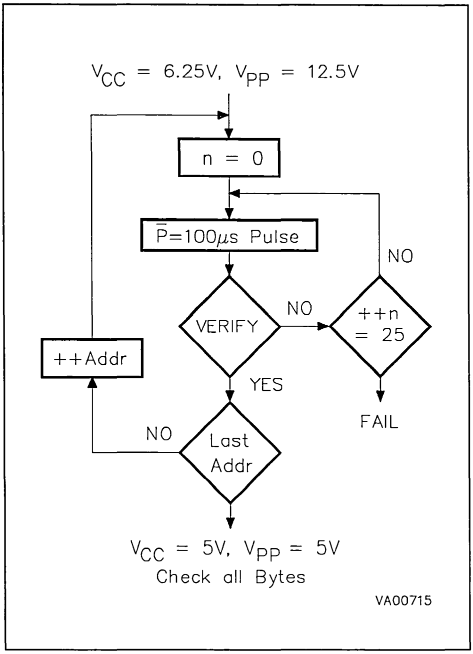

A0–A16
VALID
tAVPL
Q0–Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00714

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
P=100µs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00715

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 12 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C1001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C1001 may be common. A TTL low level pulse applied to a M27C1001's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C1001. A high level $\overline{E}$ input inhibits the other M27C1001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

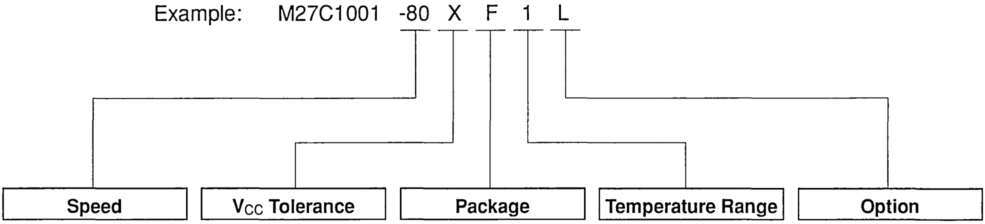
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1001, with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C1001, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1001 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C1001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION



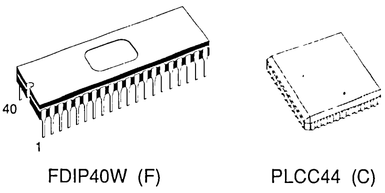
Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	L	Low Power
-10	100 ns	blank	± 10%	B	PDIP32	3	–40 to 125 °C	X	Additional Burn-in
-12	120 ns			C	PLCC32	6	–40 to 85 °C		
-15	150 ns			L	LCCC32W			TR	Tape & Reel
-20	200 ns								
-25	250 ns								

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

CMOS 1Megabit (64K x16) UV EPROM and OTP ROM

- FAST ACCESS TIME: 120 ns
- COMPATIBLE WITH HIGH SPEED MICRO-PROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 35 mA
  - Standby Current 100 µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIME OF AROUND 6 sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C1024 is a 1 Megabit UV erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits.

The 40 pin Ceramic Frit Seal Window package has a transparent lid whide allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For application where the content is programmed only one time and erasure is not required, the M27C1024 is offered in a Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

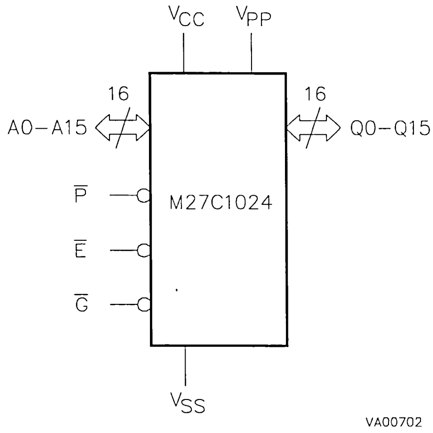
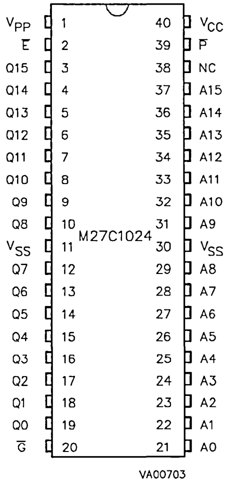
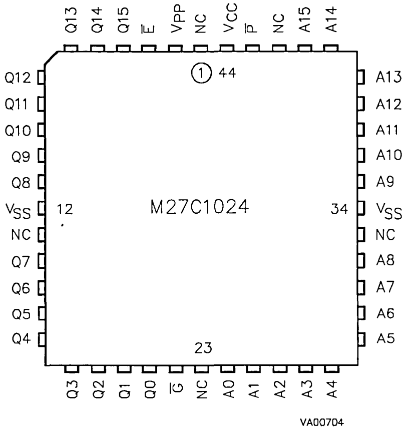


Figure 2A. DIP Pin Connections


VPP 1
$\overline{E}$ 2
Q15 3
Q14 4
Q13 5
Q12 6
Q11 7
Q10 8
Q9 9
Q8 10
VSS 11
Q7 12
Q6 13
Q5 14
Q4 15
Q3 16
Q2 17
Q1 18
Q0 19
$\overline{G}$ 20
40 VCC
39 $\overline{P}$
38 NC
37 A15
36 A14
35 A13
34 A12
33 A11
32 A10
31 A9
30 VSS
29 A8
28 A7
27 A6
26 A5
25 A4
24 A3
23 A2
22 A1
21 A0
M27C1024
VA00703

Warning: NC = No Connection.

Figure 2B. LCC Pin Connections


Q13
Q14
Q15
$\overline{E}$
VPP
NC
VCC
$\overline{P}$
NC
A15
A14
1
44
Q12
Q11
Q10
Q9
Q8
VSS
NC
Q7
Q6
Q5
Q4
12
M27C1024
34
A13
A12
A11
A10
A9
VSS
NC
A8
A7
A6
A5
23
Q3
Q2
Q1
Q0
$\overline{G}$
NC
A0
A1
A2
A3
A4
VA00704

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The modes of operations of the M27C1024 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp and 12V on A9 for Electronic Signature.

Read Mode

The M27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1024 has a standby mode which reduces the active current from 35 mA to 100 µA.

DEVICE OPERATION (cont'd)

The M27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1024 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C1024 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied, 16 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Output
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Program	V_{IL}	X	V_{IL} Pulse	X	V_{PP}	Data Input
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Output
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ±0 5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8Ch

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

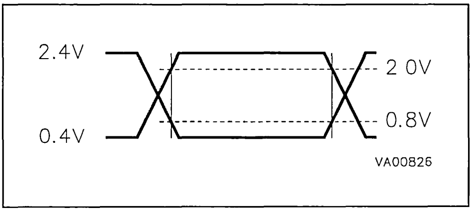

2.4V
0.4V
2 0V
0.8V
VA00826

Figure 4. AC Testing Load Circuit

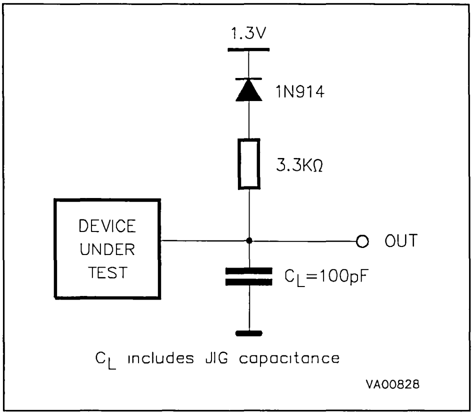

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L=100pF
C_L includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Figure 5. Read Mode AC Waveforms

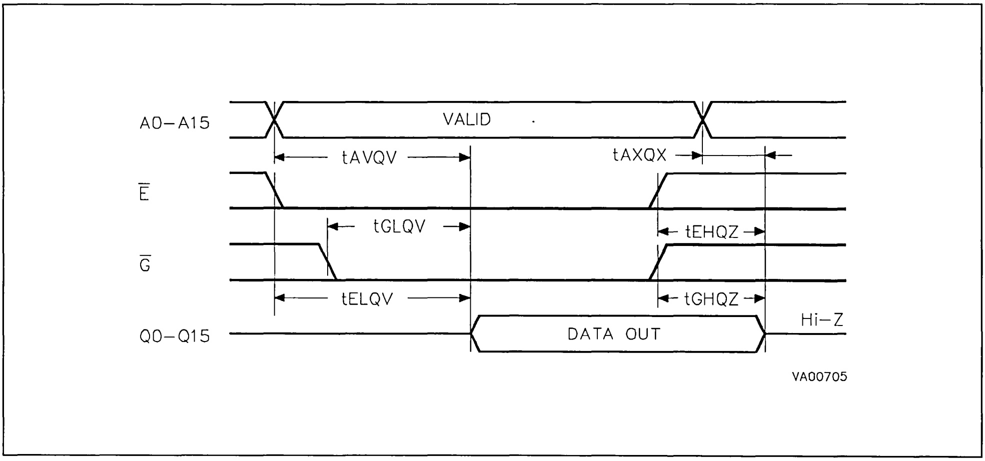

A0–A15
VALID
tAVQV
tAXQX
$\overline{E}$
tGLQV
tEHQZ
$\overline{G}$
tELQV
tGHQZ
Q0–Q15
DATA OUT
Hi–Z
VA00705

Table 6. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		35	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1024				Unit
				-12		-15		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1024				Unit
				-20		-25		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		70		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	80	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	80	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}

2. This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}

2. This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

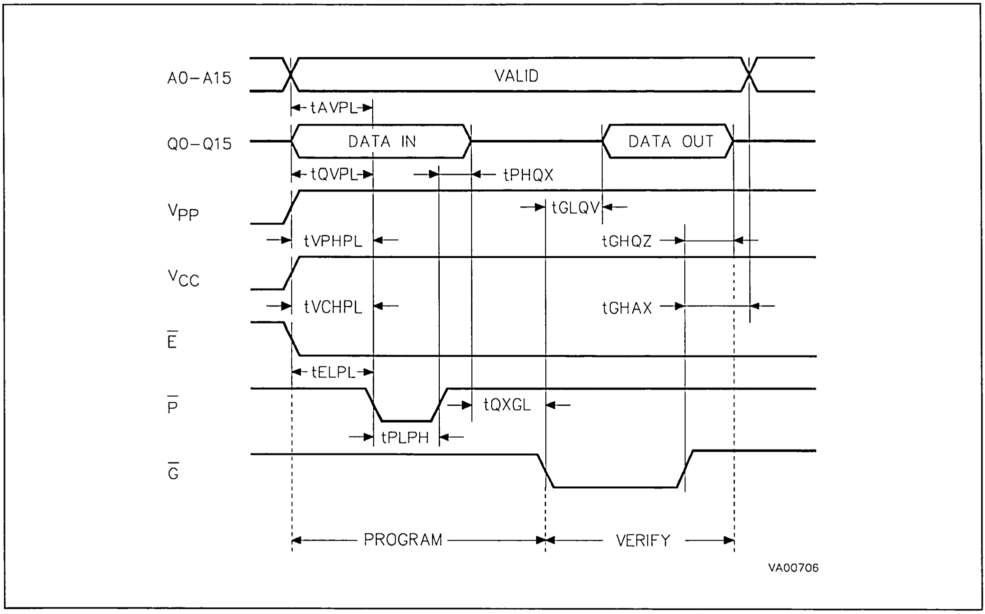
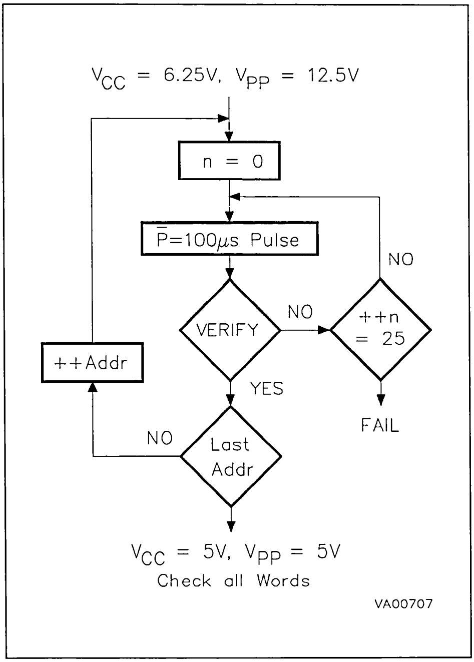

A0-A15
VALID
tAVPL
Q0-Q15
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00706

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
P=100μs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Words
VA00707

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows programming of the whole array with a guaranteed margin, in a typical time of less than 6 seconds. Programming with PRESTO II consists of applying a sequence of 100 μs program pulses to each word until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C1024s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C1024 may be common. A TTL low level pulse applied to a M27C1024's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C1024. A high level $\overline{E}$ input inhibits the other M27C1024s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1024. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1024 with V_{PP} = V_{CC} = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C1024, these two iden-tifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1024 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C1024 -12 X F 1 L

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-12	120 ns	X	± 5%	F	FDIP40W	1	0 to 70 °C	L	Low Power
-15	150 ns	blank	± 10%	C	PLCC44	6	–40 to 85 °C	X	Additional Burn-in
-20	200 ns								
-25	250 ns							TR	Tape & Reel

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

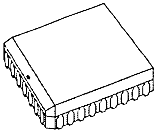
SGS-THOMSON
MICROELECTRONICS

M27V101

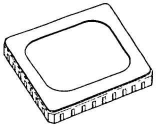
LOW VOLTAGE CMOS
1 Megabit (128K x 8) UV EPROM and OTP ROM

ADVANCE DATA

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES FOR SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES OF AROUND 12sec. (PRESTO II ALGORITHM)
- M27V101 IS PROGRAMMABLE AS M27C1001 WITH IDENTICAL SIGNATURE



PLCC32 (K)



LCCC32W (L)

DESCRIPTION

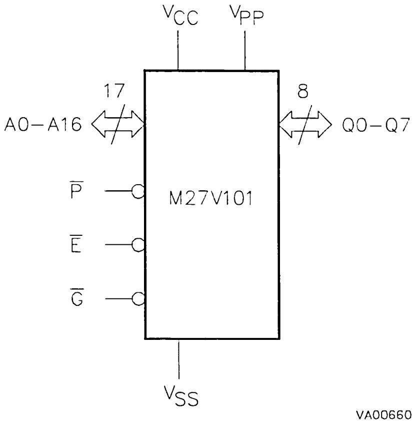
The M27V101 is a low voltage, low power 1 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The M27V101 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



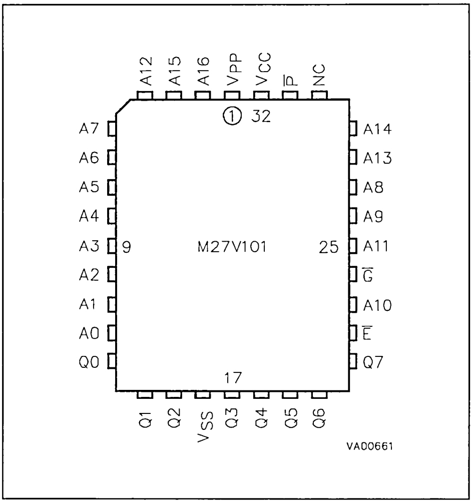
This is advance information on a new product now in development or undergoing evaluation Details are subject to change without notice

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. LCC Pin Connections



Warning: NC = No Connection

DESCRIPTION (cont'd)

The M27V101 can also be operated as a standard 1 Megabit EPROM (similar to M27C1001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27V101 is offered in Plastic Leaded Chip Carrier package.

DEVICE OPERATION

The modes of operation of the M27V101 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V101 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V101 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V101 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

DEVICE OPERATION (cont'd)

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V101 has been designed to be fully compatible with the M27C1001. As a result the M27V101 can be programmed as the M27C1001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V101 has the same electronic signature and uses the same PRESTO II algorithm .

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven

Figure 3. AC Testing Input Output Waveforms

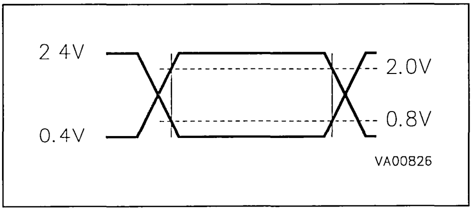


Figure 4. AC Testing Load Circuit

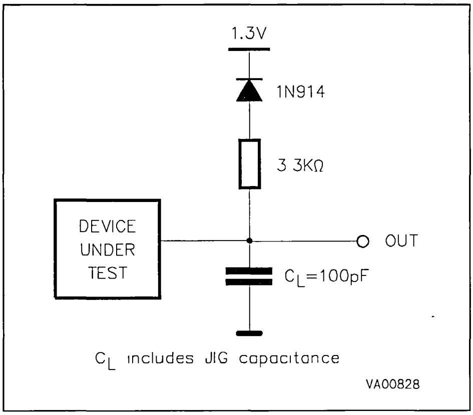


Table 5. Capacitance (T$_A$ = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Table 6. Read Mode DC Characteristics [1]
(T$_A$ = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T$_A$ = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

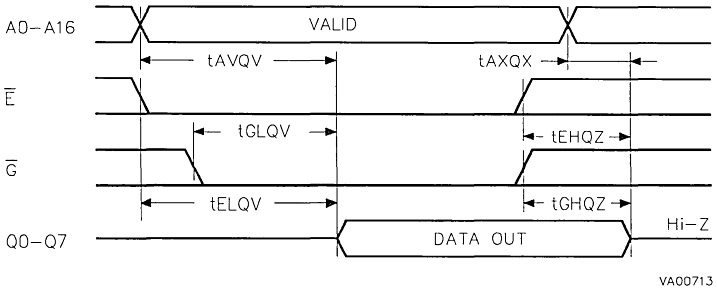
Table 7. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V101				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		130		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	80	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	80	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested

Figure 5. Read Mode AC Waveforms



DEVICE OPERATION (cont'd)

When delivered (and after each erasure for UV EPROM), all bits of the M27V101 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V101 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

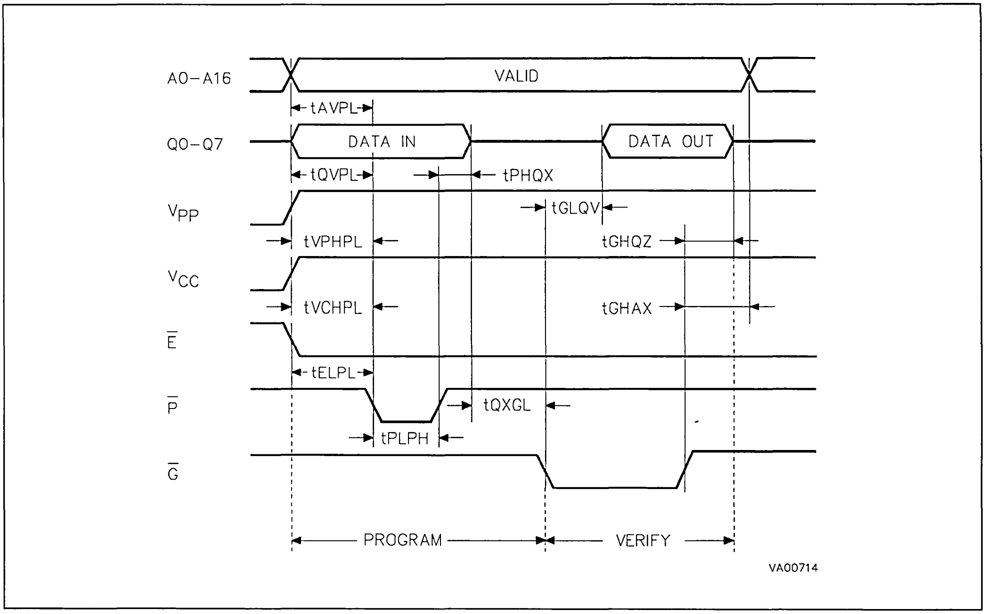
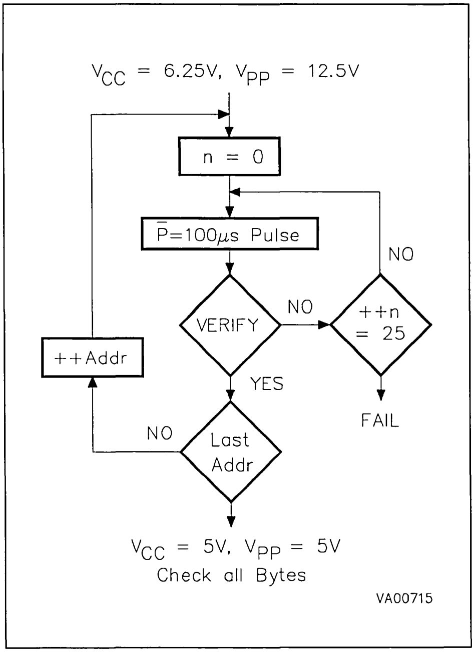

A0–A16
VALID
tAVPL
Q0–Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00714

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
P=100μs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00715

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 12 seconds. Programming with PRESTO II involves in applying a sequence of 100μs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V101s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V101 may be common. A TTL low level pulse applied to a M27V101's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V101. A high level $\overline{E}$ input inhibits the other M27V101s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V101. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V101, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V101, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7. Note that the M27V101 and M27C1001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V101 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V101 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V101 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V101 window to prevent unintentional erasure. The recommended erasure procedure for the M27V101 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V101 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which

ORDERING INFORMATION

Example: M27V101 -200 K 6 TR

Speed		Package		Temperature Range		Option	
-200	200 ns	K	PLCC32	1	0 to 70 °C	TR	Tape & Reel
-250	250 ns	L	LCCC32W	6	–40 to 85 °C		

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

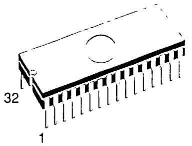
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

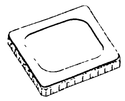
M27C2001

CMOS 2 Megabit (256K x 8) UV EPROM and OTP ROM

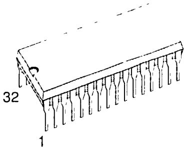
- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 24sec. (PRESTO II ALGORITHM)



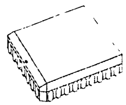
FDIP32W (F)



LCCC32W (L)



PDIP32 (B)



PLCC32 (C)

DESCRIPTION

The M27C2001 is a high speed 2 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C2001 is offered in both Plastic Dual-in-Line and Plastic Leaded Chip Carrier packages.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

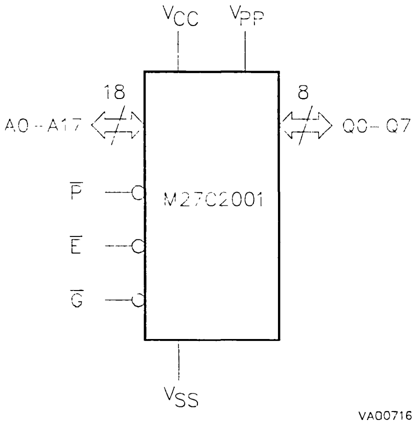


Figure 2A. DIP Pin Connections

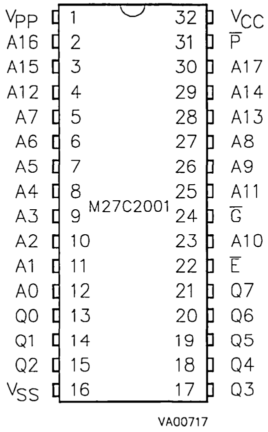

VPP 1 32 VCC
A16 2 31 P̅
A15 3 30 A17
A12 4 29 A14
A7 5 28 A13
A6 6 27 A8
A5 7 26 A9
A4 8 25 A11
A3 9 24 G̅
A2 10 23 A10
A1 11 22 E̅
A0 12 21 Q7
Q0 13 20 Q6
Q1 14 19 Q5
Q2 15 18 Q4
VSS 16 17 Q3
M27C2001
VA00717

Figure 2B. LCC Pin Connections

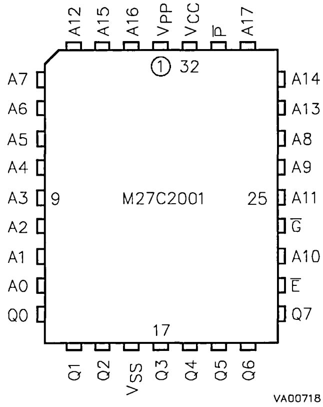

A12 A15 A16 VPP VCC P̅ A17
① 32
A7 A6 A5 A4 A3 A2 A1 A0 Q0
9
M27C2001
25
A14 A13 A8 A9 A11 G̅ A10 E̅ Q7
17
Q1 Q2 VSS Q3 Q4 Q5 Q6
VA00718

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{E}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{G}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{\text{E}}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{\text{G}}$, assuming that $\overline{\text{E}}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C2001 has a standby mode which reduces the active current from 30mA to 100µA (or

DEVICE OPERATION (cont'd)

35mA to 200µA, see Read Mode DC Characteristics Table for details). The M27C2001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C2001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C2001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0 5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

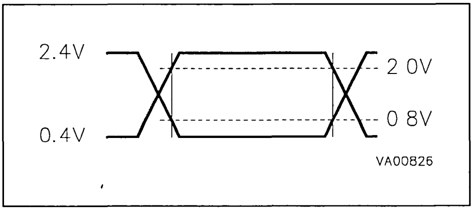


Figure 4. AC Testing Load Circuit

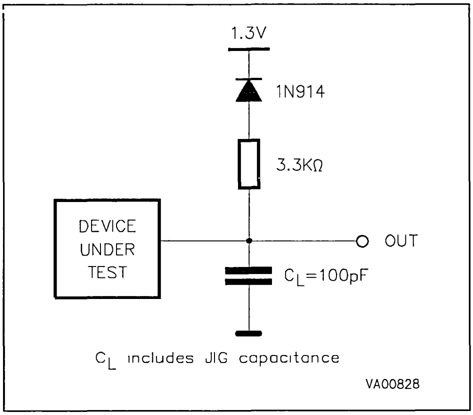


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		12	pF

Note: This parameter is sampled only and not tested 100%

Table 6. Read Mode DC Characteristics [(1)]
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}[(2)]	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}[(3)]	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	$V_{CC} - 0.7V$		V

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2 For Speeds -80, -10, -12 and Option "L" at 0 to 70 °C only. For other types the maximum I_{CC} is 35mA.
3 For Speeds -80, -10, -12 and Option "L" at 0 to 70 °C only. For other types the maximum I_{CC2} is 200µA.

Table 7A. Read Mode AC Characteristics [1]
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001						Unit
				-80		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		50	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	40	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics [1]
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001						Unit
				-15		-20		-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		70		100	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	0	60	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

2. This parameter is sampled only and not 100% tested.

Figure 5. Read Mode AC Waveforms

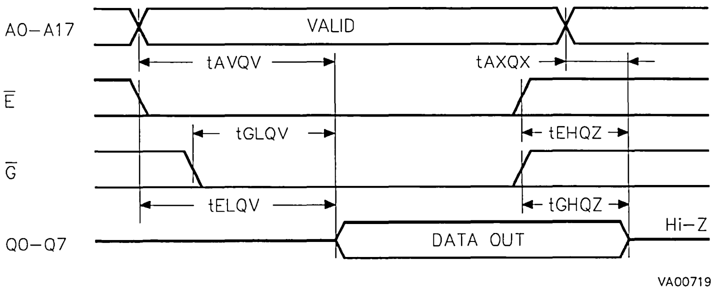


Table 8. Programming Mode DC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

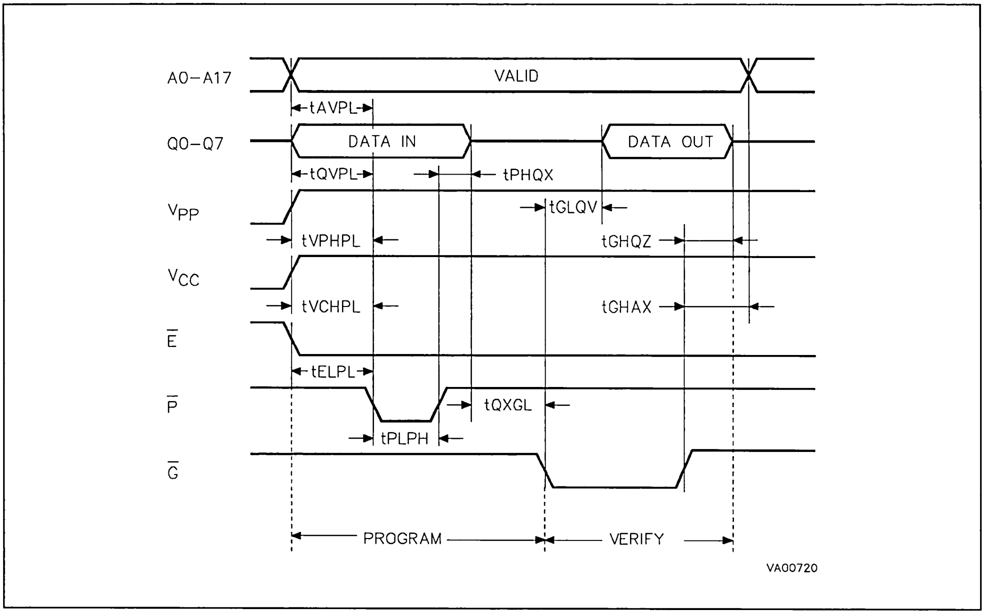
Table 9. Programming Mode AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

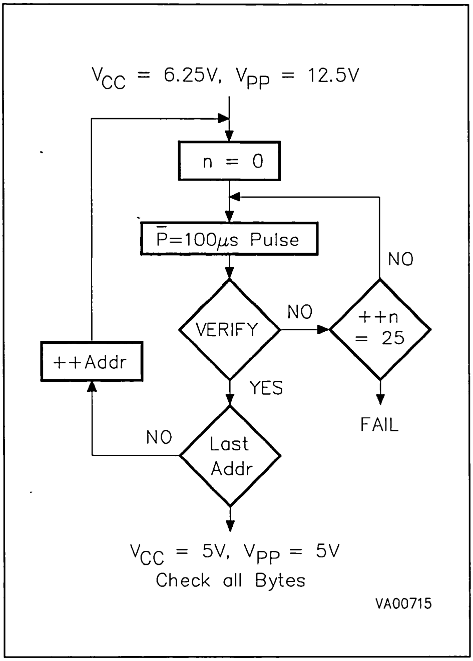
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



A0–A17
VALID
tAVPL
Q0–Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00720

Figure 7. Programming Flowchart



VCC = 6.25V, VPP = 12.5V
n = 0
P=100µs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00715

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 24 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C2001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C2001 may be common. A TTL low level pulse applied to a M27C2001's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C2001. A high level $\overline{E}$ input inhibits the other M27C2001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C2001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C2001 with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C2001, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C2001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C2001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C2001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C2001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C2001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C2001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C2001 -80 X F 1 L

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	L	Low Power
-10	100 ns	blank	± 10%	B	PDIP32	6	–40 to 85 °C	X	Additional Burn-in
-12	120 ns			C	PLCC32			TR	Tape & Reel
-15	150 ns			L	LCCC32W				
-20	200 ns								
-25	250 ns								

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

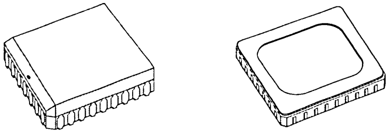
For further information on any aspect of this device, please contact our Sales Office nearest to you.

M27V201

LOW VOLTAGE CMOS
2 Megabit (256K x 8) UV EPROM and OTP ROM

ADVANCE DATA

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER “CMOS” CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES FOR SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES OF AROUND 24sec. (PRESTO II ALGORITHM)
- M27V201 IS PROGRAMMABLE AS M27C2001 WITH IDENTICAL SIGNATURE



DESCRIPTION

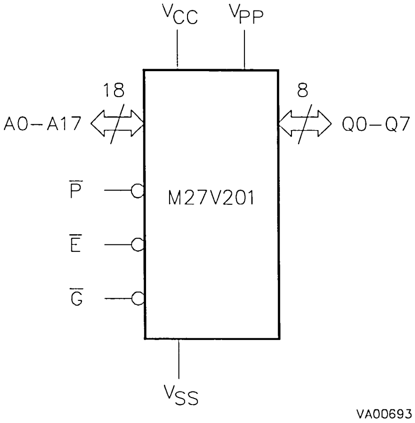
The M27V201 is a low voltage, low power 2 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 262,144 by 8 bits.

The M27V201 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



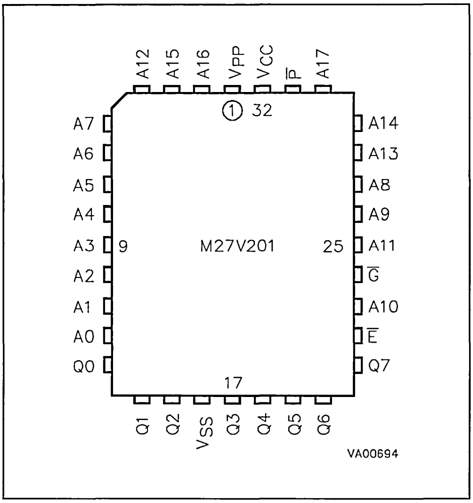
This is advance information on a new product now in development or undergoing evaluation Details are subject to change without notice

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

The M27V201 can also be operated as a standard 2 Megabit EPROM (similar to M27C2001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27V201 is offered in Plastic Leaded Chip Carrier package.

DEVICE OPERATION

The modes of operation of the M27V201 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V201 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V201 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V201 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

DEVICE OPERATION (cont'd)

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V201 has been designed to be fully compatible with the M27C2001. As a result the M27V201 can be programmed as the M27C2001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V201 has the same electronic signature and uses the same PRESTO II algorithm .

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	X	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

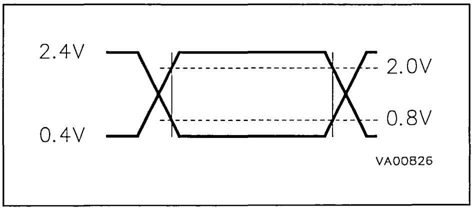


Figure 4. AC Testing Load Circuit

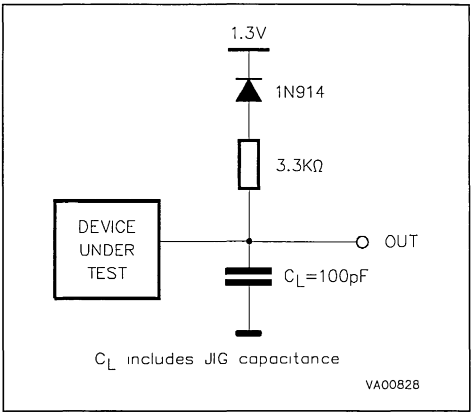


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Table 6. Read Mode DC Characteristics [1]

(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz, $V_{CC} \le 3.2V$		15	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$, $V_{CC} \le 3.2V$		20	µA
		$\overline{E} > V_{CC} - 0.2V$, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

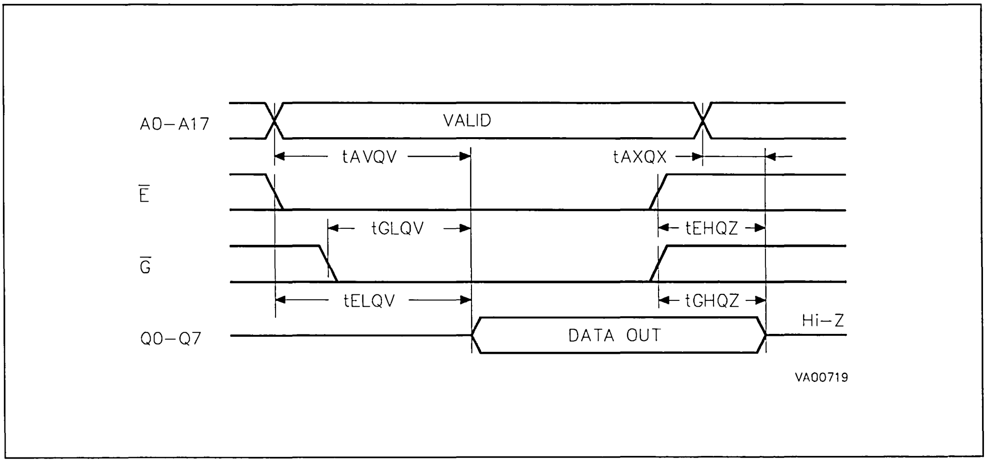
Table 7. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; $V_{PP} = V_{CC}$)
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M27V201				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		130		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	80	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	80	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested

Figure 5. Read Mode AC Waveforms



DEVICE OPERATION (cont'd)

When delivered (and after each erasure for UV EPROM), all bits of the M27V201 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V201 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 8. Programming Mode DC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 9. Programming Mode AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

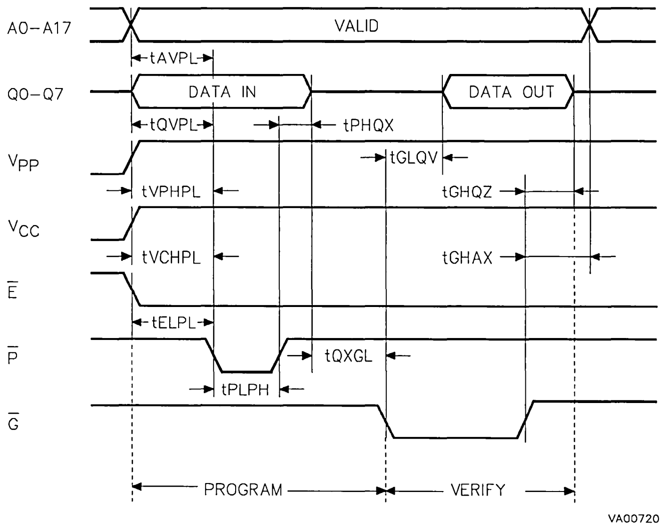
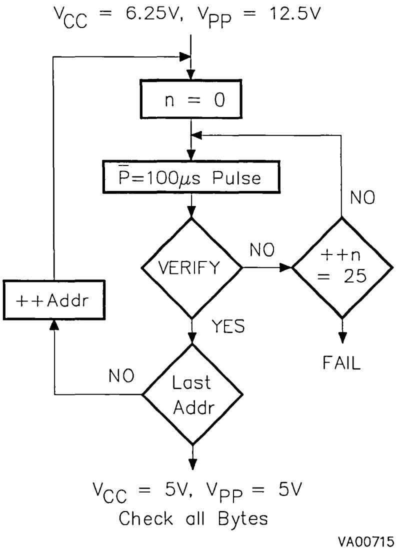

A0-A17
VALID
tAVPL
Q0-Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00720

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
P=100µs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00715

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 26 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V201s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V201 may be common. A TTL low level pulse applied to a M27V201's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V201. A high level $\overline{E}$ input inhibits the other M27V201s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V201. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V201, with $V_{PP} = V_{CC}$ = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27V201, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7. Note that the M27V201 and M27C2001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V201 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V201 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V201 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V201 window to prevent unintentional erasure. The recommended erasure procedure for the M27V201 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V201 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which

ORDERING INFORMATION

Example: M27V201 -200 K 6 TR

Speed		Package		Temperature Range		Option	
-200	200 ns	K	PLCC32	1	0 to 70 °C	TR	Tape & Reel
-250	250 ns	L	LCCC32W	6	–40 to 85 °C		

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

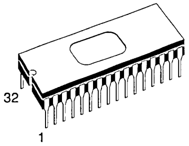
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

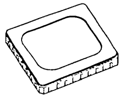
M27C4001

CMOS 4 Megabit (512K x 8) UV EPROM and OTP ROM

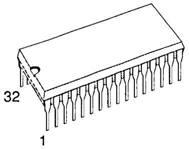
- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 50mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 48sec. (PRESTO II ALGORITHM)



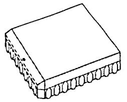
FDIP32W (F)



LCCC32W (L)



PDIP32 (B)



PLCC32 (C)

DESCRIPTION

The M27C4001 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 524,288 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4001 is offered in both Plastic Dual-in-Line and Plastic Leaded Chip Carrier packages.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

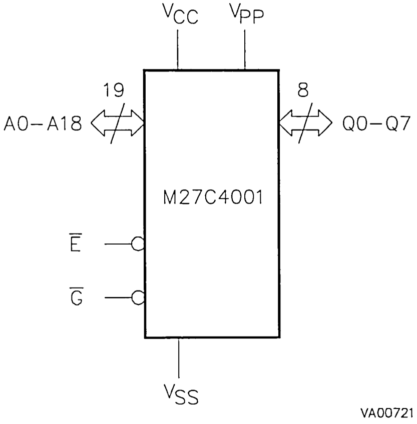


Figure 2A. DIP Pin Connections

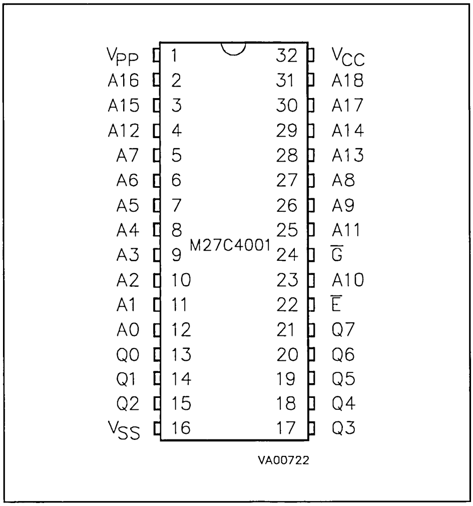

VPP 1
A16 2
A15 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
Q0 13
Q1 14
Q2 15
VSS 16
32 VCC
31 A18
30 A17
29 A14
28 A13
27 A8
26 A9
25 A11
24 $\overline{G}$
23 A10
22 $\overline{E}$
21 Q7
20 Q6
19 Q5
18 Q4
17 Q3
M27C4001
VA00722

Figure 2B. LCC Pin Connections

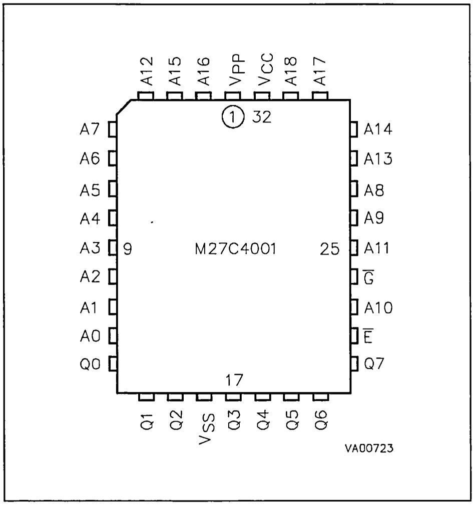

A12
A15
A16
VPP
VCC
A18
A17
1
32
A7
A6
A5
A4
A3
A2
A1
A0
Q0
9
M27C4001
25
A14
A13
A8
A9
A11
$\overline{G}$
A10
$\overline{E}$
Q7
17
Q1
Q2
VSS
Q3
Q4
Q5
Q6
VA00723

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The modes of operations of the M27C4001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4001 has a standby mode which reduces the active current from 50mA to 100µA. The

DEVICE OPERATION (cont'd)

M27C4001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C4001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C4001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

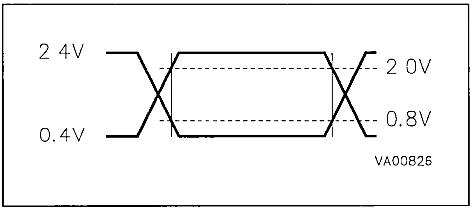

2 4V
0.4V
2 0V
0.8V
VA00826

Figure 4. AC Testing Load Circuit

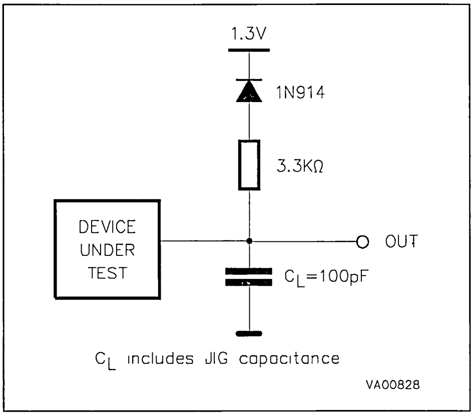

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L=100pF
C_L includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Figure 5. Read Mode AC Waveforms

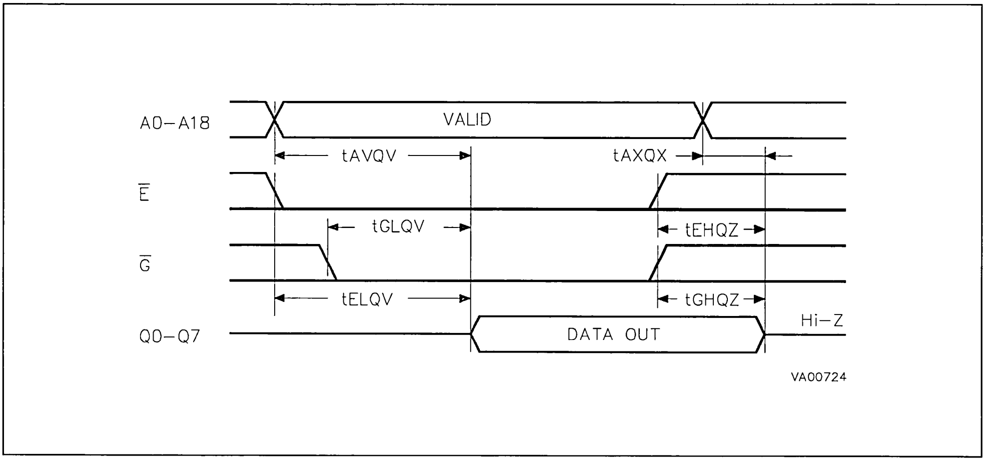

A0–A18
VALID
tAVQV
tAXQX
$\overline{E}$
tGLQV
tEHQZ
$\overline{G}$
tELQV
tGHQZ
Q0–Q7
DATA OUT
Hi–Z
VA00724

Table 6. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10MHz		70	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	$V_{CC} - 0.7V$		V

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001						Unit
				-80		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		80		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		80		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001				Unis
				-15		-20		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

2 This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

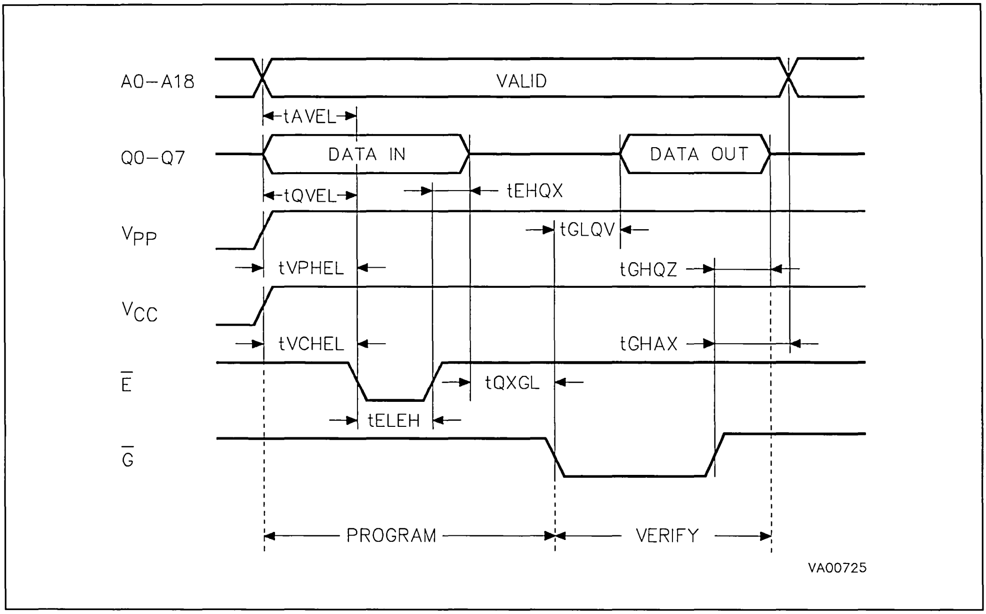
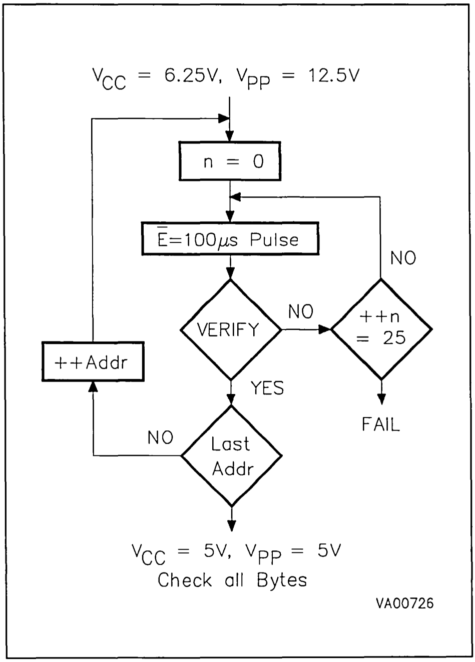

A0–A18
VALID
tAVEL
Q0–Q7
DATA IN
DATA OUT
tQVEL
tEHQX
VPP
tGLQV
tVPHEL
tGHQZ
VCC
tVCHEL
tGHAX
E
tQXGL
tELEH
G
PROGRAM
VERIFY
VA00725

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
E=100µs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00726

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 52 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C4001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C4001 may be common. A TTL low level pulse applied to a M27C4001's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C4001. A high level $\overline{E}$ input inhibits the other M27C4001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4001 with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C4001, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C4001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C4001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C4001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C4001 -80 X F 1 L

Speed	
-80	80 ns
-10	100 ns
-12	120 ns
-15	150 ns
-20	200 ns

V_{CC} Tolerance	
X	± 5%
blank	± 10%

Package	
F	FDIP32W
B	PDIP32
C	PLCC32
L	LCCC32W

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

Option	
L	Low Power
X	Additional Burn-in
TR	Tape & Reel

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

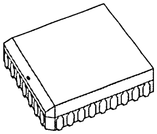
For further information on any aspect of this device, please contact our Sales Office nearest to you.

M27V401

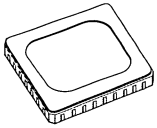
LOW VOLTAGE CMOS
4 Megabit (512K x 8) UV EPROM and OTP ROM

ADVANCE DATA

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER “CMOS” CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES FOR SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES OF AROUND 48sec. (PRESTO II ALGORITHM)
- M27V401 IS PROGRAMMABLE AS M27C4001 WITH IDENTICAL SIGNATURE



PLCC32 (K)



LCCC32W (L)

DESCRIPTION

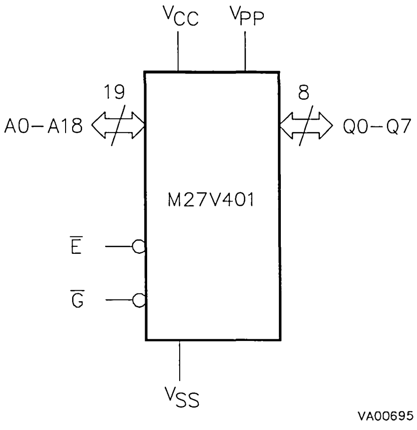
The M27V401 is a low voltage, low power 4 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 524,288 by 8 bits.

The M27V401 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



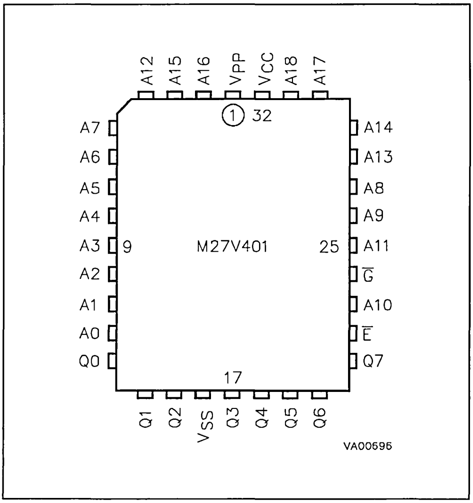
This is advance information on a new product now in development or undergoing evaluation Details are subject to change without notice.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. LCC Pin Connections



DESCRIPTION (cont'd)

The M27V401 can also be operated as a standard 4 Megabit EPROM (similar to M27C4001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27V401 is offered in Plastic Leaded Chip Carrier package.

DEVICE OPERATION

The modes of operation of the M27V401 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V401 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V401 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V401 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

DEVICE OPERATION (cont'd)

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V401 has been designed to be fully compatible with the M27C4001. As a result the M27V401 can be programmed as the M27C4001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V401 has the same electronic signature and uses the same PRESTO II algorithm .

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

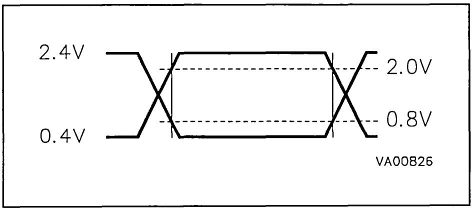


Figure 4. AC Testing Load Circuit

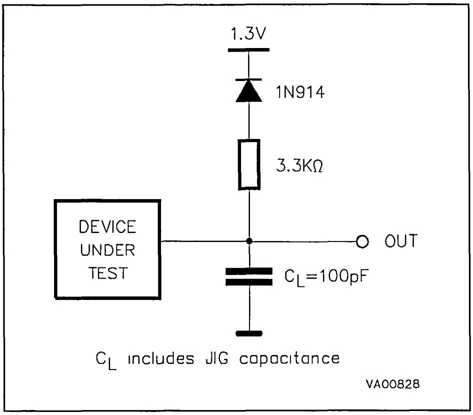


Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Table 6. Read Mode DC Characteristics [(1)]

(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz, V_{CC} = 5.5V		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

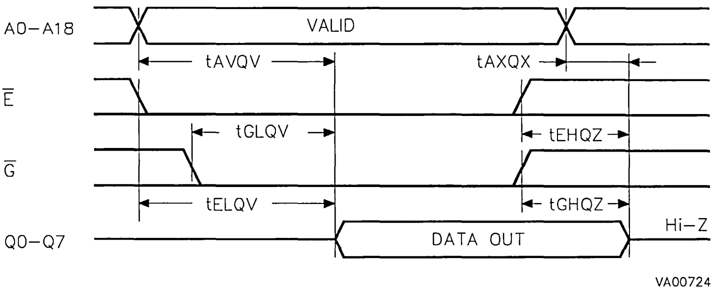
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics [1]
(T_A = 0 to 70 °C; V_{CC} = 3V to 5.5V unless specified; $V_{PP} = V_{CC}$)
(T_A = –40 to 85 °C; V_{CC} = 3.2V to 5.5V unless specified; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M27V401				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		130		150	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	80	0	80	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	80	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested.

Figure 5. Read Mode AC Waveforms



DEVICE OPERATION (cont'd)

When delivered (and after each erasure for UV EPROM), all bits of the M27V401 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V401 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

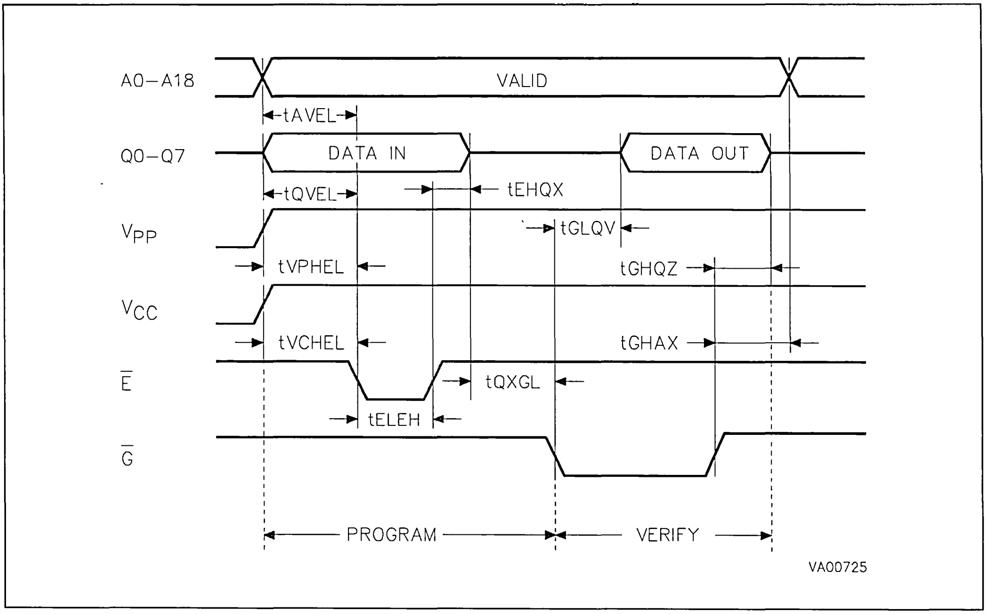
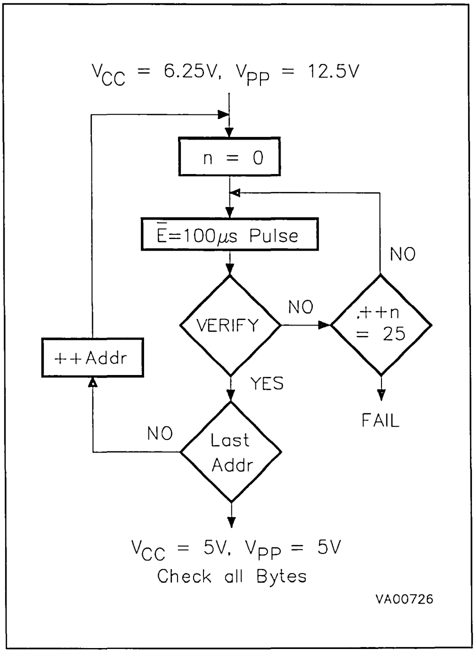

A0–A18
VALID
tAVEL
Q0–Q7
DATA IN
DATA OUT
tQVEL
tEHQX
VPP
tGLQV
tVPHEL
tGHQZ
VCC
tVCHEL
tGHAX
E
tQXGL
tELEH
G
PROGRAM
VERIFY
VA00725

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
E=100µs Pulse
VERIFY
NO
++n = 25
NO
YES
FAIL
++Addr
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00726

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 52 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V401s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V401 may be common. A TTL low level pulse applied to a M27V401's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V401. A high level $\overline{E}$ input inhibits the other M27V401s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH},, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V401. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V401, with $V_{PP} = V_{CC}$ = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27V401, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7. Note that the M27V401 and M27C4001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V401 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V401 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V401 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V401 window to prevent unintentional erasure. The recommended erasure procedure for the M27V401 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V401 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which

ORDERING INFORMATION

Example: M27V401 -200 K 6 TR

Speed		Package		Temperature Range		Option	
-200	200 ns	K	PLCC32	1	0 to 70 °C	TR	Tape & Reel
-250	250 ns	L	LCCC32W	6	–40 to 85 °C		

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

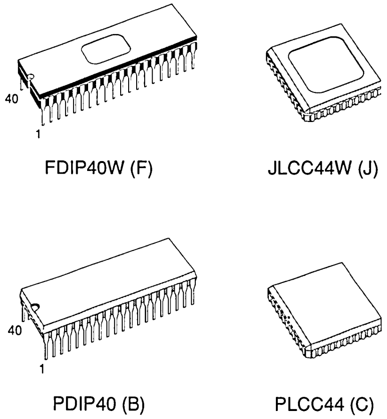
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M27C4002

CMOS 4 Megabit (256K x 16) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 100ns
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER “CMOS” CONSUMPTION:
  - Active Current 50mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES OF AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C4002 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 16 bits.

The Window Ceramic Frit-Seal Dual-in-Line and J-Lead Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4002 is offered in both Plastic Dual-in-Line and Plastic Leaded Chip Carrier packages.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

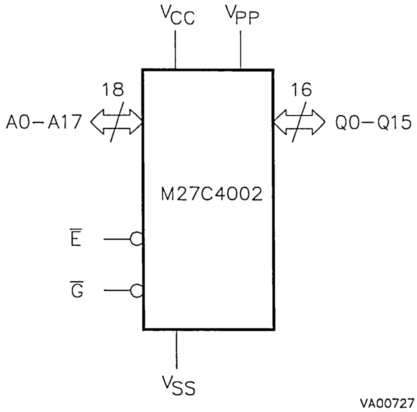


Figure 2A. DIP Pin Connections

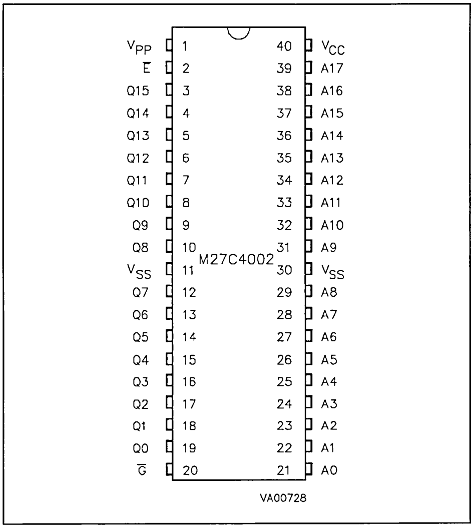
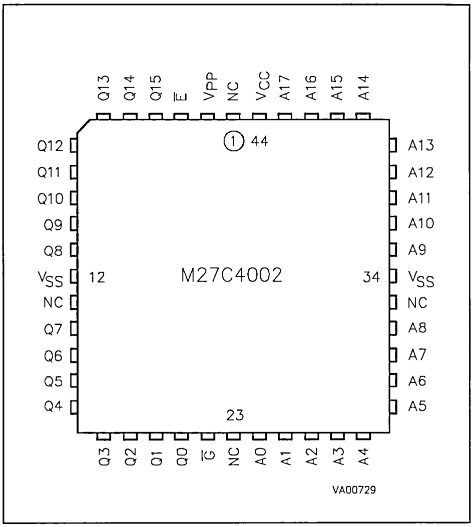

VPP 1 40 VCC
Ē 2 39 A17
Q15 3 38 A16
Q14 4 37 A15
Q13 5 36 A14
Q12 6 35 A13
Q11 7 34 A12
Q10 8 33 A11
Q9 9 32 A10
Q8 10 31 A9
VSS 11 30 VSS
Q7 12 29 A8
Q6 13 28 A7
Q5 14 27 A6
Q4 15 26 A5
Q3 16 25 A4
Q2 17 24 A3
Q1 18 23 A2
Q0 19 22 A1
Ḡ 20 21 A0
M27C4002
VA00728

Figure 2B. LCC Pin Connections


Q13 Q14 Q15 Ē VPP NC VCC A17 A16 A15 A14
① 44
Q12 Q11 Q10 Q9 Q8 VSS NC Q7 Q6 Q5 Q4
12
M27C4002
34
A13 A12 A11 A10 A9 VSS NC A8 A7 A6 A5
23
Q3 Q2 Q1 Q0 Ḡ NC A0 A1 A2 A3 A4
VA00729

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature: grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DEVICE OPERATION

The modes of operations of the M27C4002 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4002 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4002 has a standby mode which reduces the active current from 50mA to 100µA. The

DEVICE OPERATION (cont'd)

M27C4002 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the output capacitive and inductive loading of the device.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C4002 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C4002 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	1	0	0	44h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

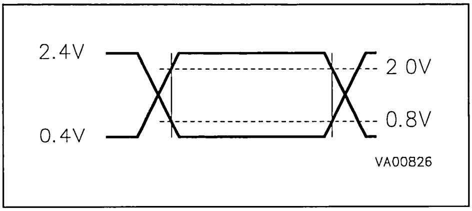

2.4V
0.4V
2 0V
0.8V
VA00826

Figure 4. AC Testing Load Circuit

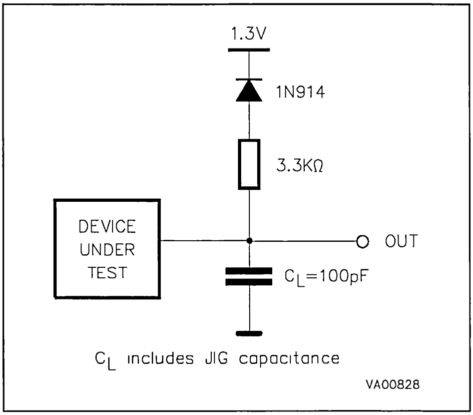

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
CL includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Figure 5. Read Mode AC Waveforms

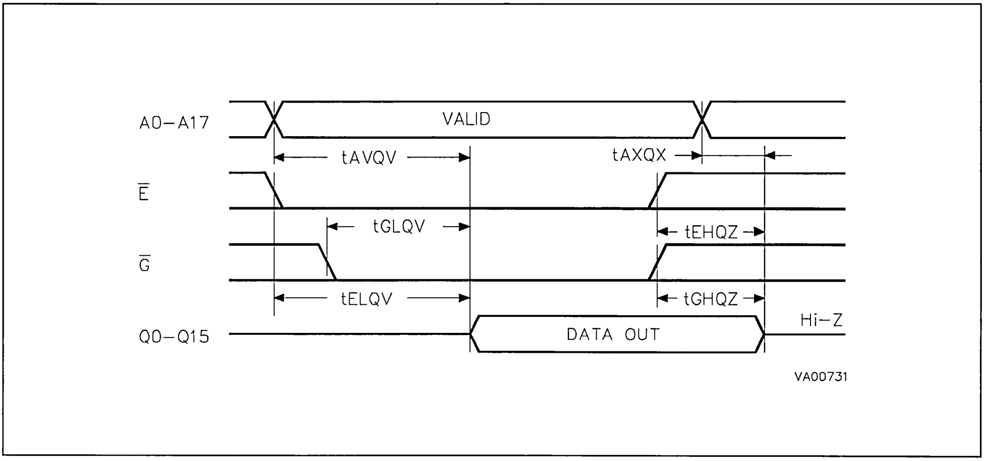

A0–A17
VALID
tAVQV
tAXQX
E̅
tGLQV
tEHQZ
G̅
tELQV
tGHQZ
Q0–Q15
DATA OUT
Hi–Z
VA00731

Table 6. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10MHz		70	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4002				Unit
				-10		-12		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4002				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is sampled only and not 100% tested

Table 8. Programming Mode DC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 9. Programming Mode AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2 This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

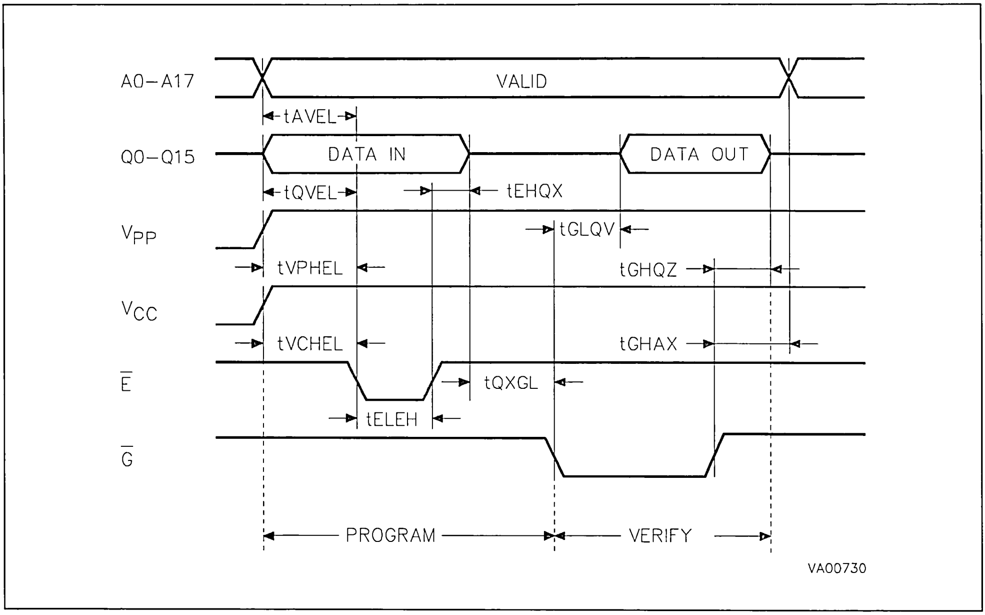
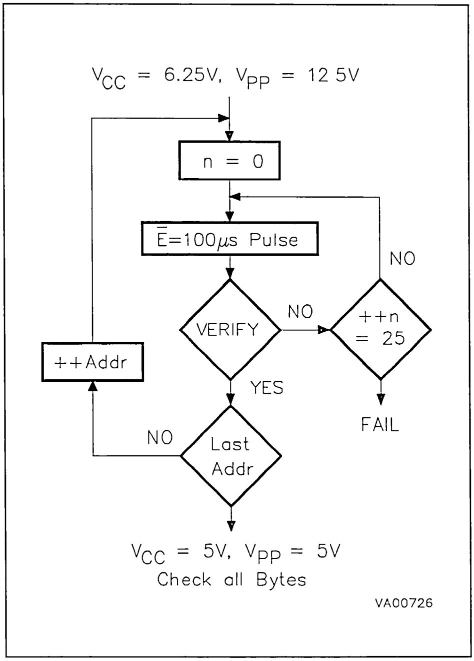

A0–A17
VALID
tAVEL
Q0–Q15
DATA IN
DATA OUT
tQVEL
tEHQX
VPP
tGLQV
tVPHEL
tGHQZ
VCC
tVCHEL
tGHAX
E
tQXGL
tELEH
G
PROGRAM
VERIFY
VA00730

Figure 7. Programming Flowchart


VCC = 6.25V, VPP = 12.5V
n = 0
E=100µs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all Bytes
VA00726

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 24 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C4002s in parallel with different data is also easily accomplished. Except for E, all like inputs including G of the parallel M27C4002 may be common. A TTL low level pulse applied to a M27C4002's E input, with V_{PP} at 12.75V, will program that M27C4002. A high level E input inhibits the other M27C4002s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with G at V_{IL}, E at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4002. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4002 with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C4002, these two identifier bytes are given here below, and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C4002 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C4002 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4002 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4002 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4002 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M27C4002 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27C4002 -10 X F 1 L

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-10	100 ns	X	± 5%	F	FDIP40W	1	0 to 70 °C	L	Low Power
-12	120 ns	blank	± 10%	B	PDIP40	6	–40 to 85 °C	X	Additional Burn-in
-15	150 ns			C	PLCC44			TR	Tape & Reel
-20	200 ns			L	JLCC44W				

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

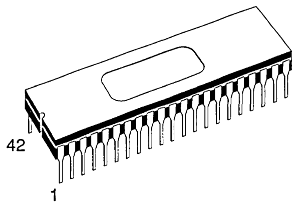
SGS-THOMSON
MICROELECTRONICS

M27C160

CMOS 16 Megabit (2M x 8 or 1M x 16) UV EPROM

ADVANCE DATA

- FAST ACCESS TIME: 150ns
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 16 Megabit, 42 Pin, MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
  - Active Current 70mA at 8MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE 12.5V ± 0.3V
- PROGRAMMING TIME OF AROUND 10sec. (PRESTO III ALGORITHM)



FDIP42W (F)

DESCRIPTION

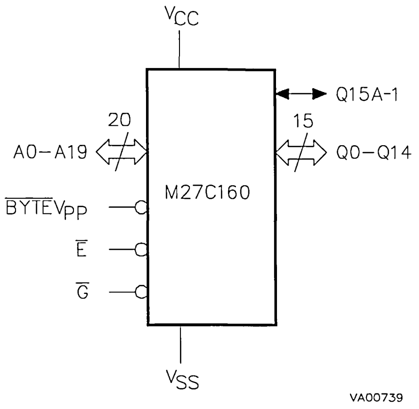
The M27C160 is a 16 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 2M words of 8 bit or 1M words of 16 bit. The pin-out is compatible with a 16 Megabit Mask ROM.

The 42 pin Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

Table 1. Signal Names

A0 - A19	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{\text{BYTE}}V_{PP}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



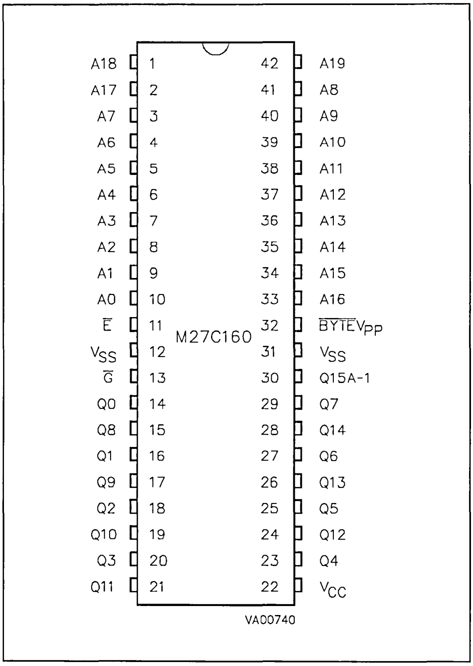
This is advance information on a new product now in development or undergoing evaluaion Detail are subject to change without notice

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1	0 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 80	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. DIP Pin Connections



DEVICE OPERATION

The operating modes of the M27C160 are listed in the Operating Modes Table. A single 5V supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}V_{PP}$ pin. When $\overline{BYTE}V_{PP}$ is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the $\overline{BYTE}V_{PP}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C160 has two control inputs, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected. The $\overline{E}$ signal is the power control and should be used for device selection. The $\overline{G}$ signal is the output control and should be used to gate data to the output pins. With $\overline{E}=V_{IL}$ and $\overline{G}=V_{IL}$ the output data will be valid in a time t_{AVQV} after the all address lines are valid and stable. The Chip Enable to Output Valid time t_{ELQV} is equal to the Address Valid to output Valid time t_{AVQV}. When the Addresses are valid and $\overline{E}=V_{IL}$, the output data is valid after a time of t_{GLQV} from the falling edge of the Output Enable signal.

Standby Mode

The M27C160 has a standby mode which reduces the active current from 50mA (f = 5MHz) to 100µA. The standby mode is entered by applying a CMOS high level V_{CC} –0.2V to $\overline{E}$. When in the standby mode the outputs are in an high impedance state, independant of the $\overline{G}$ input level.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{BYTE}V_{PP}$	A9	Q0 - Q7	Q8 - Q14	Q15A-1
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IL}
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{IH}	V_{PP}	X	Data In	Data In	Data In
Verify	X	V_{IL}	V_{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes	Codes	Code

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7 or Q15	Q6 or Q14	Q5 or Q13	Q4 or Q12	Q3 or Q11	Q2 or Q10	Q1 or Q9	Q0 or Q8	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	0	1	B1h

Table 5. Read Mode DC Characteristics [1]
(T_A = 0 to 70 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 8Mhz		70	mA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
I_{OS}	Output Short Circuit Current	Note 2 and 3		100	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is sampled only and not tested 100%.
3. Output shortcircuited for no more than one second. No more than one output shorted at a time.

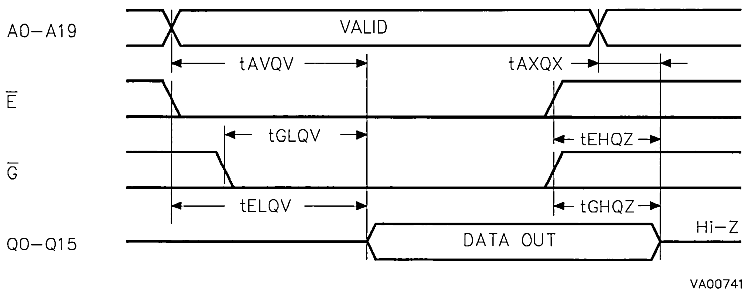
Table 6. Read Mode AC Characteristics [1]
(T_A = 0 to 70 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C160				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{BHQV}	t_{ST}	BYTE High to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		60		70	ns
t_{BLQZ} [2]	t_{STD}	BYTE Low to Output Hi-Z	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		50		60	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	5		5		ns
t_{BLQX}	t_{OH}	BYTE Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	5		5		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

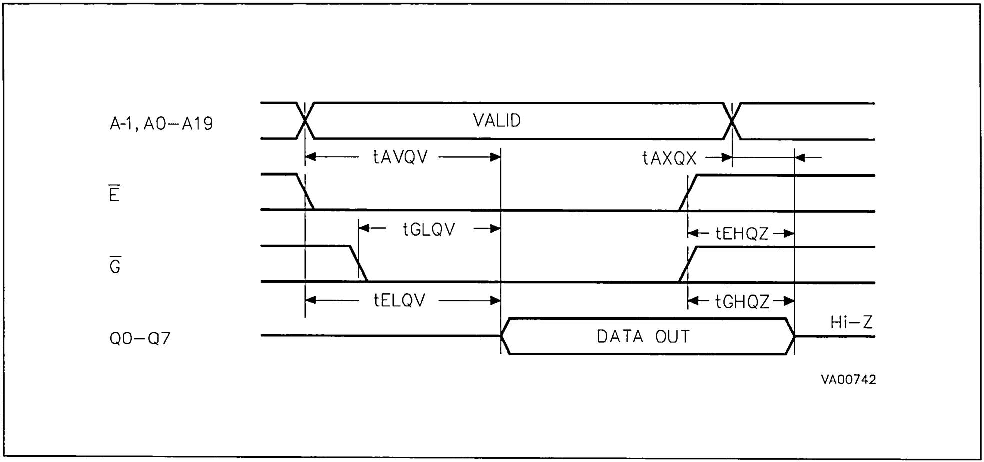
2. This parameter is sampled only and not 100% tested.

Figure 3. Word-Wide Read Mode AC Waveforms



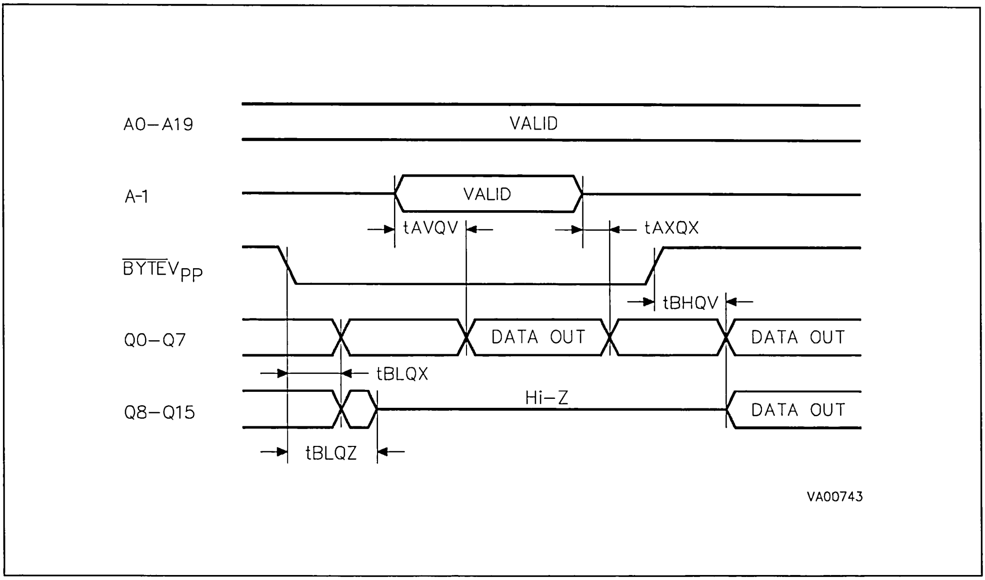
Note: $\overline{BYTE}V_{PP} = V_{IH}$

Figure 4. Byte-Wide Read Mode AC Waveforms


A-1, A0-A19
VALID
tAVQV
tAXQX
E
tGLQV
tEHQZ
G
tELQV
tGHQZ
Q0-Q7
DATA OUT
Hi-Z
VA00742

Note: $\overline{\text{BYTE}}V_{PP} = V_{IL}$

Figure 5. $\overline{\text{BYTE}}$ Transition AC Waveforms


A0-A19
VALID
A-1
VALID
tAVQV
tAXQX
BYTEVPP
tBHQV
Q0-Q7
DATA OUT
DATA OUT
tBLQX
Q8-Q15
Hi-Z
DATA OUT
tBLQZ
VA00743

Note: $\overline{E}$ and $\overline{G} = V_{IL}$

AC Measurement Conditions

Input Rise and Fall Times	< 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 6. AC Testing Input Output Waveforms

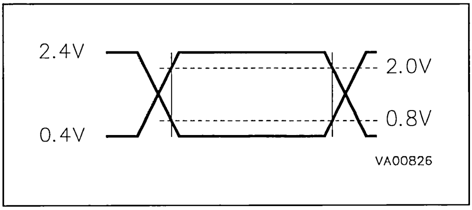


Figure 7. AC Testing Load Circuit

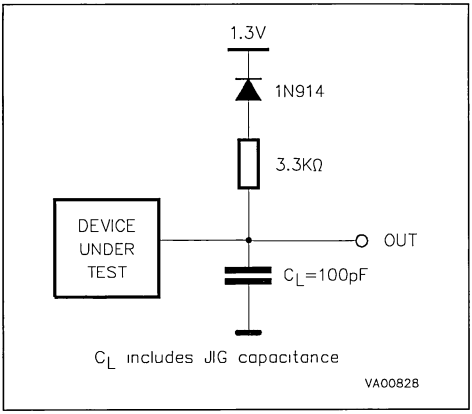


Table 7. Capacitance (TA = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{\text{BYTE}}V_{PP}$)	$V_{IN} = 0V$		10	pF
	Input Capacitance ($\overline{\text{BYTE}}V_{PP}$)	$V_{IN} = 0V$		120	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		12	pF

Note: This parameter is sampled only and not tested 100%

Table 8. Programming Mode DC Characteristics [1]

(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±1	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHAV}	t_{VPS}	V_{PP} High to Address Valid		2		µs
t_{VCHAV}	t_{VCS}	V_{CC} High to Address Valid		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		9.5	10.5	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			120	ns
t_{GHQZ} [2]	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms

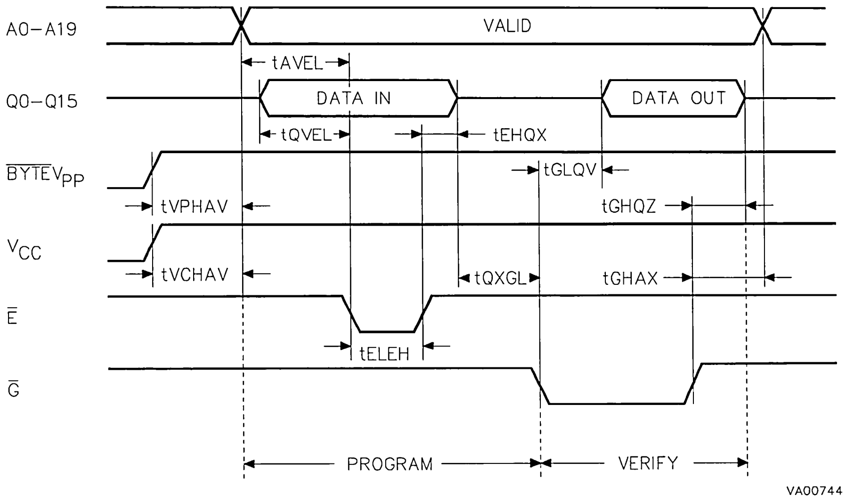
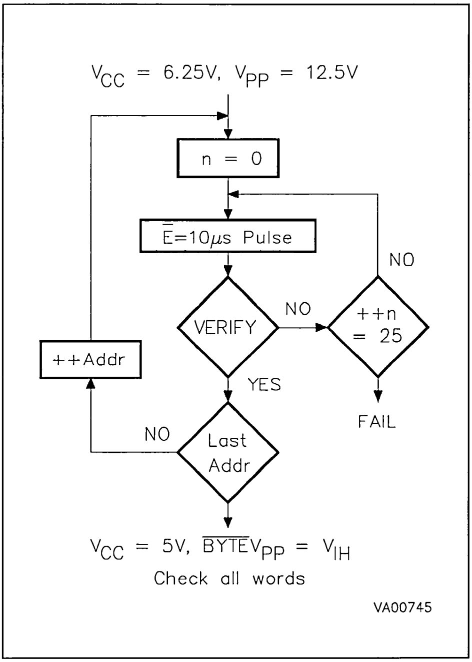

A0–A19
VALID
tAVEL
Q0–Q15
DATA IN
DATA OUT
tQVEL
tEHQX
BYTEVPP
tGLQV
tVPHAV
tGHQZ
VCC
tVCHAV
tQXGL
tGHAX
E
tELEH
G
PROGRAM
VERIFY
VA00744

Figure 9. Programming Flowchart



Output Disable Mode

When EPROMs are used in memory arrays two line output control should be used. This function uses the output disable mode which allows:

a. the lowest possible power consumption

b. complete assurance that output bus contention will not occur

For the best use of the two control lines $\overline{E}$ and $\overline{G}$, the input $\overline{E}$ should be decoded and used as the primary selection, while $\overline{G}$ should be made a common connection to all memories in the array. $\overline{G}$ should be connected to the $\overline{READ}$ signal of the system bus. This will ensure that all deselected devices are in the low power standby mode and that the output lines are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require carefull decoupliing of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependant on the capacititive and inductive loading of the device outputs. The associated transient voltage peaks can be supressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1μF ceramic capacitor is used on every device between V_{CC} and V_{SS}. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7μF electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programing

When first delivered, and after erasure for UV EPROMs, all bits are in the "1" logic state (Output High). Data with both "1's" and "0's" is applied and the "0s'" are programed into the memory array. For programing V_{CC} is raised to 6.25V. The M27C160 is in the Program Mode when V_{PP} is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. Data to be programed is applied 16 bits in parallel to the data output pins Q0 - Q15.

PRESTO III Algorithm

The PRESTO III Algorithm allows the whole 16 Megabit array to be programed with a guaranteed margin in a typical time of less than 10 seconds. The algorithm applies a series of 10μs program pulses to each word until a correct verify is made. During programing and verify a MARGIN MODE circuit is automatically activated to guarantee that each cell is programed with an adequate margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the neccessary threshold margin for each cell.

Program Inhibit

Multiple M27C160s may be programed in parallel with different data. This is done by putting in parallel all inputs except $\overline{E}$ and $\overline{G}$. With V_{CC} at 6.25V and V_{PP} at 12.5V, data should be applied to all devices and $\overline{G}$ placed at V_{IH}. Low level pulses on the $\overline{E}$ of one device will program that device.

Program Verify

After each program pulse a verify read is made by reading the data output with V_{CC} at 6.25V, V_{PP} at 12.5V and $\overline{G}$ placed at V_{IL}.

Electronic Signature

The Electronic Signature Mode allows a binary code to be read from the EPROM which identifies the Manufacturer and Device Type. These codes are intended to be used to match the programing equipment to the device being programed and its corresponding algorithm.

The Electronic Signature Mode is activated by applying a voltage V_{ID} of 12V to the Address line A9 and V_{IL} to all other Address lines, with $\overline{E}$ and $\overline{G}$ at V_{IL} and $\overline{BYTE}$ at V_{IH}. The identifier bytes may be read from either Q0-Q7 or Q8-Q15. With Address line A0 at V_{IL} the byte output is the Manufacture's code, with A0 at V_{IH} the byte identifies the Device Type. The codes for the SGS-THOMSON M27C160 are shown in the table.

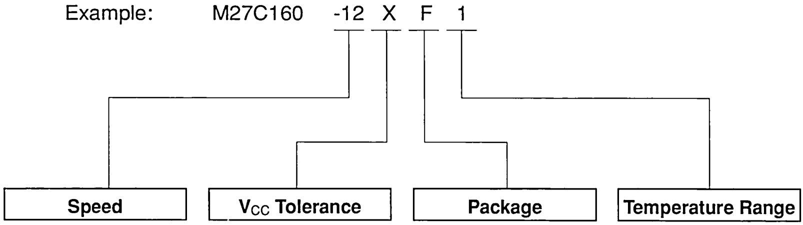
Erasure

The erasure of the M27C160 begins when the cells are exposed to light of wavelengths shorter than approximately 4000 Å. Sunlight and some types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Constant exposure to room level fluorescent lighting could erase a typical EPROM in about 3 years, while it takes approximately 170 hours to cause erasure when exposed to direct sunlight. To prevent accidental erasure it is recommended that opaque labels be placed over the M27C160 window.

The erase procedure for the M27C160 is exposure to UV light with a wavelength of 2537 Å. The integrated dose (UV intensity x time) for erasure should be a minimum of 15 W-sec/cm^2. The erase time with this dosage is 15 to 20 minutes using an UV lamp with 12,000 µW/cm^2 rating. The M27C160 should be placed within 2.5cm of the lamp tube during erasure. No filter should be used on the lamp.

ORDERING INFORMATION

Example: M27C160 -12 X F 1



Speed		V_{CC} Tolerance		Package		Temperature Range	
-150	150 ns	X	± 5%	F	FDIP42W	1	0 to 70 °C
-200	200 ns	blank	± 10%				

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

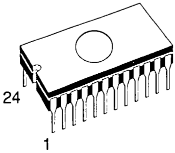
NMOS EPROM

SGS-THOMSON
MICROELECTRONICS

M2716

NMOS 16K (2K x 8) UV EPROM

- 2048 x 8 ORGANIZATION
- 525 mW Max ACTIVE POWER, 132 mW Max STANDBY POWER
- ACCESS TIME:
  - M2716-1 is 350ns
  - M2716 is 450ns
- SINGLE 5V SUPPLY VOLTAGE
- STATIC-NO CLOCKS REQUIRED
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH TIED-OR- CAPABILITY
- EXTENDED TEMPERATURE RANGE
- PROGRAMMING VOLTAGE: 25V



FDIP24W (F)

DESCRIPTION

The M2716 is a 16,384 bit UV erasable and electrically programmable memory EPROM, ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M2716 is housed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A10	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$P	Chip Enable / Program
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

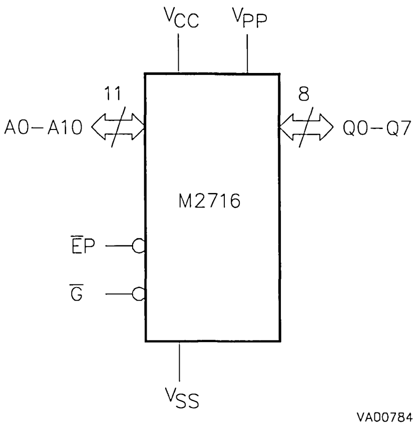
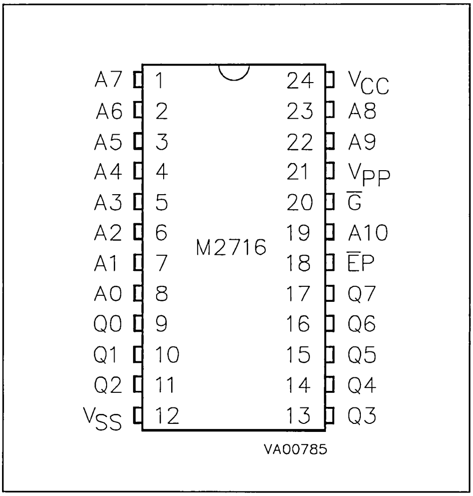


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{CC}	Supply Voltage		–0.3 to 6	V
V_{IO}	Input or Output Voltages		–0.3 to 6	V
V_{PP}	Program Supply		–0.3 to 26.5	V
P_D	Power Dissipation		1.5	W

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The M2716 has 3 modes of operation in the normal system environment. These are shown in Table 3.

Read Mode. The M2716 read operation requires that $\overline{G}$ = V_{IL}, $\overline{EP}$ = V_{IL} and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after time t_{AVQV}, t_{GLQV} or t_{ELQV} (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode. The M2716 is deselected by making $\overline{G}$ = V_{IH}. This mode is independent of $\overline{EP}$ and the condition of the addresses. The outputs are Hi-Z when $\overline{G}$ = V_{IH}. This allows tied-OR of 2 or more M2716's for memory expansion.

Standby Mode (Power Down). The M2716 may be powered down to the standby mode by making $\overline{EP}$ = V_{IH}. This is independent of $\overline{G}$ and automatically puts the outputs in the Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V. Access time at power up remains either t_{AVQV} or t_{ELQV} (see Switching Time Waveforms).

Programming

The M2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table 3 shows the 3 programming modes.

Program Mode. The M2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, sequential addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the $\overline{EP}$ pin. All input voltage levels including the program pulse on chip enable are TTL compatible.

The programming sequence is: with V_{PP} = 25V, V_{CC} = 5V, $\overline{G}$ = V_{IH} and $\overline{EP}$ = V_{IL}, an address is selected and the desired data word is applied to the output pins (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a

DEVICE OPERATION (cont'd)

pulse width between 45ms and 55ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than t_{PHPL} (max) on the program pin during programming. M2716's may be programmed in parallel in this mode.

Program Verify Mode. The programming of the M2716 may be verified either one byte at a time during the programming (as shown in Figure 6) or by reading all of the bytes out at the end of the programming sequence. This can be done with V_{PP} = 25V or 5V in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

Program Inhibit Mode. The program inhibit mode allows several M2716's to be programmed simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{G}$ = V_{IH} will put its outputs in the Hi-Z state.

ERASURE OPERATION

The M2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 power rating is used. The M2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age, it is therefore important to periodically check that the UV system is in good order.

This will ensure that the EPROMs are being completely erased. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Table 3. Operating Modes

Mode	$\overline{EP}$	$\overline{G}$	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IH} Pulse	V_{IH}	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{PP} or V_{CC}	Data Out
Program Inhibit	V_{IL}	V_{IH}	V_{PP}	Hi-Z
Deselect	X	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

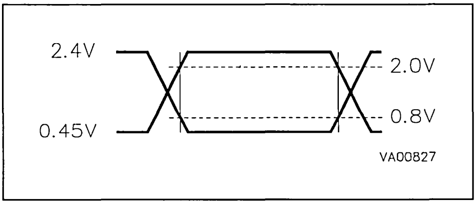


Figure 4. AC Testing Load Circuit

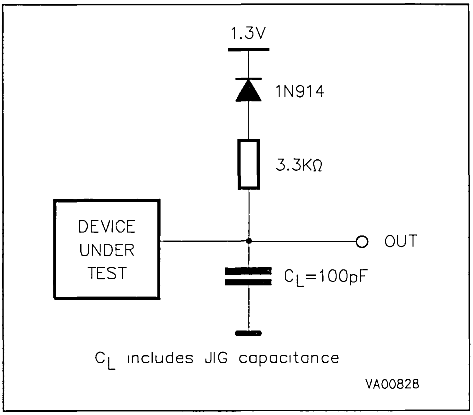


Table 4. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$, $\overline{E}P = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\overline{E}P = V_{IH}$, $\overline{G} = V_{IL}$		25	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics [1]
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2716				Unit
				-1		blank		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{EP} = V_{IL}$, $\overline{G} = V_{IL}$		350		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		350		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{EP} = V_{IL}$		120		120	ns
t_{EHQZ} [2]	t_{OD}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	100	0	100	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{EP} = V_{IL}$	0	100	0	100	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{EP} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested.

Figure 5. Read Mode AC Waveforms

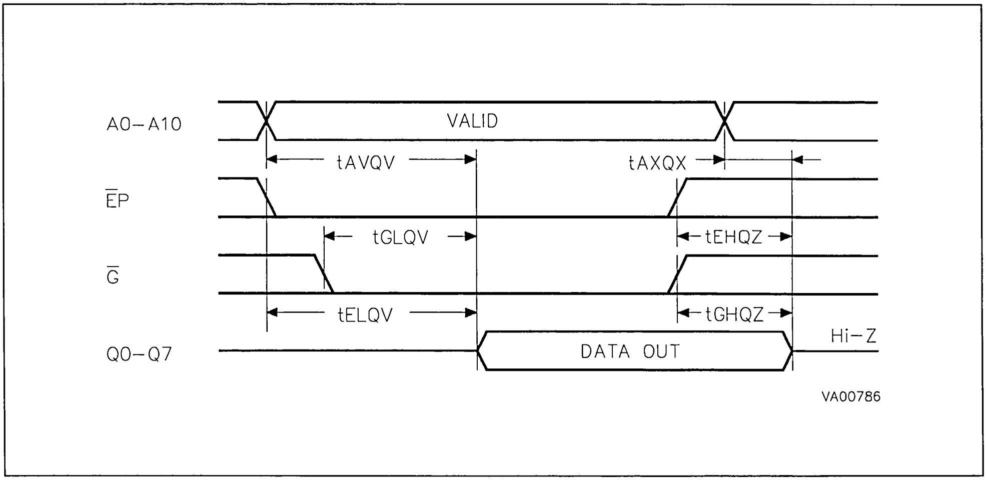


Table 7. Programming Mode DC Characteristics [1]
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current			5	mA
I_{PP1}	Program Current Pulse	$\overline{EP} = V_{IH}$ Pulse		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V

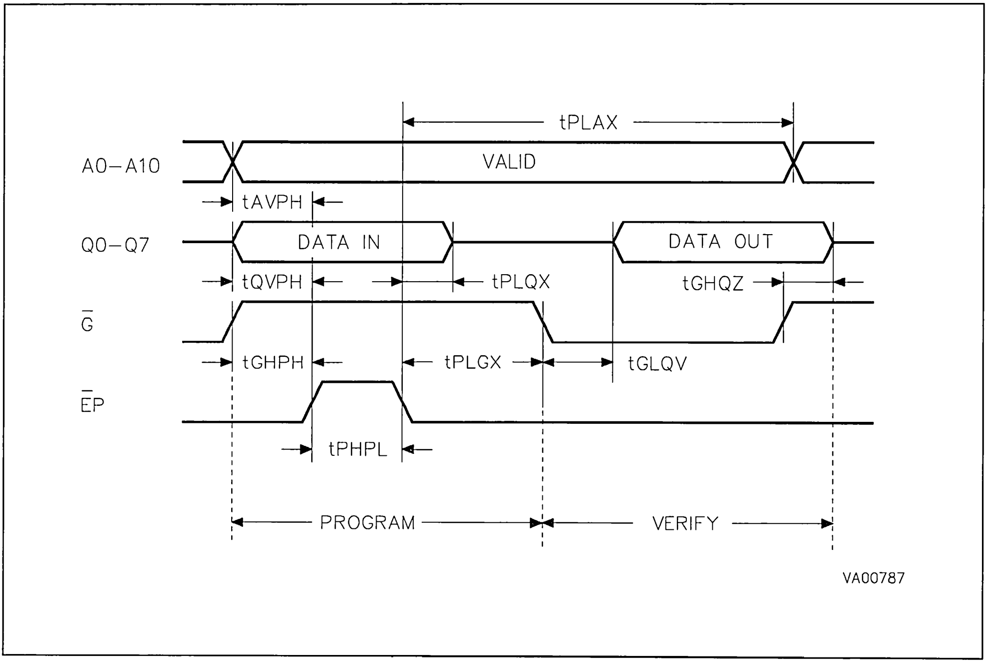
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 8. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVPH}	t_{AS}	Address Valid to Program High	$\overline{G} = V_{IH}$	2		µs
t_{QVPH}	t_{DS}	Input Valid to Program High	$\overline{G} = V_{IH}$	2		µs
t_{GHPH}	t_{OS}	Output Enable High to Program High		2		µs
t_{PL1PL2}	t_{PR}	Program Pulse Rise Time		5		ns
t_{PH1PH2}	t_{PF}	Program Pulse Fall Time		5		ns
t_{PHPL}	t_{PW}	Program Pulse Width		45	55	ms
t_{PLQX}	t_{DH}	Program Low to Input Transition		2		µs
t_{PLGX}	t_{OH}	Program Low to Output Enable Transition		2		µs
t_{GLQV}	t_{OE}	Output Enable to Output Valid	$\overline{EP} = V_{IL}$		120	ns
t_{GHQZ}	t_{DF}	Output Enable High to Output Hi-Z		0	100	ns
t_{PLAX}	t_{AH}	Program Low to Address Transition		2		µs

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms


tPLAX
A0–A10
VALID
tAVPH
Q0–Q7
DATA IN
DATA OUT
tQVPH
tPLQX
tGHQZ
G
tGHPH
tPLGX
tGLQV
EP
tPHPL
PROGRAM
VERIFY
VA00787

ORDERING INFORMATION

Example: M2716 -1 F 1

Speed and V_{CC} Tolerance	
-1	350 ns, 5V ±10%
blank	450 ns, 5V ±5%

Package	
F	FDIP24W

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

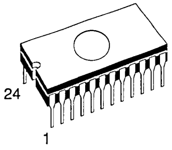
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M2732A

NMOS 32K (4K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING READ AND PROGRAM
- COMPLETELY STATIC



FDIP24W (F)

DESCRIPTION

The M2732A is a 32,768 bit UV erasable and electrically programmable memory EPROM. It is organized as 4,096 words by 8 bits. The M2732A with its single 5V power supply and with an access time of 200 ns, is ideal suited for applications where fast turn around and pattern experimentation one important requirements.

The M2732A is honsed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be then written to the clerice by following the programming procedure.

Table 1. Signal Names

A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

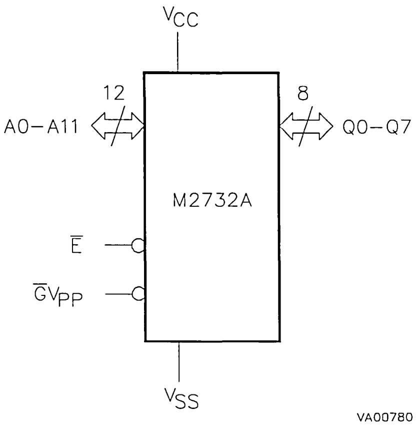
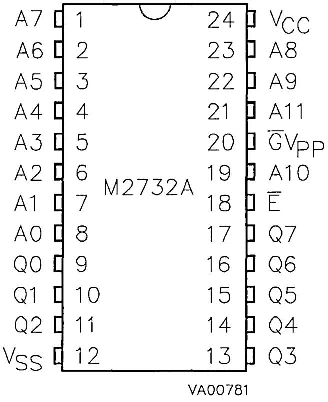


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6	V
V_{CC}	Supply Voltage		–0.6 to 6	V
V_{PP}	Program Supply Voltage		–0.6 to 22	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operation for the M2732A are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL level except for V_{PP}.

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVAQ}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{E}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{E}$ be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Programming

When delivered, and after each erasure, all bits of the M2732A are in the “1" state. Data is introduced by selectively programming "0’s" into the desired bit locations. Although only “0’s” will be programmed, both “1’s” and “0’s” can be presented in the data word. The only way to change a “0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{G}V_{PP}$ input is at 21V. A 0.1µF capacitor must be placed across $\overline{G}V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50ms, active low, TTL program pulse is applied to the $\overline{E}$ input. A program pulse must be applied at each address location to be programmed. Any location can be programmed at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55ms. The M2732A must not be programmed with a DC signal applied to the $\overline{E}$ input.

Programming of multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{E}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}V_{PP}$) of the parallel M2732As may be common. A TTL level program pulse applied to a M2732A’s $\overline{E}$ input with $\overline{G}V_{PP}$ at 21V will program that M2732A. A high level $\overline{E}$ input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is carried out with $\overline{G}V_{PP}$ and $\overline{E}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	V_{CC}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IL} Pulse	V_{PP}	V_{CC}	Data In
Verify	V_{IL}	V_{IL}	V_{CC}	Data Out
Program Inhibit	V_{IH}	V_{PP}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

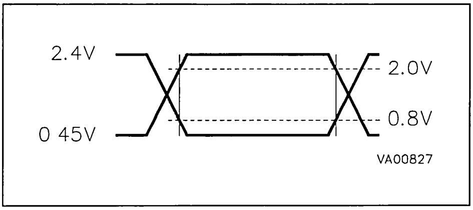

2.4V
0 45V
2.0V
0.8V
VA00827

Figure 4. AC Testing Load Circuit

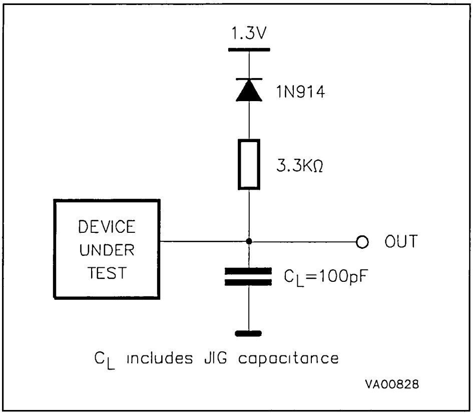

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L=100pF
C_L includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{G}V_{PP}$)	V_{IN} = 0V		6	pF
C_{IN1}	Input Capacitance ($\overline{G}V_{PP}$)	V_{IN} = 0V		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%

Figure 5. Read Mode AC Waveforms

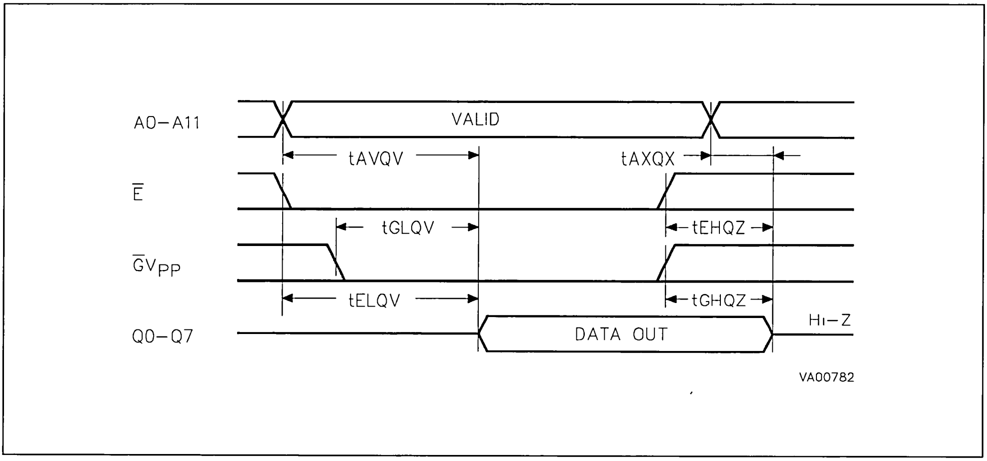

A0–A11
VALID
tAVQV
tAXQX
E̅
tGLQV
tEHQZ
G̅VPP
tELQV
tGHQZ
Q0–Q7
DATA OUT
Hi–Z
VA00782

Table 6. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Value		Unit
			Min	Max	
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$		35	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2732A								Unit
				-2, -20		blank, -25		-3		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		100		100		150		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

2. This parameter is sampled only and not 100% tested

Table 8. Programming Mode DC Characteristics (1)

(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

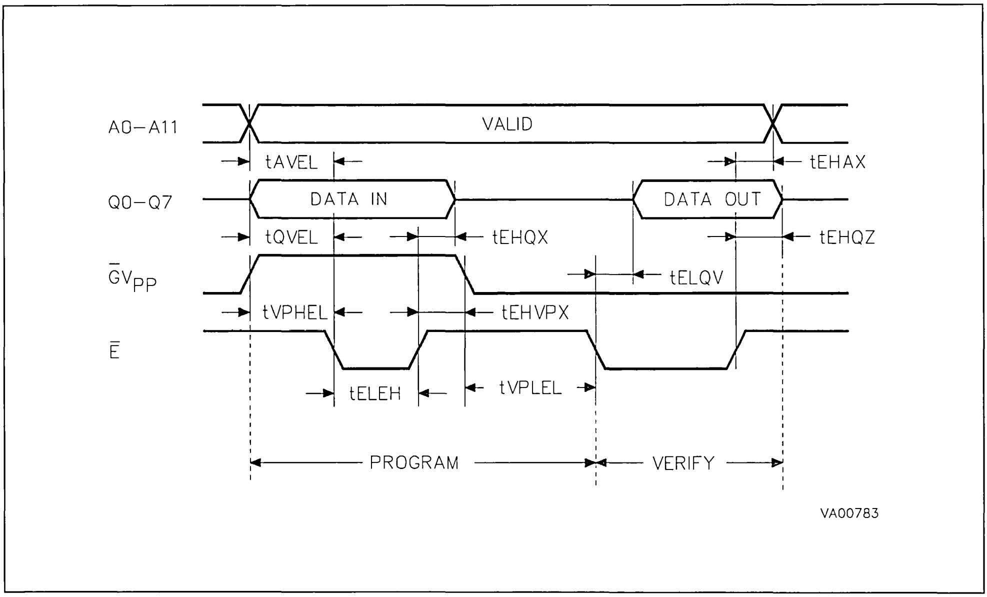
Table 9. Programming Mode AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
$t_{VPL1VPL2}$	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		45	55	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		1	µs
t_{EHQZ}	t_{DF}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Figure 6. Programming and Verify Modes AC Waveforms


A0–A11
VALID
tAVEL
tEHAX
Q0–Q7
DATA IN
DATA OUT
tQVEL
tEHQX
tEHQZ
$\overline{G}V_{PP}$
tELQV
tVPHEL
tEHVPX
$\overline{E}$
tELEH
tVPLEL
PROGRAM
VERIFY
VA00783

ORDERING INFORMATION

Example: M2732A -2 F 1

Speed and V$_{CC}$ Tolerance	
-2	200 ns, 5V ±5%
blank	250 ns, 5V ±5%
-3	300 ns, 5V ±5%
-4	450 ns, 5V ±5%
-20	200 ns, 5V ±10%
-25	250 ns, 5V ±10%

Package	
F	FDIP24W

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

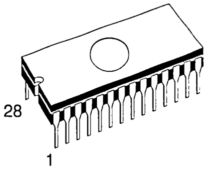
For a list of available options of Speed, V$_{CC}$ Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M2764A

NMOS 64K (8K x 8) UV EPROM

- FAST ACCESS TIME: 180ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M2764A is a 65,536 bit UV erasable and electrically programmable memory EPROM. It is organized as 8,192 words by 8 bits.

The M27C64A is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

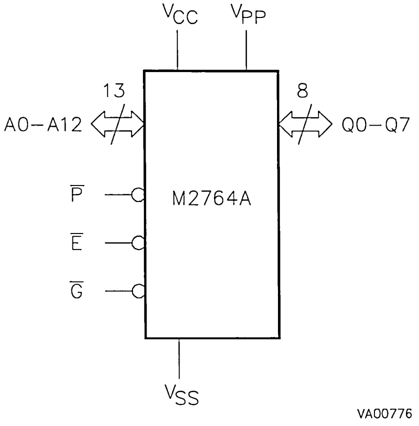
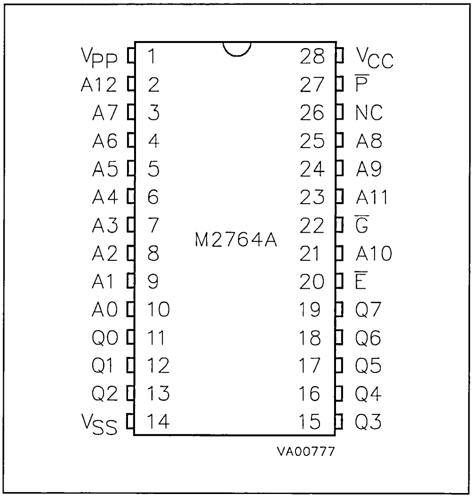


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.6 to 6.5	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. DIP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The seven modes of operations of the M2764A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M2764A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2764A has a standby mode which reduces the maximum active power current from 75mA to 35mA. The M2764A is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M2764A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2764A is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M2764A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes Out

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0 5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	0	0	0	08h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

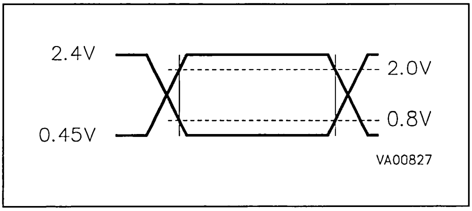

2.4V
0.45V
2.0V
0.8V
VA00827

Figure 4. AC Testing Load Circuit

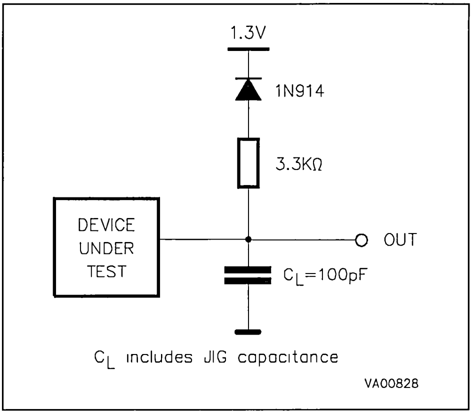

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
CL includes JIG capacitance
VA00828

Table 5. Capacitance ($T_A = 25$ °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		12	pF

Note: This parameter is sampled only and not tested 100%.

Figure 5. Read Mode AC Waveforms

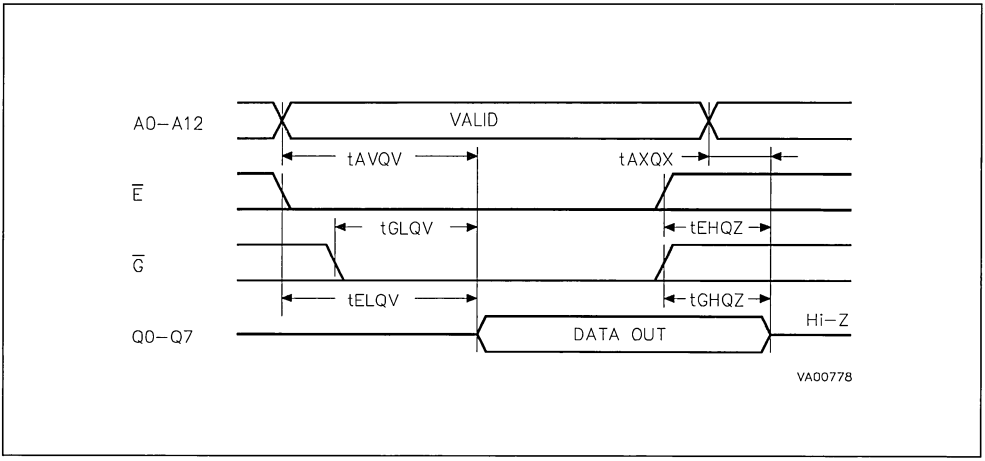

A0–A12
VALID
tAVQV
tAXQX
E
tGLQV
tEHQZ
G
tELQV
tGHQZ
Q0–Q7
DATA OUT
Hi–Z
VA00778

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		75	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		35	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M2764A						Unit
				-1		-2, -20		blank, -25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		180		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		180		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		65		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	55	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M2764A				Unit
				-3		-4		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$,		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$V_{IL} \leq V_{IN} \leq V_{IH}$		±10	µA
I_{CC}	Supply Current			75	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
VA9	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{PLPH}	t_{OPW}	Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending of the multiplication value of the iteration counter.
4 This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

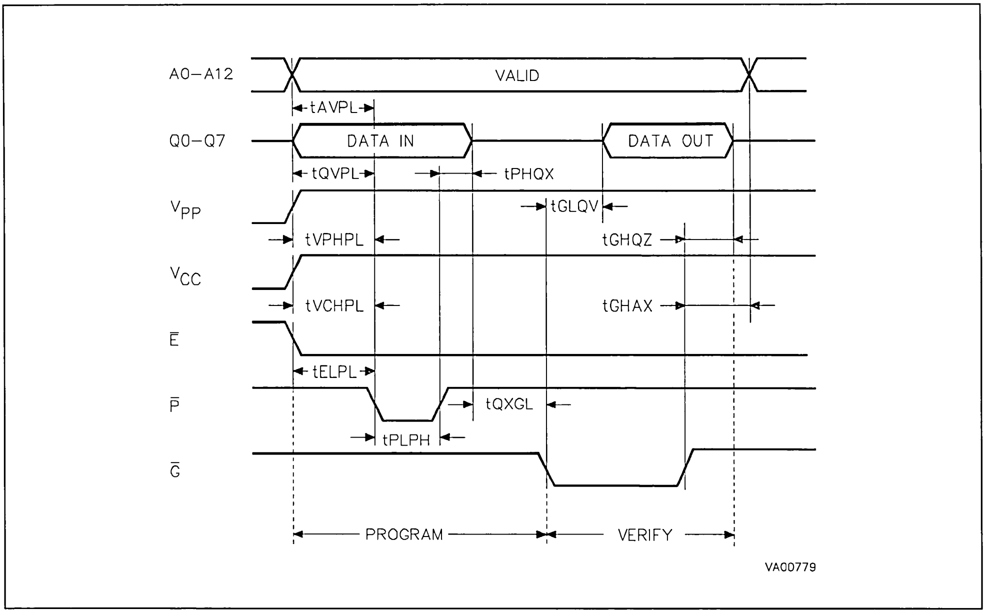
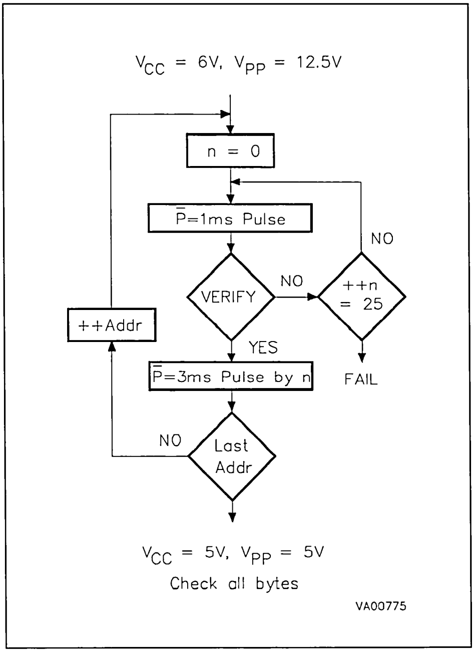

A0–A12
VALID
tAVPL
Q0–Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00779

Figure 7. Fast Programming Flowchart


VCC = 6V, VPP = 12.5V
n = 0
P=1ms Pulse
VERIFY
NO
++n = 25
NO
YES
FAIL
P=3ms Pulse by n
++Addr
NO
Last Addr
VCC = 5V, VPP = 5V
Check all bytes
VA00775

DEVICE OPERATION (cont'd)

been successfully programmed. A flowchart of the M2764A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram.

The duration of the initial $\overline{P}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied to a particular M2764A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V and V_{PP} = 5V.

Program Inhibit

Programming of multiple M2764A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M2764A may be common. A TTL low pulse applied to a M2764A's $\overline{E}$ input, with V_{PP} at 12.5V, will program that M2764A. A high level $\overline{E}$ input inhibits the other M2764As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$ and $V_{PP} = 12.5V$.

Electronic Signature

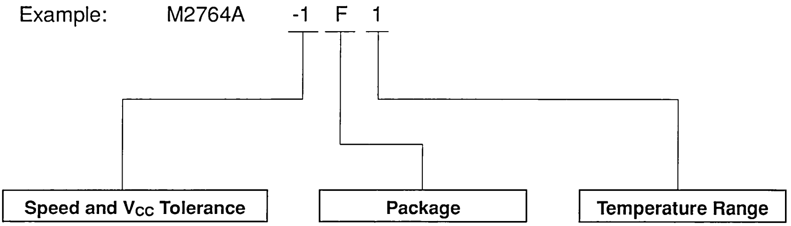
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M2764A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M2764A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON M2764A, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPPROM)

The erasure characteristic of the M2764A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2764A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2764A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2764A window to prevent unintentional erasure. The recommended erasure procedure for the M2764A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M2764A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION



Speed and V_{CC} Tolerance	
-1	180 ns, 5V ±5%
-2	200 ns, 5V ±5%
blank	250 ns, 5V ±5%
-3	300 ns, 5V ±5%
-4	450 ns, 5V ±5%
-20	200 ns, 5V ±10%
-25	250 ns, 5V ±10%

Package	
F	FDIP28W

Temperature Range	
1	0 to 70 °
6	–40 to 85 °C

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

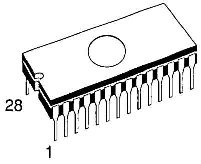
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M27128A

NMOS 128K (16K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5 V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27128A is a 131,072 bit UV erasable and electrically programmable memory EPROM. It is organized as 16,384 words by 8 bits.

The M27128A is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A13	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

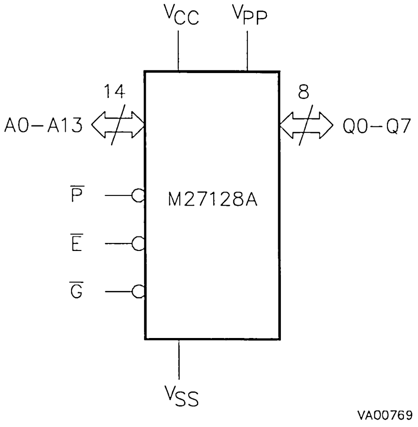
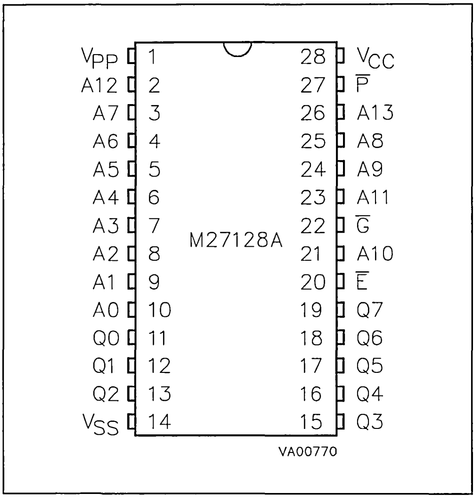


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.25	V
V_{CC}	Supply Voltage		–0.6 to 6.25	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. DIP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The seven modes of operation of the M27128A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27128A has a standby mode which reduces the maximum active power current from 85mA to 40mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPPROM), all bits of the M27128A are in the “1" state. Data is introduced by selectively programming ”0s" into the desired bit locations. Although only “0s” will be programmed, both “1s” and “0s” can be present in the data word. The only way to change a “0” to a ”1" is by ultraviolet light erasure.

The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes Out

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0 5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	0	0	1	89h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

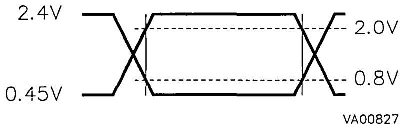

2.4V
0.45V
2.0V
0.8V
VA00827

Figure 4. AC Testing Load Circuit

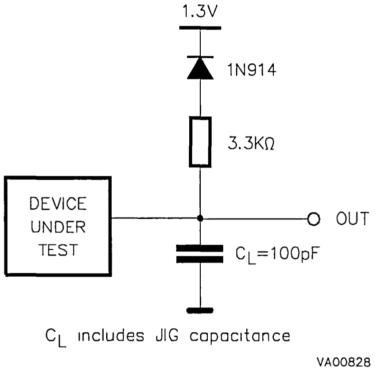

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L=100pF
C_L includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	=	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	=	12	pF

Note: This parameter is sampled only and not tested 100%.

Figure 5. Read Mode AC Waveforms

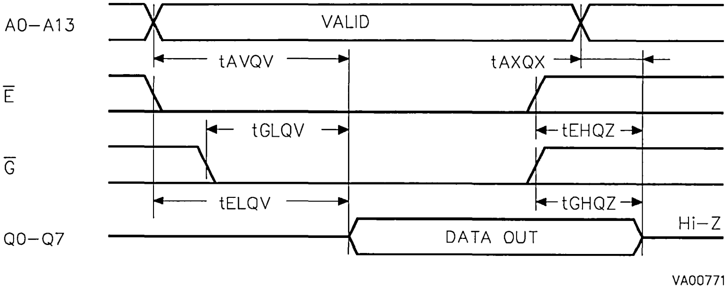

A0–A13
VALID
tAVQV
tAXQX
E̅
tGLQV
tEHQZ
G̅
tELQV
tGHQZ
Hi–Z
Q0–Q7
DATA OUT
VA00771

Table 6. Read Mode DC Characteristics [1]

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		75	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		35	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	=	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics [1]

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; $V_{PP} = V_{CC}$)

Symbol	Alt	Parameter	Test Condition	M27128A								Unit
				-2, -20		blank, -25		-3, -30		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		100		120		150	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{PLPH}	t_{OPW}	Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.
4 This parameter is sampled only and not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

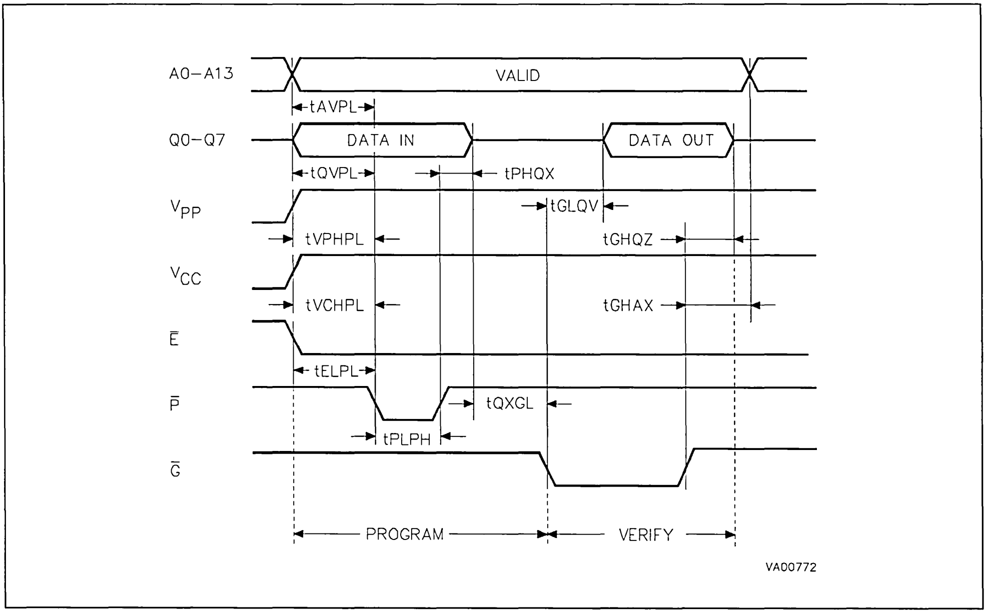
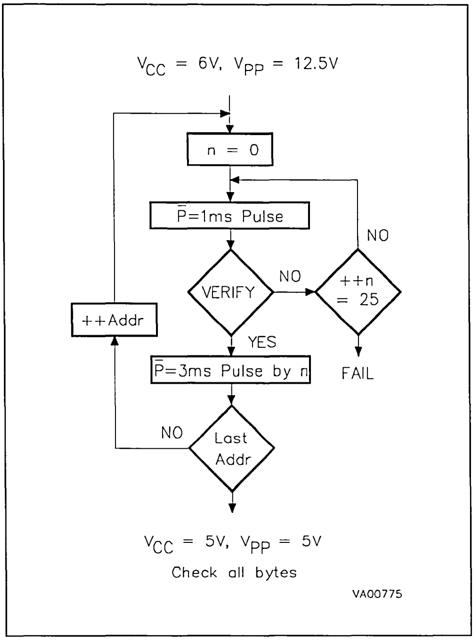

A0–A13
VALID
tAVPL
Q0–Q7
DATA IN
DATA OUT
tQVPL
tPHQX
VPP
tGLQV
tVPHPL
tGHQZ
VCC
tVCHPL
tGHAX
E
tELPL
P
tQXGL
tPLPH
G
PROGRAM
VERIFY
VA00772

Figure 7. Programming Flowchart


VCC = 6V, VPP = 12.5V
n = 0
P=1ms Pulse
VERIFY
NO
++n = 25
NO
YES
FAIL
++Addr
P=3ms Pulse by n
NO
Last Addr
VCC = 5V, VPP = 5V
Check all bytes
VA00775

DEVICE OPERATION (cont'd)

continually monitored to determine when it has been successfully programmed. A flowchart of the M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial P pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5 and V_{PP} = 5V.

Program Inhibit

Programming of multiple M27128A's in parallel with different data is also easily accomplished. Except for E, all like inputs (including G) of the parallel M27128A may be common. A TTL low pulse applied to a M27128A's E input, with V_{PP} = 12.5V, will program that M27128A. A high level E input inhibits the other M27128As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, $\overline{P}$ = V_{IH} and V_{PP} at 12.5V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the25°C ± 5°C ambient temperature range that is required when programming the M27128A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27128A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27128A, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27128A should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Example: M27128A -2 F 1

Speed and V_{CC} Tolerance	
-2	200 ns, 5V ±5%
blank	250 ns, 5V ± 5%
-3	300 ns, 5V ± 5%
-4	450 ns, 5V ± 5%
-20	200 ns, 5V ± 10%
-25	250 ns, 5V ± 10%
-30	300 ns, 5V ± 10%

Package	
F	FDIP28W

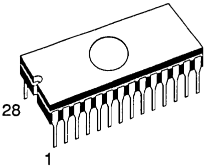
Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

NMOS 256K (32K x 8) UV EPROM

- FAST ACCESS TIME: 170ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27256 is a 262,144 bit UV erasable and electrically programmable memory EPROM. It is organized as 32.768 words by 8 bits.

The M27256 is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user toexpose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure

Figure 1. Logic Diagram

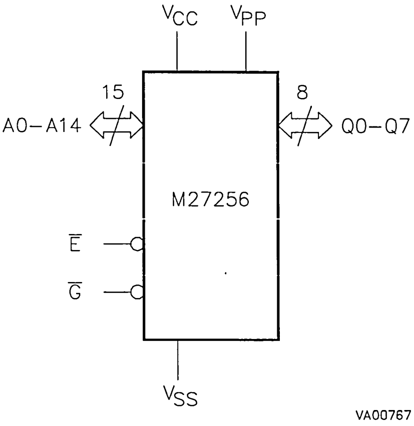


Table 1. Signal Names

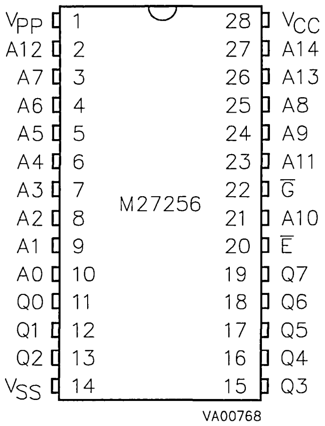
A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.25	V
V_{CC}	Supply Voltage		–0.6 to 6.25	V
V_{A9}	VA9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27256 has a standby mode which reduces the maximum active power current from 100mA to 40mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitors should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programmain

When delivered, (and after each erasure for UV EPROM), all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the Flowchart. The Fast Programming Algorithm utilizes two different pulse types : initial and over-program. The duration of the initial $\overline{E}$ pulse(s) is 1ms, which will then be followed by a longer over-program pulse of length 3ns by n (n is equal to the number of the initial one millisecond pulses applied

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

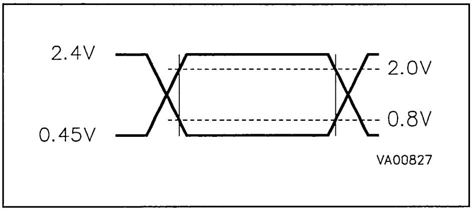

2.4V
0.45V
2.0V
0.8V
VA00827

Figure 4. AC Testing Load Circuit

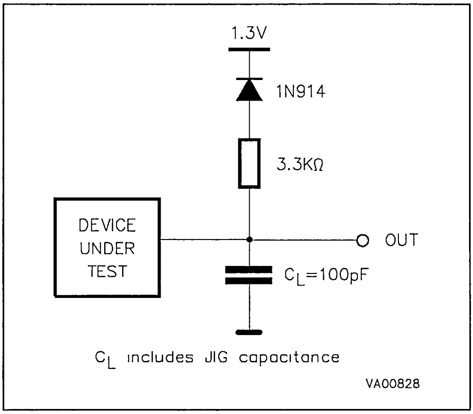

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L=100pF
C_L includes JIG capacitance
VA00828

Table 5. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Figure 5. Read Mode AC Waveforms

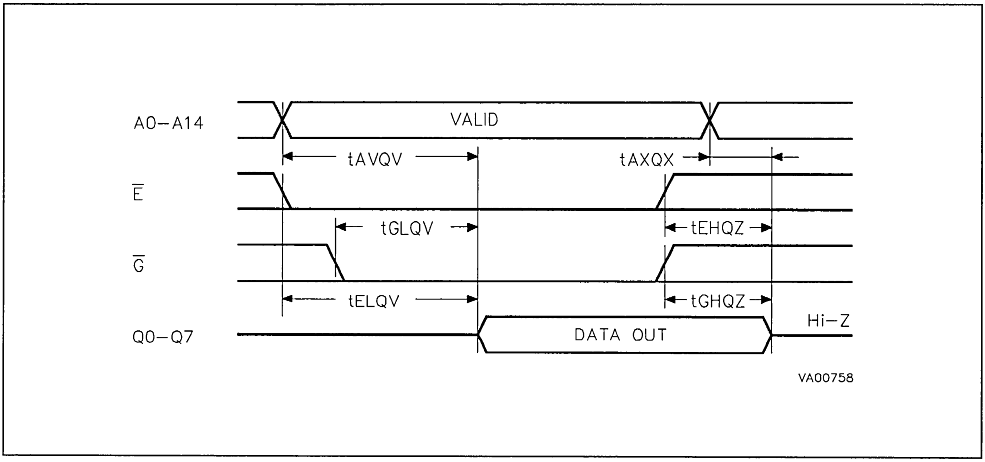

A0–A14
VALID
tAVQV
tAXQX
E̅
tGLQV
tEHQZ
G̅
tELQV
tGHQZ
Q0–Q7
DATA OUT
Hi–Z
VA00758

Table 6. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		40	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27256						Unit
				-1		-2, -20		blank, -25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		170		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		170		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		70		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	35	0	55	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27256				Unit
				-3		-4		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$,		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)

(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{ELEH}	t_{OPW}	Chip Enable Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable Low to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.
4. This parameter is sampled only and not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

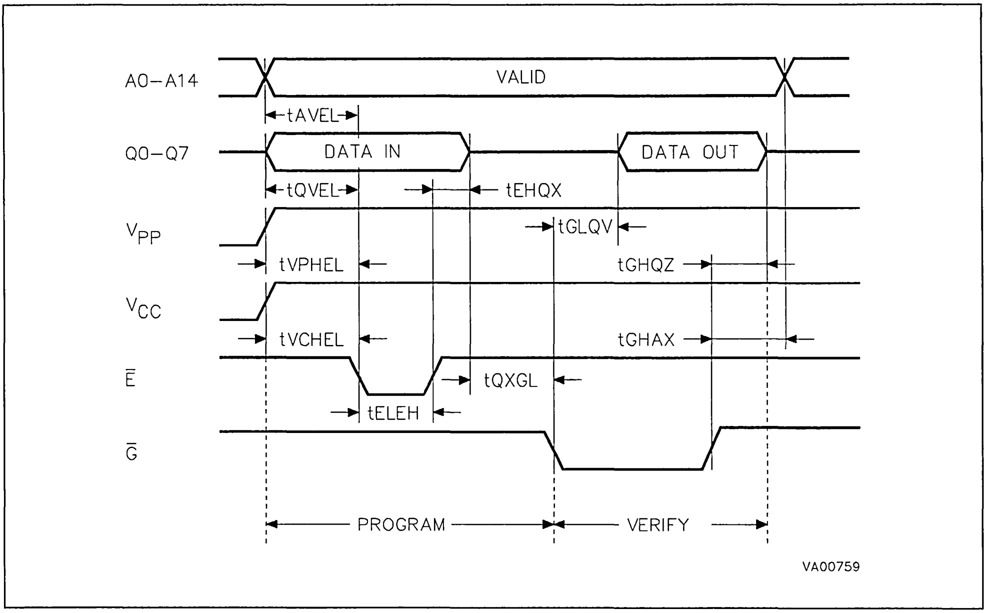
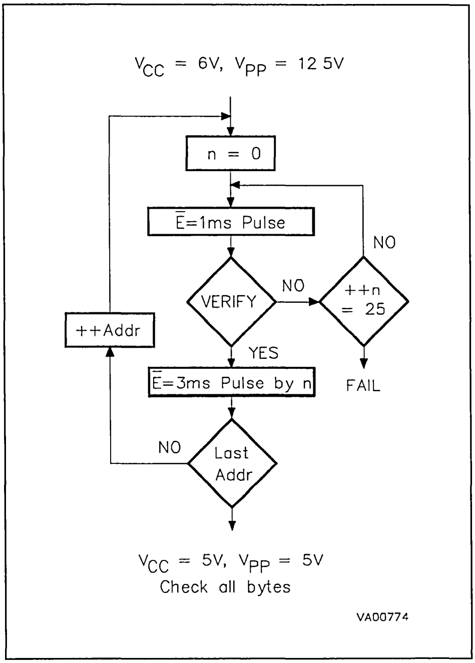

A0–A14
VALID
tAVEL
Q0–Q7
DATA IN
DATA OUT
tQVEL
tEHQX
VPP
tGLQV
tVPHEL
tGHQZ
VCC
tVCHEL
tGHAX
E
tQXGL
tELEH
G
PROGRAM
VERIFY
VA00759

Figure 7. Programming Flowchart


VCC = 6V, VPP = 12 5V
n = 0
E=1ms Pulse
VERIFY
NO
++n = 25
NO
YES
++Addr
E=3ms Pulse by n
FAIL
NO
Last Addr
VCC = 5V, VPP = 5V
Check all bytes
VA00774

DEVICE OPERATION (cont'd)

to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V.

When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V and V_{PP} = 5V.

Program Inhibit

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{E}$ input, with V_{PP} = 12.5V, will program that M27256. A high level $\overline{E}$ input inhibits the other M27256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$ and V_{PP} = 12.5V.

Optional Verify

The optional verify may be performed instead of the verify mode. It is performed with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$ (as opposed to the standard verify which has $\overline{E}$ =

DEVICE OPERATION (cont'd)

V_{IH}), and V_{PP} = 12.5V. The outputs will be in a Hi-z state according to the signal presented to $\overline{G}$. Therefore, all devices with V_{PP} = 12.5V and $\overline{G} = V_{IL}$ will present data on the bus independent of the $\overline{E}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (6V) and the normal read mode used to execute a program verify.

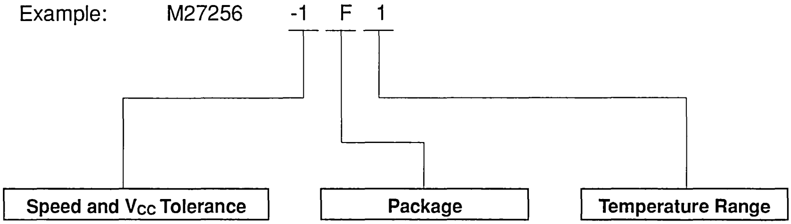
Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27256. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27256, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27256 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque lables be put over the M27256 window to prevent unintentional erasure. The recommended erasure procedure for the M27256 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27256 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION



Speed and V_{CC} Tolerance	
-1	170 ns, 5V ±5%
-2	200 ns, 5V ±5%
blank	250 ns, 5V ±5%
-3	300 ns, 5V ±5%
-4	400 ns, 5V ±5%
-20	200 ns, 5V ±10%
-25	250 ns, 5V ±10%

Package	
F	FDIP28W

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

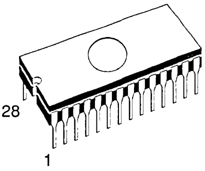
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M27512

NMOS 512K (64K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAM MING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27512 is a 524,288 bit UV erasable and electrically programmable memory EPROM. It is organized as 65,536 words by 8 bits.

The M27512 is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

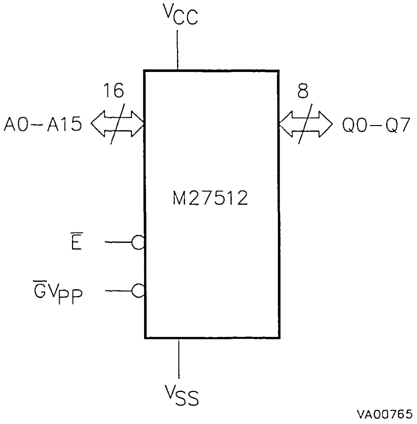
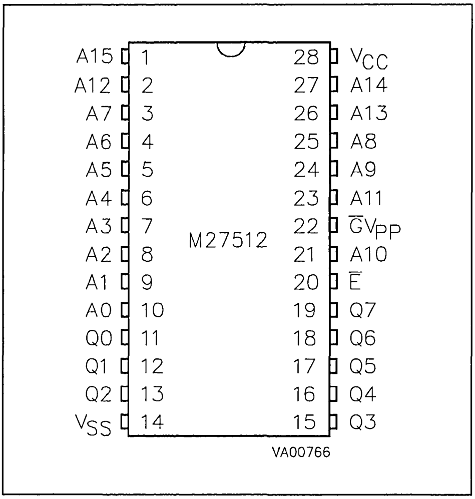


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	Grade 1 Grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	Grade 1 Grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.6 to 6.5	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27512 has a standby mode which reduces the maximum active power current from 125mA to 40mA. The M27512 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommenced that a 1μF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when $\overline{G}V_{PP}$ input is at 12.5V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27512 can use PRESTO Programming Algorithm that drastically reduces the programming time (typically less than 50 seconds). Nevertheless to achieve compatibility with all programming equipment, the standard Fast Programming Algorithm may also be used.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 Fast Programming Algorithm is shown in Figure 8.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Verify	V_{IH}	V_{IL}	X	Data Out
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Notes: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	1	0	1	0Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

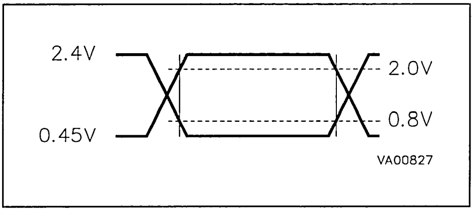

2.4V
2.0V
0.8V
0.45V
VA00827

Figure 4. AC Testing Load Circuit

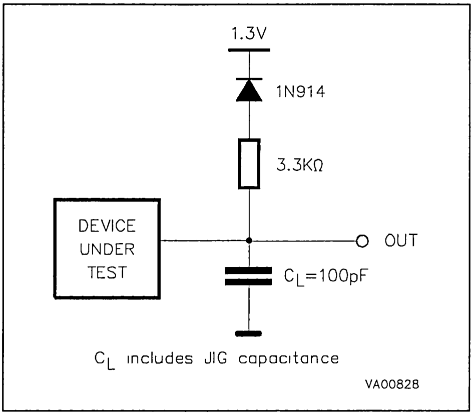

1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
CL includes JIG capacitance
VA00828

Table 5. Capacitance (T$_A$ = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: This parameter is sampled only and not tested 100%.

Figure 5. Read Mode AC Waveforms

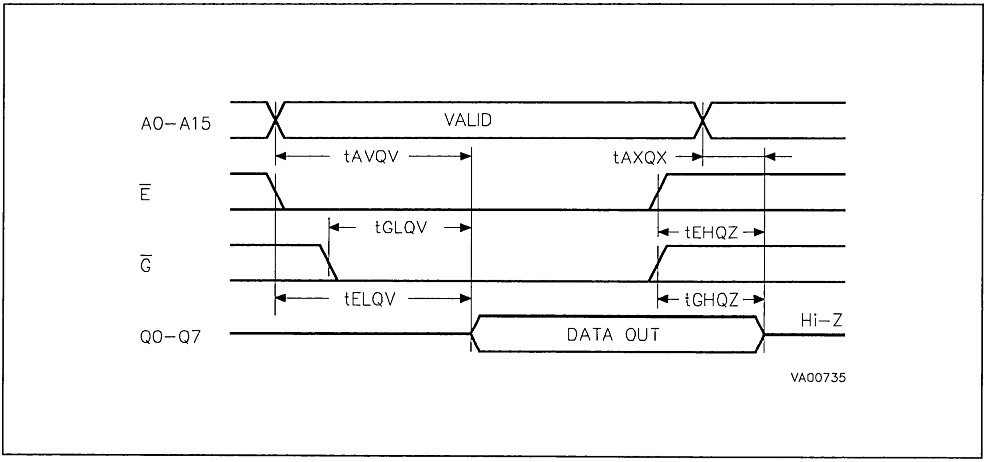

A0-A15
VALID
tAVQV
tAXQX
E̅
tGLQV
tEHQZ
G̅
tELQV
tGHQZ
Q0-Q7
DATA OUT
Hi-Z
VA00735

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		40	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27512						Unit
				-2, -20		blank, -25		-3		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		100		120	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	0	105	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	60	0	105	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 This parameter is sampled only and not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			150	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{ELEH}	t_{OPW}	Chip Enable Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (4)	t_{DF}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.
4. This parameter is sampled only and not 100% tested.

Figure 6. MARGIN MODE AC Waveform

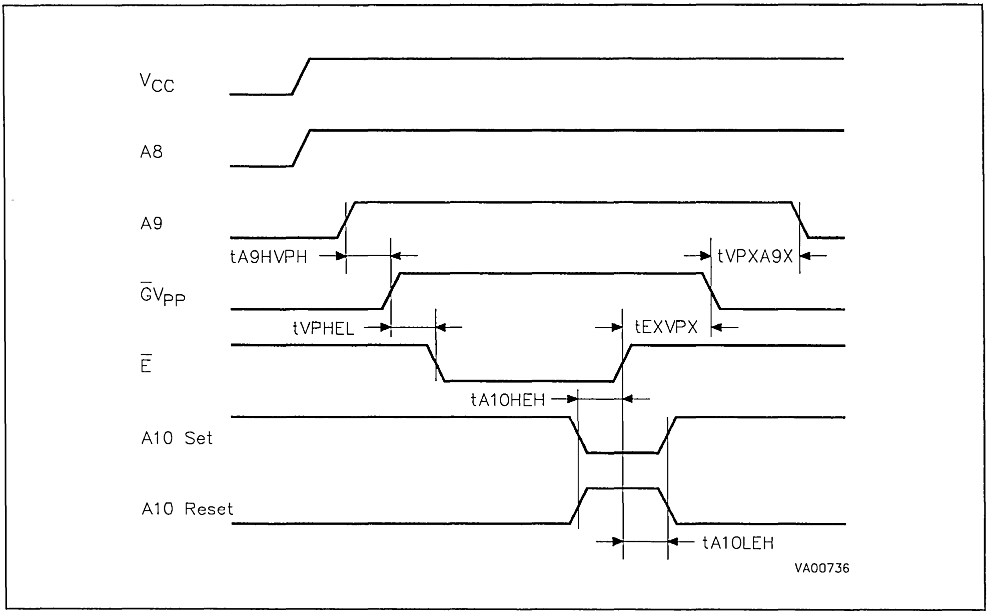

VCC
A8
A9
tA9HVPH
tVPXA9X
GVPP
tVPHEL
tEXVPX
E
tA10HEH
A10 Set
A10 Reset
tA10LEH
VA00736

Figure 7. Programming and Verify Modes AC Waveforms

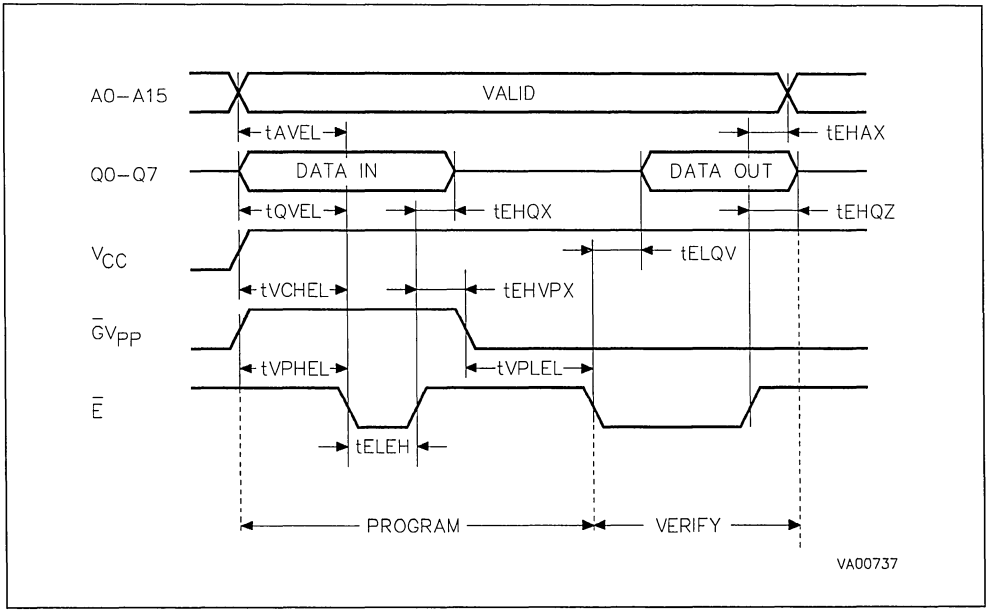

A0-A15
VALID
tAVEL
tEHAX
Q0-Q7
DATA IN
DATA OUT
tQVEL
tEHQX
tEHQZ
VCC
tELQV
tVCHEL
tEHVPX
GVPP
tVPHEL
tVPLEL
E
tELEH
PROGRAM
VERIFY
VA00737

Figure 8. Fast Programming Flowchart

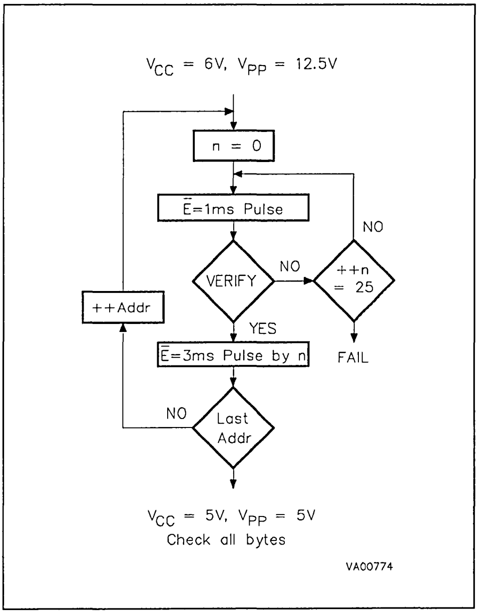
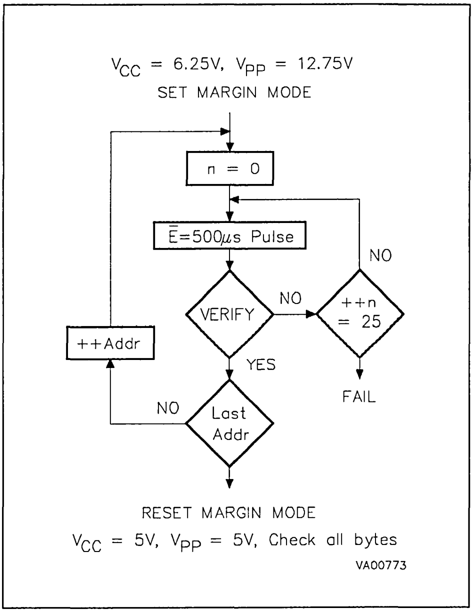

V_{CC} = 6V, V_{PP} = 12.5V
n = 0
$\overline{E}$=1ms Pulse
VERIFY
NO
++n = 25
NO
++Addr
YES
$\overline{E}$=3ms Pulse by n
FAIL
NO
Last Addr
V_{CC} = 5V, V_{PP} = 5V
Check all bytes
VA00774

Figure 9. PRESTO Programming Flowchart


V_{CC} = 6.25V, V_{PP} = 12.75V
SET MARGIN MODE
n = 0
$\overline{E}$=500µs Pulse
NO
VERIFY
NO
++n = 25
++Addr
YES
FAIL
NO
Last Addr
RESET MARGIN MODE
V_{CC} = 5V, V_{PP} = 5V, Check all bytes
VA00773

DEVICE OPERATION (cont'd)

The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram. The duration of the initial $\overline{E}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ns by n (n is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses is performed at V_{CC} = 6V and $\overline{G}V_{PP}$ = 12.5V (byte verifications at V_{CC} = 6V and $\overline{G}V_{PP}$ = V_{IL}). When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V.

PRESTO Programming Algorithm

PRESTO Programming Algorithm allows to program the whole array with a guaranted margin, in a typical time of less than 50 seconds (to be compared with 283 seconds for the Fast algorithm). This can be achieved with the SGS-THOMSON M27512 due to several design innovations described in the next paragraph that improves programming efficiency and brings adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin.

Then a sequence of 500µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}V_{PP}$) of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's $\overline{E}$ input, with $\overline{G}V_{pp}$ at 12.5V, will program that M27512. A high level $\overline{E}$ input inhibits the other M27512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}V_{pp}$ and $\overline{E}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{E}$.

Electronic Signature

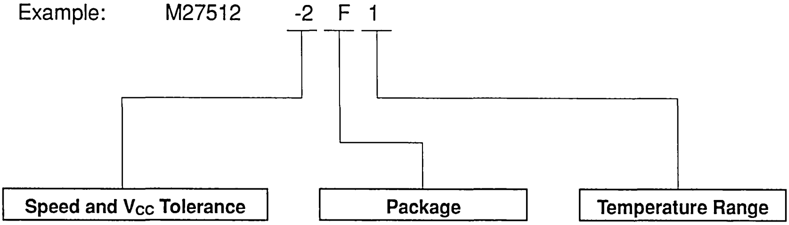
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25 °C ± 5 °C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be high. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å.

The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION



Speed and V_{CC} Tolerance	
-2	200 ns, 5V ±5%
blank	250 ns, 5V ±5%
-3	300 ns, 5V ±5%
-20	200 ns, 5V ±10%
-25	250 ns, 5V ±10%

Package	
F	FDIP28W

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

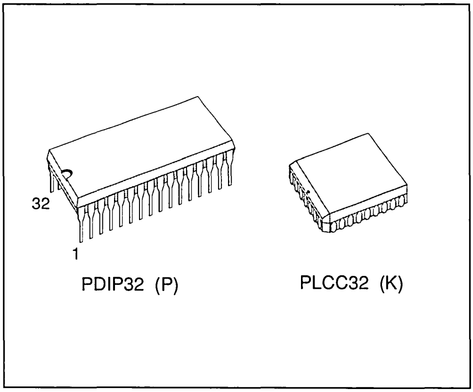
For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

FLASH MEMORIES

CMOS 256K (32K x 8) FLASH MEMORY

- FAST ACCESS TIME: 100ns
- 1,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 100µs (PRESTO F PROGRAMMING)
- ELECTRICAL CHIP ERASE IN 1s RANGE



DESCRIPTION

The M28F256 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

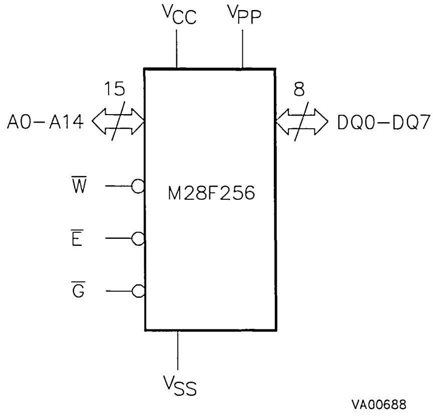
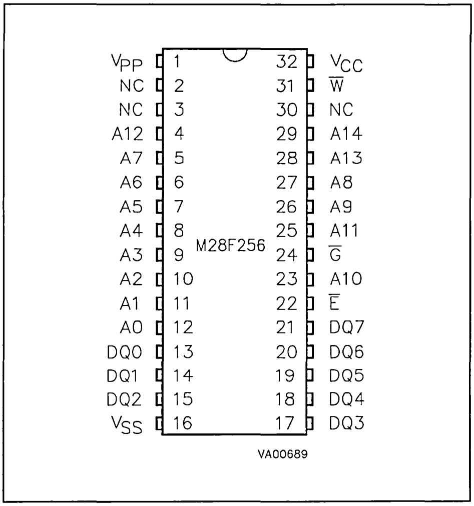
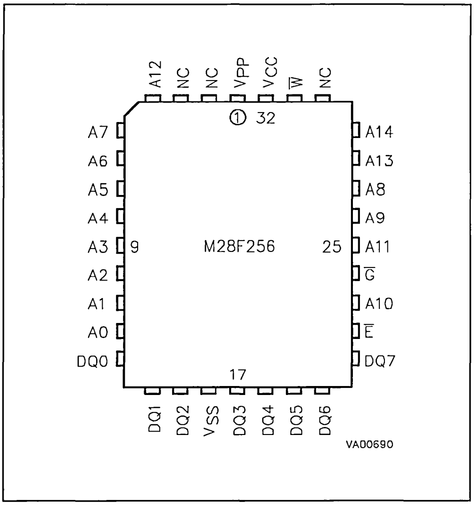


Figure 2A. DIP Pin Connections


VPP 1
NC 2
NC 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
DQ0 13
DQ1 14
DQ2 15
VSS 16
32 VCC
31 W
30 NC
29 A14
28 A13
27 A8
26 A9
25 A11
24 G
23 A10
22 E
21 DQ7
20 DQ6
19 DQ5
18 DQ4
17 DQ3
M28F256
VA00689

Warning: NC = No Connection

Figure 2B. LCC Pin Connections


A12
NC
NC
VPP
VCC
W
NC
① 32
A7
A6
A5
A4
A3
A2
A1
A0
DQ0
9
M28F256
25
A14
A13
A8
A9
A11
G
A10
E
DQ7
17
DQ1
DQ2
VSS
DQ3
DQ4
DQ5
DQ6
VA00690

Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F256 FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F256 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}

2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	0	1	0	0	0	0A8h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A14	DQ0-DQ7	Operation	A0-A14	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	0A8h
Setup Erase/	2	Write	X	20h			
Erase					Write	X	20h
Erase Verify	2	Write	A0-A14	0A0h	Read	X	Data Output
Setup Program/	2	Write	X	40h			
Program					Write	A0-A14	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

READ/WRITE MODES (cont'd)

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this second cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

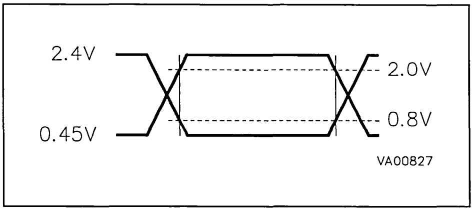


Figure 4. AC Testing Load Circuit

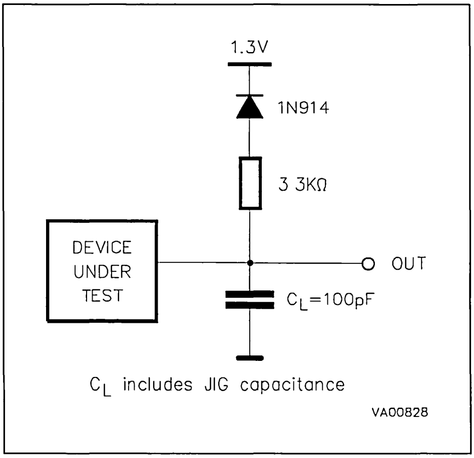


Table 6. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: this parameter is sampled only and not tested100%

Table 7. DC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \leq V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \leq V_{CC}$		±100	µA
I_{PP1}(1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2}(1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3}(1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4}(1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage TTL	IOH = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA

Note: 1. Not 100% Tested Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256				Unit
				-10		-12		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		45		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1 Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

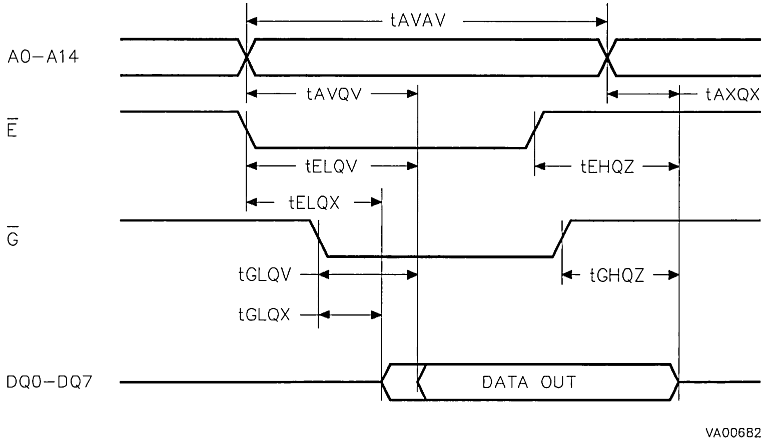

tAVAV
A0–A14
tAVQV
tAXQX
E̅
tELQV
tEHQZ
tELQX
G̅
tGLQV
tGHQZ
tGLQX
DQ0–DQ7
DATA OUT
VA00682

Figure 6. Read Command Waveforms

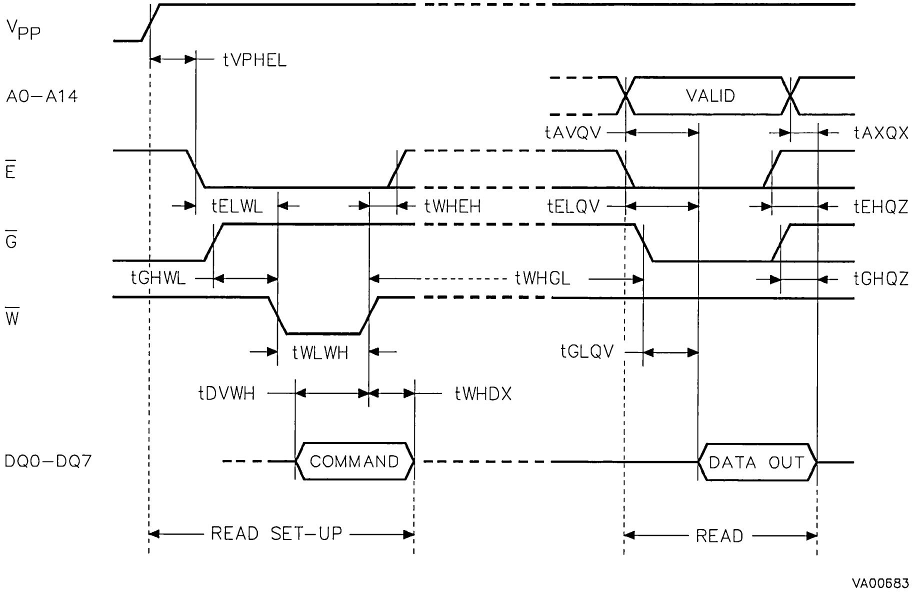

VPP
tVPHEL
A0–A14
VALID
tAVQV
tAXQX
E̅
tELWL
tWHEH
tELQV
tEHQZ
G̅
tGHWL
tWHGL
tGHQZ
W̅
tWLWH
tGLQV
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA OUT
READ SET–UP
READ
VA00683

Figure 7. Electronic Signature Command Waveforms

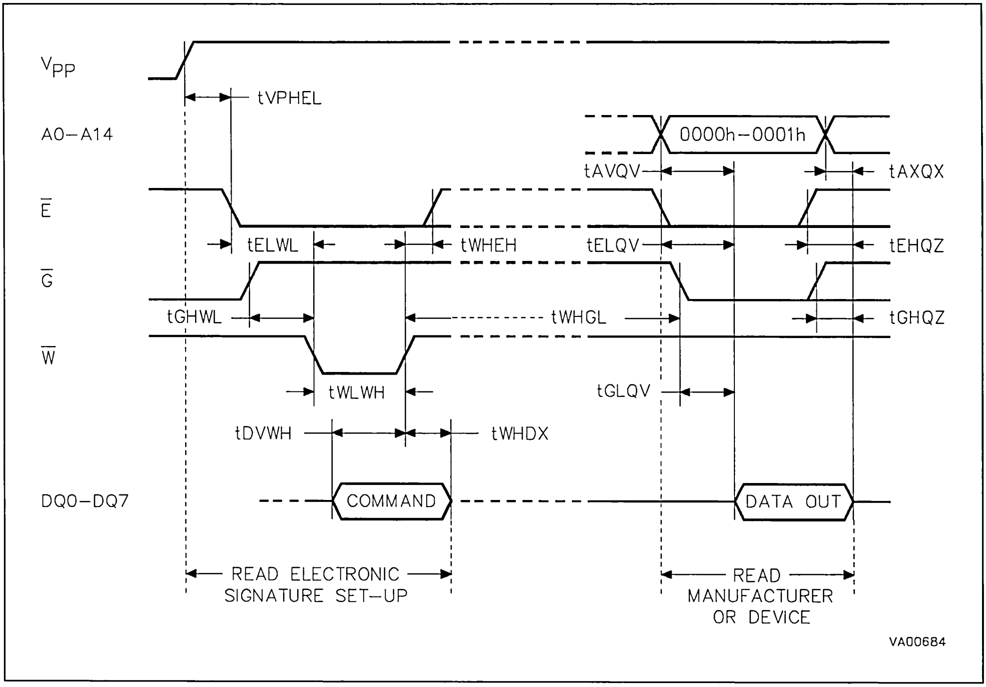

VPP
tVPHEL
A0–A14
0000h–0001h
tAVQV
tAXQX
E
tELWL
tWHEH
tELQV
tEHQZ
G
tGHWL
tWHGL
tGHQZ
W
tWLWH
tGLQV
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA OUT
READ ELECTRONIC SIGNATURE SET–UP
READ MANUFACTURER OR DEVICE
VA00684

Table 9A. Read/Write Mode AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A				Unit
			-10		-12		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}(2)		Chip Enable Low to Chip Enable High (Write Pulse)	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	95	105	95	105	µs
t_{WHWH2}		Duration of Erase Operation	9.5	10.5	9.5	10.5	ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		40		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

2 A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}(2)		Chip Enable Low to Chip Enable High (Write Pulse)	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	95	105	95	105	µs
t_{WHWH2}		Duration of Erase Operation	9.5	10.5	9.5	10.5	ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested
2 A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

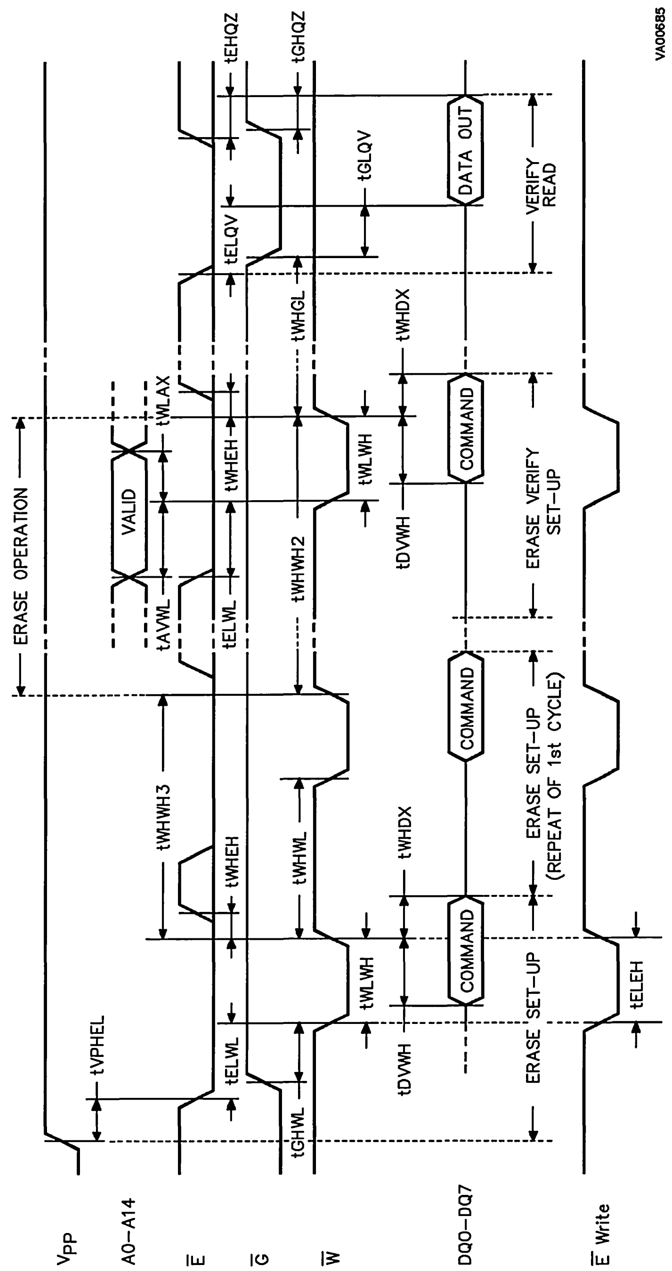

ERASE OPERATION
VPP
tVPHEL
A0-A14
VALID
tWHWH3
tAVWL
tWLAX
E
tELWL
tWHEH
tELWL
tWHEH
tELQV
tEHQZ
G
tGHWL
tWHWL
tWHWH2
tWHGL
tGHQZ
W
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
DQ0-DQ7
COMMAND
COMMAND
COMMAND
DATA OUT
ERASE SET-UP
ERASE SET-UP (REPEAT OF 1st CYCLE)
ERASE VERIFY SET-UP
VERIFY READ
E Write
tELEH
VA00685

Figure 9. Program Set-up and Program Verify Commands Waveforms

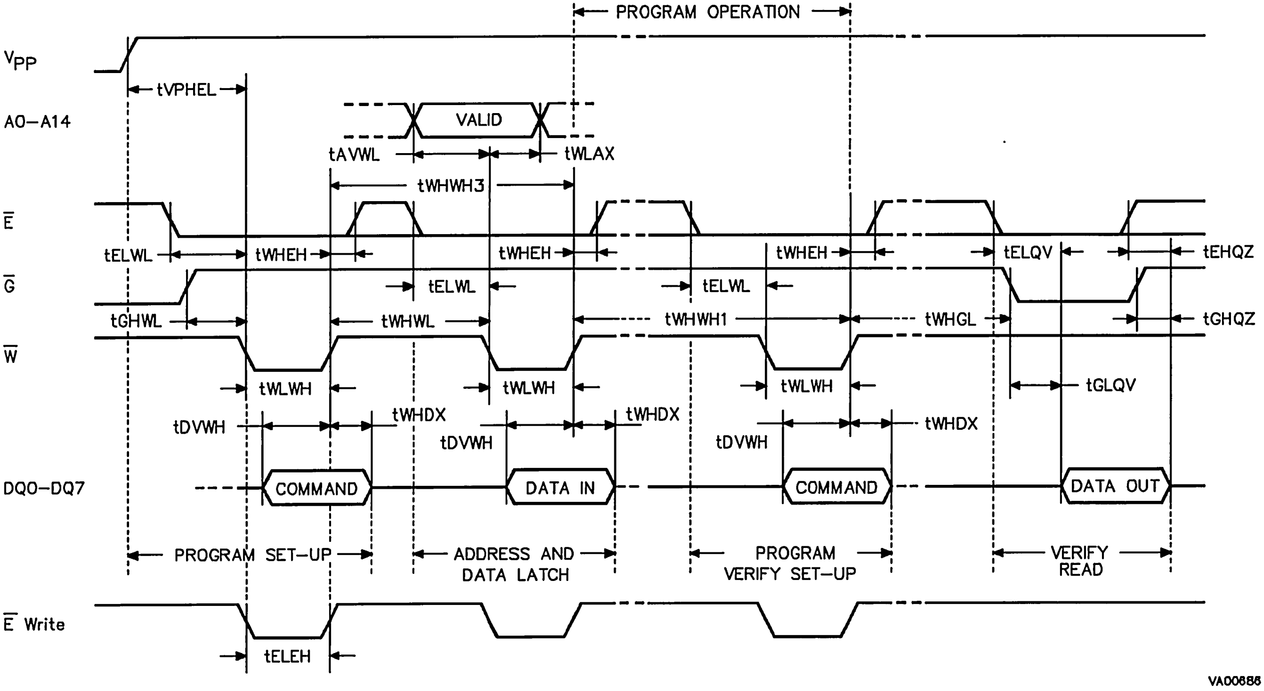

PROGRAM OPERATION
VPP
tVPHEL
A0–A14
VALID
tAVWL
tWLAX
tWHWH3
E
tELWL
tWHEH
tWHEH
tWHEH
tELQV
tEHQZ
G
tELWL
tELWL
tGHWL
tWHWL
tWHWH1
tWHGL
tGHQZ
W
tWLWH
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
E Write
tELEH
VA00686

Figure 10. Erasing Flowchart

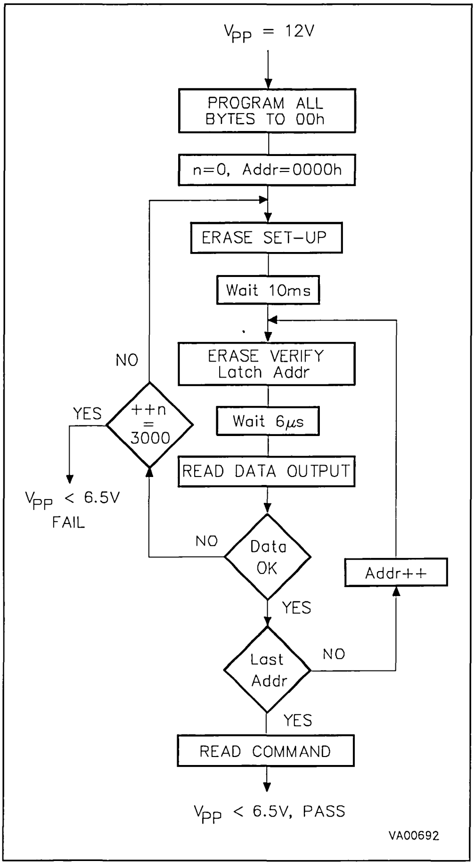
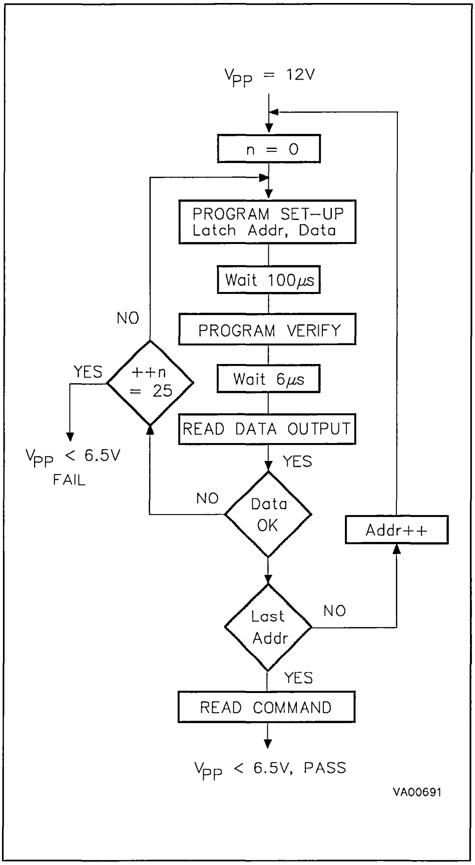

V_{PP} = 12V
PROGRAM ALL BYTES TO 00h
n=0, Addr=0000h
ERASE SET-UP
Wait 10ms
ERASE VERIFY Latch Addr
Wait 6µs
READ DATA OUTPUT
Data OK
YES
NO
++n = 3000
YES
NO
V_{PP} < 6.5V FAIL
Last Addr
NO
Addr++
YES
READ COMMAND
V_{PP} < 6.5V, PASS
VA00692

Figure 11. Programming Flowchart


V_{PP} = 12V
n = 0
PROGRAM SET-UP Latch Addr, Data
Wait 100µs
PROGRAM VERIFY
Wait 6µs
READ DATA OUTPUT
NO
YES
++n = 25
V_{PP} < 6.5V FAIL
YES
NO
Data OK
Addr++
Last Addr
NO
YES
READ COMMAND
V_{PP} < 6.5V, PASS
VA00691

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programs all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 100µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION

Example: M28F256 -10 X B 1

Speed	
-10	100 ns
-12	120 ns
-15	150 ns
-20	200 ns

V_{CC} Tolerance	
X	± 5%
blank	± 10%

Package	
B	PDIP32
C	PLCC32

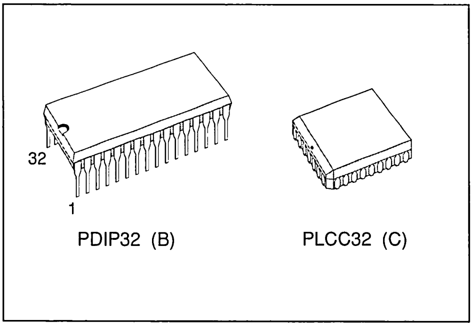
Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

CMOS 256K (32K x 8) FLASH MEMORY

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



DESCRIPTION

The M28F256A FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256A FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

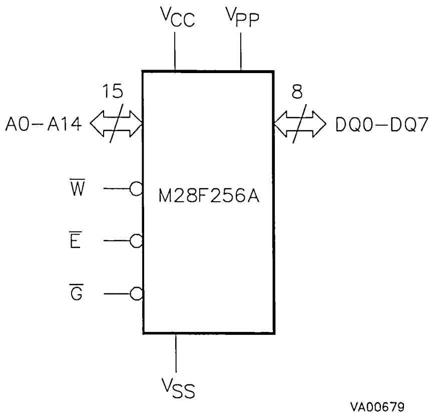
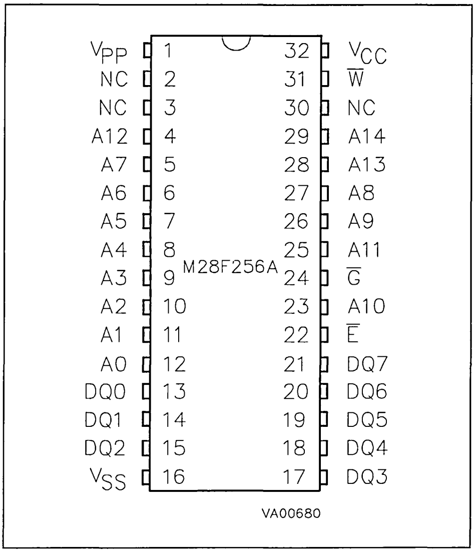
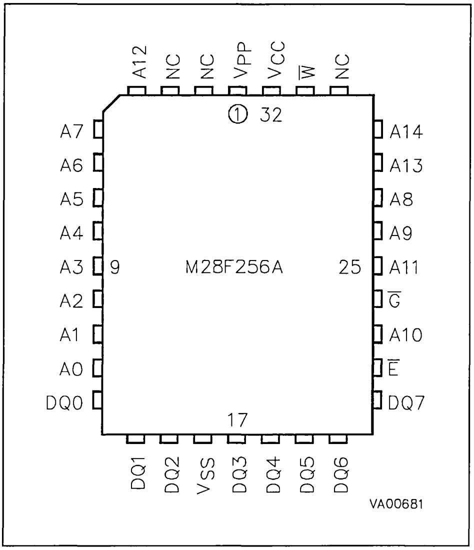


Figure 2A. DIP Pin Connections


VPP 1
NC 2
NC 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
DQ0 13
DQ1 14
DQ2 15
VSS 16
32 VCC
31 W
30 NC
29 A14
28 A13
27 A8
26 A9
25 A11
24 G
23 A10
22 E
21 DQ7
20 DQ6
19 DQ5
18 DQ4
17 DQ3
M28F256A
VA00680

Warning: NC = No Connection

Figure 2B. LCC Pin Connections


A12
NC
NC
VPP
VCC
W
NC
① 32
A7
A6
A5
A4
A3
A2
A1
A0
DQ0
9
M28F256A
25
A14
A13
A8
A9
A11
G
A10
E
DQ7
17
DQ1
DQ2
VSS
DQ3
DQ4
DQ5
DQ6
VA00681

Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DEVICE OPERATION

The M28F256A FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256A functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F256A has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	0	1	0	1	0	0AAh

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A14	DQ0-DQ7	Operation	A0-A14	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	0AAh
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A14	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A14	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising

READ/WRITE MODES (cont'd)

edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

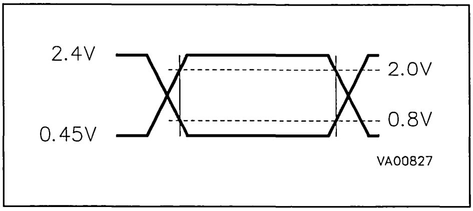


Figure 4. AC Testing Load Circuit

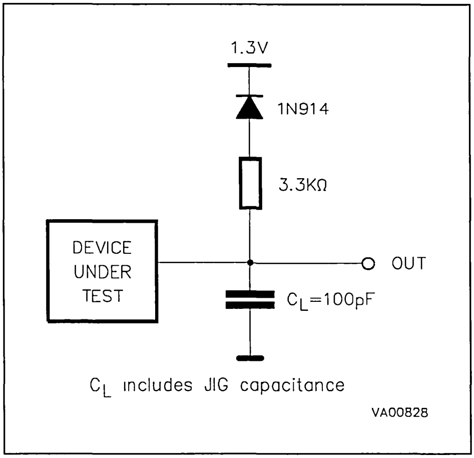


Table 6. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: this parameter is sampled only and not tested100%

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \leq V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \leq V_{CC}$		±100	µA
I_{PP1}(1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2}(1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3}(1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4}(1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grades 3 & 6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
		I_{OH} = –2.5mA (grade 1)	V_{CC} –0.8		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID} (grade 1)		200	µA
		A9 = V_{ID} (grades 3 & 6)		500	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% Tested. Characterisation Data available

Table 8A. Read Only Mode AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256A				Unit
				-10		-12		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics

((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256A				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

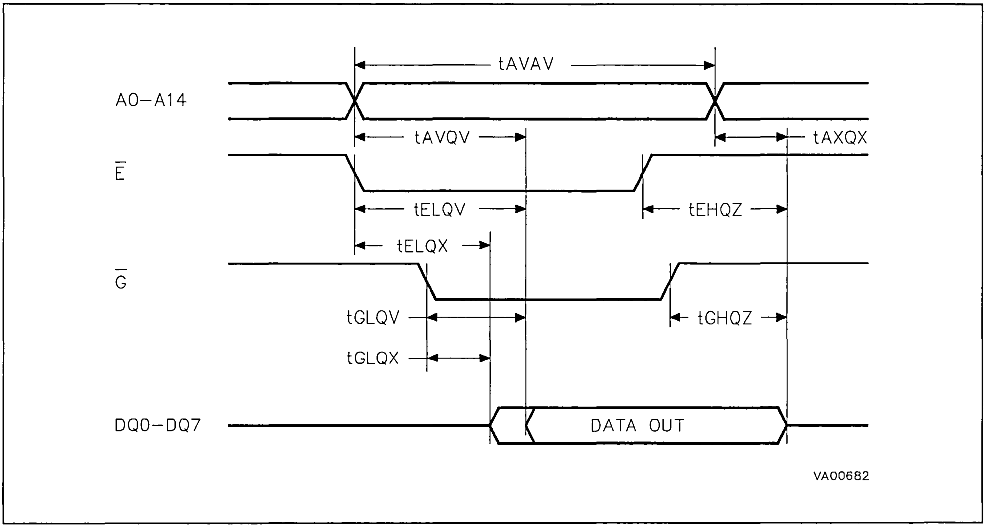

tAVAV
A0–A14
tAVQV
tAXQX
E̅
tELQV
tEHQZ
tELQX
G̅
tGLQV
tGHQZ
tGLQX
DQ0–DQ7
DATA OUT
VA00682

Figure 6. Read Command Waveforms

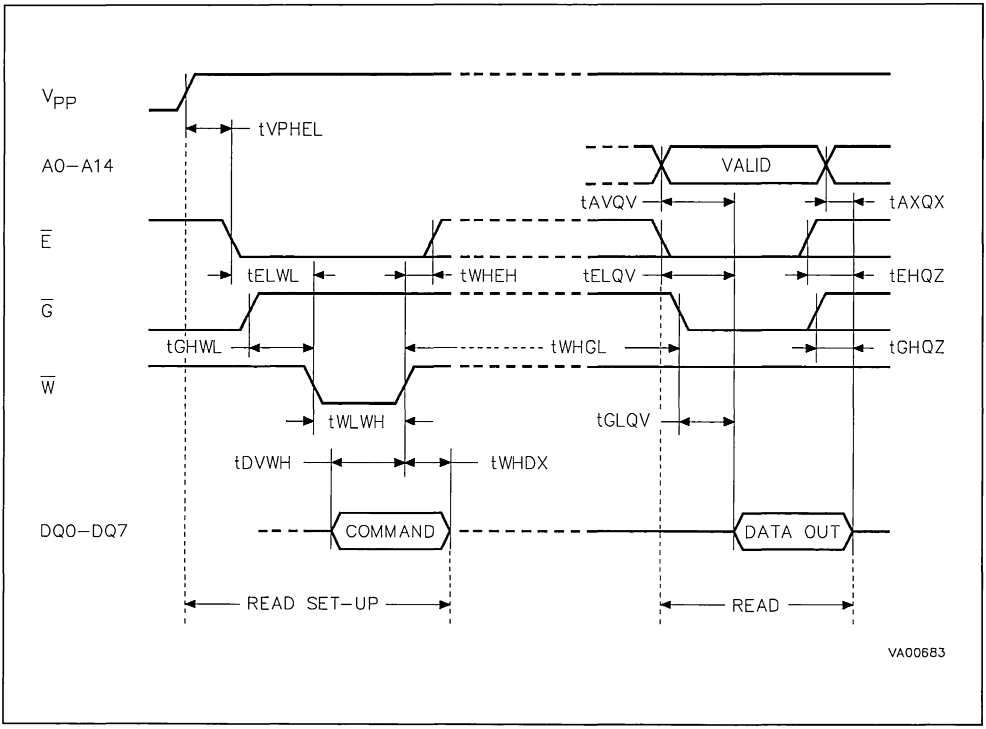

VPP
tVPHEL
A0–A14
VALID
tAVQV
tAXQX
E̅
tELWL
tWHEH
tELQV
tEHQZ
G̅
tGHWL
tWHGL
tGHQZ
W̅
tWLWH
tGLQV
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA OUT
READ SET–UP
READ
VA00683

Figure 7. Electronic Signature Command Waveforms

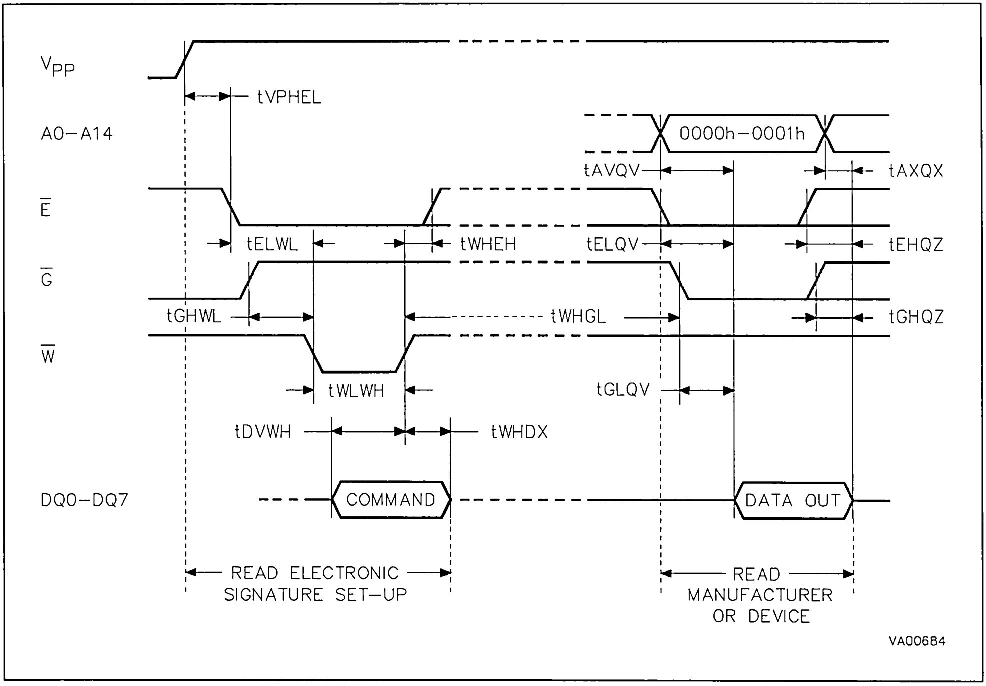

VPP
tVPHEL
A0–A14
0000h–0001h
tAVQV
tAXQX
E
tELWL
tWHEH
tELQV
tEHQZ
G
tGHWL
tWHGL
tGHQZ
W
tWLWH
tGLQV
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA OUT
READ ELECTRONIC SIGNATURE SET–UP
READ MANUFACTURER OR DEVICE
VA00684

Table 9A. Read/Write Mode AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%: V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A				Unit
			-10		-12		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}(2)		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	10		10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		40		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%: V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}(2)		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	10		10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

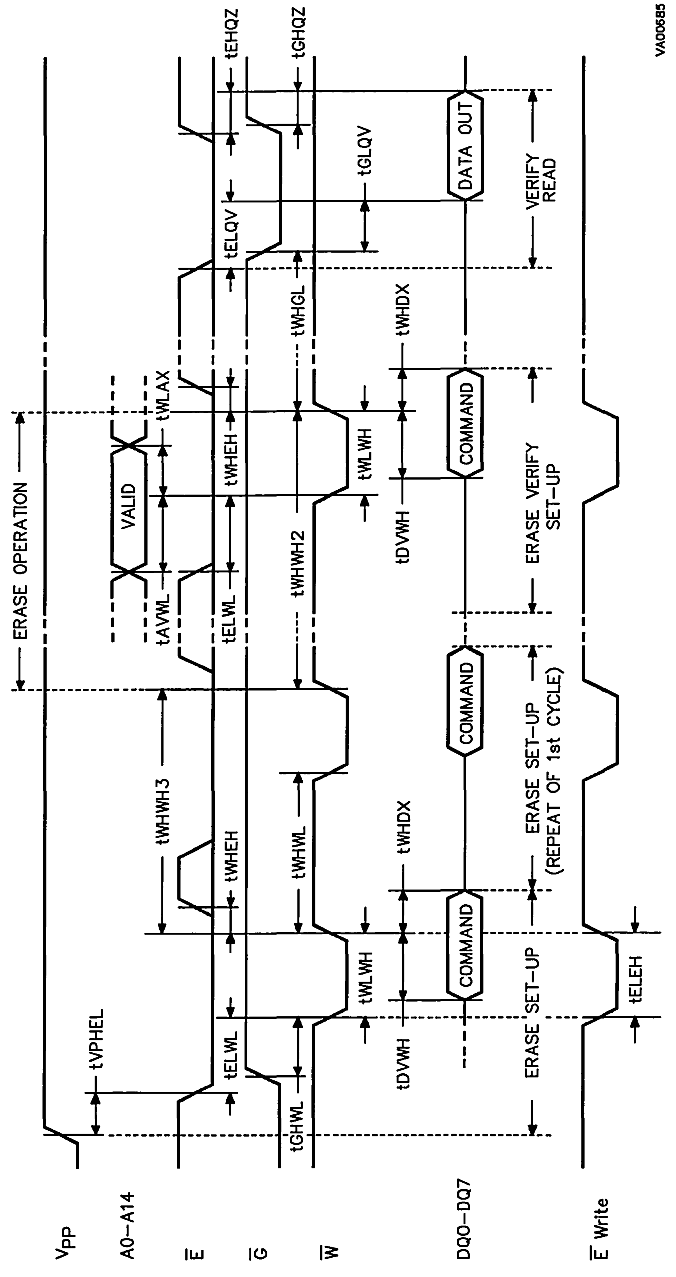

ERASE OPERATION
VPP
tVPHEL
A0–A14
VALID
tWHWH3
tAVWL
tWLAX
E
tELWL
tWHEH
tELWL
tWHEH
tELQV
tEHQZ
G
tGHWL
tWHWL
tWHWH2
tWHGL
tGHQZ
W
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
DQ0–DQ7
COMMAND
COMMAND
COMMAND
DATA OUT
ERASE SET–UP
ERASE SET–UP
(REPEAT OF 1st CYCLE)
ERASE VERIFY
SET–UP
VERIFY
READ
E Write
tELEH
VA00685

Figure 9. Program Set-up and Program Verify Commands Waveforms

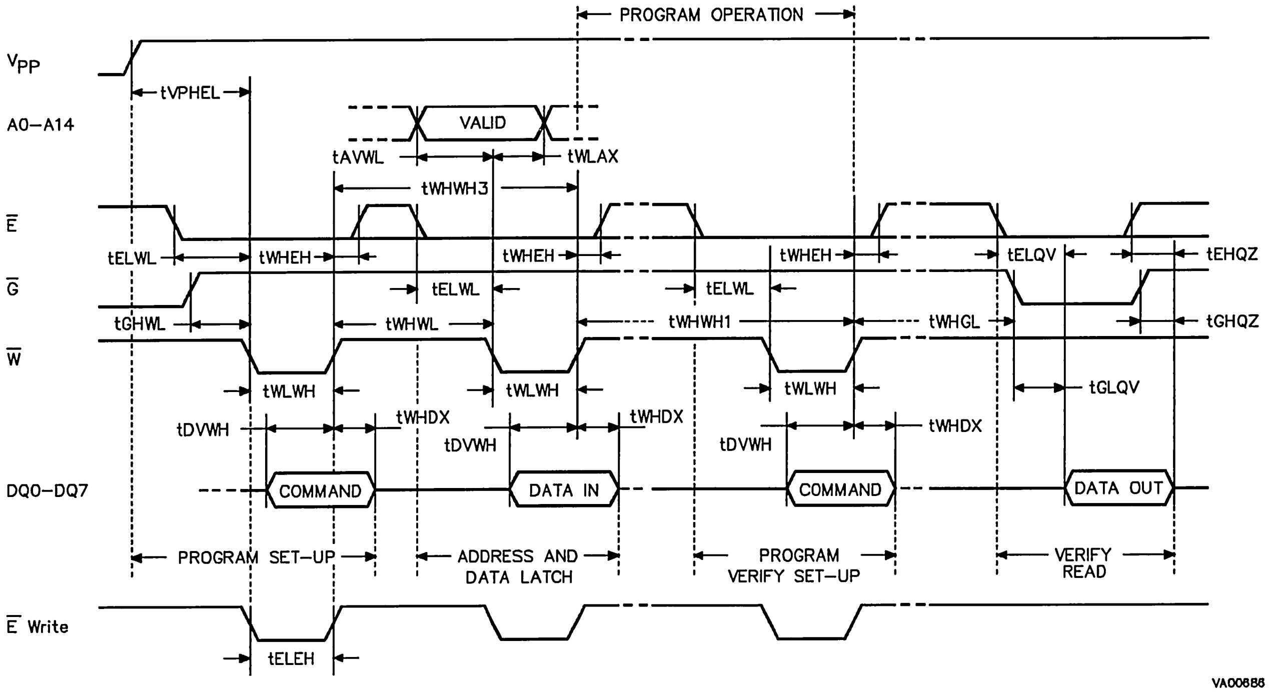
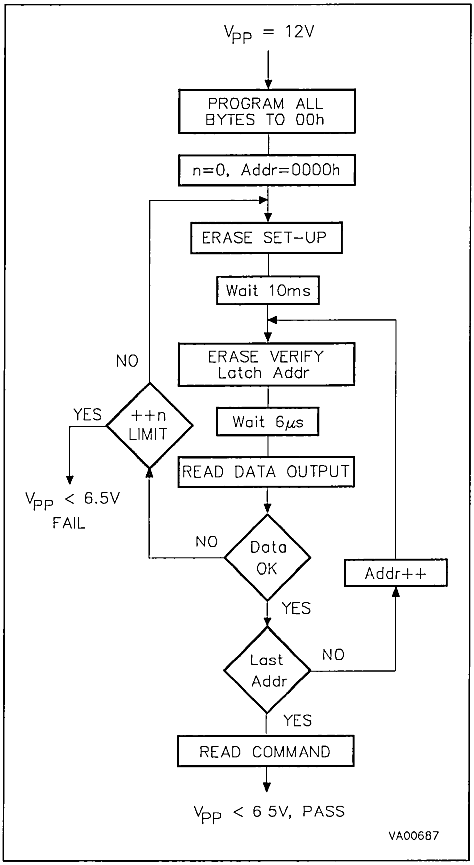

PROGRAM OPERATION
V_{PP}
tVPHEL
A0–A14
VALID
tAVWL
tWLAX
tWHWH3
$\overline{E}$
tELWL
tWHEH
tWHEH
tWHEH
tELQV
tEHQZ
$\overline{G}$
tELWL
tELWL
tGHWL
tWHWL
tWHWH1
tWHGL
tGHQZ
$\overline{W}$
tWLWH
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
$\overline{E}$ Write
tELEH
VA00688

Figure 10. Erasing Flowchart

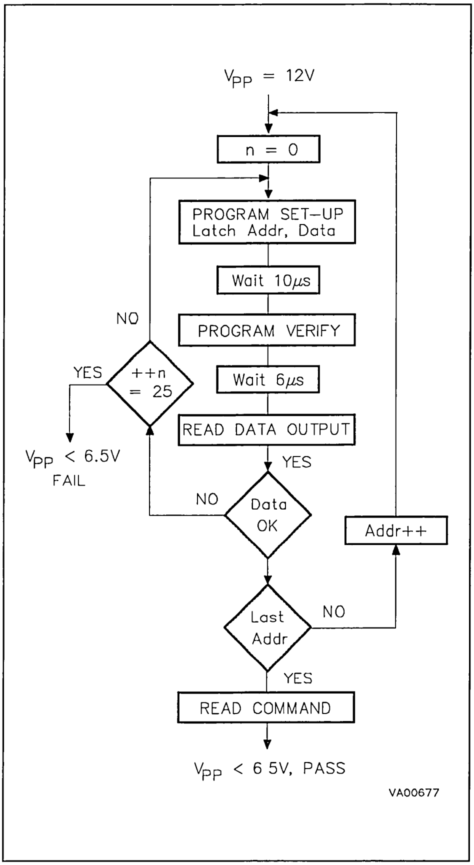

V_{PP} = 12V
PROGRAM ALL BYTES TO 00h
n=0, Addr=0000h
ERASE SET-UP
Wait 10ms
ERASE VERIFY Latch Addr
Wait 6µs
READ DATA OUTPUT
Data OK
NO
YES
Last Addr
NO
Addr++
YES
READ COMMAND
V_{PP} < 6 5V, PASS
++n LIMIT
NO
YES
V_{PP} < 6.5V FAIL
VA00687

Limit: 1000 at grades 1 & 6; 6000 at grade 3.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

Figure 11. Programming Flowchart


V_{PP} = 12V
n = 0
PROGRAM SET-UP Latch Addr, Data
Wait 10µs
PROGRAM VERIFY
Wait 6µs
READ DATA OUTPUT
YES
Data OK
NO
Last Addr
NO
Addr++
YES
READ COMMAND
V_{PP} < 6 5V, PASS
++n = 25
NO
YES
V_{PP} < 6.5V FAIL
VA00677

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION

Example: M28F256A -10 X B 1

Speed		V_{CC} Tolerance		Package		Temperature Range	
-10	100 ns	X	± 5%	B	PDIP32	1	0 to 70 °C
-12	120 ns	blank	± 10%	C	PLCC32	3	–40 to 125 °C
-15	150 ns					6	–40 to 85 °C
-20	200 ns						

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

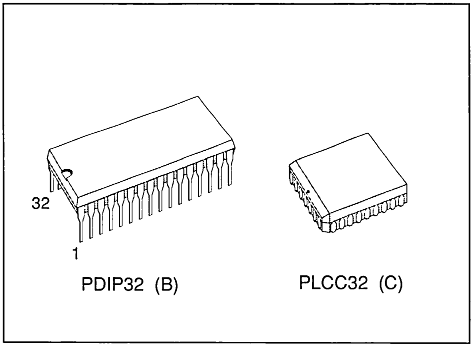
For further information on any aspect of this device, please contact our Sales Office nearest you.

SGS-THOMSON
MICROELECTRONICS

M28F512

CMOS 512K (64K x 8) FLASH MEMORY

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



DESCRIPTION

The M28F512 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 64K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F512 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A15	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

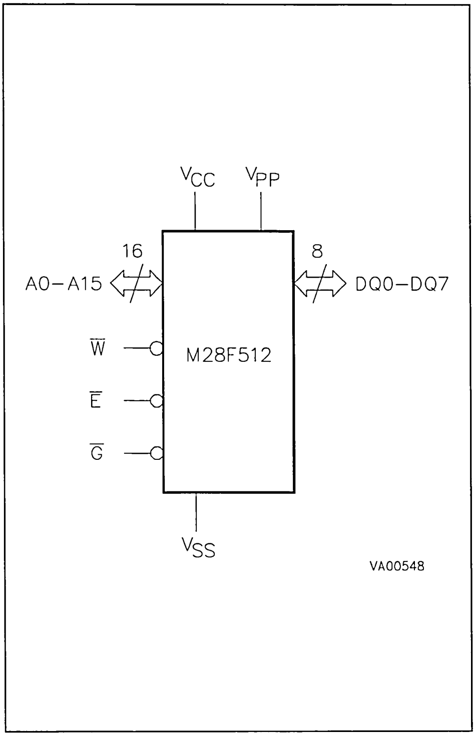
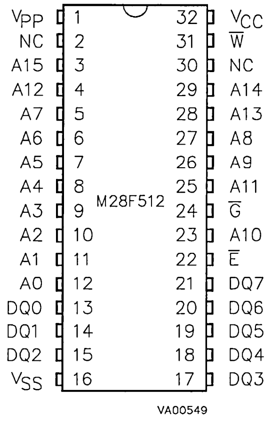
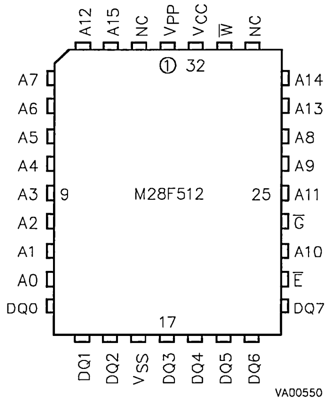


Figure 2A. DIP Pin Connections


VPP 1
NC 2
A15 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
DQ0 13
DQ1 14
DQ2 15
VSS 16
32 VCC
31 $\overline{W}$
30 NC
29 A14
28 A13
27 A8
26 A9
25 A11
24 $\overline{G}$
23 A10
22 $\overline{E}$
21 DQ7
20 DQ6
19 DQ5
18 DQ4
17 DQ3
M28F512
VA00549

Warning: NC = No Connection

Figure 2B. LCC Pin Connections


A12
A15
NC
VPP
VCC
$\overline{W}$
NC
① 32
A7
A6
A5
A4
A3
A2
A1
A0
DQ0
9
M28F512
25
A14
A13
A8
A9
A11
$\overline{G}$
A10
$\overline{E}$
DQ7
17
DQ1
DQ2
VSS
DQ3
DQ4
DQ5
DQ6
VA00550

Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DEVICE OPERATION

The M28F512 FLASH MEMORY employs a technology similar to a 512K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F512 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F512 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2 Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	0	1	0	02h

Table 5. Commands [(1)]

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A15	DQ0-DQ7	Operation	A0-A15	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	02h
Setup Erase/	2	Write	X	20h			
Erase					Write	X	20h
Erase Verify	2	Write	A0-A15	0A0h	Read	X	Data Output
Setup Program/	2	Write	X	40h			
Program					Write	A0-A15	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1 X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is

READ/WRITE MODES (cont'd)

followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

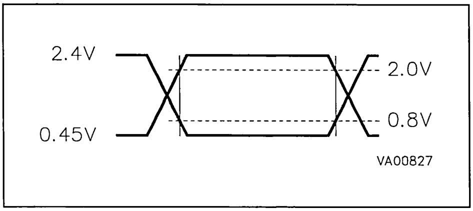


Figure 4. AC Testing Load Circuit

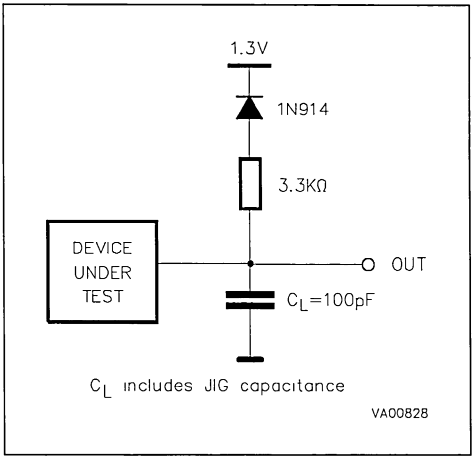


Table 6. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: this parameter is sampled only and not tested100%

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±100	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 3 & 6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
		I_{OH} = –2.5mA (grade 1)	V_{CC} –0.8		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% Tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; $0V \leq V_{PP} \leq 6.5V$)

Symbol	Alt	Parameter	Test Condition	M28F512				Unit
				-10		-12		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; $0V \leq V_{PP} \leq 6.5V$)

Symbol	Alt	Parameter	Test Condition	M28F512				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

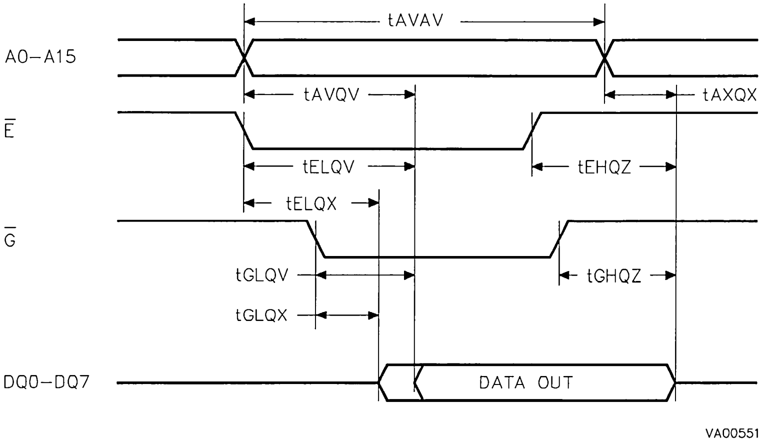

tAVAV
A0–A15
tAVQV
tAXQX
E̅
tELQV
tEHQZ
tELQX
G̅
tGLQV
tGHQZ
tGLQX
DQ0–DQ7
DATA OUT
VA00551

Figure 6. Read Command Waveforms

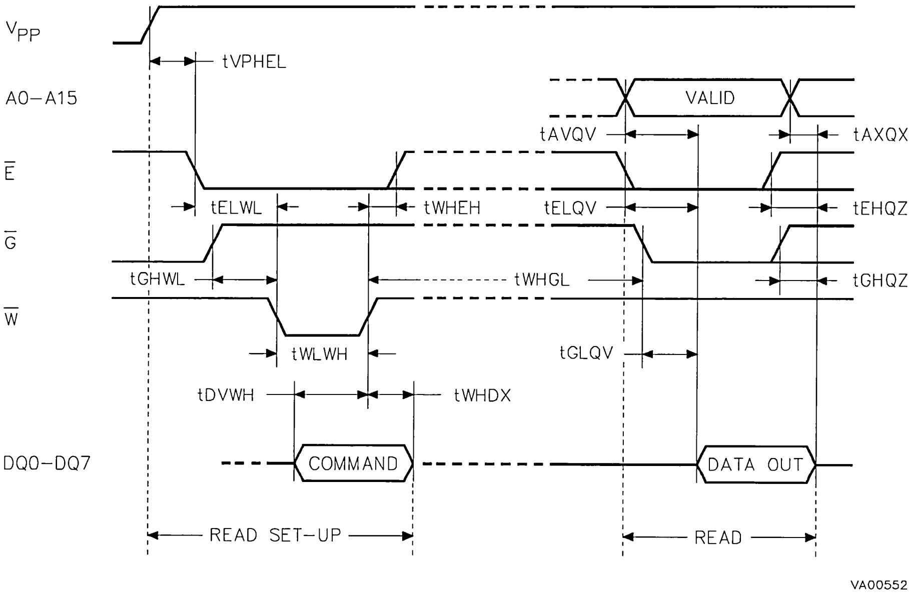

VPP
tVPHEL
A0–A15
VALID
tAVQV
tAXQX
E̅
tELWL
tWHEH
tELQV
tEHQZ
G̅
tGHWL
tWHGL
tGHQZ
W̅
tWLWH
tGLQV
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA OUT
READ SET–UP
READ
VA00552

Figure 7. Electronic Signature Command Waveforms

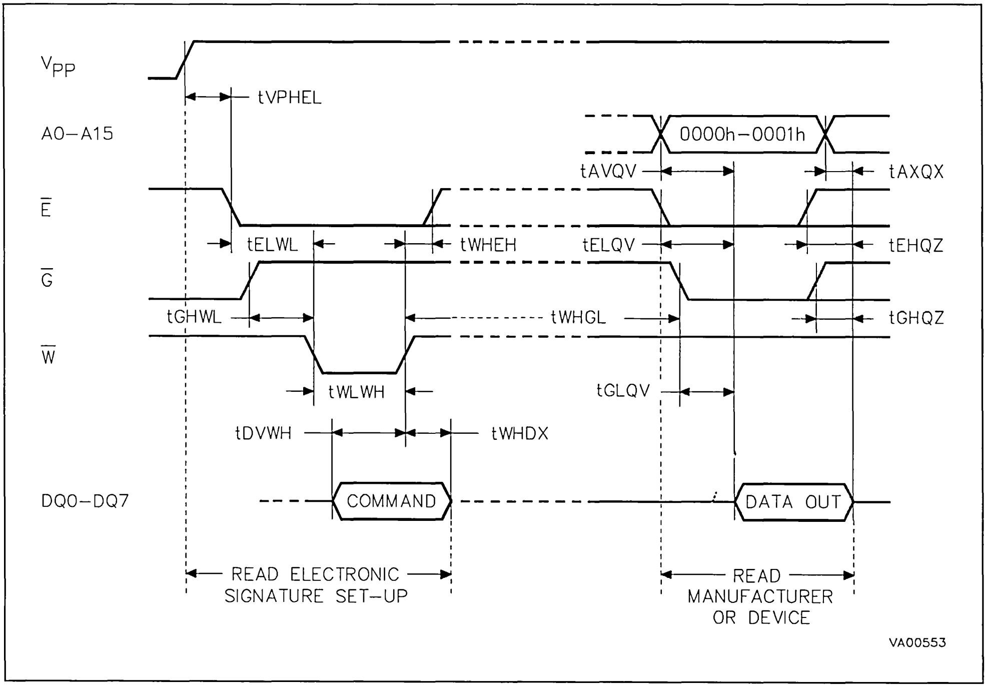

VPP
A0–A15
E
G
W
DQ0–DQ7
tVPHEL
0000h–0001h
tAVQV
tAXQX
tELWL
tWHEH
tELQV
tEHQZ
tGHWL
tWHGL
tGHQZ
tWLWH
tGLQV
tDVWH
tWHDX
COMMAND
DATA OUT
READ ELECTRONIC SIGNATURE SET-UP
READ MANUFACTURER OR DEVICE
VA00553

Table 9A. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F512				Unit
			-10		-12		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		40		50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F512				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

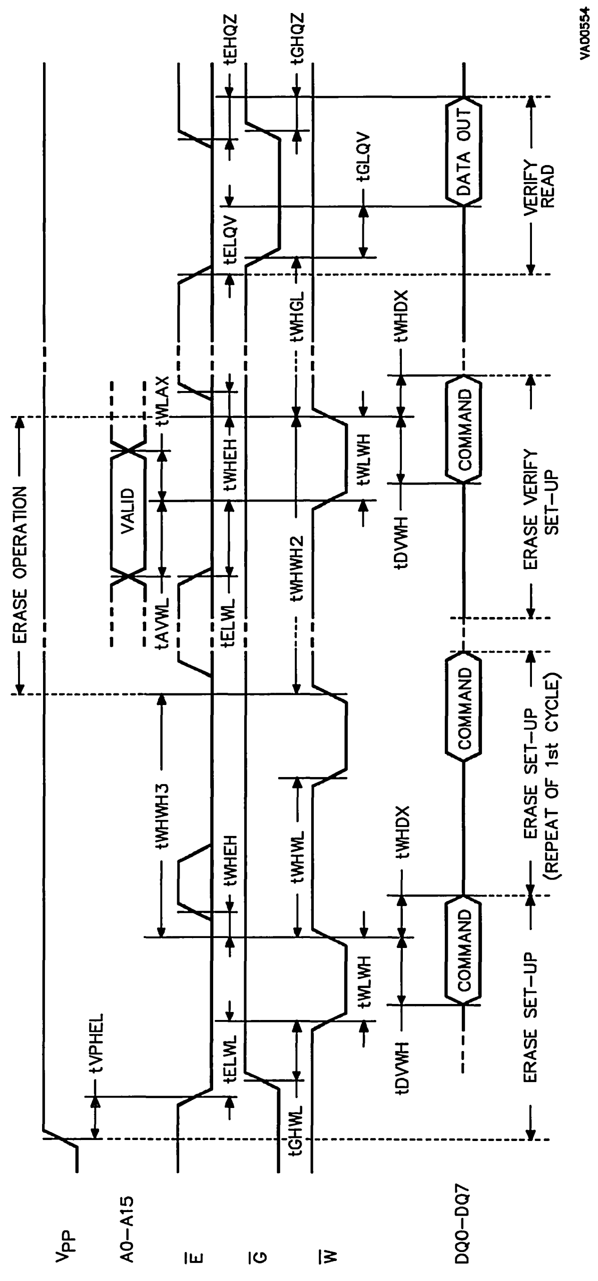

VPP
A0–A15
E
G
W
DQ0–DQ7
ERASE OPERATION
VALID
tVPHEL
tWHWH3
tAVWL
tWLAX
tELWL
tWHEH
tELWL
tWHEH
tELQV
tEHQZ
tGHWL
tWHWL
tWHWH2
tWHGL
tGHQZ
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
COMMAND
COMMAND
COMMAND
DATA OUT
ERASE SET–UP
ERASE SET–UP (REPEAT OF 1st CYCLE)
ERASE VERIFY SET–UP
VERIFY READ
VA00554

Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

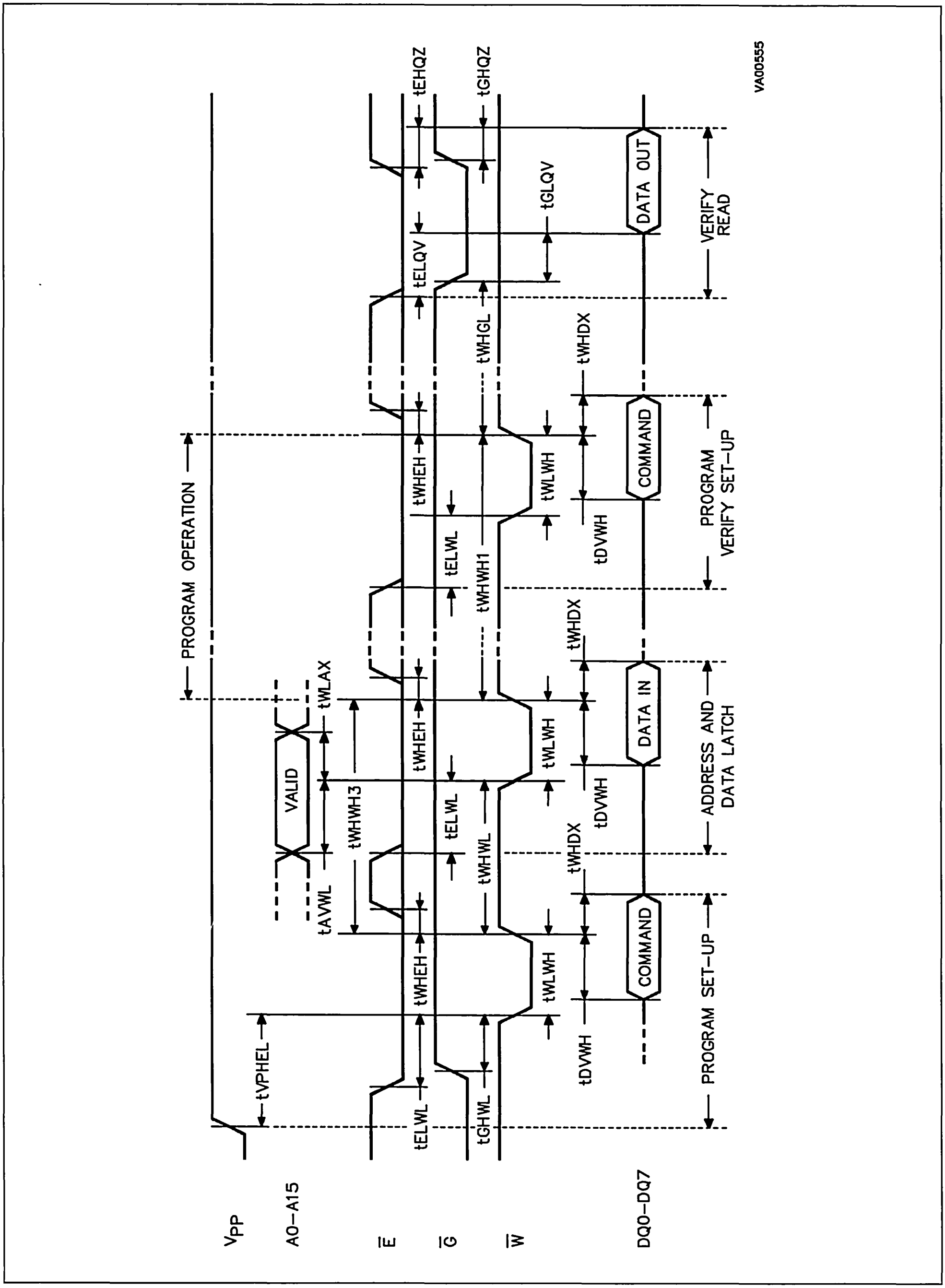

VPP
A0–A15
E
G
W
DQ0–DQ7
PROGRAM OPERATION
tVPHEL
VALID
tAVWL
tWLAX
tWHWH3
tELWL
tWHEH
tWHEH
tWHEH
tELWL
tELWL
tELQV
tEHQZ
tGHWL
tWHWL
tWHWH1
tWHGL
tGHQZ
tWLWH
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
tDVWH
tWHDX
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET-UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET-UP
VERIFY READ
VA00555

Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

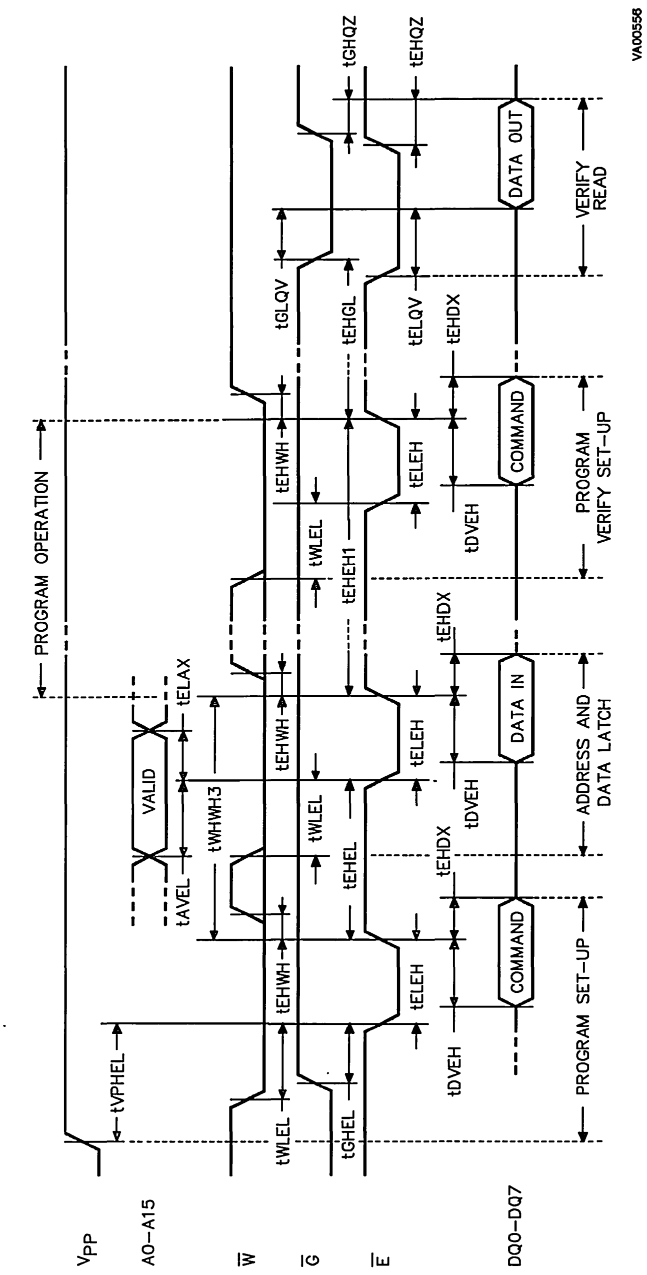
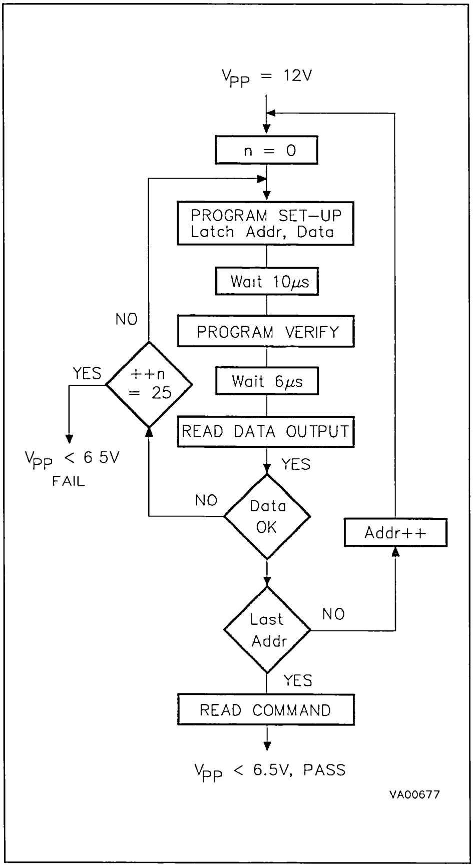
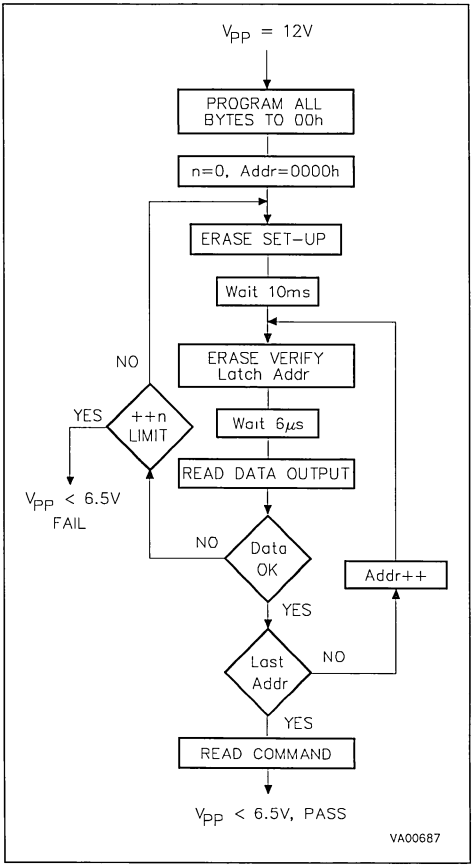

VPP
A0–A15
W̄
Ḡ
Ē
DQ0–DQ7
PROGRAM OPERATION
tVPHEL
VALID
tAVEL
tELAX
tWHWH3
tWLEL
tEHWH
tEHWH
tEHWH
tWLEL
tWLEL
tGLQV
tGHEL
tEHEL
tEHEH1
tEHGL
tGHQZ
tELEH
tELEH
tELEH
tELQV
tEHQZ
tDVEH
tEHDX
tDVEH
tEHDX
tDVEH
tEHDX
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET–UP
ADDRESS AND
DATA LATCH
PROGRAM
VERIFY SET–UP
VERIFY
READ
VA00556

Figure 11. Erasing Flowchart


VPP = 12V
n = 0
PROGRAM SET–UP
Latch Addr, Data
Wait 10µs
PROGRAM VERIFY
Wait 6µs
READ DATA OUTPUT
NO
YES
++n
= 25
VPP < 6 5V
FAIL
YES
NO
Data
OK
Addr++
Last
Addr
NO
YES
READ COMMAND
VPP < 6.5V, PASS
VA00677

Limit: 1000 at grades 1 & 6; 6000 at grade 3.

Figure 12. Programming Flowchart


VPP = 12V
PROGRAM ALL
BYTES TO 00h
n=0, Addr=0000h
ERASE SET–UP
Wait 10ms
ERASE VERIFY
Latch Addr
NO
YES
++n
LIMIT
Wait 6µs
READ DATA OUTPUT
VPP < 6.5V
FAIL
NO
Data
OK
Addr++
YES
Last
Addr
NO
YES
READ COMMAND
VPP < 6.5V, PASS
VA00687

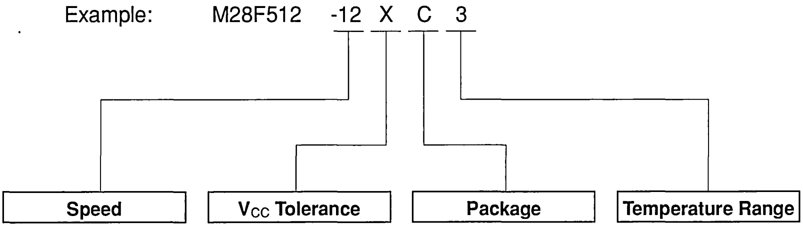
PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION


Example:
M28F512 -12 X C 3
Speed
V$_{CC}$ Tolerance
Package
Temperature Range

Speed	
-10	100 ns
-12	120 ns
-15	150 ns
-20	200 ns

V$_{CC}$ Tolerance	
X	± 5%
blank	± 10%

Package	
B	PDIP32
C	PLCC32

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

For a list of available options of Speed, V$_{CC}$ Tolerance, Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

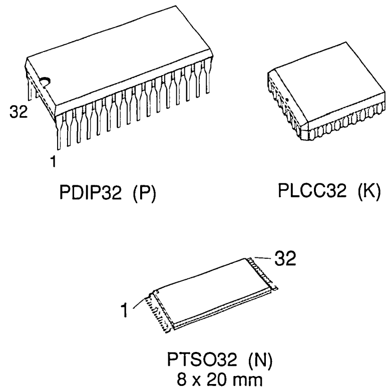
SGS-THOMSON
MICROELECTRONICS

M28F101

CMOS 1 Megabit (128K x 8) FLASH MEMORY

ADVANCE DATA

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



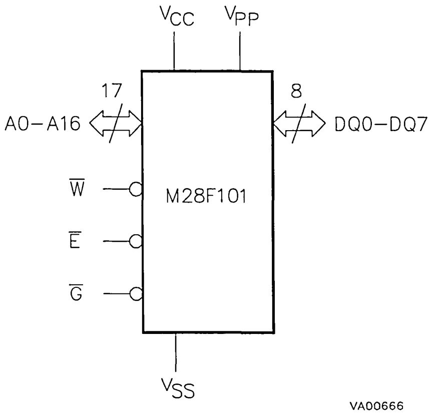
DESCRIPTION

The M28F101 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 128K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F101 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

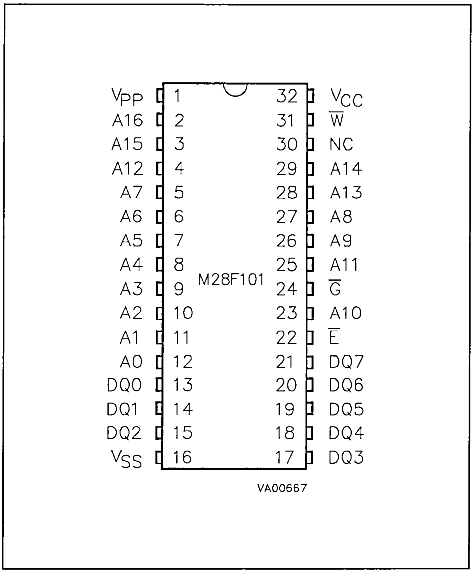
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



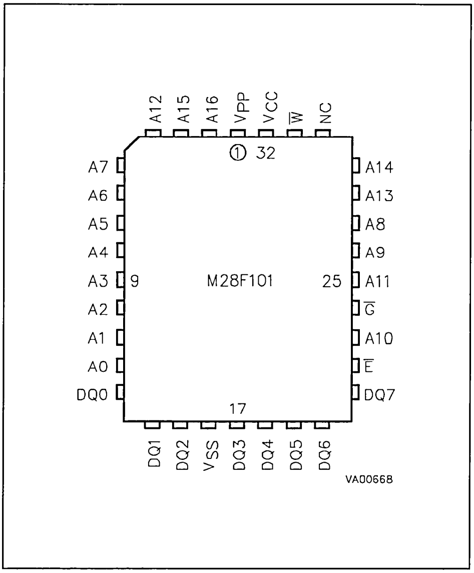
This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice

Figure 2A. DIP Pin Connections


VPP 1
A16 2
A15 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
DQ0 13
DQ1 14
DQ2 15
VSS 16
32 VCC
31 W
30 NC
29 A14
28 A13
27 A8
26 A9
25 A11
24 G
23 A10
22 E
21 DQ7
20 DQ6
19 DQ5
18 DQ4
17 DQ3
M28F101
VA00667

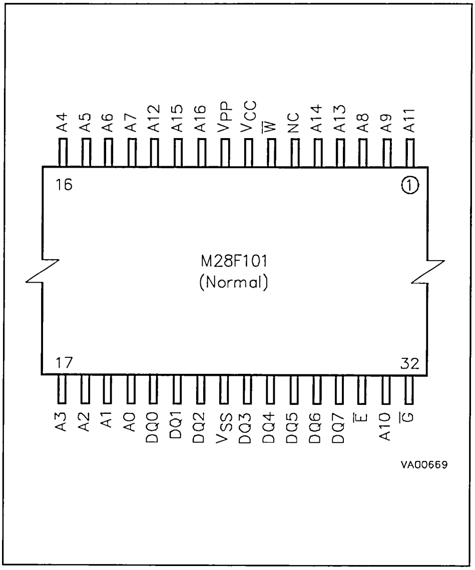
Warning: NC = No Connection

Figure 2B. LCC Pin Connections


A12
A15
A16
VPP
VCC
W
NC
① 32
A7
A6
A5
A4
A3 9
A2
A1
A0
DQ0
M28F101
25 A11
A14
A13
A8
A9
G
A10
E
DQ7
17
DQ1
DQ2
VSS
DQ3
DQ4
DQ5
DQ6
VA00668

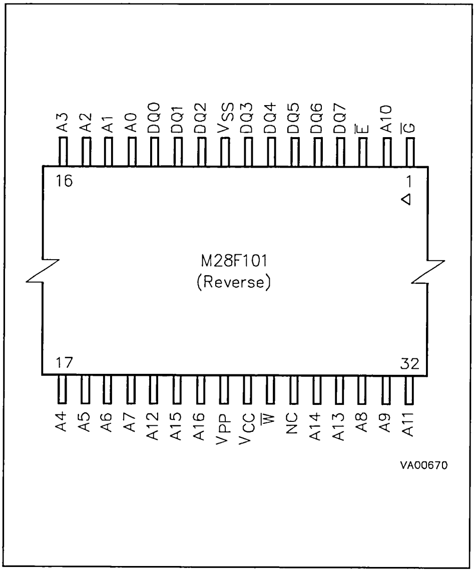
Warning: NC = No Connection

Figure 2C. PTSO Pin Connections


A4
A5
A6
A7
A12
A15
A16
VPP
VCC
W
NC
A14
A13
A8
A9
A11
16
①
M28F101
(Normal)
17
32
A3
A2
A1
A0
DQ0
DQ1
DQ2
VSS
DQ3
DQ4
DQ5
DQ6
DQ7
E
A10
G
VA00669

Warning: NC = No Connection

Figure 2D. PTSO Reverse Pin Connections


A3
A2
A1
A0
DQ0
DQ1
DQ2
VSS
DQ3
DQ4
DQ5
DQ6
DQ7
E
A10
G
16
1
M28F101
(Reverse)
17
32
A4
A5
A6
A7
A12
A15
A16
VPP
VCC
W
NC
A14
A13
A8
A9
A11
VA00670

Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F101 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F101 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F101 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	1	1	07h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A16	DQ0-DQ7	Operation	A0-A16	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	00000h	20h
					Read	00001h	07h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A16	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A16	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

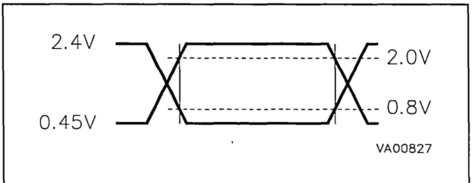


Figure 4. AC Testing Load Circuit

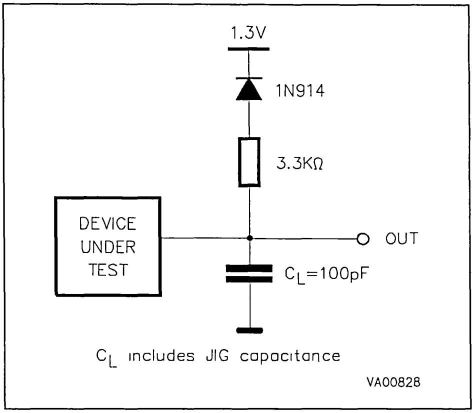


Table 6. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: this parameter is sampled only and not tested100%

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming (grade 1 & 6)		10	mA
		During Programming (grade 3)		30	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify (grade 1 & 6)		15	mA
		During Verify (grade 3)		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure (grade 1 & 6)		15	mA
		During Erasure (grade 3)		30	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify (grade 1 & 6)		15	mA
		During Erase Verify (grade 3)		30	mA
I_{CC6}	Supply Current (Electronic Signature)	A9 = V_{ID} (grade 3 only)		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \leq V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \leq V_{CC}$		±10	µA
I_{PP1}(1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2}(1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3}(1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4}(1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
I_{PP5}(1)	Program Current (Electronic Signature)	A9 = V_{ID} (grade 3 only)		500	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grades 3 & 6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% Tested Characterisation Data available

Table 8A. Read Only Mode AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101				Unit
				-100		-120		
				Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	45	0	55	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	0		0		ns

Note: 1 Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics

((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

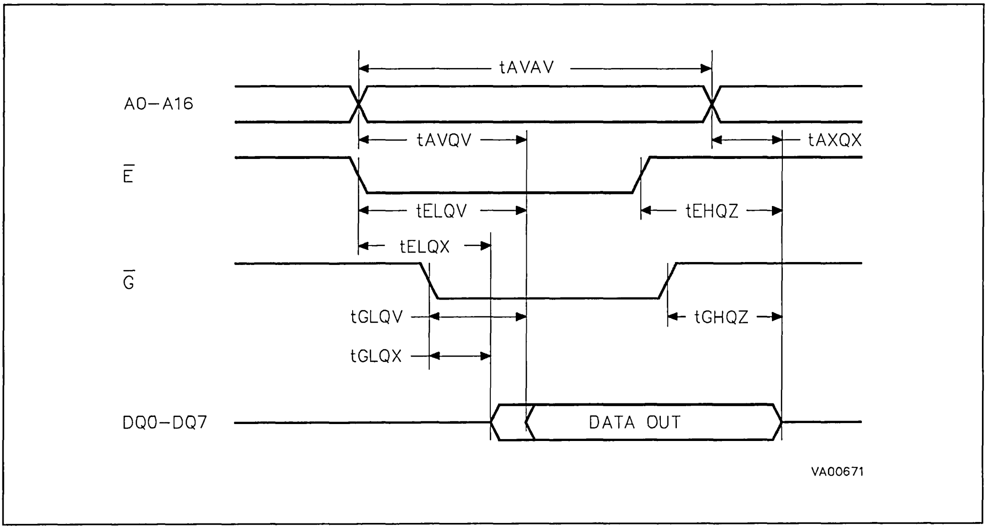

tAVAV
A0–A16
tAVQV
tAXQX
E
tELQV
tEHQZ
tELQX
G
tGLQV
tGHQZ
tGLQX
DQ0–DQ7
DATA OUT
VA00671

Figure 6. Read Command Waveforms

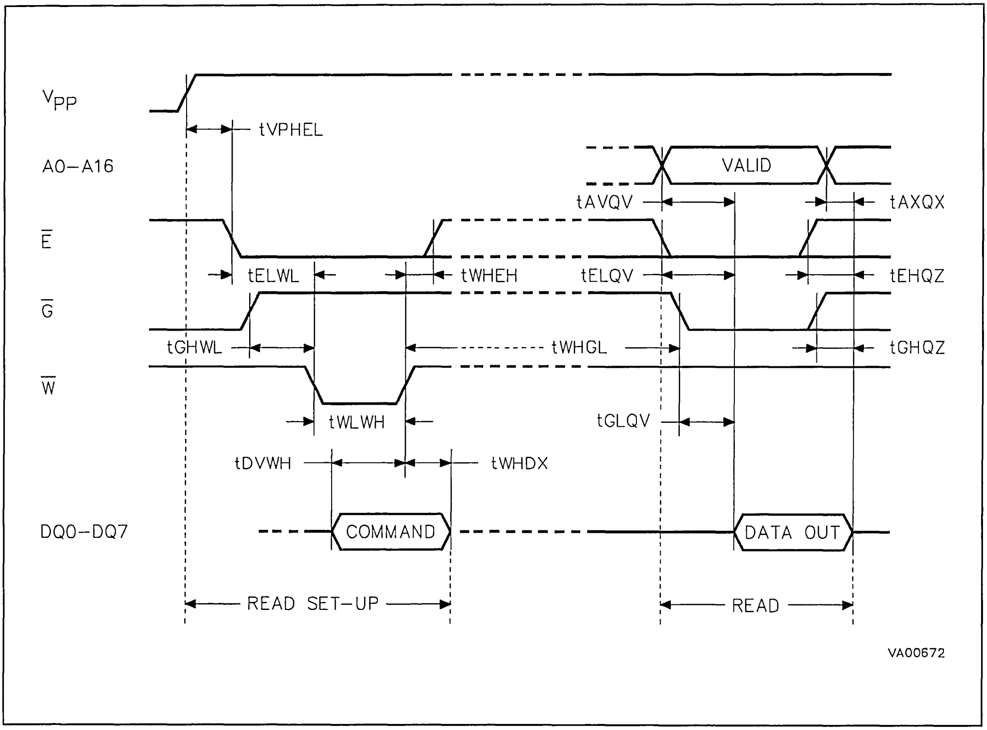
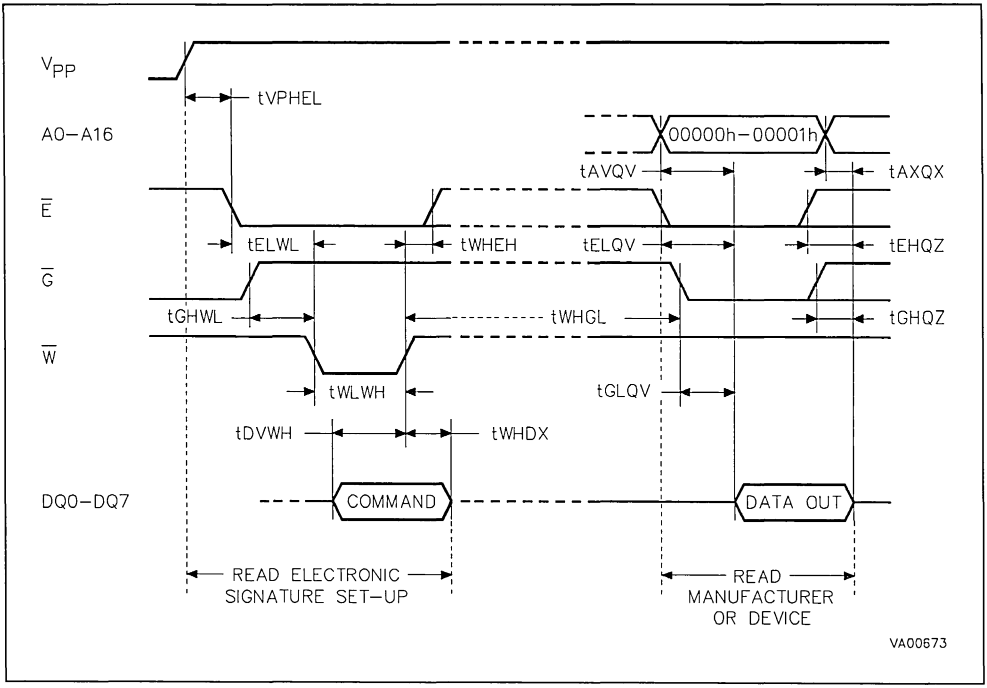

VPP
tVPHEL
A0–A16
VALID
tAVQV
tAXQX
E
tELWL
tWHEH
tELQV
tEHQZ
G
tGHWL
tWHGL
tGHQZ
W
tWLWH
tGLQV
tDVWH
tWHDX
DQ0–DQ7
COMMAND
DATA OUT
READ SET–UP
READ
VA00672

Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 9A. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F101				Unit
			-10		-12		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		40		50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 9B. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F101				Unit
			-150		-200		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

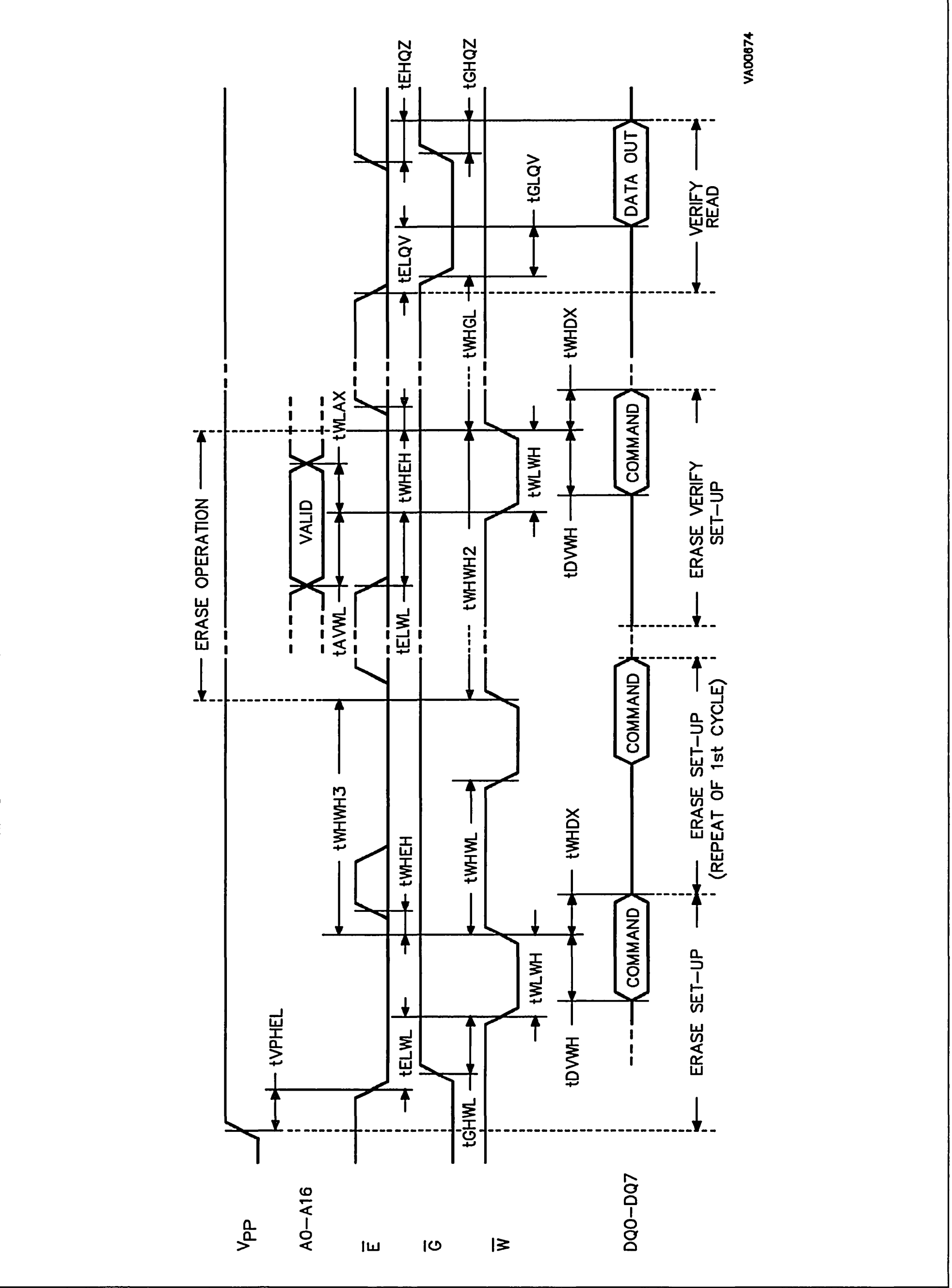

VPP
A0–A16
E
G
W
DQ0–DQ7
ERASE OPERATION
tVPHEL
VALID
tWHWH3
tAVWL
tWLAX
tELWL
tWHEH
tELWL
tWHEH
tELQV
tEHQZ
tGHWL
tWHWL
tWHWH2
tWHGL
tGHQZ
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
COMMAND
COMMAND
COMMAND
DATA OUT
ERASE SET–UP
ERASE SET–UP
(REPEAT OF 1st CYCLE)
ERASE VERIFY
SET–UP
VERIFY
READ
VA00674

Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

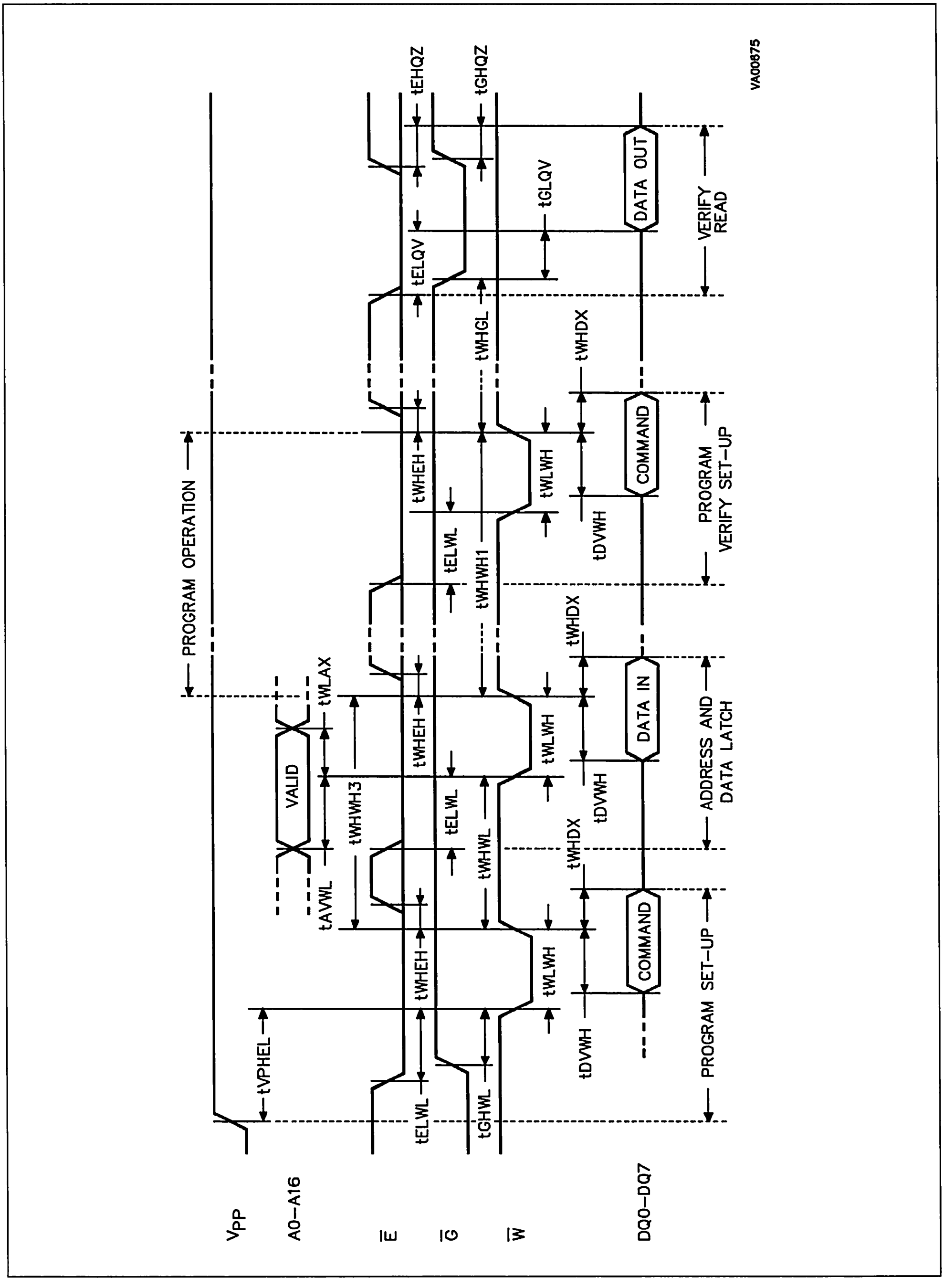

VPP
A0–A16
E
G
W
DQ0–DQ7
PROGRAM OPERATION
tVPHEL
VALID
tAVWL
tWLAX
tWHWH3
tELWL
tWHEH
tGHWL
tWHWL
tWHWH1
tWHGL
tELQV
tEHQZ
tGHQZ
tGLQV
tWLWH
tDVWH
tWHDX
COMMAND
DATA IN
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
VA00675

Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

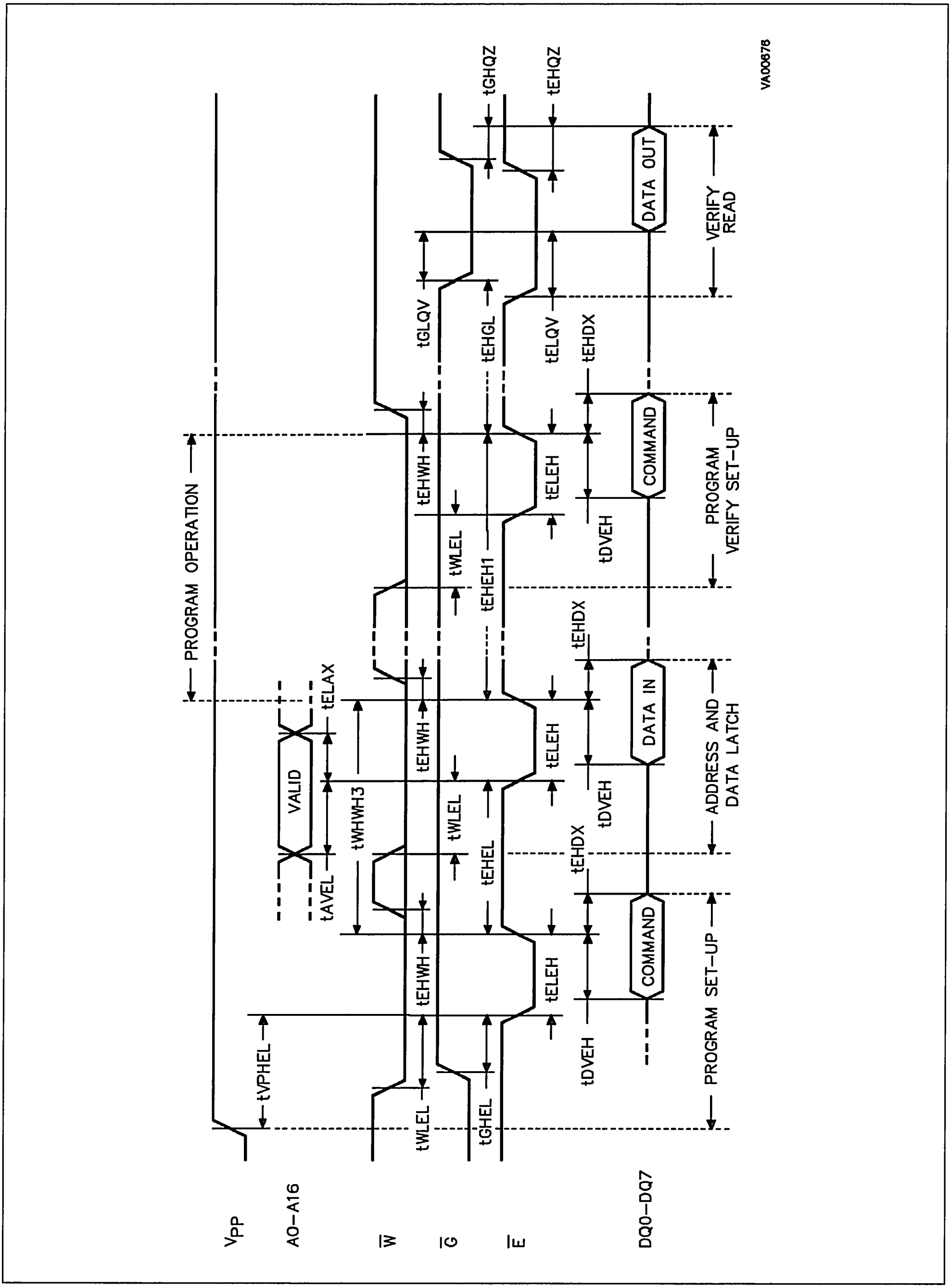
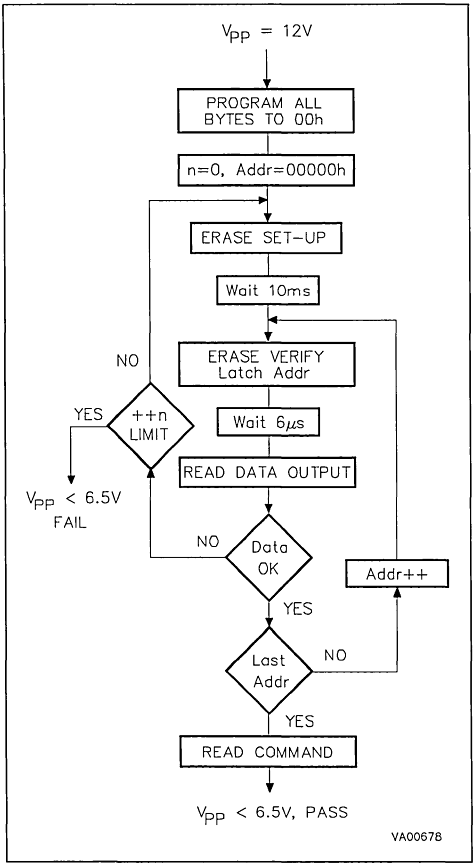
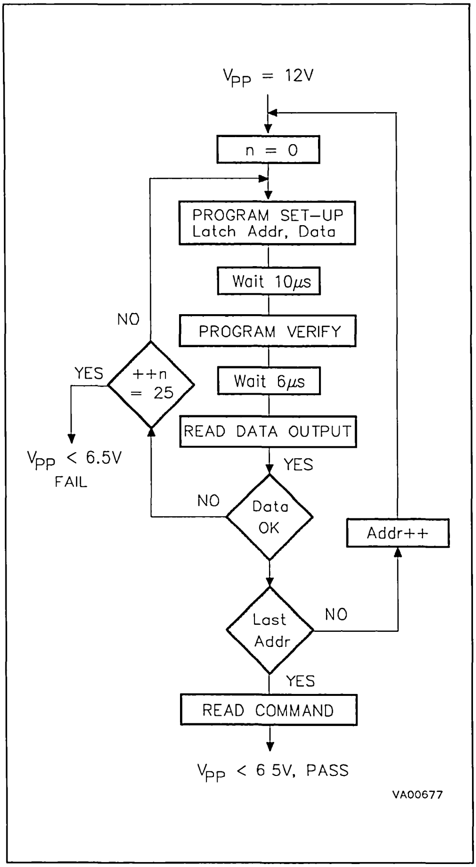

VPP
A0–A16
W̅
G̅
E̅
DQ0–DQ7
PROGRAM OPERATION
tVPHEL
VALID
tAVEL
tELAX
tWHWH3
tWLEL
tEHWH
tGLQV
tGHEL
tEHEL
tEHEH1
tEHGL
tGHQZ
tELEH
tELQV
tEHQZ
tDVEH
tEHDX
COMMAND
DATA IN
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
VA00678

Figure 11. Erasing Flowchart


V_{PP} = 12V
PROGRAM ALL BYTES TO 00h
n=0, Addr=00000h
ERASE SET–UP
Wait 10ms
ERASE VERIFY Latch Addr
Wait 6µs
READ DATA OUTPUT
Data OK
NO
YES
Last Addr
NO
YES
Addr++
READ COMMAND
V_{PP} < 6.5V, PASS
++n LIMIT
NO
YES
V_{PP} < 6.5V FAIL
VA00678

Limit: 1000 at grade 1; 6000 at grades 3 & 6.

Figure 12. Programming Flowchart


V_{PP} = 12V
n = 0
PROGRAM SET–UP Latch Addr, Data
Wait 10µs
PROGRAM VERIFY
Wait 6µs
READ DATA OUTPUT
YES
Data OK
NO
++n = 25
NO
YES
V_{PP} < 6.5V FAIL
Last Addr
NO
YES
Addr++
READ COMMAND
V_{PP} < 6 5V, PASS
VA00677

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION

Example: M28F101 -100 X N 1 R

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-100	100 ns	X	± 5%	P	PDIP32	1	0 to 70 °C	R	Reverse Pin-Out
-120	120 ns	blank	± 10%	K	PLCC32	3	–40 to 125 °C		
-150	150 ns			N	PTSO32 8 x 20 mm	6	–40 to 85 °C		
-200	200 ns								

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

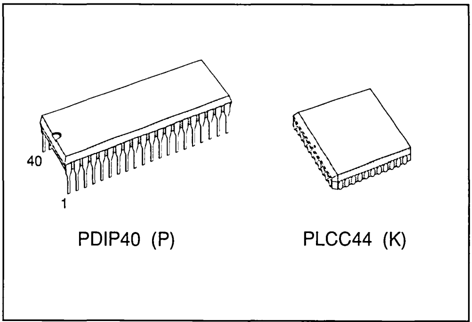
For further information on any aspect of this device, please contact our Sales Office nearest you.

M28F102

CMOS 1 Megabit (64K x 16) FLASH MEMORY

ADVANCE DATA

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



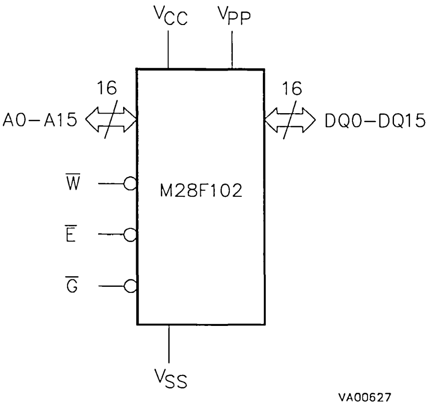
DESCRIPTION

The M28F102 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed word-by-word. It is organised as 64K words of 16 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F102 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

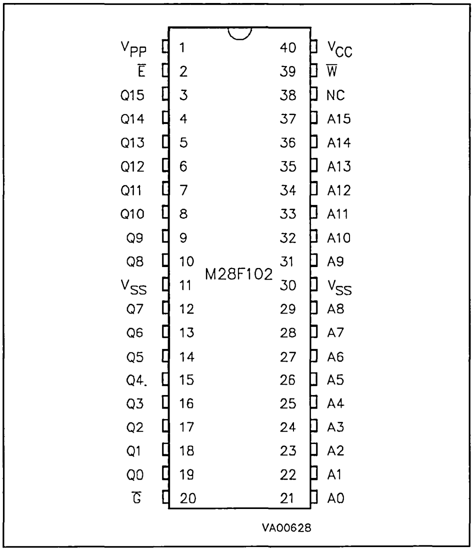
A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



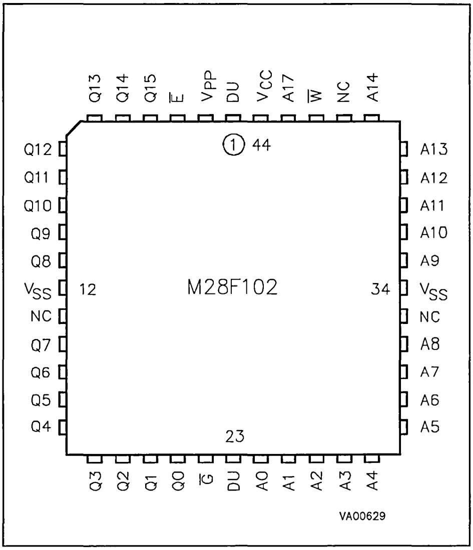
This is advance information on a new product now in development or undergoing evaluation Details are subject to change without notice

Figure 2A. DIP Pin Connections


VPP 1 40 VCC
E 2 39 W
Q15 3 38 NC
Q14 4 37 A15
Q13 5 36 A14
Q12 6 35 A13
Q11 7 34 A12
Q10 8 33 A11
Q9 9 32 A10
Q8 10 31 A9
VSS 11 30 VSS
Q7 12 29 A8
Q6 13 28 A7
Q5 14 27 A6
Q4 15 26 A5
Q3 16 25 A4
Q2 17 24 A3
Q1 18 23 A2
Q0 19 22 A1
G 20 21 A0
M28F102
VA00628

Warning: NC = No Connection

Figure 2B. LCC Pin Connections


Q13 Q14 Q15 E VPP DU VCC A17 W NC A14
Q12 Q11 Q10 Q9 Q8 VSS NC Q7 Q6 Q5 Q4
A13 A12 A11 A10 A9 VSS NC A8 A7 A6 A5
Q3 Q2 Q1 Q0 G DU A0 A1 A2 A3 A4
1
44
12
34
23
M28F102
VA00629

Warning: NC = No Connection, DU = Don't Use

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}	A9 Voltage	–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming	–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DEVICE OPERATION

The M28F102 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F102 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F102 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 50mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 0000h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 0000h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when

Table 3. Operations [1]

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ15
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write [2]	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ15-DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	0	1	0	0	0	0	0	0020h
Device Code	V_{IH}	0	0	1	0	1	0	0	0	0	0050h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A15	DQ0-DQ15	Operation	A0-A15	DQ0-DQ15
Read	1	Write	X	0000h			
Electronic Signature	2	Write	X	0090h	Read	0000h	0020h
					Read	0001h	0050h
Setup Erase/	2	Write	X	0020h			
Erase					Write	X	0020h
Erase Verify	2	Write	A0-A15	00A0h	Read	X	Data Output
Setup Program/	2	Write	X	0040h			
Program					Write	A0-A15	Data Input
Program Verify	2	Write	X	00C0h	Read	X	Data Output
Reset	2	Write	X	0FFFFh	Write	X	0FFFFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 0000h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 0090h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 0000h, the Erase command then erases them to 0FFFFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFFFh.

The Erase Mode is set-up by writing 0020h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is

READ/WRITE MODES (cont'd)

followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 00A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFFFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 00A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFFFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 00C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFFFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

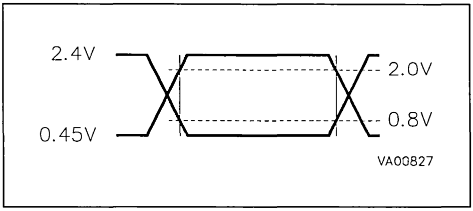


Figure 4. AC Testing Load Circuit

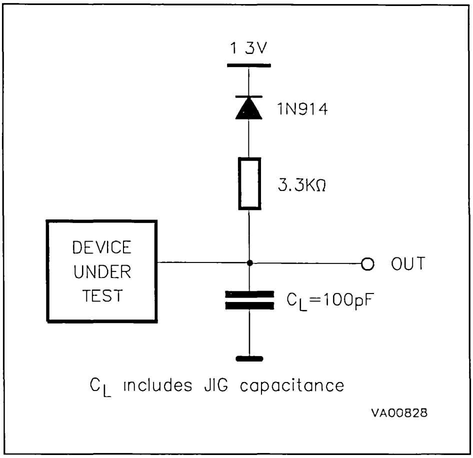


Table 6. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: this parameter is sampled only and not tested100%

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1}(1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		50	mA
I_{PP2}(1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3}(1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		50	mA
I_{PP4}(1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 3 & 6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% Tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F102				Unit
				-100		-120		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics

((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F102				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

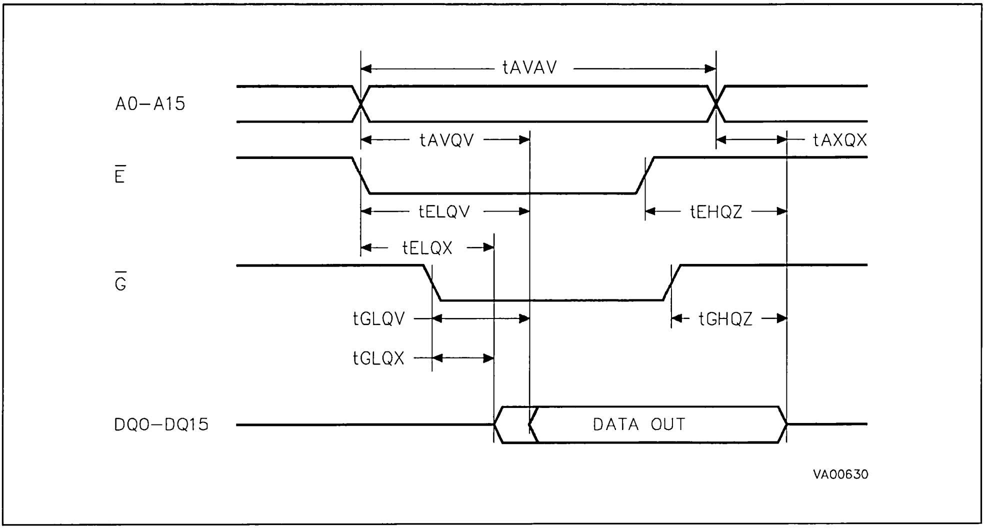

tAVAV
A0–A15
tAVQV
tAXQX
E
tELQV
tEHQZ
tELQX
G
tGLQV
tGHQZ
tGLQX
DQ0–DQ15
DATA OUT
VA00630

Figure 6. Read Command Waveforms

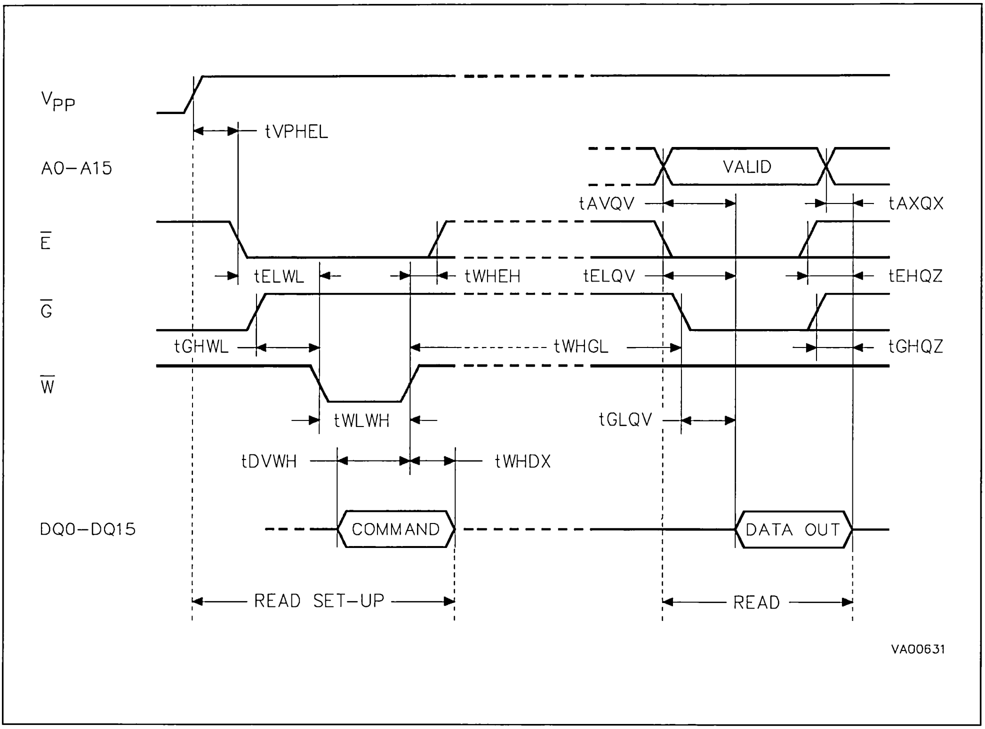

VPP
tVPHEL
A0–A15
VALID
tAVQV
tAXQX
E
tELWL
tWHEH
tELQV
tEHQZ
G
tGHWL
tWHGL
tGHQZ
W
tWLWH
tGLQV
tDVWH
tWHDX
DQ0–DQ15
COMMAND
DATA OUT
READ SET-UP
READ
VA00631

Figure 7. Electronic Signature Command Waveforms

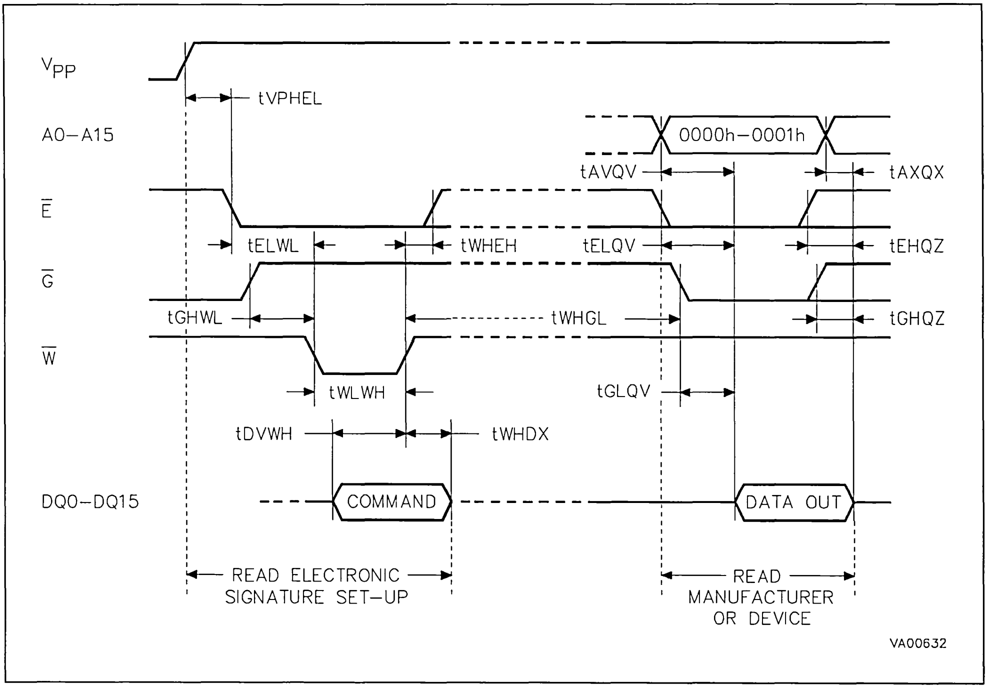

VPP
tVPHEL
A0-A15
0000h-0001h
tAVQV
tAXQX
E
tELWL
tWHEH
tELQV
tEHQZ
G
tGHWL
tWHGL
tGHQZ
W
tWLWH
tGLQV
tDVWH
tWHDX
DQ0-DQ15
COMMAND
DATA OUT
READ ELECTRONIC SIGNATURE SET-UP
READ MANUFACTURER OR DEVICE
VA00632

Table 9A. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F102				Unit
			-100		-120		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		40		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

Table 9B. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F102				Unit
			-150		-200		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		80		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

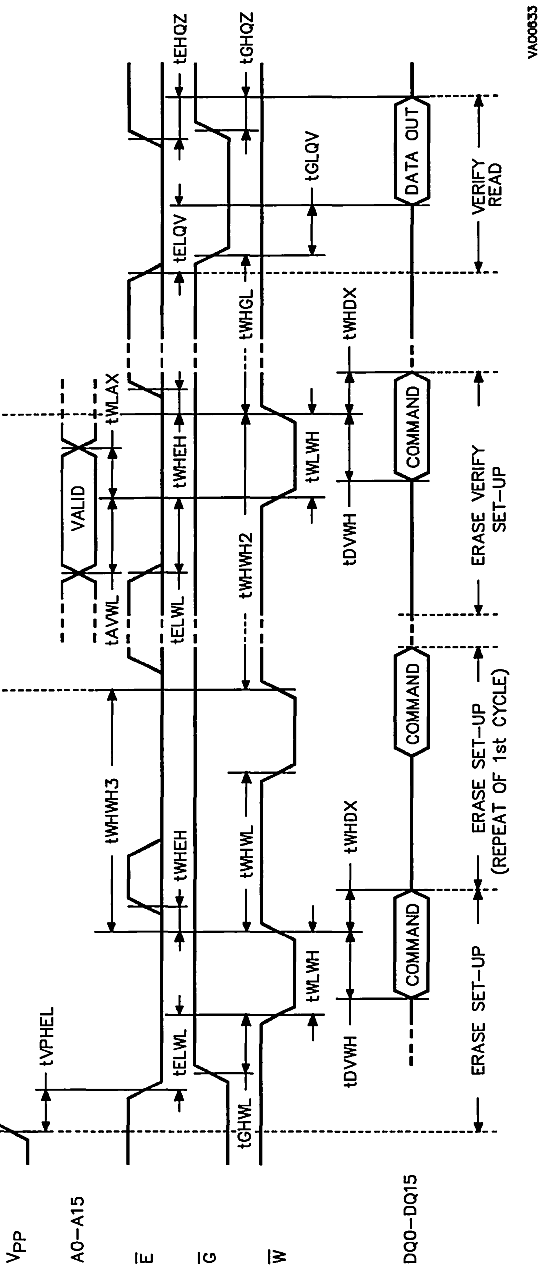

VPP
A0–A15
E
G
W
DQ0–DQ15
ERASE OPERATION
tVPHEL
VALID
tWHWH3
tAVWL
tWLAX
tELWL
tWHEH
tELWL
tWHEH
tELQV
tEHQZ
tGHWL
tWHWL
tWHWH2
tWHGL
tGHQZ
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
COMMAND
COMMAND
COMMAND
DATA OUT
ERASE SET–UP
ERASE SET–UP
(REPEAT OF 1st CYCLE)
ERASE VERIFY
SET–UP
VERIFY
READ
VA00833

Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

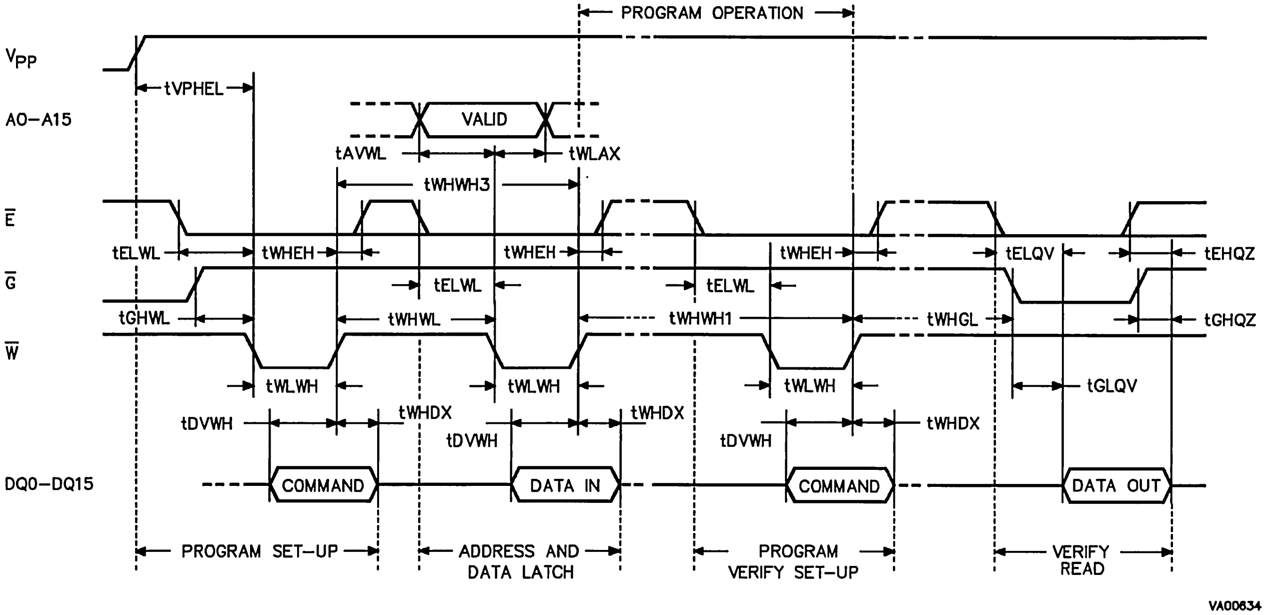

PROGRAM OPERATION
VPP
tVPHEL
A0–A15
VALID
tAVWL
tWLAX
tWHWH3
E
tELWL
tWHEH
tWHEH
tWHEH
tELQV
tEHQZ
G
tELWL
tELWL
tGHWL
tWHWL
tWHWH1
tWHGL
tGHQZ
W
tWLWH
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
tDVWH
tWHDX
DQ0–DQ15
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
VA00634

Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

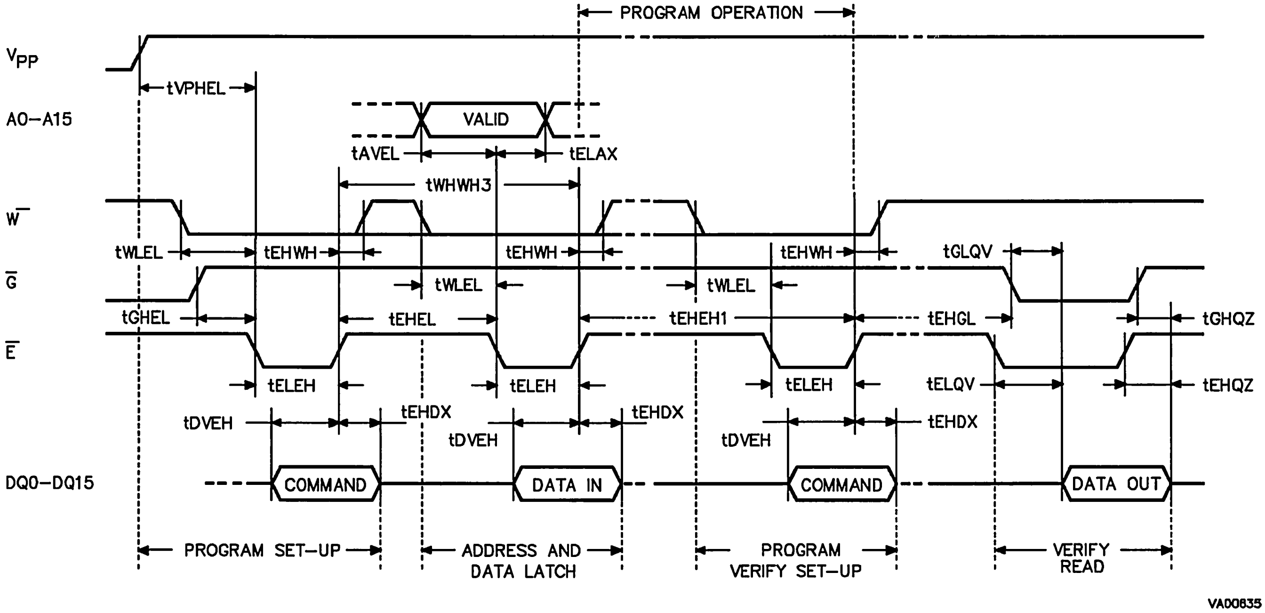
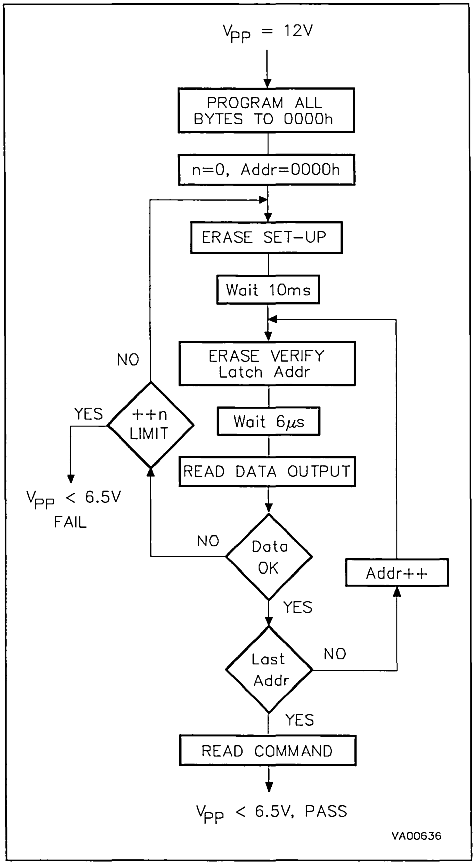
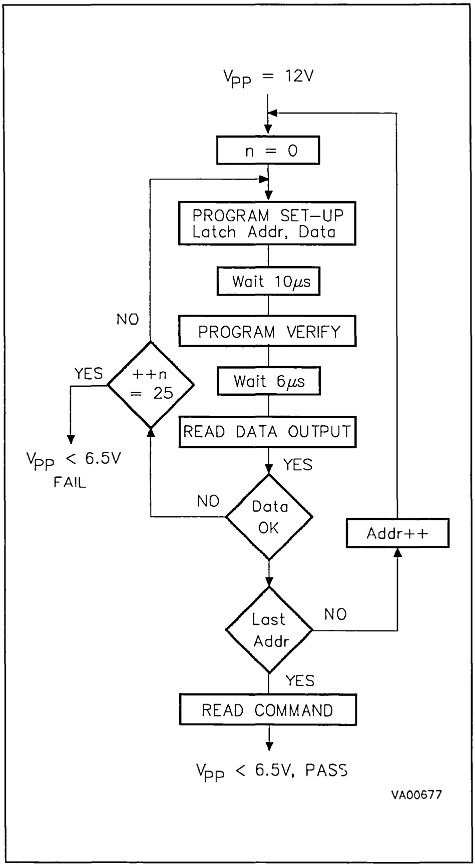

PROGRAM OPERATION
VPP
tVPHEL
A0–A15
VALID
tAVEL
tELAX
tWHWH3
W
tWLEL
tEHWH
tEHWH
tEHWH
tGLQV
G
tWLEL
tWLEL
tGHEL
tEHEL
tEHEH1
tEHGL
tGHQZ
E
tELEH
tELEH
tELEH
tELQV
tEHQZ
tEHDX
tEHDX
tEHDX
tDVEH
tDVEH
tDVEH
DQ0–DQ15
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
VA00635

Figure 11. Erasing Flowchart


VPP = 12V
PROGRAM ALL BYTES TO 0000h
n=0, Addr=0000h
ERASE SET-UP
Wait 10ms
ERASE VERIFY Latch Addr
Wait 6µs
READ DATA OUTPUT
Data OK
NO
YES
Last Addr
NO
YES
Addr++
READ COMMAND
VPP < 6.5V, PASS
++n LIMIT
NO
YES
VPP < 6.5V
FAIL
VA00636

Limit: 1000 at grade 1; 6000 at grades 3 & 6.

Figure 12. Programming Flowchart


VPP = 12V
n = 0
PROGRAM SET-UP Latch Addr, Data
Wait 10µs
PROGRAM VERIFY
Wait 6µs
READ DATA OUTPUT
YES
Data OK
NO
Last Addr
NO
YES
Addr++
READ COMMAND
VPP < 6.5V, PASS
++n = 25
NO
YES
VPP < 6.5V
FAIL
VA00677

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all words to 0000h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 0020h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 00A0h to the command register together with the address of the word to be verified. The subsequent read cycle reads the data which is compared to 0FFFFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFFFh fails. If this occurs, the address of the last word checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a word until a correct verify occurs. Up to 25 programming operations are allowed for one word. Program is set-up by writing 0040h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 00C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION

Example: M28F102 -100 X P 1

Speed	
-100	100 ns
-120	120 ns
-150	150 ns
-200	200 ns

V_{CC} Tolerance	
X	± 5%
blank	± 10%

Package	
P	PDIP40
K	PLCC44

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

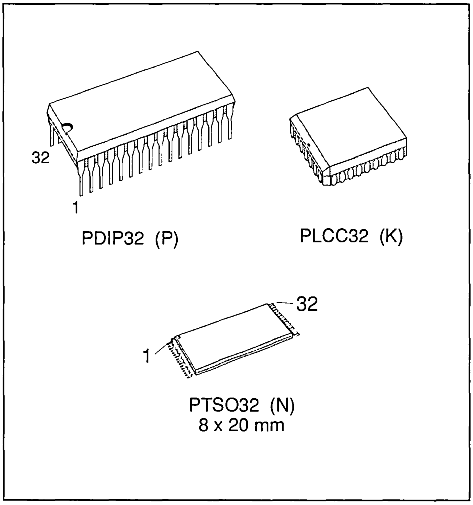
For further information on any aspect of this device, please contact our Sales Office nearest you.

M28F201

CMOS 2 Megabit (256K x 8) FLASH MEMORY

ADVANCE DATA

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



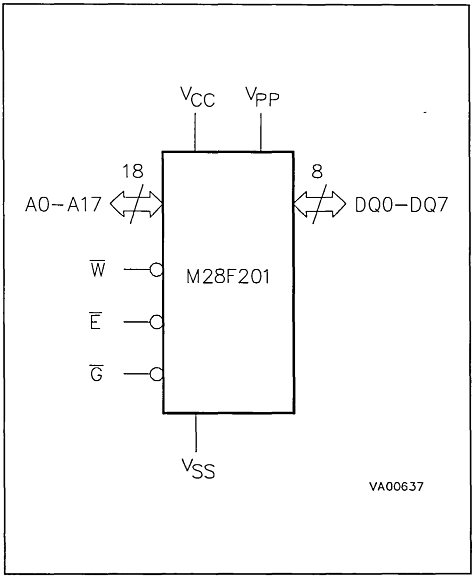
DESCRIPTION

The M28F201 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 256K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F201 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

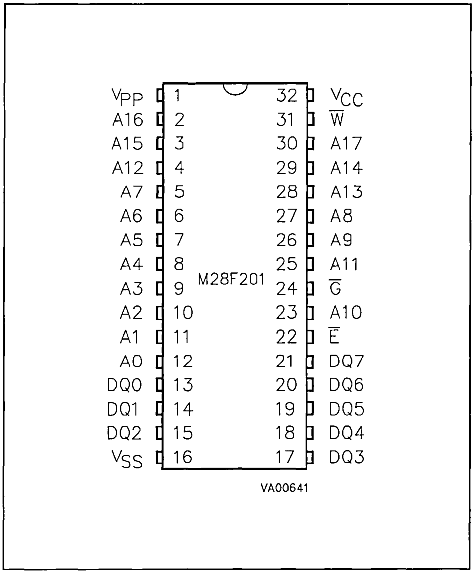
A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



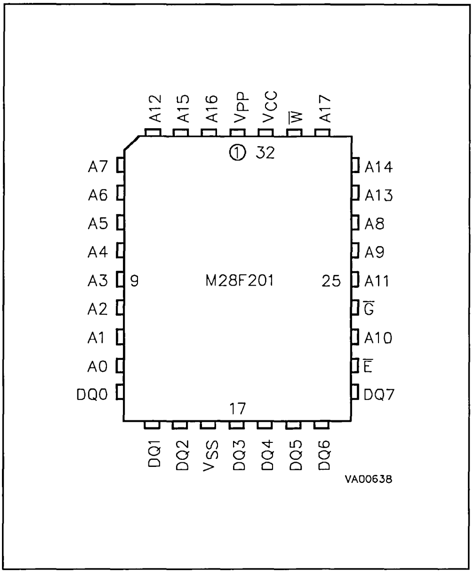
This is advance information on a new product now in development or undergoing evaluation Details are subject to change without notice

Figure 2A. DIP Pin Connections


VPP 1
A16 2
A15 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
DQ0 13
DQ1 14
DQ2 15
VSS 16
32 VCC
31 W
30 A17
29 A14
28 A13
27 A8
26 A9
25 A11
24 G
23 A10
22 E
21 DQ7
20 DQ6
19 DQ5
18 DQ4
17 DQ3
M28F201
VA00641

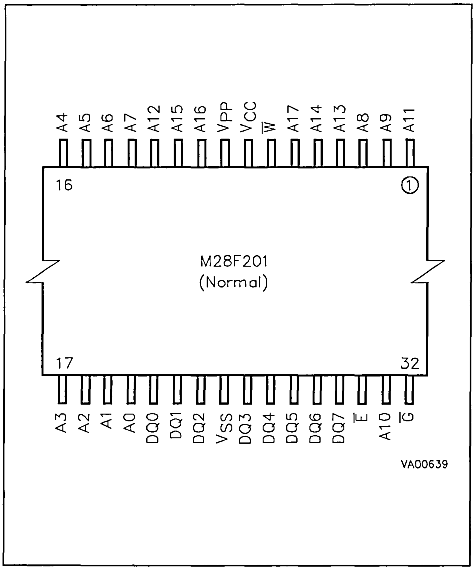
Warning: NC = No Connection

Figure 2B. LCC Pin Connections


A12 A15 A16 VPP VCC W A17
① 32
A7 A6 A5 A4 A3 A2 A1 A0 DQ0
9
M28F201
25
A14 A13 A8 A9 A11 G A10 E DQ7
17
DQ1 DQ2 VSS DQ3 DQ4 DQ5 DQ6
VA00638

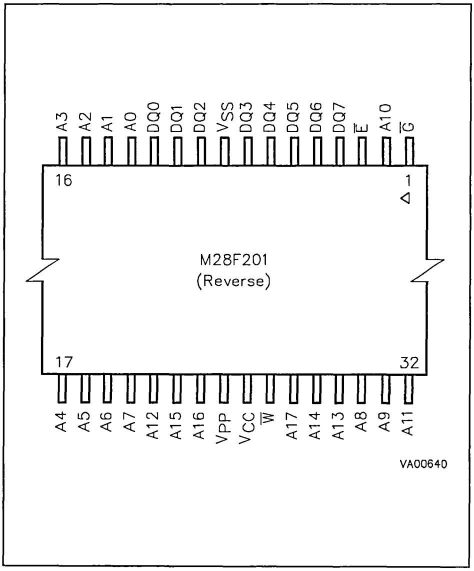
Warning: NC = No Connection

Figure 2C. PTSO Pin Connections


A4 A5 A6 A7 A12 A15 A16 VPP VCC W A17 A14 A13 A8 A9 A11
16
①
M28F201
(Normal)
17
32
A3 A2 A1 A0 DQ0 DQ1 DQ2 VSS DQ3 DQ4 DQ5 DQ6 DQ7 E A10 G
VA00639

Warning: NC = No Connection

Figure 2D. PTSO Reverse Pin Connections


A3 A2 A1 A0 DQ0 DQ1 DQ2 VSS DQ3 DQ4 DQ5 DQ6 DQ7 E A10 G
16
1
M28F201
(Reverse)
17
32
A4 A5 A6 A7 A12 A15 A16 VPP VCC W A17 A14 A13 A8 A9 A11
VA00640

Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F201 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and the M28F201 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F201 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device code. All other address lines should be maintained Low while reading the codes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	1	0	0	0	1	11h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A17	DQ0-DQ7	Operation	A0-A17	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	00000h	20h
					Read	00001h	11h
Setup Erase/	2	Write	X	20h			
Erase					Write	X	20h
Erase Verify	2	Write	A0-A17	0A0h	Read	X	Data Output
Setup Program/	2	Write	X	40h			
Program					Write	A0-A17	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

When the device is powered up and when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for onboard programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

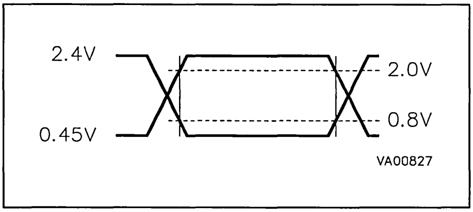


Figure 4. AC Testing Load Circuit

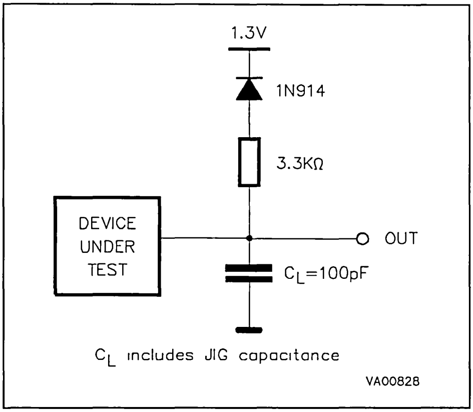


Table 6. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: this parameter is sampled only and not tested100%

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		15	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify)		15	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1}(1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2}(1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3}(1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4}(1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% Tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F201				Unit
				-100		-120		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics

((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F201				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	55	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

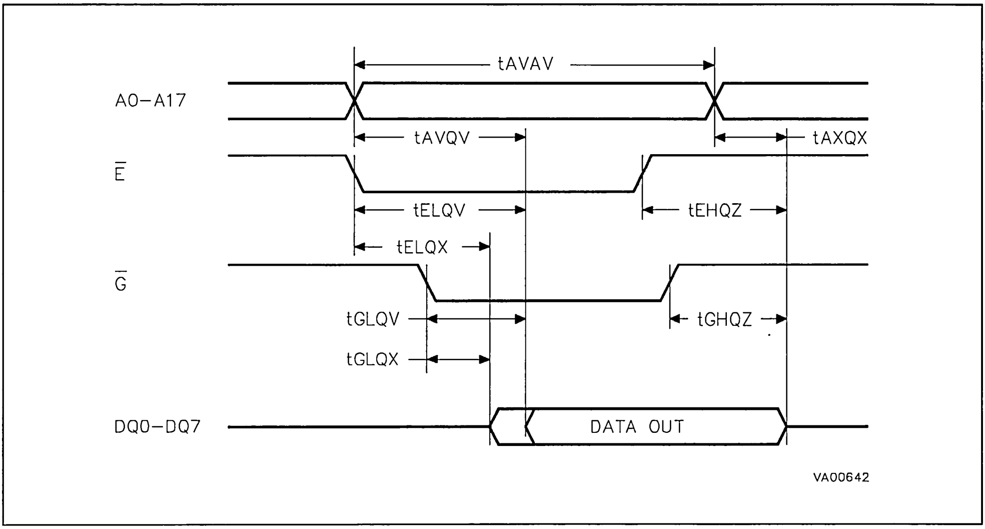

A0-A17
$\overline{E}$
$\overline{G}$
DQ0-DQ7
tAVAV
tAVQV
tAXQX
tELQV
tEHQZ
tELQX
tGLQV
tGHQZ
tGLQX
DATA OUT
VA00642

Figure 6. Read Command Waveforms

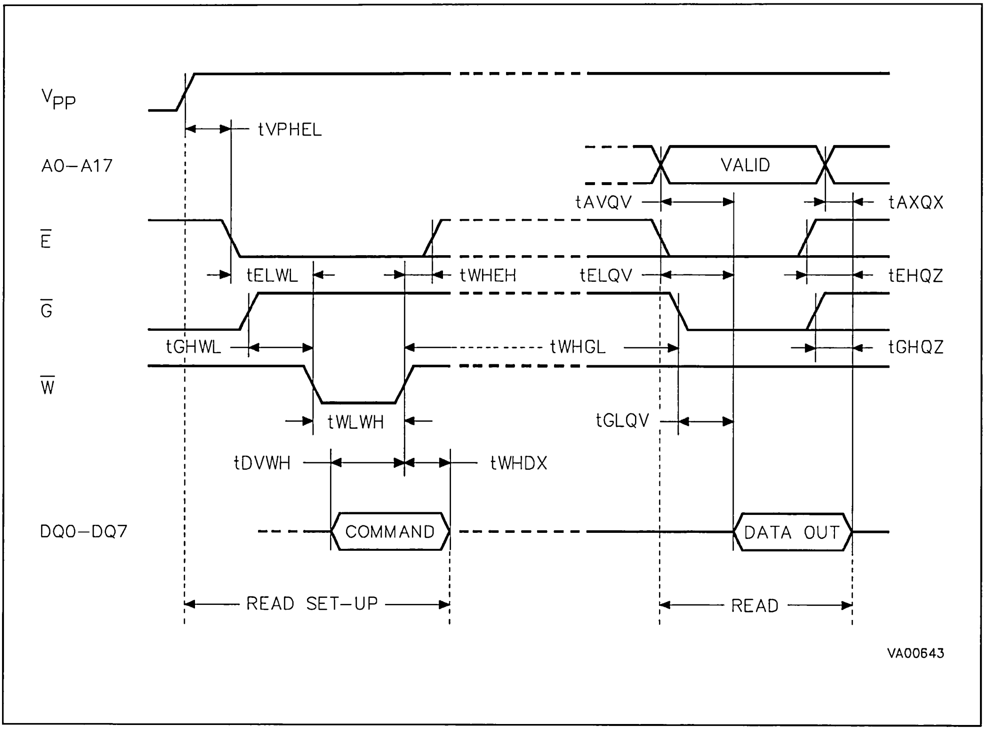
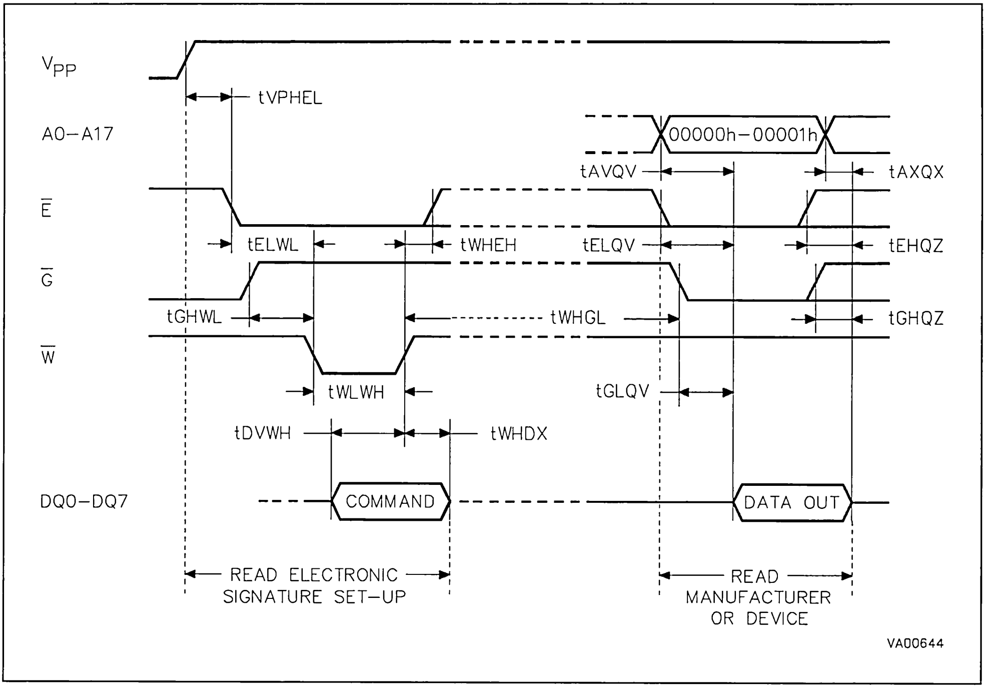

VPP
A0-A17
$\overline{E}$
$\overline{G}$
$\overline{W}$
DQ0-DQ7
tVPHEL
VALID
tAVQV
tAXQX
tELWL
tWHEH
tELQV
tEHQZ
tGHWL
tWHGL
tGHQZ
tWLWH
tGLQV
tDVWH
tWHDX
COMMAND
DATA OUT
READ SET-UP
READ
VA00643

Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this second cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 9A. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F201				Unit
			-100		-120		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	40		50		ns
t_{ELAX}		Chip Enable Low to Address Transition	40		50		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	40		40		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		30		30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Table 9B. Read/Write Mode AC Characteristics - $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	M28F201				Unit
			-150		-200		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{AVAV}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		95		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		80		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		35		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

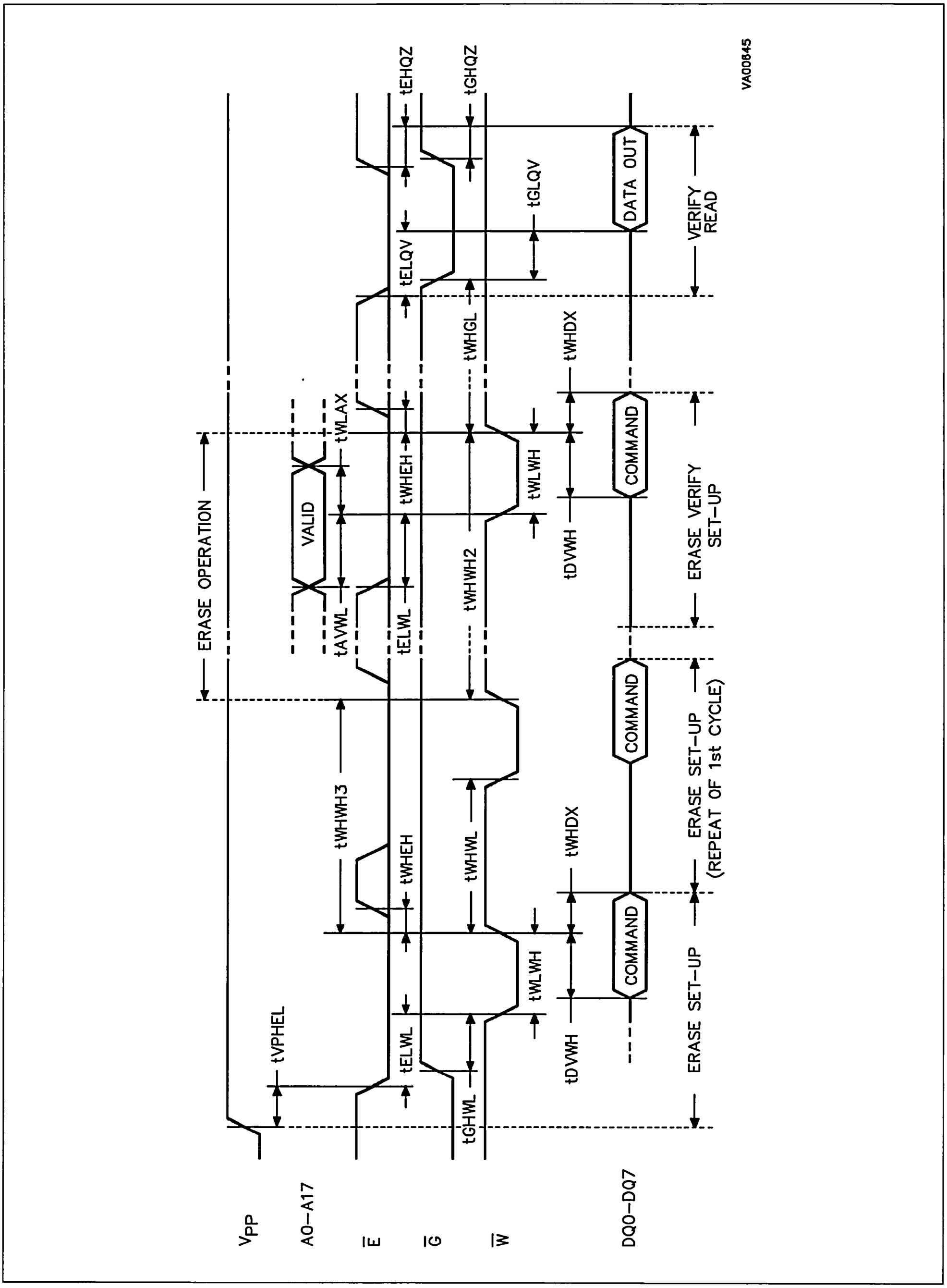

VPP
A0–A17
E
G
W
DQ0–DQ7
ERASE OPERATION
VALID
tVPHEL
tWHWH3
tAVWL
tWLAX
tELWL
tWHEH
tELWL
tWHEH
tELQV
tEHQZ
tGHWL
tWHWL
tWHWH2
tWHGL
tGHQZ
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
COMMAND
COMMAND
COMMAND
DATA OUT
ERASE SET–UP
ERASE SET–UP
(REPEAT OF 1st CYCLE)
ERASE VERIFY
SET–UP
VERIFY
READ
VA00845

Figure 9. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

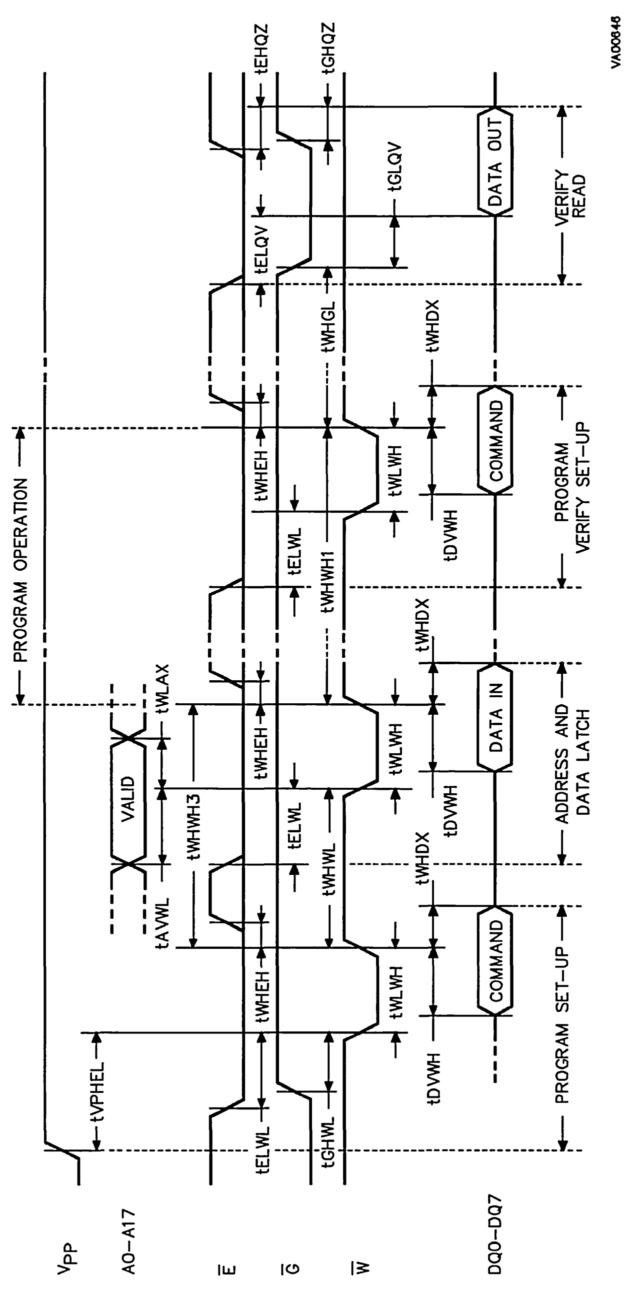

VPP
A0–A17
E
G
W
DQ0–DQ7
PROGRAM OPERATION
tVPHEL
VALID
tAVWL
tWLAX
tWHWH3
tELWL
tWHEH
tELWL
tWHEH
tELWL
tWHEH
tELQV
tEHQZ
tGHWL
tWHWL
tWHWH1
tWHGL
tGHQZ
tWLWH
tWLWH
tWLWH
tGLQV
tDVWH
tWHDX
tDVWH
tWHDX
tDVWH
tWHDX
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
VA00646

Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

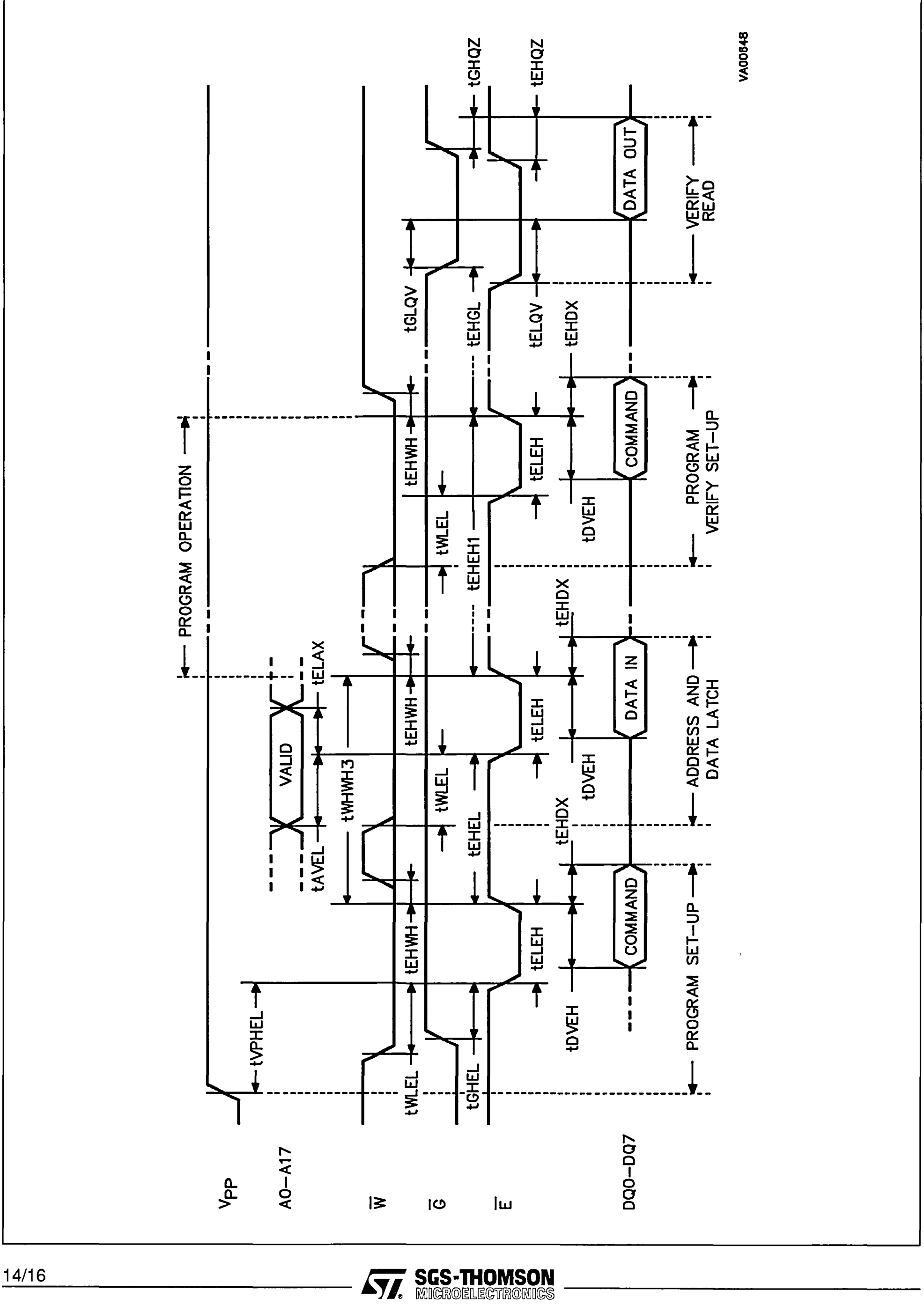

VPP
A0–A17
W
G
E
DQ0–DQ7
PROGRAM OPERATION
tVPHEL
VALID
tAVEL
tELAX
tWHWH3
tWLEL
tEHWH
tWLEL
tEHWH
tEHWH
tWLEL
tGLQV
tGHEL
tEHEL
tEHEH1
tEHGL
tGHQZ
tELEH
tELEH
tELEH
tELQV
tEHQZ
tDVEH
tEHDX
tDVEH
tEHDX
tDVEH
tEHDX
COMMAND
DATA IN
COMMAND
DATA OUT
PROGRAM SET–UP
ADDRESS AND DATA LATCH
PROGRAM VERIFY SET–UP
VERIFY READ
VA00848

Figure 11. Erasing Flowchart

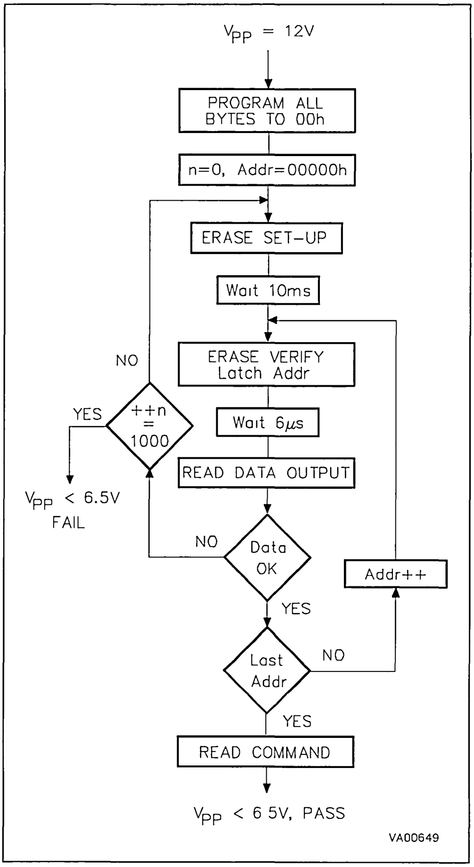
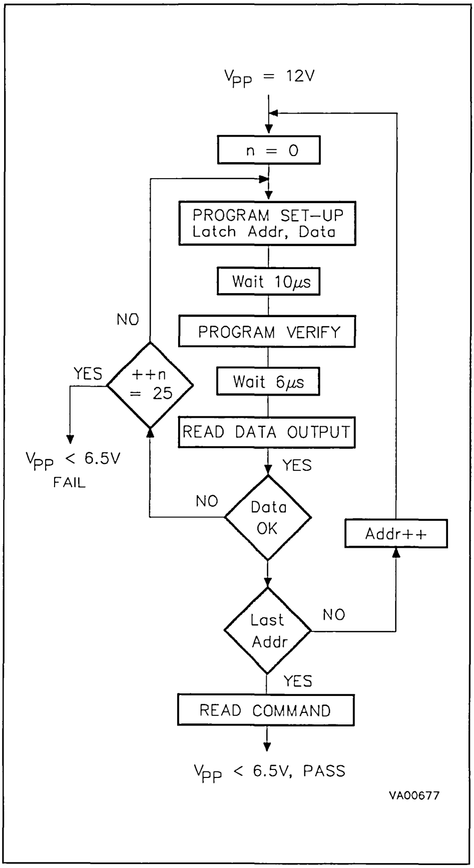

V_{PP} = 12V
PROGRAM ALL BYTES TO 00h
n=0, Addr=00000h
ERASE SET–UP
Wait 10ms
ERASE VERIFY Latch Addr
Wait 6µs
READ DATA OUTPUT
Data OK
NO
YES
++n = 1000
NO
YES
V_{PP} < 6.5V FAIL
Last Addr
NO
YES
Addr++
READ COMMAND
V_{PP} < 6 5V, PASS
VA00649

Figure 12. Programming Flowchart


V_{PP} = 12V
n = 0
PROGRAM SET–UP Latch Addr, Data
Wait 10µs
PROGRAM VERIFY
Wait 6µs
READ DATA OUTPUT
++n = 25
NO
YES
V_{PP} < 6.5V FAIL
Data OK
NO
YES
Addr++
Last Addr
NO
YES
READ COMMAND
V_{PP} < 6.5V, PASS
VA00677

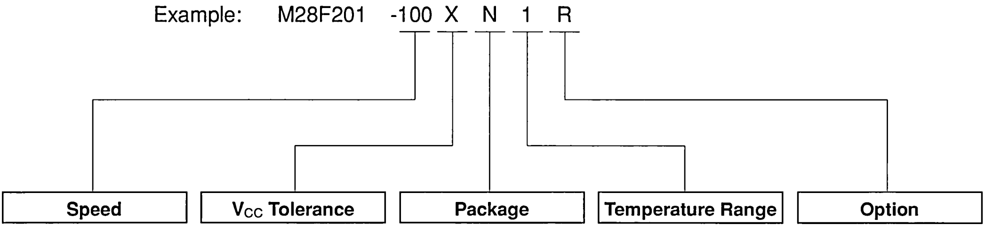
PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION



Example: M28F201 -100 X N 1 R

Speed	
-100	100 ns
-120	120 ns
-150	150 ns
-200	200 ns

V_{CC} Tolerance	
X	± 5%
blank	± 10%

Package	
P	PDIP32
K	PLCC32
N	PTSO32 8 x 20 mm

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option	
R	Reverse Pin-Out

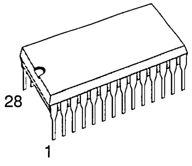
For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

ROM

CMOS 512K (64K x 8) ROM

- FAST ACCESS TIME: 100ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 40mA Max
  - Standby Current 20µA Max
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- STATIC OPERATION
- CHIP ENABLE ACTIVE LEVEL MASK PROGRAMMABLE
- AUTOMATIC POWER DOWN



PDIP28 (B)

DESCRIPTION

The M23C512 is a 512K bit, CMOS Mask Programmed Read Only Memory (ROM), organised as 64K bytes of 8 bits. The fast access time of 100ns makes it ideal for EPROM replacement in high volume applications. The Chip Select input may be mask programmed to be Active Low or High. When Chip Enable is not active the M23C512 enters a standby mode, making it very suitable for battery powered systems. After a memory cycle plus 50ns with no change in inputs, the M23C512 enters automatically the standby mode with the power consumption reduced from 40mA to 1mA Max. Data remains latched on the output.

Two line control may be implemented using the Chip Enable and the Output Enable signals.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$ or E	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

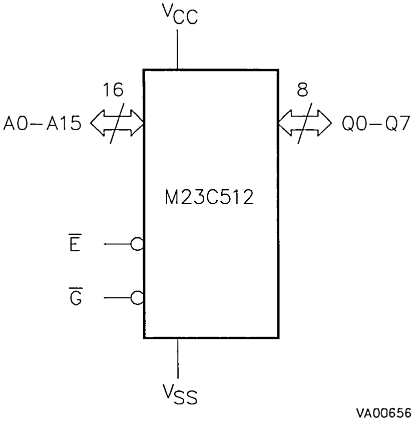


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1	0 to 70	°C
T_{BIAS}	Temperature Under Bias	0 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V

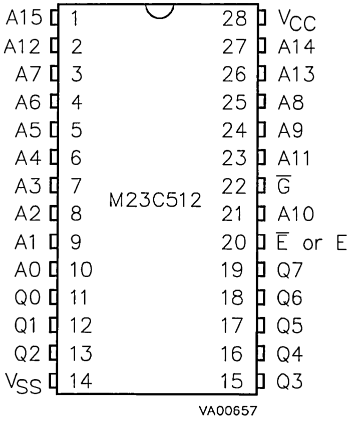
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes

Mode	$\overline{E}$ or E		$\overline{G}$	Q0 - Q7
Read	V_{IL}	V_{IH}	V_{IL}	Data Output
Output Disable	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	V_{IL}	X	Hi-Z

Notes: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections


A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
V_{SS} 14
28 V_{CC}
27 A14
26 A13
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{E}$ or E
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3
M23C512
VA00657

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

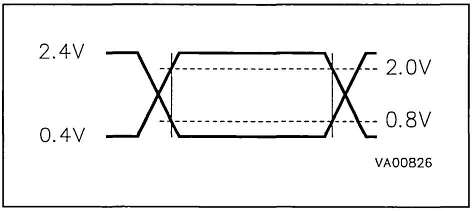


Figure 4. AC Testing Load Circuit

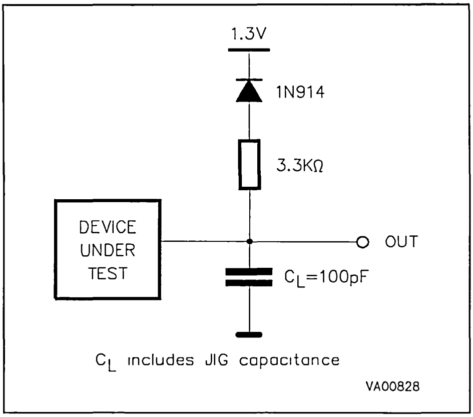


Table 4. Capacitance (T_A = 25 °C; f = 1MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

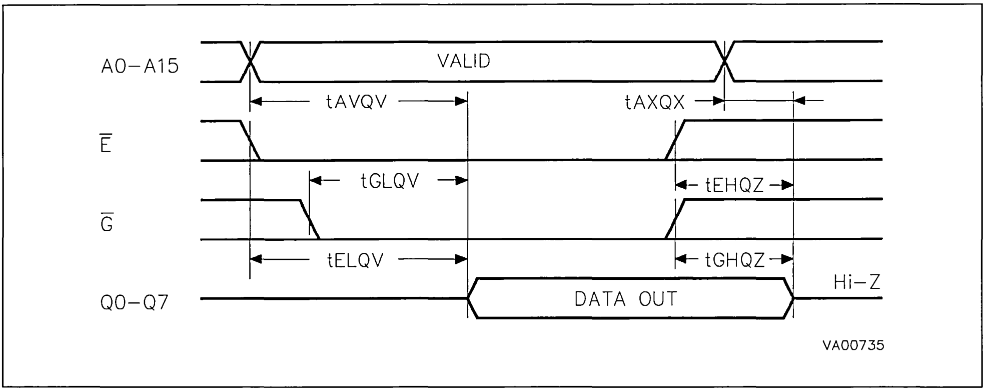
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 10MHz		40	mA
	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz		20	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		20	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

Table 6. Read Mode AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100	ns
t_{AVAV}	t_{CYC}	Address Cycle Time			100	
t_{ELQV} (1)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	10		ns

Notes: 1. Parameter shown for the mask option of Chip Enable Active Low
2. Sampled only not 100% tested

Figure 5. Read Mode AC Waveforms



ORDERING INFORMATION

Example: M23C512 B 1 AA

Package	Temperature Range	Option
B PDIP28	1 0 to 70 °C	AA-ZZ Content Identification

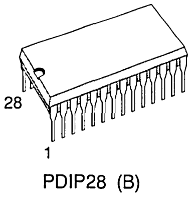
For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M23C1000

CMOS 1 Megabit (128K x 8) ROM

- FAST ACCESS TIME: 100ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 40mA Max
  - Standby Current 20µA Max
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- STATIC OPERATION
- CHIP ENABLE ACTIVE LEVEL MASK PROGRAMMABLE
- AUTOMATIC POWER DOWN



DESCRIPTION

The M23C1000 is a 1 Megabit, CMOS Mask Programmed Read Only Memory (ROM), organised as 128K bytes of 8 bits. The fast access time of 100ns makes it ideal for EPROM replacement in high volume applications. The Chip Select input may be mask programmed to be Active Low or High. When Chip Enable is not active the M23C1000 enters a standby mode, making it very suitable for battery powered systems. After a memory cycle plus 50ns with no change in inputs, the M23C1000 enters automatically the standby mode with the power consumption reduced from 40mA to 1mA Max. Data remains latched on the output.

Figure 1. Logic Diagram

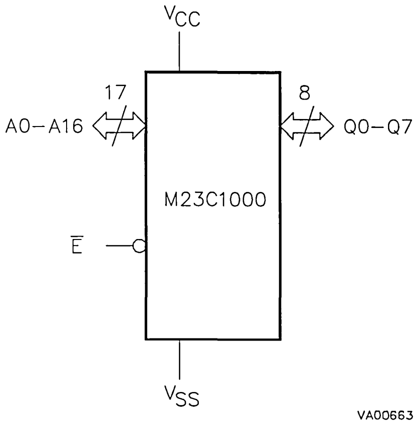


Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$ or E	Chip Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

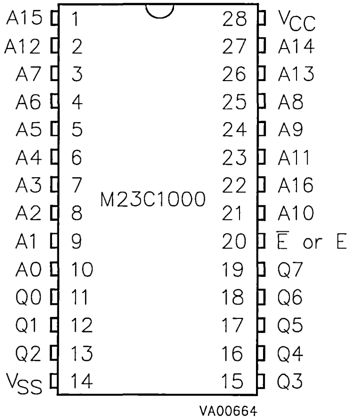
Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1	0 to 70	°C
T_{BIAS}	Temperature Under Bias	0 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes

Mode	$\overline{E}$ or E		Q0 - Q7
Read	V_{IL}	V_{IH}	Data Output
Standby / Output Disable	V_{IH}	V_{IL}	Hi-Z

Figure 2. DIP Pin Connections


A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
V_{SS} 14
28 V_{CC}
27 A14
26 A13
25 A8
24 A9
23 A11
22 A16
21 A10
20 $\overline{E}$ or E
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3
M23C1000
VA00664

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

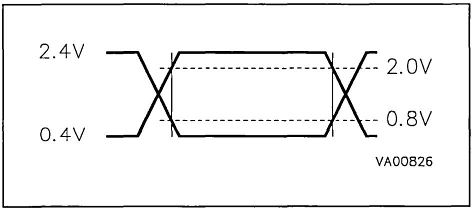


Figure 4. AC Testing Load Circuit

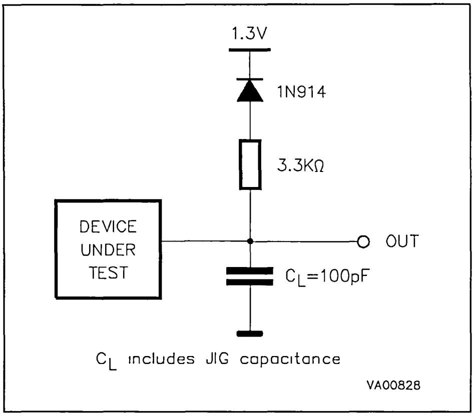


Table 4. Capacitance (TA = 25 °C; f = 1MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 10MHz		40	mA
	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5MHz		20	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		20	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

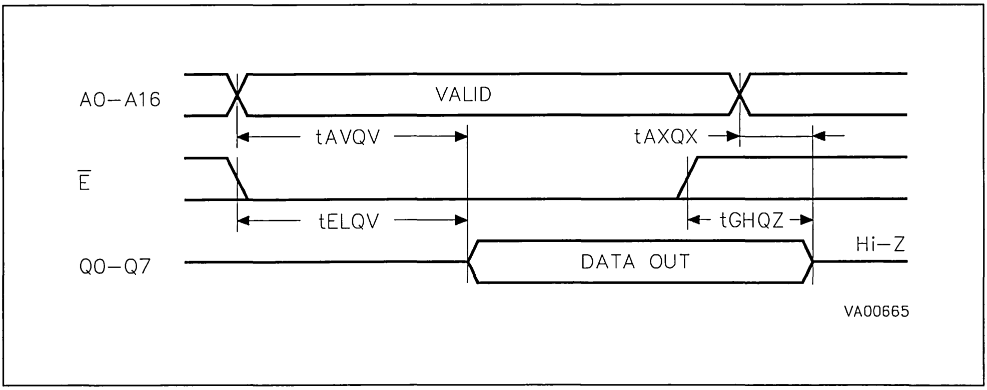
Table 6. Read Mode AC Characteristics

(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

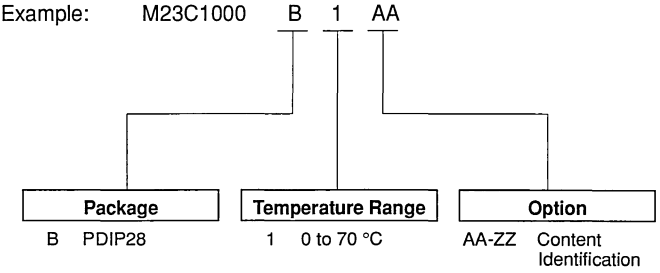
Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$		100	ns
t_{AVAV}	t_{CYC}	.Address Cycle Time			100	
t_{ELQV} (1)	t_{CE}	Chip Enable Low to Output Valid			100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z		0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$	10		ns

Notes: 1. Parameter shown for the mask option of Chip Enable Active Low
2. Sampled only not 100% tested

Figure 5. Read Mode AC Waveforms



ORDERING INFORMATION



Example: M23C1000 B 1 AA

Package	Temperature Range	Option
B PDIP28	1 0 to 70 °C	AA-ZZ Content Identification

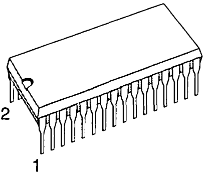
For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M23C1001

CMOS 1 Megabit (128K x 8) ROM

- FAST ACCESS TIME: 100ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 40mA Max
  - Standby Current 20µA Max
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- STATIC OPERATION
- CHIP ENABLE ACTIVE LEVEL MASK PROGRAMMABLE
- AUTOMATIC POWER DOWN



PDIP32 (B)

DESCRIPTION

The M23C1001 is a 1 Megabit, CMOS Mask Programmed Read Only Memory (ROM), organised as 128K bytes of 8 bits. The fast access time of 100ns makes it ideal for EPROM replacement in high volume applications. The Chip Select input may be mask programmed to be Active Low or High. When Chip Enable is not active the M23C1001 enters a standby mode, making it very suitable for battery powered systems. After a memory cycle plus 50ns with no change in inputs, the M23C1001 enters automatically the standby mode with the power consumption reduced from 40mA to 1mA Max. Data remains latched on the output.

Two line control may be implemented using the Chip Enable and the Output Enable signals.

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$ or E	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

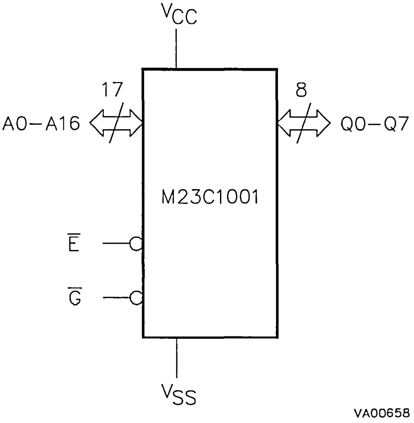


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1	0 to 70	°C
T_{BIAS}	Temperature Under Bias	0 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltages	–0.5 to 7	V
V_{CC}	Supply Voltage	–0.5 to 7	V

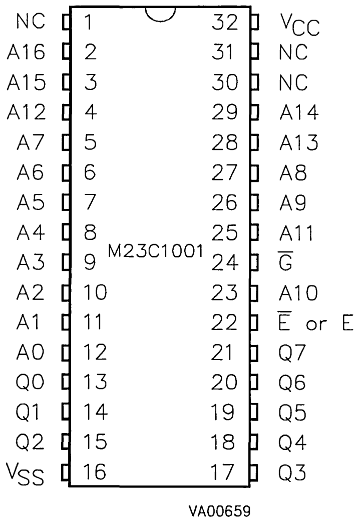
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes

Mode	$\overline{E}$ or E		$\overline{G}$	Q0 - Q7
Read	V_{IL}	V_{IH}	V_{IL}	Data Output
Output Disable	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	V_{IL}	X	Hi-Z

Notes: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections


NC 1
A16 2
A15 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
Q0 13
Q1 14
Q2 15
VSS 16
32 VCC
31 NC
30 NC
29 A14
28 A13
27 A8
26 A9
25 A11
24 G
23 A10
22 E or E
21 Q7
20 Q6
19 Q5
18 Q4
17 Q3
M23C1001
VA00659

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

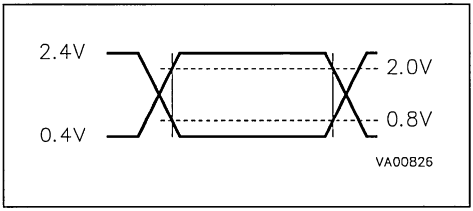


Figure 4. AC Testing Load Circuit

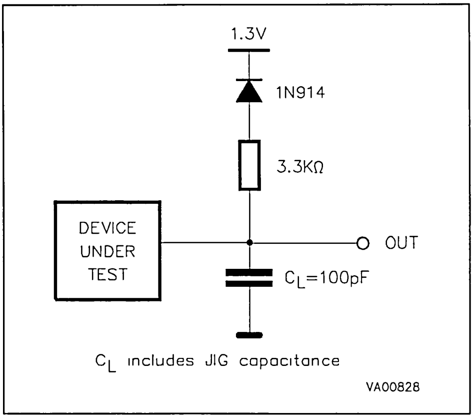


Table 4. Capacitance (T_A = 25 °C; f = 1MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

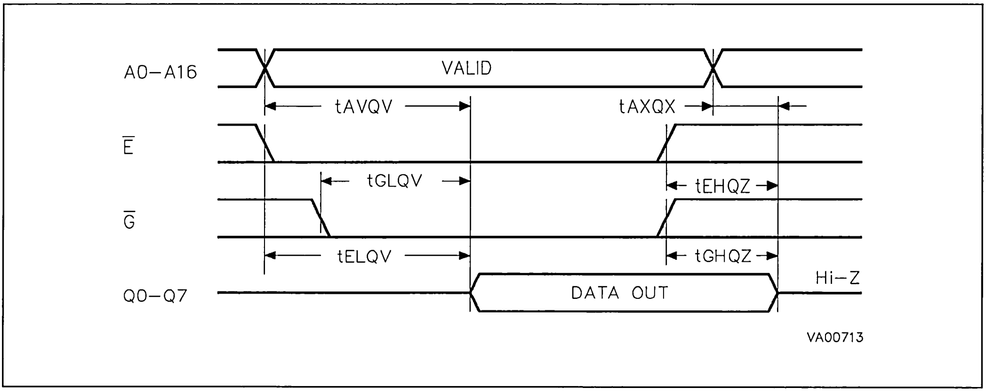
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10MHz		40	mA
	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		20	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		20	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

Table 6. Read Mode AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

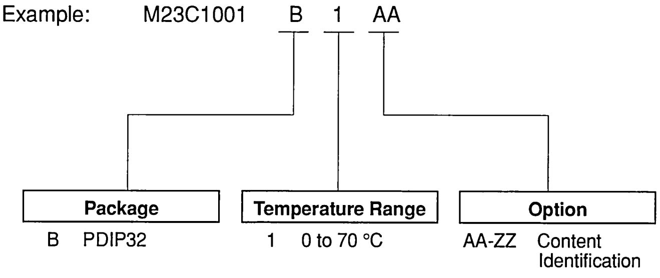
Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100	ns
t_{AVAV}	t_{CYC}	Address Cycle Time			100	
t_{ELQV} (1)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	10		ns

Notes: 1. Parameter shown for the mask option of Chip Enable Active Low
2. Sampled only not 100% tested

Figure 5. Read Mode AC Waveforms



ORDERING INFORMATION



Example: M23C1001 B 1 AA

Package
B PDIP32

Temperature Range
1 0 to 70 °C

Option
AA-ZZ Content Identification

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

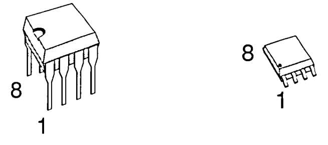
For further information on any aspect of this device, please contact our Sales Office nearest to you.

I^{2}C BUS EEPROM

ST24C01

SERIAL ACCESS CMOS 1K (128 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE, FULLY I^{2}C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



PSDIP8 (B)
0.25mm Frame

PSO8 (M)

DESCRIPTION

The ST24C01 is a 1K bit electrically erasable programmable memory (EEPROM), organised as 128 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^{2}C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST24C01 carries a built-in 4 bit, unique device identification code corresponding to the I^{2}C bus definition. This is used together with a 3 bit chip enable input to form a 7 bit memory select signal. In this way up to 8

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

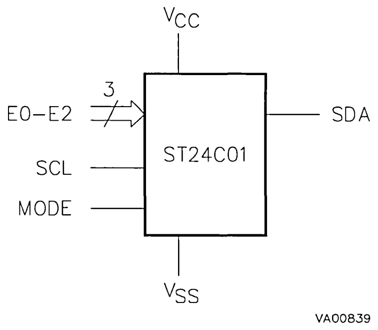


Figure 2A. DIP Pin Connections

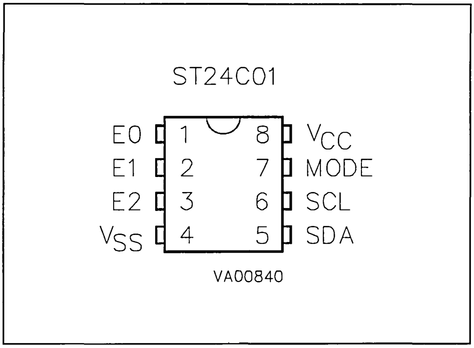


Figure 2B. SO Pin Connections

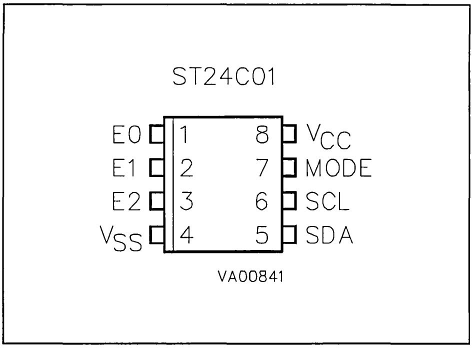


Table 2. Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
TA	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)			4000	V
	Electrostatic Discharge Voltage (Machine model)			1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

ST24C01's may be attached to the I^{2}C bus and selected individually.

The ST24C01 behaves as a slave device in the I^{2}C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 device select bits plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode.

The 8 bits sent after a START condition are made up of 4 bits that identify the device type, 3 chip enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

OPERATING MODES (cont'd)

Byte Write. In this mode a device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 4 or up to 8 bytes respectively may be written in one programing cycle. Multibyte mode is activated when the MODE pin is at V_{IH} level and Page Write when $\overline{MODE}$ is at V_{IL}. A device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes written in the Page Write mode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the $R\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the $R\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the $R\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Table 3. Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: The MSB b7 is sent first

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 128	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

DEVICE OPERATION

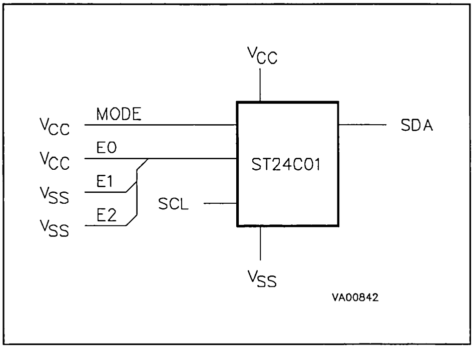
The ST24C01 supports the I^{2}C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24C01 is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

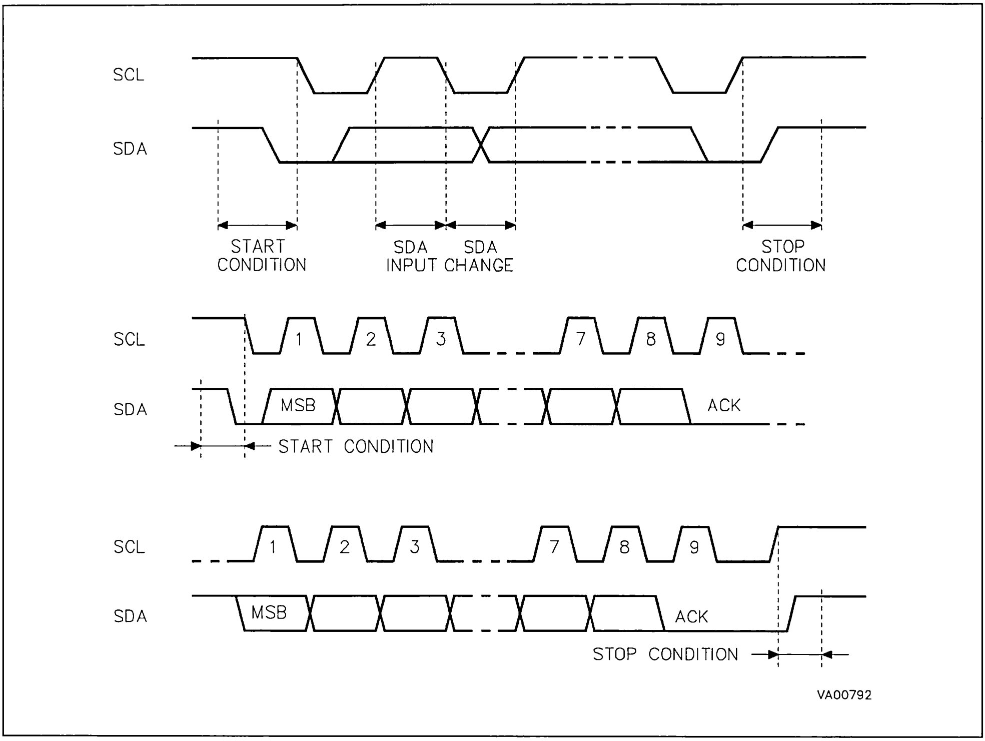
Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24C01 continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 3. Typical Interface


VCC
VCC
MODE
VCC
E0
VSS
E1
VSS
E2
SCL
ST24C01
SDA
VSS
VA00842

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24C01 and the bus master and forces the device into the standby power state.

Figure 4. I^{2}C Bus Protocol


SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 5. AC Testing Input Output Waveforms

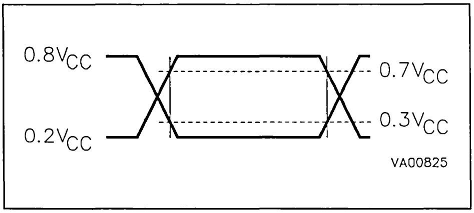

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance [(1)] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested

Figure 6. AC Waveforms

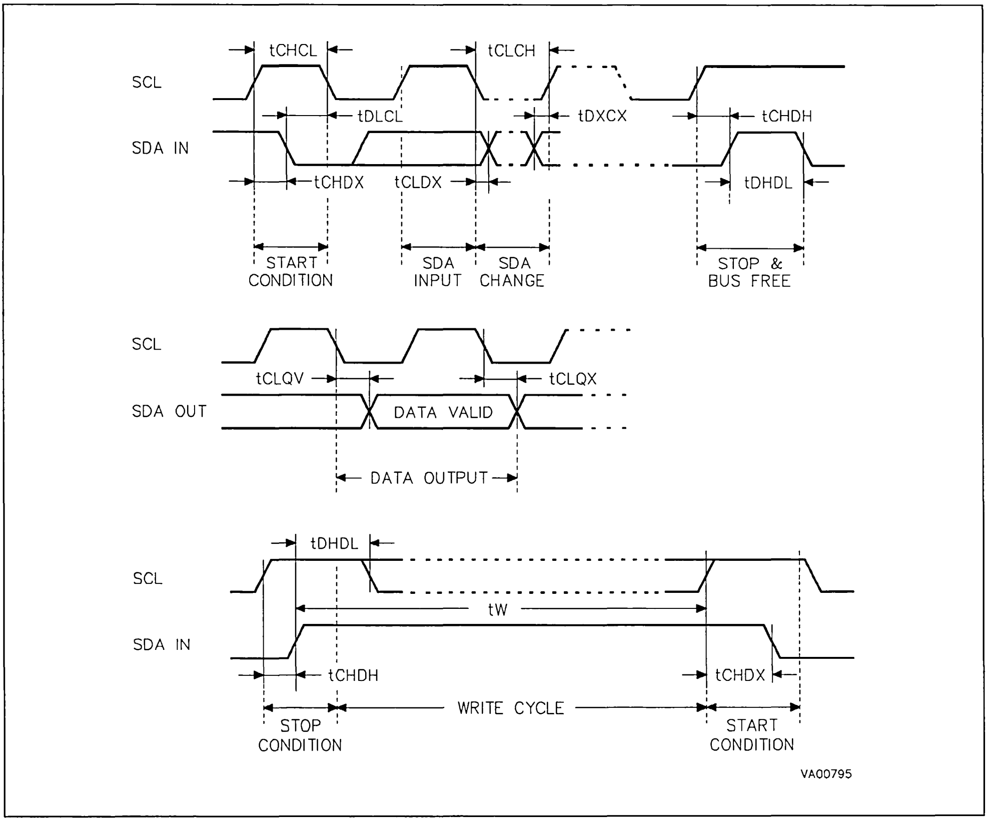

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
STOP CONDITION
WRITE CYCLE
START CONDITION
VA00795

Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	f = 100kHz		2	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = 0V or V_{CC}		100	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0 - E2, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0 - E2, MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

DEVICE OPERATION (cont'd)

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data input. During data input the ST24C01 samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST24C01, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^{2}C bus definition. For the ST24C01 these are fixed as 1010b (0Ah).

The following 3 bits identify the specific ST24C01 on the bus. They are matched to the chip enable signals E0 - E2. Thus up to 8 ST24C01's can be connected on the same bus giving a memory capacity total of 8k bits. After a START condition all ST24C01's on the bus will identify the device code and compare the following 3 bits to the chip enable inputs E0 - E2. If a match is found the corresponding ST24C01 will acknowledge the identification on the SDA bus during the 9th bit time.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST24C01 acknowledges this and waits for a byte address. The byte address of 7 bits (MSB b7 is 'don't care) provides access to any of the 128 bytes of the memory. After receipt of the byte address the ST24C01 again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST24C01. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the ST24C01. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from 1-8 bytes of data, which are each acknowledged by the ST24C01. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24C01 will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Figure 7. Write Modes Sequence

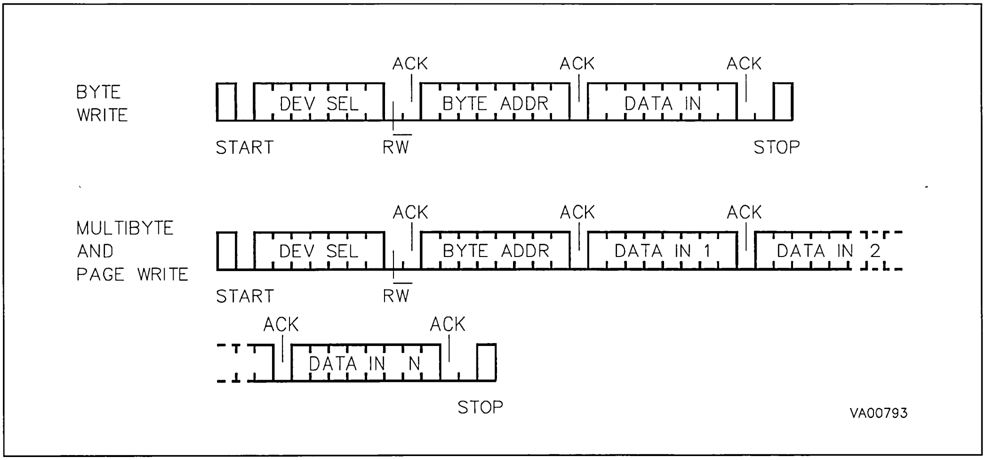
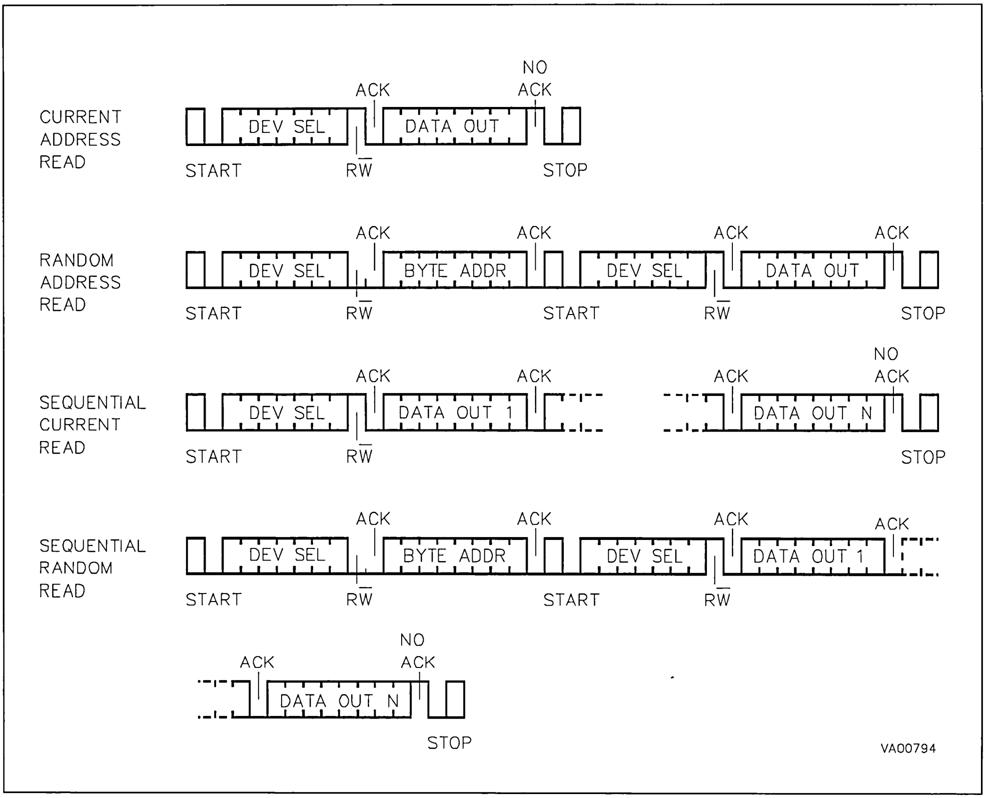

BYTE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN
START
RW
STOP
MULTIBYTE AND PAGE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN 1
DATA IN 2
START
RW
ACK
ACK
DATA IN N
STOP
VA00793

Figure 8. Read Modes Sequence


CURRENT ADDRESS READ
ACK
NO ACK
DEV SEL
DATA OUT
START
RW
STOP
RANDOM ADDRESS READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT
START
RW
START
RW
STOP
SEQUENTIAL CURRENT READ
ACK
ACK
ACK
NO ACK
DEV SEL
DATA OUT 1
DATA OUT N
START
RW
STOP
SEQUENTIAL RANDOM READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT 1
START
RW
START
RW
ACK
NO ACK
DATA OUT N
STOP
VA00794

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST24C01 has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R$\overline{W}$ bit set to '1'. The ST24C01 acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the R$\overline{W}$ bit set to '1'. The ST24C01 acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST24C01 continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 128 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24C01 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24C01 terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

ORDERING INFORMATION

Example: ST24C01 M 1 013TR

Package		Temperature Range		Option	
B	PSDIP8 0.25 mm Frame	1	0 to 70 °C	013TR	Tape & Reel
M	PSO8	3	–40 to 125 °C		
		6	–40 to 85 °C		

Parts are shipped with the memory content set at all "1's" (0FFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

ST24C02A

SERIAL ACCESS CMOS 2K (256 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE, FULLY I^{2}C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL

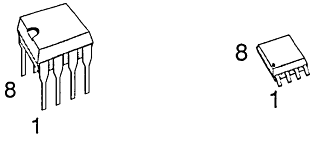
DESCRIPTION

The ST24C02A is a 2K bit electrically erasable programmable memory (EEPROM), organised as 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^{2}C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST24C02A carries a built-in 4 bit, unique device identification code corresponding to the I^{2}C bus definition. This is used together with a 3 bit chip enable input to form a 7 bit memory select signal. In this way up to 8

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground



PSDIP8 (B)
0.25mm Frame

PSO8 (M)

Figure 1. Logic Diagram

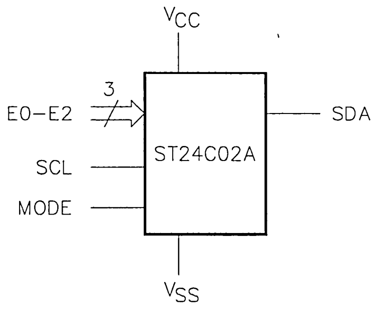


Figure 2A. DIP Pin Connections

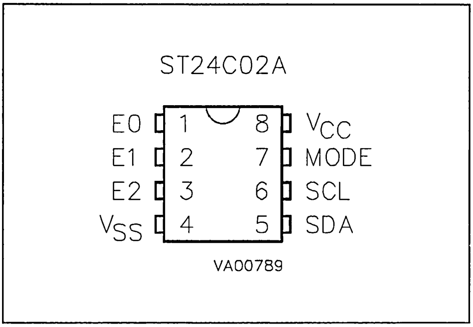


Figure 2B. SO Pin Connections

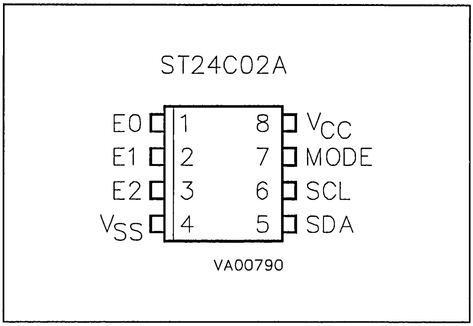


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

ST24C02A's may be attached to the I^{2}C bus and selected individually.

The ST24C02A behaves as a slave device in the I^{2}C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 device select bits plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode.

The 8 bits sent after a START condition are made up of 4 bits that identify the device type, 3 chip enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

OPERATING MODES (cont'd)

Byte Write. In this mode a device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the byte. This is follwed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 4 or up to 8 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when $\overline{MODE}$ is at V_{IL}. A device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes written in the Page Write mode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the $R\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the $R\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the $R\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Table 3. Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 256	As Current or Random Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

DEVICE OPERATION

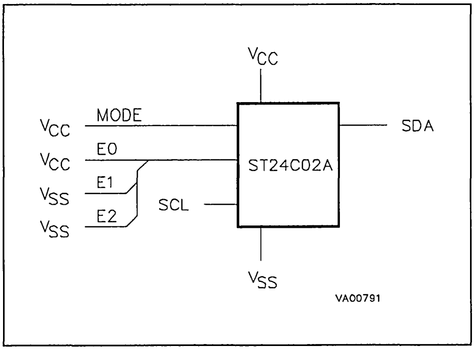
The ST24C02A supports the I^{2}C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24C02A is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24C02A continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

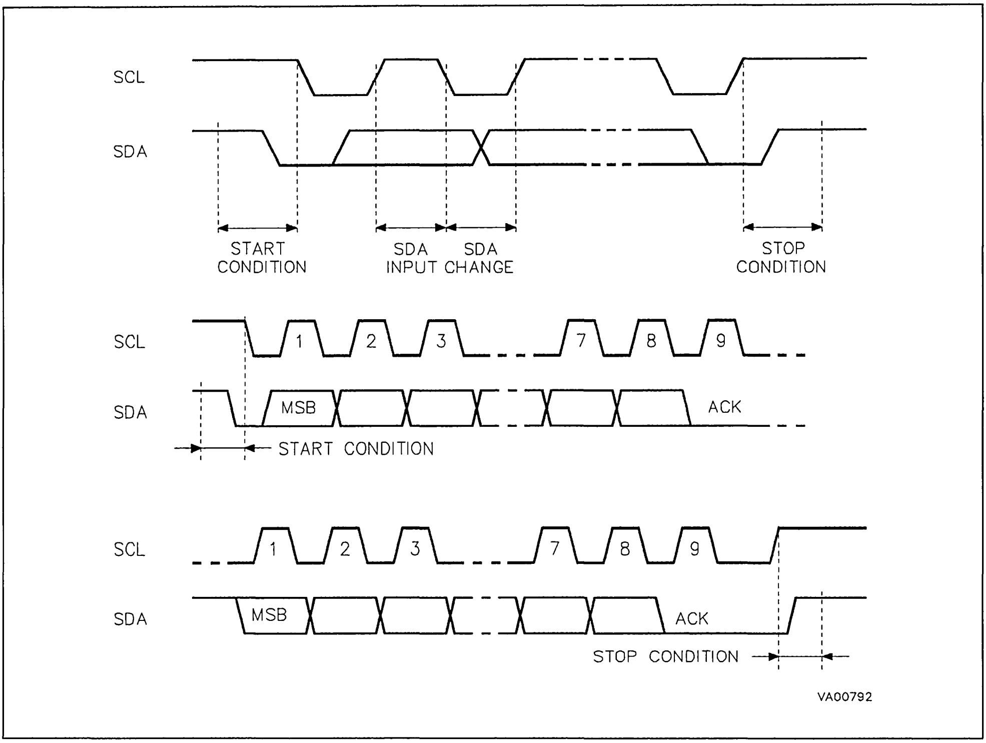
Figure 3. Typical Interface



V_{CC}
V_{CC}
MODE
V_{CC}
E0
V_{SS}
E1
V_{SS}
E2
SCL
ST24C02A
SDA
V_{SS}
VA00791

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24C02A and the bus master and forces the device into the standby power state.

Figure 4. I^{2}C Bus Protocol



SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 5. AC Testing Input Output Waveforms

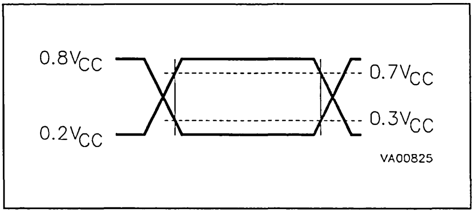

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance [(1)] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested.

Figure 6. AC Waveforms

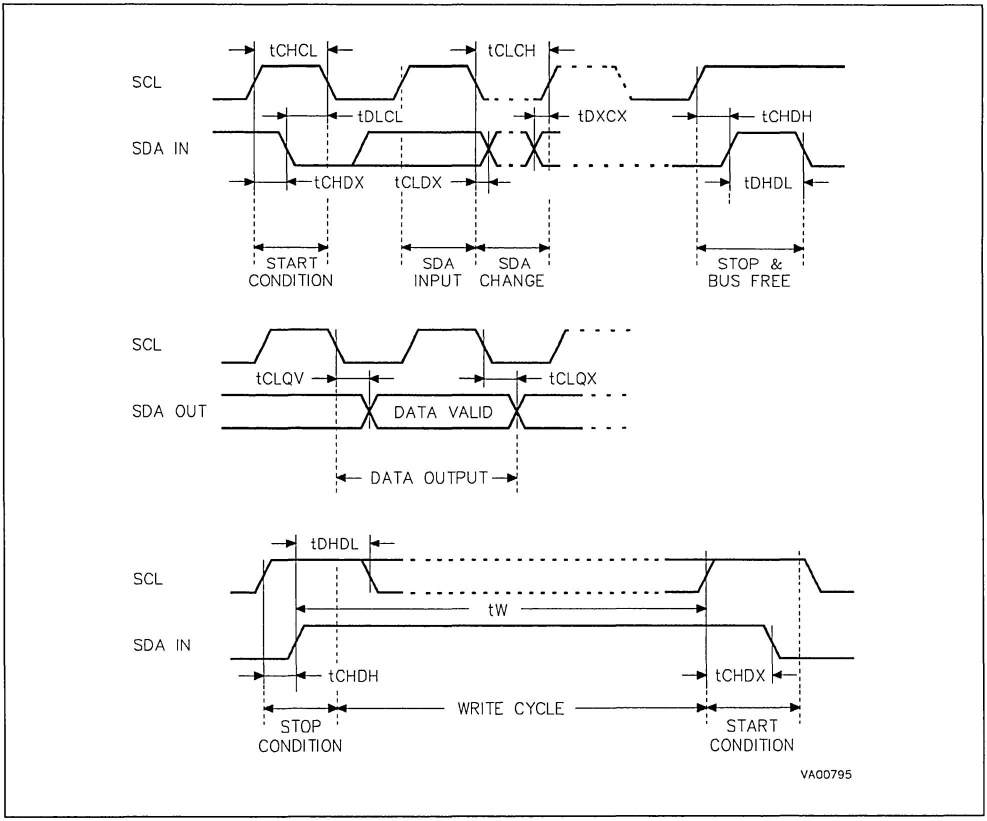

SCL
SDA IN
tCHCL
tCLCH
tDLCL
tDXCX
tCHDH
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
SDA OUT
tCLQV
tCLQX
DATA VALID
DATA OUTPUT
SCL
SDA IN
tDHDL
tW
tCHDH
tCHDX
STOP CONDITION
WRITE CYCLE
START CONDITION
VA00795

Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	f = 100kHz		2	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = 0V or V_{CC}		100	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0 - E2, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0 - E2, MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU.STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD.DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

DEVICE OPERATION (cont'd)

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24C02A samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST24C02A, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For the ST24C02A these are fixed as 1010b (0Ah).

The following 3 bits identify the specific ST24C02A on the bus. They are matched to the chip enable signals E0 - E2. Thus up to 8 ST24C02A's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST24C02A's on the bus will identify the device code and compare the following 3 bits to the chip enable inputs E0 - E2. If a match is found the corresponding ST24C02A will acknowledge the identification on the SDA bus during the 9th bit time.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST24C02A acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes of the memory. After receipt of the byte address the ST24C02A again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST24C02A. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the ST24C02A. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from 1-8 bytes of data, which are each acknowledged by the ST24C02A. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24C02A will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programming time is doubled to a maximum of 20ms.

Figure 7. Write Modes Sequence

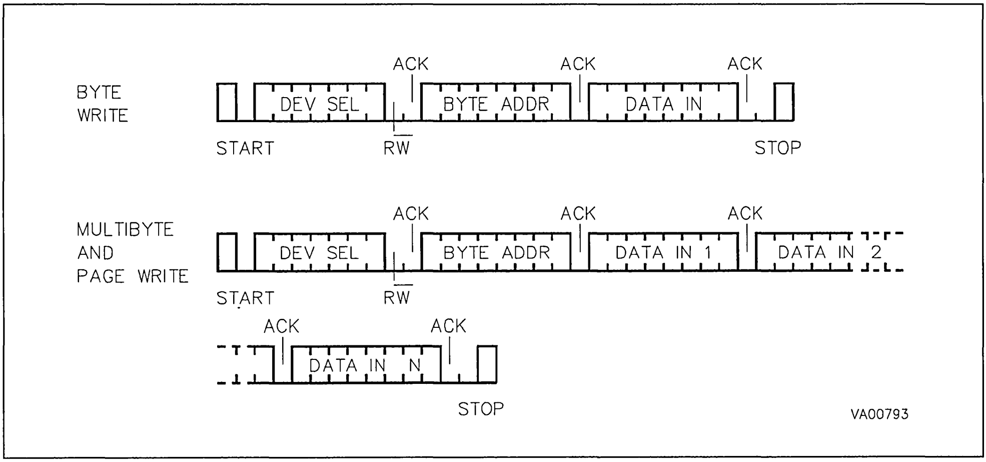
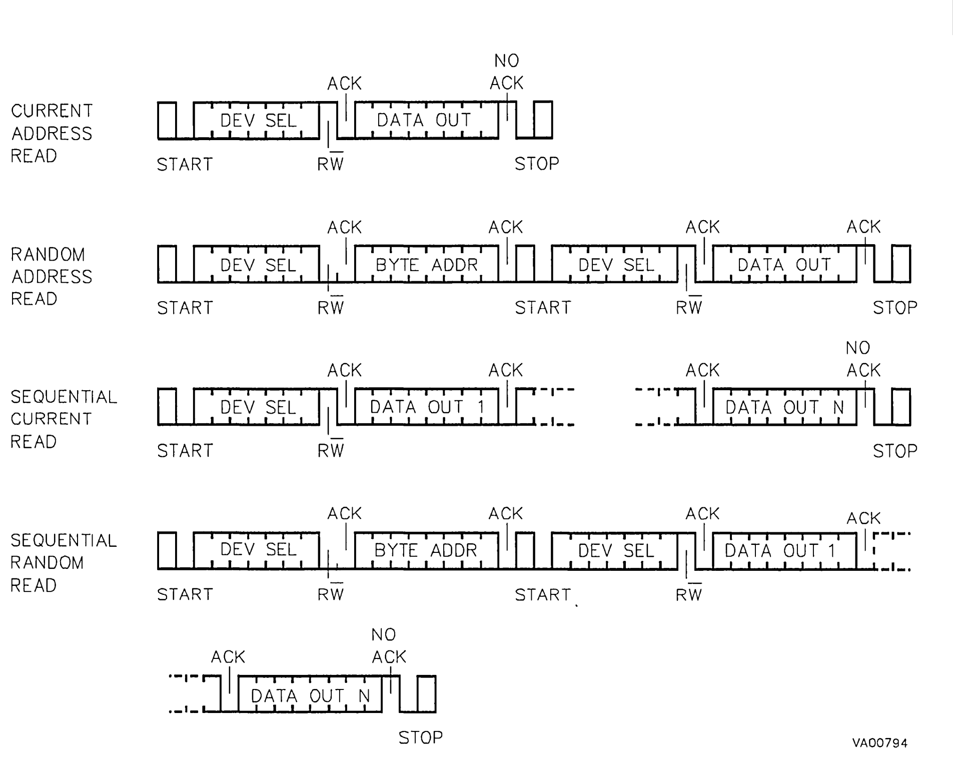

BYTE
WRITE
START
DEV SEL
RW
ACK
BYTE ADDR
ACK
DATA IN
ACK
STOP
MULTIBYTE
AND
PAGE WRITE
START
DEV SEL
RW
ACK
BYTE ADDR
ACK
DATA IN 1
ACK
DATA IN 2
ACK
DATA IN N
ACK
STOP
VA00793

Figure 8. Read Modes Sequence


CURRENT
ADDRESS
READ
START
DEV SEL
RW
ACK
DATA OUT
NO
ACK
STOP
RANDOM
ADDRESS
READ
START
DEV SEL
RW
ACK
BYTE ADDR
ACK
START
DEV SEL
RW
ACK
DATA OUT
ACK
STOP
SEQUENTIAL
CURRENT
READ
START
DEV SEL
RW
ACK
DATA OUT 1
ACK
ACK
DATA OUT N
NO
ACK
STOP
SEQUENTIAL
RANDOM
READ
START
DEV SEL
RW
ACK
BYTE ADDR
ACK
START
DEV SEL
RW
ACK
DATA OUT 1
ACK
ACK
DATA OUT N
NO
ACK
STOP
VA00794

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST24C02A has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\mathrm{R}\overline{\mathrm{W}}$ bit set to '1'. The ST24C02A acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the $\mathrm{R}\overline{\mathrm{W}}$ bit set to '1'. The ST24C02A acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST24C02A continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 256 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24C02A waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24C02A terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

ORDERING INFORMATION

Example: ST24C02A M 1 013TR

Package	
B	PSDIP8 0.25 mm Frame
M	PSO8

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option	
013TR	Tape & Reel

Parts are shipped with the memory content set at all "1's" (0FFh).

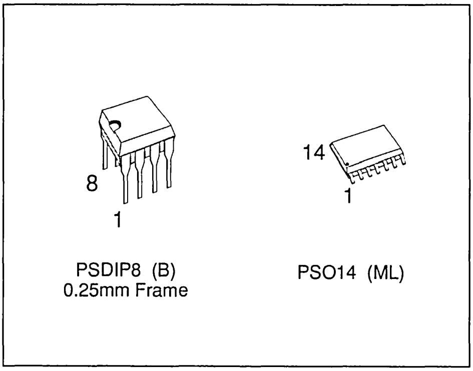
For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

ST24C04

SERIAL ACCESS CMOS 4K (2 by 256 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V POWER SUPPLY
- USER DEFINED WRITE PROTECT AREA
- TWO WIRE SERIAL INTERFACE, FULLY I^{2}C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



DESCRIPTION

The ST24C04 is a 4K bit electrically erasable programmable memory (EEPROM), organised as 2 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^{2}C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST24C04 carries a built-in 4 bit, unique device identification code corresponding to the I^{2}C bus definition. This is used together with a 2 bit chip enable input to form a 6 bit memory select signal. In this way up to 4

Table 1. Signal Names

PRE	Write Protect Enable
E1 - E2	Chip Enable Inputs
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

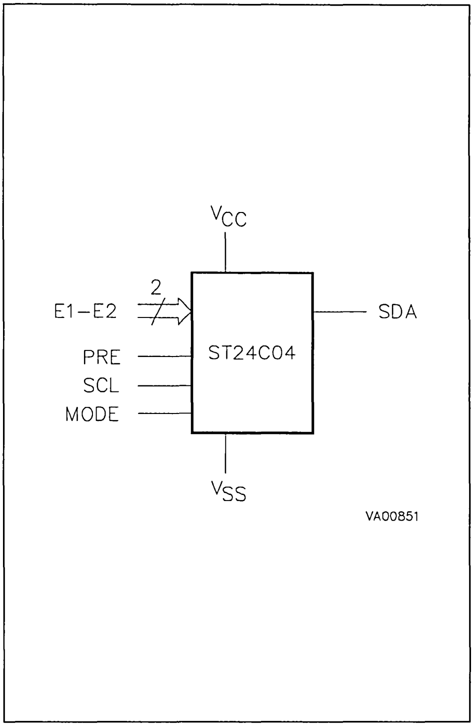


Figure 2A. DIP Pin Connections

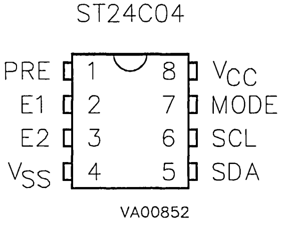
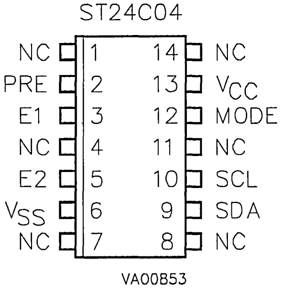


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO14 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

ST24C04's may be attached to the I^{2}C bus and selected individually.

The ST24C04 behaves as a slave device in the I^{2}C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 6 device select bits, one block select bit, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the upper block of the memory may be write protected. The protected area is programmable to start on any 8 byte boundary. Protection is enabled by setting a memory bit flag and the PRE signal input.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode. For the Protect mode

OPERATING MODES (cont'd)

the status of the PRE input determines whether protection is enabled or disabled.

The 8 bits sent after a START condition are made up of a device select of 4 bits that identify the device type, 2 chip enable bits, one block select bit and one bit for a READ (R$\overline{W}$ = 1) or WRITE (R$\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

Byte Write. In this mode a device select is sent with the R$\overline{W}$ bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 4 or up to 8 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when MODE is at V_{IL}. A device select is sent with the R$\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes written in the Page Write mode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the R$\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the R$\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the R$\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

Write Protect. Data in the upper 256 byte block of the memory may be write protected. The protection starts at any 8 byte boundary. The address at which protection starts is defined by the contents of the upper 5 bits (b7- b3 of the top memory location (block 1, byte address 1FFh). Bit 2 of this memory location is used as a flag to indicate that the protection is enabled (b2 = '0') or disabled (b2 = '1'). The lower two bits, b1 & b0, are not used. The sequence to follow to use the memory protect feature is as follows: write the memory contents to be protected into the top of the upper block of the memory, up to location 1FEh. Then establish the memory protect area and set the protection by writing the correct contents into location 1FFh. The area will now be protected when the PRE signal is active (High).

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	R$\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	A8	R$\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	R$\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, R$\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 512	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, R$\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, R$\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

Figure 3. Memory Protection

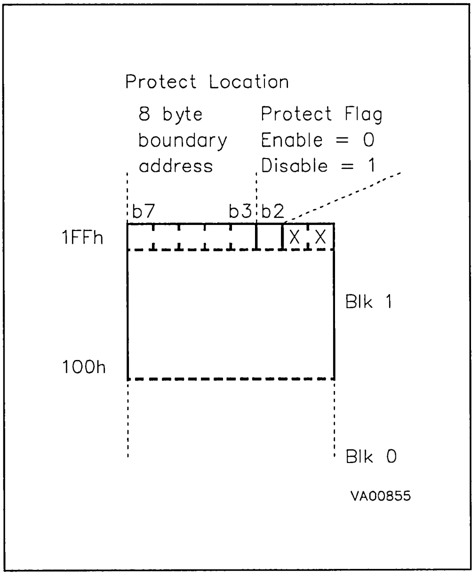

Protect Location
8 byte boundary address
Protect Flag
Enable = 0
Disable = 1
b7
b3
b2
X
X
1FFh
100h
Blk 1
Blk 0
VA00855

Figure 4. Typical Interface

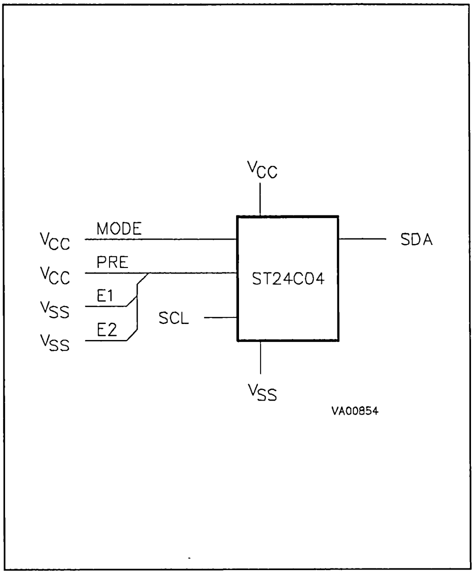
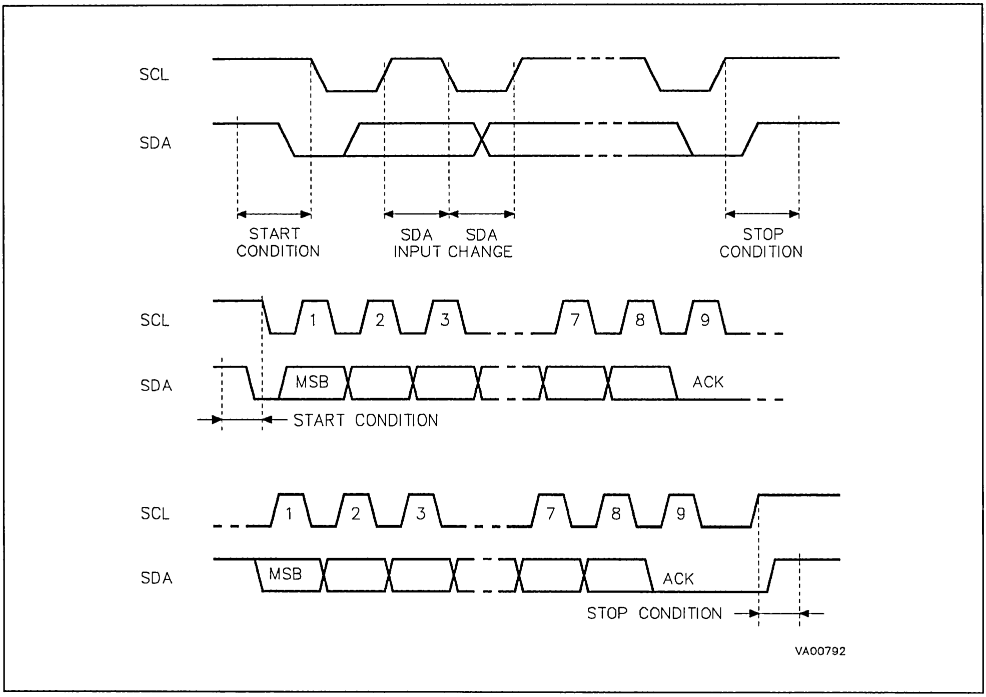

VCC
MODE
VCC
PRE
VCC
E1
VSS
E2
VSS
SCL
ST24C04
SDA
VSS
VA00854

Figure 5. I^{2}C Bus Protocol


SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 6. AC Testing Input Output Waveforms

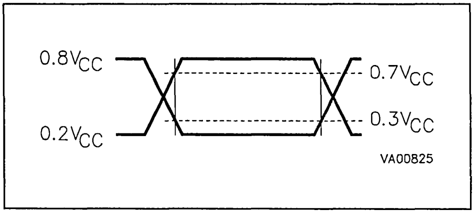

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance [1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested

Figure 7. AC Waveforms

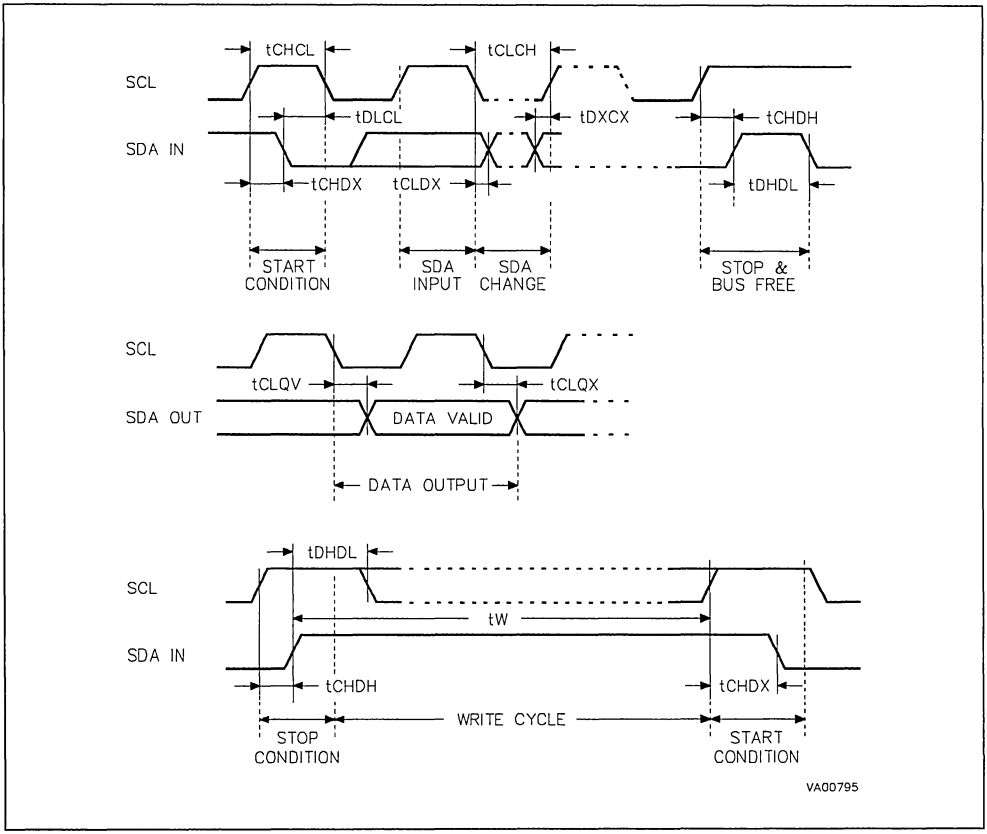

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
STOP CONDITION
WRITE CYCLE
START CONDITION
VA00795

Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	f = 100kHz		2	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = 0V or V_{CC}		100	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E1 - E2, PRE, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E1 - E2, PRE, MODE)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

OPERATING MODE (cont'd)

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input High). If the Multibyte write of up to 4 bytes starts at the location just before the protected area then it is able to write over the first 3 bytes in the protected area. The true area protected is therefore smaller and equal to the content of defined in the location 1FFh plus 3 bytes. This does not apply to the Page write mode as the address counter rolls over and thus cannot go above the 8 byte lower boundary of the protected area.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E1 - E2). These chip enable inputs are used to set the 2 least significant bits of the 6 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Protect Enable (PRE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

DEVICE OPERATION

The ST24C04 supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24C04 is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24C04 continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24C04 and the bus master and forces the device into the standby power state.

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24C04 samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST24C04, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code, block select bit and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^{2}C bus definition. For the ST24C04 these are fixed as 1010b (0Ah).

The following 2 bits identify the specific ST24C04 on the bus. They are matched to the chip enable signals E1 - E2. Thus up to 4 ST24C04's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST24C04's on the bus will identify the device code and compare the following 2 bits to the chip enable inputs E1 - E2. If a match is found the corresponding ST24C04 will acknowledge the identification on the SDA bus during the 9th bit time.

The 7th bit sent selects one of the two blocks of 256 bytes of the memory, effectively acting as memory address A8 (A7 - A0 byte addresses are sent later).

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST24C04 acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes in the selected block of the memory. After receipt of the byte address the ST24C04 again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST24C04. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the ST24C04. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A8-A4) are the same. The master sends from 1-8 bytes of data, which are each acknowledged by the ST24C04. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24C04 will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST24C04 has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $R\overline{W}$ bit set to '1'. The ST24C04 acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the $R\overline{W}$ bit set to '1'. The ST24C04 acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Figure 8. Write Modes Sequence

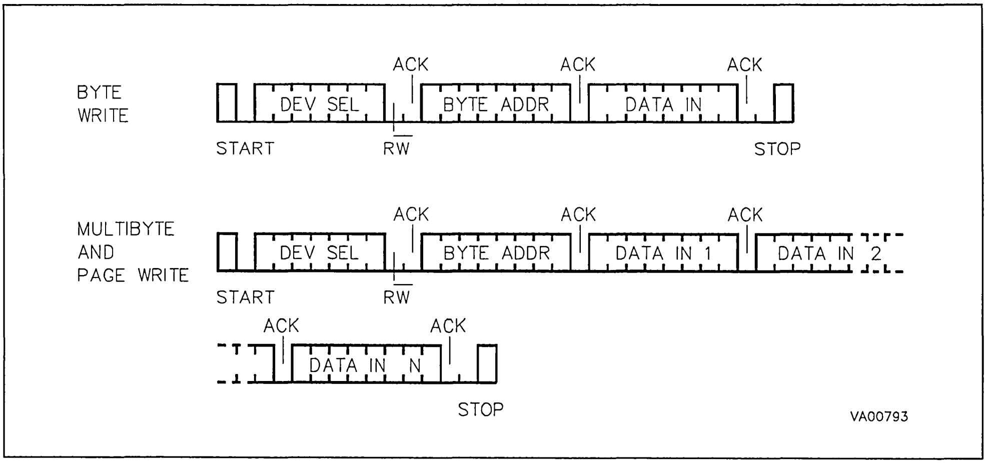
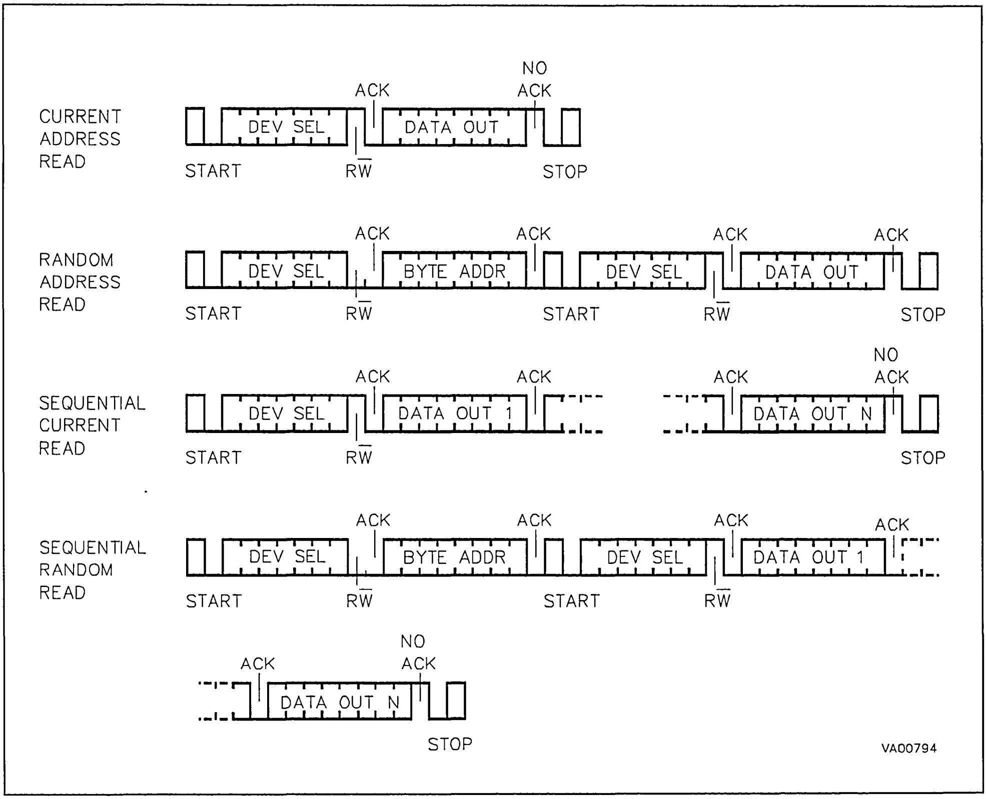

BYTE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN
START
RW
STOP
MULTIBYTE AND PAGE WRITE
DEV SEL
BYTE ADDR
DATA IN 1
DATA IN 2
DATA IN N
VA00793

Figure 9. Read Modes Sequence

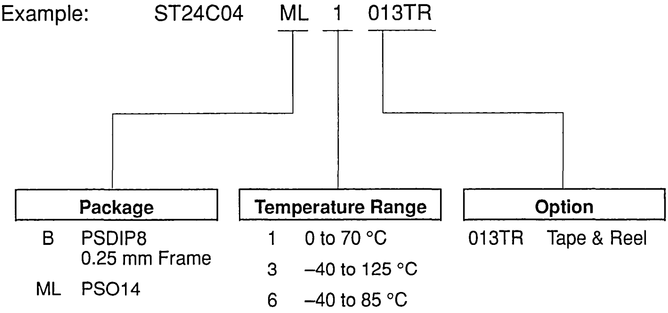

CURRENT ADDRESS READ
RANDOM ADDRESS READ
SEQUENTIAL CURRENT READ
SEQUENTIAL RANDOM READ
ACK
NO ACK
DEV SEL
BYTE ADDR
DATA OUT
DATA OUT 1
DATA OUT N
START
RW
STOP
VA00794

DEVICE OPERATION (cont'd)

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST24C04 continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 512 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24C04 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24C04 terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

ORDERING INFORMATION



Example: ST24C04 ML 1 013TR

Package	
B	PSDIP8 0.25 mm Frame
ML	PSO14

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option	
013TR	Tape & Reel

Parts are shipped with the memory content set at all "1's" (0FFh).

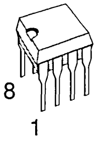
For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

ST24C08

SERIAL ACCESS CMOS 8K (4 by 256 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V POWER SUPPLY
- USER DEFINED WRITE PROTECT AREA
- TWO WIRE SERIAL INTERFACE, FULLY I^{2}C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 8 BYTES)
- PAGE WRITE (UP TO 16 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



PSDIP8 (B)
0.25mm Frame

DESCRIPTION

The ST24C08 is an 8K bit electrically erasable programmable memory (EEPROM), organised as 4 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^{2}C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST24C08 carries a built-in 4 bit, unique device identification code corresponding to the I^{2}C bus definition. This is used together with a chip enable input to form a 5 bit memory select signal. In this way up to 2

Table 1. Signal Names

PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

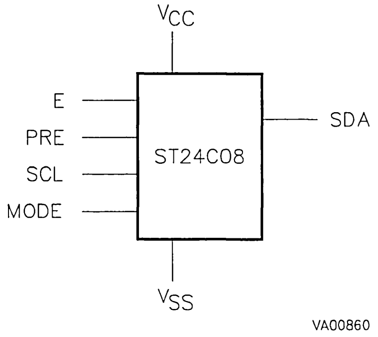
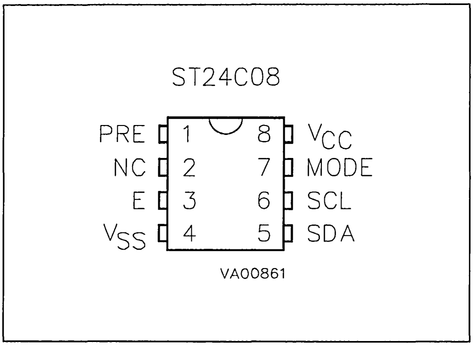


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSDIP8 package) 10 sec	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

ST24C08's may be attached to the I^{2}C bus and selected individually.

The ST24C08 behaves as a slave device in the I^{2}C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 5 device select bits, 2 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the upper block of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. Protection is enabled by setting a memory bit flag and the PRE signal input.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode. For the Protect mode the status of the PRE input determines whether protection is enabled or disabled.

The 8 bits sent after a START condition are made up of a device select of 4 bits that identify the device type, a chip enable bit, 2 block select bits and one bit for a READ ($\overline{RW}$ = 1) or WRITE ($\overline{RW}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

Byte Write. In this mode a device select is sent with the $\overline{RW}$ bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 8 or up to 16 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when MODE is at V_{IL}. A device select is sent with the $\overline{RW}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes in the Page Write mode must have the same five upper address bits.

OPERATING MODES (cont'd)

Current Address Read. In this mode the device select is sent with the $R\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the $R\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the $R\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

Write Protect. Data in the upper 256 byte block of the memory may be write protected. The protection starts at any 16 byte boundary. The address at which protection starts is defined by the contents of the upper 4 bits (b7- b4) of the top memory location (block 3, byte address 3FFh). Bit 3 of this memory location is always '0' and bit 2 is used as a flag to indicate that the protection is enabled (b2 = '0') or disabled (b2 = '1'). The lower two bits, b1 & b0, are not used. The sequence to follow to use the memory protect feature is as follows: write the memory contents to be protected into the top of the upper block of the memory, up to location 3FEh. Then establish the memory protect area and set the protection by writing the correct contents into location 3FFh. The area will now be protected when the PRE signal is active (High).

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input High). If the Multibyte write of up to 8 bytes starts at the location just before the protected area then it is able to write over the first 7 bytes in the protected area. The true area protected is therefore smaller and equal to the content of defined in the location 3FFh plus 7 bytes. This does not apply to the Page write mode as the address counter rolls over and thus cannot go above the 16 byte lower boundary of the protected area.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E	A9	A8	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 1024	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	8	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, $R\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

Figure 3. Memory Protection

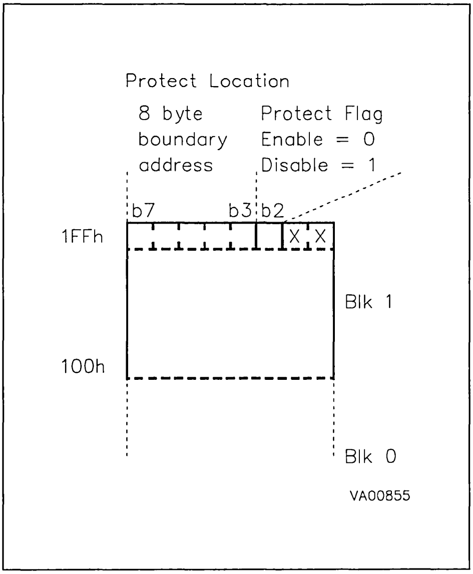

Protect Location
8 byte boundary address
Protect Flag
Enable = 0
Disable = 1
b7
b3
b2
X
X
1FFh
Blk 1
100h
Blk 0
VA00855

Figure 4. Typical Interface

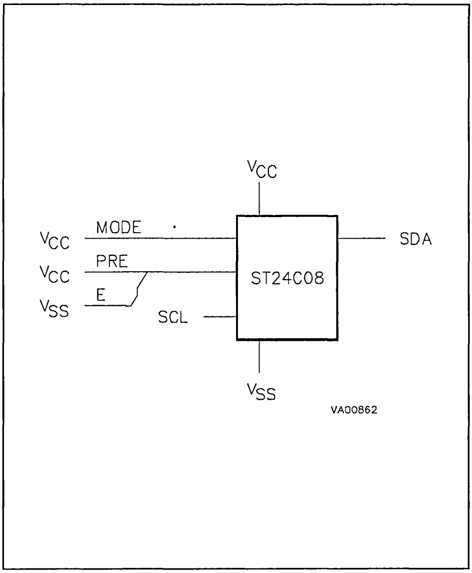
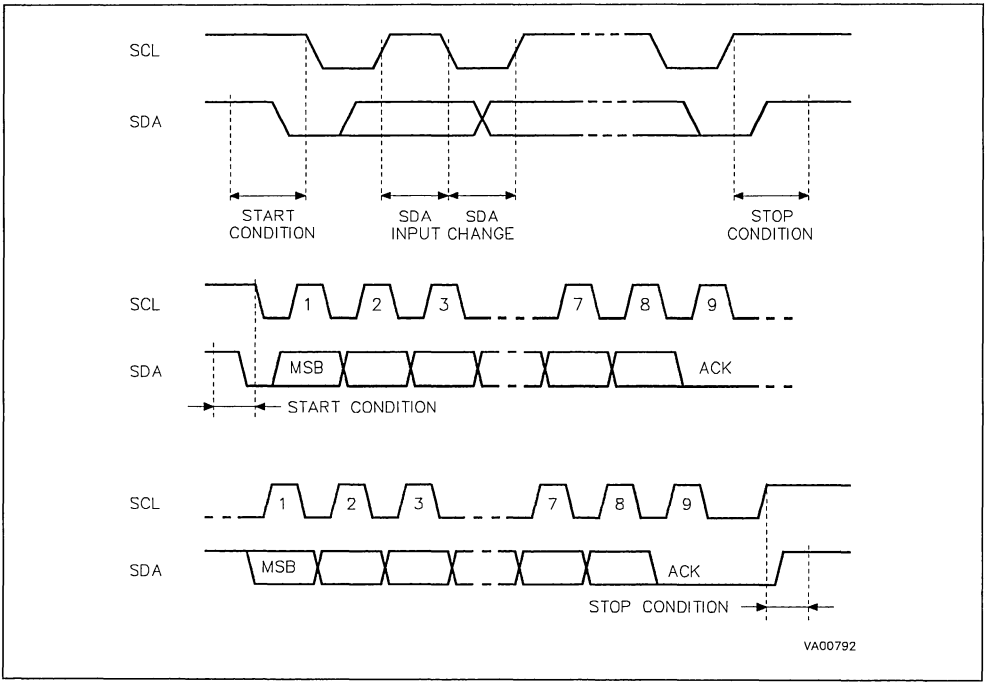

VCC
VCC
MODE
VCC
PRE
VSS
E
SCL
ST24C08
SDA
VSS
VA00862

Figure 5. I²C Bus Protocol


SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

SGS-THOMSON MICROELECTRONICS

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 6. AC Testing Input Output Waveforms

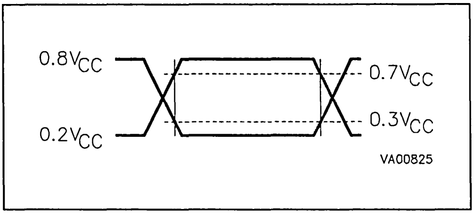

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance [1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested

Figure 7. AC Waveforms

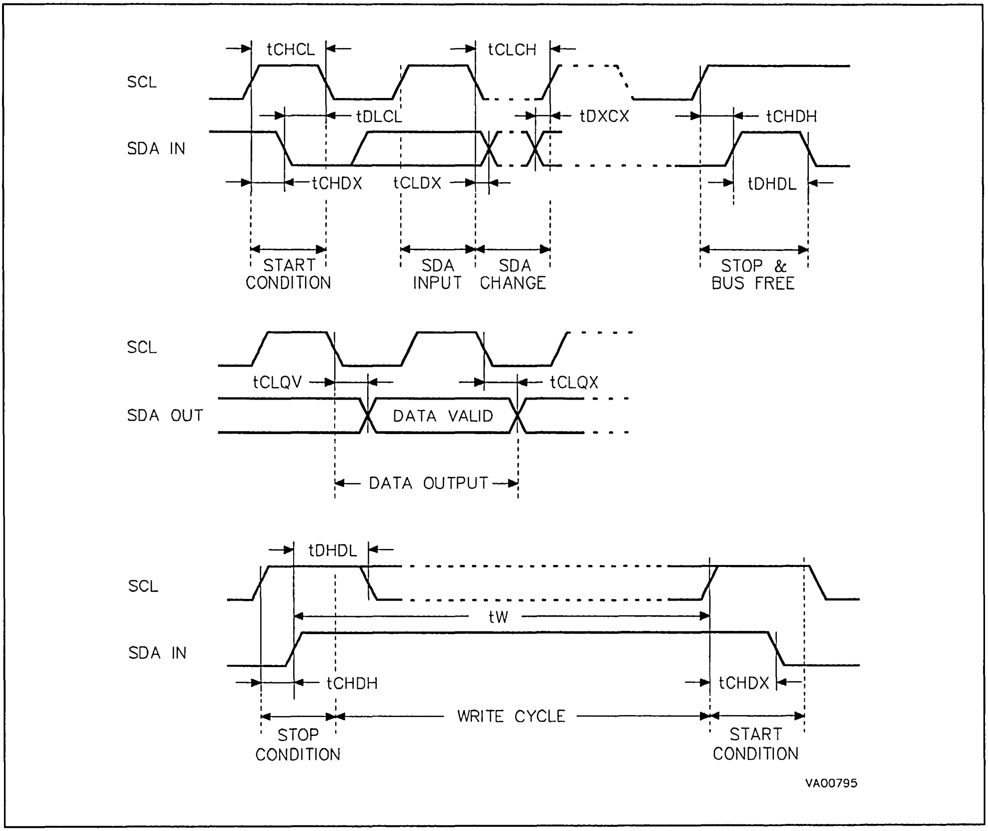

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
STOP CONDITION
WRITE CYCLE
START CONDITION
VA00795

Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	f = 100kHz		2	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = 0V or V_{CC}		100	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E, PRE, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E, PRE, MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

SIGNAL DESCRIPTION (cont'd)

Chip Enable (E). This chip enable input is used to set the least significant bit of the 5 bit device select code. It may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Protect Enable (PRE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

DEVICE OPERATION

The ST24C08 supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24C08 is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24C08 continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24C08 and the bus master and forces the device into the standby power state.

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24C08 samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST24C08, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code, block select bits and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For the ST24C08 these are fixed as 1010b (0Ah).

The following bit identifies the specific ST24C08 on the bus. It is matched to the chip enable signal E. Thus up to 2 ST24C08's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST24C08's on the bus will identify the device code and compare the following bit to the chip enable inputs E. If a match is found the corresponding ST24C08 will acknowledge the identification on the SDA bus during the 9th bit time.

The 6th and 7th bits sent select one of the four blocks of 256 bytes of the memory, effectively acting as memory addresses A9 and A8 (A7 - A0 byte addresses are sent later).

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

DEVICE OPERATION (cont'd)

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST24C08 acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes in the selected block of the memory. After receipt of the byte address the ST24C08 again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST24C08. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the ST24C08. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A9-A5) are the same. The master sends from 1-16 bytes of data, which are each acknowledged by the ST24C08. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24C08 will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST24C08 has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $R\overline{W}$ bit set to '1'. The ST24C08 acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the $R\overline{W}$ bit set to '1'. The ST24C08 acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST24C08 continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 1024 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24C08 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24C08 terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

Figure 8. Write Modes Sequence

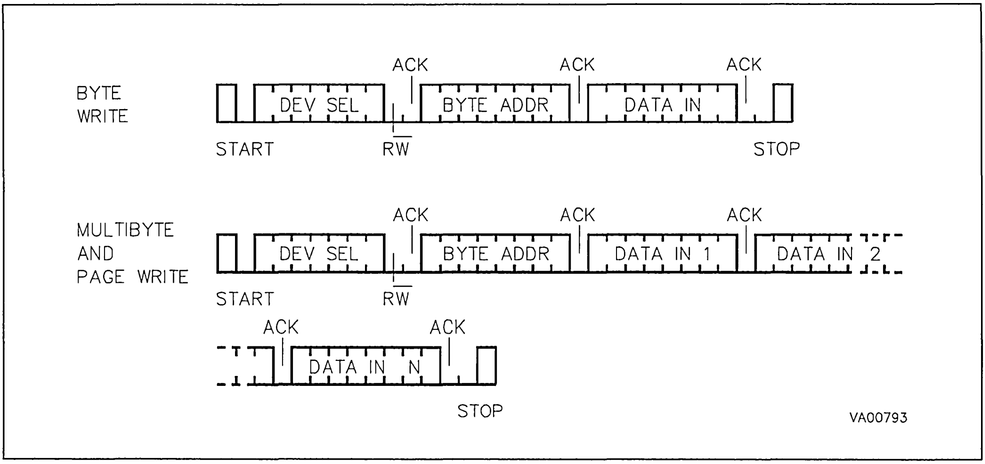
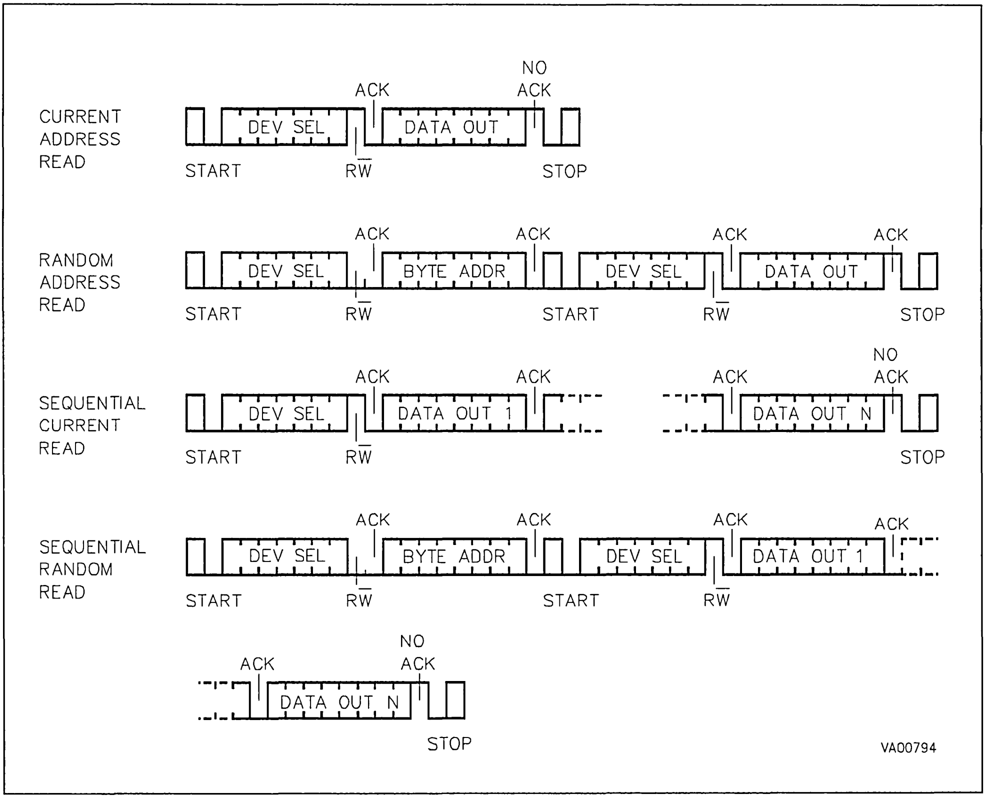

BYTE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN
START
RW
STOP
MULTIBYTE AND PAGE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN 1
DATA IN 2
START
RW
ACK
ACK
DATA IN N
STOP
VA00793

Figure 9. Read Modes Sequence


CURRENT ADDRESS READ
ACK
NO ACK
DEV SEL
DATA OUT
START
RW
STOP
RANDOM ADDRESS READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT
START
RW
START
RW
STOP
SEQUENTIAL CURRENT READ
ACK
ACK
ACK
NO ACK
DEV SEL
DATA OUT 1
DATA OUT N
START
RW
STOP
SEQUENTIAL RANDOM READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT 1
START
RW
START
RW
ACK
NO ACK
DATA OUT N
STOP
VA00794

ORDERING INFORMATION

Example: ST24C08 B 1

Package	
B	PSDIP8 0.25 mm Frame

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Parts are shipped with the memory content set at all "1's" (0FFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

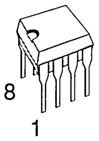
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

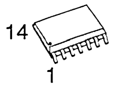
ST24C16C

SERIAL ACCESS CMOS 16K (8 by 256 x 8) EEPROM

- 100,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 4.5V TO 5.5V POWER SUPPLY
- USER DEFINED WRITE PROTECT AREA
- TWO WIRE SERIAL INTERFACE, FULLY I^{2}C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 8 BYTES)
- PAGE WRITE (UP TO 16 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



PSDIP8 (B)
0.25mm Frame



PSO14 (ML)

DESCRIPTION

The ST24C16C is a 16K bit electrically erasable programmable memory (EEPROM), organised as 8 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one hundred thousand erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^{2}C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST24C16C carries a built-in 4 bit, unique device identification code corresponding to the I^{2}C bus definition.

Table 1. Signal Names

PRE	Write Protect Enable
PB0 - PB1	Protect Start Block Select
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

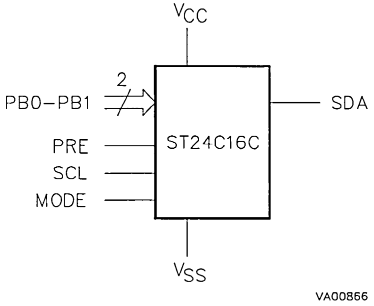


Figure 2A. DIP Pin Connections

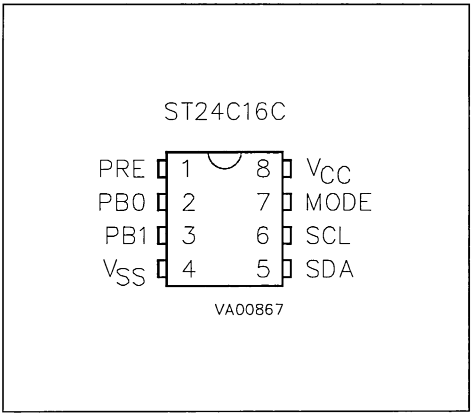
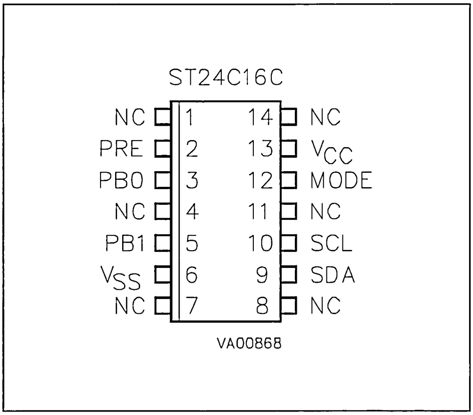


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO14 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

The ST24C16C behaves as a slave device in the I^{2}C protocol with all memory operations synchronised by the serial clock.

Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 device select bits, 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the upper 4 blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the inputs PB0-PB1. Protection is enabled by setting a memory bit flag and the PRE signal input.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode. For the Protect mode the status of the PRE input determines whether protection is enabled or disabled.

The 8 bits sent after a START condition are made up of a device select of 4 bits that identify the device type, 3 block select bits and one bit for a READ (R$\overline{\text{W}}$ = 1) or WRITE (R$\overline{\text{W}}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

Byte Write. In this mode a device select is sent with the R$\overline{\text{W}}$ bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 8 or up to 16 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when MODE is at V_{IL}. A device select is sent with the R$\overline{\text{W}}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes in the Page Writemode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the R$\overline{\text{W}}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the R$\overline{\text{W}}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the R$\overline{\text{W}}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

Write Protect. Data in the upper 4 x 256 byte blocks of the memory may be write protected. The protection starts at any 16 byte boundary. The block containing the address at which protection starts is defined by the PB0- PB1 inputs ('00b' is block 4, '11b' is block 7). The address within this block is the contents of the upper 4 bits (b7-b4) of the top memory location (block 7, byte address 7FFh). Bit 3 of this memory location is always '0' and bit 2 is used as a flag to indicate that the protection is enabled (b2 = '0') or disabled (b2 = '1'). The lower two bits, b1 & b0, are not used. The sequence to follow to use the memory protect feature is as follows: write the memory contents to be protected

Table 3. Device Select Code

	Device Code				Block Select			R$\overline{\text{W}}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	A10	A9	A8	R$\overline{\text{W}}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	R$\overline{\text{W}}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R$\overline{\text{W}}$ = '1'
Random Address Read	'0'	X		START, Device Select, R$\overline{\text{W}}$ = '0', Address
	'1'	X	1	reSTART, Device Select, R$\overline{\text{W}}$ = '1'
Sequential Read	'1'	X	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{\text{W}}$ = '0'
Multibyte Write	'0'	V_{IH}	8	START, Device Select, R$\overline{\text{W}}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, R$\overline{\text{W}}$ = '0'

Note: X = V_{IH} or V_{IL}.

Figure 3. Memory Protection

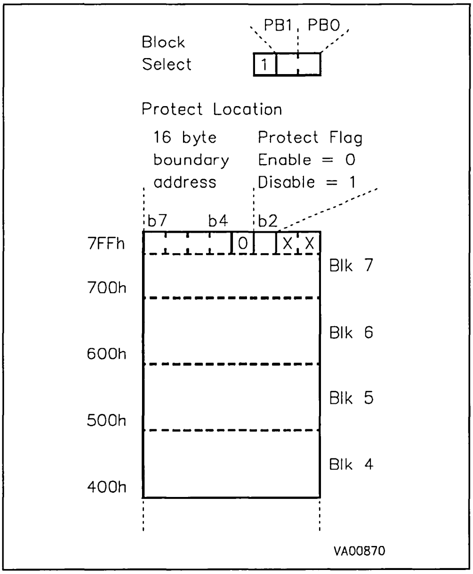

Block
Select
PB1
PB0
1
Protect Location
16 byte
boundary
address
Protect Flag
Enable = 0
Disable = 1
b7
b4
b2
0
X
X
7FFh
700h
600h
500h
400h
Blk 7
Blk 6
Blk 5
Blk 4
VA00870

Figure 4. Typical Interface

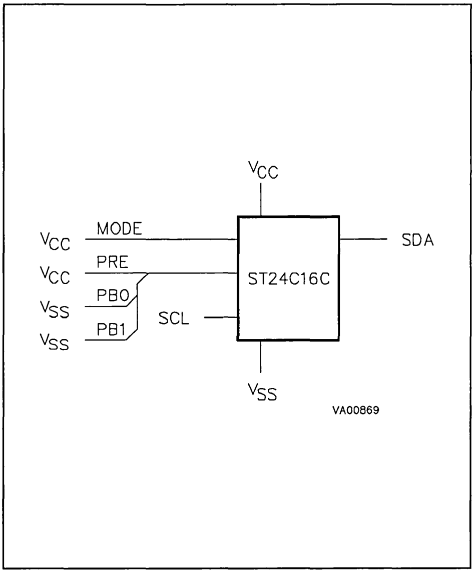
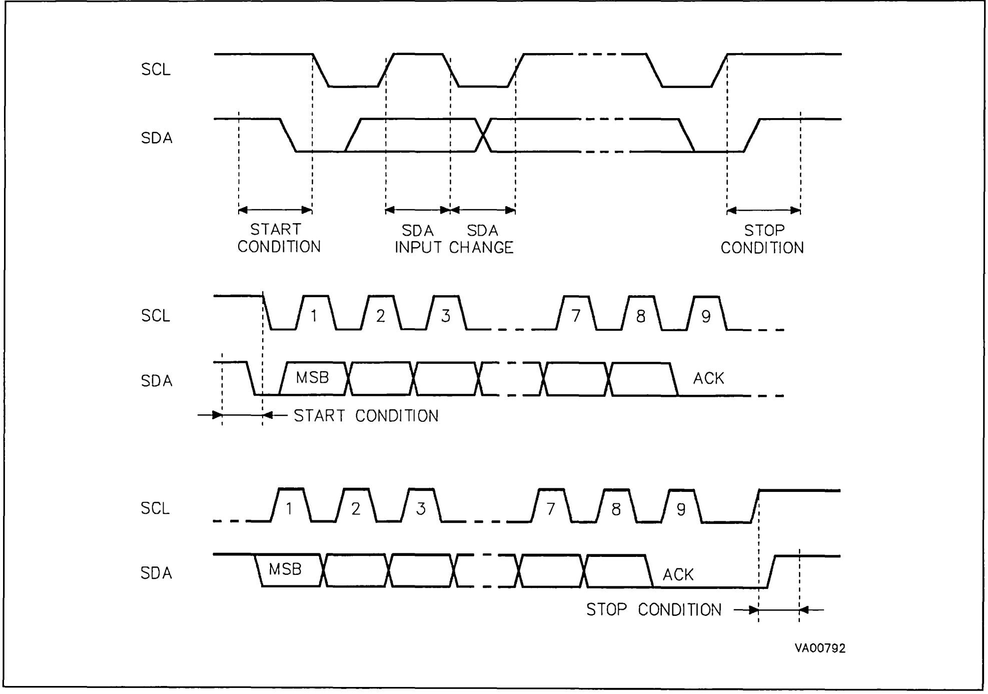

V_{CC}
MODE
V_{CC}
PRE
V_{SS}
PB0
V_{SS}
PB1
SCL
ST24C16C
SDA
V_{CC}
V_{SS}
VA00869

Figure 5. I^{2}C Bus Protocol


SCL
SDA
START
CONDITION
SDA
INPUT
SDA
CHANGE
STOP
CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 6. AC Testing Input Output Waveforms

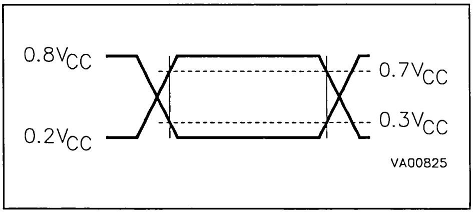

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance [1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested

Figure 7. AC Waveforms

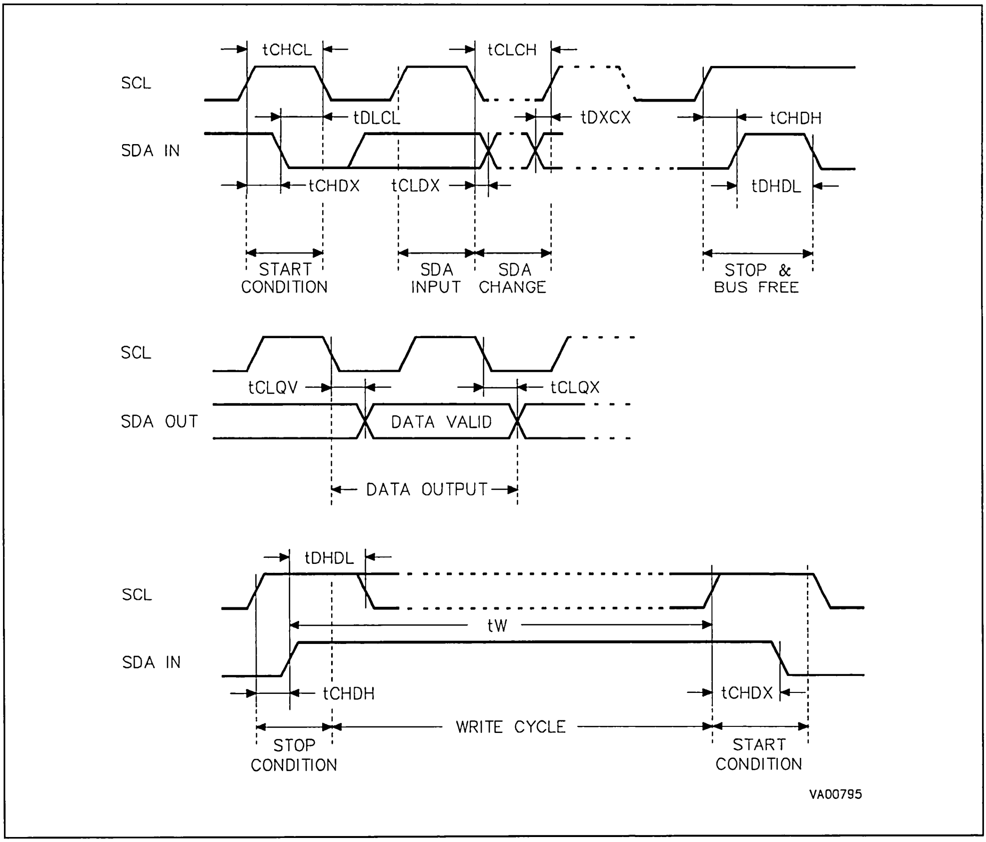

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
STOP CONDITION
WRITE CYCLE
START CONDITION
VA00795

Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
ILO	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	f = 100kHz		2	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = 0V or V_{CC}		100	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (PB0 - PB1, PRE & MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (PB0 - PB1, PRE & MODE)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2 In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

OPERATING MODE (cont'd)

into the top of the upper blocks of the memory, up to location 7FEh. Then establish the memory protect area by hardwiring PB0 & PB1 and set the protection by writing the correct contents into location 7FFh. The area will now be protected when the PRE signal is active (High).

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input High). If the Multibyte write of up to 8 bytes starts at the location just before the protected area then it is able to write over the first 7 bytes in the protected area. The true area protected is therefore smaller and equal to the content of defined in the location 7FFh plus 7 bytes. This does not apply to the Page write mode as the address counter rolls over and thus cannot go above the 16 byte lower boundary of the protected area.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E). This chip enable input is used to set the least significant bit of the 5 bit device select code. It may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Protect Enable (PRE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

DEVICE OPERATION

The ST24C16C supports the I^{2}C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24C16C is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24C16C continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24C16C and the bus master and forces the device into the standby power state.

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24C16C samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST24C16C, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code, block select bits and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^{2}C bus definition. For the ST24C16C these are fixed as 1010b (0Ah).

After a START condition the ST24C16C will acknowledge on the SDA bus during the 9th bit time.

The 5th, 6th and 7th bits sent select one of the 8 blocks of 256 bytes of the memory, effectively acting as memory addresses A10 - A8 (A7 - A0 byte addresses are sent later).

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST24C16C acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes in the selected block of the memory. After receipt of the byte address the ST24C16C again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST24C16C. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the ST24C16C. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A9-A5) are the same. The master sends from 1-16 bytes of data, which are each acknowledged by the ST24C16C. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24C16C will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST24C16C has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $R\overline{W}$ bit set to '1'. The ST24C16C acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the $R\overline{W}$ bit set to '1'. The ST24C16C acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST24C16C continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output; but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 2048 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24C16C waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24C16C terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

Figure 8. Write Modes Sequence

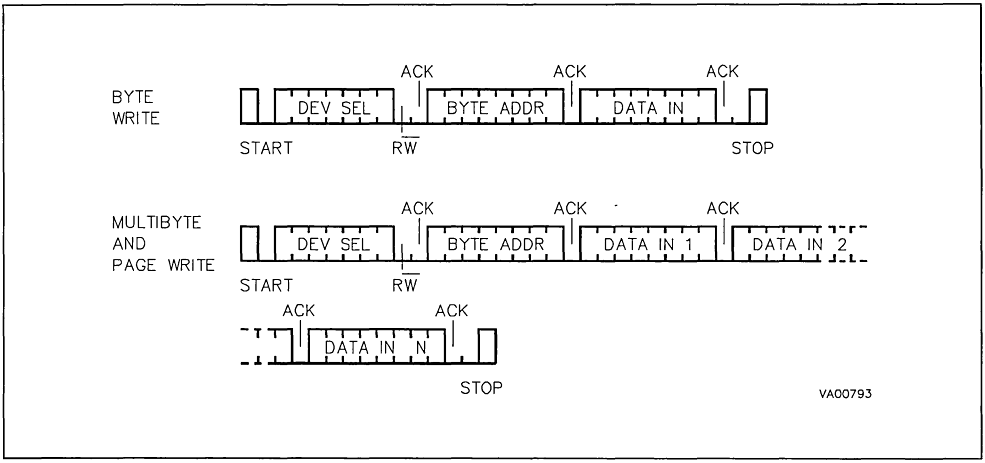
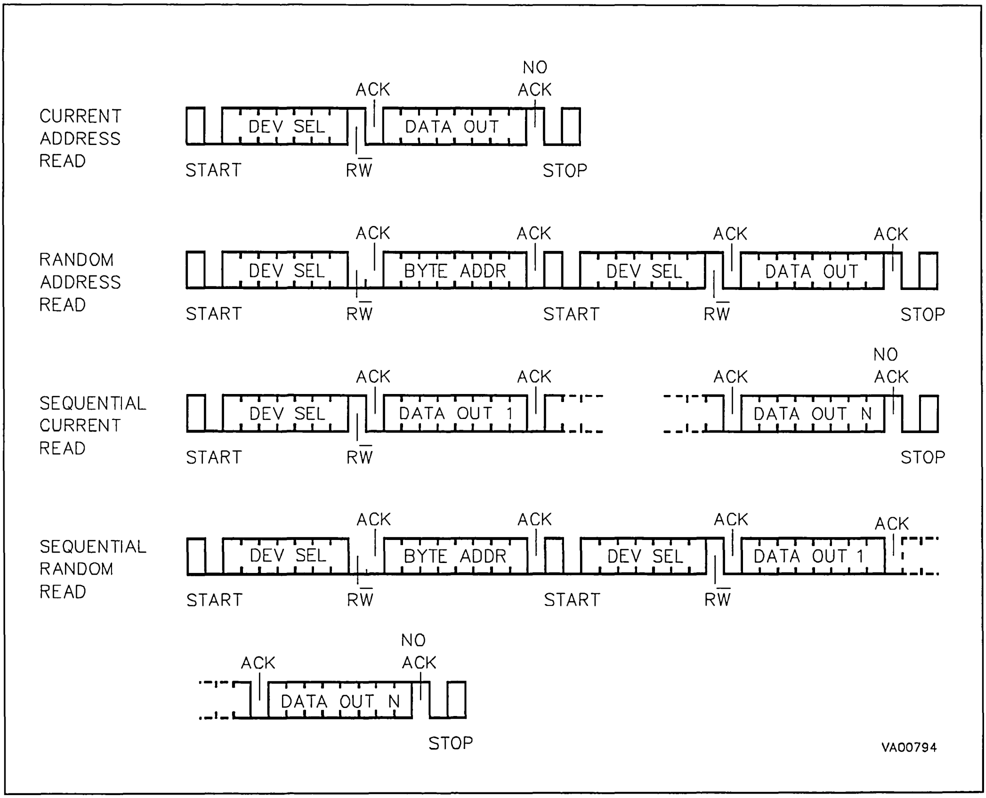

BYTE WRITE
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
DATA IN
ACK
STOP
MULTIBYTE AND PAGE WRITE
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
DATA IN 1
ACK
DATA IN 2
ACK
DATA IN N
ACK
STOP
VA00793

Figure 9. Read Modes Sequence


CURRENT ADDRESS READ
START
DEV SEL
ACK
RW
DATA OUT
NO ACK
STOP
RANDOM ADDRESS READ
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
START
DEV SEL
ACK
RW
DATA OUT
ACK
STOP
SEQUENTIAL CURRENT READ
START
DEV SEL
ACK
RW
DATA OUT 1
ACK
ACK
DATA OUT N
NO ACK
STOP
SEQUENTIAL RANDOM READ
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
START
DEV SEL
ACK
RW
DATA OUT 1
ACK
ACK
DATA OUT N
NO ACK
STOP
VA00794

ORDERING INFORMATION

Example: ST24C16C ML 1 013TR

Package	
B	PSDIP8 0.25 mm Frame
ML	PSO14

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option	
013TR	Tape & Reel

Parts are shipped with the memory content set at all "1's" (0FFh).

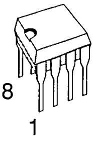
For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

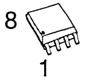
ST25C01

2.5V SERIAL ACCESS CMOS 1K (128 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 2.5V TO 5.5V SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE, FULLY I^{2}C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



PSDIP8 (B)
0.25mm Frame



PSO8 (M)

DESCRIPTION

The ST25C01 is a 1K bit electrically erasable programmable memory (EEPROM), organised as 128 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25C01 operates down to a supply voltage of 2.5V. Both Plastic Dual- in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^{2}C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST25C01 carries a built-in 4 bit, unique device identification code corresponding to the I^{2}C bus definition. This is used together with a 3 bit chip enable input to form a 7 bit memory select signal. In this way up to 8

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

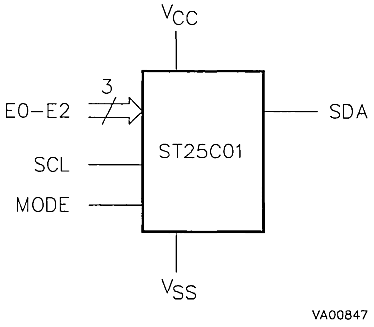


Figure 2A. DIP Pin Connections

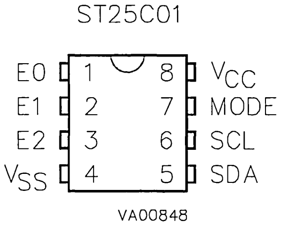


Figure 2B. SO Pin Connections

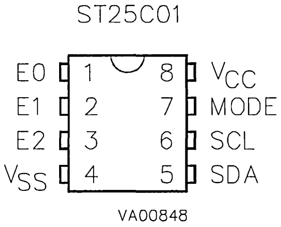


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

ST25C01's may be attached to the I^{2}C bus and selected individually.

The ST25C01 behaves as a slave device in the I^{2}C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 device select bits plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode.

The 8 bits sent after a START condition are made up of 4 bits that identify the device type, 3 chip enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

OPERATING MODES (cont'd)

Byte Write. In this mode a device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the byte. This is follwed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 4 or up to 8 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when $\overline{MODE}$ is at V_{IL}. A device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes written in the Page Write mode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the $R\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the $R\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the $R\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Table 3. Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 128	As Current or Random Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}.

DEVICE OPERATION

The ST25C01 supports the I^{2}C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST25C01 is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST25C01 continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST25C01 and the bus master and forces the device into the standby power state.

Figure 3. Typical Interface

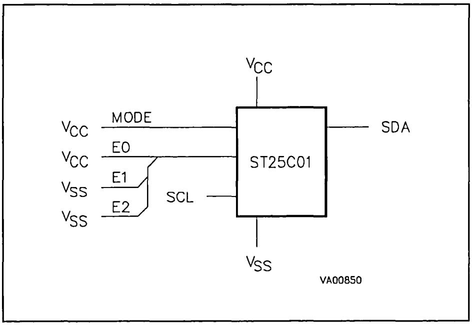
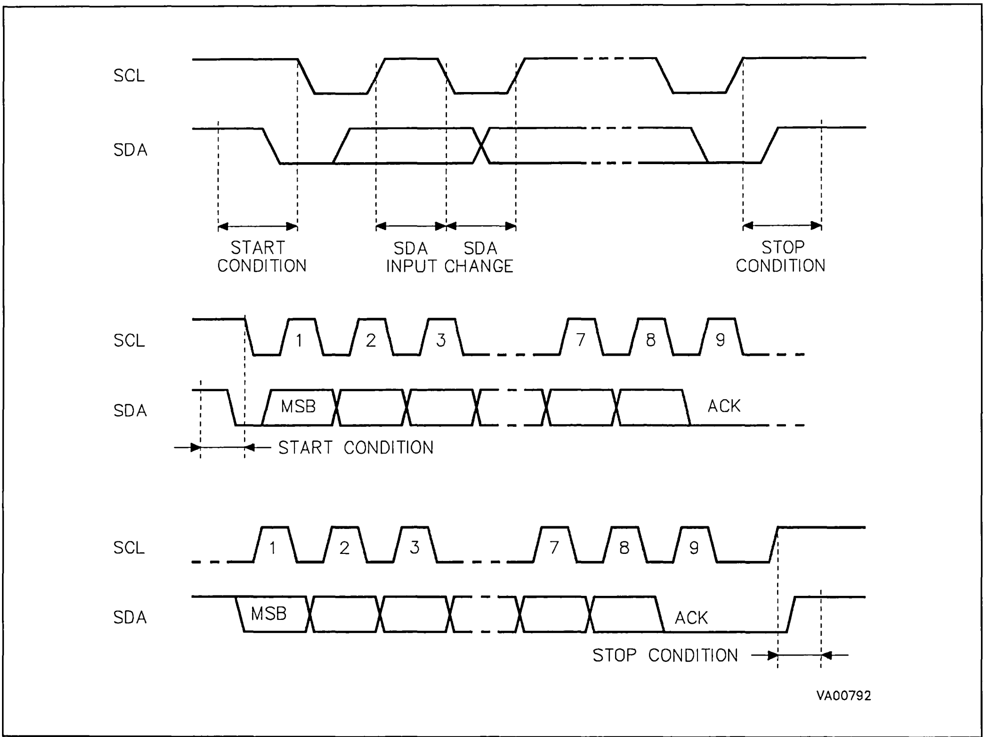

VCC
VCC
MODE
VCC
E0
E1
VSS
E2
VSS
SCL
ST25C01
SDA
VSS
VA00850

Figure 4. I^{2}C Bus Protocol


SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 5. AC Testing Input Output Waveforms

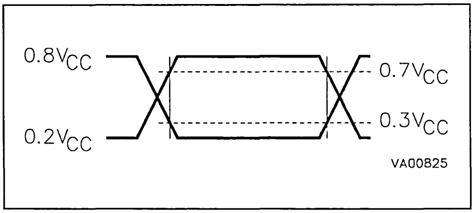

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance [1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only and not 100%. tested.

Figure 6. AC Waveforms

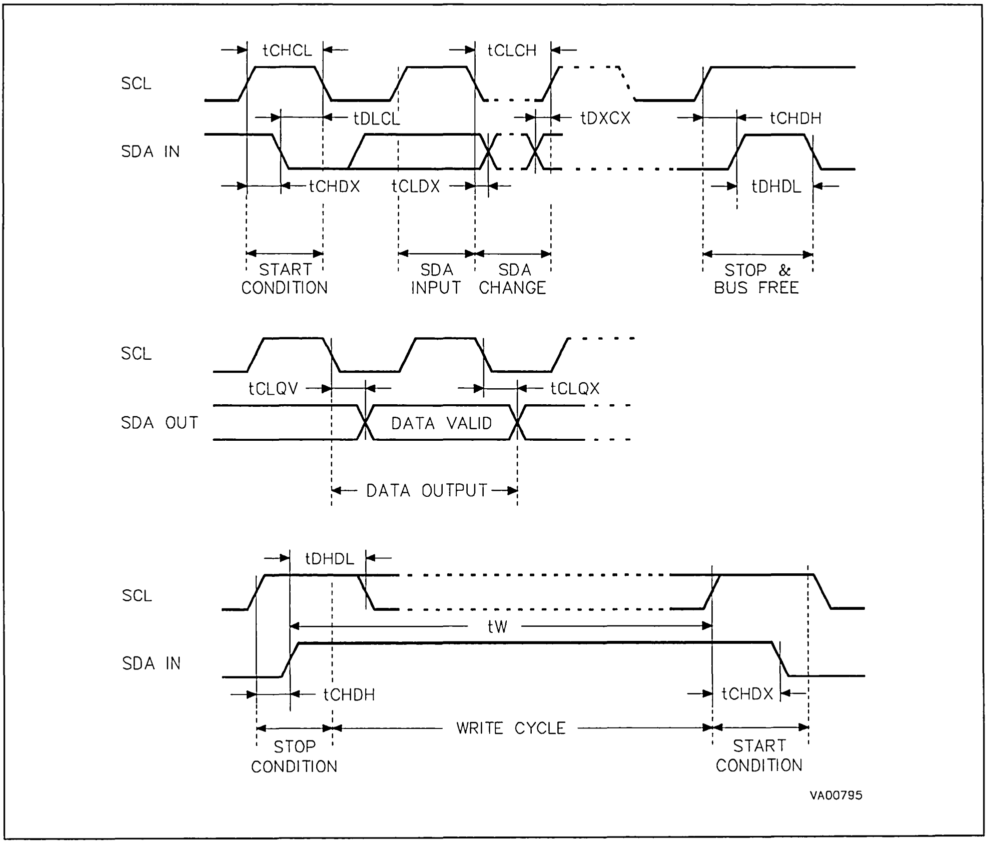

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
WRITE CYCLE
STOP CONDITION
START CONDITION
VA00795

Table 5. DC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	V_{CC} = 2.5V, f = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 2.5V, V_{IN} = 0V or V_{CC}		5	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0 - E2, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0 - E2, MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V

Table 6. AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.

2 In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

DEVICE OPERATION (cont'd)

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST25C01 samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST25C01, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^{2}C bus definition. For the ST25C01 these are fixed as 1010b (0Ah).

The following 3 bits identify the specific ST25C01 on the bus. They are matched to the chip enable signals E0 - E2. Thus up to 8 ST25C01's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST25C01's on the bus will identify the device code and compare the following 3 bits to the chip enable inputs E0 - E2. If a match is found the corresponding ST25C01 will acknowledge the identification on the SDA bus during the 9th bit time.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST25C01 acknowledges this and waits for a byte address. The byte address of 8 bits (the MSB, bit 7, is not used or 'don't care') provides access to any of the 128 bytes of the memory. After receipt of the byte address the ST25C01 again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST25C01. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the ST25C01. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from 1-8 bytes of data, which are each acknowledged by the ST25C01. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST25C01 will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programming time is doubled to a maximum of 20ms.

Figure 7. Write Modes Sequence

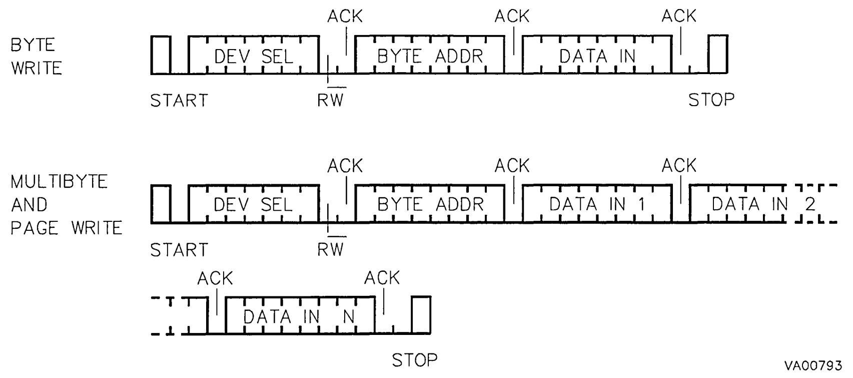
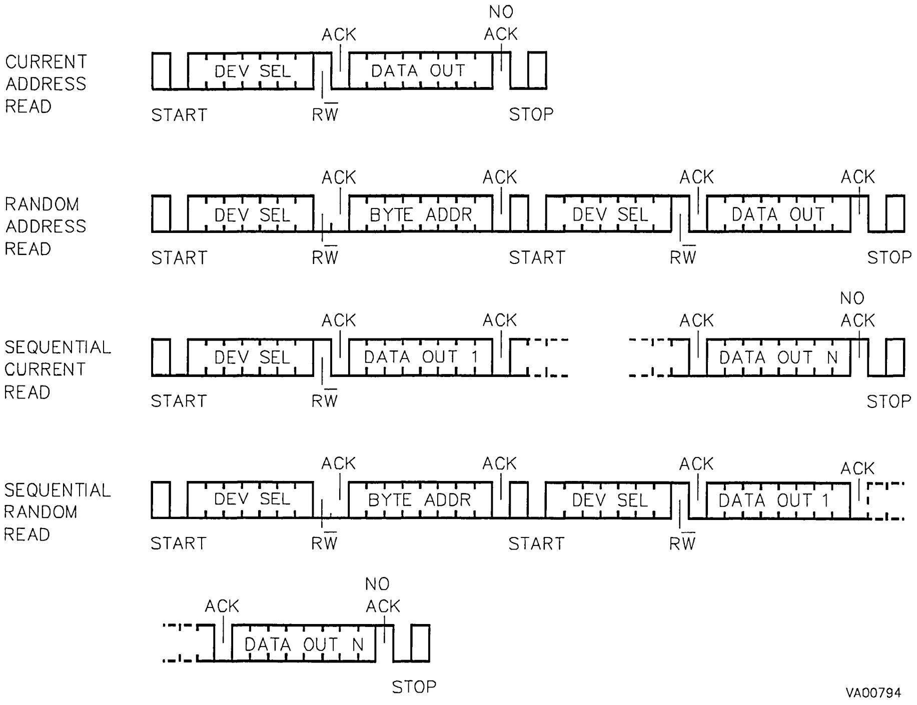

BYTE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN
START
RW
STOP
MULTIBYTE AND PAGE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN 1
DATA IN 2
START
RW
ACK
ACK
DATA IN N
STOP
VA00793

Figure 8. Read Modes Sequence


CURRENT ADDRESS READ
NO ACK
ACK
DEV SEL
DATA OUT
START
RW
STOP
RANDOM ADDRESS READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT
START
RW
START
RW
STOP
SEQUENTIAL CURRENT READ
ACK
ACK
ACK
NO ACK
DEV SEL
DATA OUT 1
DATA OUT N
START
RW
STOP
SEQUENTIAL RANDOM READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT 1
START
RW
START
RW
ACK
NO ACK
DATA OUT N
STOP
VA00794

Read Operation

Read operations are independent of the state of the MODE signal.

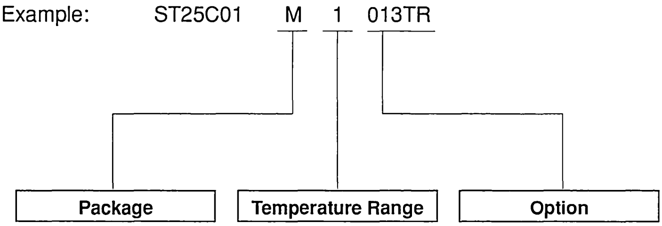
Current Address Read. The ST25C01 has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R$\overline{W}$ bit set to '1'. The ST25C01 acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the R$\overline{W}$ bit set to '1'. The ST25C01 acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST25C01 continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 128 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST25C01 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST25C01 terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

ORDERING INFORMATION



Package		Temperature Range		Option	
B	PSDIP8 0.25 mm Frame	1	0 to 70 °C	013TR	Tape & Reel
M	PSO8	3	–40 to 125 °C		
		6	–40 to 85 °C		

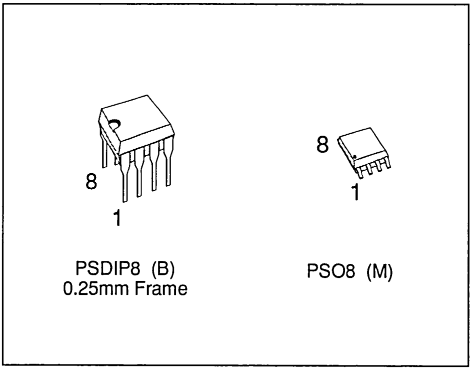
Parts are shipped with the memory content set at all "1's" (0FFh).

For a list of available options of Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

2.5V SERIAL ACCESS CMOS 2K (256 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 2.5V TO 5.5V SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE, FULLY I²C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



DESCRIPTION

The ST25C02A is a 2K bit electrically erasable programmable memory (EEPROM), organised as 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25C02A operates down to a supply voltage of 2.5V. Both Plastic Dual- in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I²C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST25C02A carries a built-in 4 bit, unique device identification code corresponding to the I²C bus definition. This is used together with a 3 bit chip enable input to form a 7 bit memory select signal. In this way up to 8

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

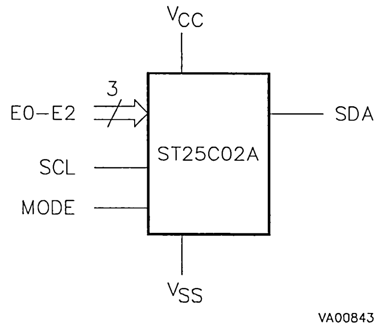


Figure 2A. DIP Pin Connections

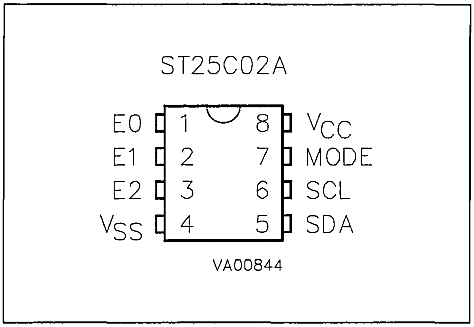


Figure 2B. SO Pin Connections

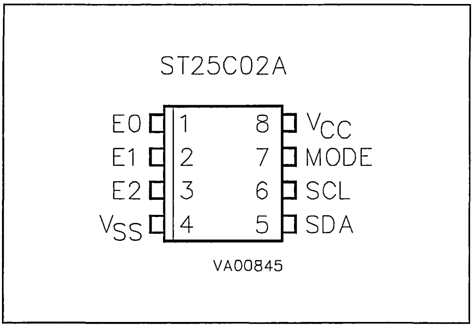


Table 2. Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)			4000	V
	Electrostatic Discharge Voltage (Machine model)			1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DESCRIPTION (cont'd)

ST25C02A's may be attached to the I²C bus and selected individually.

The ST25C02A behaves as a slave device in the I²C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 device select bits plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode.

The 8 bits sent after a START condition are made up of 4 bits that identify the device type, 3 chip enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

OPERATING MODES (cont'd)

Byte Write. In this mode a device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the byte. This is follwed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 4 or up to 8 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when MODE is at V_{IL}. A device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes written in the Page Write mode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the $R\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the $R\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the $R\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Table 3. Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 256	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

DEVICE OPERATION

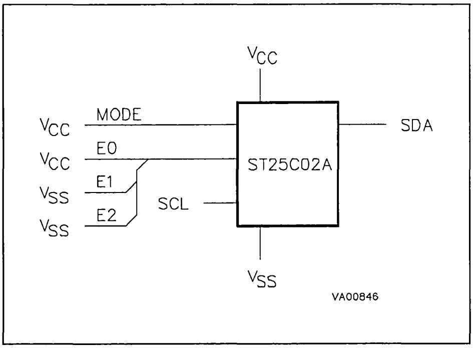
The ST25C02A supports the I^{2}C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST25C02A is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

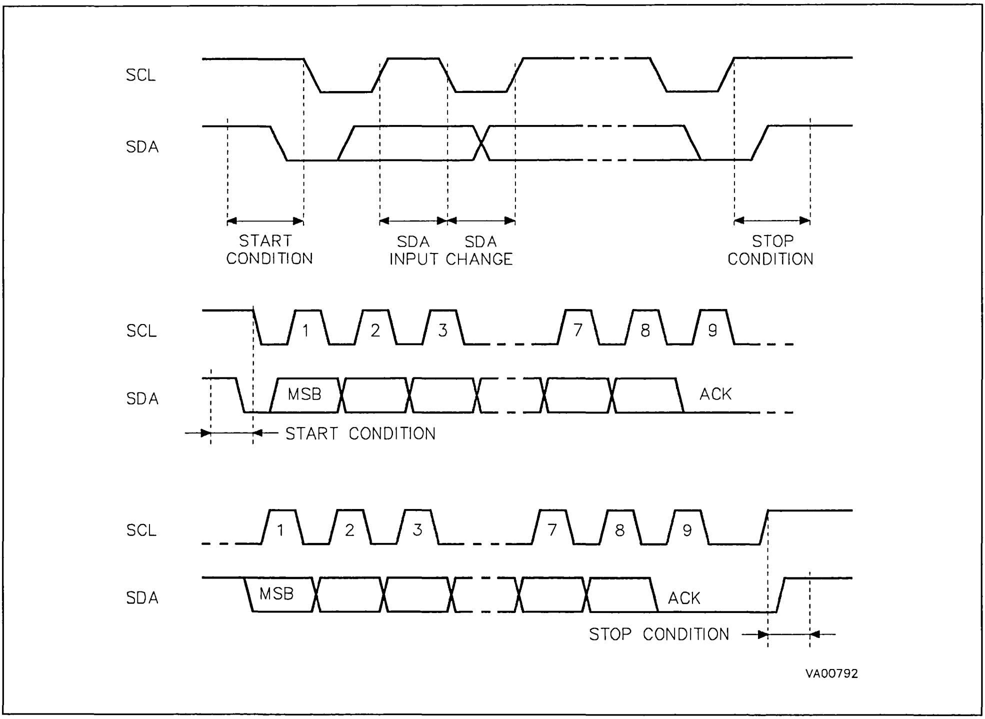
Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST25C02A continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 3. Typical Interface


VCC
VCC
MODE
E0
VCC
E1
VSS
E2
VSS
SCL
ST25C02A
SDA
VSS
VA00846

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST25C02A and the bus master and forces the device into the standby power state.

Figure 4. I^{2}C Bus Protocol


SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 5. AC Testing Input Output Waveforms

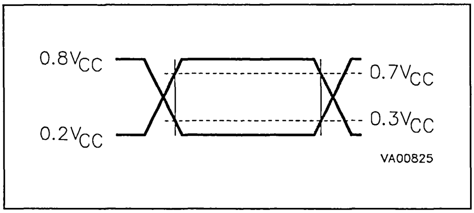

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance[1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only and not 100% tested.

Figure 6. AC Waveforms

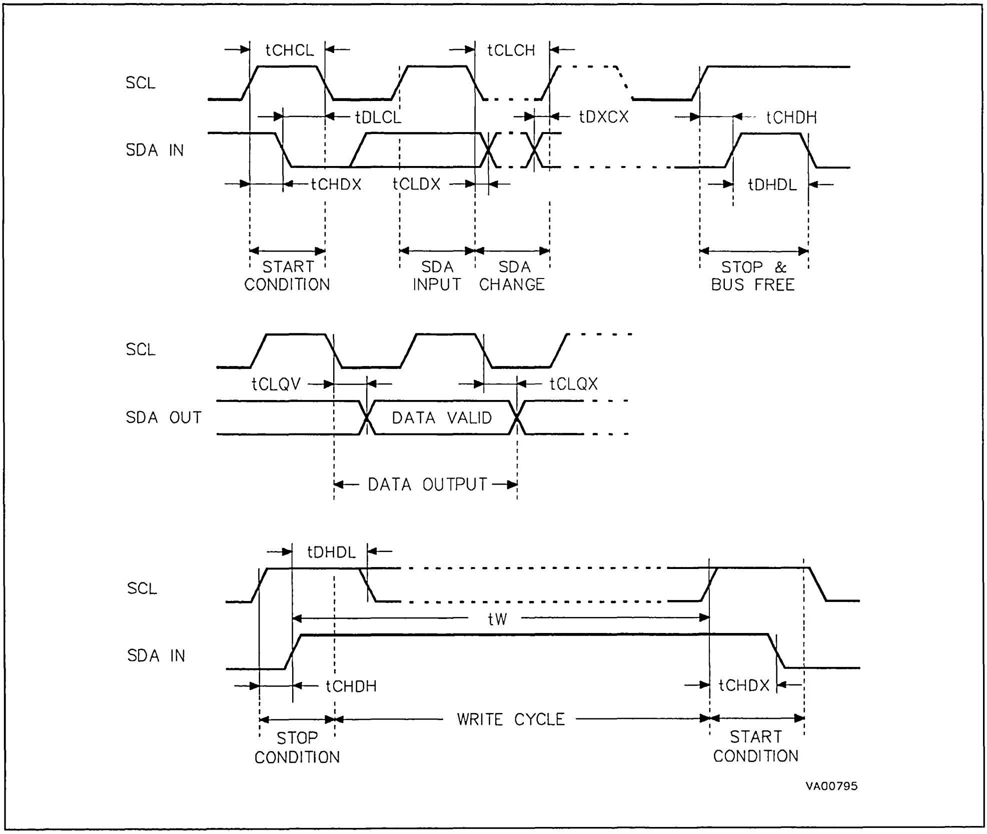

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
STOP CONDITION
WRITE CYCLE
START CONDITION
VA00795

Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±2	µA
I_{CC}	Supply Current	V_{CC} = 2.5V, f = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 2.5V, V_{IN} = 0V or V_{CC}		5	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0 - E2, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0 - E2, MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1 For a re START condition, or following a write cycle
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

DEVICE OPERATION (cont'd)

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST25C02A samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST25C02A, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^{2}C bus definition. For the ST25C02A these are fixed as 1010b (0Ah).

The following 3 bits identify the specific ST25C02A on the bus. They are matched to the chip enable signals E0 - E2. Thus up to 8 ST25C02A's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST25C02A's on the bus will identify the device code and compare the following 3 bits to the chip enable inputs E0 - E2. If a match is found the corresponding ST25C02A will acknowledge the identification on the SDA bus during the 9th bit time.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST25C02A acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes of the memory. After receipt of the byte address the ST25C02A again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST25C02A. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the ST25C02A. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from 1-8 bytes of data, which are each acknowledged by the ST25C02A. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST25C02A will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Figure 7. Write Modes Sequence

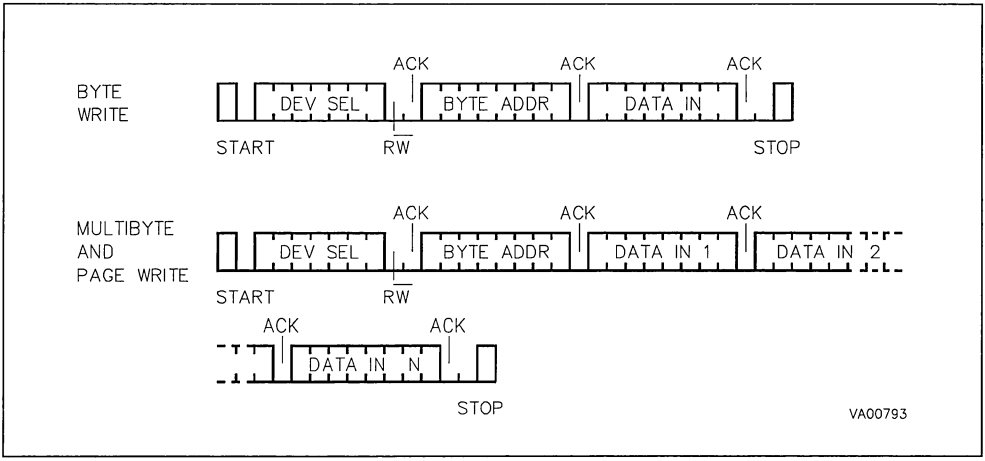
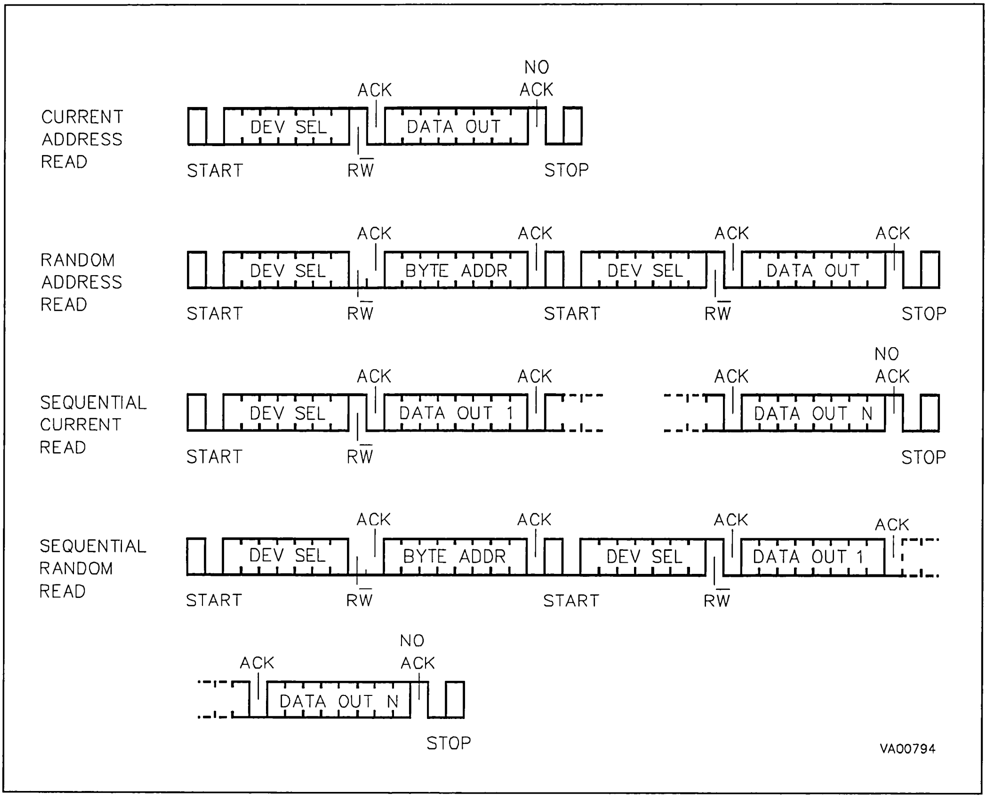

BYTE WRITE
ACK
ACK
ACK
START
DEV SEL
RW
BYTE ADDR
DATA IN
STOP
MULTIBYTE AND PAGE WRITE
ACK
ACK
ACK
START
DEV SEL
RW
BYTE ADDR
DATA IN 1
DATA IN 2
ACK
ACK
DATA IN N
STOP
VA00793

Figure 8. Read Modes Sequence


CURRENT ADDRESS READ
ACK
NO ACK
START
DEV SEL
RW
DATA OUT
STOP
RANDOM ADDRESS READ
ACK
ACK
ACK
ACK
START
DEV SEL
RW
BYTE ADDR
START
DEV SEL
RW
DATA OUT
STOP
SEQUENTIAL CURRENT READ
ACK
ACK
ACK
NO ACK
START
DEV SEL
RW
DATA OUT 1
DATA OUT N
STOP
SEQUENTIAL RANDOM READ
ACK
ACK
ACK
ACK
START
DEV SEL
RW
BYTE ADDR
START
DEV SEL
RW
DATA OUT 1
ACK
NO ACK
DATA OUT N
STOP
VA00794

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST25C02A has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R$\overline{\text{W}}$ bit set to '1'. The ST25C02A acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the R$\overline{\text{W}}$ bit set to '1'. The ST25C02A acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST25C02A continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 256 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST25C02A waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST25C02A terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

ORDERING INFORMATION

Example: ST25C02A M 1 013TR

Package

B	PSDIP8 0.25 mm Frame
M	PSO8

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option

013TR	Tape & Reel

Parts are shipped with the memory content set at all "1's" (0FFh).

For a list of available options of Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

SGS-THOMSON
MICROELECTRONICS

ST25C04

2.5V SERIAL ACCESS CMOS 4K (2 by 256 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 2.5V TO 5.5V POWER SUPPLY
- USER DEFINED WRITE PROTECT AREA
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL

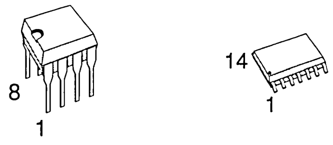
DESCRIPTION

The ST25C04 is a 4K bit electrically erasable programmable memory (EEPROM), organised as 2 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^2C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST25C04 carries a built-in 4 bit, unique device identification code corresponding to the I^2C bus definition. This is used together with a 2 bit chip enable input to form a 6 bit memory select signal. In this way up to 4

Table 1. Signal Names

PRE	Write Protect Enable
E1 - E2	Chip Enable Inputs
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground



PSDIP8 (B)
0.25mm Frame

PSO14 (ML)

Figure 1. Logic Diagram

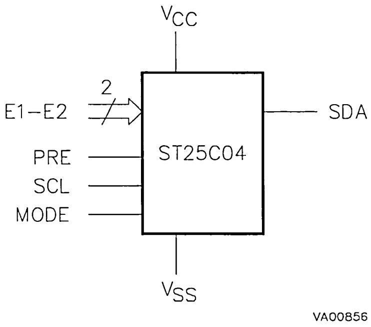


Figure 2A. DIP Pin Connections

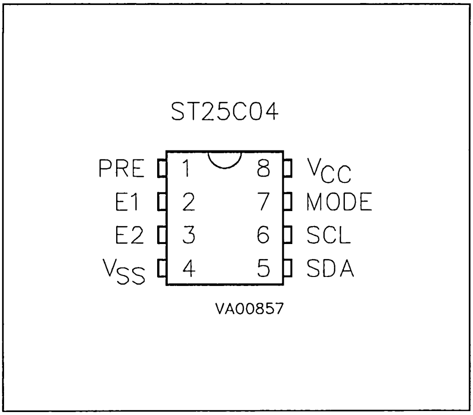
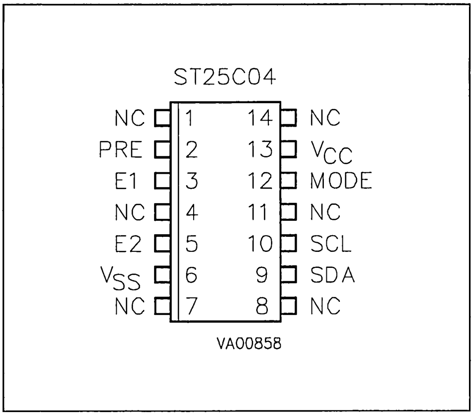


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO14 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

ST25C04's may be attached to the I^2C bus and selected individually.

The ST25C04 behaves as a slave device in the I^2C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 6 device select bits, one block select bit, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the upper block of the memory may be write protected. The protected area is programmable to start on any 8 byte boundary. Protection is enabled by a memory bit flag and the PRE signal input.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used

OPERATING MODES (cont'd)

to set the operating mode. For the Protect mode the status of the PRE input determines whether protection is enabled or disabled.

The 8 bits sent after a START condition are made up of a device select of 4 bits that identify the device type, 2 chip enable bits, one block select bit and one bit for a READ (R$\overline{W}$ = 1) or WRITE (R$\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

Byte Write. In this mode a device select is sent with the R$\overline{W}$ bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 4 or up to 8 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when MODE is at V_{IL}. A device select is sent with the R$\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes written in the Page Write mode must have the same five upper address bits.

Current Address Read. In this mode the device select is sent with the R$\overline{W}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the R$\overline{W}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the R$\overline{W}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

Write Protect. Data in the upper 256 byte block of the memory may be write protected. The protection starts at any 8 byte boundary. The address at which protection starts is defined by the contents of the upper 5 bits (b7- b3 of the top memory location (block 1, byte address 1FFh). Bit 2 of this memory location is used as a flag to indicate that the protection is enabled (b2 = '0') or disabled (b2 = '1'). The lower two bits, b1 & b0, are not used. The sequence to follow to use the memory protect feature is as follows: write the memory contents to be protected into the top of the upper block of the memory, up to location 1FEh. Then establish the memory protect area and set the protection by writing the correct contents into location 1FFh. The area will now be protected when the PRE signal is active (High).

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	R$\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	A8	R$\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	R$\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, R$\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 512	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, R$\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, R$\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

Figure 3. Memory Protection

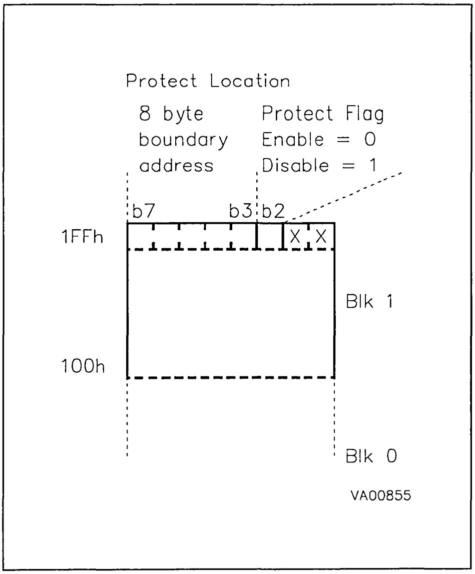

Protect Location
8 byte boundary address
Protect Flag
Enable = 0
Disable = 1
b7
b3
b2
X
X
1FFh
100h
Blk 1
Blk 0
VA00855

Figure 4. Typical Interface

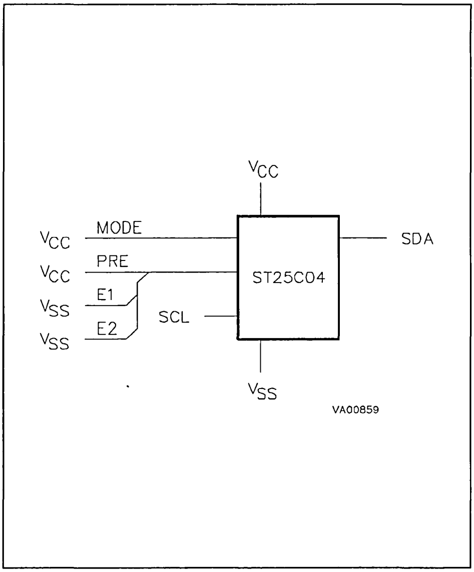
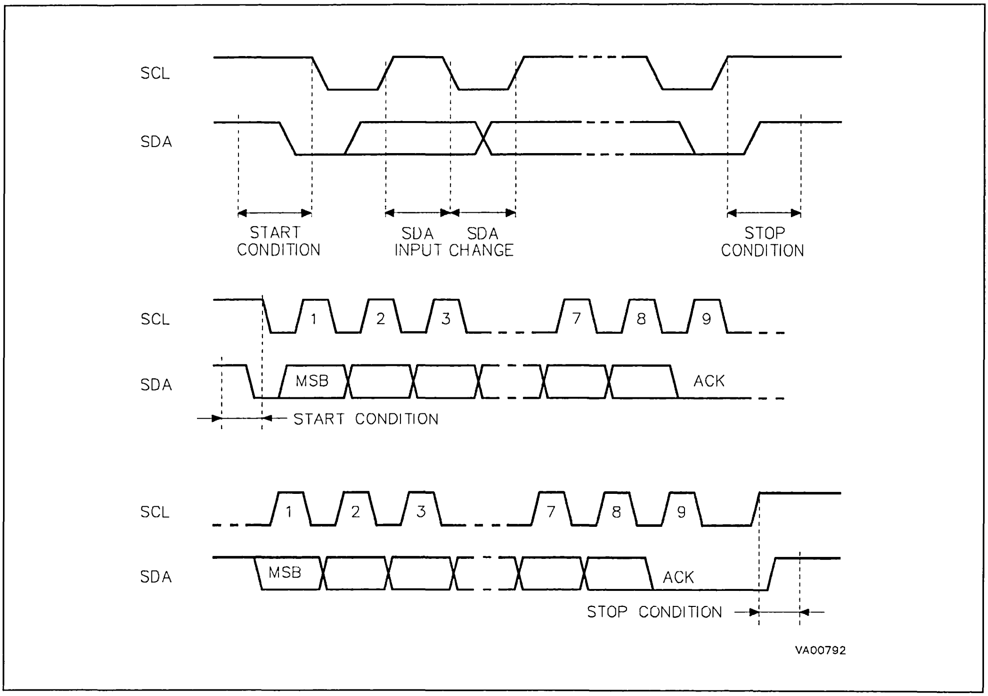

VCC
MODE
VCC
PRE
VSS
E1
VSS
E2
SCL
ST25C04
SDA
VCC
VSS
VA00859

Figure 5. I^{2}C Bus Protocol


SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 6. AC Testing Input Output Waveforms

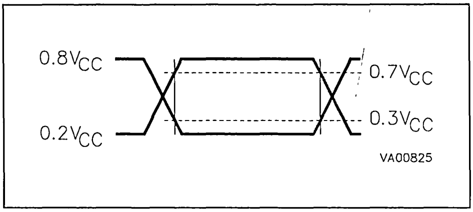

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 7. Capacitance [(1)] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested

Figure 7. AC Waveforms

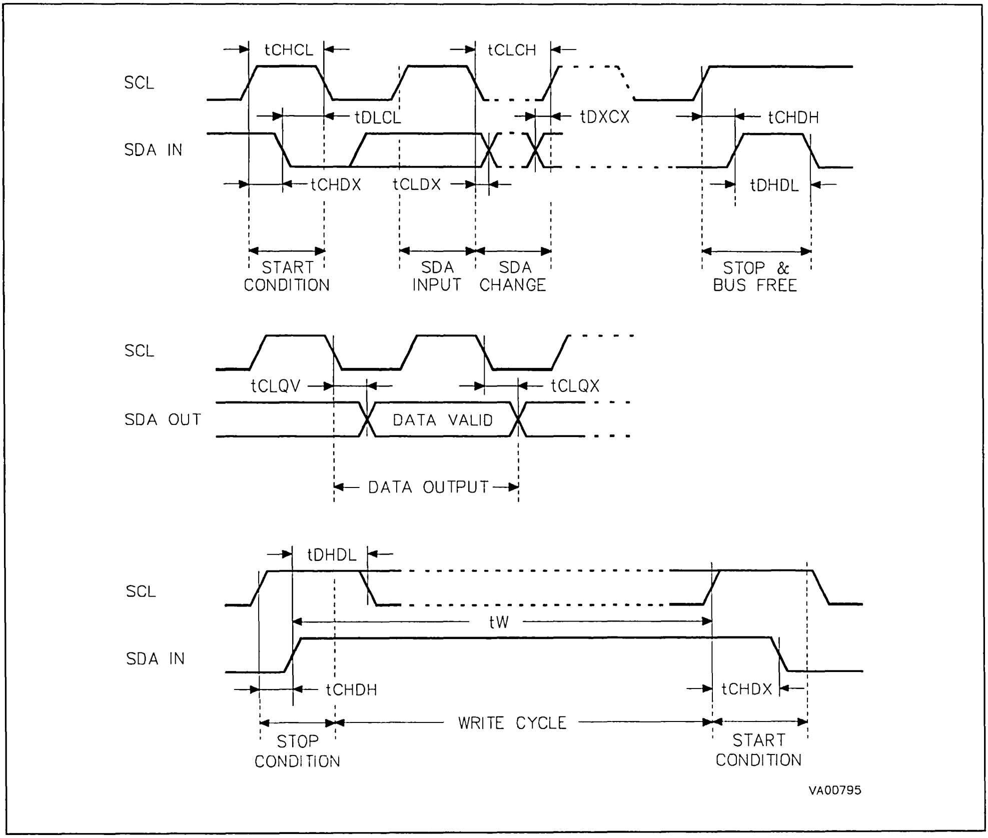

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
WRITE CYCLE
STOP CONDITION
START CONDITION
VA00795

Table 5. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	V_{CC} = 2.5V, f = 100kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 2.5V, V_{IN} = 0V or V_{CC}		5	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E1 - E2, PRE, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E1 - E2, PRE, MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 6. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

OPERATING MODE (cont'd)

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input High). If the Multibyte write of up to 4 bytes starts at the location just before the protected area then it is able to write over the first 3 bytes in the protected area. The true area protected is therefore smaller and equal to the content of defined in the location 1FFh plus 3 bytes. This does not apply to the Page write mode as the address counter rolls over and thus cannot go above the 8 byte lower boundary of the protected area.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Chip Enable (E1 - E2). These chip enable inputs are used to set the 2 least significant bits of the 6 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Protect Enable (PRE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

DEVICE OPERATION

The ST25C04 supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST25C04 is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST25C04 continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST25C04 and the bus master and forces the device into the standby power state.

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST25C04 samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST25C04, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code, block select bit and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^{2}C bus definition. For the ST25C04 these are fixed as 1010b (0Ah).

The following 2 bits identify the specific ST25C04 on the bus. They are matched to the chip enable signals E1 - E2. Thus up to 4 ST25C04's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST25C04's on the bus will identify the device code and compare the following 2 bits to the chip enable inputs E1 - E2. If a match is found the corresponding ST25C04 will acknowledge the identification on the SDA bus during the 9th bit time.

The 7th bit sent selects one of the two blocks of 256 bytes of the memory, effectively acting as memory address A8 (A7 - A0 byte addresses are sent later).

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST25C04 acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes in the selected block of the memory. After receipt of the byte address the ST25C04 again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST25C04. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the ST25C04. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A8-A4) are the same. The master sends from 1-8 bytes of data, which are each acknowledged by the ST25C04. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST25C04 will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST25C04 has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $R\overline{W}$ bit set to '1'. The ST25C04 acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the $R\overline{W}$ bit set to '1'. The ST25C04 acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Figure 8. Write Modes Sequence

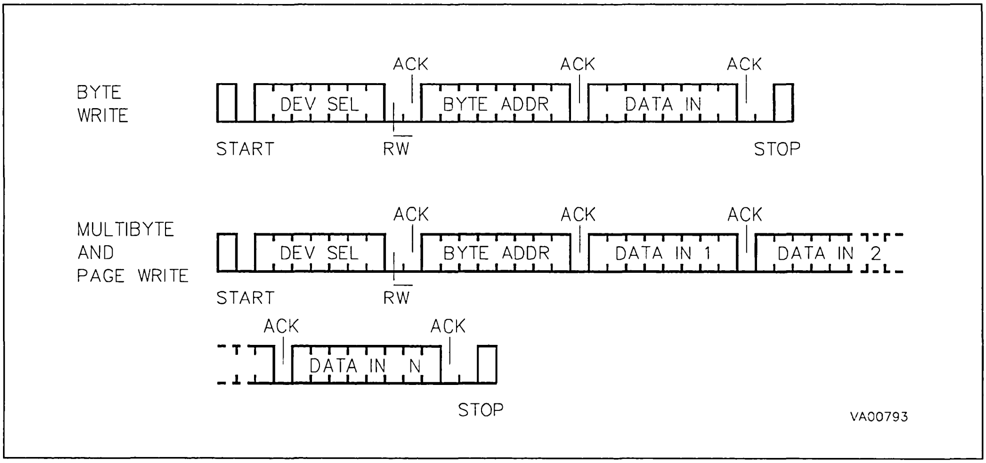
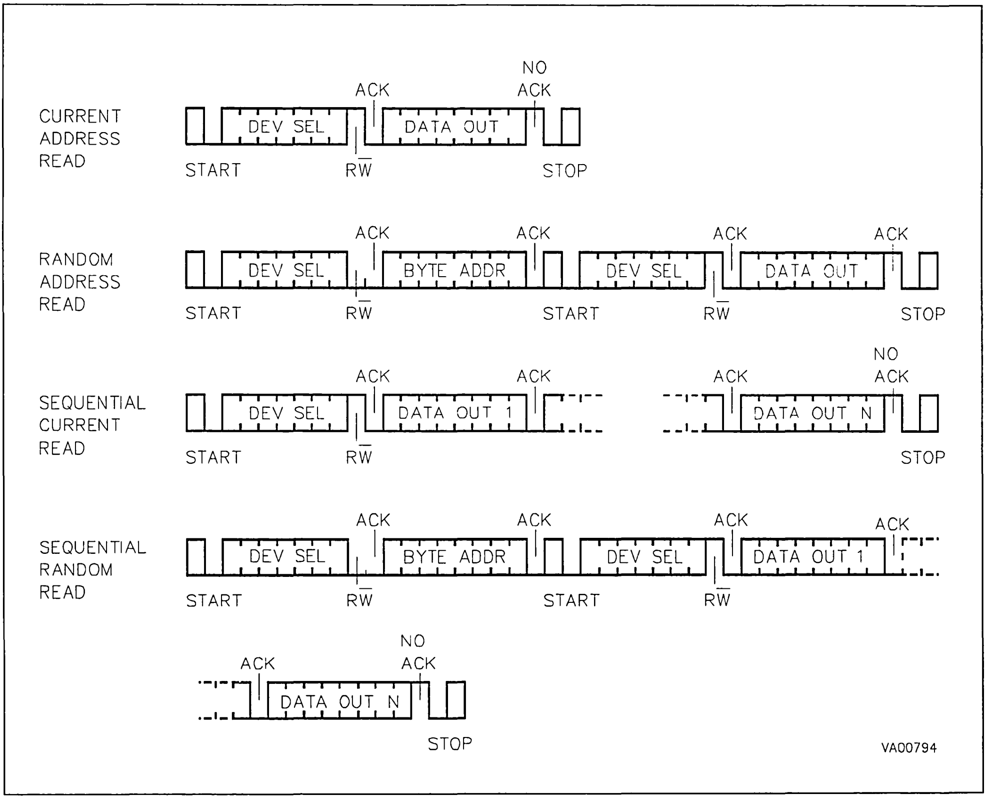

BYTE WRITE
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
DATA IN
ACK
STOP
MULTIBYTE AND PAGE WRITE
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
DATA IN 1
ACK
DATA IN 2
ACK
DATA IN N
ACK
STOP
VA00793

Figure 9. Read Modes Sequence


CURRENT ADDRESS READ
START
DEV SEL
ACK
RW
DATA OUT
NO ACK
STOP
RANDOM ADDRESS READ
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
START
DEV SEL
ACK
RW
DATA OUT
ACK
STOP
SEQUENTIAL CURRENT READ
START
DEV SEL
ACK
RW
DATA OUT 1
ACK
ACK
DATA OUT N
NO ACK
STOP
SEQUENTIAL RANDOM READ
START
DEV SEL
ACK
RW
BYTE ADDR
ACK
START
DEV SEL
ACK
RW
DATA OUT 1
ACK
ACK
DATA OUT N
NO ACK
STOP
VA00794

DEVICE OPERATION (cont'd)

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST25C04 continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 512 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST25C04 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST25C04 terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

ORDERING INFORMATION

Example: ST25C04 ML 1 013TR

Package

B	PSDIP8 0.25 mm Frame
ML	PSO14

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option

013TR	Tape & Reel

Parts are shipped with the memory content set at all "1's" (0FFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

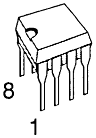
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

ST25C08

2.5V SERIAL ACCESS CMOS 8K (4 by 256 x 8) EEPROM

- 1,000,000 ERASE/WRITE CYCLES MINIMUM, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 2.5V TO 5.5V POWER SUPPLY
- USER DEFINED WRITE PROTECT AREA
- TWO WIRE SERIAL INTERFACE, FULLY I^{2}C BUS COMPATIBLE
- BYTE AND MULTIBYTE WRITE (UP TO 8 BYTES)
- PAGE WRITE (UP TO 16 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- GUARANTED 4kV ESD PROTECTION, USING HUMAN BODY MODEL



PSDIP8 (B)
0.25mm Frame

DESCRIPTION

The ST25C08 is an 8K bit electrically erasable programmable memory (EEPROM), organised as 4 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with the I^{2}C standard, two wire, serial interface which uses a bi-directional data bus and serial clock. The ST25C08 carries a built-in 4 bit, unique device identification code corresponding to the I^{2}C bus definition. This is used together with a chip enable input to form a 5 bit memory select signal. In this way up to 2

Table 1. Signal Names

PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

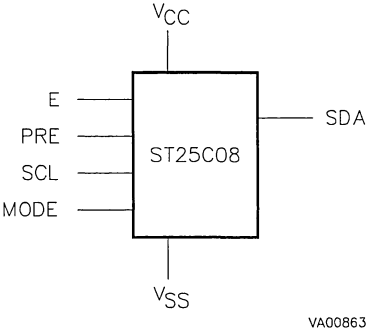
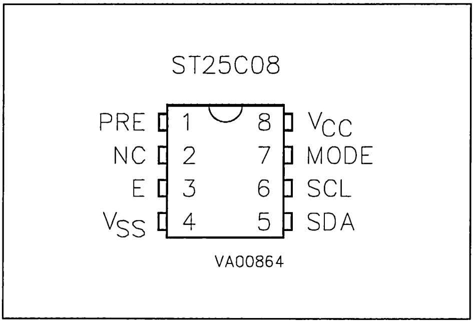


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSDIP8 package) 10 sec	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

ST25C08's may be attached to the I^2C bus and selected individually.

The ST25C08 behaves as a slave device in the I^2C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 5 device select bits, 2 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the upper block of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. Protection is enabled by setting a memory bit flag and the PRE signal input.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode. For the Protect mode the status of the PRE input determines whether protection is enabled or disabled.

The 8 bits sent after a START condition are made up of a device select of 4 bits that identify the device type, a chip enable bit, 2 block select bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

Byte Write. In this mode a device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programing cycle.

Multibyte Write and Page Write. In these modes up to 8 or up to 16 bytes respectively may be written in one programing cycle. Multibyte Write mode is activated when the MODE pin is at V_{IH} level and Page Write when MODE is at V_{IL}. A device select is sent with the $R\overline{W}$ bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programing cycle. All 8 bytes in the Page Write mode must have the same five upper address bits.

OPERATING MODES (cont'd)

Current Address Read. In this mode the device select is sent with the $\overline{RW}$ bit at '1'. The address of the previous byte accessed is automatically incremented and the new byte read.

Random Address Read. This mode allows random access to the memory. A device select is sent with the $\overline{RW}$ bit at '0' (write), followed by the byte address. Then a new START condition is forced with the same device select is sent with the $\overline{RW}$ bit at '1' (read) and the byte is read.

Sequential Read. This mode starts with either a Current Address or Random Address read sequence, it reads consecutive bytes as long as the bus master acknowledges each one without generating a STOP condition.

Write Protect. Data in the upper 256 byte block of the memory may be write protected. The protection starts at any 16 byte boundary. The address at which protection starts is defined by the contents of the upper 4 bits (b7- b4) of the top memory location (block 3, byte address 3FFh). Bit 3 of this memory location is always '0' and bit 2 is used as a flag to indicate that the protection is enabled (b2 = '0') or disabled (b2 = '1'). The lower two bits, b1 & b0, are not used. The sequence to follow to use the memory protect feature is as follows: write the memory contents to be protected into the top of the upper block of the memory, up to location 3FEh. Then establish the memory protect area and set the protection by writing the correct contents into location 3FFh. The area will now be protected when the PRE signal is active (High).

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input High). If the Multibyte write of up to 8 bytes starts at the location just before the protected area then it is able to write over the first 7 bytes in the protected area. The true area protected is therefore smaller and equal to the content of defined in the location 3FFh plus 7 bytes. This does not apply to the Page write mode as the address counter rolls over and thus cannot go above the 16 byte lower boundary of the protected area.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input is used to synchronise all Data In and Data Out of the memory. A resistor must be connected from the SCL line to V_{CC} to act as a pull up.

Serial Data (SDA). The SDA signal is bi-directional and used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E	A9	A8	$\overline{RW}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$\overline{RW}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	X		START, Device Select, $\overline{RW}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	X	1 to 1024	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IH} or V_{IL}	1	START, Device Select, $\overline{RW}$ = '0'
Multibyte Write	'0'	V_{IH}	8	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, $\overline{RW}$ = '0'

Note: X = V_{IH} or V_{IL}

Figure 3. Memory Protection

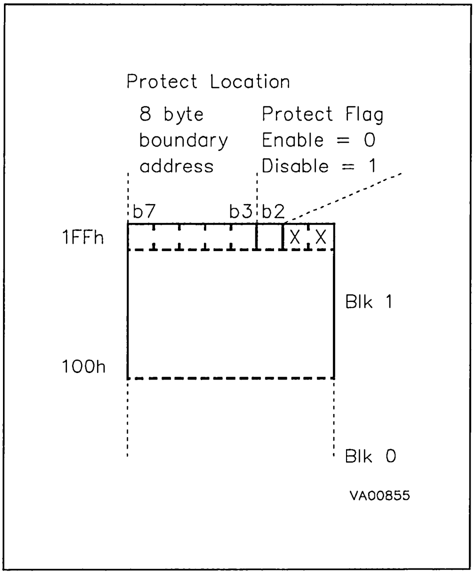

Protect Location
8 byte boundary address
Protect Flag
Enable = 0
Disable = 1
b7
b3
b2
X
X
1FFh
Blk 1
100h
Blk 0
VA00855

Figure 4. Typical Interface

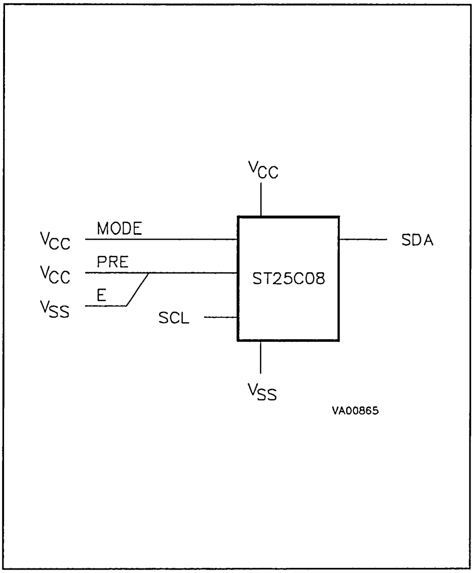
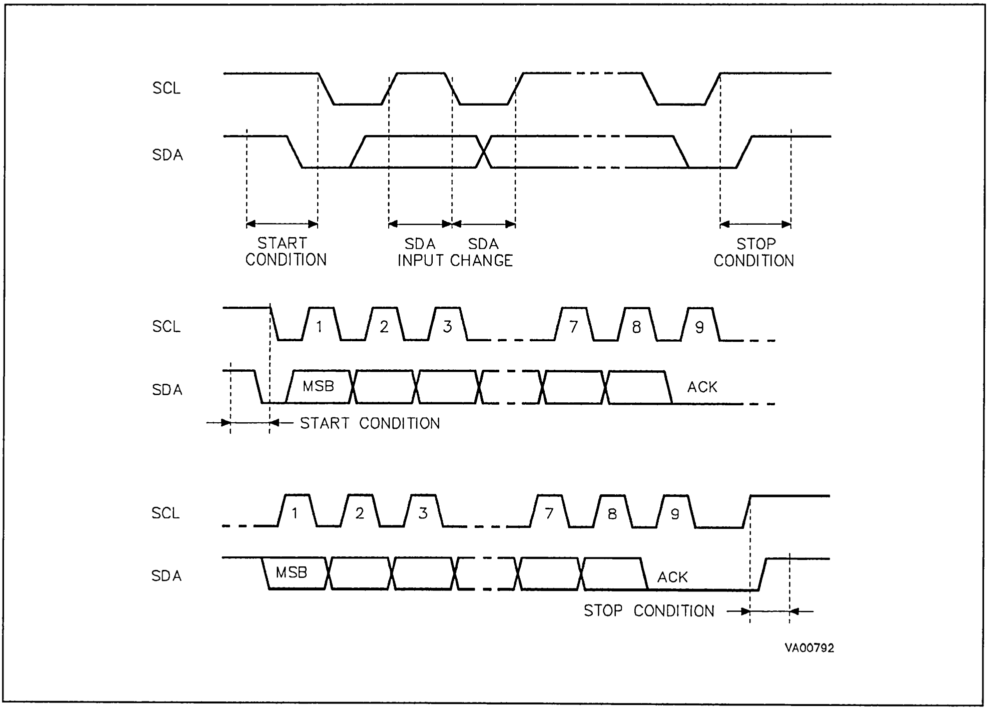

VCC
VCC
MODE
VCC
PRE
VSS
E
SCL
SDA
ST25C08
VSS
VA00865

Figure 5. I^{2}C Bus Protocol


SCL
SDA
START CONDITION
SDA INPUT
SDA CHANGE
STOP CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
START CONDITION
SCL
1
2
3
7
8
9
SDA
MSB
ACK
STOP CONDITION
VA00792

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 6. AC Testing Input Output Waveforms

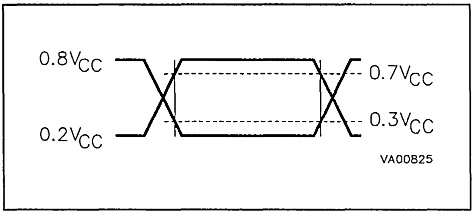

0.8VCC
0.2VCC
0.7VCC
0.3VCC
VA00825

Table 5. Capacitance [1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)		8	pF
C_{IN}	Input Capacitance (Other)		6	pF

Note: 1. Sampled only not 100% tested

Figure 7. AC Waveforms

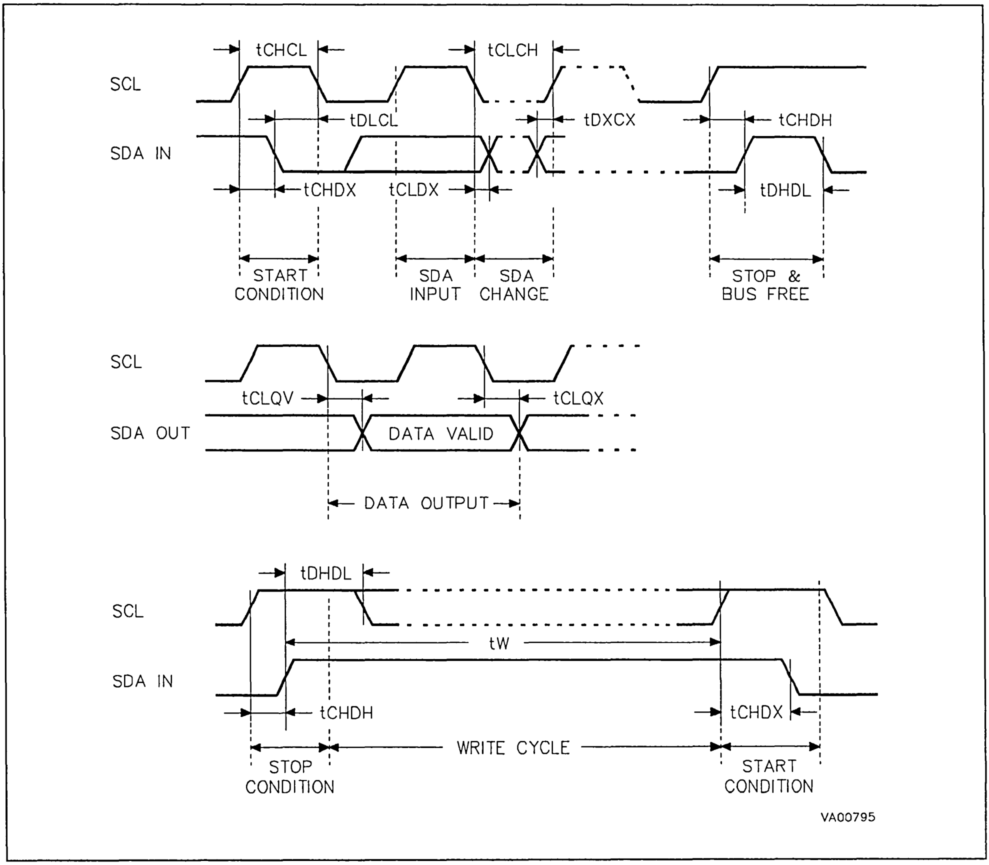

tCHCL
tCLCH
SCL
tDLCL
tDXCX
tCHDH
SDA IN
tCHDX
tCLDX
tDHDL
START CONDITION
SDA INPUT
SDA CHANGE
STOP & BUS FREE
SCL
tCLQV
tCLQX
SDA OUT
DATA VALID
DATA OUTPUT
tDHDL
SCL
tW
SDA IN
tCHDH
tCHDX
WRITE CYCLE
STOP CONDITION
START CONDITION
VA00795

Table 6. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±2	µA
I_{CC}	Supply Current	V_{CC} = 2.5V, f = 100kHz		1	mA
		V_{CC} = 5.5V, f = 100kHz		2	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 2.5V, V_{IN} = 0V or V_{CC}		5	µA
		V_{CC} = 5.5V, V_{IN} = 0V or V_{CC}		10	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL & SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E, PRE, MODE)		–0.3	0.5	V
V_{IH}	Input High Voltage (E, PRE, MODE)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD \cdot STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD.DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Output Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock High to Output Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{LPF}	T_I	Input Low Pass 1st Order Filter Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a re START condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive rows (upper 5 MSB must not change) the maximum programming time is doubled to 20ms.

Table 8. Endurance and Data Retention

Endurance	The ability of the EEPROM to withstand Erase/Write cycles without failure.
Failure	A failure after cycling is defined as any bit that cannot be written or loses its data after a subsequent retention bake of 2 years equivalent at 55 °C.
Guarantee	With 60% confidence, more than 99.9% of units can be cycled over 1,000,000 times.

SIGNAL DESCRIPTION (cont'd)

Chip Enable (E). This chip enable input is used to set the least significant bit of the 5 bit device select code. It may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL, compatible.

Mode (MODE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

Protect Enable (PRE). This signal may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. Note that the voltages are CMOS levels, not TTL, compatible.

DEVICE OPERATION

The ST25C08 supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST25C08 is always a slave device is all communications.

Communications Protocol

Data Transition or Change. Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP conditions.

Start Condition. START is identified by a high to low transition of the data bus SDA signal while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST25C08 continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the data bus SDA signal while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST25C08 and the bus master and forces the device into the standby power state.

Acknowledge Bit. An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST25C08 samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing

To start communication between the master and the slave ST25C08, the master must initiate a START condition. Following this the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code, block select bits and a READ or WRITE instruction.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For the ST25C08 these are fixed as 1010b (0Ah).

The following bit identifies the specific ST25C08 on the bus. It is matched to the chip enable signal E. Thus up to 2 ST25C08's can be connected on the same bus giving a memory capacity total of 16k bits. After a START condition all ST25C08's on the bus will identify the device code and compare the following bit to the chip enable inputs E. If a match is found the corresponding ST25C08 will acknowledge the identification on the SDA bus during the 9th bit time.

The 6th and 7th bits sent select one of the four blocks of 256 bytes of the memory, effectively acting as memory addresses A9 and A8 (A7 - A0 byte addresses are sent later).

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations.

DEVICE OPERATION (cont'd)

Write Operation

The Multibyte Write mode is available when the MODE signal is at V_{IH} and the Page Write mode when this signal is at V_{IL}. The MODE signal may be driven dynamically with CMOS input levels. The Byte Write mode is independant of the state of the MODE signal and the pin could be left floating if only this mode was to be used. However it is recommended that the signal is connected to either V_{IH} or V_{IL}.

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The ST25C08 acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes in the selected block of the memory. After receipt of the byte address the ST25C08 again responds with an acknowledge.

Byte Write. In the Byte Write mode the master sends one data byte, this is acknowledged by the ST25C08. The master then terminates the transfer by generating a STOP condition.

Multibyte Write. For the Multibyte mode the MODE signal must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the ST25C08. The transfer is terminated by the master generating a STOP condition.

Page Write. For the Page mode the MODE signal must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A9-A5) are the same.

The master sends from 1-16 bytes of data, which are each acknowledged by the ST25C08. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

For any write mode the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST25C08 will not respond to any request. The duration of this cycle is t_W = 10ms maximum except when, in the Multibyte Write mode, bytes are accessed that are on different rows (that is have different values for the 5 most significant address bits), when the programing time is doubled to a maximum of 20ms.

Read Operation

Read operations are independent of the state of the MODE signal.

Current Address Read. The ST25C08 has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $R\overline{W}$ bit set to '1'. The ST25C08 acknowledges this and immediately outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the byte address into the memory. This is followed by another START condition from the master and the byte address repeated with the $R\overline{W}$ bit set to '1'. The ST25C08 acknowledges this and immediately outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However in this case the master DOES acknowledge the data byte output and the ST25C08 continues to output the next byte in sequence. To terminate the stream of bytes the master must NOT acknowledge the last byte output, but must generate a STOP sequence. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of 1024 the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge In Read Mode. In all read modes the ST25C08 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST25C08 terminates the data transfer and switches to a receiver state. The STOP condition is used only in the WRITE modes to initiate the write cycle and is ignored in the READ modes.

Figure 8. Write Modes Sequence

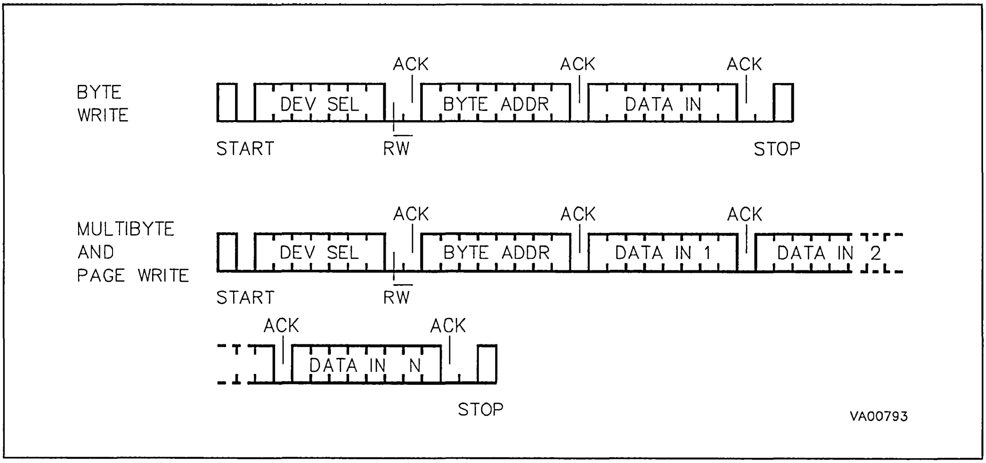
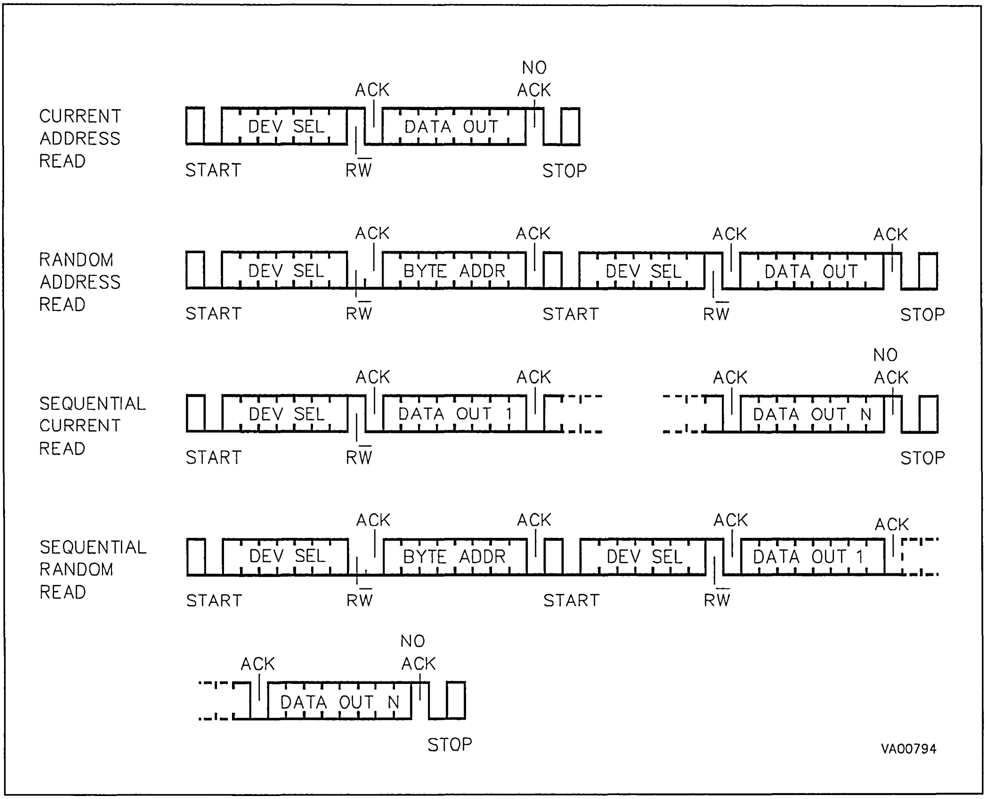

BYTE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN
START
RW
STOP
MULTIBYTE AND PAGE WRITE
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DATA IN 1
DATA IN 2
START
RW
ACK
ACK
DATA IN N
STOP
VA00793

Figure 9. Read Modes Sequence


CURRENT ADDRESS READ
ACK
NO ACK
DEV SEL
DATA OUT
START
RW
STOP
RANDOM ADDRESS READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT
START
RW
START
RW
STOP
SEQUENTIAL CURRENT READ
ACK
ACK
ACK
NO ACK
DEV SEL
DATA OUT 1
DATA OUT N
START
RW
STOP
SEQUENTIAL RANDOM READ
ACK
ACK
ACK
ACK
DEV SEL
BYTE ADDR
DEV SEL
DATA OUT 1
START
RW
START
RW
ACK
NO ACK
DATA OUT N
STOP
VA00794

ORDERING INFORMATION

Example: ST25C08 B 1

Package

B	PSDIP8 0.25 mm Frame

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Parts are shipped with the memory content set at all "1's" (0FFh).

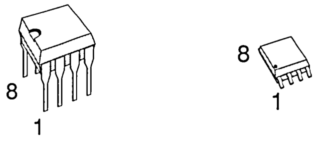
For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

MICROWIRE BUS EEPROM

SERIAL ACCESS CMOS 256 bit (16 x 16 or 32 x 8) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- DUAL ORGANISATION: 16 x 16 or 32 x 8
- BYTE/WORD AND CHIP PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

PSO8 (M)

DESCRIPTION

The ST93C06 is a 256 bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface.

The 256 bit memory is divided into either 16 x 16 bit words or 32 x 8 bit bytes. The organisation may be selected by a signal on the ORG input.

The memory is accessed by a set of instructions which includes Read, Write, Erase, Erase All and Write All. A Read instruction loads the address of the first word/byte to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the data is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

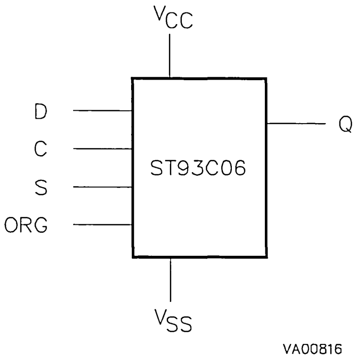
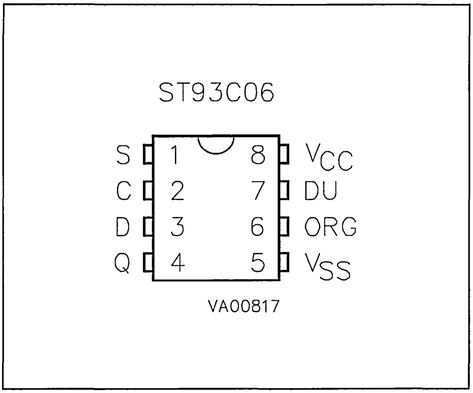
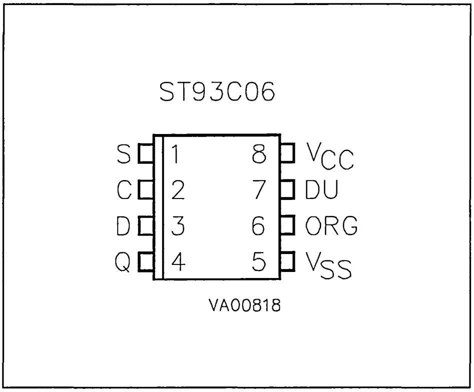


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

stream of data words/bytes. In this way the memory can be read as a continuous data stream from 16 to 256 bits long.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 or 8 bits at one time into one of the 16 words or 32 bytes. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

An internal feature of the ST93C06 provides Power-on Data Protection by inhibiting operation when the Supply is too low. This feature is particularly usefull when powering up the chip.

The design of the ST93C06 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to any voltage between V_{SS} and V_{CC}.

MEMORY ORGANISATION

The ST93C06 is organised as 16 words x 16 bits or 32 bytes x 8 bits. If the ORG input is left unconnected or connected to the Supply (V_{CC}) the x16 organisation is selected, when ORG is connected to Ground (V_{SS}) the x8 organisation is selected.

POWER-ON DATA PROTECTION

During power-up operations are inhibited until the Supply (V_{CC}) has reached a level between 2.5V and 3.5V. At power down operation in inhibited when the Supply falls to below between 3V and 2V.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

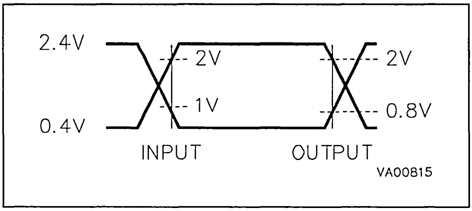


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		2	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	grade 1	100		ns
			grade 3 and 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

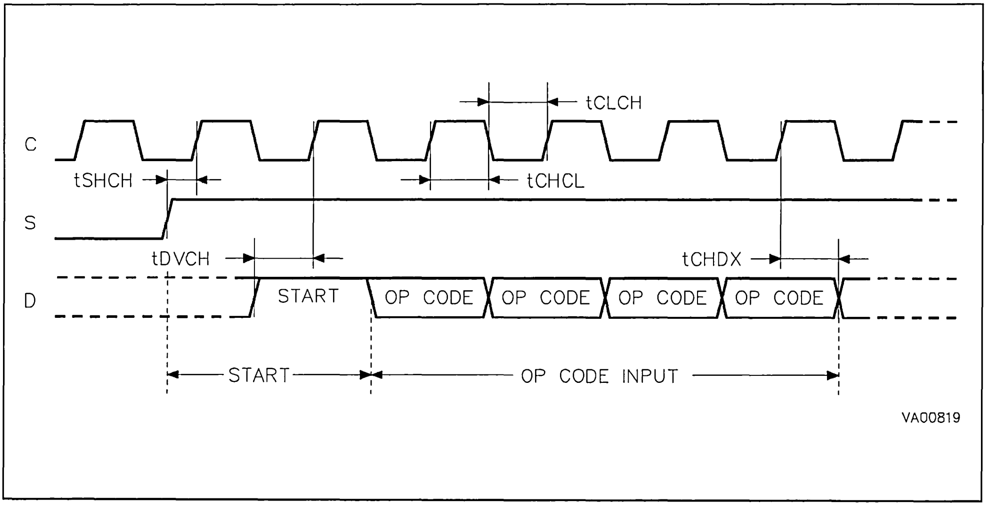
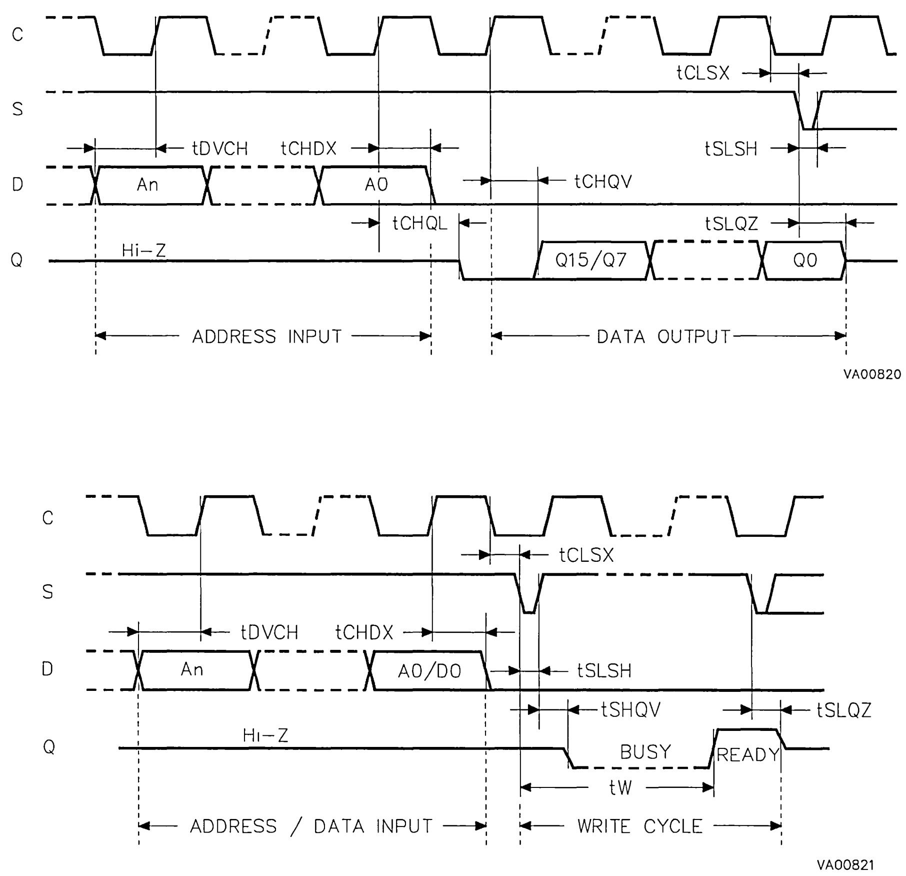


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi–Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
C
S
D
Q
tCLSX
tDVCH
tCHDX
An
A0/D0
tSLSH
tSHQV
tSLQZ
Hi–Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00821

INSTRUCTIONS

The ST93C06 has seven instructions which are shown in Table 3. The op-codes of the instructions are made up of 4 bits, preceded by a start bit which is always at logic '1'. Some instructions use only the first two bits and ignore the last two, others use all four bits to define the op-code. The op-code is followed by an address for the word/byte which is made up of four bits for the x16 organisation or five bits for the x8 organisation.

The start sequence starts with the Chip Select signal going High. The first clock pulse after Chip Select has gone High is ignored by the ST93C06, and the Data Input is sampled on the second and third Clock pulses. Even though the first clock pulse after Chip Select going High is ignored, it is recommended to establish the Data Input at Low during this first clock pulse in order to have the same timing reference as other ST93CXX series devices. A start condition is recognised when the Data Input is '1' and this synchronises the internal circuits of the memory.

Read

The Read instruction (READ) outputs serial data on the Data Output. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word or 8 bit byte with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word/byte as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words/bytes and a continuous stream of data can be read.

Erase/Write Enable and Disable

Programming instructions must be preceded by an Erase/Write Enable instruction (EWEN). When power is first applied to the ST93C06 programming is inhibited. When the EWEN instruction is executed programming remains enabled until an Erase/Write Disable instuction (EWDS) is executed or V_{CC} falls below the power-down threshold.

The EWDS instruction can be used to protect data against accidental disturbance by noise on the data busses. It should be used following all programming instructions.

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory word or byte bits to '1'. After the address the falling edge of the Chip Select starts a self-timed programming cycle. During the cycle the state of the Data Output signal indicates Busy('0') or Ready('1') after Chip Select is returned to High.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is made on the Low to High transition of the clock. After the last data bit has been input, Chip Select is brought Low to start the programming cycle. During the cycle the state of the Data Output signal indicates Busy('0') or Ready('1') after Chip Select is returned High.

Erase All

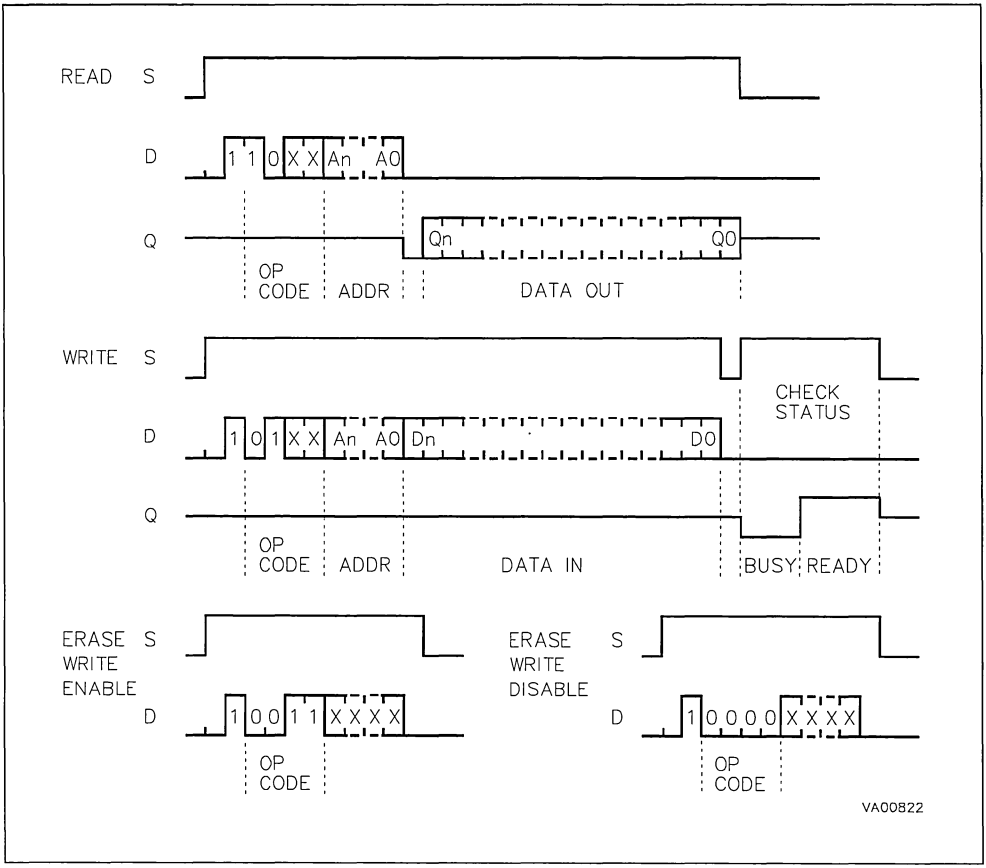
The Erase All instruction (ERAL) erases the whole memory. Using this instruction the entire memory content can be erased to '1'. A dummy address is

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address	Data	x16 Org Address	Data
READ	Read Data from memory	10XX	A4-A0	Q7-Q0	A3-A0	Q15-Q0
WRITE	Write Data to memory	01XX	A4-A0	D7-D0	A3-A0	D15-D0
EWEN	Erase/Write Enable	0011	X4-X0		X3-X0	
EWDS	Erase/Write Disable	0000	X4-X0		X3-X0	
ERASE	Erase Byte or Word	11XX	A4-A0		A3-A0	
ERAL	Erase All	0010	X4-X0		X3-X0	
WRAL	Write All with Data	0001	X4-X0	D7-D0	X3-X0	D15-D0

Note: X5-X0 or X4-X0 are dummy addresses

Figure 6. READ, WRITE, EWEN, EWDS Sequence


READ
S
D
1 1 0 X X An A0
Q
Qn Q0
OP CODE
ADDR
DATA OUT
WRITE
S
CHECK STATUS
D
1 0 1 X X An A0 Dn D0
Q
OP CODE
ADDR
DATA IN
BUSY
READY
ERASE WRITE ENABLE
S
D
1 0 0 1 1 X X X X
OP CODE
ERASE WRITE DISABLE
S
D
1 0 0 0 0 X X X X
OP CODE
VA00822

INSTRUCTION (cont'd)

input during the instruction transfer and the erase is made in the same way as the ERASE instruction above.

Write All

The Write All instruction (WRAL) writes the Data Input word or byte to all addresses of the memory. In the WRAL instruction NO automatic erase is made so all words/bytes must be erased before the WRAL instruction. So for correct operation an ERAL instruction should be used before the WRAL instruction.

Busy/Ready Status

During every programming cycle (after a Write, Erase, Write All or Erase All instruction) the Data Output indicates the Busy/Ready status of the memory. The output is available after the Chip Select is returned to High. A '0' indicates Busy and a '1' Ready. A '1' indicates that the word/byte at the location addressed, or all of the memory for ERAL and WRAL instructions, has been programmed and the memory is ready for another instruction. After the memory is ready, the Data Output '1' will disappear when a new start bit is input or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, please refer to the SGS-THOMSON application note "EEPROM Common I/O Operation".

Figure 7. ERASE, ERAL Sequence

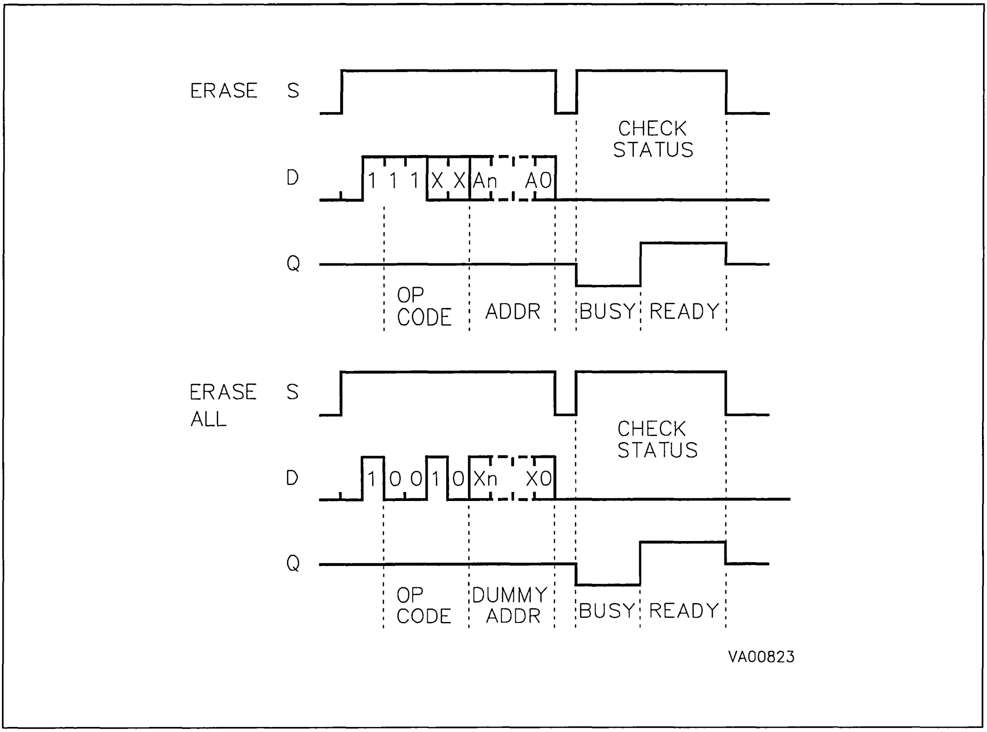
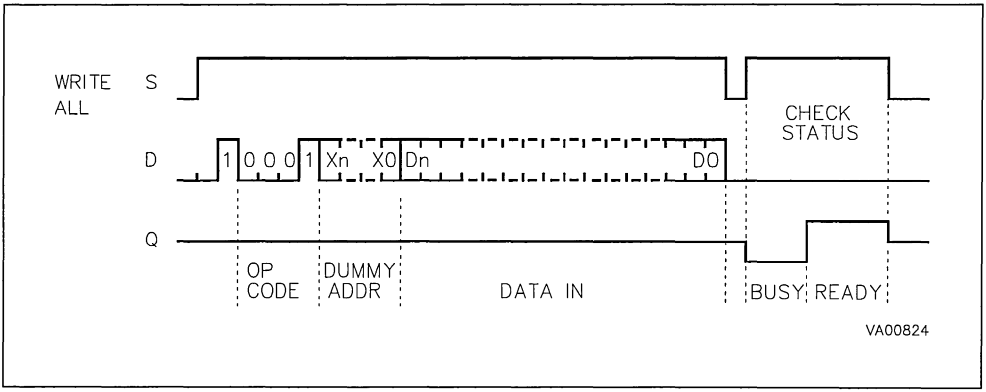

ERASE
S
D
Q
1 1 1 X X An A0
CHECK STATUS
OP CODE
ADDR
BUSY
READY
ERASE ALL
S
D
Q
1 0 0 1 0 Xn X0
CHECK STATUS
OP CODE
DUMMY ADDR
BUSY
READY
VA00823

Figure 8. WRAL Sequence


WRITE ALL
S
D
Q
1 0 0 0 1 Xn X0 Dn D0
CHECK STATUS
OP CODE
DUMMY ADDR
DATA IN
BUSY
READY
VA00824

ORDERING INFORMATION

Example: ST93C06 M 1 013TR

Package

B	PSDIP8 0.4 mm Frame
M	PSO8

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option

013TR	Tape & Reel

Parts are shipped with the memory content set at all “1’s” (0FFFFh for x16, 0FFh for x8).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

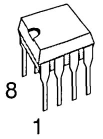
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

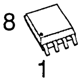
ST93C46A
ST93C46T

SERIAL ACCESS CMOS 1K bit (64 x 16 or 128 x 8) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- DUAL ORGANISATION: 64 x 16 or 128 x 8
- BYTE/WORD AND CHIP PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame



PSO8 (M)

DESCRIPTION

The ST93C46 is a 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface.

The 1K bit memory is divided into either 64 x 16 bit words or 128 x 8 bit bytes. The organisation may be selected by a signal on the ORG input.

The memory is accessed by a set of instructions which includes Read, Write, Erase, Erase All and Write All. A Read instruction loads the address of the first word/byte to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the data is output and it is possible, if the Chip

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

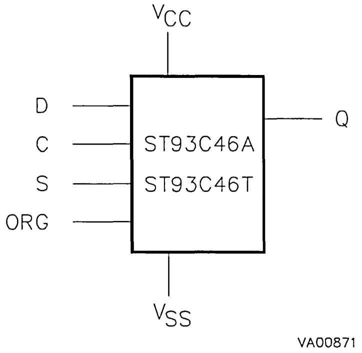
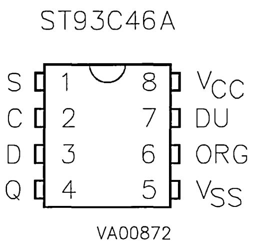


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	2000	V

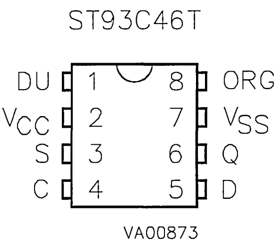
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2A. DIP Pin Connections



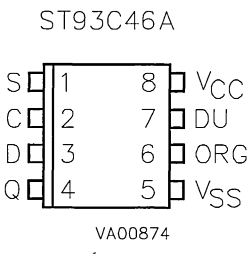
Warning: DU = Don’t Use

Figure 2B. DIP, 90° Turn, Pin Connections



Warning: DU = Don’t Use

Figure 2C. SO Pin Connections



Warning: DU = Don’t Use

DESCRIPTION (cont’d)

Select input is held High, to output a sequential stream of data words/bytes. In this way the memory can be read as a continuous data stream from 16 to 1024 bits long.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 or 8 bits at one time into one of the 64 words or 128 bytes. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

An internal feature of the ST93C46 provides Power-on Data Protection by inhibiting operation when the Supply is too low. This feature is particularly usefull when powering up the chip.

DESCRIPTION (cont'd)

The design of the ST93C46 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to any voltage between V_{SS} and V_{CC}.

MEMORY ORGANISATION

The ST93C46 is organised as 64 words x 16 bits or 128 bytes x 8 bits. If the ORG input is left unconnected or connected to the Supply (V_{CC}) the x16 organisation is selected, when ORG is connected to Ground (V_{SS}) the x8 organisation is selected.

POWER-ON DATA PROTECTION

During power-up, operations are inhibited until the Supply (V_{CC}) has reached a level between 2.5V and 3.5V. At power down operation in inhibited when the Supply falls to below between 3V and 2V.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

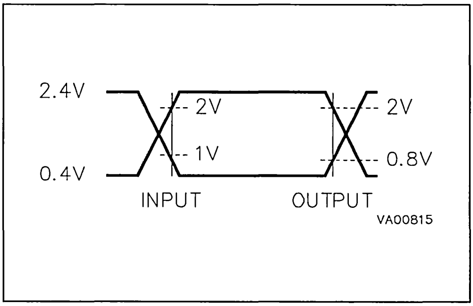


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	grade 1	100		ns
			grade 3 and 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

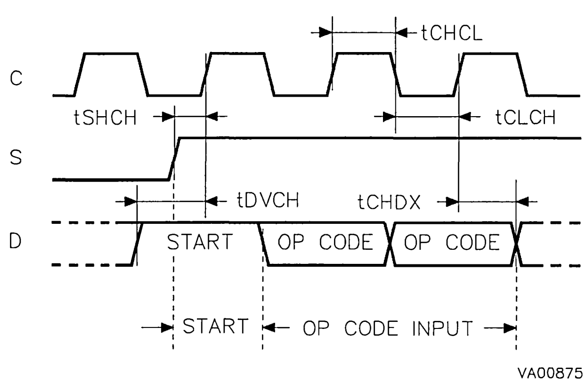
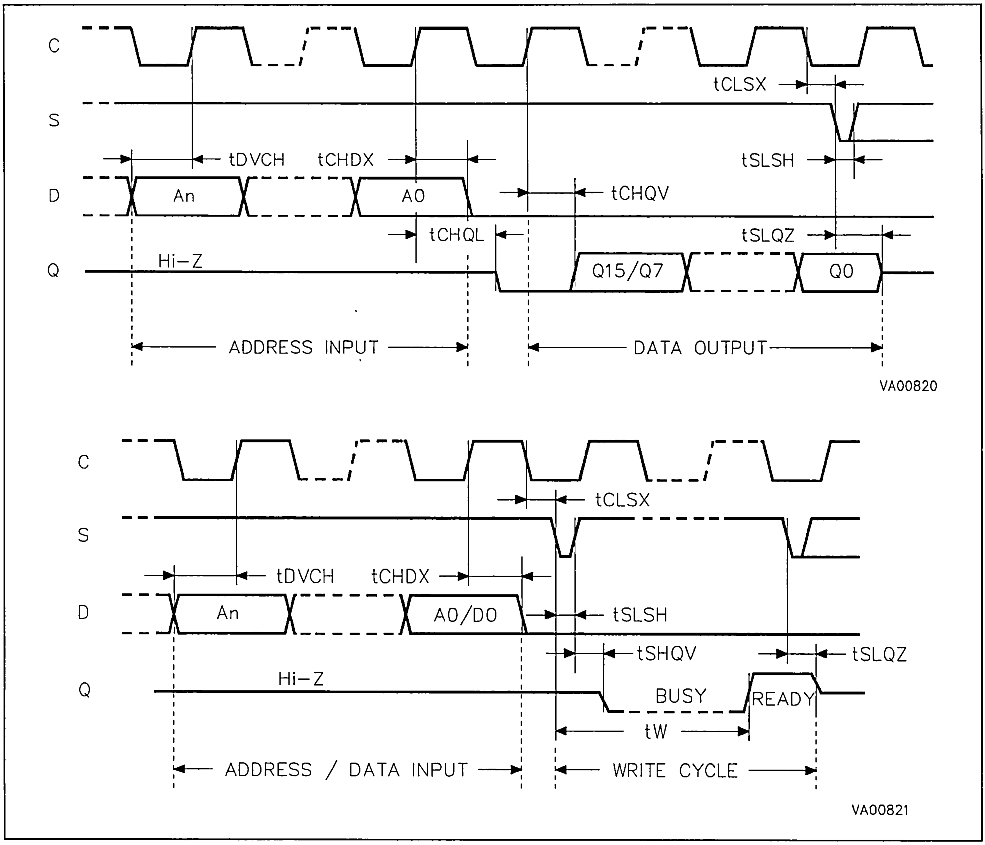


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi-Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
C
S
D
Q
tCLSX
tDVCH
tCHDX
An
A0/D0
tSLSH
tSHQV
tSLQZ
Hi-Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00821

INSTRUCTIONS

The ST93C46 has seven instructions which are shown in Table 3. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word/byte which is made up of six bits for the x16 organisation or seven bits for the x8 organisation.

The start sequence requires the Chips Select and Data Input signals to be set up before a Low to High transition of the Clock.

Read

The Read instruction (READ) outputs serial data on the Data Output. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word or 8 bit byte with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word/byte as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words/bytes and a continuous stream of data can be read.

Erase/Write Enable And Disable

Programming instructions must be preceded by an Erase/Write Enable instruction (EWEN). When power is first applied to the ST93C46 programming is inhibited. When the EWEN instruction is executed programming remains enabled until an Erase/Write Disable instuction (EWDS) is executed or V_{CC} falls below the power-down threshold.

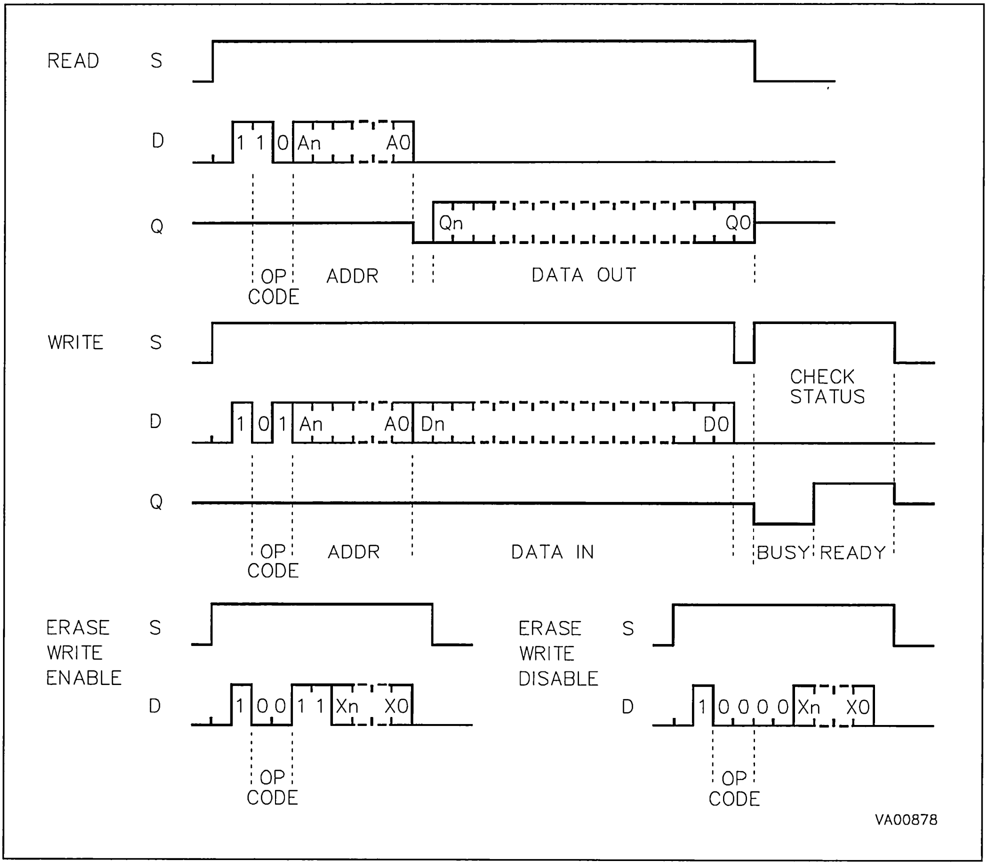
The EWDS instruction can be used to protect data against accidental disturbance by noise on the data busses. It should be used following all programming instructions.

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address	Data	x16 Org Address	Data
READ	Read Data from memory	10	A6-A0	Q7-Q0	A5-A0	Q15-Q0
WRITE	Write Data to memory	01	A6-A0	D7-D0	A5-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXXXX		11XXXX	
EWDS	Erase/Write Disable	00	00XXXXX		00XXXX	
ERASE	Erase Byte or Word	11	A6-A0		A5-A0	
ERAL	Erase All	00	10XXXXX		10XXXX	
WRAL	Write All with Data	00	01XXXXX	D7-D0	01XXXX	D15-D0

Note: X = dummy address bit.

Figure 6. READ, WRITE, EWEN, EWDS Sequence


READ
S
D
1 1 0 An A0
Q
Qn Q0
OP CODE
ADDR
DATA OUT
WRITE
S
CHECK STATUS
D
1 0 1 An A0 Dn D0
Q
OP CODE
ADDR
DATA IN
BUSY
READY
ERASE WRITE ENABLE
S
D
1 0 0 1 1 Xn X0
OP CODE
ERASE WRITE DISABLE
S
D
1 0 0 0 0 Xn X0
OP CODE
VA00878

INSTRUCTIONS (cont'd)

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory word or byte bits to '1'. After the address the falling edge of the Chip Select starts a self-timed programming cycle. During the cycle the state of the Data Output signal indicates Busy('0') or Ready('1') after Chip Select is returned to High.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is made on the Low to High transition of the clock. After the last data bit has been input, Chip Select is brought Low to start the programming cycle. During the cycle the state of the Data Output signal indicates Busy('0') or Ready('1') after Chip Select is returned High.

Erase All

The Erase All instruction (ERAL) erases the whole memory. Using this instruction the entire memory content can be erased to '1'. A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction above.

Write All

Thi Write All instruction (WRAL) writes the Data Input word or byte to all addresses of the memory. In the WRAL instruction NO automatic erase is made so all words/bytes must be erased before the WRAL instruction. So for correct operation an ERAL instruction should be used before the WRAL instruction.

Busy/Ready Status

During every programming cycle (after a WRITE, Erase, Write All or Erase All instruction) the Data Output indicate the Busy/Ready status of the memory. The output is available after the Chip Select is returned to High. A '0' indicates Busy and a '1' Ready. A '1' indicates that the word/byte at the location addressed, or all of the memory for ERAL and WRAL instructions, has been programmed and the memory is ready for another instruction. After the memory is ready, the Data Output '1' will disappear when a new start bit is input or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, please refer to the SGS-THOMSON application note "EEPROM Common I/O Operation".

Figure 7. ERASE, ERAL Sequence

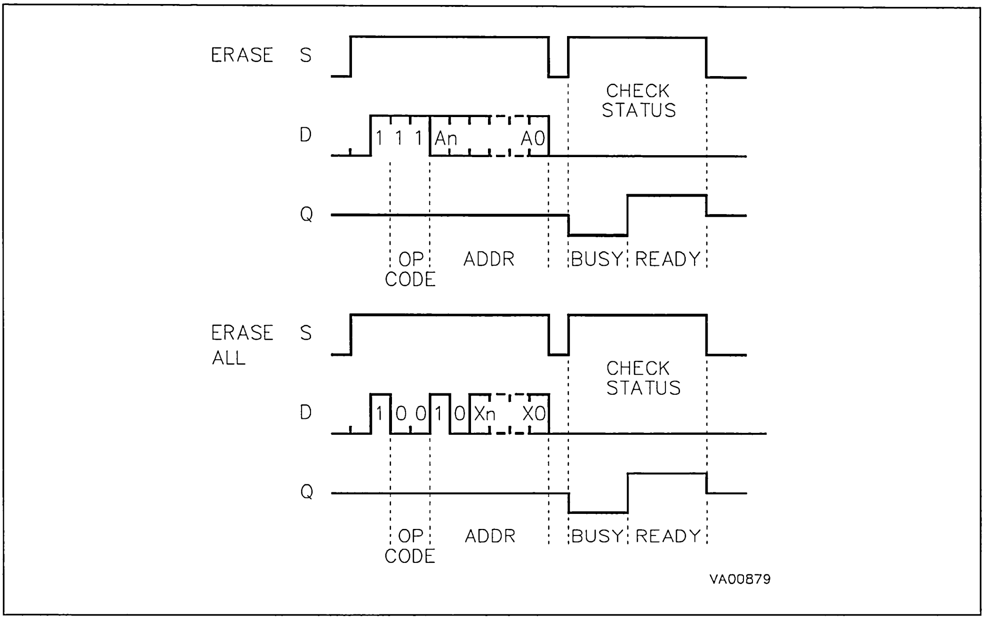
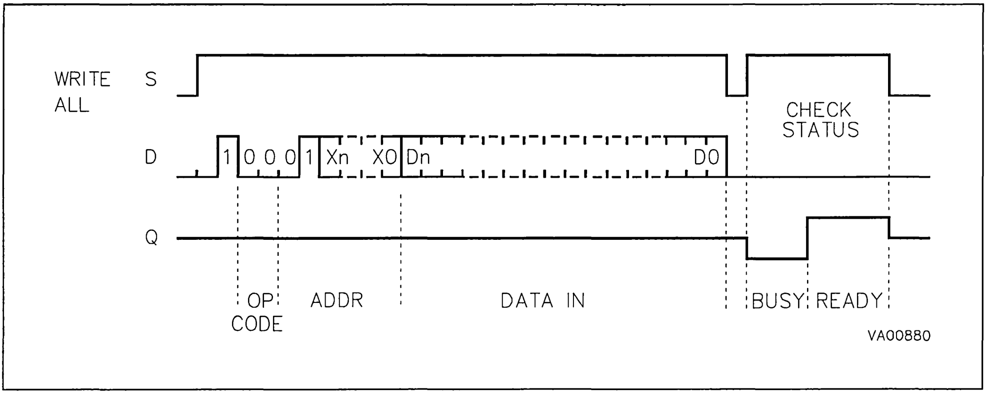


Figure 8. WRAL Sequence


WRITE ALL
S
D
Q
1 0 0 0 1 Xn X0 Dn D0
CHECK STATUS
OP CODE
ADDR
DATA IN
BUSY
READY
VA00880

ORDERING INFORMATION

Example: ST93C46 A M 1 013TR

Suffix

A	Standard pin out
T	90° Turn pin out

Package

B	PSDIP8 0.4 mm Frame
M	PSO8

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option

013TR	Tape & Reel

Parts are shipped with the memory content set at all "1's" (0FFFFh for x16, 0FFh for x8).

For a list of available options of Package and Temperature Range, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

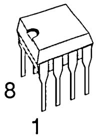
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

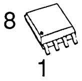
ST93C56

SERIAL ACCESS CMOS 2K bit (128 x 16 or 256 x 8) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- DUAL ORGANISATION: 128 x 16 or 256 x 8
- BYTE/WORD AND CHIP PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame



PSO8 (M)

DESCRIPTION

The ST93C56 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface.

The 2K bit memory is divided into either 128 x 16 bit words or 256 x 8 bit bytes. The organisation may be selected by a signal on the ORG input.

The memory is accessed by a set of instructions which includes Read, Write, Erase, Erase All and Write All. A Read instruction loads the address of the first word/byte to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the data is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

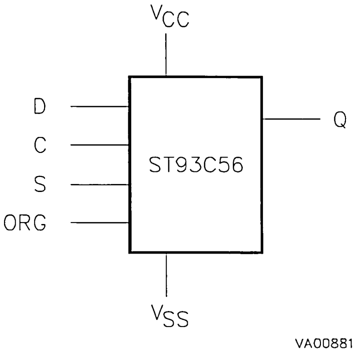
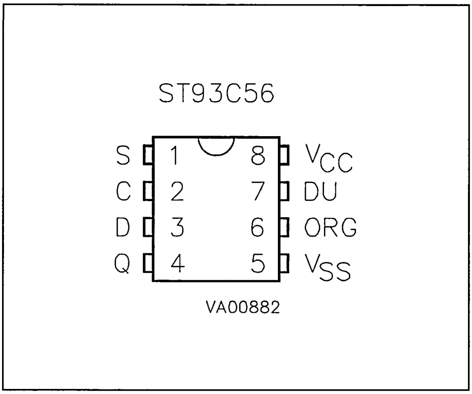
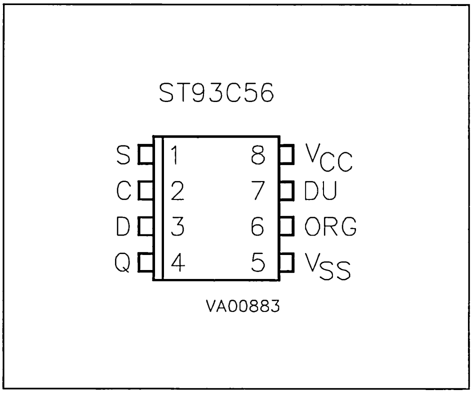


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DESCRIPTION (cont'd)

stream of data words/bytes. In this way the memory can be read as a continuous data stream from 16 to 2048 bits long.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 or 8 bits at one time into one of the 128 words or 256 bytes. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

An internal feature of the ST93C56 provides Power-on Data Protection by inhibiting operation when the Supply is too low. This feature is particularly usefull when powering up the chip.

The design of the ST93C56 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

The DU (don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to any voltage between V_{SS} and V_{CC}.

MEMORY ORGANISATION

The ST93C56 is organised as 128 words x 16 bits or 256 bytes x 8 bits. If the ORG input is left unconnected or connected to the Supply (V_{CC}) the x16 organisation is selected, when ORG is connected to Ground (V_{SS}) the x8 organisation is selected.

POWER-ON DATA PROTECTION

During power-up, operations are inhibited until the Supply (V_{CC}) has reached a level between 2.5V and 3.5V. At power down operation in inhibited when the Supply falls to below between 3V and 2V.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

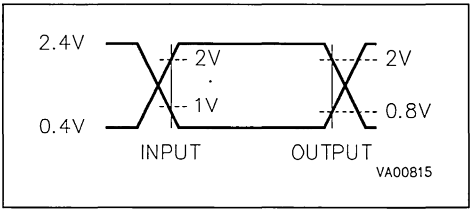


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T$_A$ = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V$_{CC}$ = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	grade 1	100		ns
			grade 3 and 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

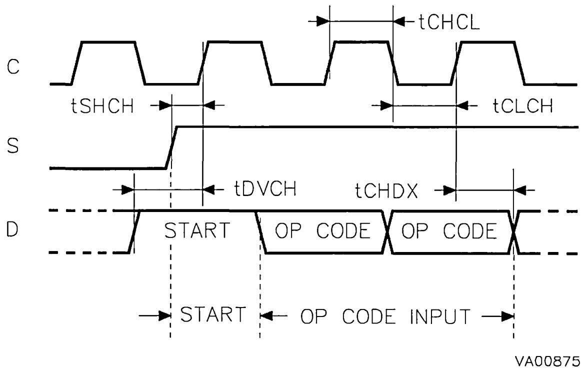
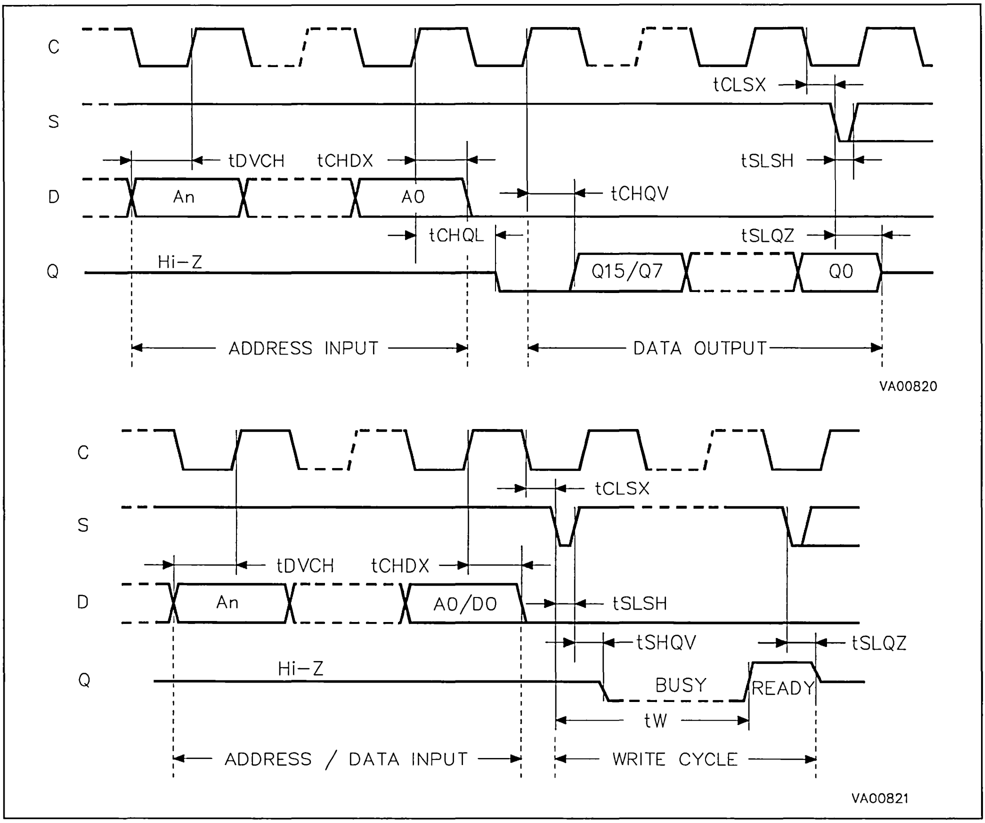


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi-Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
C
S
D
Q
tCLSX
tDVCH
tCHDX
An
A0/D0
tSLSH
tSHQV
tSLQZ
Hi-Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00821

INSTRUCTIONS

The ST93C56 has seven instructions which are shown in Table 6. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word/byte which is made up of seven bits for the x16 organisation or eight bits for the x8 organisation.

The start sequence requires the Chips Select and Data Input signals to be set up before a Low to High transition of the Clock.

Read

The Read instruction (READ) outputs serial data on the Data Output. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word or 8 bit byte with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word/byte as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words/bytes and a continuous stream of data can be read.

Erase/Write Enable and Disable

Programming instructions must be preceded by an Erase/Write Enable instruction (EWEN). When power is first applied to the ST93C56 programming is inhibited. When the EWEN instruction is executed programming remains enabled until an Erase/Write Disable instuction (EWDS) is executed or V_{CC} falls below the power-down threshold.

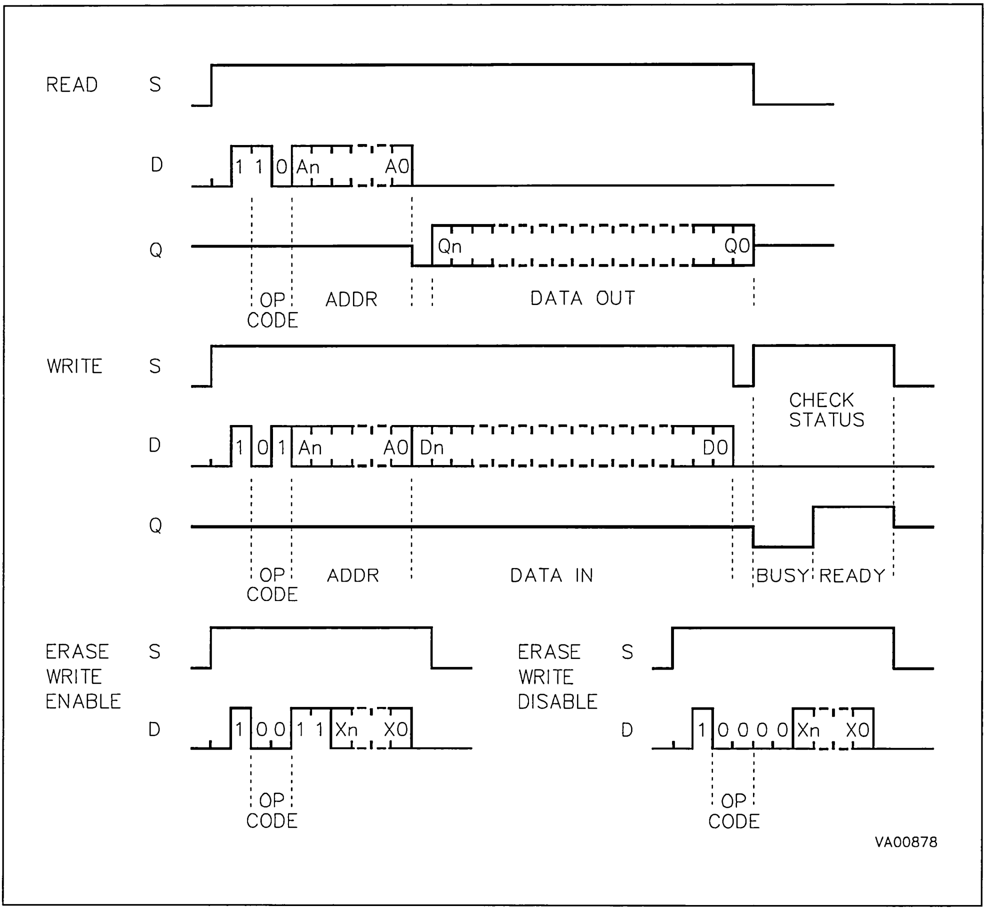
The EWDS instruction can be used to protect data against accidental disturbance by noise on the data busses. It should be used following all programming instructions.

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address	Data	x16 Org Address	Data
READ	Read Data from memory	10	A8-A0	Q7-Q0	A7-A0	Q15-Q0
WRITE	Write Data to memory	01	A8-A0	D7-D0	A7-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXXXX		11XXXX	
EWDS	Erase/Write Disable	00	00XXXXX		00XXXX	
ERASE	Erase Byte or Word	11	A8-A0		A7-A0	
ERAL	Erase All	00	10XXXXX		10XXXX	
WRAL	Write All with Data	00	01XXXXX	D7-D0	01XXXX	D15-D0

Note: X = dummy address bit.

Figure 6. READ, WRITE, EWEN, EWDS Sequence


READ
S
D
1 1 0 An A0
Q
Qn Q0
OP CODE
ADDR
DATA OUT
WRITE
S
D
1 0 1 An A0 Dn D0
CHECK STATUS
Q
OP CODE
ADDR
DATA IN
BUSY READY
ERASE WRITE ENABLE
S
D
1 0 0 1 1 Xn X0
OP CODE
ERASE WRITE DISABLE
S
D
1 0 0 0 0 Xn X0
OP CODE
VA00878

INSTRUCTIONS (cont'd)

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory word or byte bits to '1'. After the address the falling edge of the Chip Select starts a self-timed programming cycle. During the cycle the state of the Data Output signal indicates Busy('0') or Ready('1') after Chip Select is returned to High.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is made on the Low to High transition of the clock. After the last data bit has been input, Chip Select is brought Low to start the programming cycle. During the cycle the state of the Data Output signal indicates Busy('0') or Ready('1') after Chip Select is returned High.

Erase All

The Erase All instruction (ERAL) erases the whole memory. Using this instruction the entire memory content can be erased to '1'. A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction above.

Write All

The Write All instruction (WRAL) writes the Data Input word or byte to all addresses of the memory. The WRAL instruction works in the same way as WRITE and does not require a previous ERAL instruction.

Busy/Ready Status

During every programming cycle (after a Write, Erase, Write All or Erase All instruction) the Data Output indicates the Busy/Ready status of the memory. The output is available after the Chip Select is returned to High. A '0' indicates Busy and a '1' Ready. A '1' indicates that the word/byte at the location addressed, or all of the memory for ERAL and WRAL instructions, has been programmed and the memory is ready for another instruction. After the memory is ready, the Data Output '1' will disappear when a new start bit is input or the Chip Select is brought Low.

Common I/O Operation

The Data Output (Q) and Data Input (D) signals can be connected together to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, please refer to the SGS-THOMSON application note "EEPROM Common I/O Operation".

Figure 7. ERASE, ERAL Sequence

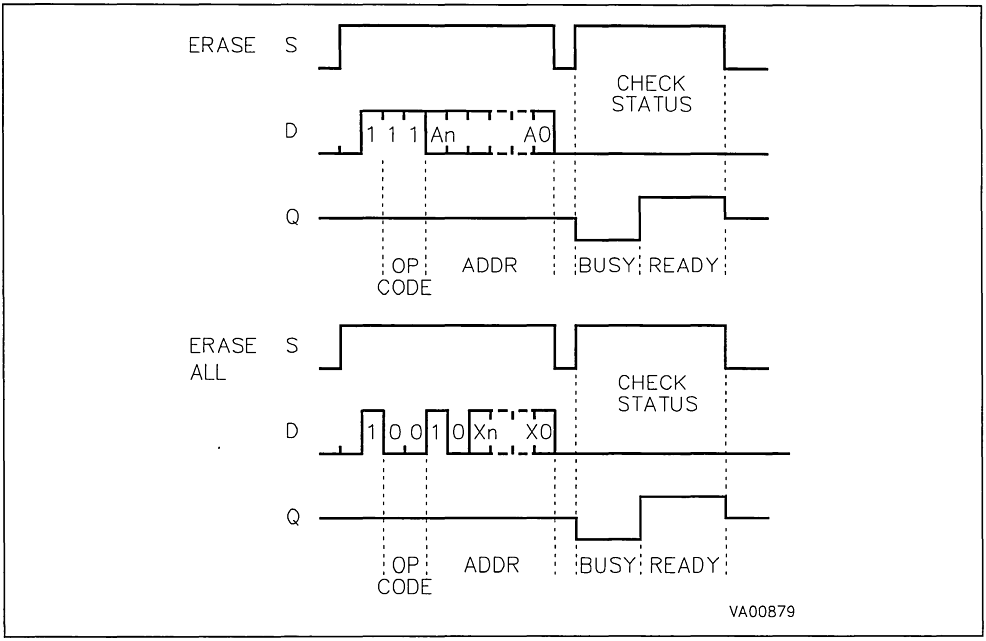
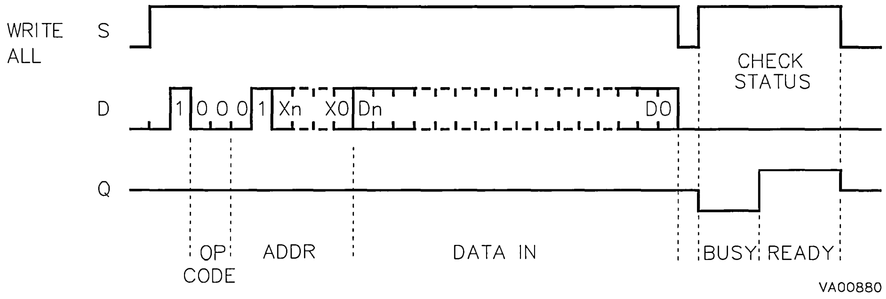
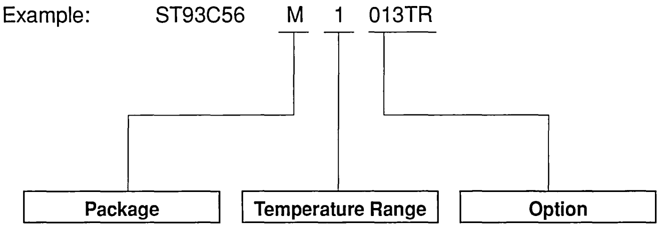


Figure 8. WRAL Sequence


WRITE ALL
S
D
Q
1
0 0 0
1
Xn
X0
Dn
D0
CHECK STATUS
OP CODE
ADDR
DATA IN
BUSY
READY
VA00880

ORDERING INFORMATION



Example: ST93C56 M 1 013TR

Package		Temperature Range		Option	
B	PSDIP8 0.4 mm Frame	1	0 to 70 °C	013TR	Tape & Reel
M	PSO8	3	–40 to 125 °C		
		6	–40 to 85 °C		

Parts are shipped with the memory content set at all “1’s” (0FFFFh for x16, 0FFh for x8).

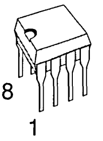
For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

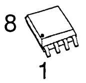
ST93CS46

SERIAL ACCESS CMOS 1K bit (64 x 16) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V SUPPLY VOLTAGE
- USER DEFINED WRITE PROTECT AREA
- PAGE WRITE MODE (4 WORDS)
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame



PSO8 (M)

DESCRIPTION

The ST93CS46 is a 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface. The 1K bit memory is organised as 64 x 16 bit words.

The memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to manage memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the word is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

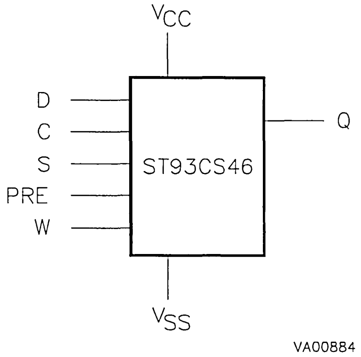


Figure 2A. DIP Pin Connections

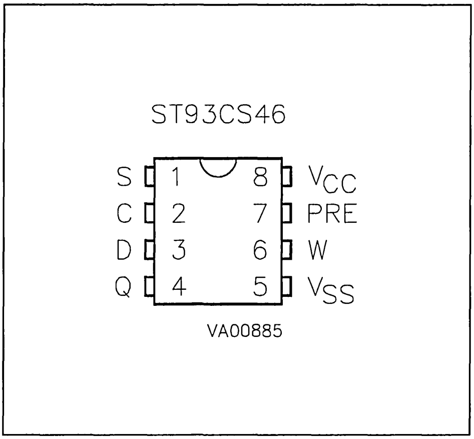


Figure 2B. SO Pin Connections

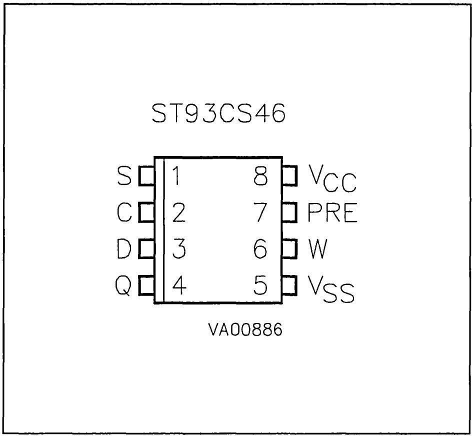


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages		–0.3 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)		2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

stream of data words. In this way the memory can be read as a continuous data stream from 16 to 1024 bits long. Up to 4 words may be written in a single program cycle using the Page Write instruction. The memory may be 'erased', or set to a predetermined pattern, by using the Write All instruction. An external siganl controls Write Enable. A user defined area of the memory may be write protected. An external signal (PRE) enables access to the Protect Register which stores the lowest address to be write protected. Data may be permanently protected by programming an OTP bit which prevents further changes to the write protect starting address and the protect flag.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 bits at one time into one of the 64 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, both providing that all addresses are outside the write protect area. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

The design of the ST93CS46 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

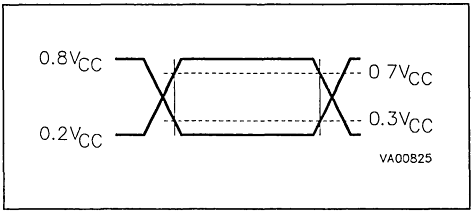


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
V_{IH}	Input High Voltage	$4.5V \le V_{CC} \le 5.5V$	2	V_{CC} + 1	V
V_{IL}	Input Low Voltage	$3V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage	$3V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	grade 1	100		ns
		Clock High to Input Transition	grade 3 and 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

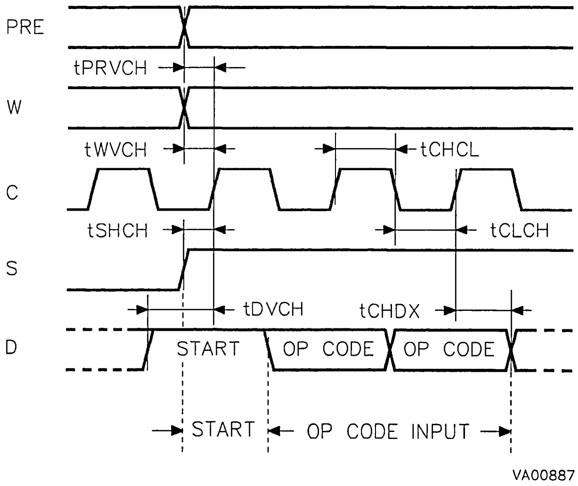
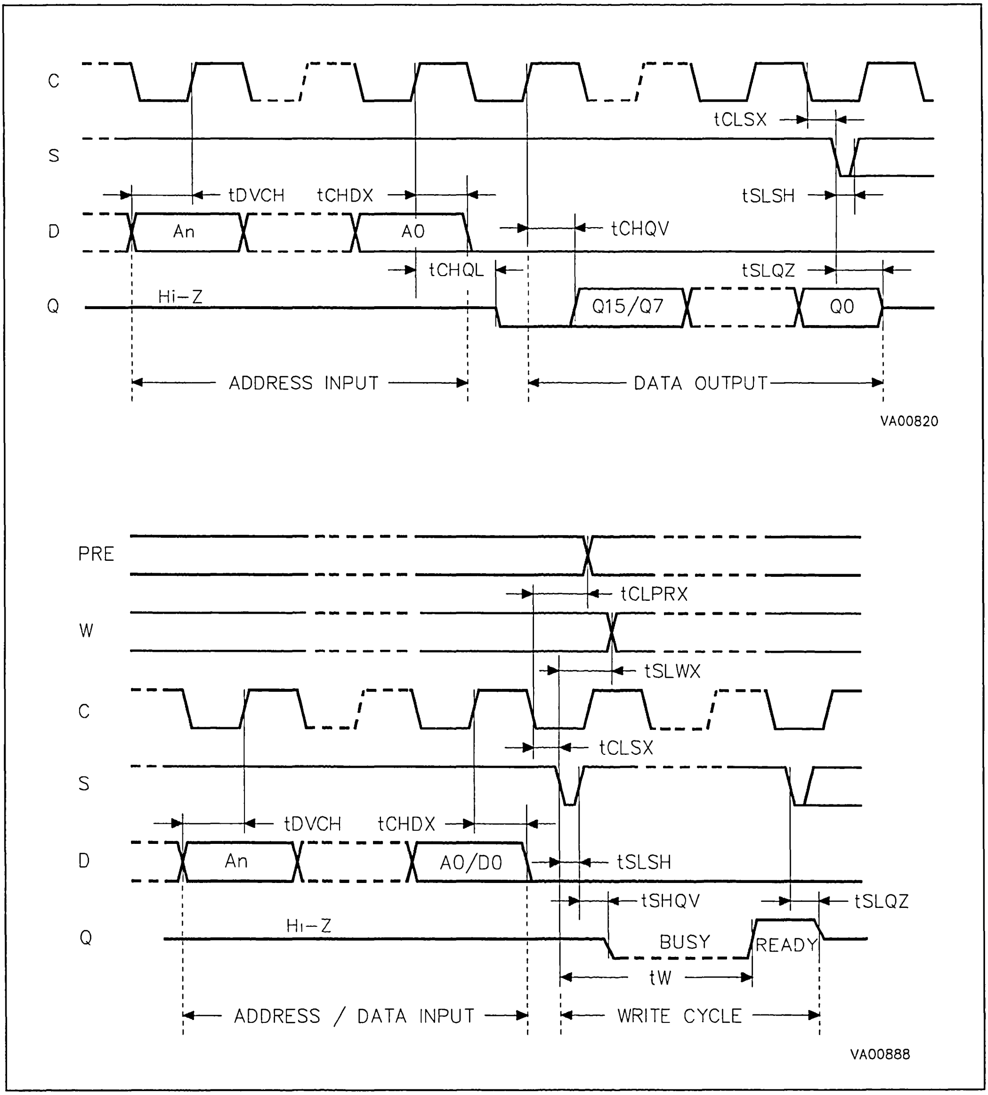


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi-Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
PRE
W
C
S
D
Q
tCLPRX
tSLWX
tCLSX
tDVCH
tCHDX
An
A0/D0
tSLSH
tSHQV
tSLQZ
Hi-Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00888

INSTRUCTIONS

The ST93CS46 has eleven instructions which are shown in Table 6. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word which is made up of six bits A5-A0.

The start sequence requires the Chip Select and Data Input signals to be set up before a Low to High transition of the Clock. For write instructions the Write Enable signal (W) must be High and for Protect Register instructions the Protect Register Enable signal (PRE) must also be High.

Read

The Read instruction (READ) outputs serial data on the Data Output Q. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable

When power is first applied to the ST93CS46 write operations are disabled. To enable write operations the Write Enable signal (W) must be High and a Write Enable instruction (WEN) must be executed. After the WEN instruction write operation remains enabled until either a Write Disable instruction (WDS) is executed or the supply is removed from the device.

Write

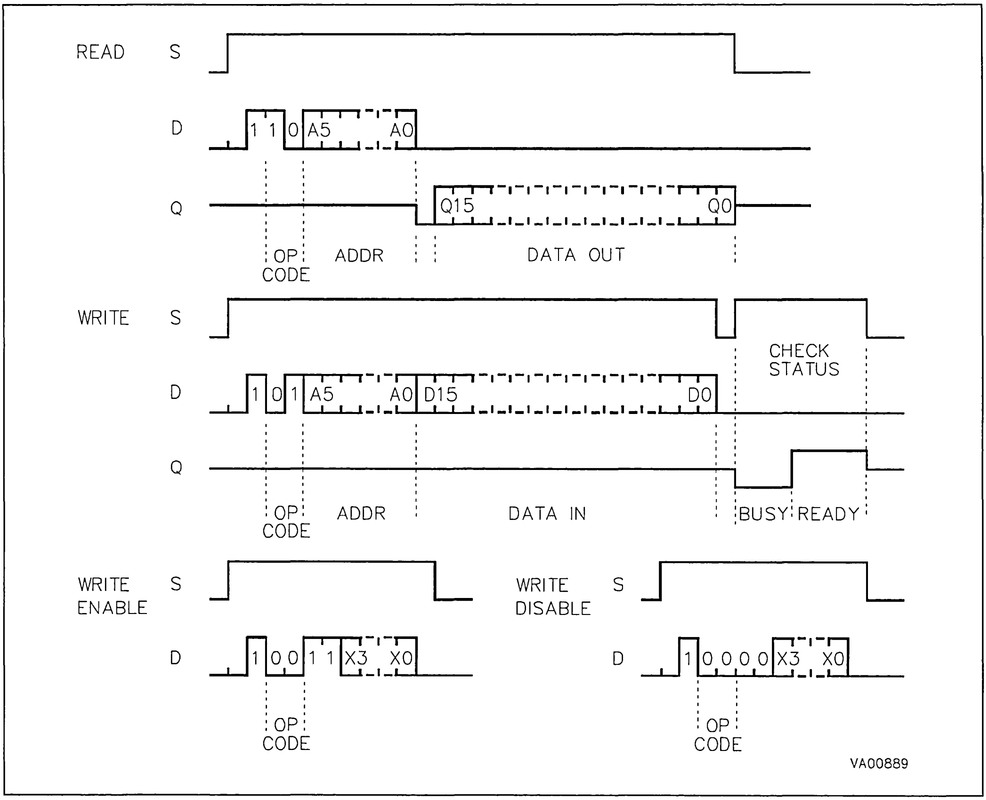
A Write instruction (WRITE) contains the address followed by the data to be written. The Write Enable signal (W) must be High before and during the WRITE instruction, but is subsequently ignored (don't care). Input address and data are read on

Table 6. Instruction Set

Instruction	Description	Op Code	PRE	W	Address	Data	Additional Information
READ	Read Data from memory	10	'0'	X	A5-A0	Q15-Q0	
WRITE	Write Data to memory	01	'0'	'1'	A5-A0	D15-D0	Write if address unprotected
PAWRITE	Page Write to memory	11	'0'	'1'	A5-A0	D15-D0	Write one to 4 words, if all addresses are unprotected
WRALL	Write All	00	'0'	'1'	01XXXX	D15-D0	Write all if Protect Register cleared
WEN	Write Enable	00	'0'	'1'	11XXXX		
WDS	Write Disable	00	'0'	'1'	00XXXX		
PRREAD	Protect Register Read	10	'1'	X	XXXXXX	Q6-Q0	Data Output is Protect Address (A5-A0) plus Protect Flag
PRWRITE	Protect Register Write	01	'1'	'1'	A5-A0		Data above A5-A0 is protected
PRCLEAR	Protect Register Clear	11	'1'	'1'	111111		Protect Flag also cleared ('1')
PREN	Protect Register Enable	00	'1'	'1'	11XXXX		
PRDS	Protect Register Disable	00	'1'	'1'	000000		OTP Flag set, prevents any further change to Protect Register

Note: X = don't care or drummy address bit.

Figure 6. READ, WRITE, WEN, WDS Sequence



INSTRUCTIONS (cont'd)

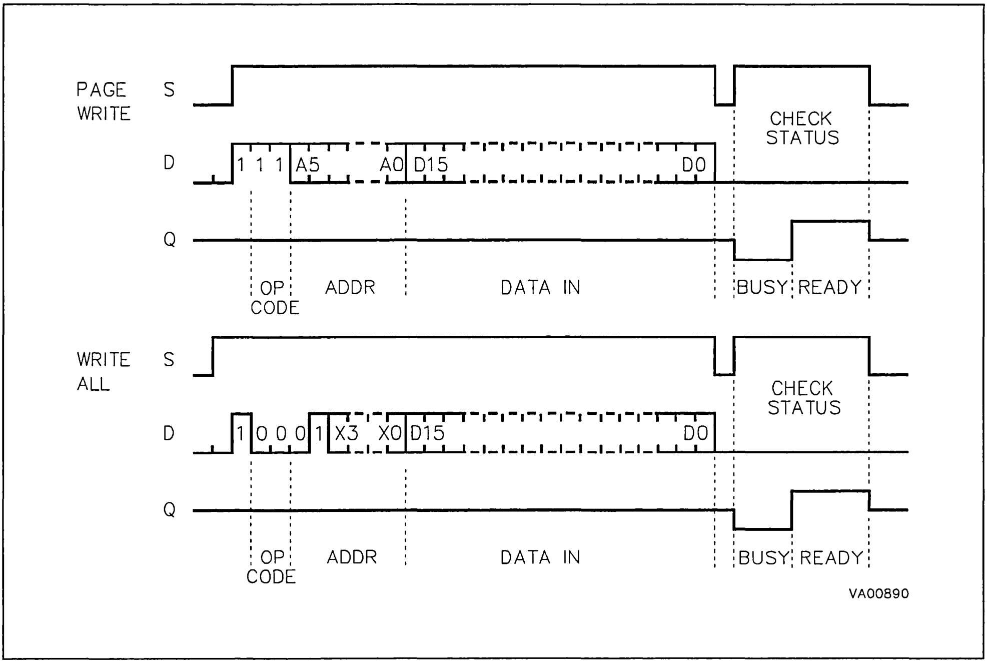
the Low to High transition of the clock. After the LSB of data has been received, the Chip Select signal (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle, providing that the address is NOT in the protected area. If Chip Select (S) is brought High again after a minimum time of tSLSH then the Data Output (D) will indicate the Busy/Ready status. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the receipt of each data word bits A1-A0 of the internal address register are incremented, the high order bits A5-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The write operation will proceded only if NONE of the addresses of the 1-4 data words has its address bits A5-A2 within the protected area. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Figure 7. PRWRITE, WRALL Sequence



INSTRUCTIONS (cont'd)

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes all memory locations with the data word included in the instruction. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. During the write cycle, the Data Output indicates Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write Disable

The Write Disable instruction (WDS) disables all write operations. It should be used after all write instructions to disable writing to the memory and provide protection against noise and accidental write operations.

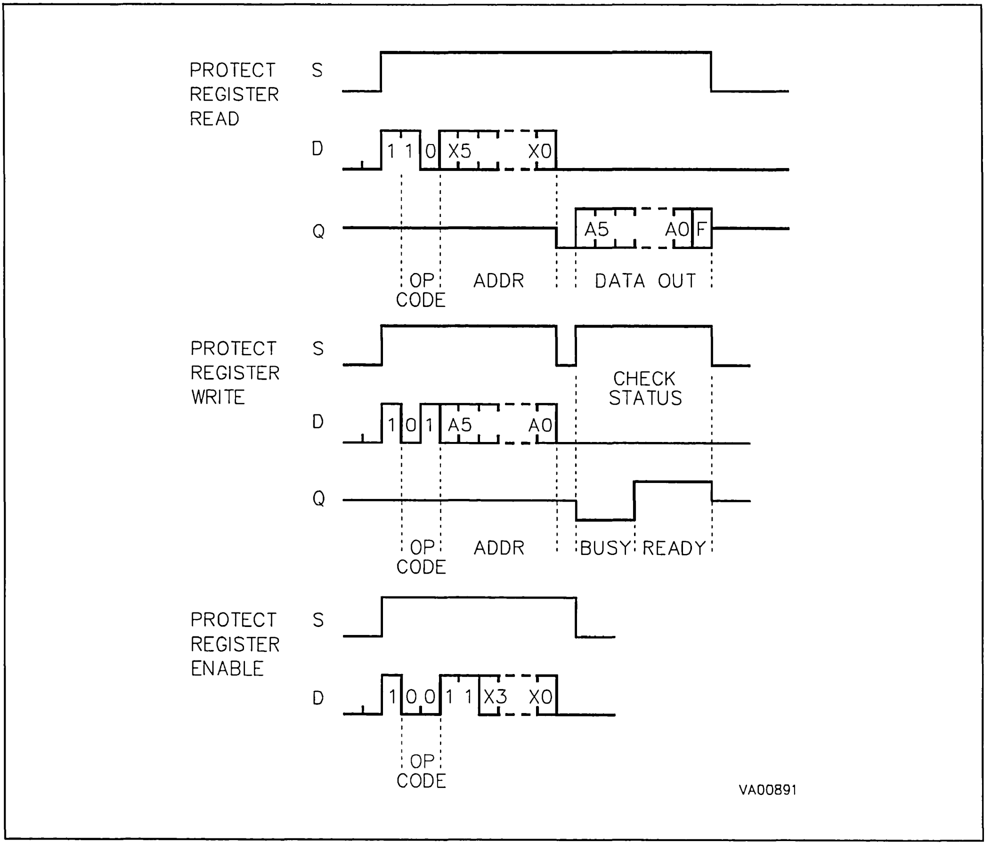
Write Disable does not affect the Read operations.

MEMORY WRITE PROTECTION

The ST93CS46 contains a specific Protect Register. This register stores the bottom address of the memory area which is protected against write together with two flag bits, the Protect Flag which indicates the protection status and an OTP bit which may be set to permanently disable access to the Protect Register and thus prevent any further changes to the memory protection setting. The address from which the memory is to be protected is loaded using the PRWRITE instruction, it may be read using the PRREAD instruction. There is a specific instruction, Protect Register Enable (PREN), to enable the protect instructions PRCLEAR, PRWRITE and PRDS, this is used together with the Protect Register Enable signal (PRE).

In order to program the protection the Write Enable instruction must first be executed. This is followed by asserting both Write Enable (W) and Protect Register Enable (PRE) signals and executing the PREN instruction. The protection may then be set using Protect Register Write (PRWRITE), cleared using the Protect Register Clear (PRCLEAR) or set permanently using the Protect Register Disable (PRDS) instructions.

Figure 8. PRREAD, PRWRITE, PREN Sequence


PROTECT REGISTER READ
S
D
1 1 0 X5 X0
Q
A5 A0 F
OP CODE
ADDR
DATA OUT
PROTECT REGISTER WRITE
S
CHECK STATUS
D
1 0 1 A5 A0
Q
OP CODE
ADDR
BUSY
READY
PROTECT REGISTER ENABLE
S
D
1 0 0 1 1 X3 X0
OP CODE
VA00891

MEMORY WRITE PROTECTION (cont'd)

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the address stored, followed by the Protect Flag status bit. The Protect Register Enable signal (PRE) must be High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish between the status when the Protect Register is cleared (all 1's) and when it is written with all 1's, users must check the Protect Flag status, not the Protect Register contents to ascertain the setting of the memory protection.

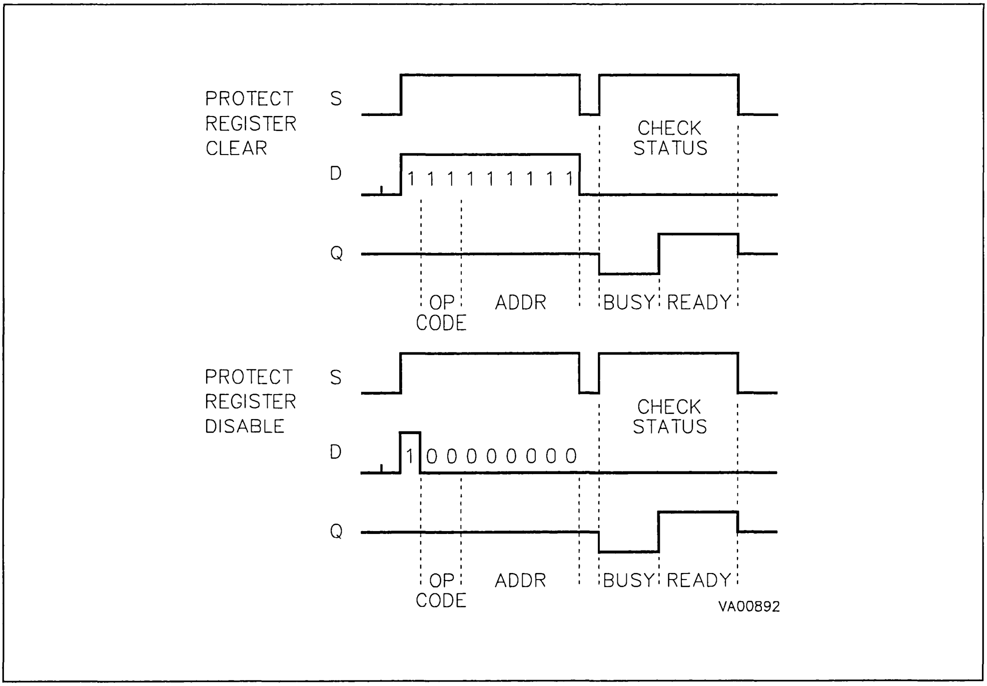
Protect Register Enable

The Protect Register Enable instruction (PREN) is used to enable the PRCLEAR, PRWRITE and PRDS instructions. A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the protect register to all 1's, and thus enables all registers for WRITE and WRALL instructions. It also clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write

Figure 8. PRCLEAR, PRDS Sequence


PROTECT REGISTER CLEAR
S
D
1 1 1 1 1 1 1 1 1
Q
CHECK STATUS
OP CODE
ADDR
BUSY
READY
PROTECT REGISTER DISABLE
S
D
1 0 0 0 0 0 0 0 0
Q
CHECK STATUS
OP CODE
ADDR
BUSY
READY
VA00892

MEMORY WRITE PROTECTION (cont'd)

Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the protect register the address of the first memory location to be protected. After the instruction all memory locations equal to and above the location specified are protected from writing. The Protect Flag status bit is set to '0'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRWRITE instruction, but it is not neccessary to execute first a PRCLEAR.

Protect Register Disable

Caution: The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which makes the Protect Register unalterable in the future, it does this by setting a One Time Programmable bit in the Protect Register. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRDS instruction.

ORDERING INFORMATION

Example: ST93CS46 M 1 013TR

Package

B	PSDIP8 0.4 mm Frame
M	PSO8

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option

013TR	Tape & Reel

Parts are shipped with the memory content set at all “1’s” (0FFFFh).

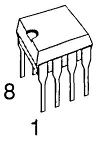
For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

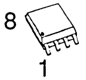
ST93CS56

SERIAL ACCESS CMOS 2K bit (128 x 16) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V SUPPLY VOLTAGE
- USER DEFINED WRITE PROTECT AREA
- PAGE WRITE MODE (4 WORDS)
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame



PSO8 (M)

DESCRIPTION

The ST93CS56 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface. The 2K bit memory is organised as 128 x 16 bit words.

The memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to manage memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the word is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

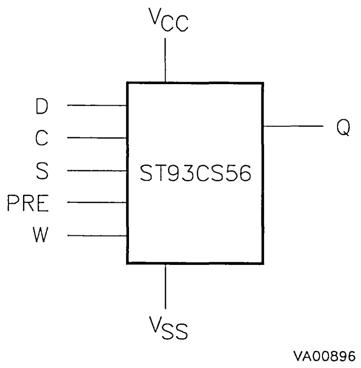


Figure 2A. DIP Pin Connections

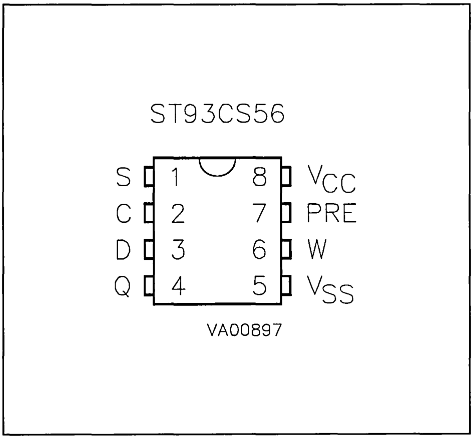


Figure 2B. SO Pin Connections

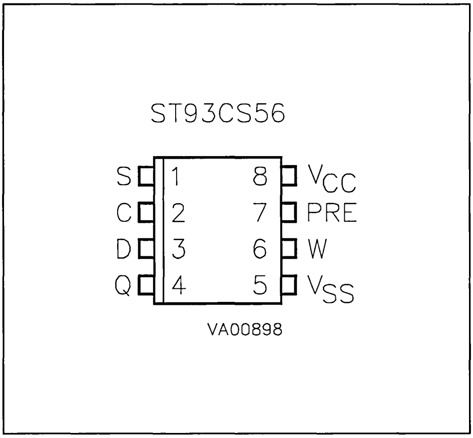


Table 2. Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)			2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

stream of data words. In this way the memory can be read as a continuous data stream from 16 to 2048 bits long. Up to 4 words may be written in a single program cycle using the Page Write instruction. The memory may be 'erased', or set to a predetermined pattern, by using the Write All instruction. An external siganl controls Write Enable. A user defined area of the memory may be write protected. An external signal (PRE) enables access to the Protect Register which stores the lowest address to be write protected. Data may be permanently protected by programming an OTP bit which prevents further changes to the write protect starting address and the protect flag.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 bits at one time into one of the 128 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, both providing that all addresses are outside the write protect area. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

The design of the ST93CS56 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

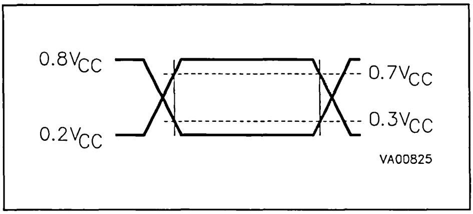


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
V_{IH}	Input High Voltage	$4.5V \le V_{CC} \le 5.5V$	2	V_{CC} + 1	V
V_{IL}	Input Low Voltage	$3V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage	$3V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	grade 1	100		ns
			grade 3 and 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1 The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.
2 Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles

Figure 4. Syncrounus Timing, Start and Op-Code Input

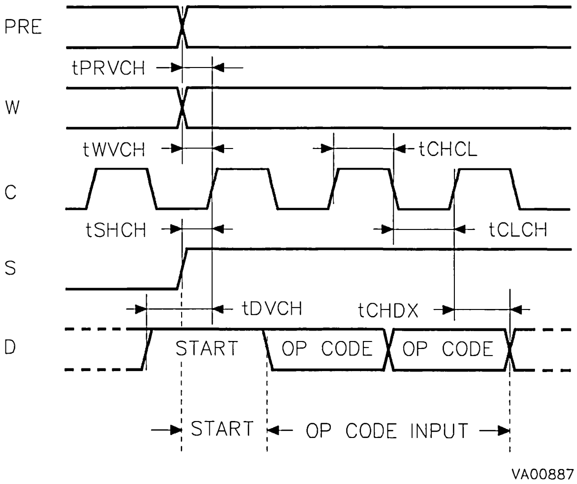
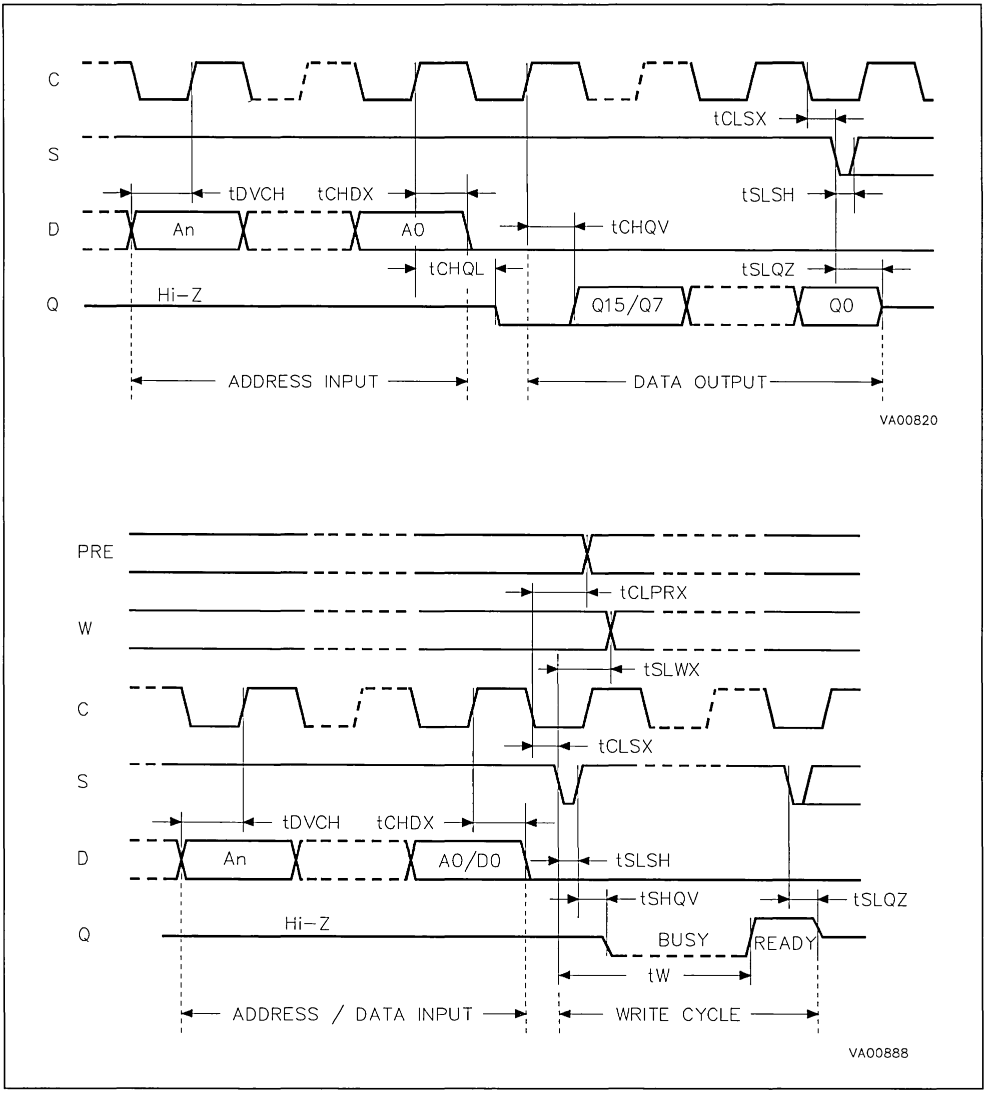


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi-Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
PRE
tCLPRX
W
tSLWX
C
tCLSX
S
tDVCH
tCHDX
D
An
A0/D0
tSLSH
tSHQV
tSLQZ
Q
Hi-Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00888

INSTRUCTIONS

The ST93CS56 has eleven instructions which are shown in Table 6. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word which is made up of eight bits A7-A0, but for the 2K ST93CS56 the MSB of the address (A7) is ignored (don't care).

The start sequence requires the Chip Select and Data Input signals to be set up before a Low to High transition of the Clock. For write instructions the Write Enable signal (W) must be High and for Protect Register instructions the Protect Register Enable signal (PRE) must also be High.

Read

The Read instruction (READ) outputs serial data on the Data Output Q. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable

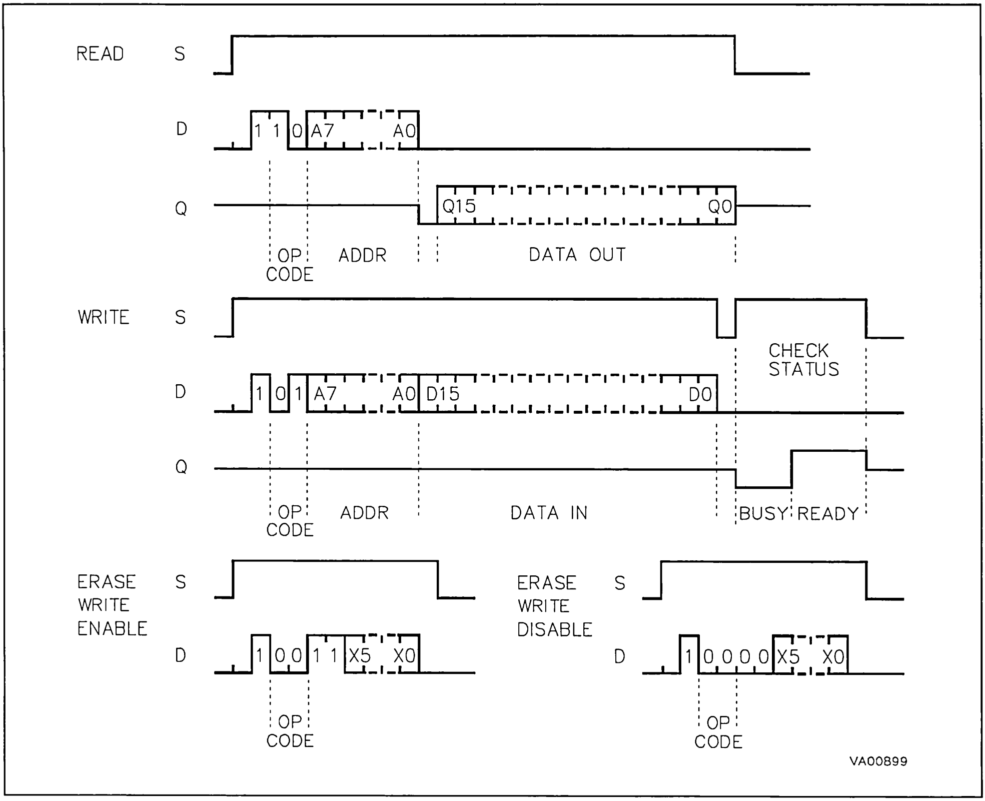
When power is first applied to the ST93CS56 write operations are disabled. To enable write operations the Write Enable signal (W) must be High and a Write Enable instruction (WEN) must be executed. After the WEN instruction write operation remains enabled until either a Write Disable instruction (WDS) is executed or the supply is removed from the device.

Table 6. Instruction Set

Instruction	Description	Op Code	PRE	W	Address (1)	Data	Additional Information
READ	Read Data from memory	10	'0'	X	A7-A0	Q15-Q0	
WRITE	Write Data to memory	01	'0'	'1'	A7-A0	D15-D0	Write if address unprotected
PAWRITE	Page Write to memory	11	'0'	'1'	A7-A0	D15-D0	Write one to 4 words, if all addresses are unprotected
WRALL	Write All	00	'0'	'1'	01XXXXXX	D15-D0	Write all if Protect Register cleared
WEN	Write Enable	00	'0'	'1'	11XXXXXX		
WDS	Write Disable	00	'0'	'1'	00XXXXXX		
PRREAD	Protect Register Read	10	'1'	X	XXXXXXXX	Q8-Q0	Data Output is Protect Address (A7-A0) plus Protect Flag (1)
PRWRITE	Protect Register Write	01	'1'	'1'	A7-A0		Data above A7-A0 is protected (1)
PRCLEAR	Protect Register Clear	11	'1'	'1'	11111111		Protect Flag also cleared ('1')
PREN	Protect Register Enable	00	'1'	'1'	11XXXXXX		

Note: 1. Address bit A7 is not used for the 2K ST93CS56 (don't care).
2. X = don't care ot dummy address bit.

Figure 6. READ, WRITE, WEN, WDS Sequence



INSTRUCTIONS (cont'd)

Write

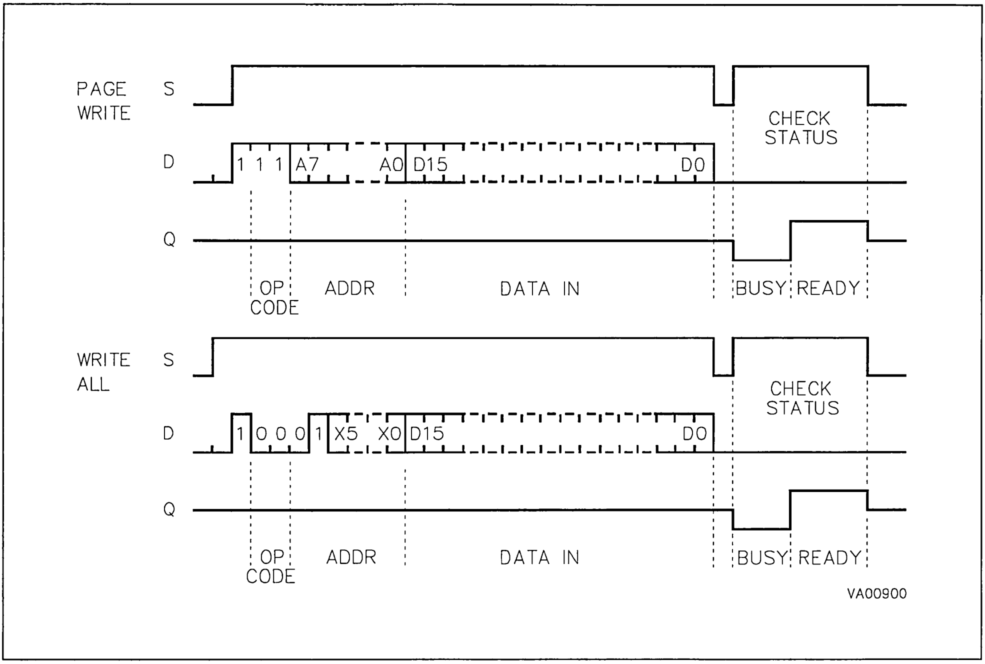
A Write instruction (WRITE) contains the address followed by the data to be written. The Write Enable signal (W) must be High before and during the WRITE instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the LSB of data has been received, the Chip Select signal (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle, providing that the address is NOT in the protected area. If Chip Select (S) is brought High again after a minimum time of tSLSH then the Data Output (D) will indicate the Busy/Ready status. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the receipt of each data word bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The write operation will proceded only if NONE of the addresses of the 1-4 data words has its address bits A6-A2 within the protected area. During the

Figure 7. PAWRITE, WRALL Sequence



INSTRUCTIONS (cont'd)

write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes all memory locations with the data word included in the instruction. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. During the write cycle, the Data Output indicates Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write Disable

The Write Disable instruction (WDS) disables all write operations. It should be used after all write instructions to disable writing to the memory and provide protection against noise and accidental write operations.

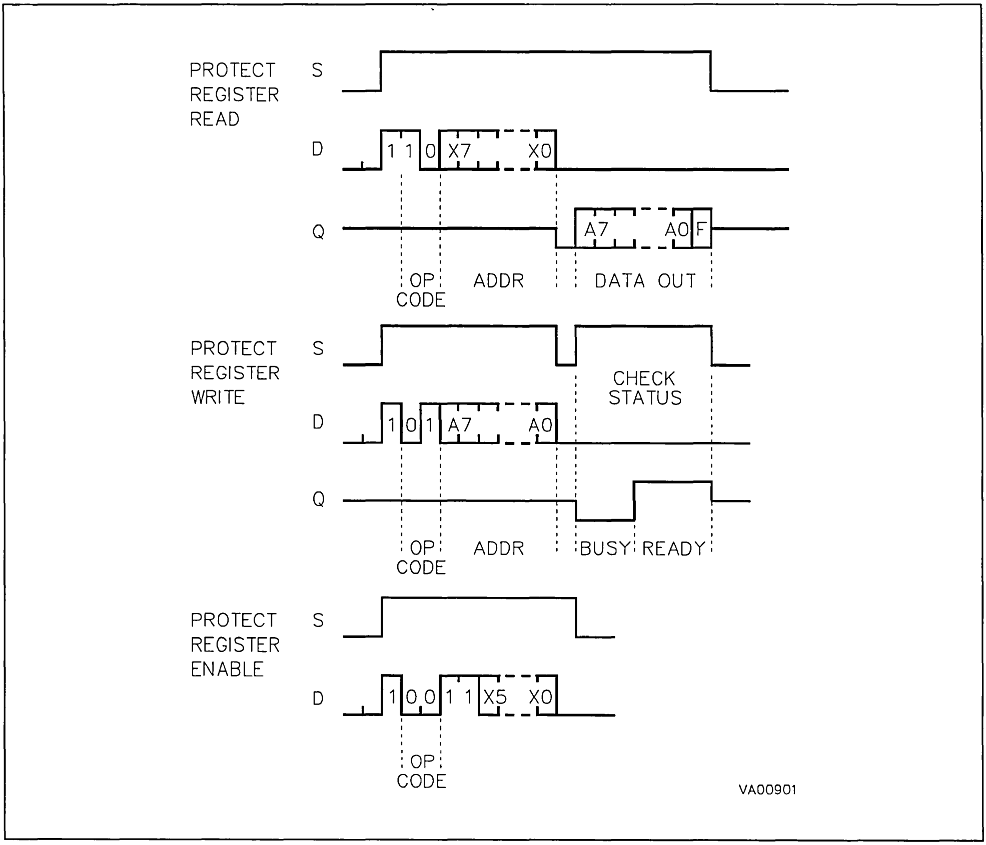
Write Disable does not affect the Read operations.

MEMORY WRITE PROTECTION

The ST93CS56 contains a specific Protect Register. This register stores the bottom address of the memory area which is protected against write together with two flag bits, the Protect Flag which indicates the protection status and an OTP bit which may be set to permanently disable access to the Protect Register and thus prevent any further changes to the memory protection setting. The address from which the memory is to be protected is loaded using the PRWRITE instruction, it may be read using the PRREAD instruction. There is a specific instruction, Protect Register Enable (PREN), to enable the protect instructions PRCLEAR, PRWRITE and PRDS, this is used together with the Protect Register Enable signal (PRE).

In order to program the protection the Write Enable instruction must first be executed. This is followed

Figure 8. PRREAD, PRWRITE, PREN Sequence


PROTECT
REGISTER
READ
S
D
1 1 0 X7 X0
Q
A7 A0 F
OP CODE
ADDR
DATA OUT
PROTECT
REGISTER
WRITE
S
CHECK STATUS
D
1 0 1 A7 A0
Q
OP CODE
ADDR
BUSY
READY
PROTECT
REGISTER
ENABLE
S
D
1 0 0 1 1 X5 X0
OP CODE
VA00901

MEMORY WRITE PROTECTION (cont'd)

by asserting both Write Enable (W) and Protect Register Enable (PRE) signals and executing the PRE instruction. The protection may then be set using Protect Register Write (PRWRITE), cleared using the Protect Register Clear (PRCLEAR) or set permanently using the Protect Register Disable (PRDS) instructions.

Protect Register Read

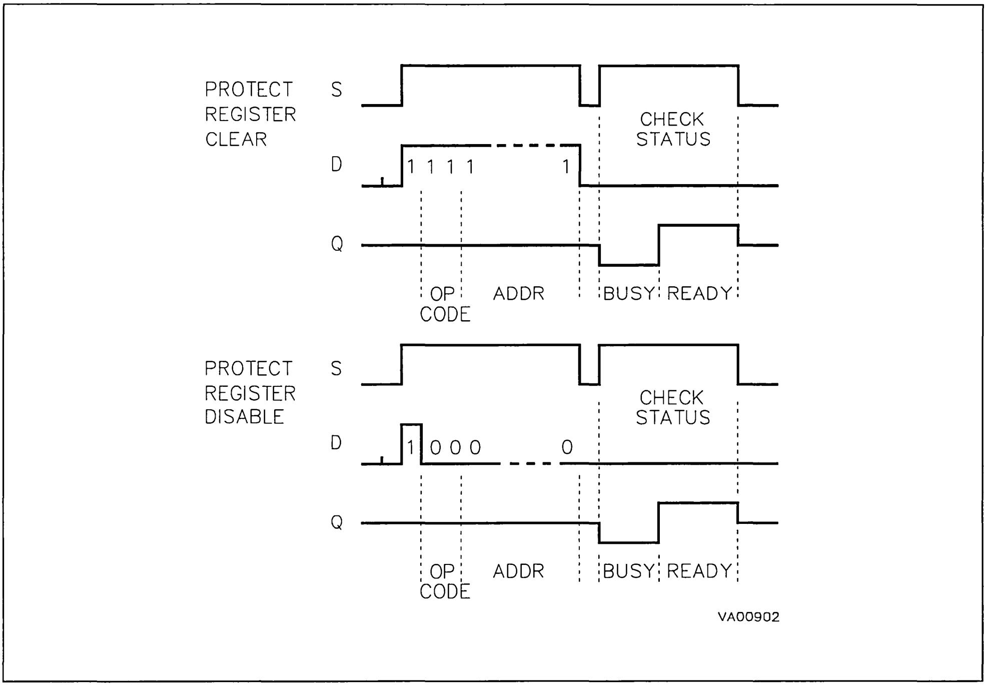
The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the address stored, followed by the Protect Flag status bit. The Protect Register Enable signal (PRE) must be High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish between the status when the Protect Register is cleared (all 1's) and when it is written with all 1's, users must check the Protect Flag status, not the Protect Register contents to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to enable the PRCLEAR, PRWRITE and PRDS instructions. A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution.

Figure 8. PRCLEAR, PRDS Sequence



MEMORY WRITE PROTECTION (cont'd)

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the protect register to all 1's, and thus enables all registers for WRITE and WRALL instructions. It also clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the protect register the address of the first memory location to be protected. After the instruction all memory locations equal to and above the location specified are protected from writing. The Protect Flag status bit is set to '0'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

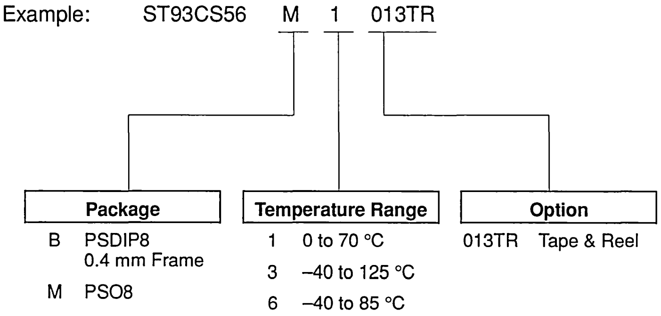
A PREN instruction must immediately precede the PRWRITE instruction, but it is not neccessary to execute first a PRCLEAR.

Protect Register Diasable

Caution: The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which makes the Protect Register unalterable in the future, it does this by setting a One Time Programmable bit in the Protect Register. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRDS instruction.

ORDERING INFORMATION



Example: ST93CS56 M 1 013TR

Package		Temperature Range		Option	
B	PSDIP8 0.4 mm Frame	1	0 to 70 °C	013TR	Tape & Reel
M	PSO8	3	–40 to 125 °C		
		6	–40 to 85 °C		

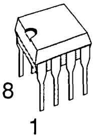
Parts are shipped with the memory content set at all “1’s” (0FFFFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

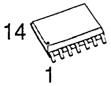
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SERIAL ACCESS CMOS 4K bit (256 x 16) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 3V TO 5.5V SUPPLY VOLTAGE
- USER DEFINED WRITE PROTECT AREA
- PAGE WRITE MODE (4 WORDS)
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame



PSO14 (ML)

DESCRIPTION

The ST93CS66 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface. The 4K bit memory is organised as 256 x 16 bit words.

The memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to manage memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the word is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

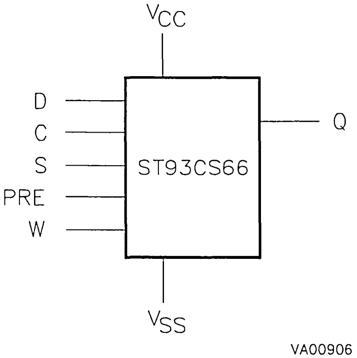


Figure 2A. DIP Pin Connections

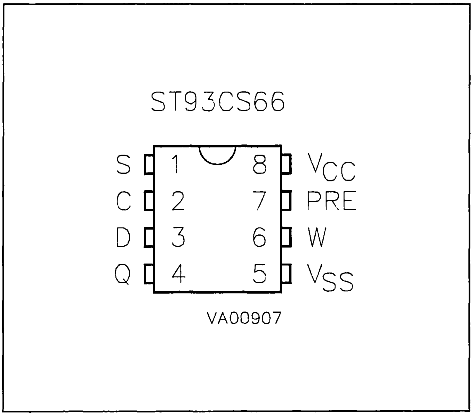
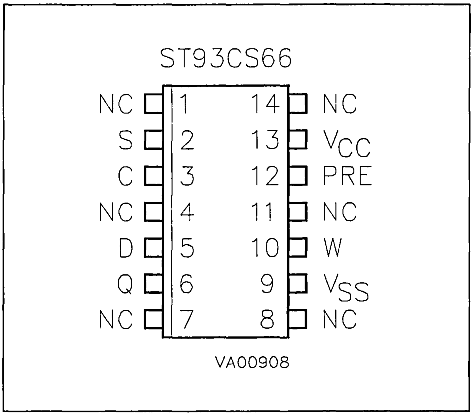


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSO14 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages		–0.3 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)		2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

DESCRIPTION (cont'd)

stream of data words. In this way the memory can be read as a continuous data stream from 16 to 4096 bits long. Up to 4 words may be written in a single program cycle using the Page Write instruction. The memory may be 'erased', or set to a predetermined pattern, by using the Write All instruction. An external siganl controls Write Enable. A user defined area of the memory may be write protected. An external signal (PRE) enables access to the Protect Register which stores the lowest address to be write protected. Data may be permanently protected by programming an OTP bit which prevents further changes to the write protect starting address and the protect flag.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 bits at one time into one of the 256 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, both providing that all addresses are outside the write protect area. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

The design of the ST93CS66 and the High Endurance CMOS technology used for its tabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

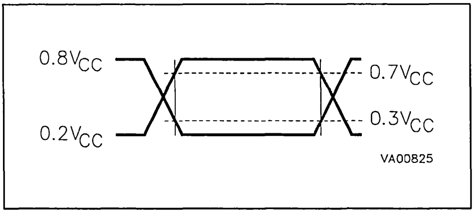


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	$S = V_{IH}$, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	$S = V_{IH}$, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage	$4.5V \leq V_{CC} \leq 5.5V$	–0.1	0.8	V
V_{IH}	Input High Voltage	$4.5V \leq V_{CC} \leq 5.5V$	2	$V_{CC} + 1$	V
V_{IL}	Input Low Voltage	$3V \leq V_{CC} \leq 5.5V$	–0.1	$0.2\ V_{CC}$	V
V_{IH}	Input High Voltage	$3V \leq V_{CC} \leq 5.5V$	$0.8\ V_{CC}$	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
		$I_{OL} = 10\ \mu A$		0.2	V
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4		V
		$I_{OH} = -10\mu A$	$V_{CC} - 0.2$		V

Table 5. AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

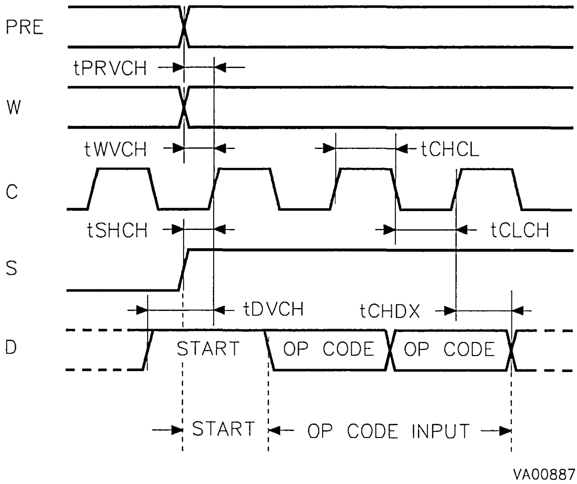
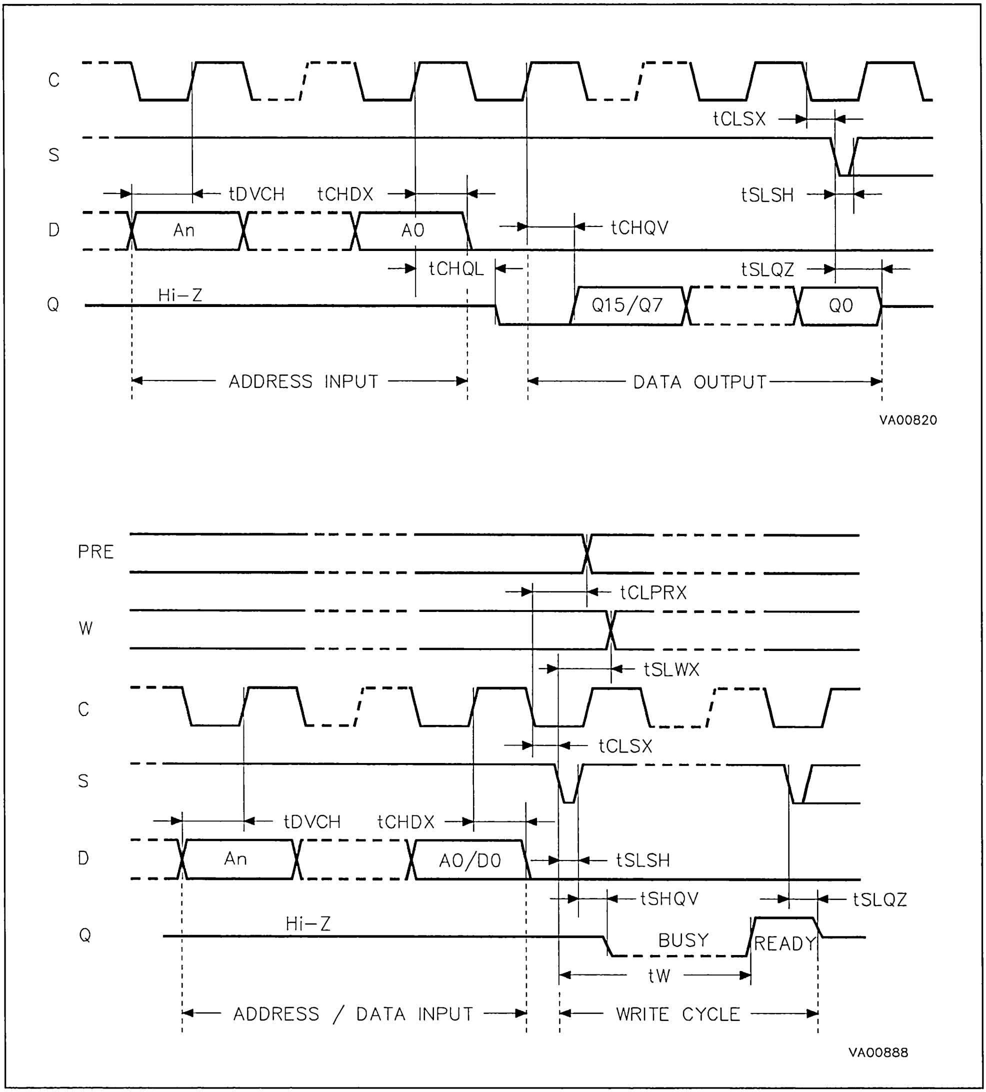


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi–Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
PRE
tCLPRX
W
tSLWX
C
tCLSX
S
tDVCH
tCHDX
D
An
A0/D0
tSLSH
tSHQV
tSLQZ
Q
Hi–Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00888

INSTRUCTIONS

The ST93CS66 has eleven instructions which are shown in Table 6. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word which is made up of eight bits A7-A0.

The start sequence requires the Chip Select and Data Input signals to be set up before a Low to High transition of the Clock. For write instructions the Write Enable signal (W) must be High and for Protect Register instructions the Protect Register Enable signal (PRE) must also be High.

Read

The Read instruction (READ) outputs serial data on the Data Output Q. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable

When power is first applied to the ST93CS66 write operations are disabled. To enable write operations the Write Enable signal (W) must be High and a Write Enable instruction (WEN) must be executed. After the WEN instruction write operation remains enabled until either a Write Disable instruction (WDS) is executed or the supply is removed from the device.

Write

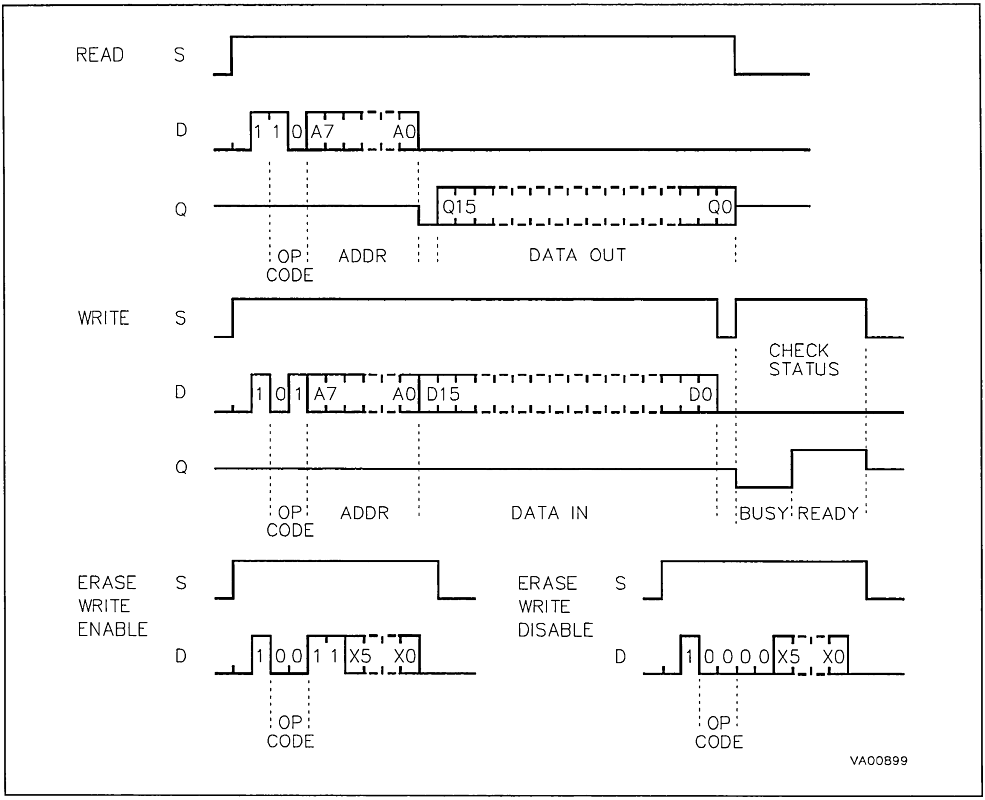
A Write instruction (WRITE) contains the address followed by the data to be written. The Write Enable signal (W) must be High before and during the WRITE instruction, but is subsequently ignored (don't care). Input address and data are read on

Table 6. Instruction Set

Instruction	Description	Op Code	PRE	W	Address	Data	Additional Information
READ	Read Data from memory	10	'0'	X	A7-A0	Q15-Q0	
WRITE	Write Data to memory	01	'0'	'1'	A7-A0	D15-D0	Write if address unprotected
PAWRITE	Page Write to memory	11	'0'	'1'	A7-A0	D15-D0	Write one to 4 words, if all addresses are unprotected
WRALL	Write All	00	'0'	'1'	01XXXXXX	D15-D0	Write all if Protect Register cleared
WEN	Write Enable	00	'0'	'1'	11XXXXXX		
WDS	Write Disable	00	'0'	'1'	00XXXXXX		
PRREAD	Protect Register Read	10	'1'	X	XXXXXXXX	Q8-Q0	Data Output is Protect Address (A7-A0) plus Protect Flag
PRWRITE	Protect Register Write	01	'1'	'1'	A7-A0		Data above A7-A0 is protected
PRCLEAR	Protect Register Clear	11	'1'	'1'	11111111		Protect Flag also cleared ('1')
PREN	Protect Register Enable	00	'1'	'1'	11XXXXXX		
PRDS	Protect Register Disable	00	'1'	'1'	00000000		OTP Flag set, prevents any further change to Protect Register

Note: X = don't care or dummy address bit.

Figure 6. READ, WRITE, WEN, WDS Sequence


READ
S
D
1 1 0 A7 A0
Q
Q15 Q0
OP CODE
ADDR
DATA OUT
WRITE
S
CHECK STATUS
D
1 0 1 A7 A0 D15 D0
Q
OP CODE
ADDR
DATA IN
BUSY
READY
ERASE WRITE ENABLE
S
D
1 0 0 1 1 X5 X0
OP CODE
ERASE WRITE DISABLE
S
D
1 0 0 0 0 X5 X0
OP CODE
VA00899

INSTRUCTIONS (cont'd)

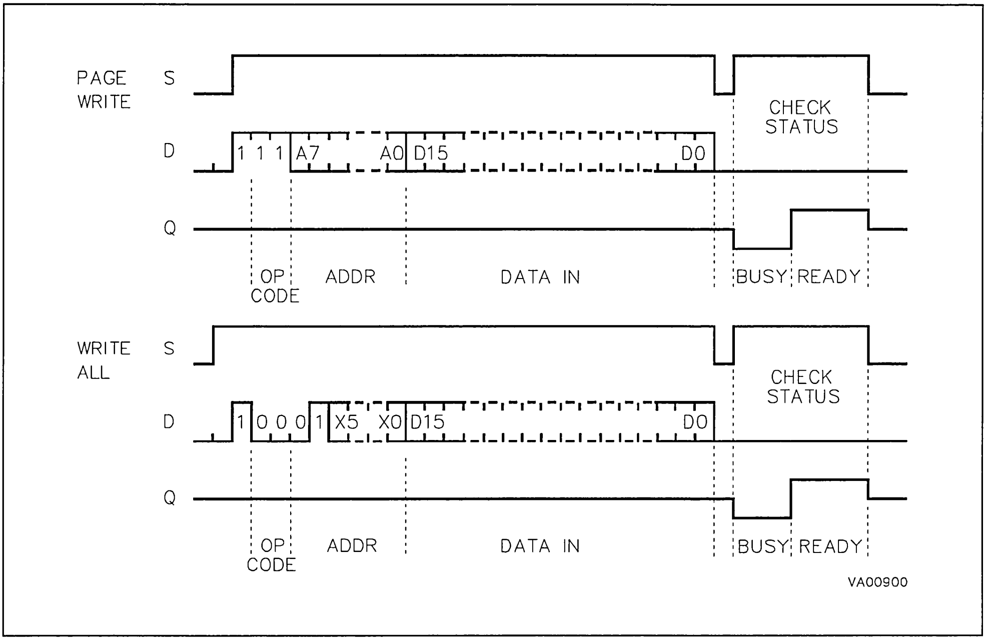
the Low to High transition of the clock. After the LSB of data has been received, the Chip Select signal (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle, providing that the address is NOT in the protected area. If Chip Select (S) is brought High again after a minimum time of tSLSH then the Data Output (D) will indicate the Busy/Ready status. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the receipt of each data word bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The write operation will proceded only if NONE of the addresses of the 1-4 data words has its address bits A7-A2 within the protected area. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Figure 7. PAWRITE, WRALL Sequence



INSTRUCTIONS (cont'd)

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes all memory locations with the data word included in the instruction. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. During the write cycle, the Data Output indicates Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write Disable

The Write Disable instruction (WDS) disables all write operations. It should be used after all write instructions to disable writing to the memory and provide protection against noise and accidental write operations.

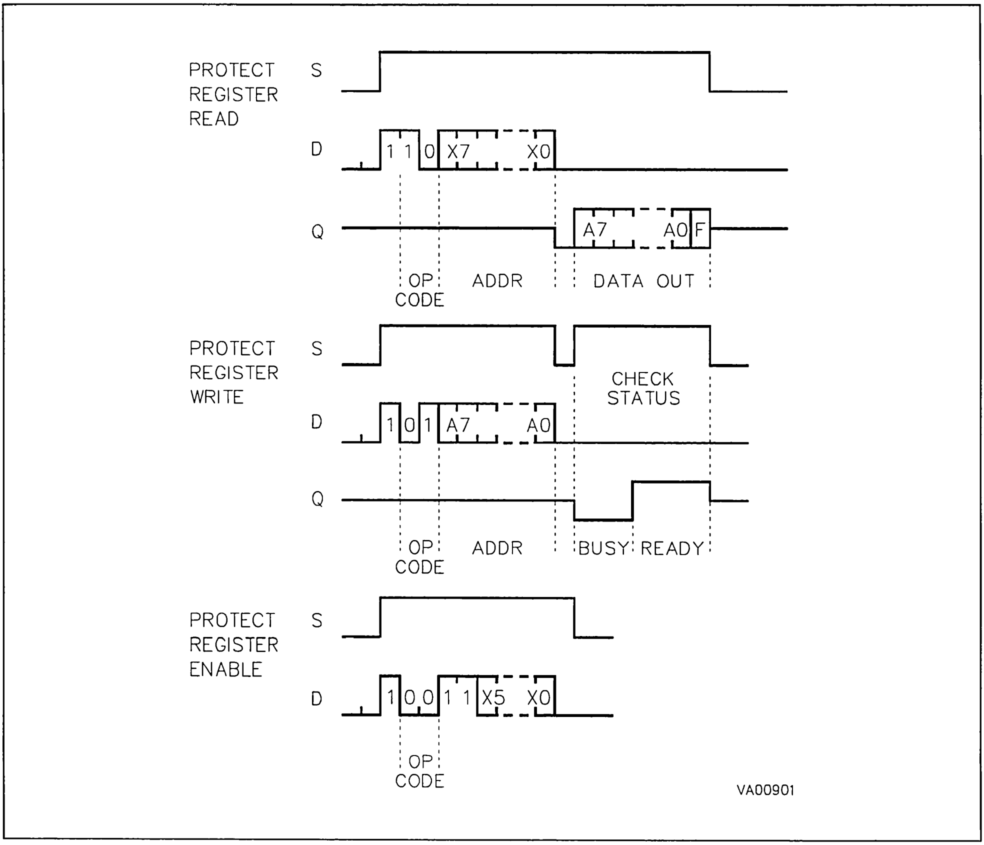
Write Disable does not affect the Read operations.

MEMORY WRITE PROTECTION

The ST93CS66 contains a specific Protect Register. This register stores the bottom address of the memory area which is protected against write together with two flag bits, the Protect Flag which indicates the protection status and an OTP bit which may be set to permanently disable access to the Protect Register and thus prevent any further changes to the memory protection setting. The address from which the memory is to be protected is loaded using the PRWRITE instruction, it may be read using the PRREAD instruction. There is a specific instruction, Protect Register Enable (PREN), to enable the protect instructions PRCLEAR, PRWRITE and PRDS, this is used together with the Protect Register Enable signal (PRE).

In order to program the protection the Write Enable instruction must first be executed. This is followed by asserting both Write Enable (W) and Protect Register Enable (PRE) signals and executing the PREN instruction. The protection may then be set using Protect Register Write (PRWRITE), cleared using the Protect Register Clear (PRCLEAR) or set permanently using the Protect Register Disable (PRDS) instructions.

Figure 8. PRREAD, PRWRITE, PREN Sequence


PROTECT REGISTER READ
S
D
1 1 0 X7 X0
Q
A7 A0 F
OP CODE
ADDR
DATA OUT
PROTECT REGISTER WRITE
S
CHECK STATUS
D
1 0 1 A7 A0
Q
OP CODE
ADDR
BUSY
READY
PROTECT REGISTER ENABLE
S
D
1 0 0 1 1 X5 X0
OP CODE
VA00901

MEMORY WRITE PROTECTION (cont'd)

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the address stored, followed by the Protect Flag status bit. The Protect Register Enable signal (PRE) must be High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish between the status when the Protect Register is cleared (all 1's) and when it is written with all 1's, users must check the Protect Flag status, not the Protect Register contents to ascertain the setting of the memory protection.

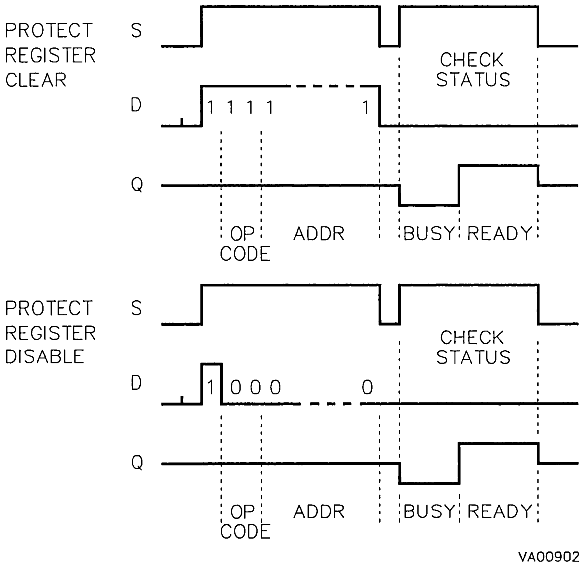
Protect Register Enable

The Protect Register Enable instruction (PREN) is used to enable the PRCLEAR, PRWRITE and PRDS instructions. A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the protect register to all 1's, and thus enables all registers for WRITE and WRALL instructions. It also clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write

Figure 9. PRCLEAR, PRDS Sequence



MEMORY WRITE PROTECTION (cont'd)

Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the protect register the address of the first memory location to be protected. After the instruction all memory locations equal to and above the location specified are protected from writing. The Protect Flag status bit is set to '0'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

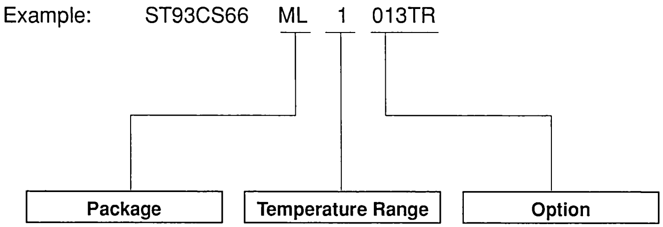
A PREN instruction must immediately precede the PRWRITE instruction, but it is not neccessary to execute first a PRCLEAR.

Protect Register Disable

Caution: The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which makes the Protect Register unalterable in the future, it does this by setting a One Time Programmable bit in the Protect Register. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRDS instruction.

ORDERING INFORMATION


Example: ST93CS66 ML 1 013TR
Package
Temperature Range
Option

Package

B	PSDIP8 0.4 mm Frame
ML	PSO14

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option

013TR	Tape & Reel

Parts are shipped with the memory content set at all “1’s” (0FFFFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

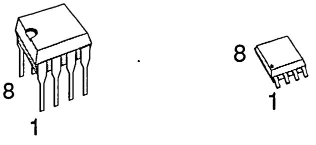
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

ST93CS47

2.5V SERIAL ACCESS CMOS 1K bit (64 x 16) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 2.5V TO 5.5V SUPPLY VOLTAGE
- USER DEFINED WRITE PROTECT AREA
- PAGE WRITE MODE (4 WORDS)
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

PSO8 (M)

DESCRIPTION

The ST93CS47 is a 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface. The 1K bit memory is organised as 64 x 16 bit words. The ST93CS47 operates in read and write down to a 2.5V supply voltage.

The memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to manage memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the word is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

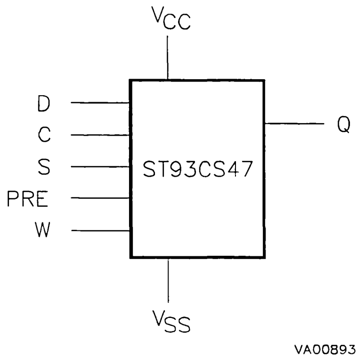


Figure 2A. DIP Pin Connections

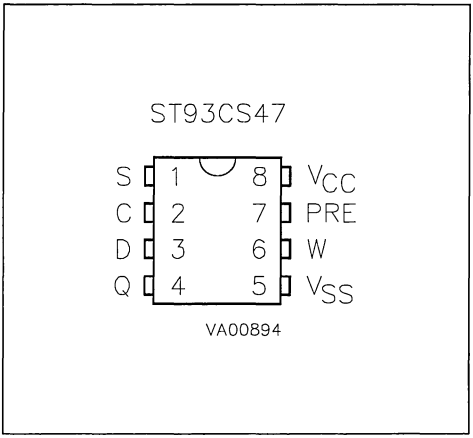


Figure 2B. SO Pin Connections

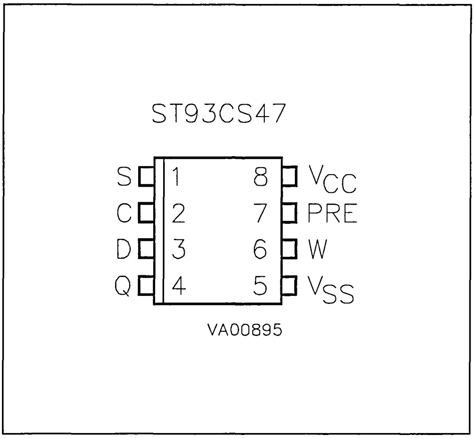


Table 2. Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)			2000	V

Note: Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

stream of data words. In this way the memory can be read as a continuous data stream from 16 to 1024 bits long. Up to 4 words may be written in a single program cycle using the Page Write instruction. The memory may be 'erased', or set to a predetermined pattern, by using the Write All instruction. An external signal controls Write Enable. A user defined area of the memory may be write protected. An external signal (PRE) enables access to the Protect Register which stores the lowest address to be write protected. Data may be permanently protected by programming an OTP bit which prevents further changes to the write protect starting address and the protect flag.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 bits at one time into one of the 64 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, both providing that all addresses are outside the write protect area. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

The design of the ST93CS47 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

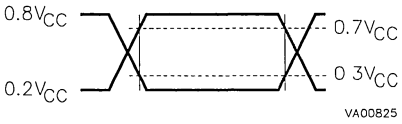


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		5	pF

Note: This parameter is sampled only and not tested 100%

Table 4. DC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	$S = V_{IH}$, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	$S = V_{IH}$, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
V_{IH}	Input High Voltage	$4.5V \le V_{CC} \le 5.5V$	2	$V_{CC} + 1$	V
V_{IL}	Input Low Voltage	$2.5V \le V_{CC} \le 5.5V$	–0.1	$0.2 V_{CC}$	V
V_{IH}	Input High Voltage	$2.5V \le V_{CC} \le 5.5V$	$0.8 V_{CC}$	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	$V_{CC} - 0.2$		V

Table 5. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	grade 1	100		ns
			grade 3 and 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

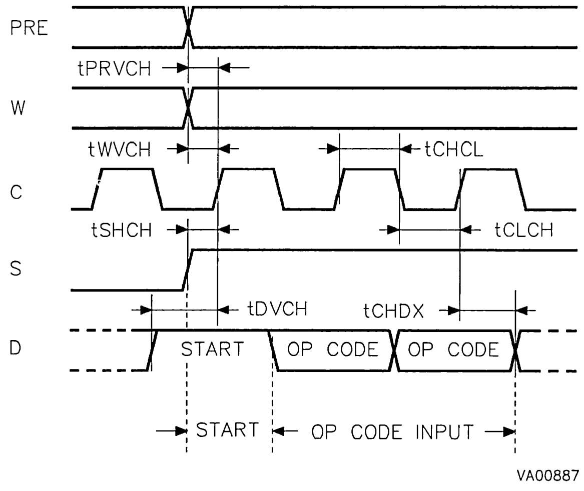
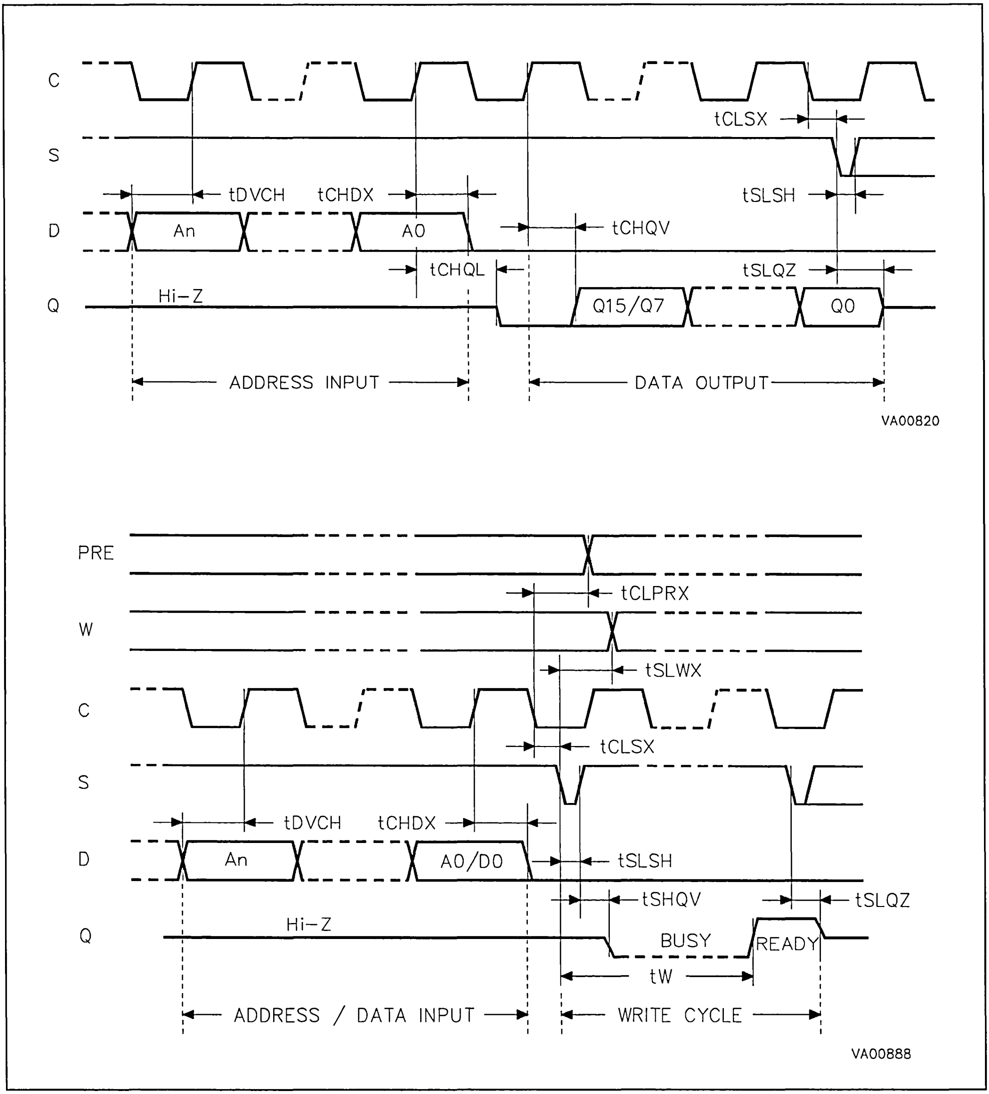


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi-Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
PRE
tCLPRX
W
tSLWX
C
tCLSX
S
tDVCH
tCHDX
D
An
A0/D0
tSLSH
tSHQV
tSLQZ
Q
Hi-Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00888

INSTRUCTIONS

The ST93CS47 has eleven instructions which are shown in Table 6. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word which is made up of six bits A5-A0.

The start sequence requires the Chip Select and Data Input signals to be set up before a Low to High transition of the Clock. For write instructions the Write Enable signal (W) must be High and for Protect Register instructions the Protect Register Enable signal (PRE) must also be High.

Read

The Read instruction (READ) outputs serial data on the Data Output Q. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable

When power is first applied to the ST93CS47 write operations are disabled. To enable write operations the Write Enable signal (W) must be High and a Write Enable instruction (WEN) must be executed. After the WEN instruction write operation remains enabled until either a Write Disable instruction (WDS) is executed or the supply is removed from the device.

Write

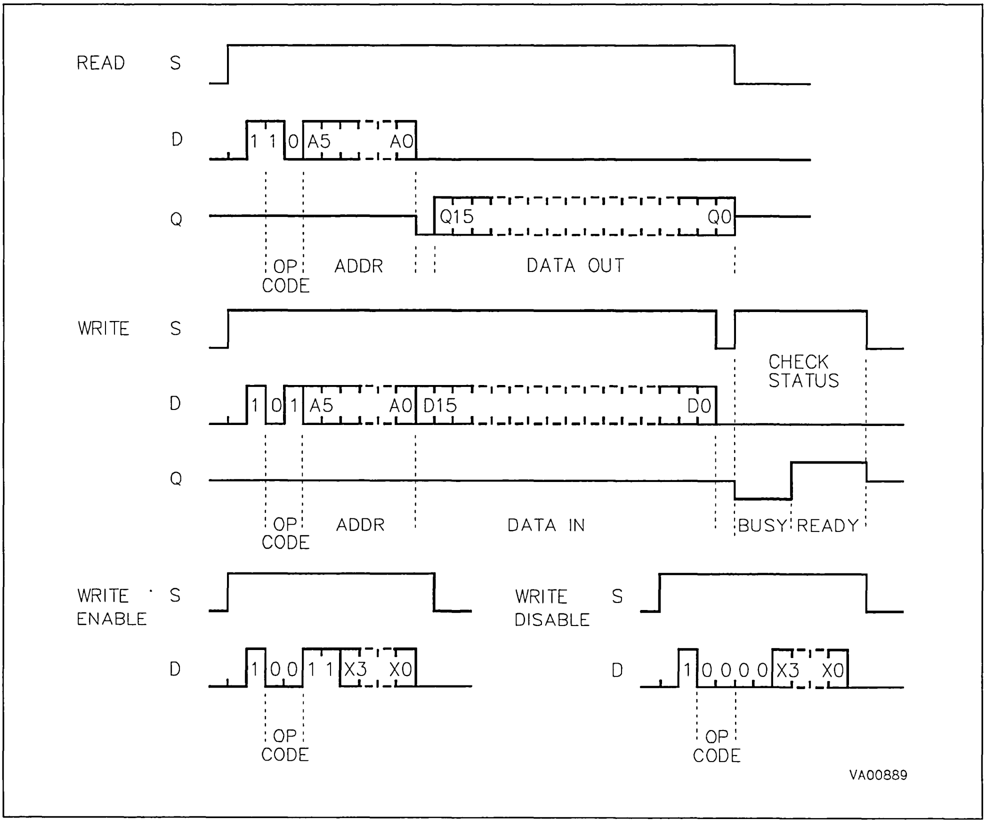
A Write instruction (WRITE) contains the address followed by the data to be written. The Write Enable signal (W) must be High before and during the WRITE instruction, but is subsequently ignored (don't care). Input address and data are read on

Table 6. Instruction Set

Instruction	Description	Op Code	PRE	W	Address	Data	Additional Information
READ	Read Data from memory	10	'0'	X	A5-A0	Q15-Q0	
WRITE	Write Data to memory	01	'0'	'1'	A5-A0	D15-D0	Write if address unprotected
PAWRITE	Page Write to memory	11	'0'	'1'	A5-A0	D15-D0	Write one to 4 words, if all addresses are unprotected
WRALL	Write All	00	'0'	'1'	01XXXX	D15-D0	Write all if Protect Register cleared
WEN	Write Enable	00	'0'	'1'	11XXXX		
WDS	Write Disable	00	'0'	'1'	00XXXX		
PRREAD	Protect Register Read	10	'1'	X	XXXXXX	Q6-Q0	Data Output is Protect Address (A5-A0) plus Protect Flag
PRWRITE	Protect Register Write	01	'1'	'1'	A5-A0		Data above A5-A0 is protected
PRCLEAR	Protect Register Clear	11	'1'	'1'	111111		Protect Flag also cleared ('1')
PREN	Protect Register Enable	00	'1'	'1'	11XXXX		
PRDS	Protect Register Disable	00	'1'	'1'	000000		OTP Flag set, prevents any further change to Protect Register

Note: X = don't care or dummy address bit

Figure 6. READ, WRITE, WEN, WDS Sequence



INSTRUCTIONS (cont'd)

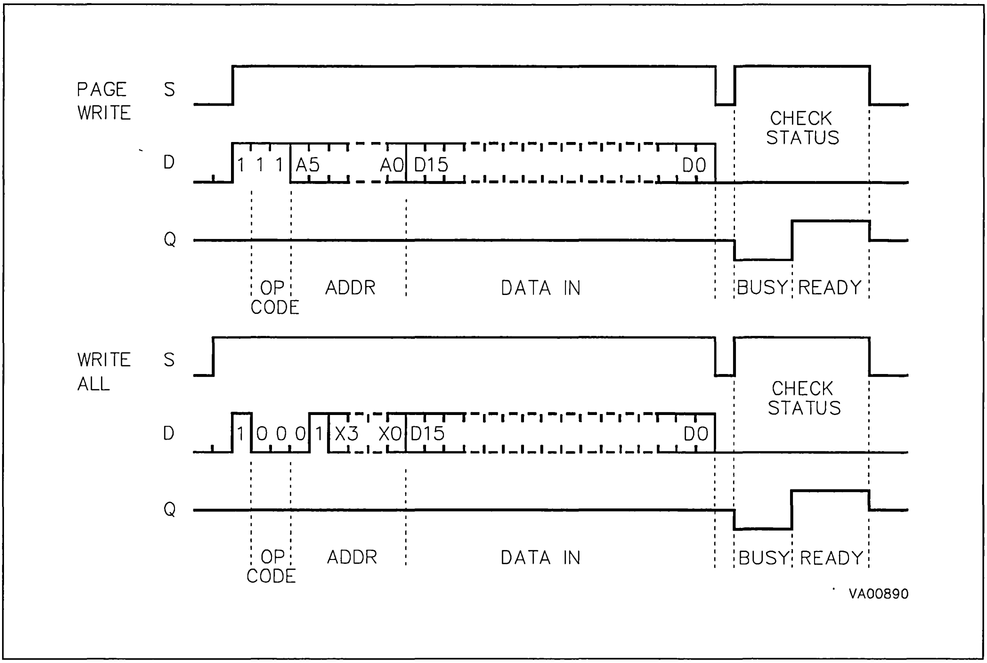
the Low to High transition of the clock. After the LSB of data has been received, the Chip Select signal (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle, providing that the address is NOT in the protected area. If Chip Select (S) is brought High again after a minimum time of tSLSH then the Data Output (D) will indicate the Busy/Ready status. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the receipt of each data word bits A1-A0 of the internal address register are incremented, the high order bits A5-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The write operation will proceded only if NONE of the addresses of the 1-4 data words has its address bits A5-A2 within the protected area. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Figure 7. PAWRITE, WRALL Sequence



INSTRUCTIONS (cont'd)

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes all memory locations with the data word included in the instruction. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. During the write cycle, the Data Output indicates Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write Disable

The Write Disable instruction (WDS) disables all write operations. It should be used after all write instructions to disable writing to the memory and provide protection against noise and accidental write operations.

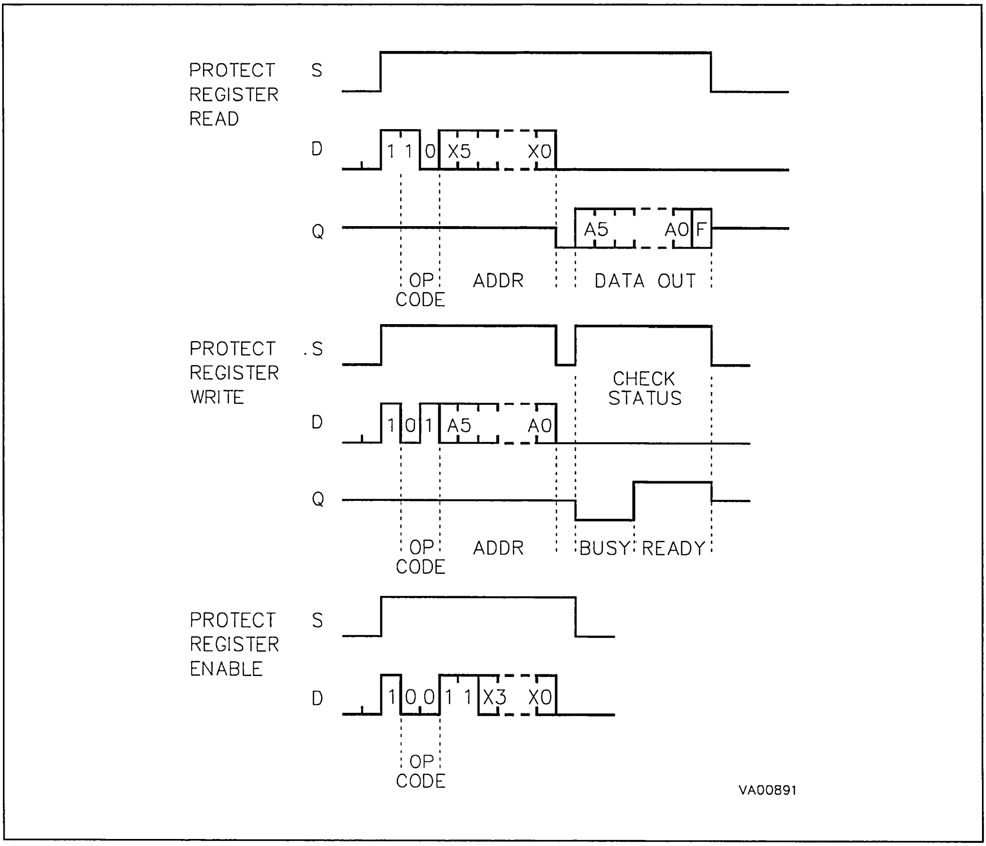
Write Disable does not affect the Read operations.

MEMORY WRITE PROTECTION

The ST93CS47 contains a specific Protect Register. This register stores the bottom address of the memory area which is protected against write together with two flag bits, the Protect Flag which indicates the protection status and an OTP bit which may be set to permanently disable access to the Protect Register and thus prevent any further changes to the memory protection setting. The address from which the memory is to be protected is loaded using the PRWRITE instruction, it may be read using the PRREAD instruction. There is a specific instruction, Protect Register Enable (PREN), to enable the protect instructions PRCLEAR, PRWRITE and PRDS, this is used together with the Protect Register Enable signal (PRE).

In order to program the protection the Write Enable instruction must first be executed. This is followed by asserting both Write Enable (W) and Protect Register Enable (PRE) signals and executing the PREN instruction. The protection may then be set using Protect Register Write (PRWRITE), cleared using the Protect Register Clear (PRCLEAR) or set permanently using the Protect Register Disable (PRDS) instructions.

Figure 8. PRREAD, PRWRITE, PREN Sequence


PROTECT REGISTER READ
S
D
1 1 0 X5 X0
Q
A5 A0 F
OP CODE
ADDR
DATA OUT
PROTECT REGISTER WRITE
S
CHECK STATUS
D
1 0 1 A5 A0
Q
OP CODE
ADDR
BUSY
READY
PROTECT REGISTER ENABLE
S
D
1 0 0 1 1 X3 X0
OP CODE
VA00891

MEMORY WRITE PROTECTION (cont'd)

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the address stored, followed by the Protect Flag status bit. The Protect Register Enable signal (PRE) must be High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish between the status when the Protect Register is cleared (all 1's) and when it is written with all 1's, users must check the Protect Flag status, not the Protect Register contents to ascertain the setting of the memory protection.

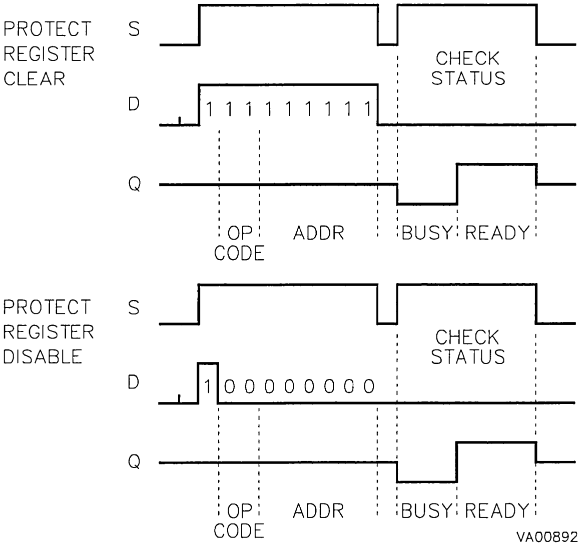
Protect Register Enable

The Protect Register Enable instruction (PREN) is used to enable the PRCLEAR, PRWRITE and PRDS instructions. A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the protect register to all 1's, and thus enables all registers for WRITE and WRALL instructions. It also clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write

Figure 9. PRCLEAR, PRDS Sequence


PROTECT
REGISTER
CLEAR
S
D
1 1 1 1 1 1 1 1 1
Q
CHECK
STATUS
OP
CODE
ADDR
BUSY
READY
PROTECT
REGISTER
DISABLE
S
D
1 0 0 0 0 0 0 0 0
Q
CHECK
STATUS
OP
CODE
ADDR
BUSY
READY
VA00892

MEMORY WRITE PROTECTION (cont'd)

Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the protect register the address of the first memory location to be protected. After the instruction all memory locations equal to and above the location specified are protected from writing. The Protect Flag status bit is set to '0'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRWRITE instruction, but it is not neccessary to execute first a PRCLEAR.

Protect Register Disable

Caution: The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which makes the Protect Register unalterable in the future, it does this by setting a One Time Programmable bit in the Protect Register. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRDS instruction.

ORDERING INFORMATION

Example: ST93CS47 M 1 013TR

Package

B	PSDIP8 0.4 mm Frame
M	PSO8

Temperature Range

1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option

013TR	Tape & Reel

Parts are shipped with the memory content set at all “1’s” (0FFFFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

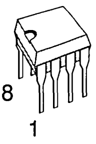
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

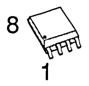
ST93CS57

2.5V SERIAL ACCESS CMOS 2K bit (128 x 16) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 2.5V TO 5.5V SUPPLY VOLTAGE
- USER DEFINED WRITE PROTECT AREA
- PAGE WRITE MODE (4 WORDS)
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame



PSO8 (M)

DESCRIPTION

The ST93CS57 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface. The 2K bit memory is organised as 128 x 16 bit words. The ST93CS57 operates in read and write down to a 2.5V supply voltage.

The memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to manage memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the word is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

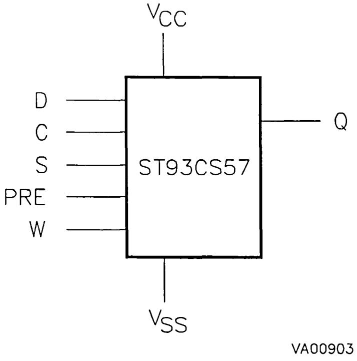


Figure 2A. DIP Pin Connections

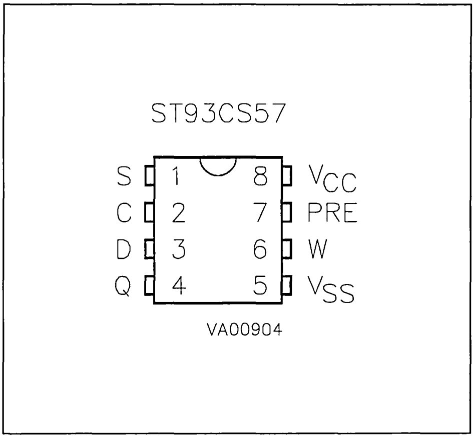


Figure 2B. SO Pin Connections

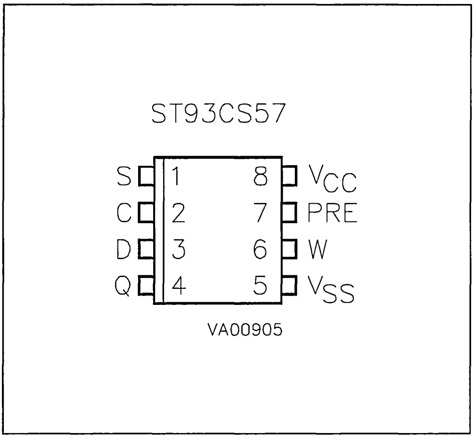


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

stream of data words. In this way the memory can be read as a continuous data stream from 16 to 2048 bits long. Up to 4 words may be written in a single program cycle using the Page Write instruction. The memory may be 'erased', or set to a predetermined pattern, by using the Write All instruction. An external siganl controls Write Enable. A user defined area of the memory may be write protected. An external signal (PRE) enables access to the Protect Register which stores the lowest address to be write protected. Data may be permanently protected by programming an OTP bit which prevents further changes to the write protect starting address and the protect flag.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 bits at one time into one of the 128 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, both providing that all addresses are outside the write protect area. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

The design of the ST93CS57 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

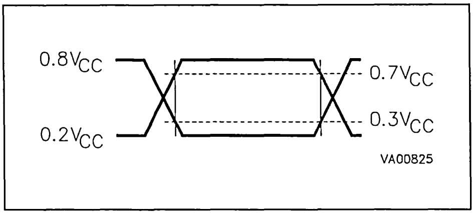


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage	$4.5V \leq V_{CC} \leq 5.5V$	–0.1	0.8	V
V_{IH}	Input High Voltage	$4.5V \leq V_{CC} \leq 5.5V$	2	V_{CC} + 1	V
V_{IL}	Input Low Voltage	$2.5V \leq V_{CC} \leq 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage	$2.5V \leq V_{CC} \leq 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

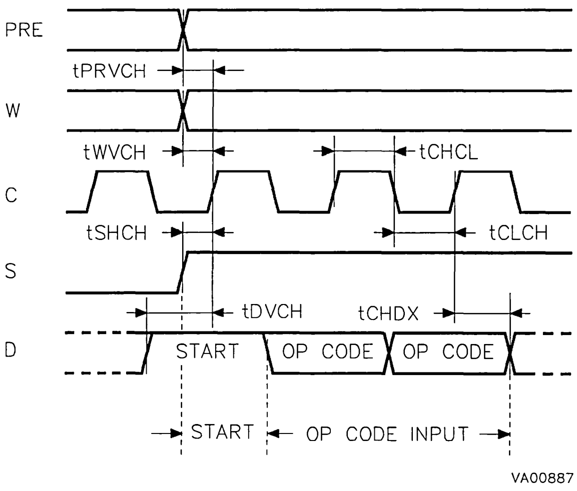
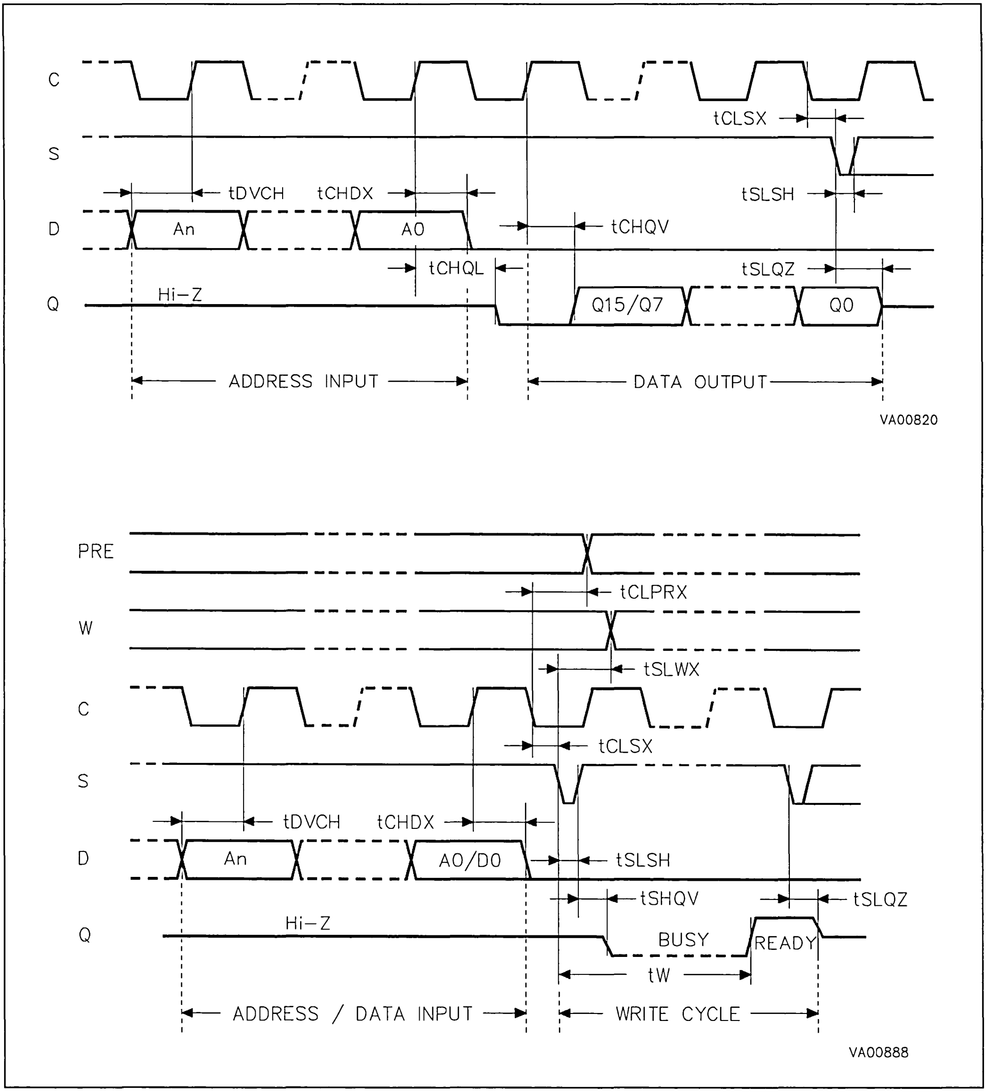


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi−Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
PRE
W
C
S
D
Q
tCLPRX
tSLWX
tCLSX
tDVCH
tCHDX
An
A0/D0
tSLSH
tSHQV
tSLQZ
Hi−Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00888

INSTRUCTIONS

The ST93CS57 has eleven instructions which are shown in Table 6. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word which is made up of eight bits A7-A0, but for the 2K ST93CS57 the MSB of the address (A7) is ignored (don't care).

The start sequence requires the Chip Select and Data Input signals to be set up before a Low to High transition of the Clock. For write instructions the Write Enable signal (W) must be High and for Protect Register instructions the Protect Register Enable signal (PRE) must also be High.

Read

The Read instruction (READ) outputs serial data on the Data Output Q. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable

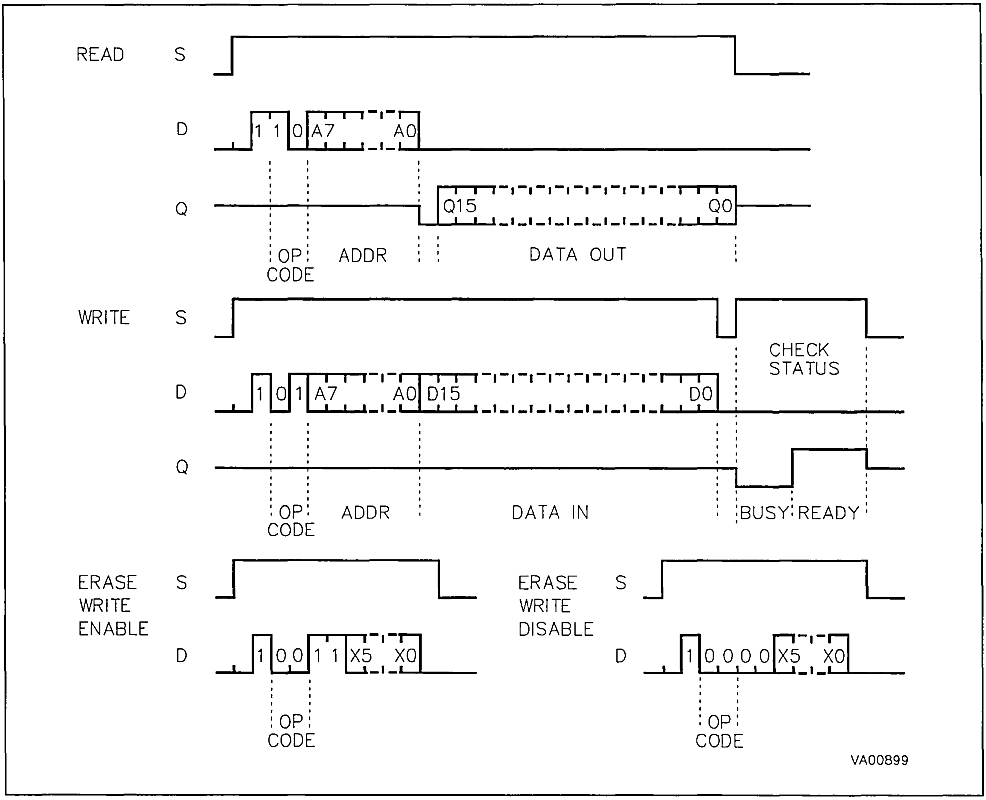
When power is first applied to the ST93CS57 write operations are disabled. To enable write operations the Write Enable signal (W) must be High and a Write Enable instruction (WEN) must be executed. After the WEN instruction write operation remains enabled until either a Write Disable instruction (WDS) is executed or the supply is removed from the device.

Table 6. Instruction Set

Instruction	Description	Op Code	PRE	W	Address [1]	Data	Additional Information
READ	Read Data from memory	10	'0'	X	A7-A0	Q15-Q0	
WRITE	Write Data to memory	01	'0'	'1'	A7-A0	D15-D0	Write if address unprotected
PAWRITE	Page Write to memory	11	'0'	'1'	A7-A0	D15-D0	Write one to 4 words, if all addresses are unprotected
WRALL	Write All	00	'0'	'1'	01XXXXXX	D15-D0	Write all if Protect Register cleared
WEN	Write Enable	00	'0'	'1'	11XXXXXX		
WDS	Write Disable	00	'0'	'1'	00XXXXXX		
PRREAD	Protect Register Read	10	'1'	X	XXXXXXXX	Q8-Q0	Data Output is Protect Address (A7-A0) plus Protect Flag (1)
PRWRITE	Protect Register Write	01	'1'	'1'	A7-A0		Data above A7-A0 is protected (1)
PRCLEAR	Protect Register Clear	11	'1'	'1'	11111111		Protect Flag also cleared ('1')
PREN	Protect Register Enable	00	'1'	'1'	11XXXXXX		

Note: 1. Address bit A7 is not used for the 2K ST93CS56 (don't care).
2 X = don't care or dummy address bit.

Figure 6. READ, WRITE, WEN, WDS Sequence



INSTRUCTIONS (cont'd)

Write

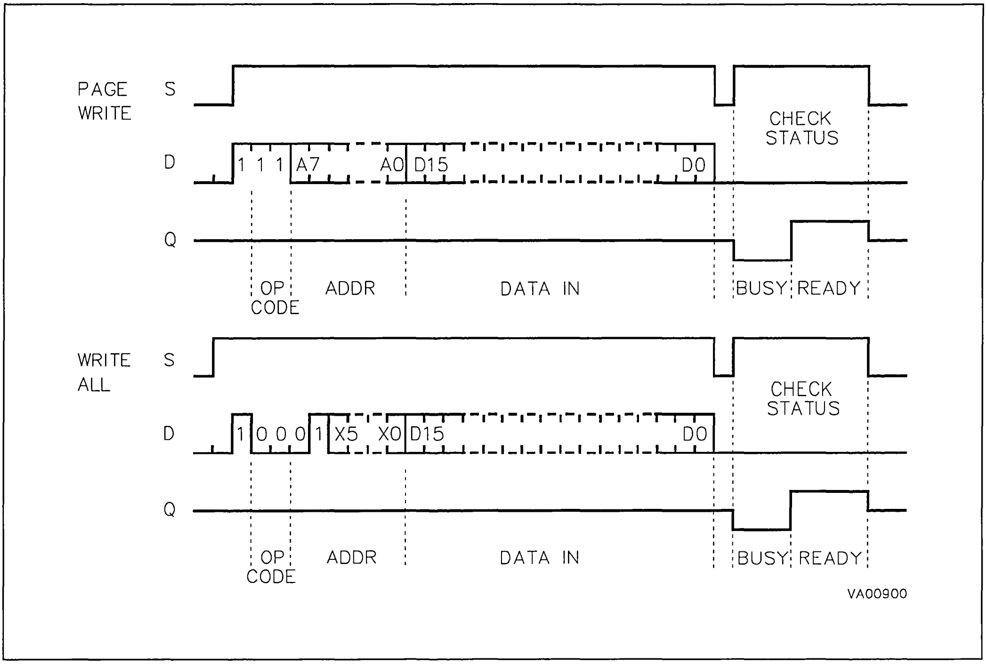
A Write instruction (WRITE) contains the address followed by the data to be written. The Write Enable signal (W) must be High before and during the WRITE instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the LSB of data has been received, the Chip Select signal (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle, providing that the address is NOT in the protected area. If Chip Select (S) is brought High again after a minimum time of tSLSH then the Data Output (D) will indicate the Busy/Ready status. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the receipt of each data word bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The write operation will proceded only if NONE of the addresses of the 1-4 data words has its address bits A6-A2 within the protected area. During the

Figure 7. PAWRITE, WRALL Sequence



INSTRUCTIONS (cont'd)

write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes all memory locations with the data word included in the instruction. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. During the write cycle, the Data Output indicates Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write Disable

The Write Disable instruction (WDS) disables all write operations. It should be used after all write instructions to disable writing to the memory and provide protection against noise and accidental write operations.

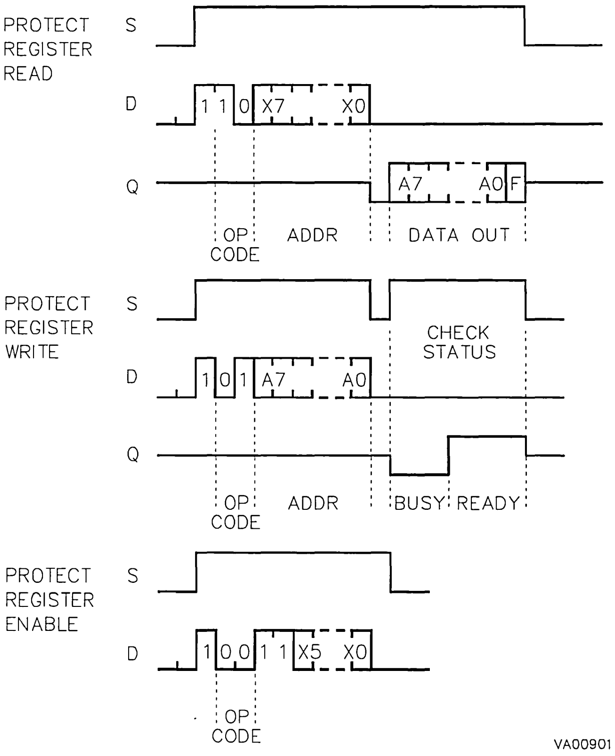
Write Disable does not affect the Read operations.

MEMORY WRITE PROTECTION

The ST93CS57 contains a specific Protect Register. This register stores the bottom address of the memory area which is protected against write together with two flag bits, the Protect Flag which indicates the protection status and an OTP bit which may be set to permanently disable access to the Protect Register and thus prevent any further changes to the memory protection setting. The address from which the memory is to be protected is loaded using the PRWRITE instruction, it may be read using the PRREAD instruction. There is a specific instruction, Protect Register Enable (PREN), to enable the protect instructions PRCLEAR, PRWRITE and PRDS, this is used together with the Protect Register Enable signal (PRE).

In order to program the protection the Write Enable instruction must first be executed. This is followed

Figure 8. PRREAD, PRWRITE, PREN Sequence


PROTECT REGISTER READ
S
D
1 1 0 X7 X0
Q
A7 A0 F
OP CODE
ADDR
DATA OUT
PROTECT REGISTER WRITE
S
CHECK STATUS
D
1 0 1 A7 A0
Q
OP CODE
ADDR
BUSY
READY
PROTECT REGISTER ENABLE
S
D
1 0 0 1 1 X5 X0
OP CODE
VA00901

MEMORY WRITE PROTECTION (cont'd)

by asserting both Write Enable (W) and Protect Register Enable (PRE) signals and executing the PREN instruction. The protection may then be set using Protect Register Write (PRWRITE), cleared using the Protect Register Clear (PRCLEAR) or set permanently using the Protect Register Disable (PRDS) instructions.

Protect Register Read

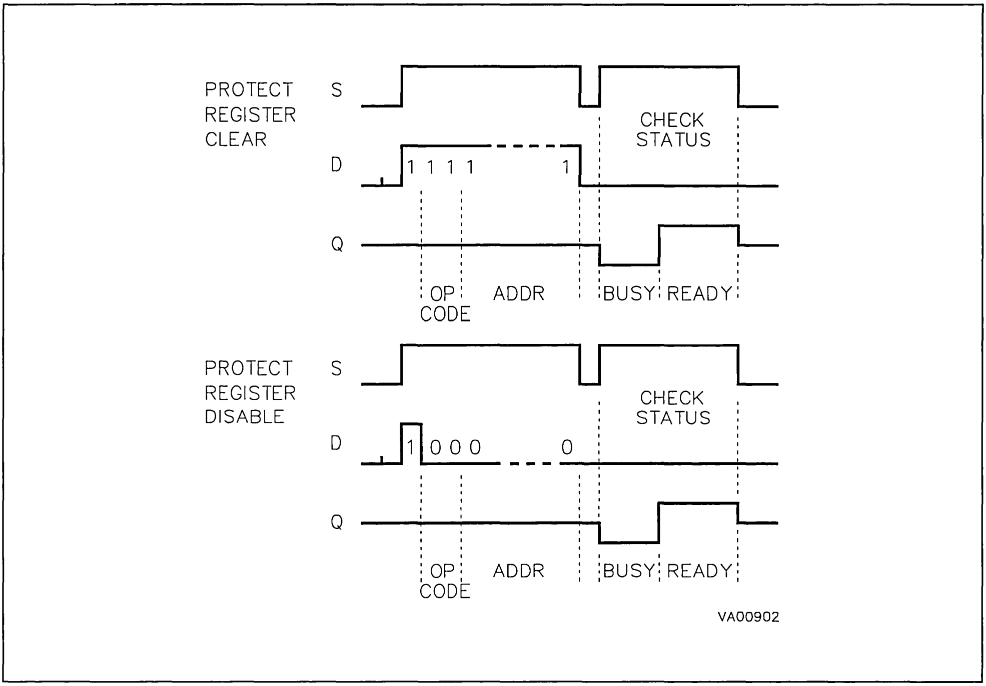
The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the address stored, followed by the Protect Flag status bit. The Protect Register Enable signal (PRE) must be High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish between the status when the Protect Register is cleared (all 1's) and when it is written with all 1's, users must check the Protect Flag status, not the Protect Register contents to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to enable the PRCLEAR, PRWRITE and PRDS instructions. A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution.

Figure 8. PRCLEAR, PRDS Sequence



MEMORY WRITE PROTECTION (cont'd)

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the protect register to all 1's, and thus enables all registers for WRITE and WRALL instructions. It also clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the protect register the address of the first memory location to be protected. After the instruction all memory locations equal to and above the location specified are protected from writing. The Protect Flag status bit is set to '0'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

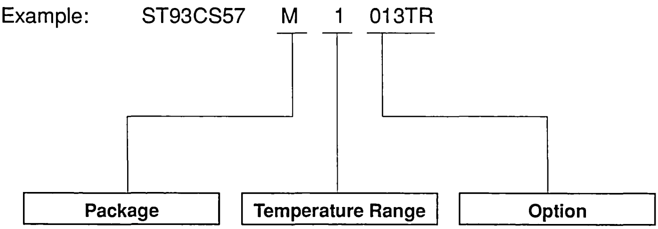
A PREN instruction must immediately precede the PRWRITE instruction, but it is not neccessary to execute first a PRCLEAR.

Protect Register Disable

Caution: The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which makes the Protect Register unalterable in the future, it does this by setting a One Time Programmable bit in the Protect Register. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRDS instruction.

ORDERING INFORMATION


Example: ST93CS57 M 1 013TR
Package
Temperature Range
Option

Package		Temperature Range		Option	
B	PSDIP8 0.4 mm Frame	1	0 to 70 °C	013TR	Tape & Reel
M	PSO8	3	–40 to 125 °C		
		6	–40 to 85 °C		

Parts are shipped with the memory content set at all “1’s” (0FFFFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

2.5V SERIAL ACCESS CMOS 4K bit (256 x 16) EEPROM

- MINIMUM 1,000,000 ERASE/WRITE CYCLES, WITH OVER 10 YEARS DATA RETENTION
- SINGLE 2.5V TO 5.5V SUPPLY VOLTAGE
- USER DEFINED WRITE PROTECT AREA
- PAGE WRITE MODE (4 WORDS)
- SELF-TIMED PROGRAMMING CYCLE WITH AUTO-ERASE
- BUSY/READY SIGNAL DURING PROGRAMMING
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME

PSDIP8 (B)
0.4mm Frame

PSO14 (ML)

DESCRIPTION

The ST93CS67 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple serial interface. The 4K bit memory is organised as 256 x 16 bit words. The ST93CS67 operates in read and write down to a 2.5V supply voltage.

The memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to manage memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data is then clocked out serially. The address pointer is automatically incremented after the word is output and it is possible, if the Chip Select input is held High, to output a sequential

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

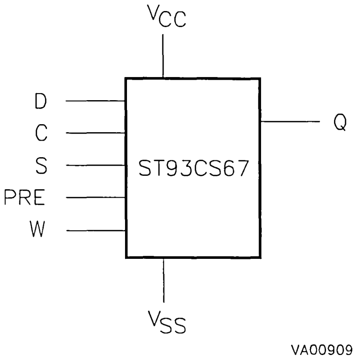


Figure 2A. DIP Pin Connections

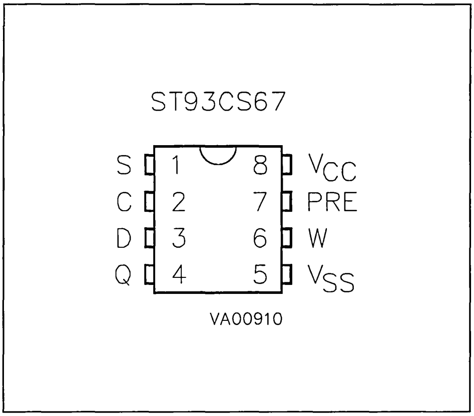
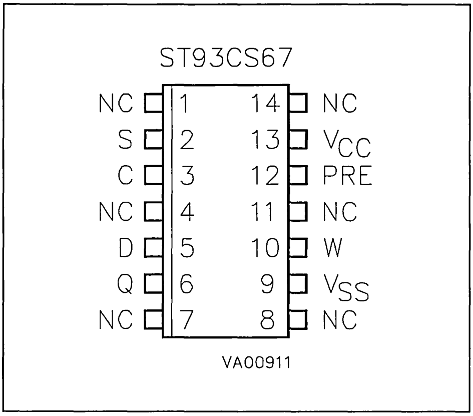


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (PSO14 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

stream of data words. In this way the memory can be read as a continuous data stream from 16 to 4096 bits long. Up to 4 words may be written in a single program cycle using the Page Write instruction. The memory may be 'erased', or set to a predetermined pattern, by using the Write All instruction. An external siganl controls Write Enable. A user defined area of the memory may be write protected. An external signal (PRE) enables access to the Protect Register which stores the lowest address to be write protected. Data may be permanently protected by programming an OTP bit which prevents further changes to the write protect starting address and the protect flag.

Programming is internally self-timed and does not require an erase cycle prior to the write instruction. The Write instruction writes 16 bits at one time into one of the 256 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, both providing that all addresses are outside the write protect area. After the start of the programming cycle a Busy/Ready signal is available on the Data Output when Chip Select is High.

The design of the ST93CS67 and the High Endurance CMOS technology used for its fabrication give a minimum Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of over 10 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

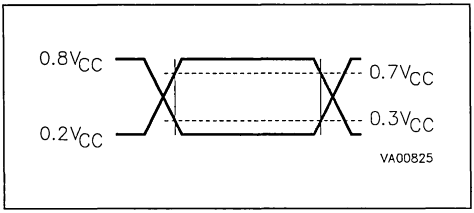


Table 3. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: This parameter is sampled only and not tested 100%.

Table 4. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = 0V		50	µA
V_{IL}	Input Low Voltage	$4.5V \leq V_{CC} \leq 5.5V$	–0.1	0.8	V
V_{IH}	Input High Voltage	$4.5V \leq V_{CC} \leq 5.5V$	2	V_{CC} + 1	V
V_{IL}	Input Low Voltage	$2.5V \leq V_{CC} \leq 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage	$2.5V \leq V_{CC} \leq 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low		500		ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid		500		ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSX}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid		500		ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		100		ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.
2. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.

Figure 4. Syncrounus Timing, Start and Op-Code Input

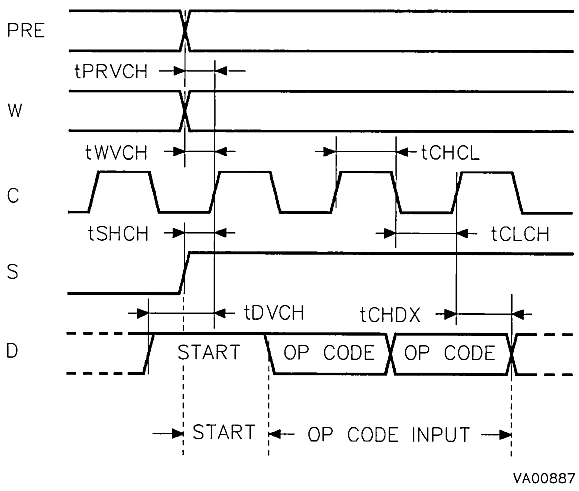
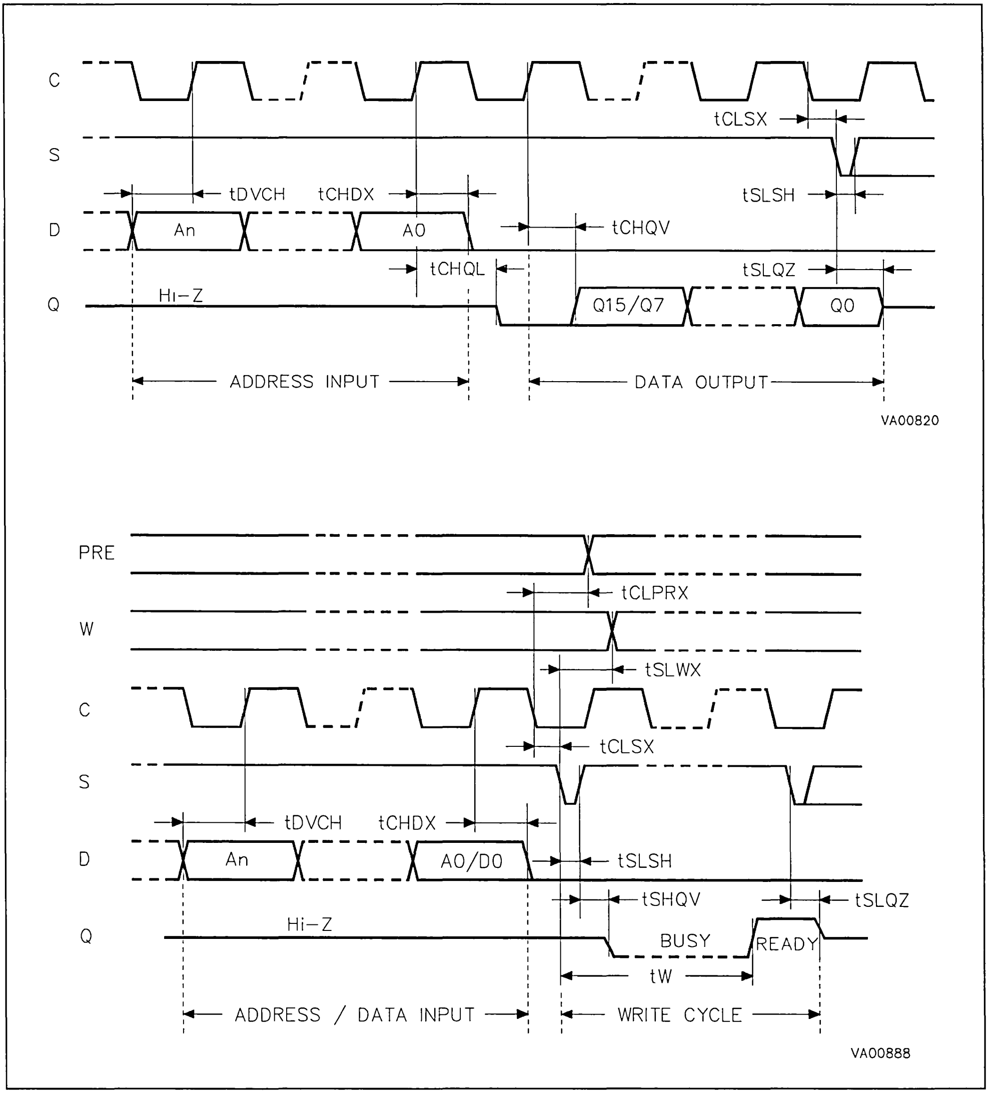


Figure 5. Syncronous Timing, Read or Write


C
S
D
Q
tCLSX
tDVCH
tCHDX
tSLSH
An
A0
tCHQV
tCHQL
tSLQZ
Hi-Z
Q15/Q7
Q0
ADDRESS INPUT
DATA OUTPUT
VA00820
PRE
W
C
S
D
Q
tCLPRX
tSLWX
tCLSX
tDVCH
tCHDX
An
A0/D0
tSLSH
tSHQV
tSLQZ
Hi-Z
BUSY
READY
tW
ADDRESS / DATA INPUT
WRITE CYCLE
VA00888

INSTRUCTIONS

The ST93CS67 has eleven instructions which are shown in Table 6. The op-codes of the instructions are made up of 2 bits, preceded by a start bit which is always at logic '1'. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the word which is made up of eight bits A7-A0.

The start sequence requires the Chip Select and Data Input signals to be set up before a Low to High transition of the Clock. For write instructions the Write Enable signal (W) must be High and for Protect Register instructions the Protect Register Enable signal (PRE) must also be High.

Read

The Read instruction (READ) outputs serial data on the Data Output Q. When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes follow the Low to High transition of the Clock. The memory will automatically increment the address and will clock out the next word as long as the Chip Select line is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable

When power is first applied to the ST93CS67 write operations are disabled. To enable write operations the Write Enable signal (W) must be High and a Write Enable instruction (WEN) must be executed. After the WEN instruction write operation remains enabled until either a Write Disable instruction (WDS) is executed or the supply is removed from the device.

Write

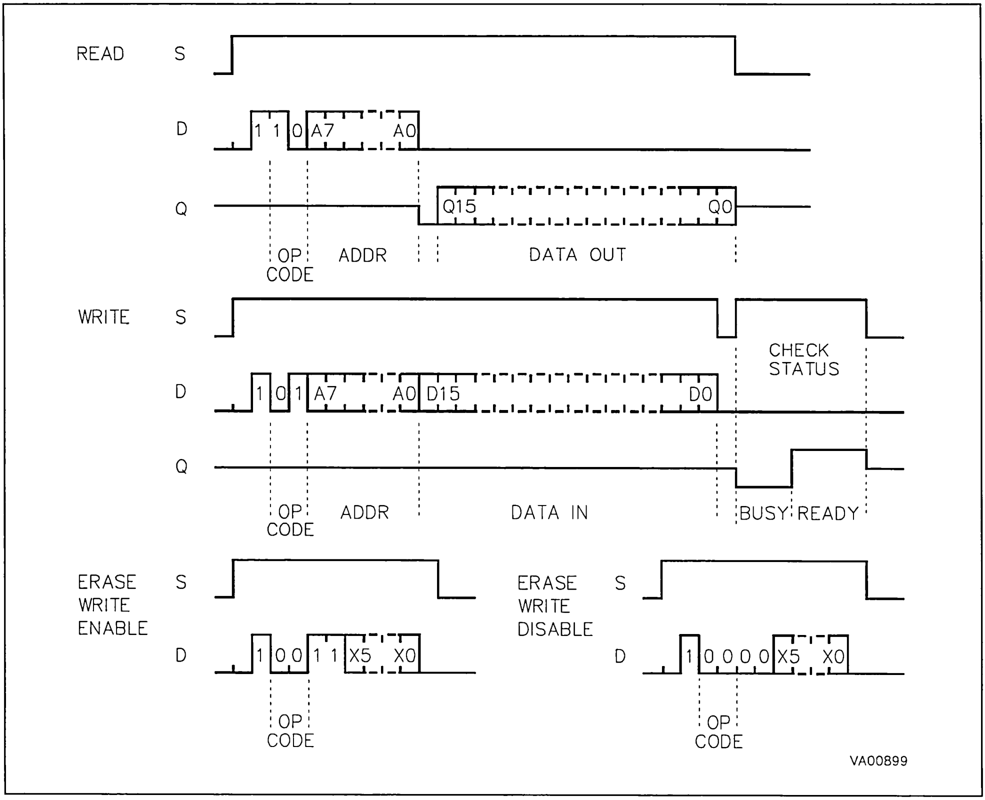
A Write instruction (WRITE) contains the address followed by the data to be written. The Write Enable signal (W) must be High before and during the WRITE instruction, but is subsequently ignored (don't care). Input address and data are read on

Table 6. Instruction Set

Instruction	Description	Op Code	PRE	W	Address	Data	Additional Information
READ	Read Data from memory	10	'0'	X	A7-A0	Q15-Q0	
WRITE	Write Data to memory	01	'0'	'1'	A7-A0	D15-D0	Write if address unprotected
PAWRITE	Page Write to memory	11	'0'	'1'	A7-A0	D15-D0	Write one to 4 words, if all addresses are unprotected
WRALL	Write All	00	'0'	'1'	01XXXXXX	D15-D0	Write all if Protect Register cleared
WEN	Write Enable	00	'0'	'1'	11XXXXXX		
WDS	Write Disable	00	'0'	'1'	00XXXXXX		
PRREAD	Protect Register Read	10	'1'	X	XXXXXXXX	Q8-Q0	Data Output is Protect Address (A7-A0) plus Protect Flag
PRWRITE	Protect Register Write	01	'1'	'1'	A7-A0		Data above A7-A0 is protected
PRCLEAR	Protect Register Clear	11	'1'	'1'	11111111		Protect Flag also cleared ('1')
PREN	Protect Register Enable	00	'1'	'1'	11XXXXXX		
PRDS	Protect Register Disable	00	'1'	'1'	00000000		OTP Flag set, prevents any further change to Protect Register

Note: X = don't care or dummy address bit.

Figure 6. READ, WRITE, WEN, WDS Sequence


READ
S
D
1 1 0 A7 A0
Q
Q15 Q0
OP CODE
ADDR
DATA OUT
WRITE
S
D
1 0 1 A7 A0 D15 D0
CHECK STATUS
Q
OP CODE
ADDR
DATA IN
BUSY
READY
ERASE WRITE ENABLE
S
D
1 0 0 1 1 X5 X0
OP CODE
ERASE WRITE DISABLE
S
D
1 0 0 0 0 X5 X0
OP CODE
VA00899

INSTRUCTIONS (cont'd)

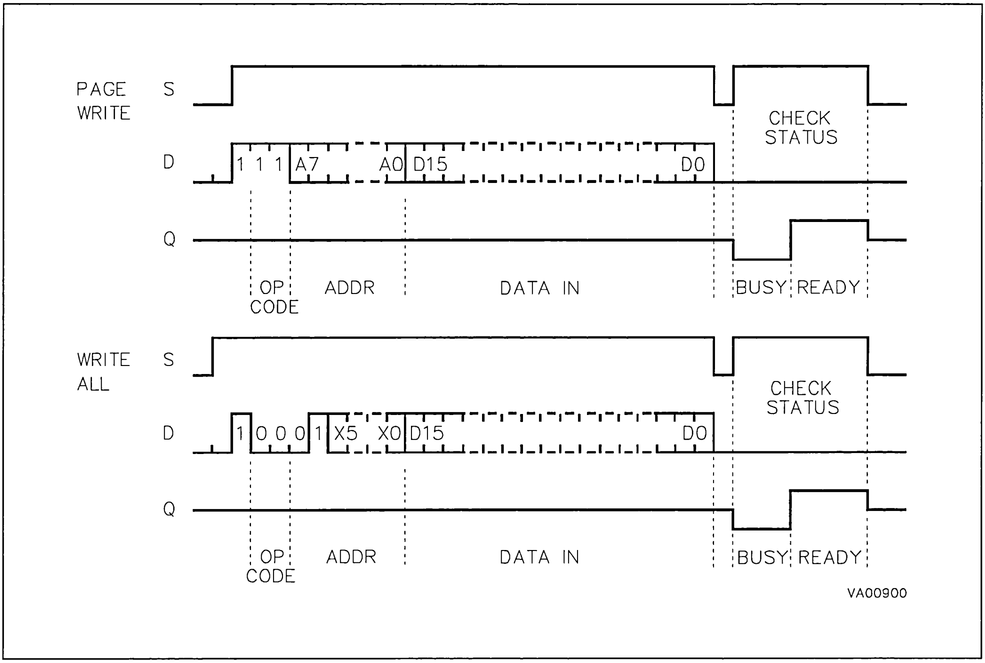
the Low to High transition of the clock. After the LSB of data has been received, the Chip Select signal (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle, providing that the address is NOT in the protected area. If Chip Select (S) is brought High again after a minimum time of tSLSH then the Data Output (D) will indicate the Busy/Ready status. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. After the receipt of each data word bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The write operation will proceded only if NONE of the addresses of the 1-4 data words has its address bits A7-A2 within the protected area. During the write cycle, the Data Output will indicate Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Figure 7. PAWRITE, WRALL Sequence



INSTRUCTIONS (cont'd)

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes all memory locations with the data word included in the instruction. The Write Enable signal (W) must be High before and during the Write instruction, but is subsequently ignored (don't care). Input address and data are read on the Low to High transition of the clock. During the write cycle, the Data Output indicates Busy D = '0' and after the cycle is completed and the memory is ready for another instruction, Ready D = '1'.

Write Disable

The Write Disable instruction (WDS) disables all write operations. It should be used after all write instructions to disable writing to the memory and provide protection against noise and accidental write operations.

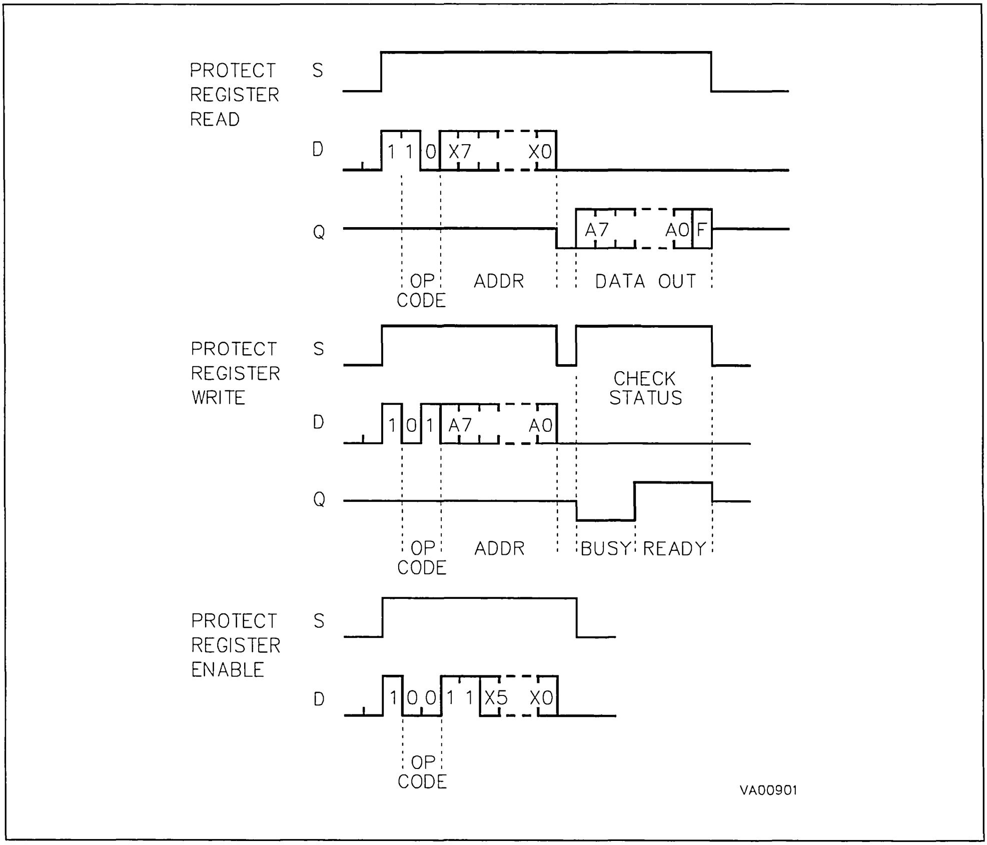
Write Disable does not affect the Read operations.

MEMORY WRITE PROTECTION

The ST93CS67 contains a specific Protect Register. This register stores the bottom address of the memory area which is protected against write together with two flag bits, the Protect Flag which indicates the protection status and an OTP bit which may be set to permanently disable access to the Protect Register and thus prevent any further changes to the memory protection setting. The address from which the memory is to be protected is loaded using the PRWRITE instruction, it may be read using the PRREAD instruction. There is a specific instruction, Protect Register Enable (PREN), to enable the protect instructions PRCLEAR, PRWRITE and PRDS, this is used together with the Protect Register Enable signal (PRE).

In order to program the protection the Write Enable instruction must first be executed. This is followed by asserting both Write Enable (W) and Protect Register Enable (PRE) signals and executing the PREN instruction. The protection may then be set using Protect Register Write (PRWRITE), cleared using the Protect Register Clear (PRCLEAR) or set permanently using the Protect Register Disable (PRDS) instructions.

Figure 8. PRREAD, PRWRITE, PREN Sequence


PROTECT REGISTER READ
S
D
1 1 0 X7 X0
Q
A7 A0 F
OP CODE
ADDR
DATA OUT
PROTECT REGISTER WRITE
S
D
1 0 1 A7 A0
CHECK STATUS
Q
OP CODE
ADDR
BUSY
READY
PROTECT REGISTER ENABLE
S
D
1 0 0 1 1 X5 X0
OP CODE
VA00901

MEMORY WRITE PROTECTION (cont'd)

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the address stored, followed by the Protect Flag status bit. The Protect Register Enable signal (PRE) must be High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish between the status when the Protect Register is cleared (all 1's) and when it is written with all 1's, users must check the Protect Flag status, not the Protect Register contents to ascertain the setting of the memory protection.

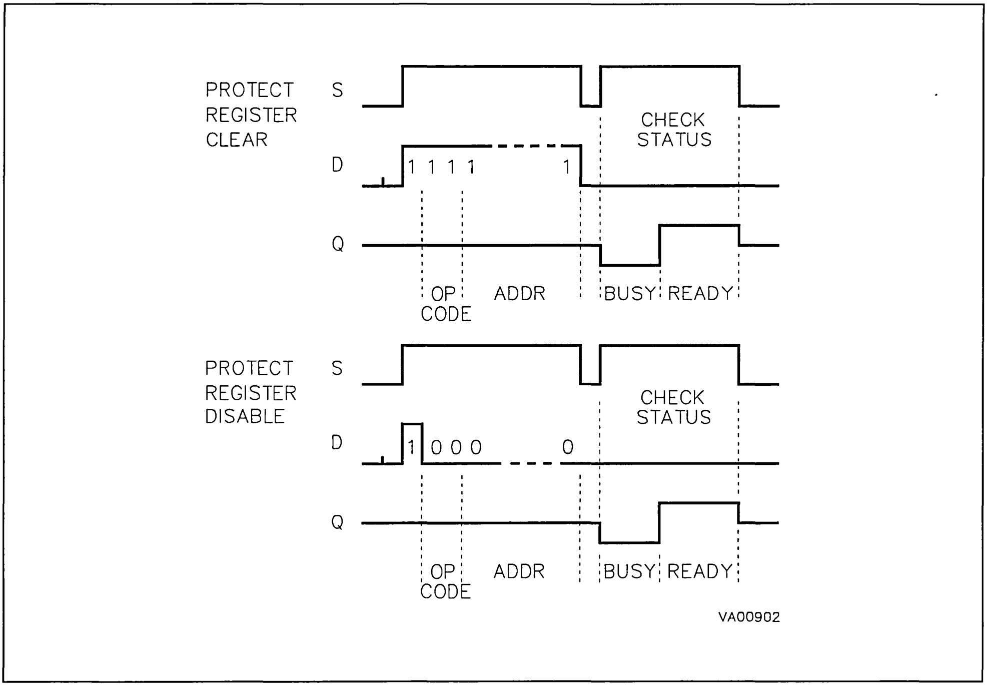
Protect Register Enable

The Protect Register Enable instruction (PREN) is used to enable the PRCLEAR, PRWRITE and PRDS instructions. A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the protect register to all 1's, and thus enables all registers for WRITE and WRALL instructions. It also clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write

Figure 9. PRCLEAR, PRDS Sequence



MEMORY WRITE PROTECTION (cont'd)

Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the protect register the address of the first memory location to be protected. After the instruction all memory locations equal to and above the location specified are protected from writing. The Protect Flag status bit is set to '0'. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRWRITE instruction, but it is not neccessary to execute first a PRCLEAR.

Protect Register Disable

Caution: The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which makes the Protect Register unalterable in the future, it does this by setting a One Time Programmable bit in the Protect Register. Both the Protect Enable (PRE) and Write Enable (W) signals must be High before and during the instruction execution, but are subsequently ignored (don't care).

A PREN instruction must immediately precede the PRDS instruction.

ORDERING INFORMATION

Example: ST93CS67 ML 1 013TR

Package	
B	PSDIP8 0.4 mm Frame
ML	PSO14

Temperature Range	
1	0 to 70 °C
3	–40 to 125 °C
6	–40 to 85 °C

Option	
013TR	Tape & Reel

Parts are shipped with the memory content set at all “1’s” (0FFFFh).

For a list of available options of Package and Temperature Range refer to the Selector Guide in this Data Book or to the current Memory Shortform that will be periodically updated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

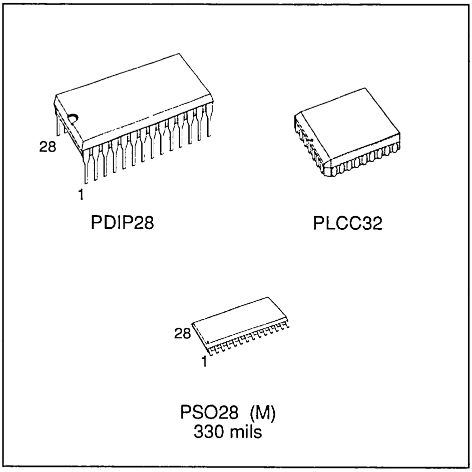
PARALLEL ACCESS EEPROM

SGS-THOMSON
MICROELECTRONICS

M28C64C

PARALLEL ACCESS CMOS 64K (8K x 8) EEPROM

- FAST ACCESS TIME: 150, 200ns
- SINGLE SUPPLY VOLTAGE: 5V ± 10%
- LOW POWER CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- FAST WRITE CYCLE:
  - 32 Bytes Page Write Operation
  - Byte Or Page Write Cycle: 5ms
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS AND DATA LATCHED ON-CHIP



DESCRIPTION

The M28C64C is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time (150ns) with low power dissipation and requires a 5V power supply.

Table 1. Signal Names

A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

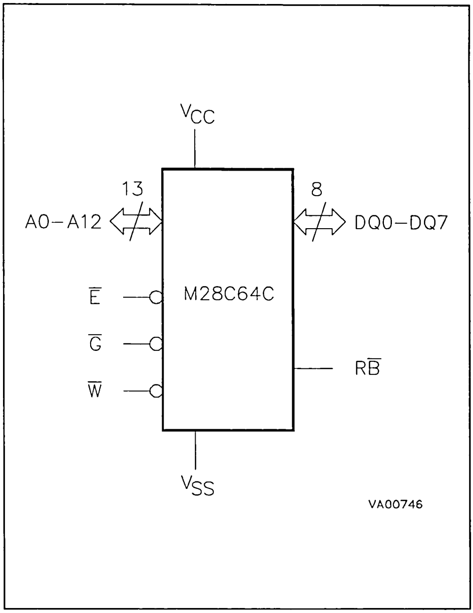
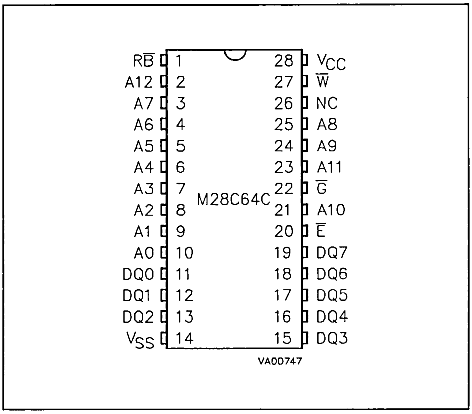


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 6	0 to 70 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input or Output Voltages		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)		2000	V

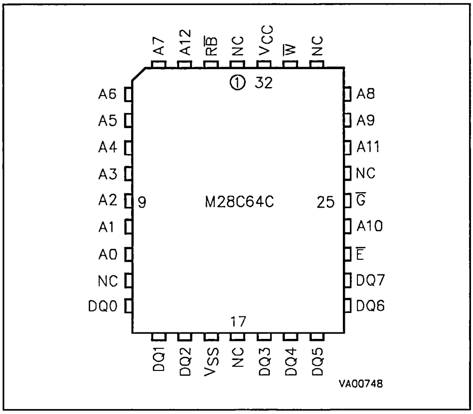
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2A. DIP Pin Connections


RB̅ 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
VSS 14
28 VCC
27 W̅
26 NC
25 A8
24 A9
23 A11
22 G̅
21 A10
20 E̅
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
M28C64C
VA00747

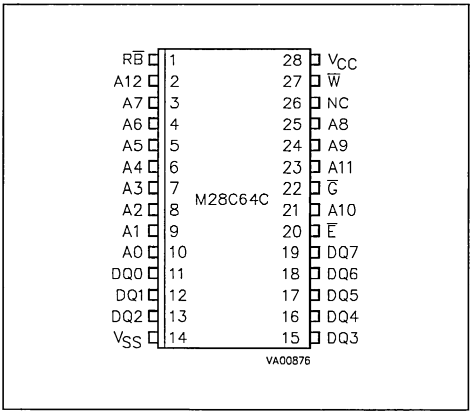
Warning: NC = No Connection

Figure 2B. LCC Pin Connections


A7
A12
RB̅
NC
VCC
W̅
NC
① 32
A6
A5
A4
A3
A2
9
A1
A0
NC
DQ0
A8
A9
A11
NC
25
G̅
A10
E̅
DQ7
DQ6
M28C64C
17
DQ1
DQ2
VSS
NC
DQ3
DQ4
DQ5
VA00748

Warning: NC = No Connection

Figure 2C. SO Pin Connections


RB̅ 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
VSS 14
28 VCC
27 W̅
26 NC
25 A8
24 A9
23 A11
22 G̅
21 A10
20 E̅
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
M28C64C
VA00876

Warning: NC = No Connection

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28C64C supports 32 byte page write operation.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C64C through the I/O pins.

Figure 3. Block Diagram

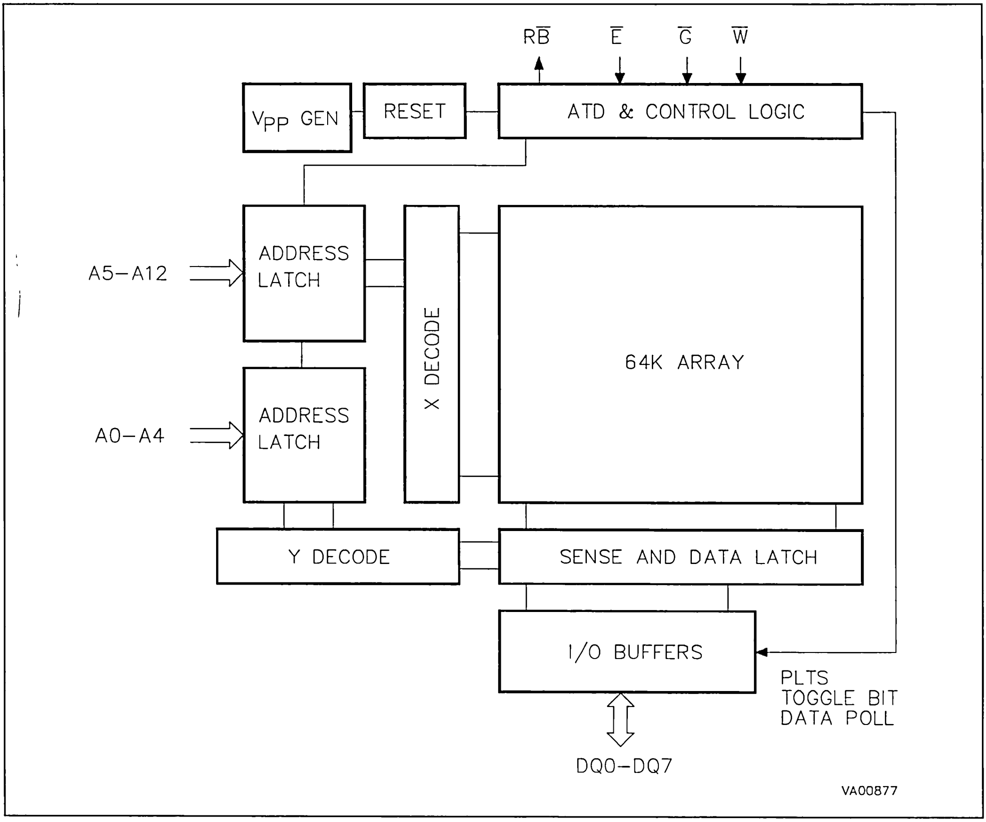

RB
E
G
W
VPP GEN
RESET
ATD & CONTROL LOGIC
A5–A12
ADDRESS LATCH
A0–A4
ADDRESS LATCH
X DECODE
64K ARRAY
Y DECODE
SENSE AND DATA LATCH
I/O BUFFERS
PLTS
TOGGLE BIT
DATA POLL
DQ0–DQ7
VA00877

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

PIN DESCRIPTION (cont'd)

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C64C.

Ready/Busy (R$\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

Read

The M28C64C is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28C64C supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion within 5ms.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5 - A12 must be the same for all bytes. The page write can be initiated during any byte write operation. Following the first byte write instruction the host may send another address and data up to a maximum of 100µs after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. If a transition of $\overline{E}$ or $\overline{W}$ is not detected within 100µs, the internal programming cycle will start.

Microcontroller Control Interface

The M28C64C provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the R$\overline{B}$ signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
R = Reserved, definition pending
PLTS = Page Load Time Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C64C also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input Output Waveforms

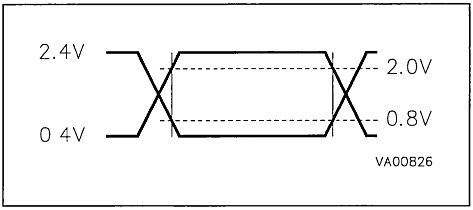


Figure 6. AC Testing Load Circuit

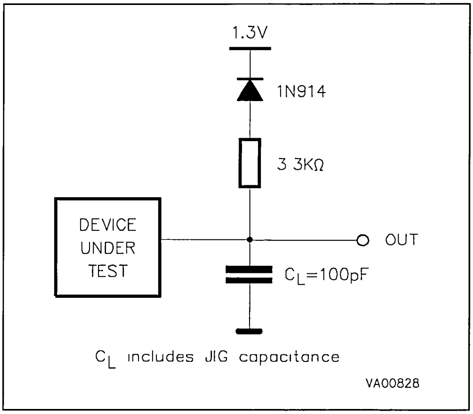


Table 4. Capacitance (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		12	pF

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is sampled only and not tested 100%.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		2	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} -0.3V$		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

OPERATION (cont'd)

Page Load Timer Status (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$ up to 100µs after the previous byte. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low. DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The R$\overline{B}$ pin provides a signal at its open drain output which is low during the erase/write cycle, but which is relased at the completing of the programming cycle.

Table 6. Read Mode AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C, V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28C64C				Unit
				-150		-200		
				min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$G = V_{IL}$		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		100	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-z	$\overline{G} = V_{IL}$	0	50	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Note: 1. Output float is defined as the point where data is no longer driving. The parameter is sampled only and not 100% tested.

Figure 7. Read Mode AC Waveforms

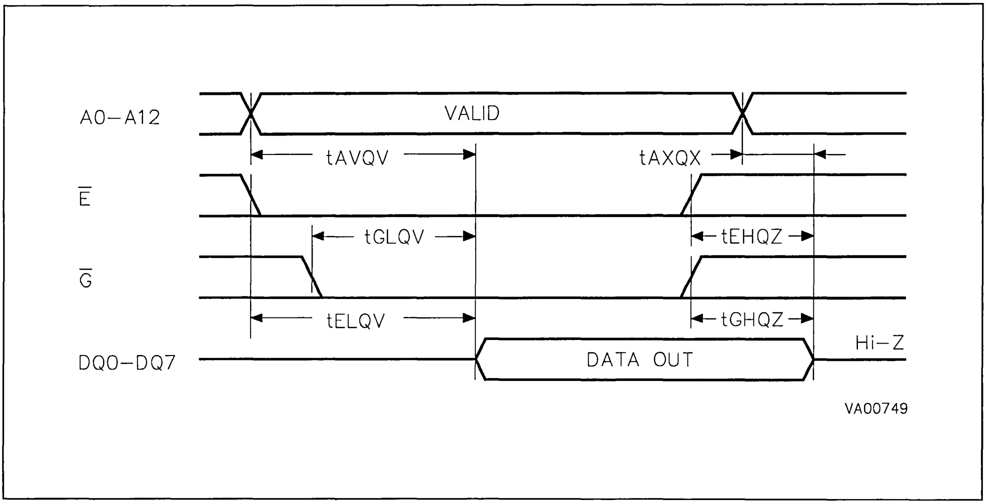

A0–A12
VALID
tAVQV
tAXQX
$\overline{E}$
tGLQV
tEHQZ
$\overline{G}$
tELQV
tGHQZ
DQ0–DQ7
DATA OUT
Hi–Z
VA00749

Table 7. Write Mode AC Characteristics
(T_A = 0 to 70 °C or –40 to 85°C, V_{CC} = 5V ±10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		150		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		150		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		150		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		150		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time			100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		50	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		50	ns

Note: 1. With a 3.3kΩ pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

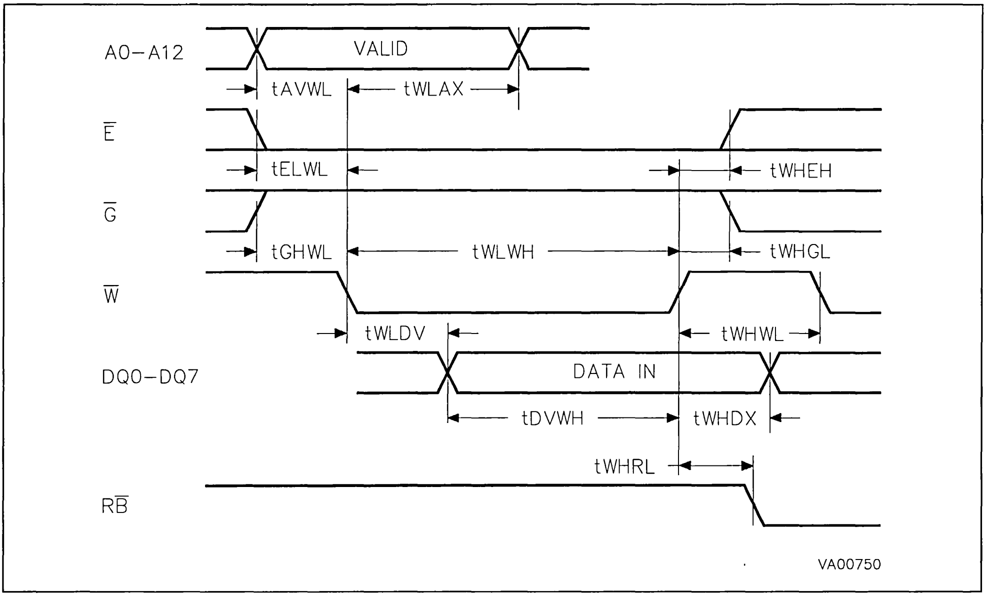

A0–A12
VALID
tAVWL
tWLAX
$\overline{E}$
tELWL
tWHEH
$\overline{G}$
tGHWL
tWLWH
tWHGL
$\overline{W}$
tWLDV
tWHWL
DQ0–DQ7
DATA IN
tDVWH
tWHDX
tWHRL
R$\overline{B}$
VA00750

Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

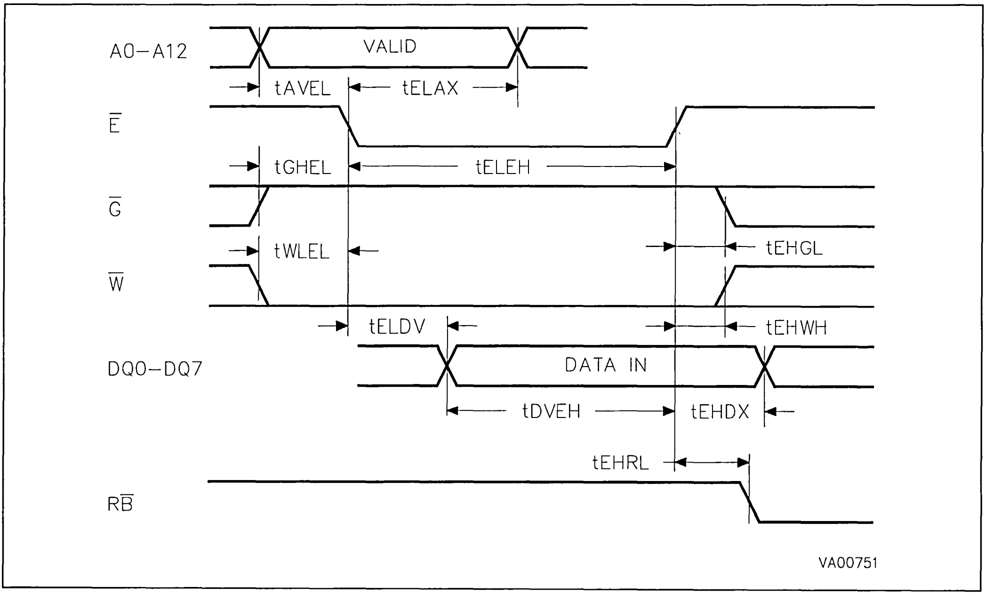

A0–A12
VALID
tAVEL
tELAX
$\overline{E}$
tGHEL
tELEH
$\overline{G}$
tWLEL
tEHGL
$\overline{W}$
tELDV
tEHWH
DQ0–DQ7
DATA IN
tDVEH
tEHDX
tEHRL
R$\overline{B}$
VA00751

Figure 10. Page Write Mode AC Waveforms

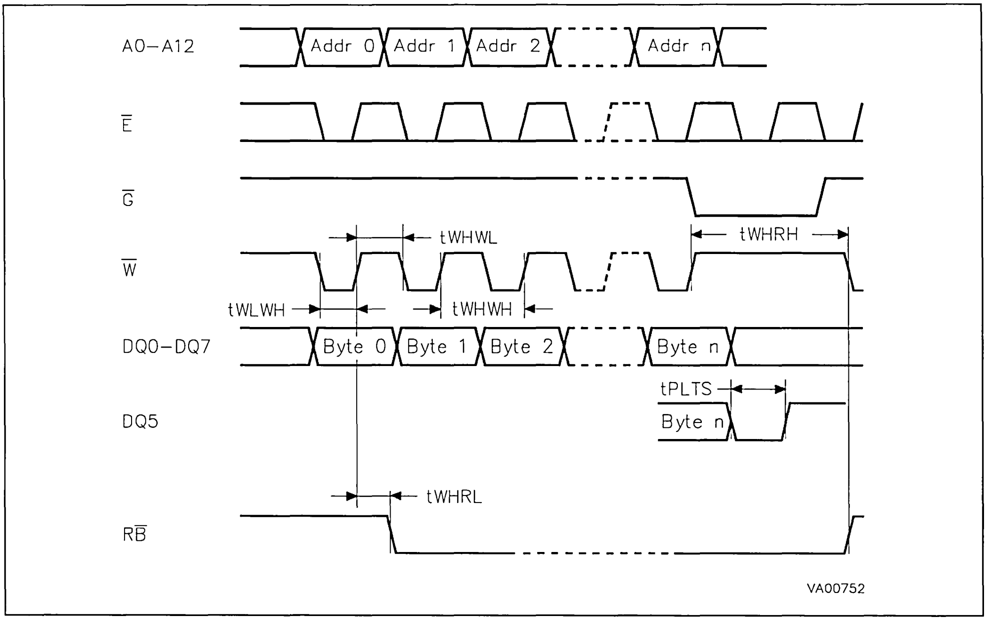

A0–A12
Addr 0
Addr 1
Addr 2
Addr n
E
G
W
tWHWL
tWHRH
tWLWH
tWHWH
DQ0–DQ7
Byte 0
Byte 1
Byte 2
Byte n
tPLTS
DQ5
Byte n
tWHRL
RB
VA00752

Figure 11. Data Polling Waveforms Sequence

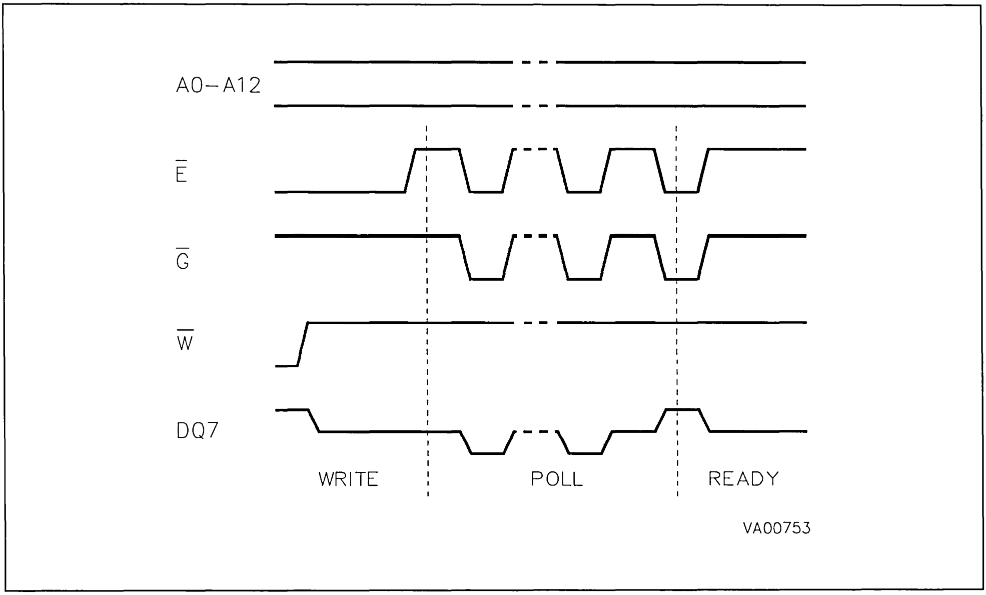
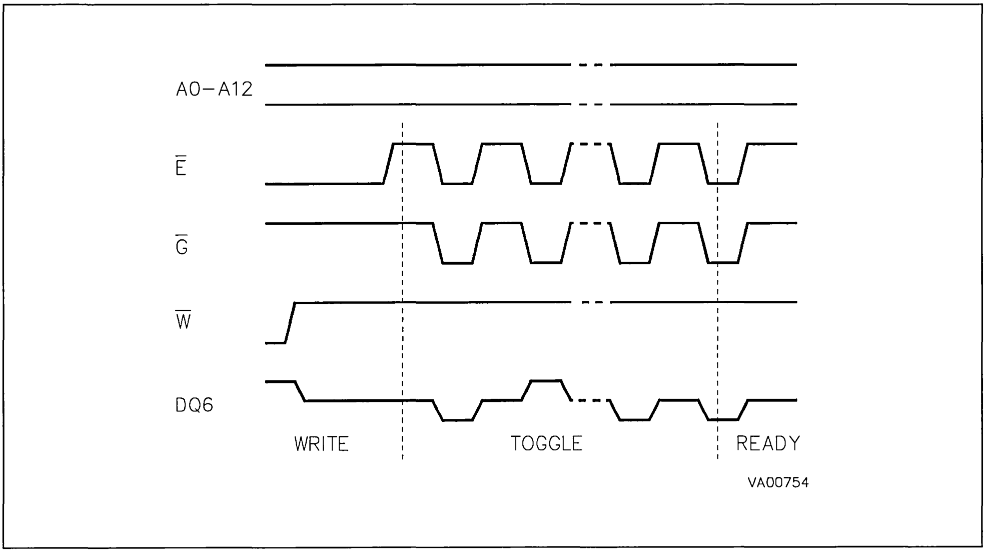

A0–A12
E
G
W
DQ7
WRITE
POLL
READY
VA00753

Figure 12. Toggle Bit Waveforms Sequence


A0–A12
$\overline{E}$
$\overline{G}$
$\overline{W}$
DQ6
WRITE
TOGGLE
READY
VA00754

ORDERING INFORMATION

Example: M28C64C -150 K 1

Speed	
-150	150 ns
-200	200 ns

Package	
K	PLCC32
P	PDIP28
M	PSO28 330 mils

Temperature Range	
1	0 to 70 °C
6	–40 to 85 °C

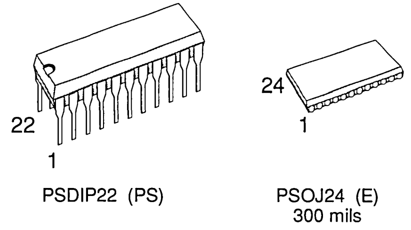
For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

FAST SRAM

VERY FAST CMOS 64K x 1 SRAM

- 64K x 1 CMOS FAST SRAM
- EQUAL CYCLE AND ACCESS TIMES: 10, 12, 15, 20ns
- SEPARATE DATA INPUT AND DATA OUTPUT PINS
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES


22
1
PSDIP22 (PS)
24
1
PSOJ24 (E)
300 mils

DESCRIPTION

The M621064 is a 64K (65,536 bit) Fast CMOS SRAM, organized as 65,536 words by 1 bit. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

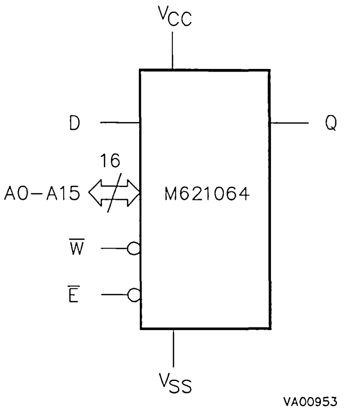

V_{CC}
D
Q
16
A0–A15
M621064
$\overline{W}$
$\overline{E}$
V_{SS}
VA00953

Table 1. Signal Names

A0 - A15	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. SDIP Pin Connections

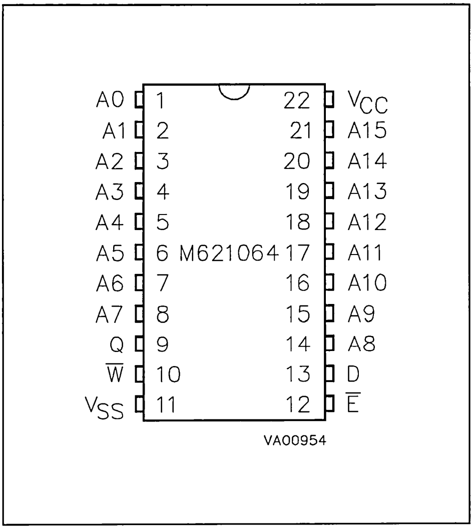
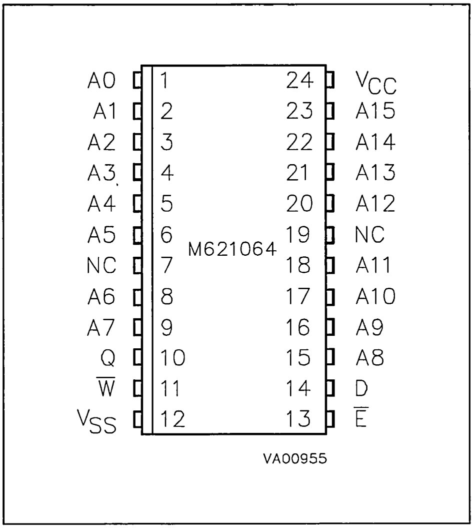

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
Q 9
W̄ 10
VSS 11
M621064
22 VCC
21 A15
20 A14
19 A13
18 A12
17 A11
16 A10
15 A9
14 A8
13 D
12 Ē
VA00954

Figure 2B. SOJ Pin Connections


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
NC 7
A6 8
A7 9
Q 10
W̄ 11
VSS 12
M621064
24 VCC
23 A15
22 A14
21 A13
20 A12
19 NC
18 A11
17 A10
16 A9
15 A8
14 D
13 Ē
VA00955

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	25	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power
Read	V_{IL}	V_{IH}	X	Data Output	Active
Write	V_{IL}	V_{IL}	Data Input	Hi-Z	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M621064 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Chip Enable ($\overline{E}$) asserted Low. This provides access to data from one of the 65,536 locations in the static memory array, specified by the 16 address inputs. Valid data will be available at the Q output pin within t_{AVQV} after the last stable address, if $\overline{E}$ is Low. If Chip Enable access time is not met, data access will be measured from the limiting parameter (t_{ELQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M621064 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ Low and $\overline{W}$ High), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVHE} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M621064 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ High). Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

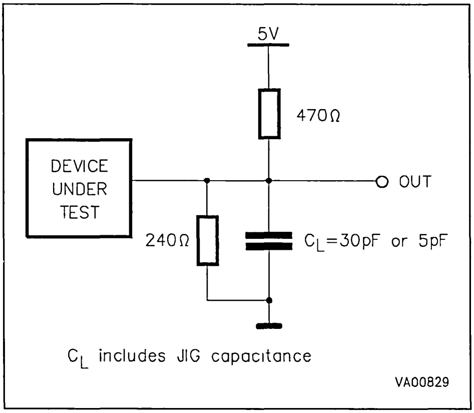


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [(2)]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	$V_{CC} = 5.5V$		160	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V$, $\overline{E} = V_{IH}$, f = 0		40	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V$, $\overline{E} \ge V_{CC} - 0.2V$, f = 0		10	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Table 6. Read Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M621064								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	10		12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		10		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		10		12		15		20	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		3		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns

Notes: 1. C_L = 30pF
2. C_L = 5pF

Figure 4. Read Mode AC Waveforms

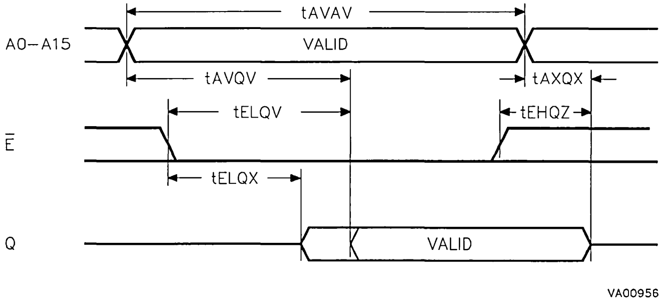


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M621064								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	10		12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	5	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	7		9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	5		7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	5		7		8		10		ns

Note: 1. C_L = 5pF

Figure 5. Write Enable Controlled, Write AC Waveforms

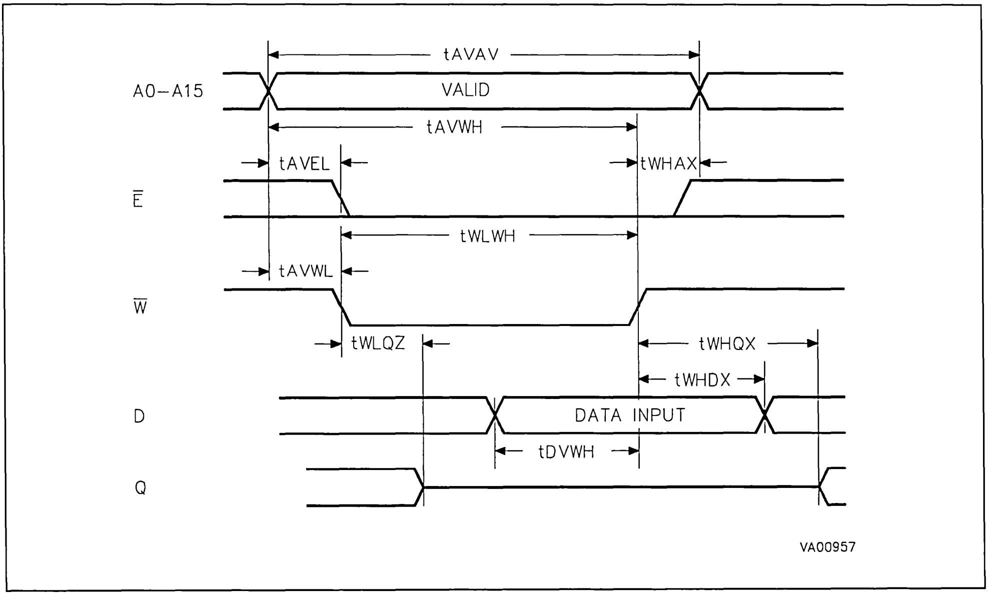
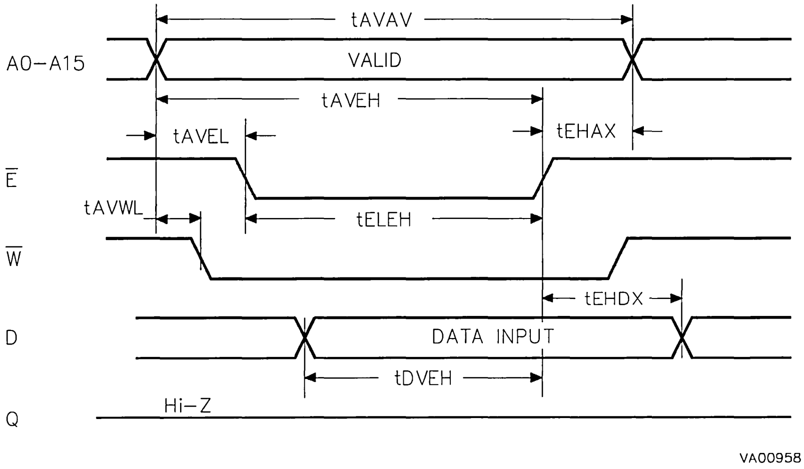

tAVAV
A0–A15
VALID
tAVWH
tAVEL
tWHAX
$\overline{E}$
tWLWH
tAVWL
$\overline{W}$
tWLQZ
tWHQX
tWHDX
D
DATA INPUT
tDVWH
Q
VA00957

Figure 6. Chip Enable Controlled, Write AC Waveforms


tAVAV
A0–A15
VALID
tAVEH
tAVEL
tEHAX
E
tAVWL
tELEH
W
tEHDX
D
DATA INPUT
tDVEH
Q
Hi–Z
VA00958

ORDERING INFORMATION

Example: M621064 -10 E 1

Speed	
-10	10 ns
-12	12 ns
-15	15 ns
-20	20 ns

Package	
PS	PSDIP22
E	PSOJ28 300 mils

Temperature Range	
1	0 to 70 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

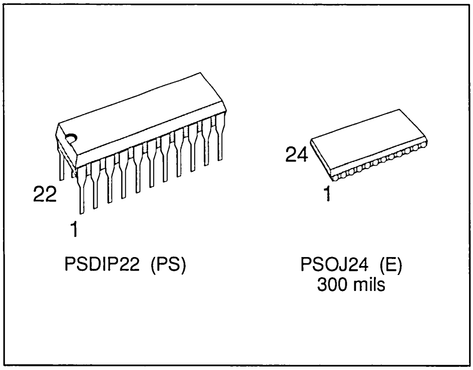
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M624016

VERY FAST CMOS 16K x 4 SRAM

- 16K x 4 CMOS FAST SRAM
- EQUAL CYCLE AND ACCESS TIMES: 10, 12, 15, 20ns
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mils PACKAGES


22
1
PSDIP22 (PS)
24
1
PSOJ24 (E)
300 mils

DESCRIPTION

The M624016 is a 64K (65,536 bit) Fast CMOS SRAM, organized as 16,384 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A13	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

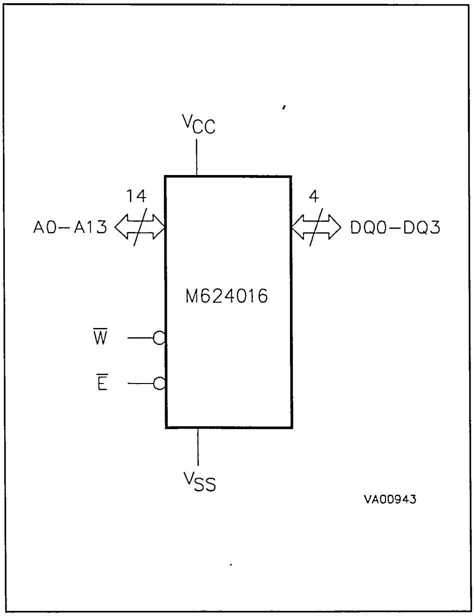

V_{CC}
14
A0–A13
4
DQ0–DQ3
M624016
$\overline{W}$
$\overline{E}$
V_{SS}
VA00943

Figure 2A. SDIP Pin Connections

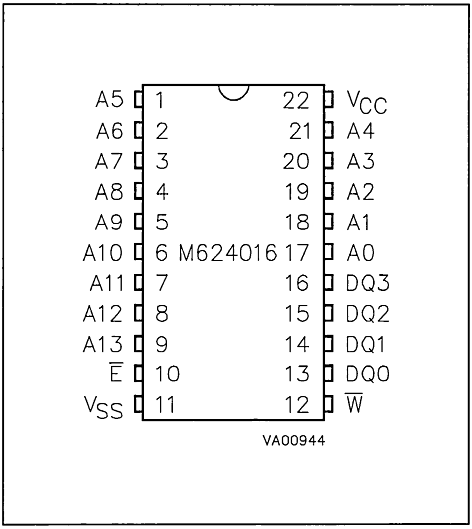
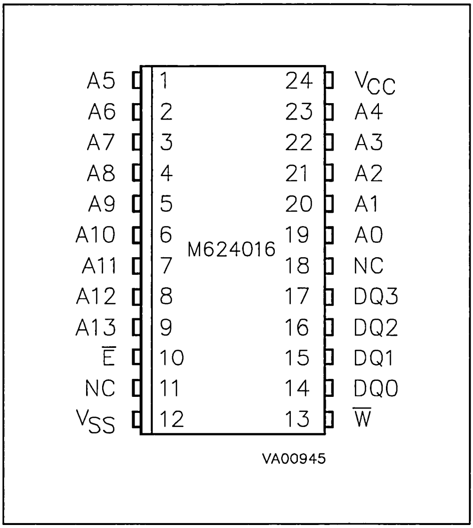

A5 1
A6 2
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
$\overline{E}$ 10
V_{SS} 11
M624016
22 V_{CC}
21 A4
20 A3
19 A2
18 A1
17 A0
16 DQ3
15 DQ2
14 DQ1
13 DQ0
12 $\overline{W}$
VA00944

Figure 2B. SOJ Pin Connections


A5 1
A6 2
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
$\overline{E}$ 10
NC 11
V_{SS} 12
M624016
24 V_{CC}
23 A4
22 A3
21 A2
20 A1
19 A0
18 NC
17 DQ3
16 DQ2
15 DQ1
14 DQ0
13 $\overline{W}$
VA00945

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	25	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	Data Output	Active
Write	V_{IL}	V_{IL}	Data Input	Active
Deselect	V_{IH}	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M624016 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Chip Enable ($\overline{E}$) asserted Low. This provides access to data from four of the 65,536 locations in the static memory array, specified by the 14 address inputs. Valid data will be available at the four Q output pins within t_{AVQV} after the last stable address, providing $\overline{E}$ is Low. If Chip Enable access time is not met, data access will be measured from the limiting parameter t_{ELQV}, rather than the address. Data out may be indeterminate at t_{ELQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M624016 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Chip Enable $\overline{E}$ or $\overline{W}$ must be deasserted during Access transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL}, respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ Low, and $\overline{W}$ High), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$, whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M624016 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E}$ High). Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$, as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

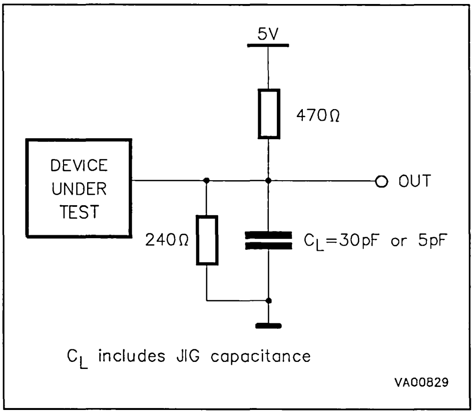


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [(2)]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	$V_{CC} = 5.5V$		160	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E} = V_{IH}, f = 0$		40	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E} \geq V_{CC} - 0.2V, f = 0$		10	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2$ 2V
3. All other Inputs at $V_{IL} \leq 0$ 2V or $V_{IH} \geq V_{CC} - 0.2V$

Table 6. Read Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624016								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	10		12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		10		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		10		12		15		20	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		3		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns

Notes: 1. C_L = 30pF
2. C_L = 5pF

Figure 4. Read Mode AC Waveforms

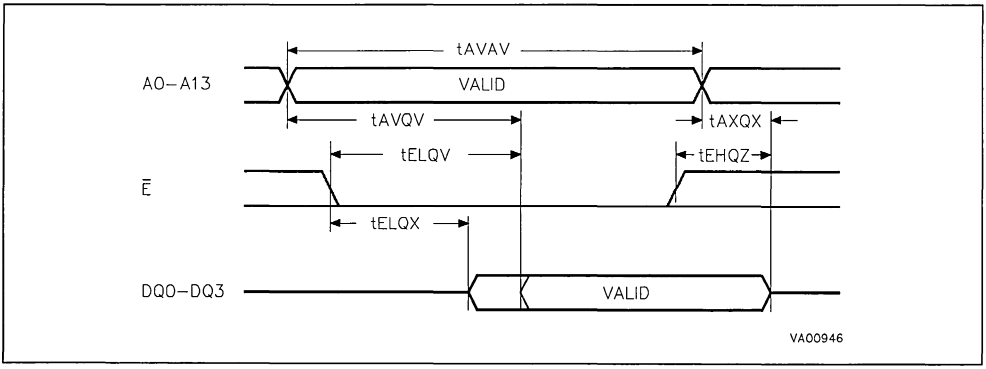
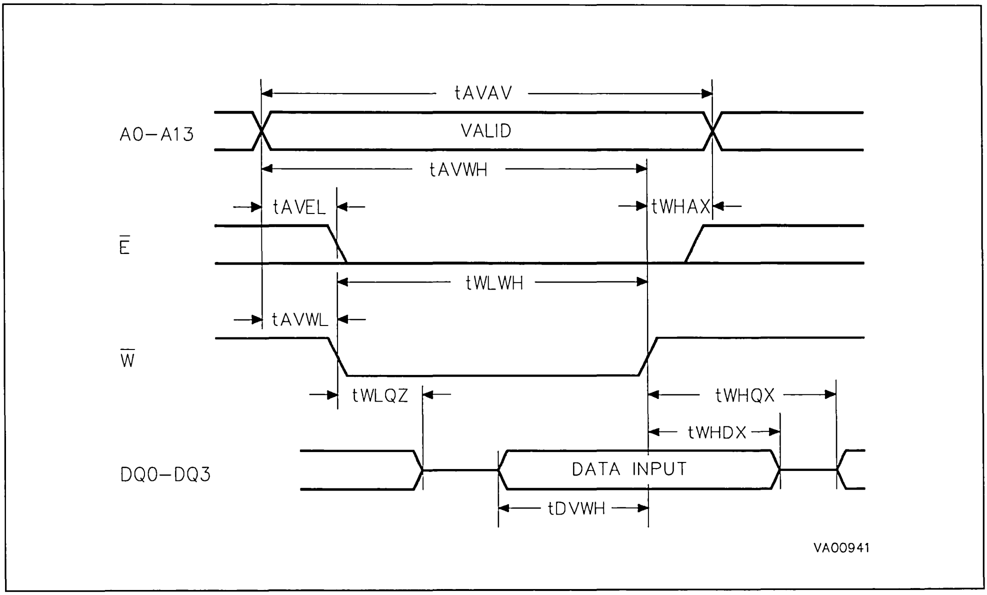


Table 7. Write Mode AC Characteristics (T$_A$ = 0 to 70°C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	M624016								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	10		12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	5	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	7		9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	5		7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	5		7		8		10		ns

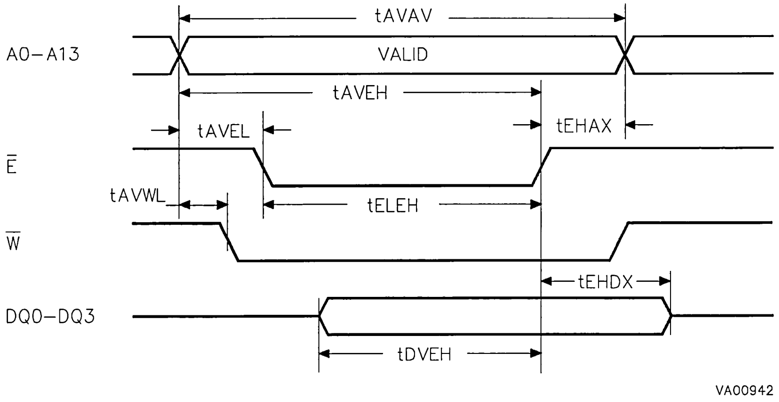
Note: 1. C_L = 5pF

Figure 5. Write Enable Controlled, Write AC Waveforms



tAVAV
A0–A13
VALID
tAVWH
tAVEL
tWHAX
$\overline{E}$
tWLWH
tAVWL
$\overline{W}$
tWLQZ
tWHQX
tWHDX
DQ0–DQ3
DATA INPUT
tDVWH
VA00941

Figure 6. Chip Enable Controlled, Write AC Waveforms


tAVAV
A0–A13
VALID
tAVEH
tAVEL
tEHAX
$\overline{E}$
tAVWL
tELEH
$\overline{W}$
tEHDX
DQ0–DQ3
tDVEH
VA00942

ORDERING INFORMATION

Example: M624016 -10 E 1

Speed	
-10	10 ns
-12	12 ns
-15	15 ns
-20	20 ns

Package	
PS	PSDIP22
E	PSOJ24 300 mils

Temperature Range	
1	0 to 70 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

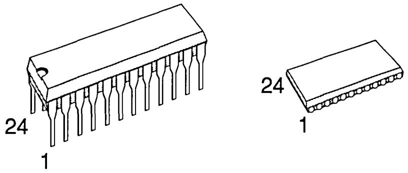
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M624017

VERY FAST CMOS 16K x 4 SRAM WITH OUTPUT ENABLE

- 16K x 4 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIME: 10, 12, 15, 20ns
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



PSDIP24 (PS)

PSOJ24 (E)
300 mils

DESCRIPTION

The M624017 is a 64K (65,536 bit) Fast CMOS SRAM, organized as 16,384 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A13	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

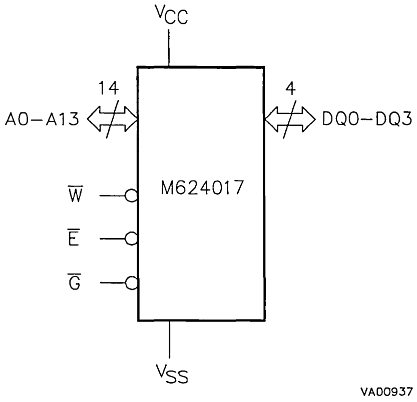
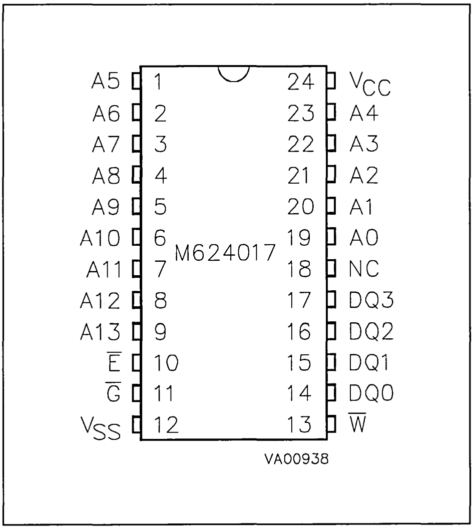
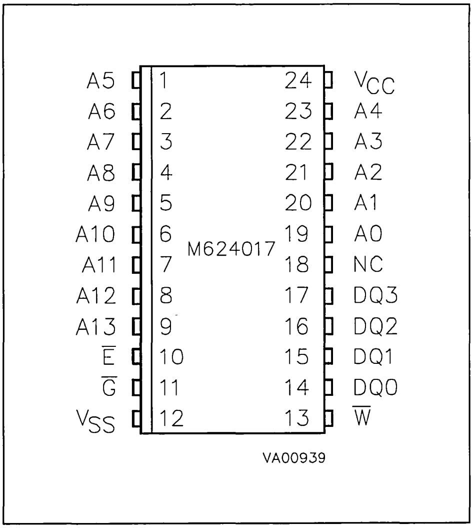


Figure 2A. SDIP Pin Connections


A5 1 24 VCC
A6 2 23 A4
A7 3 22 A3
A8 4 21 A2
A9 5 20 A1
A10 6 19 A0
A11 7 18 NC
A12 8 17 DQ3
A13 9 16 DQ2
E 10 15 DQ1
G 11 14 DQ0
VSS 12 13 W
M624017
VA00938

Warning: NC = No Connection.

Figure 2B. SOJ Pin Connections


A5 1 24 VCC
A6 2 23 A4
A7 3 22 A3
A8 4 21 A2
A9 5 20 A1
A10 6 19 A0
A11 7 18 NC
A12 8 17 DQ3
A13 9 16 DQ2
E 10 15 DQ1
G 11 14 DQ0
VSS 12 13 W
M624017
VA00939

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	25	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M624017 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable ($\overline{G}$) Low and Chip Enable ($\overline{E}$) asserted Low. This provides access to data from four of the 65,536 locations in the static memory array, specified by the 14 address inputs. Valid data will be available at the four Q output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but data address lines will always be valid at t_{AVQV}.

WRITE MODE

The M624017 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Chip Enable $\overline{E}$, or $\overline{W}$ must be deasserted during address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as tAVWL and tAVEL respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ Low, and $\overline{G}$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$, whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M624017 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ High. An Output Enable ($\overline{G}$) pin provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$, as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

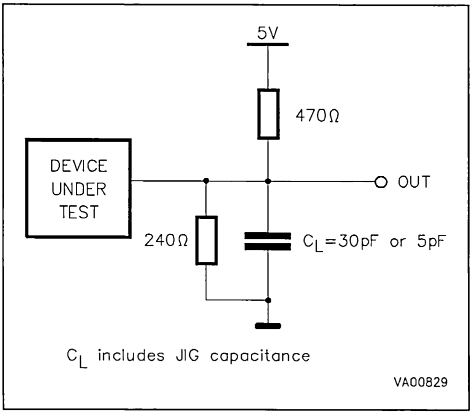


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [(2)]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	$V_{CC} = 5.5V$		160	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E} = V_{IH}, f = 0$		40	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E} \geq V_{CC} - 0.2V, f = 0$		10	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 8mA$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
3 All other Inputs at $V_{IL} \leq 0.2V$ or $V_{IH} \geq V_{CC} - 0.2V$

Table 6. Read Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624017								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	10		12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		10		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		10		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		5		7		8		10	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns

Notes: 1. C_L = 30pF
2 C_L = 5pF

Figure 4. Read Mode AC Waveforms

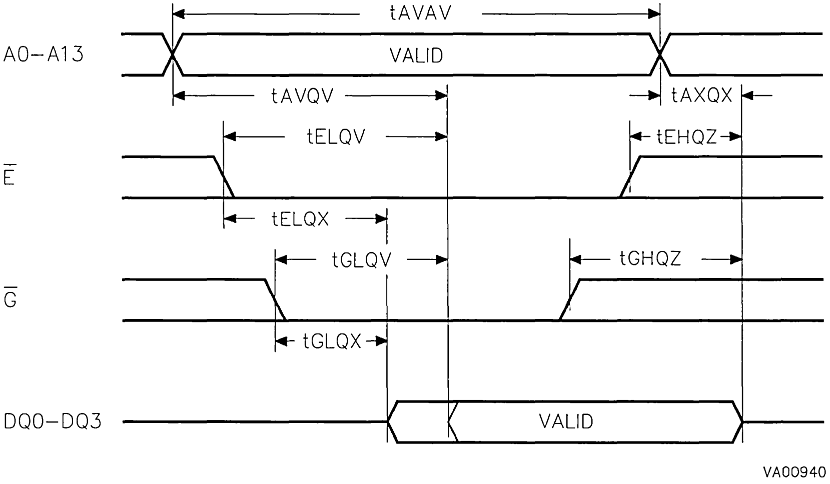

tAVAV
A0–A13
VALID
tAVQV
tAXQX
tELQV
tEHQZ
$\overline{E}$
tELQX
tGLQV
tGHQZ
$\overline{G}$
tGLQX
DQ0–DQ3
VALID
VA00940

Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624017								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	10		12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	5	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	7		9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	5		7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	5		7		8		10		ns

Note: 1. C_L = 5pF

Figure 5. Write Enable Controlled, Write AC Waveforms

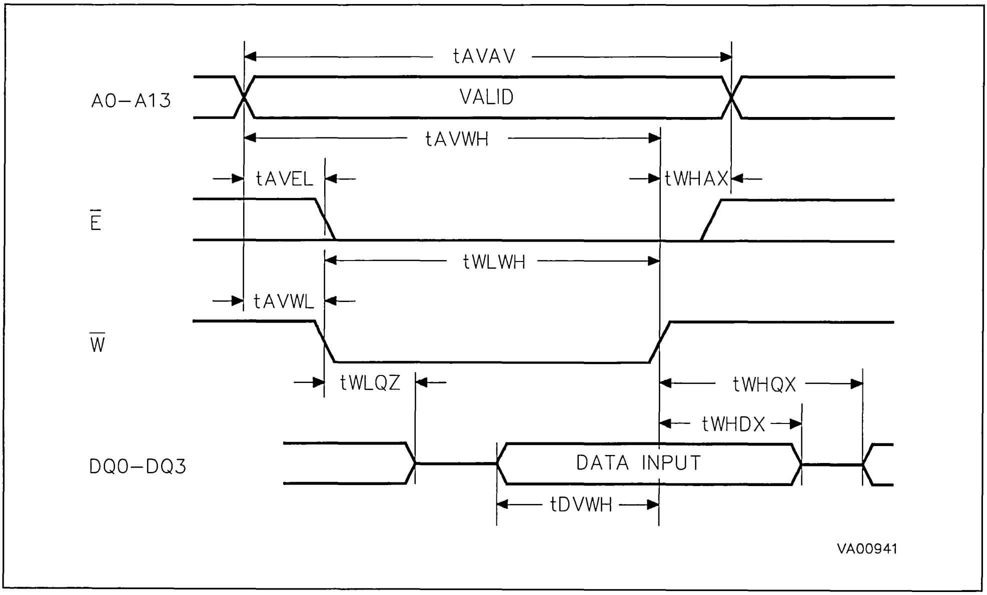
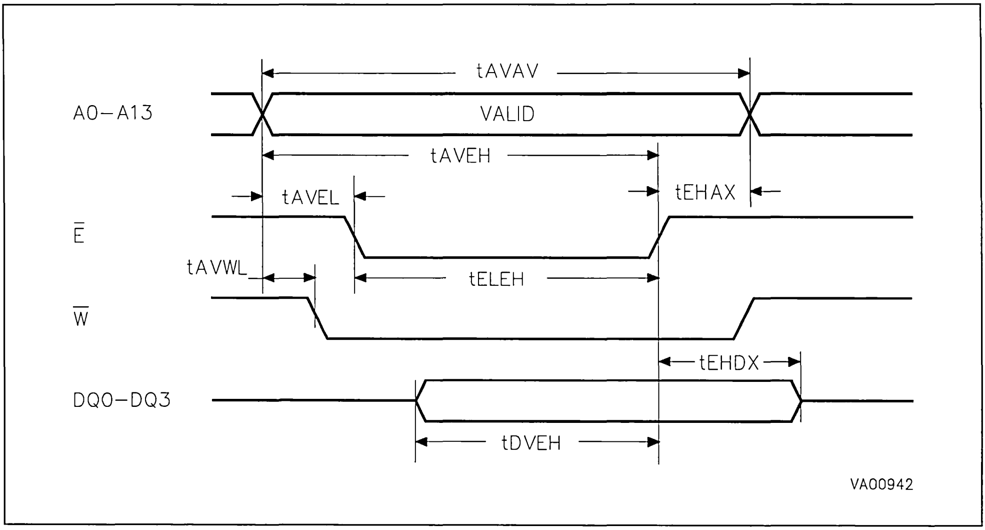


Figure 6. Chip Enable Controlled, Write AC Waveforms


tAVAV
A0–A13
VALID
tAVEH
tAVEL
tEHAX
E̅
tAVWL
tELEH
W̅
tEHDX
DQ0–DQ3
tDVEH
VA00942

ORDERING INFORMATION

Example: M624017 -10 E 1

Speed		Package		Temperature Range	
-10	10 ns	PS	PSDIP24	1	0 to 70 °C
-12	12 ns	E	PSOJ24 300 mils		
-15	15 ns				
-20	20 ns				

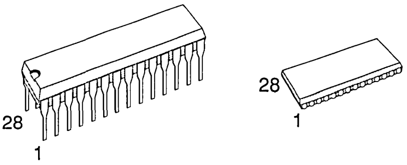
For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M628008

VERY FAST CMOS 8K x 8 SRAM WITH OUTPUT ENABLE

- 8K x 8 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIMES: 10, 12, 15, 20ns
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mils PACKAGES



PSDIP28 (PS)

PSOJ28 (E)
300 mils

DESCRIPTION

The M628008 is a 64K (65,536 bit) Fast CMOS SRAM, organized as 8,192 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

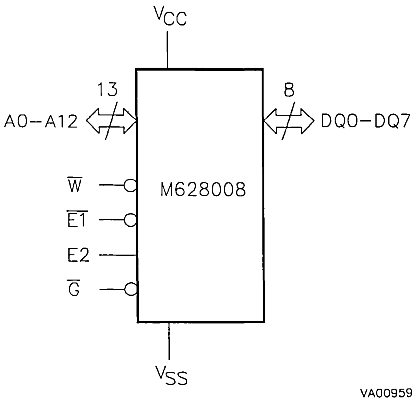
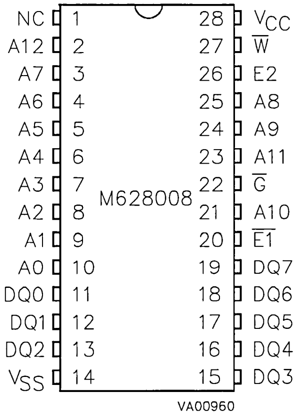
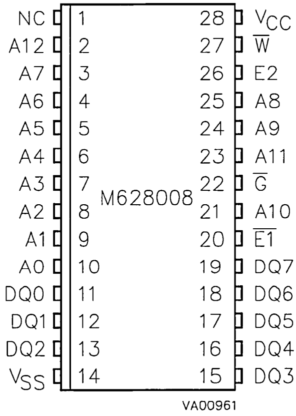


Figure 2A. SDIP Pin Connections


NC
A12
A7
A6
A5
A4
A3
A2
A1
A0
DQ0
DQ1
DQ2
V_{SS}
M628008
V_{CC}
$\overline{W}$
E2
A8
A9
A11
$\overline{G}$
A10
$\overline{E1}$
DQ7
DQ6
DQ5
DQ4
DQ3
VA00960

Warning: NC = No Connection.

Figure 2B. SOJ Pin Connections


NC
A12
A7
A6
A5
A4
A3
A2
A1
A0
DQ0
DQ1
DQ2
V_{SS}
M628008
V_{CC}
$\overline{W}$
E2
A8
A9
A11
$\overline{G}$
A10
$\overline{E1}$
DQ7
DQ6
DQ5
DQ4
DQ3
VA00961

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2 One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note. X = V_{IH} or V_{IL}

READ MODE

The M628008 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable ($\overline{G}$) Low, with both Chip Enables ($\overline{E1}$ and E2) asserted. This provides access to data from eight of the 65,536 locations in the static memory array, specified by the 13 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and Chip Enables are valid. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M628008 is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low with E2 High. Chip Enables $\overline{E1}$, E2 or $\overline{W}$ must be deasserted during Access transitions for subsequent write cycles. Write begins with the concurrence of the two Chip Enables being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVE1L}, t_{AVE2H} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or $\overline{W}$ or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ Low, E2 High and $\overline{G}$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the falling edge of E2, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

OPERATIONAL MODE

The M628008 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ High or E2 Low). An Output Enable ($\overline{G}$) pin provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E1}$, E2, as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

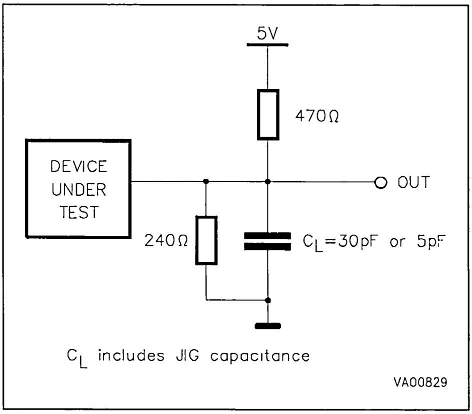


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [(2)]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-10 & -12)		140	mA
		V_{CC} = 5.5V, (-15 & -20)		120	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E1} = V_{IH}$ or $E2 = V_{IL}$, f = 0		40	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E1} \ge V_{CC} - 0.3V$ or $E2 \le 0.3V$, f = 0		10	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Table 6. Read Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628008								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	10		12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		10		12		15		20	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		10		12		15		20	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		10		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		5		7		8		10	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	3		3		3		3		ns
t_{E2HQX} (2)	Chip Enable 2 High to Output Transition	3		3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		0		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns

Notes: 1. C_L = 30pF
2. C_L = 5pF

Figure 4. Read Mode AC Waveforms

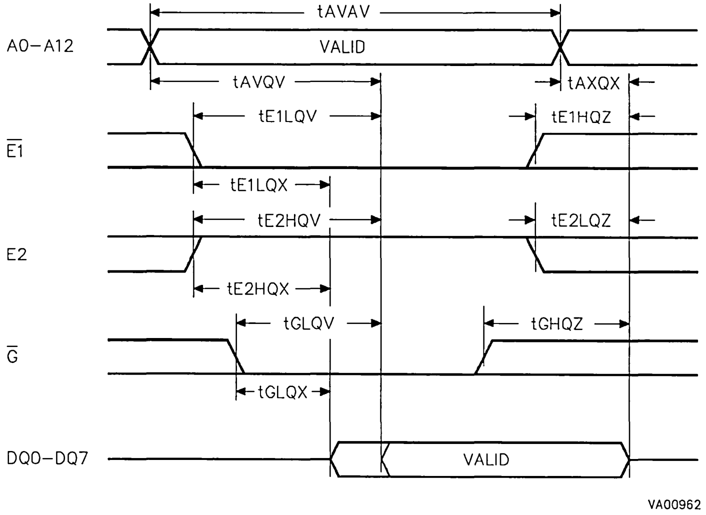

tAVAV
A0–A12
VALID
tAVQV
tAXQX
tE1LQV
tE1HQZ
$\overline{E1}$
tE1LQX
tE2HQV
tE2LQZ
E2
tE2HQX
tGLQV
tGHQZ
$\overline{G}$
tGLQX
DQ0–DQ7
VALID
VA00962

Table 7. Write Mode AC Characteristics (T$_A$ = 0 to 70°C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	M628008								Unit
		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	10		12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	10		12		15		20		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	10		12		15		20		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	10		12		15		20		ns
t_{WLWH}	Write Enable Pulse Width	10		12		15		20		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	7		9		10		15		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	7		9		10		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		0		0		0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	5	0	7	0	8	0	10	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	5		7		8		10		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	5		7		8		10		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	5		7		8		10		ns

Note: 1. C_L = 5pF

Figure 5. Write Enable Controlled, Write AC Waveforms

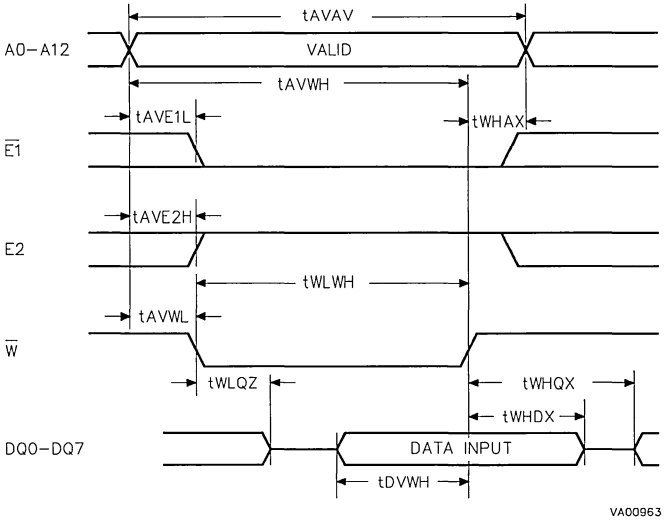
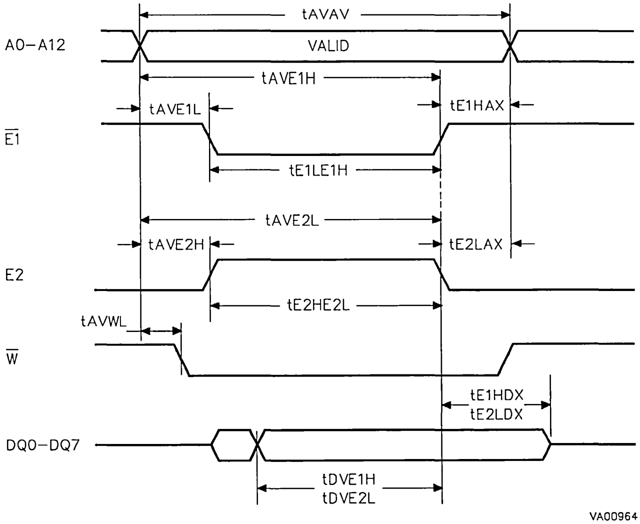

tAVAV
A0–A12
VALID
tAVWH
tAVE1L
tWHAX
E1
tAVE2H
E2
tWLWH
tAVWL
W
tWLQZ
tWHQX
tWHDX
DQ0–DQ7
DATA INPUT
tDVWH
VA00963

Figure 6. Chip Enable Controlled, Write AC Waveforms


tAVAV
A0–A12
VALID
tAVE1H
tAVE1L
tE1HAX
E1
tE1LE1H
tAVE2L
tAVE2H
tE2LAX
E2
tE2HE2L
tAVWL
W
tE1HDX
tE2LDX
DQ0–DQ7
tDVE1H
tDVE2L
VA00964

ORDERING INFORMATION

Example: M628008 -10 E 1

Speed	
-10	10 ns
-12	12 ns
-15	15 ns
-20	20 ns

Package	
PS	PSDIP28
E	PSOJ28 300 mils

Temperature Range	
1	0 to 70 °C

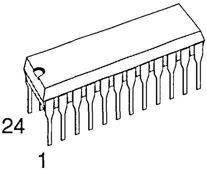
For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

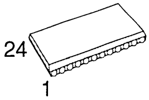
M621256

VERY FAST CMOS 256K x 1 SRAM WITH SEPARATE I/O

- 256K x 1 CMOS FAST SRAM
- EQUAL CYCLE AND ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- SEPARATE DATA INPUT AND DATA OUTPUT PINS
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



PSDIP24 (PS)



PSOJ24 (E)
300 mils

DESCRIPTION

The M621256 is a 256K (262,144 bit) Fast CMOS SRAM, organized as 262,144 words by 1 bit. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A17	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

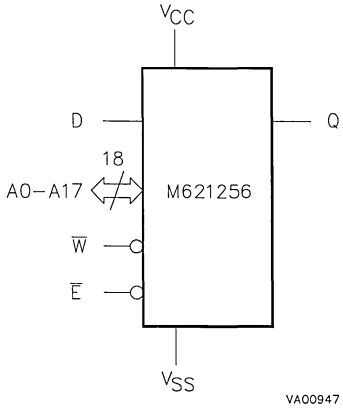


Figure 2A. SDIP Pin Connections

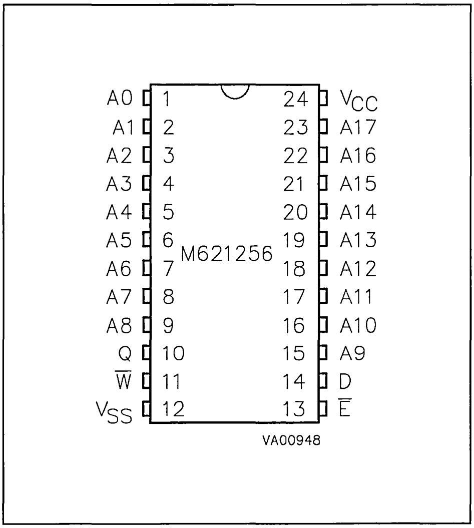

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
Q 10
$\overline{W}$ 11
V_{SS} 12
24 V_{CC}
23 A17
22 A16
21 A15
20 A14
19 A13
18 A12
17 A11
16 A10
15 A9
14 D
13 $\overline{E}$
M621256
VA00948

Figure 2B. SOJ Pin Connections

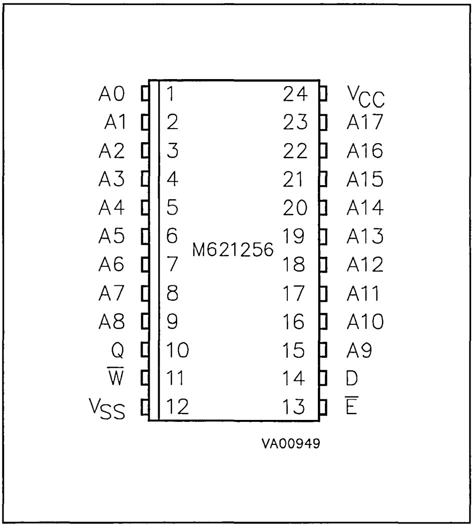

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
Q 10
$\overline{W}$ 11
V_{SS} 12
24 V_{CC}
23 A17
22 A16
21 A15
20 A14
19 A13
18 A12
17 A11
16 A10
15 A9
14 D
13 $\overline{E}$
M621256
VA00949

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5 5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power
Read	V_{IL}	V_{IH}	X	Data Output	Active
Write	V_{IL}	V_{IL}	Data Input	Hi-Z	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M621256 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Chip Enable ($\overline{E}$) asserted Low. This provides access to data from one of the 262,144 locations in the static memory array, specified by the 18 address inputs. Valid data will be available at the Q output pin within t_{AVQV} after the last stable address providing $\overline{E}$ is Low. If Chip Enable access time is not met, data access will be measured from the limiting parameter (t_{ELQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M621256 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ Low and $\overline{W}$ High), then $\overline{W}$ will return the output to high impedance within t_{WLQZ} of its falling edge. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M621256 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ High). Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

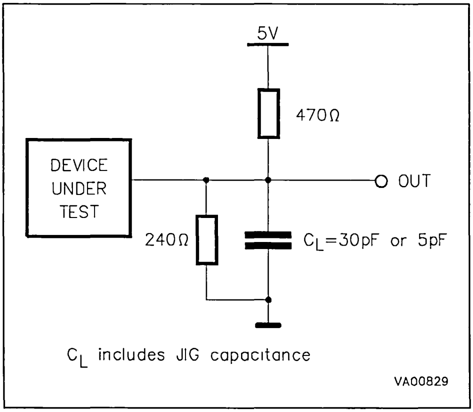


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T$_A$ = 0 to 70 °C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V (-12)		140	mA
		V_{CC} = 5.5V (-15)		130	mA
		V_{CC} = 5.5V (-20)		120	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E} = V_{IH}, f = 0$		40	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E} \geq V_{CC} - 0.2V, f = 0$		10	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
3. All other Inputs at $V_{IL} \leq 0.2V$ or $V_{IH} \geq V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T$_A$ = 0 to 70°C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	M621256						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		12		15		20	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable to Power Down		12		15		20	ns

Notes: 1. C_L = 30pF
2. C_L = 5pF

Figure 4. Read Mode AC Waveforms

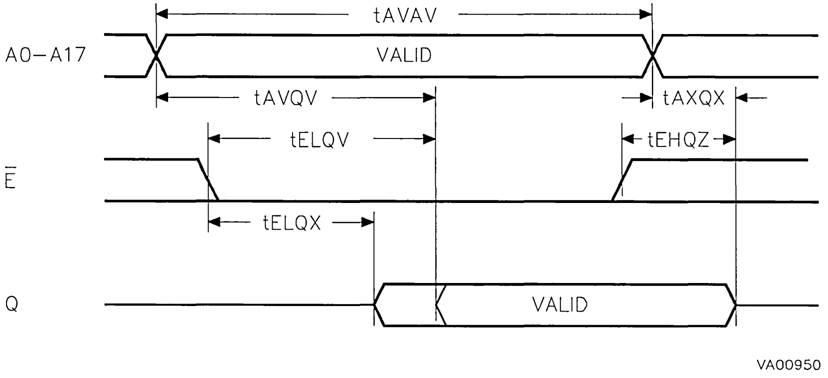

tAVAV
A0–A17
VALID
tAVQV
tAXQX
tELQV
tEHQZ
$\overline{E}$
tELQX
Q
VALID
VA00950

Figure 5. Standby Mode AC Waveforms

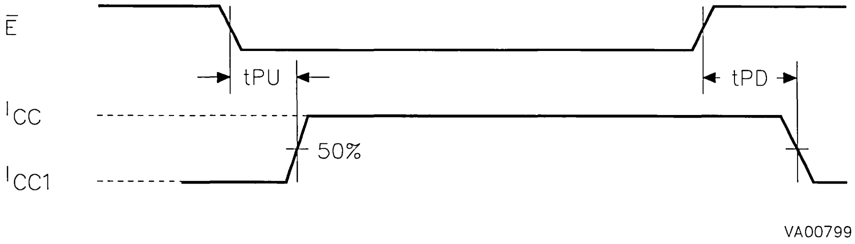

$\overline{E}$
tPU
tPD
ICC
50%
ICC1
VA00799

Table 7. Write Mode AC Characteristics (T$_A$ = 0 to 70°C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	M621256						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELEH}	Chip Enable to Write Enable High	9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	7		8		10		ns

Note: 1. C$_L$ = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

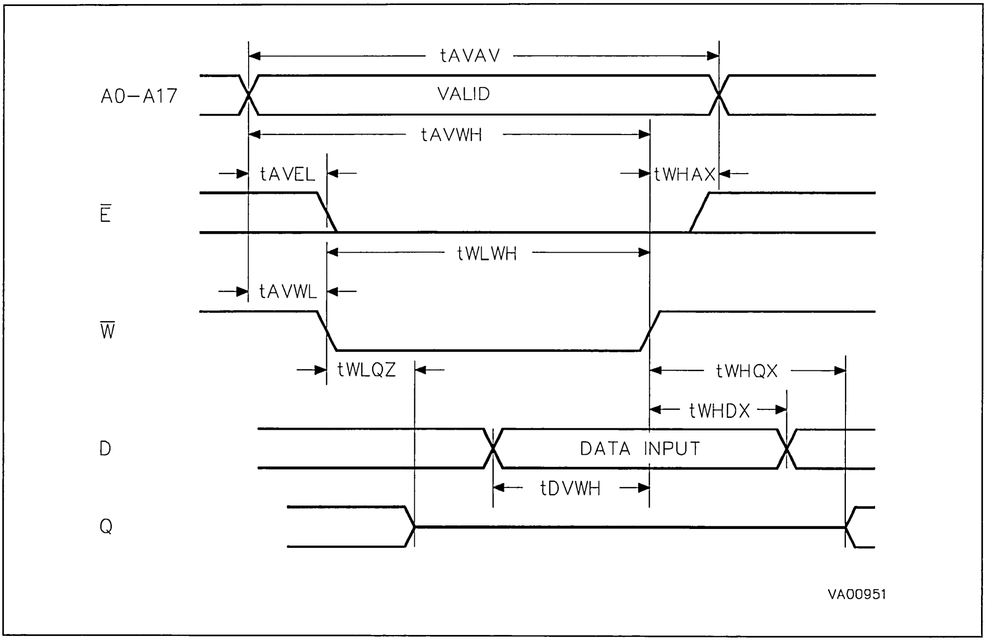


Figure 7. Chip Enable Controlled, Write AC Waveforms

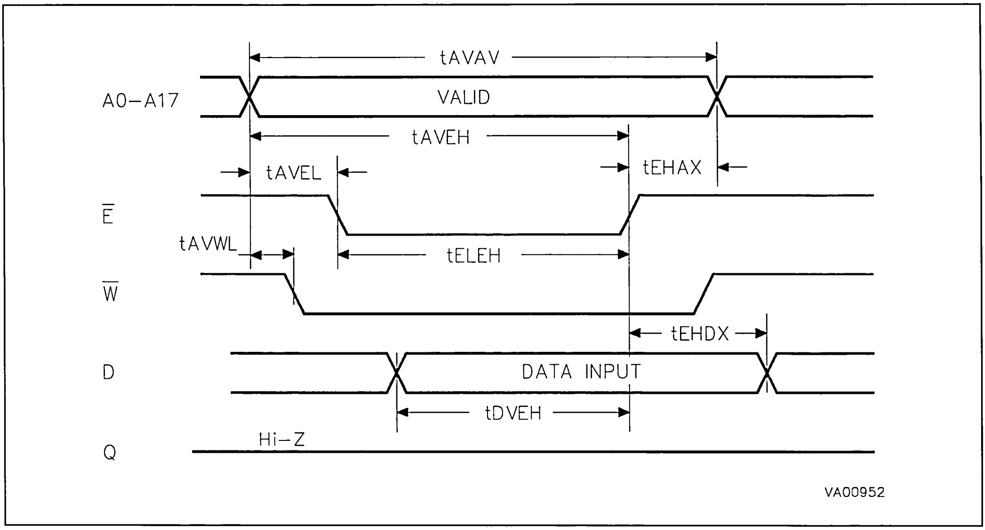
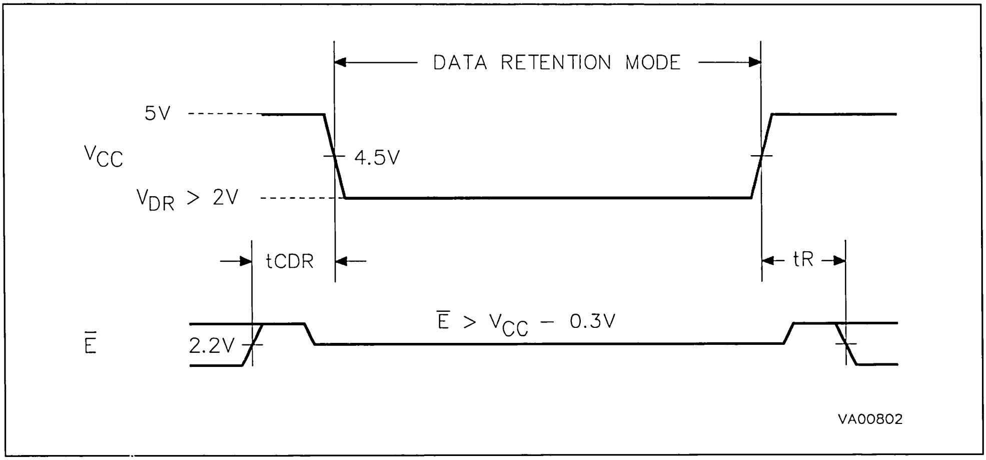

tAVAV
A0–A17
VALID
tAVEH
tAVEL
tEHAX
$\overline{E}$
tAVWL
tELEH
$\overline{W}$
tEHDX
D
DATA INPUT
tDVEH
Q
Hi–Z
VA00952

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.3V$, f = 0		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Note: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
V_{CC}
4.5V
V_{DR} > 2V
tCDR
tR
$\overline{E}$ > V_{CC} – 0.3V
$\overline{E}$
2.2V
VA00802

ORDERING INFORMATION

Example: M621256 -12 E 1

Speed	
-12	12 ns
-15	15 ns
-20	20 ns

Package	
PS	PSDIP24
E	PSOJ24 300 mils

Temperature Range	
1	0 to 70 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

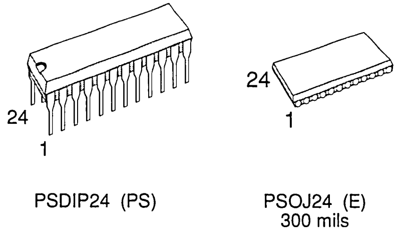
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M624064

VERY FAST CMOS 64K x 4 SRAM

- 64K x 4 CMOS FAST SRAM
- EQUAL CYCLE AND ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



DESCRIPTION

The M624064 is a 256K (262,144 bit) Fast CMOS SRAM, organized as 65,536 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A15	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

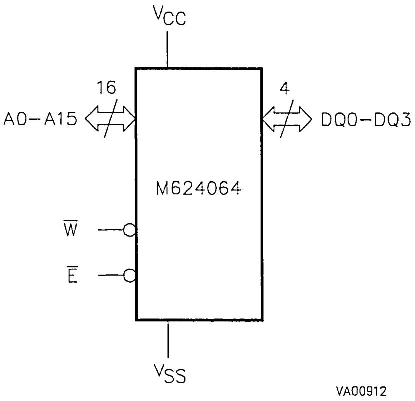


Figure 2A. SDIP Pin Connections

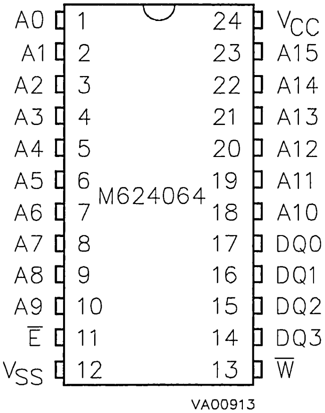

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
A9 10
E̅ 11
VSS 12
24 VCC
23 A15
22 A14
21 A13
20 A12
19 A11
18 A10
17 DQ0
16 DQ1
15 DQ2
14 DQ3
13 W̅
M624064
VA00913

Figure 2B. SOJ Pin Connections

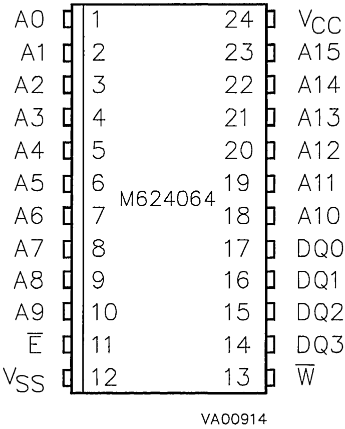

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
A9 10
E̅ 11
VSS 12
24 VCC
23 A15
22 A14
21 A13
20 A12
19 A11
18 A10
17 DQ0
16 DQ1
15 DQ2
14 DQ3
13 W̅
M624064
VA00914

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	Data Output	Active
Write	V_{IL}	V_{IL}	Data Input	Active
Deselect	V_{IH}	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M624064 is in the Read mode whenever Write Enable ($\overline{W}$) is high, with Chip Enable ($\overline{E}$) asserted low. This provides access to data from four of the 262,144 locations in the static memory array, specified by the 16 address inputs. Valid data will be available at the four output pins within t_{AVQV} after the last stable address, providing $\overline{E}$ is Low. If Chip Enable access time is not met, data access will be measured from the limiting parameter (t_{ELQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M624064 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}1$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M624064 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ High). Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

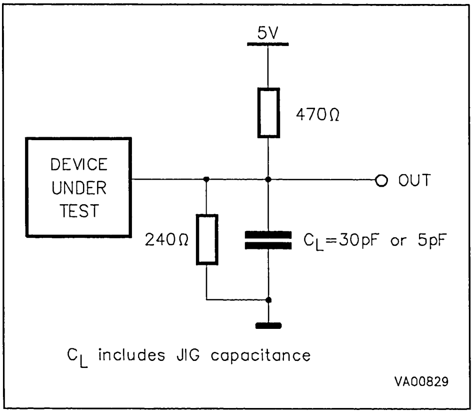


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [(2)]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-12)		140	mA
		V_{CC} = 5.5V, (-15)		130	mA
		V_{CC} = 5.5V, (-20)		120	mA
I_{CC1} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E} = V_{IH}$, f = 0		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E} \geq V_{CC} - 0.2V$, f = 0		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
3. All other Inputs at $V_{IL} \leq 0.2V$ or $V_{IH} \geq V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624064						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		12		15		20	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable to Power Down		12		15		20	ns

Notes: 1. C_L = 30pF .
2. C_L = 5pF
3 Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

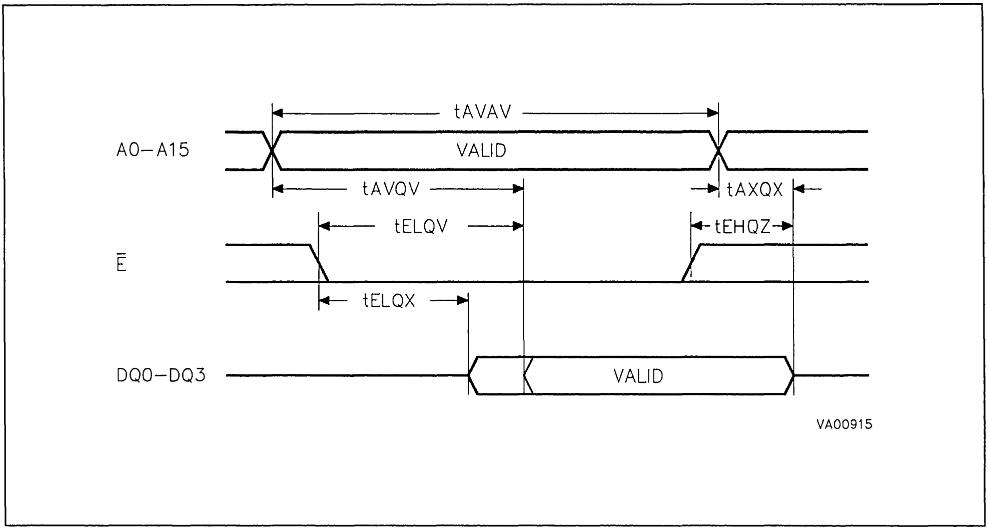

tAVAV
A0–A15
VALID
tAVQV
tAXQX
tELQV
tEHQZ
$\overline{E}$
tELQX
DQ0–DQ3
VALID
VA00915

Figure 5. Standby Mode AC Waveforms

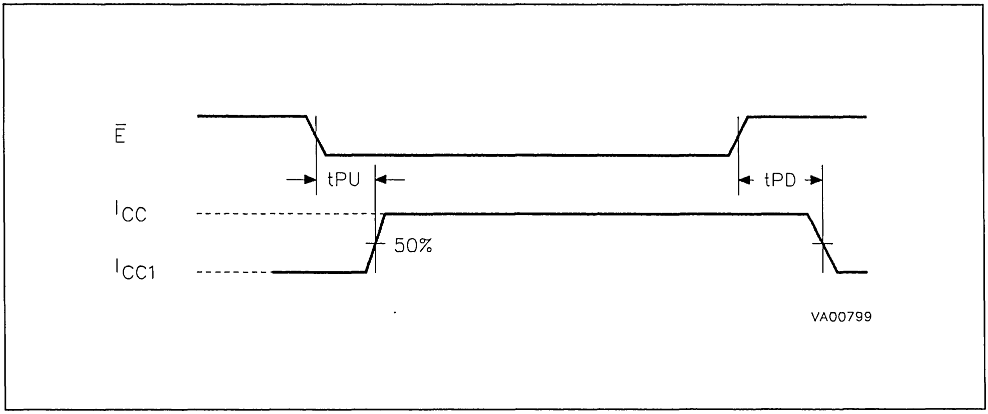

$\overline{E}$
tPU
tPD
I_{CC}
50%
I_{CC1}
VA00799

Table 7. Write Mode AC Characteristics (T$_A$ = 0 to 70°C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	M624064						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	7		8		10		ns

Note: 1. C$_L$ = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

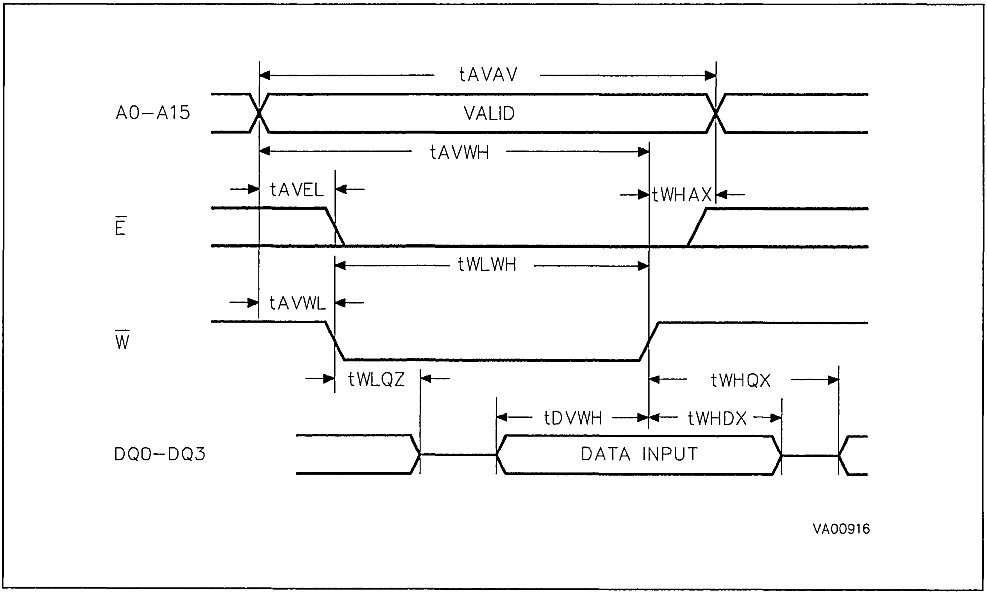


Figure 7. Chip Enable Controlled, Write AC Waveforms

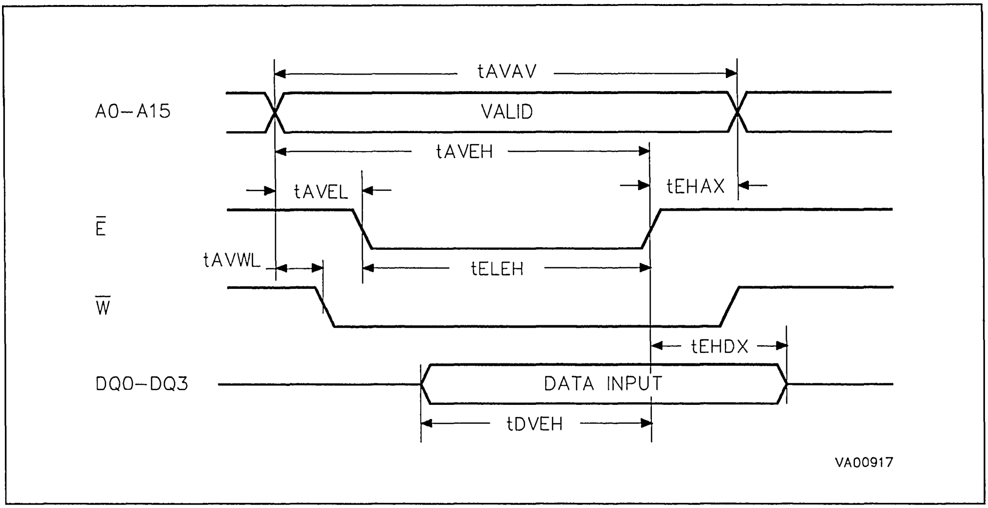
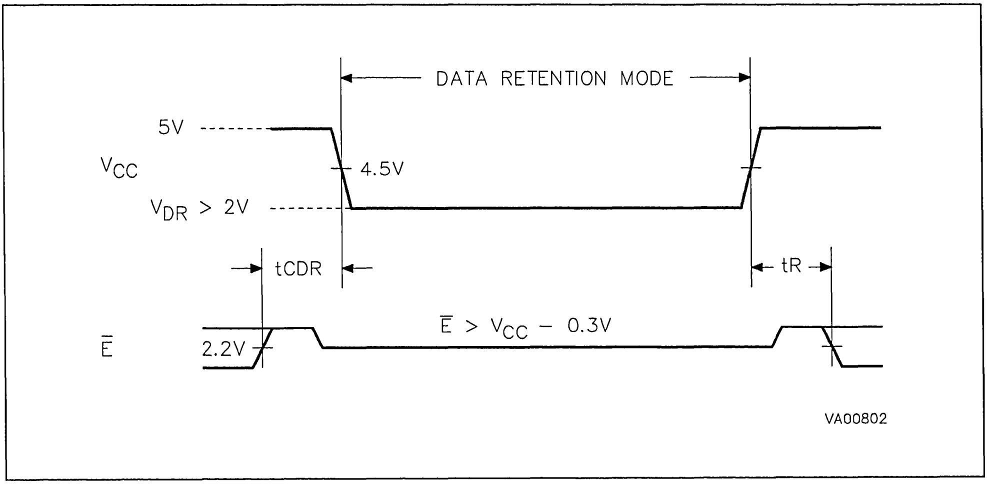

tAVAV
A0–A15
VALID
tAVEH
tAVEL
tEHAX
$\overline{E}$
tAVWL
tELEH
$\overline{W}$
tEHDX
DQ0–DQ3
DATA INPUT
tDVEH
VA00917

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	$V_{CC} = 3V, \overline{E} \geq V_{CC} - 0.3V, f = 0$		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.3V,\ f = 0$	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.3V,\ f = 0$	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
V_{CC}
4.5V
V_{DR} > 2V
tCDR
tR
$\overline{E}$ > V_{CC} – 0.3V
$\overline{E}$
2.2V
VA00802

ORDERING INFORMATION

Example: M624064 -12 E 1

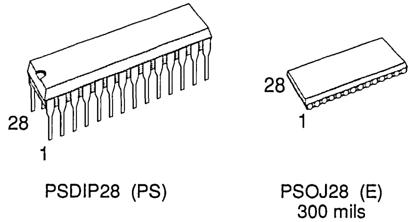
Speed		Package		Temperature Range	
-12	12 ns	PS	PSDIP24	1	0 to 70 °C
-15	15 ns	E	PSOJ24 300 mils		
-20	20 ns				

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

VERY FAST CMOS 64K x 4 SRAM WITH OUTPUT ENABLE

- 64K x 4 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



DESCRIPTION

The M624065 is a 256K (262,144 bit) Fast CMOS SRAM, organized as 65,536 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A15	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

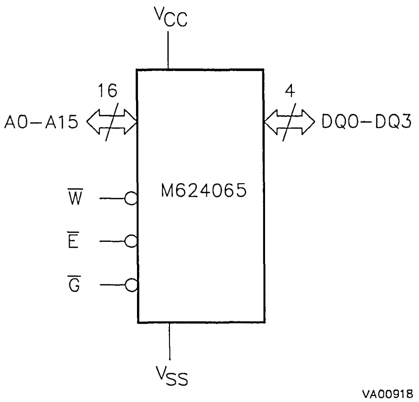


Figure 2A. SDIP Pin Connections

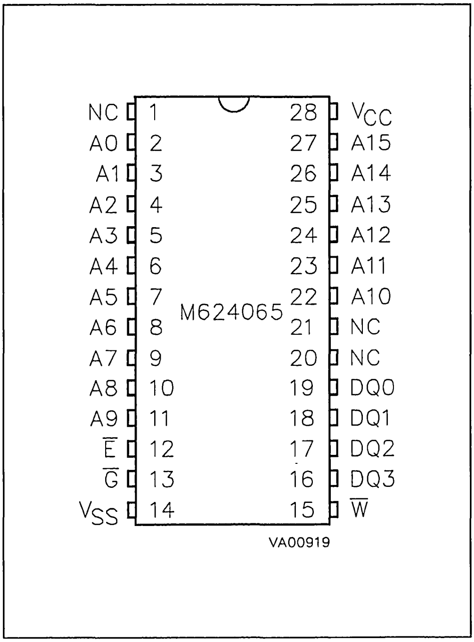

NC 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
A8 10
A9 11
$\overline{E}$ 12
$\overline{G}$ 13
V_{SS} 14
28 V_{CC}
27 A15
26 A14
25 A13
24 A12
23 A11
22 A10
21 NC
20 NC
19 DQ0
18 DQ1
17 DQ2
16 DQ3
15 $\overline{W}$
M624065
VA00919

Figure 2B. SOJ Pin Connections

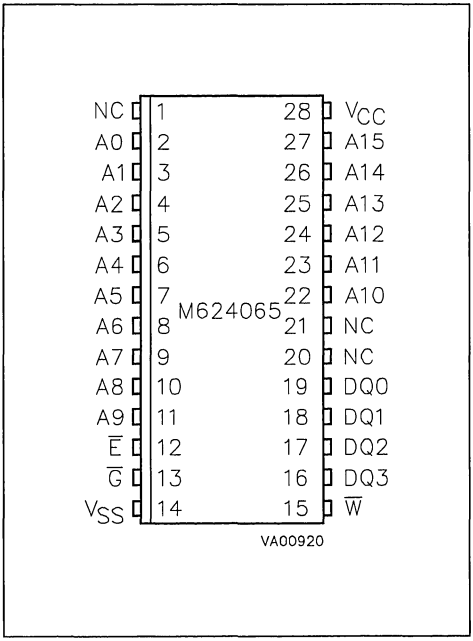

NC 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
A8 10
A9 11
$\overline{E}$ 12
$\overline{G}$ 13
V_{SS} 14
28 V_{CC}
27 A15
26 A14
25 A13
24 A12
23 A11
22 A10
21 NC
20 NC
19 DQ0
18 DQ1
17 DQ2
16 DQ3
15 $\overline{W}$
M624065
VA00920

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M624065 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable ($\overline{G}$) Low, with Chip Enable ($\overline{E}$) asserted Low. This provides access to data from four of the 262,144 locations in the static memory array, specified by the 16 address inputs. Valid data will be available at the four output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M624065 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Chip Enable $\overline{E}$ or $\overline{W}$ must be de-asserted during Address transitions for subsequent write cycles. The Write begins with the concurrence of Chip Enable and $\overline{W}$ being asserted low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively and is determined to the latter concurrence edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$. If the Output is Enabled ($\overline{E}$ Low, $\overline{G}$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} o t_{EHDX}.

OPERATIONAL MODE

The M624065 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ High). An Output Enable ($\overline{G}$) pin provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

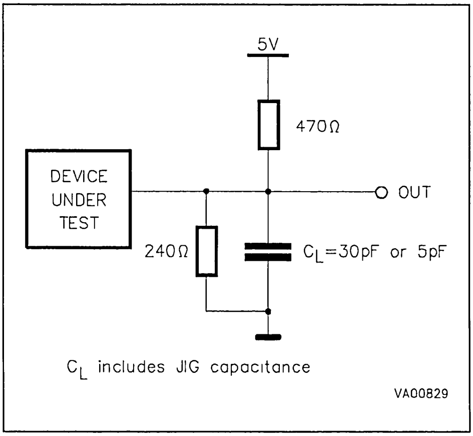


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-12)		140	mA
		V_{CC} = 5.5V, (-15)		130	mA
		V_{CC} = 5.5V, (-20)		120	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E} = V_{IH}, f = 0$		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E} \ge V_{CC} - 0.2V,$ $f = 0$		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624065						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		8		10	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable to Power Down		12		15		20	ns

Notes: 1. C_L = 30pF .
2. C_L = 5pF
3. Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

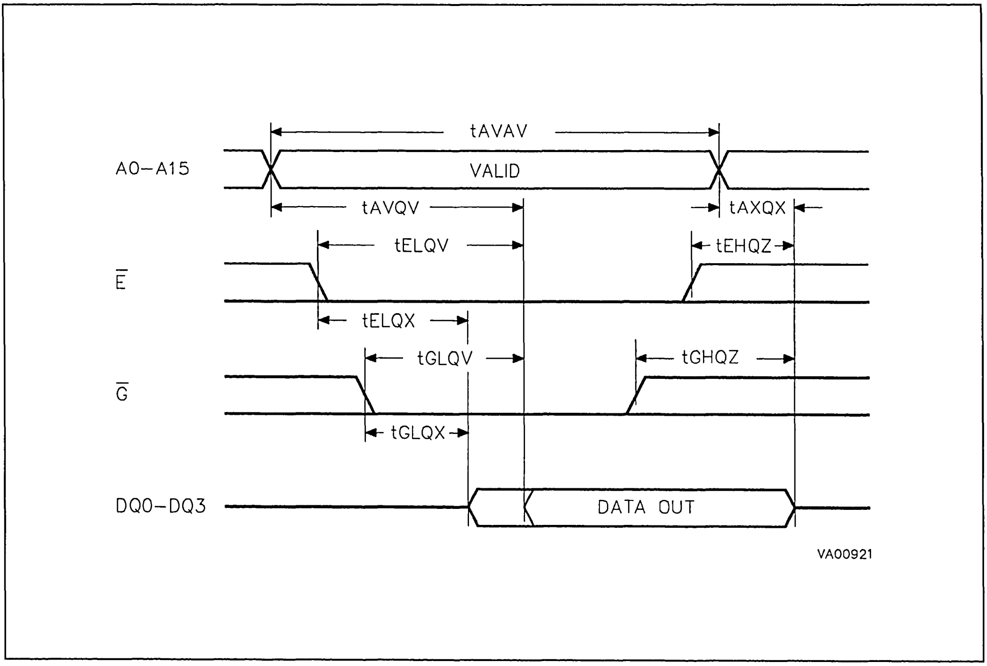

tAVAV
A0–A15
VALID
tAVQV
tAXQX
tELQV
tEHQZ
$\overline{E}$
tELQX
tGLQV
tGHQZ
$\overline{G}$
tGLQX
DQ0–DQ3
DATA OUT
VA00921

Figure 5. Standby Mode AC Waveforms

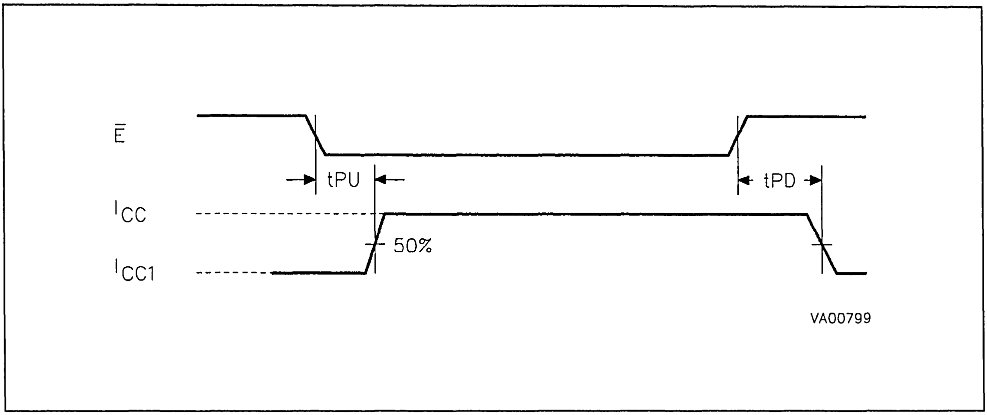

$\overline{E}$
tPU
tPD
I_{CC}
50%
I_{CC1}
VA00799

Table 7. Write Mode AC Characteristics (T$_A$ = 0 to 70°C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	M624065						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	9		10		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	7		8		10		ns

Note: 1. C_L = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

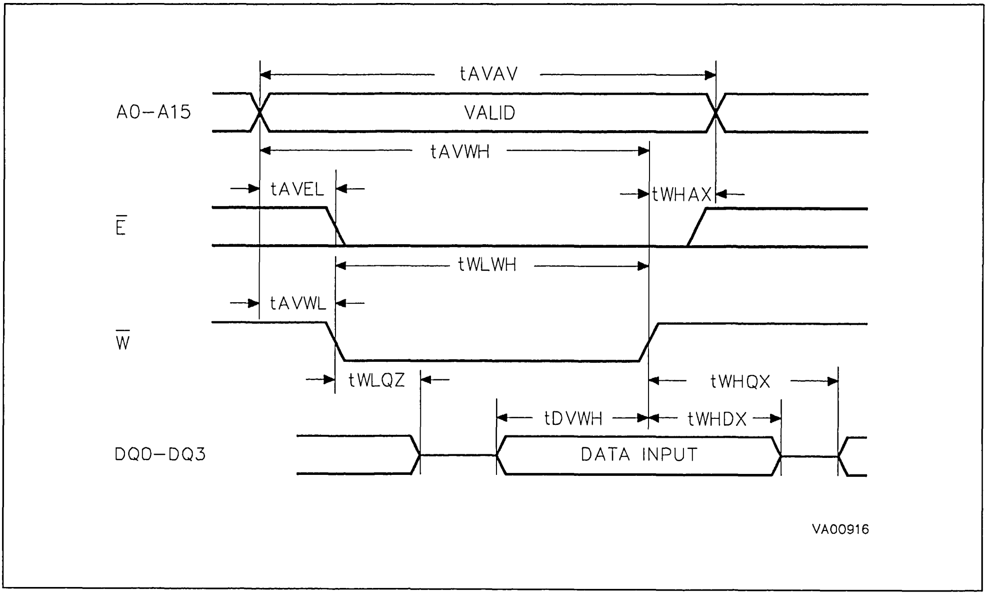

tAVAV
A0–A15
VALID
tAVWH
tAVEL
tWHAX
$\overline{E}$
tWLWH
tAVWL
$\overline{W}$
tWLQZ
tWHQX
tDVWH
tWHDX
DQ0–DQ3
DATA INPUT
VA00916

Figure 7. Chip Enable Controlled, Write AC Waveforms

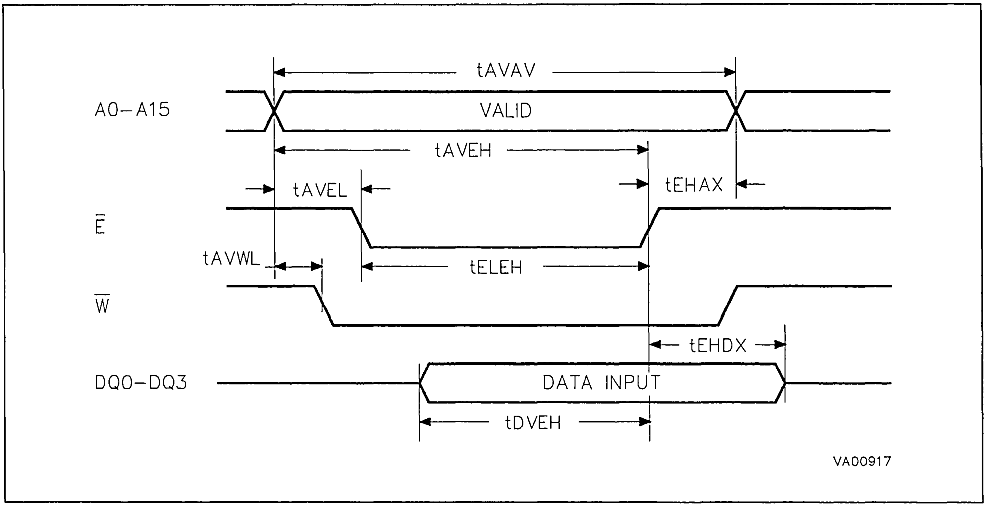
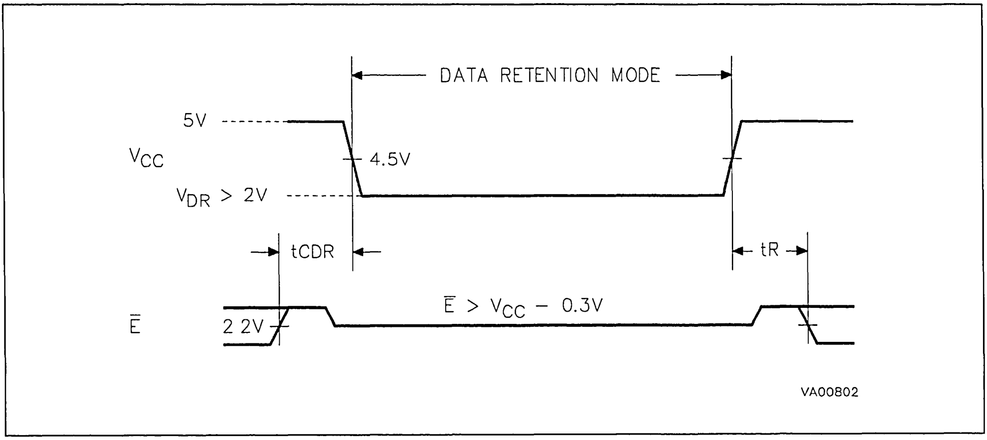

tAVAV
A0-A15
VALID
tAVEH
tAVEL
tEHAX
E
tAVWL
tELEH
W
tEHDX
DQ0-DQ3
DATA INPUT
tDVEH
VA00917

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

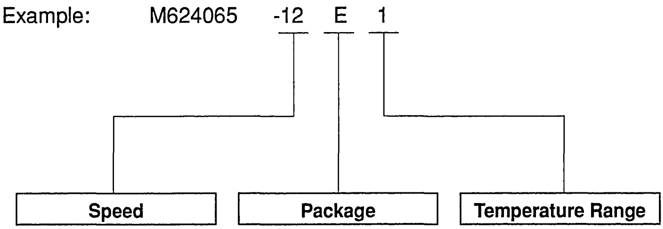
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.3V$, f = 0		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
VCC
4.5V
VDR > 2V
tCDR
tR
E > VCC - 0.3V
E
2 2V
VA00802

ORDERING INFORMATION


Example: M624065 -12 E 1
Speed
Package
Temperature Range

Speed	
-12	12 ns
-15	15 ns
-20	20 ns

Package	
PS	PSDIP28
E	PSOJ28 300 mils

Temperature Range	
1	0 to 70 °C

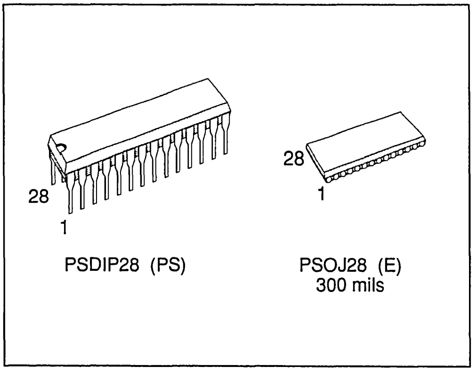
For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M628032

VERY FAST CMOS 32K x 8 SRAM WITH OUTPUT ENABLE

- 32K x 8 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIMES: 12, 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



DESCRIPTION

The M628032 is a 256K (262,144 bit) Fast CMOS SRAM, organized as 32,768 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

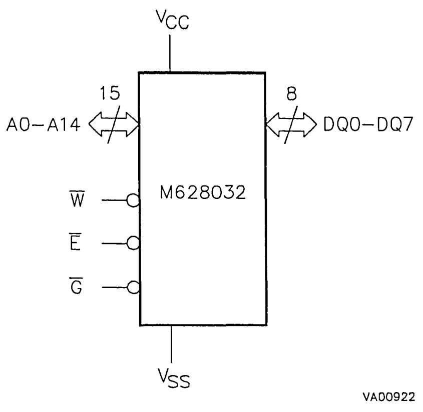


Figure 2A. SDIP Pin Connections

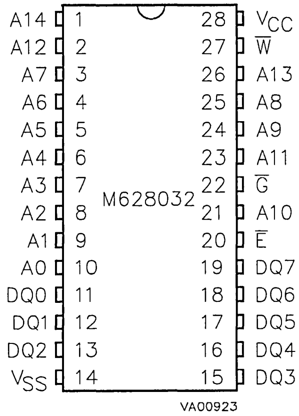

A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
V_{SS} 14
28 V_{CC}
27 $\overline{W}$
26 A13
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{E}$
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
M628032
VA00923

Figure 2B. SOJ Pin Connections

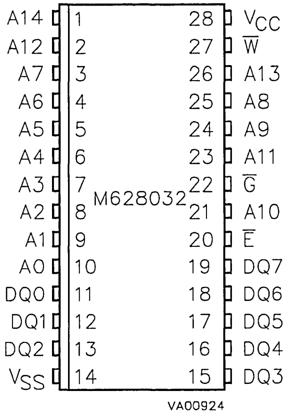

A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
V_{SS} 14
28 V_{CC}
27 $\overline{W}$
26 A13
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{E}$
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
M628032
VA00924

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5.5V only
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M628032 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable $\overline{G}$ is Low, with Chip Enable ($\overline{E}$) asserted. This provides access to data from nine of the 262,144 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, and Chip Enable $\overline{E}$ is valid. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M628032 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Chip Enable input $\overline{E}$ or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ Low and $\overline{G}$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$, whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M628032 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ High). An Output Enable ($\overline{G}$) pin provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

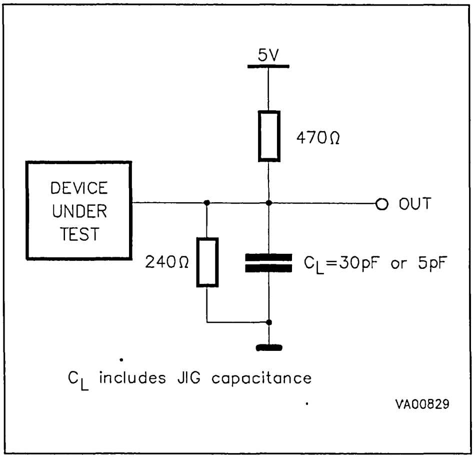


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-12)		140	mA
		V_{CC} = 5.5V, (-15)		130	mA
		V_{CC} = 5.5V, (-20)		120	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E} = V_{IH}, f = 0$		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E} \geq V_{CC} - 0.2V$, $f = 0$		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
3. All other Inputs at $V_{IL} \leq 0.2V$ or $V_{IH} \geq V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628032						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		8		10	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable to Power Down		12		15		20	ns

Notes: 1. C_L = 30pF
2. C_L = 5pF
3. Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

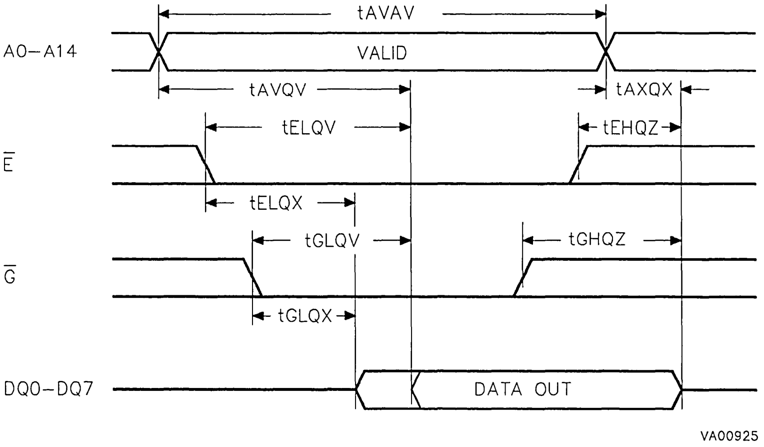

tAVAV
A0–A14
VALID
tAVQV
tAXQX
tELQV
tEHQZ
E
tELQX
tGLQV
tGHQZ
G
tGLQX
DQ0–DQ7
DATA OUT
VA00925

Figure 5. Standby Mode AC Waveforms

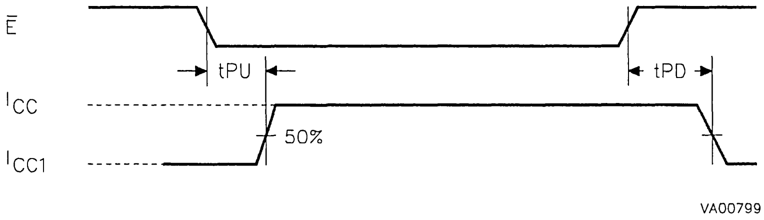

E
tPU
tPD
ICC
50%
ICC1
VA00799

Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628032						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		12		ns
t_{AVEH}	Address Valid to Chip Enable High	9		10		12		ns
t_{WLWH}	Write Enable Pulse Width	9		10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	9		10		12		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVEH}	Input Valid to Chip Enable High	7		8		10		ns

Note: 1. C_L = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

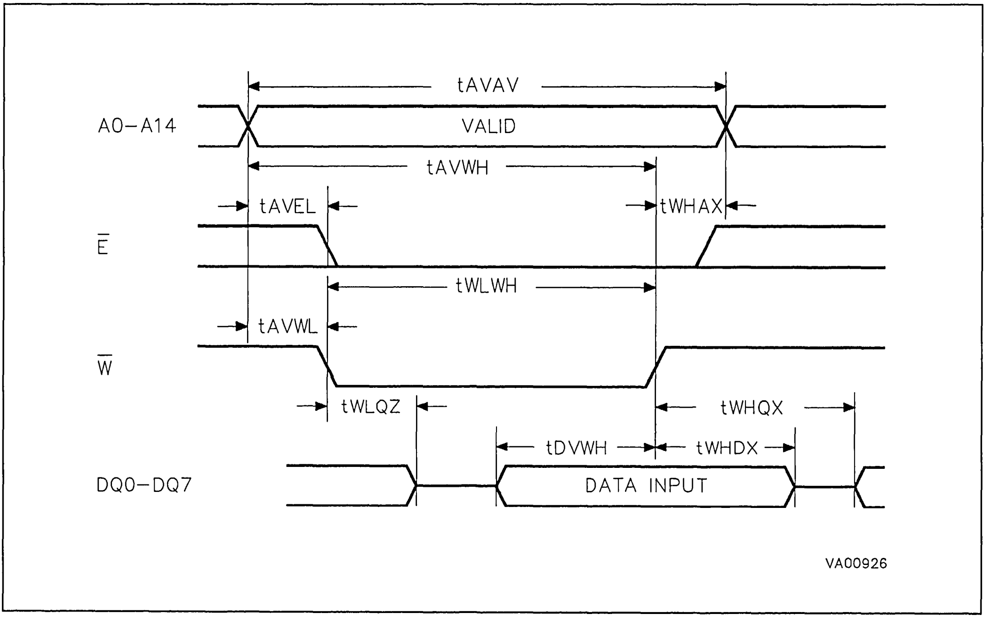


Figure 7. Chip Enable Controlled, Write AC Waveforms

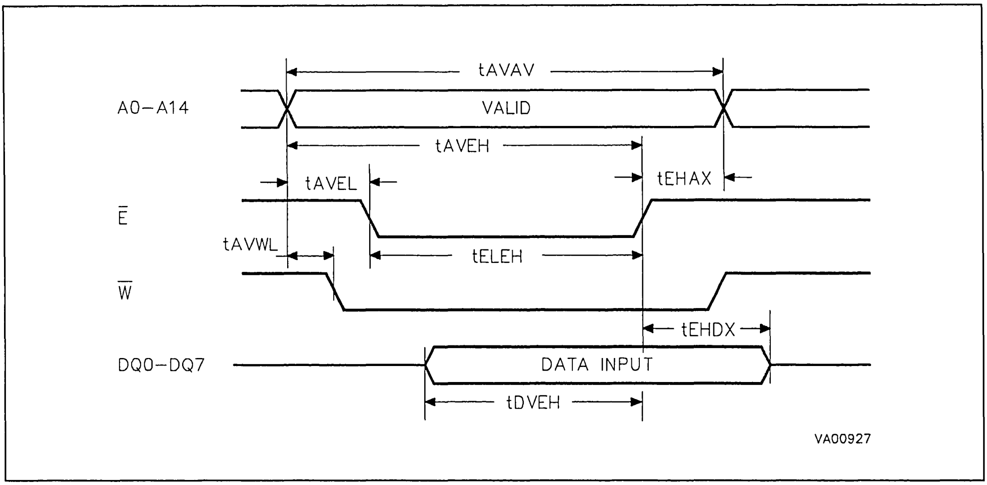
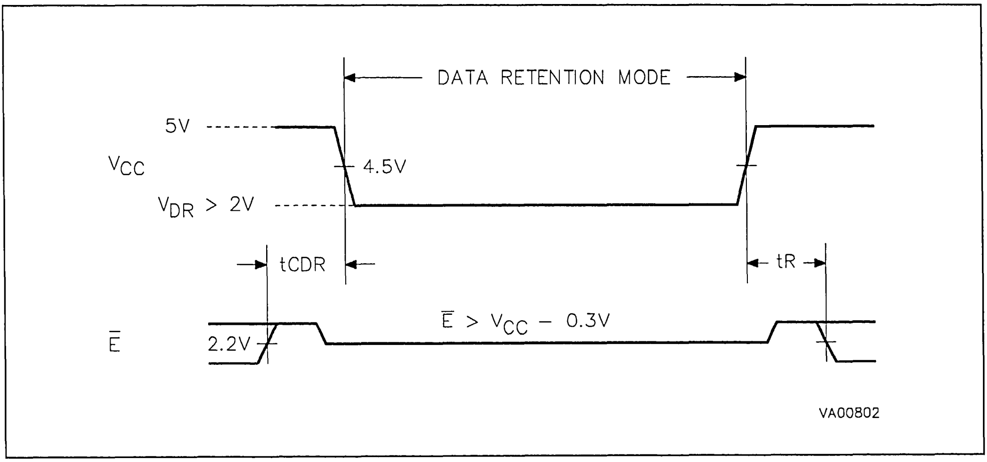

tAVAV
A0–A14
VALID
tAVEH
tAVEL
tEHAX
$\overline{E}$
tAVWL
tELEH
$\overline{W}$
tEHDX
DQ0–DQ7
DATA INPUT
tDVEH
VA00927

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	$V_{CC} = 3V, \overline{E} \geq V_{CC} - 0.3V, f = 0$		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.3V, f = 0$	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.3V, f = 0$	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1 All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
V_{CC}
4.5V
V_{DR} > 2V
tCDR
tR
$\overline{E}$ > V_{CC} – 0.3V
$\overline{E}$
2.2V
VA00802

ORDERING INFORMATION

Example: M628032 -12 E 1

Speed	
-12	12 ns
-15	15 ns
-20	20 ns

Package	
PS	PSDIP28
E	PSOJ28 300 mils

Temperature Range	
1	0 to 70 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

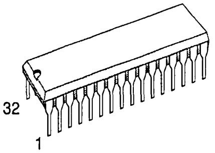
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

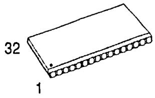
M629032

VERY FAST CMOS 32K x 9 SRAM WITH OUTPUT ENABLE

- 32K x 9 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIMES: 12, 15, 20ns
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ and DIP, 300 mil PACKAGES



PSDIP32 (PS)



PSOJ32 (E)
300 mils

DESCRIPTION

The M629032 is a 288K (294,912 bit) Fast CMOS SRAM, organized as 32,768 words by 9 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

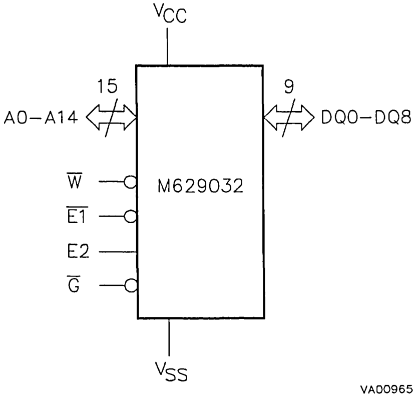
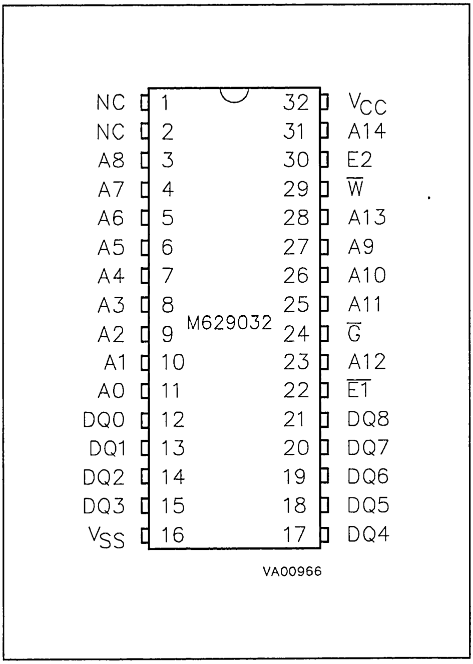


Table 1. Signal Names

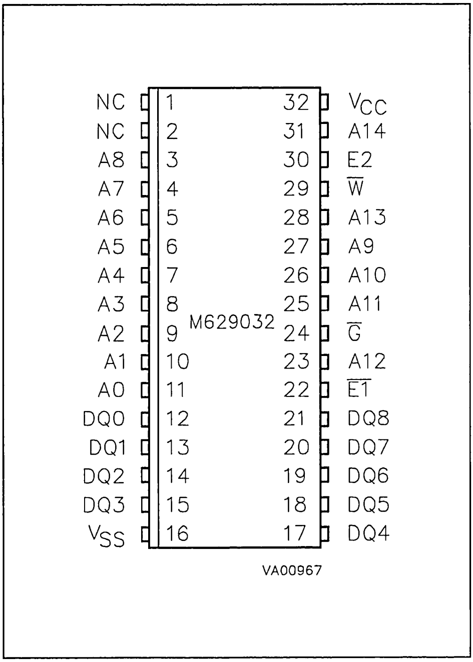
A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. SDIP Pin Connections


NC 1 32 VCC
NC 2 31 A14
A8 3 30 E2
A7 4 29 W̄
A6 5 28 A13
A5 6 27 A9
A4 7 26 A10
A3 8 25 A11
A2 9 24 Ḡ
A1 10 23 A12
A0 11 22 Ē1
DQ0 12 21 DQ8
DQ1 13 20 DQ7
DQ2 14 19 DQ6
DQ3 15 18 DQ5
VSS 16 17 DQ4
M629032
VA00966

Warning: NC = No Connection.

Figure 2B. SOJ Pin Connections


NC 1 32 VCC
NC 2 31 A14
A8 3 30 E2
A7 4 29 W̄
A6 5 28 A13
A5 6 27 A9
A4 7 26 A10
A3 8 25 A11
A2 9 24 Ḡ
A1 10 23 A12
A0 11 22 Ē1
DQ0 12 21 DQ8
DQ1 13 20 DQ7
DQ2 14 19 DQ6
DQ3 15 18 DQ5
VSS 16 17 DQ4
M629032
VA00967

Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2 One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0-DQ8	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

READ MODE

The M629032 is in the Read mode whenever Write Enable ($\overline{W}$) is High, with Output Enable ($\overline{G}$) Low, with both Chip Enables ($\overline{E1}$ and E2) asserted. This provides access to data from nine of the 294,912 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the nine Q output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and Chip Enables are valid. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but datalines will always be valid at t_{AVQV}.

WRITE MODE

The M629032 is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low with E2 High. Chip Enables $\overline{E1}$, E2 or $\overline{W}$ must be deasserted during address transitions for subsequent write cycles. Write begins with the concurrence of the two Chip Enables being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVE1L}, t_{AVE2H} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or $\overline{W}$ or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ Low, E2 High and $\overline{G}$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the falling edge of E2, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

OPERATIONAL MODE

The M629032 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ High or E2 Low). An Output Enable ($\overline{G}$) pin provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E1}$, E2, as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

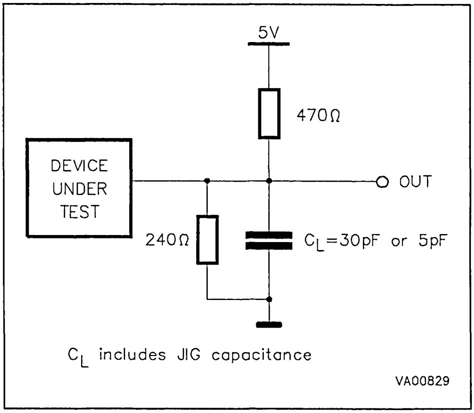


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [(2)]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-12)		140	mA
		V_{CC} = 5.5V, (-15)		130	mA
		V_{CC} = 5.5V, (-20)		120	mA
I_{CC1} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E1} = V_{IH}$ or $E2 = V_{IL}$, f = 0		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E1} \geq V_{CC} - 0.2V$ or $E2 \leq 0.2V$, f = 0		1	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
3. All other Inputs at $V_{IL} \leq 0.2V$ or $V_{IH} \geq V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M629032						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	12		15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		12		15		20	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		12		15		20	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		12		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		8		10	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	3		3		3		ns
t_{E2HQX} (2)	Chip Enable 2 High to Output Transition	3		3		3		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z	0	7	0	8	0	10	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z	0	7	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		ns
t_{PU} (3)	Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		0		0		ns
t_{PD} (3)	Chip Enable 1 High or Chip Enable 2 Low to Power Down		12		15		20	ns

Notes: 1. C_L = 30pF
2. C_L = 5pF
3. Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

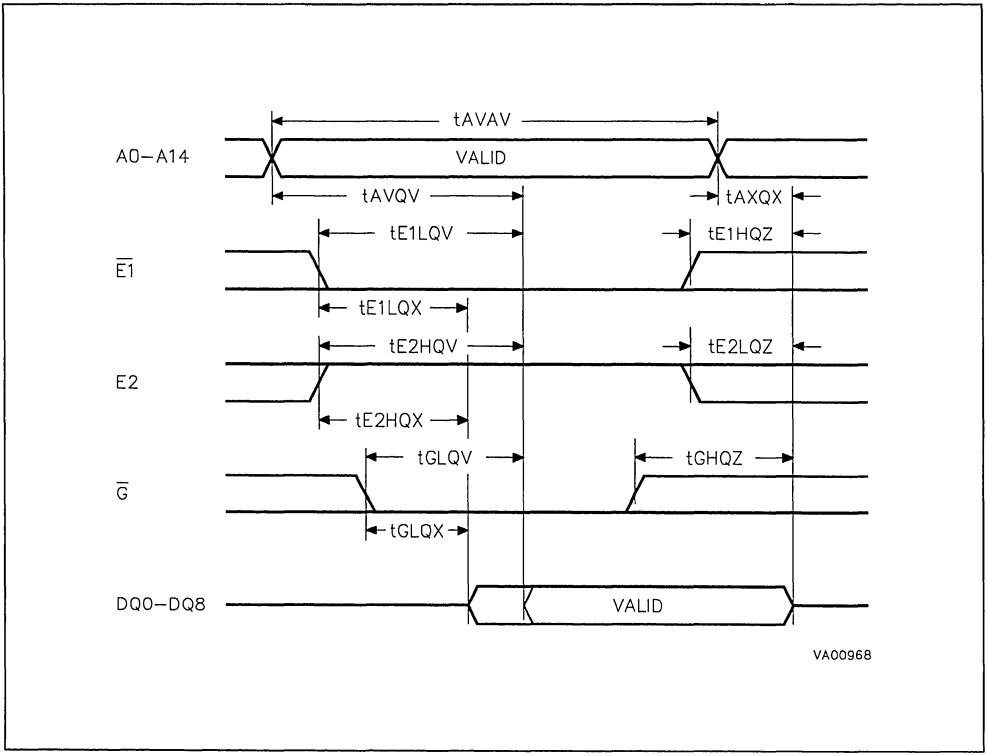

tAVAV
A0–A14
VALID
tAVQV
tAXQX
tE1LQV
tE1HQZ
$\overline{E1}$
tE1LQX
tE2HQV
tE2LQZ
E2
tE2HQX
tGLQV
tGHQZ
$\overline{G}$
tGLQX
DQ0–DQ8
VALID
VA00968

Figure 5. Standby Mode AC Waveforms

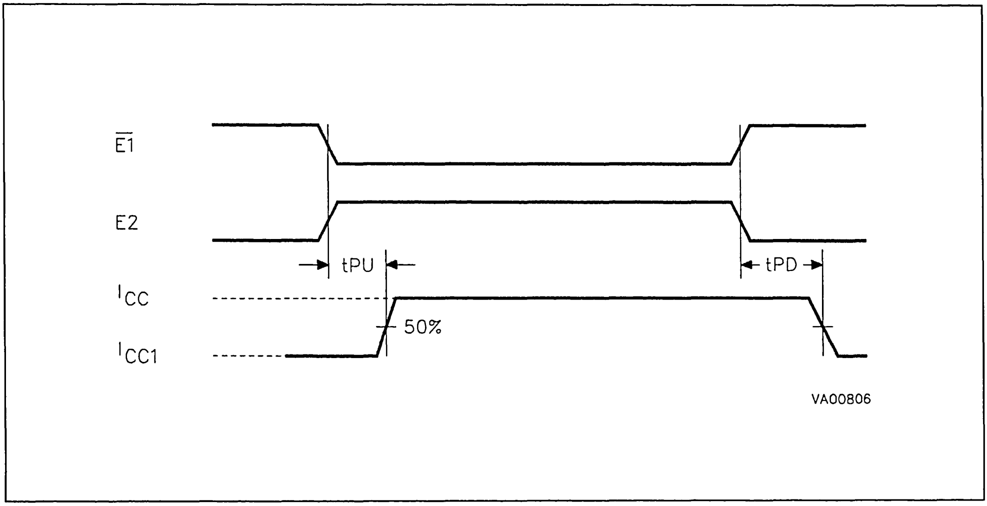

$\overline{E1}$
E2
tPU
tPD
ICC
50%
ICC1
VA00806

Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M629032						Unit
		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	12		15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	9		10		15		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	9		10		15		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	9		10		15		ns
t_{WLWH}	Write Enable Pulse Width	9		10		15		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	9		10		15		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	9		10		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		0		0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	7		8		10		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	7		8		10		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	7		8		10		ns

Note: 1. C_L = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

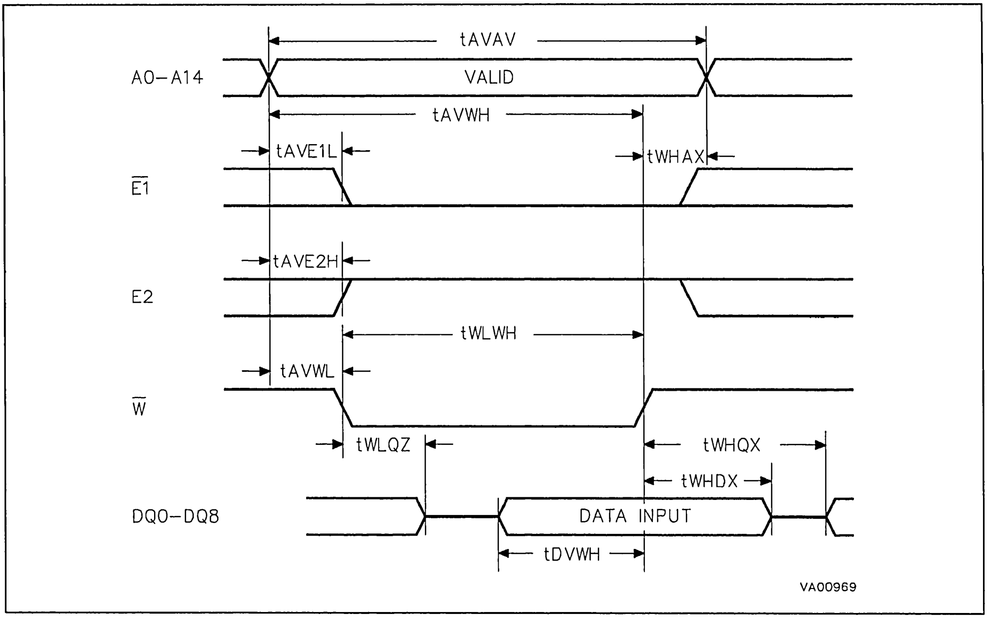

tAVAV
A0–A14
VALID
tAVWH
tAVE1L
tWHAX
E1
tAVE2H
E2
tWLWH
tAVWL
W
tWLQZ
tWHQX
tWHDX
DQ0–DQ8
DATA INPUT
tDVWH
VA00969

Figure 7. Chip Enable Controlled, Write AC Waveforms

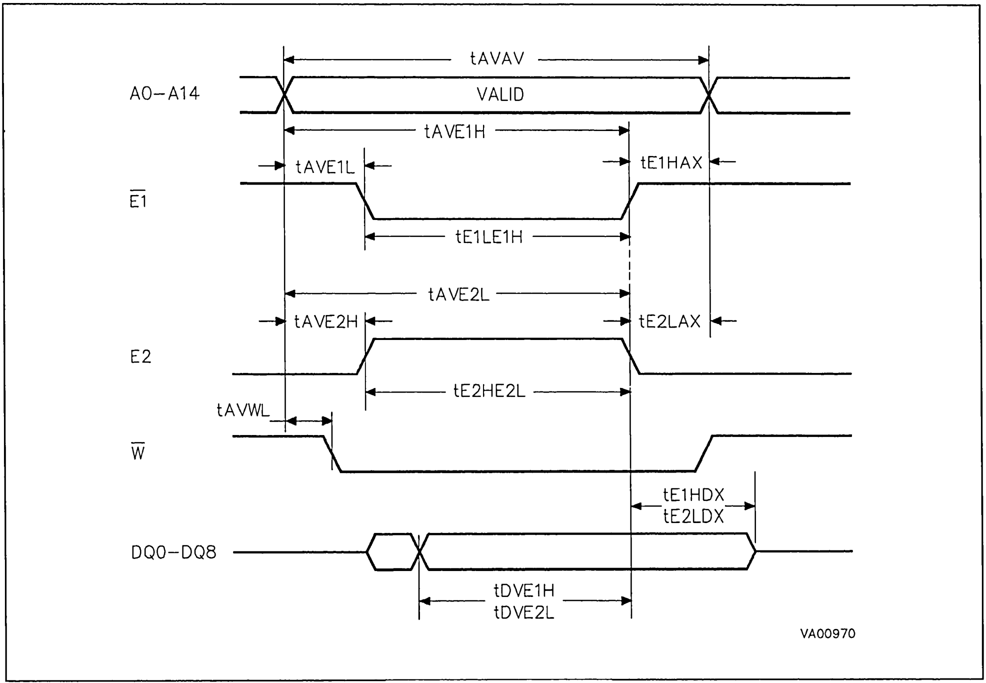
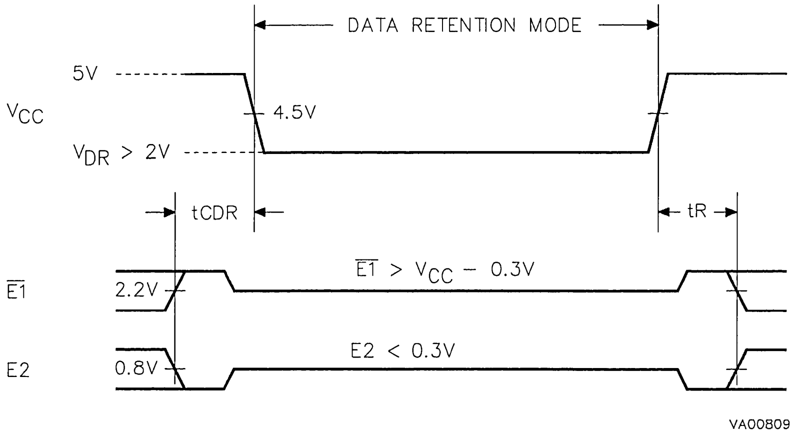

tAVAV
A0–A14
VALID
tAVE1H
tAVE1L
tE1HAX
E1
tE1LE1H
tAVE2L
tAVE2H
tE2LAX
E2
tE2HE2L
tAVWL
W
tE1HDX
tE2LDX
DQ0–DQ8
tDVE1H
tDVE2L
VA00970

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

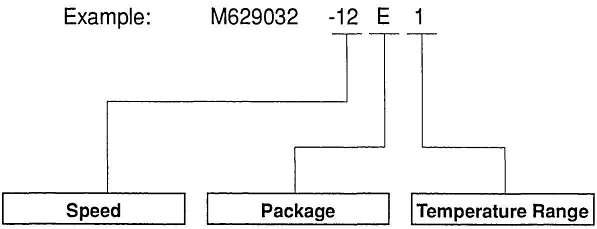
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E1} \geq V_{CC} - 0.3V$, $E2 \leq 0.3V$, f = 0		200	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC} - 0.3V$, $E2 \leq 0.3V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E1} \geq V_{CC} - 0.3V$, $E2 \leq 0.3V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
VCC
4.5V
VDR > 2V
tCDR
tR
E1
2.2V
E1 > VCC − 0.3V
E2
0.8V
E2 < 0.3V
VA00809

ORDERING INFORMATION


Example: M629032 -12 E 1
Speed
Package
Temperature Range

Speed	
-12	12 ns
-15	20 ns
-20	25 ns

Package	
PS	PSDIP32
E	PSOJ32 300 mils

Temperature Range	
1	0 to 70 °C

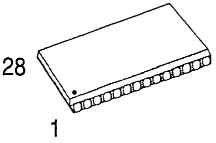
For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M621100

VERY FAST CMOS 1 Megabit (1M x 1) SRAM

- 1 Megabit CMOS FAST SRAM
- EQUAL CYCLE AND ACCESS TIMES: 15, 17, 20, 25ns
- LOW V_{CC} DATA RETENTION: 2V
- SEPARATE DATA INPUT AND OUTPUT
- JEDEC PLASTIC SOJ, 400 mil PACKAGE



PSOJ28 (E)
400 mils

DESCRIPTION

The M621100 is a 1 Megabit Fast CMOS SRAM, organized as 1,048,576 by 1 bit. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Figure 1. Logic Diagram

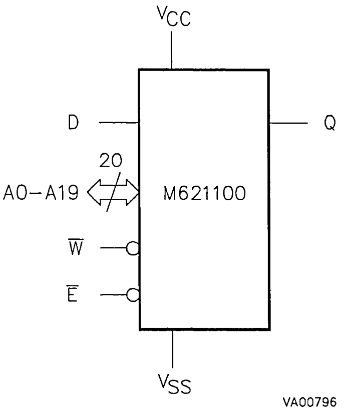


Table 1. Signal Names

A0 - A19	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
PD	Power Dissipation	1	W

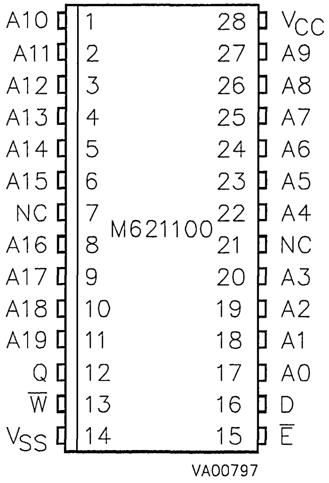
Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power
Read	V_{IL}	V_{IH}	X	Data Output	Active
Write	V_{IL}	V_{IL}	Data Input	Hi-Z	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 2. SOJ Pin Connections



Warning: NC = No Connection.

READ MODE

The M621100 is in the Read mode whenever Write Enable ($\overline{W}$) is High and Chip Enable ($\overline{E}$) is asserted. This provides access to data from one of the 1,048,576 locations in the static memory array, specified by the 20 address inputs. Valid data will be available at the output pin (Q) within t_{AVQV} after the last stable address, providing $\overline{E}$ is Low. If Chip Enable access time is not met, data access will be measured from the limiting parameter (t_{ELQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M621100 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the write input $\overline{W}$ must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ Low), then $\overline{W}$ will return the output to high impedance within t_{WLQZ} of its falling edge. Data input must be valid for t_{DVWH}

WRITE MODE (cont'd)

before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M621100 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E}$ High). Operational modes are determined by device control inputs $\overline{W}$, and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

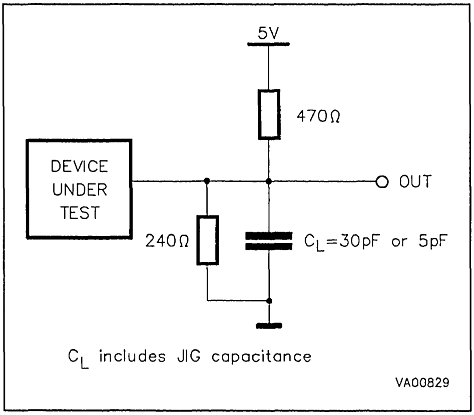


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Output deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-15 & -17)		160	mA
		V_{CC} = 5.5V, (-20)		140	mA
		V_{CC} = 5.5V, (-25)		130	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E} = V_{IH}, f = 0$		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E} \ge V_{CC} - 0.2V, f = 0$		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M621100								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	15		17		20		25		ns
t_{AVQV} (1)	Address Valid to Output Valid		15		17		20		25	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		15		17		20		25	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	2		2		2		2		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns
t_{PU} (3)	Chip Enable Low to Power Up	0		0		0		0		ns
t_{PD} (3)	Chip Enable High to Power Down		15		17		20		25	ns

Notes: 1. C_L = 30pF
2. C_L = 5pF
3. Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

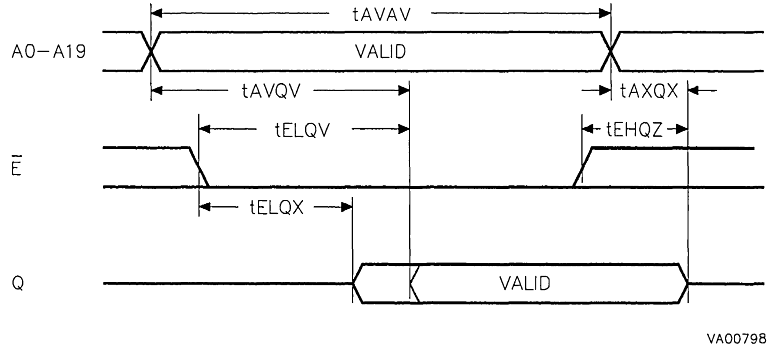

tAVAV
A0–A19
VALID
tAVQV
tAXQX
tELQV
tEHQZ
E̅
tELQX
Q
VALID
VA00798

Figure 5. Standby Mode AC Waveforms

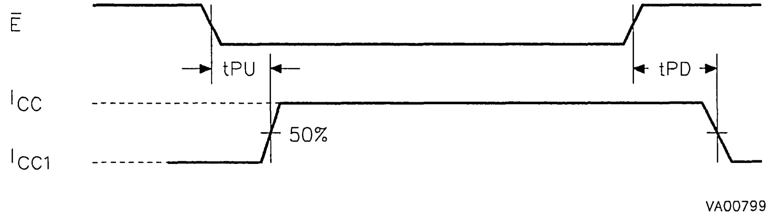

E̅
tPU
tPD
ICC
ICC1
50%
VA00799

Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M621100								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	15		17		20		25		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	12		12		12		15		ns
t_{AVEH}	Address Valid to Chip Enable High	12		12		12		15		ns
t_{WLWH}	Write Enable Pulse Width	10		12		12		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	0	12	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	10		12		12		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	8		10		12		12		ns
t_{DVEH}	Input Valid to Chip Enable High	8		10		12		12		ns

Note: 1. C_L = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

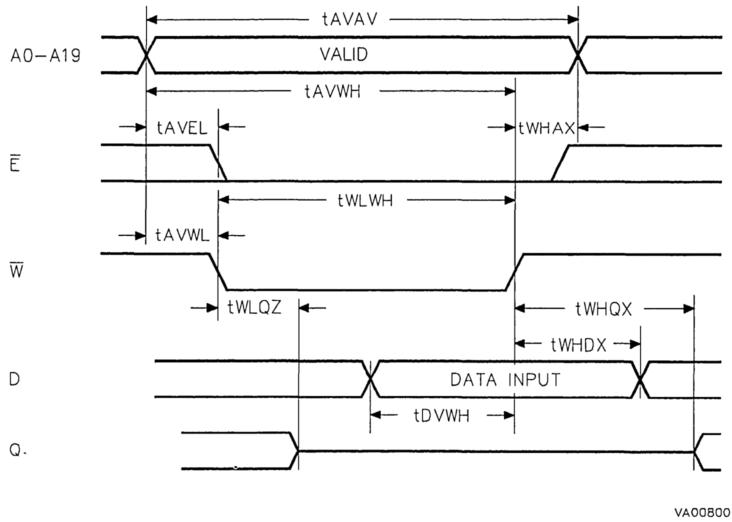


Figure 7. Chip Enable Controlled, Write AC Waveforms

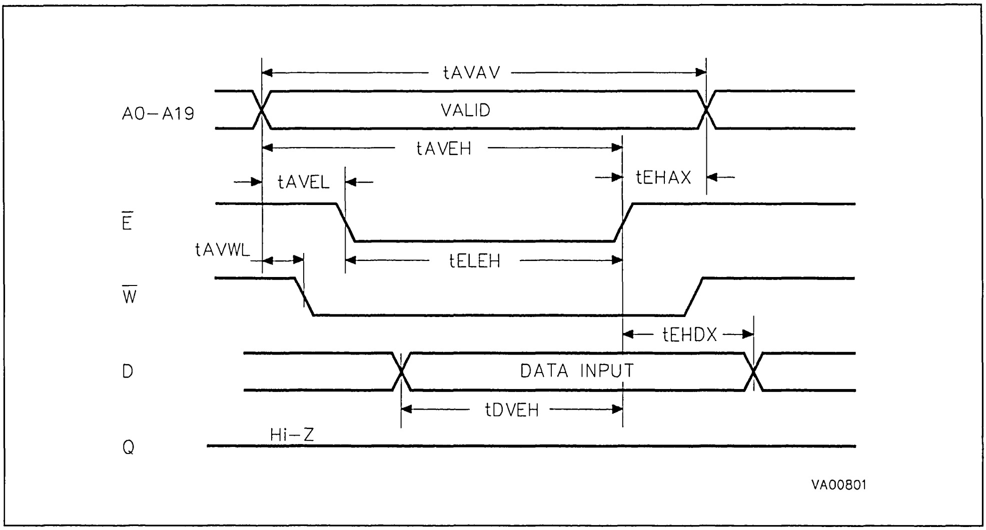
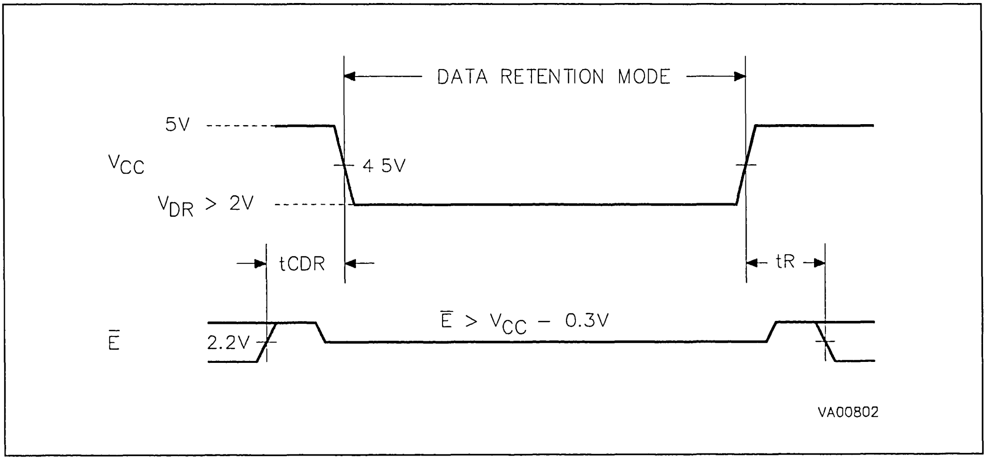

tAVAV
A0–A19
VALID
tAVEH
tAVEL
tEHAX
$\overline{E}$
tAVWL
tELEH
$\overline{W}$
tEHDX
D
DATA INPUT
tDVEH
Q
Hi–Z
VA00801

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

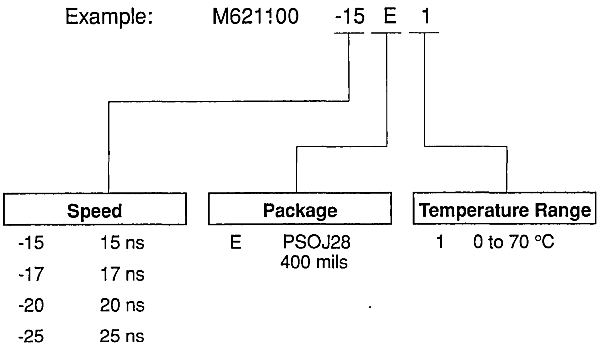
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.3V$, f = 0		1000	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Note: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
V_{CC}
4.5V
V_{DR} > 2V
tCDR
tR
$\overline{E}$ > V_{CC} – 0.3V
$\overline{E}$
2.2V
VA00802

ORDERING INFORMATION



Example: M621100 -15 E 1

Speed		Package		Temperature Range	
-15	15 ns	E	PSOJ28 400 mils	1	0 to 70 °C
-17	17 ns				
-20	20 ns				
-25	25 ns				

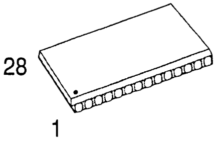
For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

M624256

VERY FAST CMOS 1 Megabit (256K x 4) SRAM WITH OUTPUT ENABLE

- 256K x 4 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIMES: 15, 17, 20, 25ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ, 400 mil PACKAGE



PSOJ28 (E)
400 mils

DESCRIPTION

The M624256 is a 1 Megabit (1,048,567 bit) Fast CMOS SRAM, organized as 262,144 words by 4 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ3	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

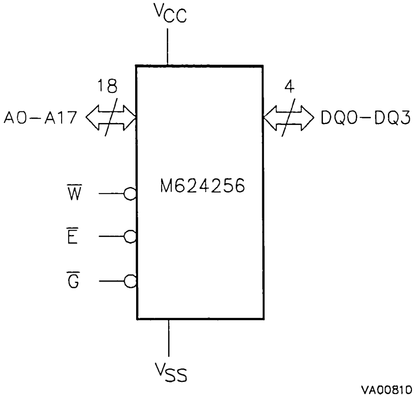


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
P_D	Power Dissipation	1	W

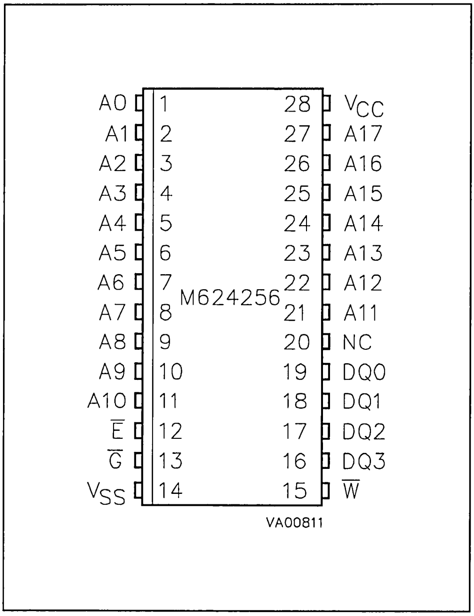
Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ3	Power
Read	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}.

Figure 2. SOJ Pin Connections



Warning: NC = No Connection.

READ MODE

The M624256 is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) asserted. This provides access to data from four of the 1,048,576 locations in the static memory array, specified by the 18 address inputs. Valid data will be available at the four output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M624256 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with $\overline{W}$ Low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

WRITE MODE (cont'd)

If the Output is enabled ($\overline{E}$ Low and $\overline{G}$ Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$ whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

OPERATIONAL MODE

The M624256 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E}$ High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$ and $\overline{E}$ as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

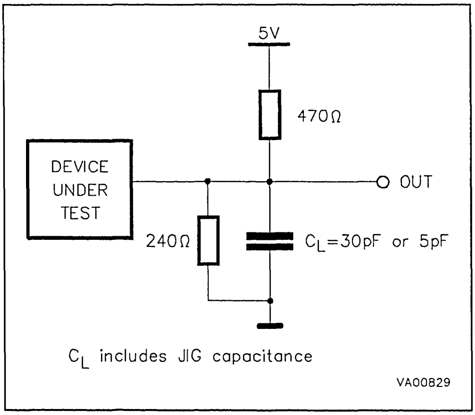


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN} [2]	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [3]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Except DQ0-DQ3
3 Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-15 & -17)		160	mA
		V_{CC} = 5.5V, (-20)		140	mA
		V_{CC} = 5.5V, (-25)		130	mA
I_{CC1} (2)	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E} = V_{IH}, f = 0$		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E} \ge V_{CC} - 0.2V,$ $f = 0$		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.2V$
3. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC} - 0.2V$

Table 6. Read and Standby Modes AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M624256								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	15		17		20		25		ns
t_{AVQV} (1)	Address Valid to Output Valid		15		17		20		25	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		15		17		20		25	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		7		8		10	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	2		2		2		2		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	9	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns
t_{PU} (3)	Chip Enable Low to Power Up	0		0		0		0		ns
t_{PD} (3)	Chip Enable High to Power Down		15		17		20		25	ns

Notes: 1. C_L = 30pF
2 C_L = 5pF
3 Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

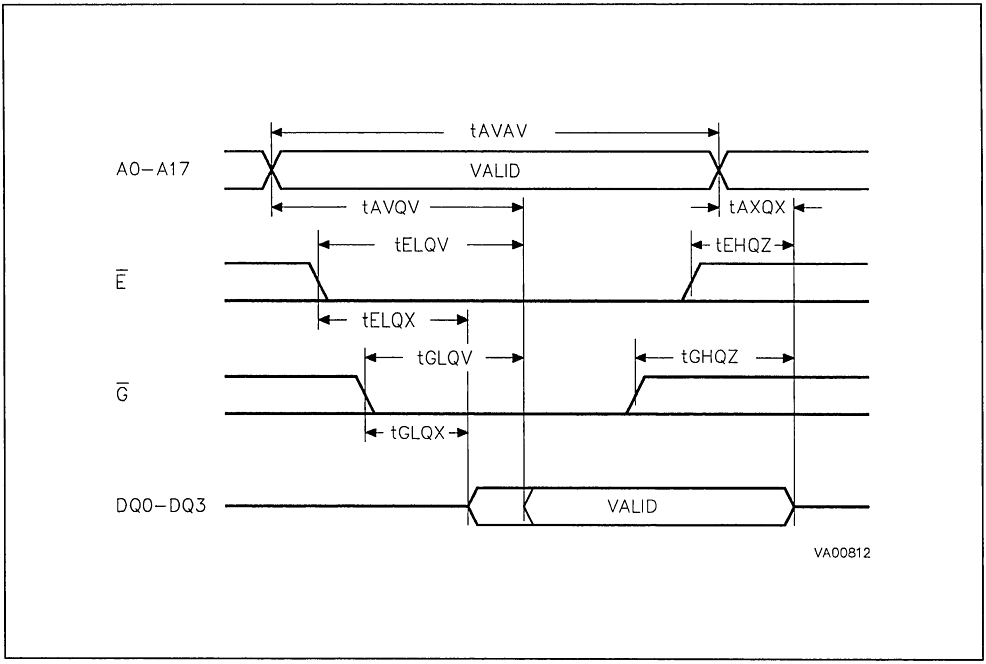

tAVAV
A0–A17
VALID
tAVQV
tAXQX
tELQV
tEHQZ
E̅
tELQX
tGLQV
tGHQZ
G̅
tGLQX
DQ0–DQ3
VALID
VA00812

Figure 5. Standby Mode AC Waveforms

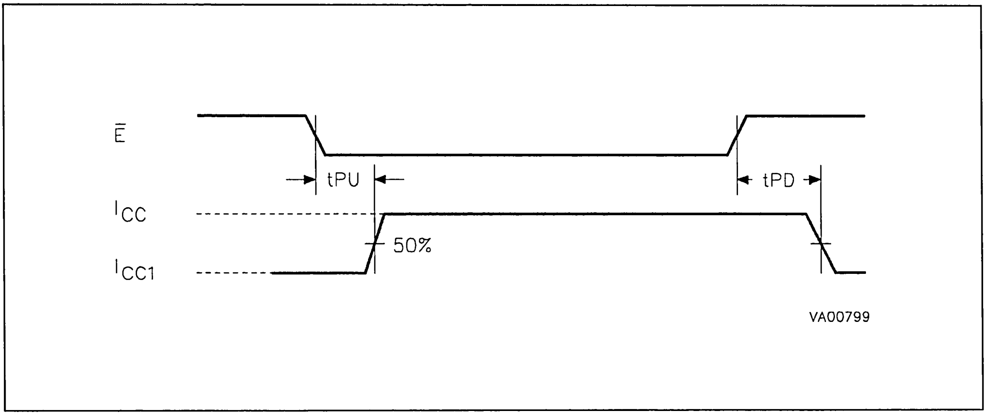

E̅
tPU
tPD
ICC
50%
ICC1
VA00799

Table 7. Write Mode AC Characteristics (T$_A$ = 0 to 70°C, V$_{CC}$ = 5V ± 10%)

Symbol	Parameter	M624256 -15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit
t_{AVAV}	Write Cycle Time	15		17		20		25		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	12		12		12		15		ns
t_{AVEH}	Address Valid to Chip Enable High	12		12		12		15		ns
t_{WLWH}	Write Enable Pulse Width	10		12		12		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	0	12	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	10		12		12		15		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	8		10		12		12		ns
t_{DVEH}	Input Valid to Chip Enable High	8		10		12		12		ns

Note: 1. C_L = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

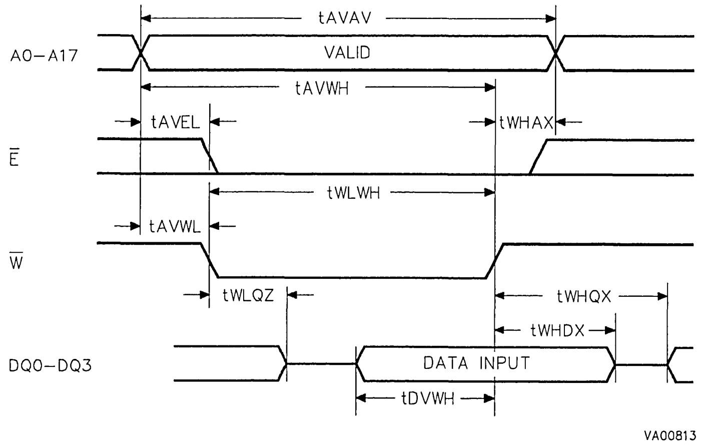


Figure 7. Chip Enable Controlled, Write AC Waveforms

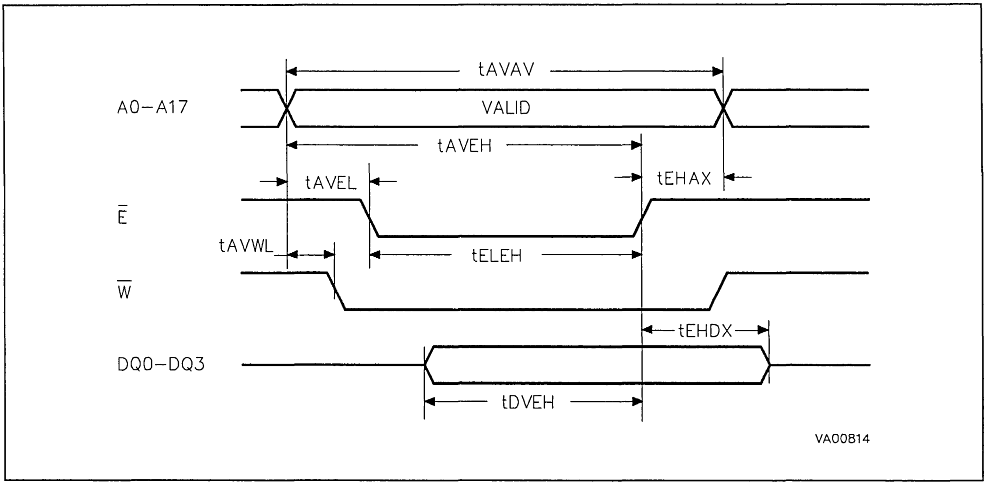
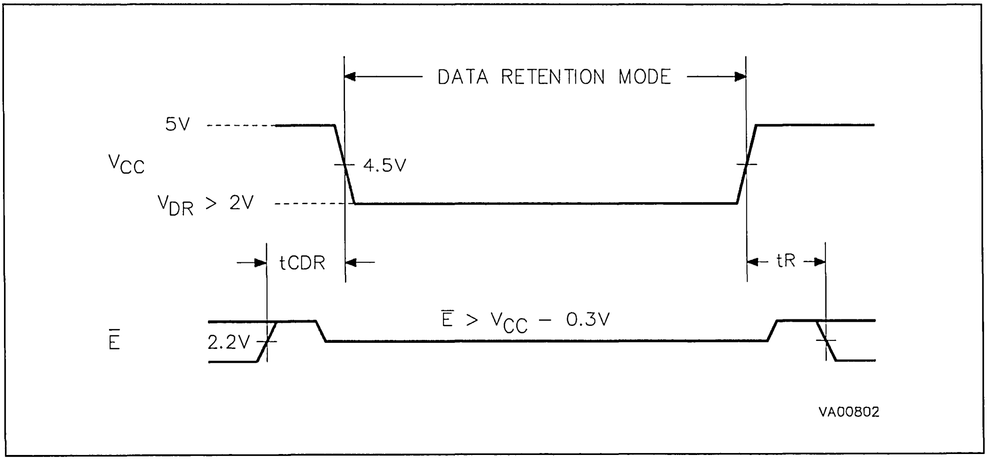

tAVAV
A0–A17
VALID
tAVEH
tAVEL
tEHAX
E̅
tAVWL
tELEH
W̅
tEHDX
DQ0–DQ3
tDVEH
VA00814

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E} \geq V_{CC} - 0.3V$, f = 0		1000	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E} \geq V_{CC} - 0.3V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0.3V$
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
VCC
4.5V
VDR > 2V
tCDR
tR
E̅ > VCC – 0.3V
E̅
2.2V
VA00802

ORDERING INFORMATION

Example: M624256 -15 E 1

Speed	
-15	15 ns
-17	17 ns
-20	20 ns
-25	25 ns

Package	
E	PSOJ28 400 mils

Temperature Range	
1	0 to 70 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

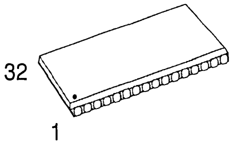
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M628128

VERY FAST CMOS 1 Megabit (128K x 8) SRAM WITH OUTPUT ENABLE

- 128K x 8 CMOS FAST SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE AND ACCESS TIMES: 15, 17, 20, 25ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ, 400 mil PACKAGE



PSOJ32 (E)
400 mils

DESCRIPTION

The M628128 is a 1 Megabit (1,048,576 bit) Fast CMOS SRAM, organized as 131,072 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

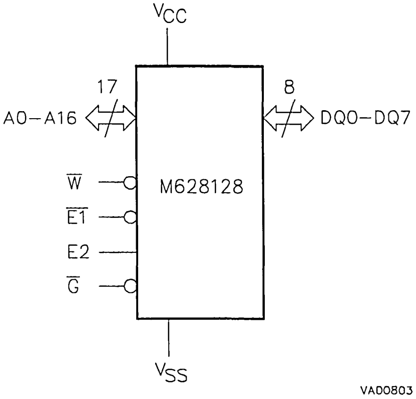


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (1)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (2)	Output Current	20	mA
PD	Power Dissipation	1	W

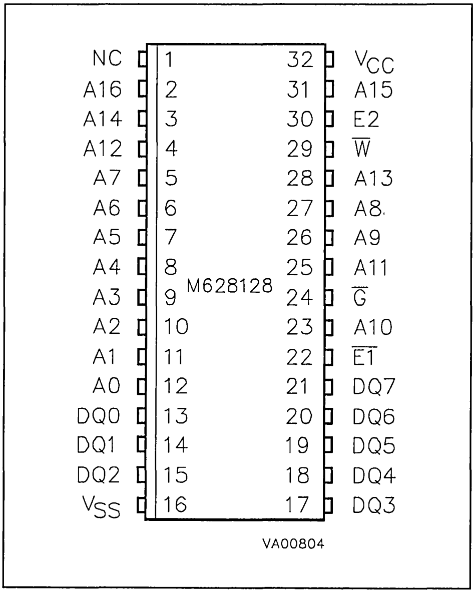
Notes: 1. Up to a maximum operating V_{CC} of 5.5V only.
2. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 2. SOJ Pin Connections



Warning: NC = No Connection.

READ MODE

The M628128 is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and both Chip Enables ($\overline{E1}$ and E2) are asserted. This provides access to data from eight of the 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, $\overline{E1}$ is Low and E2 is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M628128 is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low, with E2 High. Either the Chip Enable inputs ($\overline{E1}$ and E2) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore, address setup time is referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge.

WRITE MODE (cont'd)

The Write cycle can be terminated by the earlier rising edge of $\overline{\text{E1}}$, $\overline{\text{W}}$, or the falling edge of E2.

If the Output is enabled ($\overline{\text{E1}}$ Low, E2 High and $\overline{\text{G}}$ Low), then $\overline{\text{W}}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{\text{E1}}$ or for t_{DVE2L} before the falling edge of E2, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

OPERATIONAL MODE

The M628128 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{\text{E1}}$ High or E2 Low). An Output Enable ($\overline{\text{G}}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{\text{W}}$, $\overline{\text{E1}}$, and E2 as summarized the Operating Mode table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

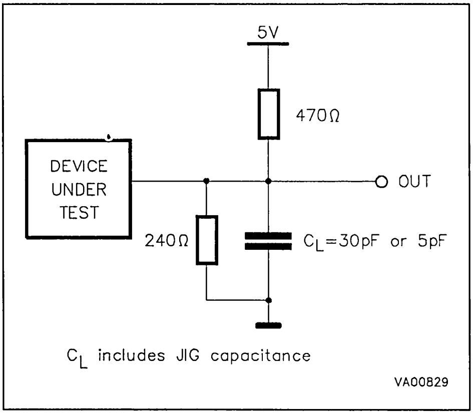


Table 4. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT} [(2)]	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC} (1)	Supply Current	V_{CC} = 5.5V, (-15 & -17)		160	mA
		V_{CC} = 5.5V, (-20)		140	mA
		V_{CC} = 5.5V, (-25)		130	mA
I_{CC1} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E1} = V_{IH}$ or E2 = V_{IL}, f = 0		25	mA
I_{CC1} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E1} \geq V_{CC} - 0.3V$ or E2 ≤ 0.3V, f = 0		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
3. All other Inputs at $V_{IL} \leq 0.3V$ or $V_{IH} \geq V_{CC} - 0.3V$

Table 6. Read and Standby Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628128								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	15		17		20		25		ns
t_{AVQV} (1)	Address Valid to Output Valid		15		17		20		25	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		15		17		20		25	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		15		17		20		25	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		7		8		10	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	2		2		2		2		ns
t_{E2HQX}	Chip Enable 2 High to Output Transition	2		2		2		2		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		0		0		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z	0	8	0	10	0	10	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	8	0	9	0	10	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		3		3		ns
t_{PU} (3)	Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		0		0		0		ns
t_{PD} (3)	Chip Enable 1 High or Chip Enable 2 Low to Power Down		15		17		20		25	ns

Notes: 1. C_L = 30pF
2. C_L = 5pF
3 Measured to 50% point between I_{CC} and I_{CC1}.

Figure 4. Read Mode AC Waveforms

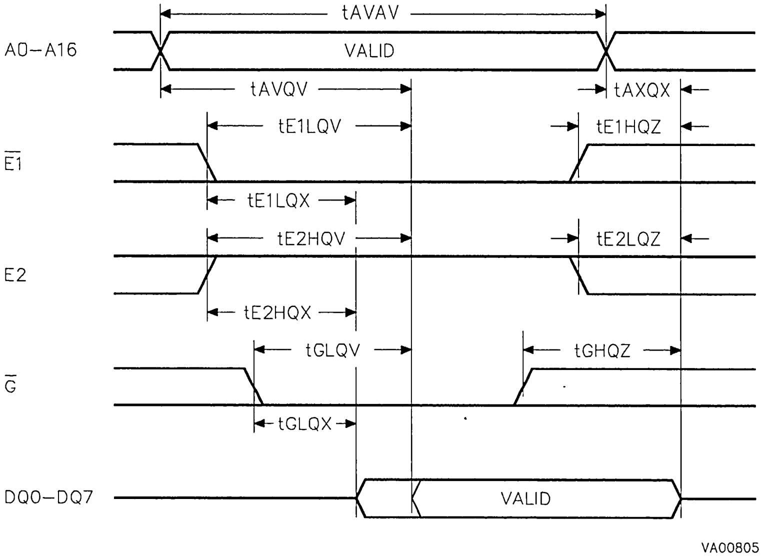

tAVAV
A0–A16
VALID
tAVQV
tAXQX
tE1LQV
tE1HQZ
E1
tE1LQX
tE2HQV
tE2LQZ
E2
tE2HQX
tGLQV
tGHQZ
G
tGLQX
DQ0–DQ7
VALID
VA00805

Figure 5. Standby Mode AC Waveforms

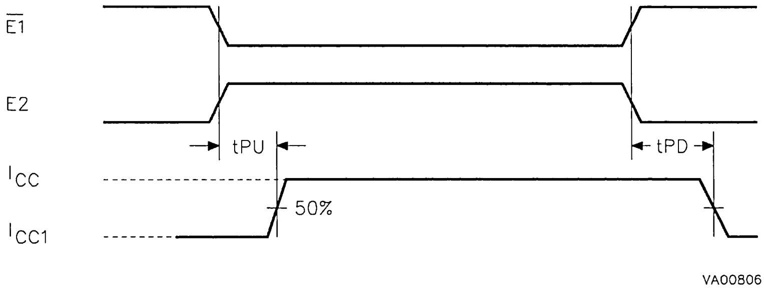

E1
E2
tPU
tPD
ICC
50%
ICC1
VA00806

Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	M628128								Unit
		-15		-17		-20		-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	15		17		20		25		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{AVWH}	Address Valid to Write Enable High	12		12		12		15		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	12		12		12		15		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	12		12		12		15		ns
t_{WLWH}	Write Enable Pulse Width	10		12		12		15		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	8	0	10	0	12	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		0		0		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	10		12		12		15		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	10		12		12		15		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		0		0		0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		0		0		0		ns
t_{DVWH}	Input Valid to Write Enable High	8		10		12		12		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	8		10		12		12		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	8		10		12		12		ns

Note: 1. C_L = 5pF

Figure 6. Write Enable Controlled, Write AC Waveforms

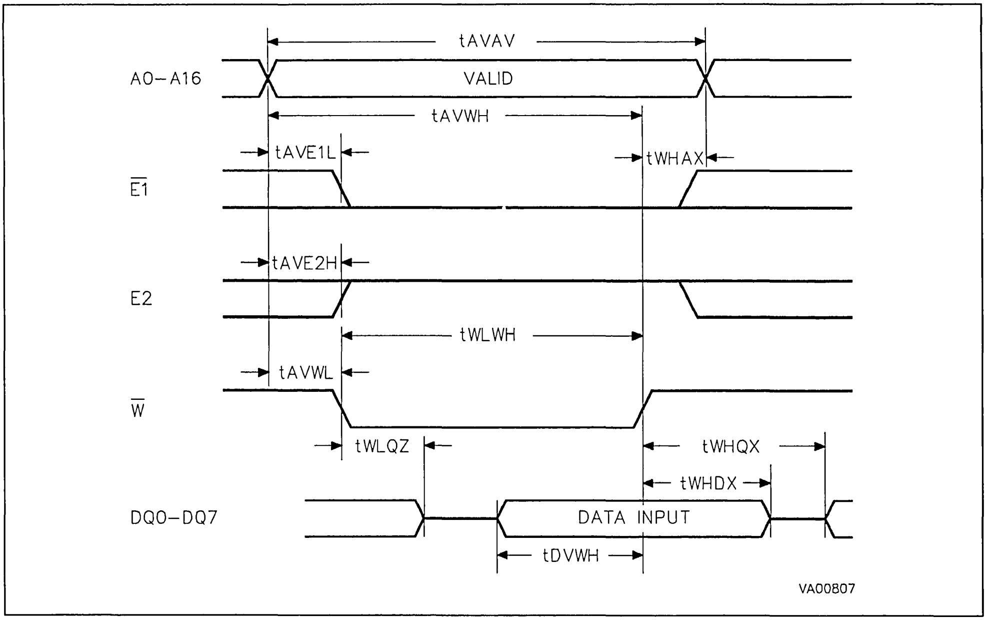

tAVAV
A0-A16
VALID
tAVWH
tAVE1L
tWHAX
E1
tAVE2H
E2
tWLWH
tAVWL
W
tWLQZ
tWHQX
tWHDX
DQ0-DQ7
DATA INPUT
tDVWH
VA00807

Figure 7. Chip Enable Controlled, Write AC Waveforms

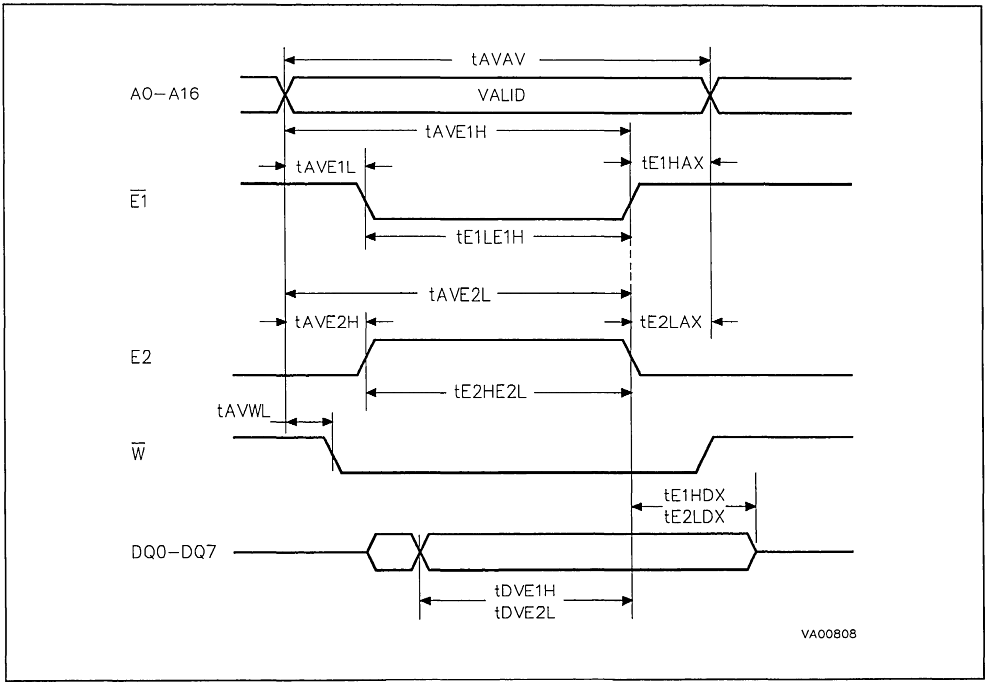
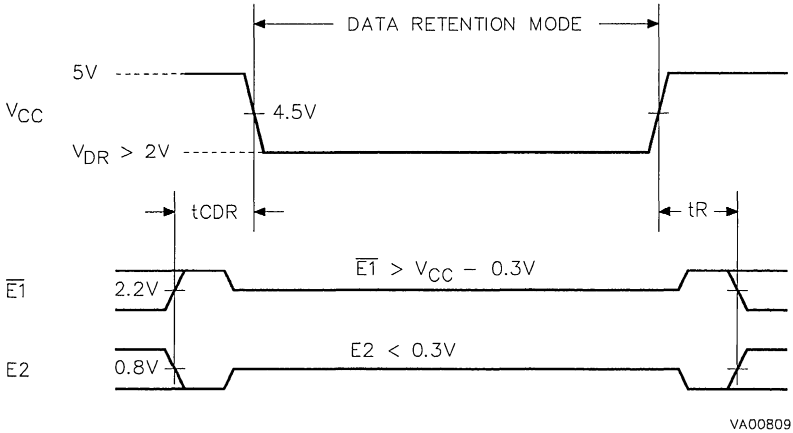

tAVAV
A0-A16
VALID
tAVE1H
tAVE1L
tE1HAX
E1
tE1LE1H
tAVE2L
tAVE2H
tE2LAX
E2
tE2HE2L
tAVWL
W
tE1HDX
tE2LDX
DQ0-DQ7
tDVE1H
tDVE2L
VA00808

Table 8. Low V_{CC} Data Retention Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

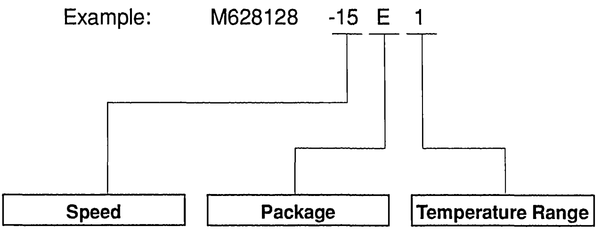
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CC2} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E1} \geq V_{CC} - 0.3V$, E2 ≤ 0.3V, f = 0		1000	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC} - 0.3V$, E2 ≤ 0.3V, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E1} \geq V_{CC} - 0.3V$, E2 ≤ 0.3V, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.3V$ or $V_{IL} \leq 0$ 3V
2. See Figure 8 for measurement points. Guaranteed but not tested

Figure 8. Low V_{CC} Data Retention AC Waveforms


DATA RETENTION MODE
5V
VCC
4.5V
VDR > 2V
tCDR
tR
E1
2.2V
E1 > VCC – 0.3V
E2
0.8V
E2 < 0.3V
VA00809

ORDERING INFORMATION


Example: M628128 -15 E 1
Speed
Package
Temperature Range

Speed	
-15	15 ns
-17	17 ns
-20	20 ns
-25	25 ns

Package	
E	PSOJ32 400 mils

Temperature Range	
1	0 to 70 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

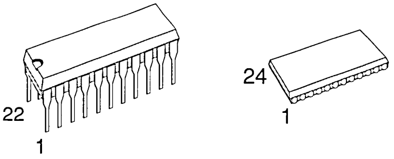
CACHE MEMORIES

SGS-THOMSON
MICROELECTRONICS

MK41S80

VERY FAST CMOS 4K x 4 CACHE TAGRAM

- 4K x 4 FAST HCMOS CACHE TAGRAM
- ADDRESS TO COMPARE ACCESS TIMES: 10,12,15,20,25ns
- FLASH CLEAR FUNCTION
- 22-PIN 300 MIL PLASTIC DIP
  24-PIN 300 MIL SOJ
- APPLICATIONS: HIGH SPEED 32-BIT CACHE SUB-SYSTEMS



PSDIP22 (N)

PSOJ24 (X)
300 mils

DESCRIPTION

The MK41S80 is a 16,384-bit CMOS Static TAGRAM™, organized as 4K x 4 using SGS-THOMSON Microelectronics' advanced fast HCMOS process technology. This device is functionally compatible with the industry standard MK41H80 4K x 4 TAGRAM. All inputs and outputs are TTL compatible using a single 5V supply.

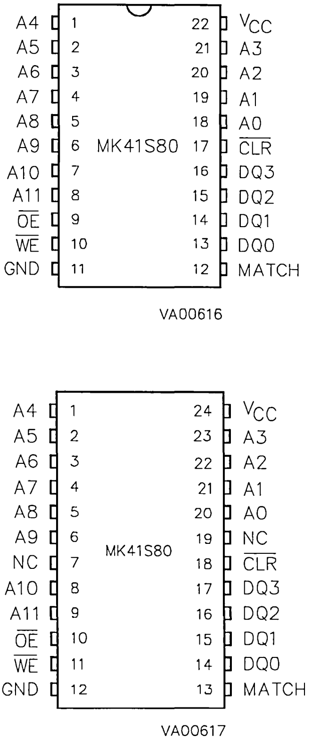
The MK41S80 provides full static operation, requiring no external clocks or refresh operations, and features a MATCH output for indicating either a cache hit or miss condition. The on-board 4-bit comparator compares RAM contents with current input (tag) data. The result is an active high level on the MATCH pin for a hit, or an active low on the MATCH pin indicating a miss. The MK41S80 offers a totem-pole MATCH output design.

The MK41S80 incorporates a Flash Clear Cycle which begins as $\overline{\text{CLR}}$ is brought active low. A Flash Clear sets all 16,384 bits in the RAM to logic zero.

Pin Names

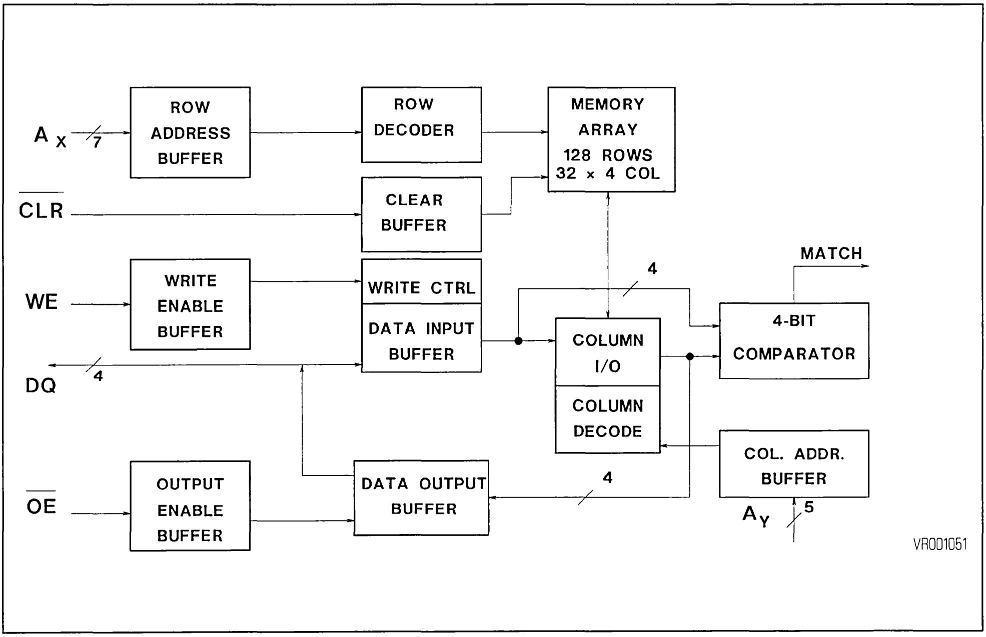
A0-A11	Address Inputs
DQ0-DQ3	Data Inputs / Outputs
MATCH	Comparator Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CLR}}$	RAM Flash Clear
V_{CC}, GND	+5 Volts, Ground
NC	Not Connected

Figure 1. Pin Connections


A4 1
A5 2
A6 3
A7 4
A8 5
A9 6
A10 7
A11 8
OE 9
WE 10
GND 11
22 VCC
21 A3
20 A2
19 A1
18 A0
17 CLR
16 DQ3
15 DQ2
14 DQ1
13 DQ0
12 MATCH
MK41S80
VA00616
A4 1
A5 2
A6 3
A7 4
A8 5
A9 6
NC 7
A10 8
A11 9
OE 10
WE 11
GND 12
24 VCC
23 A3
22 A2
21 A1
20 A0
19 NC
18 CLR
17 DQ3
16 DQ2
15 DQ1
14 DQ0
13 MATCH
MK41S80
VA00617

February 1992

Figure 2. MK41S80 Block Diagram


A_X
7
ROW ADDRESS BUFFER
ROW DECODER
MEMORY ARRAY 128 ROWS 32 x 4 COL
$\overline{CLR}$
CLEAR BUFFER
WE
WRITE ENABLE BUFFER
WRITE CTRL
DATA INPUT BUFFER
DQ
4
4
MATCH
COLUMN I/O
COLUMN DECODE
4-BIT COMPARATOR
COL. ADDR. BUFFER
A_Y
5
$\overline{OE}$
OUTPUT ENABLE BUFFER
DATA OUTPUT BUFFER
4
VR001051

TAGRAM FUNCTION

The MK41S80 is an SRAM based Cache Tag directory (hence the name TAGRAM). Figure 7 shows a general block diagram using a cache tag directory (TAGRAM) in a cache subsystem application. The system must detect whether the requested data resides in the cache data RAM, or if extended read cycles to main memory are necessary.

The MK41S80 features four modes of operation: Write, Read, Compare, and Clear. The MK41S80 incorporates an on-board 4 bit comparator that compares internal RAM contents with current (tag) input data. If the device is in the compare mode, and the comparator detects a "match", then the MATCH pin will go high for a hit condition. If a match is not detected by the comparator, then the MATCH pin drives low to denote a "miss" condition. Standard write/read operations are performed with Write ($\overline{WE}$) and Output ($\overline{OE}$) Enable inputs. Additionally, the device provides a Flash Clear operation via the $\overline{CLR}$ pin (Figure 6). When a low level (V_{IL}) is applied to the $\overline{CLR}$ input pin for the specified t_{CLP} time, all RAM bits are set to a logic zero.

Compare data (internal RAM) can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ0 - DQ3).

MK41S80 TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	Match	Mode
H	H	H	Valid	Compare
L	X	H	Invalid	Write
H	L	H	Invalid	Read
X	X	L	Invalid	RAM Clear

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 0.5 to 6	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	– 65 to 150	°C
P_D	Power Dissipation	1	W
I_O(2)	Output Current	50	mA

Notes :

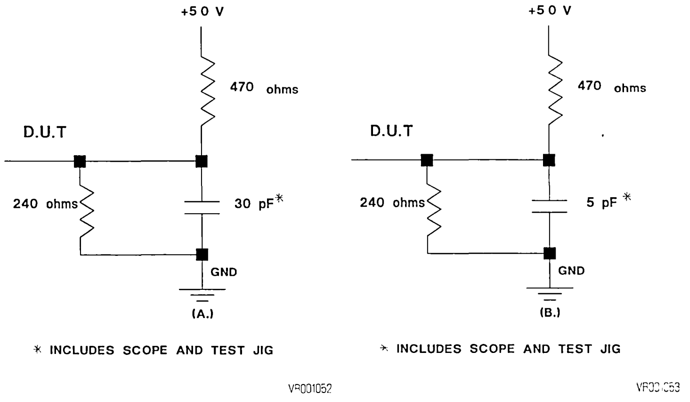
1. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliare-liability
2. Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels(1)	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5 %	V

Note: 1. AC input levels for the $\overline{\text{CLR}}$ pin are GND to 3.5 V.

Figure 3. Equivalent Output Load Circuits


+5 0 V
470 ohms
D.U.T
240 ohms
30 pF*
GND
(A.)
* INCLUDES SCOPE AND TEST JIG
VR001052
+5 0 V
470 ohms
D.U.T
240 ohms
5 pF *
GND
(B.)
* INCLUDES SCOPE AND TEST JIG
VR00:C53

COMPARE, WRITE, AND READ TIMING

The MK41S80 TAGRAM begins a Compare Cycle with the application of a valid address (see Figure 4). A valid compare is enabled when $\overline{OE}$ and $\overline{WE}$ go high in conjunction with their respective set-up and hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In (Tag). If the address and tag data are presented simultaneously, the compare-to-match access is t_{ACA}. MATCH will go invalid t_{ACH} after an address change, or t_{DCH} after the tag data changes.

A Write Cycle starts with stable addresses (Figures 4 and 5), with the $\overline{WE}$ input active low. $\overline{OE}$ may be in either logic state. $\overline{WE}$ may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be valid t_{DS} before and t_{DH} after $\overline{WE}$ goes high. DQ will go high-Z at t_{WEZ} from $\overline{WE}$ going active low. MATCH will be invalid during this cycle.

The device begins a Read Cycle with stable addresses and $\overline{WE}$ high (Figure 5). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of $\overline{OE}$. The DQ outputs become invalid t_{OH} after addresses become invalid, and become high-Z at t_{OEZ} when $\overline{OE}$ goes high. Ripple through data access may be accomplished by holding $\overline{OE}$ active low while strobing address A0-A11, and holding $\overline{CLR}$ and $\overline{WE}$ high. The MATCH output will be invalid during this cycle.

FLASH CLEAR CYCLE

The MK41S80 incorporates a Flash Clear Cycle which begins as $\overline{CLR}$ is brought active low. A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control inputs will not be recognized from t_{CX} after $\overline{CLR}$ goes low, until t_{CR} after $\overline{CLR}$ is brought high. The $\overline{OE}$ and $\overline{WE}$ inputs are Don't Care, and DQ is High-Z. MATCH will be invalid during a Flash Clear Cycle.

APPLICATION

The MK41S80 operates from a single 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Also, because the outputs can drive rail-to-rail into high impedance loads, the device can interface to 5 volt CMOS on its inputs and outputs.

The MK41S80 compares contents of addressed RAM locations to the current tag data inputs. A logic one "1" output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero "0" on the MATCH pin

Figure 4. Compare and Write Cycle

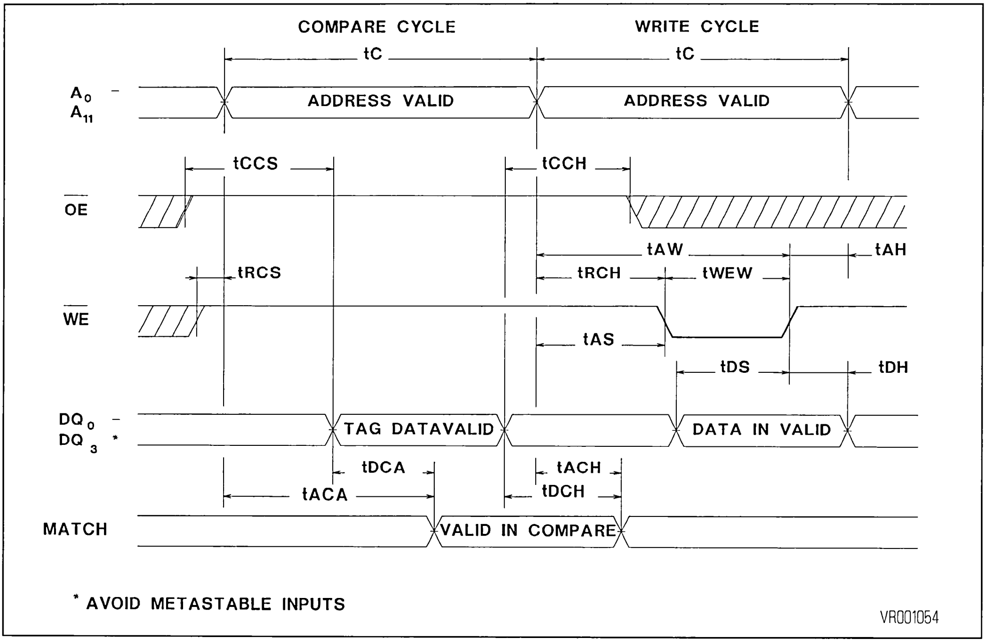


Figure 5. Write and Read Cycle

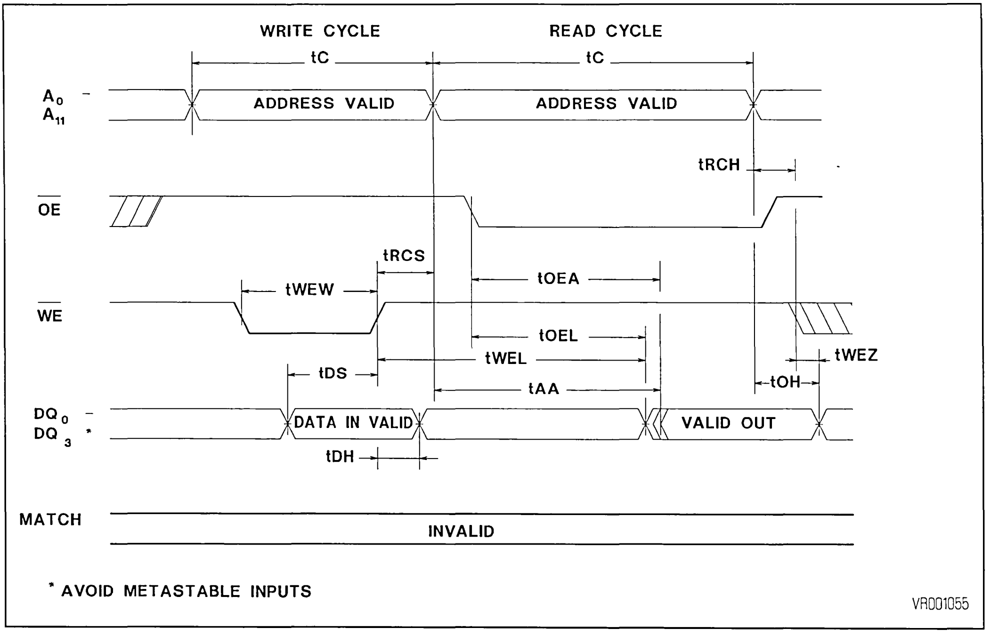
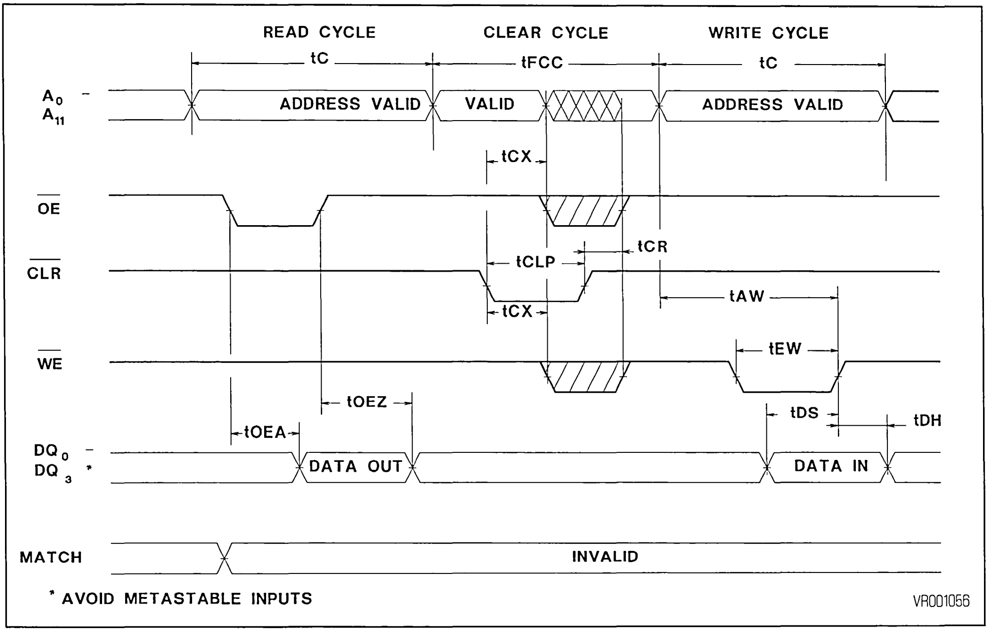

WRITE CYCLE
READ CYCLE
tC
tC
A_0 – A_{11}
ADDRESS VALID
ADDRESS VALID
tRCH
OE
tRCS
tOEA
tWEW
WE
tOEL
tWEL
tWEZ
tDS
tOH
tAA
DQ_0 – DQ_3 *
DATA IN VALID
VALID OUT
tDH
MATCH
INVALID
* AVOID METASTABLE INPUTS
VR001055

Figure 6. Read-Flash Clear-Write Cycle

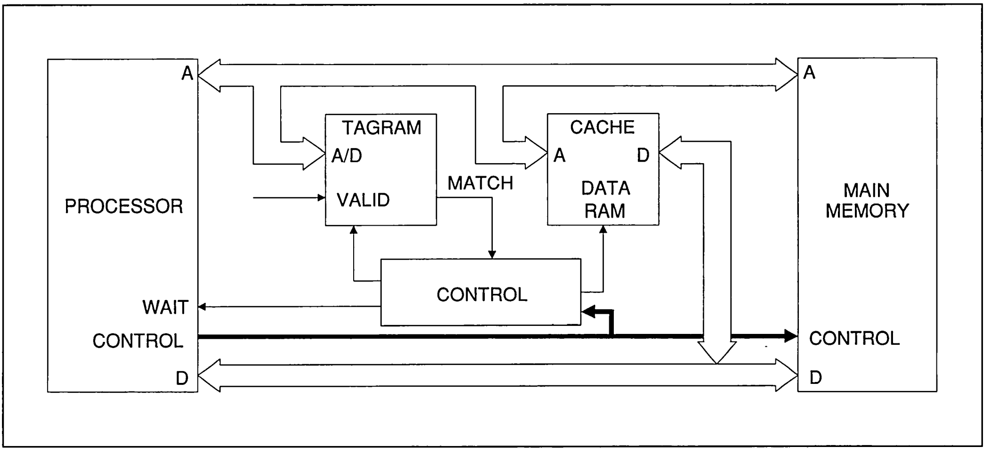

READ CYCLE
CLEAR CYCLE
WRITE CYCLE
tC
tFCC
tC
A_0 – A_{11}
ADDRESS VALID
VALID
ADDRESS VALID
tCX
OE
tCR
tCLP
CLR
tAW
tCX
tEW
WE
tOEZ
tDS
tDH
tOEA
DQ_0 – DQ_3 *
DATA OUT
DATA IN
MATCH
INVALID
* AVOID METASTABLE INPUTS
VR001056

indicates at least one bit of difference between the RAM contents and input data.

Metastable inputs can result in excessive MATCH output activity. Therefore, the use of pull-up or pull-down resistors is recommended on the data bus. Additionally, a pull-up resistor is suggested for the $\overline{\text{CLR}}$ input to enhance system operation. This will ensure that any low going system noise coupled onto the input does not drive $\overline{\text{CLR}}$ below V_{IH} minimum specifications.

Because high frequency current transients will be associated with the operation of the MK41S80, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding, or separate power planes can be employed to reduce line inductance. Additionally, any low impedance transmission lines are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination is suggested in close proximity to the drivers to improve driver/signal path impedance matching.

Figure 7. General Cache Subsystem Block Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATION

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	-10		-12		-15		-20		-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_C	Cycle Time	15		15		20		20		25		ns	
t_{CCS}	Compare Command Set-Up Time	4		5		6		7		8		ns	
t_{CCH}	Compare Command Hold Time	0		0		0		0		0		ns	
t_{RCS}	Read Command ($\overline{WE}$) Set-Up Time	0		0		0		0		0		ns	
t_{RCH}	Read Command ($\overline{WE}$) Hold Time	0		0		0		0		0		ns	
t_{AS}	Address Set-Up Time	0		0		0		0		0		ns	
t_{AW}	Address to End of Write ($\overline{WE}$)	10		10		12		16		20		ns	
t_{AH}	Address Hold after End of Write	1		1		1		1		1		ns	
t_{WEW}	Write Command ($\overline{WE}$) Pulse Width	10		11		12		16		20		ns	
t_{DS}	Data Set-Up Time	10		12		12		12		13		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{DCA}	Data (Tag) Compare Access Time		7		8		10		12		15	ns	3
t_{ACA}	Address Compare (Match) Access Time		10		12		15		20		25	ns	3
t_{ACH}	Address Compare Hold Time	2		2		2		2		2		ns	3
t_{DCH}	Data Compare Hold Time	0		0		0		0		0		ns	3
t_{OEA}	Output Enable ($\overline{OE}$) Access Time		8		8		10		10		12	ns	3
t_{OH}	Output (Q) Hold Time	2		2		2		2		2		ns	3
t_{AA}	Address to Valid Data Out Access Time		12		15		20		20		25	ns	3
t_{OEZ}	Output Enable ($\overline{OE}$) High to Q High-Z		7		7		7		7		7	ns	4
t_{OEL}	Output Enable ($\overline{OE}$) Low to Q Active	0		0		0		0		0		ns	4
t_{WEZ}	Write Enable ($\overline{WE}$) High to Q High-Z		7		7		7		7		7	ns	4
t_{WEL}	Write Enable ($\overline{WE}$) High to Q Active	1		1		1		1		1		ns	4
t_{FCC}	Flash Clear Cycle Time	50		50		50		50		50		ns	
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		0		0		0		ns	
t_{CR}	End of Clear to Inputs Recognized	0		0		0		0		0		ns	
t_{CLP}	Flash Clear Pulse Width	35		35		35		35		35		ns	

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}	Supply Voltage	4.75	5	5.25	V	1
GND	Ground	0	0	0	V	1
V_{IH}	Logic 1 All Inputs	2.2	3	$V_{CC} + 0.3$	V	1
V_{IL}	Logic 0 All Inputs	0.3	0.2	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current (Both Ports)		120	mA	5
I_{LI}	Input Leakage Current (Any Input)	– 1	1	µA	2
I_{LO}	Output Leakage Current	– 10	10	µA	2
V_{OH}	Output Logic 1 Voltage (I_{OH} = -4.0mA)	2.4		V	1
V_{OL}	Output Logic 0 Voltage (I_{OL} = 8mA)		0.4	V	1

CAPACITANCE

($T_A = 25°C$, f = 1.0 MHz)

Symbol	Parameter	Typ.	Max.	Unit	Notes
C_I	Input Capacitance on all pins (except DQ)	4	6	pF	7
C_O	Output Capacitance	8	10	pF	6, 7

Notes :

1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC}. Outputs are deselected with the exception to MATCH which is always enabled.
3 Measured with load as shown in Figure 3A.
4. Measured with load as shown in Figure 3B.
5. I_{CC1} measured with outputs open, $V_{CC\ max}$, f = min cycle.
6. Output buffer is deselected
7. Capacitances are sampled and not 100% tested.

ORDERING INFORMATION

Example: MK41S80 X 10 /20

Package	
N	PSDIP22
X	PSOJ24 300 mils

Speed	
10	10ns
12	12ns
15	15ns
20	20ns
25	25ns

Option	
/20	Tape & Reel

For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

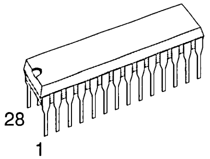
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

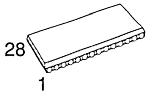
MK48S74

VERY FAST CMOS 8K x 8 CACHE TAGRAM

- 8K x 8 CMOS SRAM WITH ONBOARD COMPARATOR
- ADDRESS TO COMPARE ACCESS TIME: 20, 25, 35ns
- FAST CHIP SELECT COMPARE ACCESS 10ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF 12ns Max
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE
- FULL CMOS FOR LOW POWER OPERATION
- OPEN DRAIN MATCH OUTPUT
- 28 PIN 300 MIL DIP & 28 PIN 300 MIL SOJ



PSDIP28 (N)



PSOJ28 (X)
300 mils

TRUTH TABLE

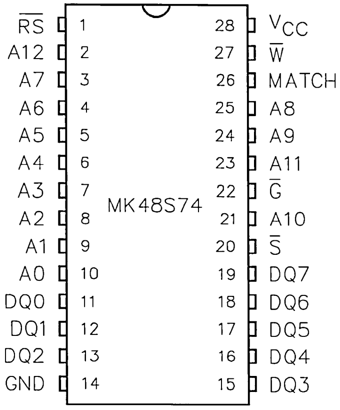
$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	Mode	DQ	Match
X	X	X	L	Reset Clear	High-Z	Invalid
X	H	X	H	Deselect	High-Z	Invalid
H	L	H	H	Miss	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High-Z
H	L	L	H	Read	Q_{OUT}	Invalid
L	L	X	H	Write	D_{IN}	Invalid

Note: MATCH is High-Z during an invalid state

PIN NAMES

A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
MATCH	Comparator Output
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RS}$	Rest Flash Clear
V_{CC}, GND	5 Volts, Ground

Figure 1. Pin Connection


RS 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
28 VCC
27 W
26 MATCH
25 A8
24 A9
23 A11
22 G
21 A10
20 S
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
MK48S74

VA00625

DESCRIPTION

The MK48S74 is a 65, 536 fast static cache TAGRAM™ organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMOS4 technology. The MK48S74 features fully static operation requiring no external clocks or timing strobes, and equal access and cycle times. The device requires a single 5V ± 5 % supply and is fully TTL compatible. The MK48S74 has a fast Chip Select control for high speed oper-ation to the Match Compare valid, and device se-lect/deselect operations. Additionally, the MK48S74 provides a Reset Clear, and MATCH compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only two cycles. The MATCH output features an open drain for wired-OR operations. During a MATCH compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A0-A12) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

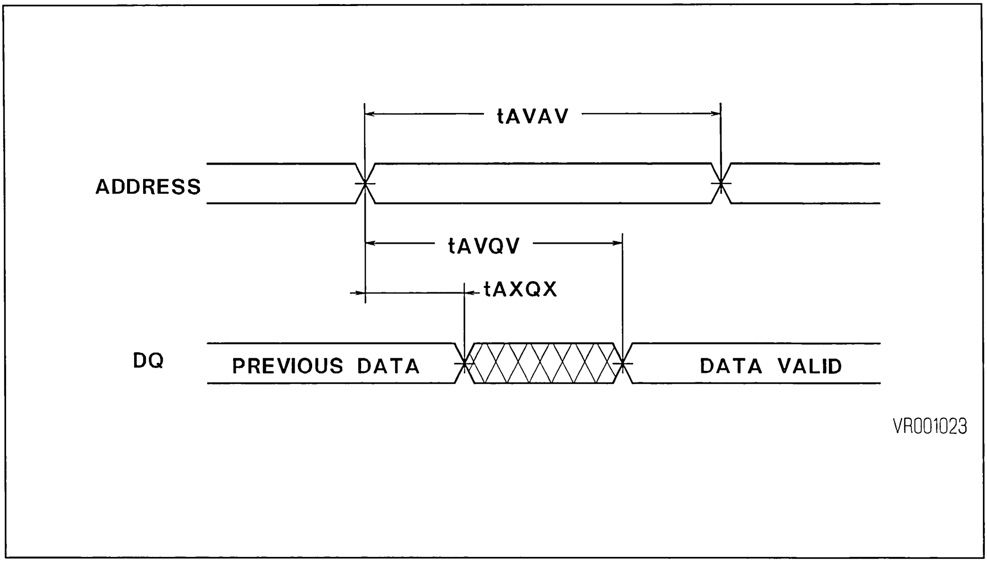
READ MODE

The MK48S74 is in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65, 536 locations in the static memory array. The unique address specified by the 13 address inputs defines which one of the 8192-8-bit bytes is to be accessed. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW and $\overline{S}$ is LOW. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV} rather than the addresses. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$ and $\overline{W}$ control signals. Data out may be inderterminate at t_{SLQX} and t_{GLQX} but data lines will always be valid at t_{AVQV}.

READ CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

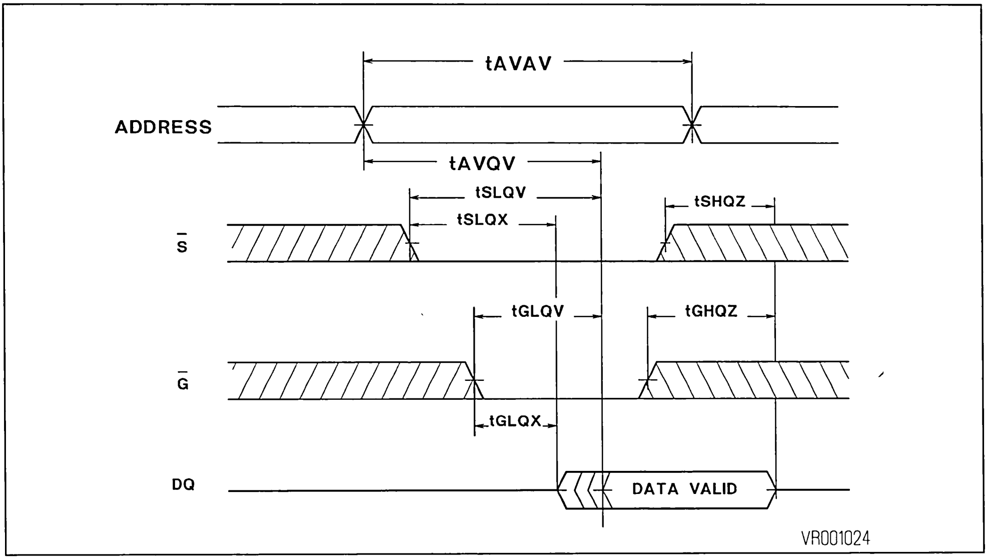
Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AVQV}	t_{AA}	Address Access Time		20		25		35	ns	1
t_{SLQV}	t_{CSA}	Chip Select Access Time		15		15		20	ns	
t_{GLQV}	t_{OEA}	Output Enable Access Time		15		15		20	ns	1
t_{SLQX}	t_{CSL}	Chip Select to Output Low-Z	0		0		0		ns	
t_{GLQX}	t_{OEL}	Output Enable to Low-Z	0		0		0		ns	
t_{SHQZ}	t_{CSZ}	Chip Select to High-Z		9		9		9	ns	
t_{GHQZ}	t_{OEZ}	Output Enable to High-Z		8		8		8	ns	2
t_{AXQX}	t_{OH}	Output Hold From Address Change	3		3		3		ns	1

Figure 2. Read Timing No. 1 (Address Access)


tAVAV
ADDRESS
tAVQV
tAXQX
DQ
PREVIOUS DATA
DATA VALID
VR001023

Note: Chip Select and Output Enable one presumed valid, $\overline{W}$ = V_{IH}

Figure 3. Read Timing No. 2 (W = V_{IH})


tAVAV
ADDRESS
tAVQV
tSLQV
tSLQX
tSHQZ
$\overline{S}$
tGLQV
tGHQZ
$\overline{G}$
tGLQX
DQ
DATA VALID
VR001024

WRITE MODE

The MK48S74 is the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL} and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$. If the outputs are enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

WRITE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AVWL}	t_{AS}	Address Set-up to Write Enable Low	0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up to Chip Select	0		0		0		ns	
t_{AVWH}	t_{AW}	Address Valid to End of Write	15		20		25		ns	
t_{WLWH}	t_{WEW}	Write Pulse Width	15		20		25		ns	
t_{WHAX}	t_{AH}	Address Hold Time After End of Write	0		0		0		ns	
t_{SLSH}	t_{CSW}	Chip Select to End of Write	15		20		25		ns	
t_{SHAX}	t_{WR}	Write Recovery Time To Chip Select	0		0		0		ns	
t_{DVWH}	t_{DW}	Data Valid to End of Write	10		13		15		ns	
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		ns	
t_{WHQX}	t_{WEL}	Write High to Output Low-Z (Active)	0		0		0		ns	2
t_{WLQZ}	t_{WEZ}	Write Enable to Output High-Z		5		5		5	ns	2

Figure 4. Writing Timing No.1 (Write Control)

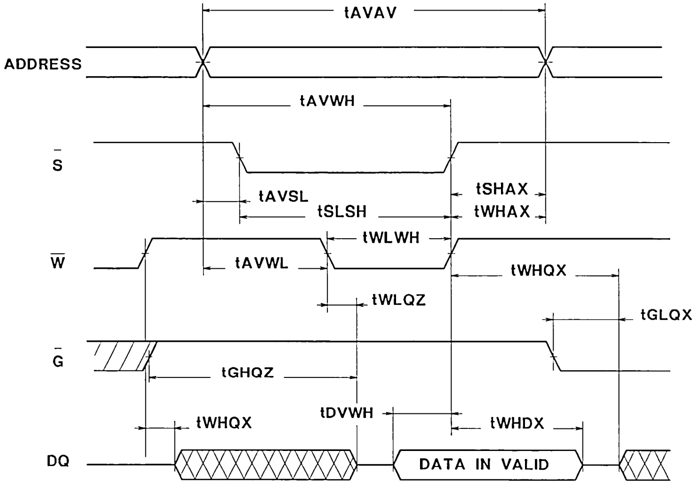
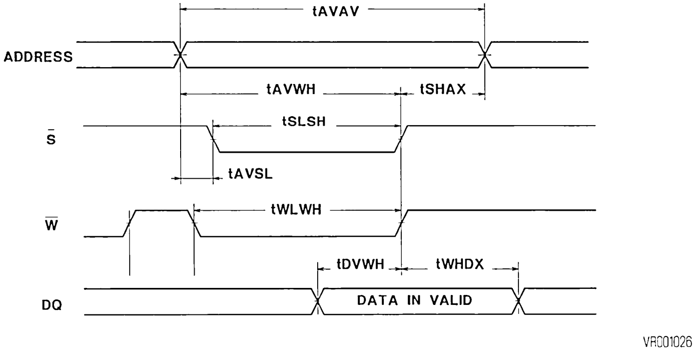

tAVAV
ADDRESS
tAVWH
$\overline{S}$
tAVSL
tSLSH
tSHAX
tWHAX
$\overline{W}$
tWLWH
tAVWL
tWHQX
tWLQZ
tGLQX
$\overline{G}$
tGHQZ
tDVWH
tWHQX
tWHDX
DQ
DATA IN VALID
VR001025

Figure 5. Writing Timing No. 2 (Chip Select Control)


tAVAV
ADDRESS
tAVWH
tSHAX
tSLSH
$\overline{S}$
tAVSL
tWLWH
$\overline{W}$
tDVWH
tWHDX
DQ
DATA IN VALID
VR001026

Note: $\overline{G} = V_{IH}$

COMPARE MODE

THe MK48S74 is in the Compare mode whevenver $\overline{W}$ and $\overline{G}$ are HIGH provided Chip Select ($\overline{S}$) is active LOW. The 13 index address inputs (A0-A12) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal, then a hit condition occurs (MATCH = High-Z). When at least one bit is not equal, the MATCH will go LOW signifying a miss condition. The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when $\overline{S}$ is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S}$ = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select ($\overline{S}$). When executing a write-to-compare cycle ($\overline{W}$ = LOW, $\overline{G}$ = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively.

RESET MODE

The MK48S74 allows an asynchronous reset clear whevever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65, 536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The MATCH output will go HIGH-Z t_{RSL-MH} from the falling edge of $\overline{RS}$ and all inputs will not be recongnized until t_{RSH-AV} from the rising edge of reset ($\overline{RS}$).

COMPARE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ± 5%)

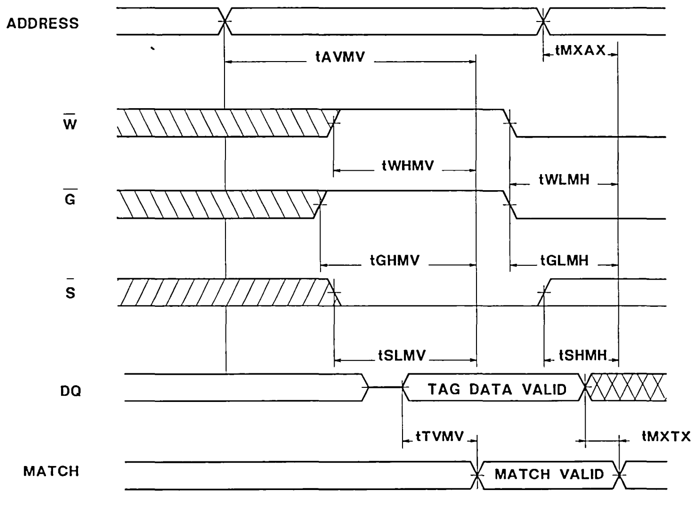
Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVMV}	t_{AMA}	Address to MATCH Valid		20		25		35	ns	3
t_{SLMV}	t_{CSM}	Chip Select to MATCH Valid		10		15		15	ns	3
t_{SHMH}	t_{CSMH}	Chip Deselect to MATCH High-Z		8		12		12	ns	3
t_{TVMV}	t_{DMA}	Tag Data to MATCH Valid		12		15		15	ns	3
t_{GHMV}	t_{OEM}	$\overline{G}$ High to MATCH Valid		10		15		15	ns	3
t_{GLMH}	t_{OEMH}	$\overline{G}$ Low to MATCH High-Z		10		12		12	ns	3
t_{WHMV}	t_{WEM}	$\overline{W}$ High to MATCH Valid		10		20		20	ns	3
t_{WLMH}	t_{WEMH}	$\overline{W}$ Low to MATCH High-Z		10		15		15	ns	3
t_{MXAX}	t_{MHA}	MATCH Hold From Address	2		2		2		ns	3
t_{MXTX}	t_{MHD}	MATCH Hold From Tag Data	0		0		0		ns	3

RESET CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-20		-25		-35		Unit	Notes
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	t_{RC}	Flash Clear Cycle Time	80		80		100		ns	
$t_{RSL\text{-}AX}$	t_{RSX}	Reset Clear ($\overline{RS}$) to Inputs Don't Care	0		0		0		ns	
$t_{RSH\text{-}AV}$	t_{RSV}	$\overline{RS}$ to Inputs Valid	5		5		5		ns	
$t_{RSL\text{-}RSH}$	t_{RSP}	Reset ($\overline{RS}$) Pulse Width	75		75		95		ns	
$t_{RSL\text{-}MH}$	t_{RSM}	Reset ($\overline{RS}$) to MATCH High-Z		15		15		15	ns	

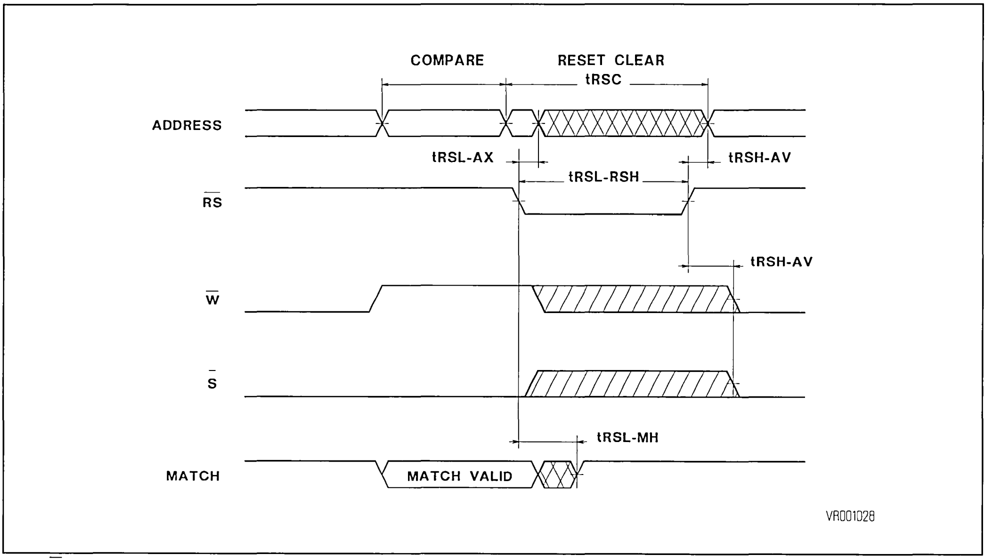
Figure 6. Match Compare Timing


ADDRESS
tAVMV
tMXAX
W̄
tWHMV
tWLMH
Ḡ
tGHMV
tGLMH
S̄
tSLMV
tSHMH
DQ
TAG DATA VALID
tTVMV
tMXTX
MATCH
MATCH VALID
VR001027

APPLICATION

The MK48S74 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaces with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally because the outputs can drive rail-to-rail into high impedance loads, the MK48S74 can also interface to 5V CMOS on all inputs and outputs. The MK48S74 provides the system designer with 64K fast static memory, a MATCH output, and a BYTEWIDE on-board comparator — all in one chip. The MK48S74 compares contents of addressed RAM locations to the current data inputs. A High-Z output on the MATCH Pin indicates that the input data and the RAM data match. Conversely, a logic zero “0" on the MATCH pin indicates at least one bit of difference between the RAM contents and the input TAG, generating in a miss. The MATCH output is constructed with an open drain arrangement. The open drain provides easy wired-OR implementation when generating a composite MATCH signal. In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of portions of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S74, and providing good hit or match ratio designs will enhance overall system performance. Because high frequency current transients will be associated with the operation of the MK48S74, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or seprarate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces of a memory board are basically unterminated, low impedance trasmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentaiton most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

Figure 7. Reset Timing



Note: $\overline{G}$ = High

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 0.3 to 6	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	– 65 to +150	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	50	mA

Note: This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.75	5.25	V	4
GND	Ground	0	0	V	4
V_{IH}	Logic 1 All Inputs	2.2	$V_{CC} + 0.3$	V	4
V_{IL}	Logic 0 All Inputs	– 0.3	0.8	V	4

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		160	mA	5
I_{IL}	Input Leakage Current	– 1	1	µA	6
I_{OL}	Output Leakage Current	– 5	5	µA	7
V_{OH}	Logic 1 Output Voltage ($I_{OUT} = -4$ mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage ($I_{OUT} = 8$ mA)		0.4	V	4
V_{OL}	Match Output LOgic 0 Voltage ($I_{OUT} = 18$ mA)		0.4	V	4

Notes :

1. Measured with load shown in Figure 8A.
2. Measured with load in Figure 8B.
3. Measured with load in Figure 8C
4. All Voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuits. $t_{AVAV} = t_{AVAV}$ (min) duty cycle 100%.
6. Input leakage current specifications are valid for all V_{IN} such that $0V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max)
7. Output leakage current specifications are valid for all V_{OUT} such that $0V < V_{OUT} < V_{CC}$, $S = V_{IH}$ and V_{CC} in valid operating range
8. Sampled, not 100% tested, outputs deselected.

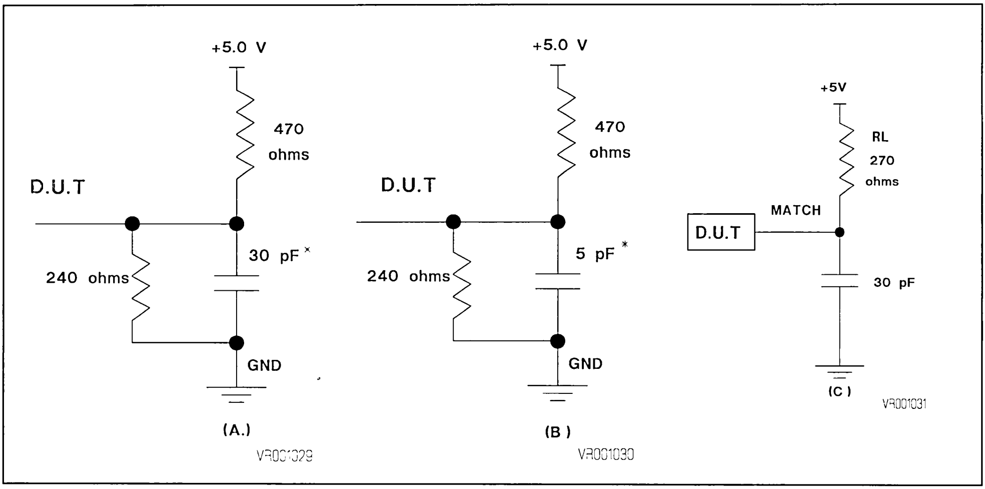
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit	Notes
C_{IN}	Capacitance on all Input pins	4	pF	8
C_{OUT}	Capacitance on Q Output pins	10	pF	8

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 8. Equivalent Output Load Circuits


+5.0 V
470 ohms
D.U.T
240 ohms
30 pF *
GND
(A.)
VR001029
+5.0 V
470 ohms
D.U.T
240 ohms
5 pF *
GND
(B)
VR001030
+5V
RL 270 ohms
MATCH
D.U.T
30 pF
(C)
VR001031

ORDERING INFORMATION

Example: MK48S74 X 20 /20

Package		Speed		Option	
N	PSDIP28	20	20ns	/20	Tape & Reel
X	PSOJ28 300mils	25	25ns		
		35	35ns		

For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

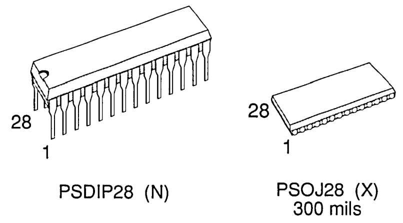
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK48S80

VERY FAST CMOS 8K x 8 CACHE TAGRAM

- 8K x 8 CMOS SRAM WITH ON BOARD COMPARATOR
- ADDRESS TO COMPARE ACCESS TIME: 15, 17, 20, 25ns
- FAST CHIP SELECT COMPARE ACCESS : 8ns
- MATCH OUTPUT WITH FAST TAG DATA TO COMPARE ACCESS OF: 12, 15ns Max
- STATIC OPERATION-NO CLOCKS OR TIMING STROBES REQUIRED
- FULL CMOS FOR LOW POWER OPERATION.
- TOTEM-POLE MATCH OUTPUT
- THREE-STATE OUTPUTS
- 28 PIN 300 MIL DIP & 28 PIN 300 MIL SOJ
- HIGH SPEED ASYNCHRONOUS RAM CLEAR


28
1
PSDIP28 (N)
28
1
PSOJ28 (X)
300 mils

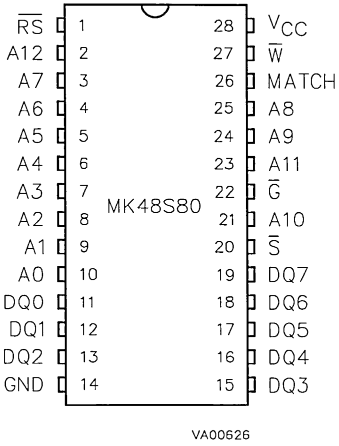
TRUTH TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	Mode	DQ	Match
X	X	X	L	Reset Clear	High-Z	High
X	H	X	H	Deselect	High-Z	High
H	L	H	H	Miss	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High
H	L	L	H	Read	Q_{OUT}	High
L	L	X	H	Write	D_{IN}	High

PIN NAMES

A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
MATCH	Comparator Output
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RS}$	Reset Flash Clear
V_{CC}, GND	5 Volts, Ground

Figure 1. Pin Connection


$\overline{RS}$ 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
28 V_{CC}
27 $\overline{W}$
26 MATCH
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{S}$
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
MK48S80
VA00626

DESCRIPTION

The MK48S80 is a 65,536 fast static cache TAGRAM™ organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMOS4 technology. The MK48S80 features fully static operation requiring no external clocks or timing strobes. The device requires a single 5V supply and is fully TLL compatible. The MK48S80 has a fast Chip Select control for high speed operation to the Match Compare valid, and device select/deselect operations. Additionally, the MK48S80 provides a Reset Clear, and MATCH compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero. The MATCH output is in a totem-pole configuration to minimize swtiching delays associated with open-drain devices. During a MATCH compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A0-A12) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

READ MODE

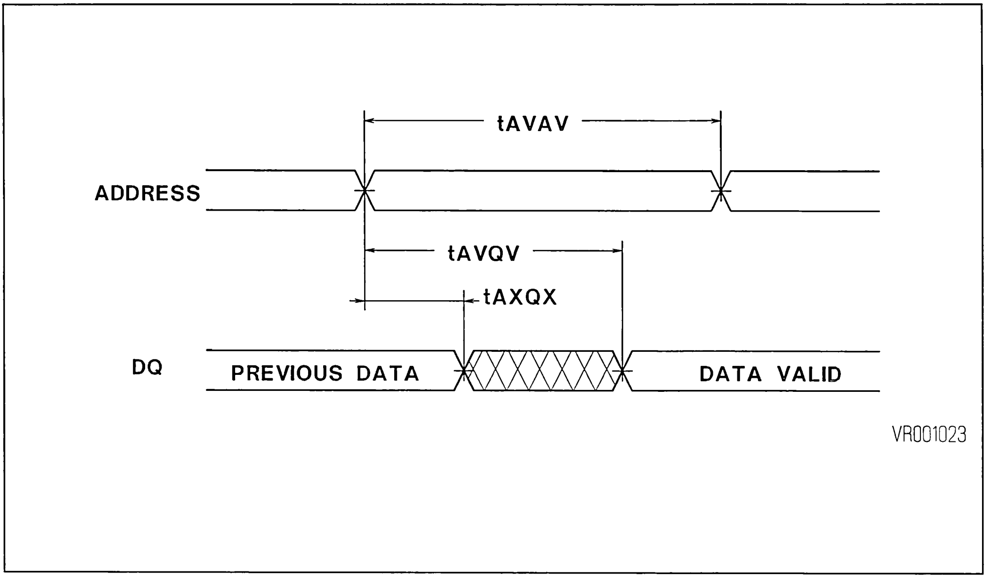
The MK48S80 is in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW, and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW, and $\overline{S}$ is LOW. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV}) rather than the addresses. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{SLQX} and t_{GLQX}, but data line will always be valid at t_{AVQV}.

READ CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

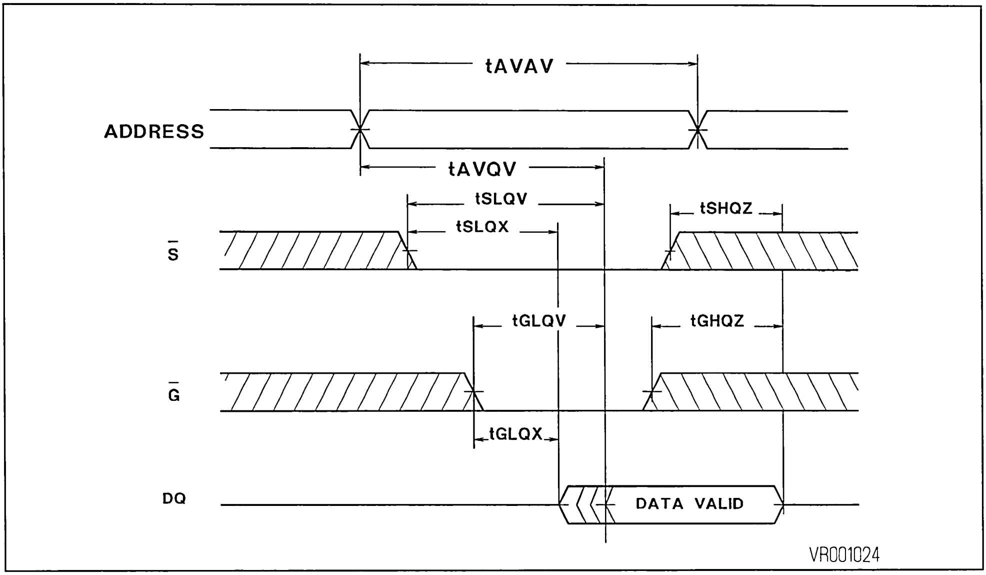
Symbol		Parameter	-15		-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{RC}	Read Cycle Time	20		20		20		25		ns	
t_{AVQV}	t_{AA}	Address Access Time		20		20		20		25	ns	1
t_{SLQV}	t_{CSA}	Chip Select Access Time		15		15		15		15	ns	
t_{GLQV}	t_{OEA}	Output Enable Access Time		10		10		10		15	ns	1
t_{SLQX}	t_{CSL}	Chip Select to Output Low-Z	0		0		0		0		ns	
t_{GLQX}	t_{OEL}	Output Enable to Low-Z	0		0		0		0		ns	
t_{SHQZ}	t_{CSZ}	Chip Select to High-Z		9		9		9		9	ns	
t_{GHQZ}	t_{OEZ}	Output Enable to High-Z		8		8		8		8	ns	2
t_{AXQX}	t_{OH}	Output Hold From Address Change	3		3		3		3		ns	1

Figure 2. Read Timing No. 1 (Address Access)


tAVAV
ADDRESS
tAVQV
tAXQX
DQ
PREVIOUS DATA
DATA VALID
VR001023

Note: Chip Select and Output Enable are presumed Valid, $\overline{W} = V_{IH}$

Figure 3. Read Timing No. 2 ($W = V_{IH}$)


tAVAV
ADDRESS
tAVQV
tSLQV
tSLQX
tSHQZ
S
tGLQV
tGHQZ
G
tGLQX
DQ
DATA VALID
VR001024

WRITE MODE

The MK48S80 is in the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL}, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$. If the output is enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

WRITE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
($0\ °C \le T_A \le +70\ °C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-15		-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{WC}	Write Cycle Time	20		20		20		25		ns	
t_{AVWL}	t_{AS}	Address Set-up to Write Enable Low	0		0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up to Chip Select	0		0		0		0		ns	
t_{AVWH}	t_{AW}	Address Valid to End of Write	15		15		15		20		ns	
t_{WLWH}	t_{WEW}	Write Pulse Width	15		15		15		20		ns	
t_{WHAX}	t_{AH}	Address Hold Time After End of Write	0		0		0		0		ns	
t_{SLSH}	t_{CSW}	Chip Select to End of Write	15		15		15		20		ns	
t_{SHAX}	t_{WR}	Write Recovery Time to Chip Select	0		0		0		0		ns	
t_{DVWH}	t_{DW}	Data Valid to End of Write	10		10		10		13		ns	
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WHQX}	t_{WEL}	Write High to Output Low-Z (Active)	0		0		0		0		ns	2
t_{WLQZ}	t_{WEZ}	Write Enable to Output High-Z		5		5		5		5	ns	2

Figure 4. Writing Timing No. 1 (Write Control)

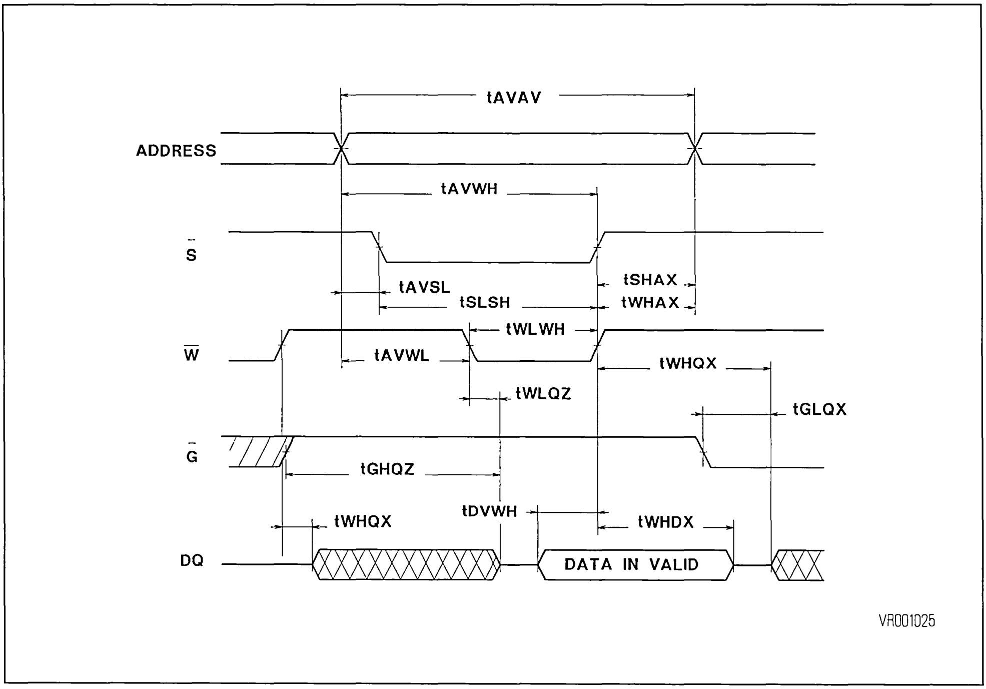
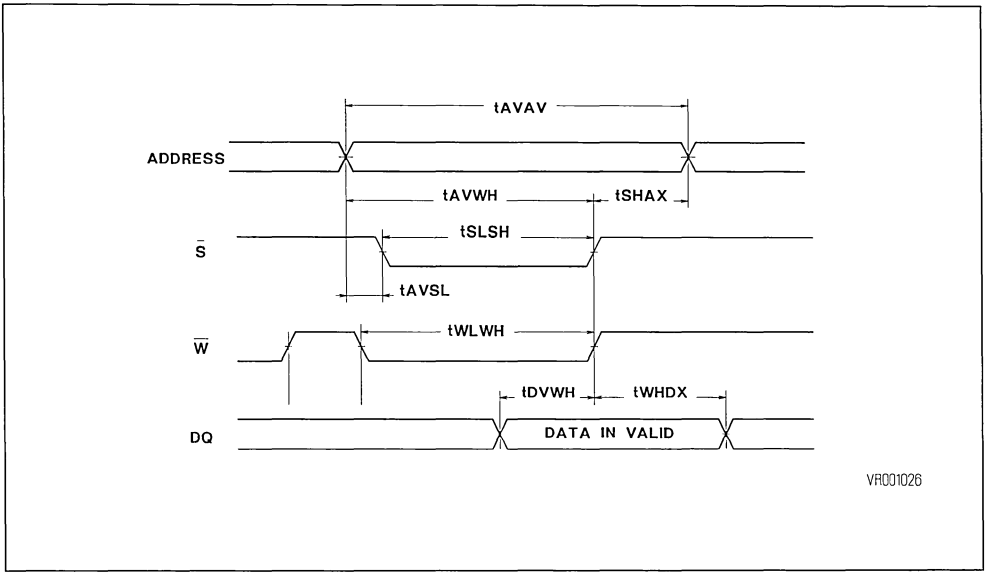

tAVAV
ADDRESS
tAVWH
S
tAVSL
tSLSH
tSHAX
tWHAX
W
tWLWH
tAVWL
tWHQX
tWLQZ
tGLQX
G
tGHQZ
tWHQX
tDVWH
tWHDX
DQ
DATA IN VALID
VR001025

Figure 5. Writing Timing No. 2 (Chip Select Control)


tAVAV
ADDRESS
tAVWH
tSHAX
tSLSH
S
tAVSL
W
tWLWH
tDVWH
tWHDX
DQ
DATA IN VALID
VR001026

Note: $\overline{G} = V_{IH}$

COMPARE MODE

The MK48S80 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided Chip Select ($\overline{S}$) is active LOW. The 13 index address inputs (A0-A12) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal, then a hit condition occurs (MATCH = HIGH). When at least one bit is not equal, then MATCH will go LOW signifying a miss condition. The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when S is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S}$ = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select ($\overline{S}$). When executing a write-to-compare cycle ($\overline{W}$ = LOW, $\overline{G}$ = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively.

RESET MODE

The MK48S80 allows an asynchronous reset clear whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65,536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The state of the outputs is determined by the control logic input pins $\overline{S}$, $\overline{W}$, and $\overline{G}$ during reset (see Truth Table). The MATCH output will go HIGH t_{RSL-MH} from the falling edge of $\overline{RS}$, and all inputs will not be recognized unit t_{RSH-AV} from the rising edge of reset ($\overline{RS}$).

APPLICATION

The MK48S80 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK48S80 can also interface to 5V CMOS on all inputs and outputs. The MK48S80 provides the system designer with 64K fast static memory, a MATCH out-put, and a BYTEWIDE on-board comparator, all in one chip. The MK48S80 compares the contents of addressed RAM locations to the current

COMPARE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

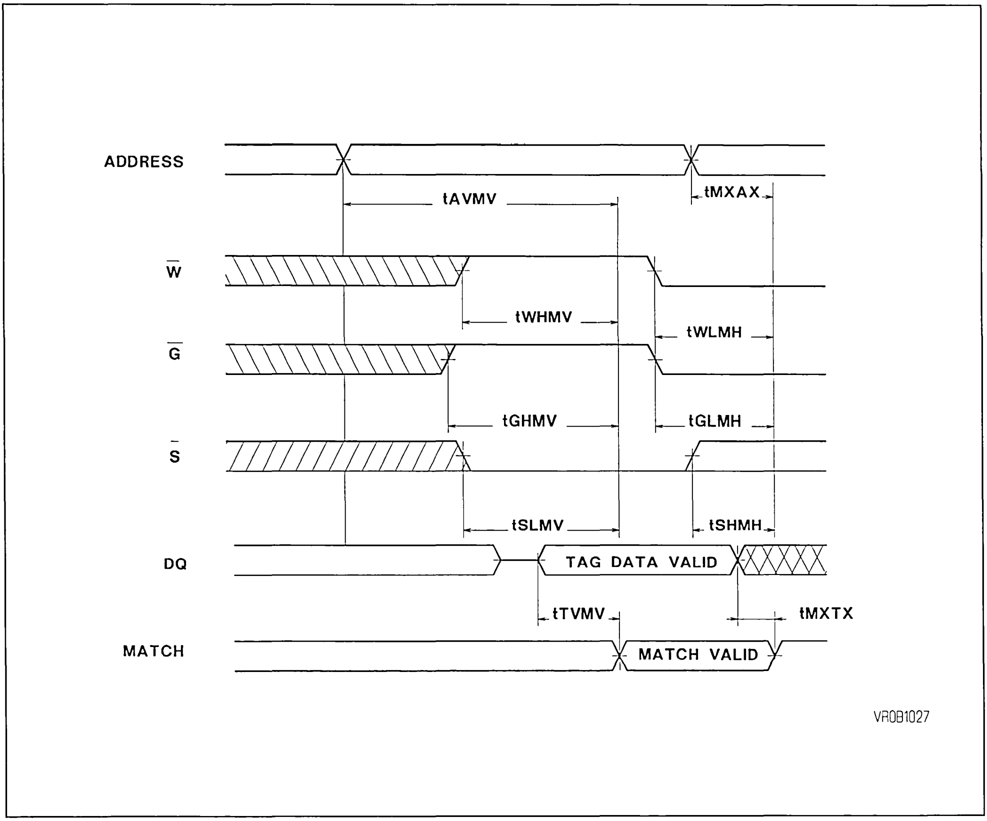
Symbol		Parameter	-15		-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVMV}	t_{AMA}	Address to MATCH Valid		15		17		20		25	ns	1
t_{SLMV}	t_{CSM}	Chip Select to MATCH Valid		8		8		10		15	ns	1
t_{SHMH}	t_{CSMH}	Chip Deselect to MATCH High		5		5		8		12	ns	1
t_{TVMV}	t_{DMA}	Tag Data to MATCH Valid		12		12		12		15	ns	1
t_{GHMV}	t_{OEM}	$\overline{G}$ High to MATCH Valid		10		10		10		15	ns	1
t_{GLMH}	t_{OEMH}	$\overline{G}$ Low to MATCH High		10		10		10		12	ns	1
t_{WHMV}	t_{WEM}	$\overline{W}$ High to MATCH Valid		10		10		10		20	ns	1
t_{WLMH}	t_{WEMH}	$\overline{W}$ Low to MATCH High		10		10		10		15	ns	1
t_{MXAX}	t_{MHA}	MATCH Hold From Address	1		1		1		1		ns	1
t_{MXTX}	t_{MHD}	MATCH Hold From Tag Data	0		0		0		0		ns	1

RESET CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

(0 °C ≤ T_A ≤ +70 °C; V_{CC} = 5V ± 5%)

Symbol		Parameter	-15		-17		-20		-25		Unit
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RSC}	t_{RC}	Flash Clear Cycle Time	80		80		80		80		ns
t_{RSL-AX}	t_{RSX}	Reset Clear (RS) to Inputs Don't Care	0		0		0		0		ns
t_{RSH-AV}	t_{RSV}	$\overline{RS}$ to Inputs Valid	5		5		5		5		ns
$t_{RSL-RSH}$	t_{RSP}	Reset ($\overline{RS}$) Pulse Width	75		75		75		75		ns
t_{RSL-MH}	t_{RSM}	Reset ($\overline{RS}$) to MATCH High		15		15		15		15	ns

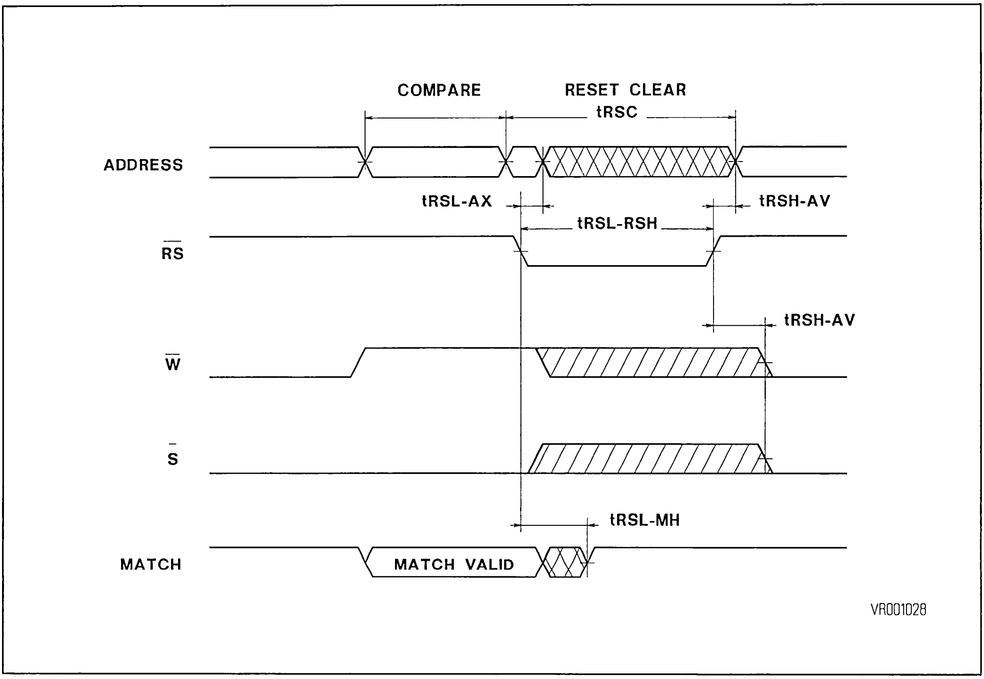
Figure 6. Match Compare Timing


ADDRESS
tAVMV
tMXAX
W
tWHMV
tWLMH
G
tGHMV
tGLMH
S
tSLMV
tSHMH
DQ
TAG DATA VALID
tTVMV
tMXTX
MATCH
MATCH VALID
VR0B1027

data inputs. A logic one "1" output on the MATCH pin indicates that the input data and the RAM data match. Conversely, a logic zero "0" on the MATCH pin indicates at least one bit of difference between the RAM contents and the input TAG, generating a miss.

The MATCH output is constructed with a totem-pole arrangement. The totem-pole configuration allows the designer to minimize switching delays and noise problems associated with open-drain devices. In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of portions of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S80, and providing good hit or match ratio designs will enhance overall system performance. Because high frequency current transients will be associated with the operation of the MK48S80, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces of a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

Figure 7. Reset Timing



Note: $\overline{G}$ = High

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.3 to 6	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	50	mA

Note: This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0\ °C \le T_A \le +70\ °C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.75	5.25	V	3
GND	Ground	0	0	V	3
V_{IH}	Logic 1 All Inputs	2.2	$V_{CC} + 0.3$	V	3
V_{IL}	Logic 0 All Inputs	–0.3	0.8	V	3

DC ELECTRICAL CHARACTERISTICS ($0\ °C \le T_A \le +70\ °C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		160	mA	4
I_{IL}	Input Leakage Current	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	6
V_{OH}	Logic 1 Output Voltage ($I_{OUT} = -4$ mA)	2.4		µA	3
V_{OL}	Logic 0 Output Voltage ($I_{OUT} = 8$ mA)		0.4	V	3

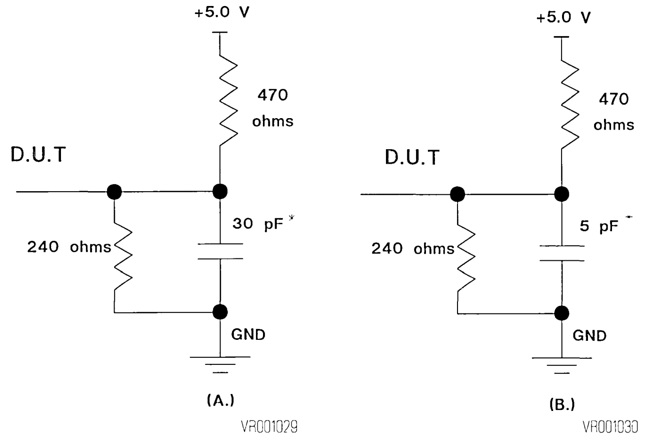
CAPACITANCE ($T_A = 25\ °C$, f = 1MHz)

Symbol	Parameter	Max.	Unit	Notes
C_{IN}	Capacitance on all Input pins	4	pF	7
C_{OUT}	Capacitance on Q Output pins	10	pF	7

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 8. Equivalent Output Load Circuits



(A.)

(B.)

Notes :

1. Measured with load shown in Figure 8A.
2. Measured with load shown in Figure 8B.
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. $t_{AVAV} = t_{AVAV}$ (min) duty cycle 100%.
5. Input leakage current specifications are valid for all V_{IN} such that $0\ V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
6. Output leakage current specifications are valid for all V_{OUT} such that $0\ V < V_{OUT} < V_{CC}$, $\overline{S} = V_{IH}$ and V_{CC} in valid operating range.
7. Sampled, not 100% tested.

ORDERING INFORMATION

Example: MK48S80 X 17 /20

Package		Speed		Option	
N	PSDIP28	15	15ns	/20	Tape & Reel
X	PSOJ28 300 mils	17	17ns		
		20	20ns		
		25	25ns		

For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

SGS-THOMSON
MICROELECTRONICS

MK45180

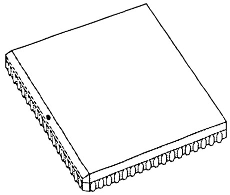
VERY FAST CMOS 4K x 10 CACHE SnoopTAG

ADVANCE DATA

- 4K x 10 BiPORT SRAM WITH LOCAL AND SNOOP PORT COMPARATORS
- ADDRESS TO MATCH ACCESS : 17ns
- PORT ENABLE TO MATCH ACCESS : 8ns
- COMPREHENDS SNOOP CACHE COHERENCY INVALIDATION
- ON-CHIP PARITY GENERATOR / CHECKERS
- MASTER / SLAVE CONFIGURATION FOR WIDTH EXPANSION
- RESET / FLASH CLEAR FUNCTION
- STATUS BIT OPTION FOR BOTH PORTS
- APPLICATION: HIGH-SPEED SINGLE AND MULTI-PROCESSOR CACHE SUBSYSTEM

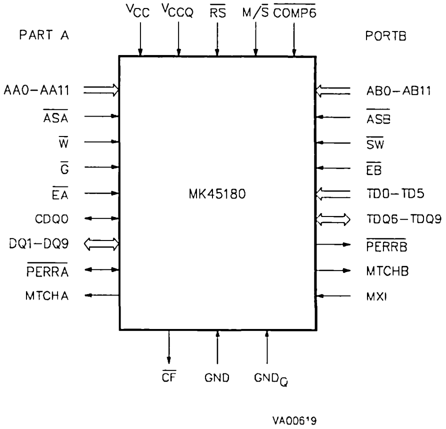
CONTROL & STATUS I/O

$\overline{W}$	Port A Write Enable
$\overline{G}$	Port A Output Enable
$\overline{EA}$	Port A Select Enable
$\overline{EB}$	Port B Select Enable
$\overline{RS}$	Reset (Clear)
$\overline{COMP6}$	Compare 6 Enable
$M/\overline{S}$	Snoop Coherency Select as Master/Slave
$\overline{SW}$	Port B Snoop Write Enable
$\overline{CF}$	Collision Flag
$\overline{ASA}$	Port A Address Strobe Input
$\overline{ASB}$	Port B Address Strobe Input
MTCHA	Port A Compare MATCH Output
MTCHB	Port B Compare MATCH Output
$\overline{PERRA}$	Port A Parity Select/ Parity Error Output
$\overline{PERRB}$	Port B Parity Error Output
$\overline{MXI}$	Port B Match Width Expansion
V_{CC},GND	5 Volts, GND



PLCC68 (Q)

Figure 1. Logic Diagram


V_{CC}
V_{CCQ}
$\overline{RS}$
$M/\overline{S}$
$\overline{COMP6}$
PART A
PORTB
AA0–AA11
$\overline{ASA}$
$\overline{W}$
$\overline{G}$
$\overline{EA}$
CDQ0
DQ1–DQ9
$\overline{PERRA}$
MTCHA
MK45180
AB0–AB11
$\overline{ASB}$
$\overline{SW}$
$\overline{EB}$
TD0–TD5
TDQ6–TDQ9
$\overline{PERRB}$
MTCHB
MXI
$\overline{CF}$
GND
GND_Q
VA00619

ADDRESS & DATA I/O

AA0 - AA11	Port A (Local) Index Inputs
AB0 - AB11	Port B (Snoop) Index Inputs
CDQ0	VALID Bit Designator; Clearable RAM I/O
DQ1 - DQ5	Port A Data - Tag I/O
DQ6 - DQ9	Port A Data - Tag I/O / Status Bit I/O
TD0 - TD5	Snoop Tag Data Inputs
TDQ6 - TDQ9	Snoop Tag Data Inputs / Status Bit Outputs

February 1992

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

DEVICE DESCRIPTION AND FEATURES

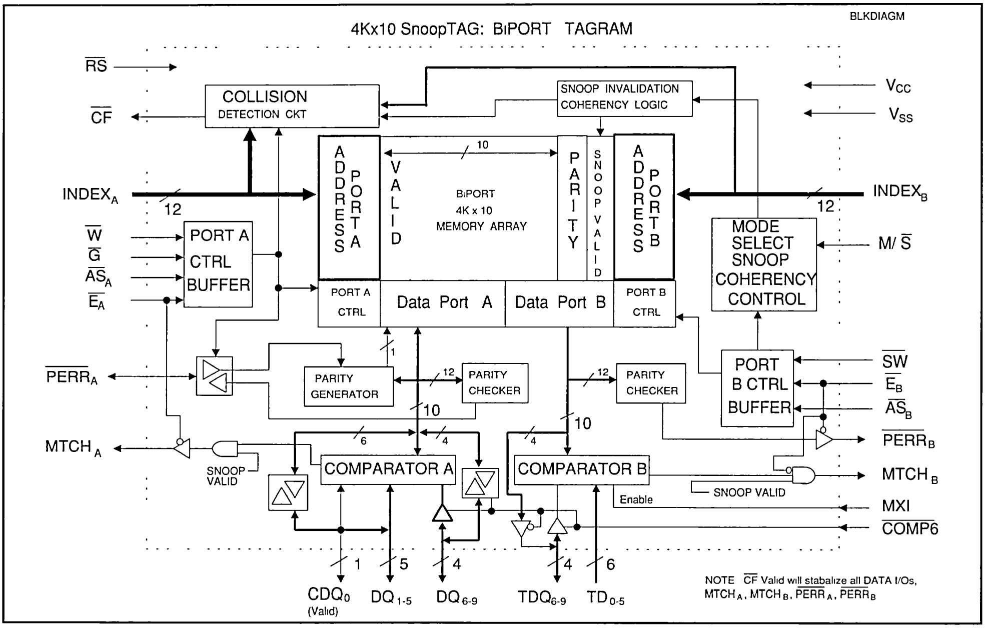
The MK45180 is a dual-port cache tag directory, SnoopTAG™, targeted for high-speed applications requiring fast tag directory access comparisons, as well as an efficient mechanism for ensuring coherency between local cache storage and system main memory. The device architecture is designed around a 49,152-bit BiPORT™ CMOS Static RAM, as 4,096 words x12 bits (including parity and snoop valid bits). It employs SGS-THOMSON advanced HCMOS process technology.

This new member of the SGS-THOMSON cache TAGRAM™ family offers separate and asynchronous ports for Local TAGRAM accesses and bus watching or "snooping" during system write/read cycles. The Local port (Port A) operates much like the industry standard MK41S80 4K x 4 TAGRAM, but features a 12-bit address index with a 10-bit Data/Tag field. Port A can write, read, or compare the SnoopTAG's contents. The Bus Watch or Snoop port (Port B) also has a 12-bit index address with a 10-bit tag data (TD0-TD5 and TDQ6-TDQ9) field, and indicates a hit each time the system bus addresses a location contained by the local cache directory. Port B does not perform typical SRAM write or read operations, but always snoops and compares system read or write cycles to detect a hit or miss condition.

The MK45180 offers a three state totem-pole MTCHA output for fast match access, and data off time. MTCHA is active only during valid compare cycles. The MTCHB output offers a totem-pole arrangement designed for fast expansion times. The snoop port (Port B) includes a Match Expansion Input (MXI) for width expansion without additional logic or cycle time penalties. Both MATCH outputs (MTCHA and MTCHB) are high for a cache "hit", and low for a cache "miss" during bus compare cycles. For easy match output control, both match outputs offer a fast access time from their respective port select enables.

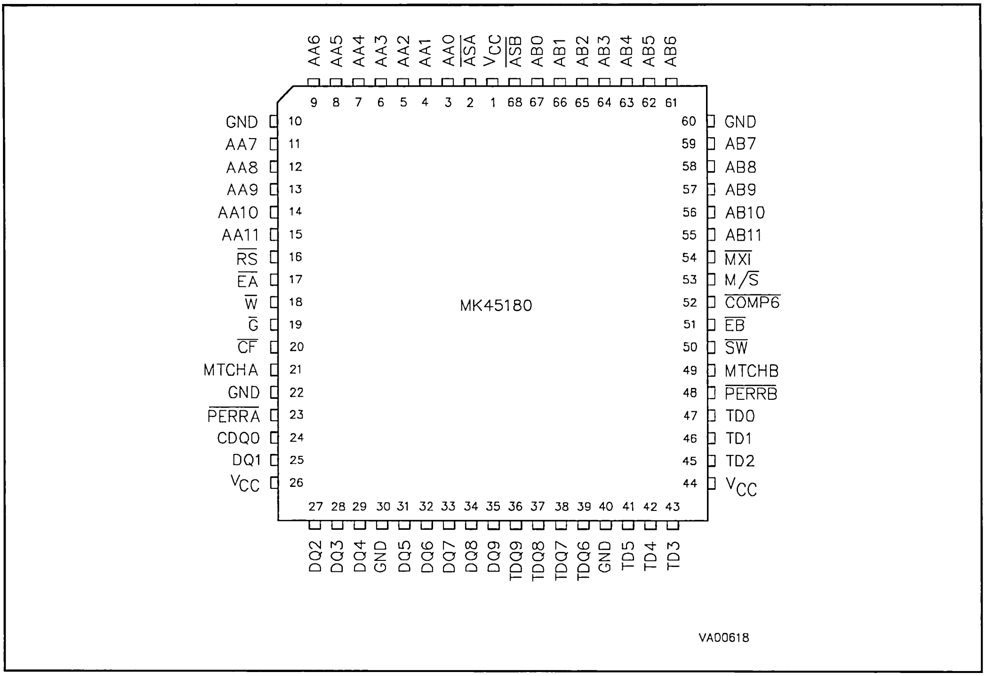
The MK45180 offers two separate enables, $\overline{\text{EA}}$ (Port A Select Enable) and $\overline{\text{EB}}$ (Port B Select Enable), to allow for independent port selection in cache designs comprised of multiple SnoopTAG devices organized for depth expansion or set-associativity. This feature reduces the device or chip selection complexity for system designers since each port can be activated independently. Furthermore, the device offers a parity error output ($\overline{\text{PERRA}}$ and $\overline{\text{PERRB}}$) for each port. Parity error flags will assert a logic zero when an error is detected by the internal parity checker for Port A or Port B compare cycles, and for Port A read cycles.

SnoopTAG BLOCK DIAGRAM


BLKDIAGM
4Kx10 SnoopTAG: BiPORT TAGRAM
RS
CF
COLLISION DETECTION CKT
SNOOP INVALIDATION COHERENCY LOGIC
Vcc
Vss
INDEXA
12
W
G
ASA
EA
PORT A CTRL BUFFER
ADDRESS PORT A
VALID
10
BiPORT 4K x 10 MEMORY ARRAY
PARITY
SNOOP VALID
ADDRESS PORT B
INDEXB
12
MODE SELECT SNOOP COHERENCY CONTROL
M/S
PORT A CTRL
Data Port A
Data Port B
PORT B CTRL
1
PERRA
PARITY GENERATOR
12
PARITY CHECKER
12
PARITY CHECKER
PORT B CTRL BUFFER
SW
EB
ASB
PERRB
10
10
MTCH A
6
4
4
SNOOP VALID
COMPARATOR A
COMPARATOR B
MTCH B
SNOOP VALID
Enable
MXI
COMP6
1
5
4
4
6
CDQ0 (Valid)
DQ1-5
DQ6-9
TDQ6-9
TD0-5

NOTE CF Valid will stabalize all DATA I/Os, MTCHA, MTCHB, PERRA, PERRB

Figure 2 : Pin Connection


AA6 9
AA5 8
AA4 7
AA3 6
AA2 5
AA1 4
AA0 3
$\overline{ASA}$ 2
VCC 1
$\overline{ASB}$ 68
AB0 67
AB1 66
AB2 65
AB3 64
AB4 63
AB5 62
AB6 61
GND 10
AA7 11
AA8 12
AA9 13
AA10 14
AA11 15
$\overline{RS}$ 16
$\overline{EA}$ 17
$\overline{W}$ 18
$\overline{G}$ 19
$\overline{CF}$ 20
MTCHA 21
GND 22
$\overline{PERRA}$ 23
CDQ0 24
DQ1 25
VCC 26
DQ2 27
DQ3 28
DQ4 29
GND 30
DQ5 31
DQ6 32
DQ7 33
DQ8 34
DQ9 35
TDQ9 36
TDQ8 37
TDQ7 38
TDQ6 39
GND 40
TD5 41
TD4 42
TD3 43
60 GND
59 AB7
58 AB8
57 AB9
56 AB10
55 AB11
54 $\overline{MXI}$
53 M/$\overline{S}$
52 $\overline{COMP6}$
51 $\overline{EB}$
50 $\overline{SW}$
49 MTCHB
48 $\overline{PERRB}$
47 TD0
46 TD1
45 TD2
44 VCC
MK45180
VA00618

MODE CONFIGURATION

Master / Slave Mode Option

Two options are incorporated in the device for bus watching and width expansion. The mode configuration input (M/$\overline{S}$) configures the device as either a Master or Slave. The M/$\overline{S}$ input is considered as a static input, and should be tied high for a Master, or tied low for a Slave. The Master will execute automatic snoop port address invalidation, and determine an index address match for collision detection. The Slave device (M/$\overline{S}$ = low) observes local and snoop port cycles, and indicates a hit or miss condition ; however, the automatic snoop invalidation and collision detection schemes are disabled. (Refer to the Coherency Mode Select State Table). If the device is configured as the Master where M/$\overline{S}$ = high, then the indicated entry in the cache will be invalidated during snoop write-hit cycles ($\overline{SW}$ = low). During system snoop-read cycles ($\overline{SW}$ = high), a hit or miss is indicated by the MTCH$_B$ output, but the SnoopTAG cache directory is not affected.

A Master/Slave combination is employed for tag data field width expansion (see the "MATCH WIDTH EXPANSION" discussion and figures). Only the Master SnoopTAG stores the Valid Bit, and parity errors ($\overline{PERRA}$, $\overline{PERRB}$) are detected and ANDed together from both the Master and Slave devices. Parity becomes valid for each RAM location that is written into the SnoopTAG devices. Thus, a complete cache fill constitutes valid parity for the entire SnoopTAG master/slave combination. It should be noted that the Master ignores parity errors after reset. $\overline{PERRA}$, $\overline{PERRB}$ will remain true on subsequent compare cycles after a reset operation occurs. This is because with the suggested master/slave combination (see Figure 3), a reset operation only affects the Master SnoopTAG, and the Slave device is not disturbed. Remembering that the Master ignores parity errors for each RAM location not yet written, a cache flush operation using RESET ($\overline{RS}$) for flash clear, will invalidate all entries generating a miss on subsequent compare cycles without generating undesired system parity errors.

Status Bit Mode Option

The $\overline{\text{COMP6}}$ input is a static input that is common to both ports. It configures the comparator on both ports (Port A and B) to compare either 6 or 10 tag data bits from the external inputs with the internal RAM to determine a match. If the $\overline{\text{COMP6}}$ input is tied high, then a tag field of 10 bits is provided, and the SnoopTAG compares all 10 inputs on either port (CDQ0, DQ1-DQ9 or TD0-TD5 and TDQ6-TDQ9) with internal RAM during port compare cycles. If $\overline{\text{COMP6}}$ is tied low, 4 bits are truncated from each port comparator resulting in a 6-bit tag, and providing four (4) status bit outputs during any valid compare cycle on either port. In summary, each port will indicate a hit or miss condition during a compare cycle in addition to providing four cache subsystem status bits simultaneously. (Note from the Block Diagram that the $\overline{\text{COMP6}}$ input configures each port with a 6-bit tag field to the comparator, and 4 status bit outputs. $\overline{\text{COMP6}}$ makes no reference to the Master/Slave selection.)

Again, all data along with any status bits are written to the SnoopTAG during port A write operations. The status bits can be written and read from port A, and are valid during Port A compare cycles. Also, the status bits are read valid during each Port B snoop cycle.

BUS WATCH PROTOCOL (SNOOPING)

The Bus Watching or Snoop port observes the $\overline{\text{SW}}$ input (Snoop Write Enable) and uses the 12-bit Snoop index and 10-bit Tag-Data (TD0-TD5 and TDQ6-TDQ9) to determine whether a system bus write cycle affects data in the *local cache*. This operation can be asynchronous to the local cache execution. If the addressed location resides in the MK45180 TAGRAM directory (hit condition), then that location will be invalidated (provided M/$\overline{\text{S}}$ = high) since it is no longer coherent with main memory.

The MK45180 SnoopTAG incorporates on-board algorithms to aid the system designer in snoop hit detection and system memory coherency. Only one condition exists where the cache tag directory will be invalidated by the snoop port during system write cycles. This is shown in the Port B Master/Slave Truth Table. It should be noted that each write/read cycle from the snoop port (Port B) is only a compare operation to determine a hit or miss condition. In other words, each snoop port operation simply checks the SnoopTAG directory for an address and tag match. (Snoop cycles allow the 4 status bits to be read when $\overline{\text{COMP6}}$ is low.) The snoop port (Port B) can only invalidate cache tag locations when a compare-hit occurs during a snoop write cycle, provided the Master configuration is selected to enable this protocol. Port A, on the other hand, can write, read, and compare all index address locations in the SnoopTAG directory regardless of its master/slave configuration (refer to the Port A Master/Slave Truth Table). The BiPORT operations for the device are discussed in more detail in the following paragraphs.

PARITY VERIFICATION

In addition to cache coherency and device configuration inputs, the MK45180 incorporates parity verification. Parity diagnostic testing allows invalid parity to be forced into the memory array via Port A through the $\overline{\text{PERRA}}$ pin by forcing the pin low during normal write cycles. (During Port A write cycles the $\overline{\text{PERRA}}$ pin is a parity select input.) A parity diagnostic write cycle generates false parity by holding $\overline{\text{PERRA}}$ low for the duration of the write cycle. When this address location is checked by the parity checker, using an even parity scheme, a parity error results and $\overline{\text{PERRA}}$ will be asserted low. The same location will also generate a parity error on Port B by asserting $\overline{\text{PERRB}}$ low. To generate and store true parity, the $\overline{\text{PERRA}}$ input pin must be held high for the duration of a Port A write cycle.

Normal write operations assume a pull-up load (high level) on the $\overline{\text{PERRA}}$ pin for writing true parity, however, this input can be forced low at t_{WLPZ} during parity diagnostic write cycles. It must be noted that the $\overline{\text{PERRA}}$ input during write cycles is not the actual parity data, but acts as a select that self generates and stores either true or false parity (false = error). During parity diagnostic write cycles where parity is expected to be written false, the $\overline{\text{PERRA}}$ input must maintain a stable V_{IL} input (t_{PLWH}) to the end of the write pulse ($\overline{\text{W}}$ goes high), and be held stable t_{WHPH} after the end of write, but not to exceed t_{WHPX} ($\overline{\text{PERRA}}$ low-Z) to avoid bus contention. Due to the "on and off" time of the bus, the parity diagnostic write cycle requires an extended cycle. Refer to the Parity Diagnostic Write Timing AC specifications.

The $\overline{\text{PERRA}}$ pin acts as an output during Port A read and compare cycles. This output will become active t_{WHPX} from the end of write, and will be valid t_{AVPV} from a stable address (read or compare cycle), or t_{WHPV} from $\overline{\text{W}}$ going high with a stable address. $\overline{\text{PERRA}}$ is asserted low whenever a parity error is detected during a Port A read or compare cycle. Port B checks the tag field inputs plus parity during snoop cycles. The parity bit is not internally generated from Port B, but both ports check valid parity. When a parity error is detected during Port B snoop cycles, the $\overline{\text{PERRB}}$ output is asserted low.

TYPICAL TAG WRITE OPERATIONS

During write cycles, the Port A address index must remain stable with Data Inputs (CDQ0 and DQ1-DQ9) presented valid for a duration of t_{DVWH}, and remaining valid for t_{WHDX} after $\overline{W}$ goes high. Since bus contention can exist when executing write cycles with $\overline{G}$ asserted low, write cycles with $\overline{G}$ held high are recommended. Otherwise, Data In can be presented valid at t_{WLQZ} from $\overline{W}$ low. Typical write cycles assume a constant high logic level load on the $\overline{PERRA}$ pin to generate and store true parity in the SnoopTAG.

AUTOMATIC INVALIDATION MODE

Although the external valid bit (V) is indicated from the Master MK45180 by the CDQ_0 pin, the MK45180 Master also uses an internal **Snoop Valid** (SV) bit for each cache SnoopTAG entry. Both valid bits must be equal to a logic one (V = SV = 1) to indicate a hit condition on either port. During Port A cache tag write operations, both bits are set to a logic one. When a snoop hit occurs on Port B during system write cycles ($\overline{SW}$ = low), the Snoop Valid (SV) bit is cleared to a logic zero, thus providing an invalid indication for that entry. During compare cycles the SV bit is passed into either port's comparator logic. This provides easy asynchronous BiPORT operations, as well as ensuring fast snoop write-hit invalidation. Both the $\overline{MTCHB}$ and $\overline{PERRB}$ outputs will remain stable during a snoop invalidation.

As stated previously, snoop write cycles during a hit condition will invalidate the current Port B index address in the SnoopTAG array by clearing the snoop valid (SV) bit. A bus snoop hit during system write operations will invalidate the snoop valid bit in the SnoopTAG array only at that specific index address, such that SV=0 (if Master Configuration is selected). This forces a miss and cache fetch-update when the local port accesses the same location at a later time (thus the new data tag is fetched and stored by local cache). This cache coherency method eliminates the possibility of invalid data being accessed by the local port.

Since CDQ_0 is designated as the external **valid bit** for all cache tag locations, the CDQ0 and TD0 inputs can be tied high (+V_{CC}) for using external valid (V) bit indication. A RESET is considered a Flash Clear operation where all of the RAM entries for the CDQ0 output are cleared to a logic zero. An asynchronous clear operation is performed by pulsing $\overline{RS}$ low for a minimum duration of t_{RLRH}. Inputs are recognized valid 10ns after $\overline{RS}$ goes high.

BiPORT COLLISION DETECTION

As can be noted in the Collision Detection Logic Table, the $\overline{CF}$ signal is asserted low whenever: (1) the index address inputs on both ports are equal (index A=B) with both address strobes active low ($\overline{ASA}$ = $\overline{ASB}$ = low), (2) both ports must be enabled, and (3) the port operations (write/compare/read) on Port A and Port B warrant a collision.

First, address collision on the MK45180 SnoopTAG assumes that the address is valid coincident with or prior to the address strobe being asserted. Therefore, the MK45180 detects collision where the address strobe inputs satisfy the required minimum set-up time of $t_{ASL\text{-}ASH}$ for collision detection. This ensures a valid address cycle. The Collision Flag ($\overline{CF}$) will be asserted for a minimum of $t_{ASH\text{-}CFH}$ after either address strobe goes high. **Address strobes cannot be tied low, as this would allow erratic collisions**. Second, collision is considered valid when both ports are enabled for a minimum set-up time of $t_{E1L\text{-}E2H}$. The $\overline{CF}$ signal will remain low for a minimum of $t_{EH\text{-}CFH}$ after either port is disabled during collision. Finally, collision can be detected when either port enters a write operation, thus collision is considered from the $\overline{W}$ and $\overline{SW}$ inputs. Collision can end whenever one port completes its current write operation or changes addresses.

If the $\overline{CF}$ signal is not asserted ($\overline{CF}$ remains high), then collision is not detected, and both ports have completed their particular operation as expected. If address collision exists from address strobe for less than or equal to 3ns, collision will not be detected for that cycle, thus $\overline{CF}$ will remain high. This avoids undesired pulses from the Collision Flag when address collision is too short to have any affect on port operations.

COLLISION : PORT OPERATIONS

The MK45180 provides the user with a Collision Detection Flag ($\overline{CF}$) to indicate when an address collision occurs during BiPORT operations while the device is in MASTER mode. Collision in itself does not provide exclusive port priority or arbitration as both port operations will be completed. When collision occurs on a snoop write-cycle, the snoop invalidation protocol will supersede a write cycle on the local port. The invalidation is not a direct result of the collision, but is a result of the device's snoop write-hit algorithm provided the following conditions are met.

To ensure invalidation, the normal Port B snoop write input ($\overline{SW}$) set-up and hold times must be met where the $\overline{SW}$ pulse is a minimum of t_{SWLSWH}, (see Figures 10 and 12). In this scenario, the entry is written invalid (SV = 0). For a successful operation, it is expected that the minimum times are met, and that $\overline{W}$ does not extend beyond the collision time ($\overline{CF}$ going high). The snoop invalidation operation is guaranteed to invalidate the entry during collision at the specified index address. However, the true parity indicator can be corrupted on collision during a “WRITEA - WRITEB Wins” situation. Care must be taken so Port A completes the Write either before of after $\overline{\text{CF}}$ VALID to insure proper parity bit generation. This will avoid potential parity errors in future Read or Compare cycles to the previously collided addresses.

By now it may be obvious that Port A write operations to the Snoop Valid (SV) bit are suspended during a collision with a simultaneous snoop write cycle. However, if the Port A write enable ($\overline{\text{W}}$) extends a minimum of $t_{SWH\text{-}WH}$ at the end of the snoop write-hit cycle, then the entry is considered written as valid (SV = 1). In this case, the Port B operation is **displaced** by the Port A write cycle (see Figure 20). Even though a local write can displace a snoop write-hit as just described, it is not considered to be the normal application. Typical applications are expected to allow the snoop invalidation operation to predominate.

STABLE OUTPUTS DURING COLLISION

Coincident write operations from one port at an identical address being accessed by the other port can cause data changes that result in unstable outputs on each port during collision. In this instance, it is necessary to ensure that the outputs remain stable. Therefore, whenever collision is detected both port match outputs, parity error flags, and data outputs are held stable for the duration of collision. Should either port extend its cycle beyond the duration of collision ($\overline{\text{CF}}$ goes high), then the match outputs, parity error flags or data outputs can begin switching logic states within $t_{CFH\text{-}QX}$. If the latter case is not desirable, then the user must latch the output condition for the desired time when collision is detected.

MATCH WIDTH EXPANSION

The local port (Port A) provides a three state MTCHA output. The MTCHA outputs for the master/slave configuration can be ANDed together for tag data width expansion. With the Master and Slave pair combination, the local port can cache up to 31 bits, plus the external valid bit, for a total of 32 bits (12-bit index and 20-bit tag). Operation cycle times are equal to the single device with this combination.

For the snoop port (Port B) interface, the Match Expansion Input (MXI) allows MATCH width Expansion without additional logic. However, the MXI input employs an expansion delay of (t_{MXDY}) to the total match compare access time (t_{AVMV}), but is within a single cycle time. Figure 3 shows a block diagram for implementing a width expansion application. Device configuration selection inputs should be set for the Master and Slave pair combination. This combination allows a 4K (12-bit) address index with a 20-bit tag field (including the valid bit), thus caching a total of 32 bits. The MTCHB output is taken from the Master device. Operation cycle times are equal to the single device with this combination.

Port control inputs and index address inputs can be connected in parallel for each device pair. The parity error ($\overline{\text{PERRA}}$ and $\overline{\text{PERRB}}$) for each Snoop-TAG must be ANDed externally. The MXI and $\overline{\text{RS}}$ inputs for the SLAVE device must be tied to +V_{CC}, while the MTCHB output of the SLAVE becomes the MXI input of the MASTER. This provides handshaking between the Master and Slave device for the snoop invalidation protocol. The $\overline{\text{RS}}$ input to the Master will allow a valid RAM dear operation. The Collision Detection Flag (CF) is taken from the Master, since collision is disabled on the Slave device.

Figure 4 shows width expansion using the Compare 6 protocol. The index remains 4K (12 bits) with a 16-bit tag field and 4 status bits. This configuration allows 28 bits to be cached on each port. Match outputs and flags are gated as in the previous example, along with port controls and index addresses bussed in parallel to both devices. Reset and MXI are tied high on the SLAVE device, and $\overline{\text{COMP6}}$ is tied low. Either device can enable the Compare 6 function, but the Slave device is suggested. If the Master detects a miss condition, then the Slave MTCHB input to MXI doesn’t matter. And using 10 tag bits on the Master increases the chance of detecting a miss. Therefore, the $\overline{\text{COMP6}}$ input to the MASTER is tied high in this example.

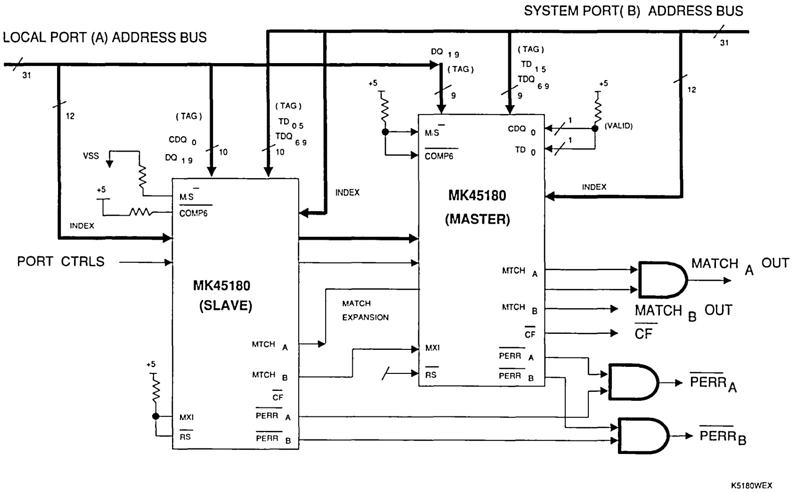
FLASH CLEAR OPERATION

The MK45180 includes an asynchronous Reset or Flash Clear function by asserting the $\overline{\text{RS}}$ pin active low (V_{IL}) for a duration of t_{RLRH}. This will effectively clear all CDQ0 RAM locations, thereby invalidating all cache entries. After reset, the remainder of the array is considered invalid.

A Reset cycle is required for each device configured as the Master before normal system tasks begin to fill the cache. This clears the valid bit for all cache tag locations, and ensures that initial compare cycles indicate a miss condition for both local and snoop compare operations. All inputs are considered don’t care and invalid while the $\overline{\text{RS}}$ input is low. All device outputs will go high impedance from the falling edge of the $\overline{\text{RS}}$ input. Device flag outputs ($\overline{\text{CF}}$, $\overline{\text{PERRA}}$ and $\overline{\text{PERRB}}$) will go high dur-ing a reset cycle. $MTCH_B$ will also go high during reset operations as shown in the “PORT B MAS-TER/SLAVE TRUTH TABLE”.

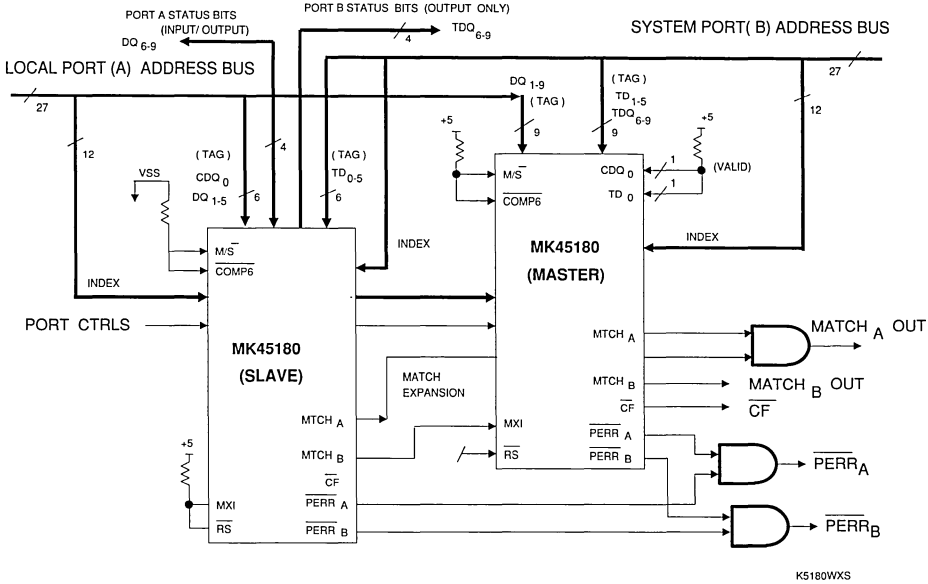
Since the reset function is asynchronous to all other operations, care should be taken to ensure that any low going system noise, coupled onto the RS input, does not cause VIH to drop below specified VIH levels. Glitches on the RS input could produce partial loss of data resulting in degraded system performance. A pull-up resistor in the range of 1K to 2.2K ohms is recommended for the $\overline{\text{RS}}$ input to enhance proper operation.

Figure 3 : Match Width Expansion Diagram


SYSTEM PORT(B) ADDRESS BUS
LOCAL PORT (A) ADDRESS BUS
31
12
(TAG)
CDQ 0
DQ 1 9
10
VSS
+5
M.S
COMP6
INDEX
(TAG)
TD 0 5
TDQ 6 9
PORT CTRLS
MK45180
(SLAVE)
MTCH A
MTCH B
CF
MXI
RS
PERR A
PERR B
MATCH EXPANSION
DQ 1 9
(TAG)
9
(TAG)
TD 1 5
TDQ 6 9
(VALID)
CDQ 0
TD 0
MK45180
(MASTER)
MTCH A
MTCH B
CF
PERR A
PERR B
MATCH A OUT
MATCH B OUT
CF
PERRA
PERRB
K5180WEX

Master/Slave 4K x 20-bit TAG with Parity

Figure 4 : Match Width Expansion Using COMP6


PORT A STATUS BITS (INPUT/ OUTPUT)
DQ 6-9
PORT B STATUS BITS (OUTPUT ONLY)
4
TDQ 6-9
SYSTEM PORT(B) ADDRESS BUS
LOCAL PORT (A) ADDRESS BUS
27
12
(TAG)
CDQ 0
DQ 1-5
6
VSS
(TAG)
TD 0-5
M/S
COMP6
INDEX
PORT CTRLS
MK45180
(SLAVE)
MTCH A
MTCH B
CF
MXI
RS
PERR A
PERR B
MATCH EXPANSION
DQ 1-9
(TAG)
9
(TAG)
TD 1-5
TDQ 6-9
(VALID)
CDQ 0
TD 0
MK45180
(MASTER)
MTCH A
MTCH B
CF
PERR A
PERR B
MATCH A OUT
MATCH B OUT
CF
PERRA
PERRB
K5180WXS

Master/Slave 4K x 16-bit TAG with Parity plus 4 Status Bits

COHERENCY MODE SELECT TABLE

$M/\overline{S}$	CONFIGURATION	MTCHA	MTCHB	$\overline{\text{PERRA}}$, $\overline{\text{PERRB}}$	$\overline{\text{CF}}$
L	SLAVE; Disable Collision-Detect & Snoop Invalidate	Valid	Valid	Valid	High
H	MASTER; Enable Collision-Detect & Snoop Invalidate	Valid	Valid	Valid(1)	Valid

Note: 1. Parity is valid for each RAM location written after reset occurs.

COMP6 CONFIGURATION TABLE

$M/\overline{S}$	$\overline{\text{COMP6}}$	MODE	CDQ_0	DQ1-DQ5	DQ6-DQ9	$\overline{\text{TD0}}$-$\overline{\text{TD5}}$	$\overline{\text{TDQ6}}$ - $\overline{\text{TDQ9}}$
X	L	COMPARE 6 with 4 Status Bits	Valid Bit	Data/Tag I/O	Status Bit I/O	Tag Input	Status Bit Out
X	H	COMPARE 10 Tag Bits	Valid Bit	Data/Tag I/O	Data/Tag I/O	Tag Input	Tag Input

PORT A MASTER/SLAVE TRUTH TABLE

$\overline{\text{RS}}$	$\overline{\text{EA}}$	$\overline{\text{W}}$	$\overline{\text{G}}$	M/$\overline{\text{S}}$	CDQ0, DQ1-DQ9 *	$\overline{\text{PERRA}}$	MTCHA	MODE
L	X	X	X	X	High-Z	High-Z	High-Z	RESET / FLASH CLEAR
H	H	X	X	X	High-Z	High-Z	High-Z	DESELECT LOCAL PORT A
H	L	L	X	X	D_{IN}	Low	High-Z	WRITE (Force Parity Error)
H	L	L	X	X	D_{IN}	High	High-Z	WRITE (True Parity)
H	L	H	L	X	D_{OUT}	VALID	High-Z	READ (MTCHA High-Z)
H	L	H	H	X	TAG_{IN}	VALID	VALID	COMPARE/ MTCHA VALID (Hit or Miss)
H	L	H	H	X	TAG_{IN}	Low	VALID	COMPARE CYCLE with PARITY ERROR

Note: $\overline{\text{ASA}}$ is determinate only in collision detection
* Presumes COMP6 is high Truth Table reflects valid port operation for either logic state of $\overline{\text{COMP6}}$.
If COMP6 is low, DQ6-DQ9 are status bit outputs instead of tag data inputs.

PORT B MASTER/SLAVE TRUTH TABLE

$\overline{\text{RS}}$	$\overline{\text{EB}}$	$\overline{\text{SW}}$	M/$\overline{\text{S}}$	MXI	TD0-TD5 TDQ6-TDQ9*	$\overline{\text{PERRB}}$	MTCHB	MODE	SNOOP INVALIDATE
L	X	X	X	X	High-Z	High-Z	Low	RESET / FLASH CLEAR	—
H	H	X	X	X	High-Z	High-Z	Low	DESELECT SYSTEM PORT B	—
H	L	X	H	L	TAG_{IN}	VALID	Low (1)	SNOOP CYCLE / MXI Low	No
H	L	X	H	H	TAG_{IN}	VALID	MISS	SNOOP CYCLE (NO Match)	No
H	L	L	H	H	TAG_{IN}	VALID	HIT †	SNOOP WRITE / (Master - MATCH)	Yes
H	L	H	H	H	TAG_{IN}	VALID	HIT †	SNOOP READ / (Master - MATCH)	No
H	L	L	L	H	TAG_{IN}	VALID	VALID	SNOOP WRITE/ VALID (Hit / Miss Slave)	No
H	L	H	L	H	TAG_{IN}	VALID	VALID	SNOOP READ/ VALID (Hit / Miss Slave)	No

Notes: $\overline{\text{ASB}}$ is determinate only in collision detection
(1) A low level on MXI (match expansion) will force the Port B match (MTCHB) to be low (miss).
† MXI must be High for a valid compare snoop-hit operation.
* Presumes COMP6 is high Truth Table reflects valid port operation for either logic state of $\overline{\text{COMP6}}$.
If COMP6 is low, TDQ6-TDQ9 are status bit outputs instead of tag data inputs.

COLLISION DETECTION LOGIC

$\overline{RS}$	$\overline{EA}$, $\overline{EB}$	PORT A OPERATION	PORT B OPERATION	$\overline{ASA}$	$\overline{ASB}$	PORT INDEX	$\overline{CF}$
L	X	RESET	RESET	X	X	X	HIGH
H	H	DESELECT	DESELECT	X	X	X	HIGH
H	L	X	X	H	X	A = B	HIGH
H	L	X	X	X	H	A = B	HIGH
H	L	READ	Snoop WRITE	L	L	A = B	LOW
H	L	WRITE	Snoop WRITE	L	L	A = B	LOW
H	L	COMPARE	Snoop WRITE	L	L	A = B	LOW
H	L	READ	Snoop READ	L	L	A = B	HIGH
H	L	WRITE	Snoop READ	L	L	A = B	LOW
H	L	COMPARE	Snoop READ	L	L	A = B	HIGH

Note: This table presumes that index AA0-AA11 = AB0-AB11 for all examples where M/$\overline{S}$ = high

COLLISION FLAG TRUTH TABLE

$\overline{W}$	$\overline{G}$	$\overline{SW}$	$\overline{CF}$
L	X	X	L
H	X	L	L
H	X	H	H

Note. Truth table assumes a valid address cycle where index A=B with $\overline{ASA}$ and $\overline{ASB}$ low.

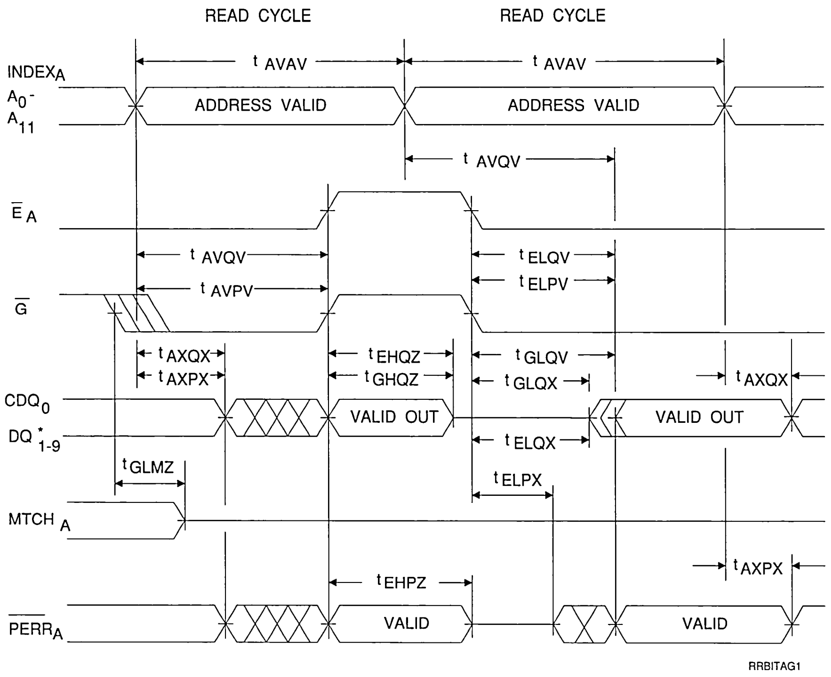
PORT A: READ CYCLE TIMING - AC OPERATING CONDITIONS AND CHARACTERISITICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		Units	Notes
		PORT A		PORT A			
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Read Cycle Time	20		25		ns	
t_{AVQV}	Address to Data Valid Access Time		20		25	ns	4
t_{GLQV}	Output Enable ($\overline{G}$) Q Valid Access Time		10		12	ns	4
t_{ELQV}	Port Enable ($\overline{EA}$) Q Valid Access Time		17		20	ns	4
t_{AVPV}	Address to $\overline{PERR}$ Valid Access Time		20		25	ns	4
t_{ELPV}	Port Enable ($\overline{EA}$) to $\overline{PERR}$ Valid		17		20	ns	4
t_{AXQX}	Output (Q) Hold from Address	2		2		ns	4
t_{AXPX}	$\overline{PERR}$ Hold Time from Address	2		2		ns	4
t_{EHQZ}	Port Disable to Q High-Z	0	10	0	10	ns	5
t_{EHPZ}	Port Disable to $\overline{PERRA}$ High-Z	0	10	0	10	ns	5
t_{GHQZ}	Output Disable ($\overline{G}$) to Q High-Z	0	8	0	10	ns	5
t_{GLQX}	Output Enable ($\overline{G}$) to Q Low-Z	0		0		ns	5
t_{ELQX}	Port Enable ($\overline{EA}$) to Q Low-Z	0		0		ns	5
t_{ELPX}	Port Enable ($\overline{EA}$) to $\overline{PERRA}$ Low-Z	0		0		ns	5

Note: $\overline{ASA}$ is presumed valid for all read timing examples

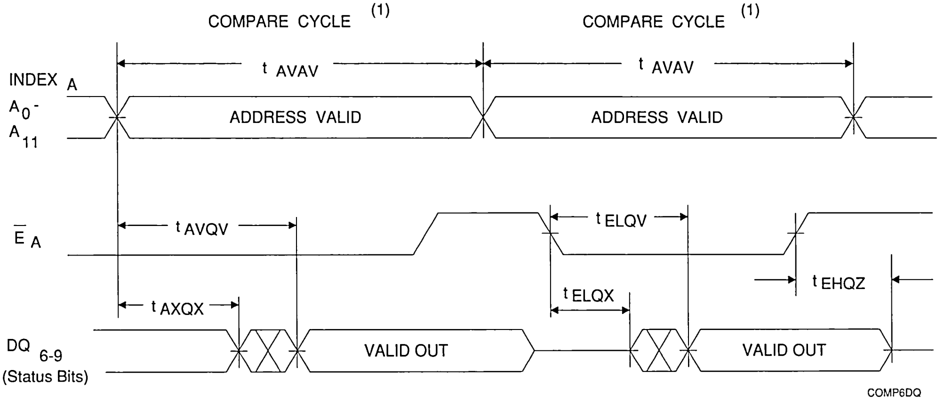
Figure 5 : PORT A : Read Cycle Timing


READ CYCLE
READ CYCLE
INDEX$_A$
A_0 -
A_{11}
t_{AVAV}
t_{AVAV}
ADDRESS VALID
ADDRESS VALID
t_{AVQV}
$\overline{E}_A$
t_{AVQV}
t_{AVPV}
t_{ELQV}
t_{ELPV}
$\overline{G}$
t_{AXQX}
t_{AXPX}
t_{EHQZ}
t_{GHQZ}
t_{GLQV}
t_{GLQX}
t_{AXQX}
CDQ_0
DQ_{1-9} *
VALID OUT
VALID OUT
t_{ELQX}
t_{GLMZ}
t_{ELPX}
MTCH $_A$
t_{AXPX}
t_{EHPZ}
$\overline{PERR}_A$
VALID
VALID
RRBITAG1

* Avoid metastable inputs.

Note: $\overline{W}$ is presumed high

Figure 6 : PORT A : Read Status Bit Timing


COMPARE CYCLE (1)
COMPARE CYCLE (1)
INDEX $_A$
A_0 -
A_{11}
t_{AVAV}
t_{AVAV}
ADDRESS VALID
ADDRESS VALID
$\overline{E}_A$
t_{AVQV}
t_{ELQV}
t_{EHQZ}
t_{ELQX}
t_{AXQX}
DQ $_{6-9}$
(Status Bits)
VALID OUT
VALID OUT
COMP6DQ

Notes : (1) $\overline{W}$ = $\overline{G}$ = high. $\overline{COMP6}$ = low.

PORT A: WRITE CYCLE TIMING - AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5.0 \pm 5\%$)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		Units	Notes
		PORT A		PORT A			
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time	20		25			
t_{AVEL}	Address Set-Up Time ($\overline{EA}$)	0		0			
t_{AVEH}	Address Valid to End of Write ($\overline{EA}$)	16		18			
t_{AVWL}	Address Set-Up Time ($\overline{W}$)	0		0			
t_{AVWH}	Address Valid to End of Write ($\overline{W}$)	16		18			
t_{EHAX}	Address Hold after End of Write ($\overline{EA}$)	3		3			
t_{WHAX}	Address Hold after End of Write ($\overline{W}$)	3		3			
t_{ELEH}	Port Enable Pulse Width	16		18			
t_{WLWH}	Write Command ($\overline{W}$) Pulse Width	14		16			
t_{ELWH}	Port Enable to End of Write	16		18			
t_{DVEH}	Data Set-Up Time to $\overline{EA}$ High	12		14			
t_{EHDX}	Data Hold Time to $\overline{EA}$ High	0		0			
t_{DVWH}	Data Set-Up Time to $\overline{W}$ High	12		14			
t_{WHDX}	Data Hold Time from $\overline{W}$ High	0		0			
t_{WLQZ}	Write Enable ($\overline{W}$) Low to Q High-Z	0	8	0	10		5
t_{WHQX}	Write Enable ($\overline{W}$) High to Q Low-Z	2		2			5

Note: $\overline{ASA}$ is presumed valid for all write cycle timing examples.

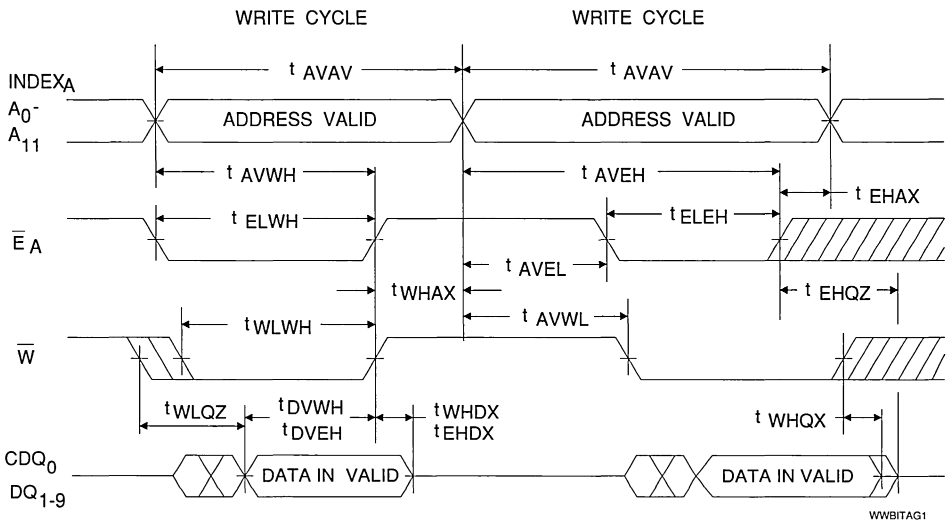
PORT A: PARITY DIAGNOSTIC WRITE TIMING - AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		Units	Notes
		PORT A		PORT A			
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Parity Diagnostic Write Cycle Time	25		30		ns	
t_{WHPV}	Write Enable ($\overline{W}$) High to $\overline{PERRA}$ Valid		20		25	ns	4
t_{WLPZ}	Write Enable ($\overline{W}$) Low to $\overline{PERRA}$ Input High-Z	0	8	0	10	ns	5
t_{PLWH}	$\overline{PERRA}$ Input Low to End of Parity Diagnostic Write	14		16		ns	
t_{WHPH}	$\overline{PERRA}$ Input Hold Time after Parity Diasgnostic Write ($\overline{W}$ = high)	0		0		ns	
t_{WHPX}	Write Enable (W) High to $\overline{PERRA}$ Low-Z	2		2		ns	5

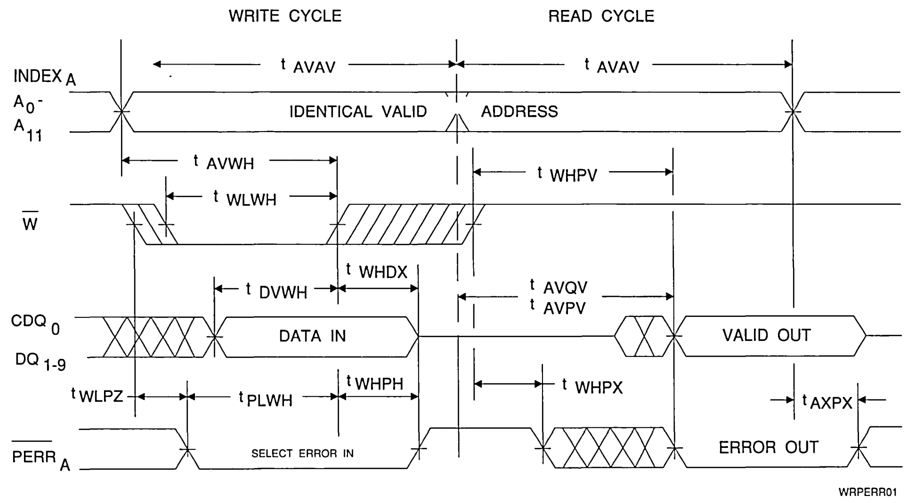
Notes: All other parameters are equal to the normal write cycle timing parameters.

Figure 7 : PORT A : Write Cycle Timing


WRITE CYCLE
WRITE CYCLE
INDEX$_A$
A_0-
A_{11}
t AVAV
t AVAV
ADDRESS VALID
ADDRESS VALID
t AVWH
t AVEH
t EHAX
$\overline{E}_A$
t ELWH
t ELEH
t AVEL
t WHAX
t EHQZ
t WLWH
t AVWL
$\overline{W}$
t WLQZ
t DVWH
t DVEH
t WHDX
t EHDX
t WHQX
CDQ$_0$
DQ$_{1-9}$
DATA IN VALID
DATA IN VALID
WWBITAG1

Notes : $\overline{G}$ is presumed high. Write cycles with $\overline{G}$ high are recommended to avoid bus contention.
Addresses must remain stable during write cycles. Either $\overline{W}$ or $\overline{E}_A$ must terminate a write cycle.

Figure 8 : Parity Diagnostic Write Cycle Timing


WRITE CYCLE
READ CYCLE
INDEX$_A$
A_0-
A_{11}
t AVAV
t AVAV
IDENTICAL VALID
ADDRESS
t AVWH
t WHPV
t WLWH
$\overline{W}$
t WHDX
t DVWH
t AVQV
t AVPV
CDQ$_0$
DQ$_{1-9}$
DATA IN
VALID OUT
t WLPZ
t PLWH
t WHPH
t WHPX
t AXPX
$\overline{PERR}_A$
SELECT ERROR IN
ERROR OUT
WRPERR01

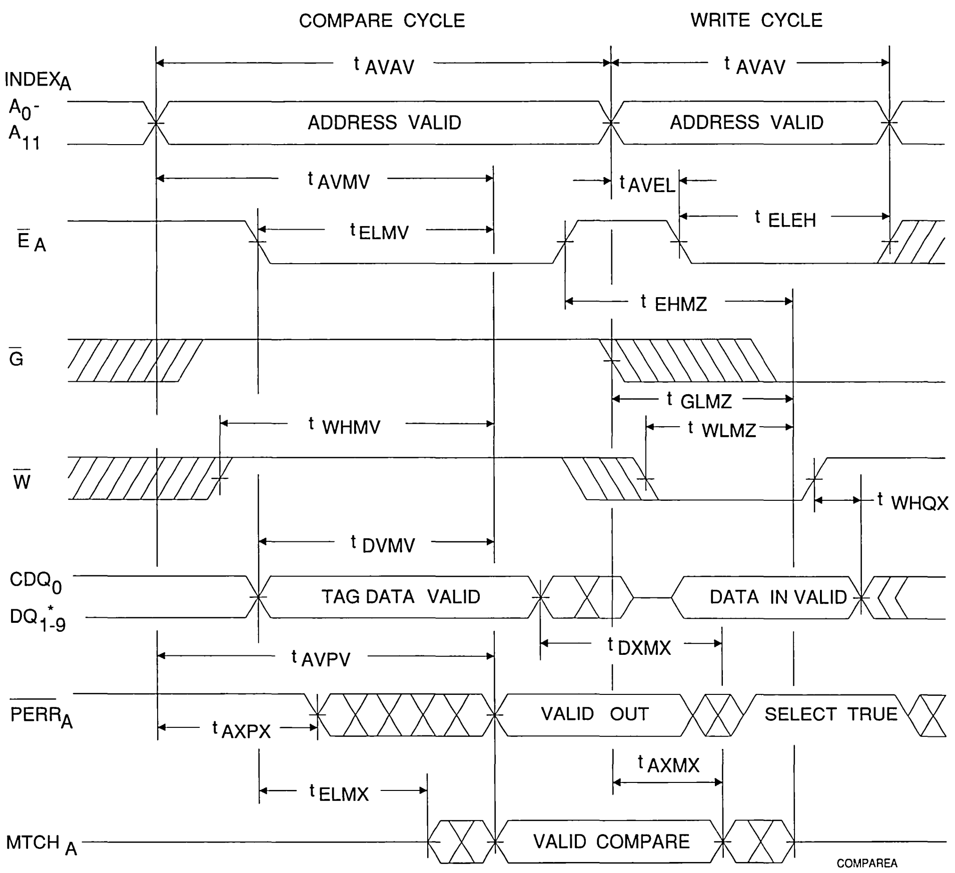
Notes : $\overline{E}_A$ is presumed low ; $\overline{G}$ is high
Addresses must remain stable during write cycles. Either $\overline{W}$ or $\overline{E}_A$ must terminate a write cycle.

PORT A: COMPARE CYCLE TIMING
AC OPERATING CONDITIONS AND CHARACTERISTICS
($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		Units	Notes
		PORT A		PORT A			
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Compare Cycle Time	20		25		ns	6
t_{WHMV}	Write Enable High to MTCHA Valid ($\overline{G}$ = high)		17		20	ns	7
t_{WLMZ}	$\overline{W}$ Low to MTCHA High-Z	0	10	0	10	ns	7
t_{GLMZ}	$\overline{G}$ Low to MTCHA High-Z	0	10	0	10	ns	7
t_{DVMV}	Data (Tag) Compare Access Time		12		15	ns	7
t_{AVMV}	Address Compare (MTCHA) Access Time		17		20	ns	7
t_{ELMV}	Port Enable Compare (MTCHA) Access Time		8		10	ns	7
t_{AXMX}	Address Compare MTCHA Hold Time	2		2		ns	7
t_{DXMX}	MTCHA Hold Time from Tag Data	2		2		ns	7
t_{ELMX}	Port Enable Low to MTCHA Low-Z	0		0		ns	7
t_{EHMZ}	Port Enable High to (MTCHA) High-Z	0	10	0	10	ns	7
t_{EHMX}	Port Enable MTCHA Hold Time	2		2		ns	7

Note: $\overline{ASA}$ is presumed valid for all compare cycle timing examples.

Figure 9 : PORT A : Compare/Write Cycle Timing


COMPARE CYCLE
WRITE CYCLE
t AVAV
t AVAV
INDEXA
A0-
A11
ADDRESS VALID
ADDRESS VALID
t AVMV
t AVEL
t ELEH
E A
t ELMV
t EHMZ
G
t GLMZ
t WHMV
t WLMZ
W
t WHQX
t DVMV
CDQ0
DQ*1-9
TAG DATA VALID
DATA IN VALID
t AVPV
t DXMX
PERRA
VALID OUT
SELECT TRUE
t AXPX
t AXMX
t ELMX
MTCH A
VALID COMPARE
COMPAREA

* Avoid metastable inputs.

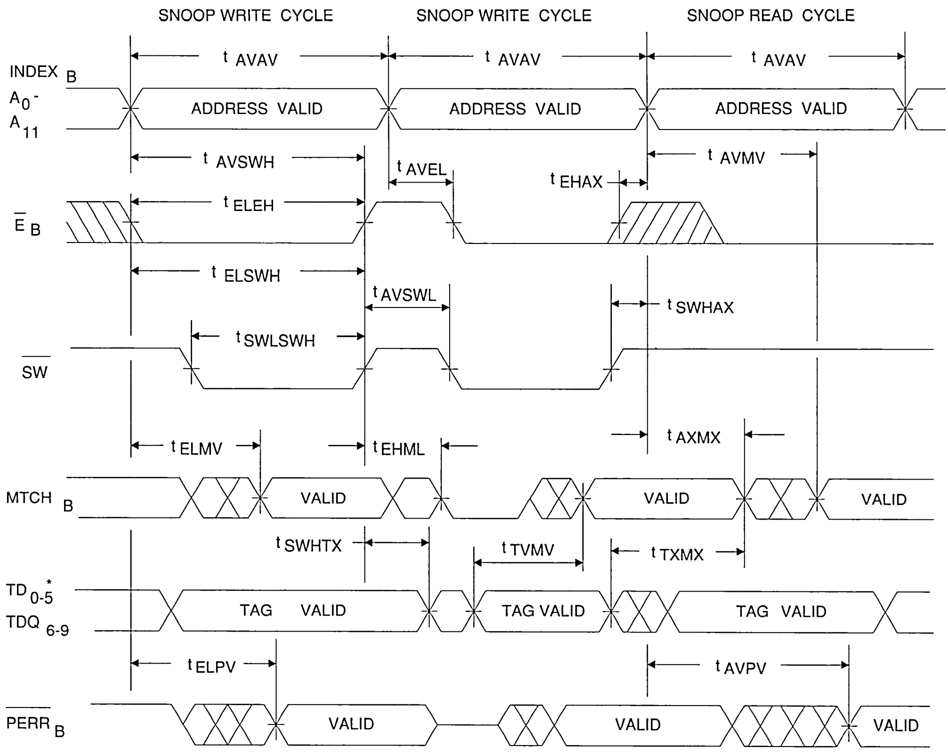
PORT B: SNOOP CYCLE TIMING - AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		Units	Notes
		PORT B		PORT B			
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Snoop Cycle Time	30		35		ns	
t_{AVEL}	Address Set-Up Time to Port Enable	0		0		ns	
t_{AVEH}	Address Valid to Port Disable ($\overline{E}$ High)	25		30		ns	
t_{EHAX}	Address Hold after End of Cycle ($\overline{E}$ High)	5		5		ns	
t_{ELEH}	Port Enable Pulse Width	25		30		ns	
t_{AVSWH}	Address Valid to End of Snoop Bus Write ($\overline{SW}$ High)	25		30		ns	
t_{ELSWH}	Port Enable ($\overline{EB}$) to End of Snoop Write	25		30		ns	
t_{AVSWL}	Address Valid to Snoop Write ($\overline{SW}$ Low)	5		5		ns	
t_{SWLSWH}	Snoop Write Command Pulse Width	20		25		ns	
t_{SWHAX}	Address Hold Time after End of Snoop Write	5		5		ns	
t_{TVSWL}	Tag Data Input Set-up Time to $\overline{SW}$ Low	0		0		ns	
t_{SWHTX}	Tag Data Input Hold Time from End of Snoop Write	5		5		ns	
t_{AVMV}	Address Compare (MTCHB) Access Time		20		23	ns	6
t_{AXMX}	Address Compare MTCHB Hold Time	2		2		ns	6
t_{ELMV}	Port Enable Compare (MTCHB) Access Time		18		21	ns	6
t_{ELMX}	Port Enable to MTCHB Low-Z	0		0		ns	7
t_{EHML}	Port Disable to Compare MTCHB Low		10		12	ns	6
t_{TVMV}	Tag Data Valid to Compare Access Time		12		15	ns	6
t_{TXMX}	Tag Data Compare MTCHB Hold Time	2		2		ns	6
$t_{SWH\text{-}MX}$	MTCHB Hold Time After Snoop Invalidation	2		2		ns	6
$t_{SWH\text{-}TQX}$	Status Bit Hold Time from End of Snoop Write ($\overline{SW}$ high)	2		2		ns	4
$t_{SWH\text{-}PX}$	$\overline{PERRB}$ Status Bit Hold Time from End of Snoop Write (SW high)	2		2		ns	4

Note: $\overline{AS}_A$ is presumed valid for all snoop cycle timing examples.

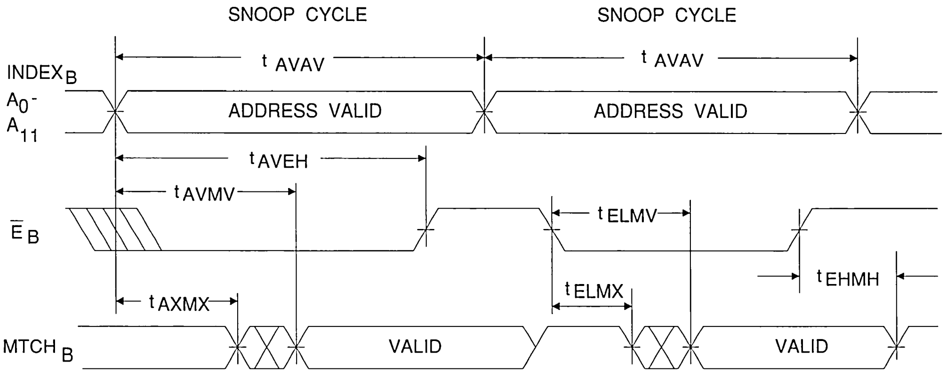
Figure 10 : PORT B Snoop Cycle Timing


SNOOP WRITE CYCLE
SNOOP WRITE CYCLE
SNOOP READ CYCLE
t AVAV
t AVAV
t AVAV
INDEX B
A0 -
A11
ADDRESS VALID
ADDRESS VALID
ADDRESS VALID
t AVSWH
t AVEL
t EHAX
t AVMV
t ELEH
E B
t ELSWH
t AVSWL
t SWHAX
t SWLSWH
SW
t ELMV
t EHML
t AXMX
MTCH B
VALID
VALID
VALID
t SWHTX
t TVMV
t TXMX
TD 0-5 *
TDQ 6-9
TAG VALID
TAG VALID
TAG VALID
t ELPV
t AVPV
PERR B
VALID
VALID
VALID

* Avoid metastable inputs

WRSNOOP

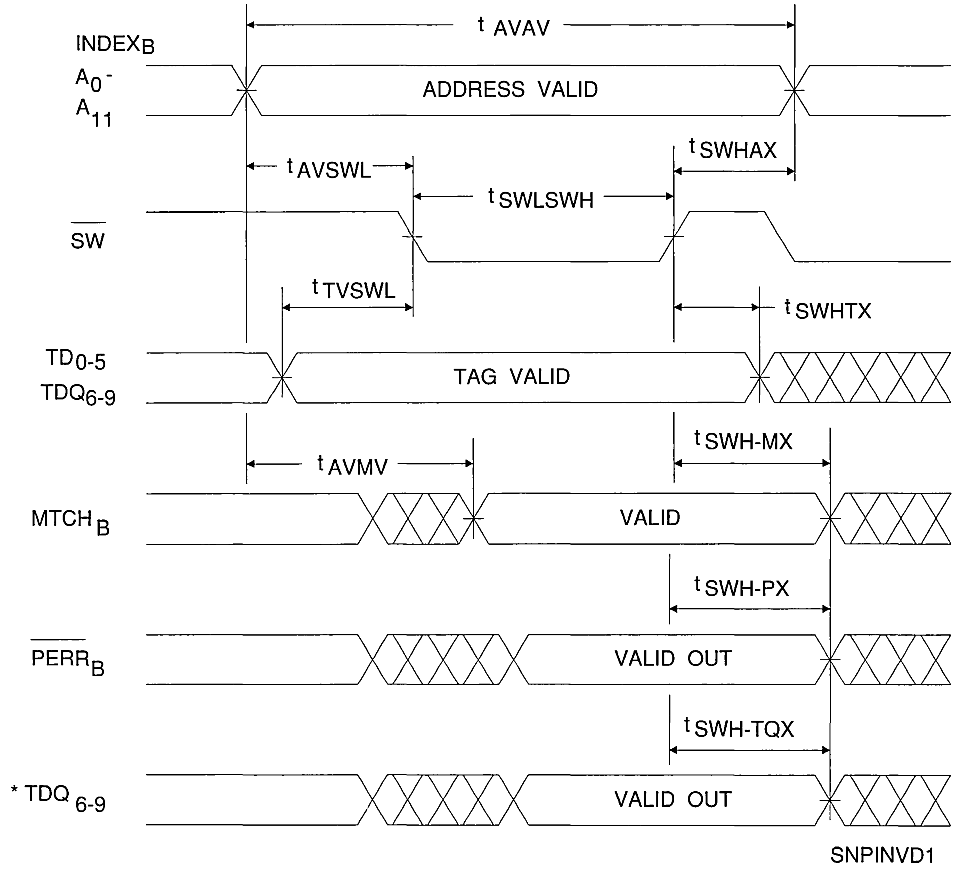
Figure 8 : PORT B Compare (match) Timing


SNOOP CYCLE
SNOOP CYCLE
t AVAV
t AVAV
INDEX B
A0 -
A11
ADDRESS VALID
ADDRESS VALID
t AVEH
t AVMV
t ELMV
E B
t ELMX
t EHMH
t AXMX
MTCH B
VALID
VALID

SNPMTCH

Notes : Valid snoop cycles are referenced from port enable ($\overline{E}_B$).

Figure 12 : PORT B Snoop Invalidation Cycle Timing


t AVAV
INDEXB
A0 -
A11
ADDRESS VALID
t AVSWL
t SWHAX
t SWLSWH
SW
t TVSWL
t SWHTX
TD0-5
TDQ6-9
TAG VALID
t AVMV
t SWH-MX
MTCH B
VALID
t SWH-PX
PERRB
VALID OUT
t SWH-TQX
* TDQ 6-9
VALID OUT
SNPINVD1

* If $\overline{\text{COMP6}}$ is low.

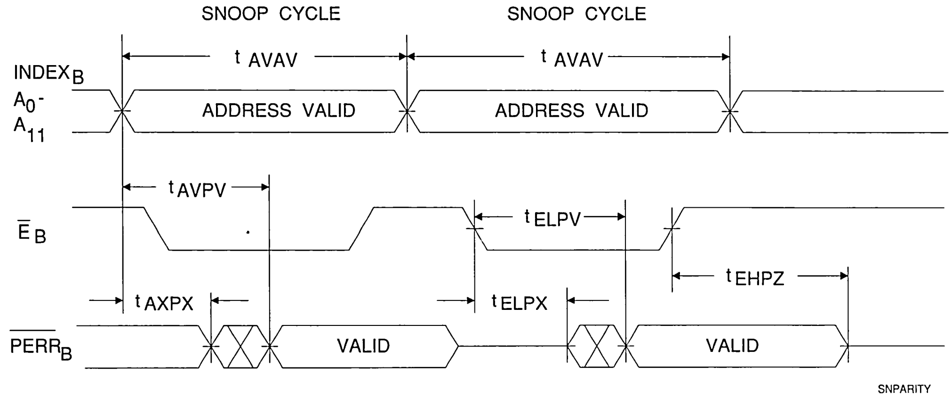
Note $\overline{E}_B$ is presumed low.

PORT B : PARITY ERROR AND STATUS BIT OUTPUT TIMING AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

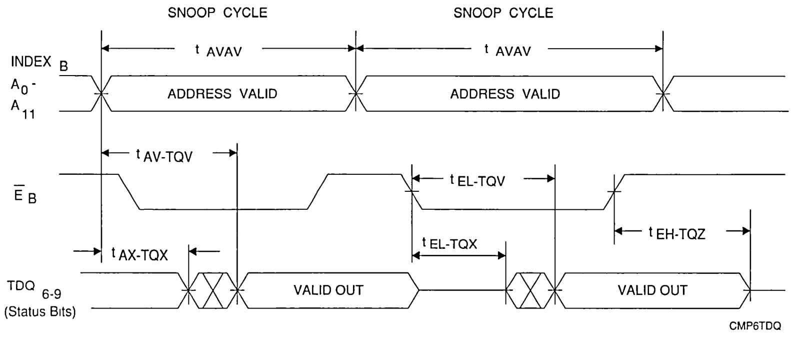
SYMBOL	PARAMETER	MK45180-17		MK45180-20		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Snoop Cycle Time	30		35		ns	
t_{AVPV}	Address Valid to $\overline{\text{PERRB}}$ Output Valid Access Time		25		30	ns	4
t_{ELPV}	Port Enable to $\overline{\text{PERRB}}$ Output Valid Access Time		17		20	ns	4
t_{EHPZ}	Port Disable ($\overline{\text{EB}}$ high) to $\overline{\text{PERRB}}$ High-Z	0	10	0	10	ns	4
t_{AXPX}	$\overline{\text{PERRB}}$ Hold from Address Change	2		2		ns	4
t_{ELPX}	Port Enable to $\overline{\text{PERRB}}$ Low-Z	0		0		ns	5
$t_{AV\text{-}TQV}$	Address Valid to Status Bits (TDQx) Valid Access Time		20		25	ns	4
$t_{EL\text{-}TQV}$	Port Enable to Status Bits Valid Access Time		17		20	ns	4
$t_{AX\text{-}TQX}$	Status Bit Hold Time from Address Change	2		2		ns	4
$t_{EL\text{-}TQX}$	Port Enable to TDQx Low-Z	0		0		ns	5
$t_{EH\text{-}TQZ}$	Port Disable ($\overline{\text{EB}}$ high) to TDQx high-Z	0	10	0	10	ns	5

Figure 13 : PORT B Parity Error Output Timing


SNOOP CYCLE
SNOOP CYCLE
t AVAV
t AVAV
INDEXB
A0 -
A11
ADDRESS VALID
ADDRESS VALID
t AVPV
EB
t ELPV
t EHPZ
t AXPX
t ELPX
PERRB
VALID
VALID
SNPARITY

Notes : Valid snoop cycles are referenced from port enable ($\overline{\text{E}}_B$)

Figure 14 : PORT B : Read Statuts Bit Timing

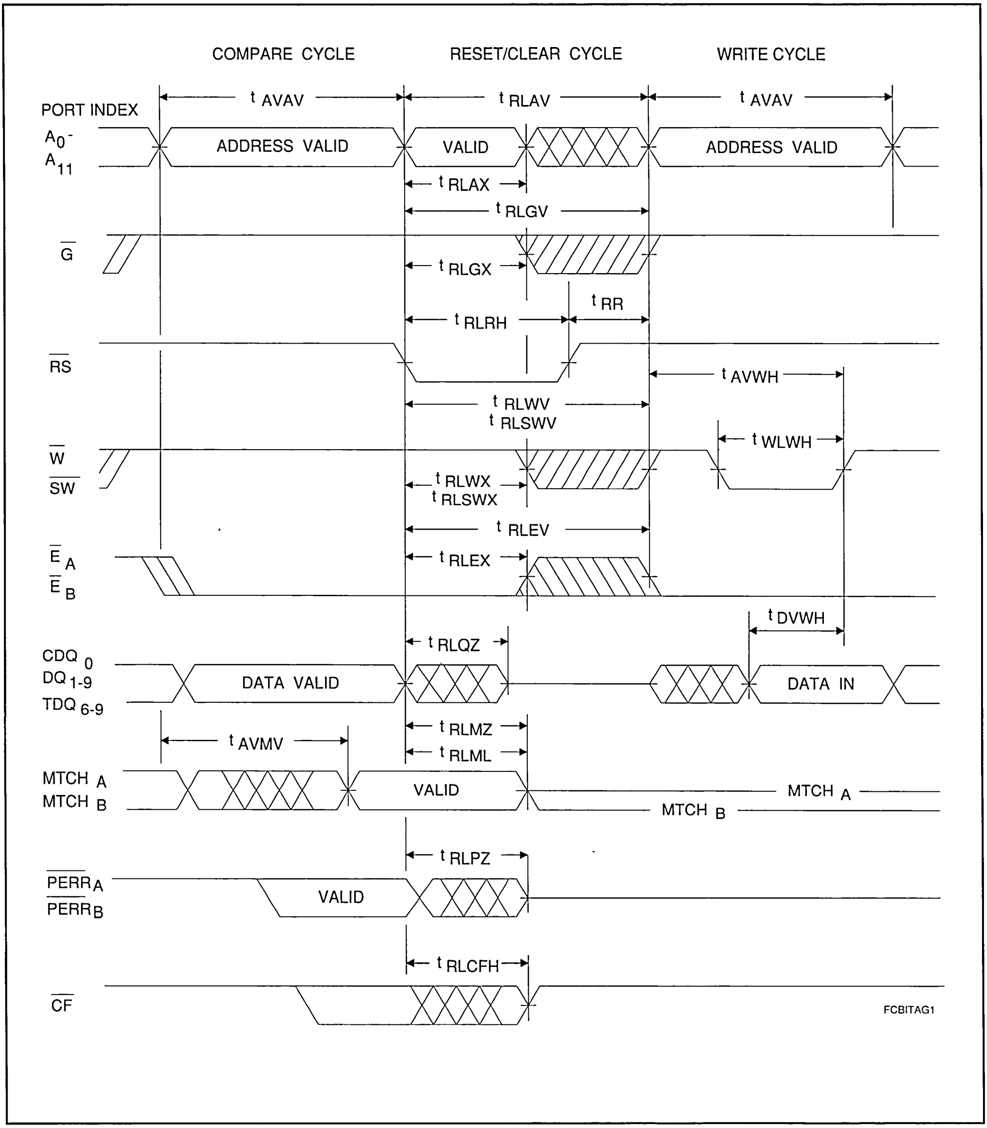

SNOOP CYCLE
SNOOP CYCLE
t AVAV
t AVAV
INDEX B
A0 -
A11
ADDRESS VALID
ADDRESS VALID
t AV-TQV
$\overline{E}$ B
t EL-TQV
t EH-TQZ
t EL-TQX
t AX-TQX
TDQ 6-9
(Status Bits)
VALID OUT
VALID OUT
CMP6TDQ

Note : $\overline{\text{COMP6}}$ is presumed low.

RESET/CLEAR CYCLE TIMING - AC OPERATING CONDITIONS AND CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		Units	Notes
		MIN.	MAX.	MIN.	MAX.		
t_{RLAV}	Reset Cycle Time	70		70		ns	
t_{RLRH}	Reset ($\overline{RS}$) Pulse Width	10		10		ns	
t_{RLAX}	Reset ($\overline{RS}$ Low) to Address Don't Care	0		0		ns	
t_{RLASX}	Reset to Address Strobe Don't Care	0		0		ns	
t_{RLGX}	Reset to $\overline{G}$ Input Don't Care	0		0		ns	
t_{RLWX}	Reset to $\overline{W}$ Input Don't Care	0		0		ns	
t_{RLSWX}	Reset to Snoop Write Enable ($\overline{SW}$) Don't Care	0		0		ns	
t_{RLEX}	Reset to $\overline{Ex}$ Don't care	0		0		ns	
t_{RR}	Reset Recovery Time	20		20		ns	
t_{RLQZ}	Reset to CDQ0 /DQ High-Z	0	20	0	25	ns	5
t_{RLPZ}	Reset to Parity Error ($\overline{PERRA}$, $\overline{PERRB}$) High-Z	0	20	0	25	ns	4
t_{RLMZ}	Reset to MTCHA High-Z	0	20	0	25	ns	7
t_{RLML}	Reset to MTCHB Low		20		25	ns	6
t_{RLCFH}	Reset to Collision Detection Flag ($\overline{CF}$) High		20		25	ns	4
t_{RLGV}	Reset to $\overline{G}$ Input Recognized	70		70		ns	
t_{RLWV}	Reset to $\overline{W}$ Input Recognized	70		70		ns	
t_{RLEV}	Reset to $\overline{Ex}$ Input Recognized	70		70		ns	

Figure 15 : Reset/Clear Cycle Timing

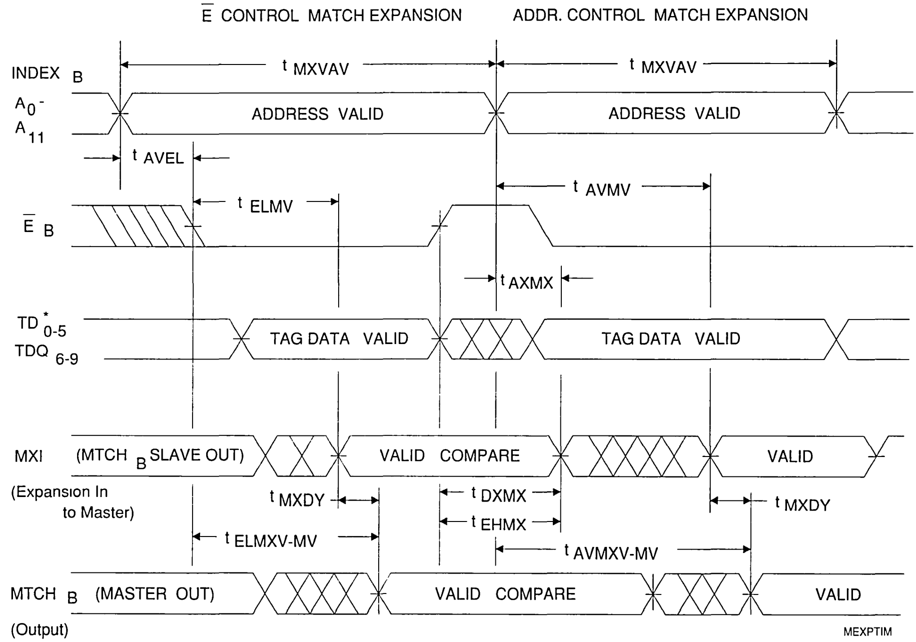

COMPARE CYCLE
RESET/CLEAR CYCLE
WRITE CYCLE
PORT INDEX
A0 - A11
tAVAV
tRLAV
ADDRESS VALID
VALID
tRLAX
tRLGV
G
tRLGX
tRLRH
tRR
RS
tAVWH
tRLWV
tRLSWV
W
SW
tWLWH
tRLWX
tRLSWX
tRLEV
tRLEX
EA
EB
tDVWH
tRLQZ
CDQ0
DQ1-9
TDQ6-9
DATA VALID
DATA IN
tAVMV
tRLMZ
tRLML
MTCHA
MTCHB
tRLPZ
PERRA
PERRB
tRLCFH
CF
FCBITAG1

PORT B : MATCH WIDTH EXPANSION CYCLE TIMING
AC OPERATING CONDITIONS AND CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{MXVAV}	Match Width Expansion Cycle Time	35		40		ns	
$t_{AVMXV\text{-}MV}$	Address Expansion MTCHB Access Time		25		28	ns	6
$t_{ELMXV\text{-}MV}$	Port Enable Expansion MTCHB Access		23		26	ns	6
t_{MXDY}	Match Expansion Delay Time		5		5	ns	6

Figure 16 : Match Width Expansion Timing


Ē CONTROL MATCH EXPANSION
ADDR. CONTROL MATCH EXPANSION
INDEX B
A0 - A11
t MXVAV
t MXVAV
ADDRESS VALID
ADDRESS VALID
t AVEL
t ELMV
t AVMV
Ē B
t AXMX
TD* 0-5
TDQ 6-9
TAG DATA VALID
TAG DATA VALID
MXI
(MTCH B SLAVE OUT)
VALID COMPARE
VALID
(Expansion In to Master)
t MXDY
t DXMX
t EHMX
t MXDY
t ELMXV-MV
t AVMXV-MV
MTCH B
(MASTER OUT)
VALID COMPARE
VALID
(Output)
MEXPTIM

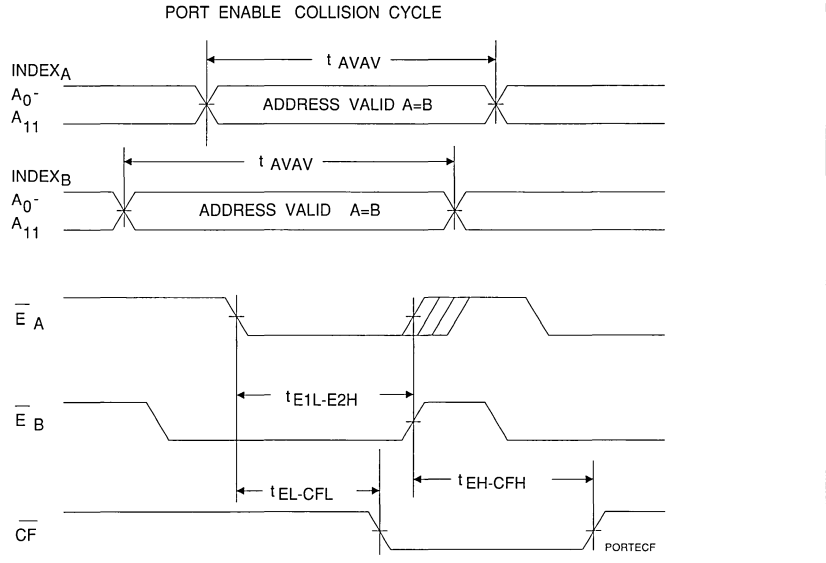
* Avoid metastable inputs

COLLISION DETECTION TIMING - AC OPERATING CONDITIONS AND CHARACTERISITICS

($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MK45180-17		MK45180-20		Units	Notes
		MIN.	MAX.	MIN.	MAX.		
$t_{AV\text{-}ASL}$	Address Index Valid to Address Strobe Active (Low)		5		5	ns	
$t_{ASH\text{-}AX}$	Address Strobe High to Address Index Change		5		5	ns	
$t_{ASL\text{-}CFL}$	Address Strobe Low to Collision Flag ($\overline{CF}$) Asserted		12		15	ns	4
$t_{ASH\text{-}CFH}$	Address Strobe High to $\overline{CF}$ High	5		5		ns	4
$t_{AX\text{-}CFH}$	Port Index Address Change to $\overline{CF}$ High	5		5		ns	4
$t_{ASL\text{-}ASH}$	Port Address Strobe Set-Up Time	12		15		ns	
$t_{E1L\text{-}E2H}$	Collision Set-Up Time for Both Ports Enabled to One Port Disabled	12		15		ns	
$t_{EL\text{-}CFL}$	Either Port Enable Low to $\overline{CF}$ Asserted		12		15	ns	4
$t_{EH\text{-}CFH}$	Either Port Disable to $\overline{CF}$ High	5		5		ns	4
$t_{WL\text{-}CFL}$	Port A Write Command ($\overline{W}$ = low) to $\overline{CF}$ Asserted		12		15	ns	4
$t_{WH\text{-}CFH}$	Port A Compare/Read Command ($\overline{W}$ = high) to $\overline{CF}$ High	5		5		ns	4
$t_{SWL\text{-}CFL}$	Port B Snoop-Write Command ($\overline{SW}$ = low) to $\overline{CF}$ Asserted		12		15	ns	4
$t_{SWH\text{-}CFH}$	Port B Snoop-Read Command ($\overline{SW}$ = high) to $\overline{CF}$ High	5		5		ns	4
$t_{SHW\text{-}WH}$	Port A Collision Displacement : $\overline{W}$ Low Hold Time after End of Snoop Write	10		12		ns	
$t_{CFH\text{-}QX}$	Output (MTCHx, $\overline{PERR}$x, DQx, TDQ6-TDQ9) Hold Time from $\overline{CF}$ High	2		2		ns	4,6

Figure 17 : Port Enable Collision Cycle Timing


PORT ENABLE COLLISION CYCLE
INDEXA A0-A11
t AVAV
ADDRESS VALID A=B
INDEXB A0-A11
t AVAV
ADDRESS VALID A=B
E A
E B
t E1L-E2H
t EL-CFL
t EH-CFH
CF
PORTECF

Note Address Strobes ($\overline{AS}_X$) are presumed low.

Figure 18 : Port Operation Collision Cycle Timing

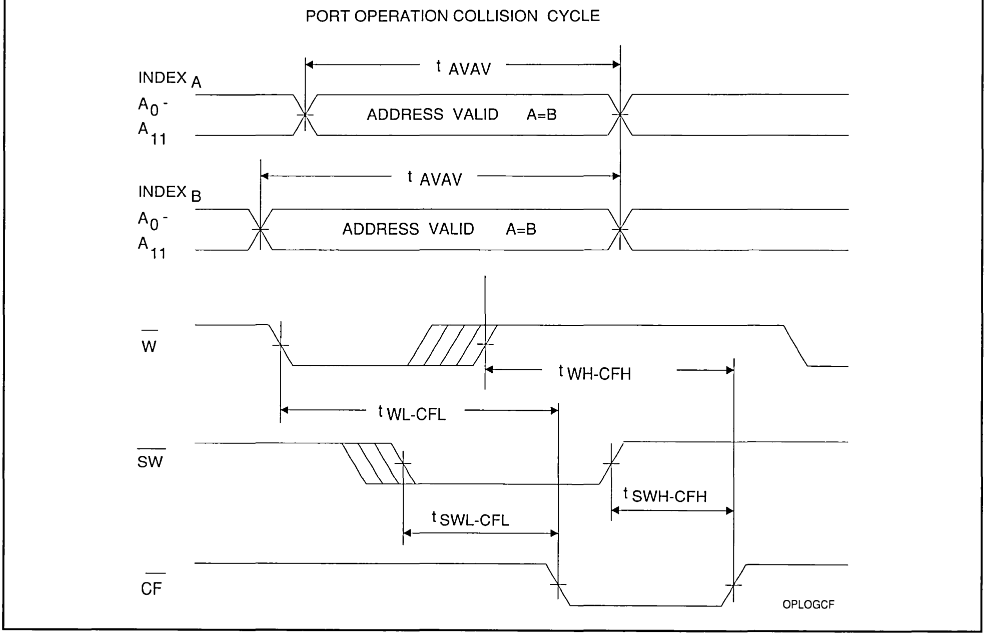
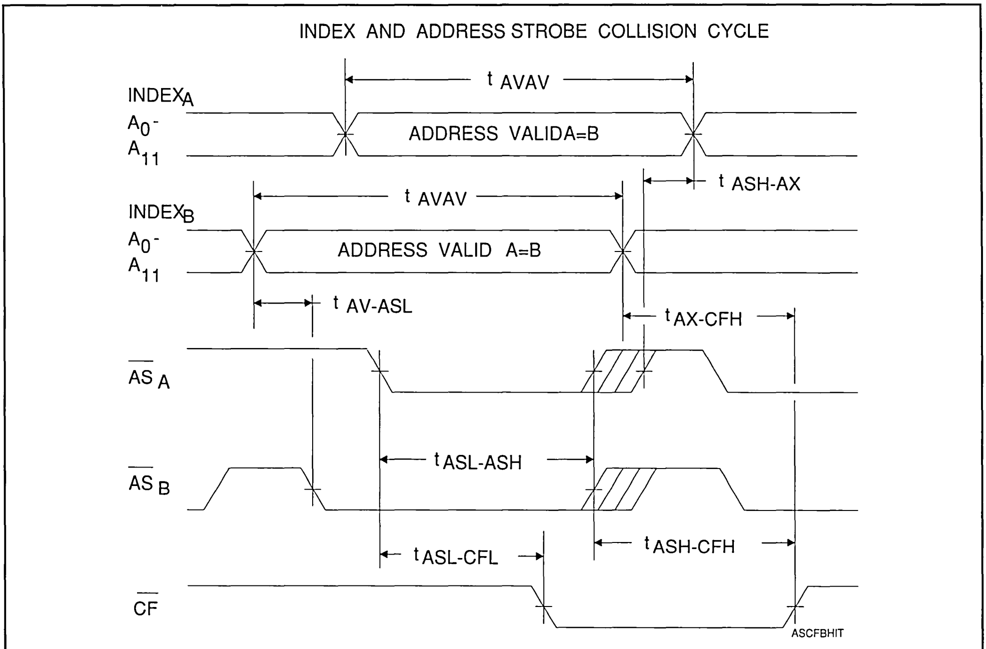
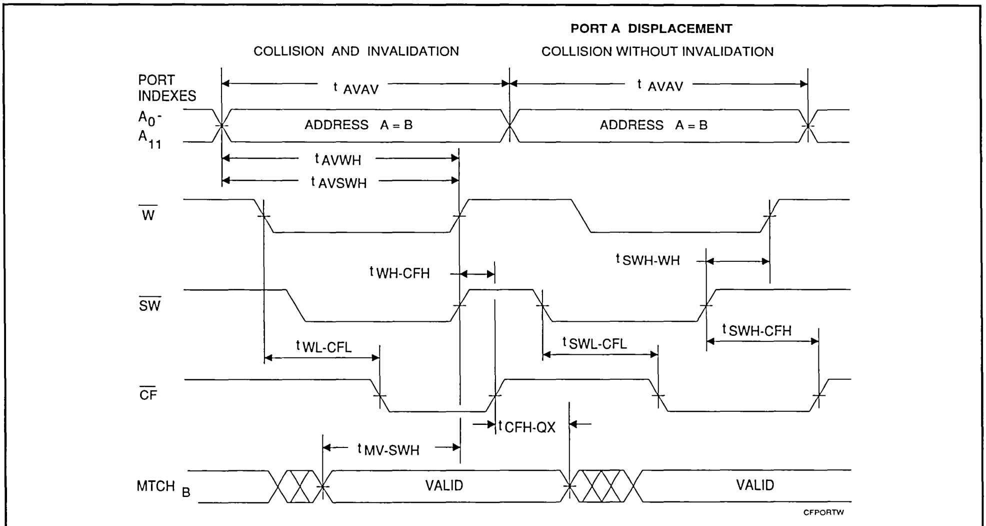

PORT OPERATION COLLISION CYCLE
INDEX A A0-A11
t AVAV
ADDRESS VALID A=B
INDEX B A0-A11
t AVAV
ADDRESS VALID A=B
W
t WH-CFH
t WL-CFL
SW
t SWH-CFH
t SWL-CFL
CF
OPLOGCF

Figure 19 : Address Collision Cycle Timing


INDEX AND ADDRESS STROBE COLLISION CYCLE
INDEXA
A0-
A11
t AVAV
ADDRESS VALIDA=B
t ASH-AX
INDEXB
A0-
A11
t AVAV
ADDRESS VALID A=B
t AV-ASL
tAX-CFH
AS A
tASL-ASH
AS B
tASL-CFL
tASH-CFH
CF
ASCFBHIT

Note : Address Enables ($\overline{E}$x) are presumed low.

Figure 20 : Collision : Snoop Invalidation Displacement


PORT A DISPLACEMENT
COLLISION AND INVALIDATION
COLLISION WITHOUT INVALIDATION
PORT INDEXES
A0-
A11
t AVAV
t AVAV
ADDRESS A = B
ADDRESS A = B
t AVWH
t AVSWH
W
t WH-CFH
t SWH-WH
SW
t WL-CFL
t SWL-CFL
t SWH-CFH
CF
t CFH-QX
t MV-SWH
MTCH B
VALID
VALID
CFPORTW

Note : Address Strobes ($\overline{AS}$x) are presumed low.

ABSOLUTE MAXIMUM RATINGS *

SYMBOL	PARAMETER	VALUE	UNIT
V_I	Voltage on any Pin Relative to Ground	–0.5 to 6	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
P_D	Power Dissipation	2.5	W
I_{OUT}	Output Current †	50	mA

*.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

† Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5	5.25	V	
GND	Ground	0	0	0	V	
V_{IH}	Logic 1 All Inputs	2.2	3	V_{CC} + 0.3	V	
V_{IL}	Logic 0 All Inputs	–0.3	0.2	0.8	V	

Note. All voltages referenced to GND. Inputs $M/\overline{S}$ and $\overline{COMP6}$ are static inputs requiring V_{IH}min = V_{CC}min, and V_{IL}max = GNDmax

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current (Both Ports)		250	mA	8,9
I_{CC2}	Active V_{CC} Power Supply Current ($\overline{Ex}$ = Low; f=0)		180	mA	9,10
I_{SB1}	CMOS Stdby Current ($\overline{Ex} \geq V_{CC}$ –0.2 V, f =0)		130	mA	11
I_{LI}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{LO}	Output Leakage Current	–5	5	µA	2
V_{OH}	Output Logic 1 Voltage (I_{OH} = –4.0mA)	2.4		V	1
V_{OL}	Output Logic 0 Voltage (I_{OL} = 8mA)		0.4	V	1
V_{OH}	MTCHA and MTCHB (I_{OH} = –12mA)	2.4		V	1
V_{OL}	MTCHA and MTCHB (I_{OL} = 18mA)		0.5	V	1

CAPACITANCE (T_A = 25°C , f = 1.0MHz)

SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance on all pins (except DQ)	6	8	pF	14
C_O	Output Capacitance	8	10	pF	3,14

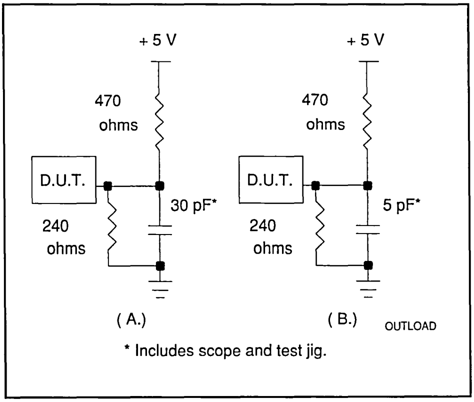
Notes :

1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC} and outputs deselected.
3. Output buffers are deselected.
4. Measured with load as shown in Figure 21A.
5. Measured with load as shown in Figure 21B.
6. Measured with load as shown in Figure 22A.
7. Measured with load as shown in Figure 22B
8. I_{CC1} measured with outputs open, V_{CC} max.
9. I_{CC1}, I_{CC2} measured in COMPARE mode.
10. I_{CC2} measured with outputs open, V_{CC} max; f=0
11. All other Inputs ≥ V_{CC}-0.2 or ≤ GND+0.2, no toggle.
12. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

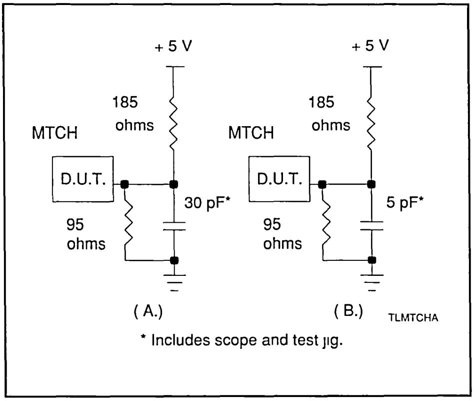
Input Levels	GND to 3V
Transition Time	1.5 ns
Input and Output Signal Timing Reference Level	1.5 Volts
Ambient Temperature	0°C to 70°C
V_{CC}	5V ± 5%

Figure 21 : Output Test Load Circuits


+ 5 V
470 ohms
D.U.T.
240 ohms
30 pF*
(A.)
+ 5 V
470 ohms
D.U.T.
240 ohms
5 pF*
(B.)
OUTLOAD

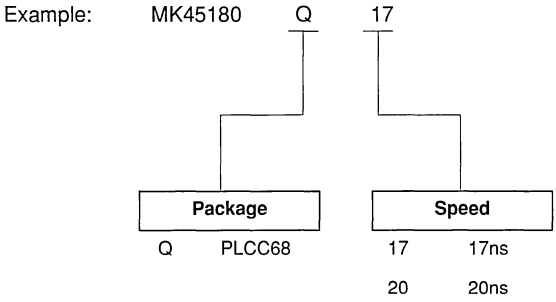
* Includes scope and test jig.

Figure 22 : Match Test Load Circuits


+ 5 V
185 ohms
MTCH
D.U.T.
95 ohms
30 pF*
(A.)
+ 5 V
185 ohms
MTCH
D.U.T.
95 ohms
5 pF*
(B.)
TLMTCHA

* Includes scope and test jig.

ORDERING INFORMATION


Example:
MK45180
Q
17
Package
Q PLCC68
Speed
17 17ns
20 20ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

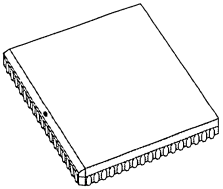
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK4202

VERY FAST CMOS 2K x 20 CACHE TAGRAM

- 2048 x 20 CMOS SRAM WITH ONBOARD COMPARATOR
- MATCH ACCESS TIME: 17, 20, 25ns
- READ ACCESS TIME: 20ns Max
- RESET CYCLE: 25ns Max
- I_{CC} (OUTPUTS DESELECTED): 250mA Max
- STANDBY: 50mA Max
- FLASH CLEAR VALID BIT FUNCTION
- TARGET APPLICATION: 68040-30, AND 80486-50 CACHE



PLCC68 (Q)

PIN NAMES

V_{CC}, GND	5 Volts, Ground
A0 - A10	Index Address Inputs
CDO0	Clearable Tag Data I/O
DQ1 - DQ19	Tag Data I/O
E0 - E3	Chip Enable (Programmable Active Low or High)
P0 - P3	Chip Enable Program Inputs
$\overline{RS}$	Reset Input (Active Low)
$\overline{S}$	Chip Select Input (Active Low)
$\overline{W}$	Write Enable (Active Low)
$\overline{G}$	Data Output Enable (Active Low)
C0	Compare 0 Output (3-State) Hit = High, Miss = Low
C1	Compare 0 Output (3-State) Hit = High, Miss = Low
$\overline{H0}$	Force Hit 0 Input (Active Low)
$\overline{H1}$	Force Hit 1 input (Active Low)
$\overline{M0}$	Force Miss 0 Input (Active Low)
$\overline{M1}$	Force Miss 1 Input (Active Low)
$\overline{CG0}$	Compare 0 Output Enable (Active Low)
$\overline{CG1}$	Compare 1 Output Enable (Active Low)

Figure 1. Logic Diagram

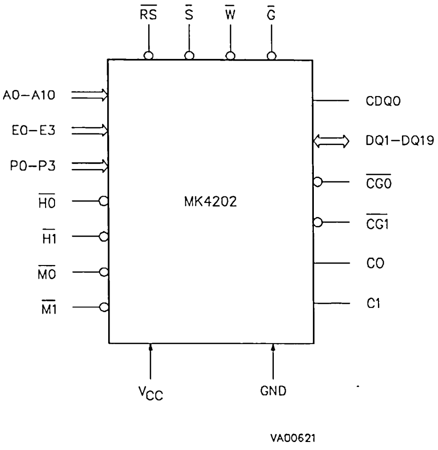
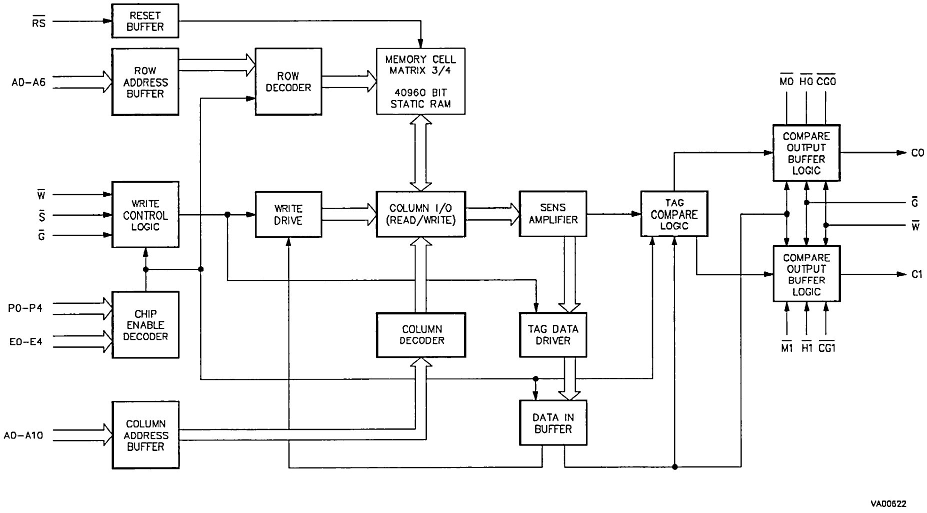


Figure 2. Block Diagram


RS
RESET BUFFER
A0-A6
ROW ADDRESS BUFFER
ROW DECODER
MEMORY CELL MATRIX 3/4
40960 BIT STATIC RAM
M0 H0 CG0
COMPARE OUTPUT BUFFER LOGIC
C0
W
S
G
WRITE CONTROL LOGIC
WRITE DRIVE
COLUMN I/O (READ/WRITE)
SENS AMPLIFIER
TAG COMPARE LOGIC
G
W
COMPARE OUTPUT BUFFER LOGIC
C1
P0-P4
E0-E4
CHIP ENABLE DECODER
COLUMN DECODER
TAG DATA DRIVER
M1 H1 CG1
A0-A10
COLUMN ADDRESS BUFFER
DATA IN BUFFER
VA00622

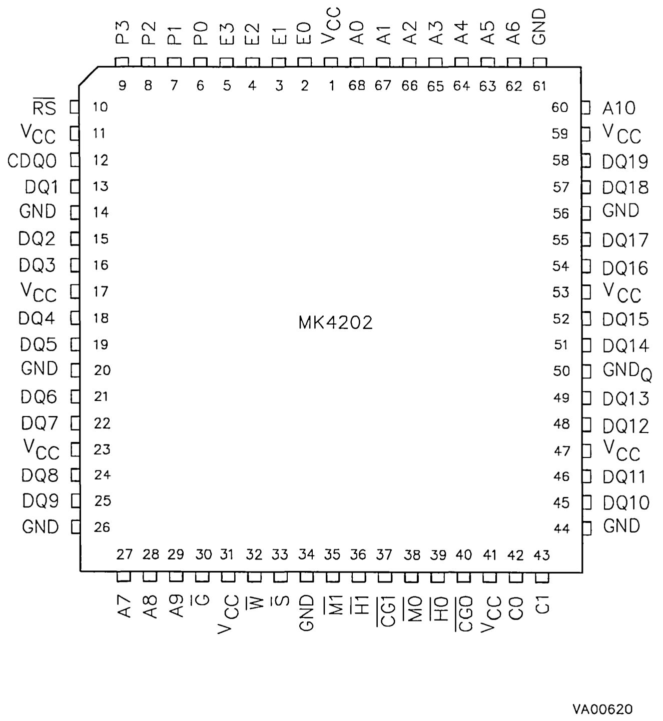
DEVICE DESCRIPTION AND FEATURES

The MK4202 is designed to be connected DIRECTLY to a high performance 32 bit microprocessor, allowing the elimination of the logic delays associated with collecting HIT or Miss outputs into a subsequent gate or the RC delays associated with wired-OR open collector match outputs.

The MK4202 TAGRAM™ has four major features that allow direct connection:

1. Wide enough for almost any TAGRAM application without requiring multiple chip width expansion and the delays that would result.
2. Four (4) programmable CHIP ENABLE inputs, allowing DEPTH EXPANSION without any of the attendant chip enable decode delays that would otherwise be required.
   P0-P3 should be tied directly to V_{CC} or Ground, or through pull-up or pull-down resistors. The MK4202 is selected when E0-E3 equals P0-P3 in a binary match.
   (Example: E0-E1 = 0110, P0-P3 = 0110.)
3. 3-STATE COMPARE OUTPUTS, allowing all Compare outputs to be bused together so the Address-to-Compare access time for a depth expanded application is identical to that of a single device. The Programmable Chip Enables prevent bus contention by assuring that only one TAGRAM at a time drives each Compare bus when in Compare mode.

Figure 3. Pin Connection


P3
P2
P1
P0
E3
E2
E1
E0
VCC
A0
A1
A2
A3
A4
A5
A6
GND
9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
$\overline{\text{RS}}$ 10
V_{CC} 11
CDQ0 12
DQ1 13
GND 14
DQ2 15
DQ3 16
V_{CC} 17
DQ4 18
DQ5 19
GND 20
DQ6 21
DQ7 22
V_{CC} 23
DQ8 24
DQ9 25
GND 26
MK4202
60 A10
59 V_{CC}
58 DQ19
57 DQ18
56 GND
55 DQ17
54 DQ16
53 V_{CC}
52 DQ15
51 DQ14
50 GND_Q
49 DQ13
48 DQ12
47 V_{CC}
46 DQ11
45 DQ10
44 GND
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
A7
A8
A9
$\overline{\text{G}}$
VCC
$\overline{\text{W}}$
$\overline{\text{S}}$
GND
$\overline{\text{M1}}$
$\overline{\text{H1}}$
$\overline{\text{CG1}}$
$\overline{\text{M0}}$
$\overline{\text{H0}}$
$\overline{\text{CG0}}$
VCC
C0
C1
VA00620

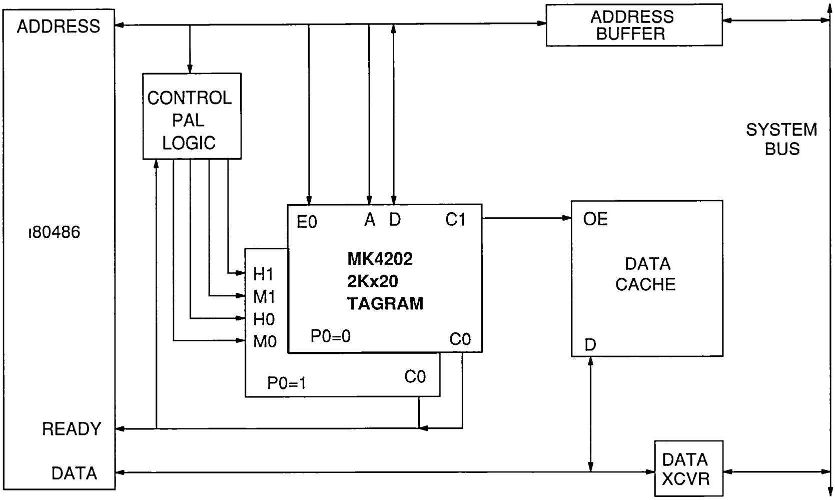
4. DUAL COMPARE OUTPUTS (C0 and C1) and FORCED HIT ($\overline{\text{H0}}$ and $\overline{\text{H1}}$) and FORCED MISS ($\overline{\text{M0}}$ and $\overline{\text{M1}}$) inputs for each. The arrangement allows direct connection of the TAGRAM to a processor input (such as the READY input on Intel based processors), and to the Output Enable (OE) on a Data CACHE bank. The connection of the signals which would have been connected to the processor inputs and/or data CACHE inputs, are PASSED THRU the MK4202 TAGRAM, thus eliminating the need for subsequent gates to collect the COMPARE OUTPUTS to develop an input to the processor and/or data CAHE. The net effect is that the Address-to-Compare access time dem-onstrated by the MK4202 is all of the delay the user must consider. The alternative approach, using narrow TAGRAMs with open collector output or narrow TAGRAMs with 2-state outputs and 7.5ns programmable logic, requires that the narrow TAGRAMs demonstrate a 9ns Address-to-Compare access time to yield the same performance in a user's system that the MK4202 provides.

POWER DISTRIBUTION

The MK4202, being a 20 output device, obviously requires the use of good power bussing techniques. MK4202 has been designed in such a way as to allow the user to minimize the effects of switching transients on overall circuit operation. Of particular interest is the separate bussing of the V_{CC} and GND lines to the output drivers. The advantage provided by these separate power pins is that voltage sags and ground bumps seen on these pins are not reflected into the other portions of the chip, particu-larly the input structures. As a result, switching noise in the supply has much less effect on input levels, providing the user with more noise margin than would otherwise be available.

Of course all V_{CC} and GND pins must always be at the same DC potential. Differences between them due to AC effects are expected, but must be minimized through the adequate use of bussing and bypassing. All specifications and testing are done with GND ± 10mV RMS, V_{CC} = ± 10mV RMS with instantaneous peak differences not exceeding 50mV.

Figure 4. Application Block Schematic


ADDRESS
ı80486
READY
DATA
CONTROL
PAL
LOGIC
ADDRESS
BUFFER
SYSTEM
BUS
E0
A
D
C1
MK4202
2Kx20
TAGRAM
H1
M1
H0
M0
P0=0
C0
P0=1
C0
OE
DATA
CACHE
D
DATA
XCVR

TRUTH TABLE

$\overline{\text{RS}}$	$\overline{\text{S}}$	E	$\overline{\text{W}}$	$\overline{\text{G}}$	$\overline{\text{M0}}, \overline{\text{M1}}$	$\overline{\text{H0}}, \overline{\text{H1}}$	$\overline{\text{CG0}}, \overline{\text{CG1}}$	MODE	C0, C1	DQ	NOTES
Hi	–	X	–	–	Lo	X	X	Force Miss	Low	–	1
Hi	–	X	–	–	Hi	Lo	X	Force Hit	High	–	1
Hi	–	X	–	–	HI	Hi	Hi	Comp Disable	Hi-Z	–	1
Hi	X	F	X	X	Hi	Hi	X	Standby	Hi-Z	Hi-Z	
Hi	X	T	Hi	Hi	Hi	Hi	Hi	Compare	Hi-Z	D in	
Hi	X	T	Hi	Hi	Hi	Hi	Lo	Compare	Hi/Lo	D in	
Hi	Hi	T	Lo	X	Hi	Hi	Lo	Hit	Hi	Hi-Z	
Hi	Hi	T	X	Lo	Hi	Hi	Lo	Hit	Hi	Hi-Z	
Hi	Lo	T	Lo	X	Hi	Hi	Lo	Write	Hi	D in	
Hi	Lo	T	Hi	Lo	Hi	Hi	Lo	Read	Hi	D Out	
Lo	Hi	X	X	X	–	–	–	Reset	–	Hi-Z	
Lo	X	F	X	X	–	–	–	Reset	–	Hi-Z	
Lo	X	X	Hi	Hi	–	–	–	Reset	–	Hi-Z	
Lo	X	X	Hi	Lo	–	–	–	Reset	–	Lo-Z	
Lo	Lo	T	Lo	X	–	–	–	Not Allowed	–	Hi-Z	2
Lo	X	T	Hi	Hi	Hi	Hi	Lo	Reset	Lo	D in	3

Notes:
1. Force hit/miss operations independent of other RAM operations.
2. May disrupt Reset, will not damage device
3. Reset will force C0 and C1 low during a valid compare when CDQ0 is D_{IN}= HIGH.

Key: X = Don't Care
F = (False) E0-E3 pattern DOES NOT match P0-P3 pattern.
T = (True) E0-E3 pattern DOES match P0-P3 pattern
– = Not related to identified mode of operation

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	–0.3 to 7.0	V
T_A	Ambient Operating Temperature (T_A)	0 to 70	°C
T_{STG}	Ambient Storage Temperature (plastic)	–55 to 125	°C
P_D	Total Device Power Dissipation	2.5	W
I_{OUT}	RMS Output Current per Pin	25	mA

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
I_{CC}	Average Power Supply Current			250	mA	1
I_{CCA}	Active Power Supply Current (f = 0)			200	mA	1
I_{SB1}	TTL Standby Current			50	mA	1
I_{IL}	Input Leakage Current			±1	µA	2
I_{OL}	Output Leakage Current			±10	µA	3
V_{IL}	Input Low Voltage	–0.3		0.8	V	4
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V	4,5
V_{OH}	Logic 1 Output Voltage (I_{OUT} = –4mA)	2.4			V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8mA)			0.4	V	4

Notes :

1. Measured with outputs open. V_{CC} max.
2 Measured with V_{IN} = 0V to V_{CC}.
3 Measured at CDQ0, DQ1-DQ19, C0 and C1
4. All voltages referenced to GND.
5. Inputs (P0-P3) require V_{IH} min. = 4 5 volts and V_{IL} max. = 0.5 volts.
6. Sampled, not 100% tested. Measured at 1 MHz.
7. Measured at all data I/O's, C0 and C1.

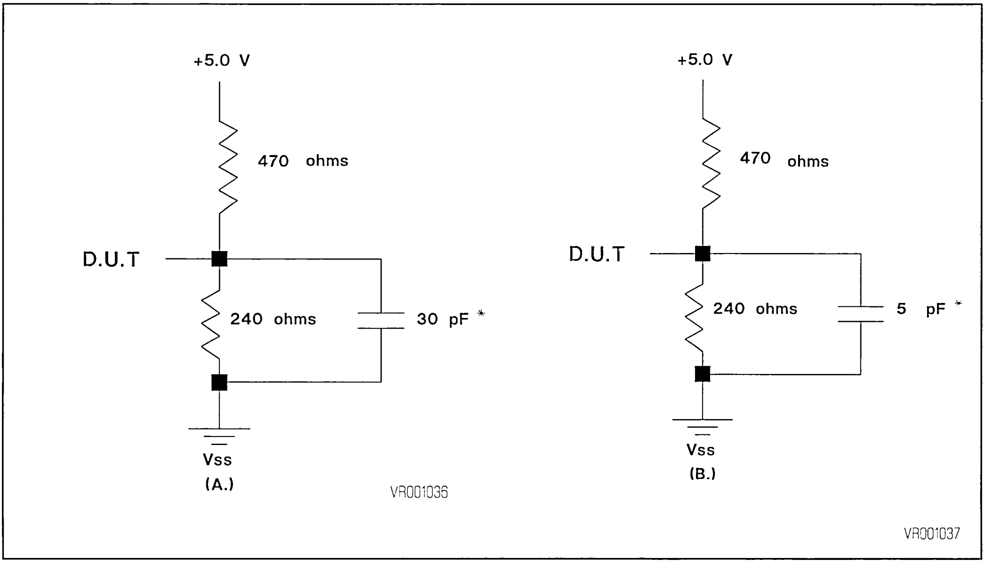
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
C_1	Input Capacitance	4		4	pF	6
C_0	Output Capacitance	8		10	pF	6.7

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	5	ns
Input and Output Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 5. Equivalent Output Load Circuits



READ MODE

The MK4202 is in the Read mode whenever $\overline{W}$ is HIGH, and $\overline{G}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E0-E3) is applied. The 11 address inputs (A0-A10) define a unique index address giving access to 20 of 40,960 bits of data in the static memory array. Valid data will be present at the 20 output pins within t_{AVQV} of the last stable address provided Chip Enable, Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) access times have been met. If Chip Enable, $\overline{S}$, or $\overline{G}$ access times are not met, data access will be measured from the latter falling edge or limiting parameter (t_{EVQV}, t_{SLQV}, or t_{GLQV}). The state of the tag data I/O pins is controlled by the (E0-E3), $\overline{S}$, $\overline{G}$, and $\overline{W}$ input pins. The data lines may be indeterminate at t_{EVQX}, or t_{SLQX}, or t_{GLQX}, but will always have valid data at t_{AVQV}.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Read Cycle Timing) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 5%)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	20		25		30		ns	
t_{AVQV}	t_{AA}	Address Access Time		20		25		30	ns	
t_{AXQX}	t_{AOH}	Address Output Hold Time	5		5		5		ns	
t_{AEQV}	t_{EA}	Chip Enable Access Time		20		25		30	ns	
t_{EXQX}	t_{EOH}	Chip Enable Output Hold Time	4		4		4		ns	
t_{EVQX}	t_{ELZ}	Chip Enable TRUE to Low-Z	4		4		4		ns	
t_{EXQZ}	t_{EHZ}	Chip Enable FALSE to high-Z		8		8		10	ns	
t_{SLQV}	t_{SA}	Chip Select Access Time		12		15		18	ns	
t_{SHQX}	t_{SOH}	Chip Select Output Hold Time	2		2		2		ns	
t_{SLQX}	t_{SLZ}	Chip Select to Low-Z	3		3		3		ns	
t_{SHQZ}	t_{SHZ}	Chip Select to High-Z		4		4		6	ns	
t_{GLQV}	t_{GA}	Output Enable Access Time		10		13		15	ns	
t_{GHQX}	t_{GOH}	Output Enable Output Hold Time	2		2		2		ns	
t_{GLQX}	t_{GLZ}	Output Enable to Low-Z	2		2		2		ns	
t_{GHQZ}	t_{GHZ}	Output Enable to High-Z		5		5		8	ns	

Figure 6. Read Cycle

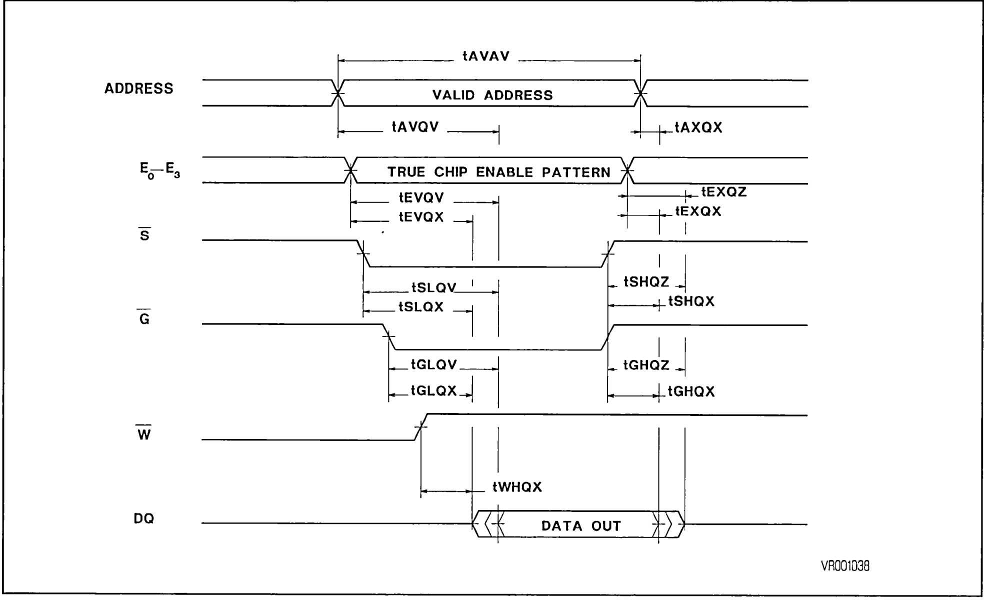

tAVAV
ADDRESS
VALID ADDRESS
tAVQV
tAXQX
E0–E3
TRUE CHIP ENABLE PATTERN
tEVQV
tEXQZ
tEVQX
tEXQX
$\overline{S}$
tSLQV
tSHQZ
tSLQX
tSHQX
$\overline{G}$
tGLQV
tGHQZ
tGLQX
tGHQX
$\overline{W}$
tWHQX
DQ
DATA OUT
VR001038

Figure 7. Address Read Cycle

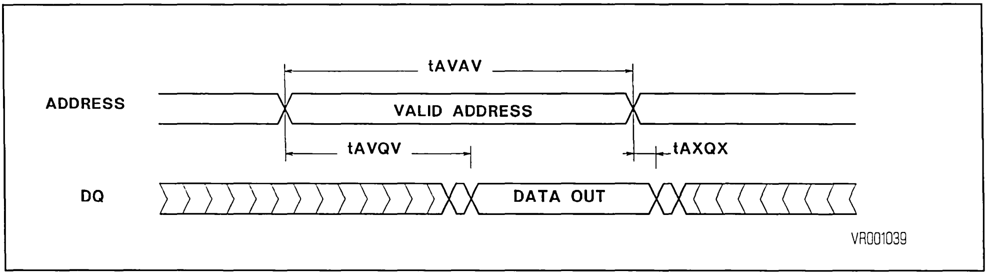

tAVAV
ADDRESS
VALID ADDRESS
tAVQV
tAXQX
DQ
DATA OUT
VR001039

Figure 8. Chip Enable Read Cycle

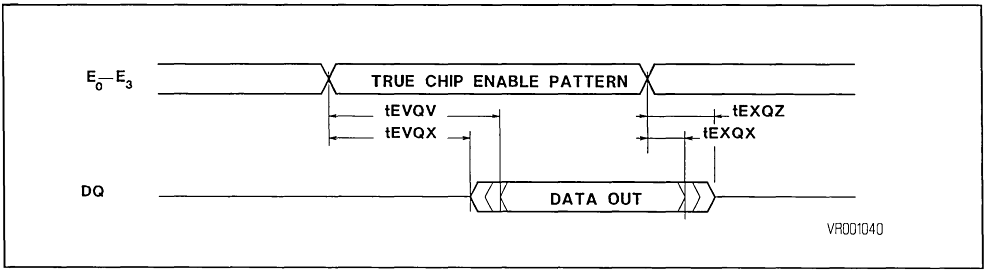

E0—E3
TRUE CHIP ENABLE PATTERN
tEVQV
tEVQX
tEXQZ
tEXQX
DQ
DATA OUT
VR001040

Figure 9. Chip Select Read Cycle

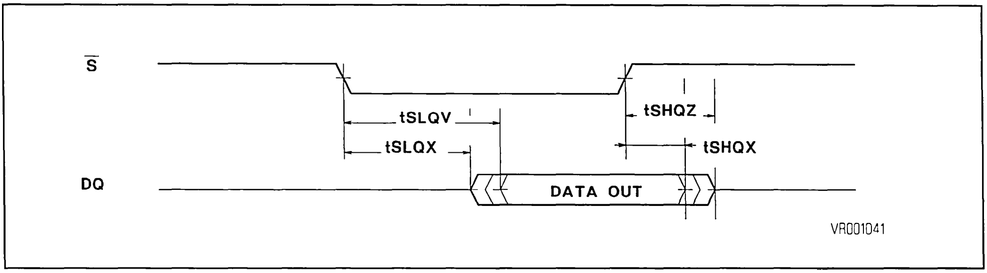
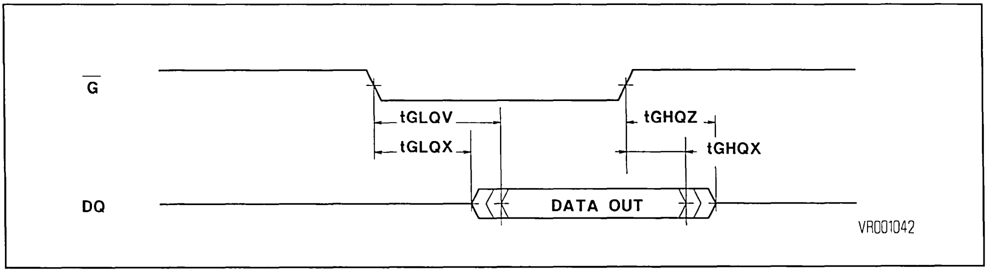

S
tSLQV
tSLQX
tSHQZ
tSHQX
DQ
DATA OUT
VR001041

Figure 10. Output Enable Read Cycle


G
tGLQV
tGLQX
tGHQZ
tGHQX
DQ
DATA OUT
VR001042

WRITE MODE

The MK4202 is in the Write mode whenever $\overline{W}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E0-E3) is applied ($\overline{G}$ may be in either logic state). Addresses must be held valid throughout a write cycle, with either $\overline{W}$ or $\overline{S}$ inactive HIGH during address transitions. $\overline{W}$ may fall with stable addresses, but must remain valid for t_{WLWH}.

Since the write begins with the concurrence of $\overline{W}$ and $\overline{S}$, should $\overline{W}$ become active first, then t_{SLSH} must be satisfied. Either $\overline{W}$ or $\overline{S}$ can terminate the write cycle, therefore t_{DVWH} or t_{DVSH} must be satisfied before the earlier rising edge, and t_{WHDX} or t_{SHDX} after the earlier rising edge. If the outputs are active with $\overline{G}$ and $\overline{S}$ asserted LOW and with true Chip Enable, then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Write Cycle Timing) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 5%)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_C	Cycle Time	20		25		30		ns	
t_{AVWL}	t_{AS}	Address Set-up Time to $\overline{W}$ LOW	0		0		0		ns	
t_{WHAX}	t_{AH}	Address Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up Time from $\overline{S}$ LOW	0		0		0		ns	
t_{SHAX}	t_{AH}	Address Hold Time from $\overline{S}$ HIGH	0		0		0		ns	
t_{EVWL}	t_{ES}	Chip Enable Set-up Time to $\overline{W}$ LOW	3		3		3		ns	
t_{WHEX}	t_{EH}	Chip Enable Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{EVSL}	t_{ES}	Chip Enable Set-up Time to $\overline{S}$ LOW	3		3		3		ns	
t_{SHEX}	t_{EH}	Chip Enable Hold time to $\overline{S}$ HIGH	0		0		0		ns	
t_{WLWH}	t_{WW}	Write Pulse Width	12		15		18		ns	
t_{SLSH}	t_{SW}	Chip Select Pulse Width	16		16		20		ns	
t_{DVWH}	t_{DS}	Data Set-up Time to $\overline{W}$ HIGH	12		12		15		ns	
t_{WHDX}	t_{DH}	Data Hold Time from $\overline{W}$ HIGH	0		0		0		ns	
t_{DVSH}	t_{DS}	Data Set-up Time to $\overline{S}$ HIGH	12		12		15		ns	
t_{SHDX}	t_{DH}	Data Set-up Time to $\overline{S}$ HIGH	0		0		0		ns	
t_{WLQZ}	t_{WZ}	Outputs Hi-Z from $\overline{W}$ LOW		8		8		10	ns	
t_{WHQX}	t_{WL}	Outputs Low-Z from $\overline{W}$ HIGH	5		5		5		ns	

Figure 11. $\overline{W}$ Write Cycle

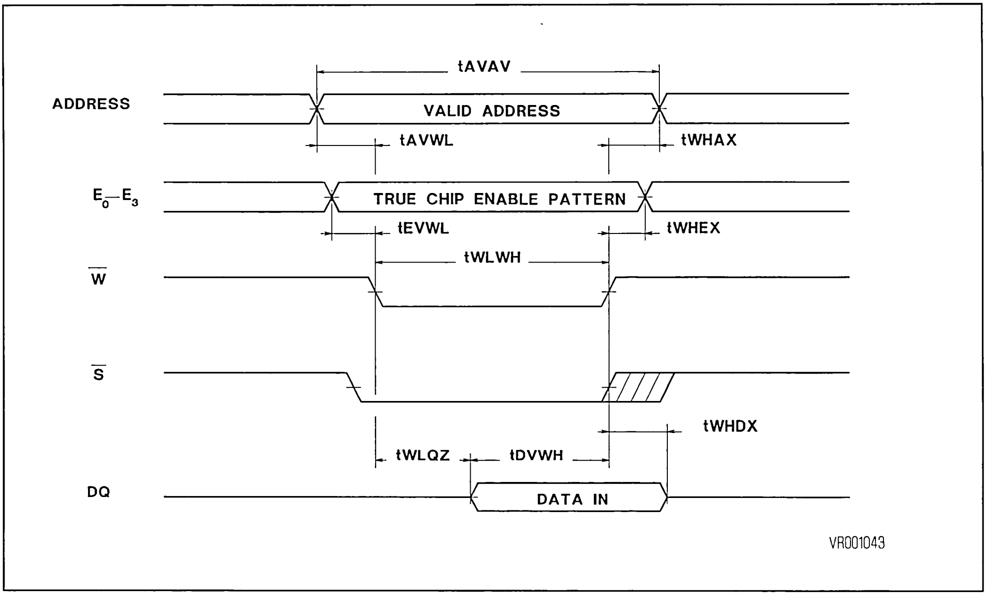
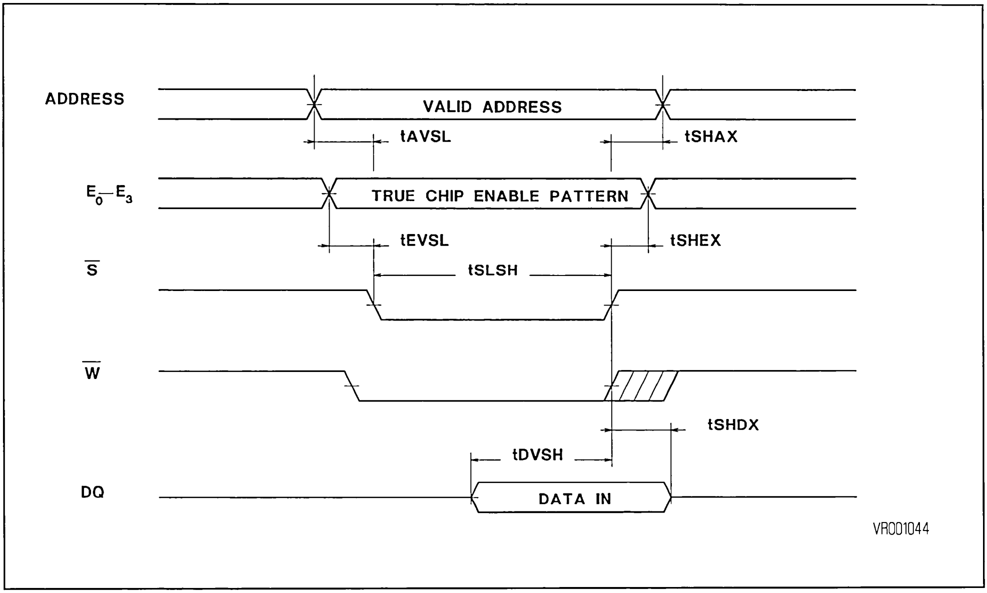

tAVAV
ADDRESS
VALID ADDRESS
tAVWL
tWHAX
E0—E3
TRUE CHIP ENABLE PATTERN
tEVWL
tWHEX
tWLWH
W
S
tWHDX
tWLQZ
tDVWH
DQ
DATA IN
VR001043

Figure 12. $\overline{S}$ Write Cycle


ADDRESS
VALID ADDRESS
tAVSL
tSHAX
E0—E3
TRUE CHIP ENABLE PATTERN
tEVSL
tSHEX
S
tSLSH
W
tSHDX
tDVSH
DQ
DATA IN
VR001044

COMPARE MODE

The MK4202 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided a true Chip Enable (E0-E3) pattern is applied. Chip Select ($\overline{S}$) is reguarded as a don't care since the user is not concerned with the data outputs, but only with the Compare (C0, C1) outputs. $\overline{Mx}$ and $\overline{Hx}$ must be HIGH, and $\overline{CG0}$, $\overline{CG1}$ active LOW to enable the Compare outputs for a valid compare hit or miss.

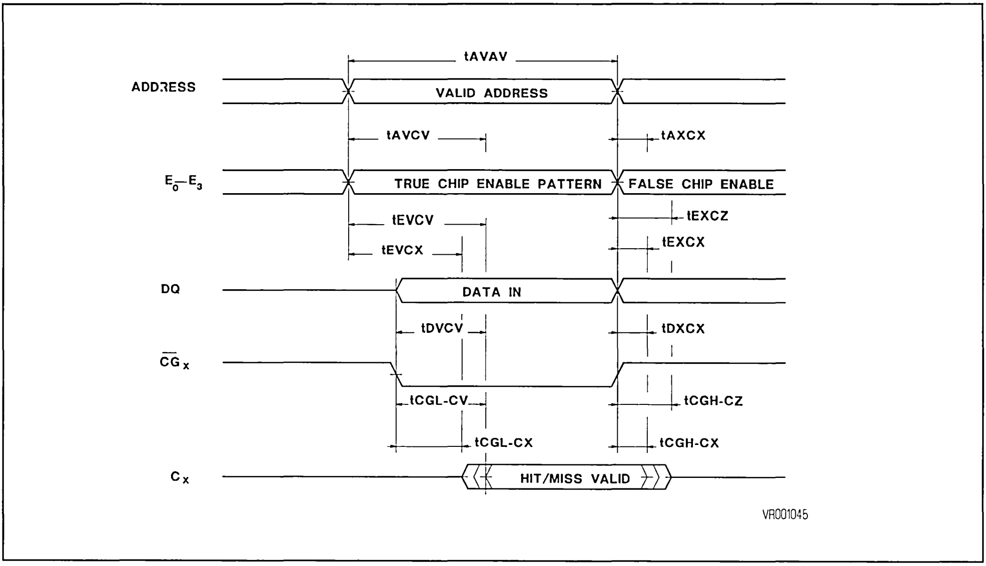
The 11 index address inputs (A0-A10) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ1-DQ19 and CDQ0) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (C0 and C1 = HIGH). If at least one bit is not equal, then a miss occurs (C0 and C1 = LOW).

The Compare output will be valid t_{AVCV} from stable address, or t_{DVCV} from valid tag data provided Chip Enable is true, and $\overline{CGx}$ is active LOW. Should the address be stable with valid tag data, and Chip Enable false, then compare access will be within t_{EVCV} from true Chip Enable. When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH), C0 and C1 will be valid t_{WHCV} or t_{GHCV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively. Finally, when gating the Cx output in the compare mode with $\overline{CGx}$, the compare output will be valid $t_{CGL\text{-}CV}$ from the falling edge of $\overline{CGx}$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Compare Cycle Timing) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 5%)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVCV}	t_{ACA}	Address Compare Access Time		17		20		25	ns	
t_{AXCX}	t_{ACOH}	Address Compare Output Hold Time	5		5		5		ns	
t_{DVCV}	t_{DCA}	Tag Data Compare Access Time		14		16		20	ns	
t_{DXCX}	t_{DCH}	Tag Data Compare Hold Time	2		2		2		ns	
t_{WLCH}	t_{WCH}	$\overline{W}$ LOW to Compare HIGH		10		10		12	ns	
t_{WHCX}	t_{WCOH}	$\overline{W}$ Compare Output hold Time	1		1		1		ns	
t_{WLCX}	t_{WLCZ}	$\overline{W}$ to Compare HOLD	3		3		3		ns	
t_{WHCV}	t_{WCV}	$\overline{W}$ to Compare Valid		10		10		12	ns	
t_{GLCH}	t_{GCH}	$\overline{G}$ Low to Compare HIGH		10		10		12	ns	
t_{GHCX}	t_{CGOH}	$\overline{G}$ Compare Output Hold Time	1		1		1		ns	
t_{GLCX}	t_{GLCZ}	$\overline{G}$ to Compare to HOLD	3		3		3		ns	
t_{GHCV}	t_{GCV}	$\overline{G}$ to Compare Valid		10		10		12	ns	
t_{EVCV}	t_{ECA}	E True to Compare Access Time		17		20		25	ns	
t_{EXCX}	t_{ECOH}	E False Compare Hold Time	4		4		4		ns	
t_{EVCX}	t_{ECLZ}	E True to Compare Low-Z	4		4		4		ns	
t_{EXCZ}	t_{ECHZ}	E False to Compare High-Z		8		8		10	ns	
$t_{CGL\text{-}CV}$	t_{CGA}	$\overline{CGx}$ to Compare Access Time		6		8		10	ns	
$t_{CGH\text{-}CX}$	t_{CGOH}	$\overline{CGx}$ Compare Hold Time	2		2		2		ns	
$t_{CGL\text{-}CX}$	t_{CGLZ}	$\overline{CGx}$ LOW to Compare Low-Z	2		2		2		ns	
$t_{CGH\text{-}CZ}$	t_{CGHZ}	$\overline{CGx}$ HIGH to Compare High-Z		8		8		10	ns	

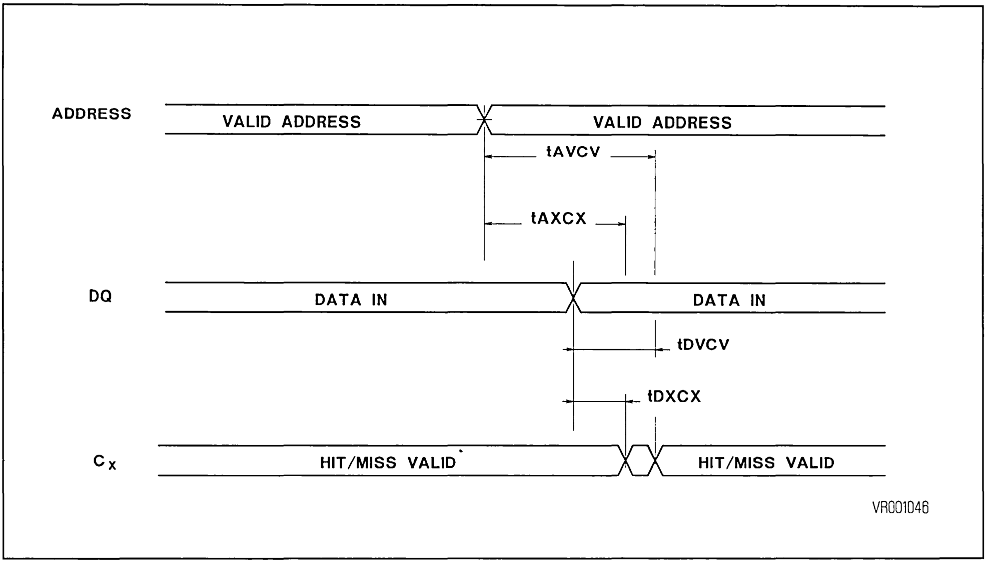
Figure 12. Summary Compare Cycle


tAVAV
ADDRESS
VALID ADDRESS
tAVCV
tAXCX
E_0–E_3
TRUE CHIP ENABLE PATTERN
FALSE CHIP ENABLE
tEVCV
tEXCZ
tEVCX
tEXCX
DQ
DATA IN
tDVCV
tDXCX
$\overline{CG}_X$
tCGL-CV
tCGH-CZ
tCGL-CX
tCGH-CX
C_X
HIT/MISS VALID
VR001045

Notes :

1. $\overline{W}$ and $\overline{G}$ are both assumed to be HIGH.
2. $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH.

Figure 13. Compare Cycle


ADDRESS
VALID ADDRESS
VALID ADDRESS
tAVCV
tAXCX
DQ
DATA IN
DATA IN
tDVCV
tDXCX
C_X
HIT/MISS VALID
HIT/MISS VALID
VR001046

Notes :

1. $\overline{W}$ and $\overline{G}$ are both HIGH, $\overline{CGx}$ is LOW and a true Chip Enable pattern is present.
2. $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH.

RESET MODE

The MK4202 allows an asynchronous reset whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits in CDQ0 (2048 bits) to a logic zero. This output can be used as a valid tag bit to insure a valid compare miss or hit . It should be noted that a valid write cycle is not allowed during a reset cycle ($\overline{W}$ = LOW, $\overline{S}$ = LOW, $\overline{RS}$ = LOW, and Chip Enable is true). The state of the data outputs is determined by the input control logic pins : Chip Enable, $\overline{S}$, $\overline{G}$, and $\overline{W}$ (see truth table). Should a reset occur during a valid compare cycle, and the CDQ_0 valid tag bit is set to a logic "1", then $\overline{C_X}$ will go LOW at t_{RSL-CL} from the falling edge of $\overline{RS}$.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Reset Cycle Timing) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RLSL-AV}$	t_{RSC}	Reset Cycle Time	20		25		30		ns	
$t_{RSL-RSH}$	t_{RSW}	Reset pulse Width	20		25		30		ns	
t_{RSL-CL}	t_{RSCL}	$\overline{RS}$ LOW to Compare Output LOW		20		25		30	ns	
t_{RSH-AV}	t_{RSR}	Address Recovery Time	0		0		0		ns	
t_{RSH-EV}	t_{RSR}	Chip Enable Recovery Time	0		0		0		ns	

FORCE HIT AND FORCE MISS

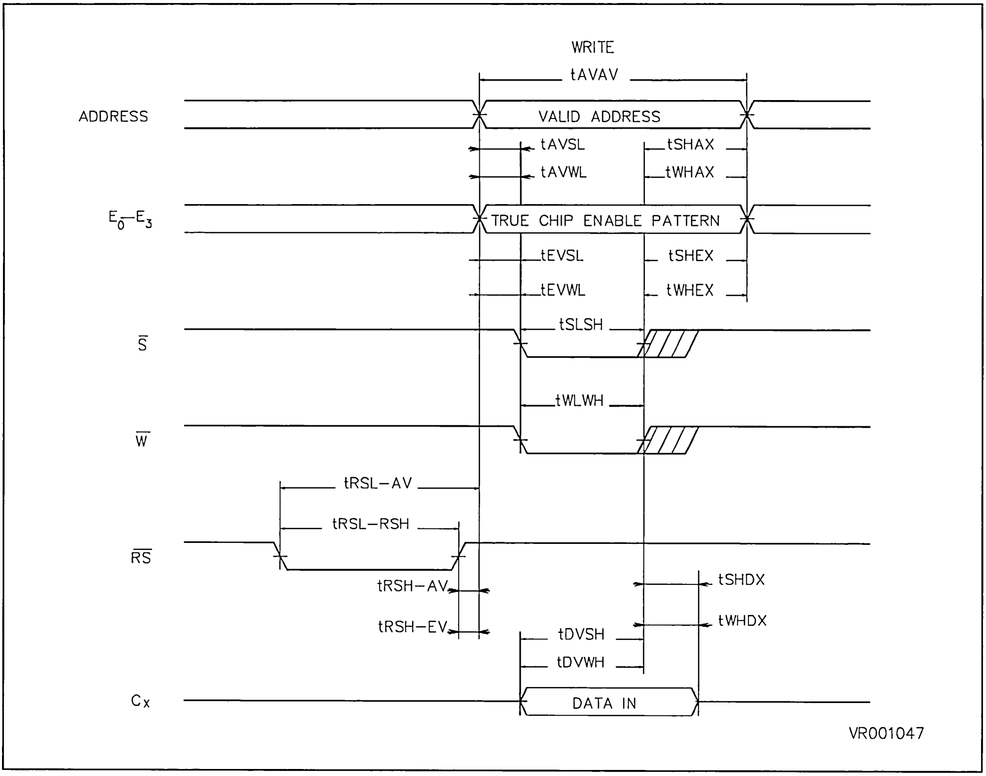
The MK4202 can force either a miss or hit condition on the C0 and C1 outputs by asserting $\overline{M0}$, $\overline{M1}$ or $\overline{H0}$, $\overline{H1}$ LOW. A Force Miss overrides a Force Hit condition and is not dependent upon Compare Output Enables ($\overline{CGx}$) (see truth table). The C0 and C1 outputs will go HIGH within t_{HLCH} from the falling edge of $\overline{H0}$, $\overline{H1}$ or C0 and C1 will go LOW within t_{MLCL} from the falling edge of $\overline{M0}$, $\overline{M1}$. All $\overline{M0}$, $\overline{M1}$ and $\overline{H0}$, $\overline{H1}$ inputs must be HIGH during a valid compare cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Force Hit or Miss Cycle Timing) ($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 10\%$)

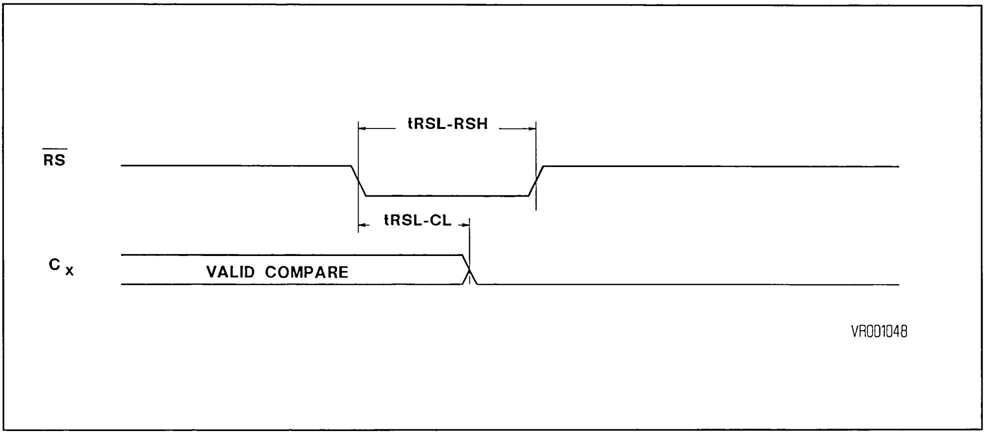
Symbol		Parameter	-17		-20		-25		Unit	Note
STD	ALT		Min.	Max.	Min.	Max.	Min.	Max.		
t_{HLCH}	t_{HA}	$\overline{Hx}$ to Force Hit Access Time		8		8		10	ns	
t_{HHCZ}	t_{HHZ}	$\overline{Hx}$ to Compare High-Z		5		5		8	ns	
t_{HL-CGX}	t_{HS}	Force Hit to $\overline{CGx}$ Don't Care	2		2		2		ns	
t_{HH-CGH}	t_{HR}	Force Hit to $\overline{CGx}$ Recognized	2		2		2		ns	
t_{MLCL}	t_{MA}	$\overline{Mx}$ to Force Miss Access Time		8		8		10	ns	
t_{MHCZ}	t_{MHZ}	$\overline{Mx}$ to Compare to High-Z		5		5		8	ns	
t_{ML-CGX}	t_{MS}	Force Miss to $\overline{CGx}$ Don't Care	2		2		2		ns	
t_{MH-CGH}	t_{MR}	Force Miss to $\overline{CGx}$ Recognized	2		2		2		ns	
t_{MLHX}	t_{MHS}	Force Miss to $\overline{Hx}$ Don't Care	2		2		2		ns	
t_{MHHH}	t_{MHR}	Force Miss to $\overline{Hx}$ Recognized	2		2		2		ns	

Figure 14. Reset Cycle


WRITE
tAVAV
ADDRESS
VALID ADDRESS
tAVSL
tSHAX
tAVWL
tWHAX
E0–E3
TRUE CHIP ENABLE PATTERN
tEVSL
tSHEX
tEVWL
tWHEX
S
tSLSH
tWLWH
W
tRSL–AV
tRSL–RSH
RS
tRSH–AV
tSHDX
tRSH–EV
tWHDX
tDVSH
tDVWH
Cx
DATA IN
VR001047

Note : Reset during an active write cycle is not allowed. A write cycle may disrupt Reset, but will not damage devcie.

Figure 15. Valid Compare - Reset


tRSL-RSH
RS
tRSL-CL
Cx
VALID COMPARE
VR001048

Note : CDQ0 is presumed to be HIGH.

Figure 16. Force Hit Force Miss

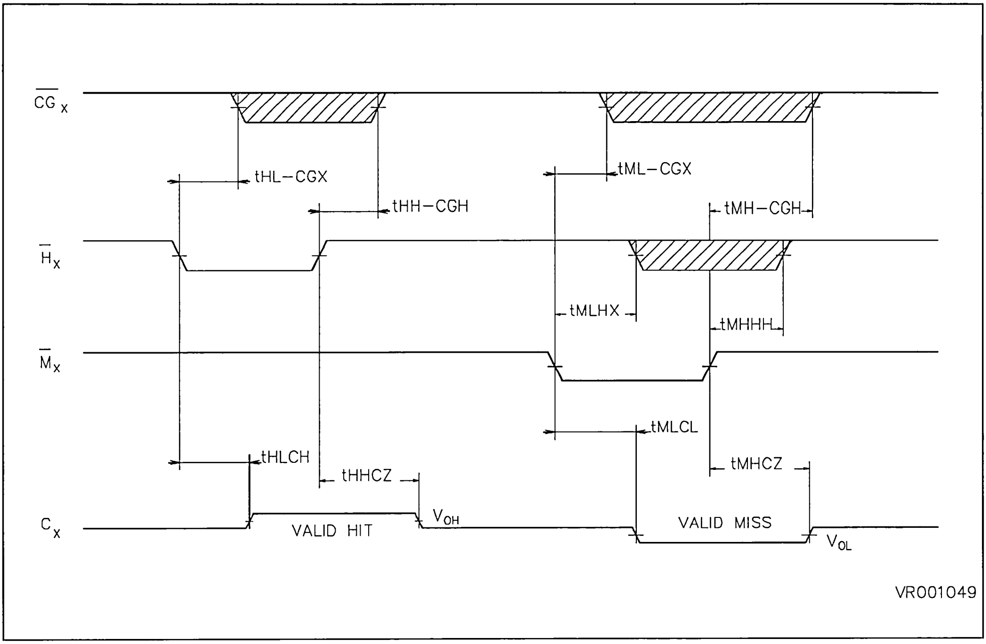
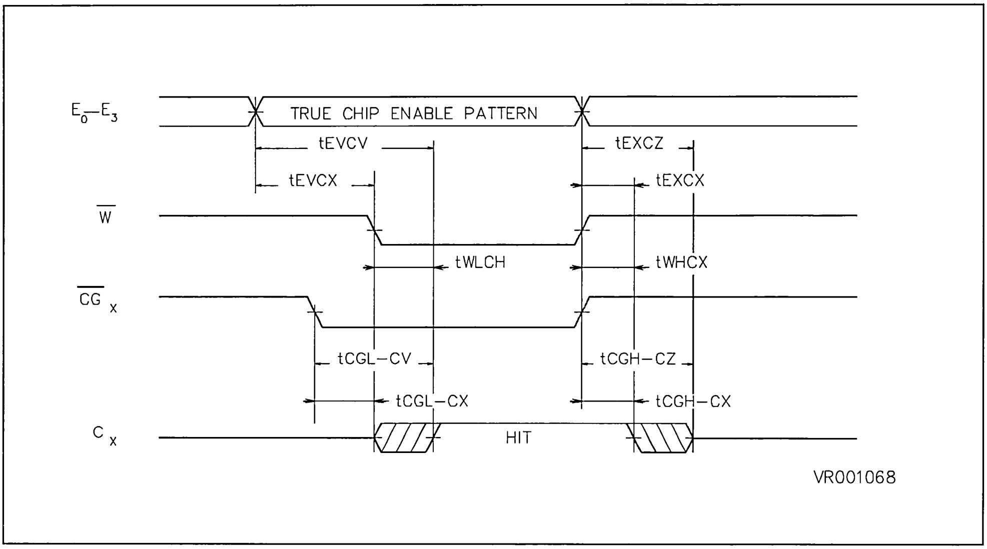
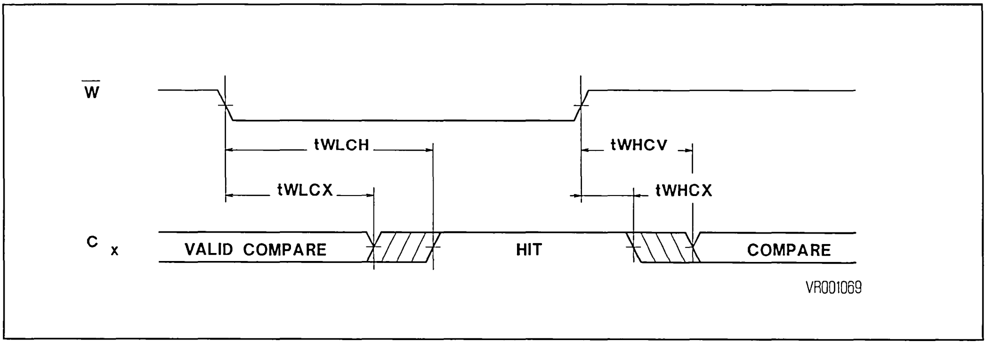

CGX
tHL-CGX
tML-CGX
tHH-CGH
tMH-CGH
HX
tMLHX
tMHHH
MX
tMLCL
tHLCH
tHHCZ
tMHCZ
CX
VALID HIT
VOH
VALID MISS
VOL
VR001049

Figure 17. Late Write - Hit Cycle


E0–E3
TRUE CHIP ENABLE PATTERN
tEVCV
tEXCZ
tEVCX
tEXCX
W
tWLCH
tWHCX
CGX
tCGL-CV
tCGH-CZ
tCGL-CX
tCGH-CX
CX
HIT
VR001068

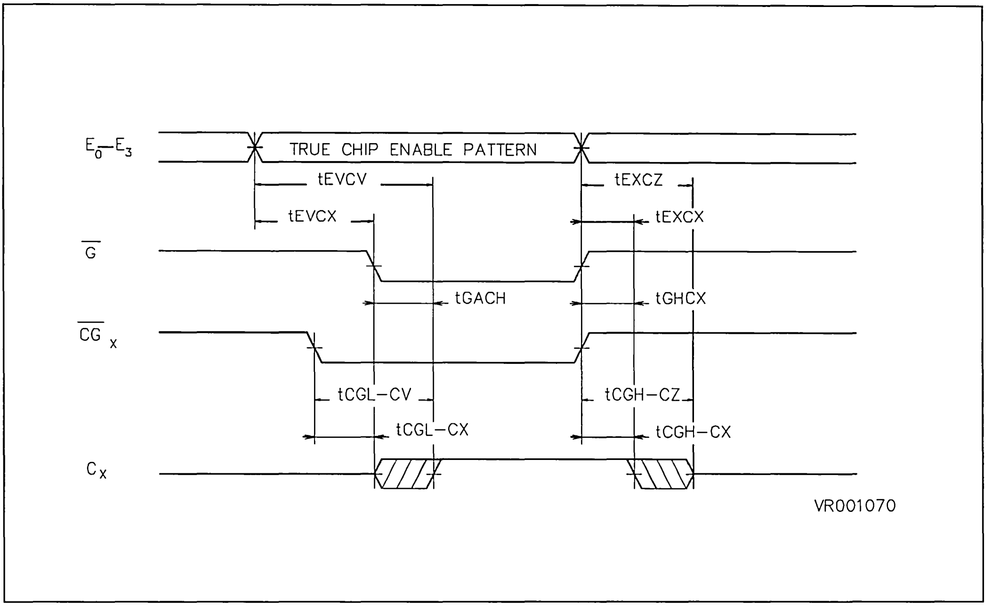
Note : $\overline{G}$ is HIGH and a Valid Address is present, $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH, with $\overline{CGx}$ LOW.

Figure 18. Compare - Write Hit - Compare Cycle


W
tWLCH
tWHCV
tWLCX
tWHCX
C x
VALID COMPARE
HIT
COMPARE
VR001069

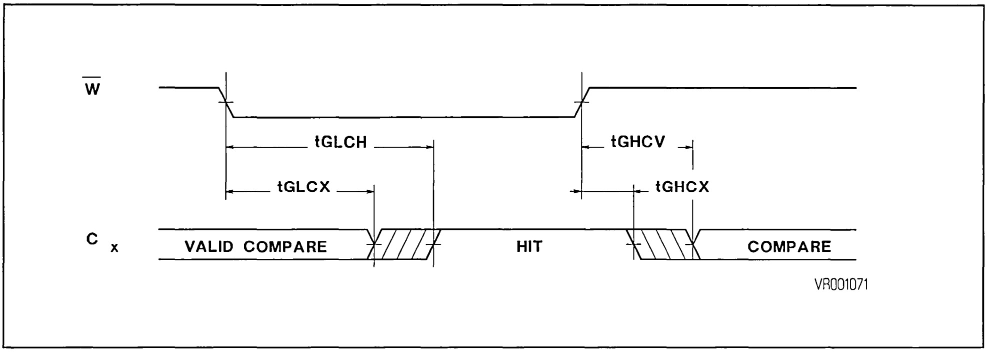
Note : $\overline{G}$ is HIGH and a Valid Address is present, $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH, with $\overline{CGx}$ LOW.

Figure 19. Late Read - Hit Cycle


E0–E3
TRUE CHIP ENABLE PATTERN
tEVCV
tEXCZ
tEVCX
tEXCX
G
tGACH
tGHCX
CG x
tCGL–CV
tCGH–CZ
tCGL–CX
tCGH–CX
Cx
VR001070

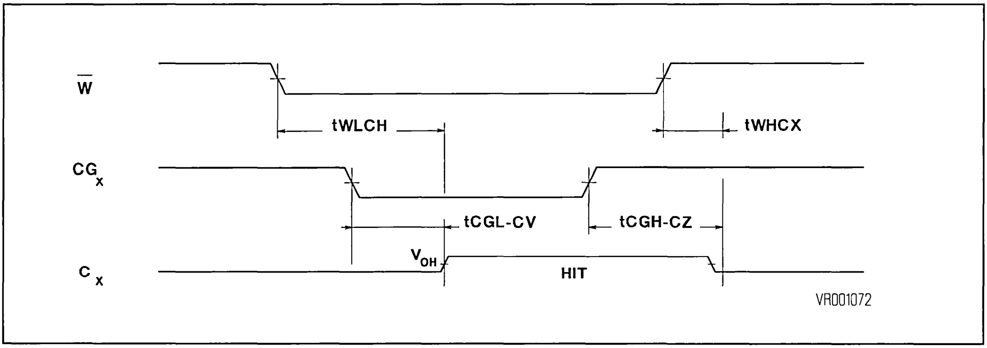
Note : $\overline{G}$ is HIGH and a Valid Address is present, $\overline{Hx}$ and $\overline{Mx}$ are both assumed to be HIGH, with $\overline{CGx}$ LOW.

Figure 20. Compare - Read Hit - Compare Cycle


W
tGLCH
tGHCV
tGLCX
tGHCX
C x
VALID COMPARE
HIT
COMPARE
VR001071

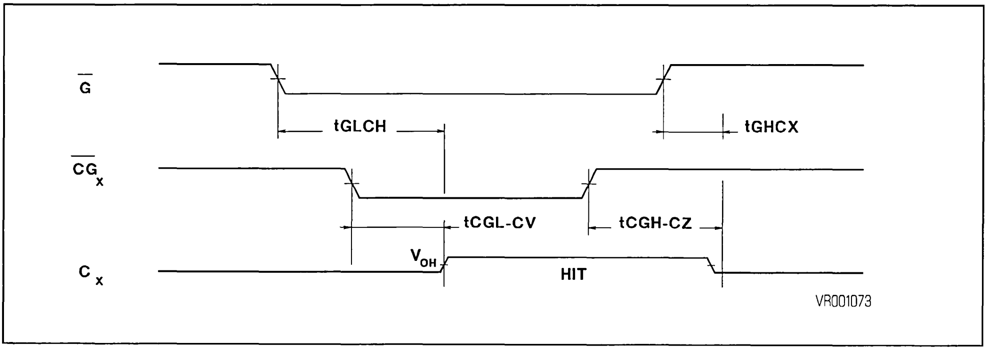
Note : W is HIGH and a Valid Address is present, Hx and Mx are both assumed to be HIGH, with CGx LOW.

Figure 21. Early Write - Hit Cycle


W
tWLCH
tWHCX
CG x
tCGL-CV
tCGH-CZ
V OH
C x
HIT
VR001072

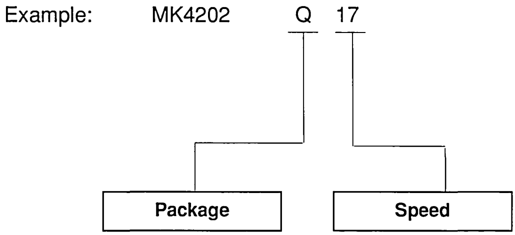
Note : G is HIGH and a Valid Address is present, (E0 - E3) = True. Hx and Mx are both assumed to be HIGH

Figure 22. Early Read - Hit Cycle


G
tGLCH
tGHCX
CG x
tCGL-CV
tCGH-CZ
V OH
C x
HIT
VR001073

Note : W is HIGH and a Valid Address is present, (E0 - E3) = True. Hx and Mx are both assumed to be HIGH.

ORDERING INFORMATION



Package	
Q	PLCC68

Speed	
17	17ns
20	20ns
25	25ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

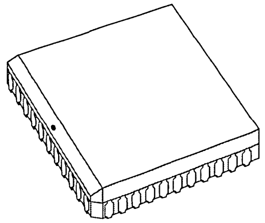
SGS-THOMSON
MICROELECTRONICS

MK62486

VERY FAST CMOS 32K x 9 CACHE BRAM

ADVANCE DATA

- 32K x 9 CMOS SYNCHRONOUS BURSTSRAM
- FAST CYCLE TIMES: 25, 30ns
- FAST ACCESS: 19, 24ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- HIGH OUTPUT DRIVE CAPABILITY
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{G}$)
- BURST CONTROL INPUTS: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$
- DUAL CHIP SELECTS FOR EASY DEPTH EXPANSION

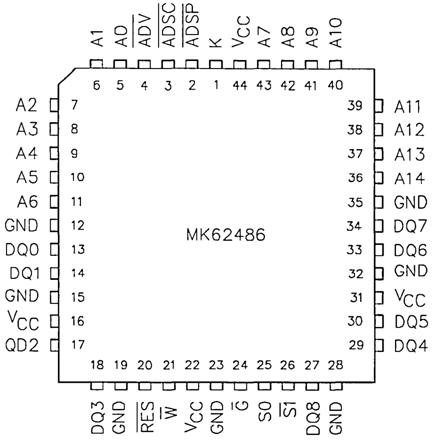


PLCC44 (Q)

PIN NAMES

A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs/Outputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0	Chip Select, Active High
$\overline{S1}$	Chip Select, Active Low
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Cache Ctrl.
$\overline{ADV}$	Burst Address Advance
$\overline{RES}$	Reserve, Tied Low
V_{CC}, GND	5 Volts, Ground

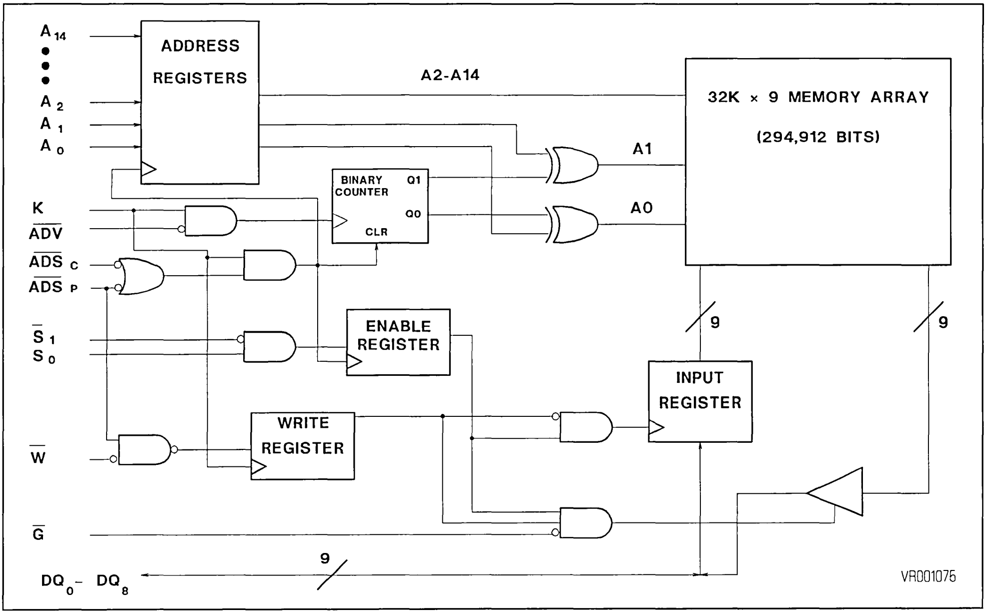
Figure 1. Pin Connection


A1
A0
ADV
ADSC
ADSP
K
VCC
A7
A8
A9
A10
6 5 4 3 2 1 44 43 42 41 40
A2 7
A3 8
A4 9
A5 10
A6 11
GND 12
DQ0 13
DQ1 14
GND 15
VCC 16
QD2 17
39 A11
38 A12
37 A13
36 A14
35 GND
34 DQ7
33 DQ6
32 GND
31 VCC
30 DQ5
29 DQ4
MK62486
18 19 20 21 22 23 24 25 26 27 28
DQ3
GND
RES
W
VCC
GND
G
S0
S1
DQ8
GND

VA00623

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

Figure 2. Block Diagram


A_{14}
A_2
A_1
A_0
ADDRESS REGISTERS
A2-A14
32K x 9 MEMORY ARRAY
(294,912 BITS)
A1
A0
BINARY COUNTER
Q1
Q0
CLR
K
$\overline{ADV}$
$\overline{ADS}_C$
$\overline{ADS}_P$
$\overline{S}_1$
S_0
ENABLE REGISTER
9
9
INPUT REGISTER
WRITE REGISTER
$\overline{W}$
$\overline{G}$
DQ_0 - DQ_8
9
VR001075

DESCRIPTION

The MK62486 BRAM™ is a 288K (294,912-bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed synchronous SRAM onto a single chip. The syn-chronous design provides precise control using an external clock (K) input. The MK62486 is specifically adapted to provide a burstable, high performance secondary cache for the i486™ microprocessor.

The MK62486 is available in a 44 pin plastic leaded chip-carrier (PLCC). The device provides multiple power and ground pins to reduce effects induced by output noise for high performance applications. Separate power and ground pins (V_{CCQ} and GND_Q) have been employed for $DQ_{0\text{-}8}$ to allow output levels referenced to 5 Volts or 3.3 Volts. The main Burst SRAM power requires a single 5V ± 5% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATIONS

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{\text{G}}$), are clock controlled inputs through non-inverting, pos-itive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{\text{ADSP}}$ (Address Status Processor) or $\overline{\text{ADSC}}$ (Address Sta-tus Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{\text{ADV}}$ input (burst address advance) provides control of the burst sequence, which imitates the i486 cache burst address sequence. Once a cache burst cycle begins, the subsequent burst address is generated internally each time the $\overline{\text{ADV}}$ input is asserted at the rising edge of the clock (K) input. The burst counter operates in the same manner for either cache burst write or read cycles.

The $\overline{\text{ADSP}}$ and the $\overline{\text{ADSC}}$ inputs control the start and the duration of the burst sequence respectively. Each time either address status input is asserted low, a new external base address is registered on the positive going edge of the clock (K).

ASYNCHRONOUS TRUTH TABLE

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[(2)]	X	Data In (High-Z)
Deselect	X	High-Z

Notes :

1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

BURST COUNT SEQUENCE

External Address	A14-A2	A1	A0
1st Burst Address	A14-A2	A1	$\overline{A0}$
2nd Burst Address	A14-A2	$\overline{A1}$	A0
3rd Burst Address	A14-A2	$\overline{A1}$	$\overline{A0}$

Note : The burst count sequence wraps around to the initial address after a full count is completed.

SYNCHRONOUS TRUTH TABLE

S0	$\overline{S1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Extend Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Extend Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Read Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst Address	Read Cycle - Suspend Burst Sequence

Notes :

1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3. All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times
5. $\overline{G}$ is a don't care when $\overline{W}$ is registered low from the previous rising clock edge.
6. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{ADSP}$ or $\overline{ADSC}$ is asserted for the device to remain enabled; Chip Selects are registered whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted low at the rising edge of the clock.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.5 to 6	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
P_D	Power Dissipation	1.2	W
I_{OUT}	Output Current	20	mA

Notes :

1. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.
2. Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second.

RECOMMENDED DC OPERATING CONDITIONS

($0\ °C \le T_A \le +70\ °C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
GND	Ground	0	0	0	V
V_{IH}	Logic 1 All Inputs	2.2	3	$V_{CC} + 0.3$	V
V_{IL}	Logic 0 All Inputs	–0.3	0.2	0.8	V

DC ELECTRICAL CHARACTERISTICS

($0\ °C \le T_A \le +70\ °C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average AC Power Supply Current ($\overline{G}$ = S0 = V_{IH}, $\overline{S1}$ = V_{IL}). All inputs = V_{IL} = 0V and $V_{IH} \ge 3V$		160	mA	4
I_{SB}	TTL Standby Current (S0 = V_{IL}, $\overline{S1}$ = V_{IH})		40	mA	5
I_{SB1}	CMOS Standby Current (S0 ≤ 0.2V, $\overline{S1} \ge V_{CC} - 0.2V$)		30	mA	6
I_{LI}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{LO}	Output Leakage Current	–1	1	µA	2
V_{OH}	Output Logic 1 Voltage (I_{OH} = –4.0mA)	2.4		V	1
V_{OL}	Output Logic 0 Voltage (I_{OL} = 8mA)		0.4	V	1

CAPACITANCE

(T_A = 25 °C, f = 1MHz)

Symbol	Parameter	Typ.	Max.	Unit	Notes
C_I	Input Capacitance on all pins (except DQ)	4	5	pF	7
C_O	Output Capacitance	8	10	pF	3, 7

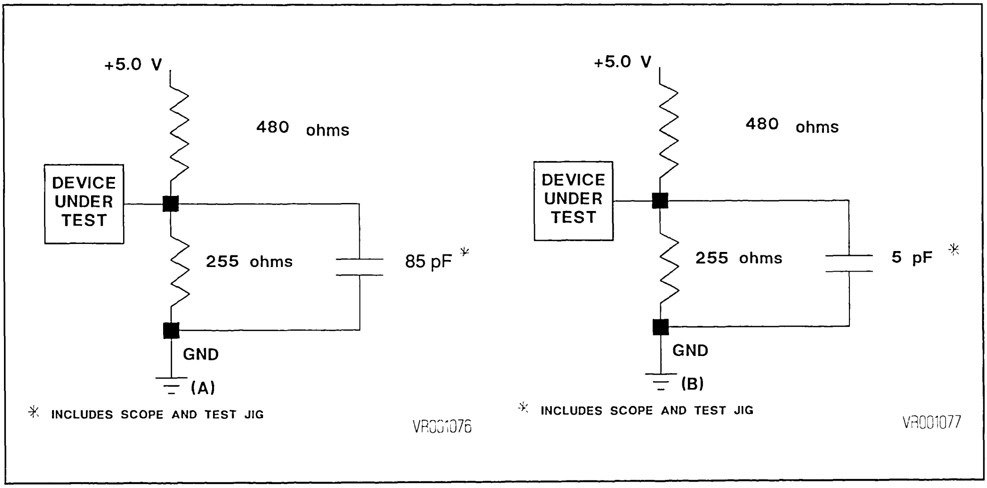
Notes :

1. All voltages referenced to GND.
2. Measured with GND ≤ V ≤ V_{CC} and outputs deselects.
3. Output buffers are deselected.
4. I_{CC1} measured as average AC current, with outputs open, V_{CC} max, t_{KHKH} min duty cycle 100%.
5. All other inputs at V_{IL} or V_{IH}, f = 0, V_{CC} max.
6. All other inputs ≥ V_{CC} – 0.2 or ≤ GND +0.2, f = 0, V_{CC} max.
7. Capacitances are sampled and not 100% tested.
8. For proper operation the $\overline{RES}$ input should be tied to ground.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 15	%

Figure 3. Equivalent Output Load Circuits


+5.0 V
480 ohms
DEVICE UNDER TEST
255 ohms
85 pF *
GND
(A)
* INCLUDES SCOPE AND TEST JIG
VR001076
+5.0 V
480 ohms
DEVICE UNDER TEST
255 ohms
5 pF *
GND
(B)
* INCLUDES SCOPE AND TEST JIG
VR001077

READ/WRITE CYCLE TIMING - AC OPERATING CONDITIONS AND CHARACTERISTICS

($0°C \leq T_A \leq 70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	-19		-24		Unit	Note
		Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	25		30		ns	
t_{KHQV}	Clock Access Time		19		24	ns	1
t_{KHKL}	Clock High Pulse Width	9.5		11		ns	
t_{KLKH}	Clock Low Pulse Width	9.5		11		ns	
t_{GLQV}	Output Enable Access Time		8		9	ns	1
t_{KHQX}	Clock High to Output Active	3		3		ns	1
t_{GLQX}	Output Enable to Output Active	0		0		ns	2
t_{KHQX2}	Clock High to Q Active (Low-Z)	3		3		ns	2
t_{KHQZ}	Clock High to Q High-Z		12		15	ns	2
t_{GHQZ}	Output Disable to Q High-Z		8		9	ns	2
t_{AVKH}	Address Set-up Time	3		3		ns	3
t_{ADSVKH}	Address Status Set-up Time	3		3		ns	3
t_{DVKH}	Data In Set-up Time	3		3		ns	3
t_{WVKH}	Write/Read Set-up Time	3		3		ns	3
t_{ADVVKH}	Address Advance Set-up Time	3		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	3		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	3		3		ns	3
t_{KHAX}	Address Hold Time	2		2		ns	3
t_{KHADSX}	Address Status Hold Time	2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		ns	3
t_{KHADVX}	Address Advance Hold Time	2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		ns	3

Notes :

1. Measured with load as shown in Figure 3A.
2. Transition is measured ± 500 mV from steady-stage voltage with load as shown in Figure 3B. This parameter is sampled and not 100 % tested.
3. This is a synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

DEVICE OPERATIONS (Continued)

When ADSP is asserted low, any ongoing burst cycle is interrupted, and a read operation (independent of W and ADSC) is performed at the new registered external base address. A new burst cycle is initiated each time ADSP is asserted. By asserting ADSC low, the present burst cycle (initiated by ADSP) is interrupted and an extended burst read or write (depending upon the logic state of W at the rising edge of K) is performed at the new registered base address. Chip selects (S0 and S1) are only sampled when a new base address is loaded. Therefore, the chip selects are registered when either address status input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either ADSP or ADSC. The MK62486 Truth Tables and timing diagrams reference specific device operations.

It should be noted that the MK62486 allows a non-burst mode of operation where ADSP is the ADS# of the i486 processor in a 2-2 cycle mode of operation, and ADSC is held high during T2 (see Figure 4). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input. Self-timed write cycles eliminate complex off-chip write pulse generation providing more flexibility for incoming signals.

The ADV input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time ADV is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced before the operation. Wait states can be inserted during burst cycles by holding the ADV pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address

GENERAL APPLICATION

The MK62486 is organized using the ninth bit as the parity bit to support byte parity. Since the i486 processor provides on-board parity generation and checking, the ninth bit of the cache Burst SRAM can be passed to one of the DP0-DP3 pins of the microprocessor. Thus the MK62486 provides an architecture for building a 32K x 32-bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Figure 4. General 128K Byte Cache Block Diagram

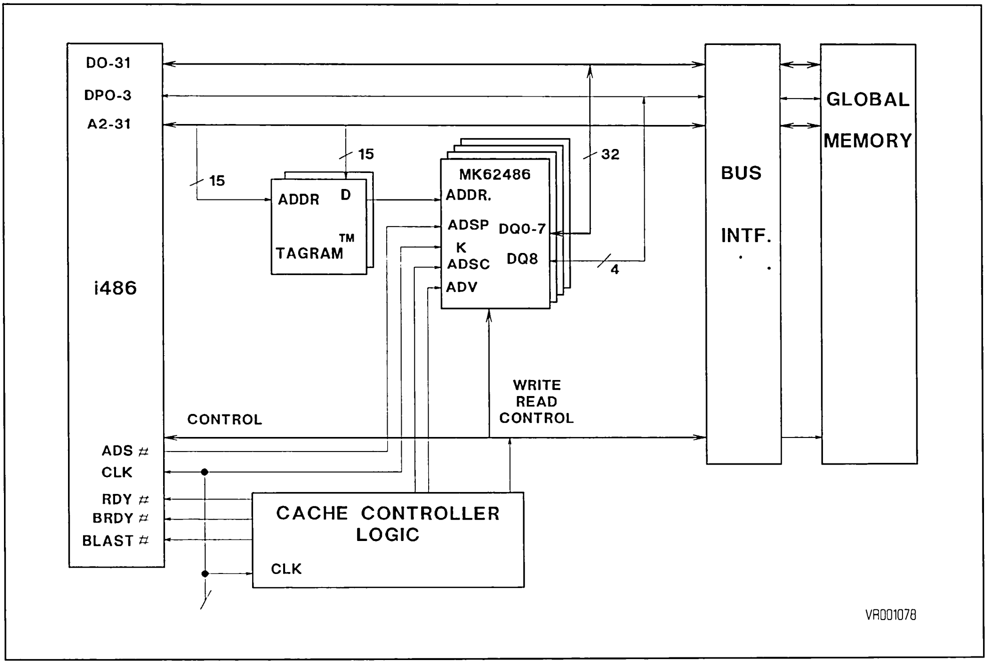
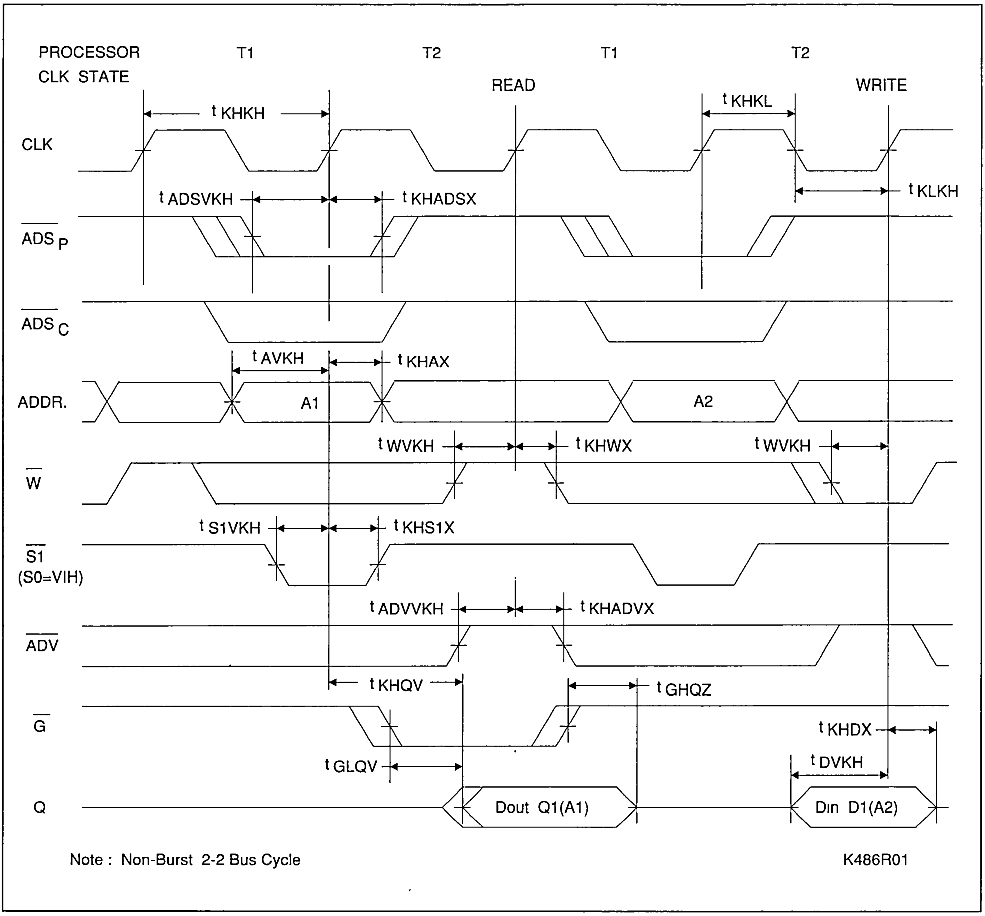


Figure 5. Non-Burst Read/Write 2-2 Cycles


PROCESSOR
CLK STATE
T1
T2
T1
T2
READ
WRITE
t KHKH
t KHKL
CLK
t ADSVKH
t KHADSX
t KLKH
ADS P
ADS C
t AVKH
t KHAX
ADDR.
A1
A2
t WVKH
t KHWX
t WVKH
W
t S1VKH
t KHS1X
S1
(S0=VIH)
t ADVVKH
t KHADVX
ADV
t KHQV
t GHQZ
G
t KHDX
t GLQV
t DVKH
Q
Dout Q1(A1)
Din D1(A2)
K486R01

Note : Non-Burst 2-2 Bus Cycle

Figure 6. Burst Read Cycle

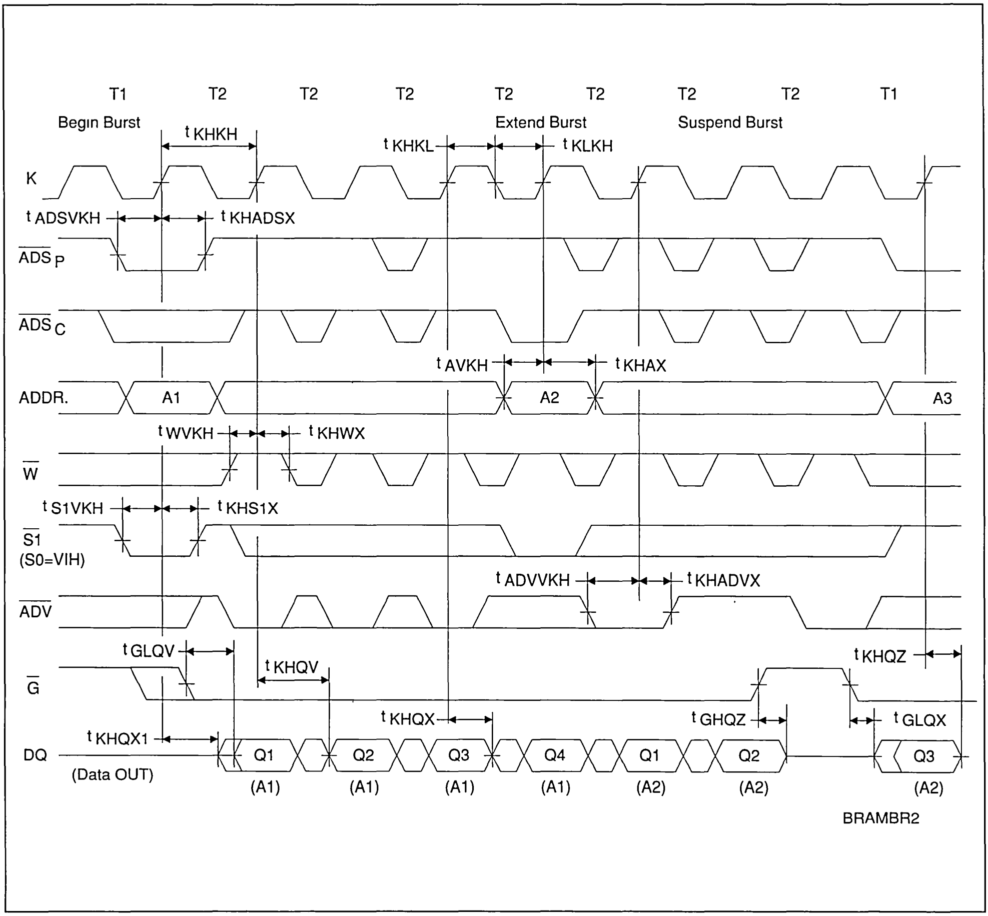

T1
T2
T2
T2
T2
T2
T2
T2
T1
Begin Burst
Extend Burst
Suspend Burst
tKHKH
tKHKL
tKLKH
K
tADSVKH
tKHADSX
ADSP
ADSC
tAVKH
tKHAX
ADDR.
A1
A2
A3
tWVKH
tKHWX
W
tS1VKH
tKHS1X
S1
(S0=VIH)
tADVVKH
tKHADVX
ADV
tGLQV
tKHQV
tKHQZ
G
tKHQX
tGHQZ
tGLQX
tKHQX1
DQ
(Data OUT)
Q1
Q2
Q3
Q4
Q1
Q2
Q3
(A1)
(A1)
(A1)
(A1)
(A2)
(A2)
(A2)
BRAMBR2

Figure 7. Burst Write Cycle

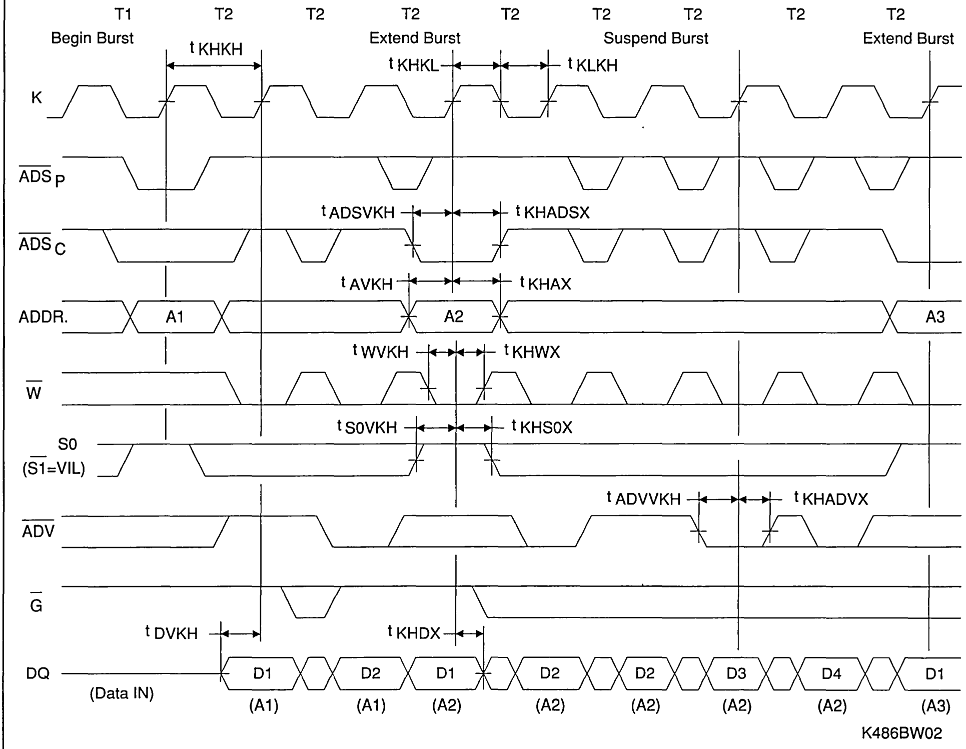
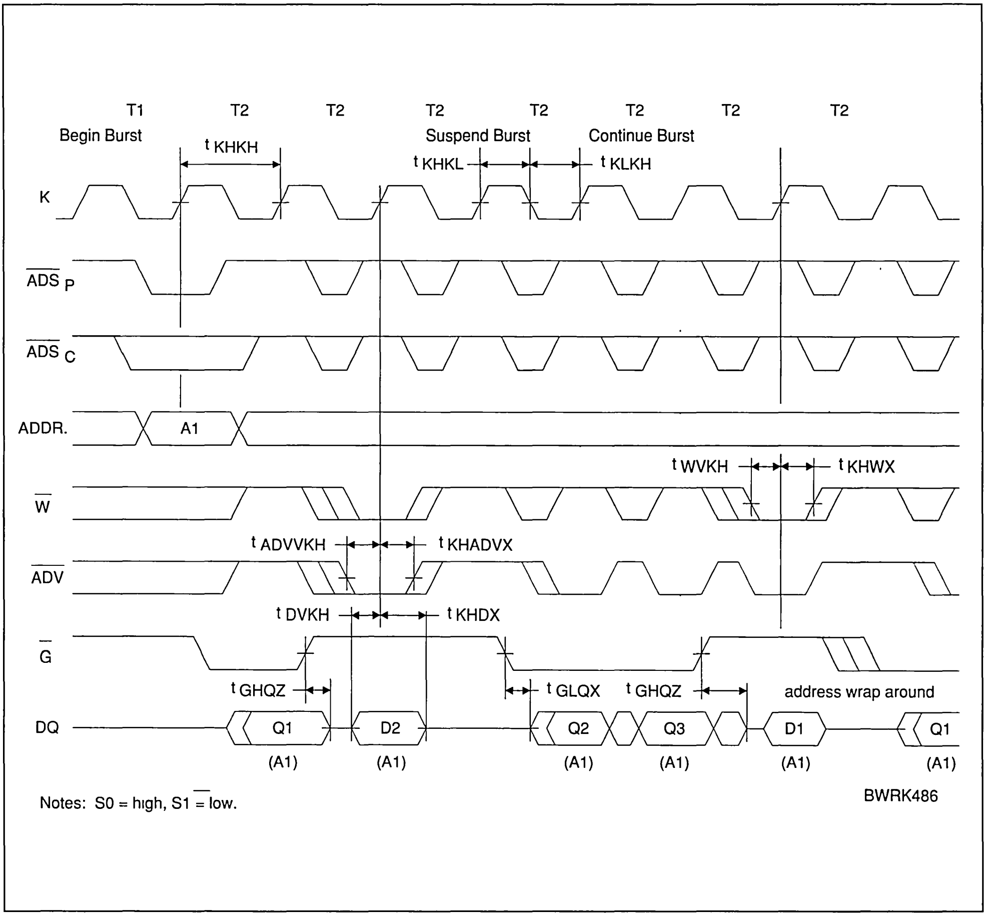

T1
Begin Burst
T2
T2
T2
Extend Burst
T2
T2
T2
Suspend Burst
T2
T2
Extend Burst
t KHKH
t KHKL
t KLKH
K
ADS P
t ADSVKH
t KHADSX
ADS C
t AVKH
t KHAX
ADDR.
A1
A2
A3
t WVKH
t KHWX
W
t S0VKH
t KHS0X
S0
(S1=VIL)
t ADVVKH
t KHADVX
ADV
G
t DVKH
t KHDX
DQ
(Data IN)
D1
D2
D1
D2
D2
D3
D4
D1
(A1)
(A1)
(A2)
(A2)
(A2)
(A2)
(A2)
(A3)
K486BW02

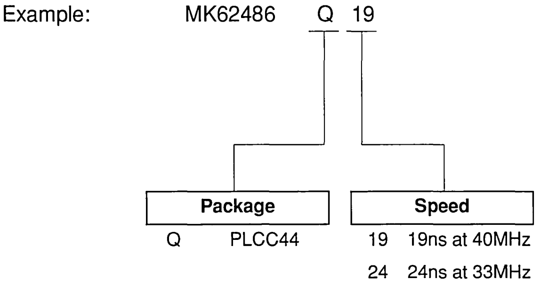
Figure 8. Combined Burst Read/Write Cycle



T1
T2
T2
T2
T2
T2
T2
T2
Begin Burst
t KHKH
Suspend Burst
Continue Burst
t KHKL
t KLKH
K
ADS P
ADS C
ADDR.
A1
t WVKH
t KHWX
W
t ADVVKH
t KHADVX
ADV
t DVKH
t KHDX
G
t GHQZ
t GLQX
t GHQZ
address wrap around
DQ
Q1
D2
Q2
Q3
D1
Q1
(A1)
(A1)
(A1)
(A1)
(A1)
(A1)
BWRK486

Notes: S0 = high, S1 = low.

ORDERING INFORMATION



Example: MK62486 Q 19

Package	
Q	PLCC44

Speed	
19	19ns at 40MHz
24	24ns at 33MHz

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

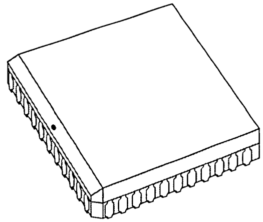
SGS-THOMSON
MICROELECTRONICS

MK62940

VERY FAST CMOS 32K x 9 CACHE BRAM

ADVANCE DATA

- 32K x 9 CMOS SYNCHRONOUS BURST SRAM
- FAST CYCLE TIMES: 25, 30ns
- FAST ACCESS: 19, 24ns Max
- ON-BOARD BURST COUNTER
- INPUT REGISTERS (ADDR.,DATA,CTRL)
- SELF-TIMED WRITE CYCLE
- THREE STATE COMMON I/O
- LATE WRITE ABORT FEATURE
- ASYNCHRONOUS OUTPUT ENABLE ($\overline{\mathrm{G}}$)
- BURST CONTROL INPUTS: $\overline{\mathrm{TSP}}$, $\overline{\mathrm{TSC}}$, $\overline{\mathrm{BAA}}$
- DUAL CHIP SELECTS FOR EASY DEPTH EXPANSION

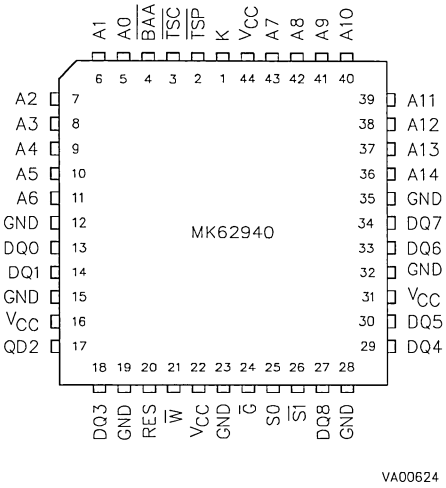


PLCC44 (Q)

PIN NAMES

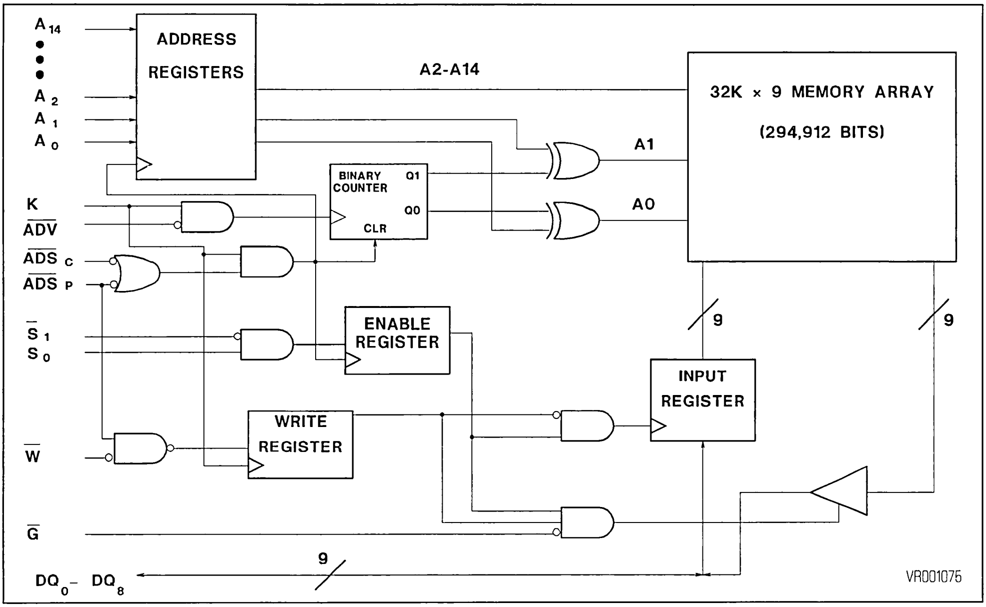
A0 - A14	Address Inputs
DQ0 - DQ8	Data Inputs / Outputs
K	Clock
$\overline{\mathrm{W}}$	Write Enable
$\overline{\mathrm{G}}$	Output Enable
S0	Chip Select, Active High
$\overline{\mathrm{S1}}$	Chip Select, Active Low
$\overline{\mathrm{TSP}}$	Transfer Start Processor
$\overline{\mathrm{TSC}}$	Transfer Start Cache Ctrl.
$\overline{\mathrm{BAA}}$	Burst Address Advance
V_{CC}, GND	5 Volts, Ground
RES	Reserve, Tied High

Figure 1. Pin Connection


A1
A0
BAA
TSC
TSP
K
VCC
A7
A8
A9
A10
6 5 4 3 2 1 44 43 42 41 40
A2 7
A3 8
A4 9
A5 10
A6 11
GND 12
DQ0 13
DQ1 14
GND 15
VCC 16
QD2 17
MK62940
39 A11
38 A12
37 A13
36 A14
35 GND
34 DQ7
33 DQ6
32 GND
31 VCC
30 DQ5
29 DQ4
18 19 20 21 22 23 24 25 26 27 28
DQ3
GND
RES
W
VCC
GND
G
S0
S1
DQ8
GND
VA00624

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

Figure 2. Block Diagram



DESCRIPTION

The MK62940 BRAM™ is a 288K (294,912-bit) CMOS Burst SRAM, organized as 32,768 words x 9 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The device integrates a 2-bit burst counter, input registers, high output drive capability, and high speed synchronous SRAM onto a single chip. The synchronous design provides precise control using an external clock (K) input. The MK62940 is specifically adapted to provide a burstable, high performance secondary cache for the MC68040 microprocessor.

The MK62940 is available in a 44 pin plastic leaded chip-carrier (PLCC). The device is pin compatible and functional equivalent to the Motorola MCM62940, but employs a single power supply design. The main Burst SRAM power (V_{CC}) requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

DEVICE OPERATION

Addresses (A0-A14), data inputs (DQ0-DQ8), and control signals, with exception of Output Enable ($\overline{G}$) are clock controlled inputs through non-inverting, positive edge triggered registers. A cache burst address sequence can be initiated by either $\overline{\mathrm{TSP}}$ (Transfer Start Processor) or $\overline{\mathrm{TSC}}$ (Transfer Start Cache Controller) inputs, with subsequent burst addresses being internally generated by the Burst SRAM. The $\overline{\mathrm{BAA}}$ input (Burst Address Advance) provides control of the burst sequence, which imitates the required MC68040 cache burst address sequence. A cache burst cycle begins by loading the internal counter with the present values of A1 and A0. Thereafter, subsequent burst addresses are generated internally. The burst counter operates in the same manner for either cache burst write or read cycles.

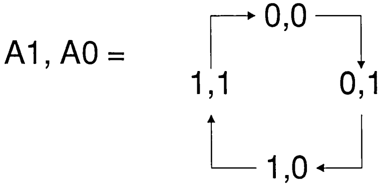
The $\overline{\mathrm{TSP}}$ and the $\overline{\mathrm{TSC}}$ inputs control the start of the burst sequence. When either $\overline{\mathrm{TSx}}$ is asserted low at the rising edge of the clock, any ongoing burst cycle is interrupted and a new external base address is registered. Chip selects (S0 and $\overline{\mathrm{S1}}$) are only sampled when a new base address is loaded.

ASYNCHRONOUS TRUTH TABLE

Mode	$\overline{G}$	DQ Status
Read	L	Data Out
Read	H	High-Z
Write[(2)]	X	High-Z
Write[(2)]	X	Data In
Deselect	X	High-Z

Note :
1. X = Don't Care.
2. For a cache write cycle following a read operation, $\overline{G}$ must be high before the input data required set-up time, and be held high through the input data hold time.

BURST COUNT SEQUENCE



Note : The external values for A1, A0 are the starting point for the burst sequence graph. The burst counter will internally advance A1 and A0 as shown After the counter reaches a full count from the initial value, the address will wrap around.

SYNCHRONOUS TRUTH TABLE

S0	$\overline{S1}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
L	X	L	X	X	X	↑	N/A	Deselected
X	H	H	L	X	X	↑	N/A	Deselected
H	L	L	X	X	X	↑	External Base Address	Read Cycle - Begin Burst
H	L	H	L	X	L	↑	External Base Address	Write Cycle - Extend Burst
H	L	H	L	X	H	↑	External Base Address	Read Cycle - Extend Burst
X	X	H	H	L	L	↑	Advance Burst Address	Write Cycle - Continue Burst Sequence
X	X	H	H	L	H	↑	Advance Burst Address	Reade Cycle - Continue Burst Sequence
X	X	H	H	H	L	↑	Hold Current Burst Address	Write Cycle - Suspend Burst Sequence
X	X	H	H	H	H	↑	Hold Current Burst Address	Read Cycle - Suspend Burst Sequence

Notes :
1. X = Don't Care.
2. All inputs except $\overline{G}$ require set-up and hold times to the rising edge (low to high transition) of the external clock (K).
3 All read and write timings are referenced from $\overline{G}$ or K.
4. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the required set-up and hold times. A write cycle is defined by $\overline{W}$ being asserted low for the set-up and hold times.
5. G is a don't care when $\overline{W}$ is registered low from the previous rising clock edge.
6. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the device to remain enable; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.
7. Chip Selects must be true (S0 = high, $\overline{S1}$ = low) at each rising of the clock while $\overline{TSP}$ or $\overline{TSC}$ is asserted for the the device to remain enabled; Chip Selects are registered whenever $\overline{TSP}$ or $\overline{TSC}$ is asserted low at the rising edge of the clock.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 0.5 to 6	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	– 65 to 150	°C
P_D	Power Dissipation	1.2	W
I_{OUT}	Output Current	20	mA

Note : This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}	Supply Voltage	4.75	5	5.25	V	
GND	Ground	0	0	0	V	
V_{IH}	Logic 1 All Inputs	2	3	$V_{CC} + 0.3$	V	
V_{IL}	Logic 0 All Inputs	– 0.3	0.2	0.8	V	
GND_Q	Output Ground	0	0	0	V	1

Note : 1. All voltages referenced to GND.

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average AC Power Supply Current ($\overline{G} = S0 = V_{IH}$, $\overline{S1} = V_{IL}$). All inputs = V_{IL} = 0V and $V_{IH} \geq 3V$		160	mA	4
I_{SB}	TTL Standby Current ($S0 = V_{IL}$, $\overline{S1} = V_{IH}$)		40	mA	5
I_{SB1}	CMOS Standby Current ($S0 \leq 0.2V$, $\overline{S1} \geq V_{CC} - 0.2V$)		30	mA	6
I_{LI}	Input Leakage Current (Any Input)	– 1	1	µA	2
I_{LO}	Output Leakage Current	– 1	1	µA	2
V_{OH}	Output Logic 1 Voltage (I_{OH} = – 4mA)	2.4		V	1
V_{OL}	Output Logic 0 Voltage (I_{OL} = 8mA)		0.4	V	1

CAPACITANCE

(T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Typ.	Max.	Unit	Notes
C_I	Input Capacitance on all pins (except DQ)	4	5	pF	7
C_O	Output Capacitance	8	10	pF	3, 7

Notes :

1 All voltages referenced to GND.

2 Measured with GND ≤ V ≤ V_{CC} and outputs deselects.

3. Output buffers are deselected.

4. I_{CC1} measured as average AC current, with outputs open, V_{CC} max, $t_{KHKH\ (min)}$ duty cycle 100%

5. All other inputs at V_{IL} or V_{IH}, f = 0, $V_{CC\ max}$.

6. All other inputs ≥ V_{CC} – 0.2 or ≤ GND +0.2, f = 0, $V_{CC\ max}$

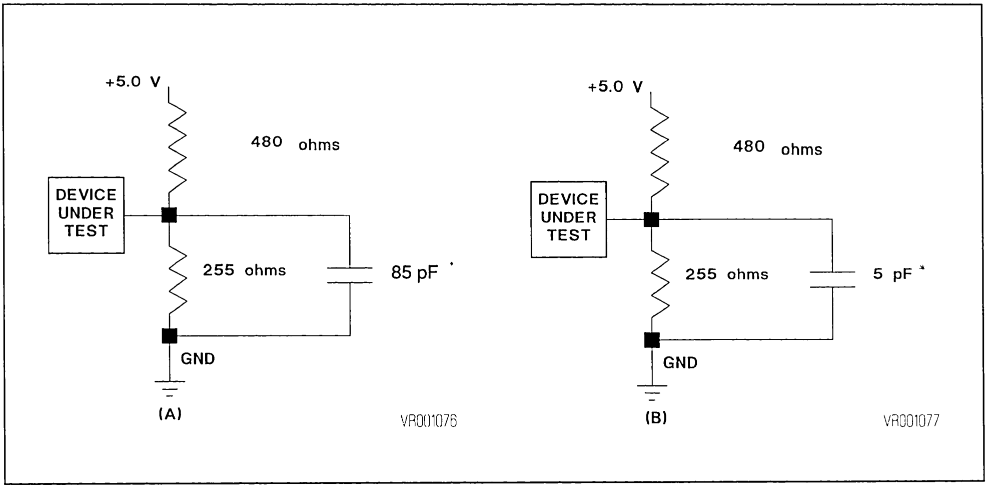
7. Capacitances are sampled and not 100% tested.

8. For proper operation RES must be tied low.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 3. Equivalent Output Load Circuits


+5.0 V
480 ohms
DEVICE UNDER TEST
255 ohms
85 pF *
GND
(A)
VR001076
+5.0 V
480 ohms
DEVICE UNDER TEST
255 ohms
5 pF *
GND
(B)
VR001077

Note: * INCLUDES SCOPE AND TEST JIG

DEVICE OPERATIONS (Continued)

Therefore, the chip selects are registered when either transfer start input is asserted low at the rising edge of the clock (K), and remain latched internally until the next assertion of either TSP or TSC. The MK62940 Truth Tables and timing diagrams reference specific device operations.

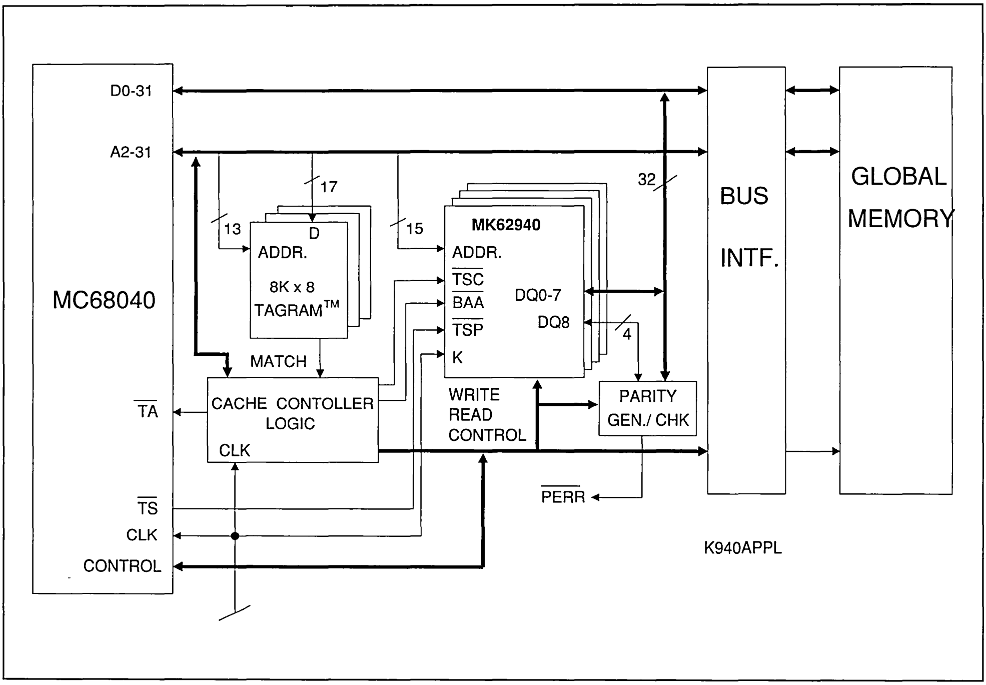
It should be noted that the MK62940 allows a non-burst mode of operation where TSP is the TS pin of the MC68040 processor in a typical 2 clock cycle mode of operation, and TSC is held high during C2 (see Figure 5). However, the non-burst mode obviously negates the advantage of the internal burst counter for fast cache fill operations. In either mode (burst or non-burst), the write cycles are internally self-timed, and are initiated by the rising edge of the clock input when W is low.

The BAA input controls subsequent burst data accesses after the first data of the burst cycle is processed. Each time BAA is asserted low for subsequent bursts at the rising edge of the clock input, the burst counter is advanced to the next burst address sequence. The address is advanced from the rising edge of K. Wait states can be inserted during burst cycles by holding the BAA pin high during positive clock transitions. Upon completion of the full internal burst count, the address will wrap-around to its initial base address.

GENERAL APPLICATION

The MK62940 is organized as 32K x 9 bit words to support byte parity. By incorporating TAGRAM™ with a 15 bit tag field and a 15 bit index address, a cache address scheme of 30 bits is monitiored. The TAGRAM in addtion to the MK62940 provides an architecture for building a 32K x 32-bit burstable data cache SRAM array, with byte parity, by using four devices in a 128K byte cache application.

Figure 4. General 128K Byte Cache Block Diagram


MC68040
D0-31
A2-31
TA
TS
CLK
CONTROL
17
13
D
ADDR.
8K x 8
TAGRAM™
MATCH
15
MK62940
ADDR.
TSC
BAA
TSP
K
DQ0-7
DQ8
4
32
CACHE CONTOLLER
LOGIC
CLK
WRITE
READ
CONTROL
PARITY
GEN./ CHK
PERR
BUS
INTF.
GLOBAL
MEMORY
K940APPL

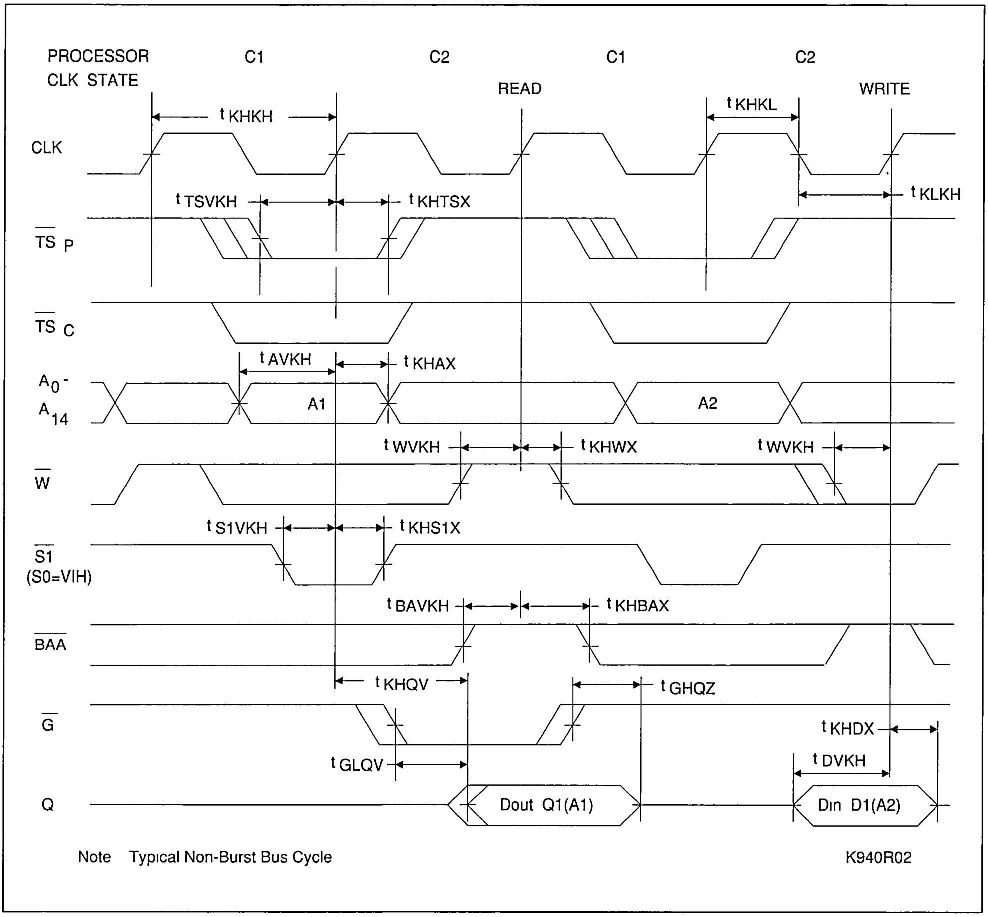
READ/WRITE CYCLE TIMING - AC OPERATING CONDITIONS AND CHARACTERISTICS
($0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	-19		-24		Unit	Note
		Min.	Max.	Min.	Max.		
t_{KHKH}	Cycle Time	25		30		ns	
t_{KHQV}	Clock Access Time		19		24	ns	1
t_{KHKL}	Clock High Pulse Width	9.5		11		ns	
t_{KLKH}	Clock Low Pulse Width	9.5		11		ns	
t_{GLQV}	Output Enable Access Time		8		9	ns	1
t_{KHQX}	Clock High to Output Active	5		5		ns	2
t_{KHQX1}	Clock High to Output Active after Write	3		3		ns	2
t_{GLQX}	Output Enable to Output Active	0		0		ns	2
t_{KHQZ}	Clock High to Q High-Z		12		15	ns	2
t_{GHQZ}	Output Disable to Q High-Z		8		9	ns	2
t_{AVKH}	Address Set-up Time	3		3		ns	3
t_{TSVKH}	Transfer Start Set-up Time	3		3		ns	3
t_{DVKH}	Data In Set-up Time	3		3		ns	3
t_{SWVKH}	Write/Read Set-up Time	3		3		ns	3
t_{BAVKH}	Burst Address Advance Set-up Time	3		3		ns	3
t_{S0VKH}	Chip Select 0 (S0) Set-up Time	3		3		ns	3
t_{S1VKH}	Chip Select 1 ($\overline{S1}$) Set-up Time	3		3		ns	3
t_{KHAX}	Address Hold Time	2		2		ns	3
t_{KHTSX}	Transfer Start Hold Time	2		2		ns	3
t_{KHDX}	Data In Hold Time	2		2		ns	3
t_{KHWX}	Write/Read Hold Time	2		2		ns	3
t_{KHBAX}	Burst Address Advance Hold Time	2		2		ns	3
t_{KHWX}	Asynchronous Write ($\overline{AW}$) Hold Time	2		2		ns	3
t_{KHS0X}	Chip Select 0 (S0) Hold Time	2		2		ns	3
t_{KHS1X}	Chip Select 1 ($\overline{S1}$) Hold Time	2		2		ns	3

Notes :

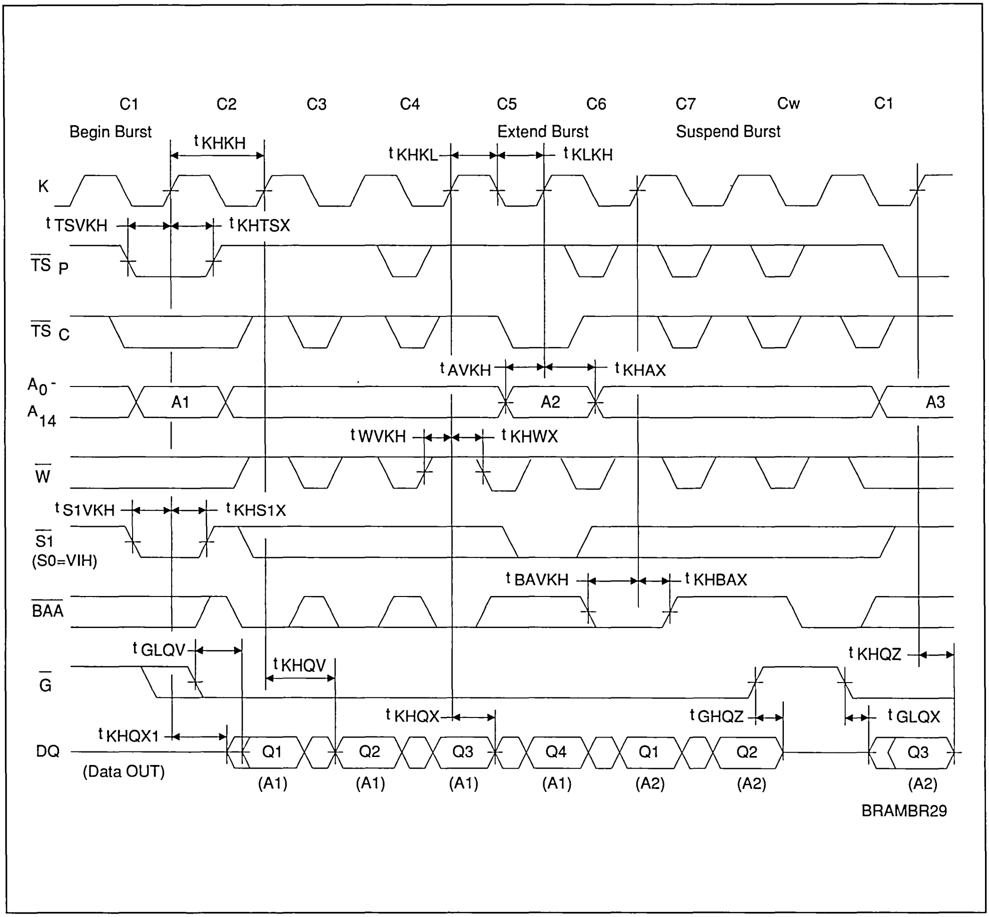
1. Measured with load as shown in Figure 3A.
2. Transition is measured ± 500 mV from steady-stage voltage with load as shown in Figure 3B. This parameter is sampled and not 100 % tested.
3. This is synchronous device requiring that all inputs must meet the specified set-up and hold times with stable logic levels for all rising edges of the clock input (K).

Figure 5. Typical Non-Burst Read/Write Cycles


PROCESSOR
CLK STATE
C1
C2
C1
C2
READ
WRITE
t KHKH
t KHKL
CLK
t TSVKH
t KHTSX
t KLKH
TS P
TS C
t AVKH
t KHAX
A0 -
A14
A1
A2
t WVKH
t KHWX
t WVKH
W
t S1VKH
t KHS1X
S1
(S0=VIH)
t BAVKH
t KHBAX
BAA
t KHQV
t GHQZ
G
t KHDX
t GLQV
t DVKH
Q
Dout Q1(A1)
Din D1(A2)
Note Typical Non-Burst Bus Cycle
K940R02

Note : Typical Non-Burst Cycle. $\overline{AW}$ = Low

Figure 6. Burst Read Cycle


C1
C2
C3
C4
C5
C6
C7
Cw
C1
Begin Burst
Extend Burst
Suspend Burst
tKHKH
tKHKL
tKLKH
K
tTSVKH
tKHTSX
TS P
TS C
tAVKH
tKHAX
A0 - A14
A1
A2
A3
tWVKH
tKHWX
W
tS1VKH
tKHS1X
S1 (S0=VIH)
tBAVKH
tKHBAX
BAA
tGLQV
tKHQV
tKHQZ
G
tKHQX
tGHQZ
tGLQX
tKHQX1
DQ (Data OUT)
Q1
Q2
Q3
Q4
Q1
Q2
Q3
(A1)
(A1)
(A1)
(A1)
(A2)
(A2)
(A2)
BRAMBR29

NOTE : $\overline{G}$ = HIGH

Figure 7. Burst Write Cycle

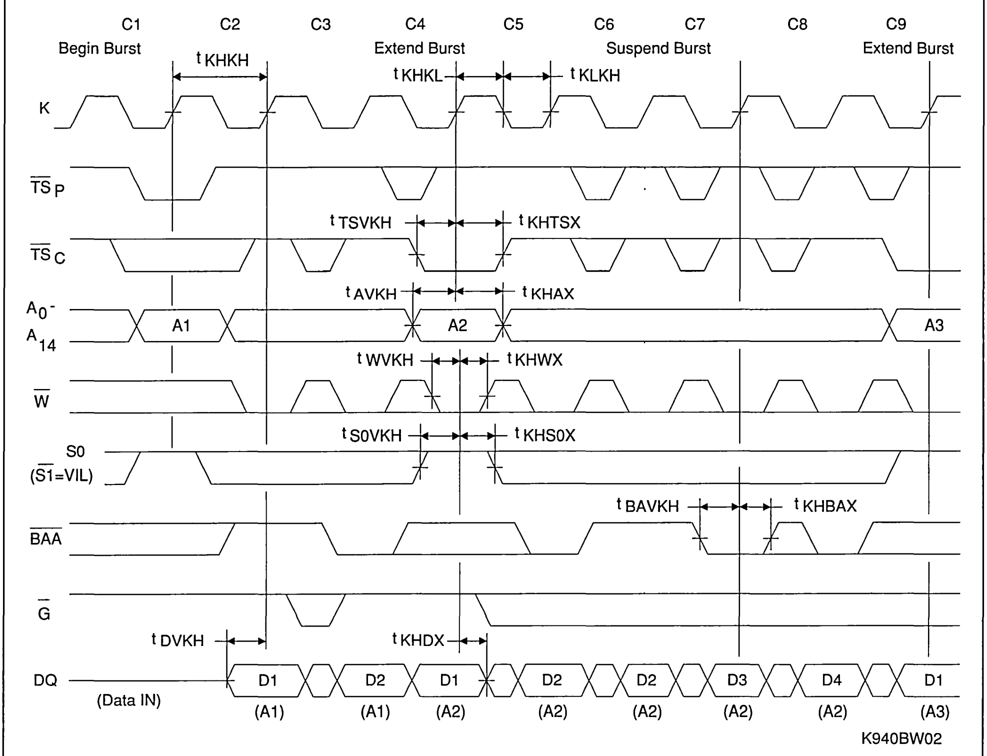
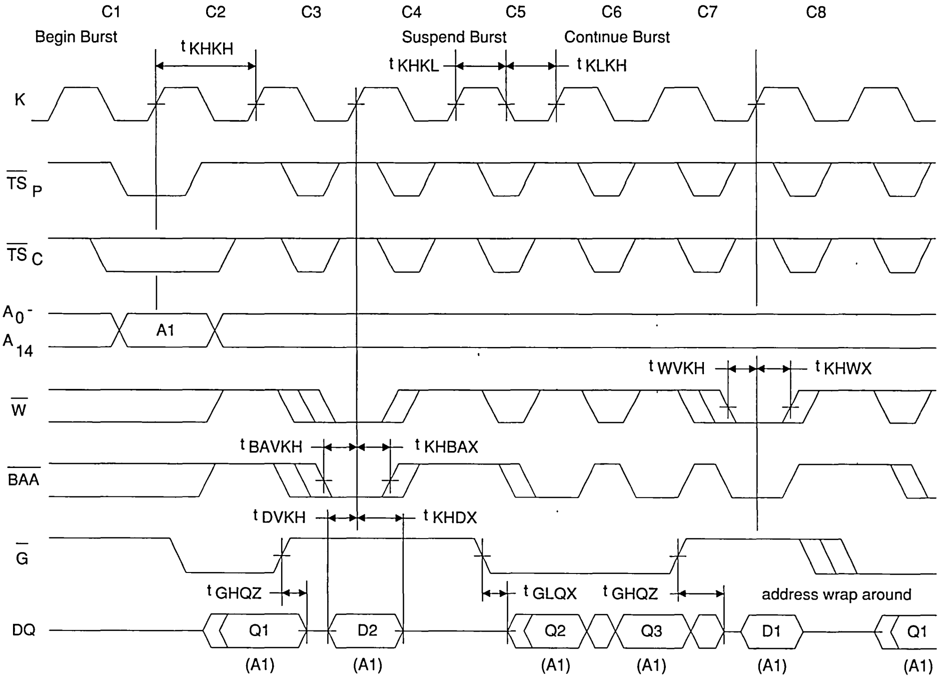

C1
C2
C3
C4
C5
C6
C7
C8
C9
Begin Burst
Extend Burst
Suspend Burst
Extend Burst
tKHKH
tKHKL
tKLKH
K
TSP
tTSVKH
tKHTSX
TSC
tAVKH
tKHAX
A0-A14
A1
A2
A3
tWVKH
tKHWX
W
tS0VKH
tKHS0X
S0
(S1=VIL)
tBAVKH
tKHBAX
BAA
G
tDVKH
tKHDX
DQ
(Data IN)
D1
D2
D1
D2
D2
D3
D4
D1
(A1)
(A1)
(A2)
(A2)
(A2)
(A2)
(A2)
(A3)
K940BW02

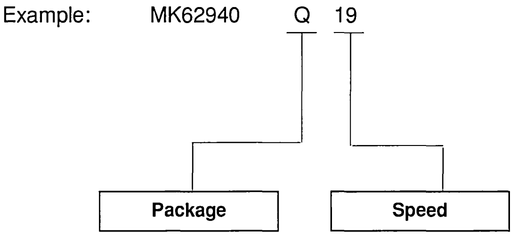
Figure 8. Combined Burst Read/Write Cycle


C1
C2
C3
C4
C5
C6
C7
C8
Begin Burst
Suspend Burst
Continue Burst
t KHKH
t KHKL
t KLKH
K
TS P
TS C
A0 - A14
A1
W
t WVKH
t KHWX
BAA
t BAVKH
t KHBAX
G
t DVKH
t KHDX
DQ
t GHQZ
t GLQX
t GHQZ
address wrap around
Q1
D2
Q2
Q3
D1
Q1
(A1)
(A1)
(A1)
(A1)
(A1)
(A1)
BWRK940

Notes: S0 = high, $\overline{S1}$ = low.

Note : SO = High, $\overline{S1}$ = $\overline{G}$ = Low

ORDERING INFORMATION



Package	
Q	PLCC44

Speed	
19	19ns at 40MHz
24	24ns at 33MHz

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

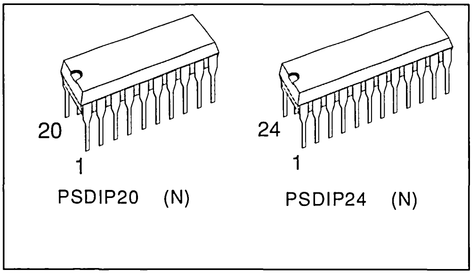
FIFO MEMORIES

SGS-THOMSON
MICROELECTRONICS

MK4505M
MK4505S

VERY FAST CMOS 1K x 5 CLOCKED FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- 1024 x 5 ORGANIZATION
- RISING EDGE TRIGGERED CLOCK INPUTS
- SUPPORTS FREE-RUNNING 40% TO 60% DUTY CYCLE CLOCK INPUTS
- SEPARATE READ AND WRITE ENABLE INPUTS
- BiPORT RAM ARCHITECTURE ALLOWS FULLY ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE OPERATION
- CASCADABLE TO ANY DEPTH WITH NO ADDITIONAL LOGIC
- WIDTH EXPANDABLE TO MORE THAN 40 BITS WITH NO ADDITIONAL LOGIC
- HALF FULL STATUS FLAG
- FULL AND EMPTY FLAGS, ALMOST FULL, ALMOST EMPTY, INPUT READY, OUTPUT VALID STATUS FLAGS (4505M)


20
1
PSDIP20 (N)
24
1
PSDIP24 (N)

DESCRIPTION

The MK4505 is a Very High Speed 1K x 5 Clocked FIFO memory. It achieves its high performance through the use of a pipelined architecture, a 1.2µ full CMOS, single poly, double level metal process, and a memory array constructed using SGS-THOMSON's 8 transistor BiPORT™ memory cell.

The device is designed for use in applications where data is moving through a system on a square wave clock ; applications such as digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, Radar return sampling or data tracing.

PIN NAMES

D0 - D4	Data Inputs
Q0 - Q4	Data Outputs
CKW, CKR	Write and Read Clock
WE1	Write Enable Input 1
RE1	Read Enable Input 1
$\overline{RS}$	Reset (active low)
HF	Half Full Flag
V_{CC}, GND	5 Volts, Ground

Figure 1. Pin Connections.

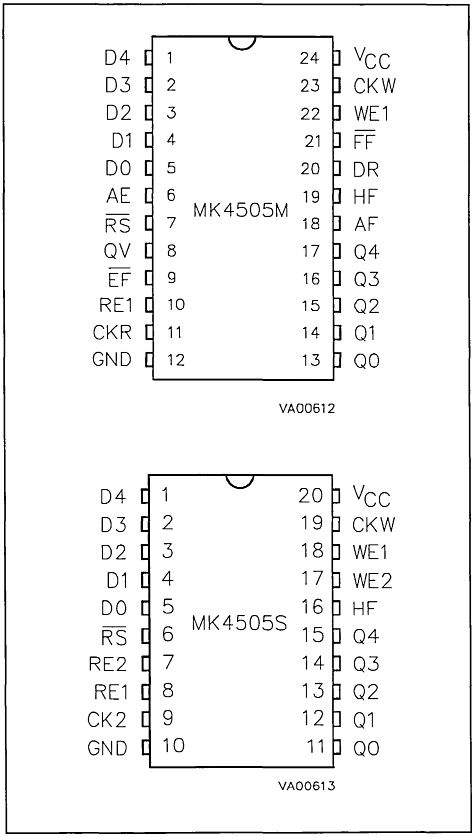
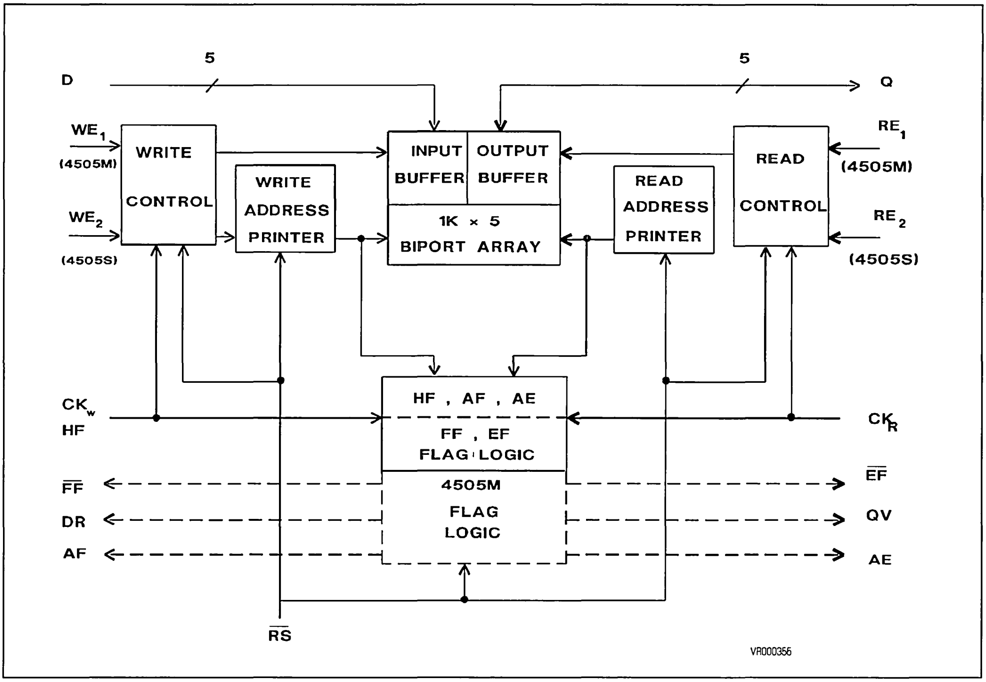

D4 1
D3 2
D2 3
D1 4
D0 5
AE 6
RS 7
QV 8
EF 9
RE1 10
CKR 11
GND 12
24 VCC
23 CKW
22 WE1
21 FF
20 DR
19 HF
18 AF
17 Q4
16 Q3
15 Q2
14 Q1
13 Q0
MK4505M
VA00612
D4 1
D3 2
D2 3
D1 4
D0 5
RS 6
RE2 7
RE1 8
CK2 9
GND 10
20 VCC
19 CKW
18 WE1
17 WE2
16 HF
15 Q4
14 Q3
13 Q2
12 Q1
11 Q0
MK4505S
VA00613

Figure 2 . Block Diagram.


5
5
D
Q
WE_1
(4505M)
WE_2
(4505S)
WRITE CONTROL
WRITE ADDRESS PRINTER
INPUT BUFFER
OUTPUT BUFFER
1K × 5 BIPORT ARRAY
READ ADDRESS PRINTER
READ CONTROL
RE_1
(4505M)
RE_2
(4505S)
CK_W
HF
HF , AF , AE
FF , EF FLAG LOGIC
CK_R
4505M FLAG LOGIC
$\overline{FF}$
DR
AF
$\overline{EF}$
QV
AE
$\overline{RS}$
VR000356

DESCRIPTION (Continued)

The device is available in two versions; a Master, the MK4505M, and a Slave, the MK4505S. The Master provides all of the control signals necessary for reliable, full speed, fully asynchronous width expansion and/or depth expansion. The Master also provides a full compliment of status flags, including Output Valid, Empty, Almost Empty, Half Full, Almost Full, Full, and Input Ready. The Master cannot be written while Full or read while Empty. The Slave, in contrast, can be forced to write and/or read continuously regardless of device status ; a feature useful in triggered data acquisitions, or for retransmit (repeat reading) applications.

4505M only

$\overline{FF}$,$\overline{EF}$ AF,AE DR,QV	Full and Empty Flags (active low) Almost, Full, Almost Empty Flags Input Ready, Output Valid

4505S only

WE2 RE2	Write Enable Input 2 Read Enable Input 2 (rising edge triggered 3 state control)

ASBOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 1.0 to 70	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Ambient Storage Temperature (plastic)	– 55 to 125	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current per Pin	25	mA

Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_A \le +70°C$)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
V_{CC}	Supply voltage	4.5	5	5.5	V	1
GND	Ground	0	0	0	V	1
V_{IH}	Logic 1 input	2.2		V_{CC} + 1.0	V	1
V_{IL}	Logic 0 input	– 0.3		0.8	V	1

Note : 1. All voltages referenced to GND.

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$; V_{CC} =5V ±10%)

Symbol	Parameter	4505-25			4505-33			4505-50			Unit	Note
		Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max		
I_{CC}	Average Power Supply Current		115	140		95	140		75	140	mA	1

Symbol	Parameter	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current		± 1	µA	2
I_{CL}	Output Leakage Current		± 10	µA	2,3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = –4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4

Notes :
1. Measured with both ports operating at t_{CK} Min, 50% duty cycle, outputs open, V_{CC} max Typical values reflect t_{CK} Min, outputs open, with V_{CC} = 5V, 25°C, with 50% duty cycle.
2. Measured with V = 0V to V_{CC}.
3. Measured at Q0 – Q4, with QV = Low (4505M) ; after clocking with RE2 = Low (4505S).
4. All voltages referenced to GND.

CAPACITANCE (T_A =25°C, f =1.0MHz)

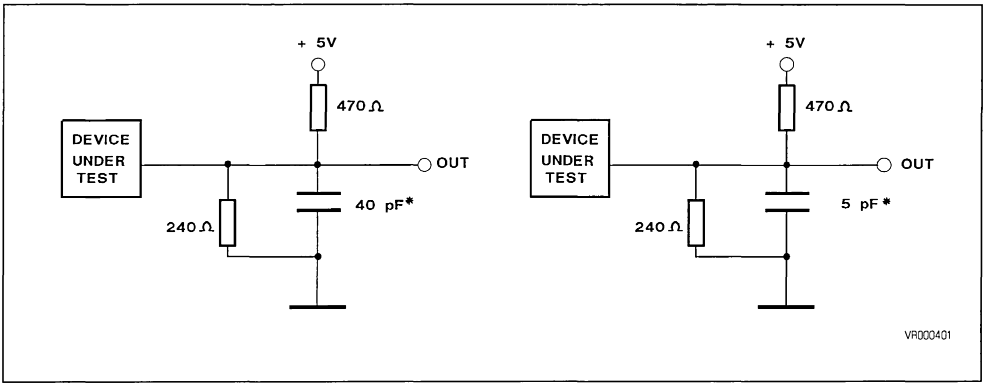
Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Input Capacitance	4		5	pF	1
C_{O1}	Output Capacitance	8		10	pF	1,2
C_{O2}	Output Capacitance	12		15	pF	1,3

Notes :
1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data and flag outputs except $\overline{EF}$ and $\overline{FF}$.
3. Measured at EF and FF.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Times	5	ns
Input and Output Timing Reference Levels	1.5	V
Ambient Temperature	0 to 70	°C
V_{CC}	5 ± 10%	V

Figure 3. Output Load Circuits.



Note : * Includes scope and test fixture.

READ AND HOLD OPERATIONS

The device will perform a Read on the next rising edge of the Read Clock (CKR) whenever (see Figure 4) :

- (4505S) RE1 and RE2 are high at the rising edge of the clock.
- (4505M) RE1 and $\overline{EF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Empty Flag ($\overline{EF}$) on the rising edge of CKR, the appearance of an active Empty Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CKR will generate an inhibit condition. All Q outputs will be High Z at t_{QZ} from the rising edge of CKR. $\overline{EF}$ is latched between subsequent read clocks.

The device will perform a Hold Cycle (hold over previous data) if RE1 is low at the rising edge of the clock (CKR). If $\overline{EF}$ (4505M) or RE2 (4505S) is low at the rising edge of the clock, then the outputs will go to High-Z.

WRITE OPERATIONS

The device will perform a Write on the next rising edge of the Write Clock (CKW) whenever (see Figure 5) :

- (4505S) WE1 and WE2 are high at the rising edge of the clock.
- (4505M) WE1 and $\overline{FF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Full Flag ($\overline{FF}$) on the rising edge of CKW, the appearance of an active Full Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CKW will generate a No-Op condition. $\overline{FF}$ is latched between subsequent write clocks.

MK4505M (Master) **WRITE TRUTH TABLE**

CKW	Present State			Operation	Next State	
	$\overline{RS}$	WE1	$\overline{FF}$		$\overline{FF}$	Data in
X	0	X	X	Reset	1	Don't Care
↑	1	0	0	No-Op	?	Don't Care
↑	1	0	1	No-Op	1	Don't Care
↑	1	1	0	No-Op	?	Don't Care
↑	1	1	1	Write	?	Data in

? = Device Status is referenced to the "next state" logic conditions.
The "next state" flag logic level is unknown due to the possible occurence of a read operation.

MK4505M (Master) **READ TRUTH TABLE**

CKR	Present State			Operation	Next State	
	$\overline{RS}$	RE1	$\overline{EF}$		$\overline{EF}$	Q_{OUT}
X	0	X	X	Reset	0	Hi Z
↑	1	0	0	Inhibit	?	Hi Z
↑	1	0	1	Hold	1	Previous Q
↑	1	1	0	Inhibit	?	Hi Z
↑	1	1	1	Read	?	Data Out

? = Device Status is referenced to the "next state" flag logic and Q_{OUT} conditions.
The "next state" flag logic level is unknown due to the possible occurrence of a write operation.

MK4505S (Slave) **WRITE TRUTH TABLE**

CKW	Present State			Operation	Next State
	$\overline{RS}$	WE1	WE2		Data
X	0	X	X	Reset	Don't Care
↑	1	0	0	No-Op	Don't Care
↑	1	0	1	No-Op	Don't Care
↑	1	1	0	No-Op	Don't Care
↑	1	1	1	Write	Data in

MK4505S (Slave) **READ TRUTH TABLE**

CKR	Present State			Operation	Next State
	$\overline{RS}$	RE1	RE2		Q_{OUT}
X	0	X	X	Reset	Hi Z
↑	1	0	0	Inhibit	Hi Z
↑	1	0	1	Hold	Previous Q
↑	1	1	0	Inhibit	Hi Z
↑	1	1	1	Read	Data Out

RESET

$\overline{RS}$ is an asynchronous master reset input. A Reset is required after power-up, before first write. Reset commences on the falling edge of $\overline{RS}$ irrespective of the state of any other input or output. The user is required to observe Reset Set Up Time (t_{RSS}) only if the device is enabled (see Figure 7). The t_{RSS} specification is a don't care if the device remains disabled (WE1 = RE1 = LOW). All status flag outputs will be valid t_{RSA} from the falling edge of $\overline{RS}$, and all Q data outputs will be high impedance t_{RSQZ} from the same falling edge.

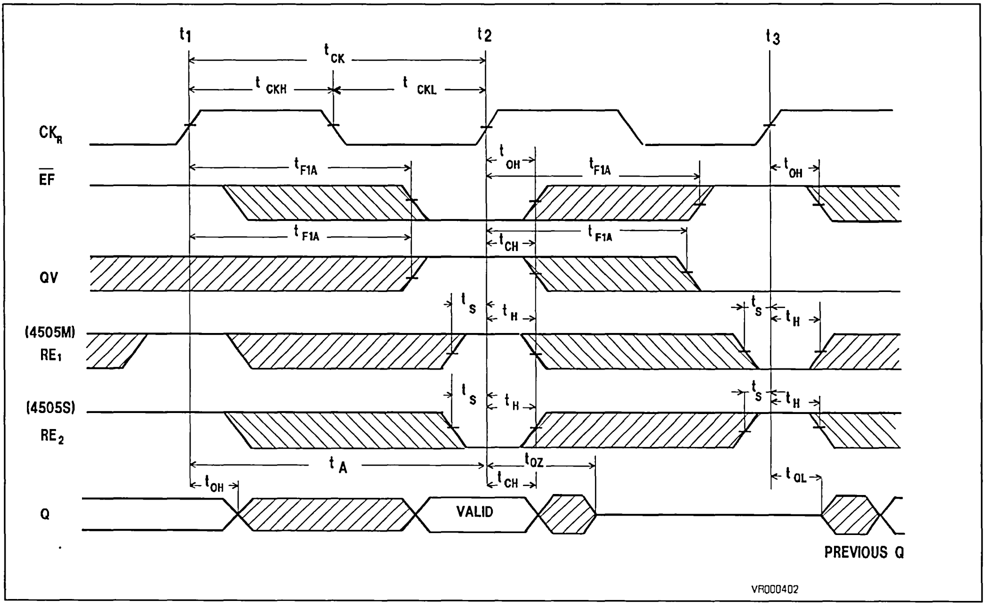
After Reset, if no valid Read operations have been performed since Reset, the "previous data" that will be output when executing the first Hold cycle will be all zeros (see Figure 8).

AC ELECTRICAL CHARACTERISTICS (T_A =0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	4505-25		4505-33		4505-50		Unit	Note
		Min.	Max	Min.	Max	Min.	Max.		
t_{CK}	Clock Cycle Time	25		33		50		ns	1
t_{CKH}	Clock High Time	10		13		20		ns	1
t_{CKL}	Clock Low Time	10		13		20		ns	1
t_S	Set Up Time	10		13		16		ns	1
t_H	Hold Time	0		0		0		ns	
t_A	Output (Q) Access Time		15		20		25	ns	1, 2
t_{F1A}	Flag 1 Access Time (7)		15		20		25	ns	1, 2
t_{F2A}	Flag 2 Access Time (8)		20		25		30	ns	1, 2
t_{OH}	Output Hold Time	5		5		5		ns	1, 2
t_{QZ}	Clock to Outputs High-Z		15		20		25	ns	1, 3
t_{QL}	Clock to Outputs Low-Z	5		5		5		ns	1, 3
t_{RSS}	Reset Set Up Time	12		16		25		ns	1, 4
t_{RS}	Reset Pulse Width	25		33		50		ns	
t_{RSA}	Reset Flag Access Time		50		66		100	ns	1, 3
t_{RSQZ}	Reset to Outputs High-Z		25		33		50	ns	1, 3
t_{FRL}	First Read Latency	50		66		100		ns	1, 5
t_{FFL}	First Flag Cycle Latency	25		33		50		ns	1, 6

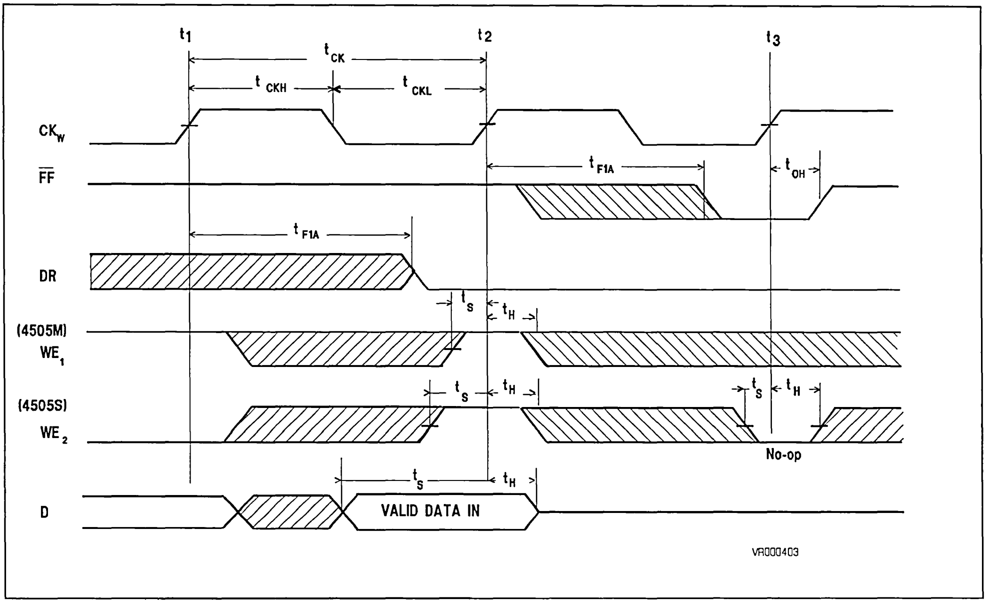
Notes :
1 All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/40pf Output Load (Figure 3A).
3. Measured w/5pf Output Load (Figure 3B).
4. Need not be met unless device is Read and/or Write Enabled.
5. Minimum first Write to first Read delay required to assure valid first Read.
6. Minimum first Write to first Read Clock delay required to assure clearing the Empty Flag.
7. Flag 1 = $\overline{EF}$, $\overline{FF}$, QV, DR.
8. Flag 2 = AE, AF, HF.

Figure 4. Read Cycle Timing.


t1
t2
t3
tCK
tCKH
tCKL
CKR
EF
tF1A
tOH
tF1A
tOH
tF1A
tCH
tF1A
QV
(4505M)
RE1
tS
tH
tS
tH
(4505S)
RE2
tS
tH
tS
tH
tA
tOZ
tOH
tCH
tQL
Q
VALID
PREVIOUS Q
VR000402

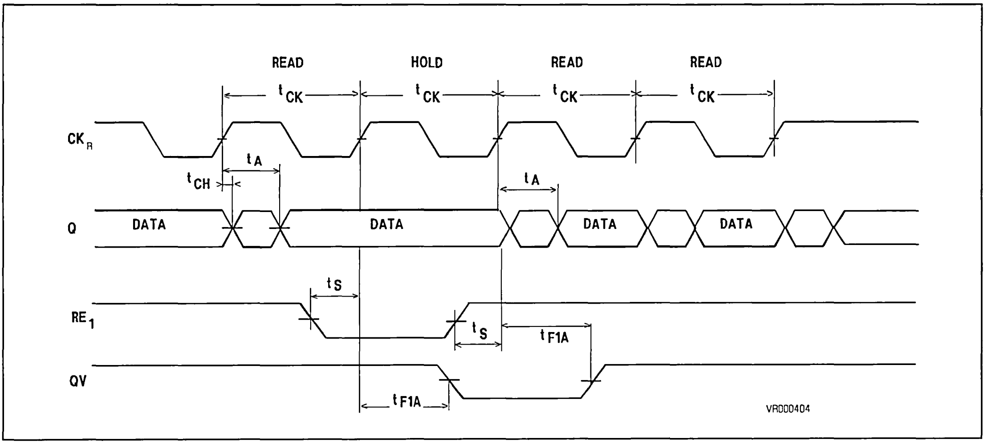
Note : For this particular diagram the $\overline{EF}$ changes logic states presuming that a valid WRITE operation has occured prior to the rising edge of CKR at t_2.

Figure 5. Write Cycle Timing.


t1
t2
t3
tCK
tCKH
tCKL
CKW
FF
tF1A
tOH
tF1A
DR
tS
tH
(4505M)
WE1
tS
tH
tS
tH
(4505S)
WE2
No-op
tS
tH
D
VALID DATA IN
VR000403

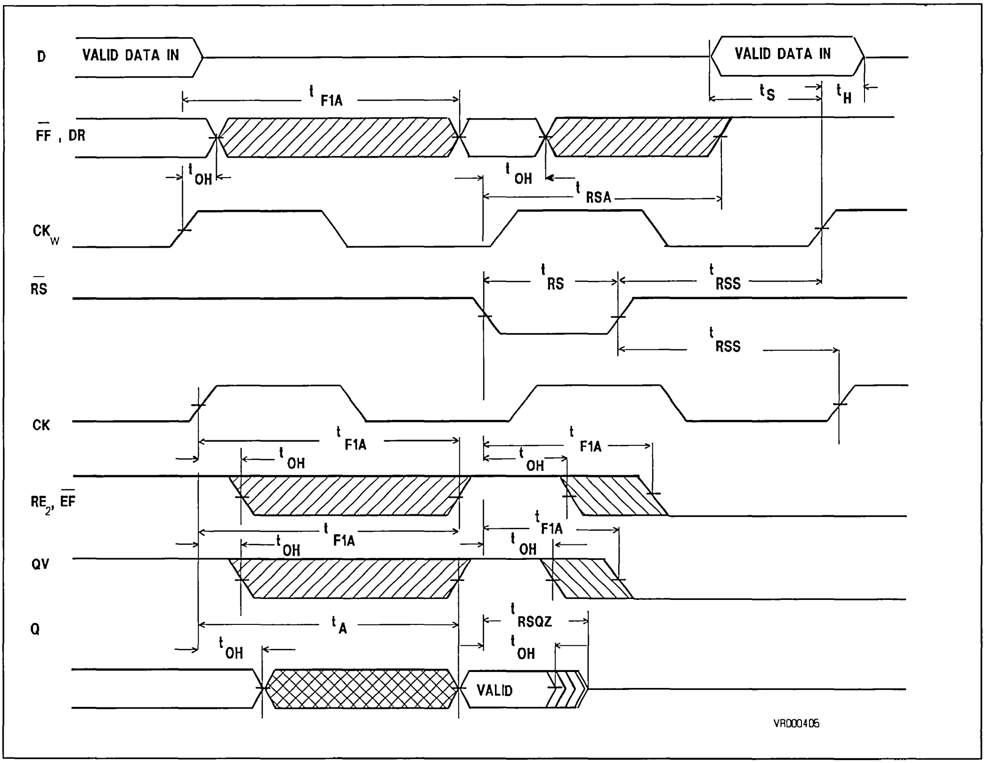
Note : For this particular diagram the $\overline{FF}$ changes logic states presuming that a valid READ operation has occured prior to the rising edge of CKW at t_3.

Figure 6 . Hold Cycle Timing.


READ
HOLD
READ
READ
tCK
tCK
tCK
tCK
CKR
tA
tCH
tA
Q
DATA
DATA
DATA
DATA
tS
RE1
tS
tF1A
QV
tF1A
VR000404

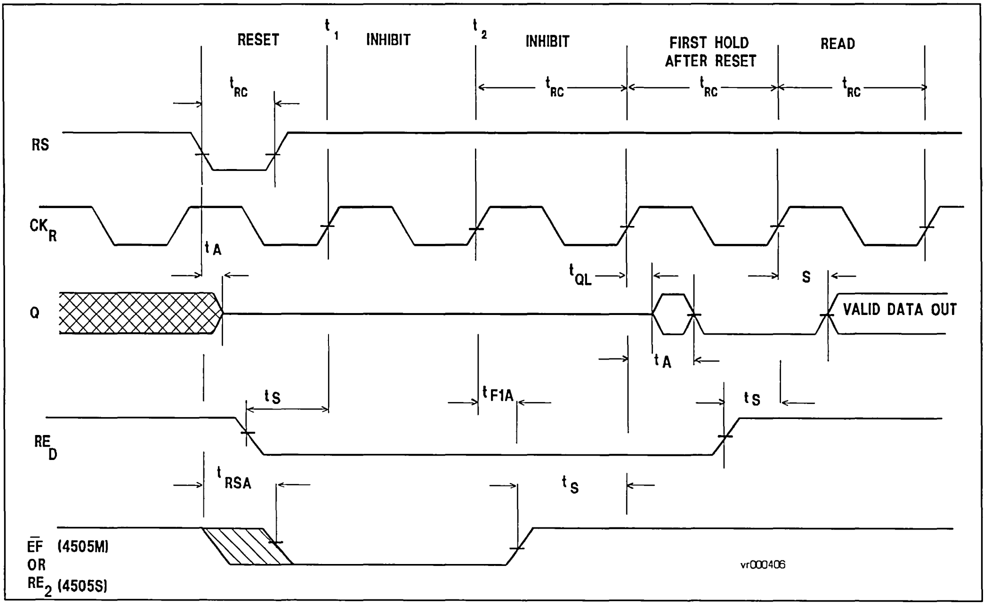
Note : $\overline{EF}$ = HIGH (master)
RE2 = HIGH (slave)

Figure 7. Reset Cycle Timing.


D
VALID DATA IN
VALID DATA IN
tF1A
tS
tH
$\overline{FF}$, DR
tOH
tOH
tRSA
CKW
$\overline{RS}$
tRS
tRSS
tRSS
CK
tF1A
tOH
tF1A
tOH
RE2, $\overline{EF}$
tF1A
tOH
tF1A
tOH
QV
Q
tA
tOH
tRSQZ
tOH
VALID
VR000405

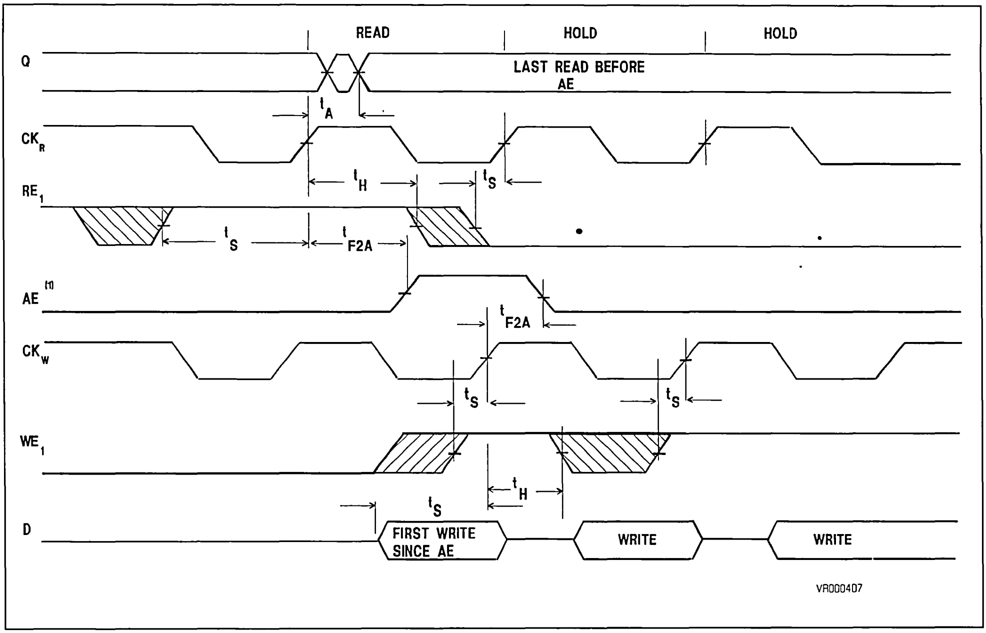
Note : t_{RSS} must be met if the device is read AND/OR write enabled (WE1, RE1 = High).

Figure 8. First Hold After Reset.


RESET
t1
INHIBIT
t2
INHIBIT
FIRST HOLD AFTER RESET
READ
tRC
tRC
tRC
tRC
RS
CKR
tA
tQL
S
Q
VALID DATA OUT
tA
tS
tF1A
tS
RED
tRSA
tS
EF (4505M) OR RE2 (4505S)
vr000406

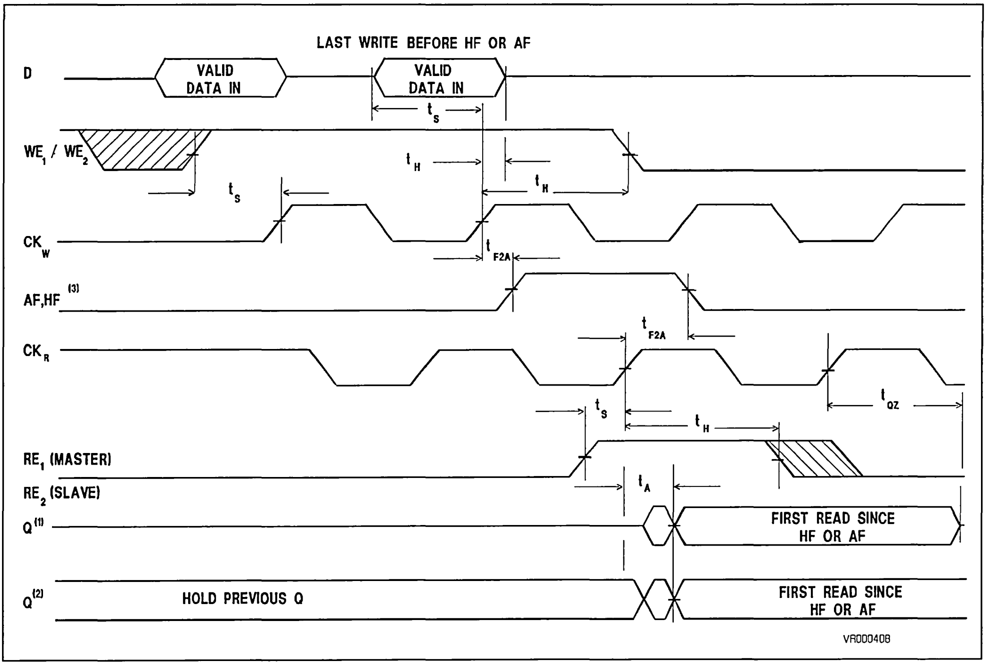
Note : A valid write operation is presumed between t₁ and t₂.

Figure 9. Almost Empty Flag Timing (4505M only).


READ
HOLD
HOLD
Q
LAST READ BEFORE AE
tA
CKR
tH
tS
RE1
tS
tF2A
AE (1)
tF2A
CKW
tS
tS
WE1
tH
tS
D
FIRST WRITE SINCE AE
WRITE
WRITE
VR000407

Note : 1. This example does not show the hysterisis in the ALMOST FLAGS.

Figure 10. Almost Full, Half Full Flag Timing.


LAST WRITE BEFORE HF OR AF
D
VALID DATA IN
VALID DATA IN
t_S
WE_1 / WE_2
t_H
t_H
t_S
CK_W
t_{F2A}
AF,HF (3)
t_{F2A}
CK_R
t_S
t_H
t_{QZ}
RE_1 (MASTER)
RE_2 (SLAVE)
t_A
Q(1)
FIRST READ SINCE HF OR AF
Q(2)
HOLD PREVIOUS Q
FIRST READ SINCE HF OR AF
VR000408

Notes : 1. Q outputs in Master/Slave Width Expansion (RE2 = $\overline{EF}$), or when using MK4505S Slave separately.
2. Q outputs in Master-to-Master Depth Expansion (RE1 with $\overline{EF}$ = HIGH), or when using the MK4505M separately.
3. This example does not show the hysterisis in the ALMOST FLAGS.

Gating Clock		Gating Operation	Flag Affected	Flag Transition	Read Locations Remaining to Empty	Write Locations Available to Full
CKR	CKW					
↑	-	READ	AE	↗	8*	1016
-	↑	WRITE	AE	↗	10	1014
↑	-	READ	AE	↘	9	1015
-	↑	WRITE	AE	↘	11	1013
↑	-	READ	AF	↗	1014	10
-	↑	WRITE	AF	↗	1016	8*
↑	-	READ	AF	↘	1013	11
-	↑	WRITE	AF	↘	1015	9
↑	-	READ	HF	↗	510	514
-	↑	WRITE	HF	↗	512	512*
↑	-	READ	HF	↘	509	515
-	↑	WRITE	HF	↘	511	513

Notes : *. Flag definition to the respective operation and clock.
1. All examples are given in reference to the flag transition point, in the direction shown, for the given clock edge and operation. The flag remains stable as long as the condition that set or cleared the flag exists in the device.
2. The table describes the number of the cycles that can be performed, including the next rising edge.
3. Remaining Read or Available Write locations at the flag transition point reflects the hysterisis inherent to the internal scheme that detects the flag status.
4. Asynchronous or simultaneous dual port operations at the flag transition point may result in a false flag status. When this occurs, the flag is evaluated and updated on the subsequent clock.

Figure 11. Simultaneous Write/Read Timing (4505M only).

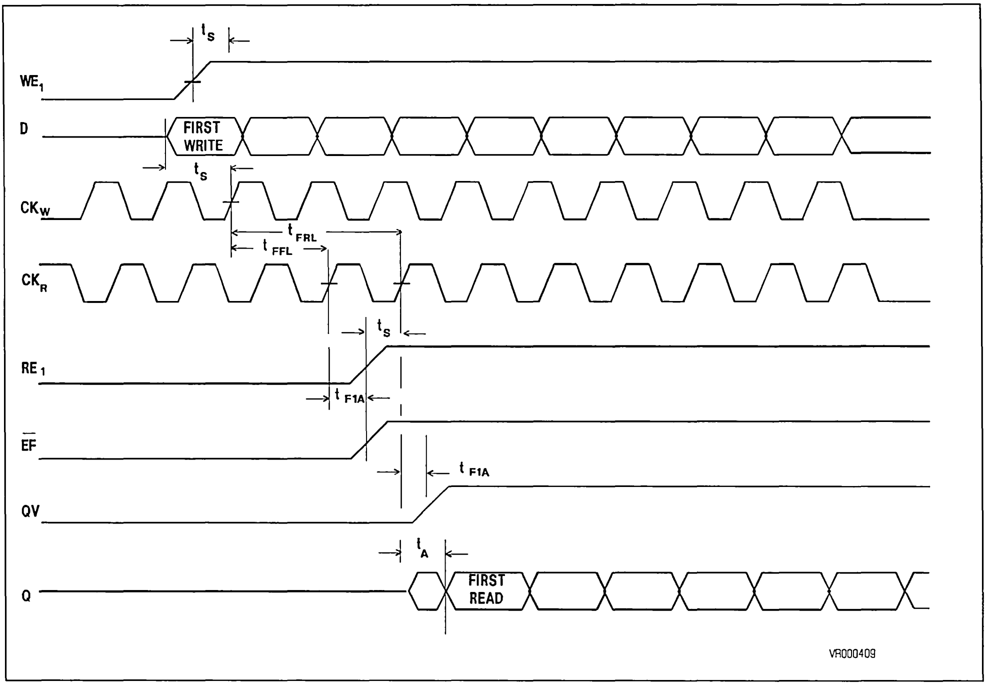
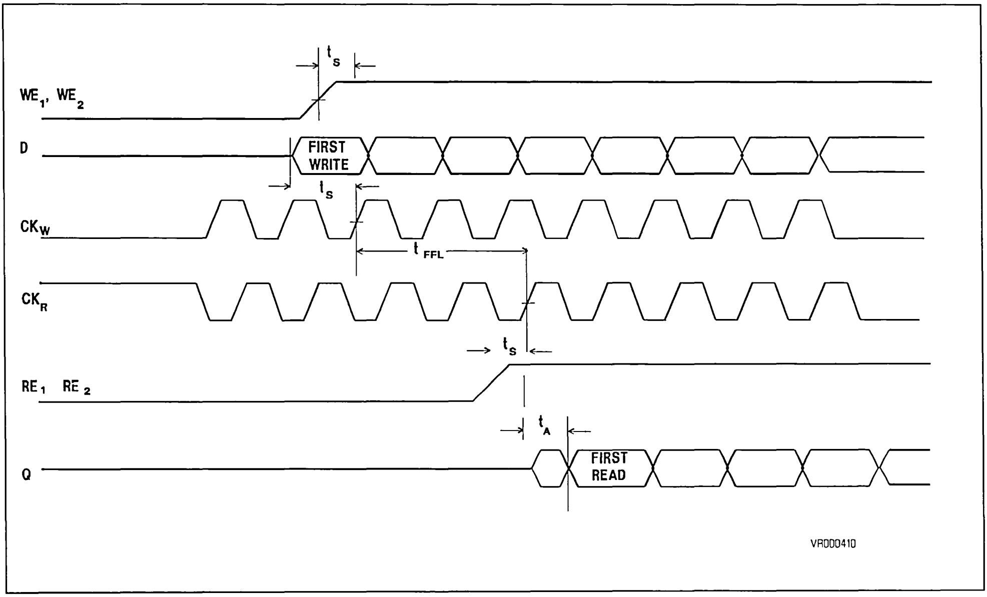

WE1
D
CKW
CKR
RE 1
EF
QV
Q
tS
tS
tFRL
tFFL
tS
tF1A
tF1A
tA
FIRST WRITE
FIRST READ
VR000409

Figure 12.. Simultaneous Write/Read Timing (4505S only).


WE1, WE2
D
CKW
CKR
RE1 RE2
Q
tS
tS
tFFL
tS
tA
FIRST WRITE
FIRST READ
VR000410

SIMULTANEOUS WRITE/READ TIMING

The Empty Flag ($\overline{EF}$) is guaranteed to clear (go HIGH) in response to the first rising edge of the read clock (CKR) to occur t_{FFL} (First Flag Latency) after a valid First Write (from the rising edge of CKW). Read clocks occurring less than t_{FFL} after a First Write may clear the $\overline{EF}$, but are not guaranteed (see Figure 10). As always, reads attempted in conjunction with an active Empty Flag are inhibited. Therefore, the next rising edge of CKR following t_{FFL} will produce the first valid read. This is the t_{FRL} (First Read Latency) pa-rameter, and must be observed for proper system operation with the latched $\overline{EF}$. Coming from an empty condition, the First Read operation should be accomplished by enabling RE1 no less than t_S before the rising edge of CKR at t_{FRL}. The Q outputs will present valid data t_A from the rising edge of CKR.

When using the MK4505S (Slave) separately, the user must observe the t_{FRL} (First Read Latency) parameter to ensure first-write-to-first-read valid data. Referring to Figure 12, the first rising edge of CKR to occur t_{FRL} after a First Write clock will guarantee valid data t_A from the rising edge of CKR. Read operations attempted before t_{FRL} is satisfied may result in reading RAM locations not yet written. Careful observance of t_{FRL} by the user is a must when using free running asynchronous read/write clocks on the MK4505S ; there is no automatic read and write protection circuitry in the Slave.

It should also be noted that the MK4505M/S has an expected "fall-through delay time" described as First Write data presented to the FIFO and clocked out to the outside world. This can be calculated as : $t_S + t_{FRL} + t_A$ (from Figure 11 or 12). Further occurring valid read clocks will present data to the Q outputs t_A from the rising edge of CKR.

WIDTH AND DEPTH EXPANSION

A single Master (MK4505M) is required for each 1K of depth configured. The number of Slaves that can be driven by a single Master is limited only by the effects of adding extra load capacitance (Write and Read Enable Input Capacitance) onto the Input Ready (DR), Output Valid (QV), Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) outputs. However, even 40 bits of width (8 devices) results in only 40pf of loading, which corresponds to the amount of load called out in the AC Test Conditions. Additional loading will slow the flags down, but as long as Enable Set Up time (t_S) is met, slowing the flags has no negative consequences.

DEPTH EXPANSION HANDSHAKE PROTOCOL

The depth expansion handshake device connections are shown in Figure 13. The expansion interface signals can be considered transparent to the user, as long as the expansion clock continues to run. The Output Ready (QV) flag, and the Data Ready (DR) flag logic descriptions are detailed in the following charts. Since the expansion clock is the read clock for the sending FIFO, as well as the write clock for the receiving FIFO, these two signals prevent data loss during depth expansion applications where the receiving bank (bank B, Figure 13) goes full simultaneously as the sending bank goes empty (bank A, Figure 13).

Before Read Clock				Operation at CKR	After Read Clock		Note
RE1	$\overline{EF}$	QV	Reads Remaining		QV	Status	
X	0	X	0	Inhibit	0	Empty	1
0	I	I	≥ 1	Hold	0	Active	2
1	1	0	1	Read	1	Empty	3
1	1	X	≥ 2	Read	1	Active	4

Notes :
1. Whenever EF is active low, further attempted read cycles are inhibited
2. QV is gated by RE1 such that the QV flag will be latched low t_{F1A} from the rising edge of CKR when RE1 is low. The RE1 input must meet the set-up time (t_S) prior to the read clock edge QV does not logically allow or prevent a read operation.
3. Whenever RE1 is active high, QV will always follows the $\overline{EF}$ signal by one read clock cycle.
4. This condition displays a typical read operation when remaining memory locations (prior to the read operation) are from 2 to 1024. $\overline{EF}$ and QV continue to acknowledge that the FIFO has more data available.

Before Write Clock				Operation at CKW	After Write Clock		Note
WE1	$\overline{FF}$	DR	Write Available		DR	Status	
X	0	0	0	No-Op	0	Full	1
0	1	0	1	No-Op	1	Full-1	2
0	1	1	1	No-Op	0	Full-1	2
1	1	X	1	Write	0	Full	1
0	1	X	2	No-Op	1	Active	3
1	1	1	2	Write	0	Full-1	4
0	1	1	≥ 3	No-Op	1	Active	
1	1	1	≥ 3	Write	1	Active	5

Notes :

1. DR can be low only when the MK4505M is full or (full-1). Whenever the device goes full ($\overline{FF}$ = low), then DR will be latched low t_{F1A} from the same write clock edge (CKW) regardless of the logic state of the DR flag at the clock transition. Further attempted write operations are blocked since FF is low.
2. If DR changes logic states after the write clock, then this example reflects the condition when the MK4505M has one (1) memory location available (full-1) DR will presume the opposite logic state of the previous cycle for subsequent write clocks if WE1 is disabled (low) and one memory location is available. Whenever the MK4505M goes full ($\overline{FF}$ = low), DR will be latched low in the same clock cycle. (This is part of the Depth Expansion Protocol, and acts to notify the sending unit that space is available.) The DR flag does not logically allow or prevent a write operation.
3. If DR is a logic 1 before and after the write clock, then this example signifies that the available memory locations in the MK4505M are greater than or equal to 2, after the completed write operation.
4. During a valid write cycle, the DR flag will go inactive low t_{F1A} from the rising edge of CK_W if the write counter is (full-2) at the clock transition. This results is a (full-1) condition. (Refer to notes 1 and 2.)
5. This condition displays a typical write cycle, where available memory locations (prior to the write operation) are from 3 to 1024. DR and $\overline{FF}$ continue to acknowledge that the FIFO is ready to accept more data.

In summary, the QV flag follows the $\overline{EF}$ signal by one read clock cycle (in all instances) when RE1 is active high at the rising edge of CKR. Whenever RE1 is disabled (low), the QV flag will go low t_{F1A} from the rising edge of CKR. Of course, the RE1 input must satisfy the set-up time (t_S) prior to CKR. The QV flag does not enable or inhibit read operations. Read protection is provided by the EF signal.

The DR flag will go low one cycle prior to a full condition (full-1), or DR will go high at (full-2) from the rising edge of CKW. However, if WE1 is disabled (low), and the device has one location available, then DR will toggle each subsequent write cycle until full. This way the device notifies the sending unit that at least one more byte of data can be accepted. When the device goes full, the DR flag will be latched low t_{F1A} from the clock edge (during the same write cycle), regardless of its previous logic state. As with all valid write cycles, the WE1 input must satisfy the set-up time (t_S) prior to CKW. The DR flag does not enable or inhibit write operations. Write protection is provided by the $\overline{FF}$ signal.

WIDTH AND DEPTH EXPANSION EXAMPLES

The width and depth expansion interface timing diagrams (Figures 14 and 15) are in reference to the width and depth expansion schematic in Figure 13 (For simplicity all clocks have the same frequency and transition rate).

Example 1 - First Write Since Empty - Reading the timing diagram from the top left to bottom right, one can determine that figure 13 illustrates the effects of the first WRITE/READ cycles from an EMPTY array of FIFOs. Both of the $\overline{EF}$ pins are initially low ($\overline{EF}_X$, $\overline{EF}$ and RE2). As data is written into Bank A, the expansion clock reads data from Bank A and writes it to Bank B, the interface $\overline{EF}$ ($\overline{EF}$ and RE2) and the external $\overline{EF}$ ($\overline{EF}_X$) go inactive (logic 1) while data is shifted through the FIFO array from Bank A through Bank B to the external output (Q0 - Q4). The $\overline{EF}$ logic goes valid (logic 0) once data is shifted out of its respective bank.

Example 2 - First Read Since Full - Reading the timing diagram from the bottom left to top right, one can determine that figure 15 illustrates the effects of the first READs from a FULL array of FIFOs. As data is read out of the system (Q0 - Q4), it allows Bank B to receive data (Q_{EXP}) shifted from Bank A. As Bank B shifts data out via Q0 - Q4, allowing Bank A to shift data into Bank B, both banks will show a cleared $\overline{FF}$ status (logic 1) on the expansion $\overline{FF}$ ($\overline{FF}$ and WE2) as well as the internal $\overline{FF}$ ($\overline{FF}_X$). When Bank A is no longer considered FULL, Data In from the system (D0 - D4) is now written into Bank A. The FIFO array is again completely Full.

APPLICATION

The MK4505 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK4505 can also interface to 5V CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK4505, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. A high frequency decoupling capacitor should be placed next to each FIFO. The capacitor should be 0.1µF or larger. Also, a pull-up resistor in the range of 1KΩ is recommended for the $\overline{\text{RESET}}$ input pin to improve proper operation.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10Ω to 33Ω often prove most suitable.

Figure 13. MK4505M/S 2K x 10 Width and Depth Expansion Schematic.

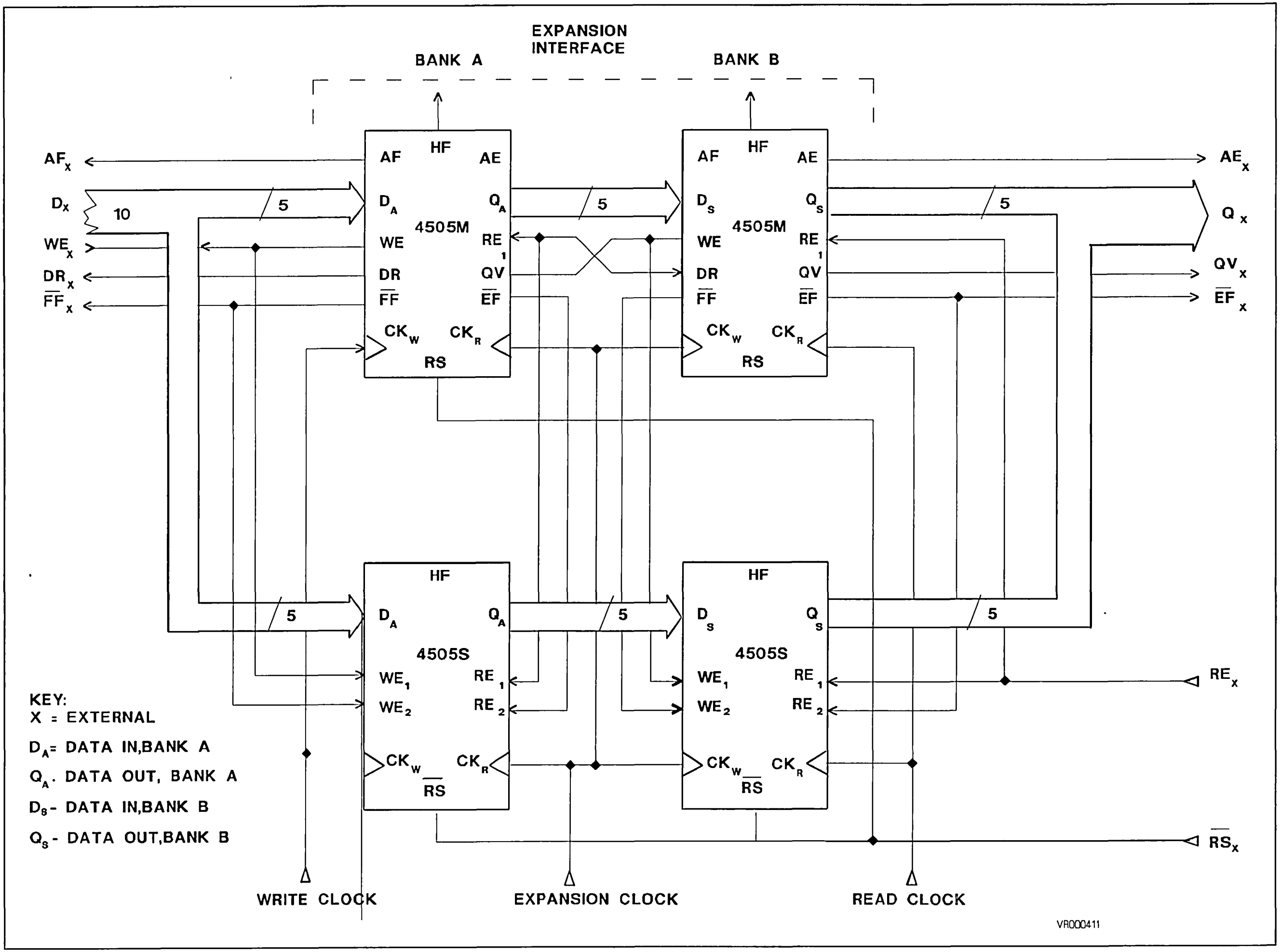
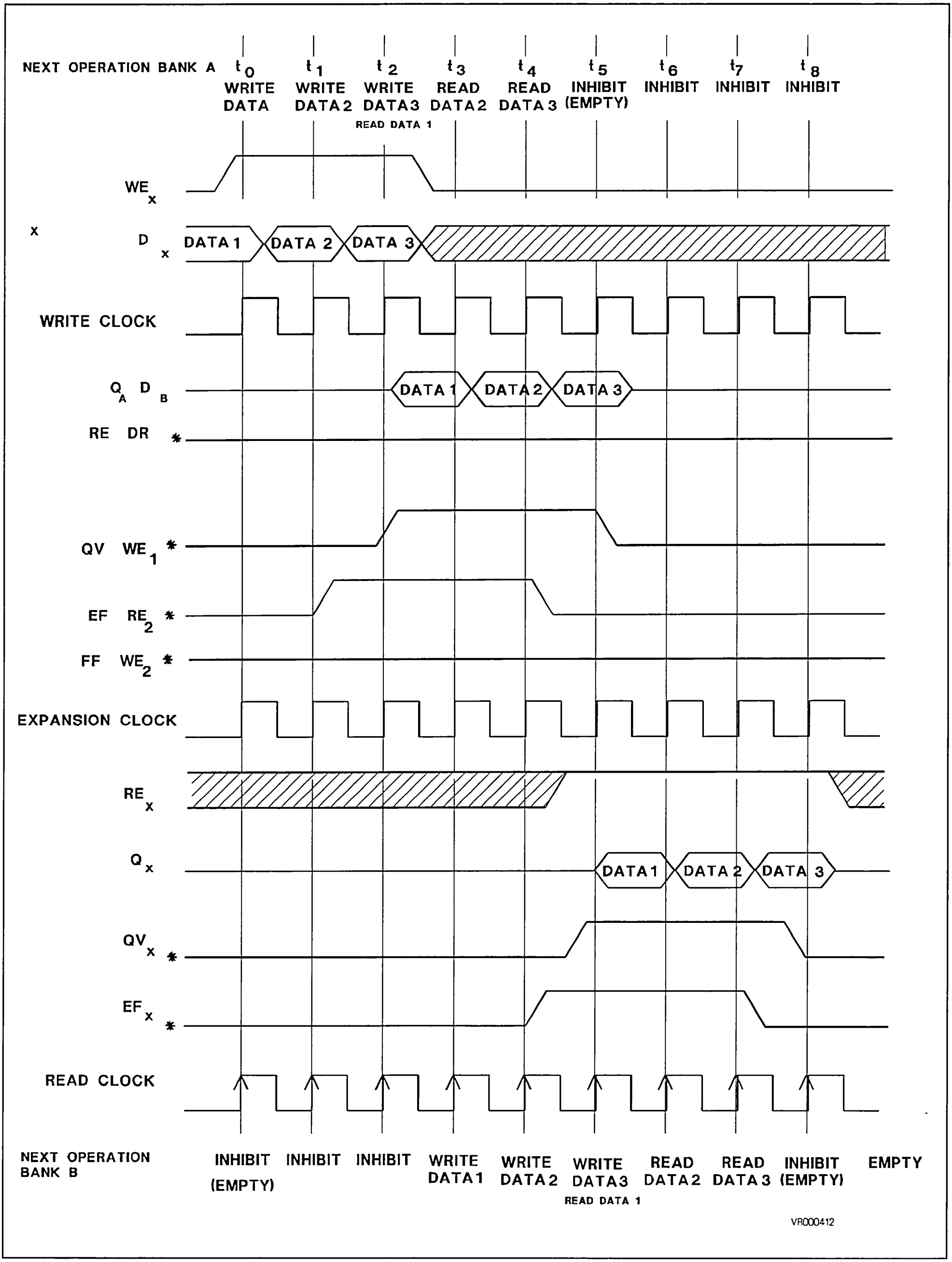
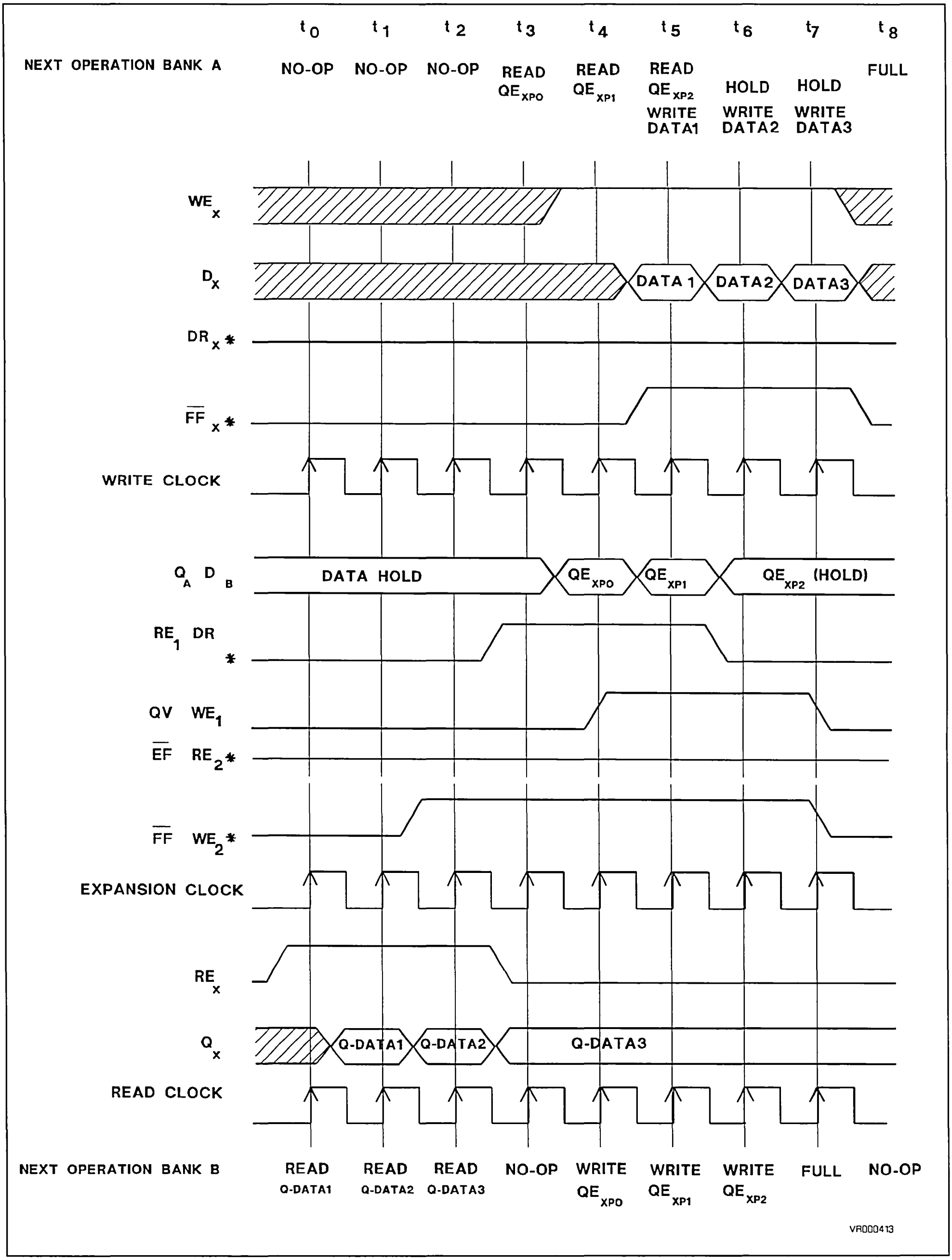

EXPANSION
INTERFACE
BANK A
BANK B
AF_X
D_X
10
WE_X
DR_X
FF_X
5
AF
HF
AE
D_A
Q_A
4505M
WE
RE 1
DR
QV
FF
EF
CK_W
CK_R
RS
D_S
Q_S
AE_X
Q_X
QV_X
EF_X
HF
4505S
WE_1
WE_2
RE_1
RE_2
RE_X
RS_X
KEY:
X = EXTERNAL
D_A= DATA IN,BANK A
Q_A. DATA OUT, BANK A
D_B- DATA IN,BANK B
Q_B- DATA OUT,BANK B
WRITE CLOCK
EXPANSION CLOCK
READ CLOCK
VR000411

Figure 14. Example 1 - Width and Depth Expansion Interface Timing.


NEXT OPERATION BANK A
t_0 WRITE DATA
t_1 WRITE DATA2
t_2 WRITE DATA3 READ DATA 1
t_3 READ DATA2
t_4 READ DATA 3
t_5 INHIBIT (EMPTY)
t_6 INHIBIT
t_7 INHIBIT
t_8 INHIBIT
WEx
Dx
DATA 1
DATA 2
DATA 3
WRITE CLOCK
QA DB
RE DR *
QV WE1 *
EF RE2 *
FF WE2 *
EXPANSION CLOCK
REx
Qx
QVx *
EFx *
READ CLOCK
NEXT OPERATION BANK B
INHIBIT (EMPTY)
INHIBIT
INHIBIT
WRITE DATA1
WRITE DATA2
WRITE DATA3 READ DATA 1
READ DATA2
READ DATA3
INHIBIT (EMPTY)
EMPTY
VR000412

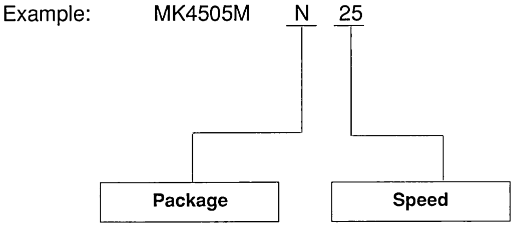
Note : *. Example begins with both banks empty, as status flags indicate.

Figure 15. Example 2 - Width and Depth Expansion Interface Timing.



t0 t1 t2 t3 t4 t5 t6 t7 t8
NEXT OPERATION BANK A
NO-OP
NO-OP
NO-OP
READ QE XPO
READ QE XP1
READ QE XP2 WRITE DATA1
HOLD WRITE DATA2
HOLD WRITE DATA3
FULL
WE x
D x
DATA 1
DATA2
DATA3
DR x *
FF x *
WRITE CLOCK
Q A D B
DATA HOLD
QE XPO
QE XP1
QE XP2 (HOLD)
RE 1 DR *
QV WE 1
EF RE 2 *
FF WE 2 *
EXPANSION CLOCK
RE x
Q x
Q-DATA1
Q-DATA2
Q-DATA3
READ CLOCK
NEXT OPERATION BANK B
READ Q-DATA1
READ Q-DATA2
READ Q-DATA3
NO-OP
WRITE QE XPO
WRITE QE XP1
WRITE QE XP2
FULL
NO-OP
VR000413

ORDERING INFORMATION



Example: MK4505M N 25

Package	
N	PSDIP20 and/or PSDIP24

Speed	
25	25ns
33	33ns
50	50ns

In a System using both M4505M and M4505S, parts should be ordered individually.

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

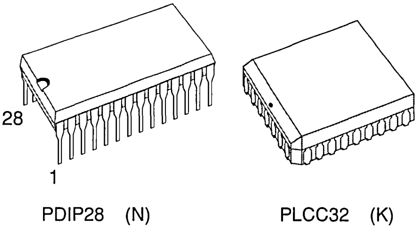
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK4501

CMOS 512 x 9 BiPORT FIFO

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 512 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE


28
1
PDIP28 (N)
PLCC32 (K)

DESCRIPTION

The MK4501 is a BiPORT™ FIFO memory, which utilizes special two-port cell tech- niques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
D0-D8	Data Inputs
Q0-Q8	Data Outputs
GND	Ground
$\overline{XI}$	Expansion Input
$\overline{XO}$	Expansion Output
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
$\overline{FL}/\overline{RT}$	First Load / Retransmit
V_{CC}/GND	5 Volts/Ground
NC	Not Connected

Figure 1. Pin Connections

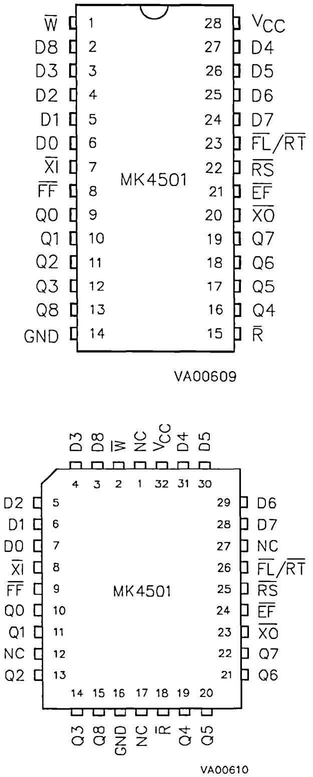
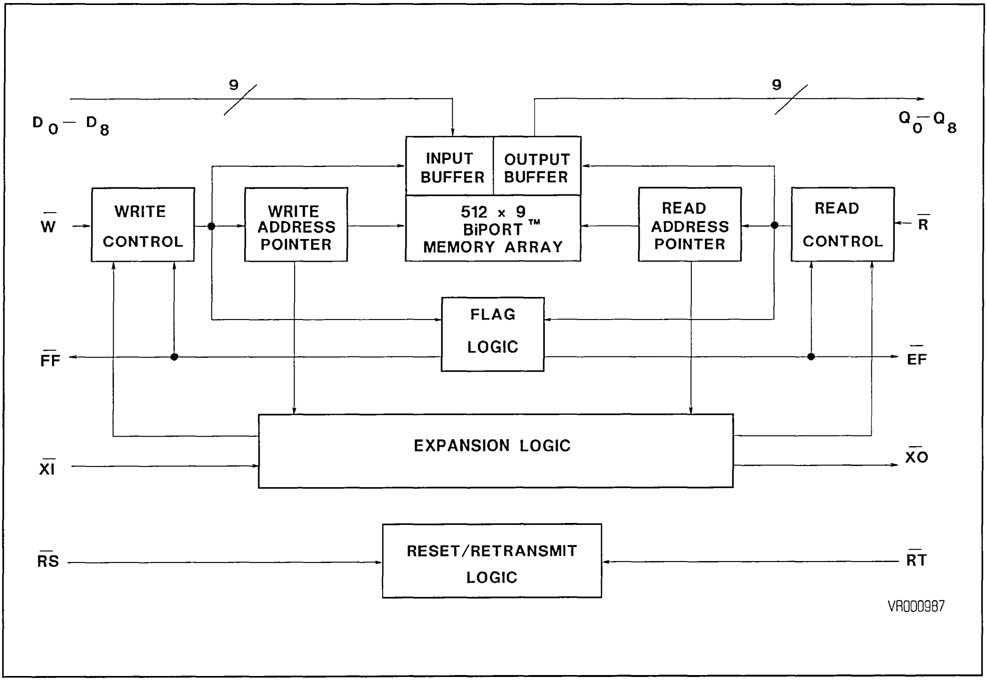

W̄ 1
D8 2
D3 3
D2 4
D1 5
D0 6
X̄Ī 7
F̄F̄ 8
Q0 9
Q1 10
Q2 11
Q3 12
Q8 13
GND 14
28 VCC
27 D4
26 D5
25 D6
24 D7
23 F̄L̄/R̄T̄
22 R̄S̄
21 ĒF̄
20 X̄Ō
19 Q7
18 Q6
17 Q5
16 Q4
15 R̄
MK4501
VA00609
D3 4
D8 3
W̄ 2
NC 1
VCC 32
D4 31
D5 30
D2 5
D1 6
D0 7
X̄Ī 8
F̄F̄ 9
Q0 10
Q1 11
NC 12
Q2 13
29 D6
28 D7
27 NC
26 F̄L̄/R̄T̄
25 R̄S̄
24 ĒF̄
23 X̄Ō
22 Q7
21 Q6
14 Q3
15 Q8
16 GND
17 NC
18 R̄
19 Q4
20 Q5
MK4501
VA00610

Figure 2. Block Diagram


9
9
$D_0 - D_8$
$Q_0 - Q_8$
INPUT BUFFER
OUTPUT BUFFER
512 x 9 BiPORT ™ MEMORY ARRAY
$\overline{W}$
WRITE CONTROL
WRITE ADDRESS POINTER
READ ADDRESS POINTER
READ CONTROL
$\overline{R}$
FLAG LOGIC
$\overline{FF}$
$\overline{EF}$
EXPANSION LOGIC
$\overline{XI}$
$\overline{XO}$
RESET/RETRANSMIT LOGIC
$\overline{RS}$
$\overline{RT}$
VR000987

INTRODUCTION (Continued)

prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4501 employs a memory-based architecture wherein a byte written into the device does not “ripple-through”. Instead, a byte written into the MK4501 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4501 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4501 allows connecting the read, write, data in, and data out lines of the MK4501s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins as appropriate (see the Expansion Timing section for a more complete discussion).

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.5	5	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" All Inputs	2.0		V_{CC} + 1	V	3
V_{IL}	Logic "0" All Inputs	–0.3		0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
I_{IL}	Input Leakage Current (Any Input)			± 1	µA	5
I_{OL}	Output Leakage Current			± 10	µA	6
V_{OH}	Output Logic 1 Voltage ($I_{OUT} = -1mA$)	2.4			V	3
V_{OL}	Output Logic 0 Voltage ($I_{OUT} = 4mA$)			0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current			80	mA	7
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)			8	mA	7
I_{CC3}	Power Down Current (all Inputs $\geq V_{CC} - 0.2V$)			500	µA	7

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Capacitance on Input Pins			7	pF	
C_Q	Capacitance on Output Pins			12	pF	8

Notes :

1. Pulse widths of less than minimum values are not valid.
2. Measured using output load shown in figure Output Load Circuit.
3. All voltages are referenced to ground.
4. 1.5 volt negativeundershoots are allowed for 10ns, once per cycle.
5. Measured with $0.4V \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4V \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open
8. With output buffer deselected.

ABSOLUTE MAXIMUM RATINGS

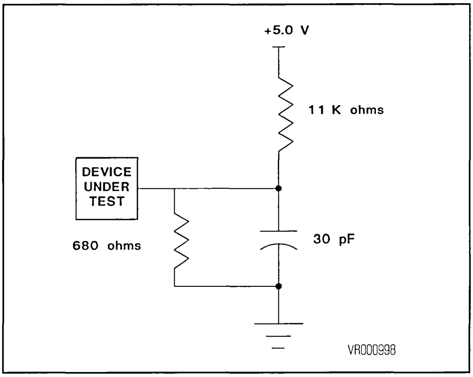
Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.5 to +7	V
T_A	Operating Temperature T_A (ambient)	0 to 70	˚C
T_{STG}	Storage Temperature	–55 to +125	˚C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current per Pin	20	mA

Note : Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

AC TEST CONDITIONS

Input Levels	GND to 3V
Transition Times	5ns
Input Signal Timing Reference Level	1.5V
Output Signal Timing Reference Level	0.8V and 2.2V
Ambient Temperature	0°C to 70°C
V_{CC}	5V ± 10%

Figure 3. Equivalent Output Load Circuit



READ MODE

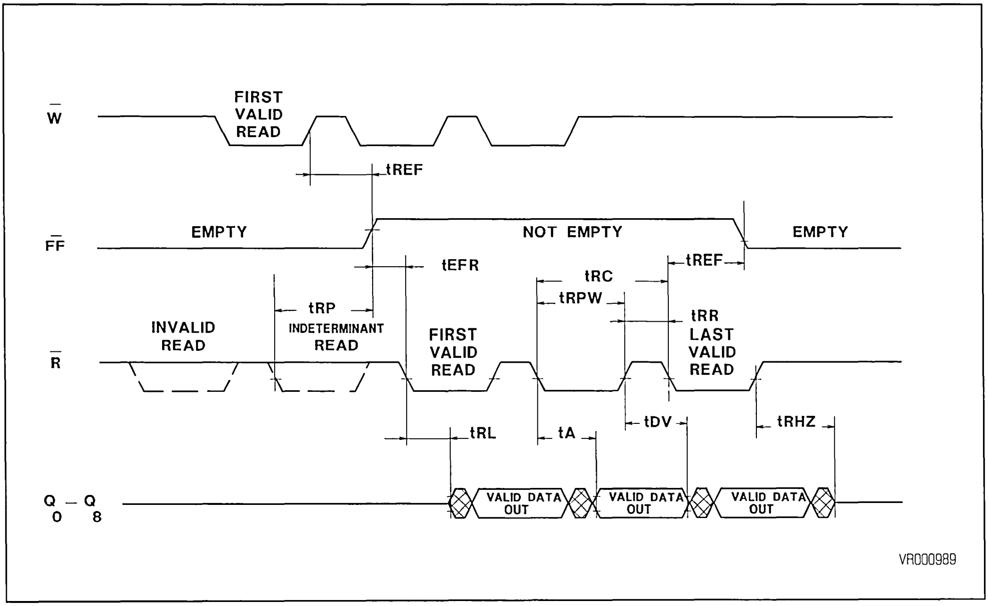
The MK4501 initiates a Read Cycle (see Figure 4a) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not set. In the Read mode of operation, the MK4501 provides a fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from High $\overline{R}$	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

Figure 4A. Read and Empty Flag Waveforms



$\overline{W}$
FIRST VALID READ
tREF
$\overline{FF}$
EMPTY
NOT EMPTY
EMPTY
tEFR
tREF
tRC
tRPW
tRP
tRR
INVALID READ
INDETERMINANT READ
FIRST VALID READ
LAST VALID READ
$\overline{R}$
tRL
tA
tDV
tRHZ
$Q_0 - Q_8$
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT
VR000989

WRITE MODE

The MK4501 initiates a Write Cycle (see Figure 4B) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not set. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4501 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	20		25		35		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		75		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		75		95		110		140		190	ns	2

Figure 4B. Write and Full Flag Waveforms

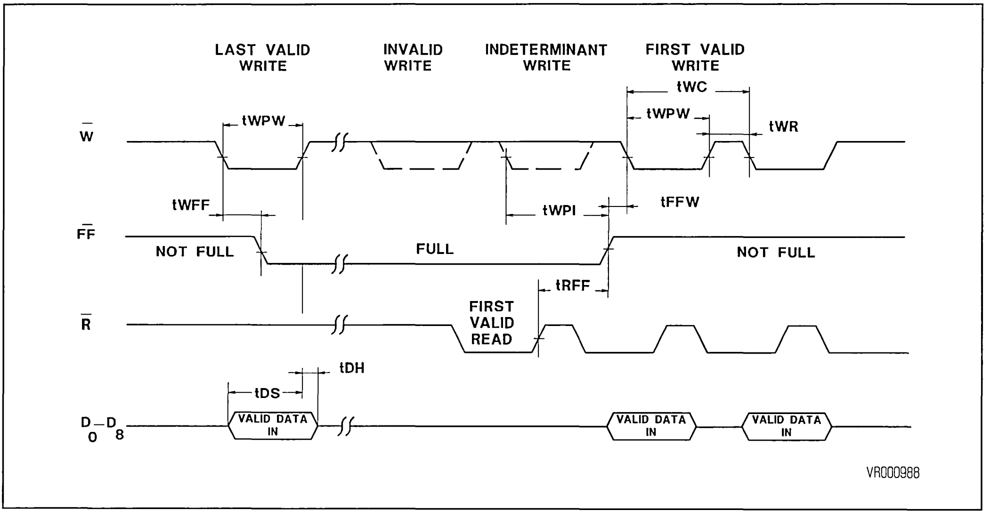

LAST VALID WRITE
INVALID WRITE
INDETERMINANT WRITE
FIRST VALID WRITE
tWC
tWPW
tWPW
tWR
W
tWFF
tWPI
tFFW
FF
NOT FULL
FULL
NOT FULL
tRFF
FIRST VALID READ
R
tDH
tDS
D0–D8
VALID DATA IN
VALID DATA IN
VALID DATA IN
VR000988

Figure 5B. Write/Read to Empty Flag Waveforms

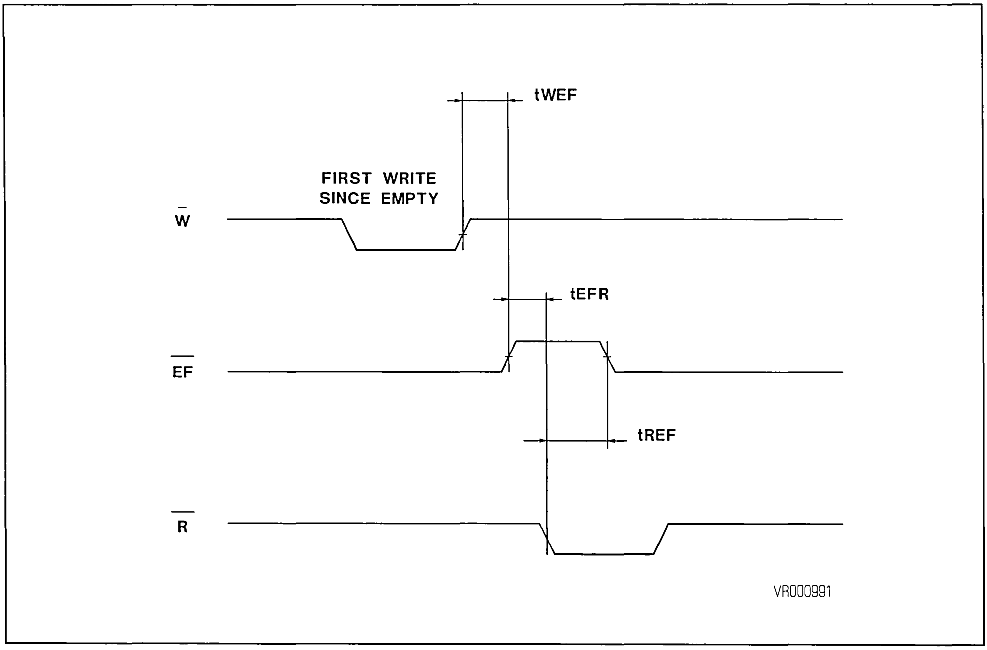
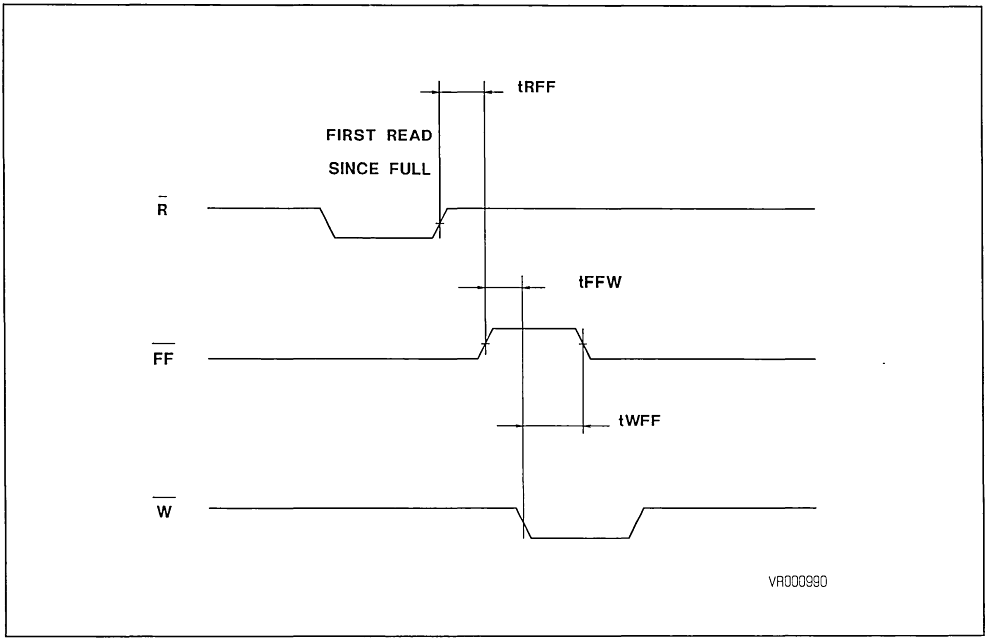

tWEF
FIRST WRITE
SINCE EMPTY
W
tEFR
EF
tREF
R
VR000991

Figure 5B. Read/Write to Full Flag Waveforms


tRFF
FIRST READ
SINCE FULL
R
tFFW
FF
tWFF
W
VR000990

RESET

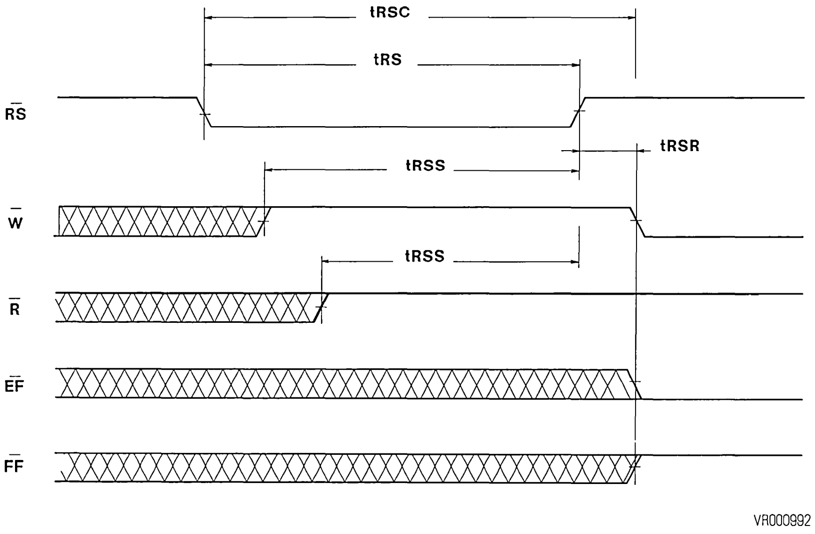
The MK4501 is reset (see Figure 6) whenever the Reset pin ($\overline{\text{RS}}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{\text{W}}$ or $\overline{\text{R}}$ need be high when $\overline{\text{RS}}$ goes low, both $\overline{\text{W}}$ and $\overline{\text{R}}$ must be high t_{RSS} before $\overline{\text{RS}}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{\text{FL}}/\overline{\text{RT}}$ and $\overline{\text{XI}}$ during Reset.

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	45		60		80		100		130		180		ns	

Figure 6. Reset Waveforms



Note : $\overline{\text{EF}}$ and $\overline{\text{FF}}$ may change status during Reset, but flags will be valid at t_{RSC}.

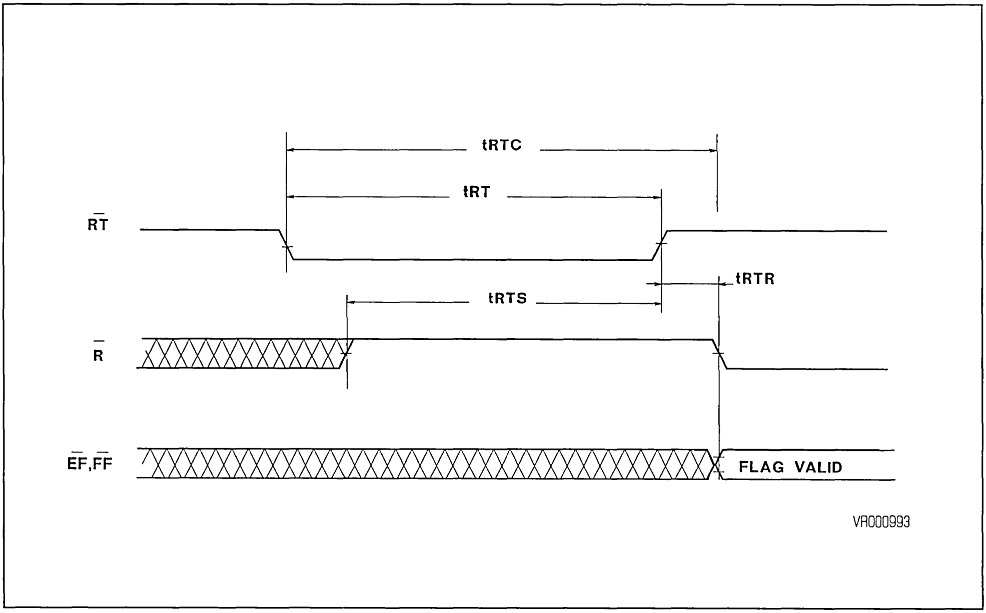
RETRANSMIT

The MK4501 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (see Figure 7).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 512 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 7. Retransmit Waveforms



Note : $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	

SINGLE DEVICE CONFIGURATION

A single MK4501 may be used when application requirements are for 512 words or less. The MK4501 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 8).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two MK4501s. Any word width can be attained by adding additional MK4501s.

Figure 8. A Single 512 x 9 FIFO Configuration

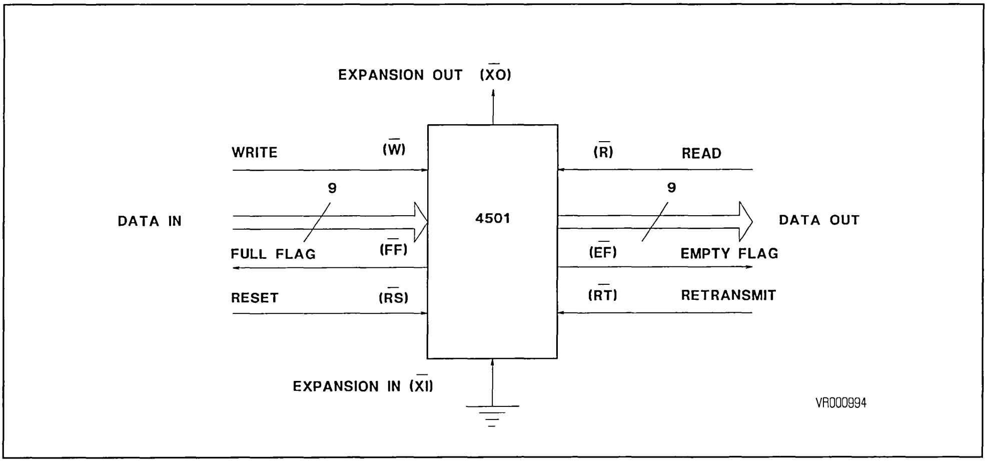
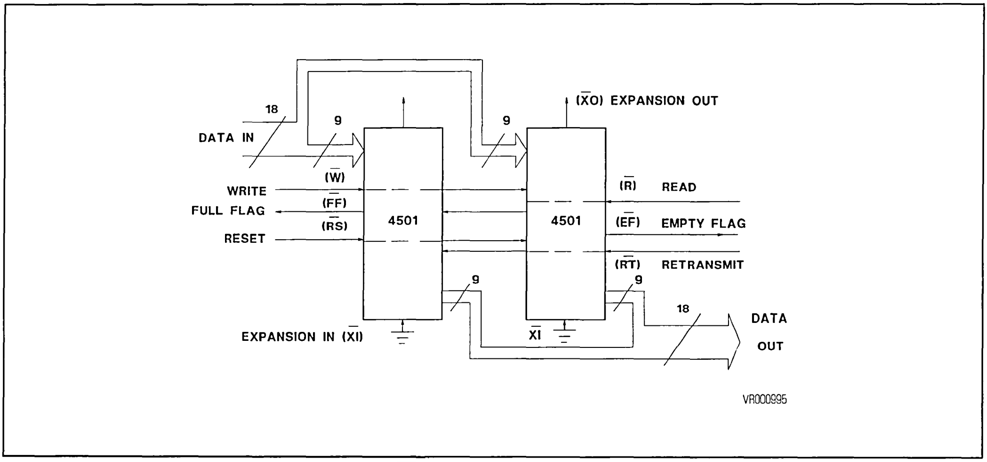

EXPANSION OUT (XO)
WRITE (W)
(R) READ
9
9
DATA IN
4501
DATA OUT
FULL FLAG (FF)
(EF) EMPTY FLAG
RESET (RS)
(RT) RETRANSMIT
EXPANSION IN (XI)
VR000994

Figure 9. A 512 x 18 FIFO Configuration (Width Expansion)


18
DATA IN
9
9
(XO) EXPANSION OUT
(W)
WRITE
(FF)
FULL FLAG
(RS)
RESET
4501
4501
(R) READ
(EF) EMPTY FLAG
(RT) RETRANSMIT
9
9
18
DATA OUT
EXPANSION IN (XI)
XI
VR000995

Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (Daisy Chain)

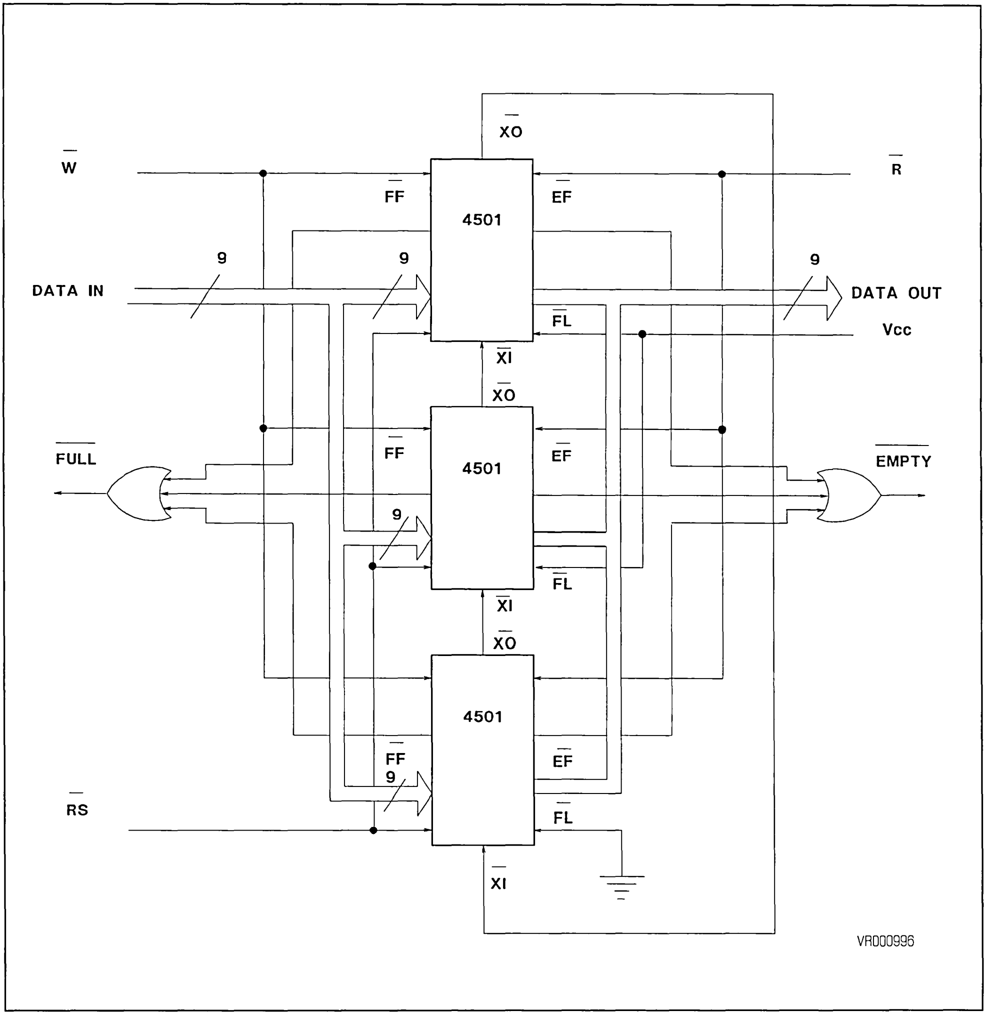
The MK4501 can easily be adapted to applications when the requirements are for greater than 512 words. Figure 10 demonstrates Depth Expansion using three MK4501s. Any depth can be attained by adding additional MK4501s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all FFs (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4501 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not valid in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.

Figure 10. A 1536 x 9 FIFO Configuration (depth expansion)

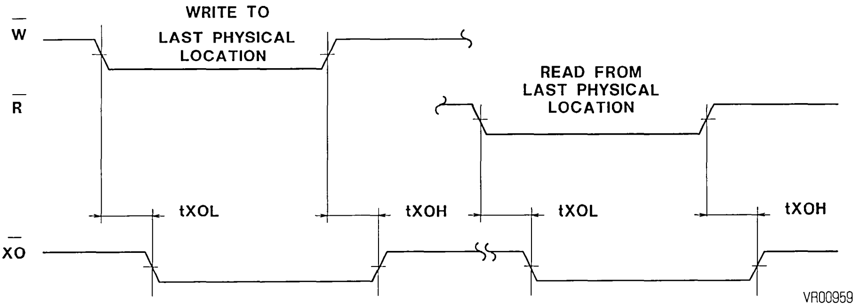

$\overline{XO}$
$\overline{W}$
$\overline{R}$
$\overline{FF}$
$\overline{EF}$
4501
9
9
9
DATA IN
DATA OUT
$\overline{FL}$
Vcc
$\overline{XI}$
$\overline{XO}$
$\overline{FULL}$
$\overline{FF}$
$\overline{EF}$
4501
$\overline{EMPTY}$
9
$\overline{FL}$
$\overline{XI}$
$\overline{XO}$
4501
$\overline{FF}$
9
$\overline{EF}$
$\overline{RS}$
$\overline{FL}$
$\overline{XI}$
VR000996

EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In as much as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 11. Expansion Out Timing Waveforms

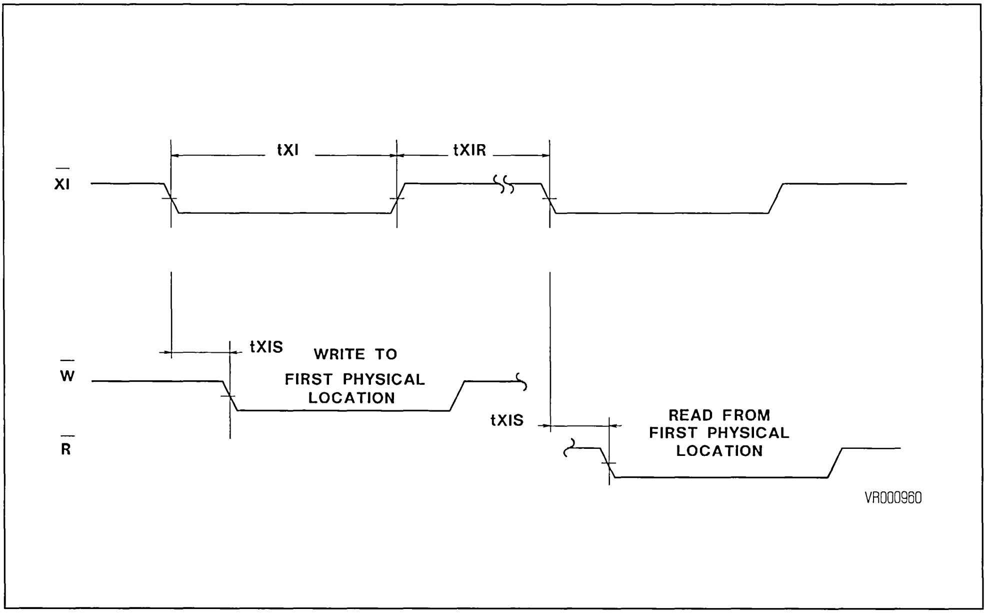

W̄
WRITE TO LAST PHYSICAL LOCATION
R̄
READ FROM LAST PHYSICAL LOCATION
tXOL
tXOH
tXOL
tXOH
X̄O
VR00959

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4501 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4501 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 12. Expansion In Timing Waveforms


tXI
tXIR
$\overline{XI}$
tXIS
WRITE TO FIRST PHYSICAL LOCATION
$\overline{W}$
tXIS
READ FROM FIRST PHYSICAL LOCATION
$\overline{R}$
VR000960

AC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	25		30		45		50		60		85		ns	

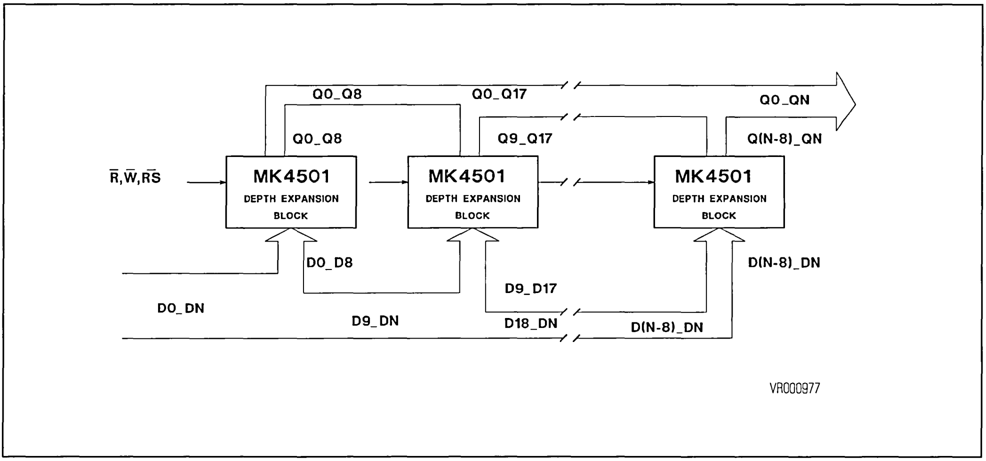
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 13).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4501s, as shown in Figure 14. Care must be taken to ensure that the appropriate flag is monitored by each system. (i.e., $\overline{\text{FF}}$ is monitored on the device where $\overline{\text{W}}$ is used ; $\overline{\text{EF}}$ is monitored on the device where $\overline{\text{R}}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

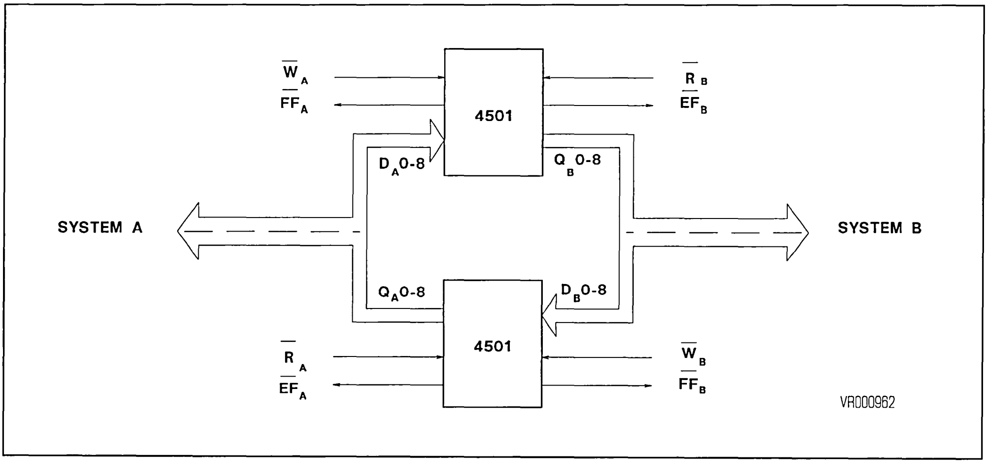
Figure 13. Compound FIFO Expansion Configuration


Q0_Q8
Q0_Q17
Q0_QN
Q0_Q8
Q9_Q17
Q(N-8)_QN
R,W,RS
MK4501
DEPTH EXPANSION
BLOCK
MK4501
DEPTH EXPANSION
BLOCK
MK4501
DEPTH EXPANSION
BLOCK
D0_D8
D(N-8)_DN
D9_D17
D0_DN
D9_DN
D18_DN
D(N-8)_DN
VR000977

Notes :

1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 9.

Figure 14. Bidirectional FIFO Application


W A
FF A
4501
R B
EF B
D A 0-8
Q B 0-8
SYSTEM A
SYSTEM B
Q A 0-8
D B 0-8
4501
R A
EF A
W B
FF B
VR000962

ORDERING INFORMATION

Example: MK4501 N 65

Package	
N	PDIP28
K	PLCC32

Speed	
65	65ns
80	80ns
10	100ns
12	120ns
15	150ns
20	200ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

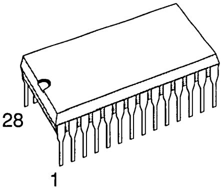
For further information on any aspect of this device, please contact our Sales Office nearest you.

SGS-THOMSON
MICROELECTRONICS

MK4503

CMOS 2K x 9 BiPORT FIFO

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 2048 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BI-DIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE
- HALF FULL FLAG IN SINGLE DEVICE MODE



PDIP28 (N)

DESCRIPTION

The MK4503 is a BiPORT™ FIFO memory, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asyn-chronous Read/Write operations, full, half full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4503 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals).

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
$\overline{FL}/\overline{RT}$	First Load / Retransmit
D0-D8	Data Inputs
Q0-Q8	Data Outputs
$\overline{XI}$	Expansion Input
$\overline{XO}/\overline{HF}$	Expansion Output / Half Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
V_{CC}	5 Volts
GND	Ground
NC	Not Connected

Figure 1. Pin Connection

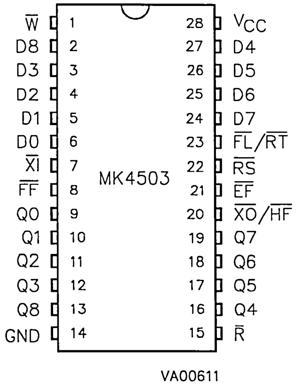
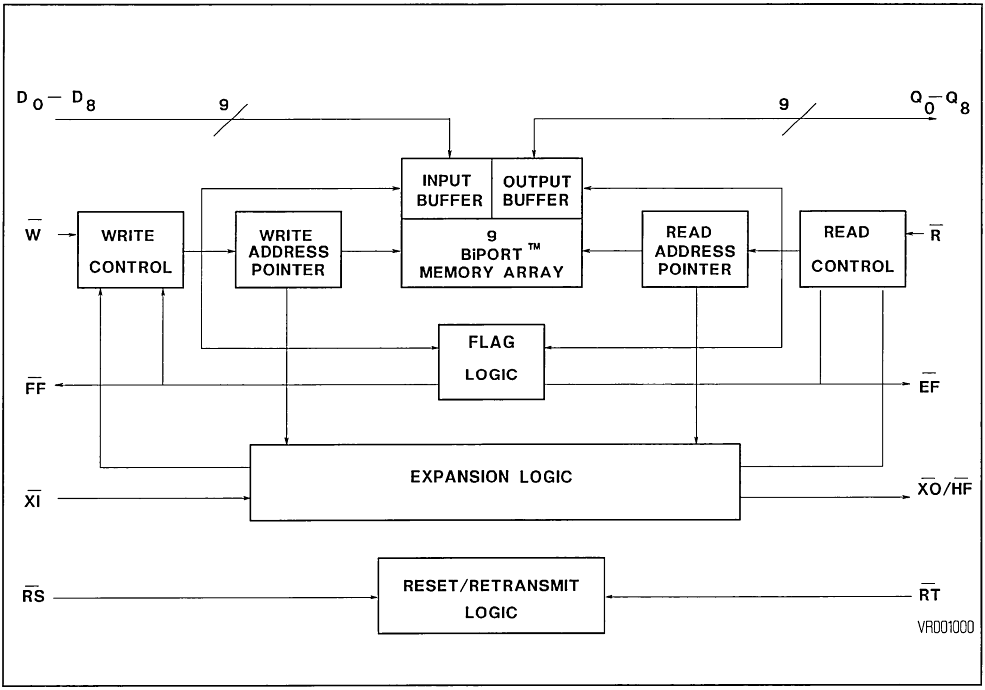

W̅ 1
D8 2
D3 3
D2 4
D1 5
D0 6
X̅I̅ 7
F̅F̅ 8
Q0 9
Q1 10
Q2 11
Q3 12
Q8 13
GND 14
28 VCC
27 D4
26 D5
25 D6
24 D7
23 F̅L̅/R̅T̅
22 R̅S̅
21 E̅F̅
20 X̅O̅/H̅F̅
19 Q7
18 Q6
17 Q5
16 Q4
15 R̅
MK4503
VA00611

Figure 2. Block Diagram



DESCRIPTION (Continued)

The full, half full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4503 employs a memory-based architecture wherein a byte written into the device does not “Ripple-Through”. Instead, a byte written into the MK4503 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Twin internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

The address pointers automatically loop back to address zero after reaching address 2047. The empty/half full and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4503 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4503 allows connecting the read, write, data in, and data out lines of the MK4503s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	–0.5 to +7	V
T_A	Ambiant Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current per Pin	20	mA

Note : Stresses above those listed under "Absolute Maximum Ratings" may be cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage all Inputs	2.2		V_{CC} + 0.3	V	3, 9
V_{IL}	Logic "0" Voltage all Inputs	–0.3		0.8	V	3, 4, 9

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
I_{IL}	Input Leakage Current (any input)			± 1	µA	5
I_{OL}	Output Leakage Current			± 10	µA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = –1mA	2.4			V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA			0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current			120	mA	7
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})			12	mA	7
I_{CC3}	Power Down Current (all inputs ≥ V_{CC} –0.2V)			4	µA	7

CAPACITANCE

(T_A = 25°C, f = 1 MHZ)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Capacitance on Input Pins			7	pF	
C_O	Capacitance on Output Pins			12	pF	8

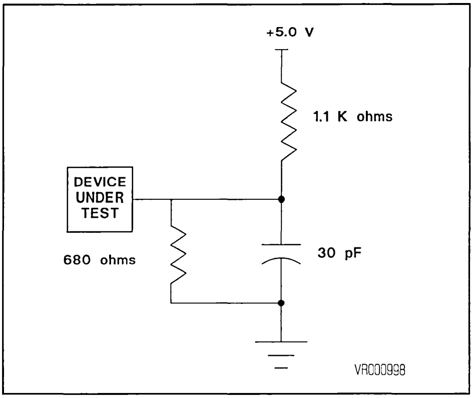
Notes :

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Circuit.
3. All voltages are referenced to ground.
4. - 1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.0 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.0 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. Input levels tested at 500ns cycle time.

AC TEST CONDITIONS

Input Levels	GND to 3V
Transition Times	5ns
Input Signal Timing Reference Level	5V
Output Signal Timing Reference Level	0.8V and 2.2V
Ambient Temperature	0°C to 70°C
V_{CC}	5V ± 10%

Figure 3. Equivalent Output Load Circuit

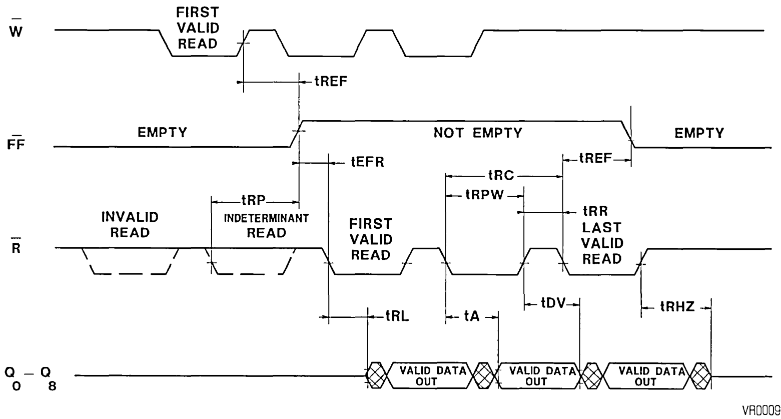


READ MODE

The MK4503 initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4503 provides a fast access to data from 9 of 18432 locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see Figure 6B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4. Read And Empty Flag Waveforms



AC ELECTRICAL CHARACTERISTICS

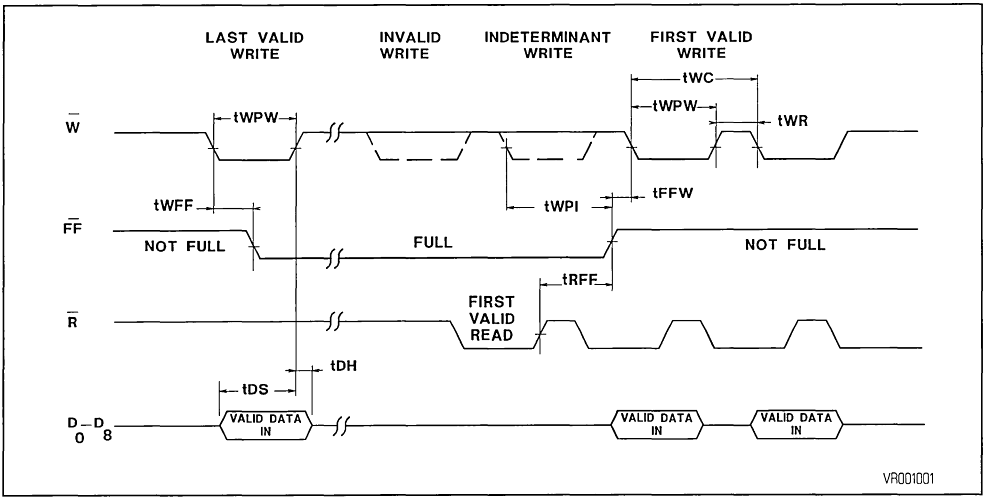
(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

WRITE MODE

The MK4503 initiates a Write Cycle (see Figure 5) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4503 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 6A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

Figure 5. Write And Full Flag Waveforms


LAST VALID WRITE
INVALID WRITE
INDETERMINANT WRITE
FIRST VALID WRITE
tWC
tWPW
tWPW
tWR
W
tWFF
tWPI
tFFW
FF
NOT FULL
FULL
NOT FULL
tRFF
FIRST VALID READ
R
tDH
tDS
D0–D8
VALID DATA IN
VALID DATA IN
VALID DATA IN
VR001001

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set-Up Time	30		40		40		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		70		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		70		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant		35		35		35		35		35		35	ns	2

Figure 6A. Read/Write To Full Flag Waveforms

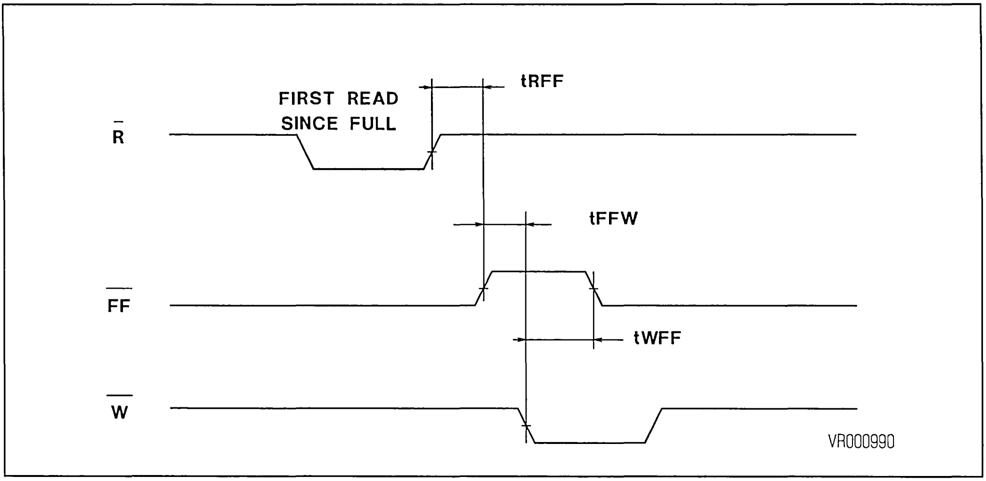
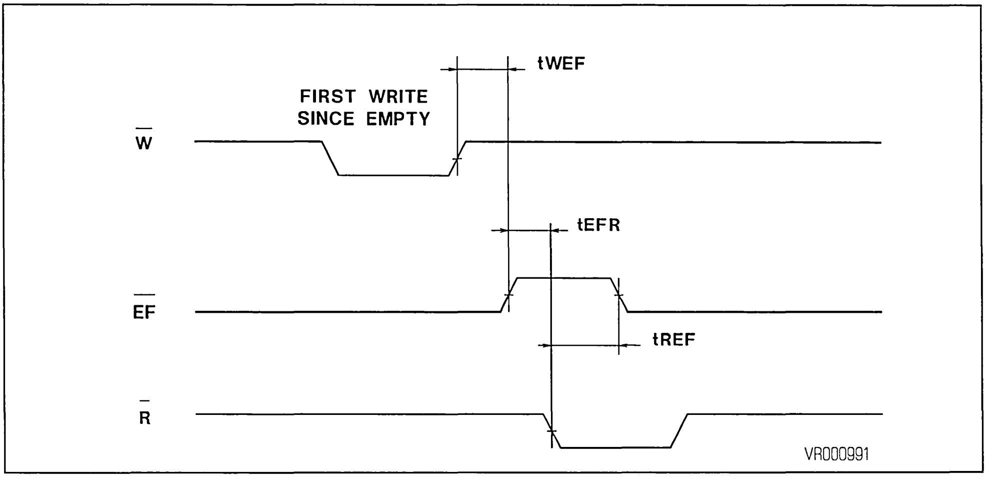

tRFF
FIRST READ
SINCE FULL
R
tFFW
FF
tWFF
W
VR000990

Figure 6B. Write/Read To Empty Flag Waveforms

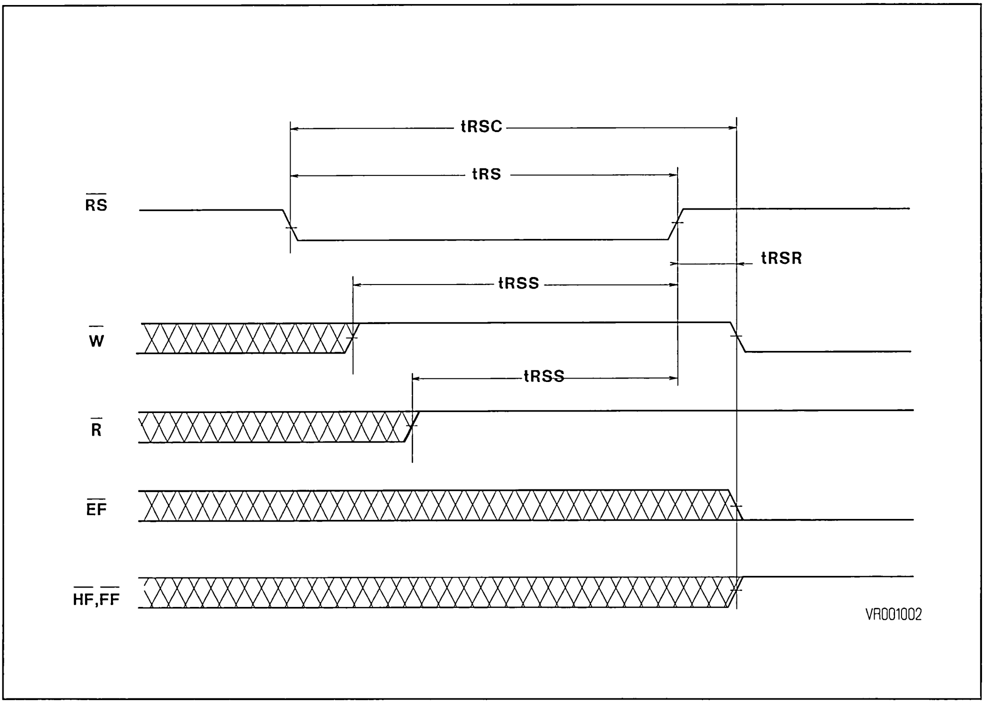

tWEF
FIRST WRITE
SINCE EMPTY
W
tEFR
EF
tREF
R
VR000991

RESET

The MK4503 is reset (see Figure 7) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 7. Reset Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set-Up Time	45		60		80		100		130		180		ns	

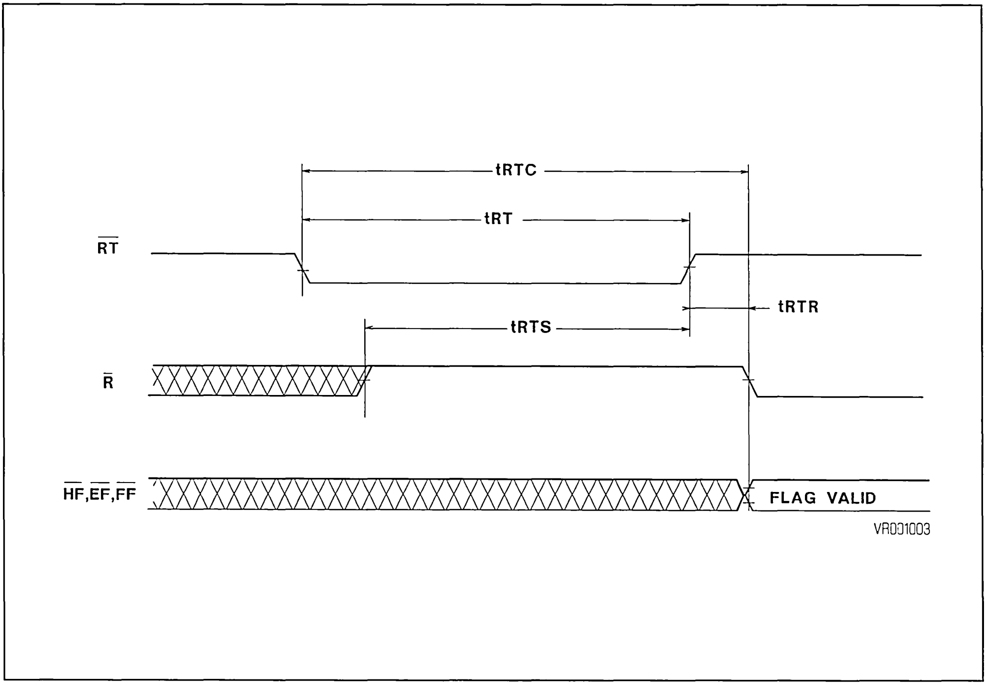
RETRANSMIT

The MK4503 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 8).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8. Retransmit Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Set-Up Time	45		60		80		100		130		180		ns	

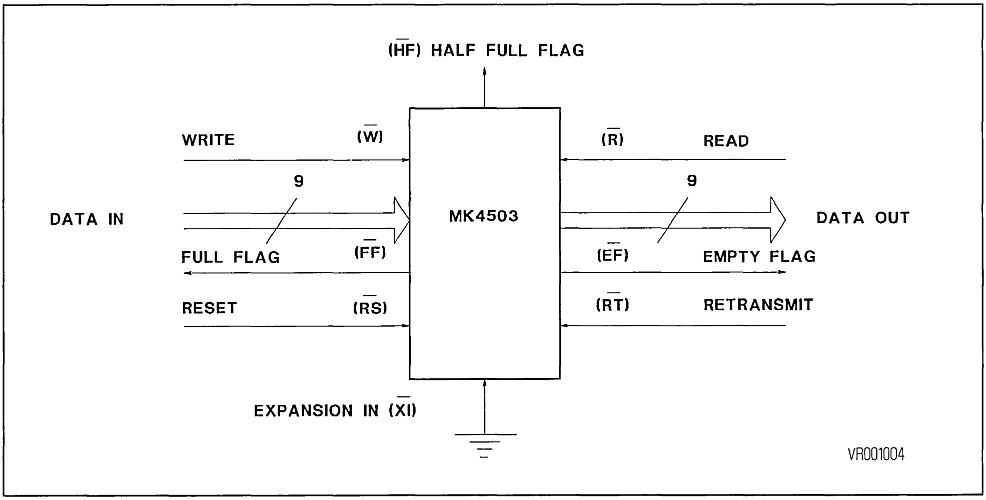
SINGLE DEVICE CONFIGURATION

A single MK4503 may be used when application requirements are for 2048 words or less. The MK4503 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 9).

WIDTH EXPANSION

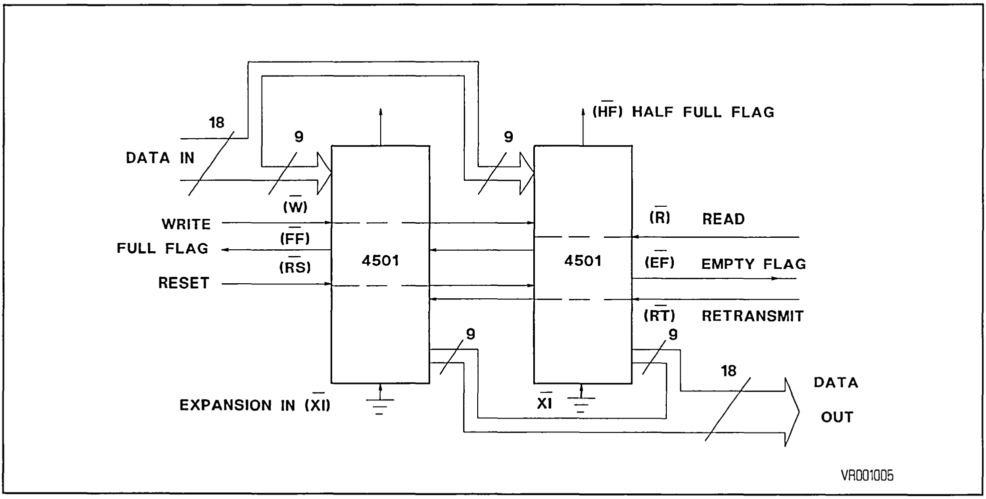
Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK4503s. Any word width can be attained by adding additional MK4503s. The half full flag ($\overline{HF}$) operates the same as in the single device configuration.

Figure 9. A Single 2047 x 9 FIFO Configuration



(HF) HALF FULL FLAG
WRITE
(W)
(R)
READ
9
9
DATA IN
MK4503
DATA OUT
FULL FLAG
(FF)
(EF)
EMPTY FLAG
RESET
(RS)
(RT)
RETRANSMIT
EXPANSION IN (XI)
VR001004

Figure 10. A 2048 x 18 FIFO Configuration (width expansion)



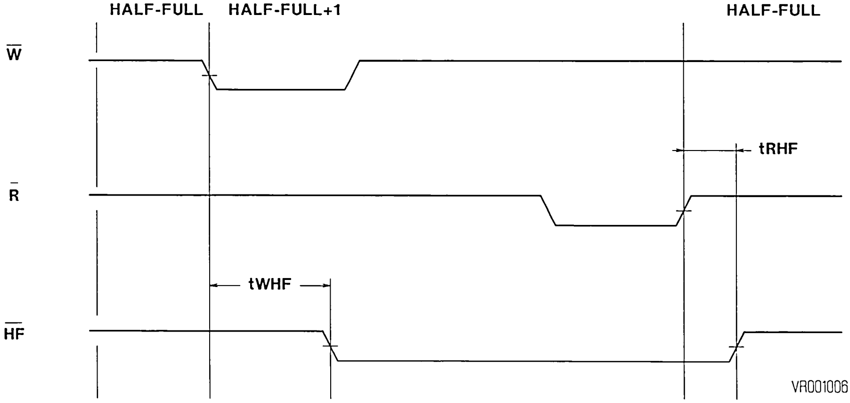
18
DATA IN
9
9
(HF) HALF FULL FLAG
(W)
WRITE
(FF)
FULL FLAG
(RS)
RESET
4501
4501
(R)
READ
(EF)
EMPTY FLAG
(RT)
RETRANSMIT
9
9
18
DATA
OUT
EXPANSION IN (XI)
XI
VR001005

Note : Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation (see Figure 11).

Figure 11. Half Full Flag Waveforms



AC CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WHF}	Write Low to Half Full Flag Low		80		100		120		140		175		235	ns
t_{RHF}	Read High to Half Full Flag High		80		100		120		140		175		235	ns

DEPTH EXPANSION (Daisy Chain)

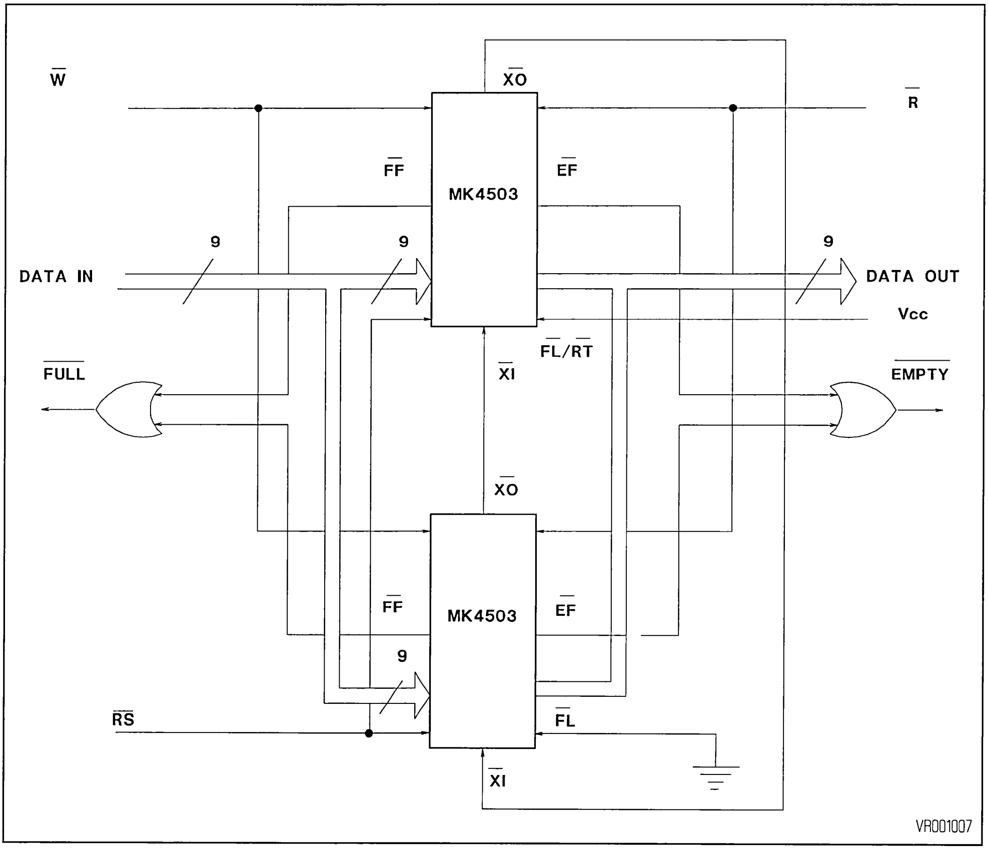
The MK4503 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 12 demonstrates Depth Expansion using the MK4503s. Any depth can be attained by adding additional MK4503s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{\text{EF}}$s and the ORing of all $\overline{\text{FF}}$s (i.e., all must be set to generate the correct composite $\overline{\text{FF}}$ or $\overline{\text{EF}}$).

The MK4503 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{\text{FL}}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{\text{FL}}$ in the high state.
3. The Expansion Out ($\overline{\text{XO}}$) pin of each device must be tied to the Expansion In ($\overline{\text{XI}}$) pin of the next device. The Half Full Flag ($\overline{\text{HF}}$) is disabled in this mode.

Figure 12. A 4K x 9 FIFO Configuration (Depth Expansion)



EXPANSION TIMING

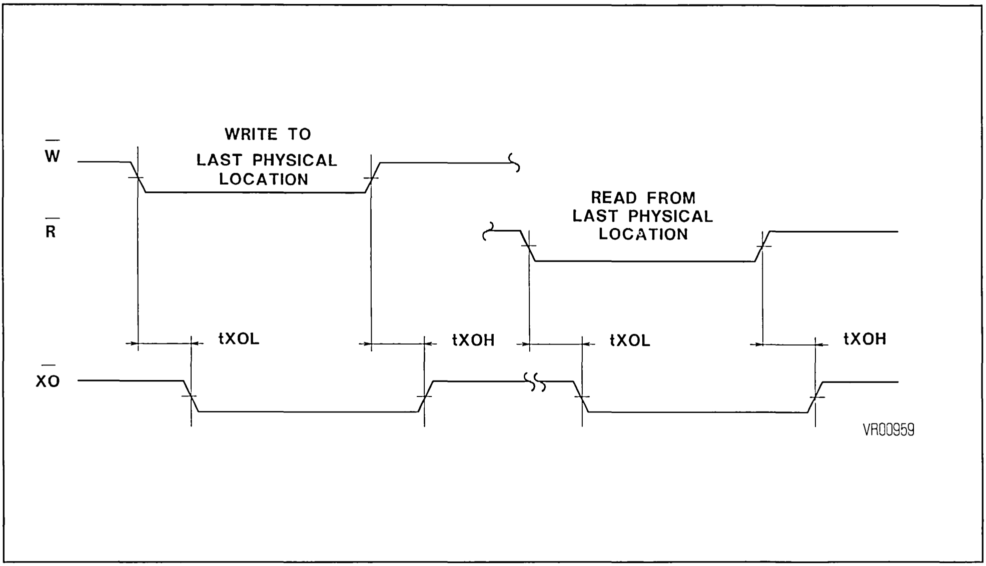
Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. In as much as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}$/$\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given MK4503 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4503 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs.

It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 13. Expansion Out Waveforms

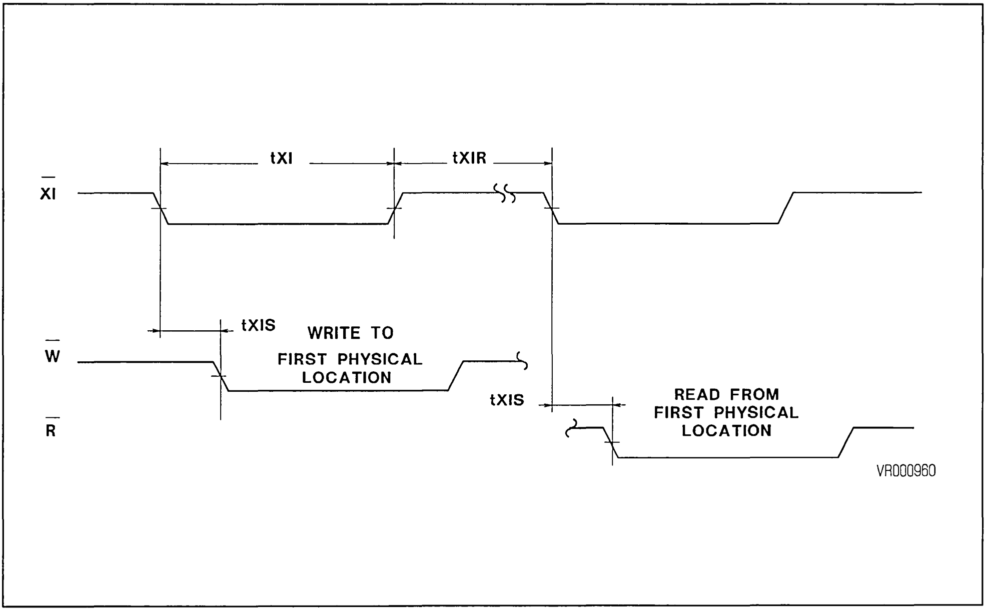


AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns

Figure 14. Expansion In Waveforms


tXI
tXIR
XI
tXIS
WRITE TO FIRST PHYSICAL LOCATION
W
tXIS
READ FROM FIRST PHYSICAL LOCATION
R
VR000960

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ± 10%)

Symbol	Parameter	-65		-80		-10		-12		-15		-20		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion in Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion in Set-up Time	25		30		45		50		60		85		ns	

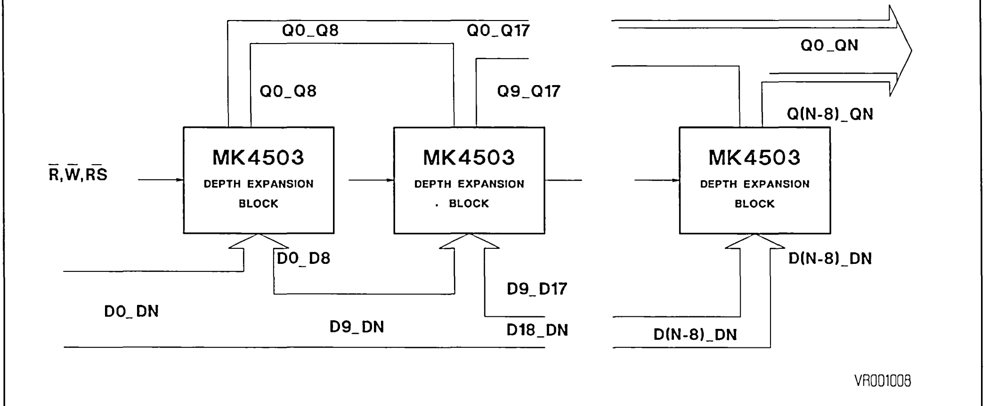
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each capable of READ and WRITE operations), can be achieved by pairing MK4503s, as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

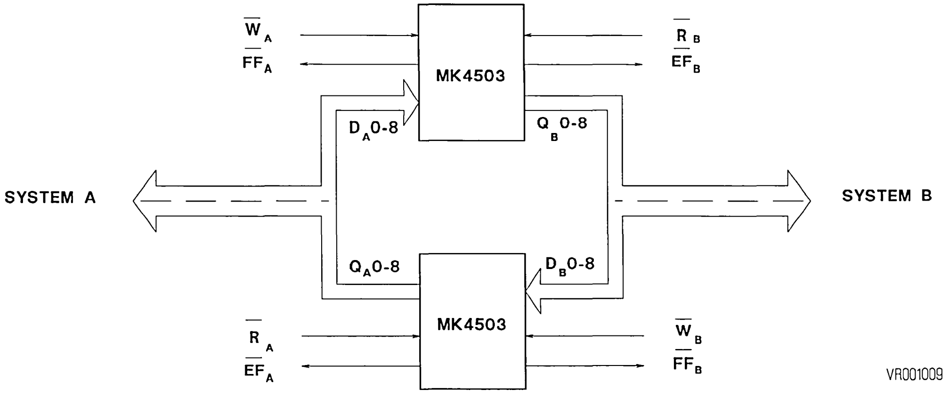
Figure 15. Compound FIFO Expansion Configuration


Q0_Q8
Q0_Q17
Q0_QN
Q0_Q8
Q9_Q17
Q(N-8)_QN
R,W,RS
MK4503
DEPTH EXPANSION
BLOCK
MK4503
DEPTH EXPANSION
BLOCK
MK4503
DEPTH EXPANSION
BLOCK
D0_D8
D(N-8)_DN
D9_D17
D0_DN
D9_DN
D18_DN
D(N-8)_DN
VR001008

Notes :

1. For depth expansion block see DEPTH EXPANSION Section and Figure 12.
2. For Flag operation see WIDTH EXPANSION Section and Figure 10.

Figure 16. Bidirectional FIFO Application


W_A
FF_A
R_B
EF_B
MK4503
D_A0-8
Q_B0-8
SYSTEM A
SYSTEM B
Q_A0-8
D_B0-8
MK4503
R_A
EF_A
W_B
FF_B
VR001009

ORDERING INFORMATION

Example: MK4503 N 65

Package	
N	PDIP28

Speed	
65	65ns
80	80ns
10	100ns
12	120ns
15	150ns
20	200ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

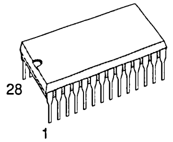
For further information on any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

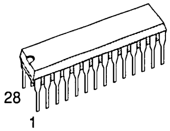
MK45H01,02,03
MK45H11,12,13

VERY FAST CMOS 512 / 1K / 2K x 9 BiPORT FIFO

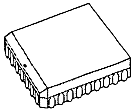
- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE x 9 ORGANIZATIONS:
  - MK45H01,11 (512 x 9)
  - MK45H02,12 (1K x 9)
  - MK45H03,13 (2K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE



PDIP28 (N)



PSDIP28 (N)



PLCC32 (K)

DESCRIPTION

The MK45H01,11,02,12,03,13 are BiPORT™ FIFO memories from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow.

PIN NAMES

$\overline{\text{W}}$	Write
$\overline{\text{R}}$	Read
$\overline{\text{RS}}$	Reset
D0-D8	Data Inputs
Q0-Q8	Data Outputs
$\overline{\text{FL}}/\overline{\text{RT}}$	First Load / Retransmit
$\overline{\text{XI}}$	Expansion Input
$\overline{\text{XO}}/\overline{\text{HF}}$	Expansion Output / Half-full Flag
$\overline{\text{FF}}$	Full Flag
$\overline{\text{EF}}$	Empty Flag
V_{CC}, GND	5 Volts, Ground
NC	Not Connected

Figure 1. Pin Connections

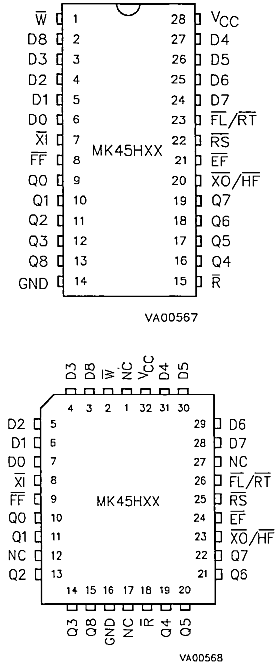
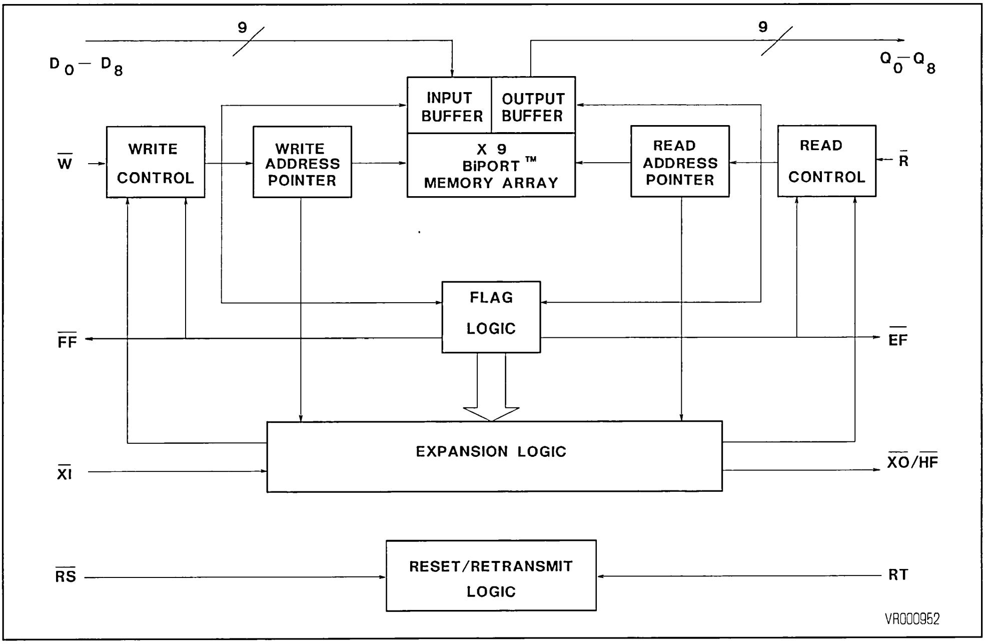

W 1
D8 2
D3 3
D2 4
D1 5
D0 6
XI 7
FF 8
Q0 9
Q1 10
Q2 11
Q3 12
Q8 13
GND 14
28 VCC
27 D4
26 D5
25 D6
24 D7
23 FL/RT
22 RS
21 EF
20 XO/HF
19 Q7
18 Q6
17 Q5
16 Q4
15 R
MK45HXX
VA00567
D3 D8 W NC VCC D4 D5
4 3 2 1 32 31 30
D2 5
D1 6
D0 7
XI 8
FF 9
Q0 10
Q1 11
NC 12
Q2 13
29 D6
28 D7
27 NC
26 FL/RT
25 RS
24 EF
23 XO/HF
22 Q7
21 Q6
MK45HXX
14 15 16 17 18 19 20
Q3 Q8 GND NC R Q4 Q5
VA00568

Figure 2. Block Diagram


9
9
$D_0 - D_8$
$Q_0 - Q_8$
INPUT BUFFER
OUTPUT BUFFER
$\overline{W}$
WRITE CONTROL
WRITE ADDRESS POINTER
X 9 BiPORT ™ MEMORY ARRAY
READ ADDRESS POINTER
READ CONTROL
$\overline{R}$
FLAG LOGIC
$\overline{FF}$
$\overline{EF}$
EXPANSION LOGIC
$\overline{XI}$
$\overline{XO}/\overline{HF}$
$\overline{RS}$
RESET/RETRANSMIT LOGIC
RT
VR000952

DESCRIPTION (Continued)

The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of $\overline{W}$ (write), and $\overline{R}$ (read) input pins. Separate data in (D0-D8) and data out (Q0-Q8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45HX1, MK45HX2, and MK45HX3 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit ($\overline{RT}$) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45HX1, MK45HX2, and MK45HX3 employ a memory-based architecture wherein a byte written into the device does not “ripple through”. Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (512, 1024, or 2048). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location.

FUNCTIONAL DESCRIPTION (Continued)

As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

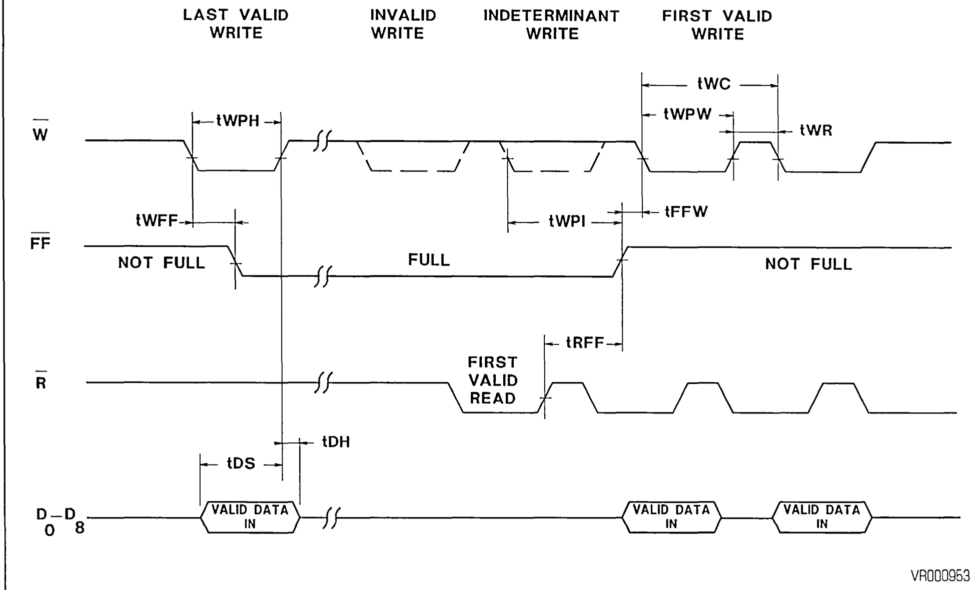
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45HX1, MK45HX2, and MK45HX3 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows the connection of the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45HXX initiates a Write Cycle (see Figure 3) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not set. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is set during the last valid write as the MK45H03 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 5). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on the internal flag status.

Figure 3. Write and Full Flag Waveforms



Write and Full Flag AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

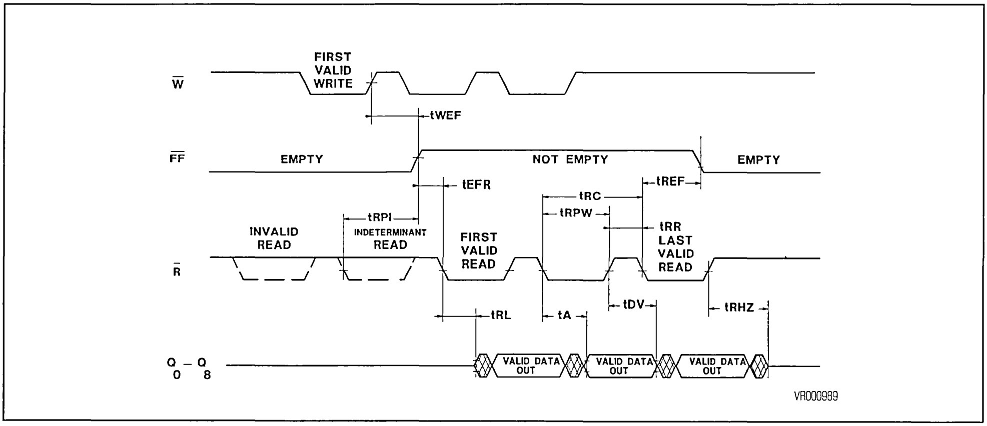
Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		25		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		25		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

READ MODE

The MK45HXX initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not set. In the read mode of operation, the MK45H0X provides fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation. In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data inputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see Figure 6). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more that t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less then t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4. Read and Empty Flag Waveforms


$\overline{W}$
FIRST VALID WRITE
tWEF
$\overline{FF}$
EMPTY
NOT EMPTY
EMPTY
tEFR
tREF
tRC
tRPW
tRPI
INVALID READ
INDETERMINANT READ
FIRST VALID READ
tRR
LAST VALID READ
$\overline{R}$
tRL
tA
tDV
tRHZ
Q0 – Q8
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT
VR000989

Read and Empty Flag AC Operating Conditions
($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		25		35		40		60		60	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		25		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

Figure 5. Read/Write to Full Flag Waveforms

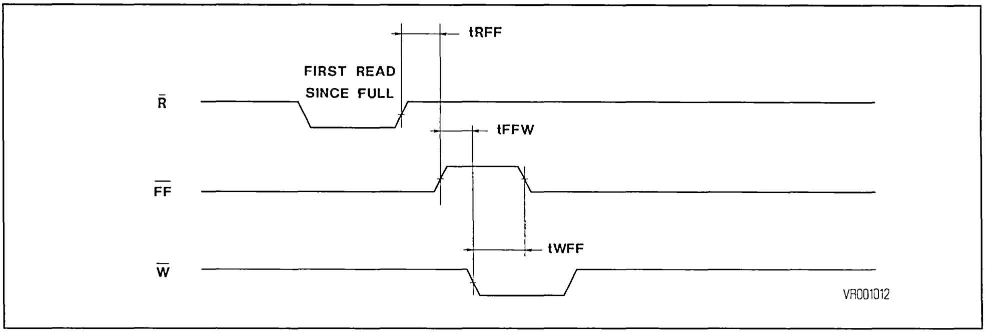
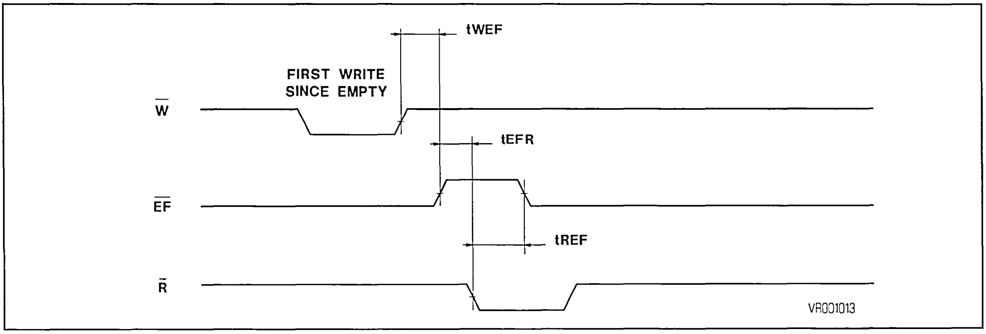

tRFF
FIRST READ SINCE FULL
R̄
tFFW
FF̄
tWFF
W̄
VR001012

Figure 6. Write/Read to Empty Flag Waveforms

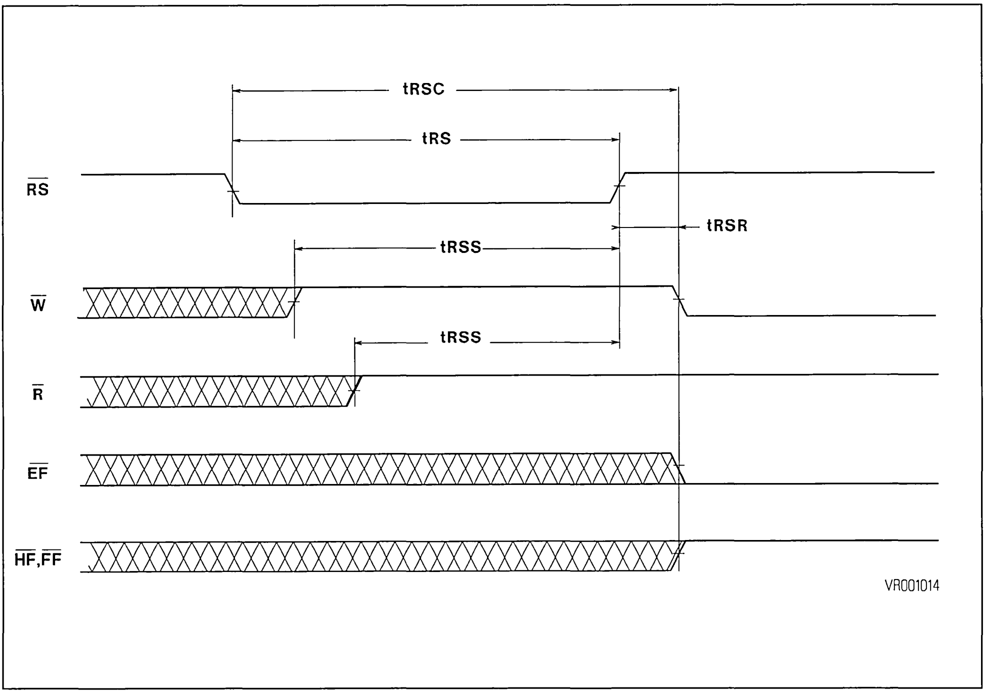

tWEF
FIRST WRITE SINCE EMPTY
W̄
tEFR
EF̄
tREF
R̄
VR001013

RESET

The MK45HXX is reset (see Figure 7) whenever the Reset pin ($\overline{\text{RS}}$) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{\text{W}}$ or $\overline{\text{R}}$ need be high when $\overline{\text{RS}}$ goes low, both $\overline{\text{R}}$ and $\overline{\text{W}}$ must be high t_{RSS} before $\overline{\text{RS}}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{\text{FL}}/\overline{\text{RT}}$ and $\overline{\text{XI}}$ during Reset.

Figure 7. Reset Waveforms



Note : $\overline{\text{HF}}$, $\overline{\text{EF}}$ and $\overline{\text{FF}}$ may change status during Reset, but flags will be valid at t_{RSC}.

Reset AC Operating Conditions (0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

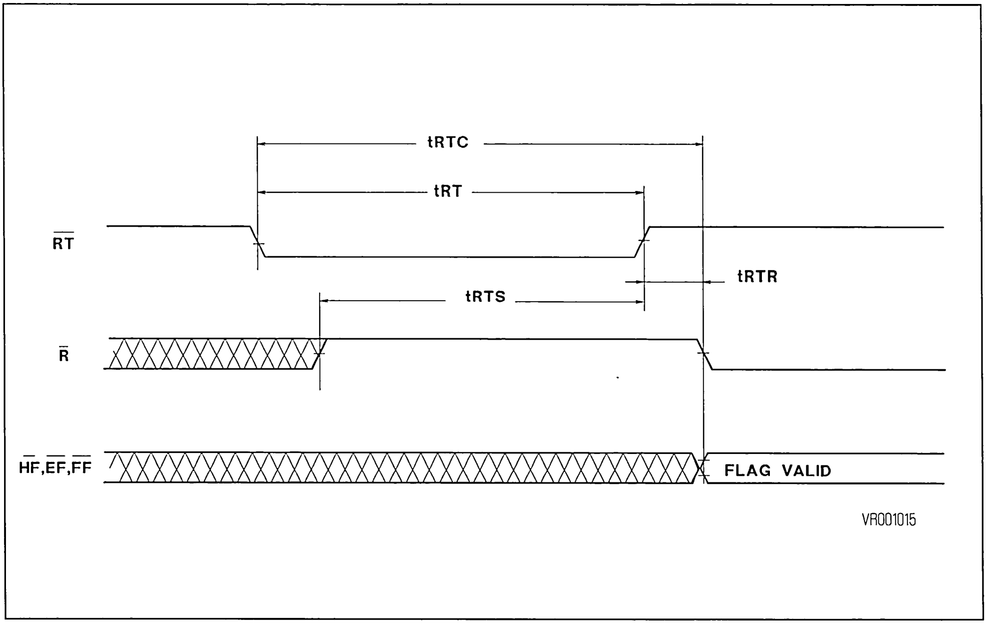
Note: 1. Pulse widths less than minimum values are not allowed

RETRANSMIT

The MK45HXX can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 8). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8. Retransmit Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Retransmit AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		50		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Set Up Time	25		30		30		45		100		ns	

Note: 1. Pulse widths less that minimum values are not allowed

SINGLE DEVICE CONFIGURATION

A single MK45HXX may be used when application requirements are for a depth of the device depth or less. The MK45HXX is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 9).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK45HXXs. Any word width can be attained by adding additional MK45HXXs. The half full flag ($\overline{HF}$) operates the same as in single device configuration.

Figure 9. A Single MK45HXX FIFO Configuration

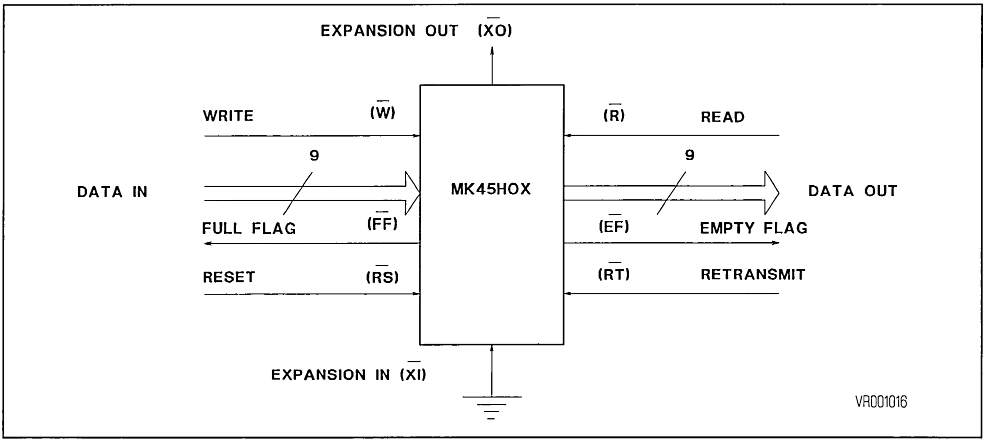
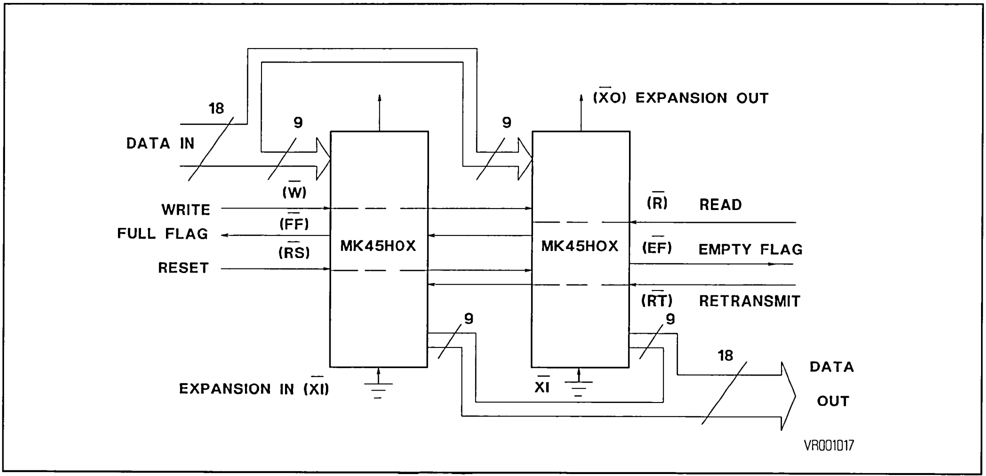

EXPANSION OUT (XO)
WRITE
(W)
(R)
READ
9
9
DATA IN
MK45HOX
DATA OUT
FULL FLAG
(FF)
(EF)
EMPTY FLAG
RESET
(RS)
(RT)
RETRANSMIT
EXPANSION IN (XI)
VR001016

Figure 10. A Two Device Width Expansion FIFO Configuration


18
DATA IN
9
9
(XO) EXPANSION OUT
(W)
WRITE
(FF)
FULL FLAG
(RS)
RESET
MK45HOX
MK45HOX
(R)
READ
(EF)
EMPTY FLAG
(RT)
RETRANSMIT
9
9
18
DATA
OUT
EXPANSION IN (XI)
XI
VR001017

Note : Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

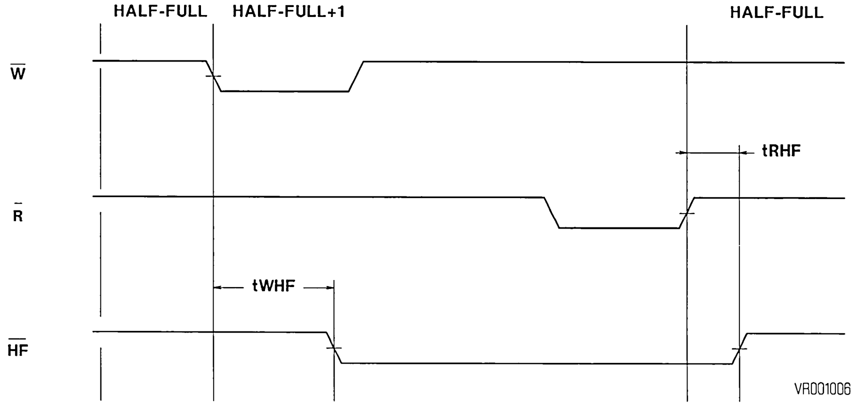
When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation (see Figure 11).

DEPTH EXPANSION (Daisy Chain)

The MK45HXX can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 12 demonstrates Depth Expansion using two MK45HXXs. Any depth can be attained by adding additional MK45HXXs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the $\overline{EF}$s and the ORing of all the $\overline{FF}$s (i.e., all must be set to generate the composite $\overline{FF}$ or $\overline{EF}$).

Figure 11. Half Full Flag Waveforms



Half Full Flag AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

The MK45HXX operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions :

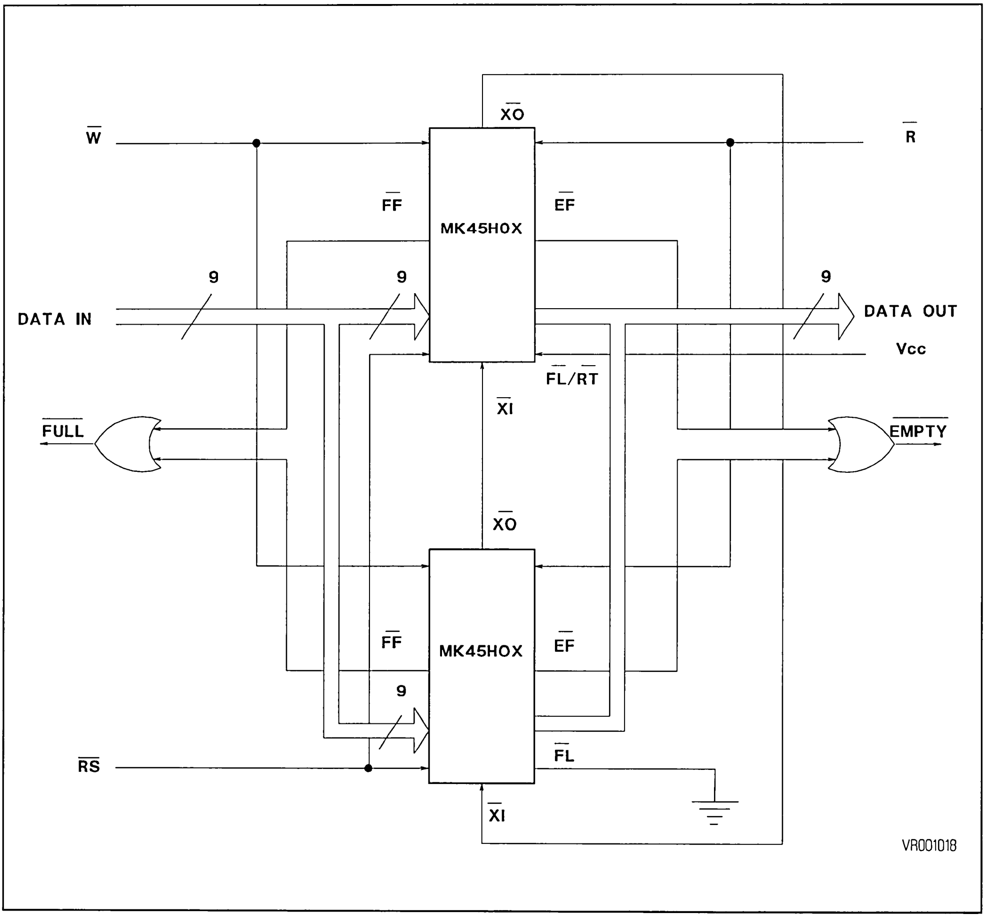
1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not available in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

EXPANSION TIMING

Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Due to the fact that Expansion Out pins are generally connected only to Expansion In pins, the user does not need to be concerned with the actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

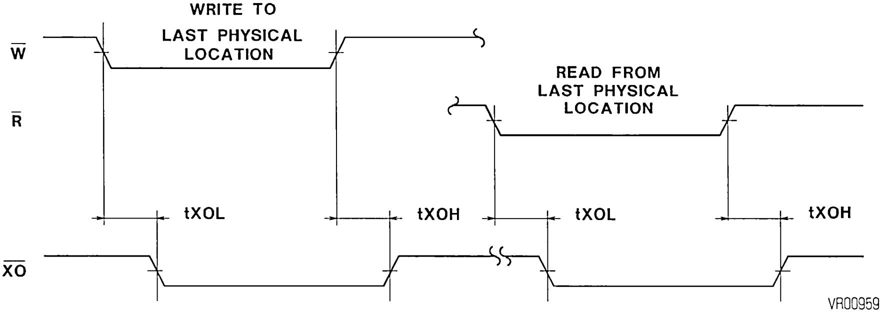
Expansion Out pulses are the identical to the WRITE and READ signals but ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

Figure 12. A Two Device Depth Expansion Configuration



When in Depth Expansion mode, a given MK45HXX will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK45HXX in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 13. Expansion Out Waveforms

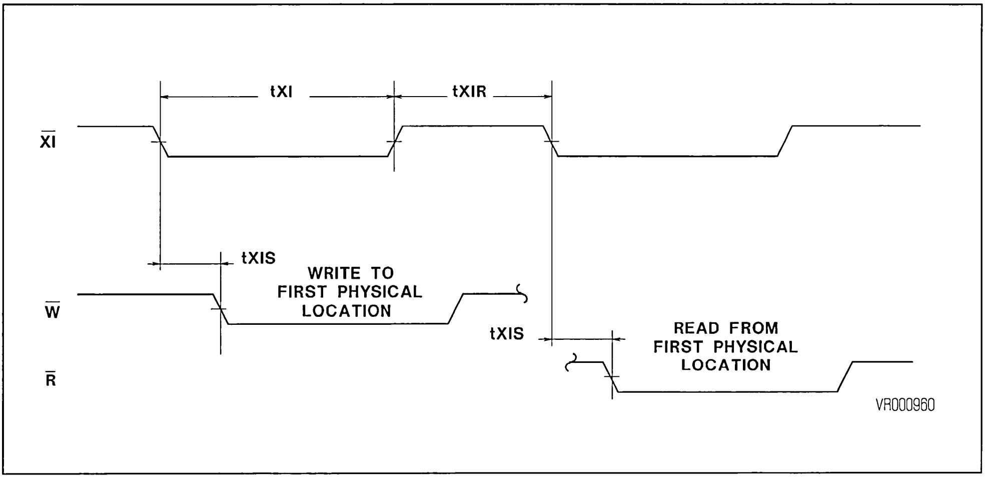

WRITE TO LAST PHYSICAL LOCATION
W
R
READ FROM LAST PHYSICAL LOCATION
tXOL
tXOH
tXOL
tXOH
XO
VR00959

Expansion Out AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

Figure 14. Expansion In Waveforms


tXI
tXIR
XI
tXIS
WRITE TO FIRST PHYSICAL LOCATION
W
tXIS
READ FROM FIRST PHYSICAL LOCATION
R
VR000960

Expansion In AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion In Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion In Setup Time	15		15		15		15		15		ns	

Note: 1. Pulse widths less than minimum values are not allowed

COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK45HXXs, as shown in Figure 16. Care must be taken to ensure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 15. Compound FIFO Expansion Configuration

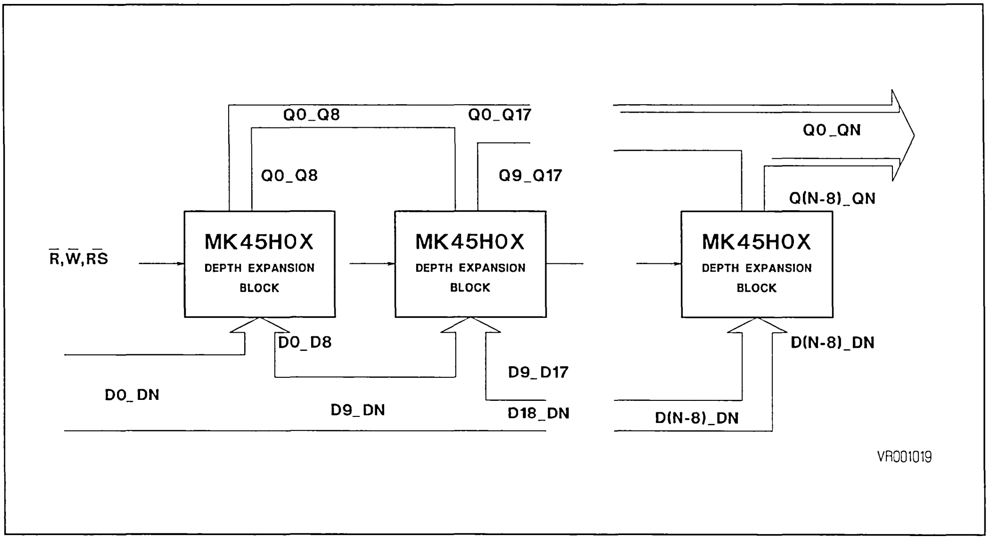
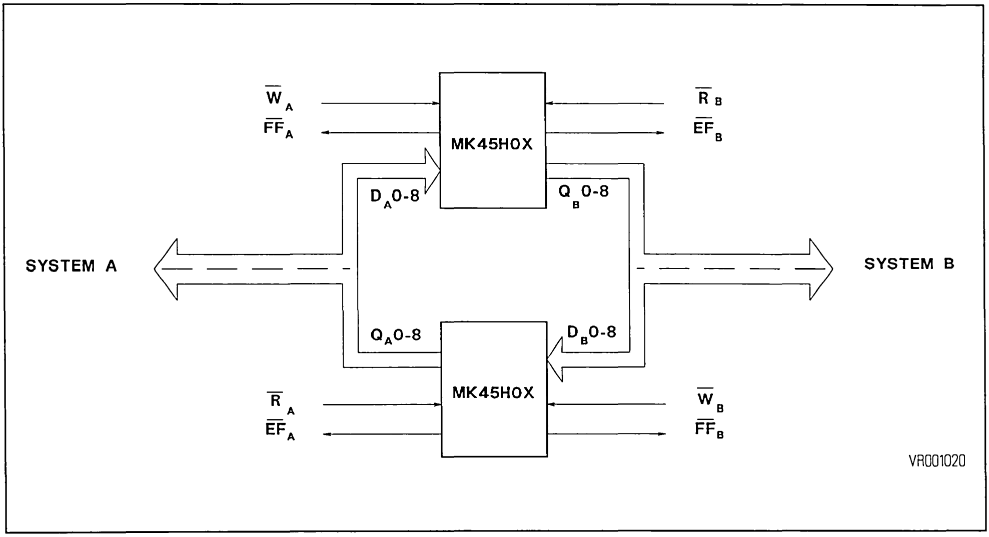

Q0_Q8
Q0_Q17
Q0_QN
Q0_Q8
Q9_Q17
Q(N-8)_QN
R,W,RS
MK45H0X
DEPTH EXPANSION
BLOCK
MK45H0X
DEPTH EXPANSION
BLOCK
MK45H0X
DEPTH EXPANSION
BLOCK
D0_D8
D(N-8)_DN
D9_D17
D0_DN
D9_DN
D18_DN
D(N-8)_DN
VR001019

Figure 16. Bidirectional FIFO Application


W_A
FF_A
R_B
EF_B
MK45H0X
D_A0-8
Q_B0-8
SYSTEM A
SYSTEM B
Q_A0-8
D_B0-8
MK45H0X
R_A
EF_A
W_B
FF_B
VR001020

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	20	mA

Note : This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this spefication in not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
V_{CC}	Supply Voltage	4.5	5.5	V	1
GND	Ground	0	0	V	
V_{IH}	Logic 1 All Inputs	2	V_{CC} + 0.3	V	1,2
V_{IL}	Logic 0 All Inputs	–0.3	0.8	V	1

Notes: 1. All Voltages are referenced to ground
2. V_{IH} = 2 5V on the RS pin for MK45H01,11, 02,12

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, V_{CC}= +5V± 10%)

Symbol	Parameter	Min.	Max.	Units	Note
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	1
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ /$\overline{RT}$ = V_{IH})		12	mA	1
I_{CC3}	Power Down Current (Inputs ≥ V_{CC} -0.2V)		2	mA	1
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{OL}	Output Leakage Current	–10	10	µA	3
V_{OH}	Output Logic 1 Voltage (I_{OUT} = -4.0mA)	2.4		V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 8.0mA)		0.4	V	4

Notes : 1. I_{CC} measurements are made with outputs open.
2. Measured with $0.4V \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
4. All voltages are referenced to ground.

CAPACITANCE (T_A= 25°C, f= 1MHz)

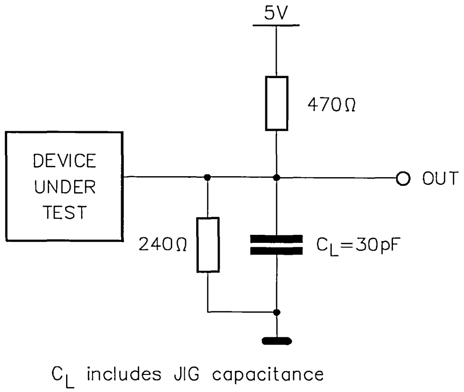
Symbol	Parameter	Typ.	Max.	Unit	Note
C_1	Capacitance on Input Pins		8	pF	1
C_0	Capacitance on Output Pins		12	pF	1,2

Notes : 1. This parameter is only sampled and not 100% tested
2. Output buffer deselected

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	5	ns
Input Signal Timing Reference Level	1.5	V
Output Signal Timing Reference Levels	1.5 and 1.9	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ±10%	V

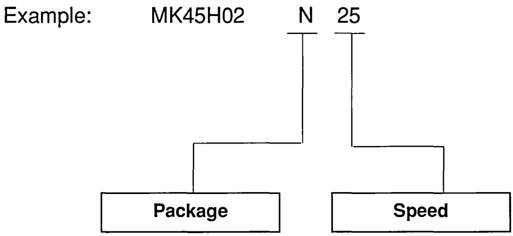
Figure 17. Equivalent Output Load Circuit


5V
470Ω
DEVICE UNDER TEST
OUT
240Ω
C_L=30pF

C_L includes JIG capacitance

VA00614

ORDERING INFORMATION



Package	
N	PDIP28 and/or PSDIP28
K	PLCC32

Speed	
25	25ns
35	35ns
50	50ns
65	65ns
12	120ns

For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

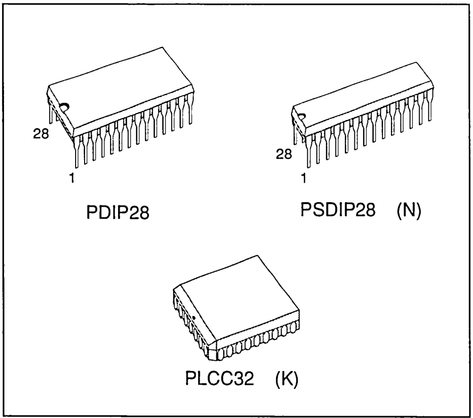
For further information on any aspect of this device, please contact our Sales Office nearest you.

SGS-THOMSON
MICROELECTRONICS

MK45H04,14
MK45H08

VERY FAST CMOS 4K / 8K x 9 BiPORT FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE x 9 ORGANIZATIONS:
  - MK45H04,14 (4K x 9)
  - MK45H08 (8K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE


28
1
PDIP28
28
1
PSDIP28 (N)
PLCC32 (K)

DESCRIPTION

The MK45HX4 and MK45H08 are BiPORT™ FIFO memories from SGS-THOMSON Microelectronics, which utilize special two-port mem-ory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow.

PIN NAMES

$\overline{\text{W}}$	Write
$\overline{\text{R}}$	Read
$\overline{\text{RS}}$	Reset
D0-D8	Data Input
Q0-Q8	Data Output
$\overline{\text{FL}}/\overline{\text{RT}}$	First Load / Retransmit
$\overline{\text{XI}}$	Expansion Input
$\overline{\text{XO}}/\overline{\text{HF}}$	Expansion Output / Half-full Flag
$\overline{\text{FF}}$	Full Flag
$\overline{\text{EF}}$	Empty Flag
V_{CC}, GND	5 Volts, Ground
NC	Not Connected

Figure 1. Pin Connections

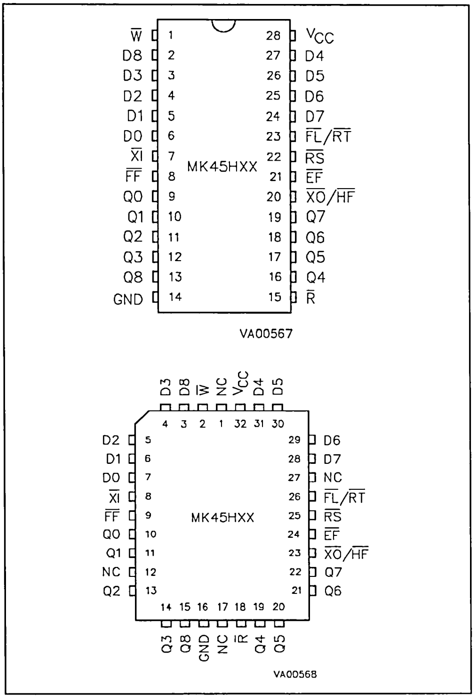
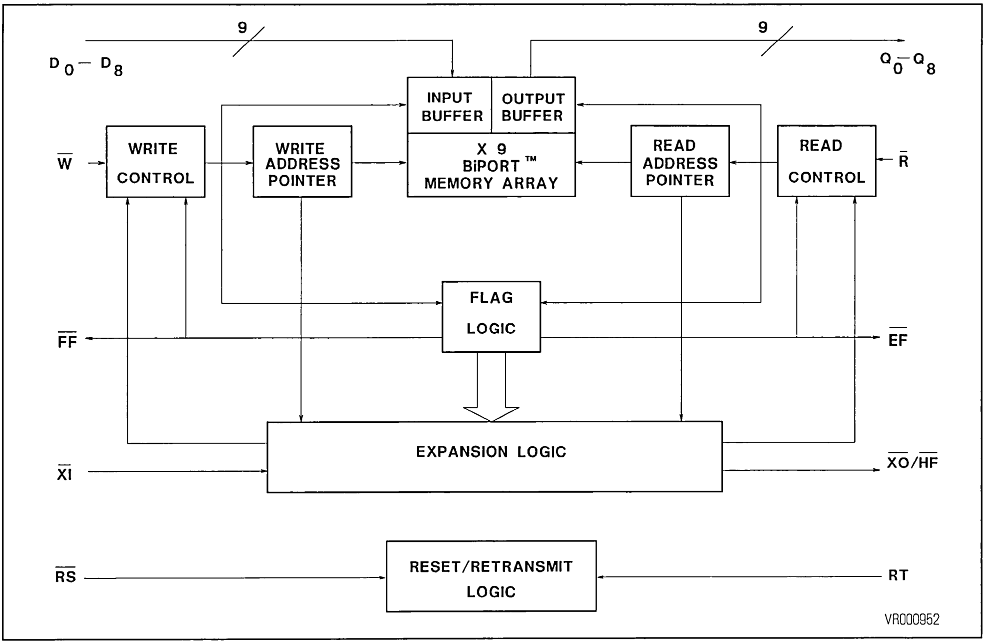

W 1
D8 2
D3 3
D2 4
D1 5
D0 6
XI 7
FF 8
Q0 9
Q1 10
Q2 11
Q3 12
Q8 13
GND 14
28 VCC
27 D4
26 D5
25 D6
24 D7
23 FL/RT
22 RS
21 EF
20 XO/HF
19 Q7
18 Q6
17 Q5
16 Q4
15 R
MK45HXX
VA00567
D3 4
D8 3
W 2
NC 1
VCC 32
D4 31
D5 30
D2 5
D1 6
D0 7
XI 8
FF 9
Q0 10
Q1 11
NC 12
Q2 13
29 D6
28 D7
27 NC
26 FL/RT
25 RS
24 EF
23 XO/HF
22 Q7
21 Q6
Q3 14
Q8 15
GND 16
NC 17
R 18
Q4 19
Q5 20
MK45HXX
VA00568

Figure 2. Block Diagram



DESCRIPTION (Continued)

The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of $\overline{W}$ (write), and $\overline{R}$ (read) input pins. Separate data in (D0-D8) and data out (Q0-Q8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45HX4 and MK45H08 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit ($\overline{RT}$) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 4096 or 8192 words.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45HX4 and MK45H08 employ a memory-based architecture wherein a byte written into the device does not “ripple through”. Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (4096 or 8192). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location.

FUNCTIONAL DESCRIPTION (Continued)

As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

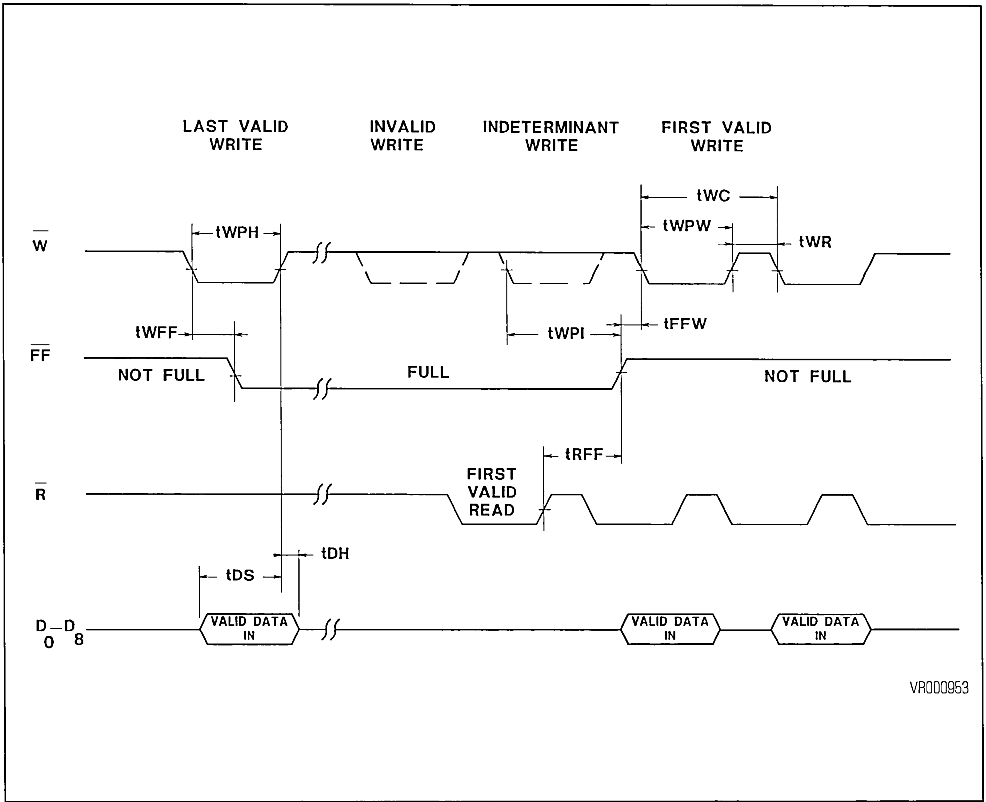
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45HX4, and MK45H08 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows the connection of the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45HXX initiates a Write Cycle (see Figure 3) on the falling edge of the Write Enable control input ($\overline{\mathrm{W}}$), provided that the Full Flag ($\overline{\mathrm{FF}}$) is not set. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{\mathrm{W}}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{\mathrm{FF}}$ is set during the last valid write as the MK45HXX becomes full. Write operations begun with $\overline{\mathrm{FF}}$ low are inhibited. $\overline{\mathrm{FF}}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{\mathrm{FF}}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 5). Writes beginning t_{FFW} after $\overline{\mathrm{FF}}$ goes high are valid. Writes beginning after $\overline{\mathrm{FF}}$ goes low and more than t_{WPI} before $\overline{\mathrm{FF}}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{\mathrm{FF}}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on the internal flag status.

Figure 3. Write and Full Flag Waveforms



Write and Full Flag AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

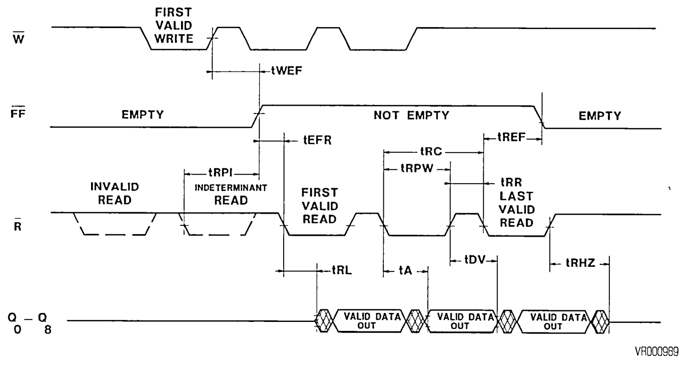
Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		25		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		25		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2 Measured using equivalent output load circuit

READ MODE

The MK45HXX initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not set. In the read mode of operation, the MK45HXX provides fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see Figure 6). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more that t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less then t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4. Read and Empty Flag Waveforms


FIRST VALID WRITE
W
tWEF
FF
EMPTY
NOT EMPTY
EMPTY
tEFR
tREF
tRC
tRPW
tRPI
INVALID READ
INDETERMINANT READ
FIRST VALID READ
tRR
LAST VALID READ
R
tRL
tA
tDV
tRHZ
Q0 – Q8
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT
VR000989

Read and Empty Flag AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		25		35		40		60		60	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		25		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

Figure 5. Read/Write to Full Flag Waveforms

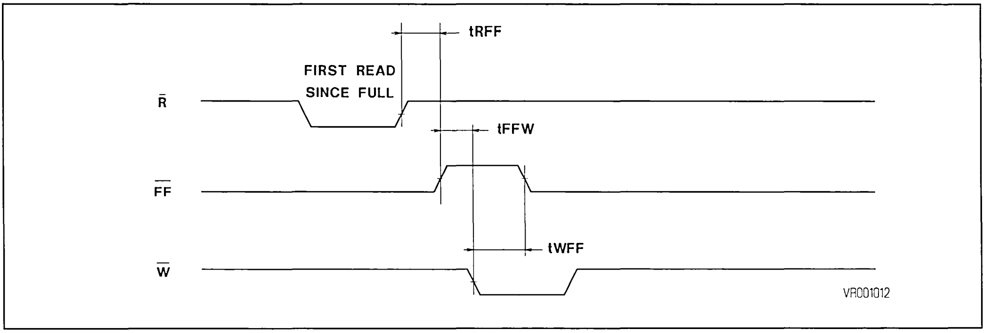
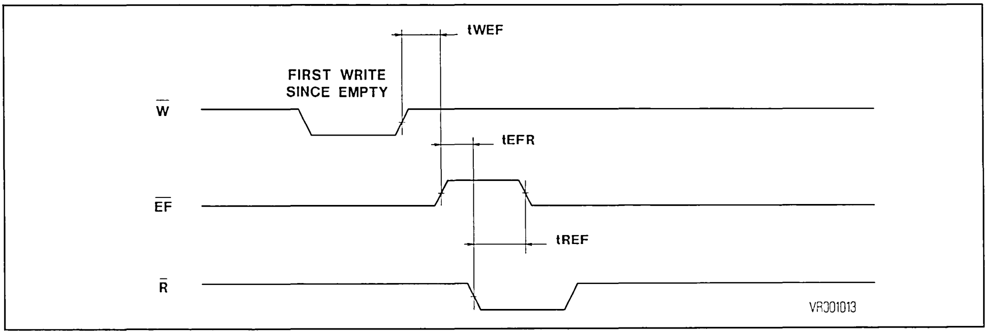

tRFF
FIRST READ SINCE FULL
R̄
tFFW
FF̄
tWFF
W̄
VR001012

Figure 6. Write/Read to Empty Flag Waveforms

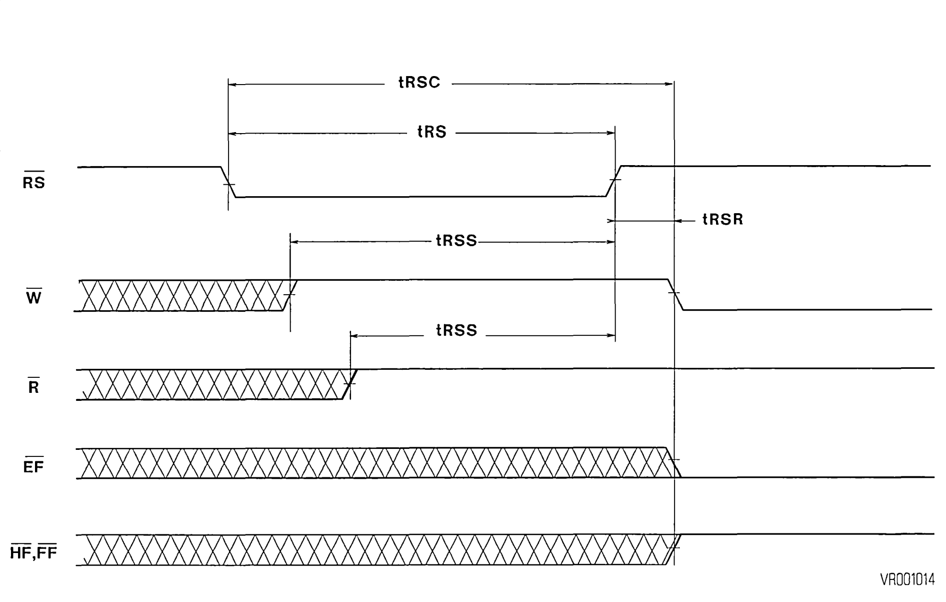

tWEF
FIRST WRITE SINCE EMPTY
W̄
tEFR
EF̄
tREF
R̄
VR001013

RESET

The MK45HXX is reset (see Figure 7) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{R}$ and $\overline{W}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 7. Reset Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Reset AC Operating Conditions (0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

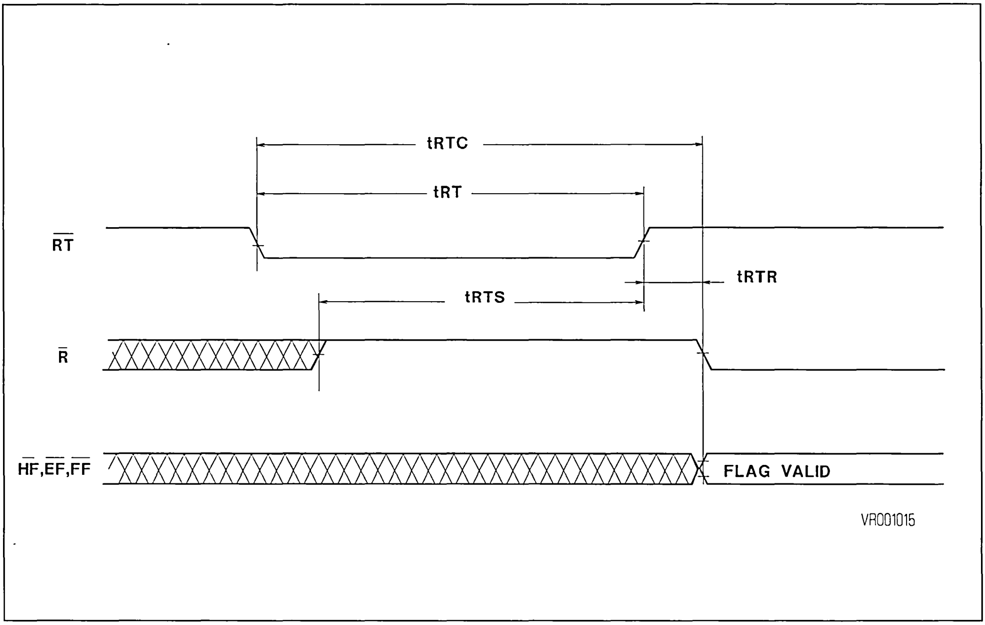
Note: 1. Pulse widths less than minimum values are not allowed

RETRANSMIT

The MK45HXX can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 8). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8. Retransmit Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Retransmit AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		50		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Set Up Time	25		30		30		45		100		ns	

Note: 1. Pulse widths less that minimum values are not allowed

SINGLE DEVICE CONFIGURATION

A single MK45HXX may be used when application requirements are for a depth of the device depth or less. The MK45HXX is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 9).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK45HXXs. Any word width can be attained by adding additional MK45HXXs. The half full flag ($\overline{HF}$) operates the same as in single device configuration.

Figure 9. A Single MK45HXX FIFO Configuration

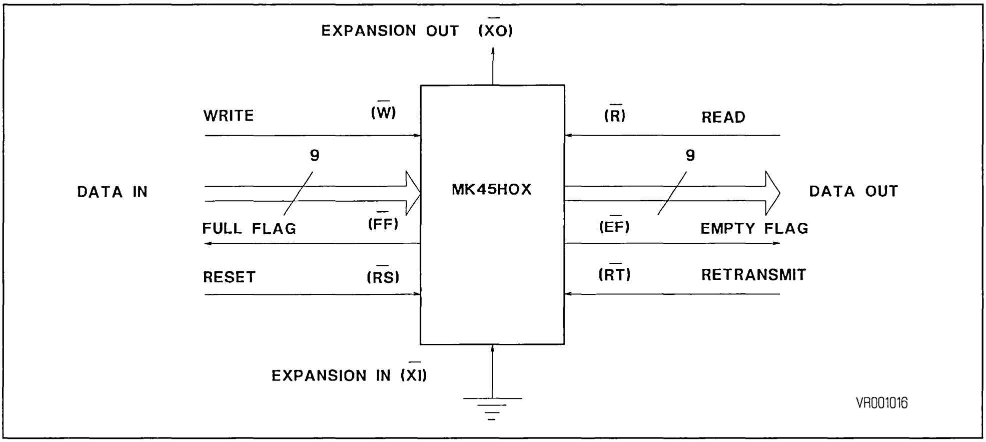
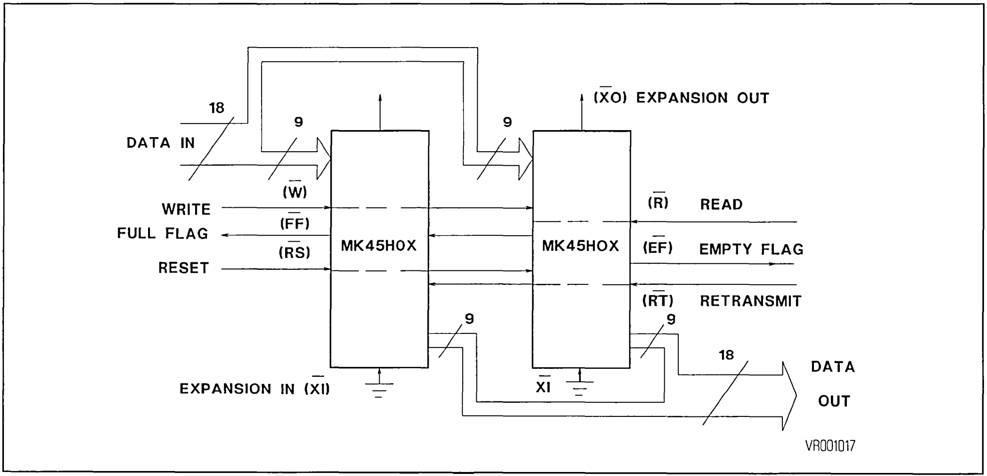

EXPANSION OUT (XO)
WRITE (W)
(R) READ
9
9
DATA IN
MK45HOX
DATA OUT
FULL FLAG (FF)
(EF) EMPTY FLAG
RESET (RS)
(RT) RETRANSMIT
EXPANSION IN (XI)
VR001016

Figure 10. A Two Device Width Expansion FIFO Configuration


18
DATA IN
9
9
(XO) EXPANSION OUT
(W)
WRITE
(R) READ
FULL FLAG
(FF)
(RS)
MK45HOX
MK45HOX
(EF) EMPTY FLAG
RESET
(RT) RETRANSMIT
9
9
18
DATA OUT
EXPANSION IN (XI)
XI
VR001017

Note : Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

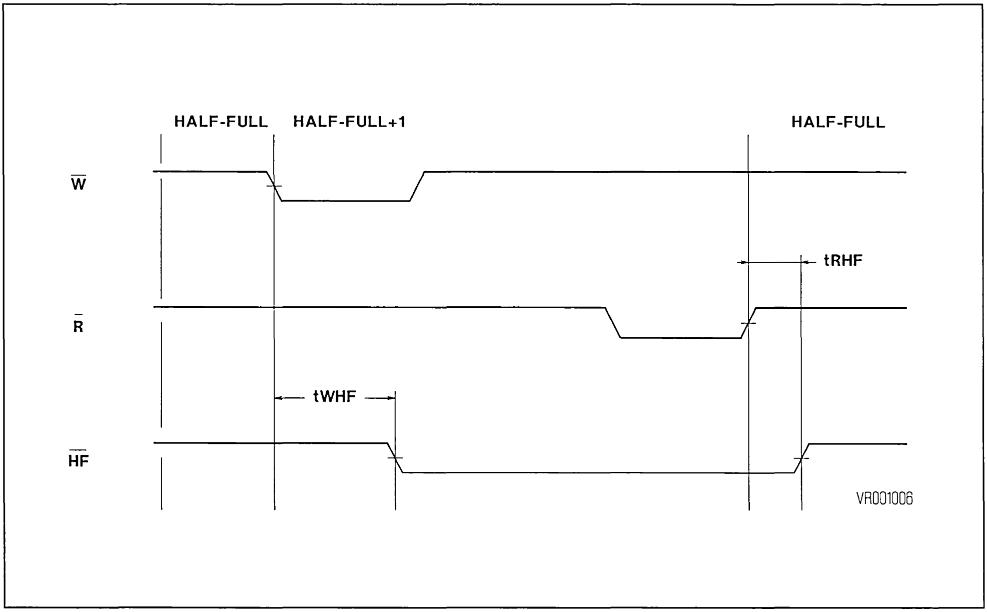
When in single device configuration, the (HF) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag (HF) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag (HF) is then reset by the rising edge of the read operation (see Figure 11).

DEPTH EXPANSION (Daisy Chain)

The MK45HXX can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 12 demonstrates Depth Expansion using two MK45HXXs. Any depth can be attained by adding additional MK45HXXs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the EFs and the ORing of all the FFs (i.e., all must be set to generate the composite FF or EF).

Figure 11. Half Full Flag Waveforms



Half Full Flag AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

The MK45HXX operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions :

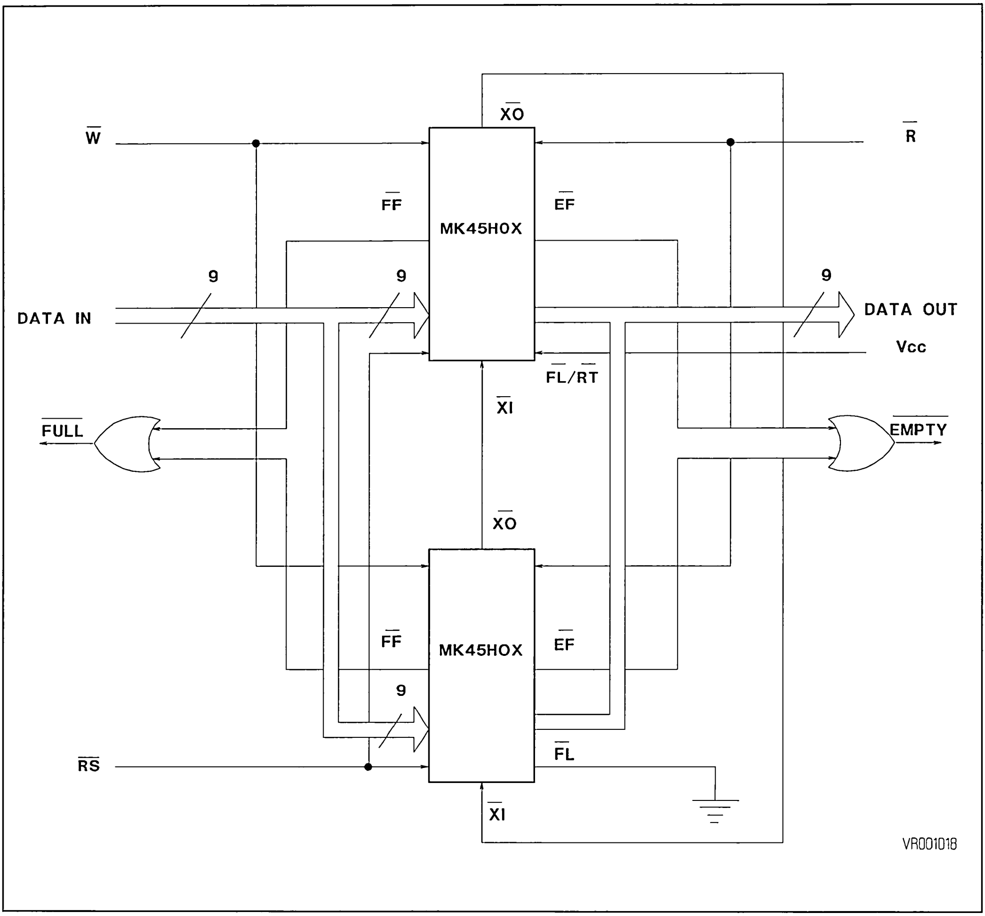
1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not available in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

EXPANSION TIMING

Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Due to the fact that Expansion Out pins are generally connected only to Expansion In pins, the user does not need to be concerned with the actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the identical to the WRITE and READ signals but ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

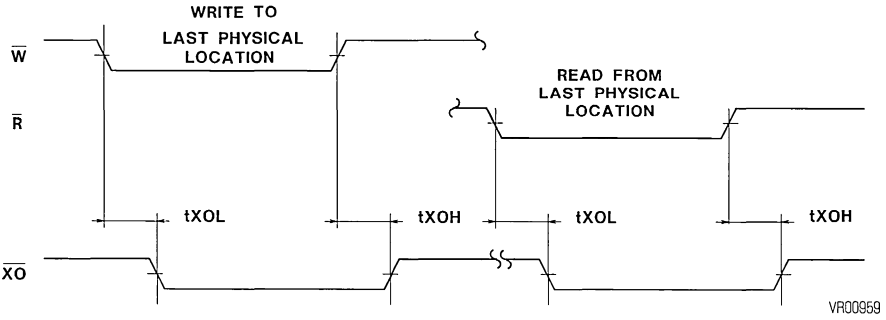
Figure 12. A Two Device Depth Expansion Configuration



$\overline{W}$
$\overline{XO}$
$\overline{R}$
$\overline{FF}$
$\overline{EF}$
MK45HOX
9
9
9
DATA IN
DATA OUT
Vcc
$\overline{FL}/\overline{RT}$
$\overline{XI}$
$\overline{FULL}$
$\overline{EMPTY}$
$\overline{XO}$
$\overline{FF}$
MK45HOX
$\overline{EF}$
9
$\overline{RS}$
$\overline{FL}$
$\overline{XI}$
VR001018

When in Depth Expansion mode, a given MK45HXX will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK45HXX in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 13. Expansion Out Waveforms

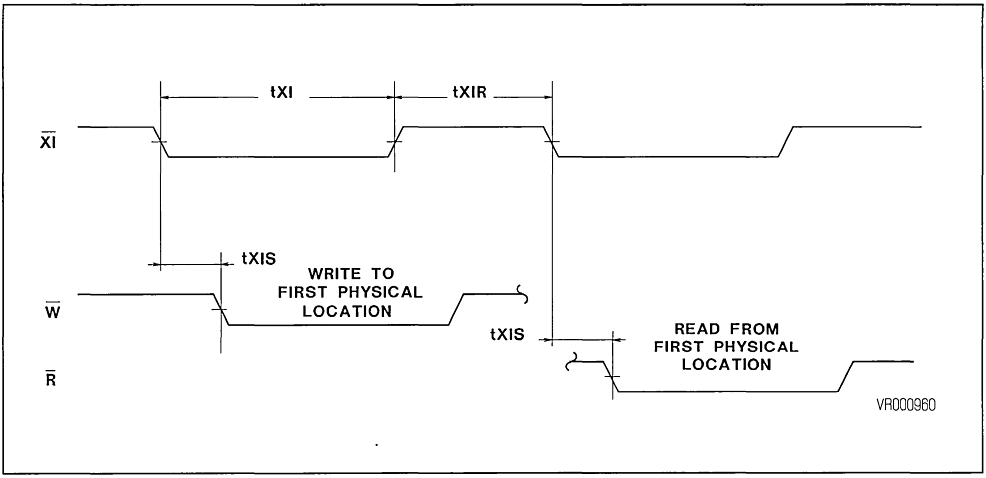

WRITE TO
LAST PHYSICAL
LOCATION
W̄
R̄
READ FROM
LAST PHYSICAL
LOCATION
tXOL
tXOH
tXOL
tXOH
X̄Ō
VR00959

Expansion Out AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

Figure 14. Expansion In Waveforms


tXI
tXIR
XI
tXIS
WRITE TO FIRST PHYSICAL LOCATION
W
tXIS
READ FROM FIRST PHYSICAL LOCATION
R
VR000960

Expansion In AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion In Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion In Setup Time	15		15		15		15		15		ns	

Note: 1. Pulse widths less than minimum values are not allowed

COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK45HXXs, as shown in Figure 16. Care must be taken to ensure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 15. Compound FIFO Expansion Configuration

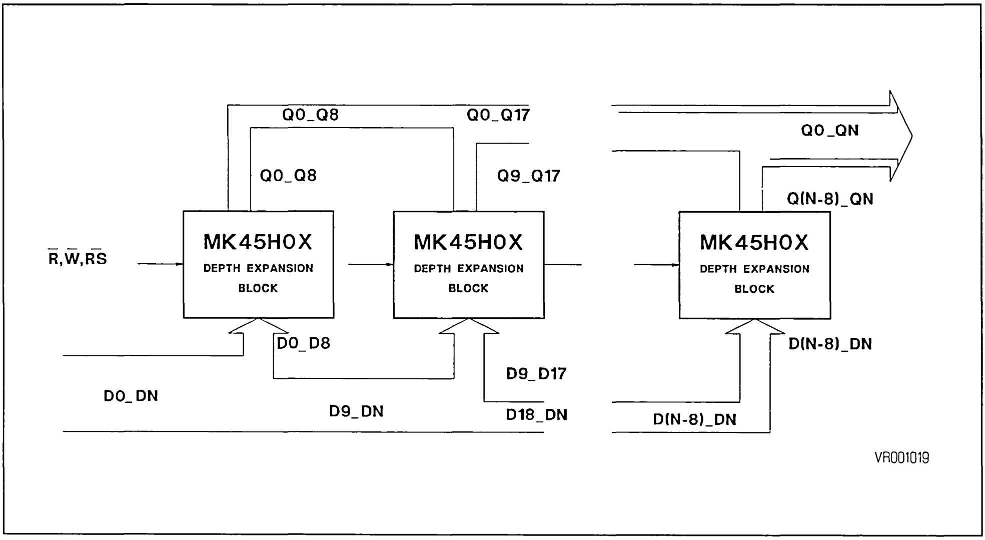
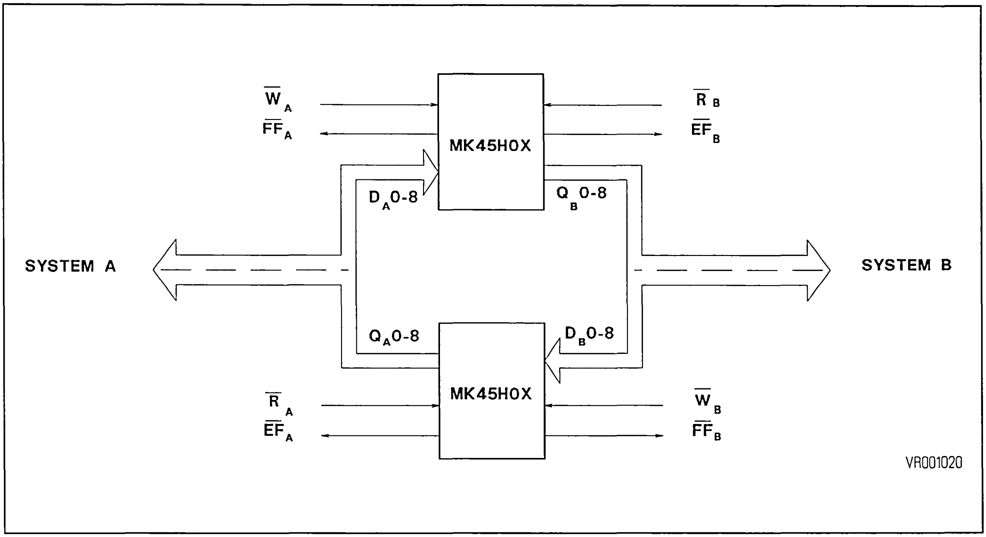

Q0_Q8
Q0_Q17
Q0_QN
Q0_Q8
Q9_Q17
Q(N-8)_QN
$\overline{R}$,$\overline{W}$,$\overline{RS}$
MK45H0X DEPTH EXPANSION BLOCK
MK45H0X DEPTH EXPANSION BLOCK
MK45H0X DEPTH EXPANSION BLOCK
D0_D8
D(N-8)_DN
D9_D17
D0_DN
D9_DN
D18_DN
D(N-8)_DN
VR001019

Figure 16. Bidirectional FIFO Application


$\overline{W}_A$
$\overline{FF}_A$
MK45H0X
$\overline{R}_B$
$\overline{EF}_B$
D_A0-8
Q_B0-8
SYSTEM A
SYSTEM B
Q_A0-8
D_B0-8
$\overline{R}_A$
$\overline{EF}_A$
MK45H0X
$\overline{W}_B$
$\overline{FF}_B$
VR001020

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	20	mA

Note : This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this spefication in not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
V_{CC}	Supply Voltage	4.5	5.5	V	1
GND	Ground	0	0	V	
V_{IH}	Logic 1 All Inputs	2	$V_{CC} + 0.3$	V	1
V_{IL}	Logic 0 All Inputs	–0.3	0.8	V	1

Note : 1. All Voltages are referenced to ground

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	Min.	Max.	Units	Note
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	1
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)		12	mA	1
I_{CC3}	Power Down Current (Inputs $\geq V_{CC}$ -0.2V)		2	mA	1
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{OL}	Output Leakage Current	–10	10	µA	3
V_{OH}	Output Logic 1 Voltage ($I_{OUT} =$ -4.0mA)	2.4		V	4
V_{OL}	Output Logic 0 Voltage ($I_{OUT} =$ 8.0mA)		0.4	V	4

Notes : 1. I_{CC} measurements are made with outputs open.
2. Measured with $0.4V \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
4. All voltages are referenced to ground.

CAPACITANCE (T_A= 25°C, f= 1MHz)

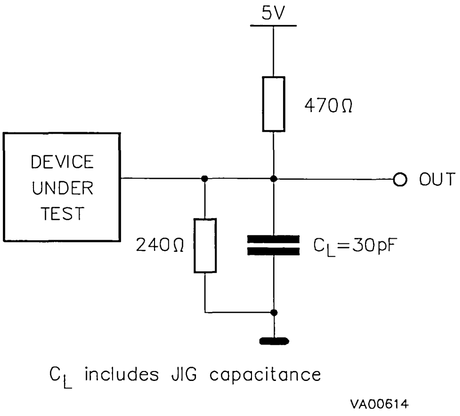
Symbol	Parameter	Typ.	Max.	Unit	Note
C_I	Capacitance on Input Pins		8	pF	1
C_O	Capacitance on Output Pins		12	pF	1,2

Notes : 1. This parameter is only sampled and not 100% tested
2. Output buffer deselected

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	5	ns
Input Signal Timing Reference Level	1.5	V
Output Signal Timing Reference Levels	1.5 and 1.9	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ±10%	V

Figure 17. Equivalent Output Load Circuit


5V
470Ω
DEVICE UNDER TEST
OUT
240Ω
C_L=30pF
C_L includes JIG capacitance
VA00614

ORDERING INFORMATION

Example: MK45H04 N 25

Package	
N	PDIP28 and/or PSDIP28
K	PLCC32

Speed	
25	25ns
35	35ns
50	50ns
65	65ns
12	120ns

For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.

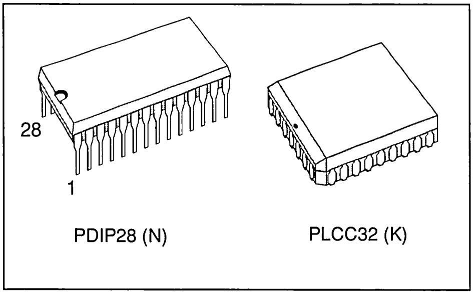
ZEROPOWER MEMORIES

SGS-THOMSON
MICROELECTRONICS

MK48C02A
MK48C12A

CMOS 2K x 8 ZEROPOWER SRAM

- LOW CURRENT (1μA @ 70°C) BATTERY INPUT FOR DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- + 5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER 440mW ACTIVE ; 5.5mW STANDBY
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE:
  - – MK48C02A 4.75V $\geq V_{PFD} \geq$ 4.50V
  - – MK48C12A 4.50V $\geq V_{PFD} \geq$ 4.20V
- POWER FAIL INTERRUPT OUTPUT


28
1
PDIP28 (N)
PLCC32 (K)

DESCRIPTION

The MK48C02A/12A ZEROPOWER™ are CMOS RAM memories with internal power fail support circuitry for battery backup applications. The fully static RAM uses an HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V_{CC} transients. A precision voltage detector write-protects the RAM to prevent inadvertent loss of data when V_{CC} falls

PIN NAMES

A0-A10	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
GND	Ground
V_{CC}	5 Volts
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_B	Battery Input
$\overline{INT}$	Power Fail Interrupt (Open Drain Type)
NC	No Connected

Figure 1. Pin Connections

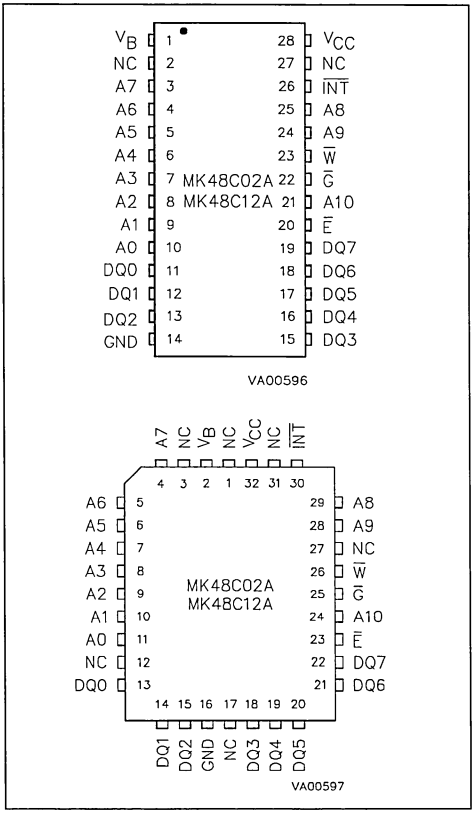
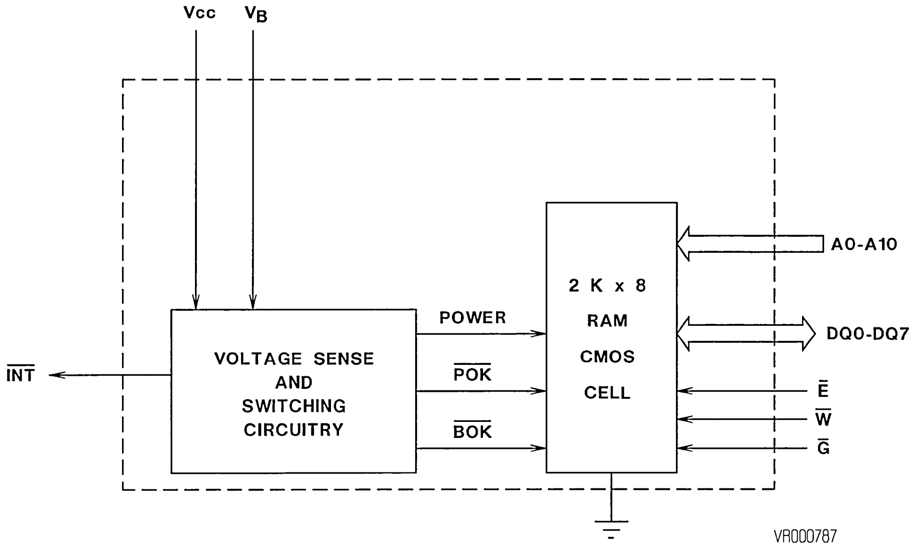

VB 1
NC 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
28 VCC
27 NC
26 INT
25 A8
24 A9
23 W
22 G
21 A10
20 E
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
MK48C02A
MK48C12A
VA00596
A7 4
NC 3
VB 2
NC 1
VCC 32
NC 31
INT 30
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
NC 12
DQ0 13
29 A8
28 A9
27 NC
26 W
25 G
24 A10
23 E
22 DQ7
21 DQ6
MK48C02A
MK48C12A
14 DQ1
15 DQ2
16 GND
17 NC
18 DQ3
19 DQ4
20 DQ5
VA00597

Figure 2. Block Diagram


Vcc
VB
INT
VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
POK
BOK
2 K x 8 RAM CMOS CELL
A0-A10
DQ0-DQ7
E
W
G
VR000787

DESCRIPTION (Continued)

out of tolerance. In this way, all input and output pins (including $\overline{E}$ and $\overline{W}$) become "don't care". The device permits full functional ability of the RAM for V_{CC} above 4.75V (MK48C02A) and 4.5V (MK48C12A). Data protection is provided for V_{CC} below 4.5V (MK48C02A) and 4.2V (MK48C12A), and maintains data in the absence of V_{CC} with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5nA) because all power-consuming circuitry is turned off. The low battery drain allows use of a long life Lithium primary cell.

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
$<V_{CC}(max)$ $>V_{CC}(min)$	V_{IH}	X	X	Deselect	High-Z
	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$<V_{PFD}(min)>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–55 to +125	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

Notes: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

***CAUTION :** Under no conditions can the "Absolute Maximum Ratings" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below – 0 3V DC.*

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48C02A)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48C12A)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2
V_B	Battery Voltage	1.8	4.0	V	1

DC ELECTRICAL CHARACTERISTICS

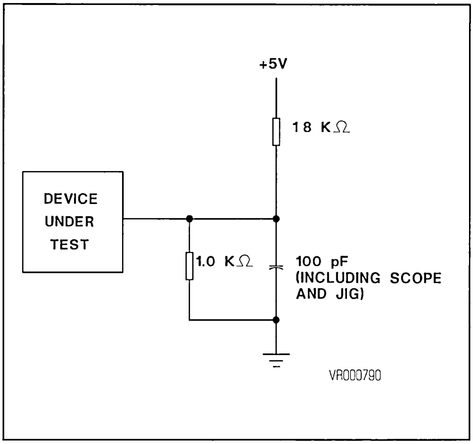
($0°C \leq T_A \leq 70°C$ $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$= V_{IH})		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ –0.2V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	4
I_{OL}	Output Leakage Current	–5	5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1mA)		0.4	V	
V_{PFL}	INT Logic "0" Voltage (I_{OUT} = 0.5 mA)		0.4	V	
I_{BATT}	Battery Backup Current V_B = 4.0V		1	µA	
I_{CHG}	Battery Charging Current V_{CC} = 5.5V	–5	5	nA	
V_{LB}	Battery OK Flag	1.8	2.6	V	

AC TEST CONDITIONS

Input Levels	0.6 V to 2.4 V
Transition Times	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V

OUTPUT LOAD DIAGRAM



CAPACITANCE
($T_A = 25°C$)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins and $\overline{INT}$	10 pF	4, 5

Notes :

1. All voltages referenced to GND
2. Negative spikes of – 1.0 volts allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
5. Effective capacitance calculated from the equation $C = I\,\Delta t/\Delta V$ with $\Delta V = 3$ volts and power supply at nominal level.

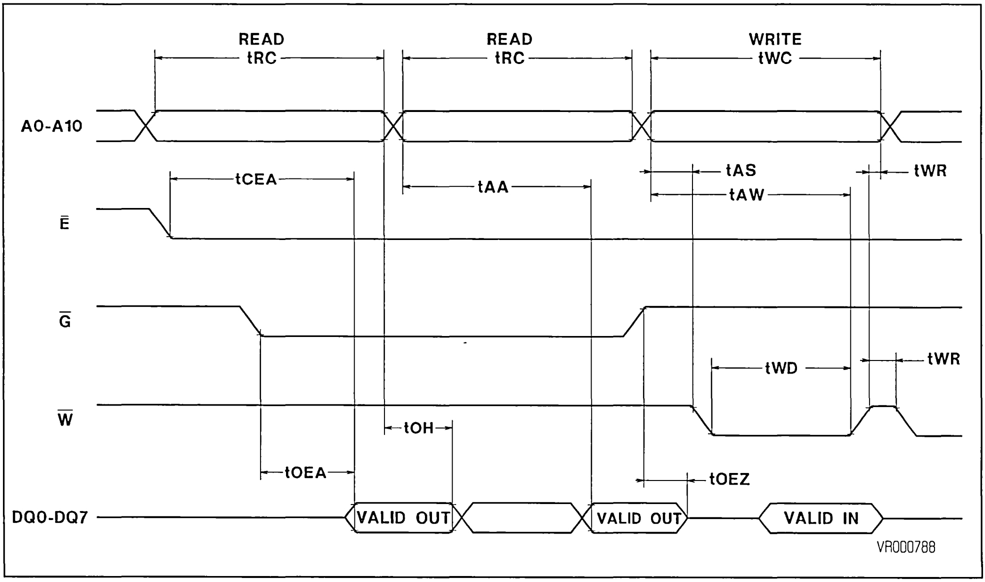
OPERATION

Read Mode

The MK48C02A/12A is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

($0°C \leq T_A \leq 70°C$; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	48CX2A-15		48CX2A-20		48CX2A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

Note : Measured using the Output Load Diagram shown page 4.

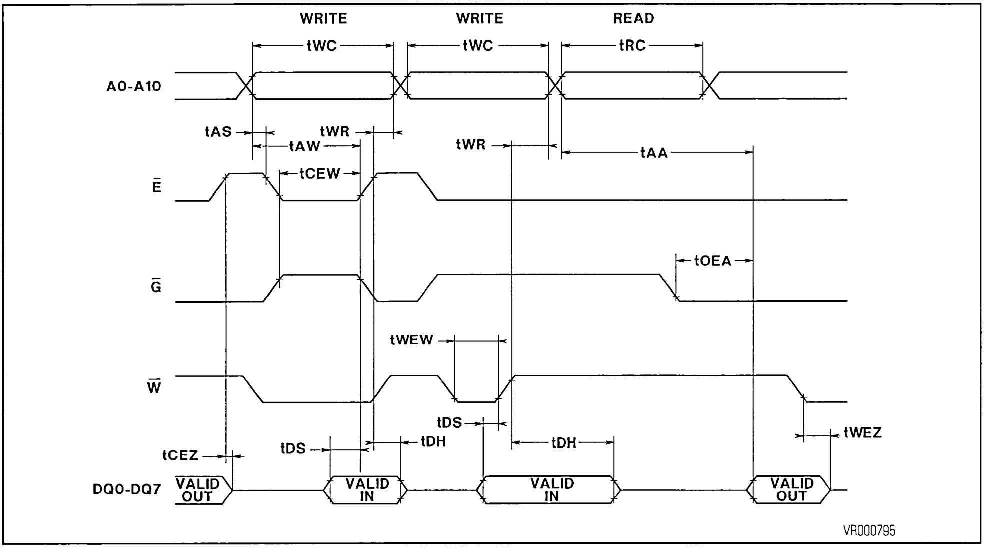
WRITE MODE

The MK48C02A/12A is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high, for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterwards.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stabilizes.

The MK48C02A/12A $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

($0°C \leq T_A \leq 70°C$; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	48CX2A-15		48CX2A-20		48CX2A-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	150		200		250		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AW}	Address Valid to End of Write	120		140		180		ns
t_{CEW}	Chip Enable to End of Write	90		120		160		ns
t_{WEW}	Write Enable to End of Write	90		120		160		ns
t_{WR}	Write Recovery Time	10		10		10		ns
t_{DS}	Data Setup Time	40		60		100		ns
t_{DH}	Data Hold Time	5		5		5		ns
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns

DATA RETENTION MODE

With V_{CC} applied, the MK48C02A/12A operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48C02A has a V_{PFD} (max) - V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48C12A has a V_{PFD} (max) - V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48C02A/12A may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

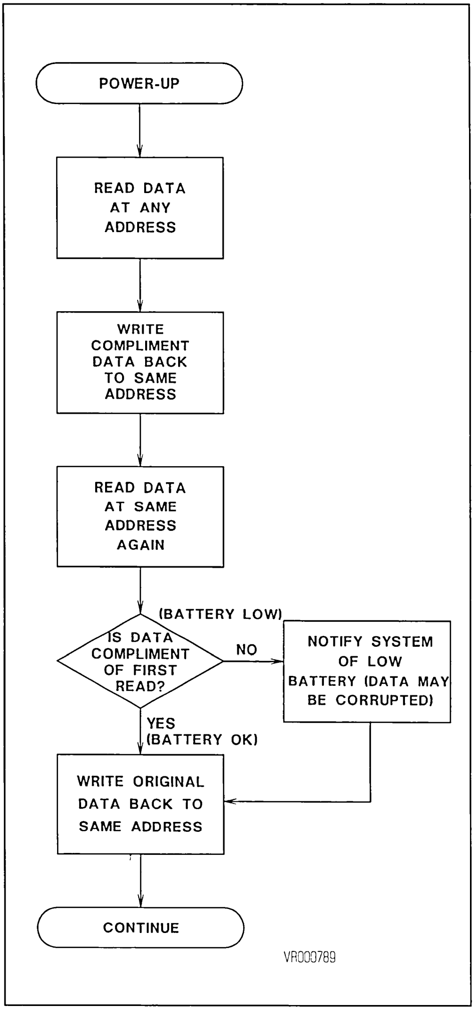
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{\text{BOK}}$) flag will be set. The $\overline{\text{BOK}}$ flag can be checked after power up. If the $\overline{\text{BOK}}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{\text{BOK}}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{\text{E}}$ or $\overline{\text{W}}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

INTERRUPT FUNCTION

The MK48C02A/12A provides a power-fail interrupt output labeled $\overline{\text{INT}}$. The $\overline{\text{INT}}$ pin eliminates the need for external power sensing components in applications where an orderly shut down of the system is necessary. The $\overline{\text{INT}}$ pin is open drain for "wire or" applications and provides the user with 10µs to 40µs advanced warning of an impending power-fail write protect.

Figure 5. Checking the $\overline{\text{BOK}}$ Flag Status


POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
IS DATA COMPLIMENT OF FIRST READ?
(BATTERY LOW)
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES (BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE
VR000789

AC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Timing)
($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after V_{PFD} (max)	120			µs	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10		40	µs	
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ High			120	µs	4

DC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Trip Point Voltages)
($0°C \leq T_A \leq +70°C$)

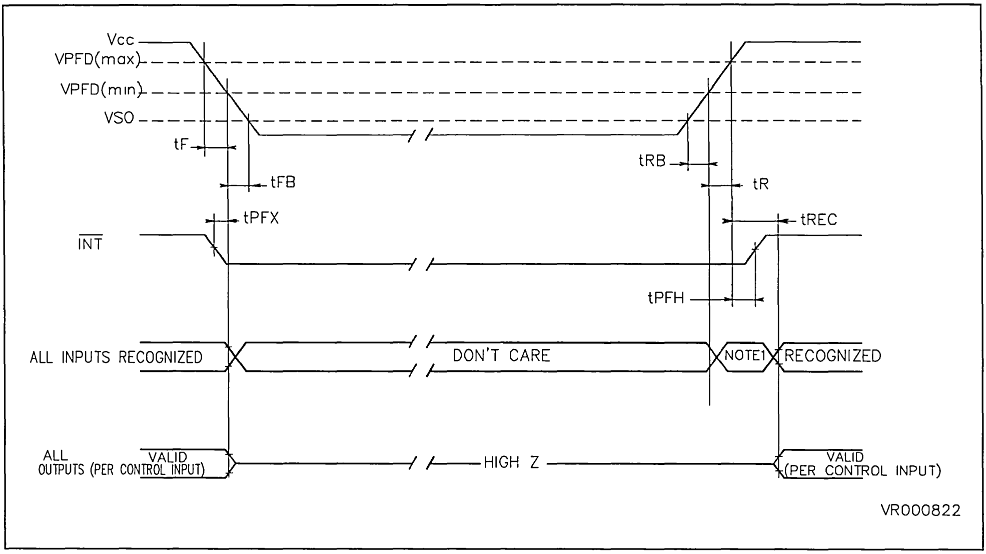
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{PFD}	Power-Fail Deselect Voltage (MK48C02A)	4.50	4.6	4.75	V	1
V_{PFD}	Power-Fail Deselect Voltage (MK48C12A)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

Notes :

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 40µs after V_{CC} passes V_{PFD} (Min).
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.
4. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

CAUTION: *Negative Undershoots Below -0.3V are not allowed on any pin while in Battery Back-up mode* .

Figure 6. Power-Down/Power-Up Timing


Vcc
VPFD(max)
VPFD(min)
VSO
tF
tFB
tRB
tR
tPFX
tREC
INT
tPFH
ALL INPUTS RECOGNIZED
DON'T CARE
NOTE1
RECOGNIZED
ALL OUTPUTS (PER CONTROL INPUT)
VALID
HIGH Z
VALID (PER CONTROL INPUT)
VR000822

Notes :

1. Inputs may or may not be recognized at this time.
2. Caution should be taken to keep $\overline{E}$ or $\overline{W}$ in the high state V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent write cycles after Vcc rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running

ORDERING INFORMATION

Example: MK48C02 K 15

Package	
N	PDIP28
K	PLCC32

Speed	
15	150ns
20	200ns
25	250ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

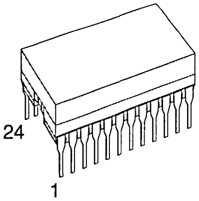
For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK48Z02
MK48Z12

CMOS 2K x 8 ZEROPOWER SRAM

- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C
- DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- + 5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- FULL CMOS-440mW ACTIVE ; 5.5mW STANDBY
- 24-PIN DUAL IN LINE PACKAGE, JEDEC PINOUTS
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE:
  - – MK48Z02 4.75V ≥ V_{PFD} ≥ 4.50V
  - – MK48Z12 4.50V ≥ V_{PFD} ≥ 4.20V

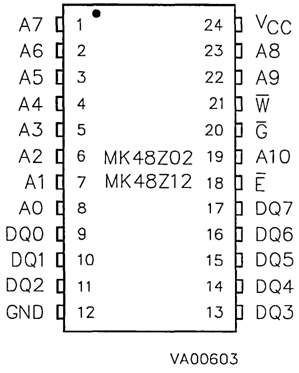


PHDIP24 WITH BATTERY TOP HAT (B)

DESCRIPTION

The MK48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an en-ergy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250ns and require only + 5 volts, no additional support circuitry is needed for interface to a microprocessor.

Figure 1. Pin Connection

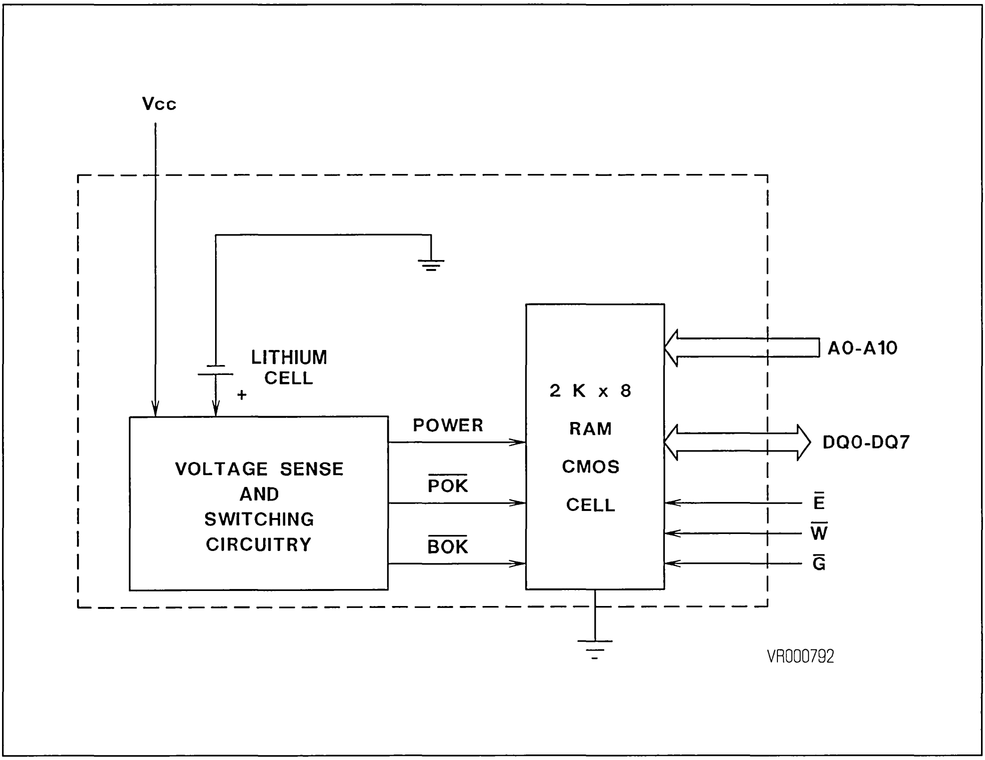


PIN NAMES

A0-A10	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
V_{CC}	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs

February 1992

Figure 2. Block Diagram


Vcc
LITHIUM CELL
+
VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
$\overline{POK}$
$\overline{BOK}$
2 K x 8 RAM CMOS CELL
A0-A10
DQ0-DQ7
$\overline{E}$
$\overline{W}$
$\overline{G}$
VR000792

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
$<V_{CC(max)}$ $>V_{CC(min)}$	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$<V_{PFD(min)}$ $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION : *Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below – 0.3V DC.*

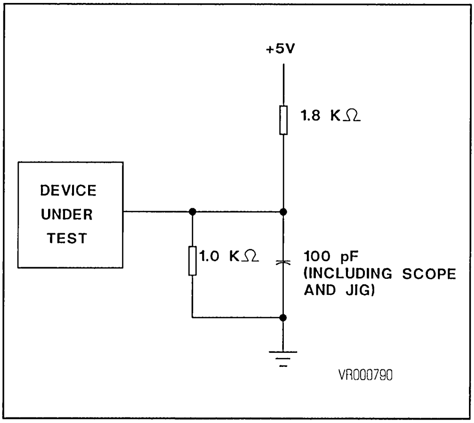
RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z02)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z12)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$; $V_{CC\,max} \geq V_{CC} \geq V_{CCmin}$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC} - 0.2V$)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	4
I_{OL}	Output Leakage Current	–5	5	µA	4
V_{OH}	Output Logic "1" Voltage ($I_{OUT} = -1.0mA$)	2.4		V	
V_{OL}	Output Logic "0" Voltage ($I_{OUT} = 2.1mA$)		0.4	V	

EQUIVALENT OUTPUT LOAD DIAGRAM



AC TEST CONDITIONS

Input Levels	0.6V to 2.4V
Transition Times	5ns
Input and Output Timing Reference Levels	0.8V or 2.2V

CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	4
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4, 5

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected.
5. Effective capacitance calculated from the equation $C = I\,\Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V.

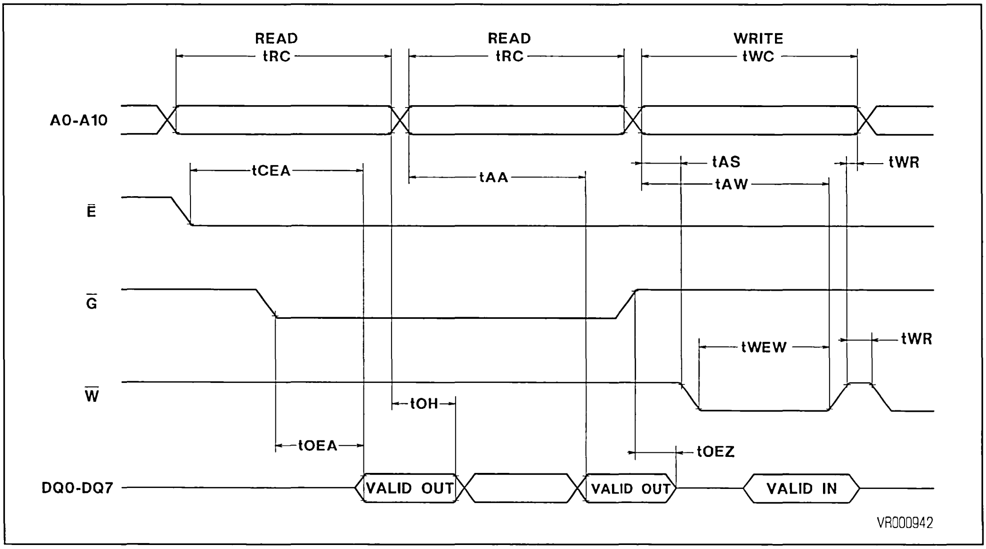
OPERATION

READ MODE

The MK48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

(0°C ≤ T_A ≤ 70°C; $V_{CC\,max} \geq V_{CC} \geq V_{CC}$ min)

Symbol	Parameter	48Z02-12		48Zx2-15		48Zx2-20		48Zx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

Note : Measured using the Output Load Diagram shown Page 4.

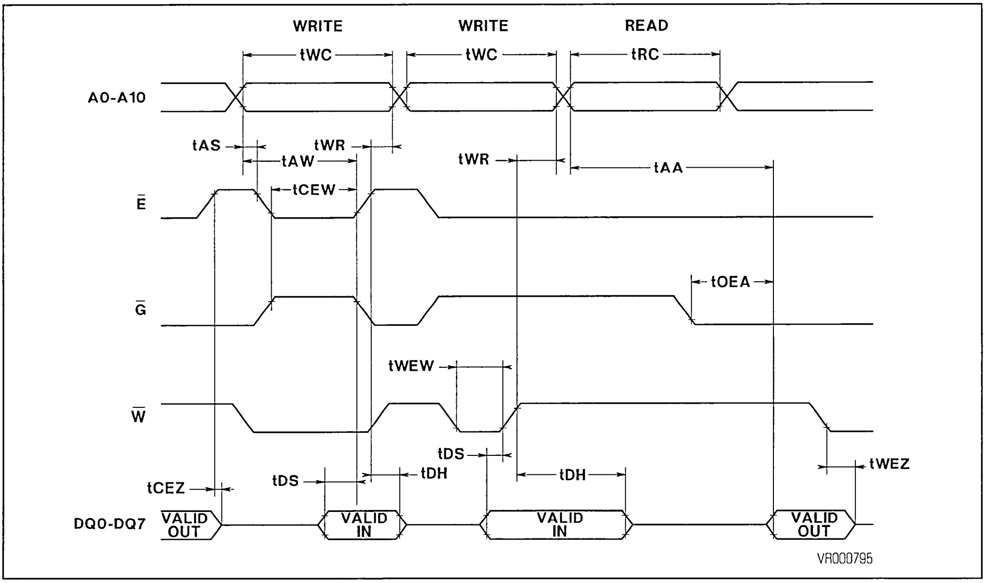
WRITE MODE

The MK48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stabilizes.

The MK48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

(0°C ≤ T_A ≤ 70°C; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	48Z02-12		48Zx2-15		48Zx2-20		48Zx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	5		5		5		5		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48Z02/12 operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48Z02 has a V_{PFD} (max) - V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48Z12 has a V_{PFD} (max) - V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{\text{BOK}}$) flag will be set. The $\overline{\text{BOK}}$ flag can be checked after power up. If the $\overline{\text{BOK}}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{\text{BOK}}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max). Caution should be taken to keep $\overline{\text{E}}$ or $\overline{\text{W}}$ high as V_{CC} rises past V_{PFD} (min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

Figure 5. Checking the $\overline{\text{BOK}}$ Flag Status

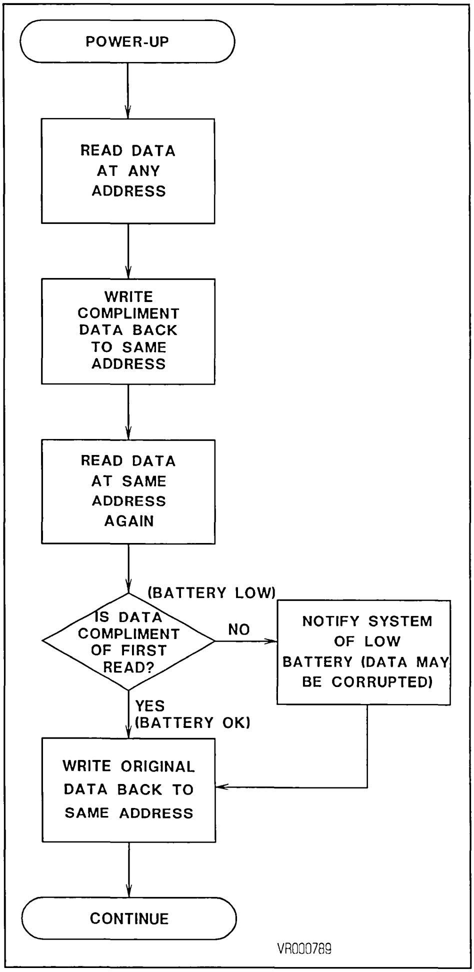
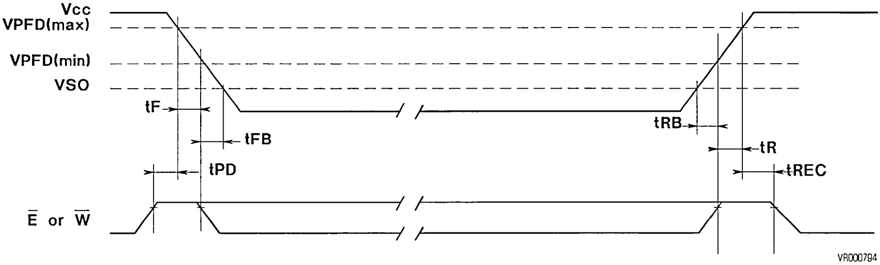

POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
IS DATA COMPLIMENT OF FIRST READ?
(BATTERY LOW)
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES (BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE
VR000789

Figure 6. Power-Down/Power-Up Timing



DC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Trip Point Voltages)
(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{PFD}	Power-Fail Deselect Voltage (MK48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-Fail Deselect Voltage (MK48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Timing)
(0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0			ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2			ms	

Notes :

1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall times of less t_F may result in deselection/write protection not occurring until 50µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MK48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-tem-perature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on-going battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note : The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years ; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case ana-lysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z02/12 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H-fabricated in Carrollton, TX; 9- assembled in Muar, Malaysia; 9-tested in Muar, Malaysia; 5B-lot designator; 9231-assembled in the year 1992, work week 31.

CALCULATING PREDICTED BATTERY LIFE

As Figure 7 indicates, the predicted life of the battery in the MK48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MK48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MK48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)] + [(TA_2/TT)/BL_2] + \ldots + [(TA_n/TT)/BL_n)]}$$

Where: TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z02/12 is exposed to temperatures of 30°C or less for 3066 hrs/yr ; temperatures greater than 25°C, but less than 40°C for 5256 hrs/yr ; and temperatures greater than 40°C, but less than 70˚C for the remaining 438 hrs/yr.

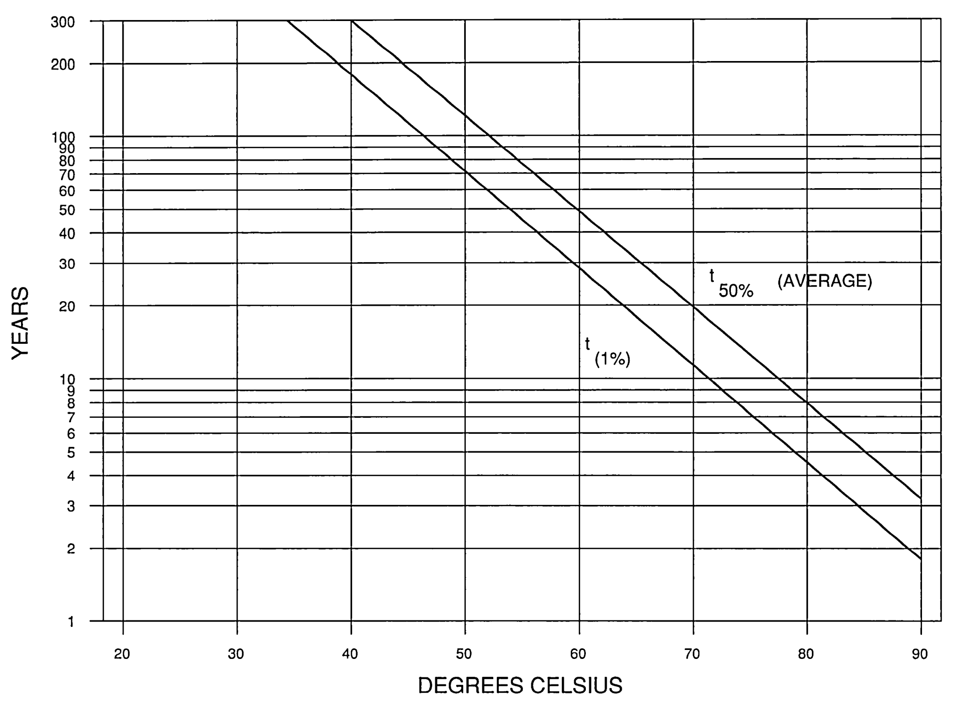
Reading predicted typical life values from Figure 7 ; BL_1 = 456 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 = 5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/456] + [(5256/8760)/175] + [(438/8760)/11.4]}$$

$$\geq 116.5 \text{ yrs.}$$

Figure 7. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION

Example: MK48Z02 B 12

Package	
B	PHDIP24

Speed	
12	120ns
15	150ns
20	200ns
25	250ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

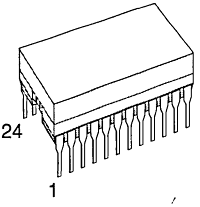
MKI48Z02
MKI48Z12

CMOS 2K x 8 ZEROPOWER SRAM

- INDUSTRIAL TEMPERATURE RANGE - 40°C to + 85°C.
- PREDICTED WORST CASE BATTERY LIFE OF 6 YEARS @ 85°C.
- DATA RETENTION IN THE ABSENCE OF POWER.
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE.
- + 5 VOLT ONLY READ/WRITE.
- CONVENTIONAL SRAM WRITE CYCLES.
- LOW POWER-440mW ACTIVE ; 5.5mW STANDBY.
- 24-PIN DUAL IN LINE PACKAGE, JEDEC 24 PIN MEMORY PINOUT.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- ON BOARD LOW-BATTERY WARNING CIRCUITRY.
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE :
  - MKI48Z02 4.75V $\geq V_{PFD} \geq$ 4.50V
  - MKI48Z12 4.50V $\geq V_{PFD} \geq$ 4.20V

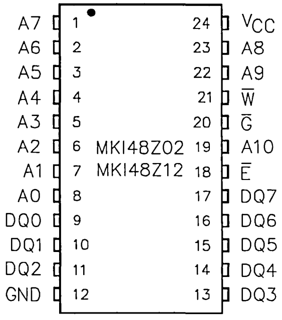
DESCRIPTION

The MKI48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an en-ergy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace exist-ing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC).



PHDIP24 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connections

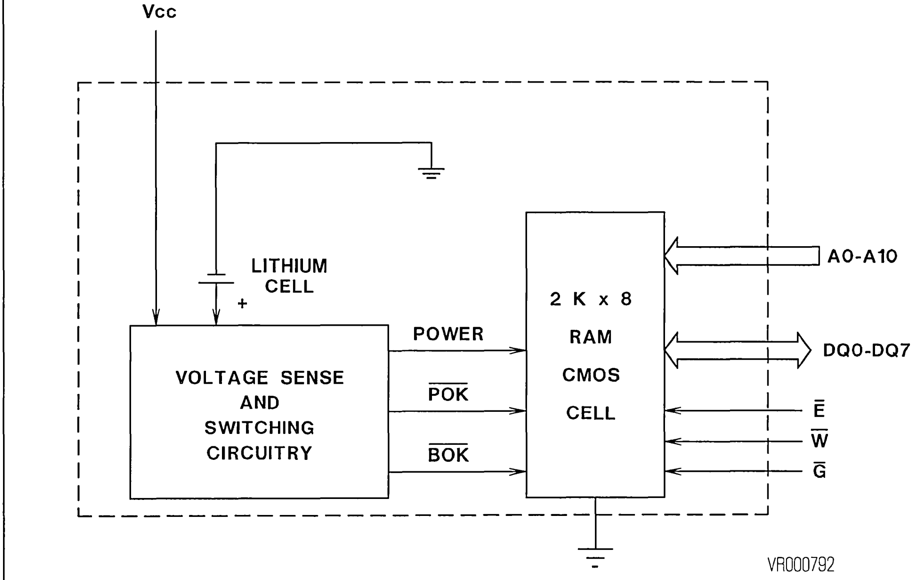


VA00604

PIN NAMES

A0-A10	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
V_{CC}	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 - DQ7	Data Inputs/Outputs

Figure 2. Block Diagram


Vcc
LITHIUM CELL
+
VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
$\overline{POK}$
$\overline{BOK}$
2 K x 8 RAM CMOS CELL
A0-A10
DQ0-DQ7
$\overline{E}$
$\overline{W}$
$\overline{G}$
VR000792

DESCRIPTION (Continued)

MKI48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250ns and require only + 5 volts, no additional support circuitry is needed for interface to a microprocessor.

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
$<V_{CC(max)}$ $>V_{CC(min)}$	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$<V_{PFD(min)}$ $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	–40 to +85	°C
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

***CAUTION :** Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below – 0.3V DC.*

RECOMMENDED DC OPERATING CONDITIONS

($-40°C \leq T_A \leq +85°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MKI48Z02)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MKI48Z12)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

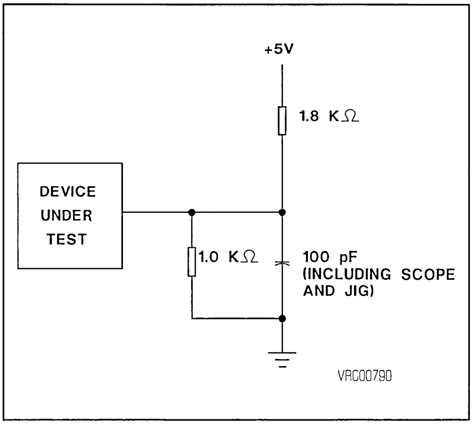
($-40°C \leq T_A \leq +85°C$; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC} - 0.2V$)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	4
I_{OL}	Output Leakage Current	–5	5	µA	4
V_{OH}	Output Logic "1" Voltage ($I_{OUT} = -1.0mA$)	2.4		V	
V_{OL}	Output Logic "0" Voltage ($I_{OUT} = 2.1mA$)		0.4	V	

AC TEST CONDITIONS

Input Levels	0.6V to 2.4V
Transition Times	5ns
Input and Output Timing Reference Levels	0.8V or 2.2V
Ambient Temperature	–40 to 85°C
VCC (MKI48Z02)	4.75 to 5.5V
VCC (MKI48Z12)	4.5 to 5.5V

EQUIVALENT OUTPUT LOAD DIAGRAM



CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	4
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4, 5

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open
4 Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected
5. Effective capacitance calculated from the equation C = I Δt/ΔV with ΔV = 3 volts and power supply at 5.0V.

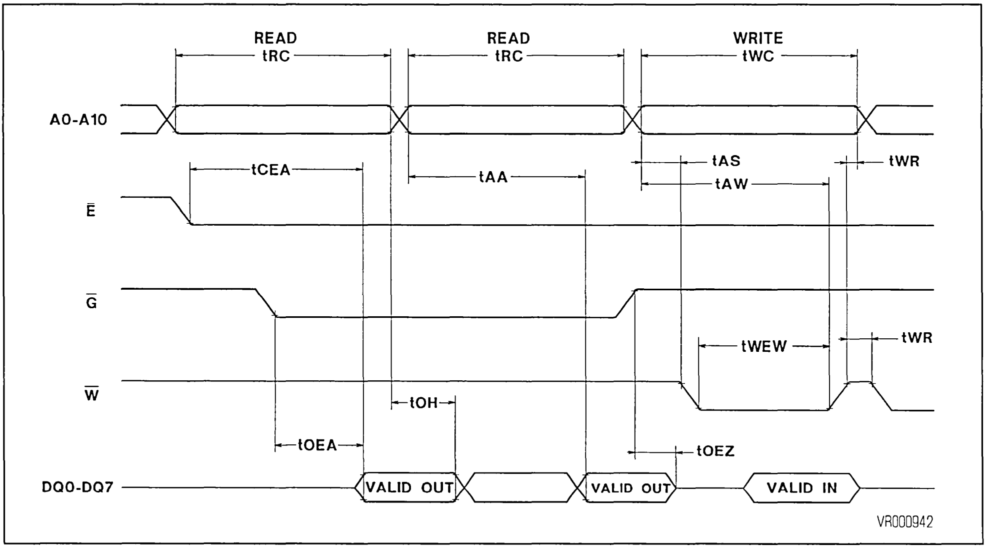
OPERATION

READ MODE

The MKI48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

($-40°C \leq T_A \leq +85°C$; V_{CC} max $\geq V_{CC} \geq V_{CC}$ min)

Symbol	Parameter	MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

Note : Measured using the Output Load Diagram shown Page 4.

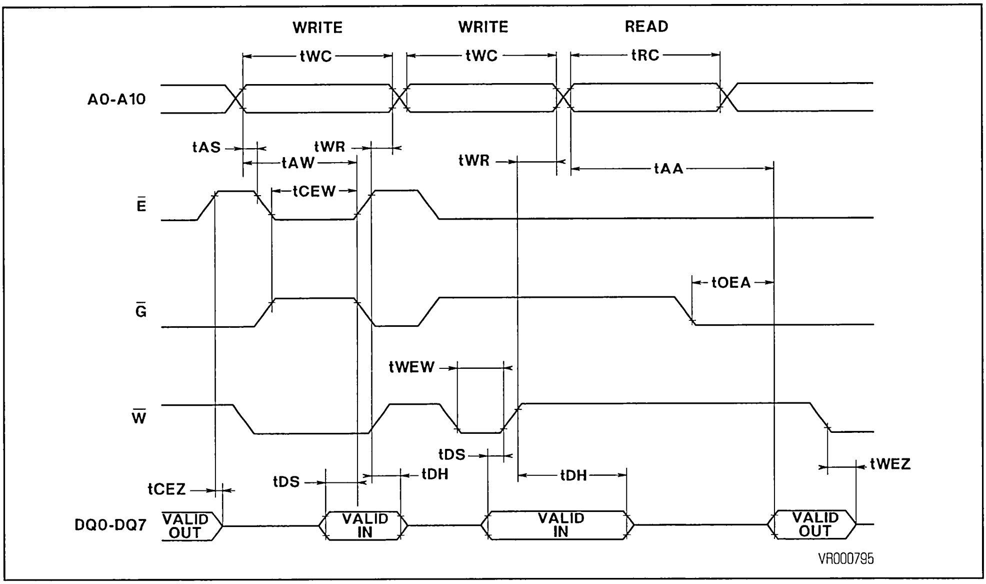
WRITE MODE

The MKI48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterwards.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC}(min) but before the processor stabilizes.

The MKI48Z02/12 $\overline{G}$ input is a don't care in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

($-40°C \leq T_A \leq +85°C$; V_{CC} max $\geq V_{CC} \geq V_{CC}$ min)

Symbol	Parameter	MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{WEW}	Write Enable to End of Write	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MKI48Z02/12 operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MKI48Z02 has a V_{PFD} (max) to V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MKI48Z12 has a V_{PFD} (max) to V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MKI48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{\text{BOK}}$) flag will be set. The $\overline{\text{BOK}}$ flag can be checked after power up. If the $\overline{\text{BOK}}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{\text{BOK}}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{\text{E}}$ or $\overline{\text{W}}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

Figure 5. Checking the $\overline{\text{BOK}}$ Flag Status

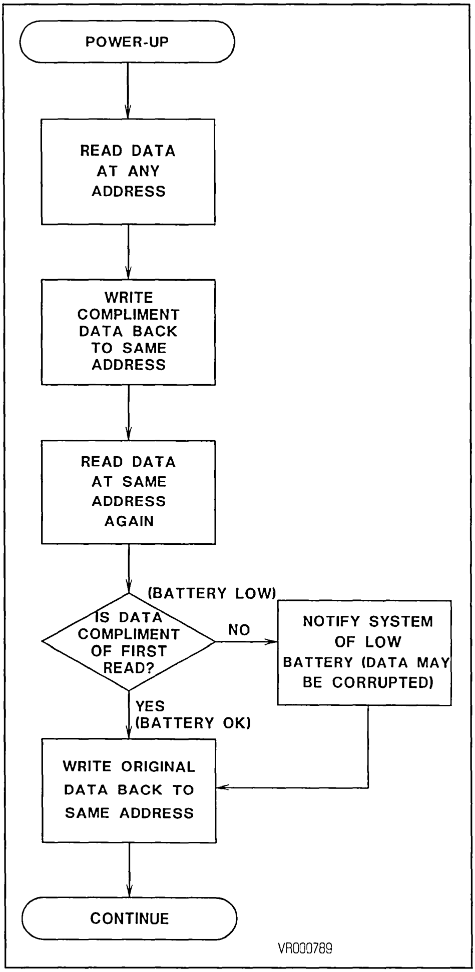
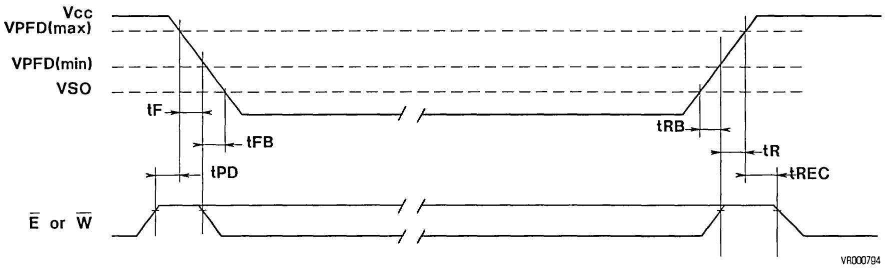

POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
(BATTERY LOW)
IS DATA COMPLIMENT OF FIRST READ?
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES (BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE
VR000789

Figure 6. Power-Down/Power-Up Timing



DC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Trip Point Voltages)

($-40°C \leq T_A \leq +85°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{PFD}	Power-Fail Deselect Voltage (MKI48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-Fail Deselect Voltage (MKI48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Timing)

($-40°C \leq T_A \leq +85°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0			ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2			ms	

Notes :

1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall times of less t_F may result in deselection/write protection not occurring until 50µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MKI48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MKI48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note : The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 80°C is at issue, Figure 7 indicates that a particular MKI48Z02/12 has a 1% chance of having a battery failure 10 years into its life and a 50% chance of failure at the 17 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 10 years ; 50% of them can be expected to fail within 17 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MKI48Z02/12 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H -fabricated in Carrollton, TX; 9 -assembled in Muar, Malaysia; 9 -tested in Muar, Malaysia; 58 -lot designator; 9231 -assembled in the year 1992, work week 31.

CALCULATING PREDICTED BATTERY LIFE

As Figure 7 indicates, the predicted life of the battery in the MKI48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MKI48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MKI48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)] + [(TA_2/TT)/BL_2] + \ldots + [(TA_n/TT)/BL_n)]}$$

Where: TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

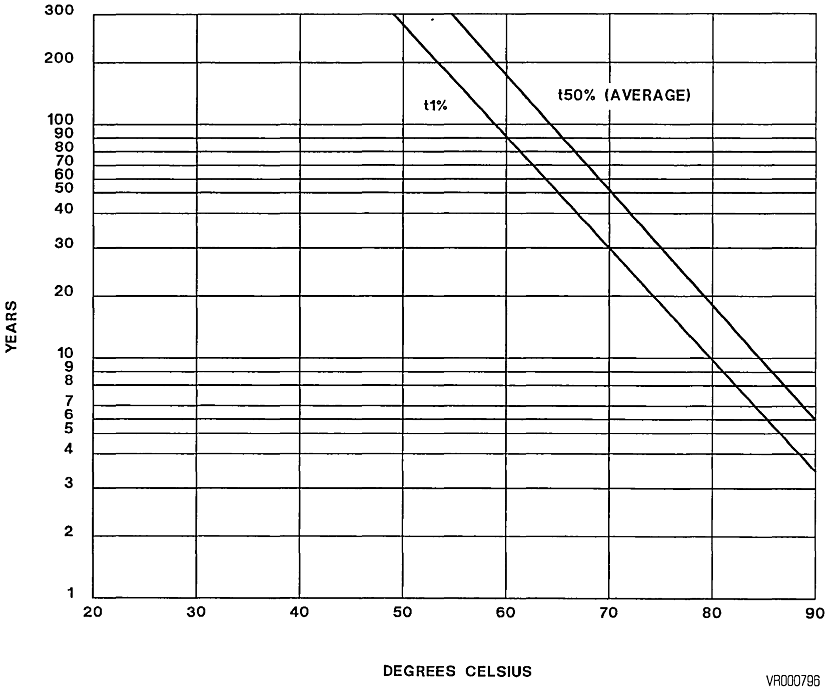
A process control computer operates in an environment where the MKI48Z02/12 is exposed to temperatures of 50°C or less for 3066 hrs/yr ; temperatures greater than 25°C, but less than 60°C for 5256 hrs/yr ; and temperatures greater than 40°C, but less than 85°C for the remaining 438 hrs/yr.

Reading predicted typical life values from Figure 7 ; BL_1 = 275 yrs., BL_2 = 95 yrs., BL_3 = 6 yrs.
Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 = 5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/275] + [(5256/8760)/95] + [(438/8760)/6]}$$

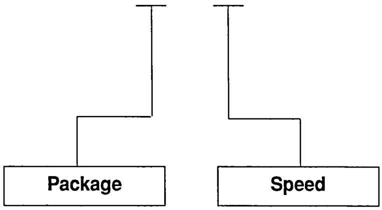
$$\geq 62.8 \text{ yrs.}$$

Figure 7. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION

Example: MKI48Z02 B 15



Package	
B	PHDIP24

Speed	
15	150ns
20	200ns
25	250ns

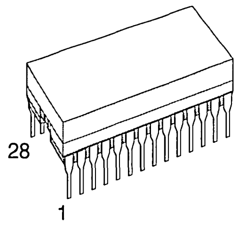
For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

MK48Z08,18
MK48Z09,19

CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES :
  - MK48Z08/09 - 4.50V ≤ V_{PFD} ≤ 4.75V
  - MK48Z18/19 - 4.20V ≤ V_{PFD} ≤ 4.50V



PHDIP28 WITH BATTERY TOP HAT (B)

DESCRIPTION

The MK48Z08/18/09/19 ZEROPOWER™ RAM combines an 8K x 8 full CMOS SRAM and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48Z08/18/09/19 is a Non Volatile, pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z08/18/09/19 has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

PIN NAMES

A0-A12	Address Inputs
$\overline{E}_1$, E_2	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs
$\overline{INT}$	Power Fail Interrupt
V_{CC} / GND	5 Volts / Ground
NC	Not Connected

Figure 1. Pin Connections

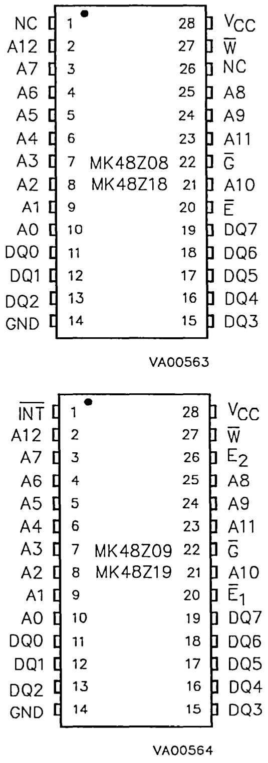
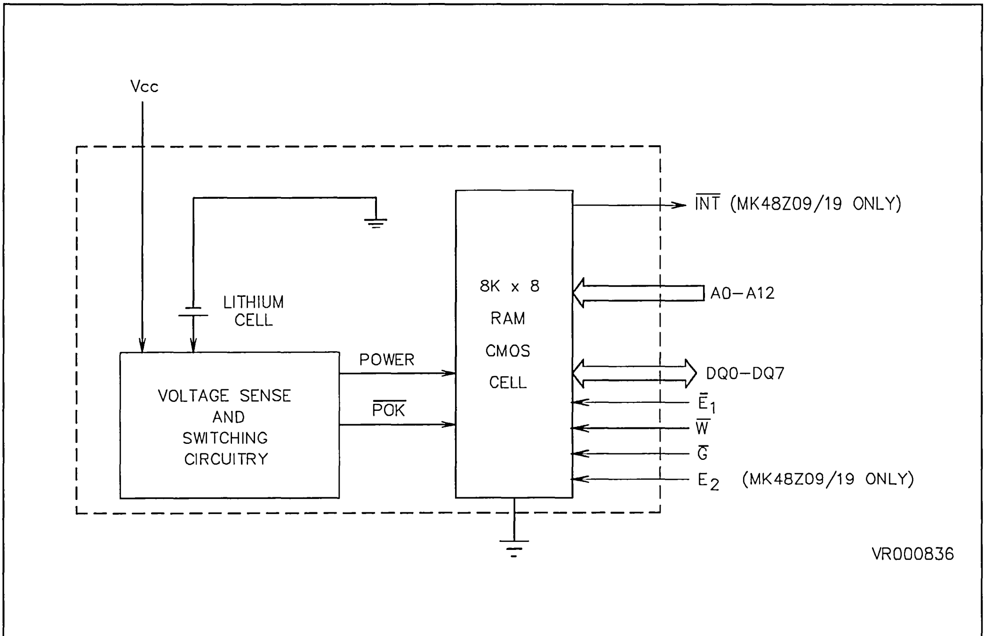

NC 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
MK48Z08
MK48Z18
28 VCC
27 W
26 NC
25 A8
24 A9
23 A11
22 G
21 A10
20 E
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
VA00563
INT 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
MK48Z09
MK48Z19
28 VCC
27 W
26 E2
25 A8
24 A9
23 A11
22 G
21 A10
20 E1
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
VA00564

Figure 2. Block Diagram


Vcc
LITHIUM CELL
VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
$\overline{POK}$
8K x 8 RAM CMOS CELL
$\overline{INT}$ (MK48Z09/19 ONLY)
A0–A12
DQ0–DQ7
$\overline{E}_1$
$\overline{W}$
$\overline{G}$
E_2 (MK48Z09/19 ONLY)
VR000836

TRUTH TABLE (MK48Z08/18)

V_{CC}	E	$\overline{G}$	$\overline{W}$	Mode	DQ	Power
< V_{CC} (max) > V_{CC}(min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up

TRUTH TABLE (MK48Z09/19)

V_{CC}	$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	Mode	DQ	Power
< V_{CC} (max) > V_{CC}(min)	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	X	Deselect	High Z	Battery Back-up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	20	mA
V_{DD}	Voltage on any Pin Relative to GND	–0.3 to +7.0	V
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to 85	°C
T_A	Ambient Operating Temperature	0 to 70	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION *: Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z08/09)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z18/19)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; $V_{CC\,min} \leq V_{CC} \leq V_{CC\,max}$)

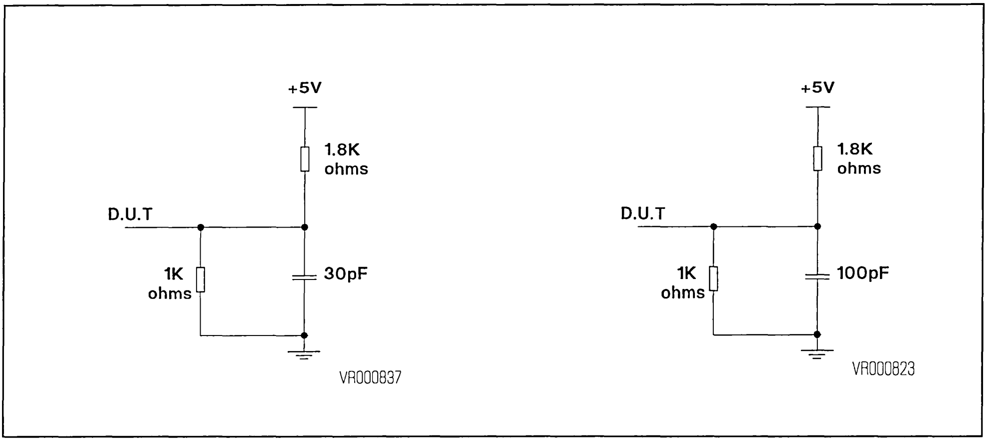
Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		80, 125	mA	3, 6
I_{CC2}	TTL Standby Current ($\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}_1 = V_{CC}$ –0.2V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5mA)		0.4	V	

AC TEST CONDITIONS

Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD DIAGRAM

MK48Z08-70 **MK48Z08,18,09,19**



CAPACITANCE

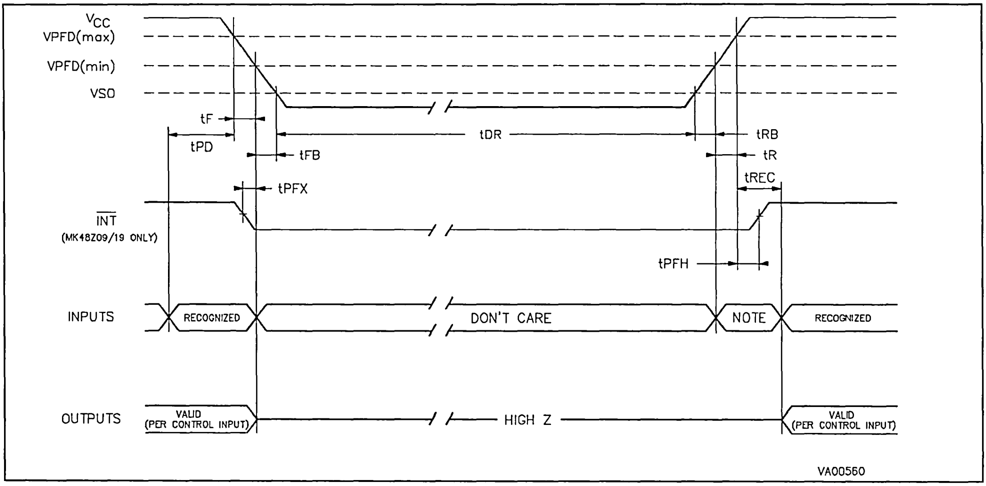
(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	7
C_Q	Capacitance On DQ Pins	10.0	pF	7, 8

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with $V_{CC} \geq V_I \geq$ GND and outpus deselected.
6. 80mA@ 100ns, & 125mA @ 70ns.
7. Effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0V.
8. Measured with outputs deselected.

Figure 3. Power Down/Up Timing


VCC
VPFD(max)
VPFD(min)
VSO
tF
tPD
tFB
tDR
tRB
tR
tREC
tPFX
INT
(MK48Z09/19 ONLY)
tPFH
INPUTS
RECOGNIZED
DON'T CARE
NOTE
RECOGNIZED
OUTPUTS
VALID (PER CONTROL INPUT)
HIGH Z
VALID (PER CONTROL INPUT)
VA00560

Note: Inputs may not be recognized at this time. Caution should be taken to keep $\overline{E}_1$ high or E_2 low as V_{CC} rises past V_{PFD}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PFD}(min)but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
t_{PD}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} before Power Down	0		µs	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs	
t_{REC}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		ms	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ High		120	µs	4

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Values			Unit	Note
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48Z08/09)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z18/19)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	11			YEARS	

Notes : 1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passesV_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.
4. INT may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

READ MODE

The MK48Z08/18/09/19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$(Chip Enable 1) is low, and E_2(Chip Enable 2) is high (MK48Z09/19). The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied. If Chip Enable or Output Enable access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0°C \le T_A \le +70°C$; $V_{CC\,min} \le V_{CC} \le V_{CC\,max}$)

Symbol	Parameter	MK48Z08-70		MK48Zxx-10		Unit	Note
		Min.	Max.	Min.	Max.		
t_{E1LQX}	Chip Enable 1 to Q Low-Z	10		10		ns	
t_{E2HQX}	Chip Enable 2 to Q Low-Z	10		10		ns	
t_{AXQX}	Output Hold from Address	5		5		ns	
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	
t_{AVAV}	Read Cycle Time	70		100		ns	
t_{AVQV}	Address Access Time		70		100	ns	
t_{E1LQV}	Chip Enable 1 Access Time		70		100	ns	
t_{E2HQV}	Chip Enable 2 Access Time		70		100	ns	
t_{GLQV}	Output Enable Access Time		20		50	ns	
t_{E1HQZ}	Chip Enable 1 to Q High-Z		20		50	ns	
t_{E2LQZ}	Chip Enable 2 to Q High-Z		20		50	ns	
t_{GHQZ}	Output Disable to Q High-Z		15		40	ns	

Figure 4. Read Timing n° 1 (Address Access)

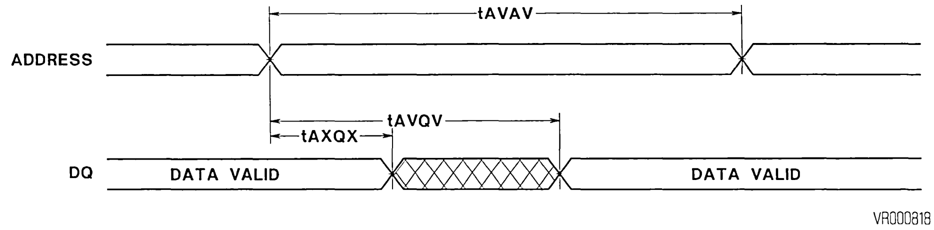
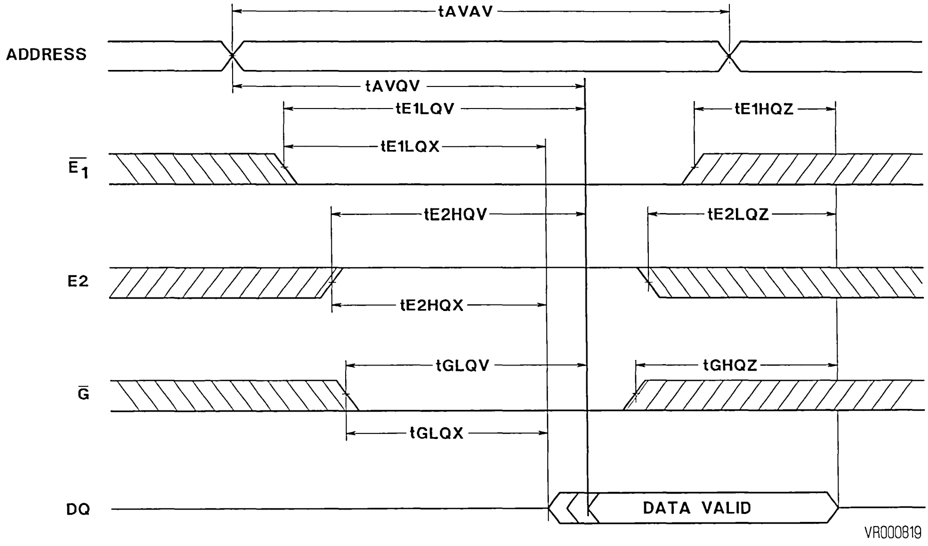

tAVAV
ADDRESS
tAVQV
tAXQX
DQ
DATA VALID
DATA VALID
VR000818

Figure 5. Read Timing n° 2


tAVAV
ADDRESS
tAVQV
tE1LQV
tE1HQZ
tE1LQX
$\overline{E_1}$
tE2HQV
tE2LQZ
E2
tE2HQX
tGLQV
tGHQZ
$\overline{G}$
tGLQX
DQ
DATA VALID
VR000819

WRITE MODE

The MK48Z08/18/09/19 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}_1$ or rising edge of E_2 (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}_1$, or the falling edge of E_2 (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E}_1$ or $\overline{W}$ must return high or E_2 low for minimum of t_{E1HAX} or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterwards.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ goes low. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \leq T_A \leq +70°C$; $V_{CC\ min} \leq V_{CC} \leq V_{CC\ max}$)

Symbol	Parameter	MK48Z08-70		MK48Zxx-10		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVE1L}	Address Set-Up Time to Chip Enable Active	0		0		ns	
t_{AVE2H}		0		0		ns	
t_{E1HAX}	Write Recovery from Chip Enable (Address Hold Time)	10		10		ns	2
t_{E2LAX}		10		10		ns	2
t_{WHDX}	Data Hold Time	5		5		ns	1, 2
t_{AVAV}	Write Cycle Time	70		100		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	50		80		ns	
t_{WLWH}	Write Pulse Width	50		80		ns	
t_{WHAX}	Address Hold after End of Write	10		10		ns	1
t_{E1LE1H}	Chip Enable Active to End of Write	50		80		ns	2
t_{E2HE2L}		50		80		ns	2
t_{DVWH}	Data Valid to End of Write	40		50		ns	1, 2
t_{WHQX}	End of Write to Q Low-Z	10		10		ns	
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		40		50	ns	

Notes :

1. In a $\overline{W}$ Controlled Cycle.
2. In a $\overline{E}_1$, E_2 Controlled Cycle.

Figure 6. Write Control Write Cycle Timing

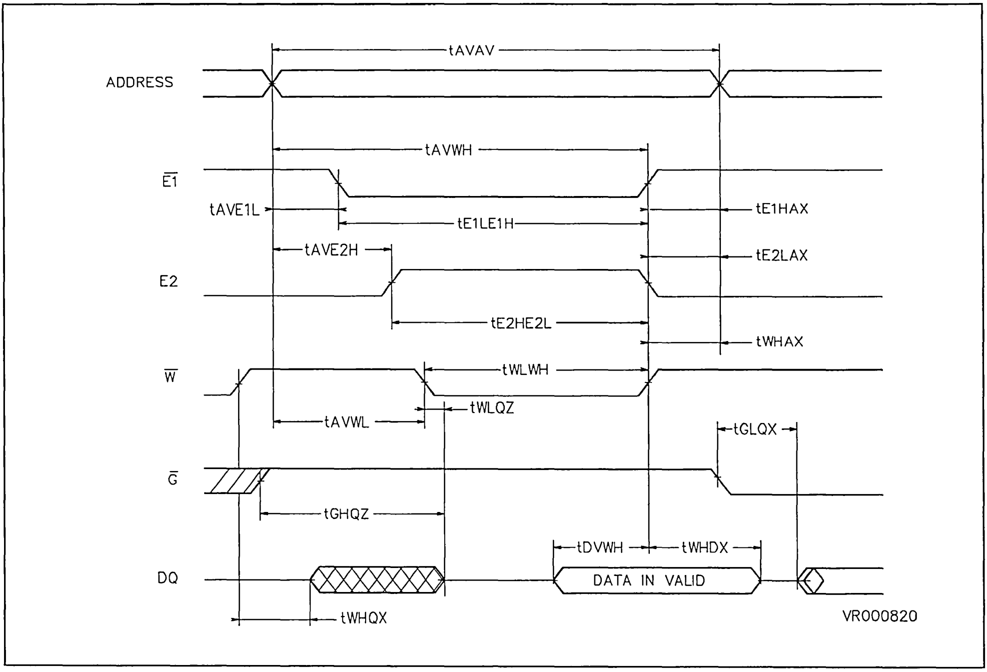
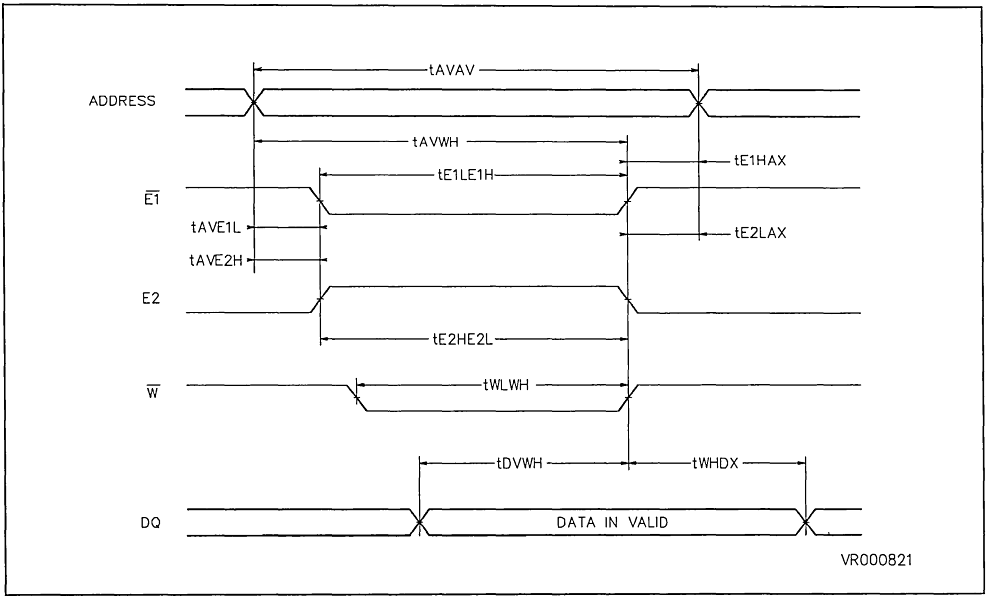

tAVAV
ADDRESS
tAVWH
E1
tAVE1L
tE1HAX
tE1LE1H
tAVE2H
tE2LAX
E2
tE2HE2L
tWHAX
W
tWLWH
tWLQZ
tAVWL
tGLQX
G
tGHQZ
tDVWH
tWHDX
DQ
DATA IN VALID
tWHQX
VR000820

Figure 7. Chip Enable Control Write Cycle Timing


tAVAV
ADDRESS
tAVWH
tE1HAX
tE1LE1H
E1
tAVE1L
tE2LAX
tAVE2H
E2
tE2HE2L
W
tWLWH
tDVWH
tWHDX
DQ
DATA IN VALID
VR000821

DATA RETENTION MODE

With V_{CC} applied, the MK48Z08/18/09/19 operates as a conventional BYTEWIDE™ Static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

Note : A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(Min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48Z08/18/09/19 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}_1$ high (MK48Z08/18) or E_2 low (MK48Z09/19) as V_{CC} rises past V_{PFD}(min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48Z09/19 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point of the MK48Z09/19 an interrupt is immediately generated. An internal clock provides a delay no less than 10µs but no greater than 40 µs before automatically deselecting the MK48Z09/19.The $\overline{INT}$ pin is an open drain output and requires an external pull up resistor.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48Z08/18/09/19 is expected to ultimately come to an end for one of two reasons : either because it has been discharged while providing current to an external load ; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

With V_{CC} on, the battery is disconnected from the RAM and aging effects become the determining factor in battery life. With V_{CC} off, leakage currents in the RAM provide the only load on the Battery during battery back-up. For the MK48Z08/18/09/19, the leakage currents are so low that the Back-up System Life of the device is simply the Storage Life of the cell. The Storage Life of the cell is a function of temperature.

PREDICTING STORAGE LIFE

Figure 8 illustrates how temperature affects Storage Life of the MK48Z08/18/09/19 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48Z08/18/09/19.

Storage Life predictions presented in Figure 8 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

A Special Note : The summary presented in Figure 8 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 8. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 8 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years ; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48Z08/18/09/19 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H -fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9- tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Calculating Predicted Storage Life of the Battery

As Figure 8 indicates, the predicted Storage Life of the battery in the MK48Z08/18/09/19 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 8. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

Example Predicted Storage Life Calculation

Predicted Storage Life = 1 / { [(TA_1 / TT) / SL_1] + [(TA_2 / TT) / SL_2] + ...+ [(TA_N / TT) / SL_N] }

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = TA_1 + TA_2 + ... + TA_N

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 8)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48Z08/18/09/19 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

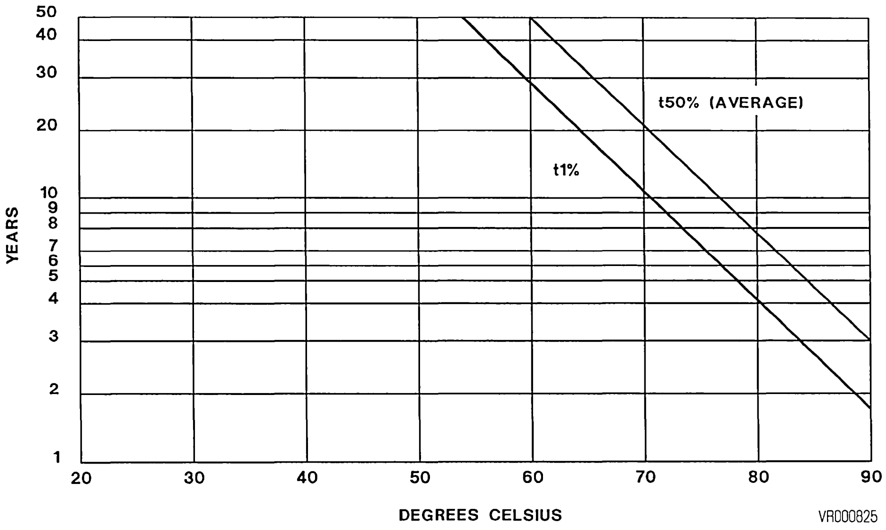
Reading Predicted $t_{1\%}$ values from Figure 8; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

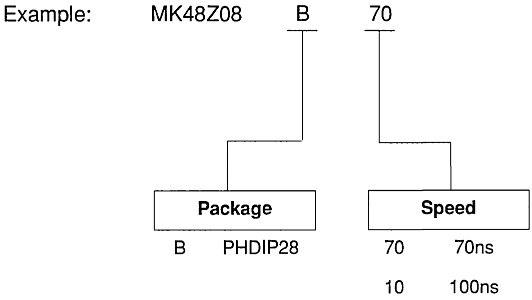
Predicted Typical Storage Life ≥ 1 / { [(8322 / 8760) / 41] + [(438 / 8760) / 11.4]

Predicted Typical Storage Life ≥ 36 years

Figure 8. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION


Example:
MK48Z08
B
70
Package
Speed
B PHDIP28
70 70ns
10 100ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MKI48Z18

CMOS 8K x 8 ZEROPOWER SRAM

ADVANCE DATA

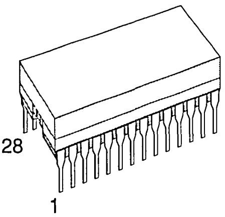
- INDUSTRIAL TEMPERATURE RANGE -40°C TO +85°C
- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND ENERGY SOURCE
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- PREDICTED WORST CASE BATTERY LIFE OF 6 YEARS @ 85°C
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT /WRITE PROTECTION.

DESCRIPTION

The MKI48Z18 8K x 8 ZEROPOWER™ RAM is a nonvolatile 65,536 bit SRAM organized as 8192 words by 8 bits. The device combines an internal long life lithium battery and a full CMOS SRAM in a plastic 28 pin DIP. The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

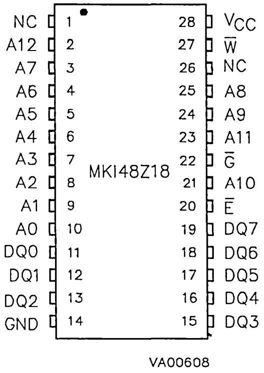
The MKI48Z18 has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

The MKI48Z18 is offered with an access time of 100ns. The device is operational over a temperature range of -40°C to +85°C. For a complete description of electrical characteristics and bus timing, refer to the MK48Z18B10 specifications contained within the MK48Z08,18 data sheet.



PHDIP28 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection



PIN NAMES

A0-A12	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
Vcc	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data In/Data Out

This is advance information on a new product now in develpment or undergoing evaluation Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Symbol	PARAMETER	VALUES	UNITS
P_D	Total Device Power Dissipation	1.0	W
I_{OUT}	Output Current Per Pin	20	mA
V_I	Voltage on any Pin Relative to Ground	–0.3 to + 7.0	V
T_{STG}	Ambient Storage (V_{cc} Off) Temperature	–40 to +85	°C
T_A	Ambient Operating Temperature	–40 to +85	°C

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS (–40°C≤ T_A ≤+85°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
Vcc	Supply Voltage	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

(-40°C≤ T_A ≤+85°C; Vcc min ≤ Vcc ≤ Vcc max)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{cc1}	Average Vcc Power Supply Current		80	mA	3
I_{cc2}	TTL Standby Current ($\overline{E}$= V_{IH})		3	mA	
I_{cc3}	CMOS Standby Current ($\overline{E}$ = Vcc –0.2V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)		0.4	V	

NOTES :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1mA typical.
5. Measured with Vcc ≥ V_I≥ GND and outputs deselected.

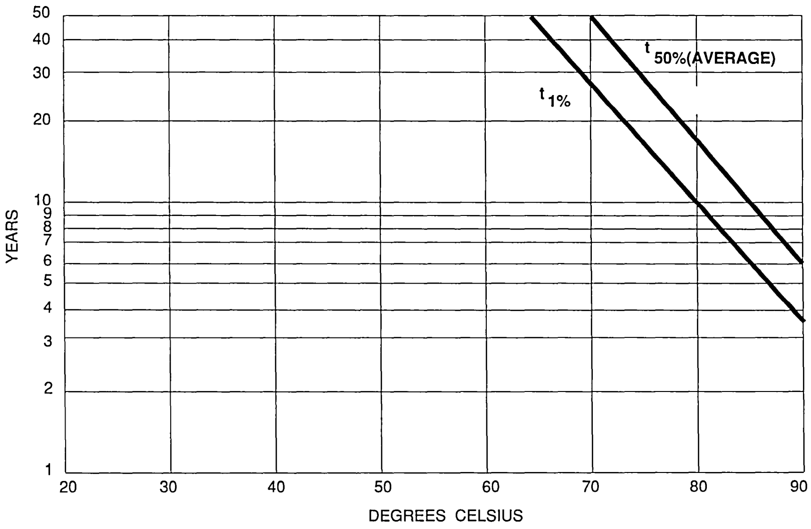
PREDICTING BATTERY LIFE

Figure 2 illustrates how temperature affects Battery Storage Life of the MKI48Z18. Since the leakage currents of the MKI48Z18 are so low, Storage Life of the battery is the limiting factor in defining the Battery Lifetime of the device. Thus, Battery Lifetime is controlled by temperature and is virtually unaffected by the current requirements of the MKI48Z18 RAM.

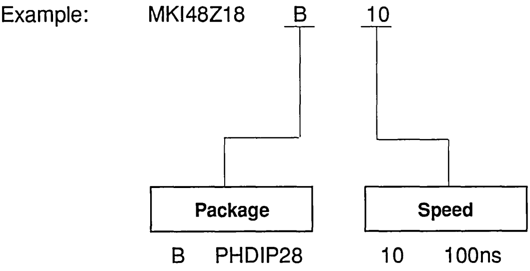
Storage Life predictions presented in Figure 2 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K load resistance.

Two end of life curves are presented in Figure 2. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 85°C is at issue, Figure 2 indicates that a particular MKI48Z18 has a 1% chance of having a battery failure 6.5 years into its life and a 50% chance of failure at the 10 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 6.5 years; 50% of them can be expected to experience a failure within 10 years.

Figure 2. Predicted Battery Storage Life Versus Temperature



ORDERING INFORMATION


Example: MKI48Z18 B 10
Package
B PHDIP28
Speed
10 100ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK48Z30
MK48Z30Y

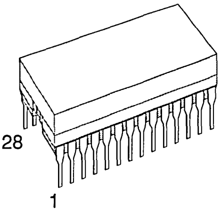
CMOS 32K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- MINIMUM BATTERY BACK-UP OF 10 YEARS @ 25°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32K X 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT / WRITE PROTECTION.
- DUAL WRITE PROTECT VOLTAGES:
  MK48Z30 - $4.50V \leq V_{PFD} \leq 4.75V$
  MK48Z30Y - $4.20V \leq V_{PFD} \leq 4.50V$

DESCRIPTION

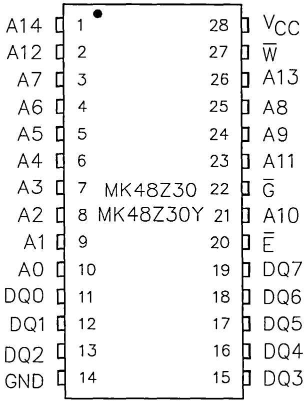
The MK48Z30/30Y ZEROPOWER™ RAM combines a 32K x 8 full CMOS SRAM and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48Z30/30Y is a nonvolatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z30/30Y has its own Powerfail Detect Circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.



PHDIP28 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection

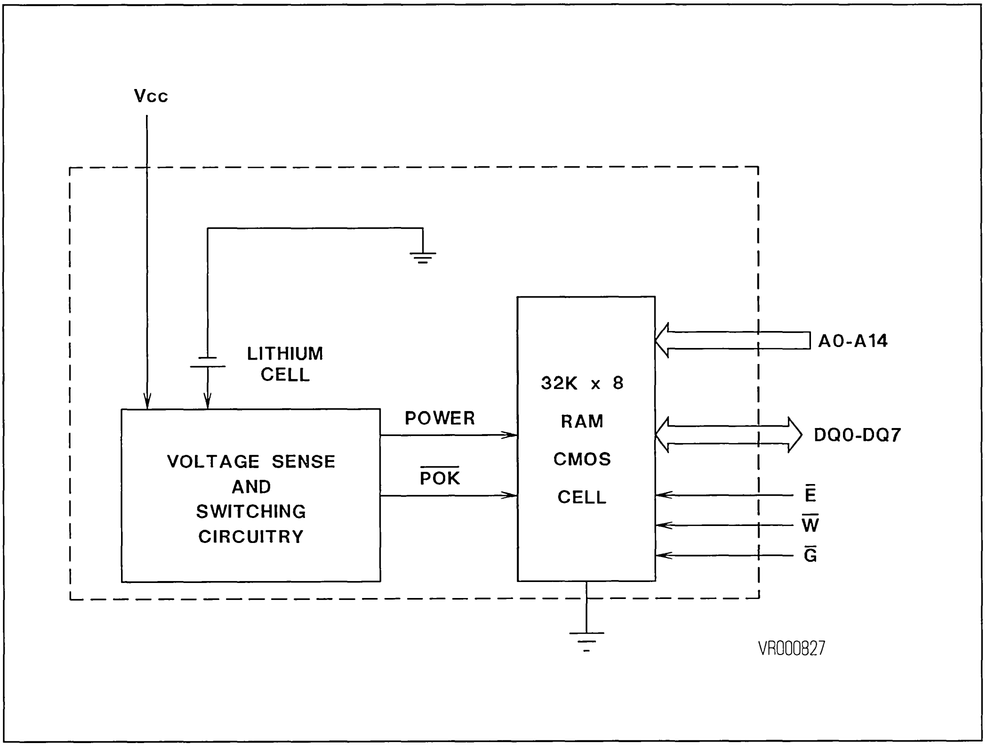

A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
28 VCC
27 W
26 A13
25 A8
24 A9
23 A11
22 G
21 A10
20 E
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
MK48Z30
MK48Z30Y

VA00605

PIN NAMES

A0-A14	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs
V_{CC}, GND	5 Volts, Ground

Figure 2. Block Diagram


Vcc
LITHIUM CELL
VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
$\overline{\text{POK}}$
32K x 8 RAM CMOS CELL
A0-A14
DQ0-DQ7
$\overline{\text{E}}$
$\overline{\text{W}}$
$\overline{\text{G}}$
VR000827

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ	Power
< V_{CC} (max) > V_{CC}(min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	50	mA
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7.0	V
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to 70	°C
T_A	Ambient Operating Temperature	0 to 70	°C

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

***CAUTION:** Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z30)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z30Y)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS
($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le$ V_{CC} max)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current (70ns)		85	mA	3
I_{CC1}	Average V_{CC} Power Supply Current (120ns)		70	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current (V_{CC} max $\ge \overline{E} \ge$ V_{CC} –0.3V)		2	mA	
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	4
I_{OL}	Output Leakage Current	–2	2	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –4.0mA)	2.4		V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +8.0mA)		0.4	V	1

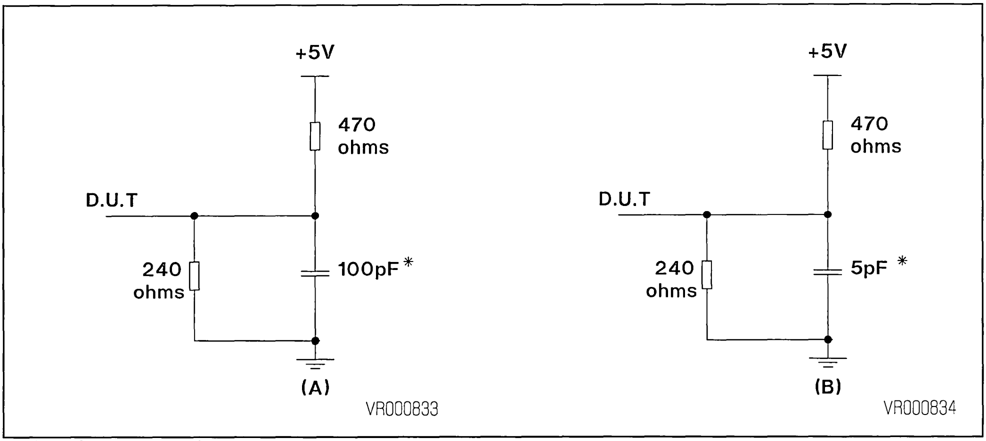
Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $V_{CC} \ge V_I \ge$ GND and outputs deselected.

AC TEST CONDITIONS

Input Levels	0.0V to 3.0V
Transition Times	1.5 ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS


+5V
470 ohms
D.U.T
240 ohms
100pF *
(A)
VR000833
+5V
470 ohms
D.U.T
240 ohms
5pF *
(B)
VR000834

* Includes Scope and Test Jig

CAPACITANCE

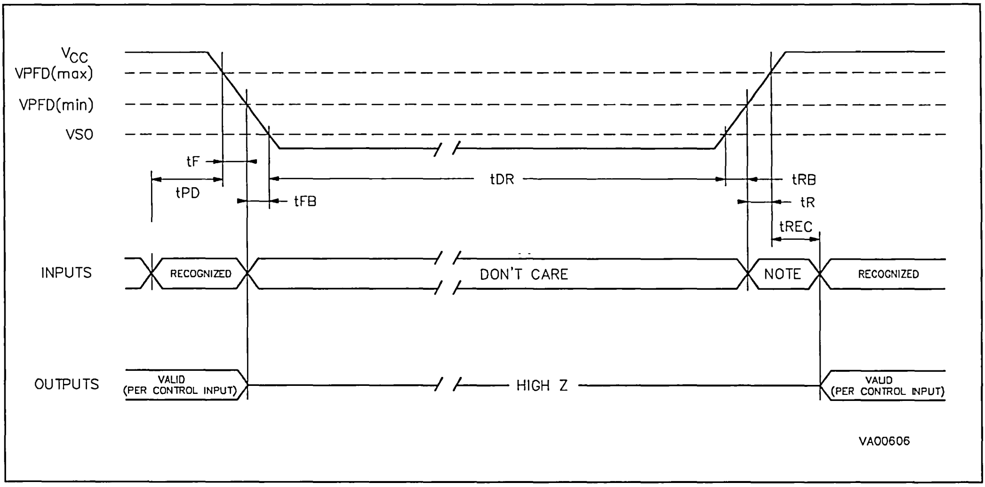
(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	1
C_{DQ}	Capacitance On DQ Pins	10.0	pF	1, 2

Notes :

1. Effective capacitance calculated from the equation C = I Δt/ΔV with ΔV = 3 volts and power supply at 5.0 V.
2. Measured with outputs deselected.

Figure 3. Power Up/Down Waveform


VCC
VPFD(max)
VPFD(min)
VSO
tF
tPD
tFB
tDR
tRB
tR
tREC
INPUTS
RECOGNIZED
DON'T CARE
NOTE
RECOGNIZED
OUTPUTS
VALID (PER CONTROL INPUT)
HIGH Z
VALID (PER CONTROL INPUT)
VA00606

REFERENCE : Inputs may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PDF}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PDF}(min)but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD}(min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	5		ms	

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Value			Units	Notes
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48Z30)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z30Y)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		2.5		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	4

Notes :
1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.
4. @ 25°C

READ MODE

The MK48Z30/30Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied. If Chip Enable or Output Enable access times are not met, valid data will be available at the Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Data Hold Time (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

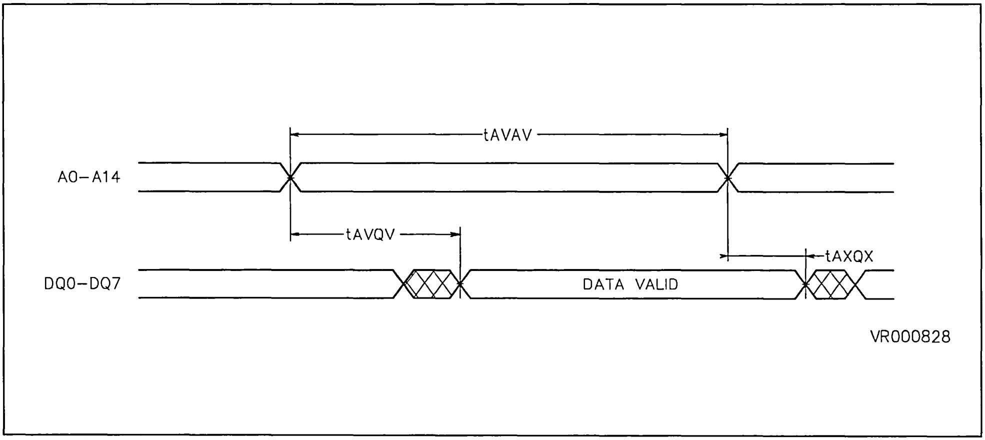
($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le$ V_{CC} max)

Symbol	Parameter	MK48Z30/30Y-70		MK48Z30/30Y-12		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVAV}	Read Cycle Time	70		120		ns	
t_{AVQV}	Address Access Time		70		120	ns	1
t_{ELQV}	Chip Enable Access Time		70		120	ns	1
t_{GLQV}	Output Enable Access Time		35		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	10		10		ns	2
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	2
t_{EHQZ}	Chip Disable ($\overline{E}$) High to Q High-Z	0	25	0	35	ns	2
t_{GHQZ}	Output Disable ($\overline{G}$) High to Q High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

Notes :

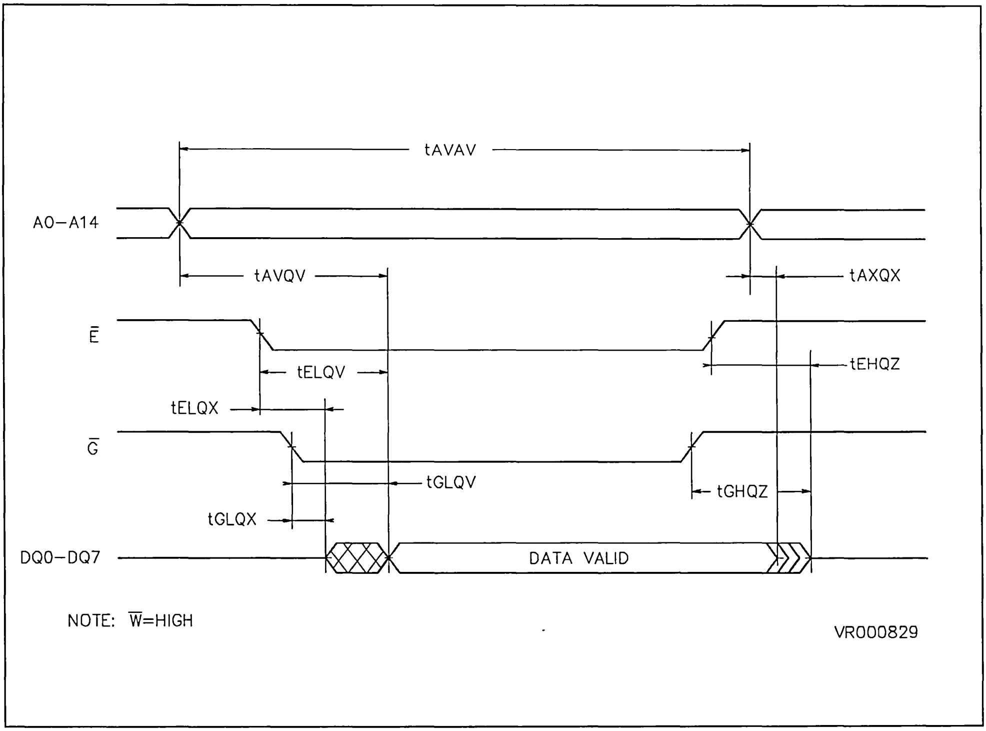
1. Measured with load as shown in Figure A page 4.
2. Measured with load as shown in Figure B page 4.

Figure 4. Read Timing n° 1 (Address Access)


tAVAV
A0–A14
tAVQV
tAXQX
DQ0–DQ7
DATA VALID
VR000828

Note: $\overline{E}$ = $\overline{G}$ = Low, $\overline{W}$ = High

Figure 5. Read Timing n° 2


tAVAV
A0–A14
tAVQV
tAXQX
Ē
tELQV
tEHQZ
tELQX
G̅
tGLQV
tGHQZ
tGLQX
DQ0–DQ7
DATA VALID
NOTE: W̅=HIGH
VR000829

WRITE MODE

The MK48Z30/30Y is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of Write Enable or Chip Enable. A write is terminated by the earlier rising edge of Write Enable or Chip Enable. The addresses must be held valid throughout the cycle. Chip Enable or Write Enable must return high or for minimum of t_{WHAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward.

Because Output Enable is a Don't Care in the Write Mode and a low on Write Enable will return the outputs to High-Z, Output Enable can be tied low and two-wire RAM control can be implemented. A low on Write Enable will disable the outputs t_{WLQZ} after Write Enable falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \leq T_A \leq +70°C$; V_{CC} min $\leq V_{CC} \leq$ V_{CC} max)

Symbol	Parameter	MK48Z30/30Y-70		MK48Z30/30Y-12		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVAV}	Write Cycle Time	70		120		ns	
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-Up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	60		85		ns	
t_{WLWH}	Write Pulse Width	50		65		ns	
t_{WHAX}	Address Hold after End of Write	0		0		ns	
t_{ELEH}	Chip Enable Active to End of Write	55		85		ns	
t_{EHAX}	Address Hold Time from Chip Enable	0		0		ns	
t_{DVWH}	Data Valid to End of Write	30		40		ns	
t_{WHDX}	Data Hold Time	0		0		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	5		5		ns	1
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	25	0	35	ns	1

Notes :

1. Measured with load as shown in Figure B page 4.

Figure 6. Write Control Write Cycle Timing

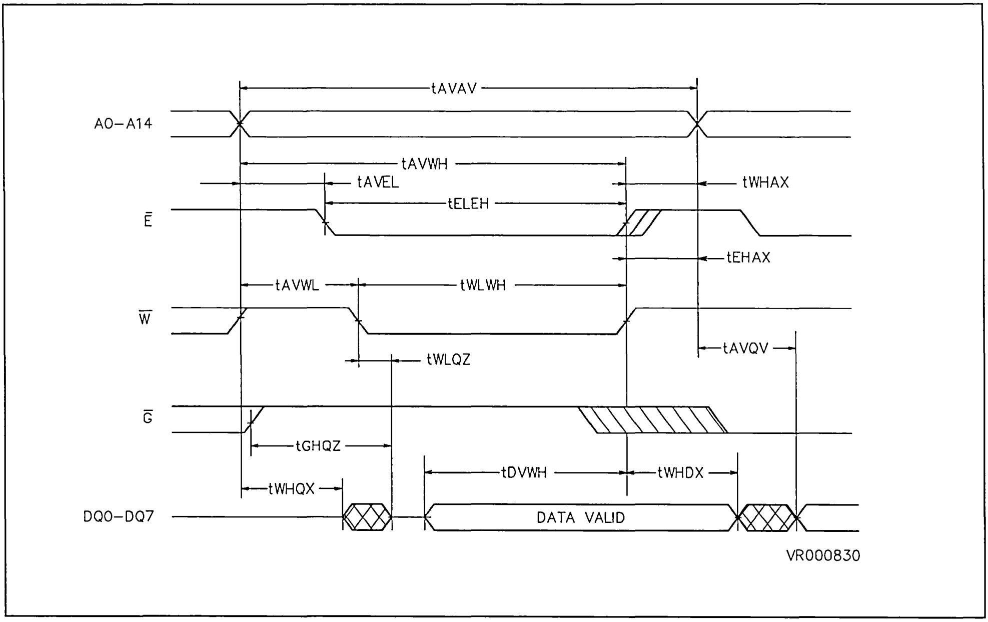
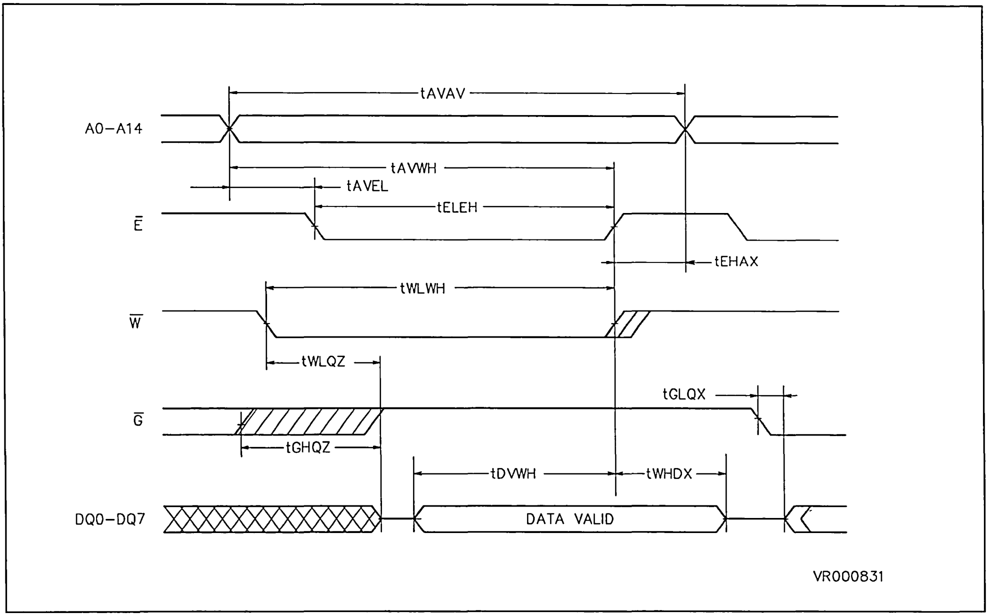

tAVAV
A0-A14
tAVWH
tAVEL
tWHAX
tELEH
E
tEHAX
tAVWL
tWLWH
W
tWLQZ
tAVQV
G
tGHQZ
tDVWH
tWHDX
tWHQX
DQ0-DQ7
DATA VALID
VR000830

Figure 7. Chip Enable Control Write Cycle Timing


tAVAV
A0-A14
tAVWH
tAVEL
tELEH
E
tEHAX
tWLWH
W
tWLQZ
tGLQX
G
tGHQZ
tDVWH
tWHDX
DQ0-DQ7
DATA VALID
VR000831

DATA RETENTION MODE

With V_{CC} applied, the MK48Z30/30Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window.

A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD}(min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

BACK-UP SYSTEM LIFE

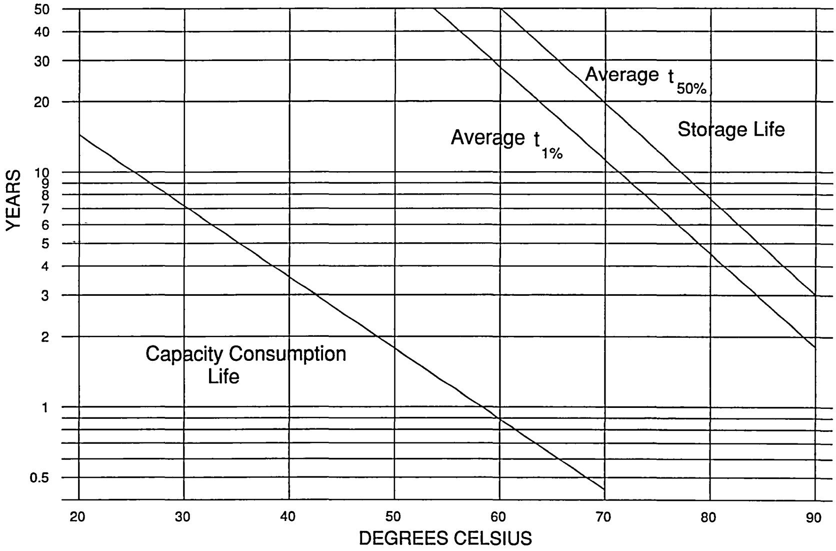
The useful life of the battery in the MK48Z30/30Y is expected to ultimately come to an end for one of two reasons: either because the effects of aging render the cells useless before it can actually be discharged; or because it has have been discharged while providing current to an external load. These two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous battery end-of-life mechanisms.

With V_{CC} on, the battery is disconnected from the RAM and Storage Life becomes the determining factor in battery longevity.

With V_{CC} off, the MK48Z30/30Y initiates back-up mode by switching power from the V_{CC} input to the internal battery. In the back-up mode, leakage current drawn by the RAM represents the only load on the battery. The load condition consumes the cell's capacity and is therefore referred to as Capacity Consumption. Capacity Consumption is the primary battery end-of-life mechanism while the MK48Z30/30Y is in the battery back-up mode.

Battery life is defined as beginning on the date of manufacture. Each MK48Z30/30Y is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H - fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9 - tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Figure 8. Predicted Battery Storage Life Versus Temperature



Storage Life

Figure 8 illustrates how temperature affects Storage Life of the MK48Z30/30Y battery.

Two End-of- Life curves related to Storage Life are presented in the Figure 8. They are labeled "Average" ($t_{1\%}$), and "Average" ($t_{50\%}$). These terms define the probability that a given number of failures will accumulate by a particular point in time. If, for example, a battery's expected life at 70°C is an issue, Figure 8 indicates that an MK48Z30/30Y has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year time. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years and 50% of them within 20 years.

Calculating Predicted Storage Life of the Battery

As Figure 8 indicates, the predicted Storage Life of the MK48Z30/30Y battery is a function of temperature. As long as the ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 8. If the MK48Z30/30Y spends an appreciable amount of time at a variety of temperatures, the following equation can be used to estimate Storage Life.

$$\text{Predicted Storage Life} \geq \frac{1}{[(TA_1/TT/SL_1) + (TA_2/TT/SL_2) + (TA_N/TT/SL_N)]}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc....

TT = Total Time = $TA_1 + TA_2 + ...+ TA_N$

SL_1, SL_2, SL_N = Storage Life at Temp.1, Temp.2, etc... (See Figure 8)

Example Storage Life Calculation

A terminal operates in an environment where the MK48Z30/30A is exposed to temperatures of 40°C or less for 4380 hrs/yr; temperatures greater than 25°C but less 50°C for 3504 hrs/yr; and temperatures greater 50°C but less than 70°C for the remaining 876 hrs/yr.

Reading Predicted $t_{1\%}$ Storage Life values from Figure 8:

SL_1 = 175 yrs, SL_2 = 70 yrs, SL_3 = 11 yrs.

Total Time (TT) = 8760 hrs/yr

TA_1 = 4380 hrs/yr, TA_2 = 3504 hrs/yr, TA_3 = 876 hrs/yr.

$$\text{Predicted Storage Life} \geq \frac{1}{[(4380/8760/175)+ (3504/8760/70) + (876/8760/11)]}$$

$$\geq 56.7 \text{ yrs.}$$

Predicting Capacity Consumption Life

The MK48Z30/30Y battery cell has a minimum rated capacity of 39 mAh. The RAM, in battery-backed mode, places a nominal load of 445nA at 25 °C. At this rate, the MK48Z30/30Y will consume the capacity of the battery cell in 87,600 hours or about 10 years.

Figure 8 also shows how Capacity Consumption varies with temperature. Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate consumption rates in a given design. As long as ambient temperature is held reasonably constant, expected Capacity Consumption Life can be estimated directly from the curve in Figure 8. At 30 °C and 0% Vcc Duty Cycle, the Capacity Consumption Life is 7 years. As Vcc Duty Cycle increases, though, so does Capacity Consumption Life. At 30 °C and 40% power on Duty Cycle, the Capacity Consumption Life is

$$7/(1-0.40) = 11.7 \text{ years.}$$

If the MK48Z30/30Y spends an appreciable amount of time at a variety of temperatures, the same equation used to estimate Storage Life can be used to estimate Capacity Consumption Life.

Example Consumption Life Calculation

Using the same terminal example described earlier, assume the terminal is turned off for 14 hours a day. During these 14 hours the MK48Z30/30Y is in the battery back-up mode and is exposed to 35°C for 5 hrs and 25°C for the remaining 9 hrs. The two points of interest on the Capacity Consumption curve of Figure 8 are at the 35°C and the 25°C temperatures.

Reading the Capacity Consumption values from Figure 8 :

$$CL_1 = 5 \text{ yrs}, CL_2 = 10 \text{ yrs}$$

$$\text{Total Time (TT)} = 8760 \text{ hrs/yr}$$

$$TA_1 = 1825 \text{ hrs/yr}, TA_2 = 3285 \text{ hrs/yr.}$$

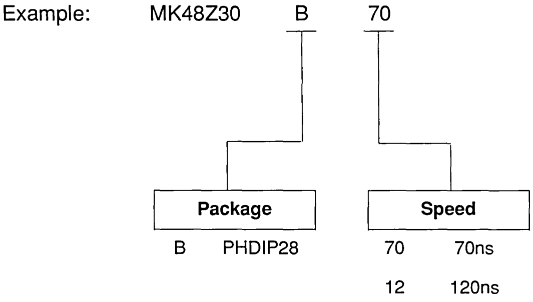
$$\text{Predicted Storage Life} \geq \frac{1}{[(1825/8760/5) + (3285/8760/10)]}$$

$$\geq 12.6 \text{ yrs.}$$

Estimating Back-up System Life

Either Storage or Capacity Consumption can end the System Life of the MK48Z30/30Y. Since these mechanisms are independent, the lower of the two estimated lifetimes defines the Battery Life. In the previous examples, the System Life of the MK48Z30/30Y would be at least 12.6 years.

ORDERING INFORMATION



Package	
B	PHDIP28

Speed	
70	70ns
12	120ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

MK48Z32
MK48Z32Y

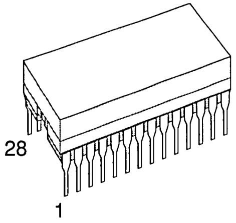
CMOS 32K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- UNLIMITED WRITE-CYCLES.
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME.
- MINIMUM BATTERY BACK-UP OF 10 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 32K x 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT / WRITE PROTECTION.
- DUAL WRITE PROTECT VOLTAGE:
  - MK48Z32 - 4.50V $\leq V_{PFD} \leq$ 4.75V
  - MK48Z32Y - 4.20V $\leq V_{PFD} \leq$ 4.50V

DESCRIPTION

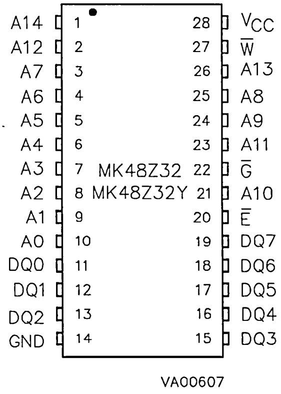
The MK48Z32/32Y ZEROPOWER™ RAM combines an 32K x 8 full CMOS SRAM and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48Z32/32Y is a nonvolatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into may EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

In addition, the MK48Z32/32Y has its own Power-fail Detect Circuit. The circuit deselects the device whenever V_{CC} is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.



PHDIP28 WITH BATTERY TOP HAT (B)

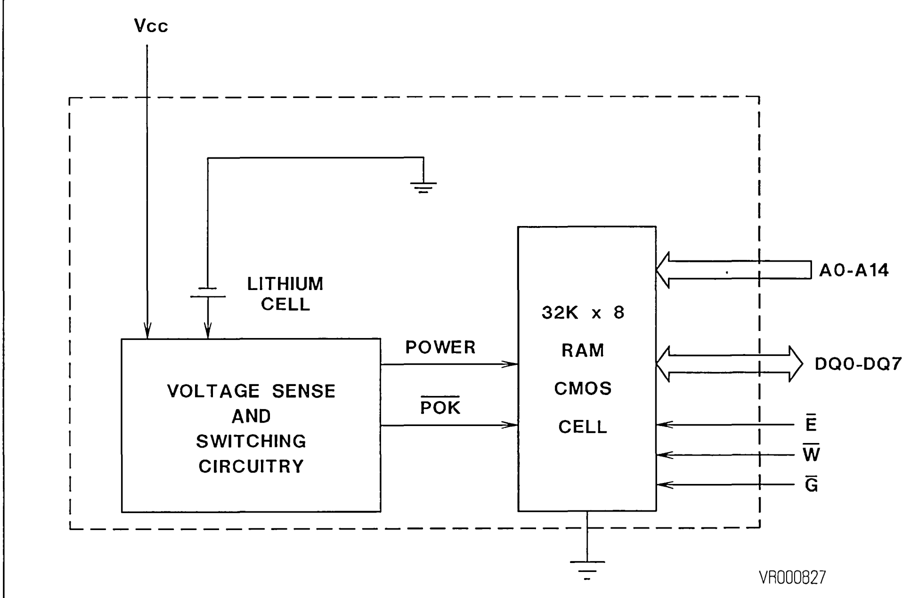
Figure 1. Pin Connection


A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
28 VCC
27 W
26 A13
25 A8
24 A9
23 A11
22 G
21 A10
20 E
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3
MK48Z32
MK48Z32Y
VA00607

PIN NAMES

A0-A14	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Inputs/Outputs
V_{CC} , GND	5 Volts, Ground

Figure 2. Block Diagram


Vcc
LITHIUM CELL
VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
$\overline{\text{POK}}$
32K x 8 RAM CMOS CELL
A0-A14
DQ0-DQ7
$\overline{\text{E}}$
$\overline{\text{W}}$
$\overline{\text{G}}$
VR000827

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ	Power
< V_{CC} (max) > V_{CC}(min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	50	mA
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7.0	V
T_{STG}	Ambient Storage (V_{CC} Off) Temperature	–40 to 70	°C
T_A	Ambient Operating Temperature	0 to 70	°C

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48Z32)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48Z32Y)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS
(0°C $\leq T_A \leq$ +70°C; V_{CC} min $\leq V_{CC} \leq$ V_{CC} max)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current (70ns)		85	mA	3
I_{CC1}	Average V_{CC} Power Supply Current (120ns)		70	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current (V_{CC} max $\geq \overline{E} \geq$ V_{CC} –0.3V)		2	mA	
I_{IL}	Input Leakage Current (Any Input)	-1	+1	µA	4
I_{OL}	Output Leakage Current	-2	+2	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –4.0mA)	2.4		V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +8.0mA)		0.4	V	1

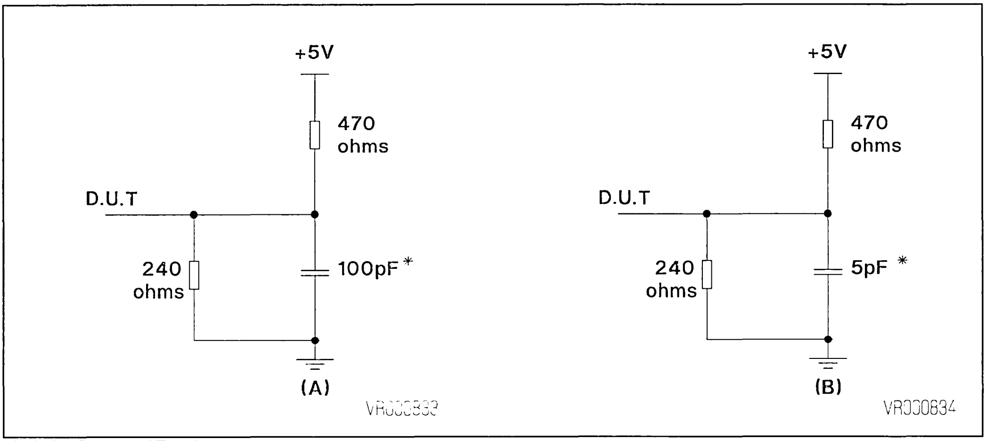
Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10 ns once per Cycle.
3 I_{CC1} measured with outputs open.
4 Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected

AC TEST CONDITIONS

Input Levels	0.0V to 3.0V
Transition Times	1.5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS


+5V
470 ohms
D.U.T
240 ohms
100pF *
(A)
VR000833
+5V
470 ohms
D.U.T
240 ohms
5pF *
(B)
VR000834

* Includes Scope and Test Jig

CAPACITANCE

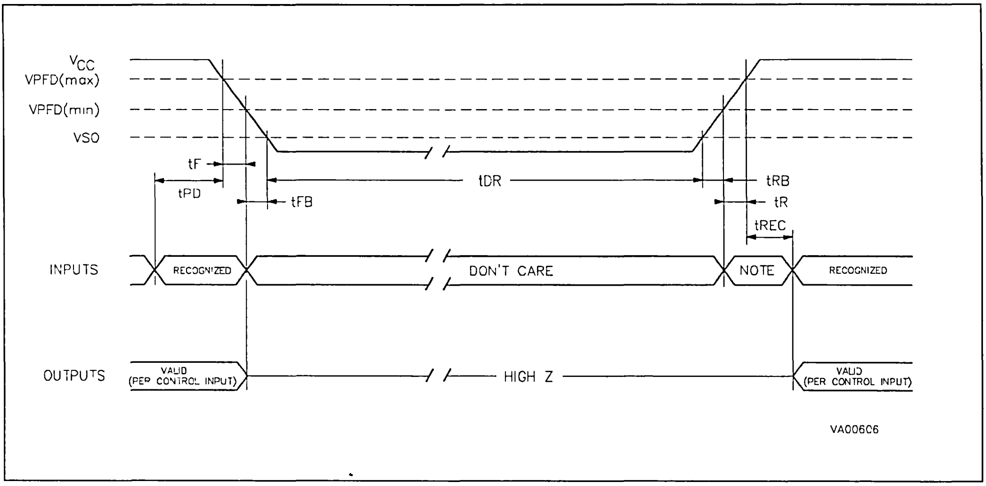
(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	1
C_{DQ}	Capacitance On DQ Pins	10.0	pF	1, 2

Notes :

1. Effective capacitance calculated from the equation $C = I\ \Delta t/\Delta V$ with ΔV = 3 volts and power supply at 5.0 V.
2. Measured with outputs deselected.

Figure 3. Power Up/Down Waveform


VCC
VPFD(max)
VPFD(min)
VSO
tF
tPD
tDR
tFB
tRB
tR
tREC
INPUTS
RECOGNIZED
DON'T CARE
NOTE
RECOGNIZED
OUTPUTS
VALID (PER CONTROL INPUT)
HIGH Z
VALID (PER CONTROL INPUT)
VA00606

NOTE : Inputs may not be recognized at this time Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PFD}(min)but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD}(min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	5		ms	

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Value			Units	Notes
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48Z32)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z32Y)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		2.5		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	

Notes :
1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3 V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data

READ MODE

The MK48Z32/32Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied. If Chip Enable or Output Enable access times are not met, valid data will be available at the Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Data Hold Time (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0°C \leq T_A \leq +70°C$; V_{CC} min $\leq V_{CC} \leq$ V_{CC} max)

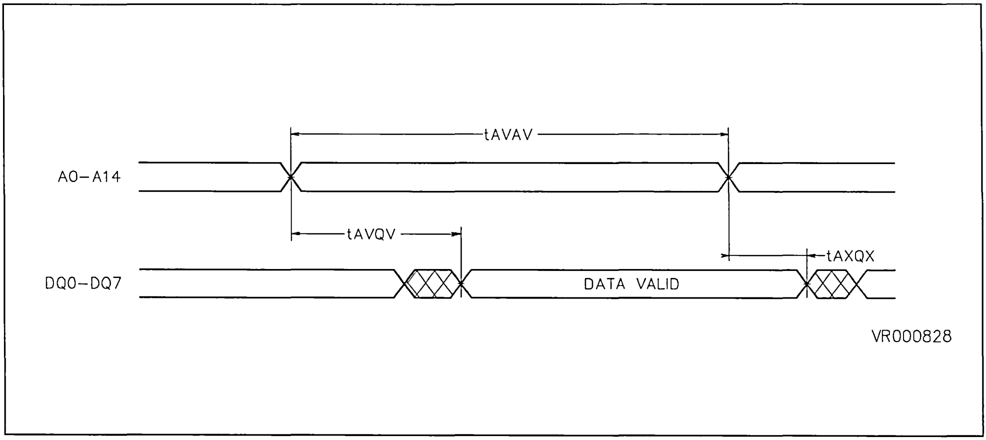
Symbol	Parameter	MK48Z32/32Y-70		MK48Z32/32Y-12		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVAV}	Read Cycle Time	70		120		ns	
t_{AVQV}	Address Access Time		70		120	ns	1
t_{ELQV}	Chip Enable Access Time		70		120	ns	1
t_{GLQV}	Output Enable Access Time		35		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	10		10		ns	2
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	2
t_{EHQZ}	Chip Disable ($\overline{E}$) High to Q High-Z	0	25	0	35	ns	2
t_{GHQZ}	Output Disable ($\overline{G}$) High to Q High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

Notes :

1 Measured with load as shown in Figure A page 4.

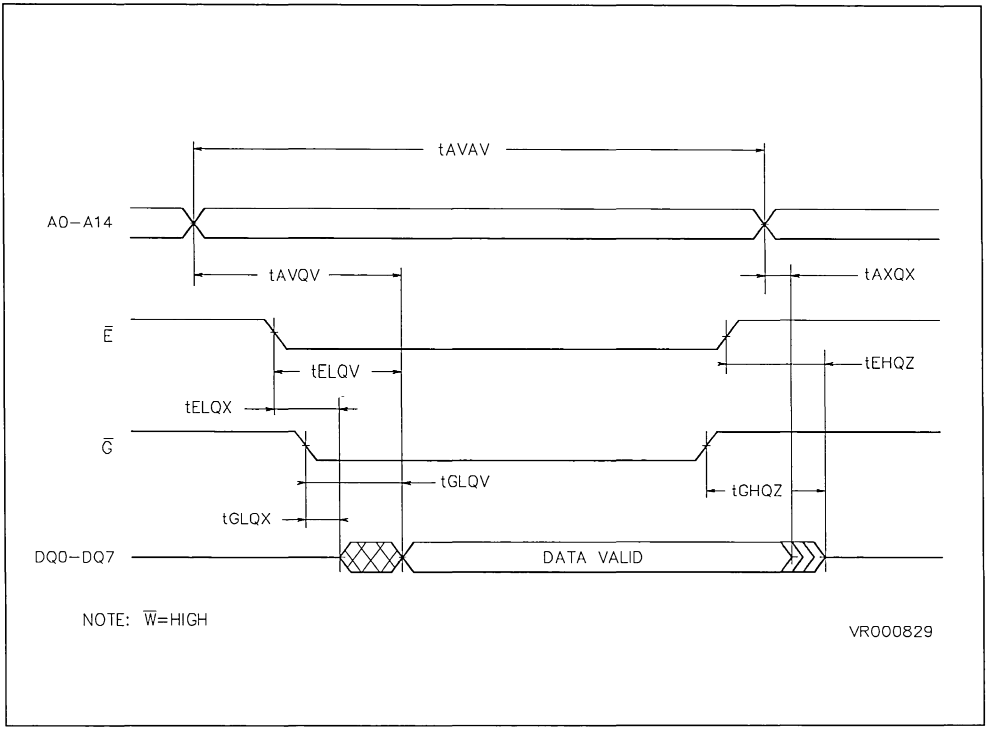
2. Measured with load as shown in Figure B page 4.

Figure 4. Read Timing n° 1 (Address Access)


tAVAV
A0–A14
tAVQV
tAXQX
DQ0–DQ7
DATA VALID
VR000828

Note: $\overline{E}$ = $\overline{G}$ = Low, $\overline{W}$ = High

Figure 5. Read Timing n° 2


tAVAV
A0–A14
tAVQV
tAXQX
E̅
tELQV
tEHQZ
tELQX
G̅
tGLQV
tGHQZ
tGLQX
DQ0–DQ7
DATA VALID
NOTE: W̅=HIGH
VR000829

WRITE MODE

The MK48Z32/32Y is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of Write Enable or Chip Enable. A write is terminated by the earlier rising edge of Write Enable or Chip Enable. The addresses must be held valid throughout the cycle. Chip Enable or Write Enable must return high or for minimum of t_{WHAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward.

Because Output Enable is a Don't Care in the Write Mode and a low on Write Enable will return the outputs to High-Z, Output Enable can be tied low and two-wire RAM control can be implemented. A low on Write Enable will disable the outputs t_{WLQZ} after Write Enable falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le$ V_{CC} max)

Symbol	Parameter	MK48Z32/32Y-70		MK48Z32/32Y-12		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVAV}	Write Cycle Time	70		120		ns	
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-Up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	60		85		ns	
t_{WLWH}	Write Pulse Width	50		65		ns	
t_{WHAX}	Address Hold after End of Write	0		0		ns	
t_{ELEH}	Chip Enable Active to End of Write	55		85		ns	
t_{EHAX}	Address Hold Time from Chip Enable	0		0		ns	
t_{DVWH}	Data Valid to End of Write	30		40		ns	
t_{WHDX}	Data Hold Time	0		0		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	5		5		ns	1
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	25	0	35	ns	1

Notes :

1. Measured with load as shown in Figure B page 4.

Figure 6. Write Control Write Cycle Timing

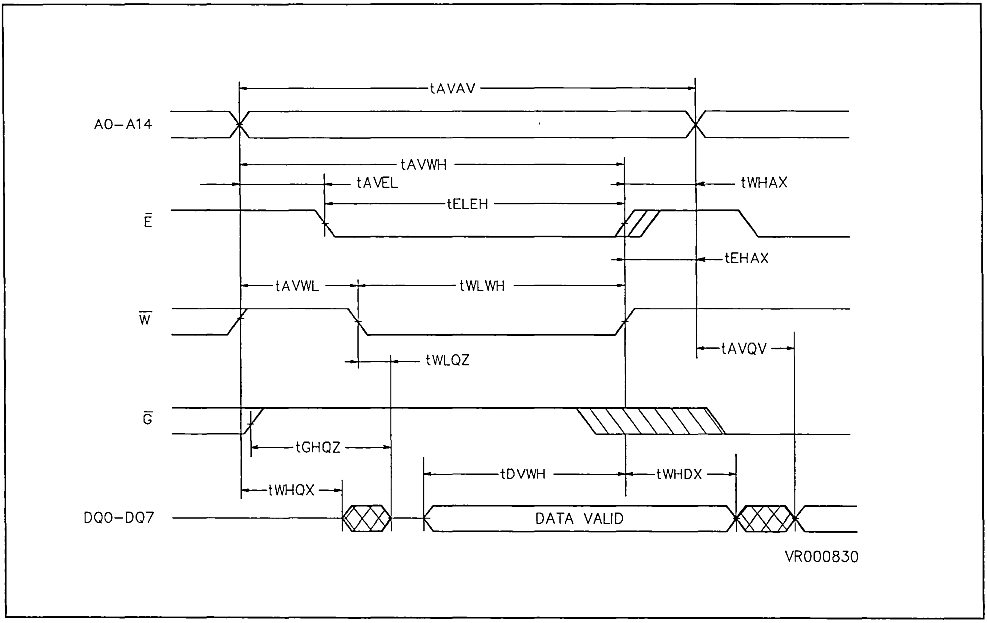
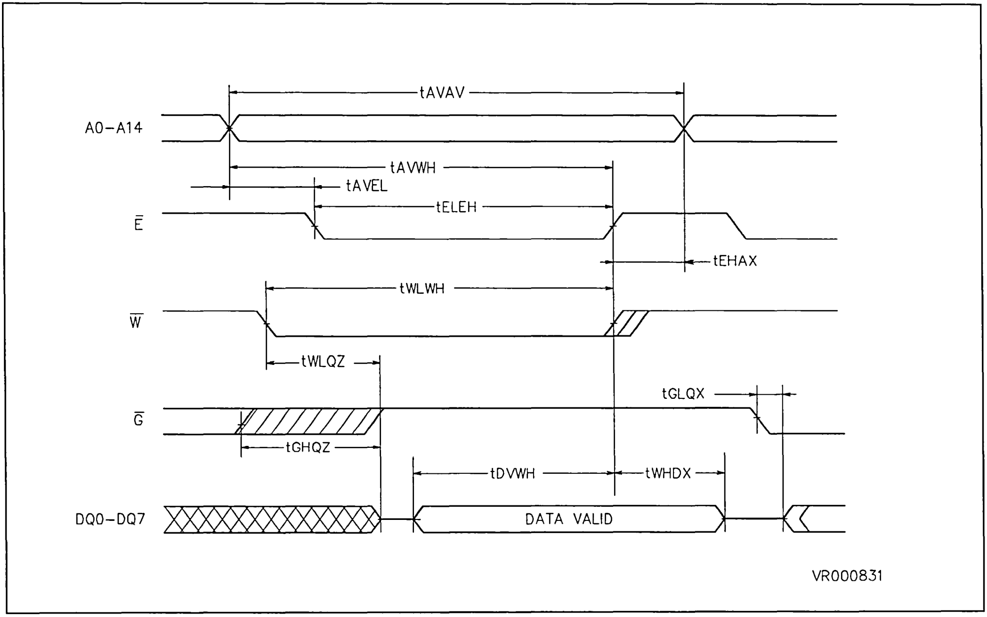

tAVAV
A0-A14
tAVWH
tAVEL
tWHAX
tELEH
E̅
tEHAX
tAVWL
tWLWH
W̅
tAVQV
tWLQZ
G̅
tGHQZ
tDVWH
tWHDX
tWHQX
DQ0-DQ7
DATA VALID
VR000830

Figure 7. Chip Enable Control Write Cycle Timing


tAVAV
A0-A14
tAVWH
tAVEL
tELEH
E̅
tEHAX
tWLWH
W̅
tWLQZ
tGLQX
G̅
tGHQZ
tDVWH
tWHDX
DQ0-DQ7
DATA VALID
VR000831

DATA RETENTION MODE

With V_{CC} applied, the MK48Z32/32Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect , write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window.

A mid-cycle power fail may corrupt data at the currently addressed location, but does not jeopar-dize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, providing the V_{CC} fall time is not less than t_F.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48Z32/32Y is expected to ultimately come to an end for one of two reasons: either because the effects of aging render the cell useless before it can actually be discharged; or because it has been discharged while providing current to an external load.

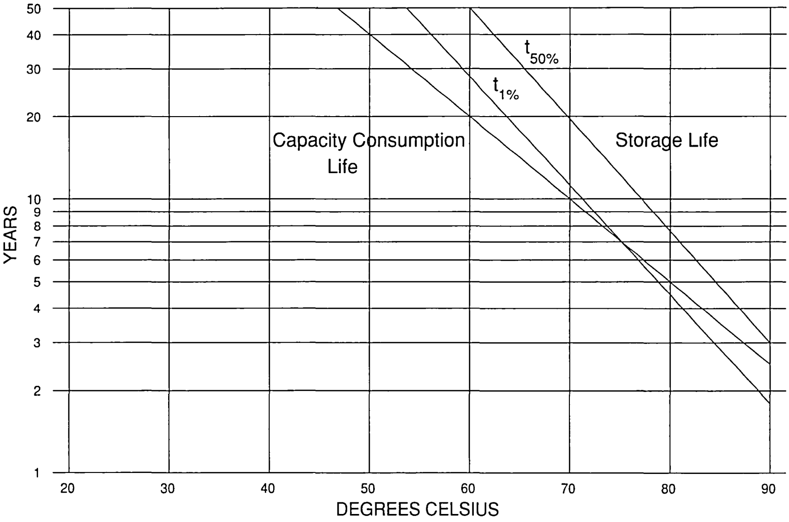
These two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous battery end-of-life mechanisms.

With V_{CC} on, the battery is disconnected from the RAM and Storage Life becomes the determining factor in battery longevity.

With V_{CC} off, the MK48Z32/32Y initiates back-up mode by switching power from the V_{CC} input to the internal battery. In the back-up mode, leakage current drawn by the RAM represents the only load on the battery. The load condition consumes the cell's capacity and is therefore referred to as Capacity Consumption. Capacity Consumption is the primary battery end-of-life mechanism while the MK48Z32/32Y is in the battery back-up mode.

Battery life is defined as beginning on the date of manufacture. Each MK48Z32/32Y is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H - fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9 -tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Figure 8. Predicted Battery Storage Life Versus Temperature



Storage Life

Figure 8 illustrates how temperature affects Storage Life of the MK48Z32/32Y battery.

Two End-of- Life curves related to Storage Life are presented in the Figure 8. They are labeled "Average" ($t_{1\%}$), and "Average" ($t_{50\%}$). These terms define the probability that a given number of failures will accumulate by a particular point in time. If, for example, a battery's expected life at 70˚C is an issue, Figure 8 indicates that an MK48Z32/32Y has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year time. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years and 50% of them within 20 years.

Capacity Consumption Life

Figure 8 also shows how Capacity Consumption varies with temperature.

The MK48Z32/32Y battery cell has a minimum rated capacity of 39 mAh. The RAM, in battery-backed mode, places a nominal load of 445nA at 70 ˚C. At this rate, the MK48Z32/32Y will consume the capacity of the battery cell in 87,600 hours or about 10 years.

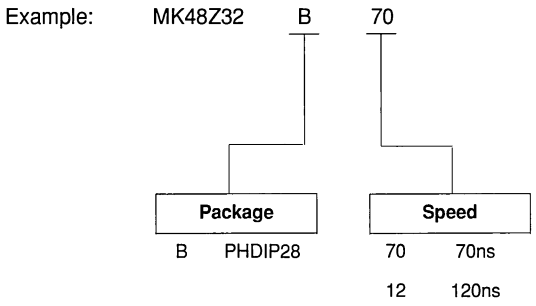
As long as ambient temperature is held reasonably constant, expected Capacity Consumption Life can be estimated directly from the curve in Figure 8. As Vcc Duty Cycle increases, though, so does Capacity Consumption Life. At 70 ˚C and 20% power on Duty Cycle, the Capacity Consumption Life is:

$$10/(1-0.20) = 12.5 \text{ years.}$$

Estimating Back-up System Life

Either Storage or Capacity Consumption can end the System Life of the MK48Z32/32Y. Since these mechanisms are independent, the lower of the two estimated lifetimes defines the Battery Life. At 70°C the System Life of the MK48Z32/32Y would be at least 10 years.

ORDERING INFORMATION


Example:
MK48Z32
B
70
Package
B PHDIP28
Speed
70 70ns
12 120ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

M48Z128
M48Z128Y

CMOS 128K x 8 ZEROPOWER SRAM

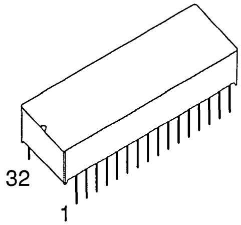
PRELIMINARY DATA

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEAR MINIMUM DATA RETENTION IN THE ABSENCE OF POWER
- COMPATIBLE WITH INDUSTRY STANDARD 128K x 8 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- DUAL WRITE PROTECT VOLTAGES:
  - M48Z128 $4.55V \leq V_{PFD} \leq 4.75V$
  - M48Z128Y $4.30V \leq V_{PFD} \leq 4.50V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED

DESCRIPTION

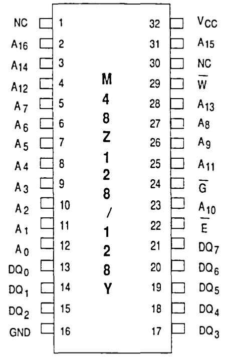
The M48Z128/128Y 128K x 8 ZEROPOWER™ RAM is a non-volatile 1,048,576 bit SRAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery and a full CMOS SRAM in a plastic 32 pin DIP. The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z128/128Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.



PMDIP32 Module

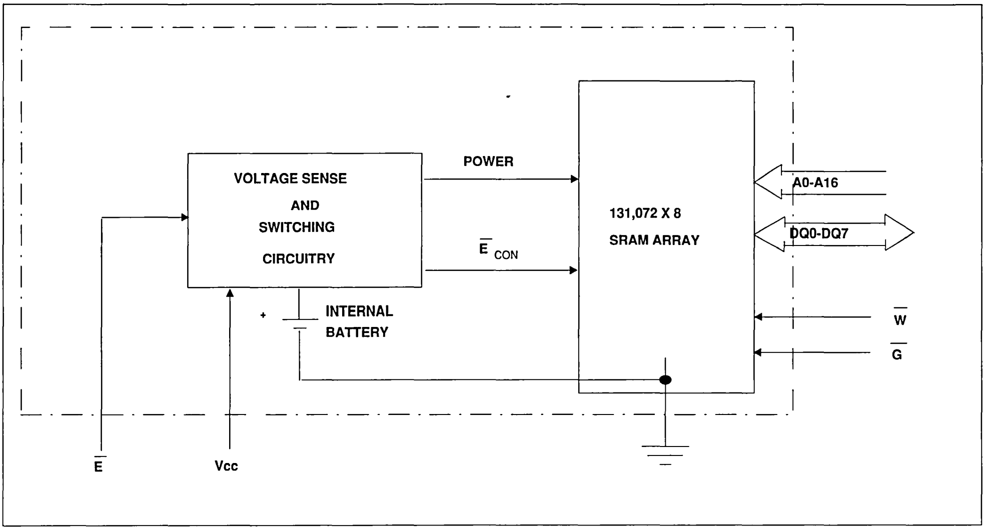
Figure 1. Pin Connections



PIN NAMES

A0-A16	Address Input	Vcc	+5 Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data In/Data Out

Figure 2. Block Diagram


VOLTAGE SENSE
AND
SWITCHING
CIRCUITRY
POWER
$\overline{E}$ CON
131,072 X 8
SRAM ARRAY
A0-A16
DQ0-DQ7
$\overline{W}$
$\overline{G}$
+
INTERNAL
BATTERY
$\overline{E}$
Vcc

TRUTH TABLE

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc(Max) > Vcc(Min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(Min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{CC} Pin Relative to GND	-0.3 to 7.0	V
V_T	Voltage on any Pin excluding V_{CC} Relative to GND ($V_T \leq V_{CC}$+0.3)	-0.3 to 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{STG}	Ambient Storage Temperature	-40 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +70	°C
T_{SLD}	Soldering Temperature for 10 Seconds	260	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	Note
Vcc	Supply Voltage (M48Z128)	4.75	5.5	V	1
Vcc	Supply Voltage (M48Z128Y)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; V_{CC} min $\leq V_{CC} \leq V_{CC}$ max)

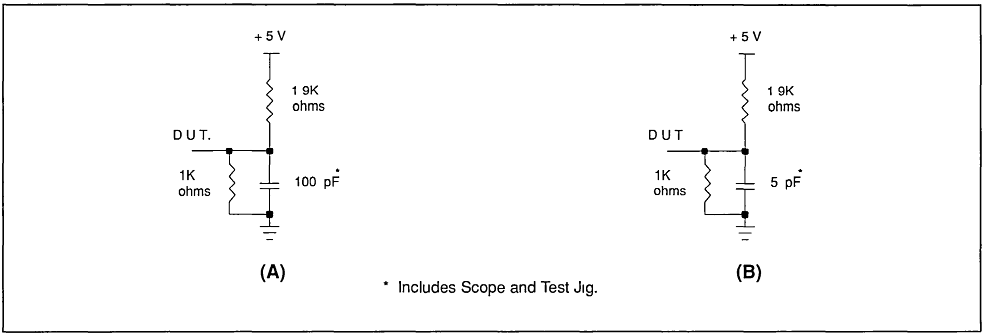
Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{CC1}	Average Vcc Power Supply Current ($\overline{E}= V_{IL}$)		75	105	mA	2,5
I_{CC2}	TTL Standby Current ($\overline{E}= V_{IH}$)		4	7	mA	5
I_{CC3}	CMOS Standby Current ($\overline{E} \geq$ Vcc -0.2V)		2.5	4	mA	3,5
I_{IL}	Input Leakage Current (Any Input)	-1		+1	µA	4
I_{OL}	Output Leakage Current	-1		+1	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4			V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)			0.4	V	1

Notes: 1. All voltages referenced to GND.
2. I_{CC1} measured with outputs open.
3 Measured with 0V≤ $V_I \leq$ 0 2V or $V_I \geq V_{CC}$ - 0.2V
4. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected
5. Typical values indicate operation at T_A=25°C and V_{CC}=5V.

AC TEST CONDITION

Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS


+5 V
1 9K ohms
D U T.
1K ohms
100 pF*
(A)
+5 V
1 9K ohms
D U T
1K ohms
5 pF*
(B)

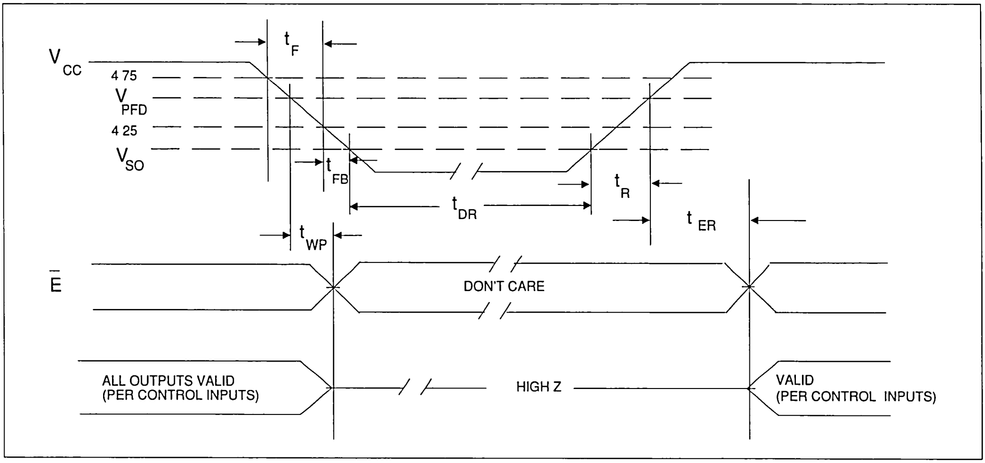
* Includes Scope and Test Jig.

CAPACITANCE (T_A = 25°C, f=1MHz)

Symbol	Parameter	Max	Unit	Note
C_I	Capacitance on All Pins (except DQ)	10.0	pF	1,2
C_{DQ}	Capacitance on DQ Pins	10.0	pF	1,2,3

Notes: 1. Effective capacitance measured with power supply at 5 0 V.
2. These parameters are sampled and not 100% tested
3. Measured with outputs deselected.

Figure 3. Power Down/Up Timing


V_{CC}
4 75
V_{PFD}
4 25
V_{SO}
t_F
t_{FB}
t_{DR}
t_R
t_{ER}
t_{WP}
$\overline{E}$
DON'T CARE
ALL OUTPUTS VALID
(PER CONTROL INPUTS)
HIGH Z
VALID
(PER CONTROL INPUTS)

AC ELECTRICAL CHARACTERISTICS (Power down/up Timing)

(0˚C ≤ T_A ≤ +70˚C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_F	4.75 to 4.25V V_{CC} Fall Time	300			µs	
t_{FB}	4.25 to V_{SO} V_{CC} Fall Time	10			µs	
t_{WP}	Write Protect Time from $V_{CC}=V_{PFD}$	40	100	150	µs	1
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	0			µs	
t_{ER}	$\overline{E}$ Recovery Time	40	80	120	ms	1

DC ELECTRICAL CHARACTERISTICS (Power down/up Trip Points)

(0˚C ≤ T_A ≤ +70˚C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{PFD}	Power- Fail Deselect Voltage (M48Z128)	4.55	4.62	4.75	V	1,2
V_{PFD}	Power- Fail Deselect Voltage (M48Z128Y)	4.30	4.37	4.50	V	1,2
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1,2
t_{DR}	Data Retention Time in Absence of V_{CC}	10			YEARS	3

Notes: 1. Typical values indicate operation at T_A=25C and V_{CC}=5V.
2. All voltages referenced to GND.
3. t_{DR} is the accumulated time in absence of power from the time V_{CC} is first applied. t_{DR} is specified @ 25°C.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z128/128Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data. The internal coin cell will maintain data in the M48Z128/128Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

READ MODE

The M48Z128/128Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 Address Inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le V_{CC}$ max)

Symbol	Parameter	48Z128/128Y-85		48Z128/128Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Read Cycle Time	85		120		ns	
t_{AVQV}	Address Access Time		85		120	ns	1
t_{ELQV}	Chip Enable Access Time		85		120	ns	1
t_{GLQV}	Output Enable Access Time		45		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	5		5		ns	2
t_{GLQX}	Output Enable to Q Low-Z	0		0		ns	2
t_{EHQZ}	Chip Enable High to Q High-Z	0	35	0	45	ns	2
t_{GHQZ}	Output Enable High to High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

Notes: 1. Measured with load as shown in Figure A page 4.
2 Measured with load as shown in Figure B page 4

Figure 4. Read Timing n° 1 (Address Access)

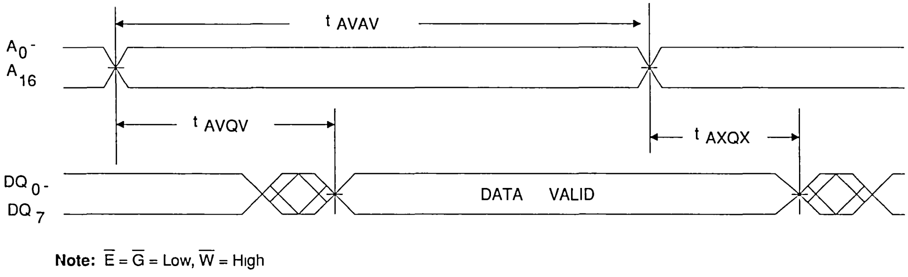
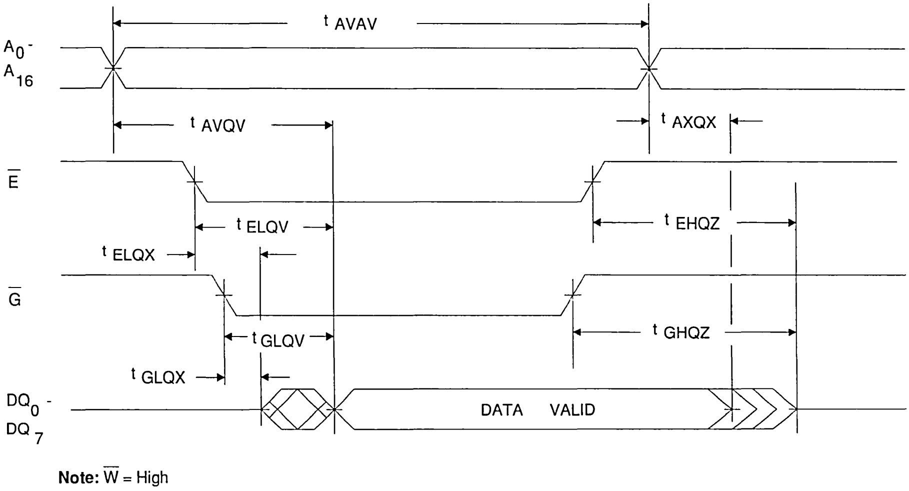

t AVAV
A0 -
A16
t AVQV
t AXQX
DQ 0 -
DQ 7
DATA VALID
Note: E = G = Low, W = High

Figure 5. Read Timing n° 2


t AVAV
A0 -
A16
t AVQV
t AXQX
E
t ELQV
t EHQZ
t ELQX
G
t GLQV
t GHQZ
t GLQX
DQ0 -
DQ 7
DATA VALID
Note: W = High

WRITE MODE

The M48Z128/128Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \leq T_A \leq +70°C$; V_{CC} min $\leq V_{CC} \leq V_{CC}$ max)

Symbol	Parameter	48Z128/128Y-85		48Z128/128Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Write Cycle Time	85		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to End of Write	75		100		ns	
t_{WLWH}	Write Pulse Width	65		85		ns	
t_{WHAX}	Address Hold after End of Write	5		5		ns	
t_{EHAX}	Address Hold Time from Chip Enable	15		15		ns	
t_{ELEH}	Chip Enable Active to End of Write	75		100		ns	
t_{DVWH}	Data Valid to End of Write	35		45		ns	
t_{WHDX}	Data Hold Time from Write Enable	0		0		ns	
t_{EHDX}	Data Hold Time from Chip Enable	10		10		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	0		0		ns	1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	30	0	40	ns	1,2

Notes: 1. Measured with load as shown in Figure B page 4

2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low or after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 6. Write Control Write Cycle Timing

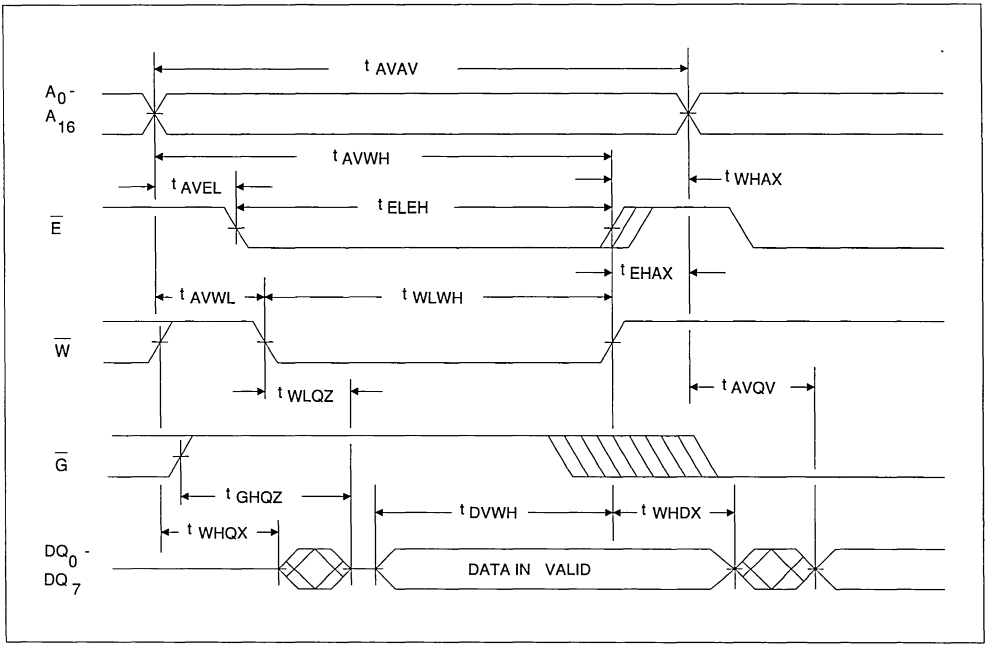
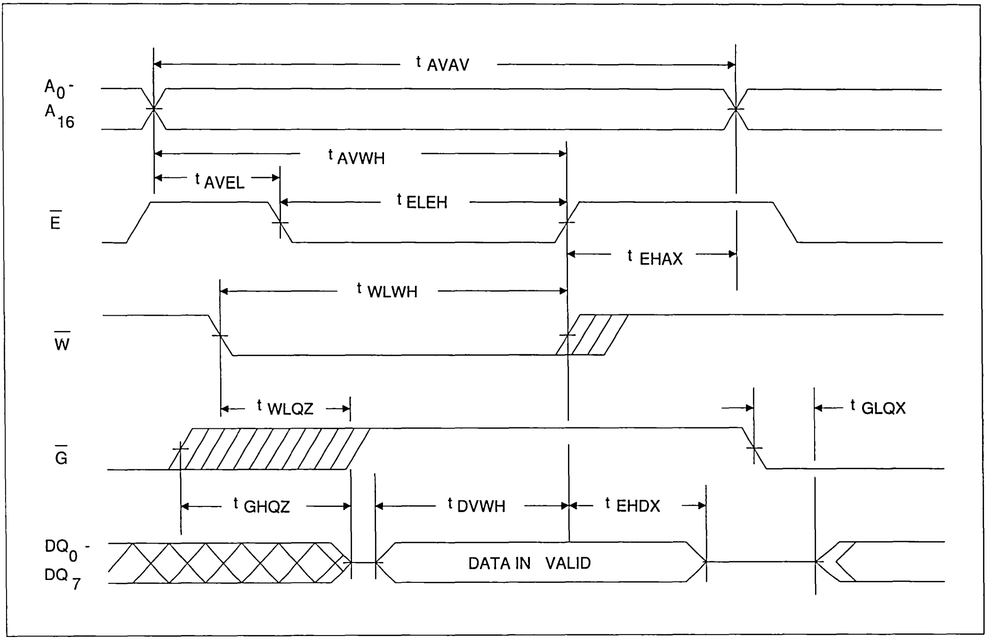
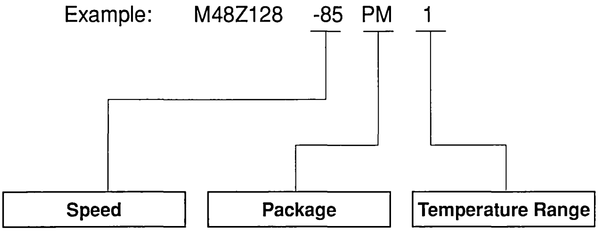

t AVAV
A0 - A16
t AVWH
t AVEL
t WHAX
t ELEH
E
t EHAX
t AVWL
t WLWH
W
t WLQZ
t AVQV
G
t GHQZ
t DVWH
t WHDX
t WHQX
DQ0 - DQ7
DATA IN VALID

Figure 7. Chip Enable Control Write Cycle Timing


t AVAV
A0 - A16
t AVWH
t AVEL
t ELEH
E
t EHAX
t WLWH
W
t WLQZ
t GLQX
G
t GHQZ
t DVWH
t EHDX
DQ0 - DQ7
DATA IN VALID

ORDERING INFORMATION


Example: M48Z128 -85 PM 1
Speed
Package
Temperature Range

Speed		Package		Temperature Range	
-85	85 ns	PM	PMDIP32	1	0 to 70 °C
-120	120 ns				

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

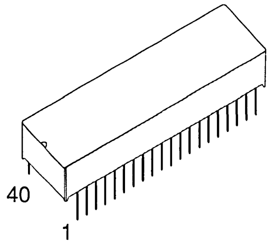
SGS-THOMSON
MICROELECTRONICS

M46Z128
M46Z128Y

CMOS 128K x 16 ZEROPOWER SRAM

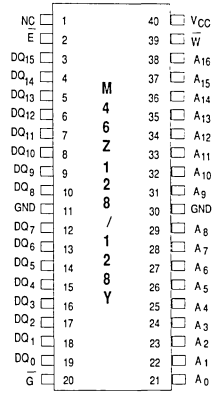
PRELIMINARY DATA

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEAR MINIMUM DATA RETENTION IN THE ABSENCE OF POWER
- COMPATIBLE WITH INDUSTRY STANDARD 128K x 16 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- DUAL WRITE PROTECT VOLTAGES:
  - M46Z128 4.55V $\leq V_{PFD} \leq$ 4.75V
  - M46Z128Y 4.30V $\leq V_{PFD} \leq$ 4.50V
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED.



PMDIP40 Module

Figure 1. Pin Connections


NC 1
$\overline{E}$ 2
DQ15 3
DQ14 4
DQ13 5
DQ12 6
DQ11 7
DQ10 8
DQ9 9
DQ8 10
GND 11
DQ7 12
DQ6 13
DQ5 14
DQ4 15
DQ3 16
DQ2 17
DQ1 18
DQ0 19
$\overline{G}$ 20
40 VCC
39 $\overline{W}$
38 A16
37 A15
36 A14
35 A13
34 A12
33 A11
32 A10
31 A9
30 GND
29 A8
28 A7
27 A6
26 A5
25 A4
24 A3
23 A2
22 A1
21 A0
M46Z128/128Y

DESCRIPTION

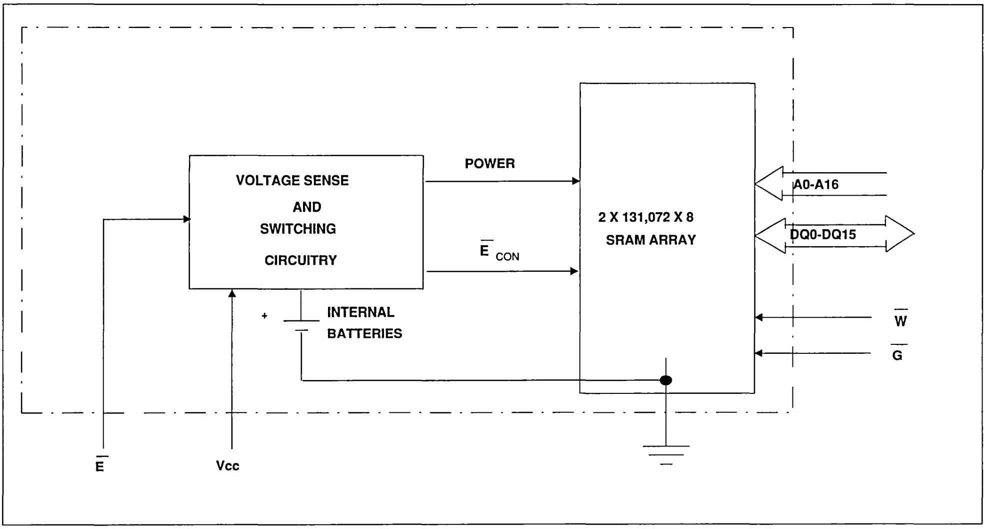
The M46Z128/128Y 128K x 16 ZEROPOWER™ RAM is a non-volatile 2,097,152 bit SRAM organized as 131,072 words by 16 bits. The device combines internal lithium batteries and full CMOS SRAMs in a plastic 40 pin DIP. The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M46Z128/128Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

PIN NAMES

A0-A16	Address Input	Vcc	+5 Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ15	Data In/Data Out

Figure 2. Block Diagram


VOLTAGE SENSE
AND
SWITCHING
CIRCUITRY
POWER
$\overline{E}_{CON}$
INTERNAL
BATTERIES
+
2 X 131,072 X 8
SRAM ARRAY
A0-A16
DQ0-DQ15
$\overline{W}$
$\overline{G}$
$\overline{E}$
Vcc

TRUTH TABLE

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc(Max)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
> Vcc(Min)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(Min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{CC} Pin Relative to GND	-0.3 to 7.0	V
V_T	Voltage on any Pin excluding V_{CC} Relative to GND ($V_T \leq V_{CC}+0.3$)	-0.3 to 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{STG}	Ambient Storage Temperature	-40 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +70	°C
T_{SLD}	Soldering Temperature for 10 Seconds	260	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability

CAUTION: *Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	Note
Vcc	Supply Voltage (M46Z128)	4.75	5.5	V	1
Vcc	Supply Voltage (M46Z128Y)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; Vcc min ≤ Vcc ≤ Vcc max)

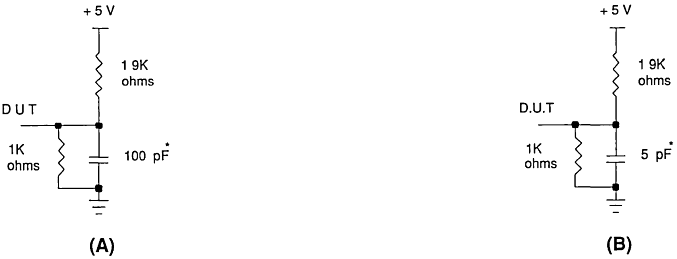
Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{cc1}	Average Vcc Power Supply Current ($\overline{E}= V_{IL}$)		95	200	mA	2,5
I_{cc2}	TTL Standby Current ($\overline{E}= V_{IH}$)		5	11	mA	5
I_{cc3}	CMOS Standby Current ($\overline{E} \geq$ Vcc -0.2V)		2.5	5	mA	3,5
I_{IL}	Input Leakage Current (Any Input)	-2		+2	µA	4
I_{OL}	Output Leakage Current	-1		+1	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT}=-1.0 mA)	2.4			V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)			0.4	V	1

Notes: 1. All voltages referenced to GND
2. I_{CC1} measured with outputs open
3 Measured with $0V \leq V_I \leq 0.2V$ or $V_I \geq V_{CC} - 0.2V$.
4 Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected
5. Typical values indicate operation at T_A=25°C and V_{CC}=5V.

AC TEST CONDITION

Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS



+5 V
1 9K ohms
DUT
1K ohms
100 pF*
(A)
+5 V
1 9K ohms
D.U.T
1K ohms
5 pF*
(B)

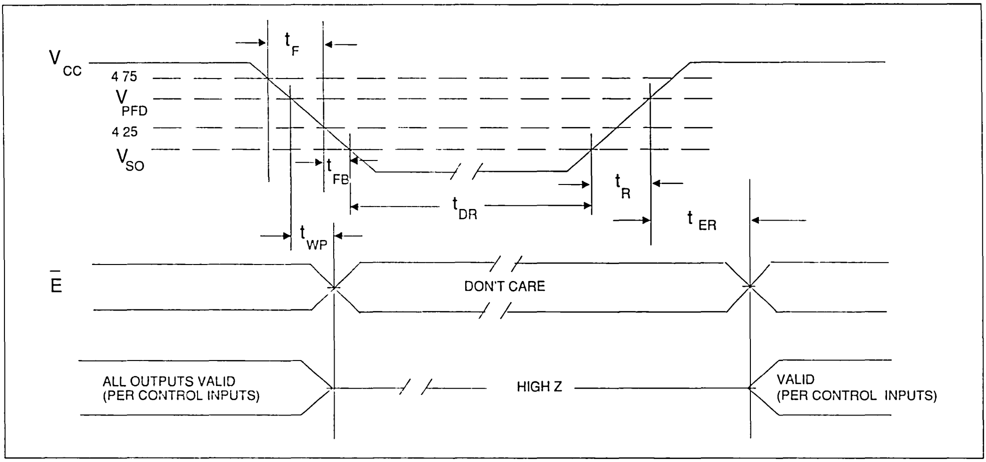
* Includes Scope and Test Jig.

CAPACITANCE (T_A = 25°C, F=1MHz)

Symbol	Parameter	Max	Unit	Note
C_I	Capacitance on All Pins (except DQ)	20.0	pF	1,2
C_{DQ}	Capacitance on DQ Pins	10.0	pF	1,2,3

Notes: 1. Effective capacitance measured with power supply at 5.0 V.
2. These parameters are sampled and not 100% tested.
3. Measured with outputs deselected.

Figure 3. Power Down/Up Timing


VCC
4 75
VPFD
4 25
VSO
tF
tFB
tDR
tR
tER
tWP
E
DON'T CARE
ALL OUTPUTS VALID (PER CONTROL INPUTS)
HIGH Z
VALID (PER CONTROL INPUTS)

AC ELECTRICAL CHARACTERISTICS (Power down/up Timing)

($0^\circ C \le T_A \le +70^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_F	4.75 to 4.25V V_{CC} Fall Time	300			µs	
t_{FB}	4.25 to V_{SO} V_{CC} Fall Time	10			µs	
t_{WP}	Write Protect Time from $V_{CC}=V_{PFD}$	40	100	150	µs	1
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	0			µs	
t_{ER}	$\overline{E}$ Recovery Time	40	80	120	ms	1

DC ELECTRICAL CHARACTERISTICS (Power down/up Trip Points)

($0^\circ C \le T_A \le +70^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{PFD}	Power- Fail Deselect Voltage (M46Z128)	4.55	4.62	4.75	V	1,2
V_{PFD}	Power- Fail Deselect Voltage (M46Z128Y)	4.30	4.37	4.50	V	1,2
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1,2
t_{DR}	Data Retention Time in Absence of V_{CC}	10			YEARS	3

Notes: 1. Typical values indicate operation at T_A=25C and V_{CC}=5V.
2. All voltages referenced to GND.
3. t_{DR} is the accumulated time in absence of power from the time V_{CC} is first applied. t_{DR} is specified @ 25°C

DATA RETENTION MODE

With valid V_{CC} applied, the M46Z128/128Y operates as a conventional static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data. The internal coin cells will maintain data in the M46Z128/128Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

READ MODE

The M46Z128/128Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from sixteen of 2,097,152 locations in the static storage array. Thus, the unique address specified by the 17 Address Inputs defines which one of the 131,072 words of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

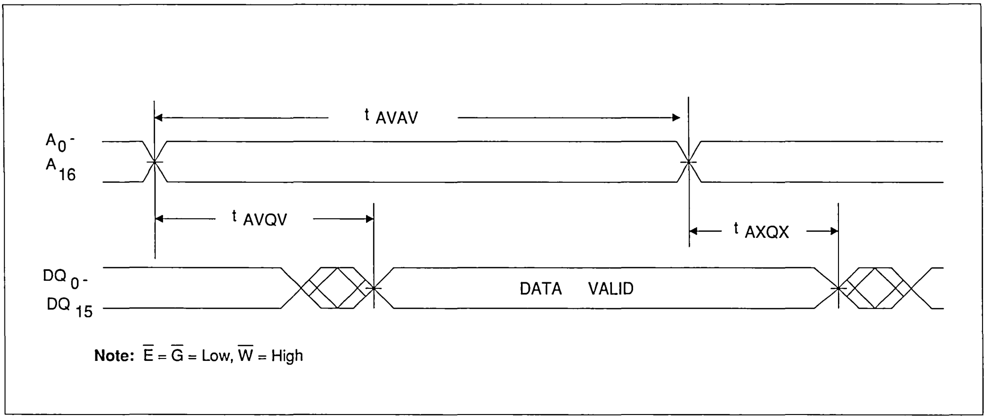
AC ELECTRICAL CHARACTERISTICS (Read Cycle)

(0°C ≤ T_A ≤ + 70°C, Vcc min ≤ Vcc ≤ Vcc max)

Symbol	Parameter	46Z128/128Y-85		46Z128/128Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Read Cycle Time	85		120		ns	
t_{AVQV}	Address Access Time		85		120	ns	1
t_{ELQV}	Chip Enable Access Time		85		120	ns	1
t_{GLQV}	Output Enable Access Time		45		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	5		5		ns	2
t_{GLQX}	Output Enable to Q Low-Z	0		0		ns	2
t_{EHQZ}	Chip Enable High to Q High-Z	0	35	0	45	ns	2
t_{GHQZ}	Output Enable High to High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

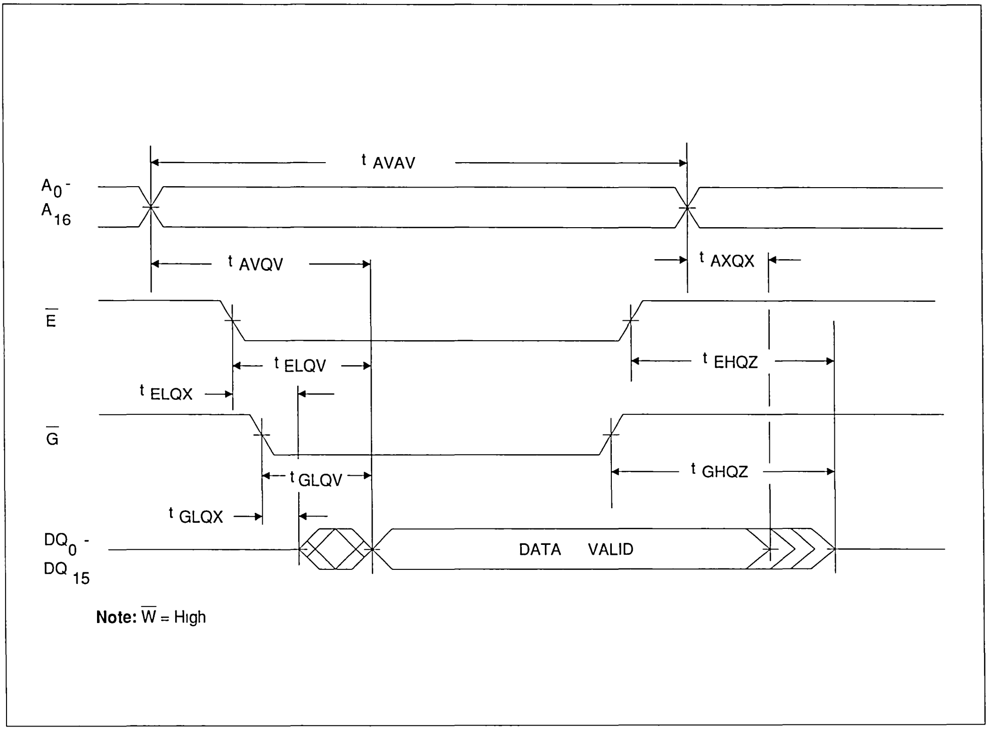
Notes: 1 Measured with load as shown in Figure A page 4.
2. Measured with load as shown in Figure B page 4.

Figure 4. Read Timing n° 1 (Address Access)


t AVAV
A0 -
A16
t AVQV
t AXQX
DQ 0 -
DQ 15
DATA VALID

Note: $\overline{E}$ = $\overline{G}$ = Low, $\overline{W}$ = High

Figure 5. Read Timing n° 2


t AVAV
A0 -
A16
t AVQV
t AXQX
E
t ELQV
t EHQZ
t ELQX
G
t GLQV
t GHQZ
t GLQX
DQ0 -
DQ 15
DATA VALID

Note: $\overline{W}$ = High

WRITE MODE

The M46Z128/128Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \le T_A \le +70°C$, V_{CC} min $\le V_{CC} \le V_{CC}$ max)

Symbol	Parameter	46Z128/128Y-85		46Z128/128Y-120		Unit	Note
		Min.	Max.	Min.	Max.		
t_{AVAV}	Write Cycle Time	85		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to End of Write	75		100		ns	
t_{WLWH}	Write Pulse Width	65		85		ns	
t_{WHAX}	Address Hold after End of Write	5		5		ns	
t_{EHAX}	Address Hold Time from Chip Enable	15		15		ns	
t_{ELEH}	Chip Enable Active to End of Write	75		100		ns	
t_{DVWH}	Data Valid to End of Write	35		45		ns	
t_{WHDX}	Data Hold Time from Write Enable	0		0		ns	
t_{EHDX}	Data Hold Time from Chip Enable	10		10		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	0		0		ns	1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	30	0	40	ns	1,2

Notes: 1. Measured with load as shown in Figure B page 4.
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low or after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 6. Write Control Write Cycle Timing

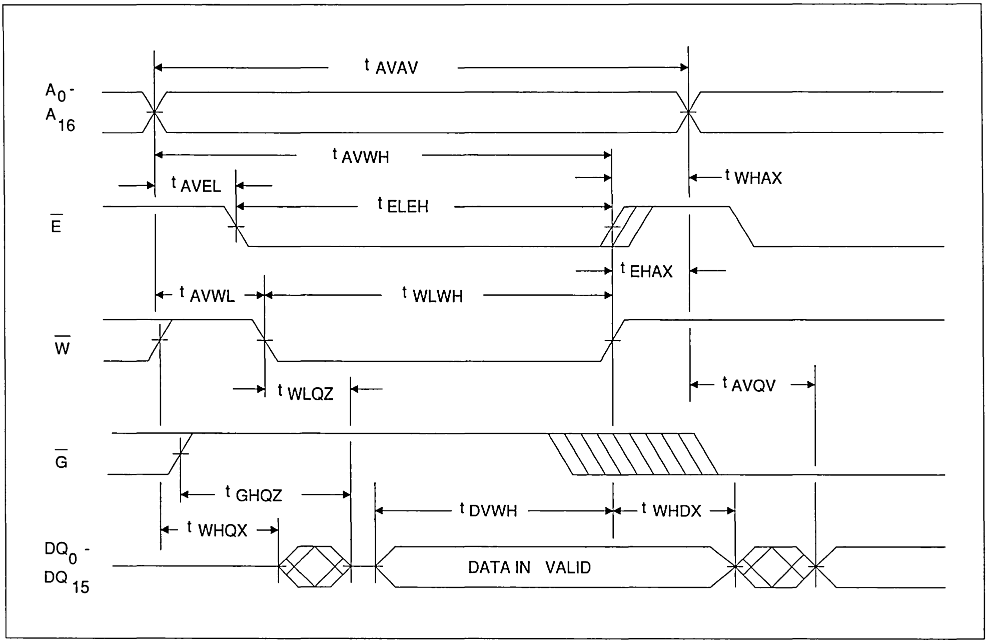
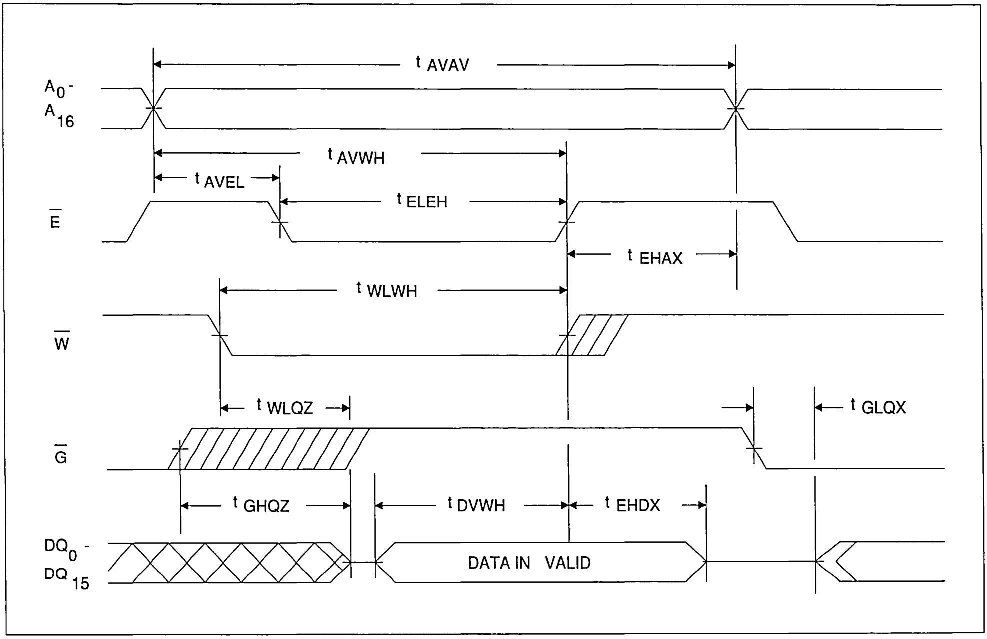

t AVAV
A0 - A16
t AVWH
t AVEL
t WHAX
t ELEH
E
t EHAX
t AVWL
t WLWH
W
t WLQZ
t AVQV
G
t GHQZ
t DVWH
t WHDX
t WHQX
DQ0 - DQ15
DATA IN VALID

Figure 7. Chip Enable Control Write Cycle Timing


t AVAV
A0 - A16
t AVWH
t AVEL
t ELEH
E
t EHAX
t WLWH
W
t WLQZ
t GLQX
G
t GHQZ
t DVWH
t EHDX
DQ0 - DQ15
DATA IN VALID

ORDERING INFORMATION

Example: M46Z128 -85 PM 1

Speed		**Package**		**Temperature Range**	
-85	85 ns	PM	PMDIP40	1	0 to 70 °C
-120	120 ns				

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

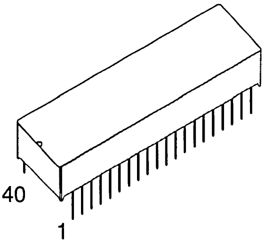
SGS-THOMSON
MICROELECTRONICS

M46Z256
M46Z256Y

CMOS 256K x 16 ZEROPOWER SRAM

PRELIMINARY DATA

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 5 YEAR MINIMUM DATA RETENTION IN THE ABSENCE OF POWER
- COMPATIBLE WITH INDUSTRY STANDARD 256K x 16 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- DUAL WRITE PROTECT VOLTAGES:
  - M46Z256 $4.55V \leq V_{PFD} \leq 4.75V$
  - M46Z256Y $4.30V \leq V_{PFD} \leq 4.50V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED.



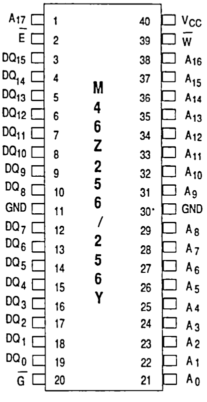
PMDIP40 Module

DESCRIPTION

The M46Z256/256Y 256K x 16 ZEROPOWER™ RAM is a non-volatile 4,194,304 bit SRAM organized as 262,144 words by 16 bits. The device combines internal lithium batteries and full CMOS SRAMs in a plastic 40 pin DIP. The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M46Z256/256Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

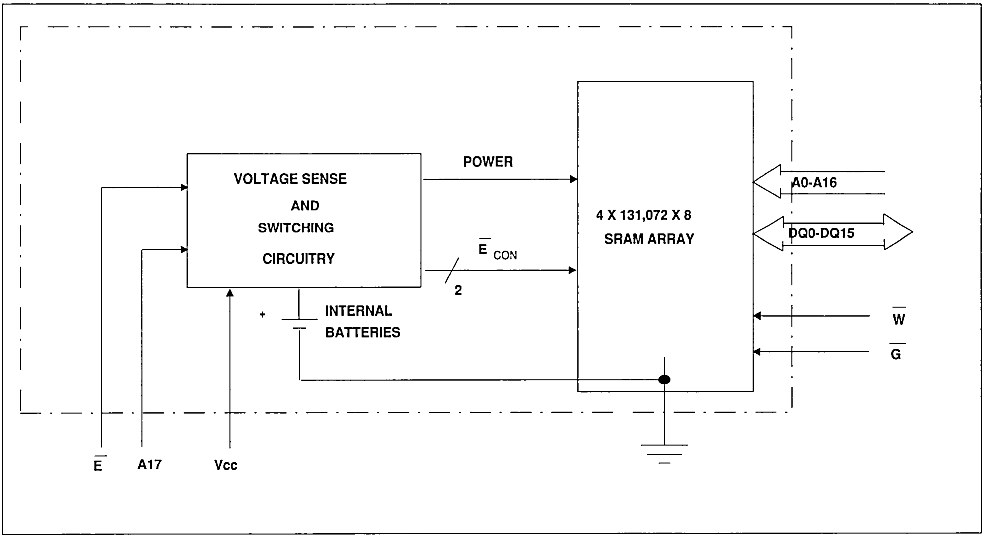
Figure 1. Pin Connections


A17 1
E 2
DQ15 3
DQ14 4
DQ13 5
DQ12 6
DQ11 7
DQ10 8
DQ9 9
DQ8 10
GND 11
DQ7 12
DQ6 13
DQ5 14
DQ4 15
DQ3 16
DQ2 17
DQ1 18
DQ0 19
G 20
40 VCC
39 W
38 A16
37 A15
36 A14
35 A13
34 A12
33 A11
32 A10
31 A9
30 GND
29 A8
28 A7
27 A6
26 A5
25 A4
24 A3
23 A2
22 A1
21 A0
M46Z256/256Y

PIN NAMES

A0-A17	Address Input	Vcc	+5 Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ15	Data In/Data Out

Figure 2. Block Diagram


VOLTAGE SENSE
AND
SWITCHING
CIRCUITRY
POWER
$\overline{E}$ CON
2
+
INTERNAL
BATTERIES
4 X 131,072 X 8
SRAM ARRAY
A0-A16
DQ0-DQ15
$\overline{W}$
$\overline{G}$
$\overline{E}$
A17
Vcc

TRUTH TABLE

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc(Max) > Vcc(Min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(Min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{CC} Pin Relative to GND	-0.3 to 7.0	V
V_T	Voltage on any Pin excluding V_{CC} Relative to GND ($V_T \leq V_{CC}+0.3$)	-0.3 to 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{STG}	Ambient Storage Temperature	-40 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +70	°C
T_{SLD}	Soldering Temperature for 10 Seconds	260	°C

* Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	Note
Vcc	Supply Voltage (M46Z256)	4.75	5.5	V	1
Vcc	Supply Voltage (M46Z256Y)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic “1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic “0" Voltage All Inputs	-0.3	0.8	V	1

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; Vcc min ≤ Vcc ≤ Vcc max)

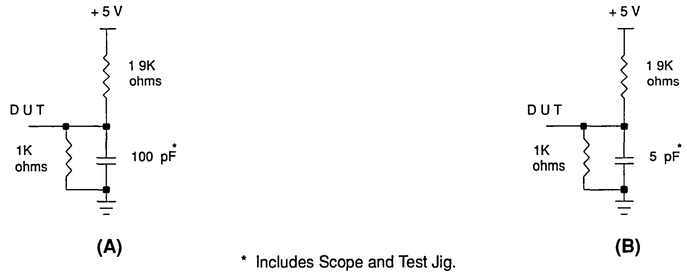
Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{cc1}	Average Vcc Power Supply Current ($\overline{E}= V_{IL}$)		95	200	mA	2,5
I_{cc2}	TTL Standby Current ($\overline{E}= V_{IH}$)		7	18	mA	5
I_{cc3}	CMOS Standby Current ($\overline{E} \geq$ Vcc -0.2V)		2.5	5	mA	3,5
I_{IL}	Input Leakage Current (Any Input)	-4		+4	µA	4
I_{OL}	Output Leakage Current	-2		+2	µA	4
V_{OH}	Output Logic “1" Voltage (I_{OUT} =-1.0 mA)	2.4			V	1
V_{OL}	Output Logic “0" Voltage (I_{OUT} = +2.1 mA)			0.4	V	1

Notes: 1. All voltages referenced to GND.
2 I_{CC1} measured with outputs open.
3 Measured with $0V \leq V_I \leq 0.2V$ or $V_I \geq V_{CC} - 0.2V$.
4. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected
5. Typical values indicate operation at T_A=25°C and V_{CC}=5V.

AC TEST CONDITION

Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS


+5 V
1 9K ohms
DUT
1K ohms
100 pF*
(A)
+5 V
1 9K ohms
DUT
1K ohms
5 pF*
(B)

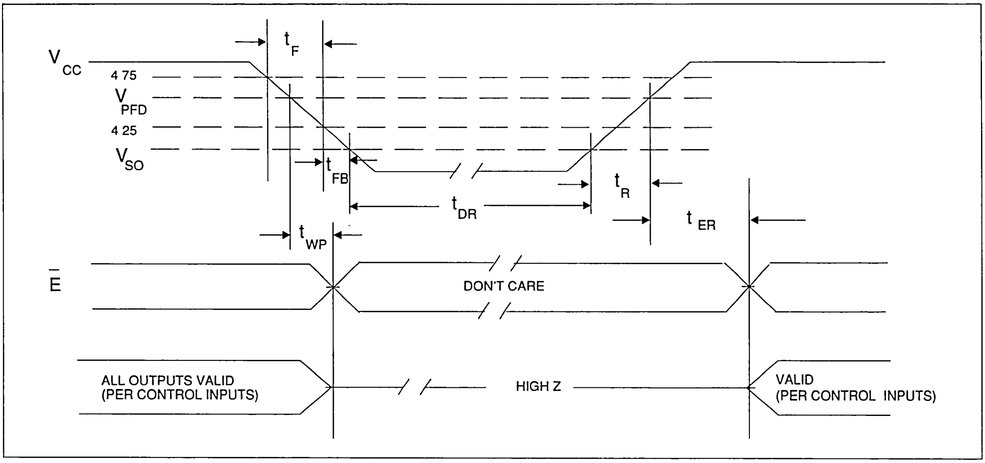
* Includes Scope and Test Jig.

CAPACITANCE (T_A = 25°C, F=1MHz)

Symbol	Parameter	Max	Unit	Note
C_I	Capacitance on All Pins (except DQ)	40.0	pF	1,2
C_{DQ}	Capacitance on DQ Pins	20.0	pF	1,2,3

Note: 1. Effective capacitance measured with power supply at 5.0 V.
2. These parameters are sampled and not 100% tested.
3. Measured with outputs deselected.

Figure 3. Power Down/Up Timing



V_{CC}
4 75
V_{PFD}
4 25
V_{SO}
t_F
t_{FB}
t_{DR}
t_R
t_{ER}
t_{WP}
$\overline{E}$
DON'T CARE
ALL OUTPUTS VALID (PER CONTROL INPUTS)
HIGH Z
VALID (PER CONTROL INPUTS)

AC ELECTRICAL CHARACTERISTICS (Power down/up Timing)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_F	4.75 to 4.25V V_{CC} Fall Time	300			µs	
t_{FB}	4.25 to V_{SO} V_{CC} Fall Time	10			µs	
t_{WP}	Write Protect Time from $V_{CC}=V_{PFD}$	40	100	150	µs	1
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	0			µs	
t_{ER}	$\overline{E}$ Recovery Time	40	80	120	ms	1

DC ELECTRICAL CHARACTERISTICS (Power down/up Trip Points)

($0°C \le T_A \le +70°C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{PFD}	Power- Fail Deselect Voltage (M46Z256)	4.55	4.62	4.75	V	1,2
V_{PFD}	Power- Fail Deselect Voltage (M46Z256Y)	4.30	4.37	4.50	V	1,2
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1,2
t_{DR}	Data Retention Time in Absence of V_{CC}	5			YEARS	3

Notes: 1. Typical values indicate operation at T_A=25C and V_{CC}=5V
2. All voltages referenced to GND.
3. t_{DR} is the accumulated time in absence of power from the time V_{CC} is first applied t_{DR} is specified @ 25°C.

DATA RETENTION MODE

With valid V_{CC} applied, the M46Z256/256Y operates as a conventional static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data. The internal coin cells will maintain data in the M46Z256/256Y after the initial application of V_{CC} for an accumulated period of at least 5 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

READ MODE

The M46Z256/256Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from sixteen of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 18 Address Inputs defines which one of the 262,144 words of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0^{\circ}C \le T_A \le +70^{\circ}C$, Vcc min $\le$ Vcc $\le$ Vcc max)

Symbol	Parameter	46Z256/256Y-85		46Z256/256Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Read Cycle Time	85		120		ns	
t_{AVQV}	Address Access Time		85		120	ns	1
t_{ELQV}	Chip Enable Access Time		85		120	ns	1
t_{GLQV}	Output Enable Access Time		45		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	5		5		ns	2
t_{GLQX}	Output Enable to Q Low-Z	0		0		ns	2
t_{EHQZ}	Chip Enable High to Q High-Z	0	35	0	45	ns	2
t_{GHQZ}	Output Enable High to High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

Notes: 1. Measured with load as shown in Figure A page 4.
2. Measured with load as shown in Figure B page 4.

Figure 4. Read Timing n° 1 (Address Access)

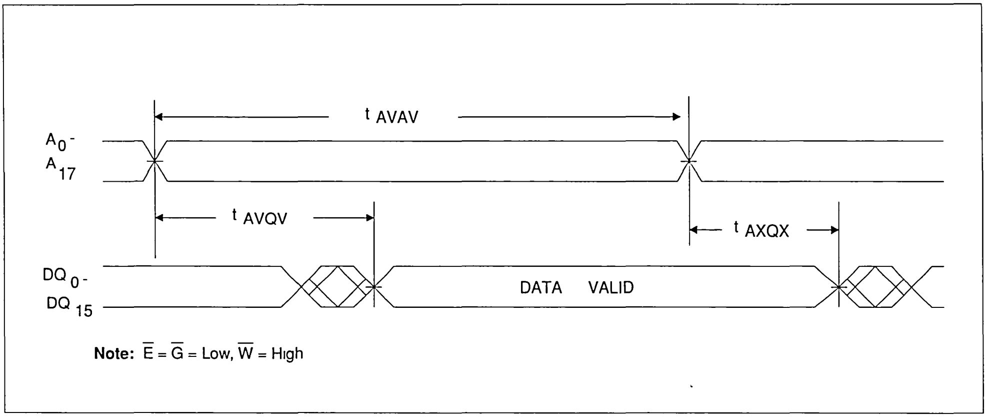
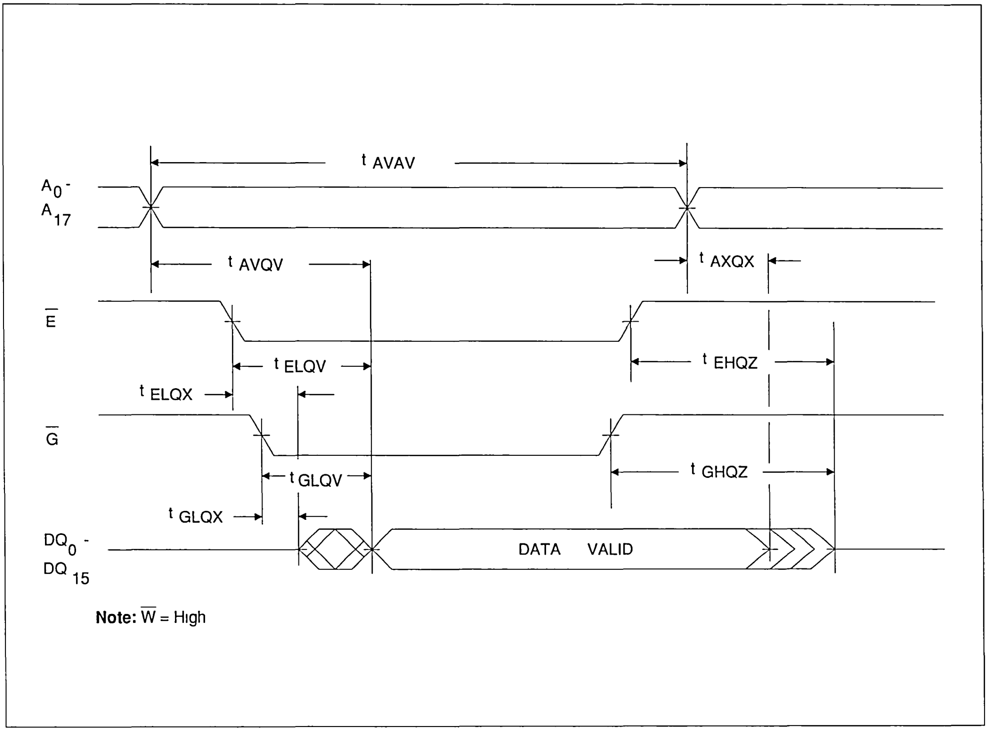

tAVAV
A0 - A17
tAVQV
tAXQX
DQ0 - DQ15
DATA VALID
Note: E̅ = G̅ = Low, W̅ = High

Figure 5. Read Timing n° 2


tAVAV
A0 - A17
tAVQV
tAXQX
E̅
tELQV
tEHQZ
tELQX
G̅
tGLQV
tGHQZ
tGLQX
DQ0 - DQ15
DATA VALID
Note: W̅ = High

WRITE MODE

The M46Z256/256Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0^{\circ}C \leq T_A \leq +70^{\circ}C$, V_{CC} min $\leq V_{CC} \leq V_{CC}$ max)

Symbol	Parameter	46Z256/256Y-85		46Z256/256Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Write Cycle Time	85		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to End of Write	75		100		ns	
t_{WLWH}	Write Pulse Width	65		85		ns	
t_{WHAX}	Address Hold after End of Write	5		5		ns	
t_{EHAX}	Address Hold Time from Chip Enable	15		15		ns	
t_{ELEH}	Chip Enable Active to End of Write	75		100		ns	
t_{DVWH}	Data Valid to End of Write	35		45		ns	
t_{WHDX}	Data Hold Time from Write Enable	0		0		ns	
t_{EHDX}	Data Hold Time from Chip Enable	10		10		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	0		0		ns	1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	30	0	40	ns	1,2

Notes: 1 Measured with load as shown in Figure B page 4
2 If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low or after $\overline{W}$ going low, the outputs remain in the high-impedance state

Figure 6. Write Control Write Cycle Timing

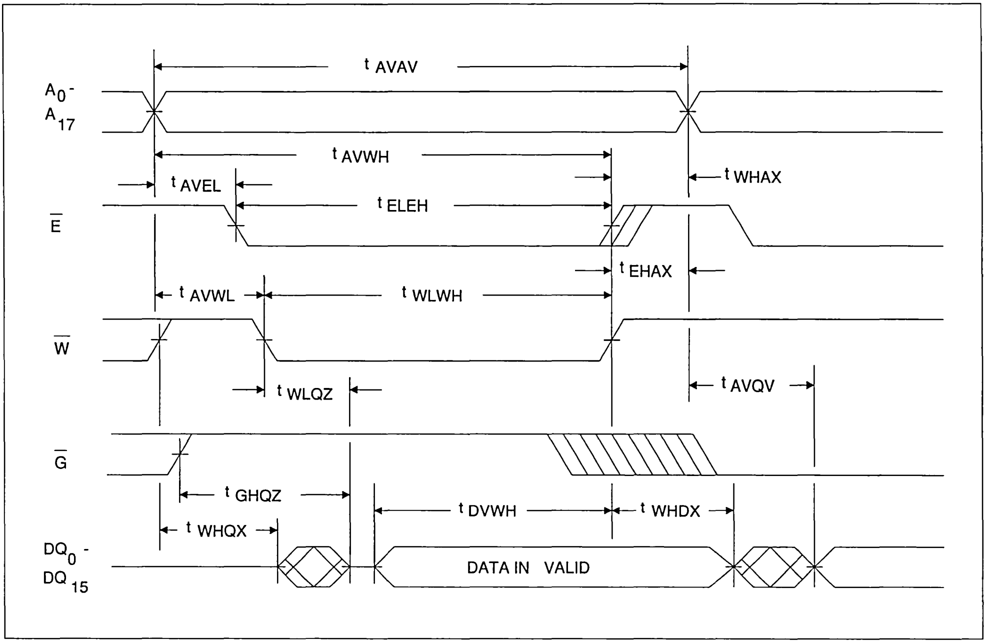
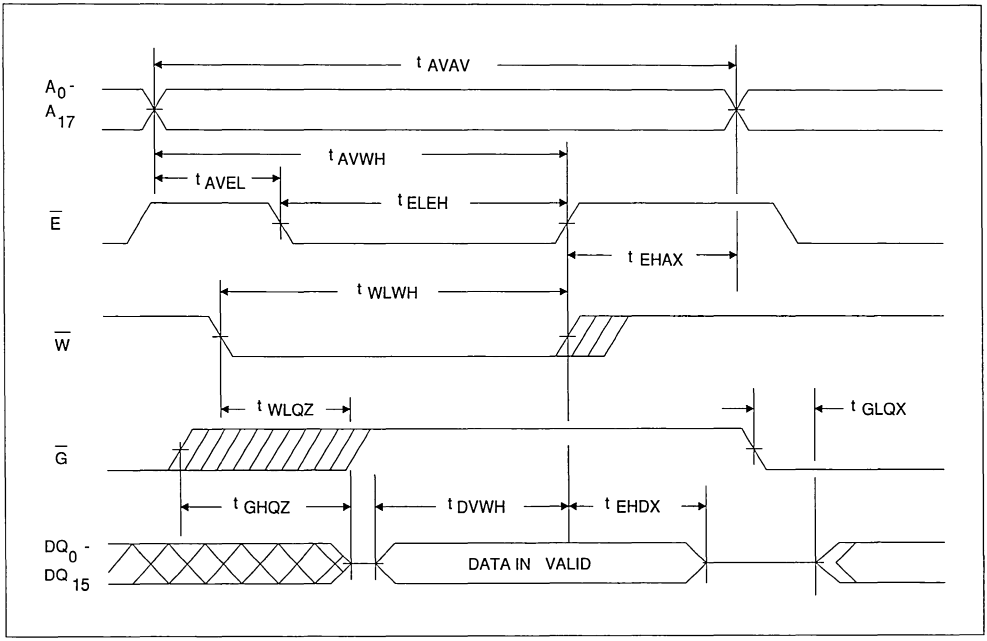
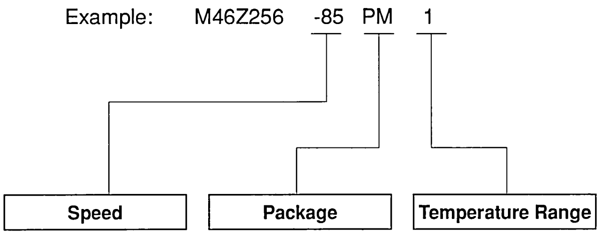

tAVAV
A0 - A17
tAVWH
tAVEL
tWHAX
tELEH
E
tEHAX
tAVWL
tWLWH
W
tWLQZ
tAVQV
G
tGHQZ
tDVWH
tWHDX
tWHQX
DQ0 - DQ15
DATA IN VALID

Figure 7. Chip Enable Control Write Cycle Timing


tAVAV
A0 - A17
tAVWH
tAVEL
tELEH
E
tEHAX
tWLWH
W
tWLQZ
tGLQX
G
tGHQZ
tDVWH
tEHDX
DQ0 - DQ15
DATA IN VALID

ORDERING INFORMATION


Example: M46Z256 -85 PM 1
Speed
Package
Temperature Range

Speed		Package		Temperature Range	
-85	85 ns	PM	PMDIP40	1	0 to 70 °C
-120	120 ns				

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

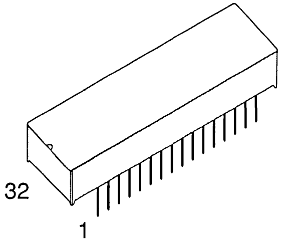
For further information on any aspect of this device, please contact our Sales Office nearest to you.

M48Z256
M48Z256Y

CMOS 256K x 8 ZEROPOWER SRAM

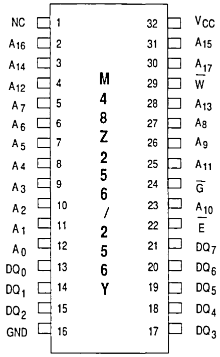
PRELIMINARY DATA

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEAR MINIMUM DATA RETENTION IN THE ABSENCE OF POWER
- COMPATIBLE WITH INDUSTRY STANDARD 256K x 8 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- DUAL WRITE PROTECT VOLTAGES:
  - M48Z256 $4.55V \leq V_{PFD} \leq 4.75V$
  - M48Z256Y $4.30V \leq V_{PFD} \leq 4.50V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED.



PMLDIP32 Module

Figure 1. Pin Connections


NC 1
A_{16} 2
A_{14} 3
A_{12} 4
A_7 5
A_6 6
A_5 7
A_4 8
A_3 9
A_2 10
A_1 11
A_0 12
DQ_0 13
DQ_1 14
DQ_2 15
GND 16
M48Z256/256Y
32 V_{CC}
31 A_{15}
30 A_{17}
29 $\overline{W}$
28 A_{13}
27 A_8
26 A_9
25 A_{11}
24 $\overline{G}$
23 A_{10}
22 $\overline{E}$
21 DQ_7
20 DQ_6
19 DQ_5
18 DQ_4
17 DQ_3

DESCRIPTION

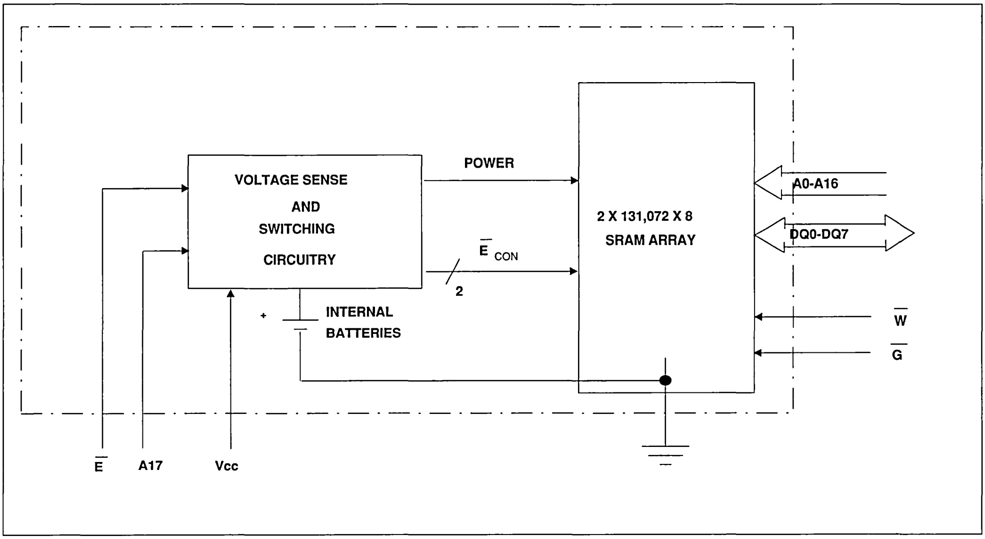
The M48Z256/256Y 256K x 8 ZEROPOWER™ RAM is a non-volatile 2,097,152 bit SRAM organized as 262,144 words by 8 bits. The device combines internal lithium batteries and full CMOS SRAMs in a plastic 32 pin DIP. The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z256/256Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

PIN NAMES

A0-A17	Address Input	Vcc	+5 Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data In/Data Out

Figure 2. Block Diagram


VOLTAGE SENSE
AND
SWITCHING
CIRCUITRY
POWER
$\overline{E}_{CON}$
2
INTERNAL
BATTERIES
+
2 X 131,072 X 8
SRAM ARRAY
A0-A16
DQ0-DQ7
$\overline{W}$
$\overline{G}$
$\overline{E}$
A17
Vcc

TRUTH TABLE

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc(Max)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
> Vcc(Min)	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(Min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
$\leq V_{SO}$	X	X	X	Deselect	High Z	Battery Back-up Mode

ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{CC} Pin Relative to GND	-0.3 to 7.0	V
V_T	Voltage on any Pin excluding V_{CC} Relative to GND ($V_T \leq V_{CC}$+0.3)	-0.3 to 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{STG}	Ambient Storage Temperature	-40 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +70	°C
T_{SLD}	Soldering Temperature for 10 Seconds	260	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	Note
Vcc	Supply Voltage (M48Z256)	4.75	5.5	V	1
Vcc	Supply Voltage (M48Z256Y)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; Vcc min ≤ Vcc ≤ Vcc max)

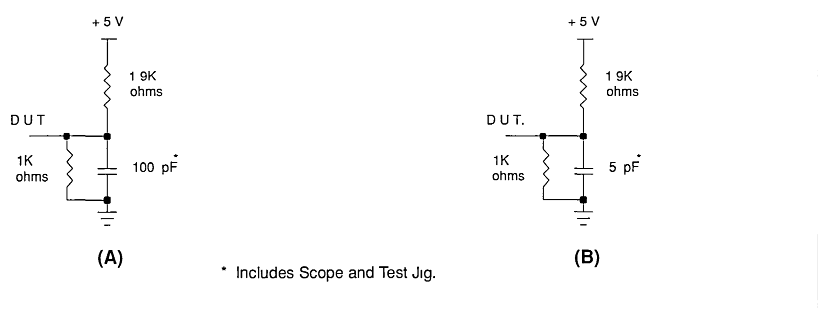
Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{CC1}	Average Vcc Power Supply Current ($\overline{E}= V_{IL}$)		75	110	mA	2,5
I_{CC2}	TTL Standby Current ($\overline{E}= V_{IH}$)		5	12	mA	5
I_{CC3}	CMOS Standby Current ($\overline{E} \geq$ Vcc -0.2V)		2.5	4	mA	3,5
I_{IL}	Input Leakage Current (Any Input)	-2		+2	µA	4
I_{OL}	Output Leakage Current	-2		+2	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-1.0 mA)	2.4			V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)			0.4	V	1

Notes: 1. All voltages referenced to GND.
2. I_{CC1} measured with outputs open.
3. Measured with $0V \leq V_I \leq 0.2V$ or $V_I \geq V_{CC}$ - 0.2V.
4. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected.
5. Typical values indicate operation at T_A=25°C and V_{CC}=5V.

AC TEST CONDITION

Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS


+ 5 V
1 9K ohms
D U T
1K ohms
100 pF*
(A)
+ 5 V
1 9K ohms
D U T.
1K ohms
5 pF*
(B)

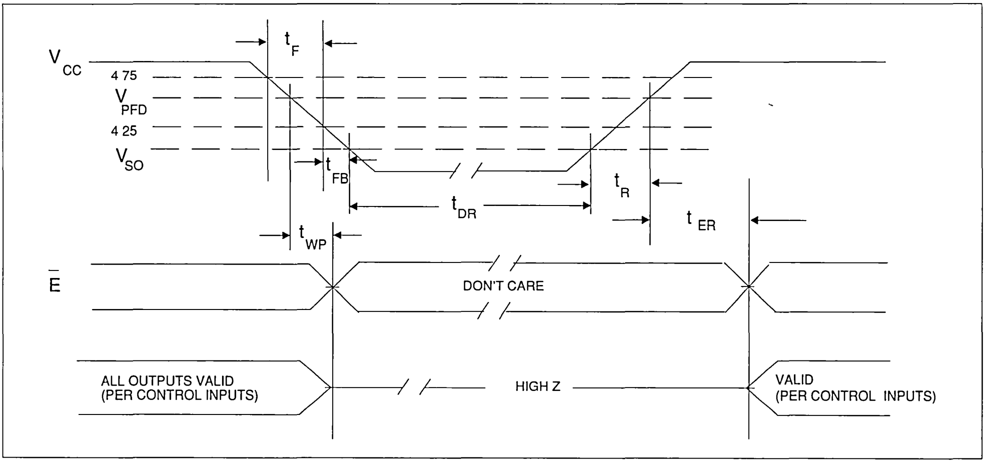
* Includes Scope and Test Jig.

CAPACITANCE (T_A = 25°C, f=1MHz)

Symbol	Parameter	Max	Unit	Note
C_I	Capacitance on All Pins (except DQ)	20.0	pF	1,2
C_{DQ}	Capacitance on DQ Pins	20.0	pF	1,2,3

Notes: 1. Effective capacitance measured with power supply at 5.0 V.
2 These parameters are sampled and not 100% tested.
3 Measured with outputs deselected

Figure 3. Power Down/Up Timing


V_{CC}
4 75
V_{PFD}
4 25
V_{SO}
t_F
t_{FB}
t_{DR}
t_R
t_{ER}
t_{WP}
$\overline{E}$
DON'T CARE
ALL OUTPUTS VALID (PER CONTROL INPUTS)
HIGH Z
VALID (PER CONTROL INPUTS)

AC ELECTRICAL CHARACTERISTICS (Power down/up Timing)

($0^\circ C \le T_A \le +70^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_F	4.75 to 4.25V V_{CC} Fall Time	300			µs	
t_{FB}	4.25 to V_{SO} V_{CC} Fall Time	10			µs	
t_{WP}	Write Protect Time from $V_{CC}=V_{PFD}$	40	100	150	µs	1
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	0			µs	
t_{ER}	$\overline{E}$ Recovery Time	40	80	120	ms	1

DC ELECTRICAL CHARACTERISTICS (Power down/up Trip Points)

($0^\circ C \le T_A \le +70^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{PFD}	Power- Fail Deselect Voltage (M48Z256)	4.55	4.62	4.75	V	1,2
V_{PFD}	Power- Fail Deselect Voltage (M48Z256Y)	4.30	4.37	4.50	V	1,2
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1,2
t_{DR}	Data Retention Time in Absence of V_{CC}	10			YEARS	3

Notes: 1. Typical values indicate operation at T_A=25C and V_{CC}=5V.
2. All voltages referenced to GND.
3 t_{DR} is the accumulated time in absence of power from the time V_{CC} is first applied. t_{DR} is specified @ 25°C.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z256/256Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data. The internal coin cells will maintain data in the M48Z256/256Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

READ MODE

The M48Z256/256Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 2,097,152 locations in the static storage array. Thus, the unique address specified by the 18 Address Inputs defines which one of the 262,144 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

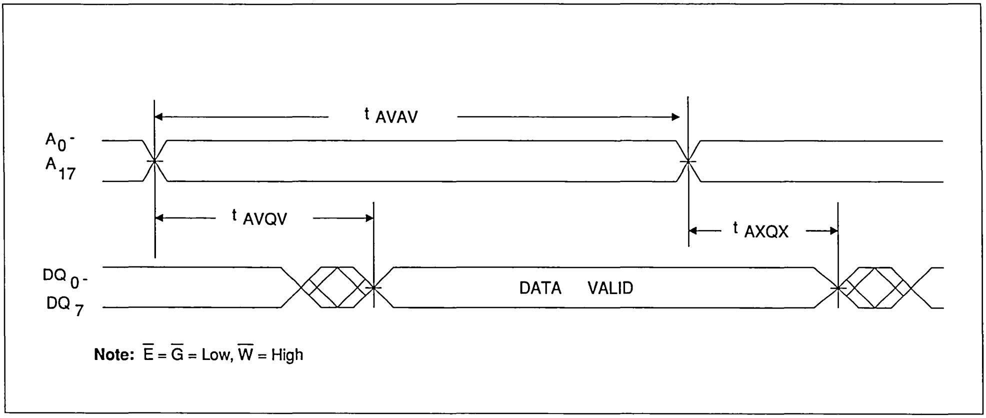
AC ELECTRICAL CHARACTERISTICS (Read Cycle)

(0°C ≤ T_A ≤ + 70°C, Vcc min ≤ Vcc ≤ Vcc max)

Symbol	Parameter	48Z256/256Y-85		48Z256/256Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Read Cycle Time	85		120		ns	
t_{AVQV}	Address Access Time		85		120	ns	1
t_{ELQV}	Chip Enable Access Time		85		120	ns	1
t_{GLQV}	Output Enable Access Time		45		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	5		5		ns	2
t_{GLQX}	Output Enable to Q Low-Z	0		0		ns	2
t_{EHQZ}	Chip Enable High to Q High-Z	0	35	0	45	ns	2
t_{GHQZ}	Output Enable High to High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

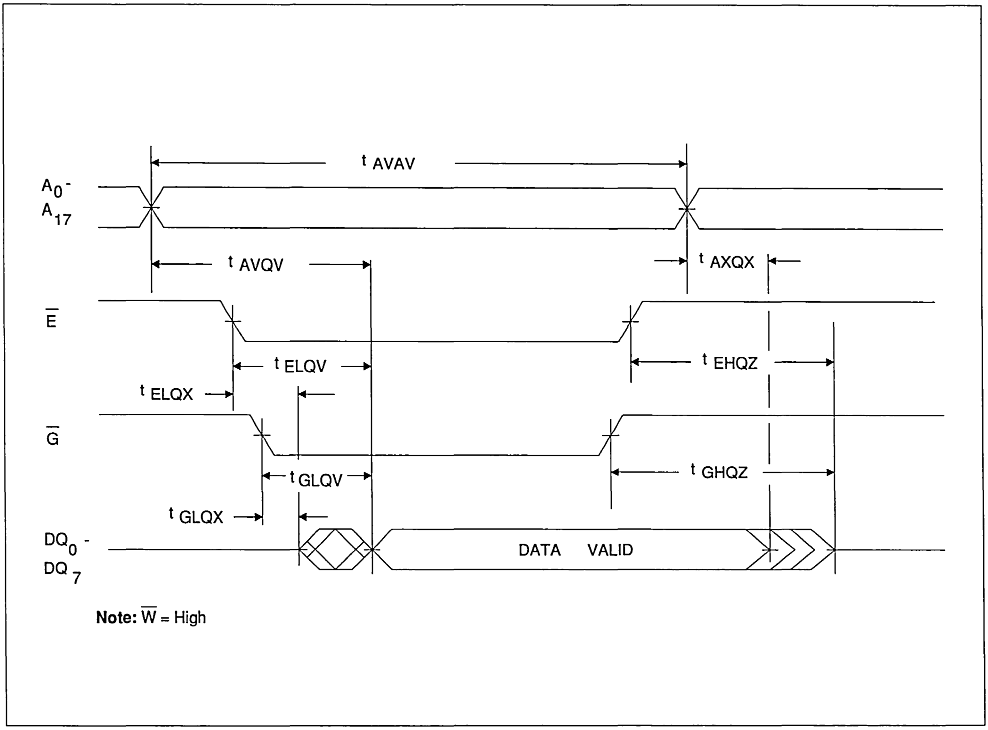
Notes: 1. Measured with load as shown in Figure A page 4.
2. Measured with load as shown in Figure B page 4.

Figure 4. Read Timing n° 1 (Address Access)


tAVAV
A0 -
A17
tAVQV
tAXQX
DQ0 -
DQ7
DATA VALID

Note: $\overline{E} = \overline{G}$ = Low, $\overline{W}$ = High

Figure 5. Read Timing n° 2


tAVAV
A0 -
A17
tAVQV
tAXQX
E
tELQV
tEHQZ
tELQX
G
tGLQV
tGHQZ
tGLQX
DQ0 -
DQ7
DATA VALID

Note: $\overline{W}$ = High

WRITE MODE

The M48Z256/256Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0^\circ C \le T_A \le +70^\circ C$, V_{CC} min $\le V_{CC} \le V_{CC}$ max)

Symbol	Parameter	48Z256/256Y-85		48Z256/256Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Write Cycle Time	85		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to End of Write	75		100		ns	
t_{WLWH}	Write Pulse Width	65		85		ns	
t_{WHAX}	Address Hold after End of Write	5		5		ns	
t_{EHAX}	Address Hold Time from Chip Enable	15		15		ns	
t_{ELEH}	Chip Enable Active to End of Write	75		100		ns	
t_{DVWH}	Data Valid to End of Write	35		45		ns	
t_{WHDX}	Data Hold Time from Write Enable	0		0		ns	
t_{EHDX}	Data Hold Time from Chip Enable	10		10		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	0		0		ns	1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	30	0	40	ns	1,2

Notes: 1. Measured with load as shown in Figure B page 4.
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low or after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 6. Write Control Write Cycle Timing

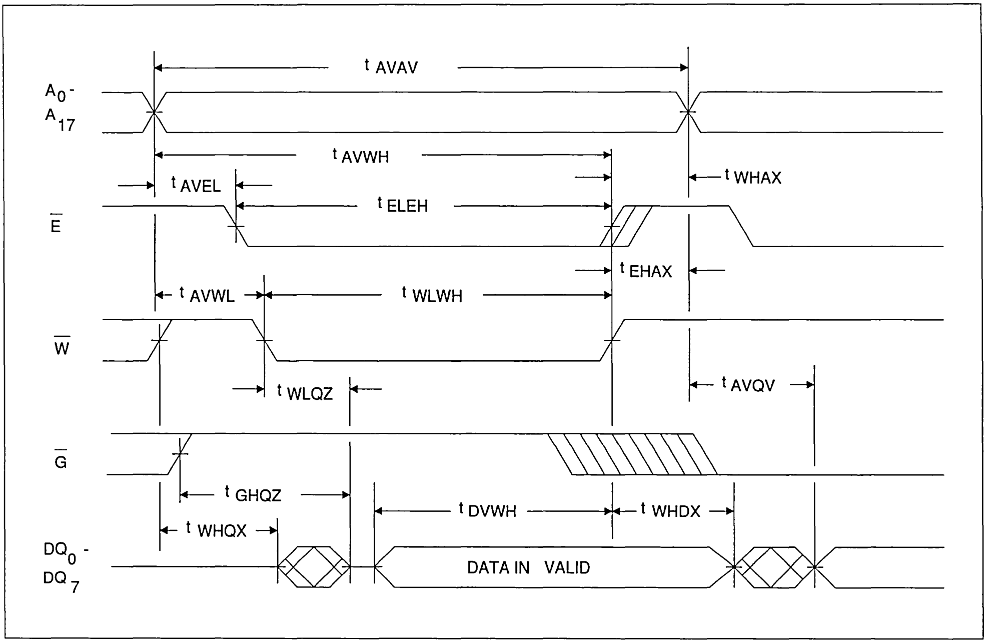
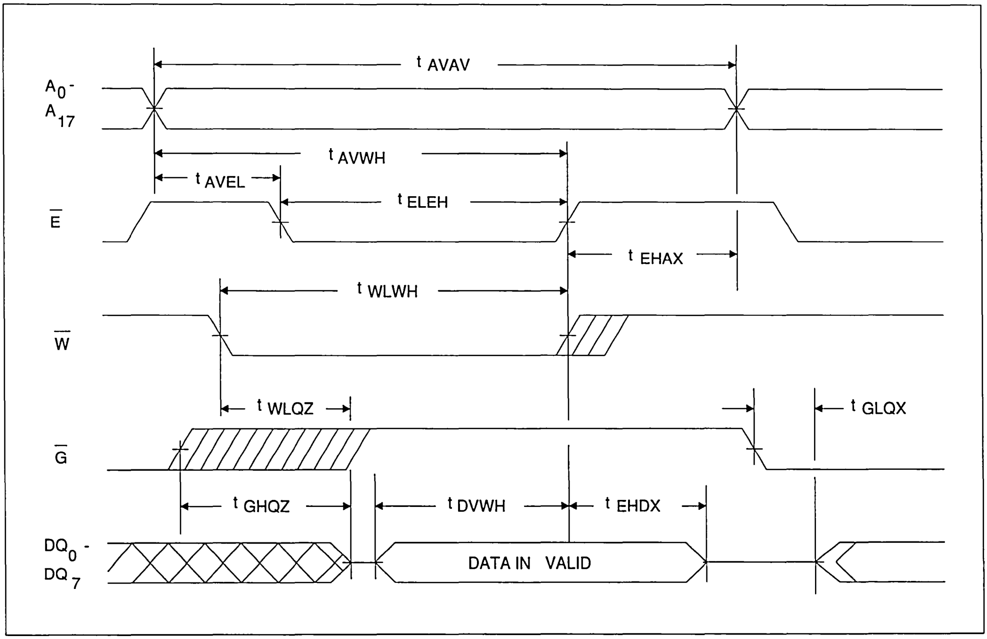

t AVAV
A0 - A17
t AVWH
t AVEL
t WHAX
t ELEH
E
t EHAX
t AVWL
t WLWH
W
t WLQZ
t AVQV
G
t GHQZ
t DVWH
t WHDX
t WHQX
DQ0 - DQ7
DATA IN VALID

Figure 7. Chip Enable Control Write Cycle Timing


t AVAV
A0 - A17
t AVWH
t AVEL
t ELEH
E
t EHAX
t WLWH
W
t WLQZ
t GLQX
G
t GHQZ
t DVWH
t EHDX
DQ0 - DQ7
DATA IN VALID

ORDERING INFORMATION

Example: M48Z256 -85 PL 1

Speed		Package		Temperature Range	
-85	85 ns	PL	PMLDIP32	1	0 to 70 °C
-120	120 ns				

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.

CMOS 512K x 8 ZEROPOWER SRAM

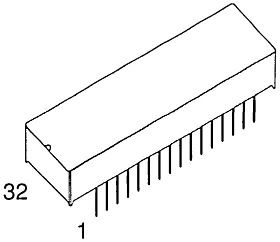
PRELIMINARY DATA

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 5 YEAR MINIMUM DATA RETENTION IN THE ABSENCE OF POWER
- COMPATIBLE WITH INDUSTRY STANDARD 512K x 8 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- DUAL WRITE PROTECT VOLTAGES:
  – M48Z512 4.55V ≤ V_{PFD} ≤ 4.75V
  – M48Z512Y 4.30V ≤ V_{PFD} ≤ 4.50V
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED.

DESCRIPTION

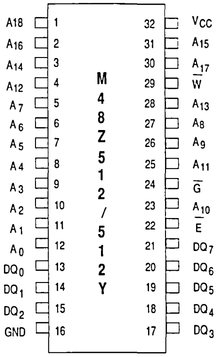
The M48Z512/512Y 512K x 8 ZEROPOWER™ RAM is a non-volatile 4,194,304 bit SRAM organized as 524,288 words by 8 bits. The device combines internal lithium batteries and full CMOS SRAMs in a plastic 32 pin DIP. The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z512/512Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.



PMLDIP32 Module

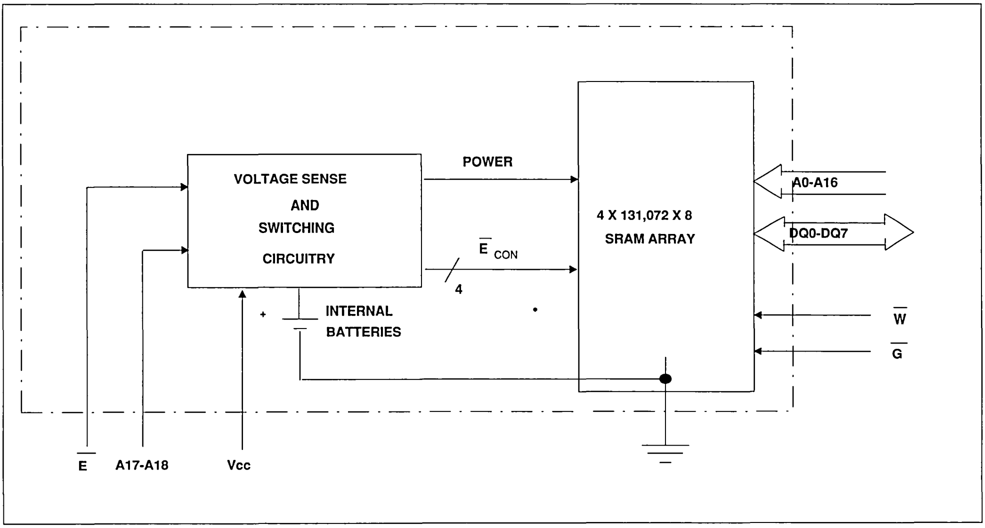
Figure 1. Pin Connections



PIN NAMES

A0-A18	Address Input	Vcc	+5 Volts
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
		$\overline{G}$	Output Enable
GND	Ground	DQ0-DQ7	Data In/Data Out

Figure 2. Block Diagram


VOLTAGE SENSE AND SWITCHING CIRCUITRY
POWER
$\overline{E}_{CON}$
4
INTERNAL BATTERIES
+
4 X 131,072 X 8 SRAM ARRAY
A0-A16
DQ0-DQ7
$\overline{W}$
$\overline{G}$
$\overline{E}$
A17-A18
Vcc

TRUTH TABLE

Vcc	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< Vcc(Max) > Vcc(Min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD}(Min) > V_{SO}	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High Z	Battery Back-up Mode

ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{CC} Pin Relative to GND	-0.3 to 7.0	V
V_T	Voltage on any Pin excluding V_{CC} Relative to GND ($V_T \leq V_{CC}+0.3$)	-0.3 to 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{STG}	Ambient Storage Temperature	-40 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +70	°C
T_{SLD}	Soldering Temperature for 10 Seconds	260	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below -0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	Note
Vcc	Supply Voltage (M48Z512)	4.75	5.5	V	1
Vcc	Supply Voltage (M48Z512Y)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	Vcc + 0.3v	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$; Vcc min ≤ Vcc ≤ Vcc max)

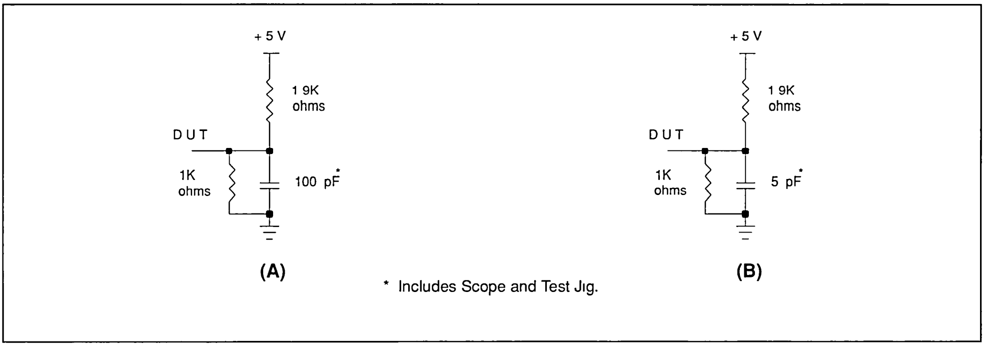
Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{CC1}	Average Vcc Power Supply Current ($\overline{E}= V_{IL}$)		75	115	mA	2,5
I_{CC2}	TTL Standby Current ($\overline{E}= V_{IH}$)		7	17	mA	5
I_{CC3}	CMOS Standby Current ($\overline{E} \geq$ Vcc -0.2V)		2.5	5	mA	3,5
I_{IL}	Input Leakage Current (Any Input)	-4		+4	µA	4
I_{OL}	Output Leakage Current	-4		+4	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT}=-1.0 mA)	2.4			V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1 mA)			0.4	V	1

Notes: 1. All voltages referenced to GND.
2. I_{CC1} measured with outputs open.
3. Measured with $0V \leq V_I \leq 0.2V$ or $V_I \geq V_{CC} - 0.2V$.
4. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected.
5. Typical values indicate operation at T_A=25°C and V_{CC}=5V.

AC TEST CONDITION

Input Levels	0.0V to 3.0V
Transition Times	5ns
Input and Output Reference Levels	1.5V

OUTPUT LOAD DIAGRAMS


+ 5 V
1 9K ohms
D U T
1K ohms
100 pF*
(A)
+ 5 V
1 9K ohms
D U T
1K ohms
5 pF*
(B)

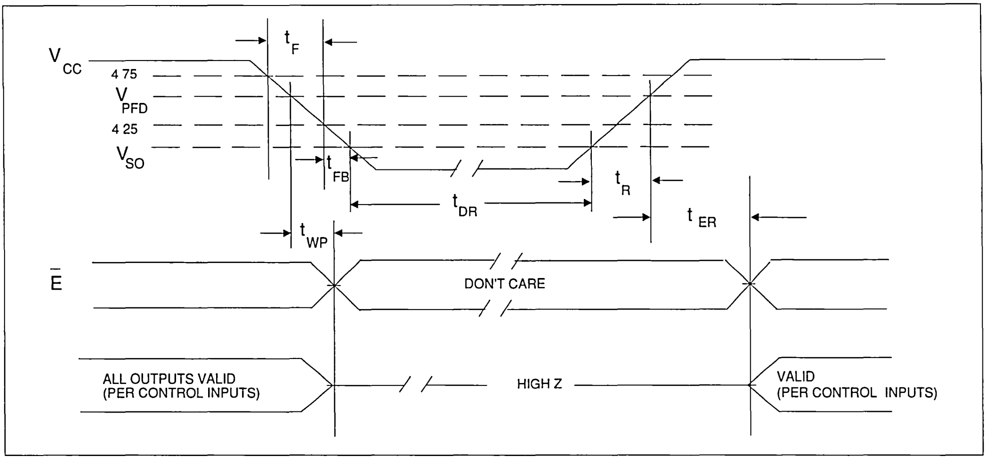
* Includes Scope and Test Jig.

CAPACITANCE (T_A = 25°C, f=1MHz)

Symbol	Parameter	Max	Unit	Note
C_I	Capacitance on All Pins (except DQ)	40.0	pF	1,2
C_{DQ}	Capacitance on DQ Pins	40.0	pF	1,2,3

Notes: 1. Effective capacitance measured with power supply at 5.0 V.
2. These parameters are sampled and not 100% tested.
3. Measured with outputs deselected.

Figure 3. Power Down/Up Timing


V_{CC}
4 75
V_{PFD}
4 25
V_{SO}
t_F
t_{FB}
t_{DR}
t_R
t_{ER}
t_{WP}
$\overline{E}$
DON'T CARE
ALL OUTPUTS VALID (PER CONTROL INPUTS)
HIGH Z
VALID (PER CONTROL INPUTS)

AC ELECTRICAL CHARACTERISTICS (Power down/up Timing)
($0^\circ C \le T_A \le +70^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_F	4.75 to 4.25V V_{CC} Fall Time	300			µs	
t_{FB}	4.25 to V_{SO} V_{CC} Fall Time	10			µs	
t_{WP}	Write Protect Time from $V_{CC}=V_{PFD}$	40	100	150	µs	1
t_R	V_{SO} to V_{PFD} (Max) V_{CC} Rise Time	0			µs	
t_{ER}	$\overline{E}$ Recovery Time	40	80	120	ms	1

DC ELECTRICAL CHARACTERISTICS (Power down/up Trip Points) ($0^\circ C \le T_A \le +70^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{PFD}	Power- Fail Deselect Voltage (M48Z512)	4.55	4.62	4.75	V	1,2
V_{PFD}	Power- Fail Deselect Voltage (M48Z512Y)	4.30	4.37	4.50	V	1,2
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1,2
t_{DR}	Data Retention Time in Absence of V_{CC}	5			YEARS	3

Notes: 1. Typical values indicate operation at T_A=25C and V_{CC}=5V.
2. All voltages referenced to GND.
3. t_{DR} is the accumulated time in absence of power from the time V_{CC} is first applied. t_{DR} is specified @ 25°C.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z512/512Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data. The internal coin cells will maintain data in the M48Z512/512Y after the initial application of V_{CC} for an accumulated period of at least 5 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

READ MODE

The M48Z512/512Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 Address Inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

(0°C ≤ T_A ≤ + 70°C; V_{CC} min ≤ V_{CC} ≤ V_{CC} max)

Symbol	Parameter	48Z512/512Y-85		48Z512/512Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Read Cycle Time	85		120		ns	
t_{AVQV}	Address Access Time		85		120	ns	1
t_{ELQV}	Chip Enable Access Time		85		120	ns	1
t_{GLQV}	Output Enable Access Time		45		60	ns	1
t_{ELQX}	Chip Enable to Q Low-Z	5		5		ns	2
t_{GLQX}	Output Enable to Q Low-Z	0		0		ns	2
t_{EHQZ}	Chip Enable High to Q High-Z	0	35	0	45	ns	2
t_{GHQZ}	Output Enable High to High-Z	0	25	0	35	ns	2
t_{AXQX}	Output Hold From Address Change	10		10		ns	1

Notes: 1. Measured with load as shown in Figure A page 4.
2 Measured with load as shown in Figure B page 4.

Figure 4. Read Timing n° 1 (Address Access)

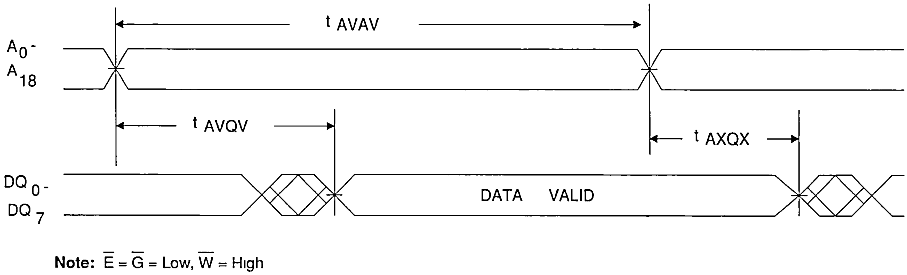
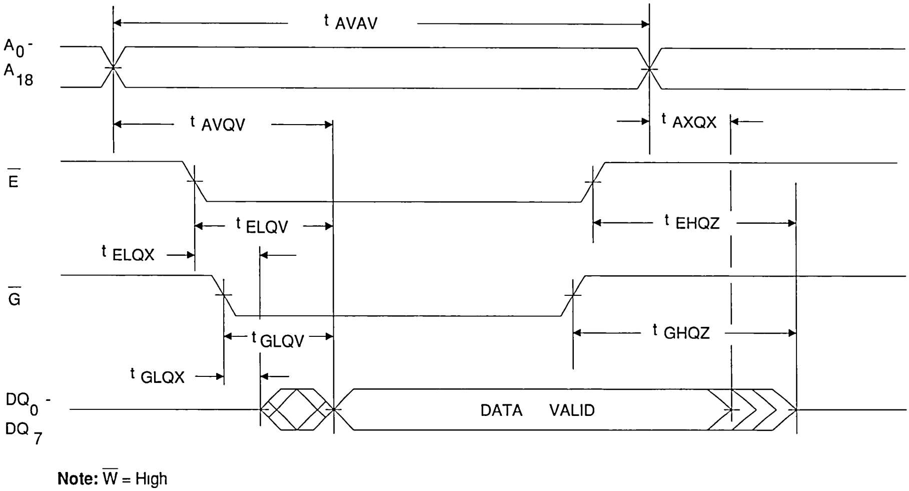

t AVAV
A0 -
A18
t AVQV
t AXQX
DQ 0 -
DQ 7
DATA VALID
Note: E = G = Low, W = High

Figure 5. Read Timing n° 2


t AVAV
A0 -
A18
t AVQV
t AXQX
E
t ELQV
t EHQZ
t ELQX
G
t GLQV
t GHQZ
t GLQX
DQ0 -
DQ 7
DATA VALID
Note: W = High

WRITE MODE

The M48Z512/512Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the later occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

($0°C \leq T_A \leq +70°C$, V_{CC} min $\leq V_{CC} \leq V_{CC}$ max)

Symbol	Parameter	48Z512/512Y-85		48Z512/512Y-120		Unit	Note
		Min	Max	Min	Max		
t_{AVAV}	Write Cycle Time	85		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0		ns	
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0		ns	
t_{AVWH}	Address Valid to End of Write	75		100		ns	
t_{WLWH}	Write Pulse Width	65		85		ns	
t_{WHAX}	Address Hold after End of Write	5		5		ns	
t_{EHAX}	Address Hold Time from Chip Enable	15		15		ns	
t_{ELEH}	Chip Enable Active to End of Write	75		100		ns	
t_{DVWH}	Data Valid to End of Write	35		45		ns	
t_{WHDX}	Data Hold Time from Write Enable	0		0		ns	
t_{EHDX}	Data Hold Time from Chip Enable	10		10		ns	
t_{WHQX}	$\overline{W}$ High to Q Active	0		0		ns	1,2
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	30	0	40	ns	1,2

Notes: 1 Measured with load as shown in Figure B page 4

2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low or after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 6. Write Control Write Cycle Timing

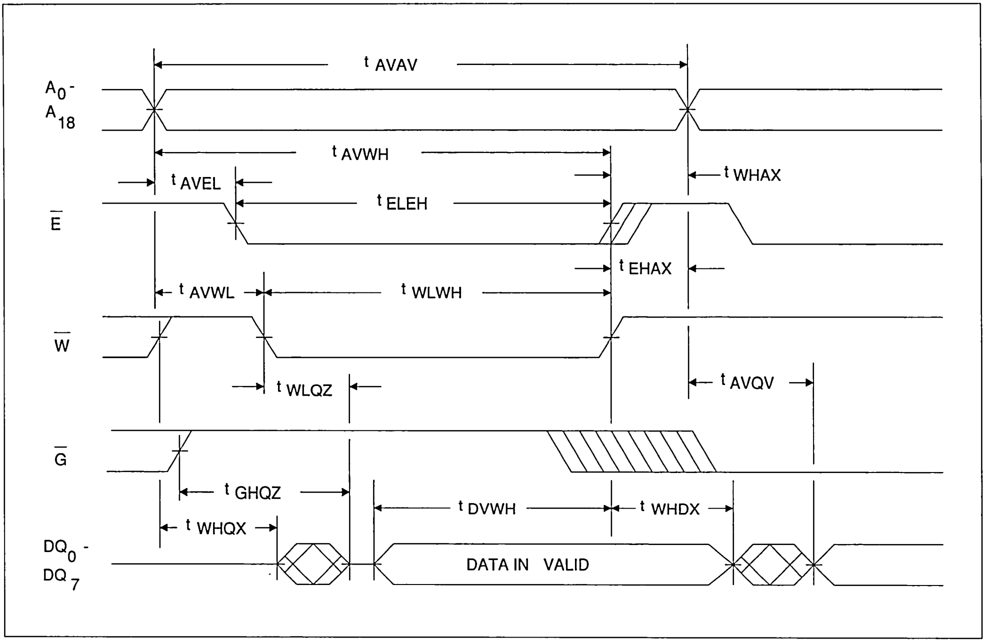
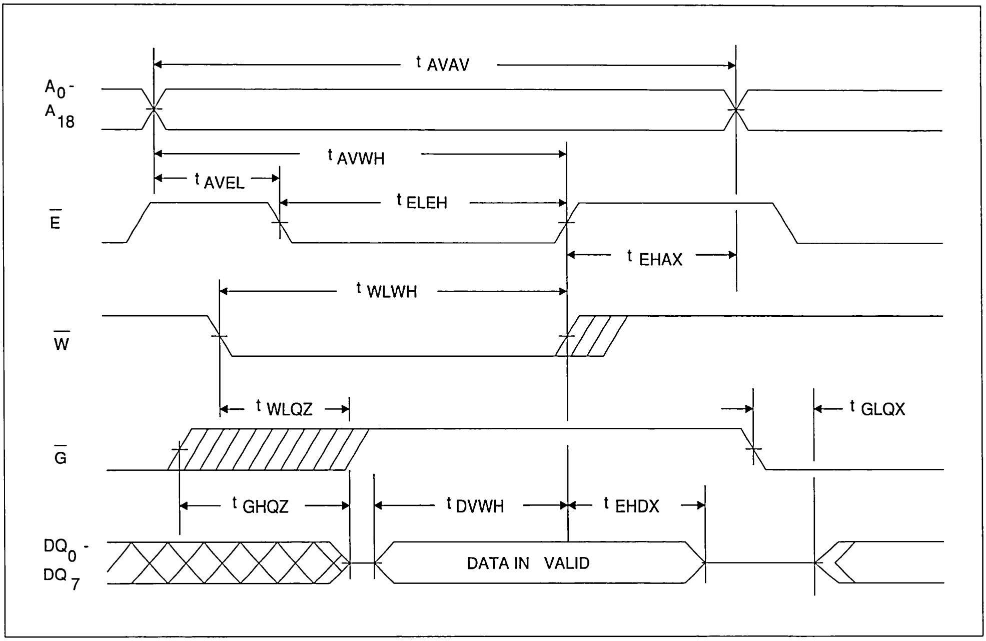
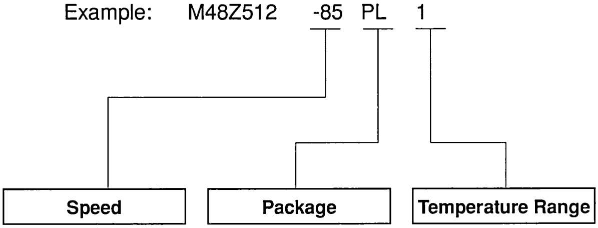

A0 - A18
E
W
G
DQ0 - DQ7
tAVAV
tAVWH
tAVEL
tWHAX
tELEH
tEHAX
tAVWL
tWLWH
tWLQZ
tAVQV
tGHQZ
tDVWH
tWHDX
tWHQX
DATA IN VALID

Figure 7. Chip Enable Control Write Cycle Timing


A0 - A18
E
W
G
DQ0 - DQ7
tAVAV
tAVWH
tAVEL
tELEH
tEHAX
tWLWH
tWLQZ
tGLQX
tGHQZ
tDVWH
tEHDX
DATA IN VALID

ORDERING INFORMATION



Example: M48Z512 -85 PL 1

Speed	
-85	85 ns
-120	120 ns

Package	
PL	PMLDIP32

Temperature Range	
1	0 to 70 °C

For a list of available options of Speed, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

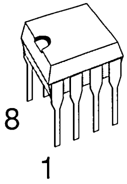
For further information on any aspect of this device, please contact our Sales Office nearest to you.

TIMEKEEPER MEMORIES

MK41T56

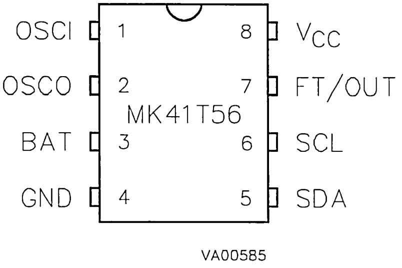
CMOS 64 x 8 SERIAL ACCESS TIMEKEEPER SRAM

- COUNTERS FOR SECONDS, MINUTES, HOURS, DAY, DATE, MONTH AND YEARS
- SOFTWARE CALIBRATION
- AUTOMATIC POWER FAIL DETECT AND SWITCH CIRCUITRY
- I^{2}C BUS COMPATIBLE
- 56 BYTES OF GENERAL PURPOSE RAM
- ULTRA-LOW BATTERY SUPPLY CURRENT OF 500nA



PSDIP8 (N)
0.4 mm Frame

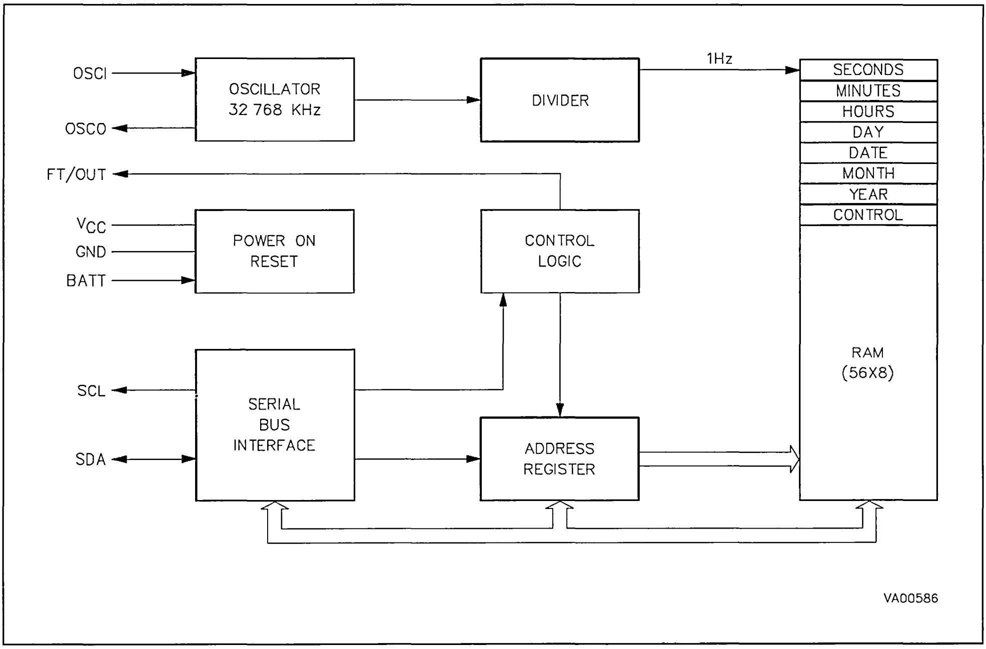
Figure 1. Pin Connection



DESCRIPTION

The MK41T56 TIMEKEEPER™ RAM is a low power 512-bit static CMOS RAM organized as 64 words by 8 bits. A built-in 32.768 kHz oscillator (externally crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in BCD format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each written or read data byte. The MK41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power fail-ures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium button cell. Typical data retention time is in excess of 10 years with a 38 mAh 3 volts lithium cell. The MK41T56 clock is supplied in a 8-pin dual-in-line plastic package.

Figure 2. Block Diagram


OSCI
OSCO
OSCILLATOR
32 768 KHz
DIVIDER
1Hz
SECONDS
MINUTES
HOURS
DAY
DATE
MONTH
YEAR
CONTROL
FT/OUT
VCC
GND
BATT
POWER ON
RESET
CONTROL
LOGIC
RAM
(56X8)
SCL
SDA
SERIAL
BUS
INTERFACE
ADDRESS
REGISTER
VA00586

OPERATION

The MK41T56 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct address (D0). The 64 bytes contained in the device can then be accessed sequentially in the following order :

1.	Seconds Register
2.	Minutes Register
3.	Hours Register
4.	Day Register
5.	Date Register
6.	Month Register
7.	Years Register
8.	Control Register
9.-64.	RAM

The MK41T56 clock continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD} the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT} the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power up the device switches from battery to V_{CC} at V_{BAT} and recognizes inputs when V_{CC} goes above V_{PFD} volts.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative To Ground	–0.3 to + 7	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{STG}	Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	–55 to + 125	°C
P_D	Total Device Power Dissipation	0.25	W
I_{OUT}	Output Sink Current	20	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for exended periods of time may affect reliability.

***CAUTION**: Negative undershoots below –0.3 volts are not allowedon any pin while in the Battery Back-up mode.*

REGISTER MAP

Address	Data								Function/Range BCD Format	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	ST								Seconds	00-59
1	X								Minutes	00-59
2	X	X							Hour	00-23
3	X	X	X	X	X				Day	01-07
4	X	X							Date	01-31
5	X	X	X						Month	01-12
6									Year	00-99
7	OUT	FT	S						Control	

KEYS :

S = SIGN BIT
ST = STOP BIT
FT = FREQUENCY TEST BIT
X = DON'T CARE
OUT = OUTPUT LEVEL

CHARACTERISTICS OF THE 2-WIRE BUS

This bus is intended for communication between different ICs. It consists of two lines : one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined :

Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined :

Bus not busy : Both data and clock lines remain HIGH.

Start data transfer : A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer : A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid : The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a low speed mode (2kHz clock rate) and a high speed mode (100kHz clock rate) are defined. The MK41T56 clock works in both modes. By definition a device that gives out a message is called “transmitter”, the receiving device that gets the message is called “receiver”. The device that controls the message is called “master”. The devices that are controlled by the master are called “slaves”.

Acknowledge : Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 3A. Data Transfer Sequence of the Serial Bus

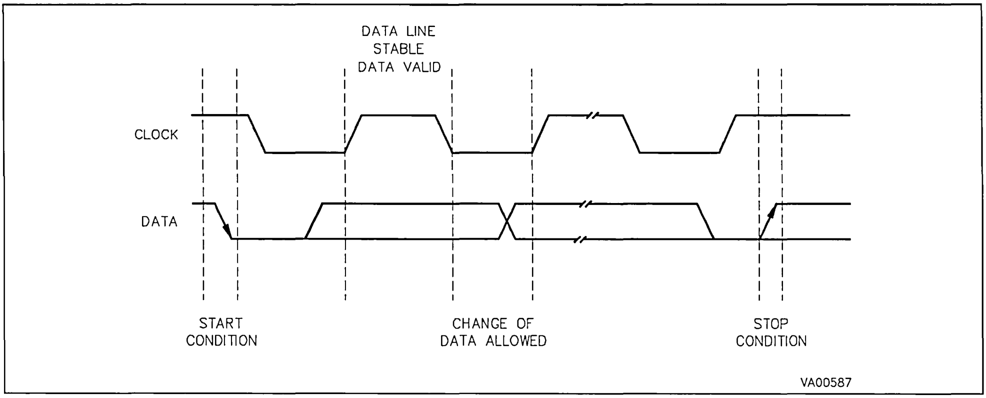

DATA LINE
STABLE
DATA VALID
CLOCK
DATA
START
CONDITION
CHANGE OF
DATA ALLOWED
STOP
CONDITION
VA00587

Figure 3B. Acknowledgement

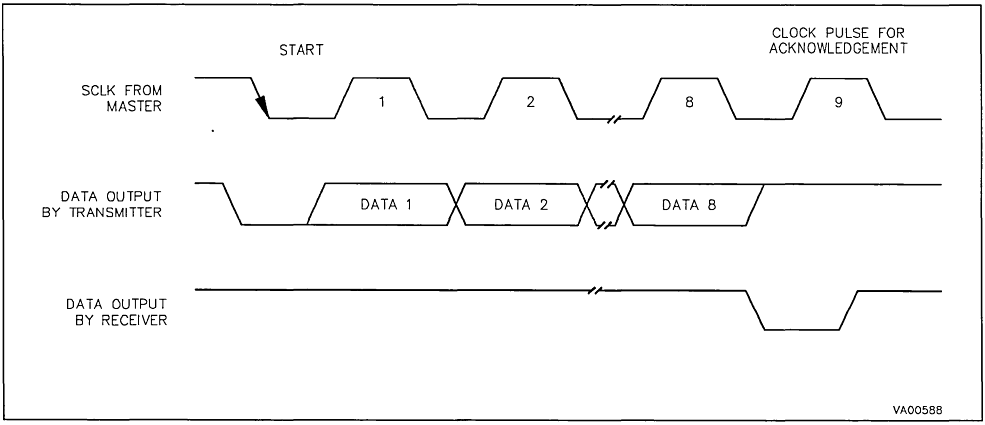
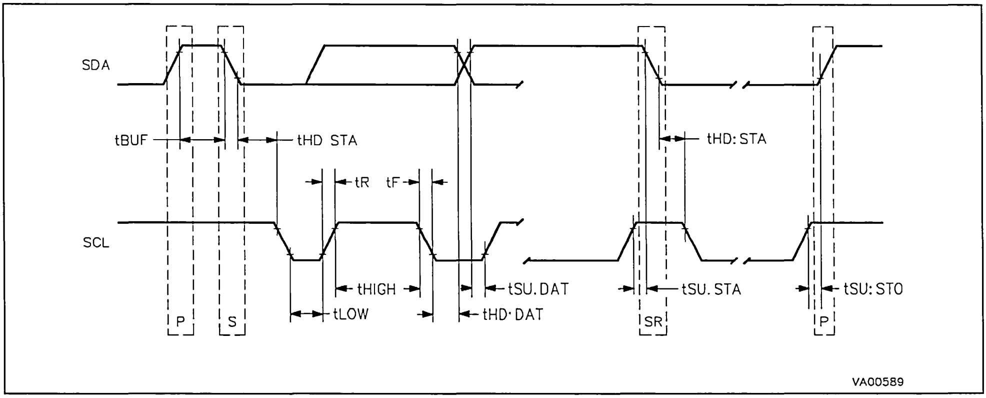

START
CLOCK PULSE FOR
ACKNOWLEDGEMENT
SCLK FROM
MASTER
1
2
8
9
DATA OUTPUT
BY TRANSMITTER
DATA 1
DATA 2
DATA 8
DATA OUTPUT
BY RECEIVER
VA00588

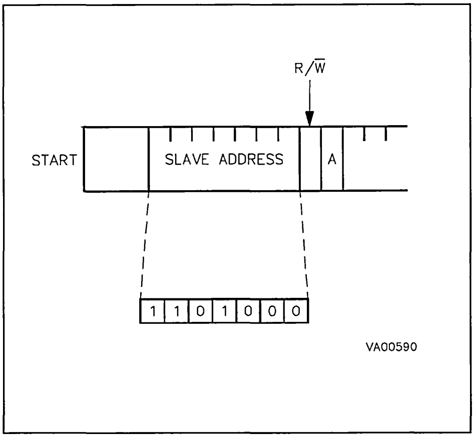
Figure 3C. Bus Timing Requirements


SDA
tBUF
tHD STA
tR
tF
tHD: STA
SCL
tHIGH
tLOW
tSU. DAT
tHD· DAT
tSU. STA
tSU: STO
P
S
SR
P
VA00589

Write Mode

In this mode the master transmitter transmits to the MK41T56 slave receiver. Bus protocol is shown in Figure 5. Following the START condition and slave address, a logic 0 (R/$\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address A_n will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The MK41T56 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

Figure 4. Slave Address Location



Read Mode

In this mode the master reads the MK41T56 slave after setting the slave address. See Figure 6. Following the write mode control bit (R/$\overline{W}$ = 0) and the acknowledge bit, the word address A_n is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$ = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The MK41T56 slave transmitter will now place the data byte at address $A_n + 1$ on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to $A_n + 2$.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the MK41T56 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer. See Figure 7.

Figure 5. Write Mode

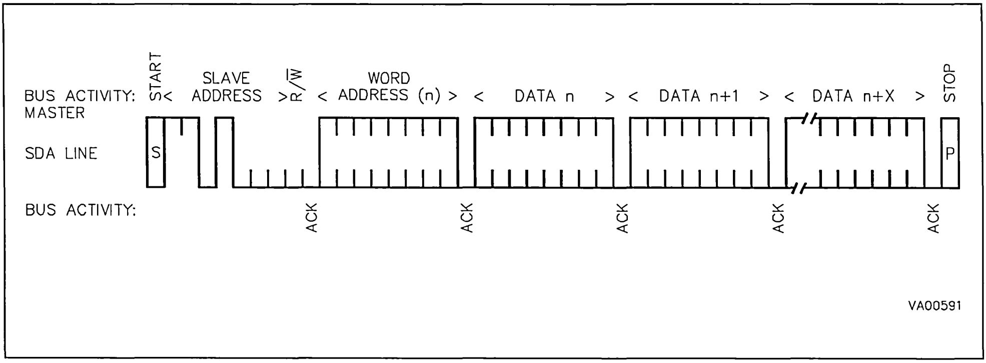

BUS ACTIVITY: MASTER
START
S
SLAVE ADDRESS
R/W
WORD ADDRESS (n)
DATA n
DATA n+1
DATA n+X
STOP
P
SDA LINE
BUS ACTIVITY:
ACK
ACK
ACK
ACK
ACK
VA00591

Figure 6. Read Mode

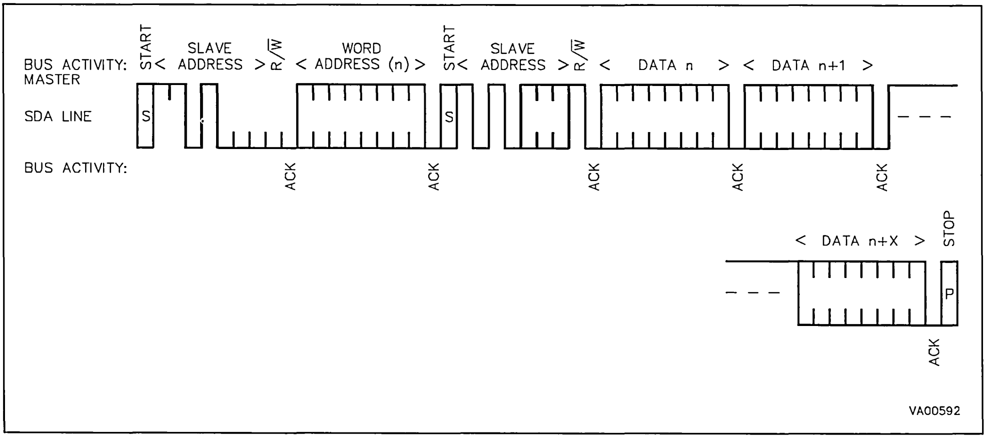
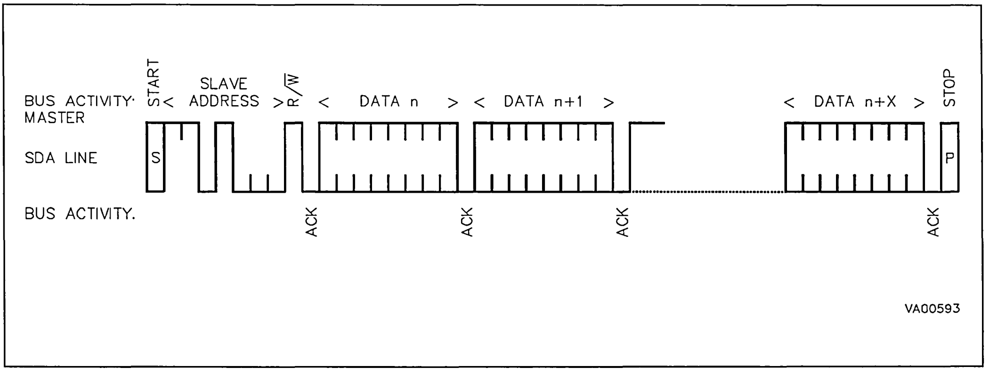

BUS ACTIVITY: MASTER
START
S
SLAVE ADDRESS
R/W
WORD ADDRESS (n)
START
S
SLAVE ADDRESS
R/W
DATA n
DATA n+1
SDA LINE
BUS ACTIVITY:
ACK
ACK
ACK
ACK
ACK
DATA n+X
STOP
P
ACK
VA00592

Figure 7. Alternate Read Mode


BUS ACTIVITY· MASTER
START
S
SLAVE ADDRESS
R/W
DATA n
DATA n+1
DATA n+X
STOP
P
SDA LINE
BUS ACTIVITY.
ACK
ACK
ACK
ACK
VA00593

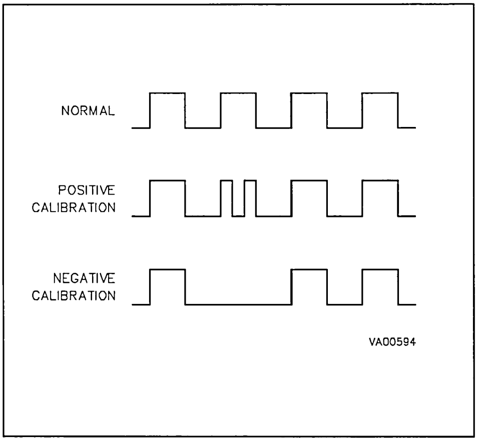
Calibration the Clock

The MK41T56 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical MK41T56 is accurate within ± 1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK41T56 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 8. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit ; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minutes cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary "1" is loaded into the register, only the first 2 minutes in the 64 minutes cycle will be modified ; if a binary 6 is loaded, the first 12 will be affected, and so on.

Figure 8. Divide by 128 Stage



Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is + 4.068 or - 2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 10.7 seconds per month.

Two methods are available for ascertaining how much calibration a given MK41T56 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration byte. The utility could even be menu driven and made foolproof.

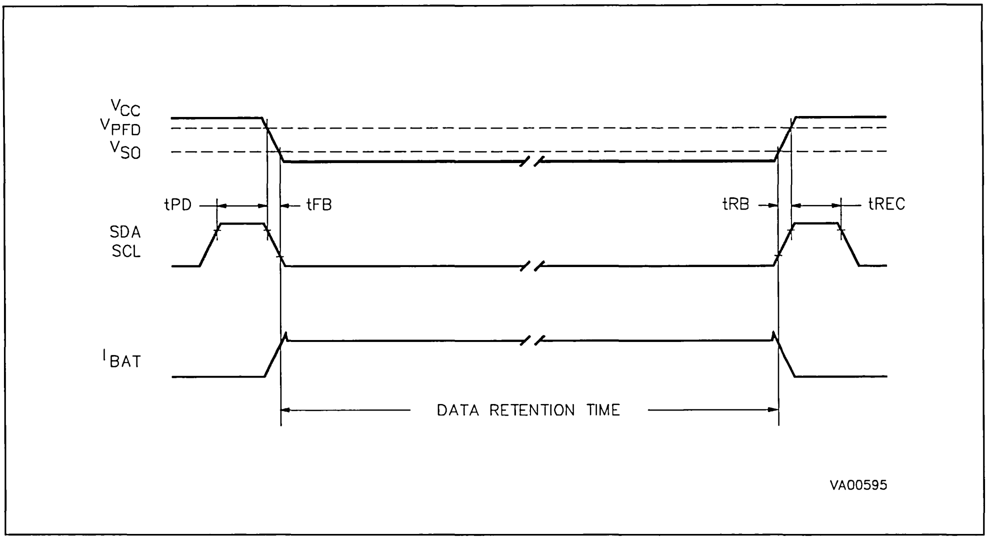
The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT.) bit, the seventh-most significant bit in the Control Register, is set to a "1", and the oscillator is running at 32768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a - 10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

OUTPUT DRIVER PIN

When the FT bit is not set the FT/OUT pin becomes an output driver that reflects the contents of D_7 of the control register. In other words when D_6 of location 7 is a zero and D_7 of location 7 is a zero and then the FT/OUT pin will be driven low.

Note : The FT/OUT pin is open drain which requires an external pullup resistor.

Figure 9. Power Up/Down Waveforms


VCC
VPFD
VSO
tPD
tFB
tRB
tREC
SDA
SCL
IBAT
DATA RETENTION TIME
VA00595

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
t_{PD}	SCL and SDA at V_{IH} before power down	0			ns	
t_{FB}	V_{PFD} to V_{SO} V_{DD} fall time	300			µs	
t_{RB}	V_{SO} to V_{PFD} V_{DD} rise time	100			µs	
t_{REC}	SCL and SDA at V_{IH} after power up	200			µs	
V_{PFD}	Power-fail deselect voltage	1.22 V_{BAT}	1.25 V_{BAT}	1.28 V_{BAT}	V	
V_{SO}	Battery back-up switchover voltage		V_{BAT}		V	

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Values		Units
		Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	KHz
t_{LOW}	The LOW period of the clock	4.7		µs
t_{HIGH}	The HIGH period of the clock	4		µs
t_R	SDA and SCL rise time		1	µs
t_F	SDA and SCL fall time		300	ns
$t_{HD\ STA}$	START condition hold time. After this period the first clock pulse is generated	4		µs
$t_{SU \cdot STA}$	Setup time for start condition (only relevant for a repeated start condition)	4.7		µs
$t_{SU\ DAT}$	Data setup time	250		ns
$t_{HD\ DAT}$	Data hold time	0 *		µs
$t_{SU \cdot STO}$	STOP condition setup	4.7		µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
C_I	Input capacitance on SCL, SDA		7	pf
T_I	Noise suppresion time constant at SCL and SDA input	0.25	1	µs

* Note that a transmitter must internally provide a hold time to bridge the undefined region (300 ns max.) of the falling edge of SCL.

CRYSTAL ELECTRICAL CHARACTERISTICS (externally supplied)

Symbol	Parameter	Values			Units
		Min.	Typ.	Max.	
f_O	Resonant frequency		32.768		kHz
r_S	Series resistance			35	kΩ
C_L	Load capacitance		12.5		pF

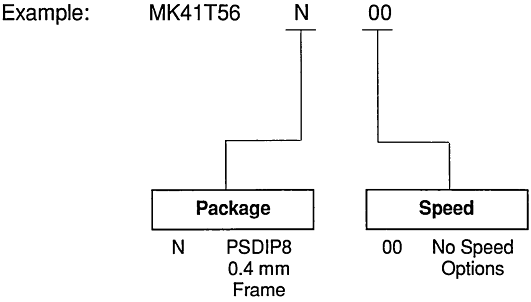
Note : Load capacitors are internally supplied with the MK41T56. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_{DD1}	Operating supply current				3	mA
I_{DD2}	Standby operating current	SCL/SDA = V_{CC} - 0.3V			1	mA
I_L	Input leakage current				10	µA
I_{OH}	Output leakage current				10	µA
V_{IH}	High level input voltage		3		V_{CC} + 0.8	V
V_{IL}	Low level input voltage		–0.3		1.5	V
V_{OL}	Low level output voltage	I_{OL} = 5mA, V_{CC} = 4.5V			0.4	V
V_{CC}	Supply voltage		4.5		5.5	V
GND	Ground			0		V
V_{BAT} (1)	Battery supply voltage		2.6	3	3.5	V
I_{BAT}	Battery supply current	V_{CC} = 0.0V, T_A = 25˚C, Oscillator On, V_{BAT} = 3V		450	500	nA

Note: 1. SGS-THOMSON recommends the RAYOVAC BR1225 or equivalent as the battery supply.

ORDERING INFORMATION



Package	
N	PSDIP8 0.4 mm Frame

Speed	
00	No Speed Options

For a list of available options refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

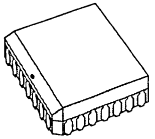
SGS-THOMSON
MICROELECTRONICS

MK48T85

CMOS 64 x 8 ADDRESS/DATA MULTIPLEXED TIMEKEEPER SRAM

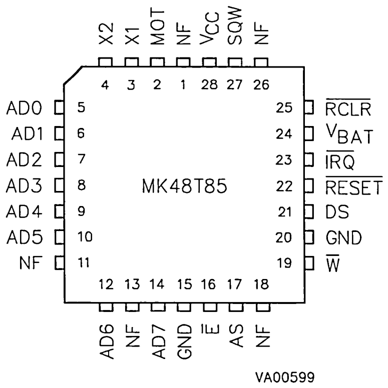
ADVANCE DATA

- DROP-IN REPLACEMENT FOR PC AT COMPUTER CLOCK/CALENDAR
- EXTERNAL BATTERY AND CRYSTAL PINS
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS:
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle



PLCC28 (C)

Figure 1. Pin Connection



PIN NAMES

$\overline{\text{RESET}}$	Reset
V_{CC}/GND	5 Volts/Ground
$\overline{\text{E}}$	Chip Select
AS	Address Strobe
$\overline{\text{W}}$	Read/Write
DS	Data Strobe
$\overline{\text{IRQ}}$	Interrupt Request
V_{BAT}	3 Volts Battery Input

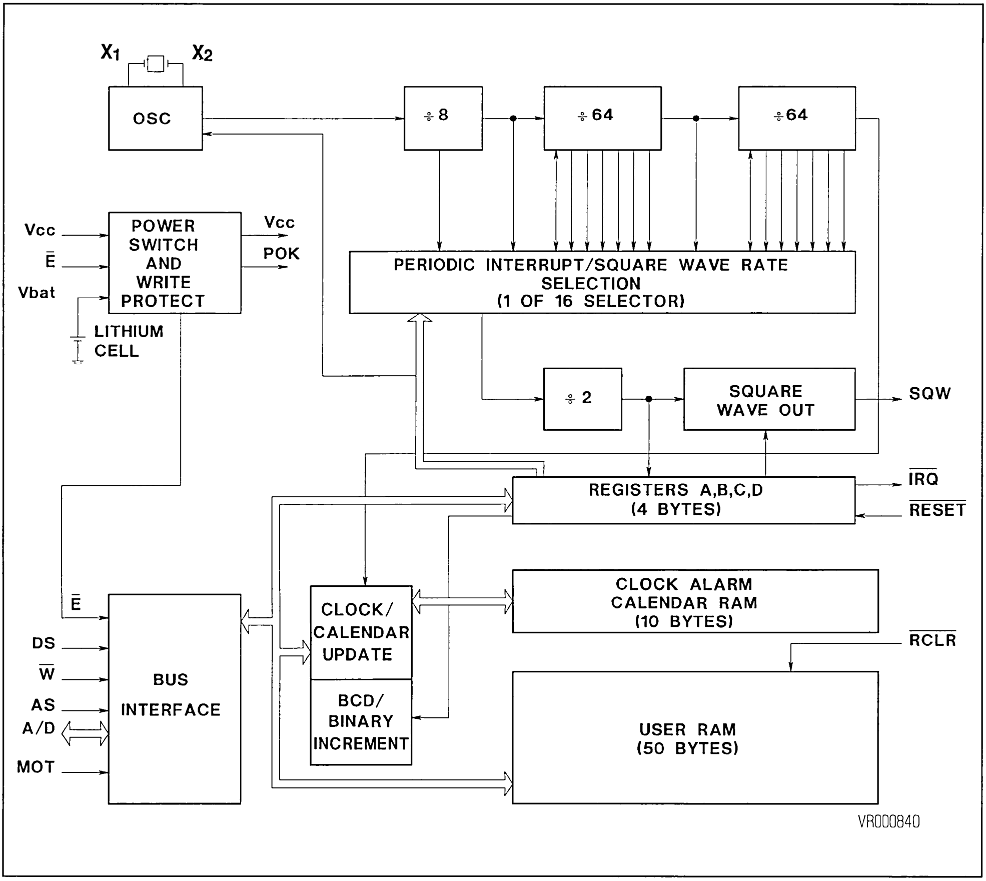
AD0-AD7	Address / Data
NF	No Function
MOT	Bus Type Selection
SQW	Square Wave Out
$\overline{\text{RCLR}}$	RAM Clear
X_1, X_2	32,768 Hz Crystal

NF pin serves no function and may be connected to other signals, within Absolute Maximum Ratings, without affecting device operation. The electrical characteristics are the same as the other inputs pins.

February 1992

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 2. Block Diagram


X1
X2
OSC
÷8
÷64
÷64
Vcc
E
Vbat
POWER SWITCH AND WRITE PROTECT
Vcc
POK
LITHIUM CELL
PERIODIC INTERRUPT/SQUARE WAVE RATE SELECTION (1 OF 16 SELECTOR)
÷2
SQUARE WAVE OUT
SQW
REGISTERS A,B,C,D (4 BYTES)
IRQ
RESET
CLOCK ALARM CALENDAR RAM (10 BYTES)
RCLR
E
DS
W
AS
A/D
MOT
BUS INTERFACE
CLOCK/ CALENDAR UPDATE
BCD/ BINARY INCREMENT
USER RAM (50 BYTES)
VR000840

DESCRIPTION

The MK48T85 TIMEKEEPER™ RAM is designed to be a functional replacement for the PC AT Computer clock/calendar. The functions available to the user include a time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupts, a square wave generator, and 50 bytes of static RAM. The MK48T85 provides connections for a battery and a 32,768 Hz crystal. The battery connection allows the user to back-up the RAM and clock functions in the absence of system voltage.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset. This allows sufficient time for V_{CC} to stabilize and gives the system clock a wake up period so that a valid system reset can be established.

OPERATION

The block diagram in Figure 2 shows the pin connections with the major functions of the MK48T85 (Real Time Clock/RAM). For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, and RCRL, see the MK8T87 datasheet.

SIGNAL DESCRIPTION

X_1, X_2 - The X1 and X2 pins are the connections for a standard 32,768 Hz quartz crystal having a load capacitance of 6pF .

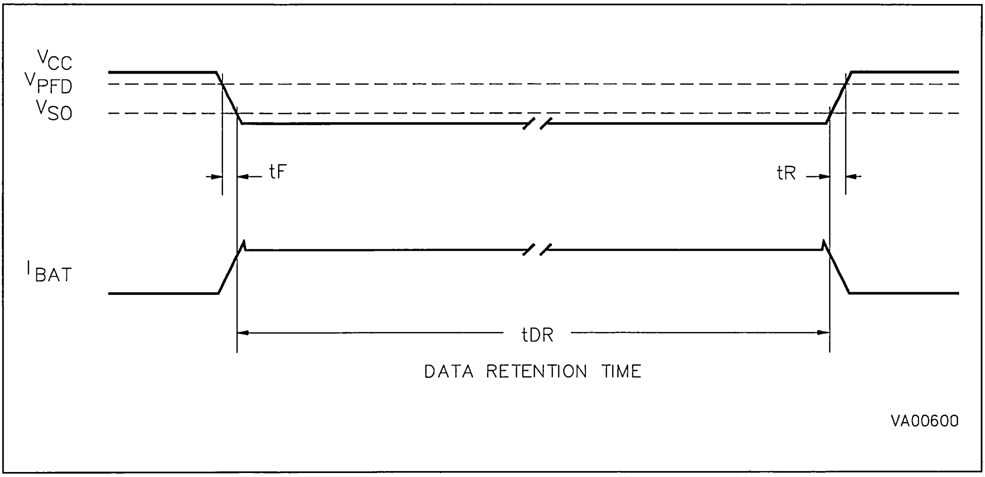
V_{BAT} - The V_{BAT} pin is the battery input for any standard 3V lithium cell or other energy source.

RCLR - The $\overline{\text{RCLR}}$ pin is used to clear (set to logic "1") all 50 bytes of the general purpose RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{\text{RCLR}}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) for a minimum of 100 ms when V_{CC} is applied.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$; V_{CC} min $\leq V_{CC} \leq V_{CC}$ max)

Symbol	Parameter	Min.	Max.	Unit
I_{CC1}	Average V_{CC} Power Supply Current		15	mA
I_{MOT}	Input Current	–1	500	µA
I_{IL}	Input Leakage Current	–1	1	µA
I_{OL}	Output Leakage Current	–5	5	µA
V_{OH}	Output Logic "1" Voltage ($I_{OUT} = -1.0$ mA)	2.4		V
V_{OL}	Output Logic "0" Voltage ($I_{OUT} = 4.0$ mA)		0.4	V
V_{BAT}	Battery Voltage	2.4	3.5	V
I_{BAT}	Battery Current (at $V_{BAT} = 3.0V$, $T_A = 25°C$)		455	nA

Figure 3. Power Up/Down Conditions


VCC
VPFD
VSO
tF
tR
IBAT
tDR
DATA RETENTION TIME
VA00600

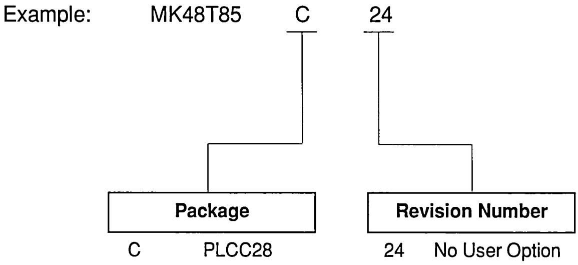
AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing)

Symbol	Parameter	Min.	Max.	Unit
t_F	V_{PFD} to V_{SO} V_{CC} Fall Time	310		µs
t_R	V_{SO} to V_{PFD} V_{CC} Rise Time	100		µs

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points) (0°C ≤ T_A ≤ 70°C)

Symbol	Parameter	Values			Unit
		Min.	Typ.	Max.	
V_{PFD}	Power-fail Deselect Voltage	1.22 V_{BAT}	1.25 VBAT	1.28 V_{BAT}	V
V_{SO}	Battery Back-up Swithover Voltage		V_{BAT}		V

ORDERING INFORMATION


Example: MK48T85 C 24
Package
C PLCC28
Revision Number
24 No User Option

For a list of available options refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

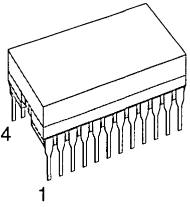
For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK48T87

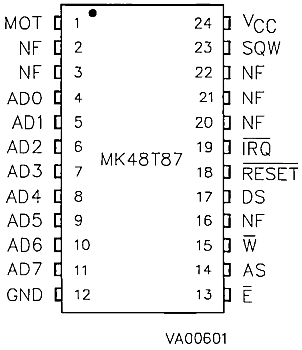
CMOS 64 x 8 ADDRESS/DATA MULTIPLEXED TIMEKEEPER SRAM

- DROP-IN REPLACEMENT FOR PC AT COMPUTER CLOCK/CALENDAR
- TOTALLY NONVOLATILE WITH 10 YEARS OF OPERATION IN THE ABSENCE OF POWER
- SELF-CONTAINED SUBSYSTEM INCLUDES LITHIUM BATTERY, QUARTZ CRYSTAL AND SUPPORT CIRCUITRY
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS:
  - 14 Bytes Of Clock And Control Registers
  - 50 Bytes Of General Purpose RAM
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE:
  - Time-of-day Alarm Once/Second To Once/Day
  - Periodic Rates From 122 µs to 500 ms
  - End Of Clock Update Cycle



PHDIP24 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection



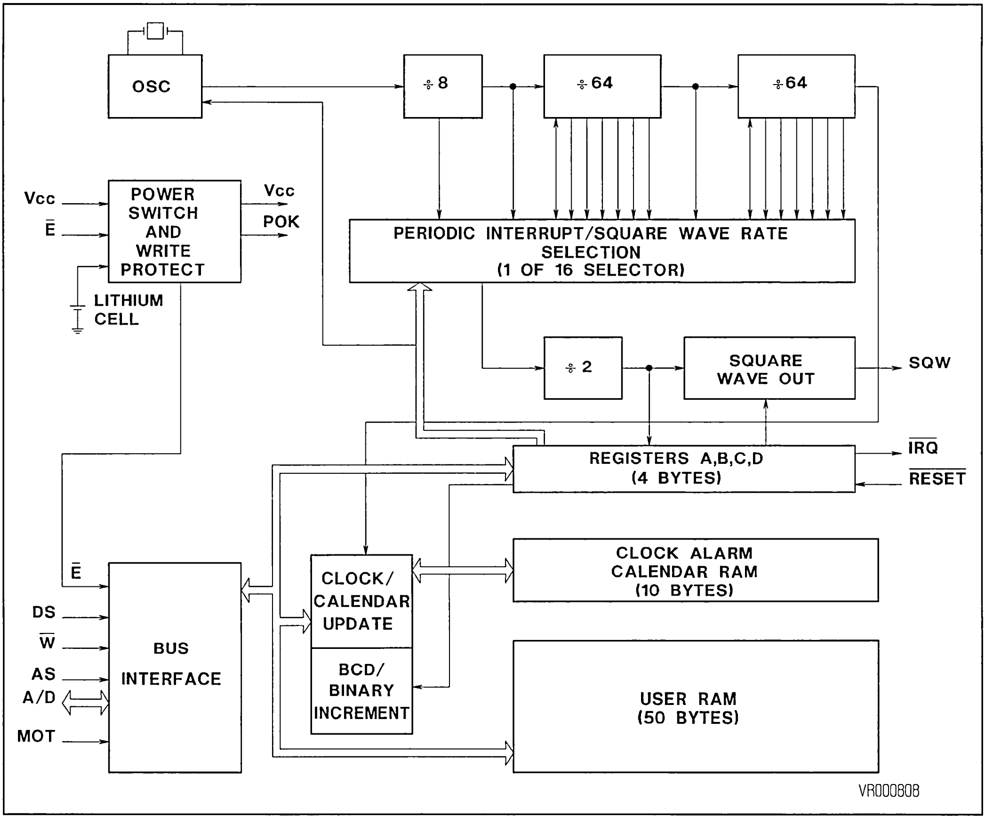
PIN NAMES

AD0 - AD7	Address / Data
V_{CC}/GND	5 Volts/Ground
$\overline{E}$	Chip Select
AS	Address Strobe
$\overline{W}$	Read/Write
SQW	Square Wave Out
MOT	Bus Type Selection

$\overline{IRQ}$	Interrupt Request
$\overline{RESET}$	Reset
DS	Data Strobe
NF	No Function

NF pin serves no function and may be connected to other signals, within Absolute Maximum Ratings, without affecting device operation. The electrical characteristics are the same as the other inputs pins.

Figure 2. Block Diagram


OSC
÷8
÷64
÷64
Vcc
E̅
POWER SWITCH AND WRITE PROTECT
Vcc
POK
LITHIUM CELL
PERIODIC INTERRUPT/SQUARE WAVE RATE SELECTION (1 OF 16 SELECTOR)
÷2
SQUARE WAVE OUT
SQW
REGISTERS A,B,C,D (4 BYTES)
IRQ
RESET
CLOCK ALARM CALENDAR RAM (10 BYTES)
E̅
DS
W̅
AS
A/D
MOT
BUS INTERFACE
CLOCK/ CALENDAR UPDATE
BCD/ BINARY INCREMENT
USER RAM (50 BYTES)
VR000808

DESCRIPTION

The MK48T87 TIMEKEEPER™ RAM is designed to be a compatible replacement for the MC146818 and the DS1287. A lithium energy source, a quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. The MK48T87 is, therefore, a complete subsystem replacing as many as 16 components in a typical application. The functions available to the user include a non-volatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The Real Time Clock/RAM is unique in that the time-of-day and memory are maintained even in the absence of power.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset. This allows sufficient time for V_{CC} to stabilize and gives the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 2 shows the pin connection with the major internal functions of MK48T87 (Real Time Clock/RAM). The following paragraphs describe the function of each pin.

SIGNAL DESCRIPTIONS

GND, V_{CC} - D.C. power is provided to the device on these pins. V_{CC} is the +5 volt input. When V_{CC} is applied and is above V_{PFD}, the device is fully accessible and the data can be written and read. When V_{CC} is below V_{PFD}, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{SO}, the RAM and timekeeper are switched over to an internal Lithium energy source. The timekeeping function maintains an accuracy of 1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ .

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin may be changed by programming Register A. As shown in Table 1, the SQW signal may be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than V_{PFD}.

Table 1. Periodic Interrupt Rate and Square Wave Frequency

Select Bits Register A				t_{PI} Periodic Interrupt Rate	SQW Output Frequency
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus) - Multiplexing the bus reduces the device pin count because address information and data information time share the same signal paths. The addresses are presented during the first portion of the bus cycle and the same pins and signal paths are used for data transfer during the second portion of the cycle. Address/data multiplexing does not slow the access time of the MK48T87 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the MK48T87 latches the address from AD0 to AD5. Valid write data must be present and held stable during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as RD transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the MK48T87.

DS (Data Strobe or Read Input) - The DS/RD pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the MK48T87 is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the MK48T87 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read (RD). RD identifies the time period when the MK48T87 drives the bus with read data. The RD signal is the same definition as the Output Enable ($\overline{\text{G}}$) signal on a typical memory.

W (Read/Write Input) - The $\overline{\text{W}}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, $\overline{\text{W}}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on $\overline{\text{W}}$ while DS is high. A write cycle is indicated when $\overline{\text{W}}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the $\overline{\text{W}}$ signal is an active low signal called WR. In this mode the $\overline{\text{W}}$ pin has the same meaning as the Write Enable signal ($\overline{\text{W}}$) on generic RAMs.

E (Chip Select Input) - The Chip Select signal ($\overline{\text{E}}$) must be asserted low for a bus cycle in which the MK48T87 is to be accessed. $\overline{\text{E}}$ must be kept in the active state during DS and AS for Motorola timing and during RD and $\overline{\text{W}}$ for Intel timing. Bus cycles which take place without asserting $\overline{\text{E}}$ will latch addresses but no access will occur. When V_{CC} is below V_{PFD}, the MK48T87 internally inhibits access cycles by internally disabling the $\overline{\text{E}}$ input. This action protects both the Real Time Clock data and RAM data during power outages.

IRQ (Interrupt Request Output) - The $\overline{\text{IRQ}}$ pin is an active low output of the MK48T87 that may be used as an interrupt input to a processor. The $\overline{\text{IRQ}}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt- enable bit is set. To clear the $\overline{\text{IRQ}}$ pin the processor program normally reads the C register. The $\overline{\text{RESET}}$ pin also clears pending interrupts. When no interrupt conditions are present, the $\overline{\text{IRQ}}$ level is in the high impedance state. Multiple interrupt devices may be connected to an $\overline{\text{IRQ}}$ bus. The $\overline{\text{IRQ}}$ bus is an open drain output and requires an external pull-up resistor.

RESET (Reset Input) - The $\overline{\text{RESET}}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{\text{RESET}}$ pin may be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{\text{RESET}}$ is held low is dependent on the application. However, if $\overline{\text{RESET}}$ is used on power up, the time $\overline{\text{RESET}}$ is low should exceed 200 ms to make sure that the internal timer which controls the MK48T87 on power-up has timed out. When $\overline{\text{RESET}}$ is low and V_{cc} is above V_{PFD}, the following occurs:

A. Periodic Interrupt Enable (PIE) bit is cleared to zero.

B. Alarm Interrupt Enable (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until $\overline{\text{RESET}}$ is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. $\overline{\text{IRQ}}$ pin is in the high impedance state.

I. Square Wave Output Enable (SQWE) bit is cleared to zero.

J. Updated Ended Interrupt Is Cleared To Zero.

In a typical application $\overline{\text{RESET}}$ may be connected to Vcc. This connection will allow the MK48T87 to go in and out of power fail without affecting any of the control registers.

ADDRESS MAP

The Address Map of the MK48T87 is shown in Figure 3. The address map consists of 50 bytes of user RAM, 10 bytes of RAM which contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

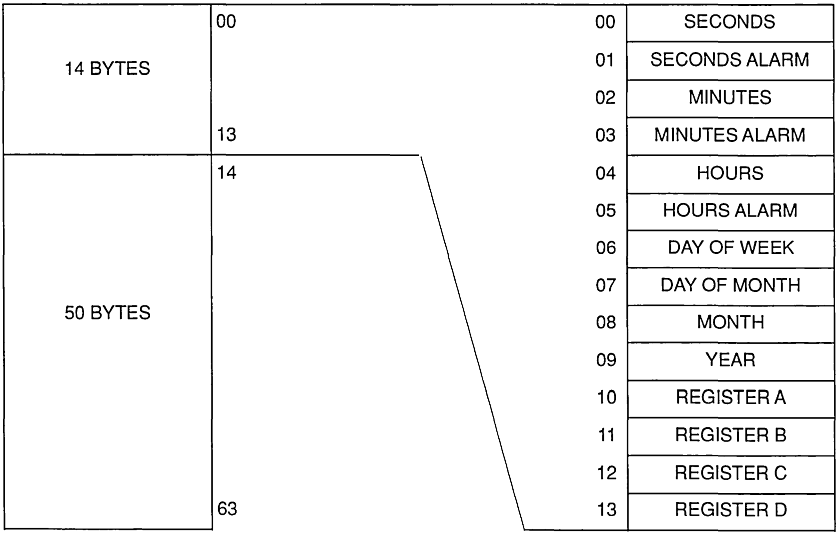
1. Registers C and D are read-only.

2. Bit 7 of Register A is read-only.

3. The high order bit of the seconds byte is read-only.

The contents of four control registers (A,B,C,D) are described in the "Register" section.

Figure 3. Address Map



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes may be either Binary or Binary-Coded (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a Logic one to prevent updates from occuring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (Binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the Binary and BCD formats of the ten time, calendar and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exits that seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

Table 2. Calendar and Alarm Data Modes

Address Location	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
0	SECONDS	00 - 59	00 - 3B	00 - 59
1	SECONDS ALARM	00 - 59	00 - 3B	00 - 59
2	MINUTES	00 - 59	00 - 3B	00 - 59
3	MINUTES ALARM	00 - 59	00 - 3B	00 - 59
4	HOURS - 12hrs MODE	1 - 12	01 - 0C AM, 81 - 8C PM	01 - 12 AM, 81 - 92 PM
	HOURS - 24hrs MODE	0 - 23	00 - 17	00 - 23
5	HOURS ALARM - 12hrs	1 - 12	01 - 0C AM, 81 - 8C PM	01 - 12 AM, 81 - 92 PM
	HOURS ALARM - 24hrs	0 - 23	00 - 17	00 - 23
6	DAY OF THE WEEK (SUNDAY=1)	1 - 7	01 - 07	01 - 07
7	DAY OF THE MONTH	1 - 31	01 - 1F	01 - 31
8	MONTH	1 - 12	01 - 0C	01 - 12
9	YEAR	0 - 99	00 - 63	00 - 99

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a “don't care” state in one or more of the three alarm bytes. The “don't care” code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the “don't care” condition when at Logic 1. An alarm will be generated each hour when the “don't care” bits are set in the hours byte. Similarly, an alarm is generated every minute with “don't care” codes in the hours and minute alarm bytes. The “don't care” codes in all three alarm bytes create an interrupt every second.

NONVOLATILE RAM

The 50 general purpose non-volatile RAM bytes are not dedicated to any special function within the MK48T87. They can be used by the processor program as non-volatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates from 122 µs to 500 ms. The update-ended interrupt may be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a Logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A “0” in an interrupt enable bit prohibits the $\overline{\text{IRQ}}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{\text{IRQ}}$ is immediately set at an active level although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to Logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary.

When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits may be set when reading Register C. Each utilized flag bit should be examined when read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{\text{IRQ}}$ pin is asserted low. $\overline{\text{IRQ}}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{\text{IRQ}}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in Bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the MK48T87. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the MK48T87 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 2. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the IRQ pin to go to an active state from once every 500 ms to once every 122 µs. This function is separate from the alarm interrupt which may be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

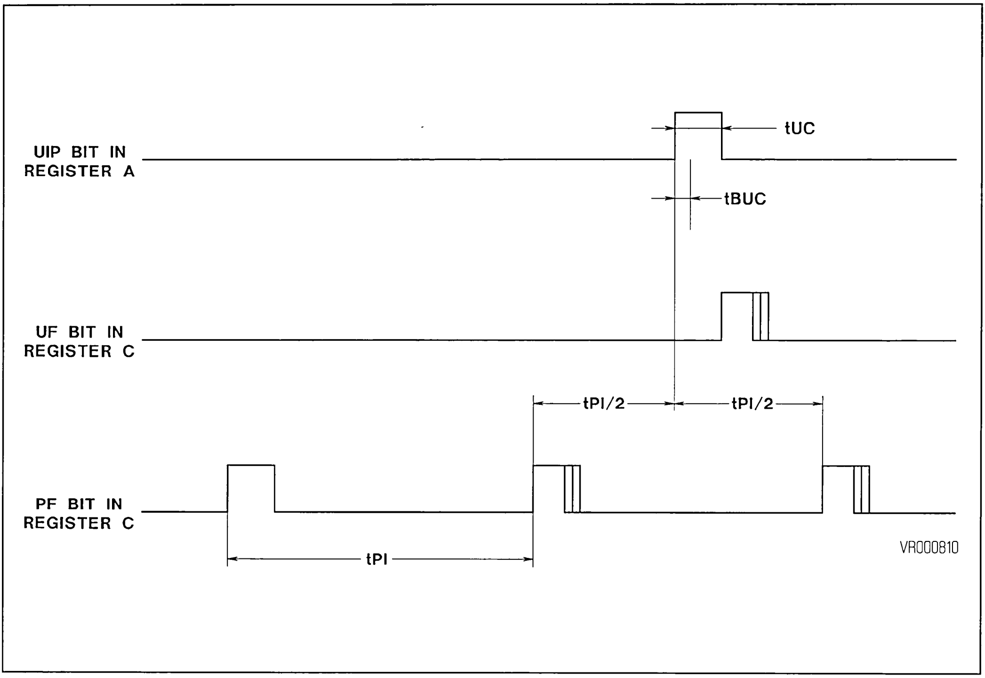
The MK48T87 executes an update cycle once per second regardless of the set bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information are consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues and alarm if a match or if a "don't care" code is present in all three positions.

There are three methods which can be employed to handle access of the Real Time Clock which avoids any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 998 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 µs later. If a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 4). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($T_{PI/2}$+t_{BUC}) to insure that data is not read during the update cycle.

Figure 4. Update Ended and Periodic Interrupt Relationship



Note : t_{PI} = Periodic Interrupt Time interval per table 1.
t_{BUC} = Delay Time Before Update Cycle = 244µs.
t_{UC} = 2ms.

REGISTERS

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update in Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is one, the update transfer will soon occur. When the UIP is a zero, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

DVO, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 1second after a pattern of 010 is written to DV0, DV1 and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;

2. Enable the SQW output pin with the SQWE bit;

3. Enable both at the same time and the same rate; or

4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by RESET or internal functions of the MK48T87.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the IRQ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the IRQ pin low at a rate specified by the RS3 through RS0 bits of Register A. A zero in the PIE bit blocks the IRQ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal MK48T87 functions, but is cleared to zero on RESET.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a one permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a “don’t care” alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The RESET pin clears AIE to zero. The internal functions of the MK48T87 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert IRQ. The RESET pin going low or the SET bit going high clears the UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or RESET. A one in DM signifies binary data and a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is a read/write and is not affected by internal functions or RESET.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF=PIE=1

AF=AIE=1

UF=UIE=1

i.e.,IRQF=PF•PIE+AF•AIE+UF•UIE

Any time the IRQF bit is a one the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are one, the $\overline{\text{IRQ}}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF

A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{\text{IRQ}}$ pin will go low and a one will appear in the IRQF bit. A $\overline{\text{RESET}}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in the UF bit causes the IRQF bit to be a one which will assert the $\overline{\text{IRQ}}$ pin. UF is cleared by reading Register C or a $\overline{\text{RESET}}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

The Valid RAM and Time (VRT) bit is set to the one state by SGS-THOMSON prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{\text{RESET}}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} off, Oscillator off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATIONING CONDITIONS (0°C ≤ T_A ≤ 70°C)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
GND	Ground	0	0	V
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3	V
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V

DC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C; V_{CC} max ≤ V_{CC} ≤ V_{CC} min)

Symbol	Parameter	Min.	Max.	Unit
I_{CC1}	Average V_{CC} Power Supply Current		15	mA
I_{MOT}	Input Current	–1	500	µA
I_{IL}	Input Leakage Current	–1	1	µA
I_{OL}	Output Leakage Current	–5	5	µA
V_{OH}	Output Logic "1" Voltage (I_{OUT} = 1.0mA)	2.4		V
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 4.0mA)		0.4	V

CAPACITANCE (T_A = 25°C)

Symbol	Parameter	Max.	Unit
C_L	Capacitance on all pins (except D/Q)	5	pF
C_{DQ}	Capacitance on DQ pins	7	pF

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 4.5V to 5.5V)

N°	Symbol	Parameter	Min.	Max.	Unit
1	t_{CYC}	Cycle Time	953	D.C.	ns
2	PW_{EL}	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	300		ns
3	PW_{EH}	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	325		ns
4	t_R, t_F	Input Rise and Fall Time		30	ns
8	t_{RWH}	R/$\overline{W}$ Hold Time	10		ns
13	t_{RWS}	R/$\overline{W}$ Set-up Time Before DS/E	80		ns
14	t_{CS}	Chip Select Set-up Time Before DS, $\overline{WR}$ or $\overline{RD}$	25		ns
15	t_{CH}	Chip Select Hold Time	0		ns
18	t_{DHR}	Read Data Hold Time	10	100	ns
21	t_{DWH}	Write Data Hold Time	0		ns
24	t_{ASL}	Muxed Address Valid Time to AS/ALE Fall	50		ns
25	t_{AHL}	Muxed Address Hold Time	20		ns
26	t_{ASD}	Delay Time DS/E to AS/ALE Fall	50		ns
27	PW_{ASH}	Pulse Width AS/ALE High	135		ns
28	t_{ASED}	Delay Time, AS/ALE to DS/E Rise	60		ns
30	t_{DDR}	Output Data Delay Time From DS/E or $\overline{RD}$	20	240	ns
31	t_{DSW}	Data Set-up Time	200		ns
32	t_{RWL}	Reset Pulse Width	5		µs
33	t_{IRDS}	$\overline{IRQ}$ Release from DS		2	µs
34	t_{IRR}	$\overline{IRQ}$ Release from $\overline{RESET}$		2	µs

Figure 5. Bus Timing for Motorola® Interface

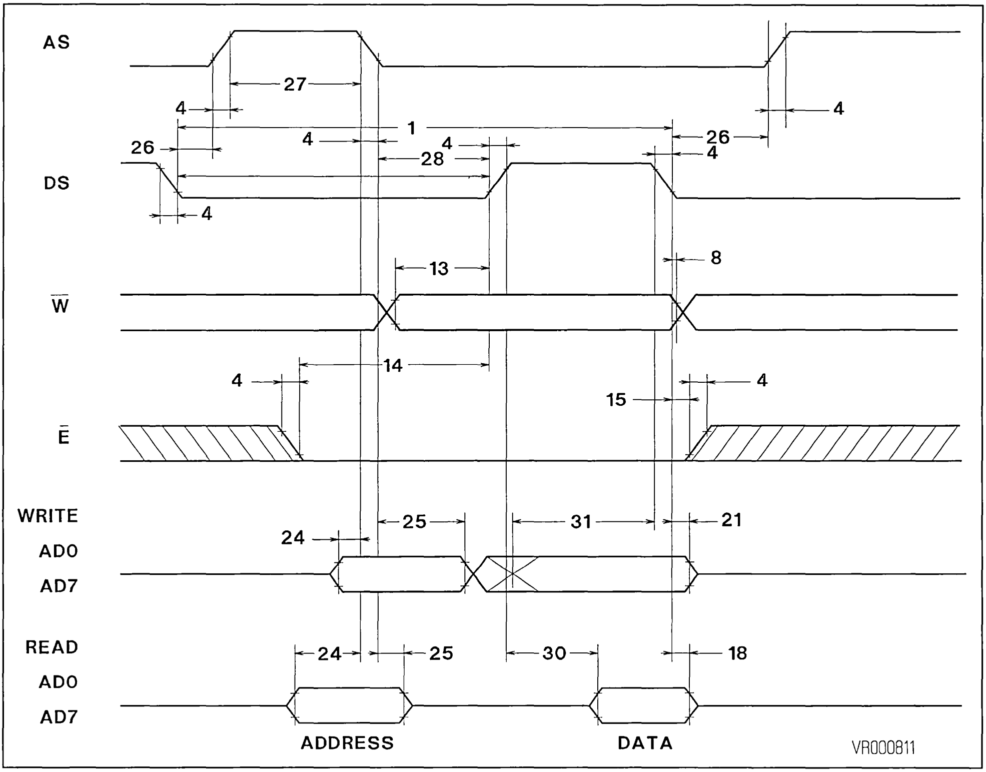

AS
DS
W
E
WRITE
AD0
AD7
READ
AD0
AD7
27
4
1
4
4
26
28
26
4
4
4
13
8
14
4
4
15
25
31
21
24
24
25
30
18
ADDRESS
DATA
VR000811

Figure 6. Bus Timing for Intel® Interface Read Cycle

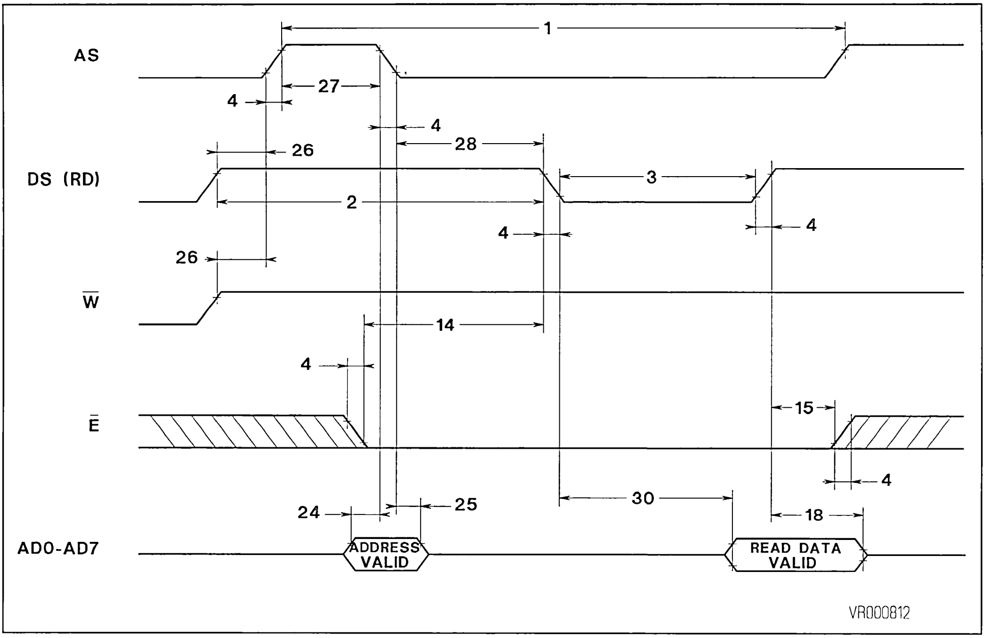

AS
1
27
4
4
28
26
DS (RD)
2
3
4
4
26
W̄
14
4
Ē
15
4
24
25
30
18
AD0-AD7
ADDRESS VALID
READ DATA VALID
VR000812

Figure 7. Bus Timing for Intel Interface Write Cycle

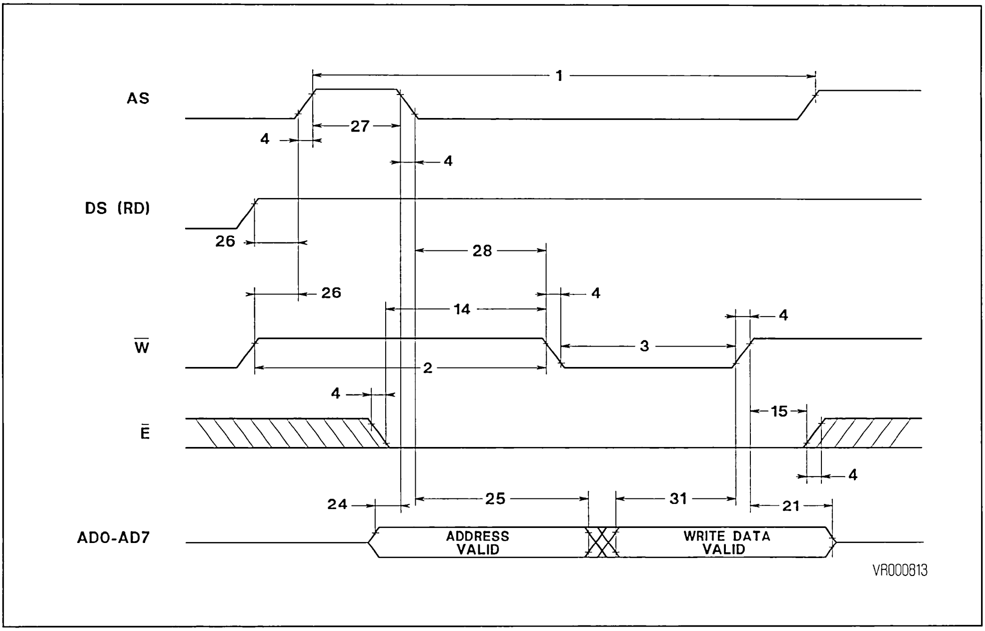

AS
1
27
4
4
DS (RD)
26
28
26
4
14
4
W̄
3
2
4
Ē
15
4
24
25
31
21
AD0-AD7
ADDRESS VALID
WRITE DATA VALID
VR000813

Figure 8. IRQ Release Timing

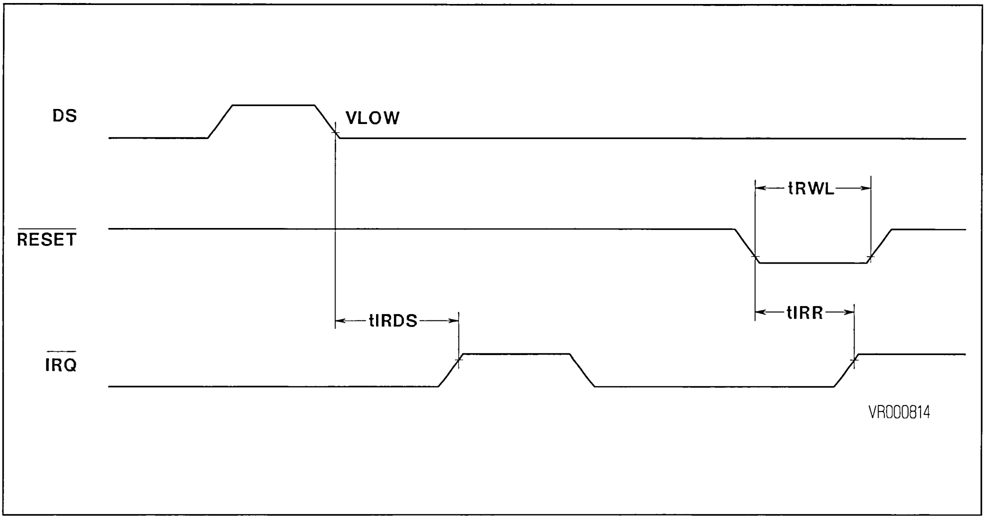
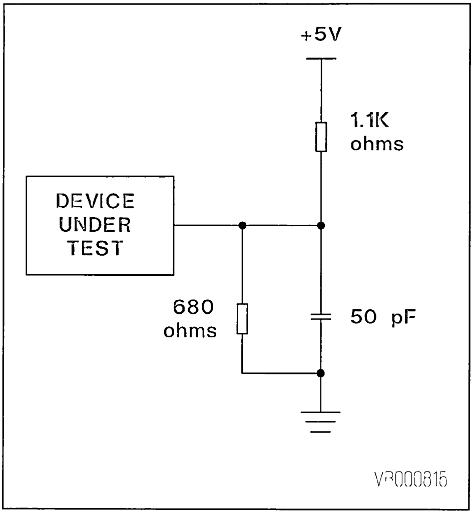

DS
VLOW
tRWL
RESET
tIRDS
tIRR
IRQ
VR000814

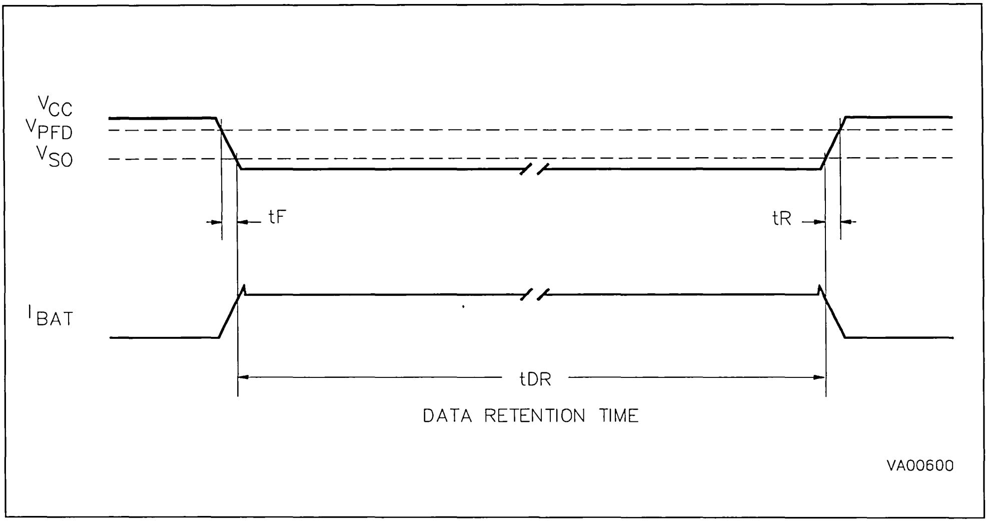
Figure 9. Output Load


+5V
1.1K ohms
DEVICE UNDER TEST
680 ohms
50 pF
VR000815

Notes :

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pull-down of 20K
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin and the SQW pin when each is in the high impedance state
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 9.

Figure 10. Power Up/Down Conditions



AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing) (0°C ≤ T_A ≤ 70°C)

Symbol	Parameter	Min.	Max.	Unit	Notes
t_F	V_{PFD} to V_{SO} V_{CC} Fall Time	310		µs	
t_R	V_{SO} to V_{PFD} V_{CC} Rise Time	100		µs	

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points) (0°C ≤ T_A ≤ 70°C)

Symbol	Parameter	Min.	Typ.	Unit	Notes
V_{PFD}	Power-Fail Deselect Voltage		4.25	V	
V_{SO}	Battery Back-up Switchover Voltage		3.2	V	
t_{DR}	Expected Data Retention Time (Oscillator on)	10		YEARS	1

Note :

1. @ 25°C.

ORDERING INFORMATION

Example: MK48T87 B 24

Package

B PHDIP24

Revision Number

24 No User Option

For a list of available options refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

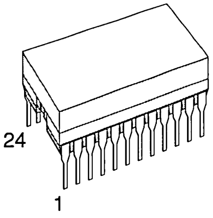
For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK48T87A

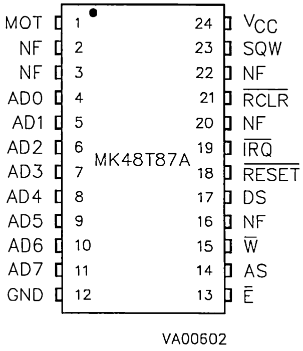
CMOS 64 X 8 ADDRESS/DATA MULTIPLEXED TIMEKEEPER SRAM

- DROP-IN REPLACEMENT FOR PC AT COMPUTER CLOCK/CALENDAR
- TOTALLY NONVOLATILE WITH 10 YEARS OF OPERATION IN THE ABSENCE OF POWER
- SELF-CONTAINED SUBSYSTEM INCLUDES LITHIUM BATTERY, QUARTZ CRYSTAL AND SUPPORT CIRCUITRY
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS:
  - 14 Bytes Of Clock And Control Registers
  - 50 Bytes Of General Purpose RAM
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE:
  - Time-of-day Alarm Once/Second To Once/Day
  - Periodic Rates From 122 µs To 500 ms
  - End Of Clock Update Cycle



PHDIP24 WITH BATTERY TOP HAT (B)

Figure 1. Pin Connection


MOT 1
NF 2
NF 3
AD0 4
AD1 5
AD2 6
AD3 7
AD4 8
AD5 9
AD6 10
AD7 11
GND 12
24 V_{CC}
23 SQW
22 NF
21 $\overline{\text{RCLR}}$
20 NF
19 $\overline{\text{IRQ}}$
18 $\overline{\text{RESET}}$
17 DS
16 NF
15 $\overline{\text{W}}$
14 AS
13 $\overline{\text{E}}$
MK48T87A
VA00602

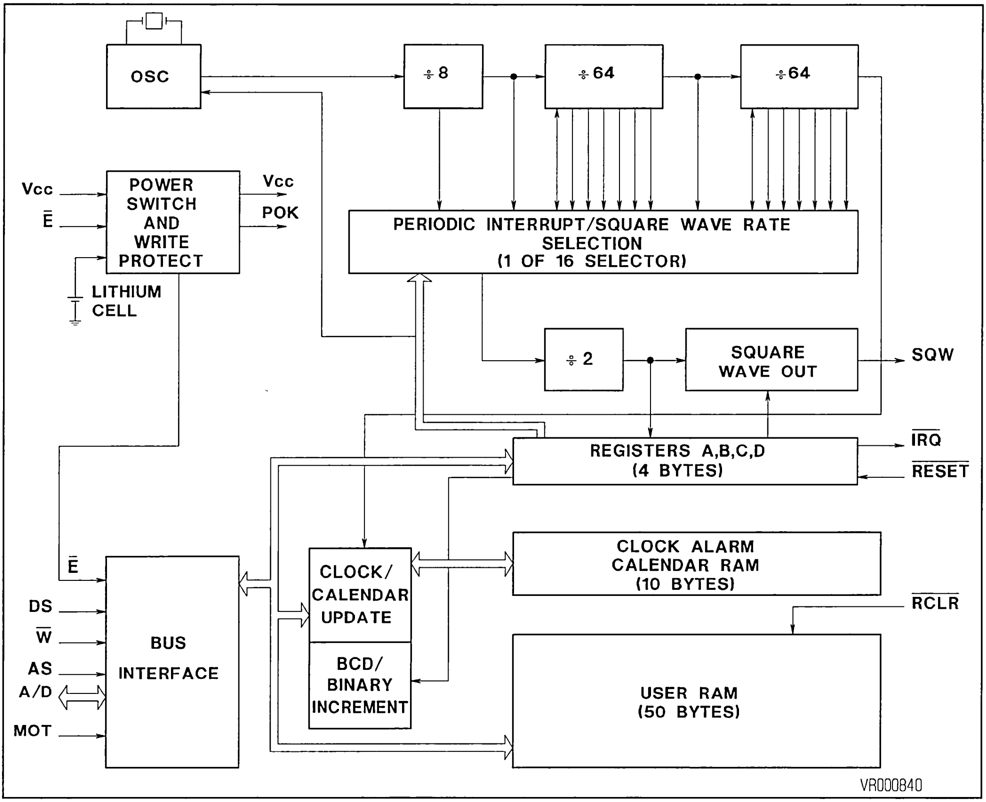
PIN NAMES

AD0 -AD7	Address / Data
V_{CC}/GND	5 Volts/Ground
$\overline{\text{E}}$	Chip Select
AS	Address Strobe
$\overline{\text{W}}$	Read/Write
SQW	Square Wave Out
MOT	Bus Type Selection

$\overline{\text{IRQ}}$	Interrupt Request
$\overline{\text{RESET}}$	Reset
DS	Data Strobe
$\overline{\text{RCLR}}$	RAM Clear
NF	No Function

NF pin serves no function and may be connected to other signals within Absolute Maximum Ratings, without affecting device operation. The electrical characteristics are the same as the other inputs pins.

Figure 2. Block Diagram


OSC
÷8
÷64
÷64
Vcc
Ē
POWER SWITCH AND WRITE PROTECT
Vcc
POK
LITHIUM CELL
PERIODIC INTERRUPT/SQUARE WAVE RATE SELECTION (1 OF 16 SELECTOR)
÷2
SQUARE WAVE OUT
SQW
REGISTERS A,B,C,D (4 BYTES)
IRQ
RESET
CLOCK ALARM CALENDAR RAM (10 BYTES)
RCLR
Ē
DS
W
AS
A/D
MOT
BUS INTERFACE
CLOCK/ CALENDAR UPDATE
BCD/ BINARY INCREMENT
USER RAM (50 BYTES)
VR000840

DESCRIPTION

The MK48T87A TIMEKEEPER™ RAM is designed to be a compatible replacement for the MC146818 and the DS1287A. A lithium energy source, a quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. The MK48T87A is, therefore, a complete subsystem replacing as many as 16 components in a typical application. The functions available to the user include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The Real Time Clock/RAM is unique in that the time-of-day and memory are maintained even in the absence of power.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset, allowing sufficient time for V_{CC} to stabilize and giving the system clock a wake up period so that a valid system reset can be established.

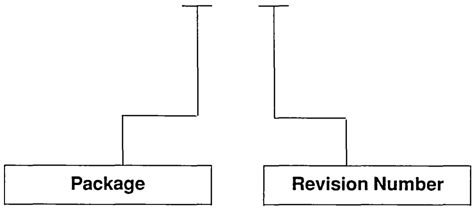
The block diagram in Figure 2 shows the pin connection with the major internal functions of MK48T87A (Real Time Clock/RAM). For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than RCLR, see the MK48T87 datasheet.

SIGNAL DESCRIPTION

RCLR - The $\overline{\text{RCLR}}$ pin is used to clear (set to logic "1") all 50 bytes of general purpose RAM but does not affect the RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{\text{RCLR}}$ must be forced to an input Logic "0" (-0.3 to 0.8 volts) for a minimun of 100 ms when V_{CC} is applied.

ORDERING INFORMATION

Example: MK48T87A B 24



B PHDIP24

24 No User Option

For a list of available options refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK48T02
MK48T12

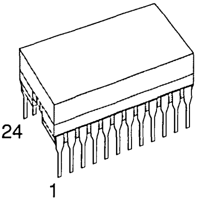
CMOS 2K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- BYTEWIDE RAM-LIKE CLOCK ACCESS.
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES AND SECONDS.
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS.
- PREDICTED WORST CASE BATTERY STORAGE LIFE OF 11 YEARS @ 70°C.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 2K x 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE :
  - MK48T02 4.75V $\geq V_{PFD} \geq$ 4.50V
  - MK48T12 4.50V $\geq V_{PFD} \geq$ 4.20V

DESCRIPTION

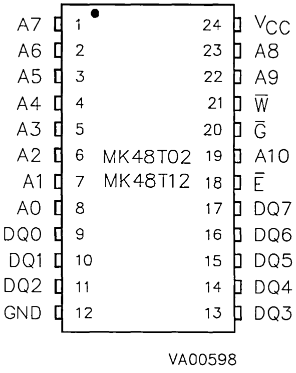
The MK48T02/12 TIMEKEEPER™ RAM combines a 2K x 8 full CMOS SRAM, a BYTEWIDE™ accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery, all in a single plastic DIP package. The MK48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM, such as the 6116 or 5517. It also easily fits into many EPROM AND EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the Clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top: year, month, date, day, hours, minutes, and seconds data in 24 Hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eight location is a Control register. These registers are not the actual clock counters ; they are BiPORT™ read/write Static RAM memory locations. The MK48T02/12 includes a clock control circuit that, once every second, transfers the counters into the BiPORT RAM.



PHDIP24 WITH BATTERY TOP HAT (B)

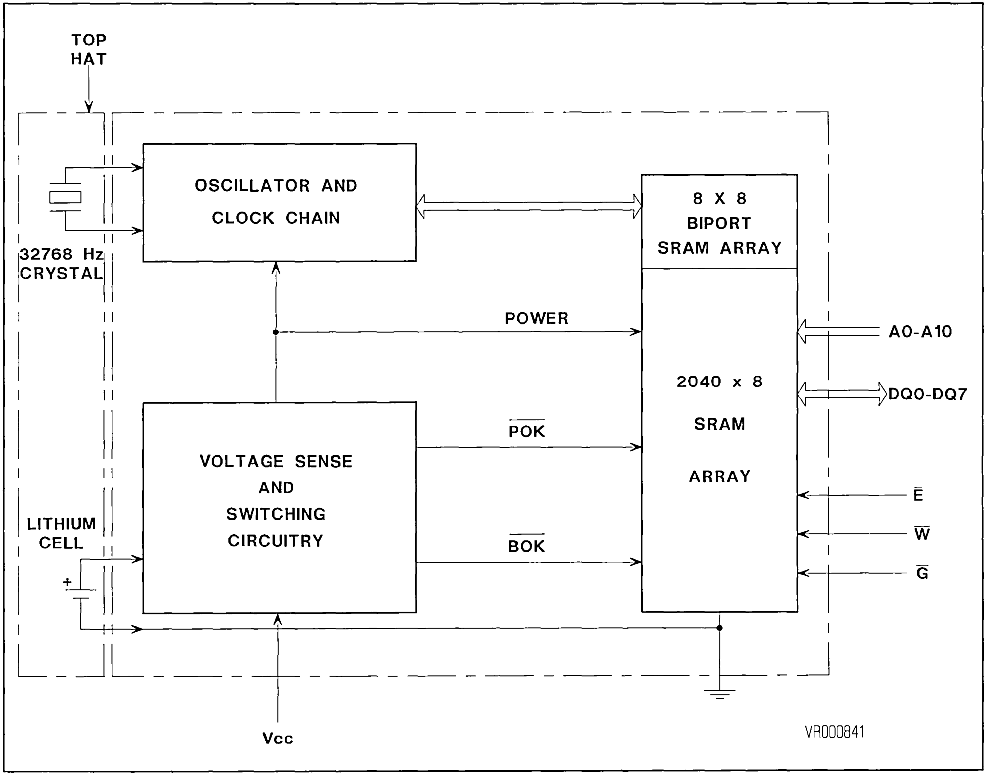
Figure 1. Pin Connection



PIN NAMES

A0-A10	Address Inputs
$\overline{E}$	Chip Enable
GND	Ground
V_{CC}	5 Volts
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 - DQ7	Data Inputs/Outputs

Figure 2. Block Diagram


TOP HAT
32768 Hz CRYSTAL
OSCILLATOR AND CLOCK CHAIN
8 X 8 BIPORT SRAM ARRAY
POWER
A0-A10
2040 x 8 SRAM ARRAY
DQ0-DQ7
VOLTAGE SENSE AND SWITCHING CIRCUITRY
$\overline{POK}$
$\overline{BOK}$
LITHIUM CELL
$\overline{E}$
$\overline{W}$
$\overline{G}$
Vcc
VR000841

DESCRIPTION (Continued)

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T02/12 also has its own Power-fail detect circuit. The circuit deselects the device whenever V_{CC} is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
$<V_{CC(max)}$ $>V_{CC(min)}$	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$<V_{PFD(min)}$ $>V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage On Any Pin Relative to Ground	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to +70	°C
T_{STG}	Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	–40 to +85	°C
P_D	Total Device Power Dissipation	1	W
I_{OUT}	Output Current Per Pin	20	mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability

CAUTION:Negative undershoots below –0.3 volts are not allowed on any pin while in Battery Back-up mode.

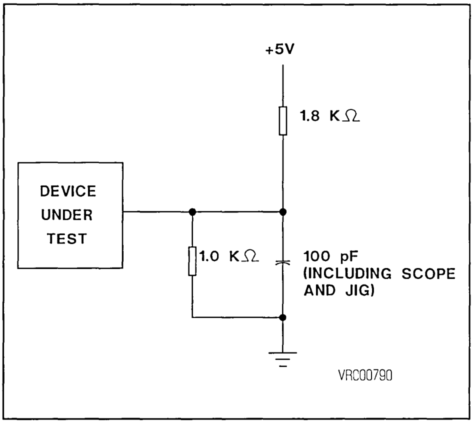
RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48T02)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48T12)	4.5	5.5	V	1
GND	Ground	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	Min.	Max.	Unit	Note
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		5	mA	4
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ –0.2V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1mA)		0.4	V	

EQUIVALENT OUTPUT LOAD DIAGRAM



AC TEST CONDITIONS

Input Levels	0.6V to 2.4V
Transition Times	5ns
Input and Output Timing Reference Levels	0.8V or 2.2V

CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Notes
C_I	Capacitance on all pins (except D/Q)	7 pF	6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	6, 7

Notes :

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volt allowed for up to 10ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with Control Bits set as follows : R = 1 ; W, ST, KS, FT = 0.
5. Measured with $V_{CC} \geq V_I \geq$ GND and outputs deselected
6. Effective capacitance calculated from the equation C = I Δt/ΔV with ΔV = 3 volts and power supply at 5 0V.
7. Measured with outputs deselected

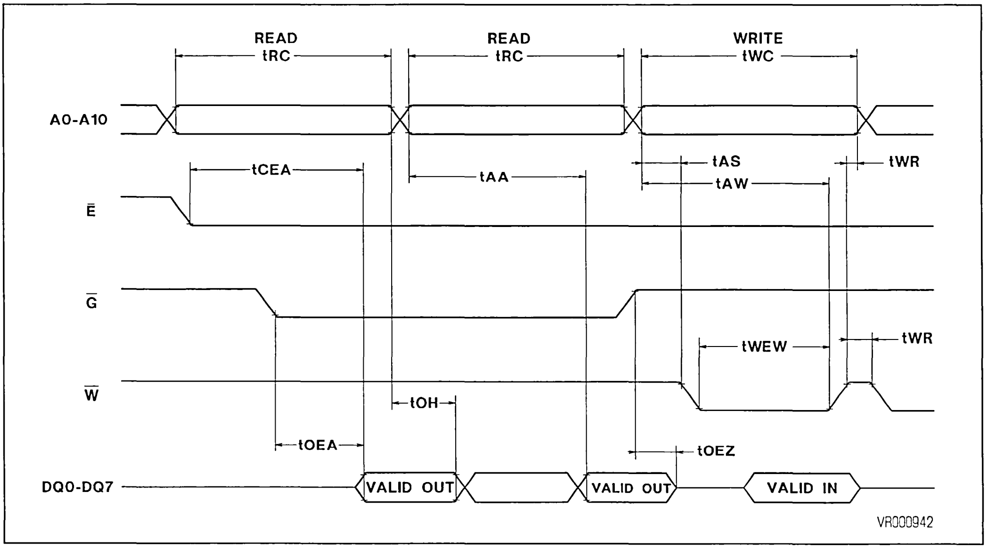
OPERATION

READ MODE

The MK48T02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access (changing Addresses without removing Chip Enable) to any of the 2048 address locations in the static storage array. Valid data will be available at the Data I/O pins within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied.

If $\overline{E}$ or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{CEA}) or at Output Enable Access Time (t_{OEA}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until t_{AA}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold Time (t_{OH}) but will go indeterminant until the next t_{AA}.

Figure 3. Read-Read-Write Timing



AC ELECTRICAL CHARACTERISTICS (Read Cycle Timing)

(0°C ≤ T_A ≤ 70°C; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	48T02-12		48Tx2-15		48Tx2-20		48Tx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

Note : Measured using the Output Load Diagram shown Page 4.

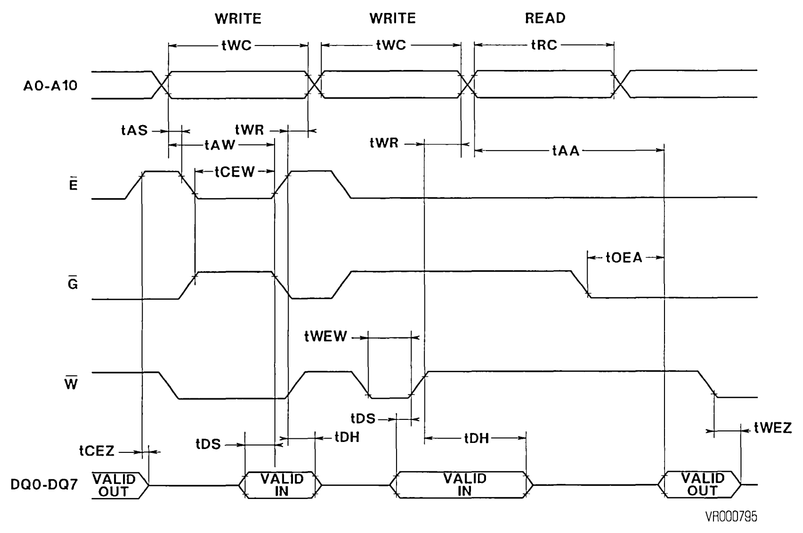
WRITE MODE

The MK48T02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterwards.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stabilizes.

The MK48T02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

Figure 4. Write-Write-Read Timing



AC ELECTRICAL CHARACTERISTICS (Write Cycle Timing)

(0°C ≤ T_A ≤ 70°C; $V_{CC\,max} \geq V_{CC} \geq V_{CC\,min}$)

Symbol	Parameter	48T02-12		48Tx2-15		48Tx2-20		48Tx2-25		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	5		5		5		5		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

CLOCK OPERATIONS

Reading The Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a “1" is written into the "Read" bit, the seventh most significant bit in the Control Register. As long as a “1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt command was issued. All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting The Clock

The eighth bit of the Control register is the “Write” bit. Setting the Write bit to a “1", like the Read Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values the actual TIMEKEEPER counters and allows normal operation to resume. The KS bit, FT bit and the bits marked with zeros in Figure 5 must be written with zeros to allow normal TIMEKEEPER and RAM operation.

Calibrating The Clock

The MK48T02/12 is driven by a quartz crystal controlled oscillator with a nominal frequency of 32768 Hz. The crystal is mounted in the Top Hat along with the battery. A typical MK48T02/12 is accurate within ± 1 minute per month at 25°C without calibration. The devices are tested not to exceed ± 35ppm (Parts Per Million) oscillator frequency error at 25°C, which equates to about 1.53 minute per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T02/12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. The byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit, “1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have

Figure 5. The MK48T02/12 Register Map

ADDRESS	DATA								FUNCTION	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
7FF	-	-	-	-	-	-	-	-	YEAR	00-99
7FE	0	0	0	-	-	-	-	-	MONTH	01-12
7FD	0	0	-	-	-	-	-	-	DATE	01-31
7FC	0	FT	0	0	0	-	-	-	DAY	01-07
7FB	KS	0	-	-	-	-	-	-	HOURS	00-23
7FA	0	-	-	-	-	-	-	-	MINUTES	00-59
7F9	ST	-	-	-	-	-	-	-	SECONDS	00-59
7F8	W	R	S	-	-	-	-	-	CONTROL	

KEY	ST	=	STOP BIT	R	=	READ BIT	FT	=	FREQUENCY TEST
	W	=	WRITE BIT	S	=	SIGN BIT	KS	=	KICK START

one second either shortened or lengthened by 128 oscillator cycles, that is one tick of the divide by 256 stage. If a binary 1 is loaded into the register, only the first two minutes in the 64 minute cycle will be modified ; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding or subtracting 256 oscillator cycles for every 125,829,120 (32768 x 60 x 64) actual oscillator cycles, that is 2.034 ppm of adjustment per calibration step ; giving the user a ±63.07 ppm calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 5.35 seconds per month, which corresponds to a total range of ± 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given MK48T02/12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While this may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple untility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ_0) of the Seconds register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.00512Hz would indicate a +10 ppm (1 – (512/512.00512)) oscillator frequency error, requiring a –5 (000101_2) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must be stable at Address 7F9 when reading the 512 Hz on DQ_0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds register is monitored by holding the MK48T02/12 in an extended read of the Second register, without having the Read bit set. The FT bit MUST be reset to a "0" for normal clock operations to resume.

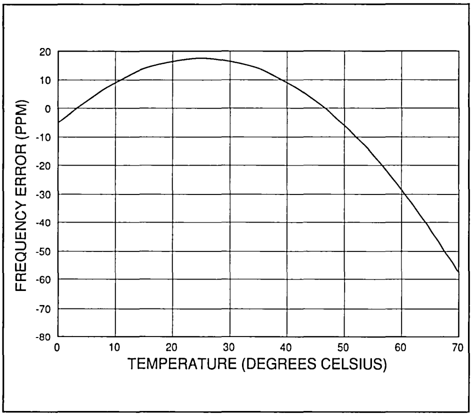
STOPPING AND STARTING THE OSCILLATOR

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB of the Seconds register. Setting it to a "1" stops the oscillator. In order to make the oscillator as stingy with current as possible, the oscillator is designed to require an extra "kick" to begin oscillation again. The extra kick is provided by the Kick Start (KS) bit, the MSB of the Hours register. To start the oscillator, implement the following procedure :

1. Set the Write Bit to "1".
2. Reset the Stop Bit to "0".
3. Set the Kick Start Bit to "1".
4. Reset the Write Bit to "0".
5. Wait 2 seconds.
6. Set the Write Bit to "1".
7. Reset the Kick Start Bit to "0".
8. Set the Correct time and date.
9. Reset the Write Bit to "0".

Note : Leaving the KS bit set will cause the Clock to draw excessive current and will shorten battery life.

Figure 6. Oscillator Frequency VS Temperature



DATA RETENTION MODE

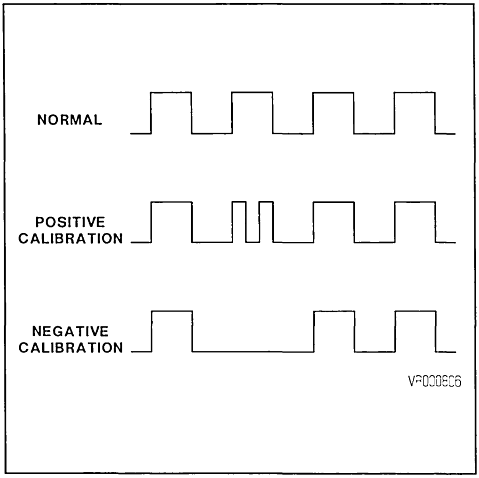
With V_{CC} applied, the MK48T02/12 operates as a conventional BYTEWIDE static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48T02 has a V_{PFD} (max) - V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48T12 has a V_{PFD} (max) - V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note : A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48T02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

Figure 7. Adjusting the Divide by 256 Pulse Train

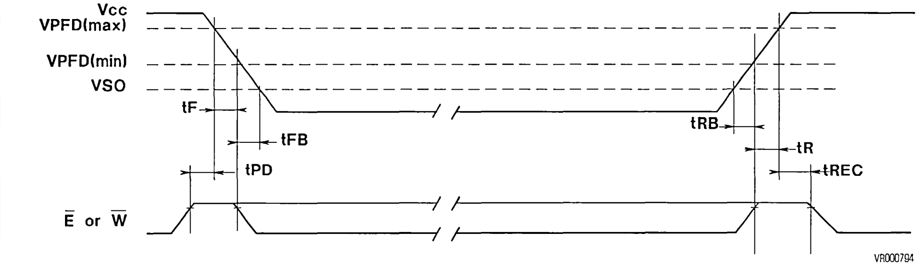


PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T02/12 is expected to ultimately come to an end for one of two reasons : either because it has been discharged while providing current to an external load ; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T02/12 are so low, they can be neglected in practical Storage Life calculations. Therefore, application of V_{CC} or turning off the oscillator can extend the effective Back-up System life.

Figure 8. Power-Down/Power-Up Timing



DC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Trip Point Voltages)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{PFD}	Power-Fail Deselect Voltage (MK48T02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-Fail Deselect Voltage (MK48T12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-Up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (Power-Down/Power-Up Timing)

($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0			ns	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300			µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10			µs	3
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1			µs	
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0			µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2			ms	

Notes :

1. All voltages referenced to GND.
2. V_{PFD} (max) to V_{PFD} (min) fall times of less t_F may result in deselection/write protection not occurring until 50µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data or stop the clock.

PREDICTING STORAGE LIFE

Figure 10 illustrates how temperature affects Storage Life of the MK48T02/12 battery. As long as V_{CC} is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T02/12.

Storage Life predictions presented in Figure 10 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K ohm load resistance.

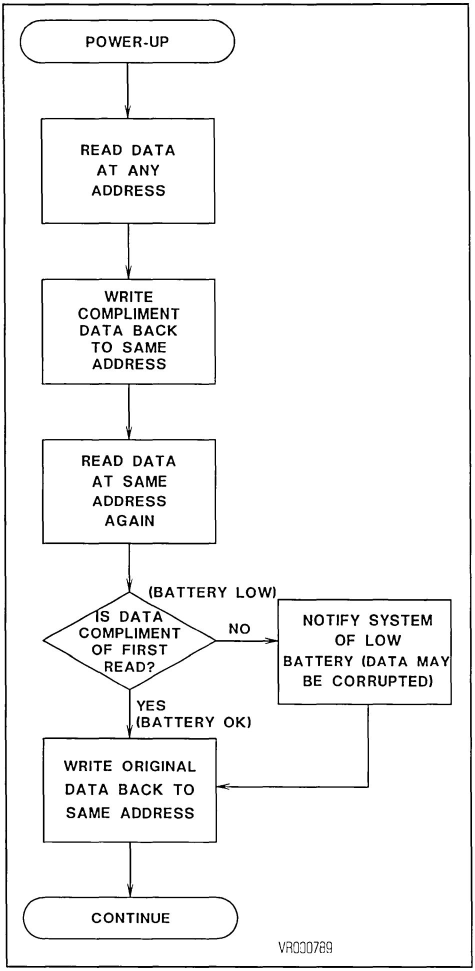
A Special Note : The summary presented in Figure 10 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final ; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 10. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 10 indicates that a particular MK48T02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years ; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The t50% figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48T02/12 is marked with a nine digit manufacturing data code in the form H99XXYYZZ, example: H995B9231 is H - fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia; 9 - tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Figure 9. Checking the $\overline{\text{BOK}}$ Flag Status


POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
(BATTERY LOW)
IS DATA COMPLIMENT OF FIRST READ?
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES (BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE
VR000789

CALCULATING PREDICTED STORAGE LIFE OF THE BATTERY

As Figure 10 indicates, the predicted Storage Life of the battery in the MK48T02/12 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 10. If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\textbf{Predicted Storage Life} = \frac{1}{[(TA_1/TT)/SL_1] + [(TA_2/TT)/SL_2] + \ldots + [(TA_n/TT)/SL_n]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

SL_1, SL_2, SL_n = Predicted Storage Life at Temp 1, Temp 2, etc. (See Figure 10).

EXAMPLE PREDICTED STORAGE LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48T02/12 is exposed to temperatures of 30°C (86°F) or less for 4672 hrs/yr ; temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs/yr ; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

Reading predicted $t_{1\%}$ values from Figure 10 ; SL_1 = 456 yrs., SL_2 = 175 yrs., SL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 3650 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Storage} \geq \frac{1}{[(4672/8760)/456] + [(3650/8760)/175] + [(438/8760)/11.4]}$$

$$\geq 126 \text{ yrs}$$

PREDICTING CAPACITY CONSUMPTION LIFE

The MK48T02/12 internal cell has a nominal capacity of 39mAh. The device places a nominal combined RAM and TIMEKEEPER load of 1.2µA on the internal battery when the clock is running and the device is in Battery Back-up mode. At that rate, the MK48T02/12 will consume the cell's capacity in 32,500 hours, or about 3.7 years. But, as Figure 11 shows, Capacity Consumption can be spread over a much longer period of time.

Naturally, Back-up current varies with temperature. As Figure 12 indicates, the rate of Current Consumption by the MK48T02/12 with the clock running in Battery Back-up mode is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate consumption rates in a given design. As long as ambient temperature is held reasonably constant, expected Capacity Consumption life can be estimated by reading 0% V_{CC} Duty Cycle Capacity Consumption life directly from Figure 12, and dividing by the expected V_{CC} Duty Cycle (i.e. at 25˚C with a 66% Duty Cycle, Capacity Consumption Life = 3.7/(1-.66) = 10.9 years).

If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the same equation provided in the previous Storage Life section should be used to estimate Capacity Consumption life.

Example consumption life calculation

Taking the same cash register/terminal used earlier, let's assume that the high and low temperature periods are the non-operating, Battery Back-up mode periods, and that the register is turned on 10 hours a day seven days per week. The two points of interest on the curves in Figure 12 will be the 25˚C and the 70˚C points.

Reading Capacity Life values from Figure 12 ; CL_1 = 3.7 yrs., CL_2 = 3.96 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 438 hrs./yr.

$$\text{Capacity Life} \geq \frac{1}{[(4672/8760)/3.7] + [(438/8760)/3.96]}$$

$$\geq 6.38 \text{ yrs.}$$

ESTIMATING BACK-UP SYSTEM LIFE

The procedure for estimating Back-up System Life is simple. Pick the lower of the two numbers. In the case calculated in the examples, that would be 6.38 years. The fact is, since either mechanism, Storage Life or Capacity Consumption, can end the system's life, the end is marked by whichever occurs first.

Figure 11. Typical Capacity Consumption Life at 25°C VS. V_{CC} Duty Cycle

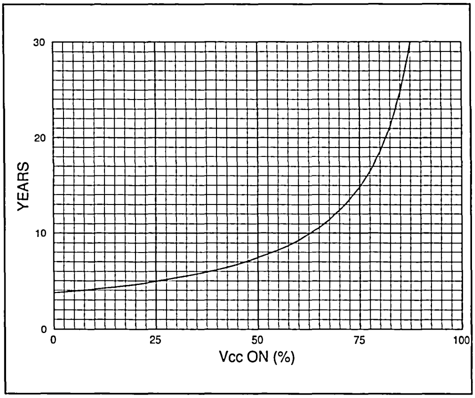


Figure 10. Predicted Battery Storage Life Versus Temperature

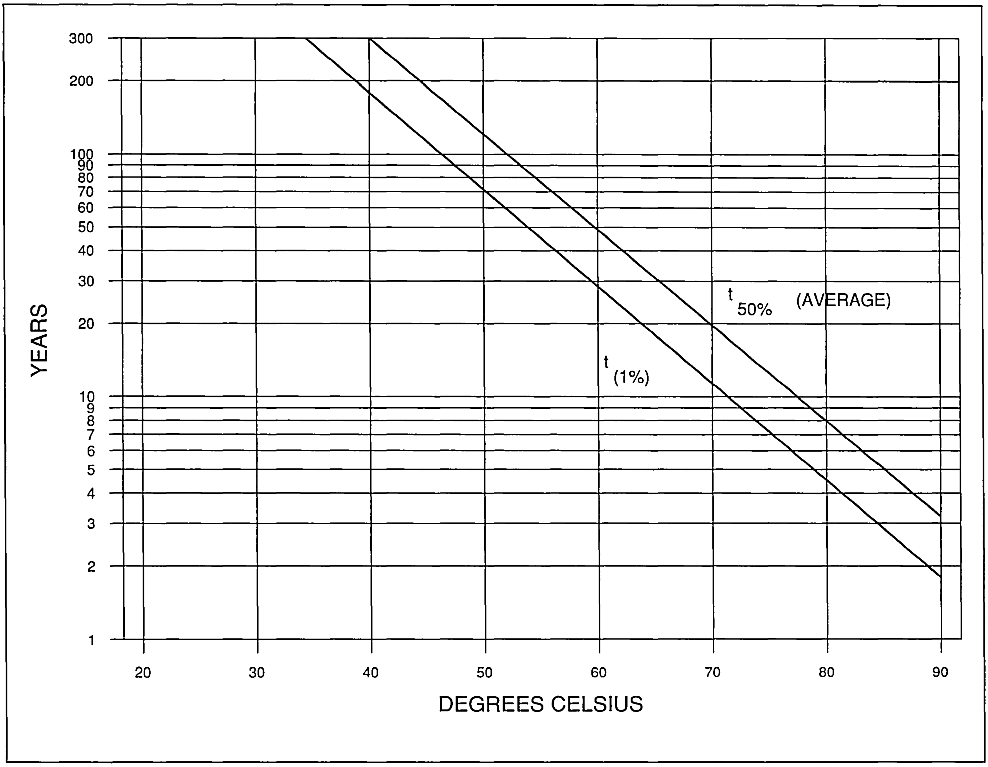
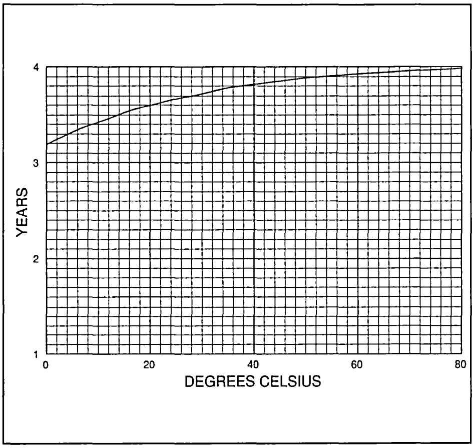


Figure 12. Current Consumption Life over Temperature with 0% V_{CC} Duty Cycle



APPLICATION NOTE :

BINARY TO BCD, AND BCD TO BINARY CONVERSION

The MK48T02/12 presents and accepts TIMEKEEPER data in BCD format. Conversion to or from other formats can be executed in a single line of code, as the following example BASIC program demonstrates.

```
10   REM   BINARY TO BCD
20   DEF   FNA (X) = INT (X/10)*16+X-INT
           (X/10)*10
30   REM   BCD TO BINARY
40   DEF   FNB (X) =  INT (X/16)
           *10+(XAND15)
```

ORDERING INFORMATION

Example: MK48T02 B 12

Package	
B	PHDIP24

Speed	
12	120ns
15	150ns
20	200ns
25	250ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

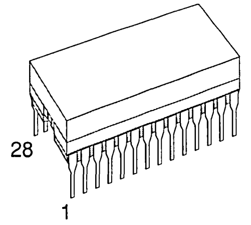
For further information or any aspect of this device, please contact our Sales Office nearest to you.

SGS-THOMSON
MICROELECTRONICS

MK48T08
MK48T18

CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY.
- BYTEWIDE RAM-LIKE CLOCK ACCESS.
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES AND SECONDS.
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS.
- 10 YEARS OF DATA RETENTION IN THE ABSENCE OF POWER.
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K x 8 SRAMS.
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION.
- CHOICE OF TWO WRITE PROTECT VOLTAGES :
  - MK48T08 - 4.50 $\leq V_{PFD} \leq$ 4.75V
  - MK48T18 - 4.20 $\leq V_{PFD} \leq$ 4.50V



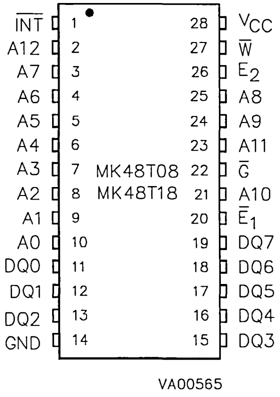
PHDIP28 WITH BATTERY TOP HAT (B)

DESCRIPTION

The MK48T08/18 TIMEKEEPER™ RAM combines an 8K x 8 full CMOS SRAM, a BYTEWIDE™ accessible Real Time Clock, a crystal and a long life lithium carbon mono-fluoride battery in a single plastic DIP package. The MK48T08/18 is a nonvolatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top: year, month, date, day, hour, minutes, and seconds data in 24 hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a control register. These registers are not the actual clock counters; they are BiPORT™ read/write Static RAM memory locations. The MK48T08/18 includes a clock control circuit that, once every second, transfers the counter information into the BiPORT RAM.

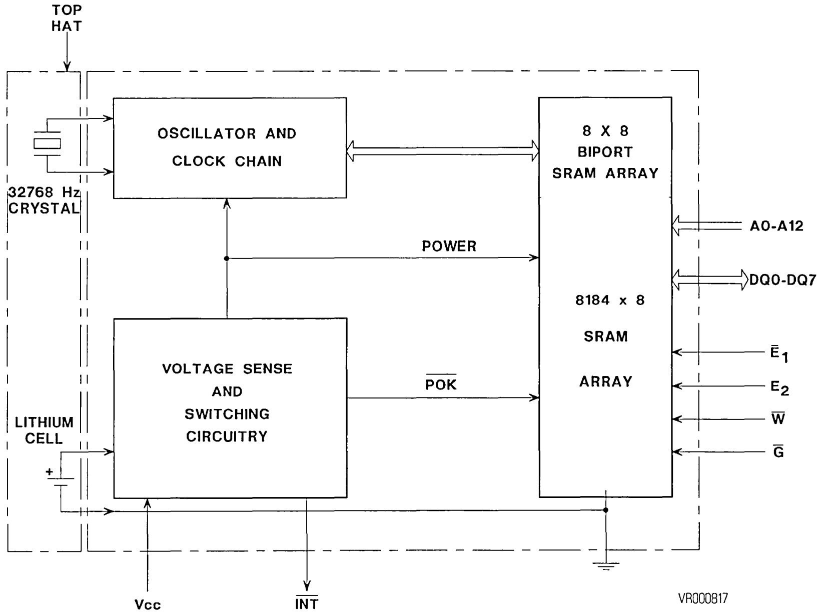
Figure 1. Pin Connections



PIN NAMES

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{\text{INT}}$	Power Fail Interrupt
$\overline{\text{E}}_1$	Chip Enable 1
E_2	Chip Enable 2
$\overline{\text{W}}$	Write Enable
$\overline{\text{G}}$	Output Enable
V_{CC}, GND	5 Volts, Ground

Figure 2. Block Diagram


TOP HAT
32768 Hz CRYSTAL
OSCILLATOR AND CLOCK CHAIN
8 X 8 BIPORT SRAM ARRAY
POWER
8184 x 8 SRAM ARRAY
A0-A12
DQ0-DQ7
$\overline{E}_1$
E_2
$\overline{W}$
$\overline{G}$
VOLTAGE SENSE AND SWITCHING CIRCUITRY
$\overline{POK}$
LITHIUM CELL
+
Vcc
$\overline{INT}$
VR000817

DESCRIPTION (Continued)

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T08/18 also has its own Power-fail Detect circuit. The circuit deselects the device whenever Vcc is below tolerance, providing a high degree of data security in the midst of unpredictable system operations brought on by low Vcc.

TRUTH TABLE

V_{CC}	$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	Mode	DQ	Power
< V_{CC} (max) > V_{CC} (min)	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	X	Deselect	High Z	CMOS Standby
≤ V_{SO}	X	X	X	X	Deselect	High Z	Battery Back-up Mode

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
P_D	Total Power Dissipation	1.0	W
I_{OUT}	Output Current per Pin	20	mA
V_{DD}	Voltage on any Pin Relative to GND	–0.3 to +7.0	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	–40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage (MK48T08)	4.75	5.5	V	1
V_{CC}	Supply Voltage (MK48T18)	4.5	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	–0.3	0.8	V	1, 2

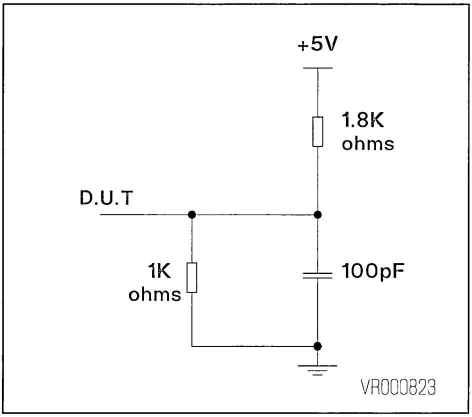
DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$; $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$)		3	mA	6
I_{CC3}	CMOS Standby Current ($\overline{E}_1 = V_{CC}$ –0.2V)		3	mA	4, 6
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	5
I_{OL}	Output Leakage Current	–5	5	µA	5
V_{OH}	Output Logic "1" Voltage (I_{OUT} = –1.0mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +2.1mA)		0.4	V	
V_{INT}	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = +0.5mA)		0.4	V	

AC TEST CONDITIONS

Input Levels	0.0 V to 3.0 V
Transition Times	5 ns
Input and Output Timing Reference Levels	1.5 V

OUTPUT LOAD DIAGRAM



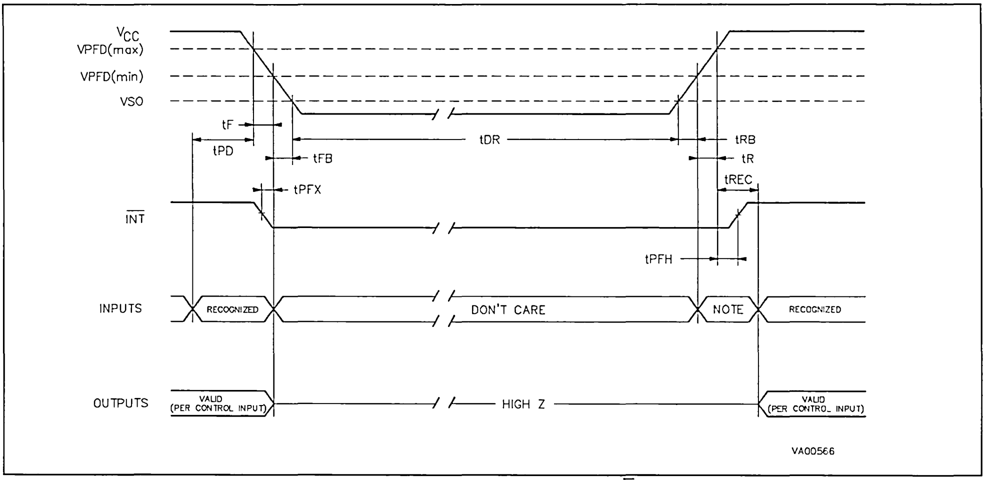
CAPACITANCE

(T_A = 25°C)

Symbol	Parameter	Max.	Unit	Notes
C_I	Capacitance On All Pins (except DQ)	10.0	pF	7
C_Q	Capacitance On DQ Pins	10.0	pF	7, 8

Notes :
1. All voltages referenced to GND.
2 Negative spikes of -1.0 volt allowed for up to 10 ns once per Cycle.
3. I_{CC1} measured with outputs open.
4. 1 mA typical.
5 Measured with $V_{CC} \geq V_I \geq$ GND and outpus deselected.
6. Measured with Control Bits set as follows : R = 1 , W, ST, FT = 0
7. Effective capacitance calculated from the equation C = I Δt/ΔV with ΔV = 3 volts and power supply at 5 0 V
8. Measured with outputs deselected.

Figure 3. Power Down/Up Timing



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}_1$ high or E_2 low as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

AC ELECTRICAL CHARACTERISTICS (Power Up/Down Timing) (0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{PD}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} before Power Down	0		µs	
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs	
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs	
t_{REC}	$\overline{E}_1$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power Up	1		ms	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ High		120	µs	4

DC ELECTRICAL CHARACTERISTICS (Power Up/Down Trip Points) (0°C ≤ T_A ≤ +70°C)

Symbol	Parameter	Value			Units	Notes
		Min.	Typ.	Max.		
V_{PFD}	Power-fail Deselect Voltage (MK48T08)	4.5	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48T18)	4.2	4.3	4.5	V	1
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	1
t_{DR}	Expected Data Retention Time	10			YEARS	5

Notes : 1. All voltages referenced to GND.

2 V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

3 V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

4. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

5. @ 25°C.

READ MODE

The MK48T08/18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}_1$ (Chip Enable 1) is low, and E_2 (Chip Enable 2) is high. The device architecture allows ripple through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} after the last address input signal is stable, providing that the Chip Enable and Output Enable access times are satisfied.

If Chip Enable or Output Enable access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{ELQV}) or at Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by Chip Enable and Output Enable. If the Outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while Chip Enable and Output Enable remain low, output data will remain valid for Output Hold from Address (t_{AXQX}) but will go indeterminate until the next Address Access.

AC ELECTRICAL CHARACTERISTICS (Read Cycle)

($0°C \le T_A \le +70°C$; V_{CC} min $\le V_{CC} \le V_{CC}$ max)

Symbol	Parameter	MK48Tx8-10		MK48Tx8-15		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{E1LQX}	Chip Enable 1 to Q Low-Z	10		10		ns	
t_{E2HQX}	Chip Enable 2 to Q Low-Z	10		10		ns	
t_{AXQX}	Output Hold from Address	5		5		ns	
t_{GLQX}	Output Enable to Q Low-Z	5		5		ns	
t_{AVAV}	Read Cycle Time	100		150		ns	
t_{AVQV}	Address Access Time		100		150	ns	
t_{E1LQV}	Chip Enable 1 Access Time		100		150	ns	
t_{E2HQV}	Chip Enable 2 Access Time		100		150	ns	
t_{GLQV}	Output Enable Access Time		50		75	ns	
t_{E1HQZ}	Chip Enable 1 to Q High-Z		50		75	ns	
t_{E2LQZ}	Chip Enable 2 to Q High-Z		50		75	ns	
t_{GHQZ}	Output Disable to Q High-Z		40		60	ns	

Figure 4. Read Timing n˚ 1 (Address Access)

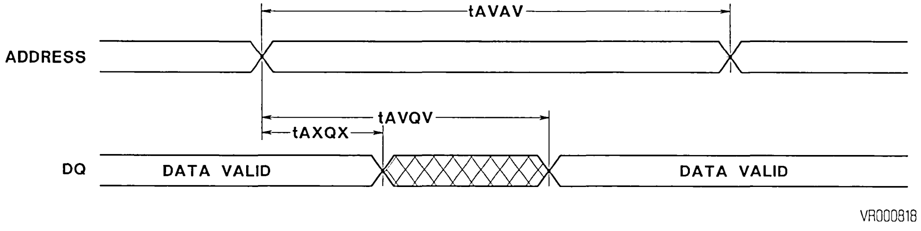
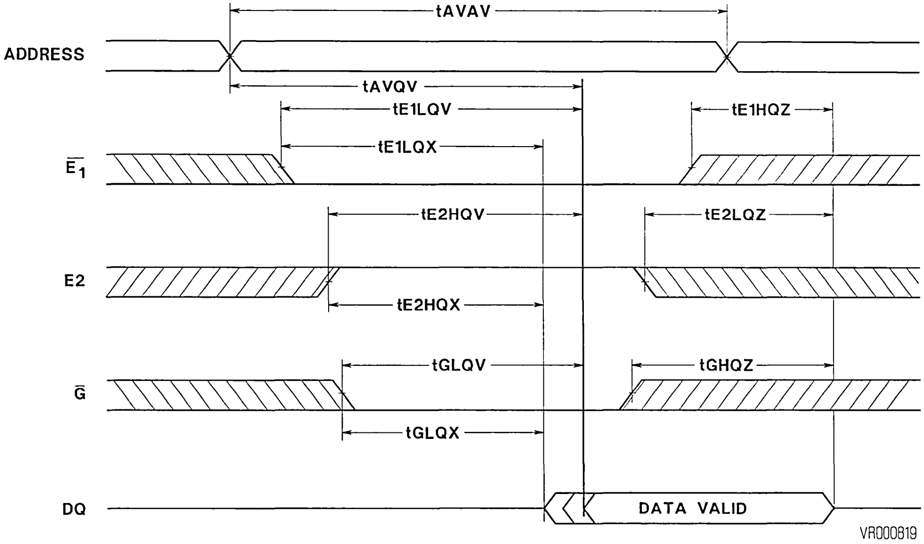

tAVAV
ADDRESS
tAVQV
tAXQX
DQ
DATA VALID
DATA VALID
VR000818

Figure 5. Read Timing n˚ 2


tAVAV
ADDRESS
tAVQV
tE1LQV
tE1HQZ
tE1LQX
$\overline{E_1}$
tE2HQV
tE2LQZ
E2
tE2HQX
tGLQV
tGHQZ
$\overline{G}$
tGLQX
DQ
DATA VALID
VR000819

WRITE MODE

The MK48T08/18 is in the Write Mode whenever Write Enable and Chip Enable are active. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}_1$ or rising edge of E_2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}_1$, or the falling edge of E_2. The addresses must be held valid throughout the cycle. $\overline{E}_1$ or $\overline{W}$ must return high or E_2 low for minimum of t_{E1HAX} or t_{E2LAX} prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

AC ELECTRICAL CHARACTERISTICS (Write Cycle)

(0°C ≤ T_A ≤ +70°C; V_{CC} min ≤ V_{CC} ≤ V_{CC} max)

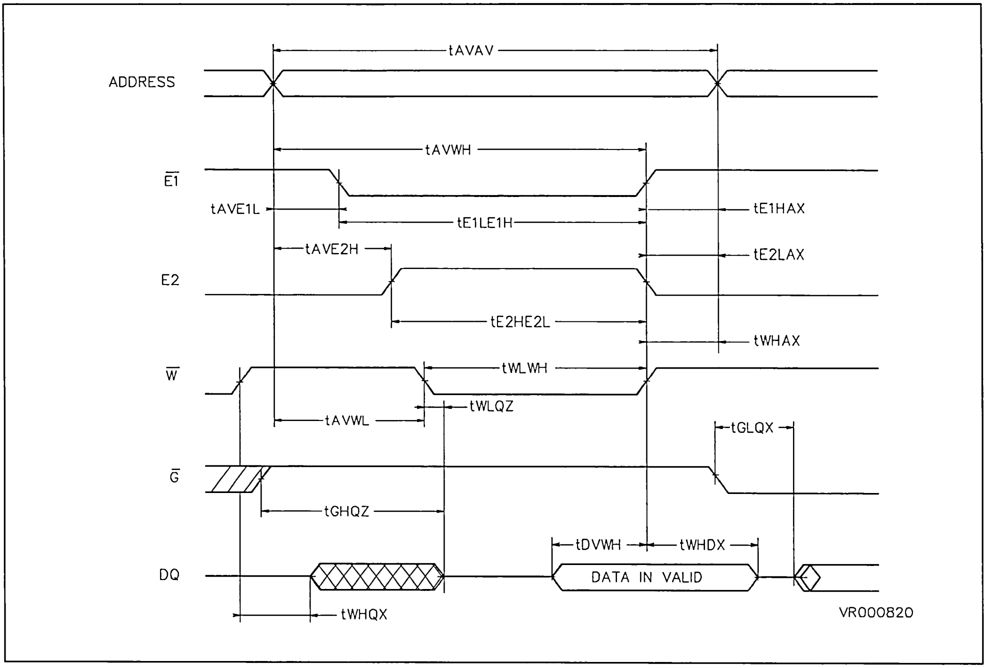
Symbol	Parameter	MK48Tx8-10		MK48Tx8-15		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AVWL}	Address Set-Up Time to $\overline{W}$ Low	0		0		ns	
t_{AVE1L}	Address Set-Up Time to Chip Enable Active	0		0		ns	
t_{AVE2H}		0		0		ns	
t_{E1HAX}	Write Recovery from Chip Enable (Address Hold Time)	10		10		ns	2
t_{E2LAX}		10		10		ns	2
t_{WHDX}	Data Hold Time	5		5		ns	1, 2
t_{AVAV}	Write Cycle Time	100		150		ns	
t_{AVWH}	Address Valid to $\overline{W}$ High	80		130		ns	
t_{WLWH}	Write Pulse Width	80		100		ns	
t_{WHAX}	Address Hold after End of Write	10		10		ns	1
t_{E1LE1H}	Chip Enable Active to End of Write	80		130		ns	2
t_{E2HE2L}		80		130		ns	2
t_{DVWH}	Data Valid to End of Write	50		70		ns	1, 2
t_{WHQX}	End of Write to Q Low-Z	10		10		ns	
t_{WLQZ}	$\overline{W}$ Low to Q High-Z		50		75	ns	

Notes:

1 In a $\overline{W}$ Controlled Cyle

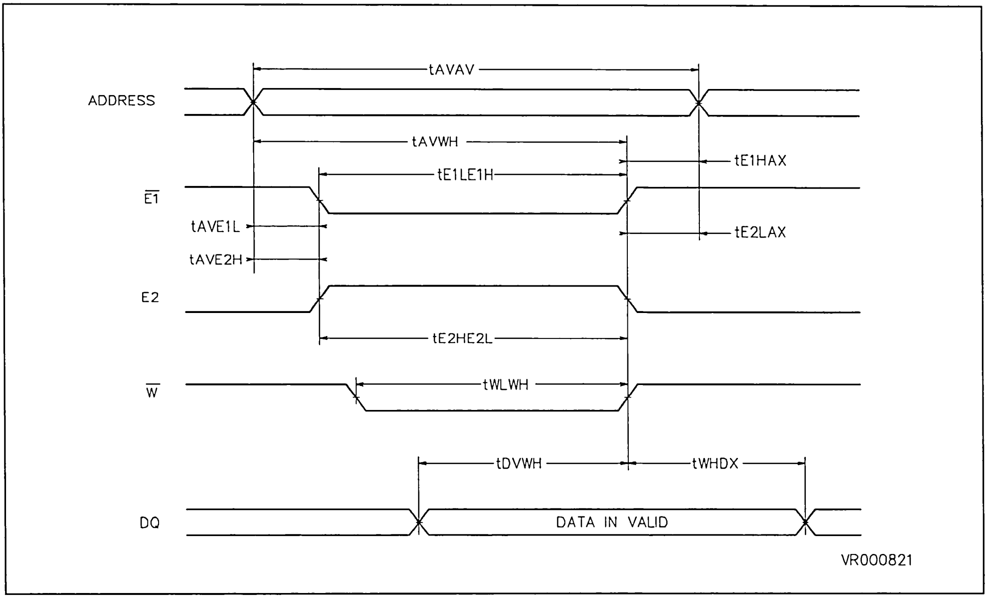
2. In a $\overline{E}_1$, E_2 Controlled Cycle

Figure 6. Write Control Write Cycle Timing



tAVAV
ADDRESS
tAVWH
E1
tAVE1L
tE1LE1H
tE1HAX
tAVE2H
tE2LAX
E2
tE2HE2L
tWHAX
W
tWLWH
tWLQZ
tAVWL
tGLQX
G
tGHQZ
tDVWH
tWHDX
DQ
DATA IN VALID
tWHQX
VR000820

Figure 7. Chip Enable Control Write Cycle Timing



tAVAV
ADDRESS
tAVWH
tE1HAX
tE1LE1H
E1
tAVE1L
tE2LAX
tAVE2H
E2
tE2HE2L
W
tWLWH
tDVWH
tWHDX
DQ
DATA IN VALID
VR000821

DATA RETENTION MODE

With V_{CC} applied, the MK48T08/18 operates as a conventional BYTEWIDE Static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(Max), V_{PFD}(Min) window.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(Min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The MK48T08/18 may respond to transient noise spikes on Vcc that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(Max). Caution should be taken to keep $\overline{E}_1$ high or E_2 low as Vcc rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

POWER FAIL INTERRUPT

The MK48T08/18 continuously monitors V_{CC}. When V_{CC} falls to the power-fail detect trip point of the MK48T08/18 an interrupt is immediately generated. An internal clock provides a delay no less than 10 µs but no greater than 40 µs before automatically deselecting the MK48T08/18. The $\overline{INT}$ pin is an open drain ouput and requires an external pull up resistor.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T08/18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying Vcc or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T08/18 are so low, they can be neglected in practical Storage Life calculations.Therefore, application of Vcc or turning off the oscillator can extend the effective Back-up System life.

PREDICTING STORAGE LIFE

Figure 8 illustrates how temperature affects Storage Life of the MK48T08/18 battery. The life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T08/18.

Storage Life predictions presented in Figure 8 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K load resistance.

Two end of life curves are presented in Figure 8. The are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 8 indicates that a particular MK48T08,T18 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience a battery failure within 11 years; 50% of them can be expected to experience a failure within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Each MK48T08/18 is marked with a nine digit manufacturing date code in the form H99XXYYZZ, example: H995B9231 is H - fabricated in Carrollton, TX; 9 - assembled in Muar, Malaysia;; 9 - tested in Muar, Malaysia; 5B - lot designator; 9231 - assembled in the year 1992, work week 31.

Calculating Predicted Storage Life of the Battery

As Figure 8 indicates, the predicted Storage Life of the battery in the MK48T08/18 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 8. If the MK48T08/18 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = 1 / \{ [(TA_1 / TT) / SL_1] + [(TA_2 / TT) / SL_2] + ...+ [(TA_N / TT) / SL_N] \}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + ... + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, etc. (See Figure 8)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T08/18 is exposed to temperatures of 55°C or less for 8322 hrs./yr.; and temperatures greater than 60°C, but less than 70°C, for the remaining 438 hrs./yr.

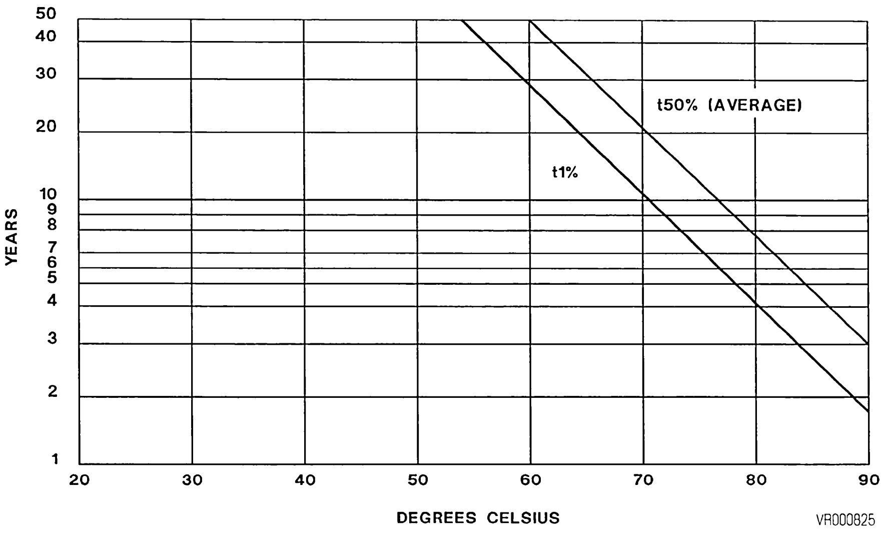
Reading Predicted $t_{1\%}$ values from Figure 8; SL_1 = 41 yrs., SL_2 = 11.4 yrs.,

Total Time (TT) = 8760 hrs./yr. TA_1 = 8322 hrs./yr. TA_2 = 438 hrs./yr. .

$$\text{Predicted Typical Storage Life} \geq 1 / \{ [(8322 / 8760) / 41] + [(438 / 8760) / 11.4]$$

Predicted Typical Storage Life ≥ 36 years

Figure 8. Predicted Battery Storage Life Versus Temperature



Calculating Predicted Capacity Consumption

The MK48T08/18 internal cell has a nominal capacity of 39mAh.The device places a nominal RAM and TIMEKEEPER load of less than 445nA at room temperature. At this rate, the Capacity Consumption life is 39E-3/445E-9=87640 hours or about 10 Years.The Capacity Consumption life can be extended by applying Vcc or turning off the oscillator. For example, if the oscillator runs 100% of the time but Vcc is applied 60% of the time, the Capacity Consumption life is 10/(1-.6) = 25 years.

Estimated Back-up System Life

Since either Storage or Capacity Consumption can end the Battery's life, System Life is marked by which-ever occurs first.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counter, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a “1" is written into the ”Read" bit, the seventh bit in the Control Register. As long as a “1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is the day, date, and time that were current at the moment the Halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a “0".

Setting the Clock

The eighth bit of the Control register is the “Write" bit. Setting the Write bit to a “1", like the Read bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a ”0" then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume.

Stopping and Starting the Oscillator

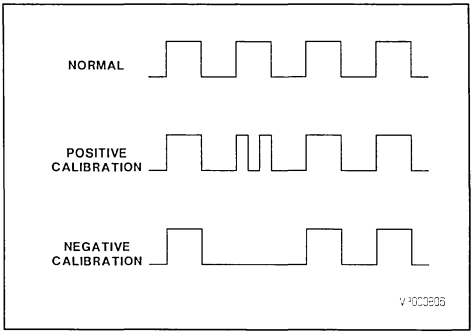
The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The “Stop" bit is the MSB for the Seconds Register. Setting it to a “1" stops the oscillator. The MK48T08/18 is shipped from SGS-Thomson with the ”Stop" bit set to a “1". When reset to a ”0", the MK48T08/18 oscillator starts within 3 seconds typically. Because of this delay, it is recommended to start the oscillator prior to setting the time.

Figure 9. The MK48T08/18 Register Map

Address	Data								Function/Range BCD Format	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1FFF									Year	00-99
1FFE	0	0	0						Month	01-12
1FFD	0	0							Date	01-31
1FFC	0	FT	0	0	0				Day	01-07
1FFB	0	0							Hour	00-23
1FFA	0								Minutes	00-59
1FF9	ST								Seconds	00-59
1FF8	W	R	S						Control	

KEYS : **S** = SIGN BIT **FT** = FREQUENCY TEST BIT **R** = READ BIT
W = WRITE BIT **ST** = STOP BIT **0** = MUST BE WRITTEN TO 0

Figure 10.



Calibrating the Clock

The MK48T08/18 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T08/18 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 11 shows the frequency error that can be expected at various temperatures. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T08/18 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 10. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary "1" is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

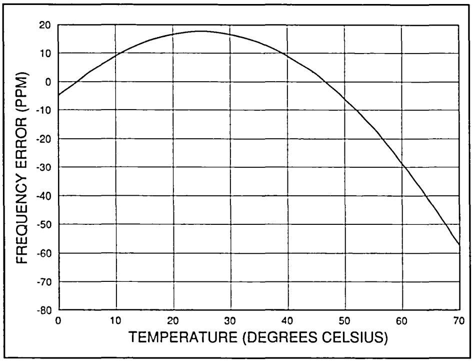
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or -2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given MK48T08/18 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

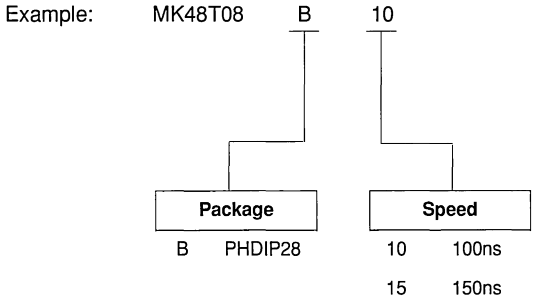
The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a "1", and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 1FF9 when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the MK48T08/18 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to "0" for normal clock operations to resume.

Figure 11. Frequency Error



ORDERING INFORMATION


Example:
MK48T08
B
10
Package
B PHDIP28
Speed
10 100ns
15 150ns

For a list of available options of Package and Speed refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information or any aspect of this device, please contact our Sales Office nearest to you.

APPLICATION NOTES

SGS-THOMSON
MICROELECTRONICS

APPLICATION NOTE

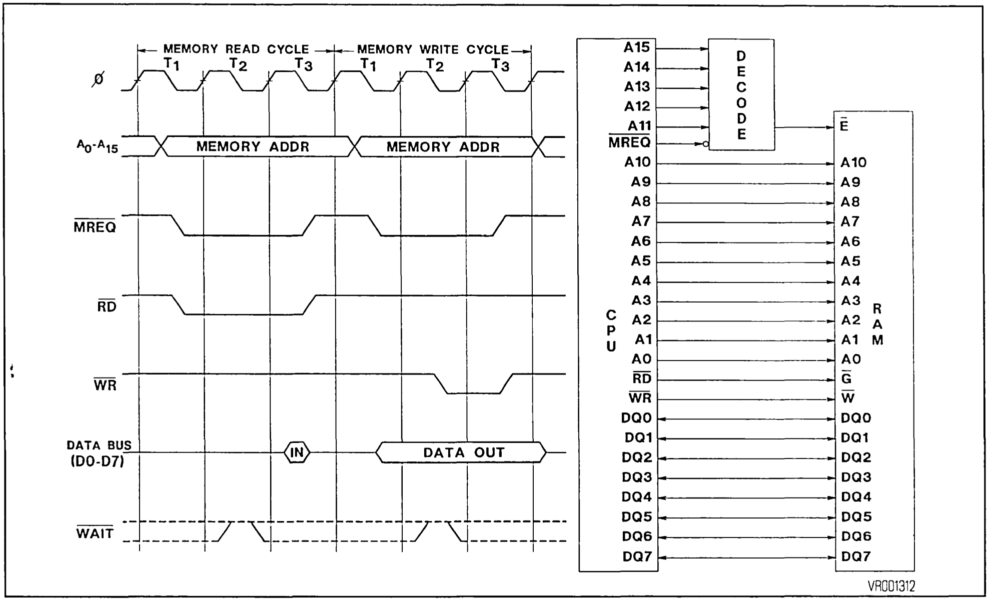
REPLACING EEPROM WITH ZEROPOWER

Currently there are two approaches for implementing non-volatile memory that can be electrically altered within the system. The first is EEPROM (electrically erasable programmable read only memory). The second is battery backed-up RAM. Many misconceptions about battery backed-up RAMs have swayed system designers away from this technology into using EEPROMs with lower performance specifications. All is not lost however, the ZEROPOWER™ technology developed by SGS THOMSON Microelectronics provides a totally integrated approach to battery backed-up RAMs, which in most cases can provide direct replacement of EEPROMs with an added advantage of upgrading system performance.

First let's clear the air about the misconceptions concerning battery backed-up RAM. The integration of a long life lithium cell and the low standby current of CMOS RAMs have made possible data retention times that typically extend beyond ten years. Periodic replacement of batteries or battery charging circuits are no longer necessary. Power fail detection and switching circuitry can be integrated into the same package along with RAM and a small button lithium cell making a complete battery backed-up system that fits into the same socket as conventional RAM. This system in a DIP (dual in-line package) has been invented and trademarked as ZEROPOWER technology by SGS-THOMSON. Extensive reliability studies of the ZEROPOWER technology have been undertaken at SGS-THOMSON which demonstrate a highly reliable approach to non-volatile memory.

Because microprocessors are designed to interface to RAMs, a ZEROPOWER RAM provides the ideal replacement for conventional RAM. Figure 1 shows a typical output timing and interface of an 8 bit microprocessor (Z80). RAM interface can be made by decoding $\overline{\text{MREQ}}$ and address information for $\overline{\text{E}}$, connecting $\overline{\text{RD}}$ to $\overline{\text{G}}$, and connecting $\overline{\text{WR}}$ to $\overline{\text{R}}$.

Figure 1. Z80 Timing



MEMORY READ CYCLE
MEMORY WRITE CYCLE
T1
T2
T3
T1
T2
T3
Ø
A0-A15
MEMORY ADDR
MEMORY ADDR
MREQ
RD
WR
DATA BUS (D0-D7)
IN
DATA OUT
WAIT
CPU
A15
A14
A13
A12
A11
MREQ
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
RD
WR
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DECODE
RAM
E
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
G
W
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
VR001312

EEPROMs, on the other hand, require some modification to the write cycle. This modification can be as simple as adding wait cycles until a write to the EEPROM is completed. In this case direct replacement with a ZEROPOWER RAM is possible. The wait cycles can be left in or eliminated to improve performance.

Some early versions of EEPROMs (2816 without any suffix), however, require a 21 volt VPP signal. This type of EEPROM is programmed the same way conventional EPROMS are programmed. The only difference being that both "ones" and "zeros" can be programmed not just "zeros". Figure 2 shows how complicated interface to this type of EEPROM can be. Replacement with a ZEROPOWER RAM can be accomplished by eliminating almost all of the external circuitry. In the example shown in Figure 2 only the inverter E is required for interface to a ZEROPOWER RAM. For interface to a ZEROPOWER RAM the output of inverter $\overline{E}$ should be connected to $\overline{G}$, and $\overline{WR}$ should be connected directly to $\overline{W}$ on the ZEROPOWER RAM.

In contrast, current technology EEPROMs are 5 volts only. There are two popular types of EEPROMs in production today. The are referred to as latched and timer EEPROMs. Latched EEPROMs latch both data and address on the falling (beginning) edge of the write pulse. Although addresses and data are allowed to change before the completion of a write cycle, write enable must be held active for the complete write cycle. Figure 3 shows latched EEPROM write timing. Timer EEPROMs, however, latch addresses on the falling edge of the write pulse and data on the rising edge. Figure 4 shows timer EEPROM write cycle timing.

Figure 2. 2816 Interface

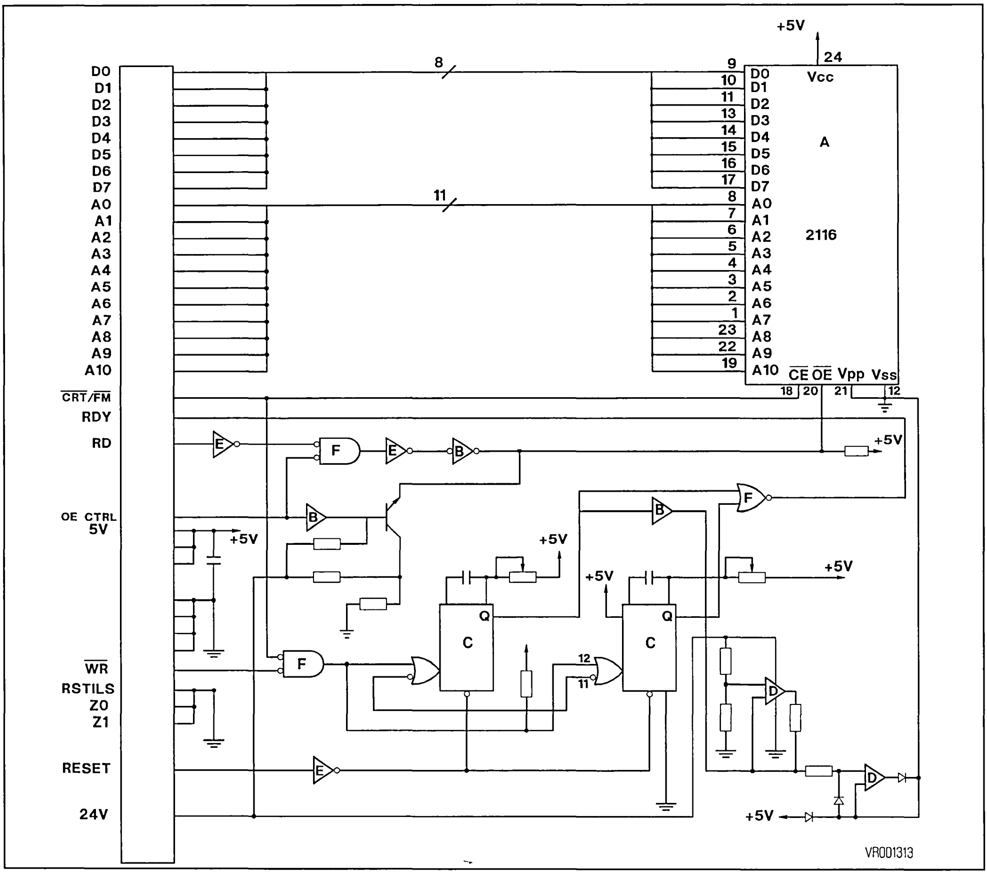

D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CRT/FM
RDY
RD
OE CTRL
5V
WR
RSTILS
Z0
Z1
RESET
24V
8
11
+5V
24
Vcc
A
2116
9
10
11
13
14
15
16
17
8
7
6
5
4
3
2
1
23
22
19
CE OE Vpp Vss
18
20
21
12
E
F
B
C
D
Q
12
11
VR001313

Figure 3. Latched EEPROM Write Cycle

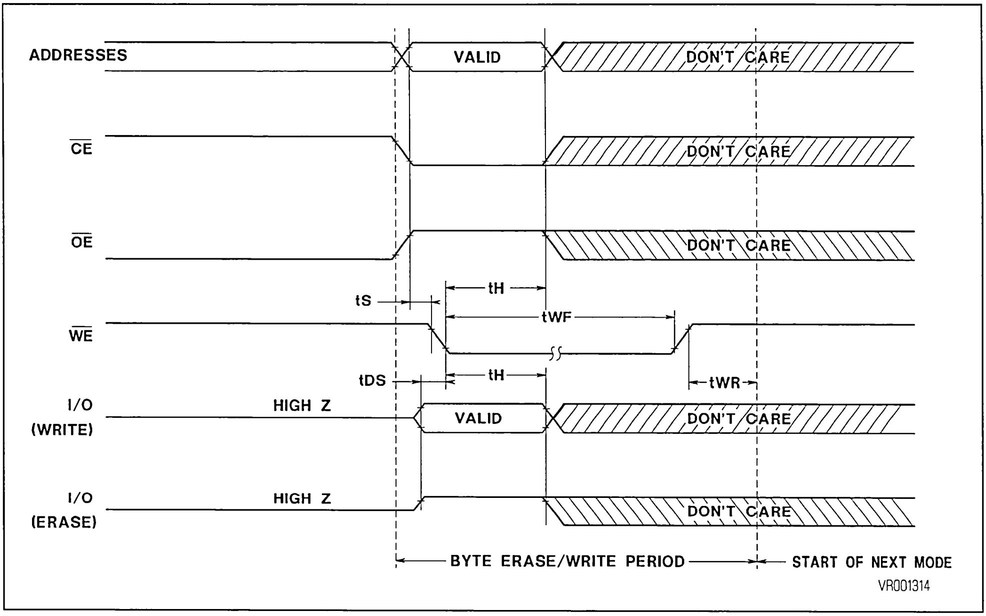
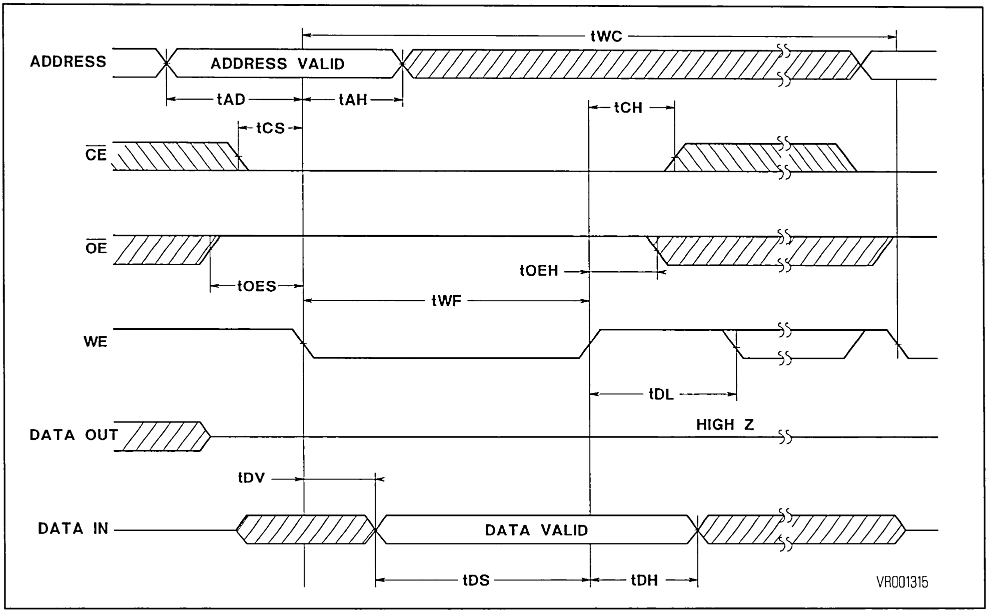

ADDRESSES
VALID
DON'T CARE
CE
DON'T CARE
OE
DON'T CARE
tS
tH
tWF
WE
tDS
tH
tWR
I/O (WRITE)
HIGH Z
VALID
DON'T CARE
I/O (ERASE)
HIGH Z
DON'T CARE
BYTE ERASE/WRITE PERIOD
START OF NEXT MODE
VR001314

Figure 4. Timer EEPROM Write Cycle


tWC
ADDRESS
ADDRESS VALID
tAD
tAH
tCH
tCS
CE
OE
tOEH
tOES
tWF
WE
tDL
DATA OUT
HIGH Z
tDV
DATA IN
DATA VALID
tDS
tDH
VR001315

Latched EEPROMs are interfaced in the system two ways. One, by latching the $\overline{WE}$ pulse until completion of the write cycle. Two by implementing multiple wait states to complete the write. Replacing latched EEPROM can be done by eliminating the $\overline{WE}$ latch, allowing the write cycle to follow the microprocessor. Multiple wait states will have no effect on the ZEROPOWER RAM, however for system efficiency they should be eliminated.

Timer EEPROMs are the most popular EEPROMs in use today because their write cycle timing is compatible with microprocessors that have cycle times in the 200 to 500 nanosecond range. The initialization of a timer EEPROM write cycle can be completed in the normal cycle time of the microprocessor and the EEPROM completes the write cycle independent of the system. Some timer EEPROMs will even allow multiple successsive writes (in page mode) before completion of the first write. ZEROPOWER RAMs are directly replaceable for timer EEPROMs in this application and have the advantage of even faster cycle times with no page mode restrictions. Timer EEPROMs, however, can also allow data and address changes during the write cycle. These data and address changes are not permited on conventional RAM and therefore in this application, data and address must be externally latched before replacement with ZEROPOWER RAM can be done. The later case is not industry standard for memories, and many systems with multiplexed address/data already have address and data latches for this reason.

Note :

Many EEPROMs require output enable to be high during the write cycle. With RAMs output enable is a "don't case" during write. In the very unlikely event that output enable should be used to gate the write cycle, a change in the circuit needs to be implemented before ZEROPOWER RAM can be used as a replacement.

APPLICATION NOTE

PROGRAMMING THE MK48Z02

The MK48Z02 serves many varied applications. It provides the ease of access for both reads and writes that conventional RAMs offer, as well as nonvolatile memory that is associated with read only memories. Because of this nonvolatile characteristic, the MK48Z02 is often utilized as a medium for storage of alterable program code (firmware) as well as parametric data.

This type of data is usually generated on a software development system and then loaded into memory prior to installation of the device into the final product. Most software development systems provide the means of downloading code either directly into an EPROM device or provide a port for transferring this code to an external PROM programmer. The MK48Z02 will of course not work in an EPROM programming circuit because of the high voltages requires for EPROM write cycles.

Figure 1 shows an inexpensive circuit, however, that can be used for transferring code from an EPROM (master) to an MK48Z02 (copy). (If data already exists in an MK48Z02 it also can be used as the master, because read cycles of the MK48Z02 and EPROM devices are similar). This circuit uses an oscillator and counter to step through all address locations in a binary sequence. The first phase of the clock (positive cycle) generates the write pulse. The second phase of the clock (negative edge) is used to clock the counter circuit to the next address. Once all addresses have been accessed, the next cycle will set a latch that resets the circuit and lights a finished light. Pushing the start button resets the latch and starts the sequence from the beginning. A switch going to V_{CC} on the master and copy sockets is provided so that V_{CC} can be removed when inserting or removing devices to insure maximum data security. Removing V_{CC} from the MK48Z02 will deselect the device making all other inputs don't care, therefore intermittent contact to the socket when inserting or removing devices will not generate spurious write cycles.

Verification of data should not be a significant issue because the MK48Z02 does not suffer from programming yield problems like EPROM devices do. However, if a device is suspected of having faulty code, verification can be accomplished on the EPROM programmer IN THE VERIFICATION MODE ONLY (caution : check with the manufacturer of the programmer to make sure no high voltages are applied to the device in the verify only mode).

There is no limit to the number of times the MK48Z02 can be programmed, and the MK48Z02 does not need to be erased before it can be programmed.

MK48Z02 Inexpensive Programmer

- Power Supply
  - 12V, 500mA
  - sleeve negative, tip positive input.
- Fuse : 1A, 250V.
- LED Busy indicator.
- Copy time under 5 seconds.
- Test sockets for easy insertion and extraction.

Operation

1. Plug the AC or DC adapter into the coaxial power input, making sure that the polarity is correct, and plug in the power supply.
2. Make sure that the power switch is in the OFF position before inserting the chips.
3. Raise the levers on the test sockets, and insert both chips with the indicator dots on the same side as the levers.
   Securely clamp the levers down all the way.
4. Switch the power ON.
5. Depress and release the start button. The busy light will stay lit for about 4 seconds as the chip is being copied.
6. When the light has turned off, switch the power off before releasing the levers on the test sockets and removing the chips.
7. Store the chips in anti-static foam.

Troubleshooting

If the MK48Z02 Programmer is not functioning properly, take the following steps :

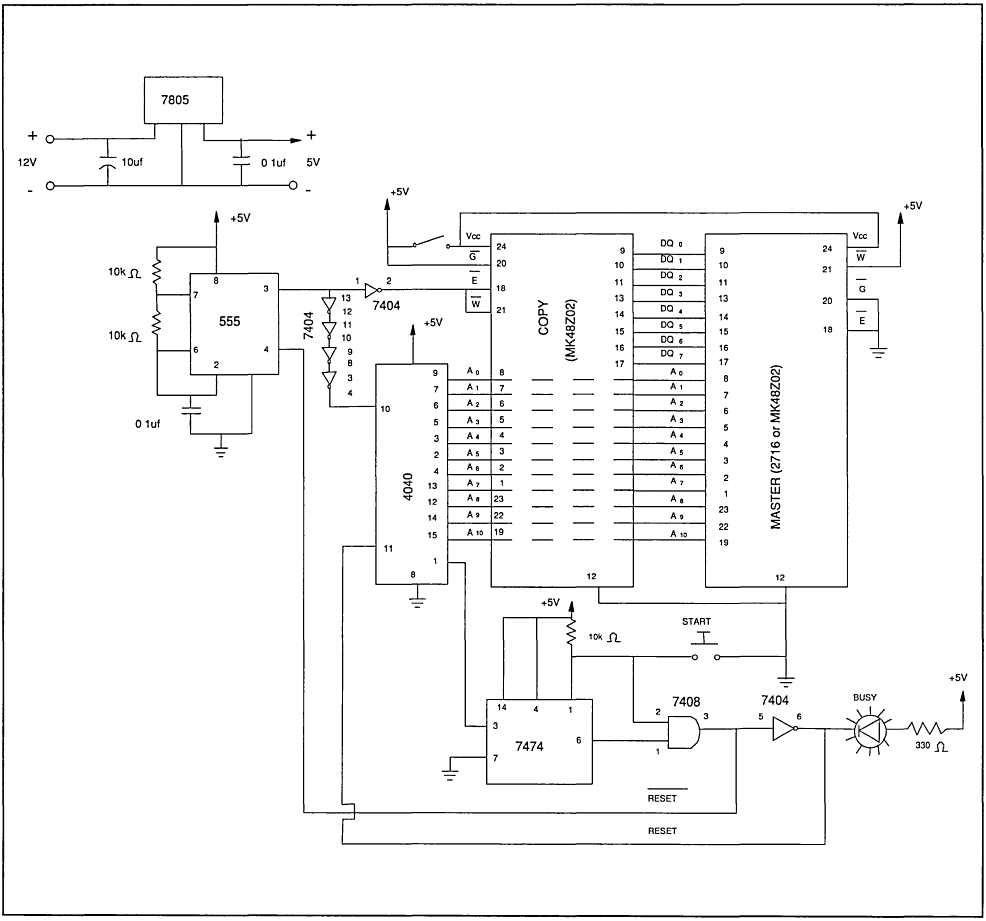
Check the fuse and replace if blown.

Make sure the polarity on the power supply is correct. (sleeve negative, tip positive).

Follow the operating instructions through step by step.

Remove the bottom of device and make sure all chips are securely in their sockets.

Figure 1. Inexpensive MK48Z02 Programmer


7805
12V
10uf
0 1uf
5V
+5V
10k Ω
10k Ω
0 1uf
555
7404
7404
4040
Vcc
G
E
W
COPY
(MK48Z02)
MASTER (2716 or MK48Z02)
DQ 0
DQ 1
DQ 2
DQ 3
DQ 4
DQ 5
DQ 6
DQ 7
A 0
A 1
A 2
A 3
A 4
A 5
A 6
A 7
A 8
A 9
A 10
START
10k Ω
7474
7408
7404
BUSY
330 Ω
RESET
RESET

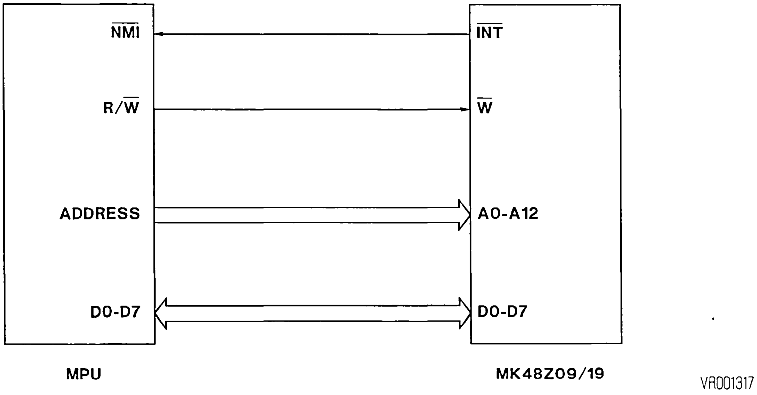
POWER FAIL INTERRUPT OF THE MK48Z09/19

A frequent dilemma faced by system designers is how to handle a power failure. Because power fail sensing components add real estate and cost to the system, some designers choose not to implement a power fail routine, allowing "the chips to fall where they may". This approach is frequently rationalized given the in-frequency of power failures and the industry drive to minimize circuit board space. It does not however represent an ideal solution. Other designers have gone to great expense to design a power fail sensing circuit only to find it difficult to control voltage trip points and experience timing requirements that are hard to predict.

The MK48Z09/19 provides a solution to the power fail dilemma. While occupying no more board area than conventional memories of the same density, the MK48Z09/19 also offers a power fail interrupt output pin along with nonvolatile memory. Because the voltage trip point of the interrupt signal on the MK48Z09/19 is temperature compensated, the user can be assured that its operation remains within specifications over the entire temperature range. The MK48Z09/19 also provides predictable timing. The amount of time between an interrupt low and a power fail write protect condition is a function of an internal oscillator within the MK48Z09/19 and therefore is independent of what may be happening at the system level. The only restriction imposed on the user is that a minimum V_{CC} fall time not be exceeded. The minimum V_{CC} fall time is, however, easily within the normal V_{CC} fall time characteristics of most applications.

The power fail interrupt pin of the MK48Z09/19 is open drain and can be easily implemented by connecting the interrupt signal to a non maskable interrupt input on the microprocessor used, thus initializing a short power fail routine. Because the MK48Z09/19 is battery backed up, the power fail routine can store important data and parameters. Sign off to data communication links and notification of a local power failure to supervisory systems are also applications made possible to the local controller through the use of the power fail interrupt.

Figure 1. Suggested MK48Z09/19 Hook Up



POWER FAIL CONDITIONS

The MK48Z09/19 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point of the MK48Z09/19 an interrupt is immediately generated. An internal clock provides a delay no less than 10μs but no greater than 40μs before automatically deselecting the MK48Z09/19.

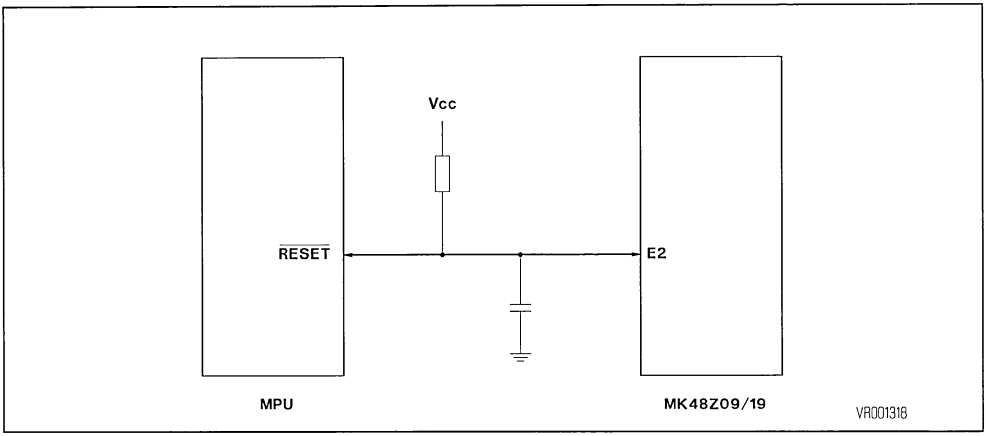
With V_{CC} allowed to fall at its maximum rate from 4.75V to 4.5V in 300μs (833V/sec), a delta voltage between when a power fail is detected and the device is deselected will be established. Because the maximum V_{CC} fall rate and maximum delay between power fail detect and deselection are given values, this delta voltage can be easily calculated 40μs * 833/V = 48mV). Therefore final testing of the MK48Z09/19 at SGS-THOMSON can assure the user that the device will be deselected no lower than the specified Power-Fail Deselect (VPFD min) level, provided that the maximum V_{CC} fall rate is not exceeded.

With V_{CC} fall times that stretch over a long period of time, the voltage at which an interrupt is generated and the voltage at which the MK48Z09/19 automatically deselects will approach the same value. Once again final testing at SGS-THOMSON can assure the user that a power fail detect or deselection will occur no higher than the specified Power-Fail Deselect (VPFD max) level.

POWER UP CONDITIONS

The MK48Z09/19, like most NVRAMs, provides automatic write protection under low voltage conditions. Unfortunately, many processors generate spurious cycles during power up, despite V_{CC} being within spec. Some processors even continue to behave erratically though their reset pin is being held low, until the system clock has had time to wake up and produce sufficient cycles to clear the processor. The MK48Z09/19 makes it easy to combat this problem by providing an active high E2 input (chip select). This input when tied to the reset line will lock out the MK48Z09/19 during the power on reset time, protecting the data in memory from being inadvertently over written with erroneous data. Figure 2 illustrates a simple power up reset scheme.

Figure 2. Write Protect Application of E2 Input



Notes:

1. Although trip points are tested by holding V_{CC} to given DC levels, the device is by no means in a static state Address, data lines, and control lines are all toggling. A series of complex patterns are input to the device to ensure that worst case noise conditions generated within the MK48Z09/19 will not affect trip point performance.
2. With even the slowest MK48Z09/19, the 250ns device, and the minimum 10μs advanced warning of a deselect condition, there is enough time for 40 memory cycles to take place. The amount of MPU cycles that can take place will of course vary according to the processor used and programming techniques.
3. The MK48Z09/19 can provide an inherent safe guard against a "Brown Out" condition i.e. V_{CC} that droops or slowly fades below spec. or operational limits and then comes back up Applications requiring the interrupt pin to remain low until a completion of a sequence of events (within 10μs), can relay on the MK48Z09/19 not to interrupt the sequence should power unexpectedly return. Once a power failure is detected and the interrupt pin goes low, the interrupt pin will remain low for the full 10μs to 40μs period and the device will be accessible during this time. Therefore the power fail interrupt application can not be aborted mid cycle. After the interrupt time period the interrupt pin will go high, should V_{CC} rise in the interim, allowing normal operation to resume. The MK48Z09/19, however, waits for a minimum of 30μs to a maximum of 120μs from the time interrupt goes high until another power fail can be selected. (Should V_{CC} remain at a level very close to the trip point for an extended period of time, a number of power failures could be detected due to noise on the V_{CC} line. Interrupt will always follow the above timing however).

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APPLICATION NOTE

TIMEKEEPER CALIBRATION OF THE MK48T02

The term "quartz accurate" has become a familiar phrase used to describe the accuracy of many time keeping functions. Although quartz oscillators provide an accuracy far superior to other conventional oscillator designs they are, however, not perfect. Quartz crystals are sensitive to temperature variations. Figure 1 shows the relationship between temperature and accuracy of the 32.768khz crystal oscillator used on the MK48T02 TIMEKEEPER™. Variations in resonant frequency from one crystal to the next also exist, although these variations typically do not exceed 20ppm (approx. 1 min. per month).

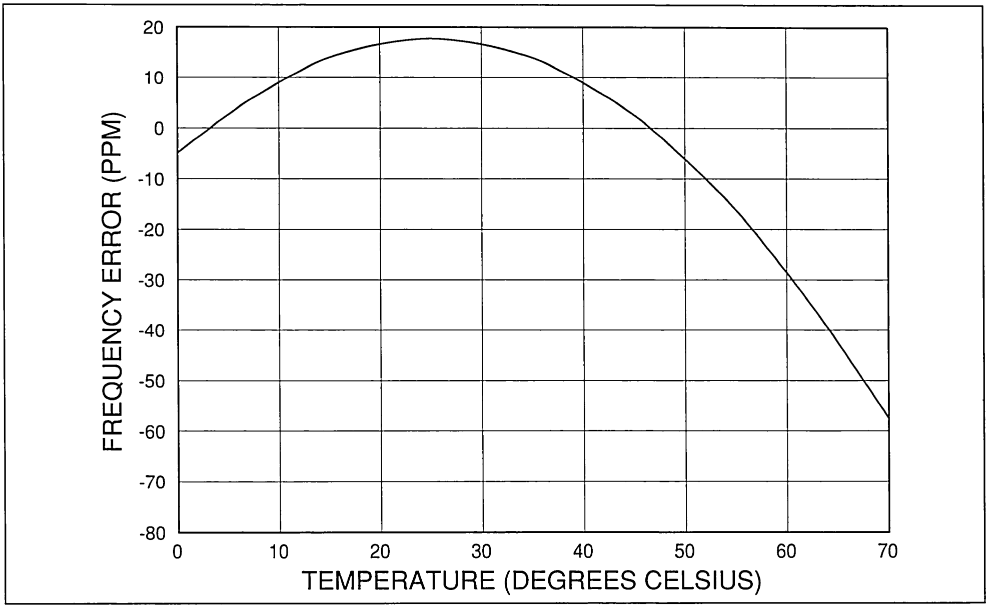
Clocks used in applications requiring a greater accuracy of 1 min. per month or have an ambient temperature that is not centered around room temperature (25°C) will need a means of calibration.

Typically, most crystal oscillators are calibrated by adjusting the load capacitance of the oscillator. This method, while effective, has several disadvantages.

1. It requires external components.
2. It requires the use of test equipment (fre- quency counter).
3. It can increase oscillator current (an important factor in battery backed-up applications).

At SGS-THOMSON Microelectronics, we believe these disadvantages are unacceptable. The MK48T02 calibrates its clock by adding or subtracting pulses from the clock chain in a predictable manner (periodic counter correction). This method can be employed under software control eliminating the disadvantages of the previously stated method and making it end user friendly.

Figure 1. Typical MK48T02 Oscillator Frequency vs. Temp.



TWO METHODS FOR CALCULATING CALIBRATION

There are two methods for establishing how much calibration will be required in a given application. The first method can be easily implemented in the user environment allowing the average ambient temperature be taken into consideration. The other method provides a fast means of calibration at the OEM site.

Empirical In System Method

This method involves setting the clock to a known standard and then comparing at a fixed time later. The longer the time period the greater the accuracy. When setting the clock, all counters in the 32.768khz to 1 second divider chain start from zero as soon as the write bit is released. Therefore, it is possible to set the clock to the standard within the response time of the system.

How to calculate the amount of calibration necessary.

N = number of seconds in the time period

T = number of seconds elapsed on the MK48T02

X = error in parts per million

$X = (T-N)/N * 1E6$

Notes :

1. Setting the sign bit does not indicate a ones complement number. Setting the sign bit speeds up the clock.
2. Each bit in the calibration bits represents a change of 2.034 parts per million.
3. Depending upon when the MK48T02 is read with respect to an update a one second error can occur. Make sure the time period for calculations is long enough so that this error becomes negligible.

Frequency Test Method

This method is best suited for use at incoming inspection on a sophisticated tester or on a bench set up. It is not practical for in system use unless a means for latching address and control lines can be implemented because the device must be held in a read state for and indefinite period of time.

Procedure for frequency test method.

1. set write bit.
2. set FT bit (DQ6 for day register).
3. reset write bit.
4. set address to seconds register and control lines for a device read.
5. measure 512hz frequency at DQ0.
6. set write bit.
7. reset FT bit.
8. set correct time and calculated calibration.
9. reset write bit.

Notes :

1. Instruments for measuring frequency should be accurate to 1 ppm for reasonable results.
2. Error in ppm = (frequency measured-512)/512 * 1E6.
3. Failure to reset the FT bit will result in gross timekeeping errors.

TIMEKEEPER CONTROL REGISTER

The control register of the MK48T02 serves three separate functions, all within the same byte of data. It allows the user to write time (write bit), read time (read bit) and calibrate the clock. When writing or reading the clock care should be taken not to disturb the calibration data.

When setting the write bit, data contained in the calibration bits will be entered into the calibration circuitry. Care should be taken to ensure this calibration data to be valid.

When setting the read bit, data contained in the calibration bits will be entered into memory only. This may seem harmless, however, it should be noted that the calibration data is not refreshed with a clock update. Therefore any record of valid calibration data will be lost if valid calibration data is not included with the read bit. This is important because valid calibration data is needed when setting the write bit.

Procedure For Setting And Resetting The Read And Write Bits

Set Write bit.

1. Read contents of Control Register.		00XXXXXX
2. Logical OR contents with the number 128.	OR	10000000
3. Load results into Control Register.		10XXXXXX

Reset Write Bit.

1. Read contents of Control Register.		10XXXXXX
2. Logical AND contents with the number 127.	AND	01111111
3. Load results into Control Register.		00XXXXXX

Set Read Bit.

1. Read contents of Control Register.		00XXXXXX
2. Logical OR contents with the number 64.	OR	01000000
3. Load results into Control Register.		01XXXXXX

Reset Read Bit.

1. Read contents of Control Register.		01XXXXXX
2. Logical AND contents with the number 191.	AND	10111111
3. Load results into Control Register.		00XXXXXX

Example BASIC program.

```
10  REM CONTROL REGISTER LOCATION
20  A = 2040
30  REM SET WRITE BIT
40  POKE A, PEEK (A) OR 128
50  REM RESET WRITE BIT
60  POKE A, PEEK (A) AND 127
70  REM SET READ BIT
80  POKE A, PEEK (A) OR 64
90  REM RESET READ BIT
100 POKE A, PEEK (A) AND 191
```

APPLICATION NOTE

MEMORY MAPPED TIMEKEEPER REGISTERS OF THE MK48T02

Although software is usually thought of as being flexible, there can be applications where the memory management of the system defines how the memory will be utilized. Because the TIMEKEEPER™ registers of the MK48T02 reside within a predetermined position within the memory map, this may present a problem in these applications. Fortunately there are easy solutions to this problem.

There are several options possible for moving the location of the TIMEKEEPER registers within memory. The first option involves inverting one, all, or any combination of the eight most significant address lines of the MK48T02. Figure 1 shows an example of how inverting address A10 will move the apparent position of the TIMEKEEPER from the top of the device memory to the middle of device memory (from 7F8-7FF to 3F8-3FF).

Another option is to use higher order address lines (above A10) to decode the chip enable input of the MK48T02, therefore moving the apparent location of the entire MK48T02 within memory. Figure 2. shows an example of how this can be done. With this technique the TIMEKEEPER registers will remain in consecutive locations. Combinting options can place the TIMEKEEPER registers in any block of eight bytes of memory.

Finally, a third option would be to bank select the MK48T02. This method would allow the TIMEKEEPER to become transparent to memory directly accessible from the processor. Implementing a bank select requires generating a pseudo address line or lines that can be decoded with other address information to select the appropriate memory. The most convenient method for creating this pseudo address is to use an output port for this purpose. Microcontrollers have these ports on board while Microprocessors require a PIA chip to accomplish I/O functions. Figure 3 shows a typical Microprocessor to PIA combination that utilizes an I/O port to bank select memory. The I/O port can be programmed high or low by loading a register within the PIA. The PIA chip is selected by decoding IOREQ (I/O request). IOREQ also disables main memory and the MK48T02.

Figure 1.

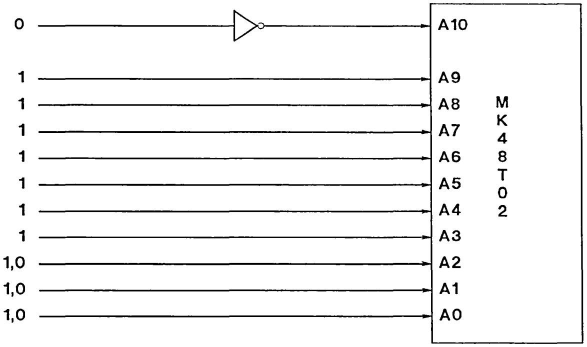


Figure 2.

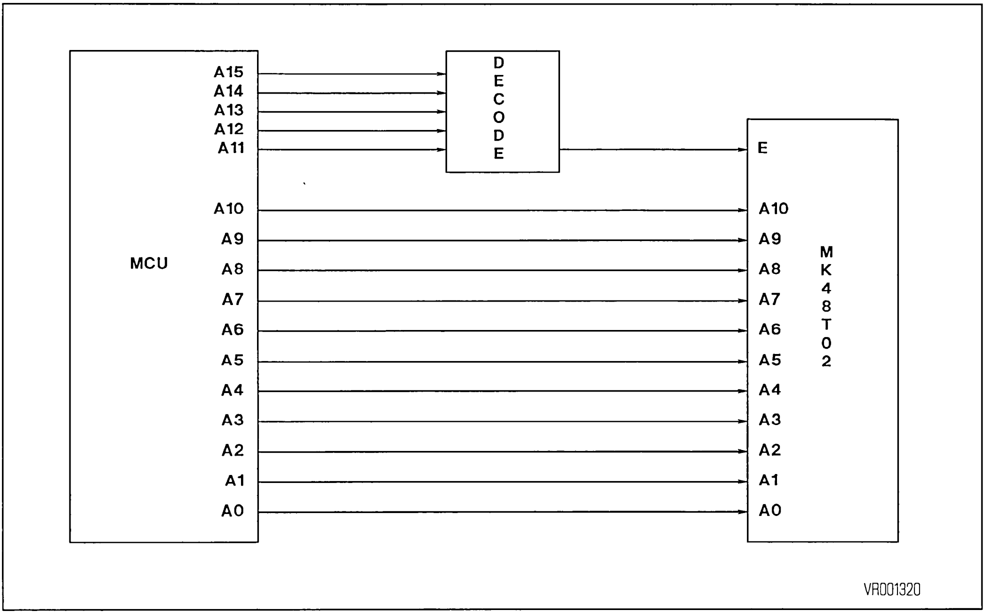
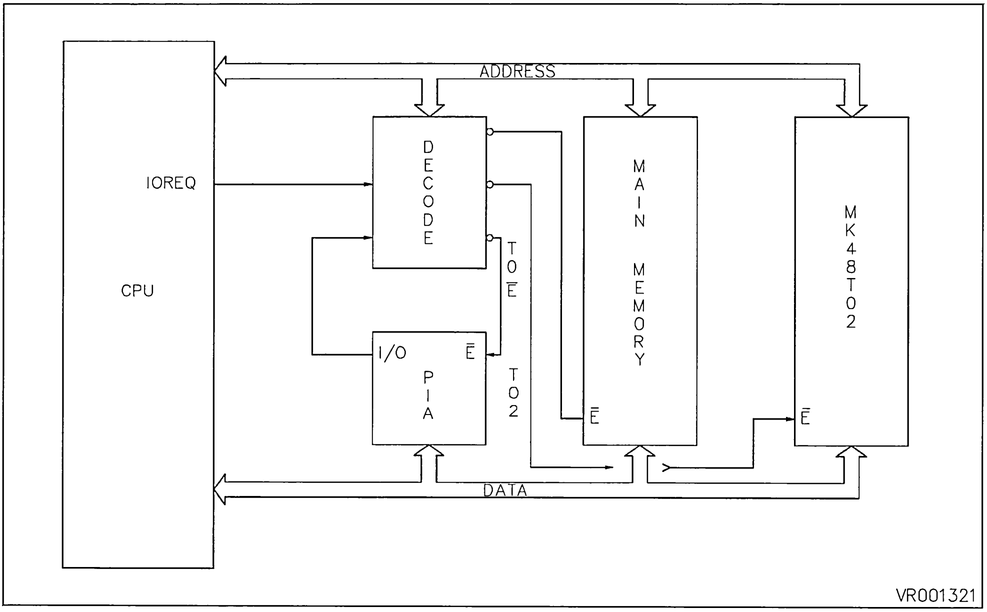

MCU
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
DECODE
E
MK48T02
VR001320

Figure 3.


ADDRESS
CPU
IOREQ
DECODE
TO $\overline{E}$
I/O
$\overline{E}$
PIA
TO2
MAIN MEMORY
$\overline{E}$
MK48T02
$\overline{E}$
DATA
VR001321

THE MK45H03 BiPORT FIFO 16-BIT TO 8-BIT CONVERSION

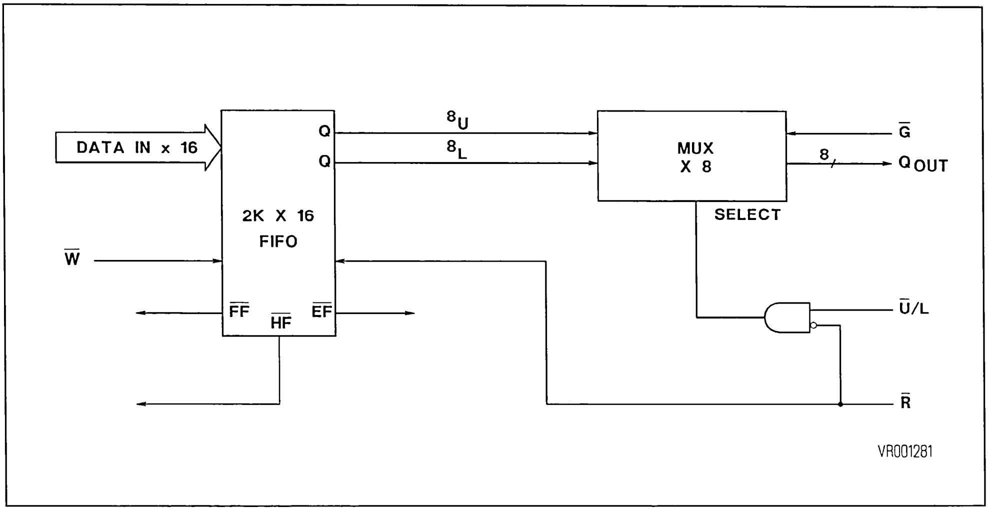
INTRODUCTION

When SGS-THOMSON Microelectronics introduced the MK4501 in 1983, it was the first high density FIFO with a BiPORT™ memory cell architecture. The MK4501 quickly became the industry standard with an organization of 512 x 9 bits, and included both an Empty and Full status flag. SGS-THOMSON has extended this technology to develop a device with four times the density - the MK45H03. The MK45H03 has a 2K x 9-bit organization, and includes the addition of a Half Full ($\overline{HF}$) status flag, as well as the Empty and Full status flags. Its BiPORT™ RAM cell design allows simultaneous and asynchronous Write/Reads, and avoids the added ripple-through delay times of conventional shift register based FIFOs. As with the MK4501, word with and depth expansion is easily achieved by using the $\overline{XI}$ and $\overline{XO}$ pins. The MK45H03 is pin-for-pin compatible with the MK4501 and MK45H01, and thus can be used as a density upgrade in many applications.

CIRCUIT DESCRIPTION

As shown in Figure 1, the block diagram for this application concept shows an example of how to interface a 16-bit Microprocessor to an 8-bit peripheral. Due to the MK45H03's architecture, which provides easy width expansion, we can interface two MK45H03 FIFOs to a 16-bit Microprocessor for collecting and holding our data dumps. By using a small amount of additional logic, we can retrieve this data in consecutive 8-bit bytes. (The diagram in Figure 2 shows the basic idea in an equivalent circuit). Using the two MK45H03 FIFOs, we start with a 2K x 16 memory buffer as our input, and convert it to a 4K x 8 memory buffer output. The status flags will keep us updated to let us know when we are Full ($\overline{FF}$ = low), or Empty ($\overline{EF}$ = low). The Half-Full status flag ($\overline{HF}$ = low) will help to avoid those sudden unpredicted halts, for example, should there not be adequate block memory space available. We will also take advantage of the asynchronous and simultaneous Write/Read capability of the MK45H03's BiPORT™ design.

Figure 1. Block Diagram



CIRCUIT OPERATION

The schematic diagram in Figure 3, shows that we will be writing 16-bit words designated as UPPER and LOWER 8-bit bytes, and then reading first the UPPER 8-bit byte, and then the LOWER 8-bit byte. As with all FIFO applications, we must start with Reset ($\overline{RS}$) to initialize the circuit. Remembering that upon reset our $\overline{EF}$ output goes active low, all Read cycles are ignored until the first Write cycle has been completed. Once a succesful Write has been performed, the $\overline{EF}$ output will go inactive high. The ideal operation would allow the Write count to remain at least one cycle ahead of the Read, thus avoiding $\overline{EF}$ from being asserted active. Referring again to Figure 3, the $\overline{A}$/B select to the data multiplexers via Q of the D-type flip-flop, alternates at the **end** (rising edge) of each Read to get ready for the next Read cycle. This avoids additional gate delay time, as well as providing a READ strobe during the full $\overline{R}$ pulse width. Therefore, after Write, and upon the first Read, we access the UPPER byte ($Q_{A\ 0\text{-}7}$), and alternate thereafter between the LOWER ($Q_{B\ 0\text{-}7}$) and UPPER byte with each consecutive Read. The flag status needs only to be taken from the LOWER byte FIFO since it will be Read last, and both are written simultaneously. Of course an (Empty - 1) function could be implemented on the 8-bit side by using the Empty Flag output from the UPPER FIFO.

In this application we have included data bus control with a fast external Output Enable ($\overline{G}$) on the multiplexer. The waveform timing diagram is referenced in Figure 4. Since there will be a specific Q-valid access time from the enabled FIFO to the data inputs of the multiplexer, the $\overline{G}$ input can be tied to the $\overline{R}$ system input without any penalty. The timing diagram in Figure 5 displays the typical access times to be considered. For example, t_{A1} is the combined access time of the OR gate plus Read access (t_A) of the MK45H03. Further definitions are : t_{A2} = MUX Q-Valid access time, t_{A3} = MUX Q-Valid access time from $\overline{R}$ asserted low, t_{GLQV} is MUX $\overline{G}$ (Output Enable) access to Q-Valid, t_{OH1} = Q-Hold time of the FIFO, t_{OH2} = Q-Hold time of the MUX, and t_{GHQZ} is output Enable to High Z. It should be noted that t_{A3} is equal to (t_{A1} + t_{A2}), where the limiting factor is t_{A1} not t_{GLQV}, when $\overline{G}$ = $\overline{R}$ (see Figure 5).

CONCLUSION

This implementation presumes that Read strobes will be halted when the lower MK45H03 indicates itself empty. In this example, should the lower FIFO become empty, additional Read strobes will continue to toggle the select D-type flip-flop even though the FIFOs will not respond. Should Read-while-Empty compatibility be required, then additional logic will be needed to disable the select flip-flop when the lower FIFO is empty.

Figure 2. Equivalent Circuit

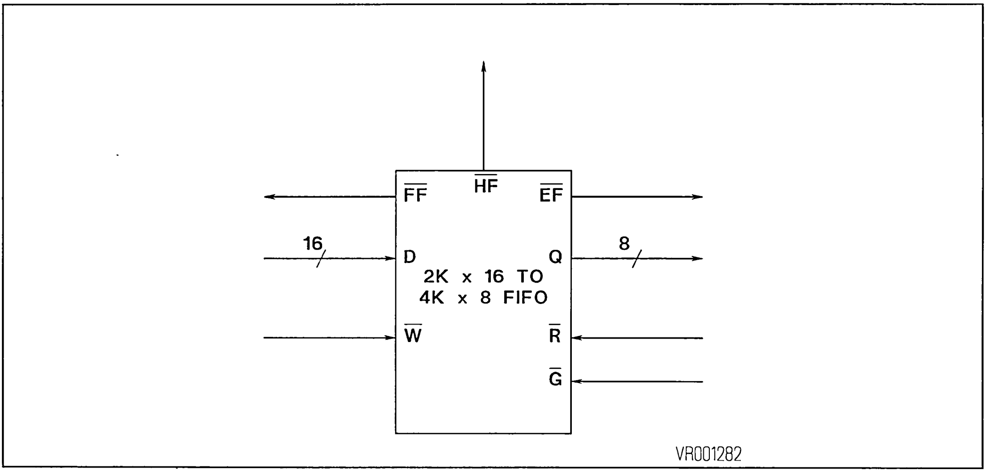


Figure 3. Asynchronous 16-Bit to Asynchronous 8-Bit Schematic

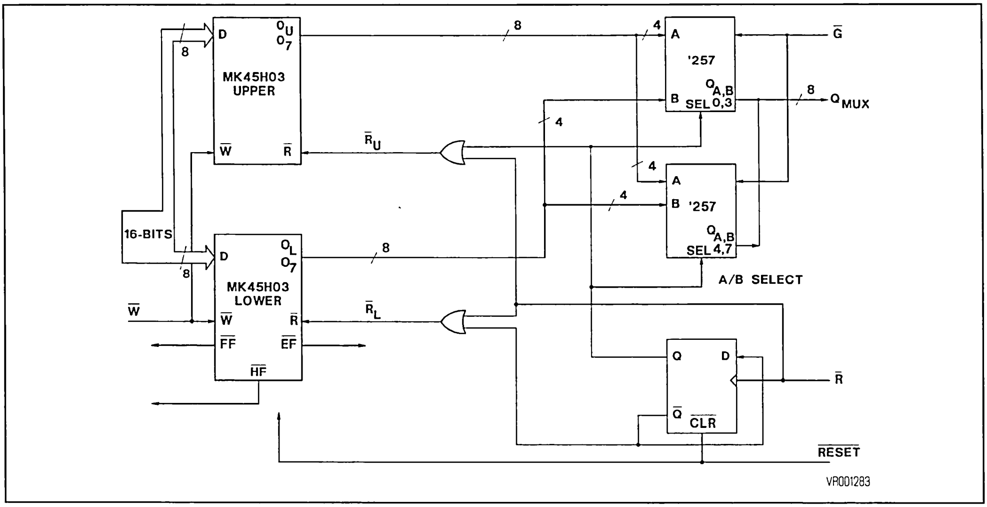

D
O_U
O_7
MK45H03
UPPER
$\overline{W}$
$\overline{R}$
8
16-BITS
D
O_L
O_7
MK45H03
LOWER
$\overline{W}$
$\overline{R}$
$\overline{FF}$
$\overline{EF}$
$\overline{HF}$
$\overline{W}$
8
8
$\overline{R}_U$
8
$\overline{R}_L$
4
4
4
4
A
B
'257
$Q_{A,B}$
SEL 0,3
A
B
'257
$Q_{A,B}$
SEL 4,7
A/B SELECT
$\overline{G}$
8
Q_{MUX}
Q
D
$\overline{Q}$
$\overline{CLR}$
$\overline{R}$
$\overline{RESET}$
VR001283

Figure 4. Timing Diagram

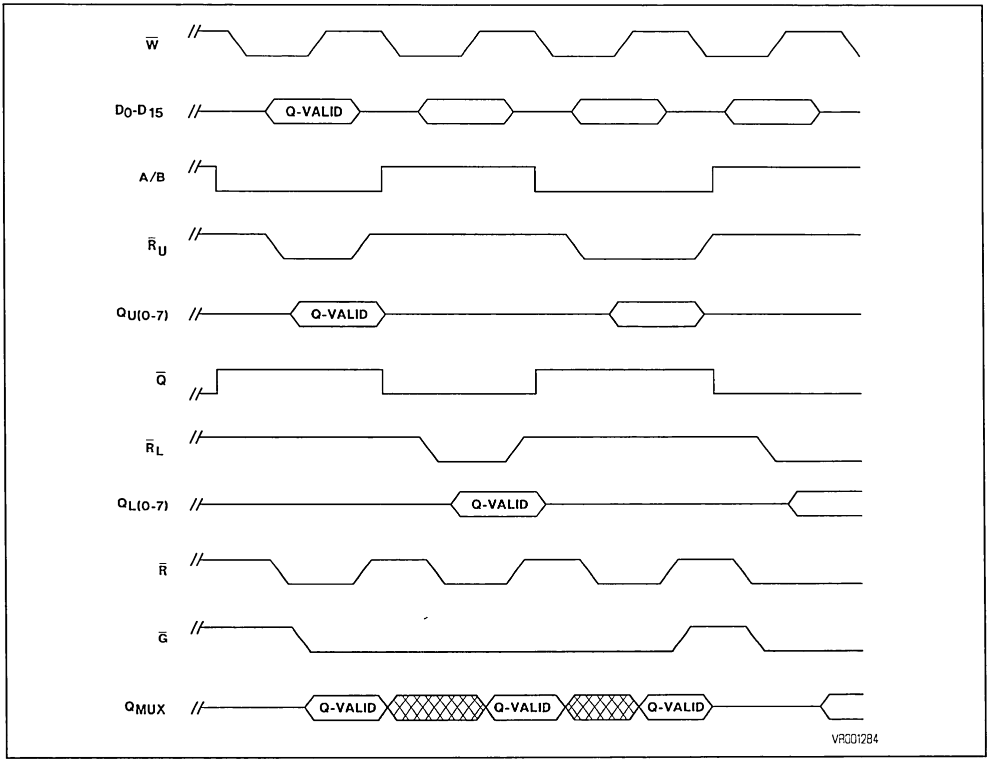
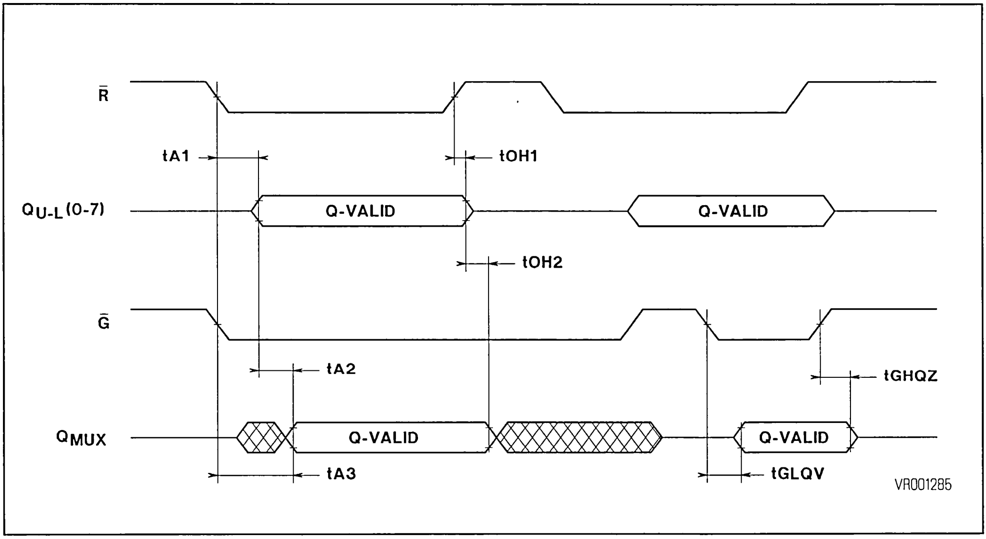

$\overline{W}$
D_0-D_{15}
Q-VALID
A/B
$\overline{R}_U$
$Q_{U(0-7)}$
Q-VALID
$\overline{Q}$
$\overline{R}_L$
$Q_{L(0-7)}$
Q-VALID
$\overline{R}$
$\overline{G}$
Q_{MUX}
Q-VALID
Q-VALID
Q-VALID
VR001284

Figure 5. Access Times


R̄
tA1
tOH1
QU-L(0-7)
Q-VALID
Q-VALID
tOH2
Ḡ
tA2
tGHQZ
QMUX
Q-VALID
Q-VALID
tA3
tGLQV
VR001285

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THE MK4505 CLOCKED FIFO INTRODUCTORY CONCEPTS

DEVICE DESCRIPTION

The MK4505 from SGS-THOMSON Microelectronics was the industry's first asynchronous clocked First-In-First-Out (FIFO) memory. This very fast clocked FIFO supports two independent, asyn-chronous, free running clock inputs, and has an organization of 1k x 5-bits with FULL, EMPTY, HALF FULL, ALMOST FULL, ALMOST EMPTY, DATA READY, and OUTPUT VALID status flags. As shown in the pin-out diagram in Figure 1, the MK4505 has two configurations : the MK4505M (Master) which features the full compliment of status flags, and the MK4505S (Slave). Either device, however, may be used in a stand-alone mode of operation. The Master features an automatic write protect when FULL, and an automatic read protect when EMPTY.

PIN NAMES

D0 - D4	Data Input
Q0 - Q4	Data Output
CK_W , CK_R	Write and Read Clock
WE_1	Write Enable Input 1
RE_1	Read Enable Input 1
$\overline{RS}$	Reset (active low)
HF	Half Full Flag
V_{CC} , GND	5Volts, Ground

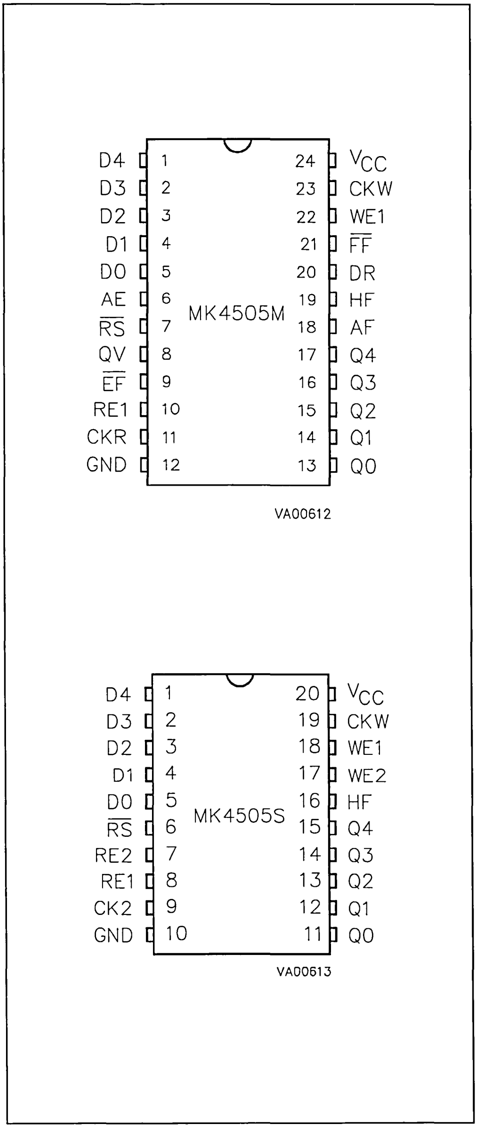
(4505M only)

$\overline{FF}$, $\overline{EF}$	Full and Empty Flag (active low)
AF , AE	Almost Full, Almost Empty Flag
DR , QV	Input Ready, Output Valid

(4505S only)

WE_2	Write Enable Input 2
RE_2	Read Enable Input 2 (rising edge triggered 3 state control)

Figure 1. Pin Connections


MK4505M
D4 1
D3 2
D2 3
D1 4
D0 5
AE 6
RS 7
QV 8
EF 9
RE1 10
CKR 11
GND 12
24 VCC
23 CKW
22 WE1
21 FF
20 DR
19 HF
18 AF
17 Q4
16 Q3
15 Q2
14 Q1
13 Q0
VA00612
MK4505S
D4 1
D3 2
D2 3
D1 4
D0 5
RS 6
RE2 7
RE1 8
CK2 9
GND 10
20 VCC
19 CKW
18 WE1
17 WE2
16 HF
15 Q4
14 Q3
13 Q2
12 Q1
11 Q0
VA00613

DEVICE DESCRIPTION (Continued)

In contrast, the Slave offers no protect circuitry, but can read and write continuously. Other MK4505 features are separate read and write enable inputs with the ability to enable or disable read/write operations upon command in the presence of a continuous periodic clock train. The MK4505 is available with a cycle rate of 40MHz, offering a 15ns access time.

MK4505M/S CIRCUIT OPERATION

The MK4505 appears to the outside world as a clocked D-type flip-flop with separate enable inputs. For example, each time a D-type flip-flop receives a clock, the Q output responds with the D input after a certain propagation time, provided data and enable set-up times are met prior to the rising edge of the clock. The MK4505 responds in somewhat the same manner, but offers a First-In-First-Out, 1024 x 5-bit sized buffer.

Referring to the block diagram schematic in Figure 2, the input stage looks like a rising edge triggered (CK_W) D-type flop with a separate enable comprised of a two input AND gate. Obviously, if either input is LOW, then the write operation is disabled. The output stage is similar, clocked by CK_R with a two input AND gate providing the read enable. If either input is LOW, the read operation is disabled. This provides the automatic read and write protection logic for the Master. The MK4505 FIFO uses the BIPORT™ RAM architecture, and appears as a dual port SRAM between the two I/O stages (see Figure 3). Internal write and read address pointers or counters automatically provide the RAM with the correct addresses. Figure 4 displays the combined logic symbol derived from the diagrams shown in Figures 2 and 3.

The MK4505 moves data only with each clock edge, as well as updating all status flags with the same clock edges. Each write function latches the input data with the rising edge of the write clock CK_W. The latched data is then transferred to a dual port RAM array. The predetermined first-in-first-out read sequence allows the read address counter to reach the stored data and present it to the input of the output latches before it is actually read. The output latches are then clocked on the rising edge of CK_R, and valid data is available t_A after the rising edge of the clock. Should a clock be turned off, as being locked LOW or HIGH, then the previous cycle is latched regardless of any input changes. This is true for the clocked D-type flip-flop, and the MK4505. Since the MK4505 supports asynchronous read/write clock functions, then either the read or write clock can discontinue without affecting the other port's activities.

Even though the MK4505 is designed for systems potentially operating from two asynchronous free running square wave clocks with cycle rates up to 40MHz, the device can be operated at much slower clock rates. A perfect square wave clock is not essential for proper device functionality. Parameters that must be satisfied are the specified minimum clock high and low times per the data sheet, and the set-up and hold times for enable inputs to the rising edge of the operational clocks. Clock duty cycle is not critical as shown in the example of Figure 5. Remember that the FIFO triggers from the rising edge of the clock, and clock transitions meeting V_{IL} and V_{IH} specifications must be obtained.

The MK4505M (Master) cannot be written while FULL, nor read while EMPTY. A FULL condition results only from writing all 1024 bit locations, but an EMPTY condition results from either a RESET or by reading all bit locations previously written. Referring to the MK4505 data sheet, First Read Latency (t_{FRL}) describes the delay from the first write clock after empty, to the first valid rising edge of CK_R that is guaranteed to produce the first write data at the Q outputs. This is the time required from Data In to be latched, presented to the BiPORT RAM array, and flow through to the output latches where it will be clocked to the outside world.

CONCLUSION

The MK4505M/S from SGS-THOMSON was the industry's first high performance clocked FIFO. The MK4505 supports two independent, asynchronous, free running clock inputs. It has a 1k x 5-bit architecture, and offers a 15ns access time with a 40 MHz clock rate. The device features both read and write enable controls in the presence of continuous read and write periodic clock trains.

The MK4505 is available in two versions as a Master or Slave. This provides for easy width and depth expansion FIFO array configurations. The MK4505M Master provides a full compliment of status flags, as well as providing all necessary controls for width and depth expansion. A MK4505M is required for each 1k of depth, and a MK4505 Slave for each additional 5 bits of width. Either device may be used separately with certain system applications. The MK4505M cannot be written while FULL, or read when EMPTY ; whereas, the MK4505S can be forced to read and write continuously regardless of device status. Both devices use SGS-THOMSON BiPORT RAM based memory cell allowing simultaneous read/write operations, and offer full TTL compatibility.

Figure 2. Block Diagram Schematic

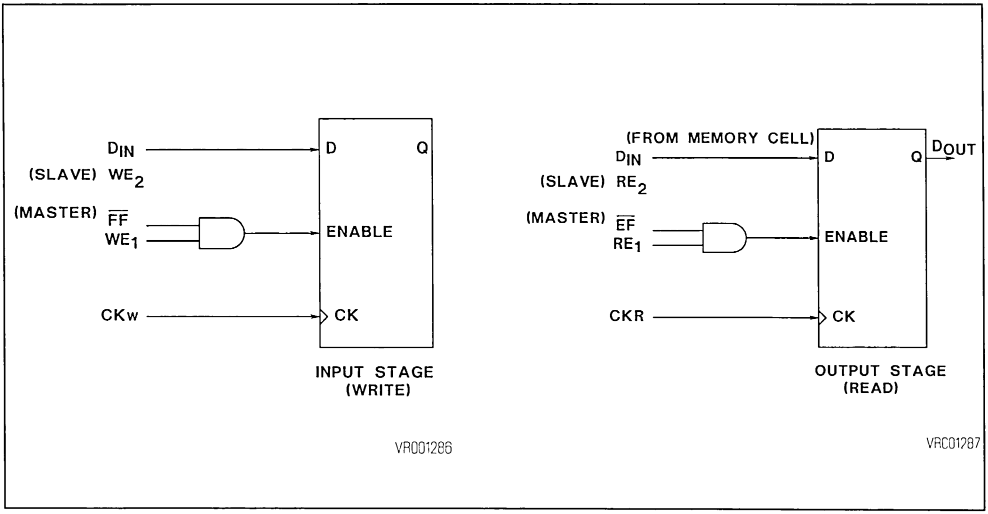

DIN
(SLAVE) WE2
(MASTER) FF
WE1
CKw
D
Q
ENABLE
CK
INPUT STAGE (WRITE)
VR001286
(FROM MEMORY CELL)
DIN
(SLAVE) RE2
(MASTER) EF
RE1
CKR
D
Q
DOUT
ENABLE
CK
OUTPUT STAGE (READ)
VRC01287

Figure 3. Representative Block Diagram

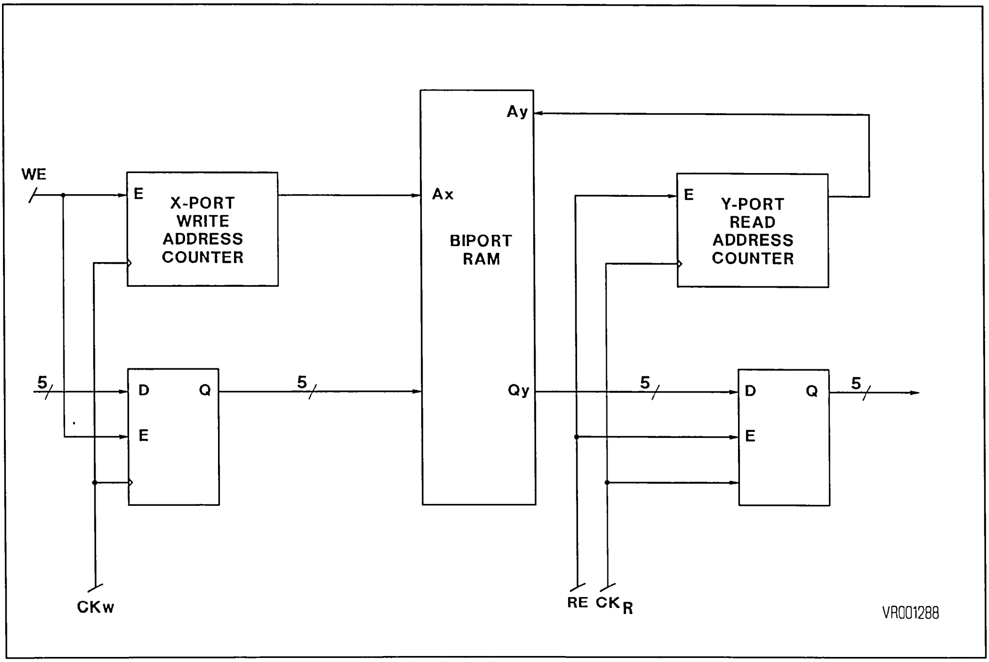

WE
E
X-PORT WRITE ADDRESS COUNTER
5
D
Q
E
5
Ax
Ay
BIPORT RAM
Qy
5
E
Y-PORT READ ADDRESS COUNTER
D
Q
E
5
CKw
RE
CKR
VR001288

Figure 4a. MK4505M Logic Symbols

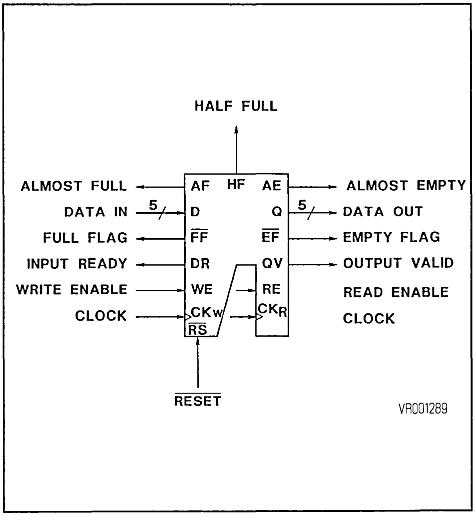

HALF FULL
ALMOST FULL
DATA IN
FULL FLAG
INPUT READY
WRITE ENABLE
CLOCK
AF
HF
AE
D
Q
FF
EF
DR
QV
WE
RE
CKW
CKR
RS
5
5
ALMOST EMPTY
DATA OUT
EMPTY FLAG
OUTPUT VALID
READ ENABLE
CLOCK
RESET
VR001289

Figure 4b. MK4505S Logic Symbols

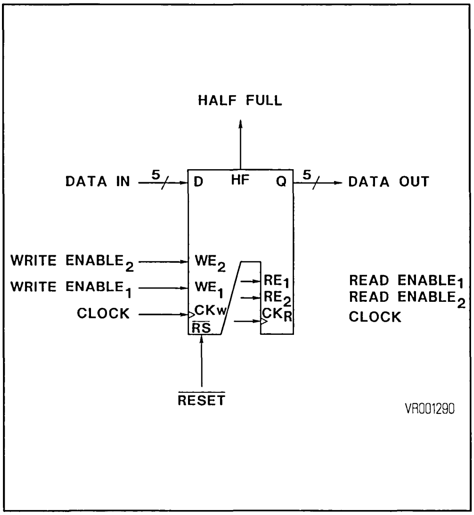
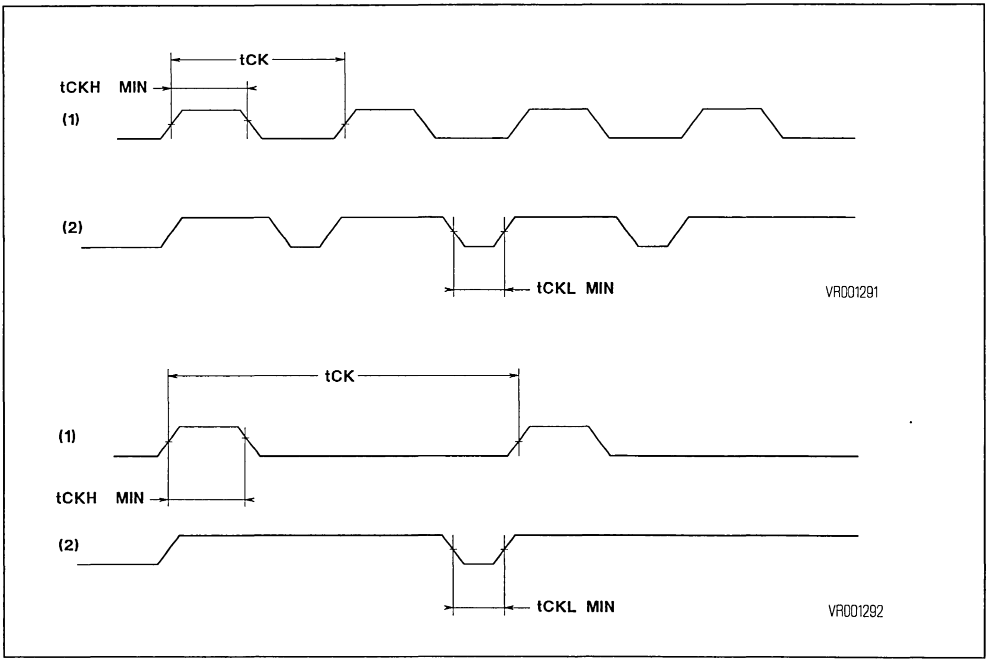

HALF FULL
DATA IN
5
D
HF
Q
5
DATA OUT
WRITE ENABLE2
WRITE ENABLE1
CLOCK
WE2
WE1
CKW
RS
RE1
RE2
CKR
READ ENABLE1
READ ENABLE2
CLOCK
RESET
VR001290

Figure 5. Possible Valid Clock Examples


tCK
tCKH MIN
(1)
(2)
tCKL MIN
VR001291
tCK
(1)
tCKH MIN
(2)
tCKL MIN
VR001292

USING THE MK4505 CLOCKED FIFO AS A DIGITAL DELAY

INTRODUCTION

The MK4505 was the first FIFO to support two independent, asynchronous, free running clock inputs. The MK4505 clocked interface makes high performance designs much simpler, eliminating the need for external registers, buffers, or pulse shaping circuits. The MK4505 is available in two configurations : the MK4505M (Master) and the MK4505S (Slave). This allows very simple width and depth expansion using one MK4505M for each 1024 bits of depth, and one MK4505M with one MK4505S for each additional 5-bits of width. Because it is BiPORT™ RAM based, it is not subject to the ripple-through delay times of conventional shift register type FIFOs. The MK4505 is suitable for applications with cycle rates up to 40MHz.

CIRCUIT DESCRIPTION

In the block diagram shown in Figure 1, we have displayed a 1k by 10 configuration that would be typical of a high performance digital video delay application. Of course narrower or wider bit fields can be accomplished just as easily. The MK4505M provides all additional enables to the MK4505S, with WE1 going to both devices, into the counter circuit, and thus generating the Read Port Enable (RE1) once the desired count is reached.

CIRCUIT OPERATION

For the following application, we have shown an example for digital data delay in a system using one free running clock (ø clock) for CKW and CKR, and one Write/Read (WE1) control clock, with a programmable counter for determining the desired delay from 2 to 1022 cycles. In this particular example, we have shown the maximum delay allowed to avoid the $\overline{FF}$ (Full Flag) from being asserted low (see Figure 2). The output of the counter circuit serves a two-fold purpose. First it provides the enable logic to the ENT pin for the first stage of the counter. Presetting the counter to 402HEX, assures that QC of the counter's third stage is set high, which sets the ENT enable of the first stage at the beginning of the count sequence. Secondly, the counter circuit provids an active high RE1 to the FIFOs enabling the delayed READ for output data once the count of 1022 (Full -2) has been reached.

After power-up and Reset ($\overline{RS}$), preset the counter circuit by presenting 402 HEX (010000000010) through the ABCD inputs while strobing LOAD active low. The 74161 4-bit counter to the far left is the first stage. The system clock (Øclock) goes to each of the clock inputs of the counter circuit, WE1 is ENP enable, and RC0 goes to each successive device ENT enable ; with the exception of the first stage which is enabled via the QC output of the final stage (loaded high during preset). Once the counter circuit has reached the count of 800 HEX, which is the delay count of 1022 as (Full -2) for the MK4505, the QD output of the third stage is set which enables the delayed Read Port (RE1 = high) to the MK4505 1K x 10 configuration. At the same time that QD is set, the QC output of the third stage is cleared, inhibiting count of the counter circuit. Since the Read Port Enable (RE1) is latched active high, continuous Write/Reads are allowed on each successive rising edge of Øclock (see Figures 3 and 4). The circuit will maintain a constant 1022 cycle delay until the next asynchronous Reset occurs.

PROGRAMMING DELAY INTERVAL

In conclusion, we have calculated a digital data delay of 1022 cycles. This is accomplished by realizing that setting QD of the third stage allows our maximum count to be 800 HEX (2048). Preset is determined by subtracting the desired delay nnn HEX from 800. Thus for this example it is (800 - 3FE HEX), which is 402. The decimal equivalent can also be used where ddd is the desired delay as (2048 - ddd) = DDDD. Preset is DDDD. Convert DDDD to nnn HEX. The final step is converting nnn HEX to its BINARY equivalent for the ABCD inputs during preset.

Figure 1. Block Diagram - Data Delay 1K x 10-bits

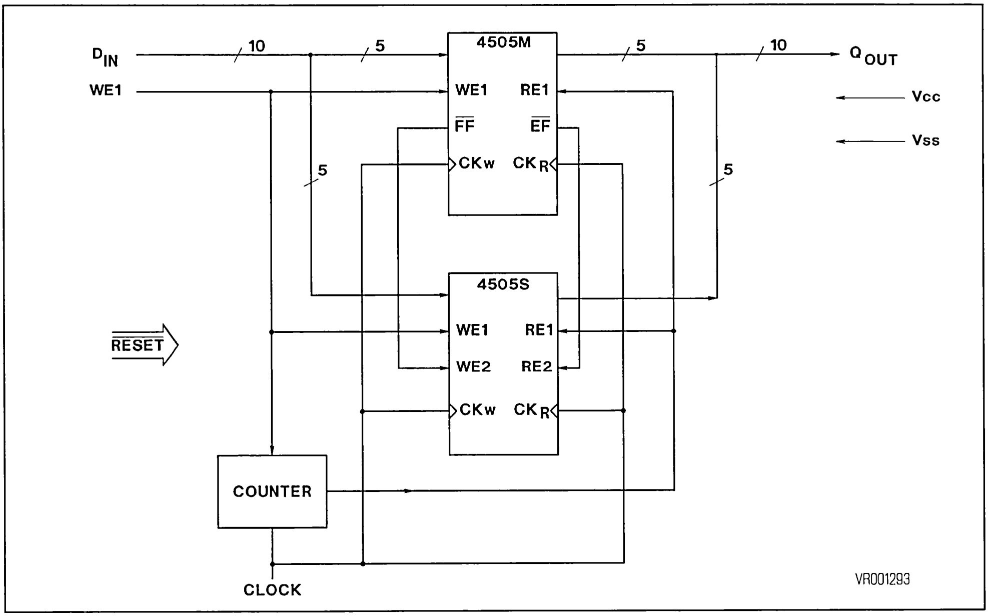
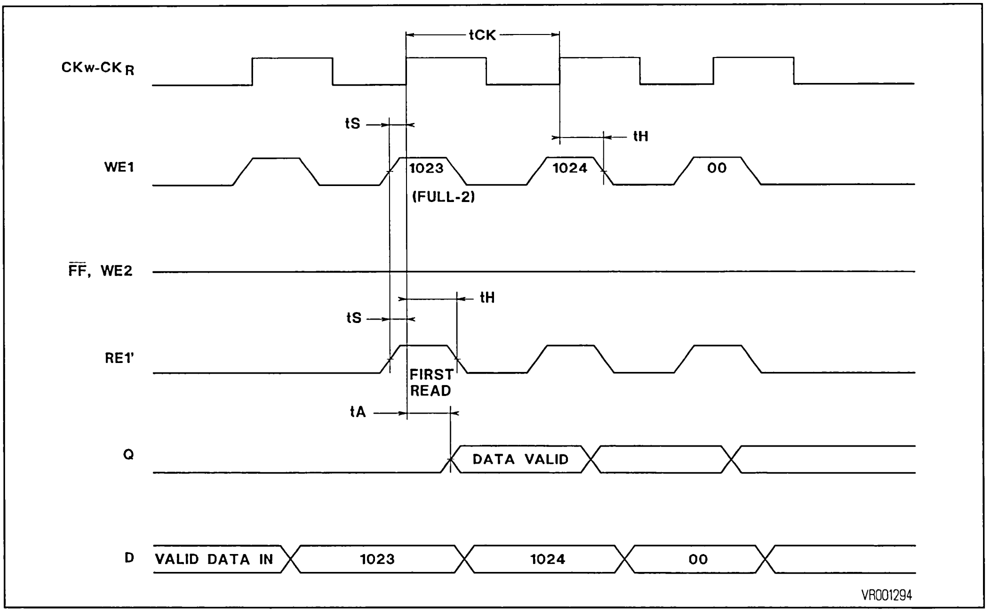

D IN
WE1
10
5
4505M
WE1
RE1
FF
EF
CKw
CK R
5
10
Q OUT
Vcc
Vss
5
5
4505S
RESET
WE1
RE1
WE2
RE2
CKw
CK R
COUNTER
CLOCK
VR001293

Figure 2. Write/Read Timing - Latest Possible First Read to Prevent Full Flag Assertion


tCK
CKw-CK R
tS
tH
WE1
1023
(FULL-2)
1024
00
FF, WE2
tH
tS
RE1'
FIRST READ
tA
Q
DATA VALID
D
VALID DATA IN
1023
1024
00
VR001294

Note : First read occurs (full -2) to avoid full flag ($\overline{FF}$) assertion.

Figure 3. Counter Delay Schematic

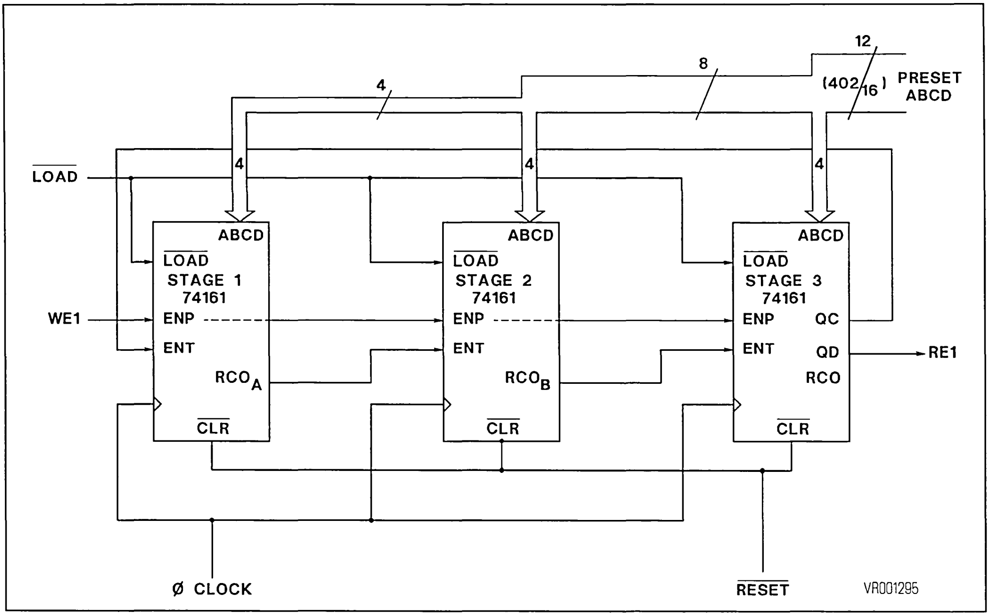
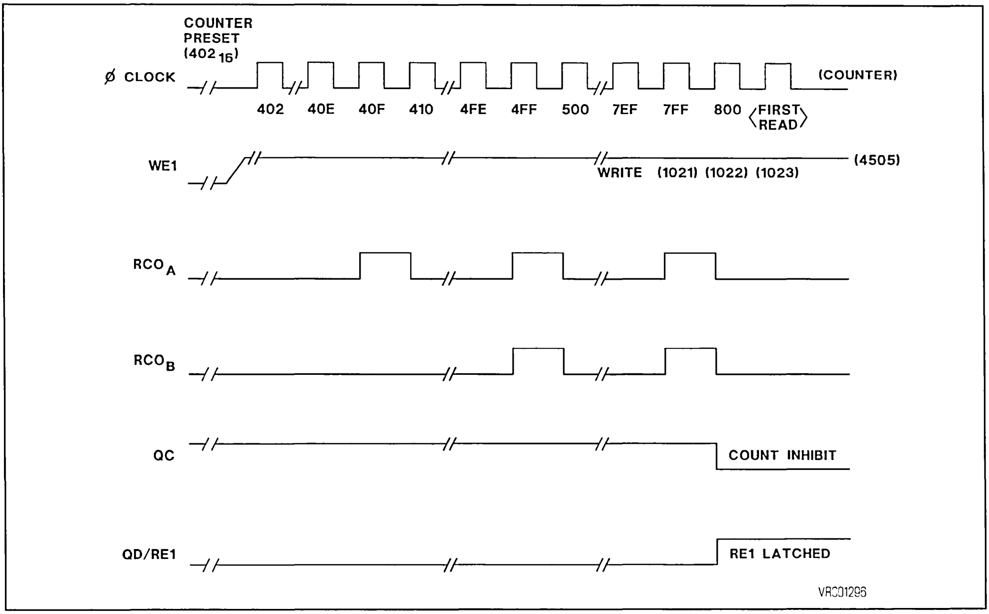

12
8
4
(402₁₆) PRESET ABCD
LOAD
WE1
4
4
4
ABCD
LOAD
STAGE 1
74161
ENP
ENT
RCO_A
CLR
ABCD
LOAD
STAGE 2
74161
ENP
ENT
RCO_B
CLR
ABCD
LOAD
STAGE 3
74161
ENP
ENT
QC
QD
RCO
CLR
RE1
Ø CLOCK
RESET
VR001295

Figure 4. Delay Timing Diagram


COUNTER PRESET (402₁₆)
Ø CLOCK
(COUNTER)
402
40E
40F
410
4FE
4FF
500
7EF
7FF
800
FIRST READ
WE1
(4505)
WRITE (1021) (1022) (1023)
RCO_A
RCO_B
QC
COUNT INHIBIT
QD/RE1
RE1 LATCHED
VR001296

Note : Timing diagram presumes preset of 402_{16} (1026) after reset, and full count of 1022 to latch re1 high when reaching 800_{16} (2048).

SGS-THOMSON
MICROELECTRONICS

APPLICATION NOTE

THE MK4505 LATCHED FLAG DESIGN CONSIDERATIONS

INTRODUCTION

The MK4505M/S (Master/Slave) is a high speed clocked FIFO from SGS-THOMSON Microelectronics. The MK4505 offers high performance, high density First-In-First-Out operation, and supports two asynchronous periodic clock inputs for write/read operations. Using the master/slave concept, the MK4505's 1K x 5 architecture is easily width and/or depth expandable, with all control and flag signals provided by the MK4505 Master. This type of organization allows ease of use to the system designer, avoids word skew in width expansion, and provides write protection when Full, and read protection when Empty. In addition to Full and Empty detection, the MK4505 provides three additional status flags for early warning as : AE (Almost Empty), AF (Almost Full), and HF (Half Full). The MK4505 also provides separate write and read enable inputs which allows the write/read operations to be enabled or disabled upon command in the presence of a continuous periodic clock.

The purpose of this application brief to discuss the latch function of the MK4505's $\overline{EF}$ (Empty Flag) and $\overline{FF}$ (Full Flag), proper operation, and design considerations. The latched flag function can cause subtle unexpected flag status operations when compared to previous ripple-through FIFO devices. This applies to both asynchronous and simultaneous write/read functions. Understanding how the flags operate and why, will enable the system designer to correctly manipulate the flag logic for proper system operation.

DEVICE OPERATION

As a brief review, the MK4505 appears to the outside world as a clocked D-type flip-flop with enable inputs. (Refer to the MK4505 application brief Introductory Concepts). Data on the D input is clocked through the flip-flop, and presented to the Q output at some propagation time (access time), and remains stable (data is held valid) until the next rising clock edge. The MK4505 functions in much the same manner, allowing 1024 bits of information to be "clocked through" in a First-In-First-Out fashion. The MK4505 also provides a full compliment of status flags dependent upont the rising edges of the write and read clocks. Figures 1 and 2 display the logic symbols for the MK4505 Master and Slave.

Figure 1. MK4505M Logic Symbols

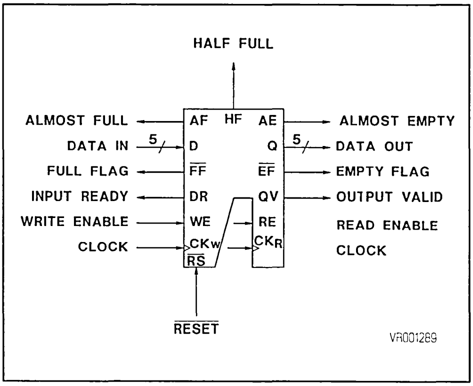
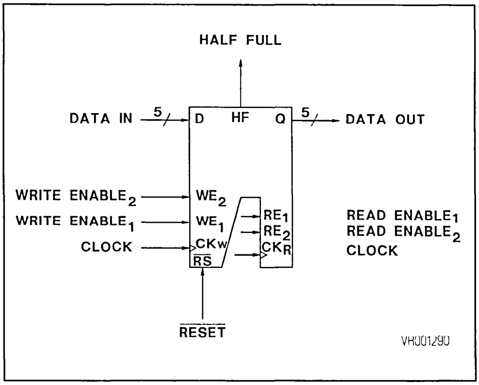

HALF FULL
ALMOST FULL
DATA IN
5
FULL FLAG
INPUT READY
WRITE ENABLE
CLOCK
AF
HF
AE
D
Q
$\overline{FF}$
$\overline{EF}$
DR
QV
WE
RE
CKW
CKR
$\overline{RS}$
5
ALMOST EMPTY
DATA OUT
EMPTY FLAG
OUTPUT VALID
READ ENABLE
CLOCK
$\overline{RESET}$
VR001289

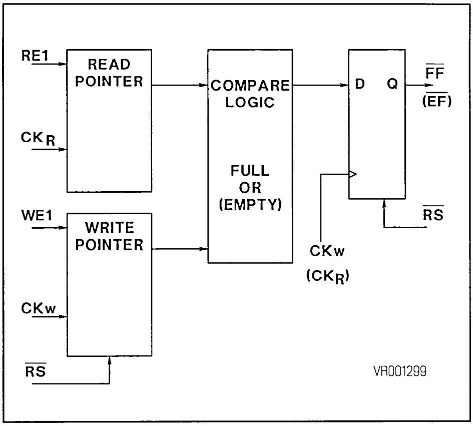
Figure 2. MK4505S Logic Symbols


HALF FULL
DATA IN
5
D
HF
Q
5
DATA OUT
WRITE ENABLE$_2$
WRITE ENABLE$_1$
CLOCK
WE$_2$
WE$_1$
CKW
$\overline{RS}$
RE$_1$
RE$_2$
CKR
READ ENABLE$_1$
READ ENABLE$_2$
CLOCK
$\overline{RESET}$
VR001290

LATCHED FLAGS

The MK4505 can only perform a valid write operation at the rising edge of CK$_W$, or a valid read operation at the rising edge of CK$_R$. Updates to all status flags are also dependent upon either CK$_W$ or CK$_R$, but not both clocks together. The $\overline{EF}$ (Empty Flag) status can only be updated with the rising edge of CK$_R$, while the $\overline{FF}$ (Full Flag) status can only be updated with the rising edge of CK$_W$. Therefore, using the D-type flip-flop analogy, we conclude that these status flags are latched on a

Figure 3. Latched Flag Logic Diagram



rising clock edge, and cannot change logic states until another clock edge occurs (refer to Figure 3). This is an important concept for design considerations when using status flag logic states to signal a processor or PAL, for example, to initiate or interrupt predefined system operations. It makes the system designer's job easier because it ensures proper set-up and hold times referenced to the rising edge. It also promises that the flag's logic state will remain valid for at least one complete cycle.

EDGE TRIGGERED STATUS

Let's presume that in our application we want to write the FIFO until Full, then disable write operations and read until Empty. In addition, we find that it would take fewer logic gates to turn CK_R and CK_W on or off than gating read (RE_1) and write (WE_1) enable inputs. (Figures 4 and 5 are simplified block examples for enable or clock control for a write-to-full, read-to-empty sequence). However, this can set the stage for unexpected flag status if both clocks are not active. The MK4505 can be operated in this manner, and deliver correct data in a first-in-first-out manner, but the designer must remember the latched flag philosophy. Specifically, one can write the MK4505 until Full where $\overline{FF}$ is latched low, and still maintain a valid empty condition with $\overline{EF}$ active low. This can happen by turning CK_W on and CK_R off, as CK_R updates the $\overline{EF}$ status. On the other hand, let's presume that we allow both clocks to run until full, and then disable the write clock (CK_W). We will find the same type of dilemma with $\overline{FF}$ remaining active low while clocking CK_R until the FIFO is empty. This would result again in both flags being set active low. Therefore, to ensure proper flag operation the system designer should use the write and read enable inputs when gating write/read operations.

Previous ripple-through FIFOs, such as the MK4501 and MK4503, allow $\overline{FF}$ and $\overline{EF}$ status updates as soon as an operation to clear or set the flag is accomplished. The MK4505, however, must determine the operation that clears or sets the flag, and then receive a rising edge clock (CK_W or CK_R) to update the flag's status. This is necessary for a clocked system environment, and again ensures set-up and hold times into the next cycle. Referring to the MK4505 data sheet, one will notice that DR (Data Ready) follows $\overline{FF}$ directly, and QV (Output

Figure 4. Clock Control Block Diagram (not suggested)

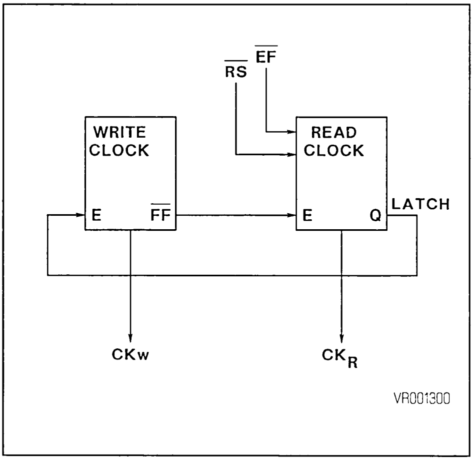


Figure 5. Enable Control Block Diagram (suggested)

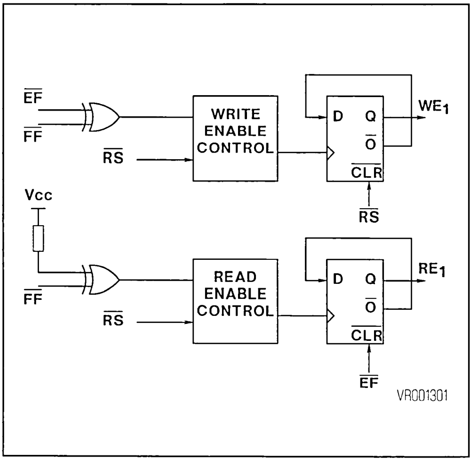
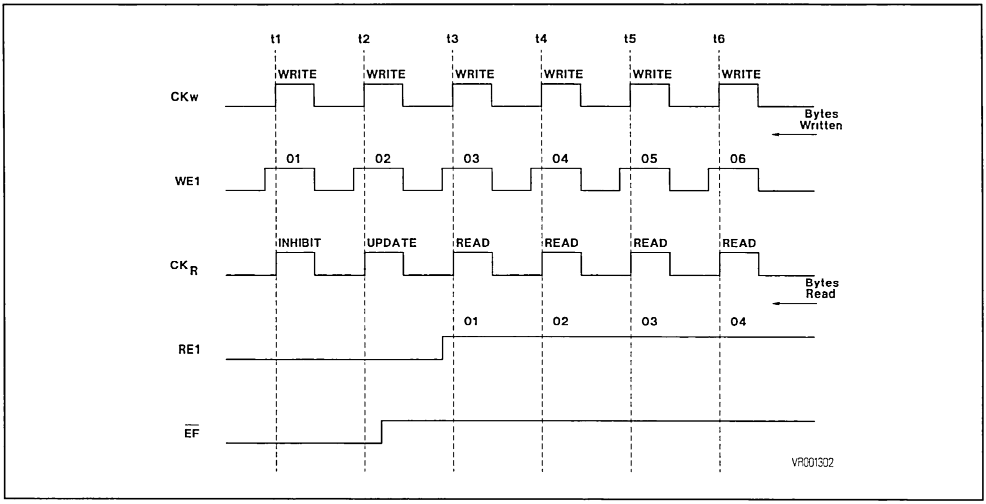


Figure 6. True Empty Flag Operation



Valid) follows $\overline{EF}$ by one cycle. All to say that these flags are latched with $\overline{EF}$ and $\overline{FF}$ as well. Their design function constitutes the handshake control for depth expansion.

TRUE FLAG OPERATION

As with other FIFOs, the MK4505 requires a reset pulse to initialize all internal counters before normal operation begins. Since the $\overline{EF}$ is latched active low after reset, two read clocks are needed to gate valid data out of the FIFO. The first rising edge of CK_R to occur t_{FFL} (First Flag Latency) after the first write will clear the Empty Flag ($\overline{EF}$ = high) within t_{F1A}. Read clocks less than t_{FFL} after the first write may clear the $\overline{EF}$, but are not guaranteed. The second rising edge of CK_R to ocur t_{FRL} (First Read Latency) after the first write will gate valid data onto the outputs provided RE_1 is active high. This is the expected "fall through" delay time, and is calculated as : $t_S + t_{FRL} + t_A$. This is true for asynchronous or simultaneous write/read operations. It should be noted that the RE_1 input should be held inactive until t_{FFL} has been satisfied, thereby observing the t_{FRL} parameter. This will ensure true $\overline{EF}$ operation ; see Figure 6. (Although WE_1 is clocked in this example, it is not mandatory for proper device operation noted by RE_1).

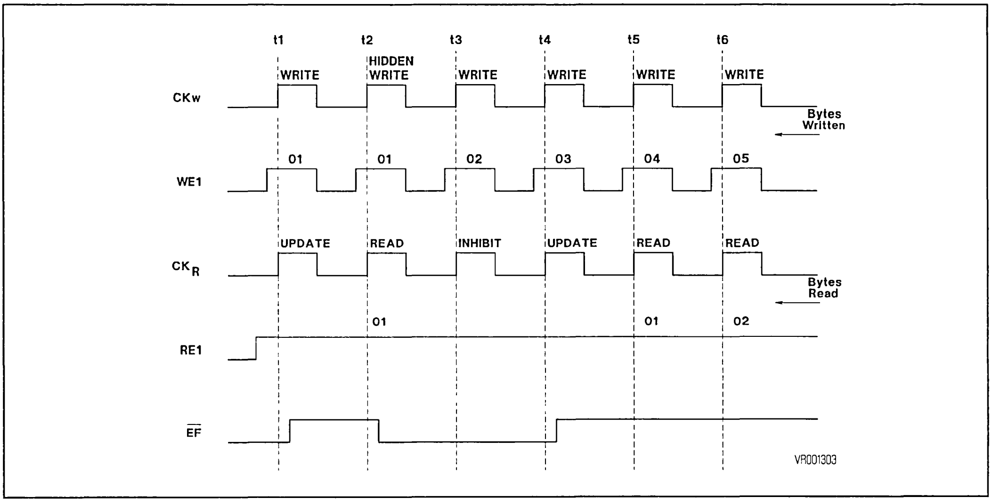
If the MK4505 is written to full where $\overline{FF}$ is latched low, two write clocks are required before more data is written into the FIFO. The rising edge of CK_W on the last available byte of data latches the $\overline{FF}$ low within t_{F1A}. Once $\overline{FF}$ is latched low, the first rising edge of CK_W to occur after the first valid read will clear the $\overline{FF}$ status ($\overline{FF}$ = high). The second rising edge of CK_W will write data into the FIFO provided WE_1 is active high. These latched flag functions are a benefit of the MK4505's clocked design, and pipeline architecture. They provide write protection when full, and read protection when empty.

FALSE FLAG AMBIGUITY

There are certain situations and conditions that can result in improper device operation and probable unexpected status flag results. These conditions can occur with the $\overline{EF}$ or $\overline{FF}$ during asynchronous or simultaneous write/read operations. The worse case scenario being simultaneous write/read operations when near or at Empty or Full. Remembering that this is an edge triggered device that latches logic states by using a pipeline architecture, the internal arbiter will give priority to the read operation when a simultaneous write/read cycle occurs on the **last byte** of data. This results in the $\overline{EF}$ being latched low even though a valid write occurred at the same time. This is the design definition for the $\overline{EF}$ flag in a pipeline architecture being updated on the rising edge of CK_R. The actual last byte of data must be read without a simultaneous write, as this can "trap" one byte of data in the FIFO until a subsequent valid write is detected, the t_{FFL} parameter is again satisfied to CK_R, and $\overline{EF}$ is cleared ($\overline{EF}$ = high).

This can be best explained by the diagram in Figure 7. If all operations were truly simultaneous, the false $\overline{EF}$ would not occur. In an actual system, however, the rising edges of CK_W and CK_R can become slightly skewed by a few nanoseconds in a simultaneous write/read operation. In the False

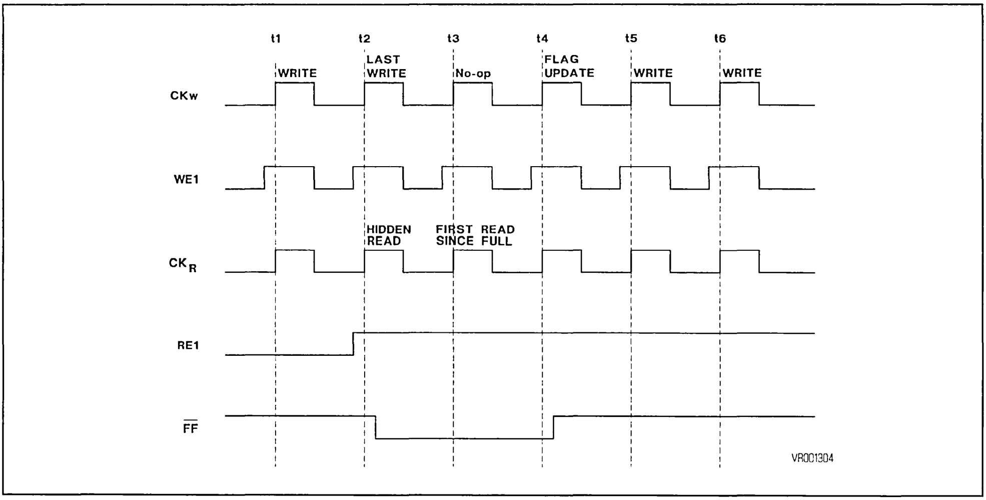
Figure 7. False Empty Flag


t1
t2
t3
t4
t5
t6
WRITE
HIDDEN WRITE
WRITE
WRITE
WRITE
WRITE
CKw
Bytes Written
01
01
02
03
04
05
WE1
UPDATE
READ
INHIBIT
UPDATE
READ
READ
CKR
Bytes Read
01
01
02
RE1
EF
VR001303

Flag Diagram, the rising edge of CK_R is presumed to occur slightly **after** CK_W at t1, and slightly **before** CK_W at t3. The $\overline{EF}$ update circuitry is annulled at t2 because $\overline{EF}$ is high, and waits to determine a valid write while $\overline{EF}$ **is low**. This example results in improper device operation as t_{FFL} and t_{FRL} are not satisfied, and an unexpected $\overline{EF}$ status is displayed. Therefore, if RE_1 is kept disabled t_S prior to t3 as in the True Flag diagram, or if CK_R occurs just before or exactly with CK_W at t1, then t_{FFL} is satisfied at t2, t_{FRL} is observed at t3, and the unexpected empty condition will not occur. The $\overline{EF}$ flag will function as anticipated without "trapping" data by allowing the writes to stay one ahead of the reads. This allows successful data transmission with asynchronous or simultaneous write/read cycles.

Since $\overline{EF}$ and $\overline{FF}$ are both latched flags, the same type of false flag can be encountered with the $\overline{FF}$. Referring to Figure 8, one can see that a simultaneous write/read on the **last available write** results in $\overline{FF}$ being latched low even though a valid read occurred at the same time. Due to the pipeline

Figure 8. False Full Flag


t1
t2
t3
t4
t5
t6
WRITE
LAST WRITE
No-op
FLAG UPDATE
WRITE
WRITE
CKw
WE1
HIDDEN READ
FIRST READ SINCE FULL
CKR
RE1
FF
VR001304

design, the arbiter gives priority to the write, thus latching the $\overline{\text{FF}}$ low. The $\overline{\text{FF}}$ will not be cleared until a subsequent rising edge of CKw **occurs after the first valid read.** The $\overline{\text{FF}}$ update circuitry is annulled at t2 because $\overline{\text{FF}}$ is high, and waits to determine a read while $\overline{\text{FF}}$ **is low**. This is the design definition for the latched Full Flag in a pipeline architecture being updated by CK$\overline{\text{W}}$.

SUMMARY

The MK4505 clocked FIFO provides latched Empty and Full flags guaranteeing a stable logic state for at least one complete cycle. This allows ease of use in a clocked system environment by ensuring that set-up and hold times are met for a subsequent cycle in reference to the system clock. Since $\overline{\text{FF}}$ and $\overline{\text{EF}}$ provide the MK4505 with automatic write protection when Full, and read protection when Empty, the designer needs to understand their design definition for proper device operation. When compared to previous ripple-through FIFOs, the latched $\overline{\text{EF}}$ and $\overline{\text{FF}}$ can result in an unexpected or false flag status. In reference to the latched Empty Flag, should the $\overline{\text{EF}}$ logic present a problem of trapping data in a given clocked system as previously described, the AE signal can be used as an option. By using the Almost Empty condition (Almost Empty by 8 bytes) for Empty, one can detect AE for system logic commands, perform a valid simultaneous write/read operation, and still read the **last byte** of data written. This will avoid a false flag situation, and allow the system to retrieve all expected data.

CONCLUSION

In this application brief, we have highlighted some subtle benefits and operations of the MK4505 clocked FIFO in regards to latched status flags. Obviously, the MK4505 demands certain design considerations when compared to previous ripple-through type FIFOs like the MK4501. By providing latched $\overline{\text{EF}}$ and $\overline{\text{FF}}$ flags, the MK4505 ensures proper operation for set-up and hold times in a clocked system environment. Previous ripple-through FIFOs cannot within themselves ensure proper set-up and hold times in a clocked system design. Therefore, the MK4505 makes design easier, and takes the worry out of interfacing a FIFO with a system operating on a periodic or free-running clock.

SGS-THOMSON
MICROELECTRONICS

APPLICATION NOTE

THE MK4505 MASTER/SLAVE WIDTH EXPANSION

INTRODUCTION

The MK4505 from SGS-THOMSON offers high performance, high density First-In-First-Out operation, and supports two asynchronous periodic clock inputs for read/write operations. The device is designed for applications where data is moving through a system on the rising edge of a free running clock, and allows simultaneous or asynchronous read/write operations. The basic concepts of the MK4505 clocked FIFO are described in an application note entitled : The MK4505 Clocked FIFO Introductory Concepts", publication number AN219. The ideas described in this brief will help first time users in understanding the different functional concepts with the MK4505 from previous low and high density FIFOs.

The main difference between the MK4505 and other FIFOs is that all operations are initiated on the rising edge of the read or write clocks, CK_R and CK_W respectively (see Figure 1 for device pinout).

PIN NAMES

D0 - D4	Data Input
Q0 - Q4	Data Output
CK_W , CK_R	Write and Read Clock
WE_1	Write Enable Input 1
RE_1	Read Enable Input 1
$\overline{RS}$	Reset (active low)
HF	Half Full Flag
V_{CC} , GND	5Volts, Ground

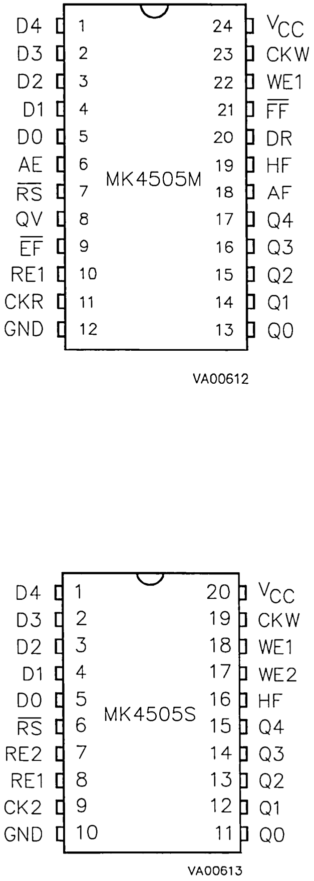
(4505M only)

$\overline{FF}$, $\overline{EF}$	Full and Empty Flag (active low)
AF , AE	Almost Full, Almost Empty Flag
DR , QV	Input Ready, Output Valid

(4505S only)

WE_2	Write Enable Input 2
RE_2	Read Enable Input 2 (rising edge triggered 3 state control)

Figure 1. Pin Connections


D4 1
D3 2
D2 3
D1 4
D0 5
AE 6
RS 7
QV 8
EF 9
RE1 10
CKR 11
GND 12
24 VCC
23 CKW
22 WE1
21 FF
20 DR
19 HF
18 AF
17 Q4
16 Q3
15 Q2
14 Q1
13 Q0
MK4505M
VA00612
D4 1
D3 2
D2 3
D1 4
D0 5
RS 6
RE2 7
RE1 8
CK2 9
GND 10
20 VCC
19 CKW
18 WE1
17 WE2
16 HF
15 Q4
14 Q3
13 Q2
12 Q1
11 Q0
MK4505S
VA00613

INTRODUCTION (Continued)

This particular application brief will discuss read and write cycles for the MK4505M (Master), and the MK4505S (Slave) as separate devices, as well as their cascadable application. Width expansion will be reviewed as Master-to-Slave and Slave-to-Slave. Master-to-Master width expansion is not allowed. Each device has a 1K x 5 bit organization, and is width expandable to at least 40 bits with no additional logic. Cycle times range from 20 to 40MHz with access times of 15 to 25ns.

MK4505M/S (MASTER/SLAVE) CONCEPT

The MK4505M/S (Master/Slave) concept provides for easy width and depth expansion capability by using one MK4505M for each 1024 bits of depth, and one MK4505S for each additional 5 bits of width. For most applications, the Master-to-Slave width expansion configuration offers the best solution. A full set of status flags is offered by the MK4505M, and thereby providing all of the necessary controls signals to the Slave. The Master-Slave width expansion arrangement gives the system designer worry free operation from word skew ambiguities that can be realized due to status flag access times during asynchronous read/write operations. The MK4505M is supplied in a 300mil, 24 pin plastic DIP, and the MK4505S comes in a 300mil, 20 pin plastic DIP which gives additional savings in printed circuit board space. An example of some simple read and write timing diagrams are shown in Figures 2 and 3 showing the differences of the MK4505M and MK4505S as stand-alone devices. These figures presume that the Master is neither full or empty.

SLAVE WIDTH EXPANSION

The key difference between the MK4505M and MK4505S is that the Master has on-chip write protection when full, and read protection when empty, whereas the Slave offers no overflow or underflow protect circuitry. The MK4505S can be used as a stand-alone device or in width expansion without the Master, but this forfeits the automatic read/write protect circuitry offered in the MK4505M. Even if no read cycles occur, previously written data will be over-written within 1025 write cycles. Of course data can also be re-read if no write cycles occur within 1025 read operations. A reset operation will also allow the user to re-read data with the MK4505S. However, during reset both the read and write pointers are reset to location (address) zero. Additionally, during reset the half full ($\overline{HF}$) counters will be initialized.

An example schematic of Slave-to-Slave width expansion is shown in Figure 4. The previous read/write diagrams in Figures 2 and 3 are also examples of the MK4505S (Slave) width expansion timing. Since the MK4505S allows continual read and write cycles, the MK4505S can be used in applications where data underflow and overflow to the FIFO cannot occur, or where data underflow and/or overflow is desired or doesn't matter. Here the Slave will offer high performance with additional board space reductions. The MK4505S also offers a rising edge triggered three state output bus control. Whenever RE2 is LOW at the rising edge of CK_R, the Qs will be high-Z at t_{QZ} from the rising edge of CK_R.

MASTER/SLAVE WIDTH EXPANSION

As previously mentioned, the Master/Slave width expansion offers a full compliment of status flags and all necessary control signals for proper operation. The MK4505M provides a high impedance data bus after reset, and whenever the FIFO is empty. An example schematic of MK4505M/S width expansion is shown in Figure 5. This example is presuming a data bus width of 32 bits with an additional 3 bits. The additional bits could be used to pass decode information or other control status information. Mas-ter/Slave width expansion timing is displayed in Figure 6. This figure shows an initial reset with flag status, and First Read Latency (tFRL) after First Write, and finally write until full with read disabled (RE1 = LOW). Additionally, the read and write clocks are asynchronous at different cycle rates.

The logic state of the DR status flag follows the $\overline{FF}$ status flag, and is updated with each rising edge of the write clock (CK_W). The QV status flag follows $\overline{EF}$ by one cycle respective to the rising edge of CK_R. The DR and QV outputs are latched status flags, with their main function being to incorporate Master-to-Master depth expansion, or Master-to-Slave with and depth expansion (refer to the MK4505M/S data sheet). Therefore, DR (Data Ready) and QV (Output Valid) are offered as optional status flags to be monitored by the user in Master-Slave with expansion mode. They are totem-pole outputs, and can be left disconnected in this configuration.

DESIGN CONSIDERATIONS

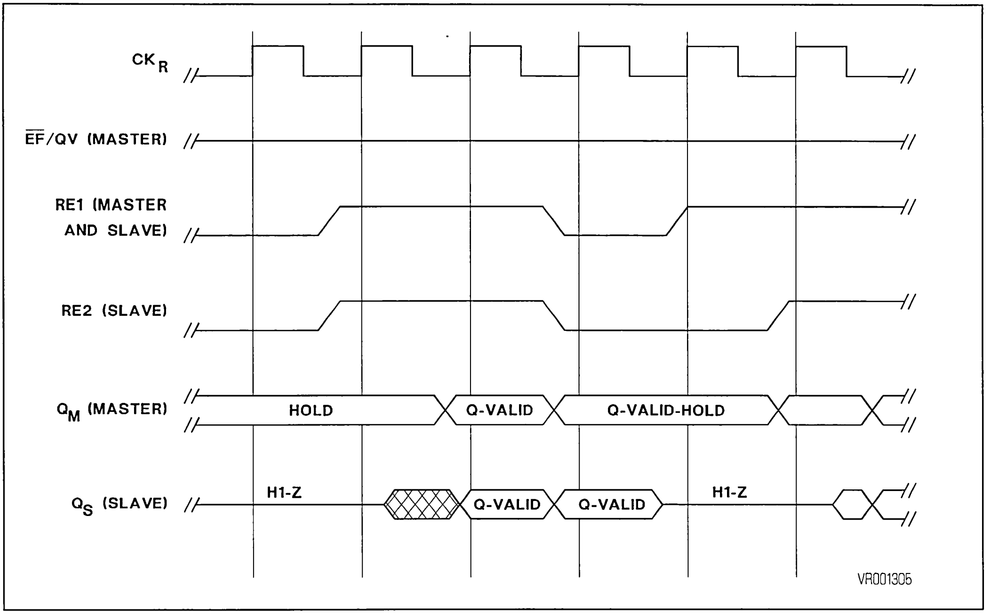
As with all FIFO applications, a reset is required to initialize all counters before normal operation begins. Referring again to the MK4505M/S data sheet, the user must take into account the first valid read delay access time from the first valid write operation after reset. This is the expected "fall-through delay time" calculated as : $t_S + t_{FRL} + t_A$. The t_S parameter being the set-up time to the First Write operation ; t_{FRL} is the First Read Latency as the First Read clock delay after the First Write ; and t_A is the Q output access time from the First Valid Read Clock. The MK4505M provides read protect circuitry via the $\overline{EF}$ status flag, therefore read operations will not be allowed until the $\overline{EF}$ is cleared. Thus first valid data after reset has a maximum of 75ns for a 40MHz cycle.

When using the MK4505S separately, the user must observe the t_{FRL} parameter to ensure First-Write-to-First Read valid data. Once t_{FRL} is satisfied, valid data is guaranteed on the Q outputs at t_A from the rising edge of CK_R. Read operations attempted before t_{FRL} is satisfied may result in reading RAM locations not yet written. Since the Slave offers no read or write protect circuitry, the user must observe t_{FRL}, especially when using free running asynchronous read/write clocks on the MK4505S.

CONCLUSION

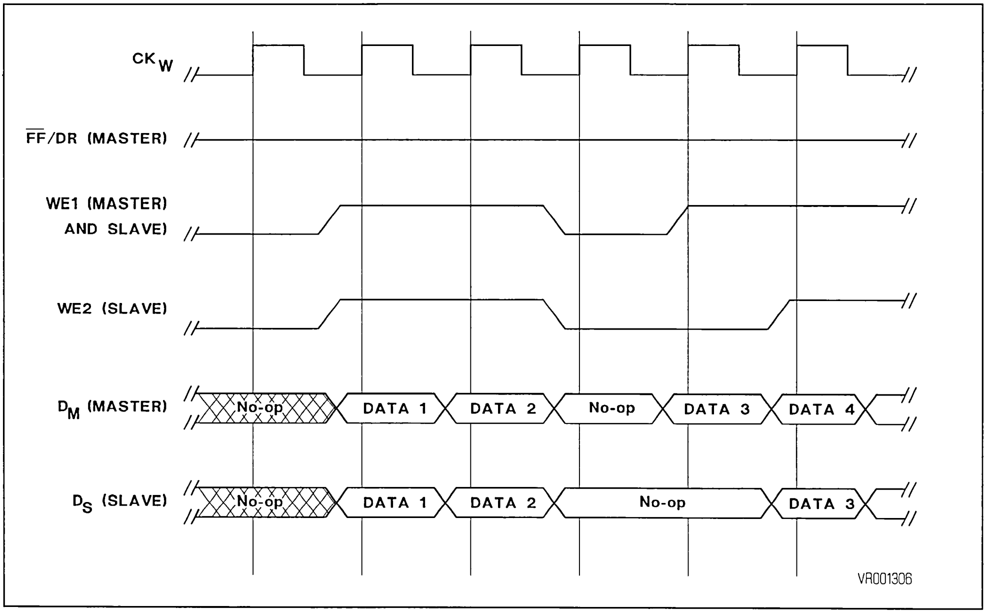
The MK4505M/S offers width expansion to any line or word size, and at least 40 bits of width without additional support circuitry. Master-to-Slave width expansion has a full compliment of status flags as well as Slave control logic for proper operation. The MK4505S is also width expandable with certain res-trictions. The MK4505M cannot be written while FULL, or read when EMPTY ; whereas, the MK4505S allows continuous read/write operations. Master-to-Master width expansion is not allowed. Both devices use the SGS-THOMSON Microelectronics BiPORT™ RAM based memory cell allowing simultaneous read/write operations, and a 1k x 5 pipeline architecture giving the MK4505 an unsurpassed 15ns access time with a 25ns cycle time.

Figure 2. Read Timing


CK R
EF/QV (MASTER)
RE1 (MASTER AND SLAVE)
RE2 (SLAVE)
QM (MASTER)
HOLD
Q-VALID
Q-VALID-HOLD
QS (SLAVE)
H1-Z
Q-VALID
Q-VALID
H1-Z
VR001305

Note : Waveforms for master or slave stand-alone operation.

Figure 3. Write Timing


CK W
FF/DR (MASTER)
WE1 (MASTER) AND SLAVE)
WE2 (SLAVE)
DM (MASTER)
No-op
DATA 1
DATA 2
No-op
DATA 3
DATA 4
DS (SLAVE)
No-op
DATA 1
DATA 2
No-op
DATA 3
VR001306

Note : Waveforms for master or slave stand-alone operation.

Figure 4. Slave width Expansion

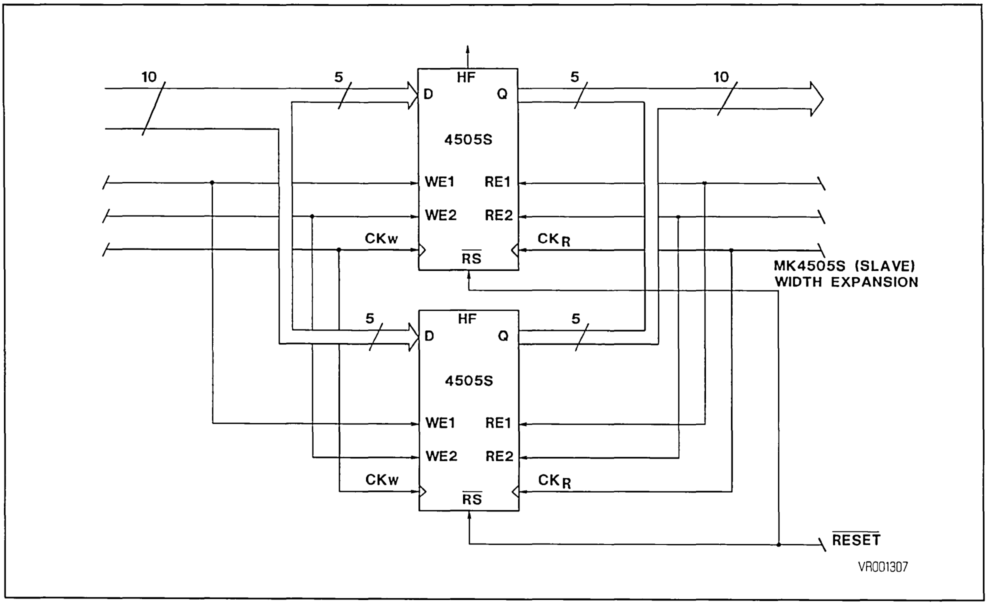

10
5
HF
D
Q
4505S
WE1
RE1
WE2
RE2
CKw
CKR
RS
5
10
MK4505S (SLAVE)
WIDTH EXPANSION
5
HF
D
Q
4505S
WE1
RE1
WE2
RE2
CKw
CKR
RS
5
RESET
VR001307

Figure 5. Master/Slave width Expansion

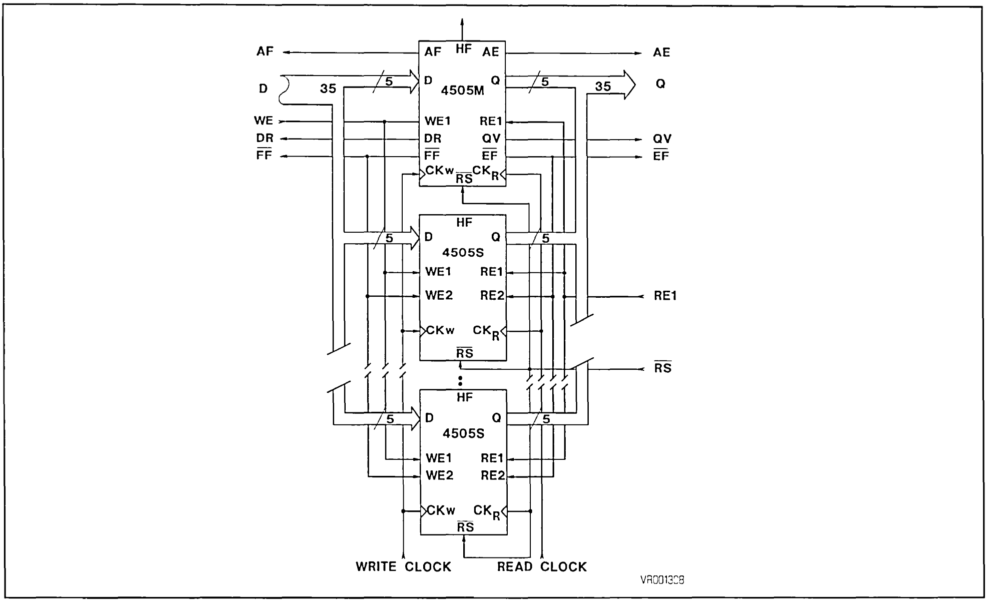
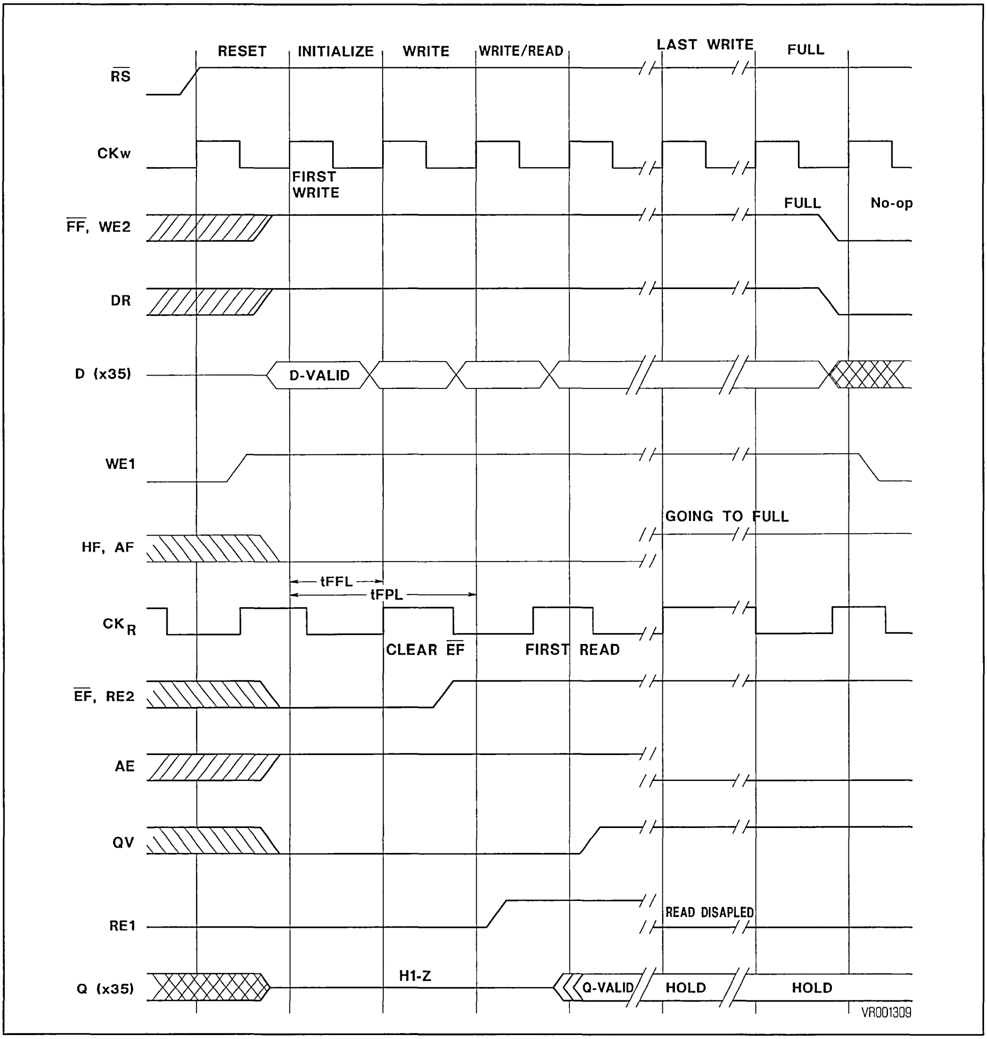

AF
D
35
WE
DR
FF
AF
HF
AE
D
4505M
Q
5
5
35
AE
Q
WE1
RE1
DR
QV
FF
EF
CKw
RS
CKR
QV
EF
HF
D
Q
4505S
5
5
WE1
RE1
WE2
RE2
RE1
CKw
CKR
RS
RS
HF
D
Q
4505S
5
5
WE1
RE1
WE2
RE2
CKw
CKR
RS
WRITE CLOCK
READ CLOCK
VR001308

Figure 6. Master-to-Slave width Expansion Timing Write/Read/Write-to-Full


RESET
INITIALIZE
WRITE
WRITE/READ
LAST WRITE
FULL
$\overline{RS}$
CKw
FIRST WRITE
$\overline{FF}$, WE2
FULL
No-op
DR
D (x35)
D-VALID
WE1
GOING TO FULL
HF, AF
tFFL
tFPL
CK_R
CLEAR $\overline{EF}$
FIRST READ
$\overline{EF}$, RE2
AE
QV
RE1
READ DISAPLED
Q (x35)
H1-Z
Q-VALID
HOLD
HOLD
VR001309

MICROWIRE EEPROM COMMON I/O OPERATION

Bernard SABY

SGS-THOMSON Microelectronics provides a wide range of serial access EEPROMs. The MICROWIRE™ product line is designed for a 4-wire interface: SK the Clock input, CS the Chip Select Input, DI the Serial Data Input, and DO the Serial Data Output. Some MCUs such as the SGS-THOMSON ST9 or ST7 series include a Serial Peripheral Interface (SPI) "on-chip", that can fit this MICROWIRE interface, but those EEPROMs can be used with any general purpose microcontroller where the interface wires are hooked to I/O ports or some equivalent circuitry.

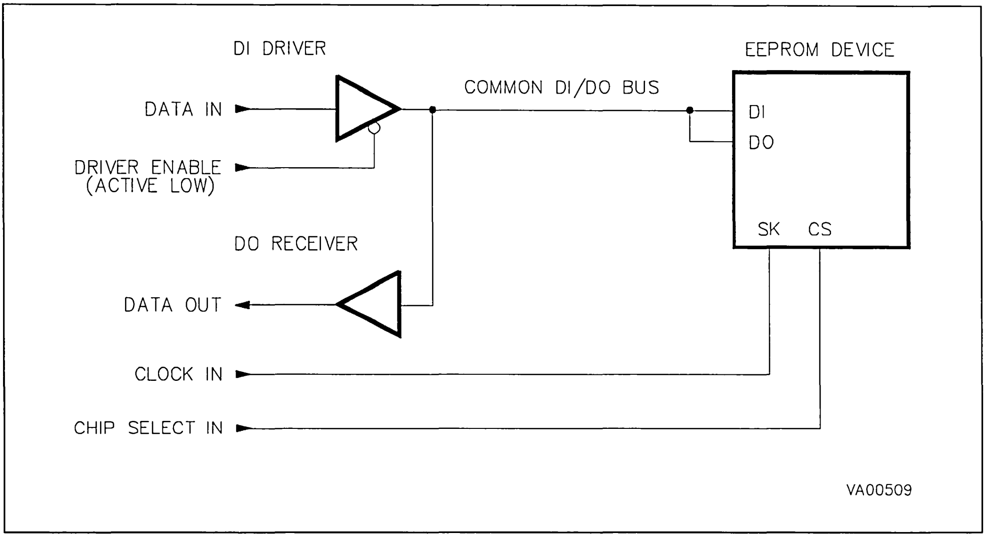
Since DO output is in high impedance while instructions, addresses and data are shifted into the DI serial input, it seems attractive to tie DI and DO pins together to provide a common DI/DO bus. The chips can operate correctly in this configuration, provided that appropriate design rules are carefully followed. The possible troublesome situations are limited to the instructions where DO output is activated.
Such instructions include: READ,WRITE, ERASE, WRAL and ERAL.

This note reviews and details the specific points where precautions must be taken in common DI/DO applications. In order to provide the designer with a safe-design guide, all calculations are carried out upon the worst case values as specified in the data sheet of these EEPROM devices.

READ INSTRUCTION

Let's consider a typical common DI/DO application (as in Figure1). The DI driver and the DO receiver can be discrete logic or part of a microcontroller I/O port or any equivalent circuitry.
DO pin is in high impedance while the READ opcode and the address bits are clocked into the chip upon the rising edge of SK clock. These bits must be kept valid for a minimum hold time of t_{DIH}: see data sheet. However, upon the rising edge of SK where the last address bit (A0) is clocked into DI, the DO pin comes out of high impedance and outputs the leading bit (logical 0) which precedes the 16 bit data string (see example in Figure 2).

Figure 1. Typical Common DI/DO Application



The maximum delay between the rising edge of SK and the leading "0" bit is specified for a maximum of t_{PD0} (between 500 ns and 1μs, depending on the product); nevertheless, typical values of less than 100 ns can be found.

Since the DI driver must remain enabled with the A0 bit for a minimum of t_{DIH} (hold time) before being disabled, a bus conflict will occur if the A0 bit is a "1" (odd address registers). The consequences are:

- a low impedance path is created between V_{CC} and ground through DI driver and the on-chip DO out-

Figure 2. Read Instruction Example

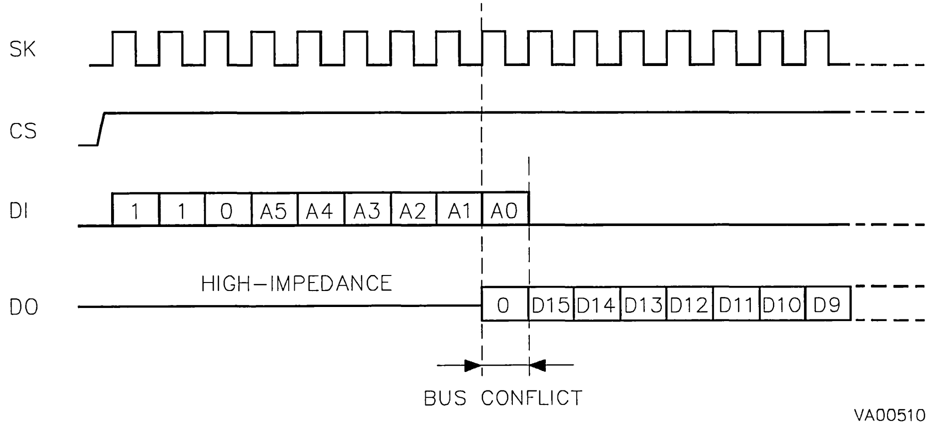
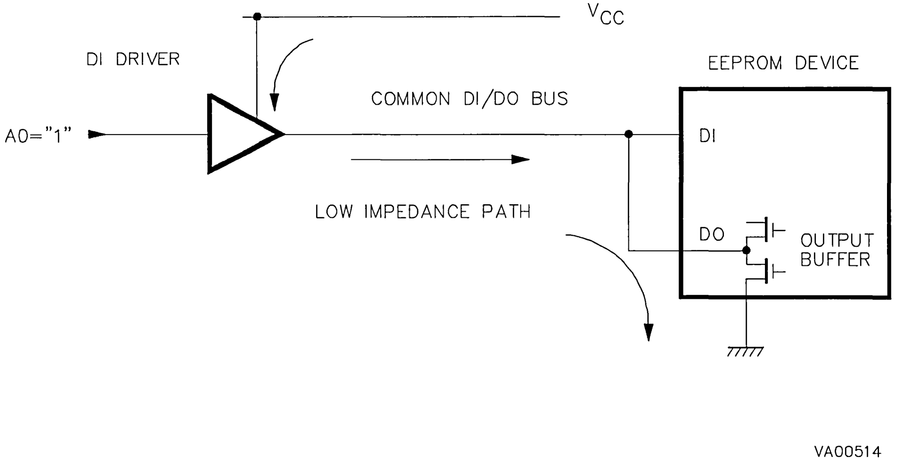

SK
CS
DI
1
1
0
A5
A4
A3
A2
A1
A0
HIGH–IMPEDANCE
DO
0
D15
D14
D13
D12
D11
D10
D9
BUS CONFLICT
VA00510

Figure 3. Short-Circuit between V_{CC} and Ground


VCC
DI DRIVER
EEPROM DEVICE
COMMON DI/DO BUS
A0="1"
DI
LOW IMPEDANCE PATH
DO
OUTPUT BUFFER
VA00514

put buffer (see Figure 3); this short-circuit may produce glitches on the power supply which can disturb all the circuits on the board;

- the logical level on the DI/DO bus is not well-defined as it is the result of the relative driving capability of the DI driver and the DO output buffer; the DI pin can even see a logical "0" preventing the access of the odd address registers.

This trouble can be solved by inserting a current limiting resistor in the sinking current path. Figure 4 shows some possible locations for this resistor; however, the best location is between the DO out-

Figure 4. Possible Locations for the Current Limiting Resistor

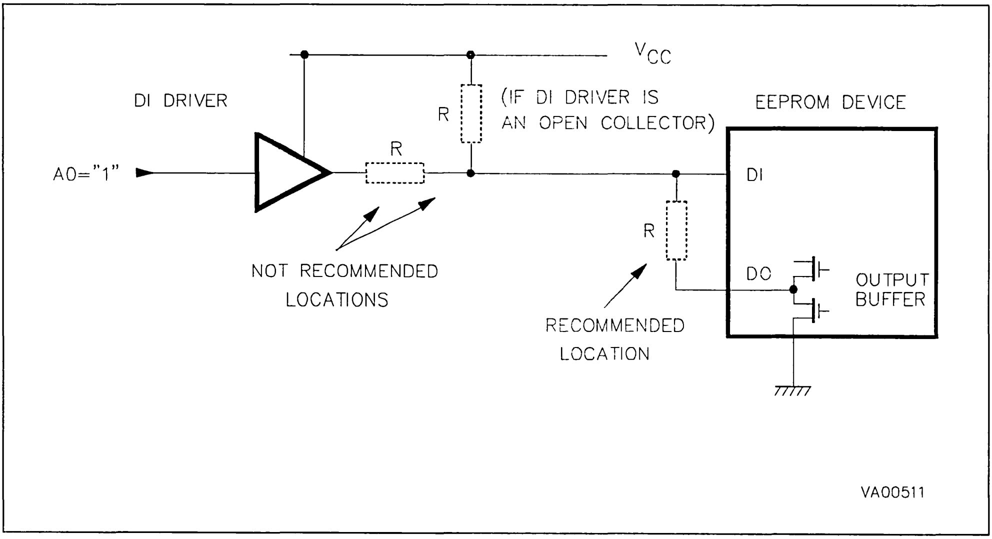
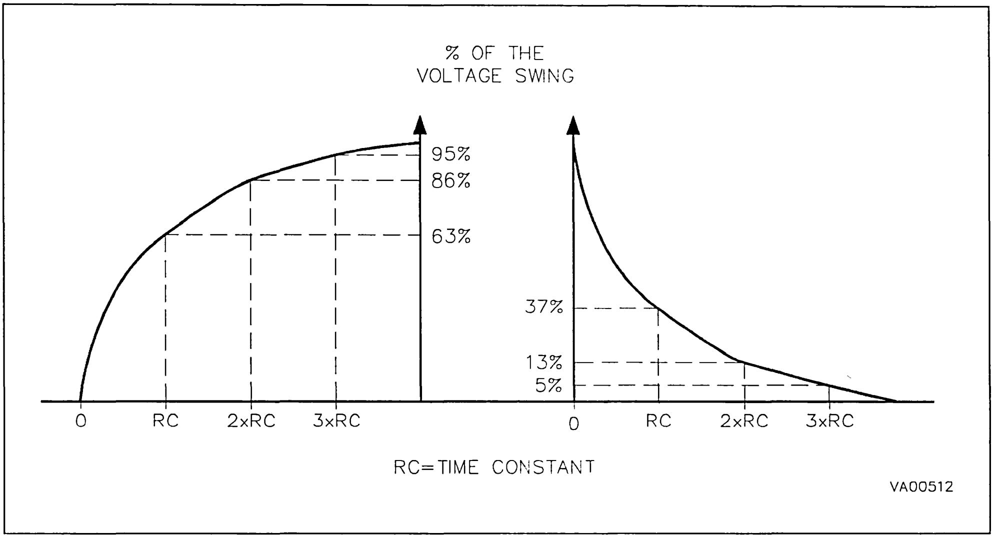

VCC
DI DRIVER
R
(IF DI DRIVER IS AN OPEN COLLECTOR)
EEPROM DEVICE
R
A0="1"
DI
R
DO
OUTPUT BUFFER
NOT RECOMMENDED LOCATIONS
RECOMMENDED LOCATION
VA00511

Figure 5. Exponential Charge and Discharge of the Bus Capacitance



put and the DI/DO bus for the following reasons:

- during the overlap time, the logical level on the DI/DO bus will be defined by the DI driver only, allowing the respect of the t_{DIH} hold time specification.
- as we discuss later, the R resistor slows down the propagation time of the DO output signals on the DI/DO bus, but only the 16 bits of data read from the chip are affected. If R were in series with the DI driver, all the input signals for all the instructions would be slowed down in the same way.

The R resistor doesn't have any effect as long as DO is in high impedance. During the execution of a READ instruction, R sinks some current from the DI driver during the short overlap time; then the DI driver is disabled and DO output takes control of the DI/DO bus through the R resistor.
Because of the bus capacitance C, the signals are distorded: the rising and falling edges of DO output are transformed into exponential curves whose shape depends on the time constant RC (see Figure 5).

The consequence is: after a rising edge of SK clock, the logical level on the DI/DO bus needs some delay before being considered as steadily established and ready to be sampled by the DO receiver. This safety delay can be estimated to be at least 3xRxC; after sampling, the subsequent rising edge of SK can occur.
When applying the results of Figure 5 to the worst case of DO output levels (see data sheet): V_{OH} min = 2.4 V, V_{OL} max = 0.4 V, Voltage Swing = 2 V, the DI/DO bus levels will be:

- logical "1" = 2.3 V minimum for a delay of 3xRC
- logical "0" = 0.5 V maximum after SK rising edge

It will be necessary to reduce the SK clock frequency when and only when shifting the 16 bits of data out from the EEPROM. All other operations can be performed at the nominal clock rate.

This reduction is of course directly related to the RC time constant of the DI/DO bus. Figures 6, 7, 8 show some experimental examples replotted from the scope with different values of R and C.

In the last example, the maximum clock frequency is: 1 / 3xRC = 100 KHz, assuming that DI/DO bus is sampled by the DO receiver circuitry just before the rising edge of the SK clock.

In order to avoid an important reduction of the clock frequency, the following techniques can be used which minimize the R and C values:

Figure 6. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, RC = 1 µs

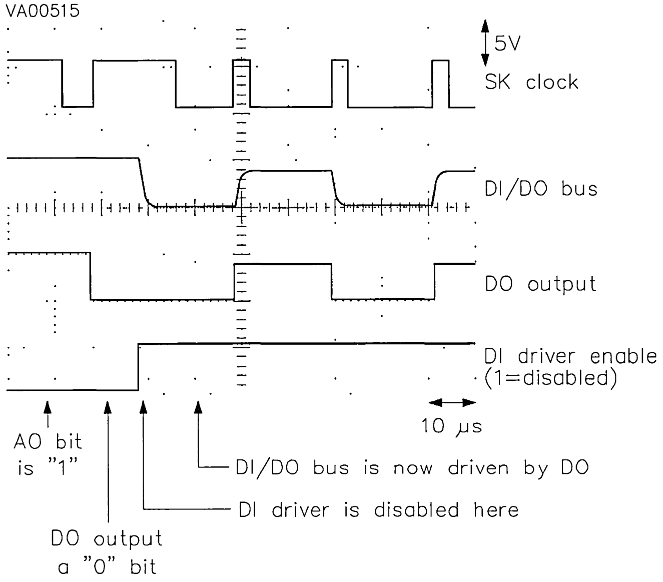


Figure 7. Oscilloscope Plot, R = 5 kΩ, C = 100 pF, RC = 500 ns

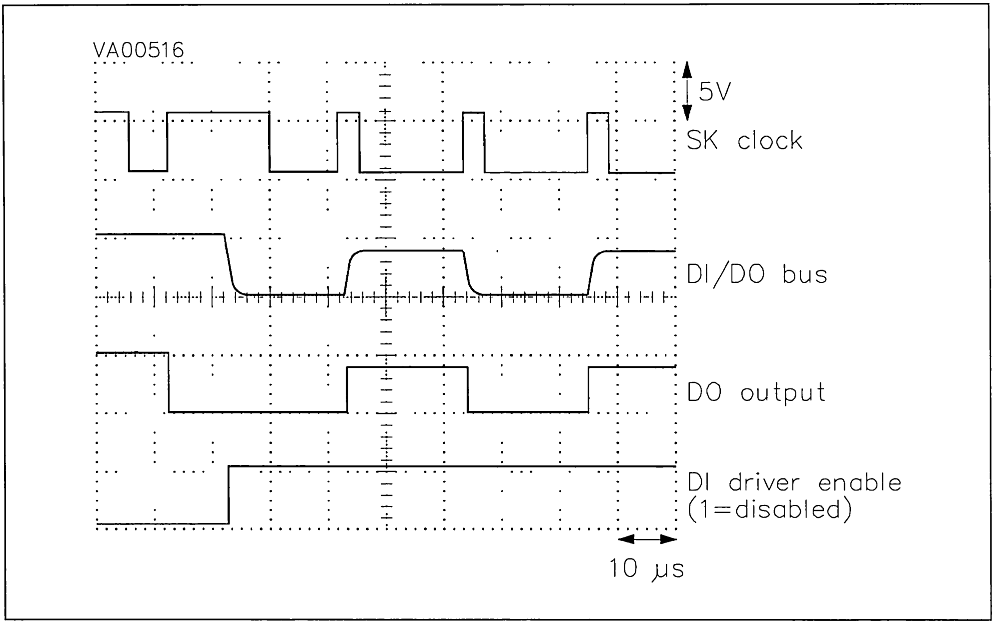
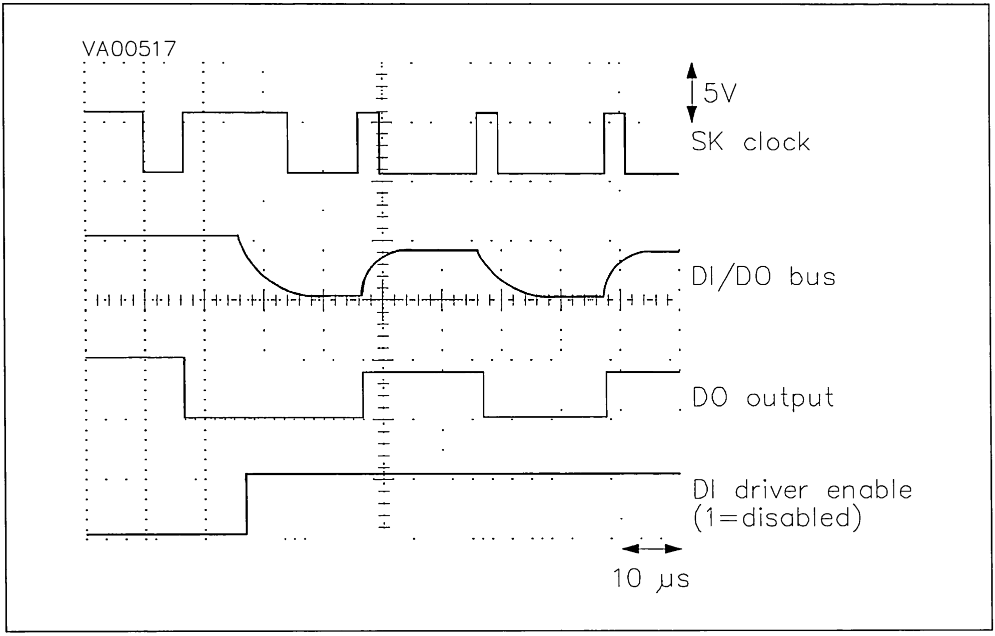


Figure 8. Oscilloscope Plot, R = 10 kΩ, C = 330 pF, RC = 3.3 µs



- to minimize the bus capacitance, it is important to implement the EEPROM device as close as possible to the DI driver/DO receiver circuitry for the shortest connection, and not share too many devices on the same DI/DO bus since the capacitance will be proportionnal to the number of devices connected in parallel to the same DI/DO bus.
- the value of the R resistor can be decreased as long as the DI driver can source the corresponding amount of current during the bus conflict time and as long as the power supply is adequately decoupled to withstand this transient of current. It's up to the designer to decide about the best trade-off based upon his specific application's requirements.

INTERFACE WITH CMOS CIRCUITS

The MICROWIRE EEPROM devices are specified for TTL compatible input/output levels; when using CMOS circuits to interface these devices, some precautions must be taken to ensure the correct interpretation of the logical levels.

Since the CMOS output-high levels are close to V_{CC} and output-low level close to 0V, it is obvious that there are no difficulties in driving the DI, CS and SK inputs of the EEPROM devices.

Concerning the DO output, the minimum output-high level is specified to 2.4 V, which is lower than the minimum input high level of CMOS (3.5 V for V_{CC} = 5 V). A common practice is to connect a pull-up resistor Rp between the DO output and V_{CC}, thus increasing the effective high-level in order to meet the CMOS specs.

Although this configuration suits perfectly to a separate DI and DO, it raises some difficulties in common DI/DO applications.

When DO output is a "zero" level, i.e. V_{OL}= 0.4 V, worst case conditions, the R and Rp resistors act together as a voltage divider on the DI/DO bus (see Figure 9); hence, the Rp resistor value must be at least 5 times greater than R value and the "zero" level on the DI/DO bus is:

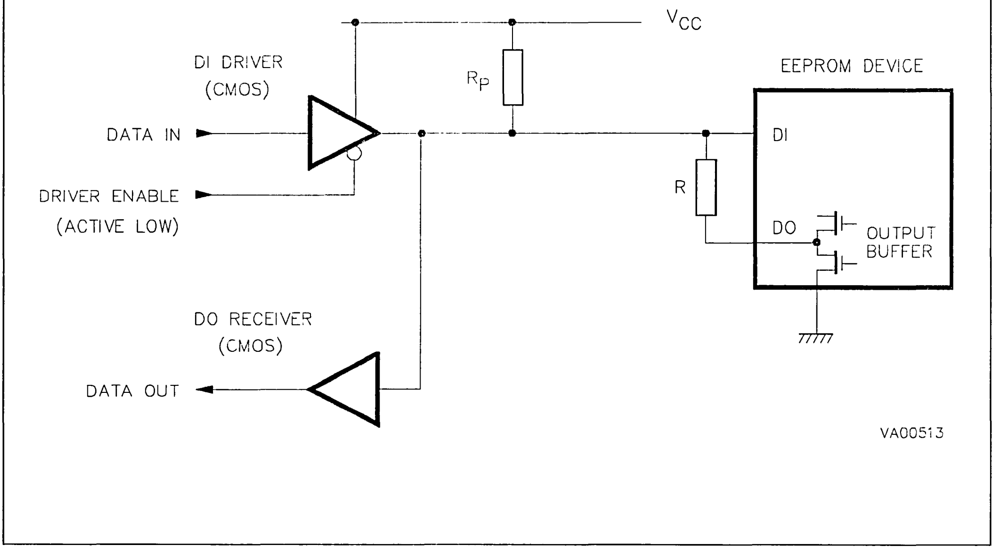
$$0.4\text{ V} + (5\text{ V} - 0.4\text{ V}) \times R / (R + Rp) = 1.17\text{ V}$$

when Rp = 5xR

Although this value is 330 mV below the 1.5 V, maximum "zero" input level of CMOS, the wide noise margin traditionally associated with CMOS is then significantly reduced.

For a "1" to "0" transition, the DO output on-chip buffer will have to discharge the bus capacitance through the R resistor and to sink some current from the V_{CC} through Rp resistor. In that case, we may

Figure 9. DI/DO Bus Configuration with Pull-up Resistor (Rp)



see that the new time constant is equal to the product of the bus capacitance C with the parallel combination of R and Rp, which is 17% smaller than the one without Rp. However, the steady "0" level is no more 0.4 V, as we assumed for TTL levels but 1.17 V as calculated above (if Rp = 5xR). Despite of this smaller time constant, the voltage swing between "0" and "1" is greater in this case (see later on); hence it is advised before sampling to keep the same "rule of the thumb" delay of 3xRC after the SK clock rising edge.

The major problem is for the "0" to "1" transition. During a first step, the bus capacitance is charged through DO output in series with R and the Vcc power supply in series with Rp. These conditions lead to the same time constant as above (i.e. 17% smaller than the one without Rp).

But once the DI/DO bus voltage reaches the DO output level, the DO on-chip buffer is automatically turned off and the Rp resistor remains the only contributor to the charge of the bus capacitance, resulting into a much higher time constant: RpxC = 5xRxC (if Rp = 5xR).
If we consider the worst case "1" output level for DO (V_{OH}= 2.4 V), it lasts a long time to go up to 3.5 V, which is the minimum "1" input level for CMOS. It will last exactly 0.55xRpC (if Vcc = 5 V) or 2.75xRC after the DO output turn off, and we must add a reasonable noise margin (300 or 400 mV).
As a result: the minimum delay between the rising edge of SK and the sampling of the DI/DO bus should be 2 or 3 times longer than the one we've found for the TTL levels (without Rp), and the clock frequency must be reduced as much.
It is possible to avoid this situation by using a TTL level compatible input CMOS device such as the 74HCTXXX devices as DO receiver circuit, or a CMOS microcontroller that provides a "TTL input levels" option on its I/O ports, such as the ST9 series, and thus get rid of this Rp resistor.

PROGRAMMING MODE: ACKNOWLEDGEMENT OF READY/BUSY STATUS

On the MICROWIRE EEPROM devices, the self-timed programming cycle uses DO output to indicate the ready/busy status of the chip.
The self-timed programming cycle begins with the falling edge of CS at the end of a programming instruction; such instructions include: WRITE, ERASE, WRAL and ERAL.

Figure 10. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, Rp = 50 kΩ

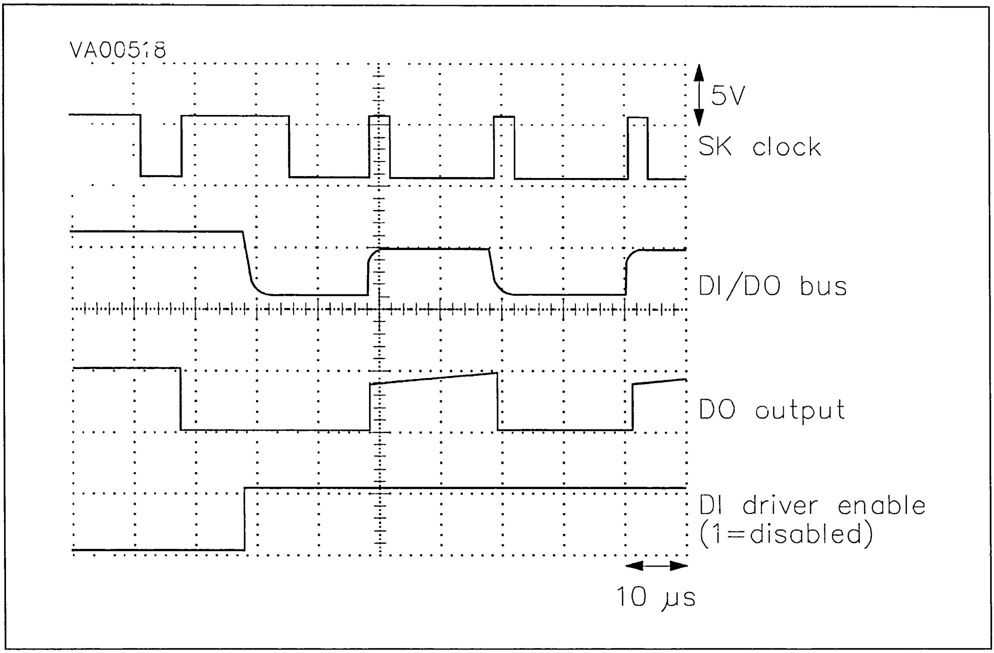
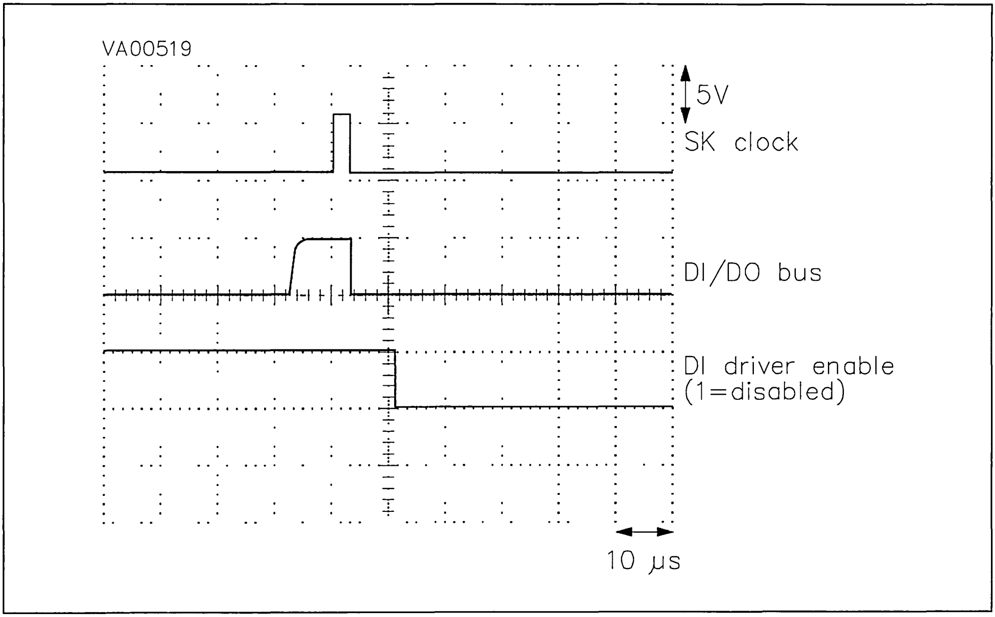


Figure 11. Acknowledge of the Ready/Busy Signal on DO Output



CS pin must be kept low for a minimum of t_{CS} (see data sheet). DO output remains in high impedance as long as CS is low; if CS is brougth high for clocking a new instruction, DO comes out of high impedance state and indicates the Ready/Busy status of the chip (0 = Busy, 1= Ready).
In common DI/DO applications, this may create again a bus conflict; therefore, it is recommended to cancel this status signal: this is very simply done by applying a single clock pulse on SK input while CS is high (see Figure 11).

The operation is scheduled as follows:

- shift into the chip a programming instruction
- bring CS low for t_{CS} minimum
- bring CS high
- monitor DI/DO bus till a "1" level is detected (Ready)
- clock SK once
- bring CS low
- the chip is ready to accept a new instruction

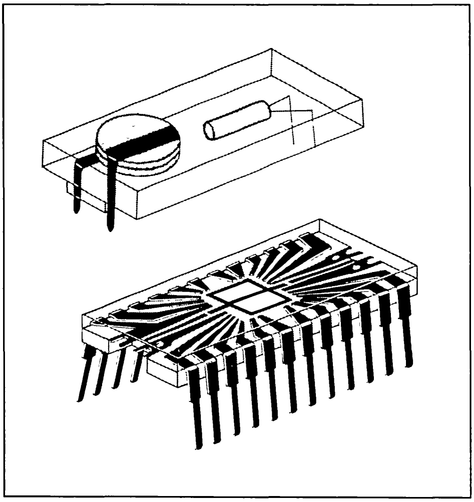
It should also be noted that this Ready/Busy status can be found active after the power-up of the chip; therefore, it is recommended to clock SK once (with CS = 1) prior to any instruction.

CONCLUSION

This note gives some guidelines for the possibilities and the conditions of a safe operation in common DI/DO applications. The safety of these designs is based on the good safety margins and the worst case data sheet values used in the calculations. These calculations are of course not exhaustive, each designer may adapt them for any given application.

APPLICATION NOTE

ENSURING DATA INTEGRITY IN ZEROPOWER AND TIMEKEEPER RAMs



The ZEROPOWER™ and TIMEKEEPER™ product families offer a unique non-volatile RAM solution. ZEROPOWER products consist of a single chip containing an ultra low power SRAM, a comparator for power supply voltage detection and battery control logic. TIMEKEEPERs include, in addition, a real time clock which loads clock/calendar information into specific locations of the memory array.

The monolithic ZEROPOWER and TIMEKEEPER chips are packaged in 600 mil wide dual-in-line plastic packages with 24 or 28 pins. The "top-hat" housing attached to the top of the DIP package contains the battery and also a crystal for the TIMEKEEPER products.

The products operate as conventional SRAMs when external power is applied. They have standard SRAM footprints and fast read and write access times. When the applied power supply drops below the specified threshold, the control circuitry write protects the memory. At a lower voltage the internal battery supplies power to maintain the data

ZEROPOWER Main Part Numbers

Size	Type	Organisation	Vcc Trip	Feature
16K	MK48C02	2K x 8	4.75 V	No battery
	MK48Z02	2K x 8	4.75 V	
	MKI48Z02	2K x 8	4.75 V	–40 °C to 85 °C
	MK48Z12	2K x 8	4.5 V	
	MKI48Z12	2K x 8	4.5 V	–40 °C to 85 °C
64K	MK48Z08	8K x 8	4.75 V	Power Fail Interrupt
	MK48Z09	8K x 8	4.75 V	
	MK48Z18	8K x 8	4.5 V	
	MKI48Z18	8K x 8	4.5 V	–40 °C to 85 °C
	MK48Z19	8K x 8	4.5 V	Power Fail Interrupt

TIMEKEEPER Main Part Numbers

Size	Type	Organisation	V_{CC} Trip	Feature
16K	MK48T02	2K x 8	4.75 V	
	MK48T12	2K x 8	4.5 V	
64K	MK48T08	8K x 8	4.75 V	Power Fail Interrupt
	MK48T18	8K x 8	4.5 V	Power Fail Interrupt

in the SRAM and power the real time clock until the system power becomes valid again.

Correct operation of the ZEROPOWER and TIMEKEEPER products requires the usual design considerations for high speed SRAM systems, however some additional points which sometimes give rise to incorrect operation are discussed below.

Data Corruption or Loss

Negative Undershoots. Loss or corruption of the data in the entire address space of the RAM can be caused by negative undershoots of more than 0.3V occurring on the device pins during a power cycle. Negative undershoots are often the result of improper termination of the signal lines. A resistor network can be used to correctly terminate the signal lines and prevent reflections and undershoots.

Inadvertent Writes. Corruption of data in isolated bytes of the SRAM after a power cycle can be caused by inadvertent write cycles occurring on power up. Inadvertent writes can occur before the system stabilizes but after the ZEROPOWER or TIMEKEEPER is active. The memory should be protected against writing during the start-up phase and the signals are stable, by gating the system RESET with the memory CHIP ENABLE, as shown in Figure 1.

Low or Noisy Power Supplies. ZEROPOWER and TIMEKEEPER products have well specified windows for the power supply voltage within which they deselect or reselect. These windows are specified as either 4.75V to 4.5V or 4.5V to 4.2V. During normal operation the supply voltage for the products must exceed the maximum window value. If however, during a memory access, the supply volt-

Figure 1. Gating of the system RESET and memory CHIP ENABLE for MK48Z02, MK48T02 and MK48Z08

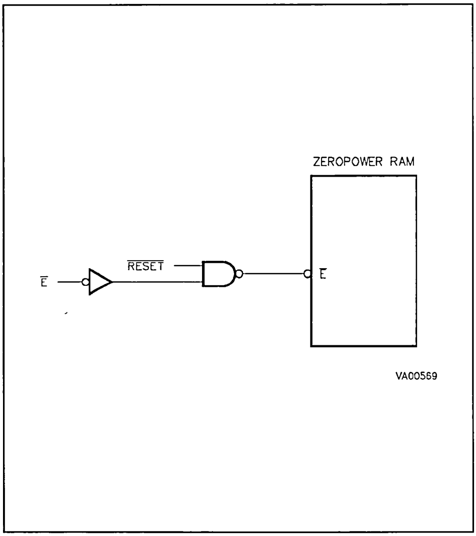
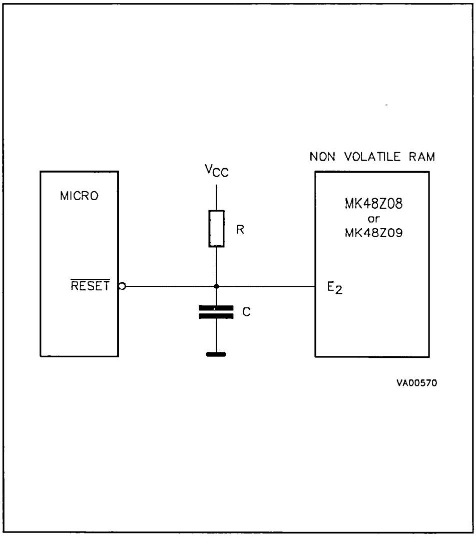


Figure 2. Power on reset using E2 input of the MK48Z08 or MK48Z09



age drops into the deselect window, an invalid read or write to the ZEROPOWER or TIMEKEEPER may occur. Power supply fluctuations caused by current transients can be reduced through the use of a supply bypass capacitor mounted close the memory package. A suggested value is 0.01 μF. If the system power supply is low and cannot be modified easily to bring it within specification, a change in the product type from a 5% to a 10% tolerance part may cure instances of unwanted deselection and apparent data corruption or loss.

TIMEKEEPER Clock Errors

Setting Unused Bits in Clock Registers. Within the eight bytes of clock/calendar information, contained in the memory array of the TIMEKEEPER products, are a number of bits which are specified as 'unused', but which must be written to zero. Some of these bits control internal test modes which speed up the clock in order to efficiently test the products at the factory. The bits are always set to zero before shipment, but if an application sets these bits a test mode may be invoked and the clock may run erratically. In a test mode the clock may run extremely fast or the seconds may not roll over to minutes after 60 counts. Software routines addressing the control registers should specifically set the unused bits to zero.

Immediate Access of Clock Information after a Power Up. During normal operation of the TIMEKEEPER products, the memory locations of the SRAM that contain the clock/calendar information are updated by the internal clock counter once per second. When a TIMEKEEPER is in the battery back-up mode, no updates to the memory locations occur. After a power up, the actual time is transferred to the memory locations one second after the product reselects. Thus access to the clock information in the memory in less than one second after a power up may yield the same information that was present at power down, not the new time.

The precautions described above are the most frequent that many users enquire about, it is hoped that this brief Application Note will provide a fast solution.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

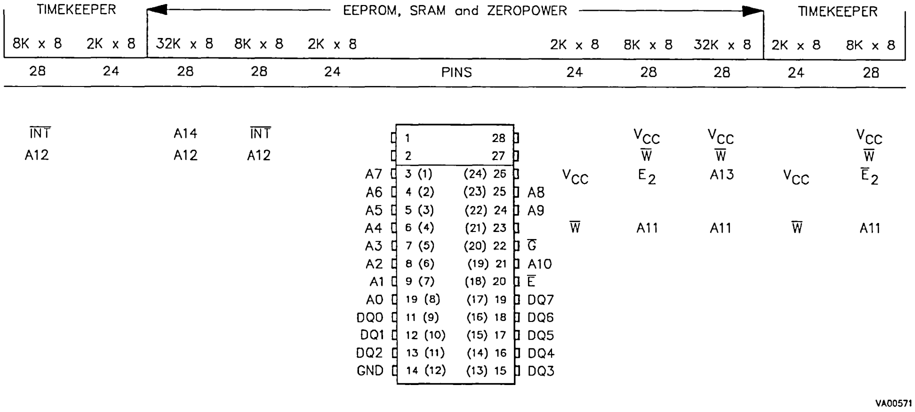
UPGRADED MEMORY CAPABILITY USING ZEROPOWER AND TIMEKEEPER PRODUCTS

Systems that need read/write non-volatile memory have several choices available: EEPROM, SRAM plus battery or the ZEROPOWER™ and TIMEKEEPER™ products from SGS-THOMSON. Many microprocessor based systems require a non-volatile memory for storing vital data such as calibration constants, set up parameters, adaptable boot programs or other routines, systems status or clock & calendar information. Consequently many systems from computer and POS terminals, video games, process controllers, medical equipment, trip computers, PABXs, to TV sets are using non- volatile memories today.

EEPROM memory access times are fast for data reading (100-200ns) but relatively slow (5-10ms) for writing which means that in many system applications data has to be copied in fast RAM and written to the EEPROM only when neccessary. Standard SRAMs can be incorporated directly into the memory map of processors since they have fast, equal read and write speeds. However additional circuitry must be designed to monitor the power supply and switch them over to battery back-up operation to make them non-volatile. A perfect solution to the need for non-volatile RAM is provided by the SGS-THOMSON ZEROPOWER and TIMEKEEPER RAMs which provide an SRAM together with battery back-up and the power supply and switch over circuitry in a single package. In addition the TIMEKEEPER products include a real time clock providing year, month, day, date, hour, minute and second information which may be read from locations in the SRAM address space.

System designers can adopt a flexible solution to non-volatile memory by making a PC board layout which will allow users to have an easy upgrade from

Figure 1. Signal definitions for 24 and 28 pin DIP


TIMEKEEPER
EEPROM, SRAM and ZEROPOWER
TIMEKEEPER
8K x 8
2K x 8
32K x 8
8K x 8
2K x 8
2K x 8
8K x 8
32K x 8
2K x 8
8K x 8
28
24
28
28
24
PINS
24
28
28
24
28
$\overline{INT}$
A12
A14
A12
$\overline{INT}$
A12
1
2
3 (1)
4 (2)
5 (3)
6 (4)
7 (5)
8 (6)
9 (7)
19 (8)
11 (9)
12 (10)
13 (11)
14 (12)
28
27
(24) 26
(23) 25
(22) 24
(21) 23
(20) 22
(19) 21
(18) 20
(17) 19
(16) 18
(15) 17
(14) 16
(13) 15
A7
A6
A5
A4
A3
A2
A1
A0
DQ0
DQ1
DQ2
GND
A8
A9
$\overline{G}$
A10
$\overline{E}$
DQ7
DQ6
DQ5
DQ4
DQ3
V_{CC}
$\overline{W}$
V_{CC}
$\overline{W}$
E_2
A11
V_{CC}
$\overline{W}$
A13
A11
V_{CC}
$\overline{W}$
V_{CC}
$\overline{W}$
$\overline{E}_2$
A11
VA00571

one solution to another. Three jumpers can be used to select the use of 2k x 8, 8k x 8 or 32k x 8 EEPROM, standard SRAMs or ZEROPOWER/ TIMEKEEPER products. Product enhancements can be easily made by changing, for example, an EEPROM to a TIMEKEEPER. This would retain the non-volatile memory, but would add the ability for fast reading and writing of the memory and have a real time clock available. Typical benefits from using the TIMEKEEPER would be to timestamp events such as data transfers or files.

The standard pin out for 2k to 32k memories is based on either a 24 or 28 pin dual-in-line package. Figure 1 shows in the center a 24 or 28 pin package with the signal definitions for the 2k x 8 memory - which can be an SRAM, EEPROM or ZEROPOWER product in 24 pin DIP. The difference in the signal definitions for each type and size of memory are show to the left and right.

Table 1 gives the full listing of memory types and the jumper connections corresponding to the circuit of Figure 2. The PC board is provided with 28 connections, but only the lower 24 are used for smaller memory sizes. Pin 2 is jumpered across to either the $\overline{INT}$ line for the TIMEKEEPER MK48T08, or the A14 address line for the larger 32k x 8 EEPROM, SRAM or MK48Z32 ZEROPOWER products. Pin 26 is jumpered across to one of three signals, the supply Vcc for smaller memories of 2k x 8 capacity including the ZEROPOWER MK48Z02, the second chip enable $\overline{E}2$ for the TIMEKEEPER MK48T08 or the address line A13 for larger memories of 32k x 8 capacity including the MK48Z32. The third jumper on pin 23 connects to either the write line $\overline{W}$ for 2k x 8 EEPROM, SRAM and ZEROPOWER/TIMEKEEPER products or to A11 for the 8k x 8 and larger 32k x 8 sizes.

Figure 2. Jumpers for pins 1, 23(21) and 26(24)

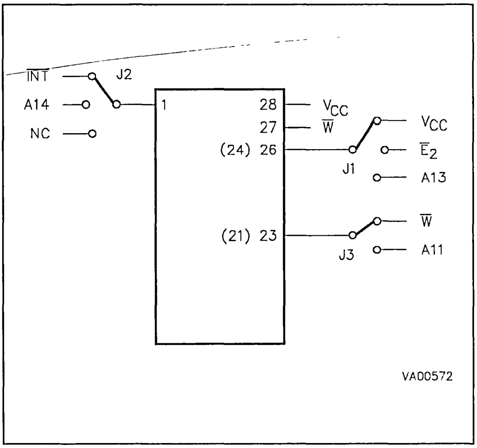


Table 1. Jumper positions for each type of memory

Type	Part Number	Size	J1	J2	J3
EEPROM		2K x 8	V_{CC}		$\overline{W}$
		8K x 8			A11
		32K x 8	A13	A14	A11
SRAM		2K x 8	V_{CC}		$\overline{W}$
		8K x 8			A11
		32K x 8	A13	A14	A11
ZEROPOWER	MK48Z02	2K x 8	V_{CC}		$\overline{W}$
	MK48Z08	8K x 8			A11
	MK48Z09	8K x 8	E2	$\overline{INT}$	A11
	MK48Z19	8K x 8	E2	$\overline{INT}$	A11
	MK48Z32	32K x 8	A13	A14	A11
TIMEKEEPER	MK48T02	2K x 8			$\overline{W}$
	MK48T08	8K x 8	$\overline{E2}$	$\overline{INT}$	A11
	MK48T18	32K x 8	$\overline{E2}$	$\overline{INT}$	A11

TIMING SPECIFICATIONS

There has been for some years misunderstandings about the definition and specification of memory timing parameters. Many companies have used different timing names and different waveform diagrams. Sometimes parameters are not clearly and unequivically defined.

Timing parameter names have historically tended to describe the functions of the time, for example:

– t_{AH}	Address Hold time
– t_{DH}	Data Hold time
– t_{ACC}	Access time

These names do not describe very well the actual time specified, t_{AH} does not say hold time from what, to what. t_{ACC} does not specify whether this is the time from, for example, addresses valid or from chip enable asserted.

A better system is to follow that outlined by JEDEC. This uses both signal names and logic states to define the timing parameters.

The system follows the rules as in the example "t_{1234}", where 1 and 3 specify the signal names (negative logic signals eg. $\overline{E}$ are shown without the negation bar), for example:

– Q	Data Output
– D	Data Input
– E	Chip Enable
– G	Output Enable
– A	Addresses
– W	Write Enable

and, 2 and 4 specify the logic level as in Figure 2 and follows:

– H	a Low to High transition to above a High level measurement threshold
– L	a High to Low transition to below a Low level measurement threshold
– V	valid signals, above High or below Low measurement levels
– X	transition or invalid signals, signals that are possibly changing and are below a high level or above a low measurement level.

Figure 1. Signal Names

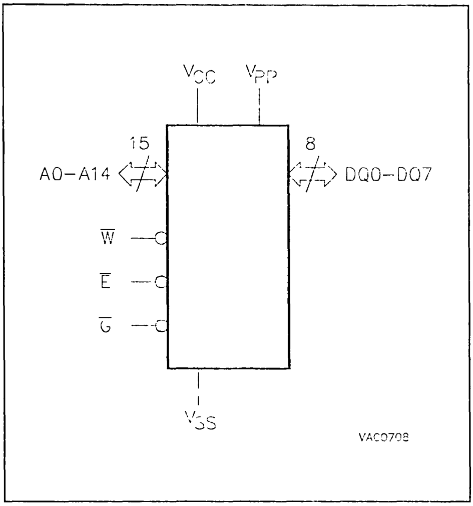
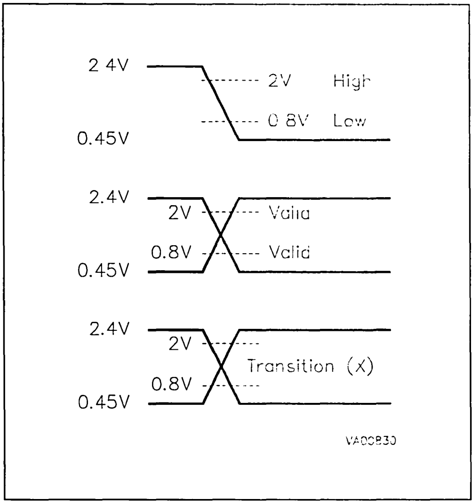


Figure 2. Input Output Waveforms References



Note: High. Low, Valid and Transition (X) levels

Some examples of these definitions, with the name it replaces, are in Table 1.

Table 1. Timing Characteristics Example

Symbol	Alt	Parameter
t_{AVAV}	t_{RC}	Read Cycle Time
t_{AVQV}	t_{ACC}	Address Valid to Output Valid
t_{ELQX}	t_{LZ}	Chip Enable Low to Output Transition
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid
t_{GLQX}	t_{OLZ}	Output Enable Low to Output Transition
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid
t_{EHQZ}		Chip Enable High to Output Hi-Z
t_{GHQZ}	t_{DF}	Output Enable High to Output Hi-Z
t_{AXQX}	t_{OH}	Address Transition to Output Transition

Note: These are taken from the FLASH MEMORY data sheets.

MEASUREMENT CONDITIONS

The signal measurement conditions are also important for the definition of timings, there are three important definitions,

The input signal rise and fall time. Although, in theory, no timings depend on this - that is the definition of parameters is not dependant on the rise or fall time of the input signals - some products may have characteristics which vary with the slew rate of the input.

The levels of the input signal. Both the Low level and High level voltage. These obviously must be at least equal to the specified V_{IL} and V_{IH} for the device input signals.

The voltage level at which the timing measurement starts and stops.

For example, for EPROMs the SGS-THOMSON specification states:

- Input Rise and Fall times are 20ns max
- Input and Output signal levels are 0.4V(min) to 2.4V(max)
- Input and Output timing reference levels are 0.8V(Low) to 2.0V(High)

and, a signal is defined as Hi-Z (high impedance) when it is not driving or being driven.

USING THIS SYSTEM

The system then works, for example, like here after described.

A time specification of t_{AVQV} means a time from the point where the address lines are ALL below 0.8V for signals at or going to a logic Low level and above 2.0V for those at or going to a High logic level, to a time where the data output signals are ALL either below 0.8V or above 2.0V.

A time specification of t_{EHQZ} means a time from the chip enable input going above 2.0V to the point where the data output is no longer driving.

A time specification of t_{AXQX} means a time from the point where any single address line rises above or falls below its stable, valid level (0.8V for Low level or 2.0V for High level), to the point where any data output line transition passes these levels and is consequently no longer valid.

TIMING DIAGRAMS

The use of these definitions makes it unneccessary to draw the timing diagrams with times shown from a notional high or low measurement point, as the measurement points are clearly specified by the definition of measurement conditions and the signals and logic are described by the timing parameter description. The diagrams can be simplified for maximum clarity and understanding by indicating, diagrammatically, the timings from the waveform center point.

For example, if the measurement conditions for timing are specified as:

- Input Voltage levels are 0.45 to 2.4V
- Input and Output reference levels are 0.8 to 2V

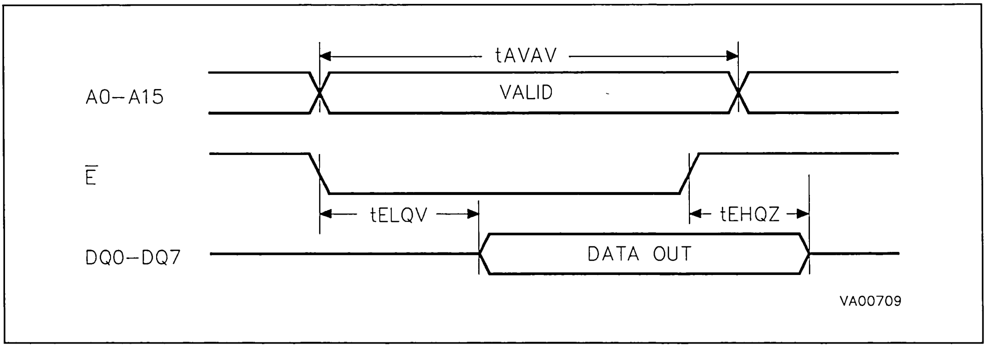
and, Output Hi-Z is defined as the point where the signal is no longer driving; then in the diagram:

- t_{AVAV} is measured from the point where all address lines are either above 2V or below 0.8V to the same levels at the end of the cycle.
- t_{ELQV} is measured from $\overline{E}$ Low, or below 0.8V to the point where all data lines are either above 2V or below 0.8V.
- t_{EHQZ} is measured from $\overline{E}$ High, or above 2V, to where the data outputs are no longer driving the signal lines.

Note that the t_{ELQV} timing, for example, is shown diagramatically not from a "low" point on the $\overline{E}$ falling edge, but from the center and is shown not to a "high/low" point on the Data Output but again to the center. This is for clarity of the diagram, as the actual measurement points are clear from the definitions and timing names.

This system has been, or will be, adopted for all SGS-THOMSON memory products.

Figure 3. Timing Diagram Example


tAVAV
A0–A15
VALID
E̅
tELQV
tEHQZ
DQ0–DQ7
DATA OUT
VA00709

TAPE AND REEL PACKING

by Antony WATTS

Surface mounting packages can be supplied with Tape and Reel packing. The reels are standard 330 mm diameter and contain between 250 and 2500 devices.

The packages supplied on Tape and Reel are listed in Table 1, with their body width in "mils". This table also shows the Tape Width and Part Pitch used, and the quantity per reel.

The reels used are either plastic antistatic or conductive with a black conductive cavity tape, the cover tape is transparents antistatic or conductive.

Devices are orientated in the cavities with the identifying pin (normally pin 1) on the same side as the sprocket holes in the tape.

Table 1. Packages on Tape and Reel

Package Type	Body Width	Description	Tape Width (W)	Part Pitch (P)	Q.ty per Reel
PSO8	150 mils	Plastic Small Outline	12 mm	8 mm	2500
PSO14	150 mils	Plastic Small Outline	16 mm	8 mm	2500
PSO16	150 mils	Plastic Small Outline	16 mm	8 mm	2500
PSO14	300 mils	Plastic Small Outline	16 mm	12 mm	2000
PSO16	300 mils	Plastic Small Outline	16 mm	12 mm	2000
PSO20	300 mils	Plastic Small Outline	24 mm	12 mm	1000
PSO24	300 mils	Plastic Small Outline	24 mm	12 mm	1000
PSOJ28	300 mils	Plastic Small Outline J-lead	24 mm	12 mm	1000
PSOJ28	330 mils	Plastic Small Outline J-lead	24 mm	12 mm	1000
PSOJ28	340 mils	Plastic Small Outline J-lead	24 mm	12 mm	1000
PLCC20	–	Plastic Leaded Chip Carrier	16 mm	12 mm	1000
PLCC28	–	Plastic Leaded Chip Carrier	24 mm	16 mm	500
PLCC32	–	Plastic Leaded Chip Carrier	24 mm	16 mm	750
PLCC44	–	Plastic Leaded Chip Carrier	32 mm	24 mm	500
PLCC52	–	Plastic Leaded Chip Carrier	32 mm	24 mm	500
PLCC68	–	Plastic Leaded Chip Carrier	44 mm	32 mm	250
PLCC84	–	Plastic Leaded Chip Carrier	44 mm	36 mm	250

Figure 1a. Reel

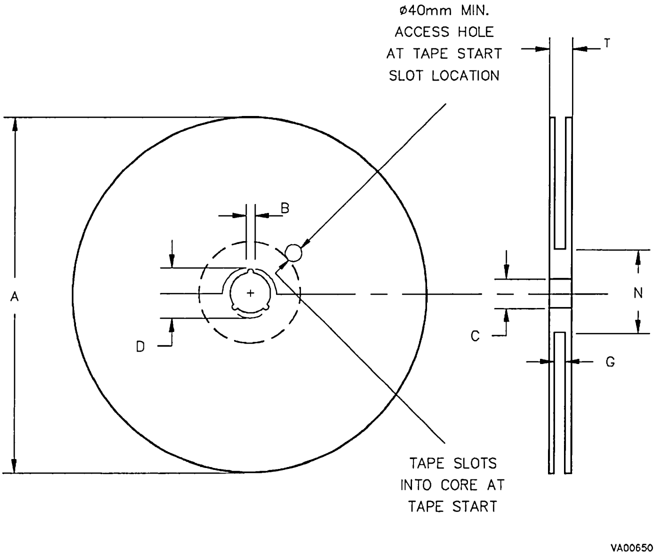

ø40mm MIN.
ACCESS HOLE
AT TAPE START
SLOT LOCATION
T
B
A
D
C
N
G
TAPE SLOTS
INTO CORE AT
TAPE START
VA00650

Figure 1b. Reel Dimensions

Tape Size	A Max	B Min	C	D Min	N Min	G	T Max	Unit
12 mm	330	1.5	13 ± 0.2	20.2	50	12.4 +2 / -0	18.4	mm
16 mm	330	1.5	13 ± 0.2	20.2	50	16.4 +2 / -0	22.4	mm
24 mm	330	1.5	13 ± 0.2	20.2	50	24.4 +2 / -0	30.4	mm
32 mm	330	1.5	13 ± 0.2	20.2	50	32.4 +2 / -0		mm
44 mm	330	1.5	13 ± 0.2	20.2	50	44.4 +2 / -0		mm

Figure 2. Leader and Trailer

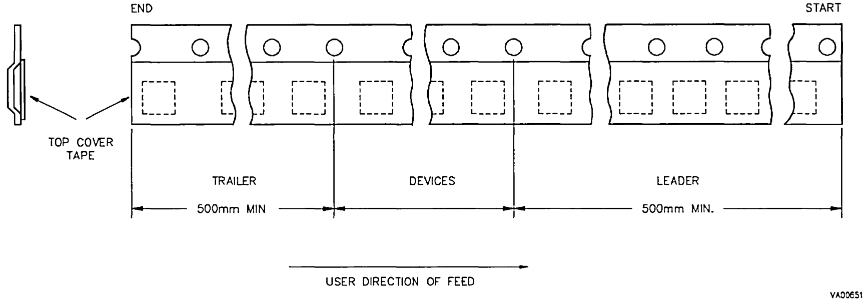

END
START
TOP COVER TAPE
TRAILER
DEVICES
LEADER
500mm MIN
500mm MIN.
USER DIRECTION OF FEED
VA00651

Figure 3. Small Outline Mechanical Polarization

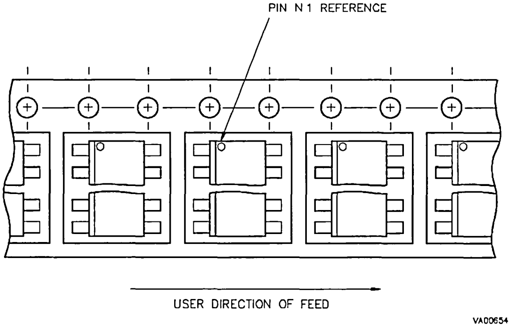

PIN N 1 REFERENCE
USER DIRECTION OF FEED
VA00654

Figure 4. PLCC Mechanical Polarization

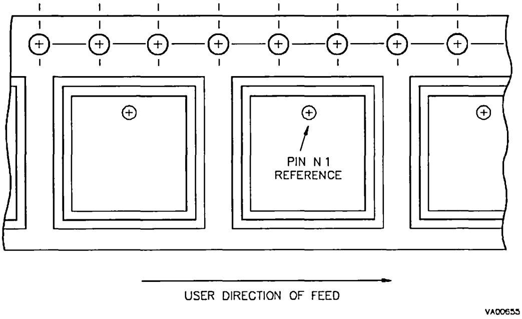

PIN N 1 REFERENCE
USER DIRECTION OF FEED
VA00655

Figure 5a. Embossed Carrier for 8, 12, 16, 24 mm Tape

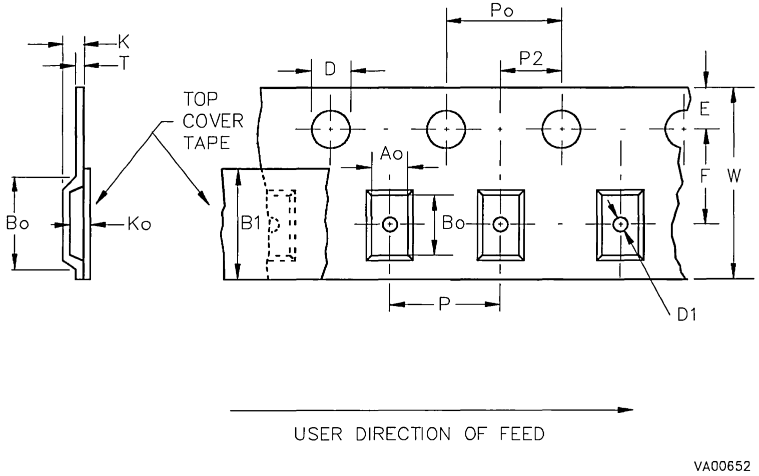


Figure 5b. Carrier Tape Constant Dimensions

Tape Size	D	E	Po	T Max	Ao, Bo, Ko	Unit
8 mm 12 mm 16 mm	1.5 +0.1 / -0	1.75 ± 0.1	4 ± 0.1	0.4	see Note	mm
24 mm	1.5 +0.1 / -0	1.75 ± 0.1	4 ± 0.1	0.4	see Note	mm

Note: Ao, Bo, Ko, are determinated by components sizes. The clearance between the component and the cavity must be within·
a. 0,05 mm min. to 0.50 mm max. for 8 mm tape
b. 0,05 mm min. to 0.65 mm max for 12 mm tape
c 0,05 mm min. to 0.90 mm max. for 16 mm tape
d. 0,05 mm min. to 1.00 mm max. for 24 mm tape

Figure 5c. Carrier Tape Variable Dimensions

Tape Size	B1 Max	D1 Min	F	K Max	P2	W	P	Unit
8 mm	4.2	1	3.5 ± 0.05	2.4	2 ± 0.05	8 ± 0.3	4 ± 0.1	mm
12 mm	8.2	1.5	5.5 ± 0.05	4.5	2 ± 0.05	12 ± 0.3	4 ± 0.1 8 ± 0.1	mm
16 mm	12.1	1.5	7.5 ± 0.1	6.5	2 ± 0.1	16 ± 0.3	4 ± 0.1 8 ± 0.1 12 ± 0.1	mm
24 mm	20.1	1.5	11.5 ± 0.1	6.5	2 ± 0.1	24 ± 0.3	12 ± 0.1 16 ± 0.1 20 ± 0.1 24 ± 0.1	mm

Figure 6a. Embossed Carrier for 35, 44 mm Tape

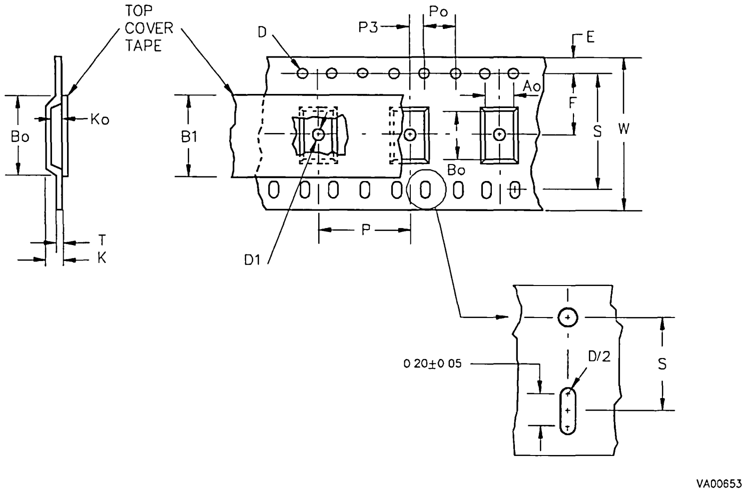


Figure 6b. Carrier Tape Constant Dimensions

Tape Size	D	D1 Min	E	K Max	Ao, Bo, Ko	Po	T Max	Unit
32 mm	1.5 +0.1 / -0	2	1.75 ± 0.1	10	see Note	4 ± 0.1	0.5	mm
44 mm	1.5 +0.1 / -0	2	1.75 ± 0.1	10	see Note	4 ± 0.1	0.5	mm

Note: Ao, Bo, Ko, are determinated by components sizes. The clearance between the component and the cavity must be within: 0,05 mm min to 1.00 mm max. for 32 mm and 44 mm tapes.

Figure 6c. Carrier Tape Variable Dimensions

Tape Size	B1 Max	F	P3	S	W	P	Unit
32 mm	23	14.2 ± 0.1	2 ± 0.1	28.4 ± 0.1	32 ± 0.3	16 ± 0.1 20 ± 0.1 24 ± 0.1 28 ± 0.1 32 ± 0.1	mm
44 mm	35	20.2 ± 0.1	2 ± 0.15	40.4 ± 0.1	44 ± 0.3	24 ± 0.1 28 ± 0.1 32 ± 0.1 36 ± 0.1 40 ± 0.1	mm

SGS-THOMSON
MICROELECTRONICS

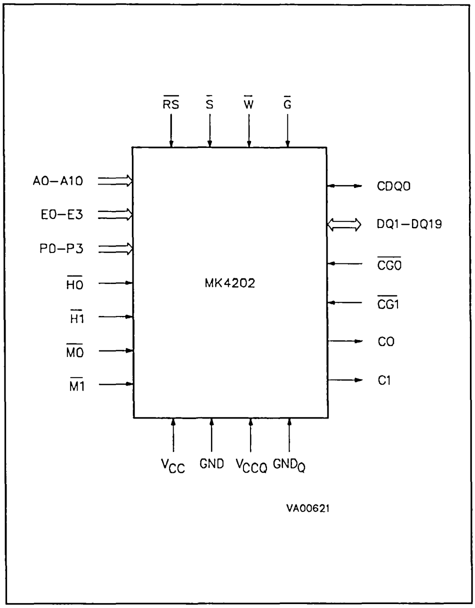
APPLICATION NOTE

THE MK4202 TAGRAM 32-BIT CACHE DESIGN CONCEPTS

INTRODUCTION

The MK4202 cache TAGRAM™ from SGS-THOMSON Microelectronics is a very fast CMOS SRAM based Cache Directory Comparator. The MK4202 offers high performance with a 20ns cycle time, and a 17ns address to tag compare access time. It is configured for the new generation 32-bit microprocessors, and implements a 2K x 20 architecture (see Figure 1). The device contains a 20-bit on-board comparator with dual compare or match outputs for easy interface to various 32-bit processors. An on-board chip enable decoder is also included to allow both width and/or depth expansion. Depth expansion is allowed up to a 32K density without speed (propagation time) penalties.

Figure 1. MK4202 TAGRAM Logic Symbol



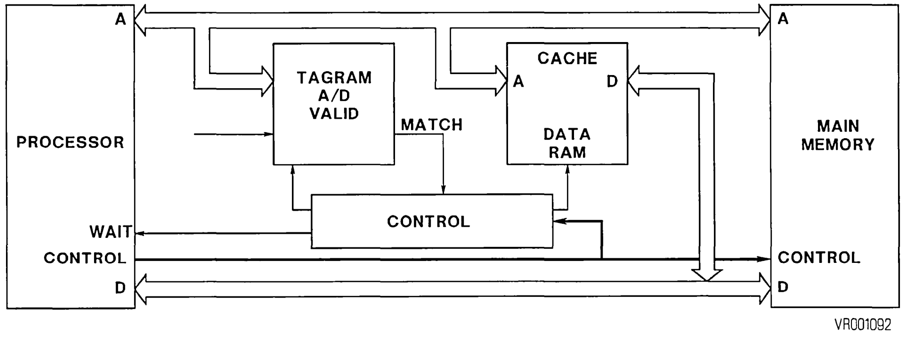
The MK4202 can enhance both system performance and cost. The high speed compare access time enhances the zero wait state logic to the processor for better system performance. Secondly, the MK4202 has high impedance data bus control inputs ($\overline{S}$) ($\overline{G}$), and eliminates separate latch, transceiver, and comparator components. This reduces the required real estate in PC board area, and results in lower system cost with no added gate delays through separate components.

TAGRAM OPERATION

A TAGRAM is that part of a ***cache subsystem*** that determines if data or instructions is retained in the cache memory (data cache). While this may be obvious, it should be noted that typical cache subsystems are designed in three sections: the **data cache** which stores the data to be used by the microprocessor, the **cache tag buffer** or **cache directory,** which stores the upper order address of each cache entry, and the **cache control** logic for processor interface, and cache read/write operations (see Figure 2). The data is identified by address location, and is stored in the cache directory (the MK4202 serves as the cache directory). If the TAGRAM "sees" a match, meaning that the necessary data is resident in the cache, it determines a **hit** and initiates a zero wait state operation to the processor. Conversely, a **miss** (nomatch) condition results in longer cycles for program execution since the cache does not contain the requested information.

During a compare cycle, the MK4202's on-board 20-bit comparator compares the upper address inputs (DQ_0 - DQ_{19}) with internal RAM data at the specified index address (A_0 - A_{10}). (The TAGRAM's architecture is shown in Figure 3). If all bits are equal (match), a hit is determined, and both Compare Outputs (C_0 and C_1) will go HIGH. If at least one bit is different, a miss condition exists, and both C_0 and C_1 will go LOW. The user can optionally force a MISS or HIT on either or both compare outputs by asserting $\overline{M}_X$ or $\overline{H}_X$ active LOW. A forced MISS overrides a forced HIT input (note the data sheet Truth Table). The Compare Ouput Enable ($\overline{CG}_X$) has no affect during a Force Hit or Force Miss operation.

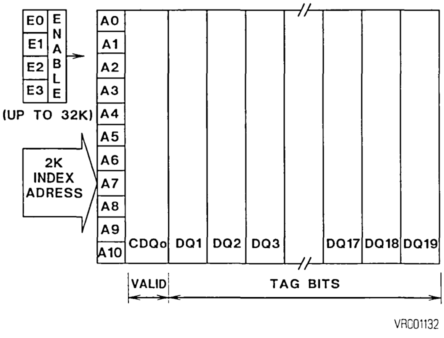
Figure 2. Generalized Cache Block Diagram



CIRCUIT DESCRIPTION

A Direct Mapped Cache subsystem application using the MK4202 is shown in the schematic block diagram in Figure 4. In this example, we are serving a 32-bit microprocessor with a 32-bit address bus and data bus. The 12 lower significant address lines (A_0 - A_{11}) are connected to the address inputs of the MK4202, with A_{11} connected to E_0 of both TAGRAMs as shown.

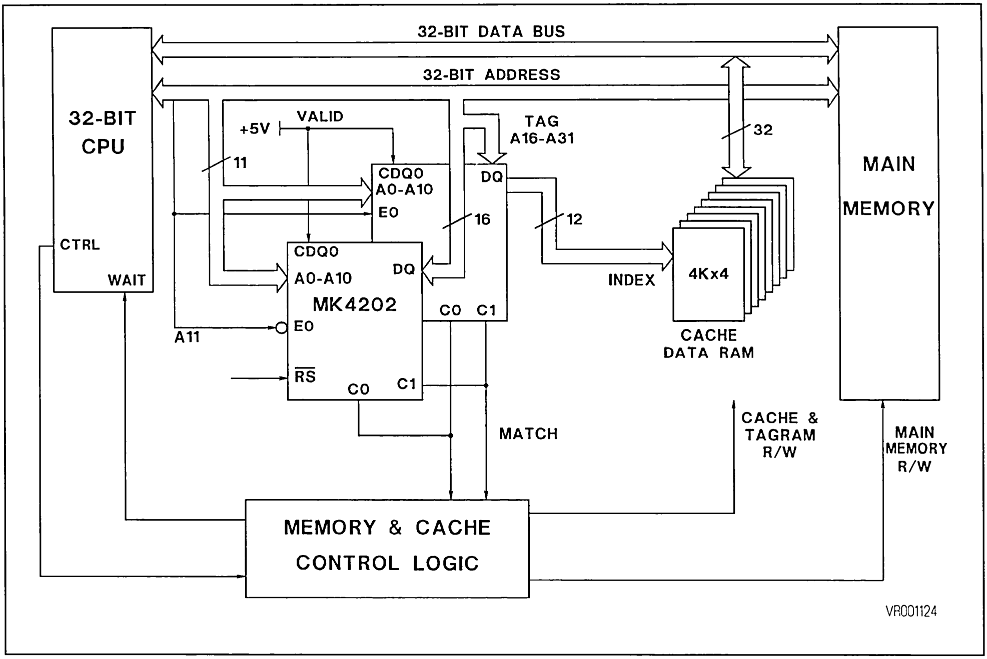
Figure 3. MK4202 TAGRAM Organization



This input will implement a 4K address index for the Cache Directory in this example, and a 4K address for the Cache Data RAM. The upper address bits of the processor (A_{16} - A_{31}), function as the tag data bits for the MK4202 TAGRAM, with CDQ_0 pulled up to V_{CC} (+5 volts) as a **valid bit**. Therefore, the cache tag buffer, or Cache Directory, consists of 4K x 16 bits, or 8K bytes. The Data Cache consists of eight very fast 4K x 4 SRAMs with Chip Enable ($\overline{E}$) for a 32-bit line width, resulting in a total of 16K bytes of memory (refer to Figure 5). Cache subsystems studies have shown that a cache design using this mapping scheme and combined memory size can yield a hit rate of better than 80%.

The MK4202 TAGRAM uniquely identifies each cache entry with an *address scheme consisting of the index and tag.* The upper addresses of a 32-bit microprocessor are considered as the tag, and are connected to the DQ pins (DQ_1 - DQ_{16}) of the MK4202 (see Figure 4). The CDQ_0 pin is designated to serve as the valid bit, as it allows the internal RAM to be reset or cleared to all zeros at all locations for the CDQ_0 output. The 11 address inputs (A_0 - A_{10}) of the MK4202 function as the **address index**, and are connected to the lower addresses of the processor. Extra lower order address lines can be connected to the Enable Inputs (E_0 - E_3) for on-board chip enable decode for depth expansion. (The E_0 - E_3 inputs correspond directly to the P_0 - P_3 inputs as described in the MK4202 data sheet). In this example, A_{11} is connected to E_0 for a depth expansion of 4K. The C_0 and C_1 Compare Outputs incorporate a CMOS totem-pole *3-state* design. This high impedance state allows

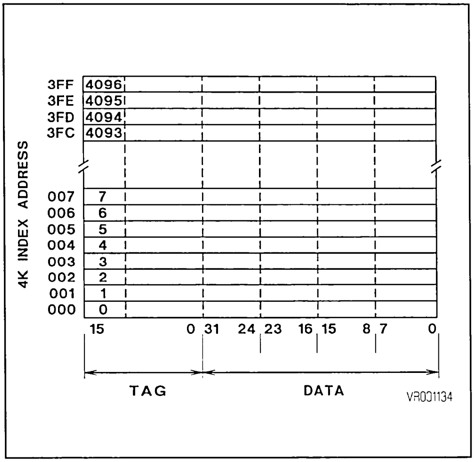
Figure 4. 16K-Byte Direct Mapped Cache Subsystem


32-BIT DATA BUS
32-BIT ADDRESS
32-BIT CPU
CTRL
WAIT
+5V
VALID
11
CDQ0
A0-A10
E0
TAG
A16-A31
DQ
16
12
32
MAIN MEMORY
CDQ0
A0-A10
DQ
MK4202
E0
A11
RS
C0
C1
C0 C1
INDEX
4Kx4
CACHE DATA RAM
MATCH
CACHE & TAGRAM R/W
MAIN MEMORY R/W
MEMORY & CACHE CONTROL LOGIC
VR001124

CIRCUIT DESCRIPTION (Continued)

each output to be tied together in a wired-OR configuration for multiple device applications, as shown in Figures 4 and 6. A pull-up resistor is suggested to enhance proper operation.

Figure 5. Cache Example Organization

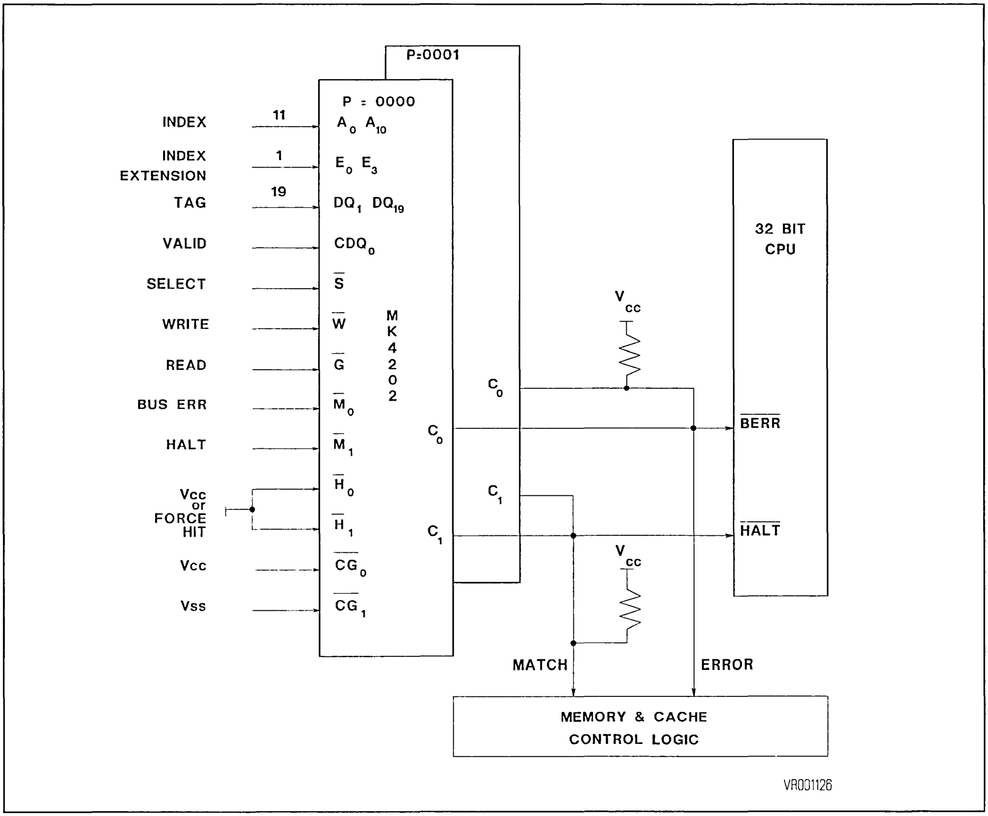

4K INDEX ADDRESS
3FF
3FE
3FD
3FC
007
006
005
004
003
002
001
000
4096
4095
4094
4093
7
6
5
4
3
2
1
0
15
0
31
24
23
16
15
8
7
0
TAG
DATA
VR001134

All processor address lines do not have to be connected to the TAGRAM, as most systems require designated *non-cached* addresses. Some address lines may define peripherals from an address vector for various I/O devices, or define DMA operations. Thus, a certain amount of address space is often required for various non-cacheable operations. Therefore, extra address lines from the processor can be used to decode these system operations. Unused addresses from the processor can be left open ; however, unused control and address inputs or tag data inputs to the MK4202 should be tied to be determined as a logic one or logic zero.

CIRCUIT OPERATION

The basic purpose of our Direct Mapped Cache subsystem is to provide the microprocessor (henceforth CPU) with a quick response for requested data from the **data cache** to avoid long memory cycles to main memory. Since typical programs spend most of their execution time in loops or nested procedures from a few localized areas of the program, the cache subsystem can maintain a copy of this localized data for faster execution. This will make our system more efficient and provide optimum performance.

Figure 6. Application Block Schematic


P=0001
P = 0000
INDEX
11
A0 A10
INDEX EXTENSION
1
E0 E3
TAG
19
DQ1 DQ19
VALID
CDQ0
SELECT
S
WRITE
W
READ
G
BUS ERR
M0
HALT
M1
MK4202
Vcc or FORCE HIT
H0
H1
Vcc
CG0
Vss
CG1
C0
C1
C0
C1
Vcc
Vcc
32 BIT CPU
BERR
HALT
MATCH
ERROR
MEMORY & CACHE CONTROL LOGIC
VR001126

CIRCUIT OPERATION (Continued)

Operation begins by initializing the MK4202 TAGRAM by asserting $\overline{RS}$ to clear all internal SRAM bits for the CDQ$_0$ output to a logic zero. This invalidates all entries in the cache directory. When the CPU begins its first read command cycle, the lower address bits select a location in the MK4202. This location in the TAGRAM is compared against the 16 bits of tag along with the single valid bit (CDQ$_0$ = V$_{CC}$). The valid bit will determine a miss condition causing C$_X$ to go LOW since data ones is being compared against data zeros. This is a **cache miss**, and the CPU will wait for a response from main memory.

In our Direct Mapped Cache subsystem example, we will assume the *write-through* method for main memory and cache coherency. This means that while the CPU is waiting for data during a **read/miss** operation, that the cache write/read control logic is designed to write data from main memory into the data cache SRAMs at the address defined by the index. When this happens, the 16 bits of tag, along with the valid bit, will be written simultaneously into the MK4202 cache directory. This way both the main memory and the **cache subsystem** contain the same information.

Now the logic one valid bit on the MK4202 TAGRAM can verify that the data in the data cache is a valid copy of main memory, since both the internal data and CDQ$_0$ (valid) are data ones. Of course, a cache miss will not occur after a reset operation, but every time the lower 12 address index bits select a location where the 17 tag bits (16 bits plus valid bit) do not match. However, each time a miss occurs, the most recent data will be written into the cache memory. This maintains cache coherency with main memory by constantly updating the cache with the most recent data.

CIRCUIT OPERATION (Continued)

After the cache has been written with valid data, and the CPU executes a read command from the same location that has been written into the cache subsystem, then the data tag bits will match, and a **cache hit** results. During a hit condition, both compare outputs, C_0 and C_1, will go HIGH. This will cause the CPU to operate in a no-wait state, and data will be gated onto the data bus from the data cache memory. The match/hit operation takes the requested data from the data cache, avoids wait state cycles to main memory, and terminates the cycle with a data acknowledge to the CPU.

It should be noted that even though both C_0 and C_1 go HIGH during a hit, that both compare/match outputs may not be required for the cache hit/miss control logic. The user could use one match output for determining a miss or hit condition, and use the other compare output to pass inputs through the MK4202 to the CPU. This is illustrated in Figure 6, where C_0 is normally HIGH except in an error condition. In this manner, a system error or halt will alert the CPU and invalidate cache execution at the same time. This is another benefit using the MK4202 and can reduce the number of required logic gates, and therefore system components.

CONCLUSION

We have given a general application and overview of the MK4202 cache TAGRAM in conjunction with a 32-bit data bus Direct Mapped Cache subsystem concept. System operation allows the cache subsystem to be updated with the most recent data for each access to main memory. The MK4202 allows easier implementation, and reduces the number of devices or components. Of course the MK4202 can also be used to implement a two or more set-associative cache design. In fact, by using the enable and chip select inputs on the MK4202, one can easily implement several cache design arrangements.

There are several features and organizational benefits when using the MK4202 for cache design. The device provides a flash clear ($\overline{RS}$) function to invalidate cache entries, which is useful for single processor systems, and for multi-processor systems sharing a cache subsystem. Additionally, the MK4202 is wide enough to provide extra bits for storing other information besides address tag data. One example might be "dirty bit" storage in a multi-processor application using a copy *back* method for cache coherency. Another example could be identification of non-cached addresses.

With the introduction of SGS-THOMSON's MK4202 TAGRAM, implementing cache subsystem designs for a 32-bit processor has been made easier. Cache subsystem implementation can now be provided for small-to-medium microcomputer systems without a large investment. The MK4202 TAGRAM provides for cost effective, high speed cache memory designs for today's 32-bit microprocessors, and is fully TTL compatible on its inputs and outputs.

SGS-THOMSON
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APPLICATION NOTE

MK45180 BiPORT SnoopTAG SIMPLIFIES CACHE COHERENCY

INTRODUCTION

Increased processor performance requirements have traditionally translated into more complex processor implementations, and higher clock frequencies. As the demands on leading edge technology have exceeded the capabilities, system designers have moved to alternate architectures to meet their throughput demands. Among these, cache memories and multi-processing are prominent.

Cache schemes in a multi-processing environment bring with them a whole new set of system concerns. Foremost among them is the maintenance of cache coherency between the remote cache memory subsystems, and the global system memory. Several protocols have evolved to address this issue, and all of them call for monitoring or "snooping" the main system bus. This type of bus monitoring is also known as "bus watching". The bus monitoring logic evaluates transactions on the system bus that may affect local cache storage. If such a transaction is detected, then the local cache subsystem is notified, and a fetch and update operation to obtain the new data will be performed by the local cache the next time it requests information from that specific location.

The current need is for the development of a high performance cost effective method for maintaining cache coherency within a global system where several processors share a common communication bus. One solution is a dual-port (or BiPORT™) cache tag directory for implementing local and global compare operations utilizing a single storage medium (such as a dual-port SRAM array). A dual-port cache tag directory (BiPORT TAGRAM™) serves a pervasive need in any shared memory system that utilizes cache storage - that is the need for a cost-effective and simplified method to maintain cache coherency in each of the local processing elements. To decrease system overhead, it would be preferable if this dual-port cache TAGRAM included a bus watch or "snoop" algorithm to self invalidate local cache entries that were overwritten in global memory by other bus masters and system processes sharing the same global data bus.

CACHE COHERENCY CONCERNS

A simplified block diagram for a uni-processor system is shown in Figure 1. The major elements are the local processor, system main memory, a local cache subsystem (blown up into it's individual elements), and some peripheral and I/O devices that share the system bus.

This can be contrasted with a typical shared memory architecture for a multiprocessing system depicted in Figure 2. Note that each of the local processors has it's own dedicated local cache subsystem, and each of these cache subsystems contains replicas of the data in system main memory that are being utilized by these processors most often. It is conceivable, even likely, that separate local processors will be processing the same system data repeatedly. This precisely, is where the issue of cache coherency in shared memory systems is born.

Although cache coherency concerns may seem more evident with multi-processor designs, even uni-processor designs can have need of special coherency logic. Referring again to Figure 1, should the I/O or peripheral device update main memory, then the local cache must be notified. The local cache must have a means of detecting the update to Main Memory in order to fetch and store the new data in the cache subsystem. Obviously, these cache coherency problems are amplified in a system with more than one processor, with each processor having its own cache subsystem.

MULTI-PROCESSOR CACHE COHERENCY

A more specific example of the cache coherency problem using a shared bus in a multi-processor system is illustrated in Figures 3 and 4. Here a local cache has data XY0, which is a replica of the data stored at location XY in main memory, stored in it's SRAM cache bank. Another processor (or DMA device, I/O device, or peripheral) writes to main memory location XY with new data XY1 (Figure 4). Unless the local cache subsystem is aware of this write, the data that it has stored will be "stale". In other words, the data that the local cache has stored will not be equivalent to the data resident at the main memory location which it is intending to

Figure 1. Typical Uniprocessor Application

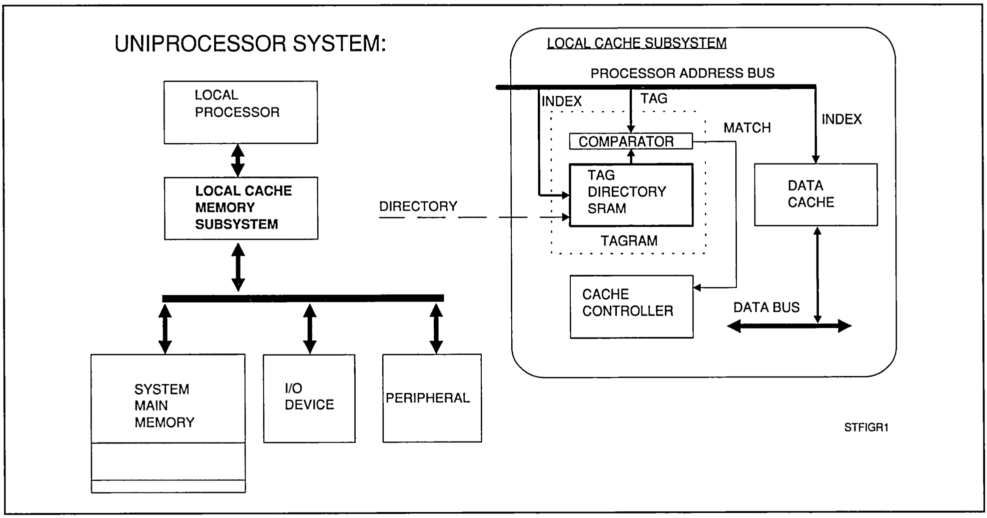
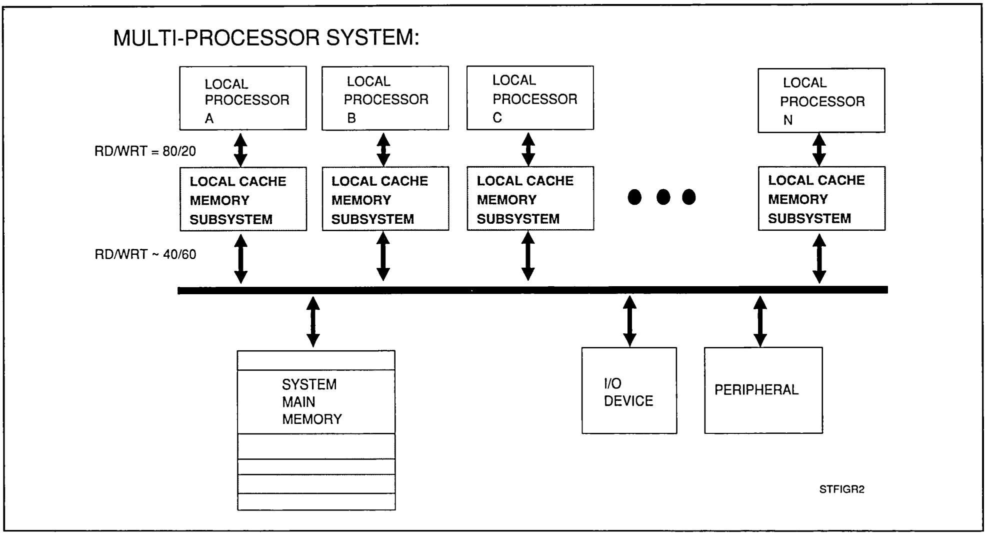

UNIPROCESSOR SYSTEM:
LOCAL PROCESSOR
LOCAL CACHE MEMORY SUBSYSTEM
SYSTEM MAIN MEMORY
I/O DEVICE
PERIPHERAL
DIRECTORY
LOCAL CACHE SUBSYSTEM
PROCESSOR ADDRESS BUS
INDEX
TAG
MATCH
INDEX
COMPARATOR
TAG DIRECTORY SRAM
TAGRAM
DATA CACHE
CACHE CONTROLLER
DATA BUS
STFIGR1

Figure 2. Typical Multiprocessor Application


MULTI-PROCESSOR SYSTEM:
LOCAL PROCESSOR A
LOCAL PROCESSOR B
LOCAL PROCESSOR C
LOCAL PROCESSOR N
RD/WRT = 80/20
LOCAL CACHE MEMORY SUBSYSTEM
LOCAL CACHE MEMORY SUBSYSTEM
LOCAL CACHE MEMORY SUBSYSTEM
LOCAL CACHE MEMORY SUBSYSTEM
RD/WRT ~ 40/60
SYSTEM MAIN MEMORY
I/O DEVICE
PERIPHERAL
STFIGR2

replicate. This is a major potential source of system errors.

The method for preventing this situation in these systems is to perform system bus watching or "bus snooping". Essentially the local cache subsystem monitors all system writes to main memory, and compares the main memory addresses being written with the addresses of the data stored in it's local cache. If the main memory location being written by an external source is resident in local cache, the local cache subsystem invalidates the location, effectively informing the local processor that the data is not coherent with the data it is replicating in main memory.

Figure 3. Cache Coherency 1

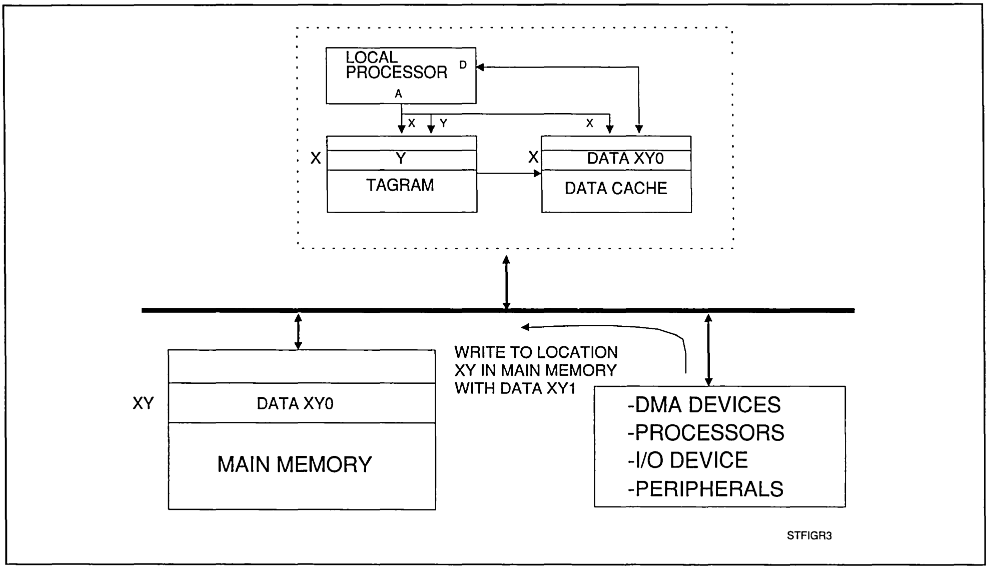

LOCAL PROCESSOR
D
A
X
Y
X
X
Y
TAGRAM
X
DATA XY0
DATA CACHE
WRITE TO LOCATION XY IN MAIN MEMORY WITH DATA XY1
XY
DATA XY0
MAIN MEMORY
-DMA DEVICES
-PROCESSORS
-I/O DEVICE
-PERIPHERALS
STFIGR3

Figure 4. Cache Coherency 2

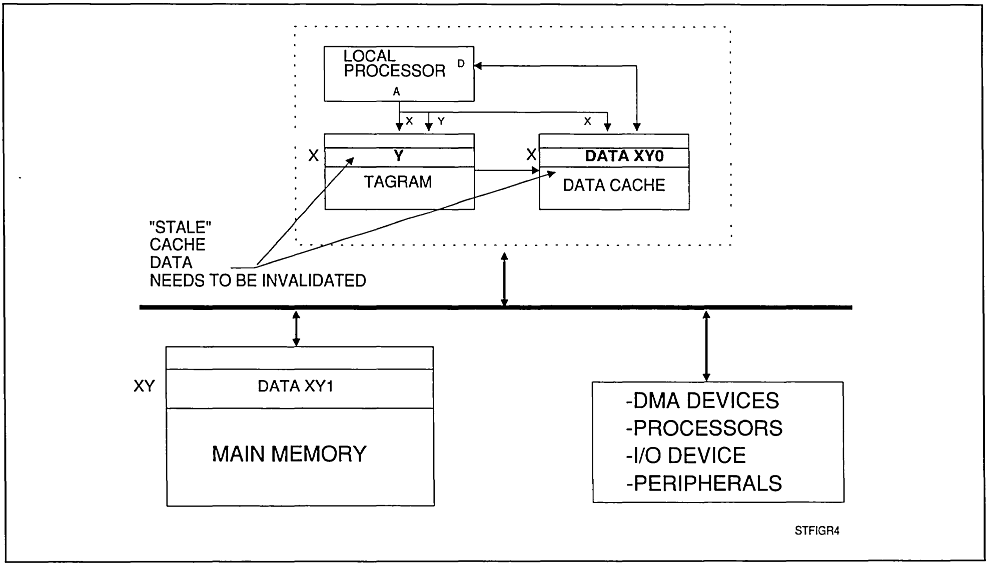
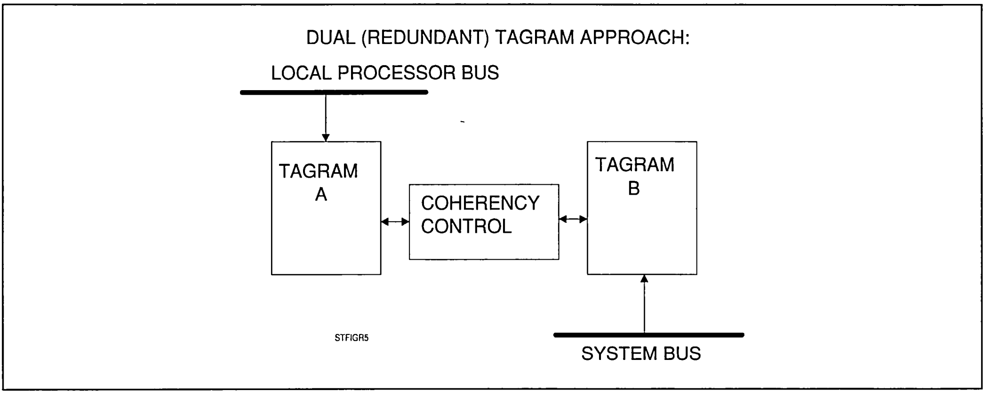

LOCAL PROCESSOR
D
A
X
Y
X
X
Y
TAGRAM
X
DATA XY0
DATA CACHE
"STALE" CACHE DATA NEEDS TO BE INVALIDATED
XY
DATA XY1
MAIN MEMORY
-DMA DEVICES
-PROCESSORS
-I/O DEVICE
-PERIPHERALS
STFIGR4

Figure 5. Conventional Bus Snooping Solution



SNOOPTAG CONCEPT

The conventional solution to the cache coherency problem previously discussed is depicted in Figure 5. In essence, system designers having little choice, use redundant TAGRAM banks each containing exactly the same data as the other. One of the TAGRAM banks is dedicated to the local processor, and the other is dedicated to snooping the system bus. This is an obvious inefficient use of resources. i.e. TAGRAM duplication which constitutes excess cost, demands additional board space, and results in more power consumption. Furthermore, the coherency control logic for the duplicate TAGRAM banks and Main Memory can become so complex that it may jeopardize system throughput. Hence, the dual-port TAGRAM (SnoopTAG ™) concept is presented as an alternative method for cache coherency.

DEVICE DESCRIPTION

As a solution to an efficient method of cache coherency in multi-processor (or uni-processor) designs, SGS-THOMSON introduces a new member to the TAGRAM family: the MK45180 CMOS BiPORT SnoopTAG™. The MK45180 SnoopTAG is a 4K x 10 dual-port cache tag directory with an on-board snoop invalidation protocol. The device is comprised of two ports as: (1) PORT A which is the local processor bus port, and (2) PORT B as the system or "snoop bus port". Both ports have an independent comparator to indicate a hit or miss condition in reference to the cache tag directory during compare cycles. The ports can operate asynchronous to each other using data stored in a common SRAM memory array. Thus, the MK45180 SnoopTAG allows the snoop invalidation process to be transparent to system performance. A simplified block diagram of the application concept is shown in Figure 6. (A thorough technical description including truth tables and timing edges is given in the MK45180 Data Sheet.)

A complete block diagram of the device concept is presented in Figure 7. The thrust of the idea is to collocate the snoop port and local port into a single device, not only eliminating the need for redundant tag directories, but also vastly simplifying the coherency control logic. Furthermore, the MK45180 has on-board parity generation and checking, allows width expansion to include a 32-bit address bus in a master/slave configuration, includes a flash clear operation to invalidate or flush the entire cache TAGRAM, has a built-in snoop invalidation protocol, and has several other user mode options that make the device adaptable to many applications.

Figure 6. Block Diagram

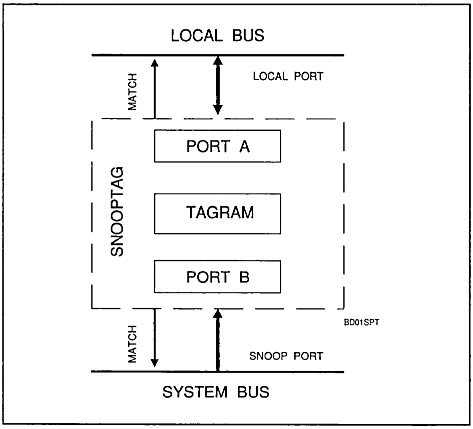
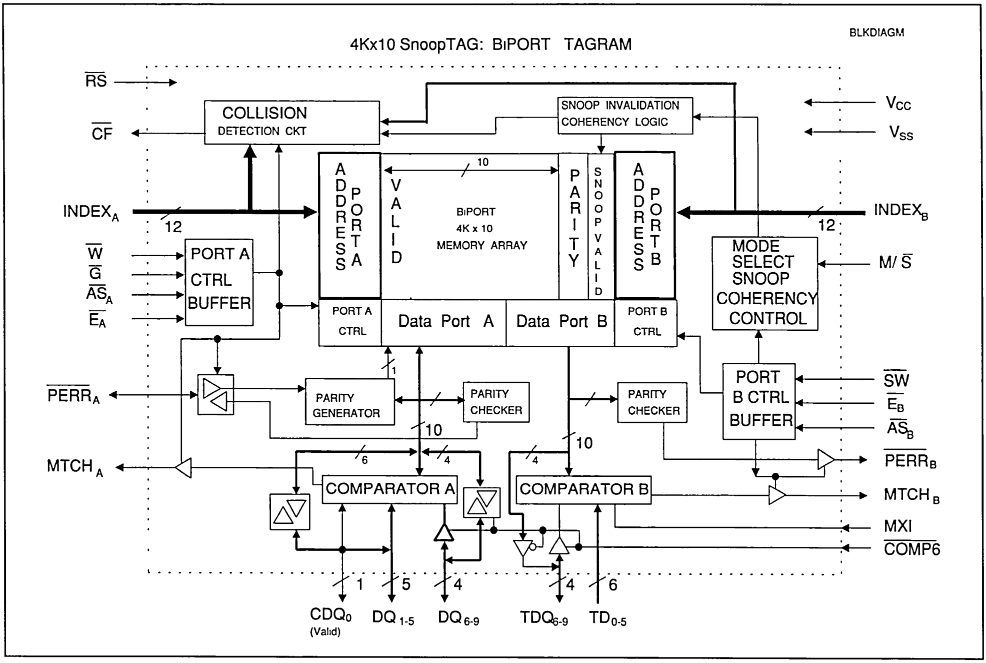


Figure 7. MK45180 Block Diagram


BLKDIAGM
4Kx10 SnoopTAG: BiPORT TAGRAM
RS
CF
COLLISION DETECTION CKT
SNOOP INVALIDATION COHERENCY LOGIC
Vcc
Vss
INDEXA
12
INDEXB
12
ADDRESS PORT A
VALID
10
BiPORT 4K x 10 MEMORY ARRAY
PARITY
SNOOP VALID
ADDRESS PORT B
W
G
ASA
EA
PORT A CTRL BUFFER
PORT A CTRL
Data Port A
Data Port B
PORT B CTRL
MODE SELECT SNOOP COHERENCY CONTROL
M/S
PORT B CTRL BUFFER
SW
EB
ASB
PERRA
PARITY GENERATOR
PARITY CHECKER
PARITY CHECKER
1
10
10
6
4
4
PERRB
MTCH A
COMPARATOR A
COMPARATOR B
MTCH B
MXI
COMP6
1
5
4
4
6
CDQ0 (Valid)
DQ 1-5
DQ 6-9
TDQ6-9
TD0-5

SNOOP INVALIDATION PROTOCOL

As shown in Figure 7, the MK45180 incorporates a hidden Snoop Valid bit (SV) for easier BiPORT operations and fast snoop invalidation during snoop write-hit operations. Figure 8 displays how the SV bit must be valid for either port to detect a valid hit condition, in addition to a valid match of the tag field data bits. It should be noted that Port A (local port) always writes the Snoop Valid bit to a logic 1. Port B on the other hand, always clears the SV bit to a logic 0 when a snoop write-hit occurs. Therefore, a bus snoop hit during system write operations will invalidate the Snoop Valid bit in the SRAM array only at that specific address. This forces a miss and cache fetch-update when the local port accesses the same location at a later time (thus the new data is fetched and stored by local cache). This cache coherency method eliminates the possibility of invalid or stale data being accessed by the local port.

TAG FIELD WIDTH EXPANSION

The width of the tag field data bits can be increased by implementing a Master/Slave configuration shown in Figure 9. This application example displays a 4K x 20 bit tag field with parity to include a 32-bit address bus. Port A provides a high speed three state totem-pole match output design for fast match accesss and data off times (MTCH$_A$ High-Z). Port B has a two state match output design for fast expansion timing. The MTCH$_B$ output of the Slave is the MXI input of the Master. The MXI pin serves as the "Match Expansion Input" to the Master by providing the handshake for the snoop invalidation protocol. Control signals and index addresses can be bused in parallel to both devices, while the tag data bits are connected to the upper significant bits of the address field.

The Master/Slave combination allows operation cycle times equal to that of the single device. The local port has a cycle time of 20ns, while the snoop port has a cycle time of 30ns. The MK45180 allows fast local compare cycle times by ANDing the MTCH$_A$ outputs, while the system snoop port can determine a hit or miss, and complete the snoop invalidation within the Port B cycle time if a snoop write-hit exists. Only the Master device can execute the snoop invalidation protocol via the snoop port, thus the MXI handshake is required for the occasion where the Master device is a "hit", and must determine if the Slave device is a hit before allowing a snoop invalidation to occur. This ensures a valid compare-hit before the snoop invalidation protocol is executed within the snoop cycle.

Figure 8. Match Comparator Logic

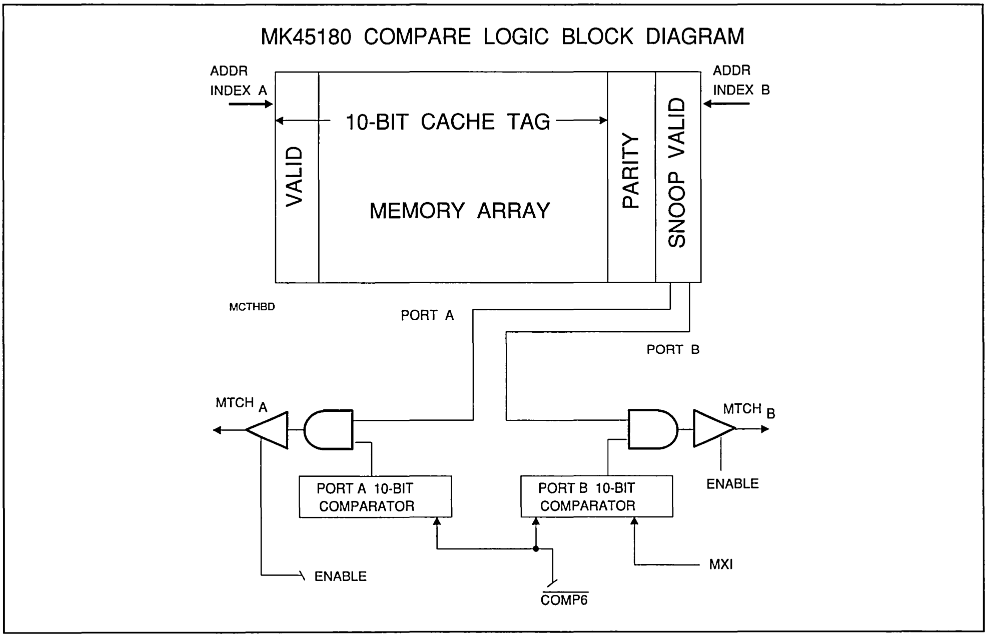
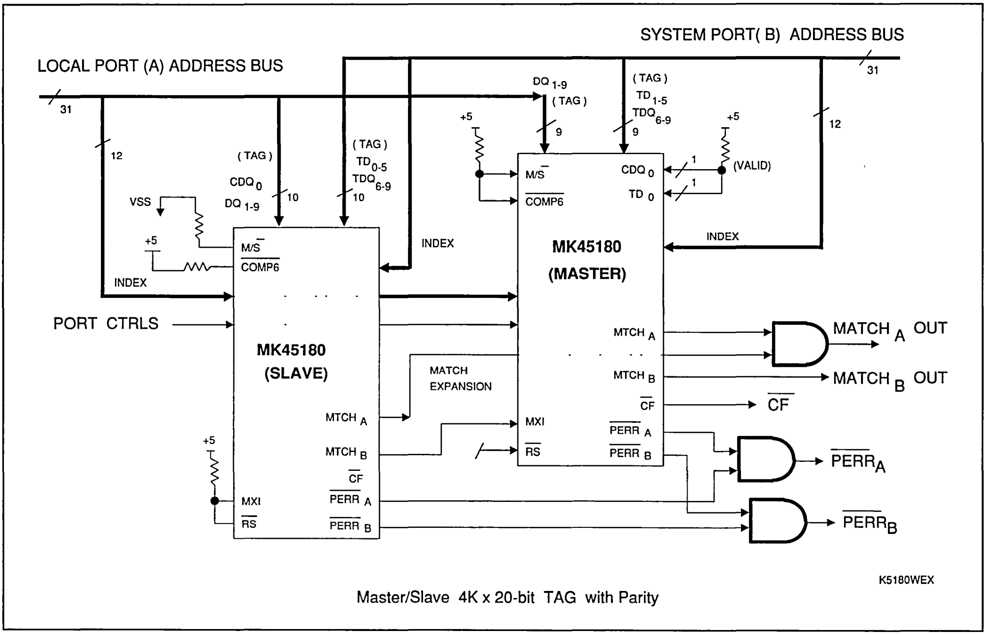

MK45180 COMPARE LOGIC BLOCK DIAGRAM
ADDR
INDEX A
ADDR
INDEX B
10-BIT CACHE TAG
MEMORY ARRAY
VALID
PARITY
SNOOP VALID
MCTHBD
PORT A
PORT B
MTCH A
MTCH B
ENABLE
PORT A 10-BIT COMPARATOR
PORT B 10-BIT COMPARATOR
ENABLE
MXI
COMP6

Figure 9. Tag Field Width Expansion


SYSTEM PORT(B) ADDRESS BUS
LOCAL PORT (A) ADDRESS BUS
31
31
12
12
DQ 1-9
(TAG)
(TAG)
TD 1-5
TDQ 6-9
9
9
+5
+5
(VALID)
1
1
(TAG)
CDQ 0
DQ 1-9
10
(TAG)
TD 0-5
TDQ 6-9
10
VSS
+5
INDEX
INDEX
INDEX
M/S
COMP6
M/S
COMP6
CDQ 0
TD 0
MK45180
(MASTER)
PORT CTRLS
MK45180
(SLAVE)
MTCH A
MTCH B
MATCH EXPANSION
MATCH A OUT
MATCH B OUT
CF
CF
MXI
RS
PERR A
PERR B
PERRA
PERRB
MTCH A
MTCH B
CF
+5
MXI
RS
PERR A
PERR B
K5180WEX

Master/Slave 4K x 20-bit TAG with Parity

COMPARE 6 OPTION

The MK45180 has another unique user configuration option for compare operations affecting both ports. The COMP6 input pin is a static input that configures the comparator on both ports (Port A and B) to compare either 6 or 10 external tag data inputs with the internal RAM to determine a match. If the COMP6 input is tied high, then a tag field of 10 bits is provided. This means both ports compare all 10 tag data bits with the internal RAM during a compare cycle to detect a hit or miss condition. If the COMP6 input is tied low, 4 bits are truncated from each port comparator, resulting in a 6-bit tag field with 4 status bit outputs during a valid compare cycle for either port (refer to the MK45180 Data Sheet). In summary, each port will indicate a hit or miss condition during a compare cycle in addition to providing four cache subsystem status bits simultaneously. Therefore, by using the COMPARE 6 option, an additional SRAM is not required to store and read cache status information. Figure 10 details the Master/Slave expansion combination with the COMP6 input of the Slave device tied low. This provides a cache tag directory of 4K x 16 tag bits with 4K x 4 status bits.

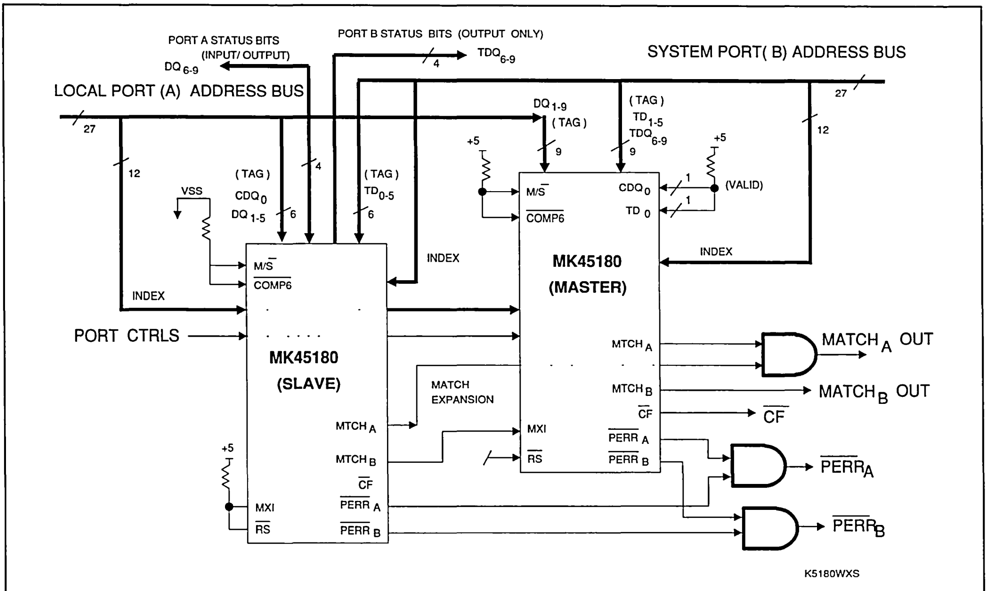
APPLICATION EXAMPLE

The next two figures show how a 32-bit bus scheme design using the SnoopTAG reduces part count, board space, and design complexity resulting in reduced design cost. The block diagram in Figure 11 uses the conventional bus snooping approach by duplicating cache TAGRAMs (refer to Figure 5). In this diagram we employ the MK41S80 4K x 4 cache TAGRAM to build a 4K x 18 bit (plus valid bit) cache tag directory. This implementation requires ten (10) MK41S80 devices in addition to the complex cache tag coherency and snoop invalidation protocol logic.

In contrast, Figure 12 displays the same basic block logic circuit using the MK45180 SnoopTAG. To summarize, the same 4K x 18 bit cache tag directory with valid bit (shown in Figure 11) requires only two MK45180 SnoopTAGs in the master/slave configuration. No off-chip cache tag coherency or snoop invalidation logic is needed. Thus, the SnoopTAG dramatically reduces part count and board space while simplifying design. Additionally, the snoop invalidation protocol is transparent to the system, thereby enhancing system performance.

As another example, should an application call for the cache tag directory to have a 4K address index,

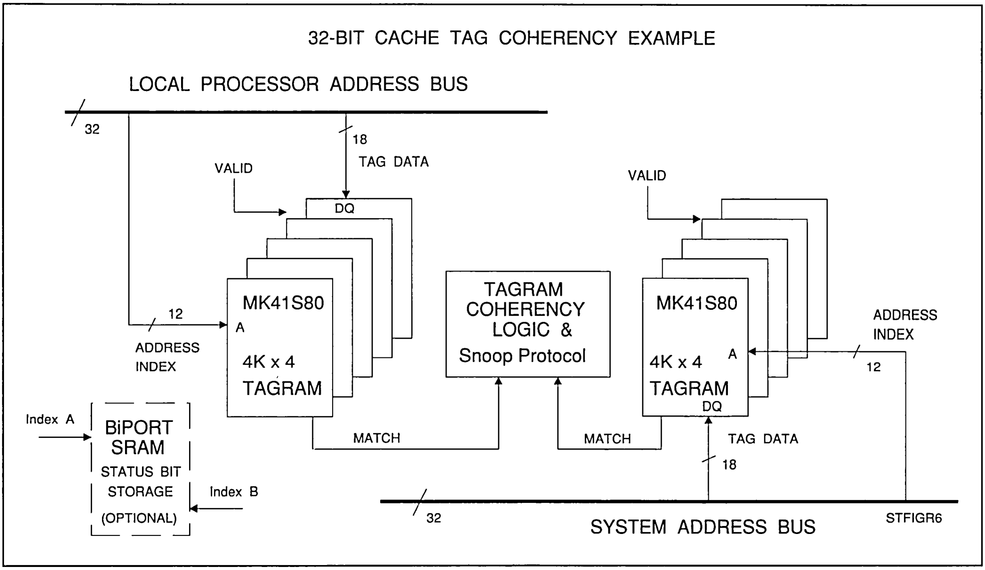
Figure 10. Compare 6 Option Width Expansion


PORT A STATUS BITS (INPUT/ OUTPUT)
DQ 6-9
PORT B STATUS BITS (OUTPUT ONLY)
4
TDQ 6-9
SYSTEM PORT(B) ADDRESS BUS
LOCAL PORT (A) ADDRESS BUS
27
27
12
12
DQ 1-9 (TAG)
9
(TAG) TD 1-5 TDQ 6-9
9
+5
+5
(VALID)
1
1
4
(TAG) CDQ 0 DQ 1-5
6
(TAG) TD 0-5
6
VSS
M/S
COMP6
CDQ 0
TD 0
INDEX
INDEX
INDEX
MK45180 (MASTER)
M/S
COMP6
MK45180 (SLAVE)
PORT CTRLS
MTCH A
MTCH B
CF
PERR A
PERR B
MATCH A OUT
MATCH B OUT
CF
PERR A
PERR B
MATCH EXPANSION
MTCH A
MTCH B
CF
PERR A
PERR B
MXI
RS
MXI
RS
+5

K5180WXS

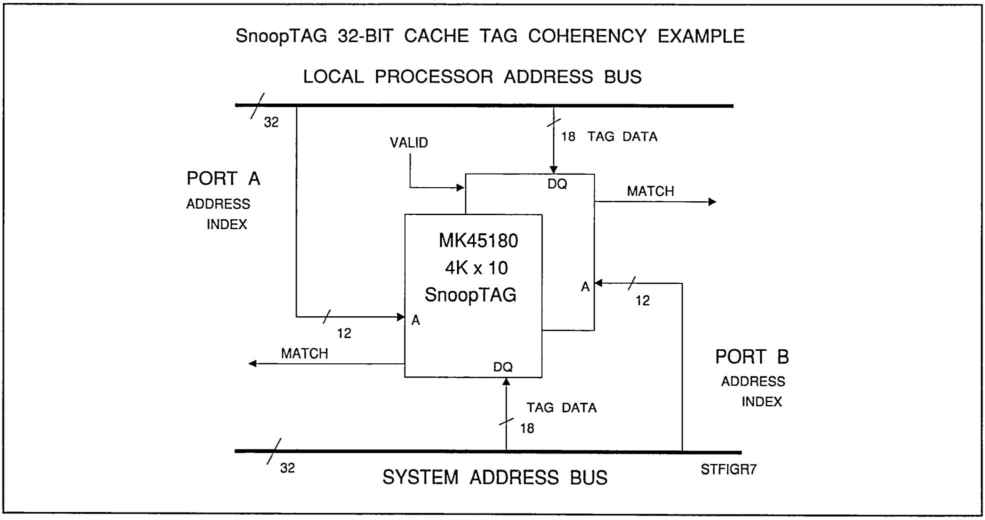
Master/Slave 4K x 16-bit TAG with Parity plus 4 Status Bits

Figure 11. Duplicate TAGRAM Cache Example


32-BIT CACHE TAG COHERENCY EXAMPLE
LOCAL PROCESSOR ADDRESS BUS
32
18
TAG DATA
VALID
DQ
12
A
ADDRESS INDEX
MK41S80
4K x 4
TAGRAM
TAGRAM COHERENCY LOGIC & Snoop Protocol
MATCH
MATCH
Index A
BiPORT SRAM
STATUS BIT STORAGE
(OPTIONAL)
Index B
VALID
MK41S80
4K x 4
TAGRAM
A
DQ
ADDRESS INDEX
12
TAG DATA
18
32
SYSTEM ADDRESS BUS
STFIGR6

16 bit tag data field, and two to four status bits, the SnoopTAG can reduce design complexity even further. Storage of status bits requires an additional external SRAM within the cache subsystem (optional BiPORT SRAM shown in Figure 11). By using the COMPARE 6 option in the master/slave configuration, the MK45180 SnoopTAG provides the 4K address index, 16 tag data bits, cache tag coherency and snoop invalidation protocol, and the needed SRAM storage for the status bits. Again, the SnoopTAG saves part count, power consumption, board space, simplifies design, and thereby reduces cost.

Figure 12. SnoopTAG Cache Example


SnoopTAG 32-BIT CACHE TAG COHERENCY EXAMPLE
LOCAL PROCESSOR ADDRESS BUS
32
VALID
18 TAG DATA
PORT A
ADDRESS INDEX
DQ
MATCH
MK45180
4K x 10
SnoopTAG
A
12
A
12
MATCH
DQ
PORT B
ADDRESS INDEX
TAG DATA
18
32
SYSTEM ADDRESS BUS
STFIGR7

CONCLUSION

The MK45180 SnoopTAG from SGS-THOMSON Microelectronics is an industry first to provide an alternate solution to multi-processor system designs implementing local processor cache storage with a shared global memory and common I/O bus. The SnoopTAG has an on-board snoop invalidation protocol providing a cache coherency method that eliminates the possibility of invalid or stale data being accessed by the local processor. The Master/Slave combination provides the ability to cache a 32-bit address bus by implementing a 4K address index and a 20 bit tag field (including parity). In addition, the MK45180 has a Compare 6 option to provide four status bits outputs during compare cycles. The Master/Slave expansion combination with the $\overline{\text{COMP6}}$ input of the Slave device tied low provides a cache tag directory of 4K x 16 tag bits with 4K x 4 status bits for both ports.

When compared to the conventional duplicate cache tag directory designs, the MK45180 provides a way to decrease device count and power consumption, while increasing system performance by eliminating duplicate tag storage coherency logic and snoop invalidation overhead. The MK45180 not only simplifies design, but has provisions to cache a 32-bit address bus with only two devices. Application examples include high-end workstations, PCs, minicomputers, graphics computers and laser printers.

With the introduction of SGS-THOMSON's 4K x 10 SnoopTAG, implementing cache coherency in either uni-processor or multi-processor environments has been simplified. The MK45180 SnoopTAG uses SGS-THOMSON's flagship HCMOS4 process technology implementing a fast match compare access time on both ports. It is TTL compatible on all dynamic inputs and outputs, and is the newest member of the fast TAGRAM family.

SGS-THOMSON
MICROELECTRONICS

APPLICATION NOTE

UNDERSTANDING CACHE MEMORY SYSTEMS

INTRODUCTION

Each new generation of microprocessors on the market has become faster and faster. Today, microprocessors, such as the Intel 486 and the Motorola 68030 have cycle times of 25 ns and plan to go faster in the future. The speed of DRAM main memory in such microprocessor-based systems has not come close to matching these cycle times. For example, it is quite common to use a DRAM with a cycle time of 100ns with an Intel 486 microprocessor. The resultant difference in cycle times between the microprocessor and DRAM means that the microprocessor cannot operate at full speed, because it must perform "wait states" during memory cycles. Wait states seriously reduce system throughput and performance.

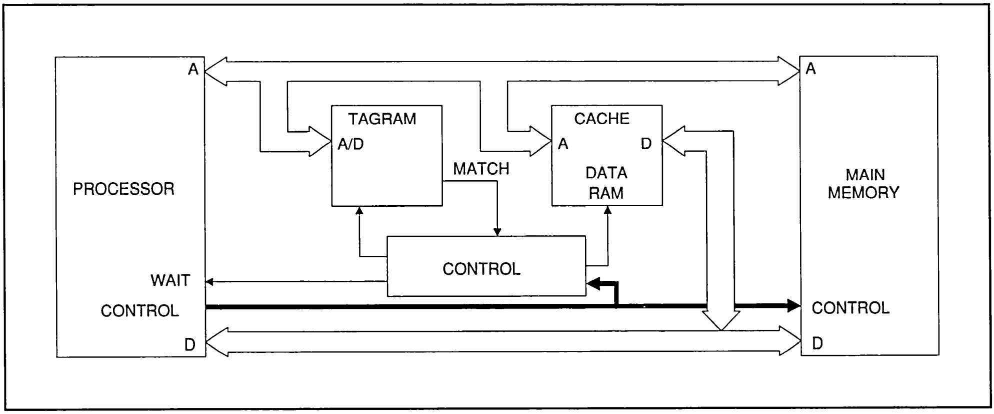
Cache memories are used to increase system throughput by reducing these microprocessor wait states. A cache system is a small, fast access SRAM bank, capable of single cycle accesses, which resides between the microprocessor and DRAM. The cache contains a copy of a block of DRAM memory which is frequently accessed by the microprocessor. By putting frequently accessed memory in the fast cache memory, the microprocessor can receive data from the cache instead of the slow DRAM during memory cycles. The DRAM only supplies data to the microprocessor when the cache memory does not have the needed data. In this way, using a cache subsystem reduces microprocessor wait states.

The theory works because most software code and data is contiguously stored in memory, and accessed repeatedly; therefore, the principals of temporal and spatial locality can be applied. The principal of temporal locality dictates that information currently being used by the microprocessor is likely to be used again in the near future. The principal of spatial locality dictates that the information to be used during the next memory cycle is likely to be close to the addresses of the information previously used by the microprocessor. Thus temporal locality is related to timing and spatial locality is related to actual physical location. According to these principles, there is a greater likelihood the microprocessor will find requested data in the cache memory and avoid wait-states.

ELEMENTS OF A CACHE SUBSYSTEM

The cache subsystem resides between the microprocessor and main memory and is comprised of three elements: the data cache, the cache tag buffer, and the cache control logic. The data cache contains the copy of prefetched data from the DRAM. The cache tag buffer or TAGRAM™ stores addresses for each corresponding entry, also called the TAG, in the data cache. The cache control logic interfaces with the microprocessor and controls all read/write operations between the processor, main memory, and cache memory. The block diagram in Figure 1 shows how these ele-

Figure 1: CACHE SUB-SYSTEM Block Diagram



ments interact with one another, the microprocessor, and the DRAM.

THEORY OF OPERATION

In order to better understand how a typical cache subsystem works, lets look at the operation of a direct mapped cache. In a direct mapped cache, each data cache location is mapped to one main memory location as shown in Figure 2 below.

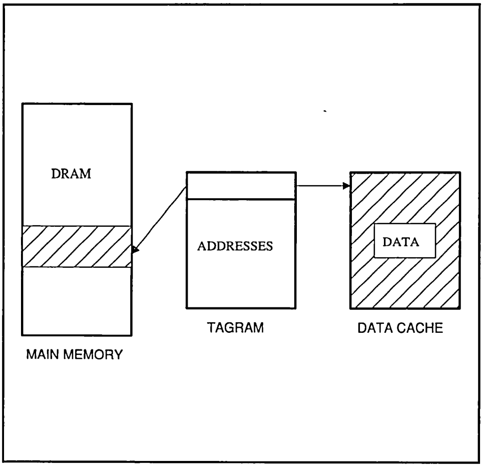
Cache Miss

Upon power-up, all locations in the data cache are set to zero. When the microprocessor initiates its first read cycle, the upper bits of the address bus are compared with the address bits stored in the TAGRAM. For this first compare, there will not be a match since the data cache is empty and the TAGRAM has no corresponding addresses. This is called a cache miss, and the MATCH output on the TAGRAM will be a logic zero. In this case, the required data will have to come from DRAM. The cache controller signals the DRAM to provide the requested data and directs the microprocessor to execute wait states until it receives data. When there is a cache miss, the controller also initiates logic which insures the data cache will be updated with a copy of DRAM data.

Cache Hit

The next time the microprocessor performs a read cycle to the same address, the data cache will contain the needed data since the data cache has been updated to reflect what is in the DRAM. Again, the address inputs to the TAGRAM are compared with the address bits stored in the TAGRAM. If there is a match, this is called a “hit” condition. The comparator inside the TAGRAM will output a logic 1 on the MATCH output for a hit condition. A MATCH output of logic 1 means that the data contained in the data cache at this location is valid. The cache control logic will gate the data immediately onto the data bus and signal the microprocessor to complete its memory cycle. This happens so quickly that the microprocessor never has to execute a wait state.

Figure 2: Direct Mapped Cache Organization



An Example ...

Consider your friendly local television repairman. When he is dispatched to your residence, he carries only those parts which are most often required for repair. It would be impractical for him to bring every part that might possibly be needed; that would be tantamount to transporting the entire inventory of parts from the shop to your home!

The repairman checks his list of parts and, if the required part is on the list, he fetches it from the truck. Since most repair jobs can be performed with those parts in the truck, it is likely your television set will be repaired immediately. However, if the required part is not in the truck, it will have to be fetched from warehouse inventory. Since this part broke in your television set, there is a greater chance of it needing to be replaced than previously thought. Hence, when the repairman goes to the warehouse, he selects two of the needed parts: one to repair your television set and the other to put in his truck. This increases the likelihood that you will not have to wait on a part if your television breaks again.

CACHE SUBSYSTEM PERFORMANCE

The performance of any cache subsystem can be measured by its hit rate. The hit rate is the percentage of memory cycles which can be completed using data from cache instead of data from the slower DRAM. For purposes of this discussion, we will talk about the cache performance of direct mapped caches. A cache hit occurs when the data cache has data requested by the microprocessor during a memory cycle. The microprocessor will receive data from the data cache and will avoid the wait states it would have incurred waiting on the DRAM. Therefore, the higher the hit rate, the more time the microprocessor spends working from fast cache memory and system performance is enhanced.

A hit rate of about 80% is common for a 64K byte direct mapped cache in a PC. This means that the microprocessor can operate with no wait states 80% of the time.

Hit Rate Versus Organization

Hit rate, for the same size cache memory, can be increased by varying the organization of the cache subsystem. Besides direct mapped, there are set associative cache organizations which achieve higher hit rates. 2-way and 4-way set associative caches are the most commonly used. The 2-way set associative cache is divided into two separate banks of memory. The 4-way set associative cache is very similar to the 2-way except that it has four banks. Figure 3 shows a typical 2-way set associative memory. The 2-way set associative system contains two TAGRAM banks, two data cache banks, and the control logic. Also, unlike the direct mapped cache, it has a LRU (Least Recently Used) memory. This is a small memory used by the control logic to determine which of the two memory banks should be updated next after a “miss”. The memory bank that was not read last, the least recently used, is updated to match main memory.

As mentioned above, the hit rate for a 64K byte direct mapped cache in a PC environment is about 80%. For a 64K byte system, the 2-way set associative memory has a hit rate of approximately 94% and the 4-way set associative is only slightly higher with a hit rate of approximately 98%. The performance increase of a set associative cache should be weighed against its higher cost. The increase in performance from the direct mapped organization to the 2-way set associative organization is substantial: from 80% to 94%. On the other hand, there is a relatively small performance increase of the 4-way set associative over the 2-way set associative cache (94% to 98%). Moreover, 4-way set associative caches generally are much more expensive than 2-way set associative caches. Figure 4 shows typical hit rates for direct mapped and set associative organizations.

CACHE EXPANSION

Cache expansion allows the designer to construct wider and deeper caches subsystems while working with readily available and relatively inexpensive parts. There are basically two types of cache expansion: width expansion and depth expansion. Below, Figure 5 shows width expansion and Figure 6 shows depth expansion using SGS-THOMSON parts.

Figure 3: 2-Way Set Associative CACHE Origanization

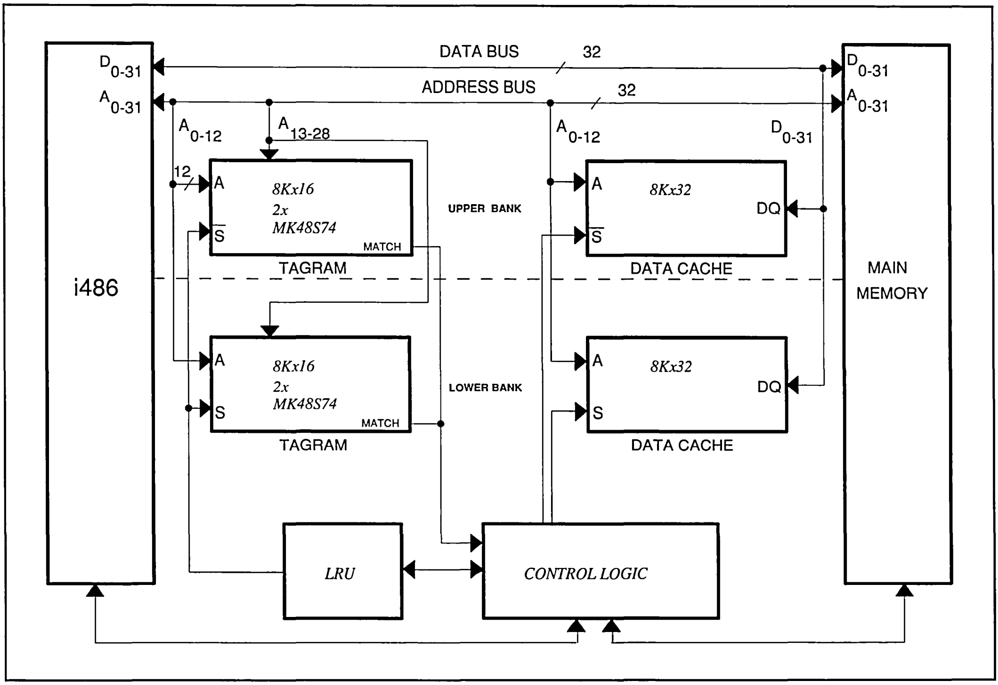
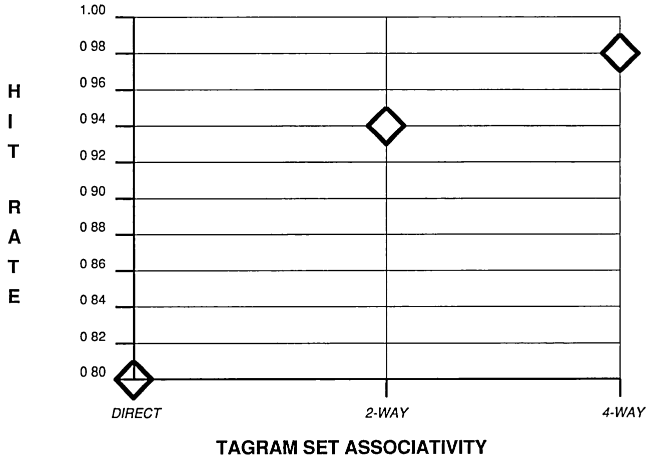


Figure 4: Hit Rate Versus Set Associativity



Width Expansion

Width expansion allows the designer to cache a larger section of main memory as shown in Figure 5. The data bus is widened by increasing the number of data cache RAMs; in the figure, four 4K x 4 SRAMs are used to increase the width of the data bus from 4 to 16 bits. The correct number of data cache RAMs is determined by dividing the width of the desired data bus by the width of the data cache RAMs. In this instance, 16 divided by 4 yields 4 data cache RAMs. Similarly, the address bus can be expanded to a wider size by increasing the number of TAGRAMs. Figure 5 shows how three MK41S80 4K x 4 TAGRAMs are used to increase the width of the address bus from 16 to 24 bits. By utilizing width expansion, the same devices can be reconfigured to adjust for the different bus widths required by various microprocessors.

Depth Expansion

Depth expansion differs from width expansion in that it increases the actual depth of the cache. Cache depth expansion is accomplished by duplicating the TAGRAM and the data cache SRAM as shown in Figure 6. In this example, the cache size was doubled from 8K x 16 to 16K x 16 by adding copies of the MK48S74 TAGRAM as well as copies of the data caches. The upper bits of the address bus are used to provide chip enable selection for the added components. Notice that adding copies of the TAGRAM and the data cache did not expand the bus width; it only increased the size of the cache as a whole. Increasing depth of the cache improves the hit rate, because you are expanding the address map and increasing the likelihood of finding requested data in the cache.

SUMMARY

Cache memories provide the means for dramatically improving microprocessor-based system performance in a cost effective way.

Using SGS-THOMSON TAGRAMs and SRAMs gives the designer the tools needed to significantly increase system throughput by minimizing wait states. Several factors, such as cache organization and size, determine cache effectiveness and must be weighed against system objectives to determine the most cost effective solution. SGS-THOMSON features a full line of TAGRAMs of varying organization and size that empowers the designer to design the right cache to fit individual system needs.

Figure 6: Width Expansion for TAGRAMs and Data Caches

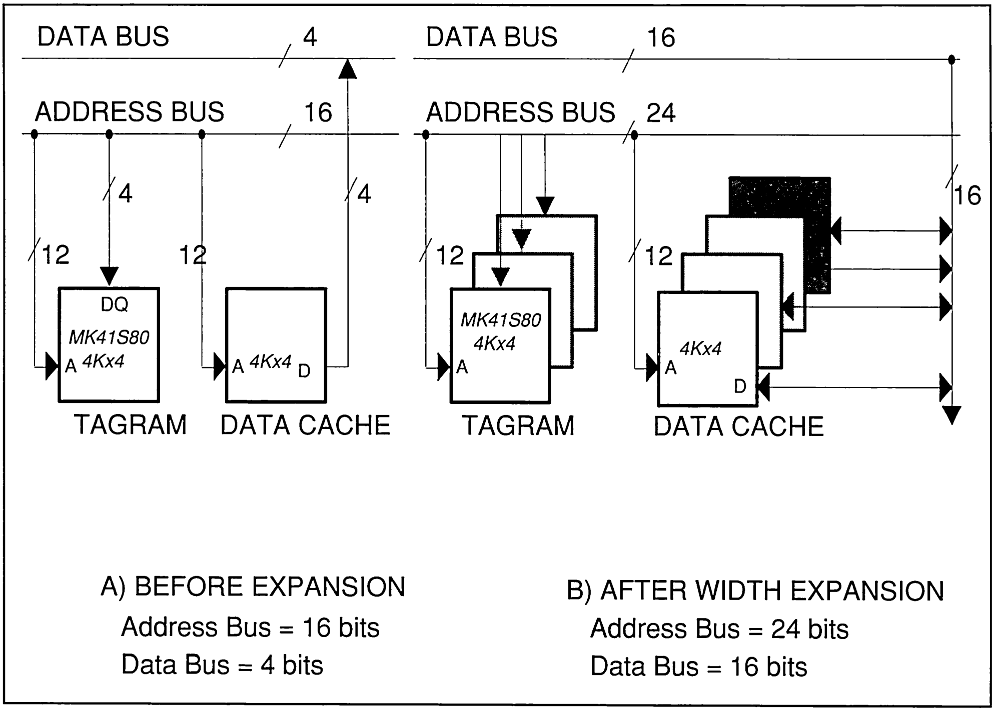
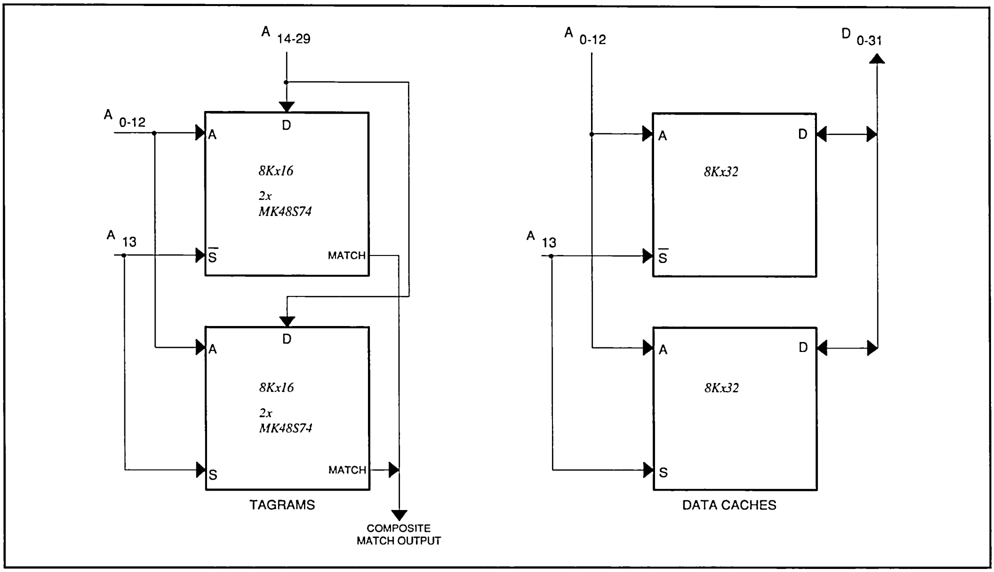

DATA BUS
4
ADDRESS BUS
16
4
4
12
12
DQ
MK41S80
4Kx4
A
A
4Kx4
D
TAGRAM
DATA CACHE
DATA BUS
16
ADDRESS BUS
24
16
12
12
MK41S80
4Kx4
A
4Kx4
A
D
TAGRAM
DATA CACHE
A) BEFORE EXPANSION
Address Bus = 16 bits
Data Bus = 4 bits
B) AFTER WIDTH EXPANSION
Address Bus = 24 bits
Data Bus = 16 bits

Figure 5: Depth Expansion for TAGRAMs and Data Caches


A 14-29
A 0-12
A
D
8Kx16
2x
MK48S74
A 13
S̅
MATCH
A
D
8Kx16
2x
MK48S74
S
MATCH
TAGRAMS
COMPOSITE
MATCH OUTPUT
A 0-12
D 0-31
A
D
8Kx32
A 13
S̅
A
D
8Kx32
S
DATA CACHES

LIST OF TERMS

Associativity. Cache organization where main memory addresses are mapped to different SETs of SRAM banks.

Cache. Fast, local memory containing a copy of frequently used main memory code and data.

Cache Hit. Microprocessor requested data is found in the cache.

Cache Miss. Microprocessor requested data is not found in the cache.

DRAM. Dynamic Random Access Memory.

Data Cache RAM. Portion of cache that stores copies of main memory data.

Direct Mapped. Type of cache organization in which each data cache location is mapped to one main memory location.

Hit Rate. Percentage of memory requests that are cache hits.

Least Recently Used (LRU). Cache update policy. Used in set associative caches to update the oldest memory bank.

Set Associative. Type of cache organization in which the cache sub-system is divided into memory banks which cache different sections of main memory.

Spatial Locality. Programs usually request data or instructions with main memory addresses close to the address of the data currently being used.

SRAM. Static Random Access Memory

TAGRAM. Portion of cache that stores the main memory addresses of data stored in the data cache RAM.

Temporal Locality. Information currently being used is likely to be used again in the near future.

QUALITY NOTES

SGS-THOMSON
MICROELECTRONICS

QUALITY NOTE

MEMORY PRODUCTS QUALITY PROGRAM

The Corporate quality program of SGS-THOMSON is published as the SURE (Semiconductor Users Reliability Evaluation) Program. The quality program for memory products follows closely this Program. Described here are the particular controls that apply specifically to memories starting with the Lot Acceptance and AOQ assessment and followed by the program for memory product qualification, an indication of the the manufacturing SPC (Statistical Process Controls) and the Short and Long term reliability tests.

Lot Acceptance

The role of a final Lot Acceptance sampling has changed from that of lot acceptance - although this still applies - more to the collection of statistical data about the outgoing quality, and the monitoring of the quality to the target defectivity in Parts Per Milion (ppm).

The Average Outgoing Quality (AOQ) is estimated from the results of Lot Acceptance testing. The measure developed by and used by SGS-THOMSON for the AOQ is known as the Average Outgoing Quality Estimator and is given by:

$$\frac{\text{Total Defective units in sample, with } d \leq c + 1}{\text{Total inspected units in samples of accepted lots}}$$

Where d = number of defects in sample, c = acceptance number. The totals are those of ALL lots inspected (1st, 2nd, etc controls).

This AOQE converges towards the real AOQ as the number of sampled lots increases, even though an acceptance number of zero is used.

Memort Product Qualification/Major Changes

Memory Product qualification is made on new memory products, new die designs and new packages and existing products when there are major changes to the design or manufacturing.

The tests performed depend on the parameters affected by a major change or the qualification of combinations of new die designs and new Plastic or Ceramic packages.

The tests performed are selected as appropriate from those listed in Tables 3 through 6.

Table 1. Finished Product Acceptance

Subgroup	Parameters	Minimum Sample Size	Acceptance Number
A1	Visual and mechanical inspection	315	0
A2+A3+A4	Cumulative electrical and inoperative mechanical failures	315	0

Table 2. Qualification

1	Wafer Fabrication Major Changes	Tests selected to control the parameters that are affected by the change, varying from the design or mask set to the fabrication plant.
2	Assembly Major Changes	Tests selected to control the parameters that are affected by the change, varying from package material changes to the assembly plant.
3	Product Qualification	Tests selected to control the parameters depending on the type of package and whether the die is new or already qualified.

Table 3. Product Qualification, Ceramic Packages - Package Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Physical Dimensions	2016	Published Data
2	Bond Strength	2011	
3	Die Attach	2019 or 2027	
4	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
5	Lid Torque	2024	
6	Internal Water Vapour	1018	5000 ppm (max)
7	Solderability:		
	– FDIP Package	2003	245°C, 5sec, Precondition Steam, 1hr
	– JLCC, LCCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air 150°C, 16hrs
8	Resistance to Solvents	2015	4 Solvent Solutions
9	Salt Atmosphere	1009	Test Condition A, 35°C, 24hrs
10	Lead Integrity	2004	Test Condition B2
11	Resistance to Soldering Heat		260°C, 10sec
12	Thermal Shock	1011	–55 to 125°C, 15 cycles
	Temperature Cycling	1010	–65 to 150°C, 100 cycles
	Moisture Resistance	1004	–10 to 65°C, RH = 90%
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
13	Mechanical Shock	2002	Test Condition B
	Vibration Variable Frequency	2007	Test Condition A
	Constant Acceleration	2001	Teat Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
14	Temperature Cycling	1010	–65 to 150°C, 10 cycles
	Constant Acceleration	2001	Test Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1

Table 4. Product Qualification, Plastic Packages - Package Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Physical Dimansions	2016	Published Data
	Coplanarity PLCC, PSOJ & JLCC Packages		Published Data
2	Bond Strength	2011	
3	Die Attach	2019 or 2027	
4	Solderability:		
	– PSO, PSOJ & PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs
	– PDIP package	2003	245°C, 5sec, Precondition Steam, 8hrs
5	Resitance to Solvents	2015	4 Solvent Solutions
6	Salt Atmosphere	1009	Test Condition A, 35°C, 24hrs
7	Lead Integrity	2004	Test Condition B2
8	Resistance to Soldering Heat:		
	– PSO, PSOJ & PLCC Packages		215°C, 40sec
	– PDIP Package		260°C, 10sec
9	Resistance to Surface Mounting:		
	Temperature Humidity:		85°C, RH = 85%
	– PSO Package		24hrs
	– PLCC & PSOJ Packages		48hrs
	Solder Dipping:		
	– PSO Package		260°C, 10sec
	– PLCC & PSOJ Packages		215°C, 120sec
	Visual Inspection		Body Cracks
	Pressure Pot		121°C, 2Atm, 168hrs

Table 5. Product Qualification, Ceramic Packages - Die Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life Test	1005	140°C, V_{CC} = 5 to 7V, 500hrs
2	Operating Life Test	1005	125°C, V_{CC} = 5.5V, 1000hrs
3	Retention Bake (EPROM)	1008	250°C, 500hrs
4	Temperature Cycling	1010	–65 to 150°C, 1000 cycles
5	Thermal Shock	1011	–55 to 125°C, 500 cycles
6	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
7	Electrostatic Discharge	EIAJ IC-121	0Ω, 200pF, 200V (min)
8	Latch-up	JEDEC STD-17	Current Injection 200mA (min), Overvoltage 14V (min)

Table 6. Product Qualification, Plastic Packages - Die Related Tests

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life Test	1005	140°C, V_{CC} = 5 to 7V, 500hrs
2	Operating Life Test	1005	125°C, V_{CC} = 5.5V, 1000hrs
3	Retention Bake (OTP, EEPROM)	1008	150°C, 1000hrs
4	Write/Erase Cycling (EEPROM, FLASH)		Published Data
5	Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5.5V, 1000hrs
6	Temperature Cycling	1010	–40 to 150°C, 1000 cycles
7	Thermal Shock	1011	–55 to 125°C, 500 cycles
8	Pressure Pot		121°C, 2Atm, 168hrs
9	HAST	CECC 90,000	130°C, RH = 85%, 96hrs
10	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
11	Electrostatic Discharge	EIAJ IC-121	0Ω, 200pF, 200V (min)
12	Latch-up	JEDEC STD-17	Current Injection 200mA (min), Overvoltage 14V (min)
13	Soft Error Testing (SRAM)		

Statistical Process Control

One of the most powerfull tools implemented throughout the production of memory products is SPC. The final goal of the SPC program is to bring each critical step of the process to “6 Sigma” capability ($Cp \geq 2$). Current controls are at Cp and Cpk 1.33. For example, in a typical wafer processing line more than 200 variables may be controlled for SPC. Data is gathered and analysed by on-line computers and provides up-to-the minute control charts (eg $\overline{X}$, R charts). The critical process steps are defined by FMEA (Failure Mode and Effects Analysis).

A selection of the most important SPC steps and the Cp and Cpk results is regularly available and can help customers to avoid the costly qualification of new products when the products come from a qualified design and a manufacturing process that is demonstrated to be under control.

The Table 7 and Table 8 show some typical SPC results from both wafer fabrication and assembly processes.

Table 7. Statistical Process Control, Wafer Fabrication, CMOS EPROM (1.2 micron)

#	Parameter	Dependant Performance	4q91		1q92	
			CP	CPK	CP	CPK
1	VTH Field Minimum P-Channel Transisitor	Latch-up Related	2.49	1.58	2.84	1.81
2	VTH Field Minimum N-Channel Transistor	Latch-up Related	2.28	2.42	2.62	2.42
3	Gate Oxide Thickness	Data Retention & ESD	1.60	1.55	1.68	1.65
4	Interpoly Oxide Thickness	Data Retention	1.70	1.64	1.43	1.41
5	Intermediate Dielectric Thickness	Data Retention	1.46	1.36	1.44	1.34

Table 8. Statistical Process Control, Ceramic Package Assembly EPROM

#	Parameter	Dependant Performance	4q91		1q92	
			CP	CPK	CP	CPK
1	Shear Test	Die Attach	1.69	1.69	2.20	2.20
2	Bond Strength	Bond Weakness	2.17	2.15	2.50	2.50
3	Torque Test	Hermeticity	2.40	2.19	1.70	1.70
4	Lead Plating Thickness	Solderability	1.50	1.13	1.70	1.90

Short Term Reliability Testing

In order to provide a rapid feedback on product reliability to manufacturing, a series of Short Term Reliability tests are performed on a lot-by-lot or weekly basis. These are summarised in Table 9 and Table 10.

Table 9. Short Term Reliability Tests, Ceramic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Thermal Shock	1011	–55 to 125°C, 60 cycles
2	Retention Bake (EPROM)		180°C, 72hrs
3	Solderability	2003	245°C, 5sec, Precondition Steam, 1hr
4	Resistance to Solvents	2015	4 Solvent Solutions
5	Physical Dimensions	2016	Published Data
6	Lead Integrity	2004	Test Condition B2
7	Hermeticity: – Fine Leak – Gross Leak	1014	 Test Condition A1 Test Condition C1
8	Lead Torque	2024	

Table 10. Short Term Reliability Tests, Plastic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Temperature Cycling	1010	–40 to 150°C, 100 cycles
2	Write/Erase Cycles (EEPROM & FLASH)		Published Data
3	Solderability: – PSO, PSOJ & PLCC Packages – PDIP Package	 CECC 90,000 2003	 215°C, 3sec, Precondition Dry Air, 150°C, 16hrs 245°C, 5sec, Precondition Steam, 8hrs
4	Resistance to Solvents	2015	4 Solvent Solutions
5	Physical Dimensions	2016	Published Data
6	Lead Integrity	2004	Test Condition B2
7	Pressure Pot		121°C, 2Atm, 168hrs

Long Term Reliability Testing

Long Term Reliability tests are performed to provide evidence of the life time reliability of memory products. Sampling is made either monthly, 3 or 6 monthly depending on the tests performed. Table 11 and Table 12 summarise the tests.

Table 11. Long Term Reliability Tests, Ceramic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life	1005	125°C, V_{CC} = 5 to 6V, 1000hrs
2	Retention Bake (EPROM)	1008	250°C, 500hrs
3	Thermal Shock	1011	–55 to 125°C, 15cycles
	Temperature Cycling	1010	–65 to 150°C, 100cycles
	Moisture Resistance	1004	–10 to 65°C, RH = 90%, 10 cycles of 24hrs
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
4	Mechanical Shock	2002	Test Condition B
	Vibration Variable Frequency	2007	Test Condition A
	Constant Acceleration	2001	Test Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
5	Temperature Cycling	1010	–65 to 150°C, 10 cycles
	Constant Acceleration	2001	Test Condition E
	Fine Leak	1014	Test Condition A1
	Gross Leak	1014	Test Condition C1
6	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
7	Salt Atmosphere	1009	Test Condition A, 35°C, 24hrs
8	Internal Water Vapour	1018	5000 ppm (max)
9	Temperature Cycling	1010	–65 to 150 °C, 500 cycles

Table 12. Long Term Reliability Tests, Plastic Packages

Subgroup	Test Procedure	MIL-STD-883 Procedure	Test Conditions
1	Operating Life	1005	125°C, V_{CC} = 5 to 6V, 1000hrs
2	Retention Bake (OTP & EEPROM)	1008	150°C, 1000hrs
3	Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5.5V, 1000hrs
4	Electrostatic Discharge	3015	1500Ω, 100pF, 2000V (min)
5	HAST	CECC 90,000	130°C, RH = 85%, 96hrs
6	Temperature Cycling	1010	–40 to 150 °C, 500 cycles

Conclusion

SGS-THOMSON believes that the extensive attention given to process control and product evaluation, combined with clear design rules and a well designed technology base, give the Company a world class overall quality rating.

TECHNICAL ARTICLES

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TA102

TECHNICAL ARTICLE

Special cell design gives highest EEPROM endurance

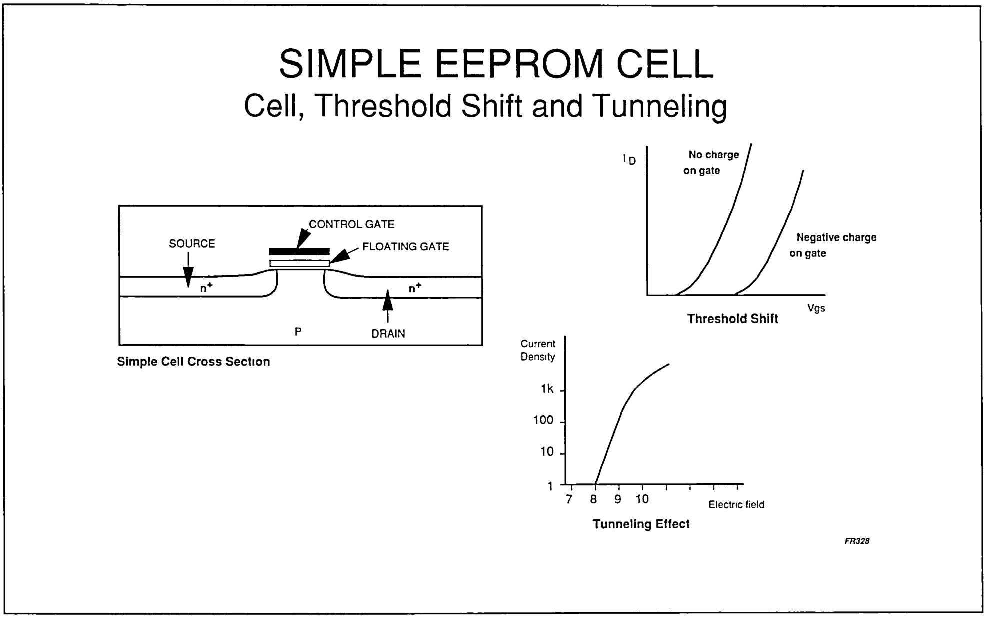
Antony Watts
SGS-THOMSON Microelectronics
Agrate, Italy

The substantial market that exists for small serial EEPROM memories differs sharply from most other branches of the memory market in that, by definition, neither the access time nor the memory density are particularly important parameters. Instead, designers focus on the endurance and data retention of the products, that is, how many times can a cell be erased and re-written and how long can it store data?

Endurance and data retention are each limited by physical factors inherent in the storage mechanism. In the case of data retention, it is the loss of stored charge through leakage current, while the finite Erase/Write endurance is the result of the physical damage that is actually done to the memory cell whenever new data is written to it. These two aspects of EEPROM products are directly influenced by the manufacturing process, especially the way in which the tunnel oxide layer is formed and subsequently treated.

As shown in Figure 1, the simplest EEPROM cell is essentially an enhancement mode MOSFET with two gates. One gate, known as the control gate, is connected to the Read/Write control circuitry via the usual matrix of address lines. The other, known

Figure 1.


SIMPLE EEPROM CELL
Cell, Threshold Shift and Tunneling
CONTROL GATE
SOURCE
FLOATING GATE
n^+
n^+
P
DRAIN
Simple Cell Cross Section
I_D
No charge on gate
Negative charge on gate
Vgs
Threshold Shift
Current Density
1k
100
10
1
7
8
9
10
Electric field
Tunneling Effect
FR328

as the floating gate, is located between the control gate and the MOSFET channel and is isolated from both by insulating layers of silicon dioxide. The floating gate is usually made from conducting polysilicon but sometimes an insulating silicon nitride floating gate is used.

When a positive voltage is applied to the control gate, electrons are attracted towards the gate insulation from the body of the device. If the gate voltage is high enough, electrons will outnumber holes in the channel, so that the MOSFET will turn on and conduct current. However, any negative charge stored on the floating gate will tend to repel electrons from the channel, so that a higher positive voltage on the control gate will be required to invert the channel.

In fact, EPROM, EEPROM and FLASH memories all exploit the ability of a charged floating gate to change the threshold voltage of a MOSFET but there are major differences in the way that each type of memory charges and discharges the floating gate. In the case of an EEPROM, electrons are moved to and from the floating gate by tunnelling, a quantum-mechanical phenomenon that depends on a sufficiently high potential difference being applied across a thin insulating barrier. FLASH memories also use tunnelling to discharge the floating gate but, like EPROMs, use hot channel electrons to charge the floating gate.

Obtaining a tunnelling current large enough to charge up the floating gate in an acceptable time requires a thin oxide layer and a high applied voltage; typically, the oxide layer is less than 100 Å thick and the applied voltage is 20V. Unfortunately, every time a high voltage is applied across the tunnel oxide, some deterioration in the integrity of the oxide layer occurs, with electron traps created within the oxide itself. As the trapped electrons are closer to the channel than those on the floating gate, they have a stronger influence on the threshold voltage. Eventually, the charge trapped in the oxide layer will be sufficient to mask the effect of the charge on the floating gate, making it impossible to clear the memory cell. Depending on the nature, thickness and quality of the insulating layer, typical endurances can range from around 100 to several million cycles.

Perhaps the most obvious way to minimise the damage to the tunnel oxide layer is to reduce the strength of electric field applied across the oxide layer during erasure. Unfortunately, the tunnel current density is an exponential function of the applied field, so a small reduction in applied voltage gives rise to a large increase in the time required to discharge the floating gate. This technique has been used to improve the endurance of flash memories because a cell erase time of, say, one second means a total device erase time of one second. For a 1K serial EEPROM configured as 128 x 8, however, increasing the typical cell programming time from 10ms to one second cell erase time gives a device erase time of more than two minutes, which is quite unacceptable. For EEPROM, therefore, there is a trade-off between endurance and erase time and the practical limit for guaranteed endurance has tended to be 100,000 Erase/Write cycles.

There is, of course, no limit on read cycles because a cell is read by sensing channel current rather than moving electrons to or from the floating gate. However, stored charge will inevitably leak away from the floating gate, either to the control gate or to the drain/channel/source area, so the MOSFET threshold will gradually be reduced until the point when the stored data is lost. EEPROM cells are typically able to store data for more than ten years, which is usually substantially longer than the application requires.

The majority of EEPROM manufacturers use the FLOTOX structure, which is derived from Figure 1 by extending the two gates over the drain region, as shown in Figure 2. The oxide thickness is reduced over the drain region to enable tunnelling to take place. To load electrons onto the floating gate, a high positive voltage is applied to the control gate. This induces a high positive voltage on the floating gate and electrons tunnel from the drain to the floating gate. To erase the cell, the applied voltage is reversed and electrons tunnel back to the drain.

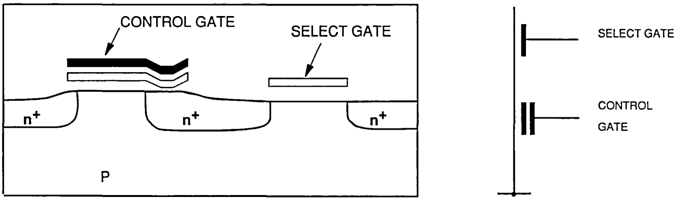
This is a relatively simple scheme that yields a compact cell some 3-4 times the size of an EPROM cell, although small cell size is not a particularly important advantage in these products. The relatively thick oxide layer that surrounds most of the floating gate gives good data retention. The problem with this structure is that endurance depends critically on the integrity of the thin tunnel oxide layer which is deposited fairly early in the processing cycle. This means that subsequent processing steps to lay down the polysilicon floating gate, another oxide layer and then the metal or polysilicon control gate can thermally stress the thin tunnel oxide and give rise to electron traps. Typical endurance figures for this structure are 10,000 or 100,000 cycles.

Two alternatives to the FLOTOX structure are currently used. One is the MNOS structure, which is essentially the structure shown in Figure 1 except that the floating gate is made from silicon nitride. Although silicon nitride is an insulator, it contains electron traps and is capable of storing charge. However, because electrons cannot move freely through the floating gate, they must tunnel to specific trap sites dispersed throughout the nitride layer. This effectively increases the thickness of the insulating barrier, which means that the actual oxide layer must be very thin. As with the FLOTOX structure, electron traps in the tunnel oxide layer degrade the storage capability.

Figure 2.

FLOTOX CELL, OPERATION

Program and Erase

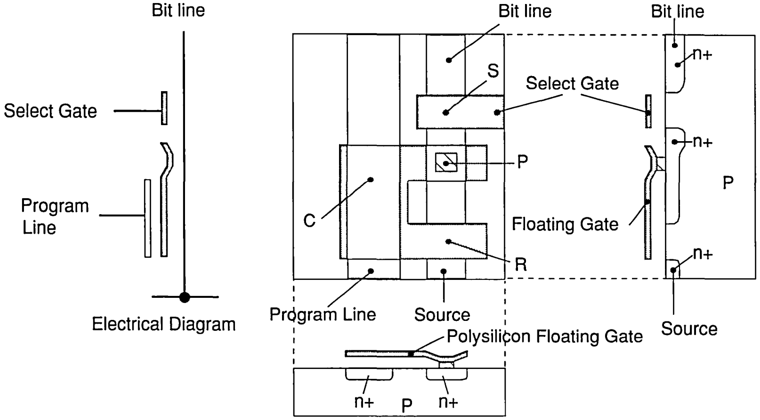

CONTROL GATE
SELECT GATE
n+
n+
n+
P
SELECT GATE
CONTROL
GATE

Cell Cross Section **Electrical Diagram**

Figure 3.

EEPROM CELL

Special Design


Bit line
Select Gate
Program
Line
Electrical Diagram
Bit line
S
Select Gate
P
C
Floating Gate
R
Program Line
Source
Polysilicon Floating Gate
n+
P
n+
Bit line
n+
n+
P
n+
Source
FR330

To load the MNOS cell, a high voltage is applied to the control gate and electrons tunnel from the p-well in the substrate to the traps in the floating gate. To erase the cell, the control gate is grounded and the positive voltage is applied to the p-well, causing tunnelling in the reverse direction.

The main problem with MNOS is that it requires an ultra-thin tunnel layer, which makes processing expecially critical and gives relatively high degradation. The main interest in MNOS is due to the simple gate arrangement that offers easier scaling for future high density memories. The second alternative to FLOTOX is the special cell structure developed by SGS-THOMSON and shown schematically in Figure 3. Here, the polysilicon floating gate extends over three separate areas: the program area (P) where the thin tunnel oxide is located, the control area (C) where the floating gate crosses the diffused program line, and the read transistor gate (R). To charge up the floating gate, the program line is taken to 17V, capacitive coupling causes a voltage of about 12V to be induced on the floating gate and electrons then tunnel across the oxide layer from the n+ diffusion. To discharge the floating gate, the program line is grounded and the n+ diffusion is taken to 17V via the select transistor (S).

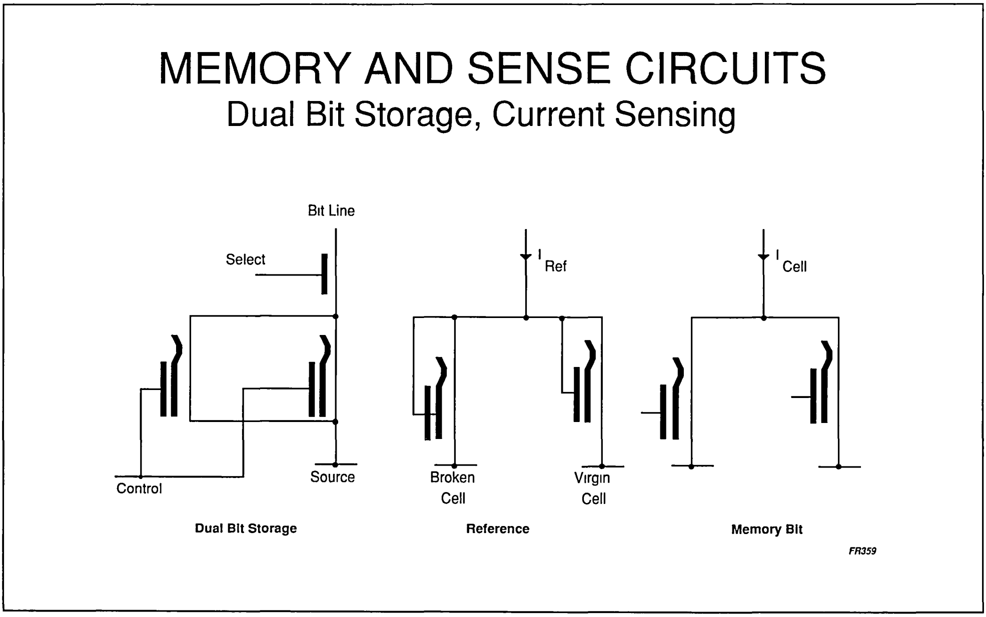
The most important difference between this cell structure and the conventional FLOTOX or MNOS structures is the elimination of the vertically stacked gates. Instead, the program line, which effectively replaces the control gate, lies alongside the bit line. This diffusion is performed before the thin tunnel oxide layer is formed and the subsequent process steps have a low thermal budget and do not damage this layer.

In addition, the CMOS processes used for EEPROM production at SGS-THOMSON are relatively simple but very reliable 1.5 and 1.2 micron processes that use a single polysilicon layer for the floating gates and a single metal layer for the interconnects. The use of a simple, proven process coupled with the use of lateral control structures makes it easier to achieve a tunnel oxide of consistently high quality. The advantage of this approach is dramatically illustrated by the resulting endurance at least **1,000,000 Erase/Write cycles guaranteed immediately**, with 2-3,000,000 cycles in the near future.

Redundancy

Like any memory device, an EEPROM is only as reliable as its weakest cell and even the highest quality oxide layers are subject to occasional random defects. If a device fails because of wearout of a random weak cell, it does not matter whether the remaining cells would have withstood another 100 or another 1,000,000 cycles. To ensure that such random failures do not cancel out the advantages of the lateral control structure, SGS-

Figure 4.



THOMSON's EPROMs employ full dual-cell redundancy.

As shown in Figure 4, two storage transistors are provided for each bit in the memory array. The two transistors, which have independant floating gates, are connected in parallel, with a common control line and a single select transistor.

For sensing, the cell reference current is obtained by connecting in parallel a virgin cell (always unloaded) and a cell with the floating gate connected to the drain, equivalent to a short circuit in the tunnel oxide. This current is compared with the combined current through the two storage transistors in the logical cell. When the two cells are unloaded, the combined current is greater than the reference current. The circuit is designed so that, if one of the memory cells becomes broken (tunnel oxide short circuit), the combined current with the good cell unloaded still exceeds the reference current. In this way, a memory bit can be correctly read even if one of the storage cells is faulty. Note that this technique does not extend the endurance of the cells but rather ensures that the endurance of the whole array is determined by the average cell endurance instead of the weakest cell endurance.

Accelerated life test results

The superiority of this EEPROM technology has been confirmed by high temperature testing. For example, Figure 5 shows the results of a high temperature bake test of data retention. the activation energy for the failure mechanism is 0.6eV, so one hour at 150°C is therefore equivalent to 117 hours at 55°C. A 1000 hours bake is thus equivalent to 13 years continuous operation at 55°C. No failures were encountered in the 21 lots (671 devices) sampled. At a 60% confidence level, this is equal to a failure rate of 10 FIT at 55°C.

Even more impressive are the results of the two endurance tests, summarised in Figure 6. The first test was a straightforward sequence of 1,000,000 Erase/Write cycles and no failures occurred in any of the 36,575 devices tested. The second test consisted of 1,000,000 Erase/Write cycles followed by a 168 hours bake at 150°C (equivalent to more than two years operation at 55°C), followed by 2,000,000 further cycles and then another 16 hours bake at 150°C. On the basis of these tests, a quality level of better than 150ppm can be assured for 1,000,000 cycles performance with better than 99.5% confidence level.

To assure this performance, a sample from every lot manufactured is submitted to a 1,000,000 cycle test. A reserved test instruction allows all memory cells to be erased and written in parallel, so the test is performed very quickly. Lots are cycled at the maximum specified frequency, with a 10ms wait between write and erase instructions.

Figure 5.

RETENTION

Q & R Results EEPROM

1 hour at 150 deg. C = 117 hours at 55 deg. C, Ea = 0.6eV

CMOS MF3 - 150 deg. C

Lots	168hrs	504hrs	1000hrs
21	0/921	0/921	0/671

60% CONFIDENCE, FR = 10 FIT/55 deg. C

FR361

Figure 6.

ENDURANCE

Erase/Write Cycles, EEPROM

TEST 1 : 1,000,000 cycles

TEST 2 : 1,000,000 cycles, 168hrs at 150 deg. C (= 2yrs at 55 deg. C)
3,000,000 cycles, 168hrs at 150 deg. C

CMOS-MF3	**TEST 1**	**TEST 2**	
Lots	1M cycles	1M cycles + Bake	3M cycles + Bake
475	0/36575	0/1095	0/870

1,000,000 Erase/Write cycles GUARANTEED to 150ppm with 99.5% confidence.

FR360

Currently, the range of serial EEPROM devices designed with the new cell structure and built with the high reliability CMOS-MF3 (1.5μ) or CMOS-MF4 (1.2μ) processes covers two quasi-standard bus interfaces (I^2C and Microwire) and array sizes up to 4K, with 8K, 16K and 32K devices in development. In addition to devices that operate from the standard 5V power supply, there are types (e.g. the 4K ST25C04) which can operate with supply voltages as low as 2.5V, making them particularly useful in mobile communications equipment. Operation at 2.5V is possible because the devices contain a charge pump capable of generating 25V from a 2.5V rail. This is stabilised to 17V for the memory array, resulting in an actual voltage applied to the tunnel oxide of about 12V. The charge pump operates almost continuously at 2.5V ; at higher supply voltages, it operates in bursts sufficient to maintain the required current.

The 1,000,000 cycle performance and future prospects of 2-3,000,000 cycles, is opening up new potential uses for EEPROMs. For example as number and redial memories in Telephone sets - an application previously met only by SRAMs with battery back-up.

TECHNICAL ARTICLE

EPROM as a technology leader

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Over the last few years EPROMs (Electrically Programmable Read Only Memories) have become the overwhelming technology of choice for those applications requiring non-volatile semiconductor memory. Developments of the EPROM towards FLASH technology - FLASH memories are electrically programmable like EPROM and electrically eraseable - will not detract from the cost effectiveness or adoption of EPROM. Many microprocessor systems have stable code and data storage requirements that are unlikely to need frequent field changes that justify the use of FLASH devices. But manufacturers wish to continue to have the flexibility to implement upgrades during manufacturing and so do not chose the most cost effective solution which is the mask programed ROM.

Recent developments in systems such as workstations using 32 bit microprocessors or printers offering a large choice of fonts and offering Postscript, require higher density and higher speed performance EPROMs.

The trend, shown in Figure 1, shows that the density of EPROMs has quadrupled every three years in the last decade. Improved performances, in particular access time and programming time, have been achieved, even with an increase in chip size for every successive generation. This rapid evolution has been achieved mainly because of the typical self-aligned, stacked cell, shown in the SEM photograph of Figure 2, with its ability to be scaled down, together with the supporting technologies and improvements in photolithography.

An EPROM cell consists of a single transistor whose threshold voltage is modified during programming by the injection of hot channel electrons on to its floating gate. To erase the EPROM, ultraviolet light is used to excite these electrons over the oxide barrier.

In developing higher densities which demand very high performance dielectrics and high voltage architectures, EPROMs have been the technology drivers which have resulted in many other products, for example microprocessors which include on the same chip many types of memory, RAM, ROM and EPROM or EEPROM.

The key points for multi-megabit EPROM technology are:

- **Compactness:** the possibility to reduce chip dimensions and cost.
- **Speed:** better device performance including both faster access time and reduced programming and test times.
- **Reliability:** good retention characteristics.
- **Manufacturability:** that is an overall valuation of the critical points of the process architecture and technology steps. For example for the process architecture the sensitivity to variations in the process technology parameters, or for the technology steps the suitability to meet defectivity targets.

Compactness

The EPROM technology trend beyond 1 Megabit size is shown in Table 1. The scaling factor is about 0.75 for each generation. To have some idea of the meaning of squeezing the memory cell area, consider that every three generations the EPROM cell fits in the contact hole area of its great grandfather: contact size was 9 μm^2 the 64K bit generation and 4 μm^2 in the 256K bit; the 4 Megabit cell, at 9 μm^2 fits the contact hole area of the 64K device and the 4 μm^2 cell of the 16 Megabit fits the contact hole of the 256K. Consequent layout rules have become more and more aggressive, stressing the role of photolithographic development.

Scaling down dimensions, taking into account the high voltage needed for programming, imposes the need for improvements of active and passive parasitic elements. As the process complexity increases the equipment requisites in terms of process control are more severe due also to the adoption of larger wafer sizes.

From an economical point of view, redesign in a new technology of previous memory sizes reduces costs and increases profitability of products that have already reached maturity in the market.

Speed

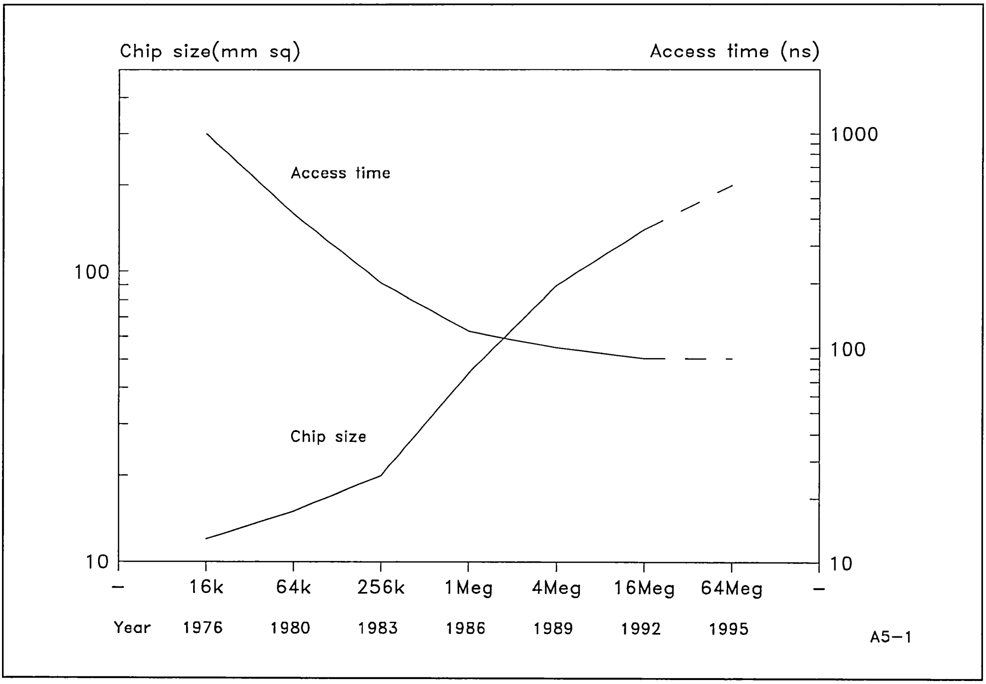
It becomes more difficult to achieve higher speeds in terms of access time as memory capacity increases, because an increase in chip size produces an increase in wiring capacitance and wiring resistance. A typical scenario is the technology scaling factor of 0.75 for a new generation, but an increase of complexity by a factor of 4. Bit line delay is proportional to single bit parasitic capacitance (the bit line resistance is neglected since it is a metal interconnect). This means that increasing the number of bits by 2 and reducing the single bit parasitic capacitance by 0.75, the bit line delay increases by 1.5 times. In the other direction the word line delay is proportional to the single bit parasitic RC time constant (in this case the resistance cannot be ignored as the interconnect of the word line is polysilicon covered by silicide) times the square of the number of cells in the minimum decoded array. This means, for the same example, an increase of the word line delay by a factor of 3.

Despite these inherent difficulties a high speed can be realized, as was shown in Figure 1, mainly by not increasing the size of the decoded array, which means increasing the area occupied by the decoders and as a consequence the overall chip area. Access times will eventually reach a limit as shown by the forecast for the 16 Megabit in Figure 1.

In the future we can expect that EPROM technology will divide so that large memory capacity oriented architectures will co-exist with high speed orientated ones. More aggressive high density EPROM cell designs are being evaluated to allow rectagularization of the array with long bit lines and short word lines.

EPROM cell design also affects speed, high memory cell current in reading and fast programming time are the main issues to trade off against the parasitic effects. In the 4 Megabit generation the typical memory cell in writing conditions ensures more than 3 Volts threshold shift after less than 10 µs programming time.

Figure 1. Chip size and access time



Reliability

EPROMs display excellent non-volatile characteristics, with the ability to retain their programed contents for over ten years, typically twenty. This is accomplished by storing electrons on a floating polysilicon gate. Because a typical EPROM has of the order of 100,000 electrons stored on its floating gate, it is sensitive to leakage currents through the oxide as low as 10^{-23} Amps, this is equivalent to a leakage of less than 10 electrons per day!

Data retention is not only determined by the leakage mechanism but also by charge sharing by mobile positive charges. A positive charge density of 10^{12} ion/cm^2 attracted near the floating gate can destroy the information stored in that bit. This means that only 10 ppb of ionic contamination into the passivation layers could affect data retention.

Other key reliability failure modes, such as electromigration, hot electrons, oxide wearout, etc have to be evaluated in the severe environment of high programming voltage and high temperatures used for the bake tests (at 250 °C) used to ensure data retention.

However due to the introduction of new oxide formation steps, device structures such as LDD (Lightly Doped Drain) and other technological innovations, reliability has reached a very high level.

The technological step evolutions for the 1 Megabit EPROM and beyond are shown in Table 2. Each star represents a technology or device innovation with respect to the previous generation. It is important to note that new photolithography has to be introduced in every new generation. Key points in the evolution are the improved interpoly dielectrics to improve data retention, barrier layer metal to improve contact resistance and reliability, as well as poly-silicide gates and LDD transistors to improve speed and high voltage handling.

Manufacturability

Four important curves bound a region in which an EPROM cell must operate to give good overall performance over a spread of manufacturing variations. These are shown in Figure 3.

The curve A at the bottom plots the gate length against the drain voltage which achieves a 3V threshold shift with a writing time of 15 microseconds and a typical applied gate voltage of 11.5 Volts. These values represent the typical good writing performance for a 4 Megabit memory cell.

Curve B is a limitation set by the need to have a reading current high enough to meet the access time speed targets for the memory. Longer gate lengths give lower currents.

Curve C is the limit imposed by the gate breakdown voltage and by an effect known as “drain turn-on” in which the leakage of unselected memory cells on the bit line causes a voltage drop and degradation of the programming characteristics. Remaining below curve C ensures that a cell with 10nA leakage has a good performance.

Snap back must be avoided because the high substrate currents it causes can lead to latch up in CMOS devices and consequent device damage. A minimum drain voltage is required to avoid snap back, this is shown as curve D.

Table 1. EPROM Technology trend

	1 Meg	4 Meg	16 Meg	64 Meg	Unit
Gate Length	1.2	0.8	0.6	0.4	µm
Active Area w/s	1.0 / 2.0	0.8 / 1.6	0.6 / 1.5	0.4 / 1.0	µm
Gate Pitch w/s	1.2 / 1.6	0.8 / 1.4	0.6 / 0.8	0.4 / 0.5	µm
Metal Pitch (two contacts)	2.8 / 1.6	2.0 / 1.0	1.2 / 0,8	0.8 / 0.5	µm
Contact Size	1.4 / 1.6	1.0 / 1.0	0.6 / 0.6	0.4 / 0.4	µm
Gate Oxide	280	200	160	130	Å
Cell Area	19	9	4	1.5	µm^2
Die Size	46	90	140	200	mm^2
Wafer Diameter	150	150	150 - 200	200	mm

Table 2. EPROM Technology evolution

	1 Meg	**4 Meg**	**16 Meg**	**64 Meg**
Min. Feature	1.2 µm	0.8 µm	0.6 µm	0.4 µm
CMOS scheme	* n-well	* Twin-tub	* Twin-tub	* Twin-tub
Isolation	LOCOS	LOCOS	* Advanced	* Recessed
Interpoly	Oxide	Oxide	* Oxide / ONO	* ONO
Gate	* Silicide	* Silicide	* Silicide	* Silicide & p*/n* poly
Drain	* LDD nch	* LDD nch/pch	* LDD nch/pch	* 3.3V nch/pch
Interlevel	PSG	* BPSG	* BPSG / RTP	* BPSG / RTP
Photolito	* G-Line	* I-Line	* I-Line	* Deep UV
Contacts	* SA on	* Barrier	* W plug	* W plug
Interconnect	1 metal	1 metal	1 metal	* 2 metal

Note: * indicates a technology or device innovation compared to the previous generation.

Figure 2. 4 Megabit EPROM cell

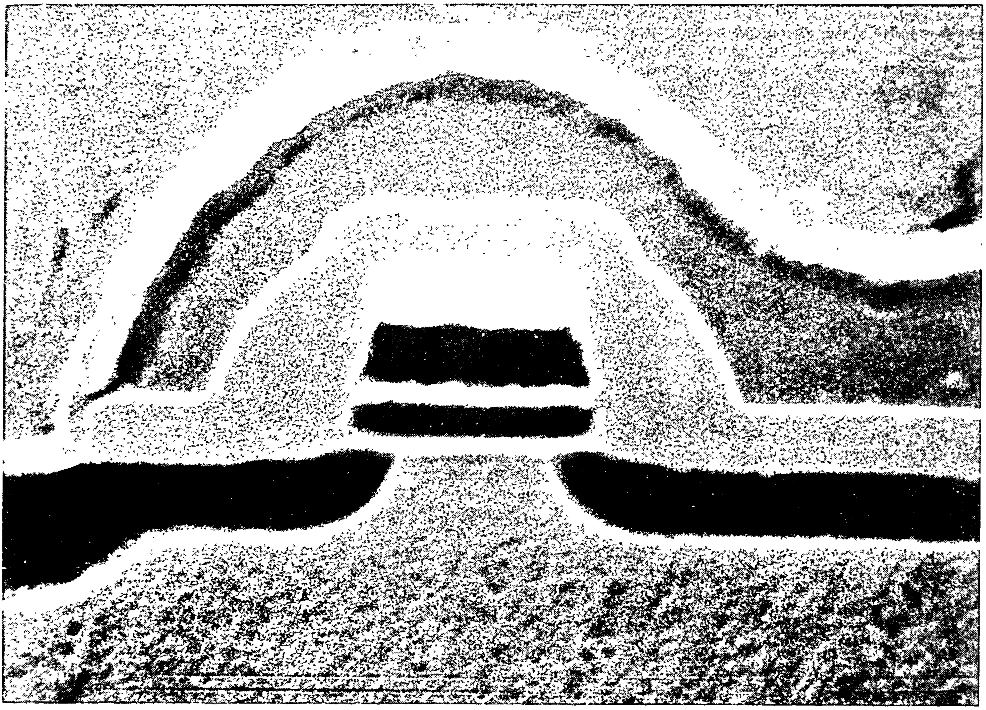


Figure 3. Cell working area, 4 Megabit EPROM (cell 9μm²)

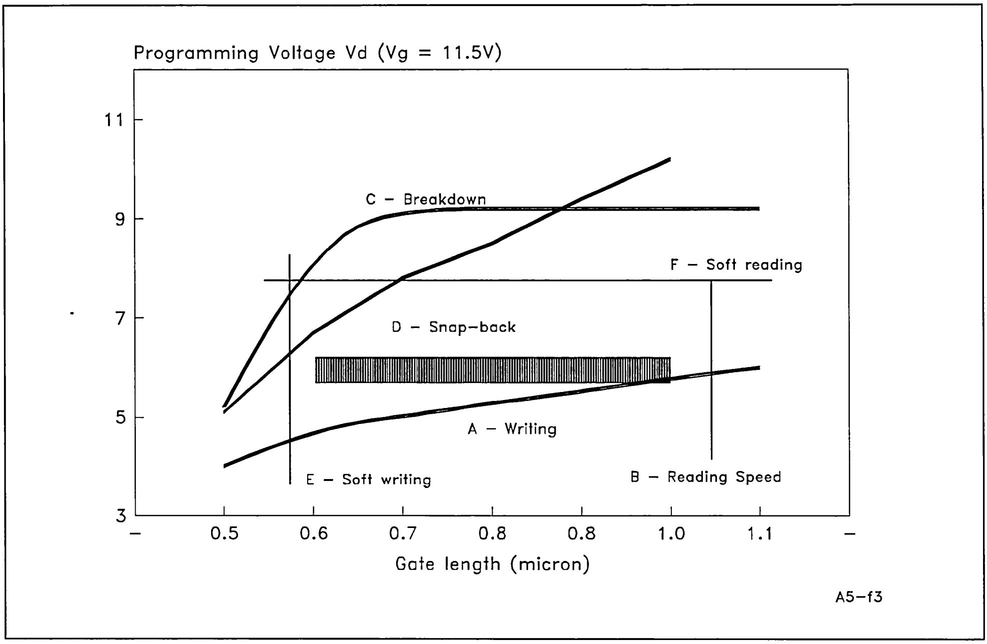
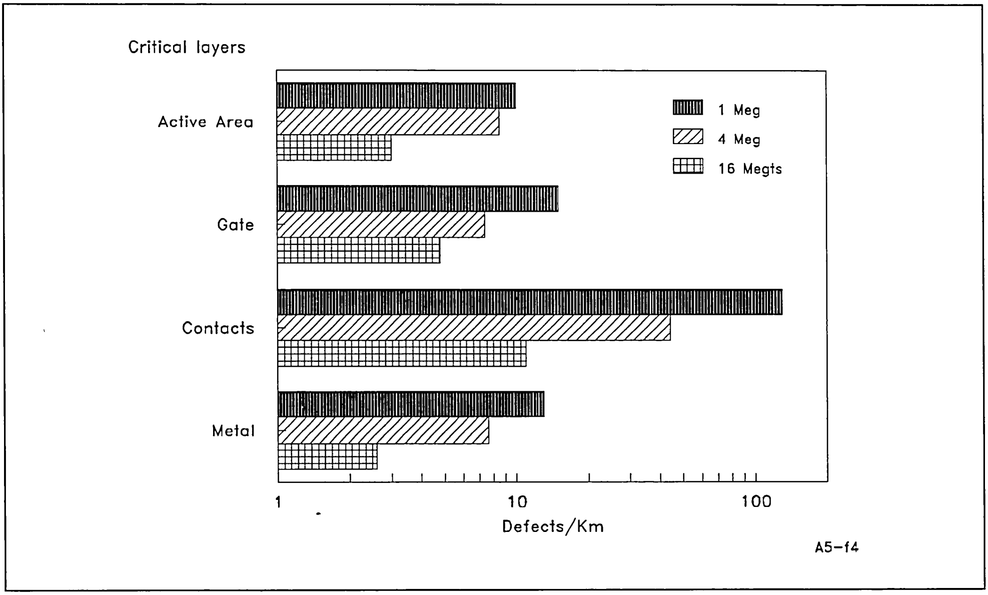


Figure 4. Defectivity targets, 1 Megabit to 16 Megabit EPROM



Manufacturability (cont'd)

These four curves define a region within which good EPROM cell performance may be obtained. Manufacturing neccessities require that the good behavior be guaranteed in spite of spreads in the writing drain voltage and gate length variations. The curves define a rectangular area shown in Figure 3, which represents a cell suitable for manufacturing. For a drain voltage of 6.1 Volts ± 300 millivolts the cell performances are well above the acceptable limits over a wide range of cell gate lengths, centered around 0.8 microns.

In addition there are two other limits shown in Figure 3, curves E and F. These are for soft writing and soft erase. Cells with short gate lengths can be affected by protracted reading operations which cause unwanted writing of the cell. Unwanted erasure can also occur at higher drain voltages.

An issue associated with technology scaling which puts continued pressure on yield and reliability is the technology sensitivity to smaller and smaller defects. As device geometry is scaled, defects that may not have had much impact on manufacturability of earlier chips can now cause yield loss and affect chip reliability.

Defectivity targets for each process step are calculated and technology is tuned to meet these specifications. The defectivity targets for the main critical layers of the construction are shown in Figure 4. Defects are shown per kilometer, for a 150 mm wafer, for example the average length of the metal interconnect is about 2 Km.

The targets are achieved by improvements in technology steps through the elimination of process excursions as well as continuously tightening the "normal variation". The use of in-line SPC monitors plays a big role in the qualification and manufacturing of new technologies.

Conclusion

Three main considerations have increased the interest in EPROM technology: first the increase in the use of EPROMs as non-volatile memories, second the need for leading edge submicron processes to meet targets of speed and density, and finally the EPROM technology skill that has resulted in improved process control methodologies, automation and manufacturing science to meet defectivity and reliability targets. For the future these form an excellent basis for the continued development of higher density EPROMs and the newer FLASH MEMORY products.

With acknowledgements to G. CRISENZA, whose inputs were the basis for this article.

SGS-THOMSON
MICROELECTRONICS

TA107

TECHNICAL ARTICLE

Fast access time non-volatile memory ZEROPOWER solution

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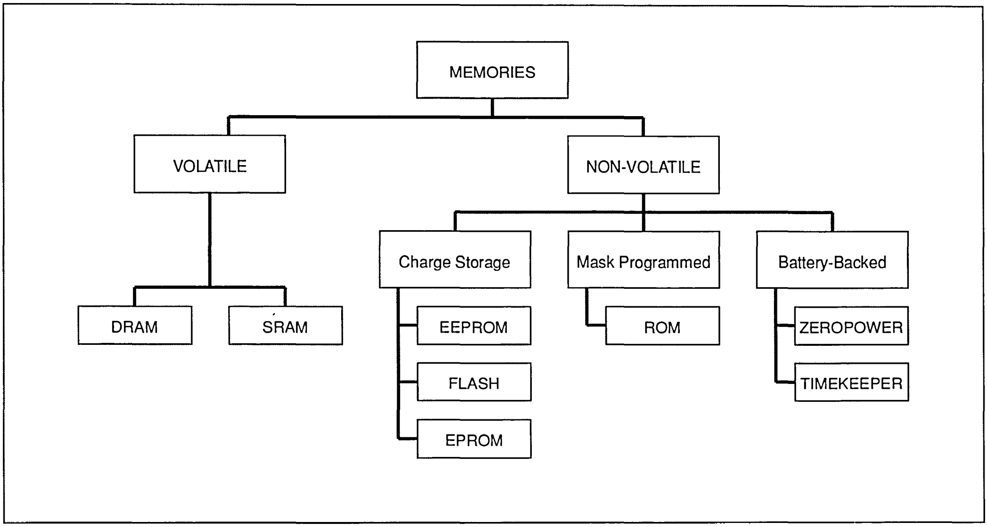
Memories are one of the most important semiconductor products in the whole spectrum of devices made today, they are fundamental in all systems that process or store information. The variety of memory products produced is very broad, but they can be broken down into two major families - volatile and non-volatile memories. Volatile memories are those types that loose their stored contents when the power is removed, while non-volatile memories are able to retain the stored data without external power applied.

Volatile Memories

Typical of the volatile family are the DRAM and the standard SRAM types, products which have medium to fast access times for both reading and writing (10-200ns) and medium to high storage capacities (in regular production up to 4 Megabit for DRAM or 1 Megabit for SRAM). DRAMs store their information bits by a charge on a small capacitor, which must be continuously refreshed to prevent charge decay with subsequent loss of the data. SRAMs use a simple 'flip-flop' circuit to store data, the state of which will be lost if power is removed, even momentarily, from the circuit.

Figure 1. Family tree of memory types



Non-volatile memories

There are more varieties of non-volatile mem-ory products. The simplest is the mask pro-gramed ROM which has read access times of 80-200ns but must be "written" at the manufac-turing stage by a custom program mask.

The most widely used non-volatile memory is the EPROM. This memory can be programed electrically, taking 10µs to 100µs per byte, and erased by exposure to UV light for about 20 minutes. The read access time is however compatible with DRAMs, in addition some high speed EPROM products offer fast 55-80 ns read access times. EPROMs store the mem-ory content by holding an electron charge on a floating gate in a dual gate transistor cell, devices up to 4 Megabit are in full production.

The EEPROM also stores its contents by charge on a floating gate in the same way as an EPROM, but can be written and erased electrically, byte-by-byte. Access times are similar or a little slower than an EPROM. EEPROMs however are limited in size due to the higher circuit complexity needed for byte erase and the size of the cell in the design, products up to 1 Megabit are available, with smaller sizes up to 16K having serial I/O bus access.

A relatively new development is the FLASH memory, this is a variation on the EPROM/EEPROM, able to be programed byte-by-byte like an EPROM, but erased electrically in bulk (ie, in a flash). The information is stored as a charge on a floating gate. The mechanism for loading the charge on the floating gate is like the EPROM (hot electrons) but for charge removal it is like the EEPROM (tunneling). Write and erase times are slow (milliseconds to seconds) but read access times are similar to EPROM. Future developments of the FLASH memory seem likely to take over a part of the ROM and the EPROM markets, and to stimulate new uses for semiconductor memory, for example the replacement of the floppy disk.

System needs

In many of today's applications, non-volatile memories are required which provide fast read, write *and* erase access times and retain their contents reliably when the power supply is removed. In addition the memory must be protected from false write operations at times when the system power supply is outside the specification limits. When the supply is completely removed the memory must switch its operation to a non-volatile storage mode.

Non of the traditional non-volatile memories (EPROM-FLASH-EEPROM) offer fast write times, all requiring milliseconds rather than nanoseconds to store a byte of data. FLASH memories have a very slow "in-system" speed as they must be programmed and erased, an operation requiring seconds, before they can be re-written. Memories types like the EPROM, FLASH and EEPROM which use charge storage also have a limited erase/write cycle life, ranging from 100 or so cycles for an EPROM, 1000 to 10,000 for a FLASH and up to 1,000,000 for the best EEPROMs.

Table 1. Access times of memory types, and data storage method

Memory	Access Time			Storage Method
	Read	Write	Erase	
DRAM	70 - 150ns	70 - 150ns	—	Charge on capacitor
SRAM	10 - 200ns	10 - 200ns	—	"flip flop" circuit
EEPROM	100 - 200ns	5 - 20ms	5 - 20ms	Charge on floating gate
FLASH	100 - 200ns	10 - 100µs	1-5sec.	Charge on floating gate
EPROM	80 - 250ns	10 - 100µs	20 min.	Charge on floating gate
ROM	< 100ns	—	—	Masked in production
ZEROPOWER	100 - 150ns	100 - 150ns	—	SRAM with battery back-up
TIMEKEEPER	100 - 150ns	100 - 150ns	—	SRAM with battery back-up

For these reasons designers have frequently resorted to using SRAM products and providing a battery and switch over circuits as a solution. The complexity of the discrete circuits needed to implement these functions reliably can become costly, both in design time, in PC board area and components. Moreover many standard SRAMs are not designed for very low power standby consumption, meaning either that a bigger and more expensive battery must be used, or that a shorter life time between battery replacements must be accepted.

ZEROPOWER and TIMEKEEPER memories

A solution to the need for long life, non-volatile memory with fast read, write and erase times is the ZEROPOWER range of SGS- THOMSON Microelectronics. These products function exactly like a standard SRAM with 100 - 150 ns access time when power is applied. But switch over to battery maintained operation when the external power is removed. They are specially designed to have ultra low standby current consumption to give long battery life.

Incorporated on the same chip as the SRAM is a circuit to detect power failure at an accurate trip voltage, this circuit write protects the memory when the power falls below the system specification level. At a lower voltage it activates a chang-over from external supply to battery back-up for the SRAM.

The construction of the ZEROPOWER prod-ucts is a standard DIP package for the SRAM with a "top-hat" mounted above which contains the battery. Thus providing a pin compatible, plug in replacement for a standard SRAM. The pin-out is the JEDEC standard for SRAM, closely matching also that of EPROM and EEPROM products.

Two sizes of ZEROPOWER memory are available, the MK48Z02 offering 2K bytes of memory and the MK48Z08 with 8K bytes of SRAM. When external power is applied these memories provide SRAM performance with read and write access times of 100-150 ns.

The external supply is constantly monitored and if it falls below the power fail threshold, the ZEROPOWER will automatically power-fail deselect, thus write protecting itself. The detection window for the power fail deselect (PFD) is accurately controlled, and the prod-ucts are offered in two versions suitable for systems with supplies of an accuracy of 5% or 10%. The voltages for PFD are 4.75-4.5V or 4.5-4.2V.

At a lower voltage of Vcc, around 3V, the SRAM is switched over to battery power to maintain its contents. In order to provide a monitor of the battery state, its voltage is checked when external power is re-applied and rises to the switch over point. If the battery voltage was too low a warning flag bit is set and can be checked by the software after power up. This flag therefore indicates that the memory contents could be unreliable.

One of the major concerns in non-volatile memory systems is the retention life of the memory. Typical EPROM or EEPROM products offer 10 year data retention. For a battery backed SRAM the retention

Table 2. Pros and Cons of EPROM, FLASH and EEPROM

Memory	Advantage	Disadvantage
EPROM	Low cost	Very slow erase Slow write time 100 cycle endurance
FLASH	Electrical erase in circuit	Bulk erase only Slow write time 10,000 cycle endurance
EEPROM	Electrical erase byte-by-byte 1,000,000 cycle endurance	Slow write time High cost

depends on the battery characteristics. The life of the battery is controlled by the temperature and almost independent of the percentage of time the ZEROPOWER device spends in battery back-up mode. From the results obtained in nearly 10 years of testing of battery performance, SGS-THOMSON is able to guarantee a battery life of more than 11 years, worst case, at the maximum operating temperature of 70 deg C. This is equivalent to nearly 200 years at room temperature.

Memory plus Real Time Clock

Another non-volatile memory product family using the same ZEROPOWER technology are the TIMEKEEPERs. These provide both a battery backed SRAM with power fail deselect and back-up operation, plus a Real Time Clock.

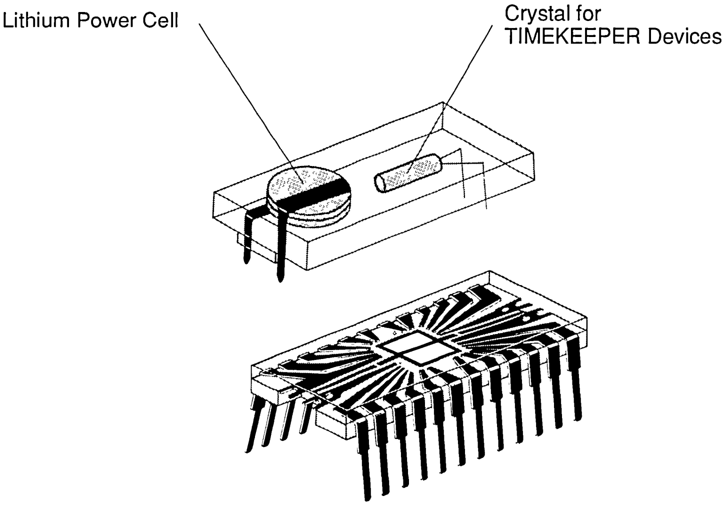
A special, very low power, 32,768Hz oscillator is incorporated in the chip design, together with a clock divider chain. The time from the clock is copied once per second into registers which are part of the SRAM address space. The user can therefore read the time, coded in BCD, as year, month, day, date, hour, minute and second. The clock automatically corrects for months with 28 to 31 days, and for leap years. The crystal for the clock oscillator is built into the “top-hat” mounted above the device dual-in-line package.

The time may be set by software and the calibration of the clock can also be made by software programming, as an ’advance’ or ’retard’ count of the clock divider chain.

The MK48T02 provides a 2K byte SRAM and the more advanced MK48T08 an 8K SRAM capacity. The MK48T02 clock crystal has an accuracy of +/-35 ppm, giving an accuracy of +/-1.53 minutes per month, worst case, typically it is better than +/-1 min/mth. Digital calibration can be made up to +/-63 ppm or +/-5.35 sec/mth.

The MK48T08 provides a memory capacity of 8K bytes and has an extended calibration range of +5.5 or -2.7 minutes per month.

Figure 2. Exploded view of TIMEKEEPER construction



Battery life

The life of the battery for the TIMEKEEPER devices depends on the current consumption of the clock oscillator and divider chain. The MK48T02 requires 1.2µs but the MK48T08 has an ultra low power circuit consuming only 445 nA. The life expectancy for the battery of the MK48T02 running continuously in battery back-up mode is 3.5 years, and over 10 years for the MK48T08.

The ZEROPOWER and TIMEKEEPER devices have found applications in many areas, from Fax and Copy machines where they provide time information and store phone numbers or service/usage data, to the recent Paris-Dakar rally where TIMEKEEPER devices were used to provide accurate timing for the navigation computers.

They provide an economic solution to the need for non-volatile memory with SRAM read and write speed performance, saving design time and many discrete components. All the products are single chip designs offering the highest possible reliability.

TECHNICAL ARTICLE

Built-in reliability for 10 FITs performance on EPROM and FLASH MEMORY

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Floating gate memories have better reliability than SRAMs or DRAMs because they are less sensitive both to breakdown of the oxide layers at low voltages and to soft errors. In addition floating gate memories are designed to operate at the high voltages needed for programming and are tested at these voltages during production as a screen to ensure good oxide integrity. Whereas the oxides of SRAM or DRAM products are thinner and cannot be tested with high voltage to screen oxide integrity.

Floating gate memories, with an oxide barrier height of 3.2eV, have an almost infinite capability for charge storage, even at high temperatures. The number of carriers generated by an alpha particle passing through the thin oxide of the floating gate is very small compared with those generated in the silicon substrate. Thus the effect of an alpha particle on the memory's stored data is small for a floating gate memory compared to that for a volatile memory where the data is stored on a node connected to part of the circuit diffused in the substrate.

Failure rate for floating gate memories is determined mainly by defect density of the technology. Quality of dielectrics is the key issue in their reliability, both for data retention in time and for endurance during repeated programming and erasure. Retention is affected by conduction at low electric fields and endurance by wearout of the oxides due to repeated high field tunneling.

Device Structure

Both EPROM and FLASH MEMORY use a "stacked gate cell", that is a cell design with a floating gate and a control gate directly above the n-channel of the MOS transistor. Both EPROM and FLASH MEMORY are programmed by channel hot-electron injection, the EPROM is erased by a photoelectric effect caused by exposure to UV light and the FLASH MEMORY is erased by tunneling through a thin gate oxide.

The memory cell structure is a T-shaped layout, see Figure 1. The cell size is determined horizontally by the metal line pitch and vertically by the source line width, source line to word line space, gate length, gate to contact distance and contact size. The actual dimensions of the latest 4 Megabit EPROM memory are a cell size of 2.0 x 2.1 microns. The cross sections of the cell in two directions are also shown in Figure 2 and Figure 3. The arsenic doped source and drain junctions are self aligned to the gate and are symetrical for the EPROM, while a phosphorous diffusion is added to the source of the FLASH MEMORY to create a tunnel region and allow high voltage to be applied for erasure. A boron dose is usually implanted in the channel to increase programming efficiency by enhancing electron multiplication.

FLASH MEMORY and EPROM cells are programmed by applying positive voltage pulses to the control gate and the drain. EPROM erasure is made by a long period of UV light exposure. FLASH MEMORY cell erasure is made by first programming all cells, then applying a high voltage to the source to cause electrons to tunnel from the floating gate through the thin oxide area overlapping the source. During the erase operation the drain is floating to prevent a large channel current.

When a charge is loaded on the floating gate the threshold voltage of the enhancement mode transistor increases. The threshold increase is equal to the charge loaded divided by the total capacitance of the floating gate (to the control gate, source, substrate and drain). The voltage on the floating gate depends on the charge, the voltages on the other electrodes and the capacitive coupling between the gate and these electrodes. The electric field stresses on the thin oxide and the interpoly oxide depend on the applied voltages and the charge on the floating gate.

Figure 1. Layout of a T-shaped stacked gate cell

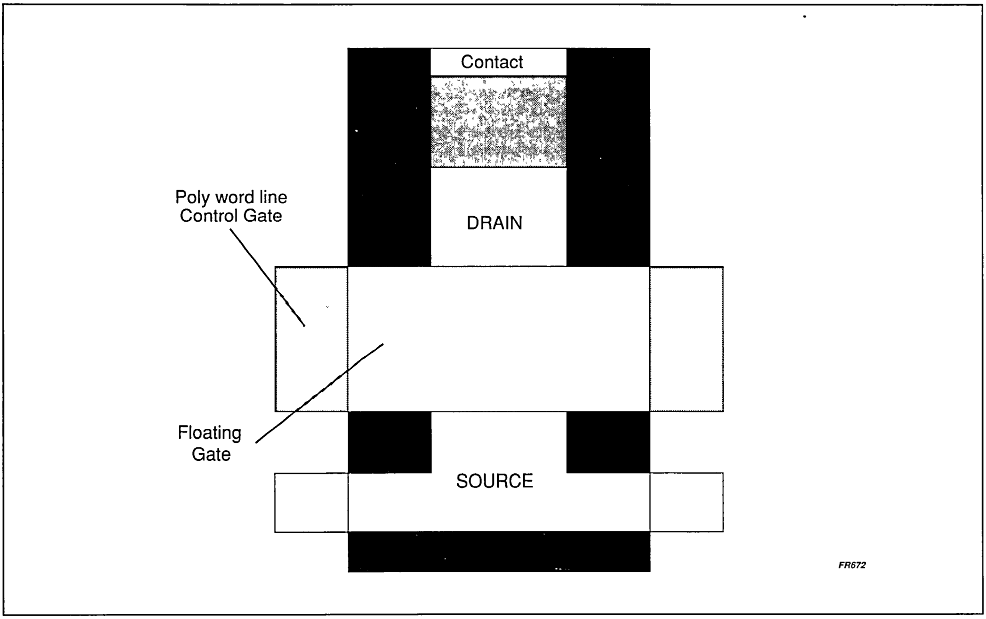
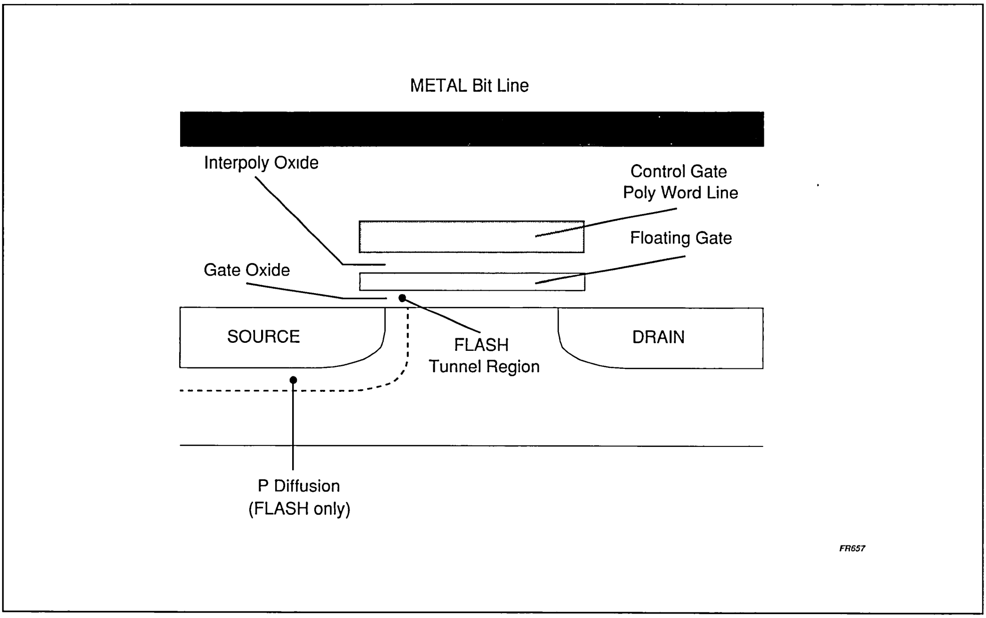

Contact
DRAIN
Poly word line
Control Gate
Floating
Gate
SOURCE
FR672

Figure 2. Vertical cross-section


METAL Bit Line
Interpoly Oxide
Control Gate
Poly Word Line
Floating Gate
Gate Oxide
SOURCE
FLASH
Tunnel Region
DRAIN
P Diffusion
(FLASH only)
FR657

RETENTION

Retention is a measure of the integrity of the stored data, held as a charge on the floating gate. It measures the time between programming and a fault in reading the data value. The data may be lost due to either charge loss or gain and due to intrinsic or defect related mechanisms. In addition during programming some stresses may affect data retention.

Programming

There are three main stress conditions that can occur when programming the array: DC Erase, Program Disturb and DC Program. These affect memory cells sharing a common gate (word line) or a common drain (bit line) as shown by the section of the memory array circuit in Figure 4. These programming stresses affect both the manufacturers production yield due to failures at programming verification, but also field reliability after prolonged reading cycles. Important design choices of the reading and programming voltages minimize these effects.

Typical programming voltages of 7V on the bit line (BL) and 12V on the word line (WL) are shown.

DC Erase

With the bias conditions shown in Figure 4, the previously programmed cell A is affected by DC Erase due to a high gate stress which results in charge loss from the floating gate. It occurs when another cell (eg B) on the same word line is programmed by applying a high gate voltage to the word line. Cell A sees this high voltage on its second poly word line while its drain bit line is held at 0V. A high electric field occurs across the interpoly oxide, large enough to cause tunneling, a loss of charge on the floating gate and lowering of the programmed threshold voltage of the cell. A similar effect could occur during reading of the memory array, and so the same defect could be induced by prolonged read cycling. The potential diagram for this condition is shown in Figure 5. As a test screening method the DC Erase can be used to test the quality of the interpoly dielectric.

Program Disturb

Program Disturb affects cell D of Figure 4 and is due to a high voltage on the drain while the gate and source are at 0V. this results in drain stress shown in the potential diagram of Figure 6 when programming bits on the same bit line.

Figure 3. Horizontal cross-section

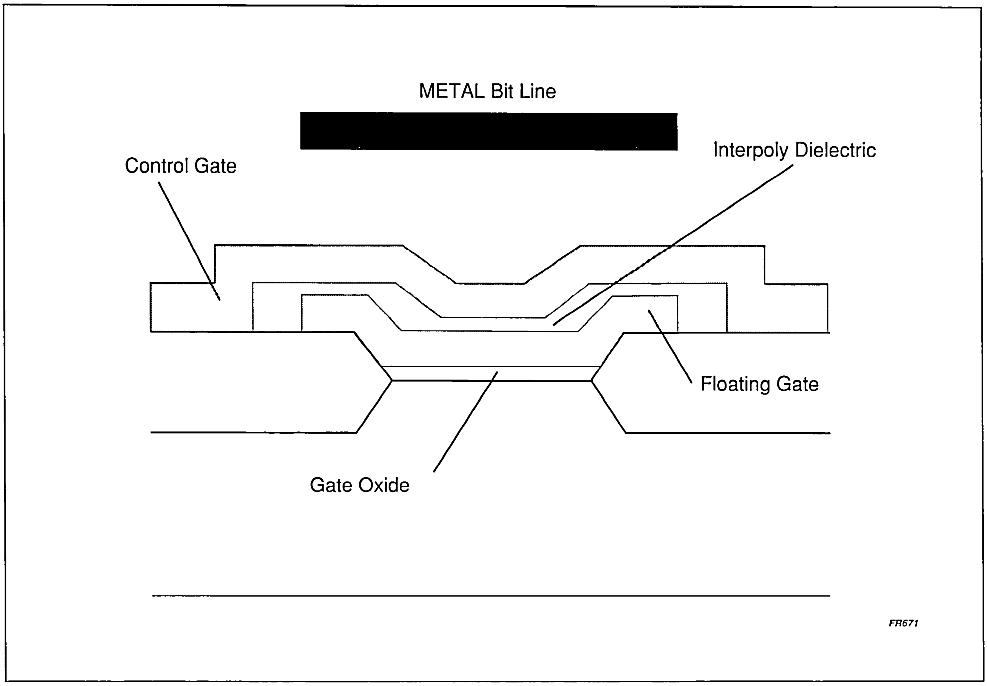


Figure 4. Memory array showing stress conditions resulting from programming

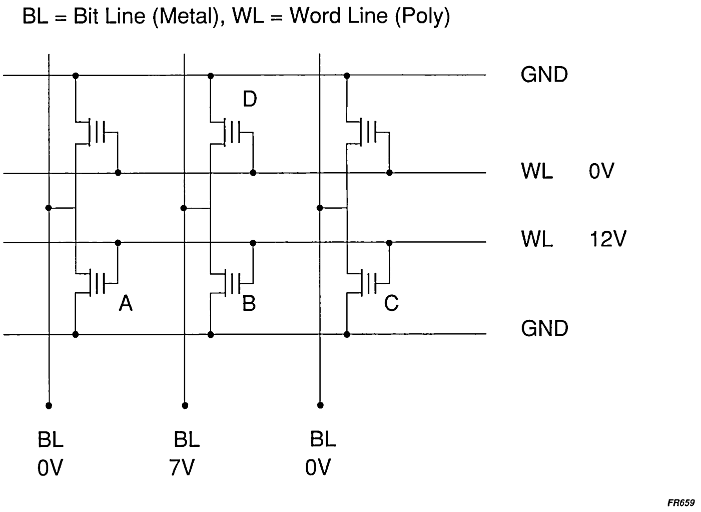

BL = Bit Line (Metal), WL = Word Line (Poly)
GND
D
WL 0V
WL 12V
A
B
C
GND
BL 0V
BL 7V
BL 0V
FR659

Figure 5. Potential diagram for gate stress on a programmed cell

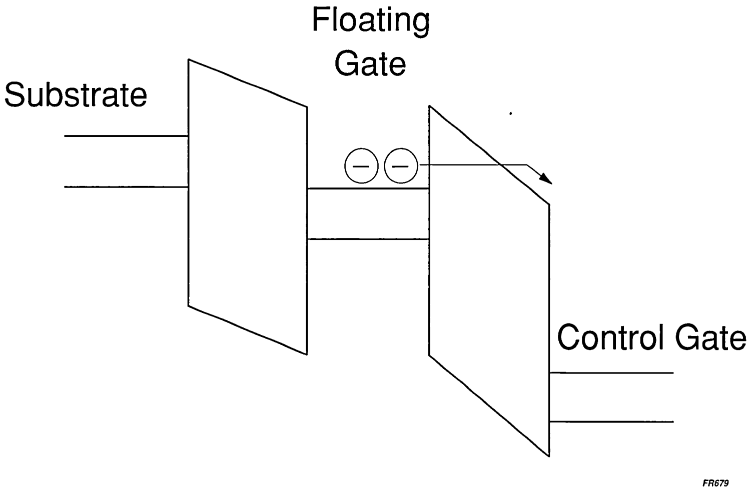

Floating Gate
Substrate
Control Gate
FR679

Figure 6. Potential diagrams for drain stress on a programmed cell

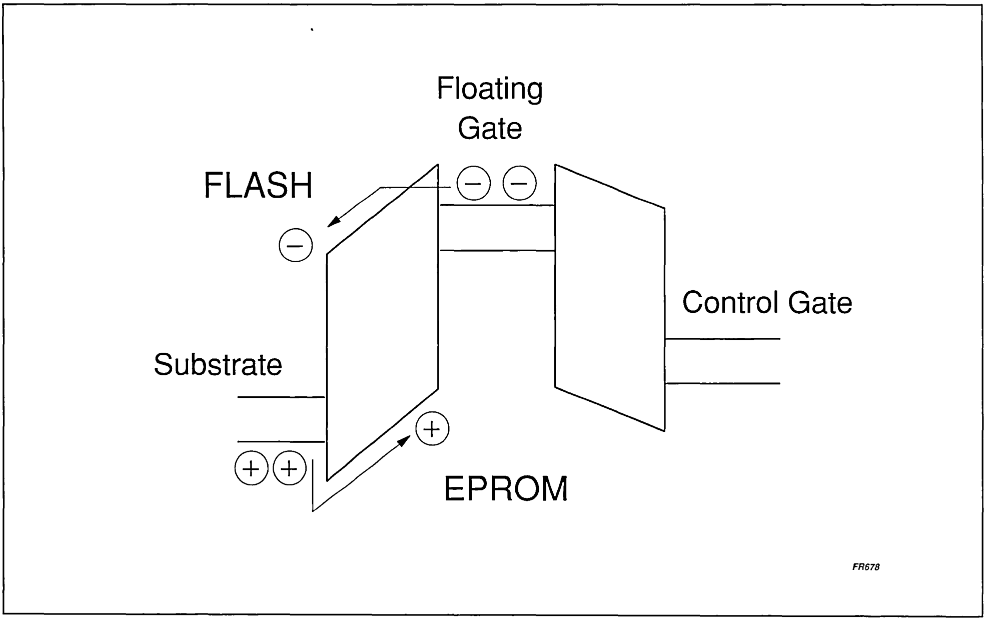
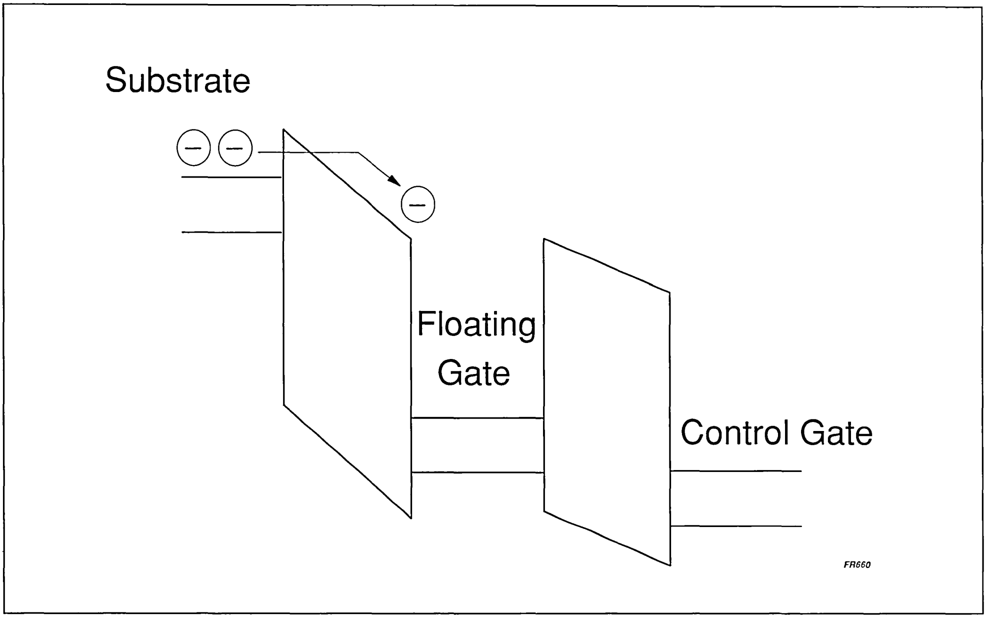

Floating
Gate
FLASH
Control Gate
Substrate
EPROM
FR678

Figure 7. Potential diagram for gate stress on an erased cell


Substrate
Floating
Gate
Control Gate
FR660

In the EPROM the electric field causes holes generated in the substrate to collect on the floating gate. In the FLASH MEMORY it causes electrons to tunnel from the floating gate to the drain. For evaluation purposes this stress may be used to assess the quality of the gate oxide of the EPROM or tunnel oxide of the FLASH MEMORY.

DC Program

DC Program affects the previously unprogrammed cell C of Figure 4 and is due to a high voltage on the gate with the source and drain at 0V, causing a gate stress on the erased cell. The potential diagram is shown in Figure 7.

A high voltage on the word line causes electron tunneling from the substrate to the floating gate, mainly on FLASH MEMORY products, and increases the cell threshold voltage. Again a similar effect could occur during extended read cycles.

The effects of these three cell programming factors are a pattern sensitivity which must be checked by proper production screening, and the reduction in Vth of stored logic levels which affects overall reliability and which depends on design choices.

Charge Losses

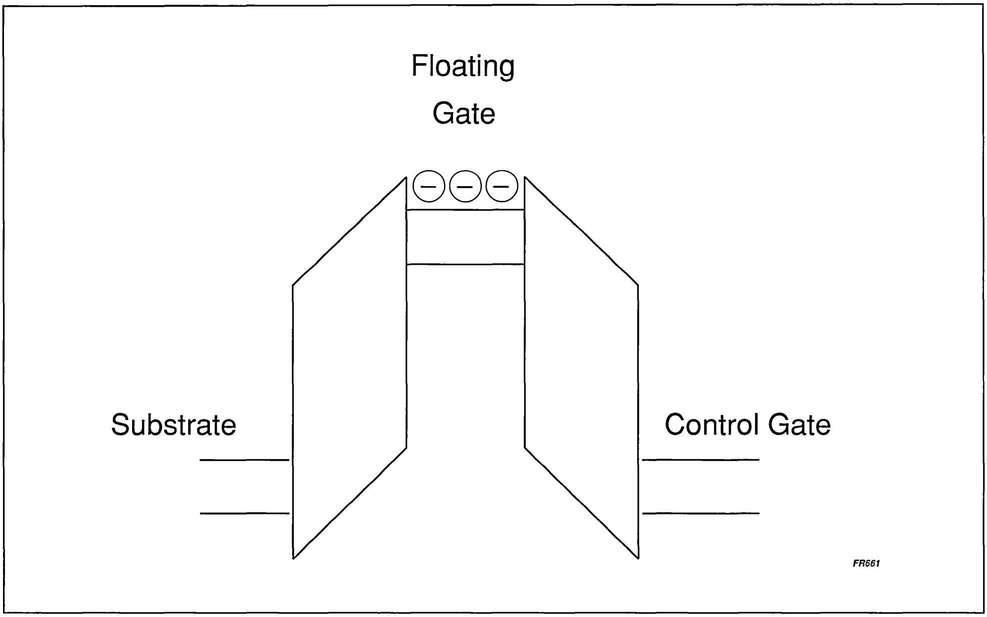
Intrinsic related charge loss. There are two charge loss mechanisms, intrinsic and defect related. Charge transfer due to intrinsic mechanisms is minimal and the retention time for a defect free cell is thousands of years.

However two conduction processes occur in dielectrics leading to intrinsic leakage current: tunneling and thermionic emission. Because of the very low voltage of the floating gate due to its stored charge and self capacitance, the tunneling leakage current does not produce any significant charge loss in tens of years. At high temperatures the thermionic emission could cause charge loss. The potential diagram for a programmed cell is shown in Figure 8. For a cell with a barrier height of larger than 1eV, tests at 250 degC show intrinsic retention of many months, equivalent to a huge number of years at normal temperatures.

But some charge loss is observed with 250 degC bake tests as shown by the decrease in the threshold voltage of a cell with time in Figure 9.

The lost charge seems to be a fixed amount which is a small percentage of the stored charge. The charge loss rate decreases with the time of the bake and does not depend on cell layout. One reason for this is the release of electrons trapped in the interpoly and gate oxides during a previous UV erase.

Figure 8. Potential diagram for a programmed cell



Another is seen in cells using ONO (Oxide - Nitride - Oxide) dielectric due to carrier movements in the Nitride, electrons moving to the Oxide-Nitride interfaces and leakage through the thin oxides. Three mechanisms correspond to three different phases of the curve of Figure 9.

The fast initial threshold change is due to carrier movement in the Nitride or polarisation effects. The second phase is caused by electrons, injected into the nitride during programming, moving from the bottom O-N to the top N-O interface. The third phase is a long term charge loss of electrons leaking through the top thin Oxide.Improvements in the passivation and the use of gettering are being used to provide a solution to the intrinsic charge losses.

Defect releated charge loss. Defect related charge loss is due to structual or statistical defects. These affect the infant mortality or the wearout of the memory. Burn-in can screen for the structural defects by activating failures which can be subsequently detected by a 100% electrical test. However random wearout defects limit most the retention of the memory, these are defect related charge losses caused by latent failures degrading, enhanced by temperature.

Two processes cause statistical defects, electrons escaping the floating gate and ionic effects. Electron escape typically causes single bit failure randomly throughout the memory array. Ionic processes, due to contamination, affect spot areas which are not well protected from environmental contamination - for example holes in the final passivation layer.

Single bit charge loss due to electron escape is probably the most important failure mode in an EPROM as shown by life tests. Figure 8 and Figure 9 show the reading current distribution of 4 Megabit EPROM cells after programming and after 1000 hours at 250°C, with the array specially programmed to easily detect any increase in cell current and so monitor the charge loss. The histogram has very little shift, but a single bit moves away from the distribution and fails.

The defect may be in the interpoly or gate oxide and can be found by making stress tests on programmed or erased cells - a charge gain on an erased cell indicates a gate oxide failure, a charge loss on a programmed cell indicates an interploy dielectric failure.

Figure 9. Threshold shift for an EPROM Cell (ONO) with 250°C bake

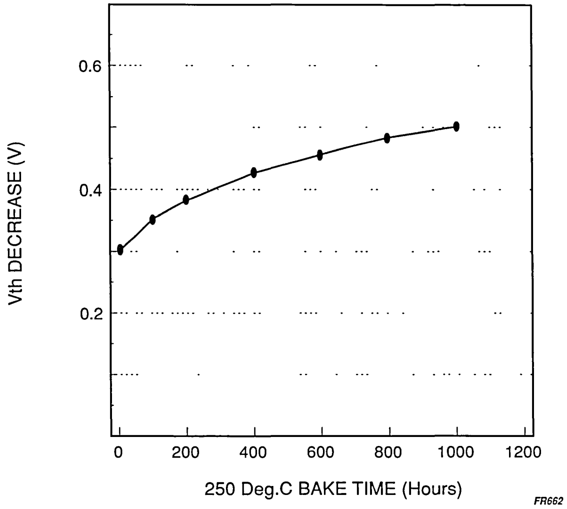


Figure 10. 4Meg EPROM cell reading current distribution after programming

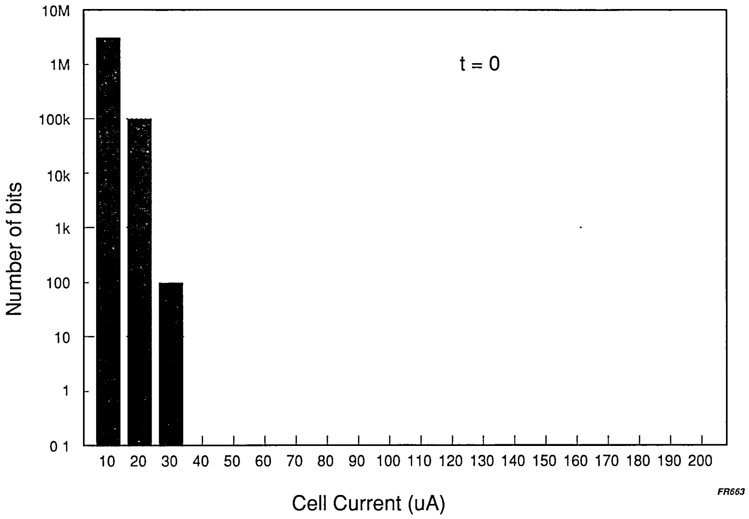
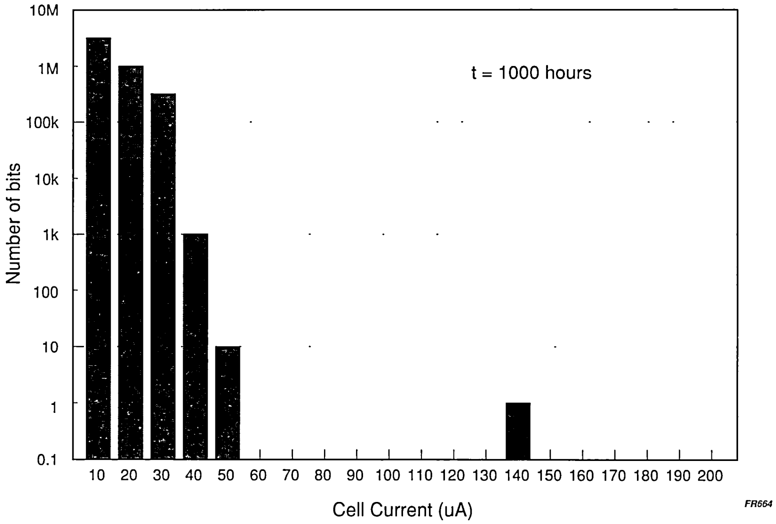


Figure 11. 4Meg EPROM cell reading current distribution after a bake at 250°C



The leakage current of gate oxide failures show a linear dependance on electric field, while it shows an exponential relationship for tunnel oxide and interpoly oxide defects. The temperature dependance displays an activation energy of 0.6eV for gate and interpoly oxides and 0.25eV or less for tunnel oxide. The activation energy for ONO interpoly dielectric is 0.8eV. Figure 10 and Figure 11 show the temperature dependance of the failure times for gate oxide and ONO.

The leakage of the gate oxide is due to hopping conduction. The tunnel oxide leakage is very similar to actual tunneling, during erasure, of the FLASH MEMORY. Charge loss when ONO dielectric is used is associated with poor quality of the bottom oxide but is also affected by the relative thicknesses of the oxide and nitride layers. So many mechanisms come into play that the defect related charge loss is not a fixed amount but depends on the nature and position of the defect itself.

Ionic processes are mostly due to defects such as pin holes in the final passivation or intermediate dielelectric which allow mobile ions to diffuse into the array. These ions compensate the charge on the floating gate and move the threshold voltage of the cell. Ionic contamination can be detected by a sequence of high temperature bake, programming, UV erasure and baking again. The charge loss after the first bake due to the electric field of the stored negaitve charge, and the charge gain after the second bake due to ion concentration gradient, cause a localized region around the pin hole defect to rapidly fail. The activation energy of these types of defects is 1.2 to 1.8eV.

ENDURANCE

Successive program and erase cycles cause progressive damage to the thin oxide under the floating gate of non-volatile memories. The current in the oxide creates traps and damage proportional to the charge density passing through. The result of the trapped charges is that the stored charge on the floating gate has a reduced effect and the threshold change between a programmed and an erased cell narrows as shown in Figure 14.

The endurance is defined as the maximum number of cycles that the memory can withstand before the threshold shift is so small that the bit(s) fail. The intrinsic wearout is due to charge trapping in the thin oxide, whereas oxide breakdown of the tunnel or gate oxide is caused by a defect related failure. FLASH MEMORY have an additional failure mechanism due to hole trapping in the thin oxide.

Figure 12. Temperature dependence of failure time for bits with gate oxide defects

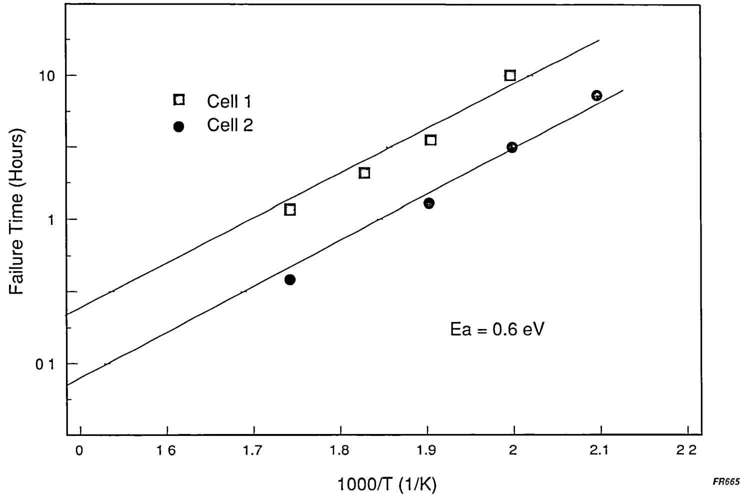


Figure 13. Temperature dependence of failure time for bits with ONO interpoly defects

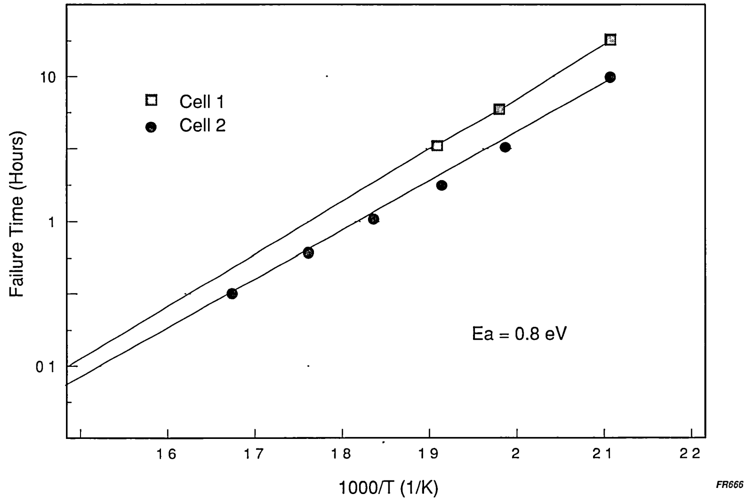
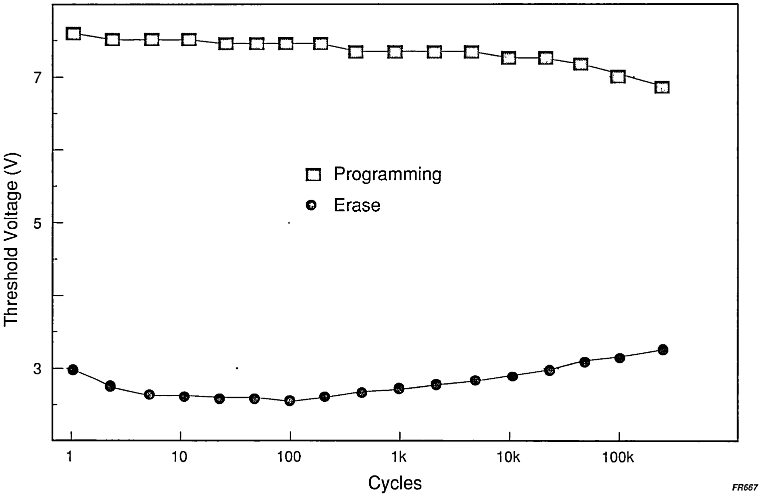


Figure14. FLASH MEMORY programmed and erased threshold voltage versus P/E cycles



Intrinsic endurance is due to trapping of a small amount of the charges flowing through the thin oxide, it is proportional to the square of the oxide thickness and affects a textured poly's oxide more than a thin oxide. It has an activation energy of -0.1eV due to thermal de-trapping during program/erase cycles.

Defect related endurance is an entirely random process of the breakdown of the thin oxide. The breakdown is gradual rather than sudden, and irreversible. Breakdown can occur also in the memory decoding circuits due to the high voltages required for program and erase. A typical defect seen is row or column failure.

Since the endurance performance is due to the thin oxide defects, the memory endurance is proportional to the memory size. However the construction of the cell, see Figure 1, greatly improves the FLASH MEMORY endurance so allowing high density memories with an endurance of a large number of program/erase cycles. The first reason for this is the smaller area of the tunnel oxide with this construction using floating gate and source overlap, as opposed to a construction where the tunnel oxide is defined by a mask. The second is the better intrinsic quality of the tunnel oxide grown over a region of lighter doping of the source. Finally in the FLASH MEMORY the longer, lower voltage erase pulses give a lower stress to the oxide. Figure 14 shows the performance of the FLASH MEMORY cell up to 100,000 program/erase cycles.

SCREENING AND LIFE TESTS

Accelerated life tests are used for reliability assessment. The data retention failure mechanisms are temperature dependant and the most important accelerating factors are known. Failure analysis techniques are advanced and can identify the specific failures. Table 1 shows the activation energies for common data loss mechanisms.

Built-in Reliability

The current approach is to build-in reliability to acheive acceptable failure rates for future floating gate memories. The approach is to understand all the reasons for failure instead of just predicting the time-to-failure. The reliability is assured by control of the manufacturing process and environment.

Effectiveness and cost considerations support this approach: As technological complexity increases and dimensions scale down failure analysis becomes less and less practical. A huge number of devices have to be tested to demonstrate a reliability goal of 10 FITs. Longer test times of high density memories are becoming too costly or even not feasible.

Table 1. Activation energies for common data loss

Failure Mode	Activation Energy
Oxide Breakdown	0.3 to 0.36 eV
Oxide Defects	0.6 eV
Intrinsic Charge Loss	1.2 to 1.4 eV
Intrinsic Charge Loss for ONO	0.36 eV
Ionic Contamination	1.2 to 1.3 eV
Cycling Induced Charge Loss	1.1 eV

All manufacturing aspects have to be controlled, for example the cleanliness of quartzware, the analysis of oxidation ambient or the control of particles due to each process and equipment. In line monitors have to be used to control process variations.

Many process variables can be correlated to each reliability failure mechanism, a fishbone diagram illustrates this dependance. Figure 15 shows a tentative diagram for data retention in EPROM products.The input variables of this diagram can be divided into intrinsic and defect related.

Variation from the target values of parameters, used for the process characterisation, have to be reduced to zero to maintain the intrinsic performance. For example oxide thickness, floating gate doping and stacked gate profile are important for intrinsic data retention.

Defect related failures are improved by modifying, updating or replacing defect generating process steps or equipment. Examples are 'in-process charging' or oxidation ambient.

Ultimately the control of the process dispersions will yield improvements in quality and production yields with a reduction in reliability failures. Table 2 shows the evolution of EPROM and FLASH MEMORY with also the target reliability FIT and quality AOQL.

Figure 15. Fishbone diagram showing input variables which affect floating gate memory data retention

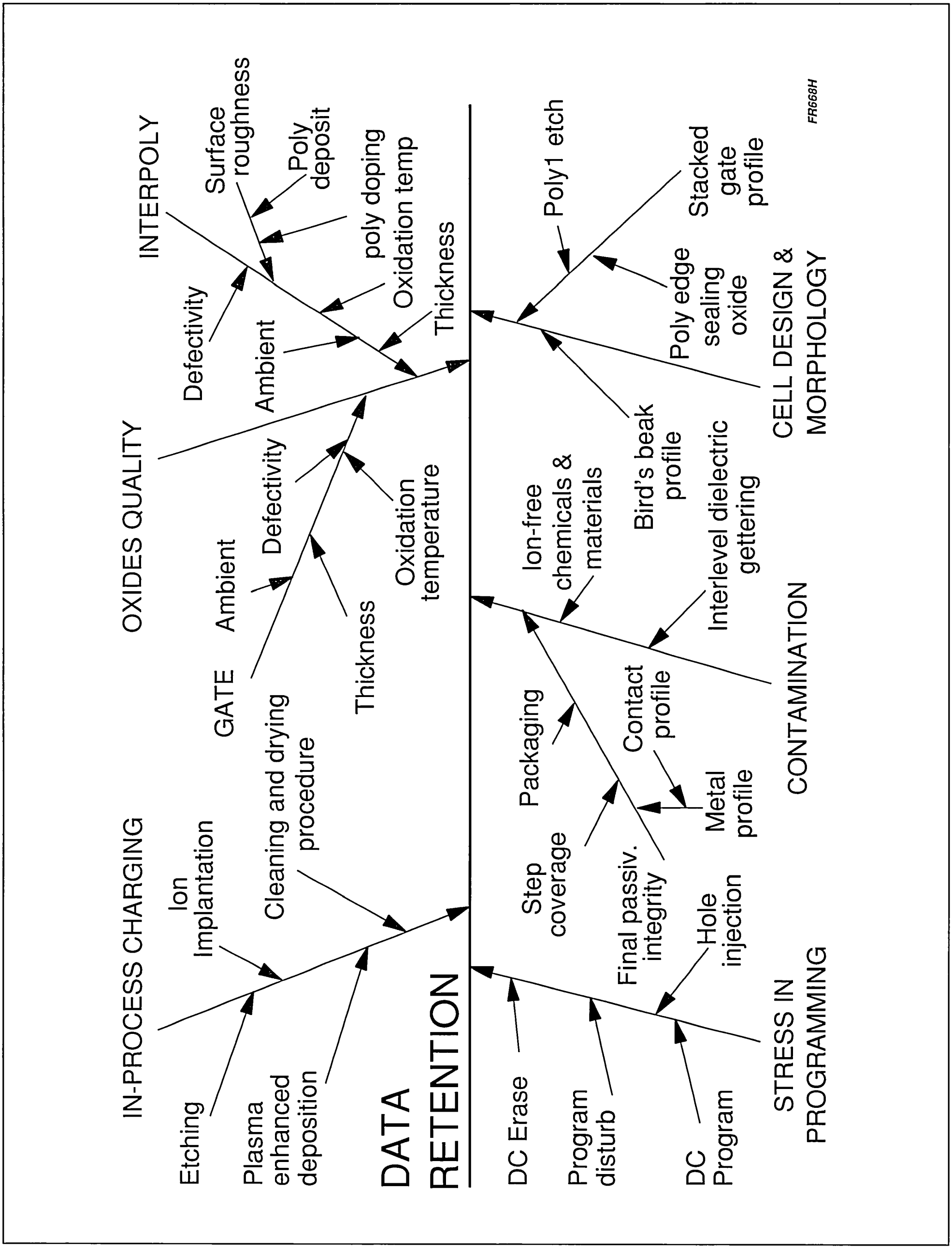

DATA RETENTION
IN-PROCESS CHARGING
Etching
Ion Implantation
Plasma enhanced deposition
Cleaning and drying procedure
OXIDES QUALITY
GATE
Ambient
Defectivity
Thickness
Oxidation temperature
INTERPOLY
Defectivity
Surface roughness
Ambient
Poly deposit
poly doping
Oxidation temp
Thickness
STRESS IN PROGRAMMING
DC Erase
Program disturb
DC Program
Hole injection
CONTAMINATION
Step coverage
Packaging
Final passiv. integrity
Contact profile
Metal profile
Ion-free chemicals & materials
Interlevel dielectric gettering
CELL DESIGN & MORPHOLOGY
Bird's beak profile
Poly1 etch
Poly edge sealing oxide
Stacked gate profile
FR668H

Table 2. EPROM & FLASH MEMORY evolution

Sector	Years					Unit
	1990	1991	1992	1993	1994	
Technology	1.2	0.8	0.6	0.5	0.35	µ
Cell Size	19	9	4	3.2	1.5	μ^2
Memory Density	1M	4M	16M	16M	64M	bit
Die Size	46	87	130	105	200	mm^2
Equivalent 1M Die	46	27	16	11	7	mm^2
FITS	26	14	10	7	5	
AOQL	65	31	10	5	3	ppm

CONCLUSION

EPROM data retention and FLASH MEMORY endurance are the two key reliability factors for these non-volatile memories. Intrinsic retention failure mechanisms make only a small contribution to the failure rate, both from electronic or ionic processes. Floating gate memory retention is most dependant on defect density. The quality of the dielectrics is the key issue: both retention and endurance are features of the same dielectric. FLASH MEMORY endurance is limited by hole trapping and destructive oxide breakdown during program/erase cycling.

A new methodology, building-in reliability, is being implemented to improve reliability by classifying and controlling the variables in the manufacturing process.

Acknowledgement is given to the paper presented by G. CRISENZA, G. GHIDINI and M. TOSI at the ESSREF 91 conference in Bordeaux for the source material for this article.

SGS-THOMSON
MICROELECTRONICS

TA110

TECHNICAL ARTICLE

Trends in Non-Volatile Memories

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The “silicon cycle” showed a dip in the market for memories in 1990 followed by a small recovery in 1991. Forecasts up to 1995 are for a recovery with the total market rising to over 25 B$.

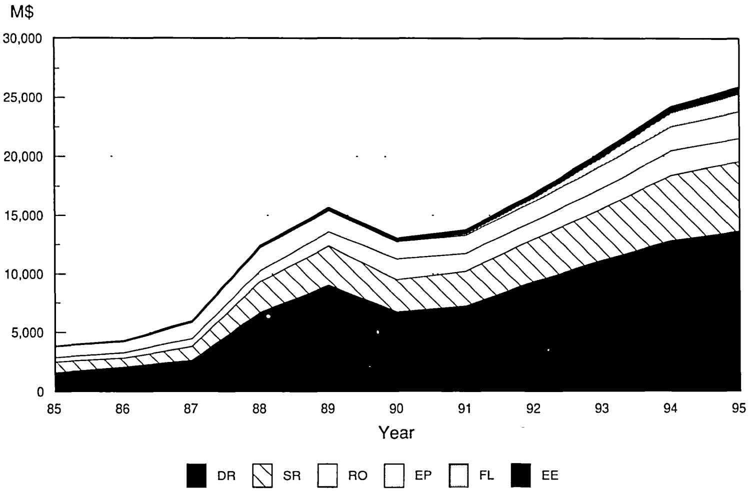
More than half the market is for DRAM. Non-Volatile memories represent 3.5 B$ in 1991 or 26% of the total. The 1991 and 1995 forecasts are shown in Table 1.

The relative share of the market held by ROM and EPROM will be eroded in favour of FLASH MEMORY during the next 4-5 years. But FLASH MEMORY will also grow from new applications and replacement of a part of the DRAM market.

The cost and functionality of the spectrum of Non-Volatile memories is shown in Table 2.

The highest functionality is shown by EEPROM devices, both the smaller (1-16k) serial access types and the medium size (64k-1M) parallel products have Byte Rewrite capability. The FLASH MEMORY, using byte programming like EPROM, have only block or bulk erase. The EPROM has only bulk erase by UV light taking minutes to cancel the content of the whole memory. ROMs are permanently programmed at the mask level.

Figure 1. Memory Market 1985-1995, to M$



Dataquest and INSTAT

FR684

Non-Volatile memory, the Stacked Gate Cell

EPROM and FLASH MEMORY Stacked Gate Cells (SGC) are n-channel transistors with the addition of a floating gate. Both EPROM and FLASH MEMORY are programmed by hot channel electron injection, but they are erased by different mechanisms: the EPROM by a photoelectric effect from exposure to UV light, the FLASH MEMORY by Fowler-Nordheim tunneling through a thin gate oxide.The conventional SGC layout is in the form of a T as shown in Figure 2. A diffused source and drain are covered by two polysilicon layers forming the floating gate and the control gate or word line. The metal bit line runs vertically and makes contact at the drain. The floating gate is isolated from the channel by thin oxide and from the second polysilicon control gate by oxide or Oxide-Nitride-Oxide interpoly dielectric. During the construction the arsenic doped source/drain junctions are self-aligned to the gate. They are symetrical in the EPROM, but a phosphorous doping is added to the source in the FLASH MEMORY cell to create the tunnel region and support the high voltage required. A boron dose is implanted in the channel to prevent punchthrough and to increase programming efficiency by enhancing electron multiplication.

The cell size, in generations up to the 4 Megabit EPROM, is limited in the horizontal direction by the metal bit line interconnect pitch. In the vertical direction the limit is from the source line width, the source line to word line space, the gate length, the gate to contact distance and the contact size. Technology improvements with self aligned source (SAS) are implemented in the 16 Megabit generations to reduce the cell size.

The operation of the SGC can be understood by the use of a simple equivalent circuit which enables the floating gate voltage Vfg to be calculated. The total floating gate capacitance Ct is,

$$Ct = Cpp + Cd + Cs + Cb$$

If Cj is the capacitance of the floating gate to any electrode 'j', the coupling ratio Aj = Cj/Ct, then,

$$Vfg = Ag^*Vcg + Ad^*Vd + As^*Vs + Ab^*Vb + Q/Ct$$

and when the floating gate is loaded with an electron charge Q,

Change in threshold voltage = Q/Cpp

When the cell is programmed by loading an electron charge on the floating gate, the transistor threshold voltage goes up from the virgin value (typically 2-3V) to the programmed value (6-7V). The values of the coupling ratios are found experimentally, and when known can be used to provide an accurate simulation of the SGC MOS transistor.

Table 1. 1991 and 1995 forecast for Non-Volatile memories

Memory Type	1991	%	1995	%
ROM	1311	40	1847	30
EPROM	1543	47	2266	37
FLASH	100	3	1400	23
EEPROM	337	10	586	10
Total	3291	100	6099	100

Table 2. Cost and Functionality

Memory type	Functionality	Cost ($/M Byte)	
		1991	1995
EEPROM	Byte Rewrite Lower Density	1275	300-350
FLASH	Electrical Erase Block or Sector	100	18-25
EPROM	UV Eraseable Or OTP	51	15-20
ROM	Not Reprogrammable	8	2.5-3.5

Figure 2A. T-Shaped Stacked Gate Cell

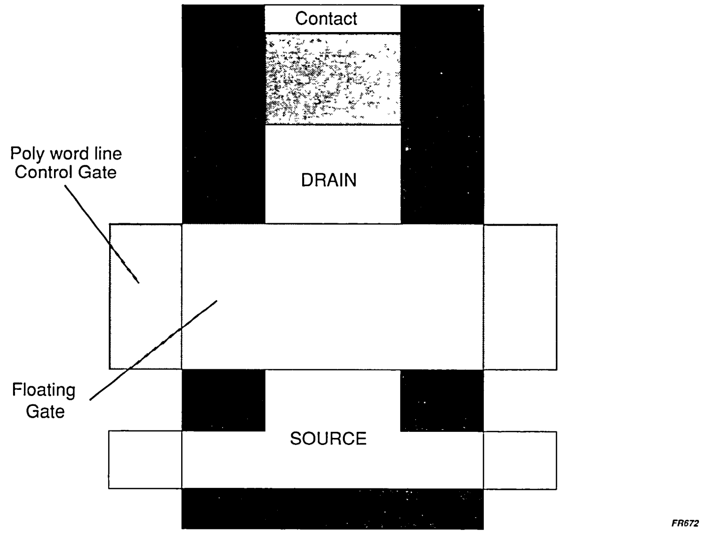

Contact
DRAIN
Poly word line
Control Gate
Floating
Gate
SOURCE
FR672

Figure 2B. Cross section along source/drain

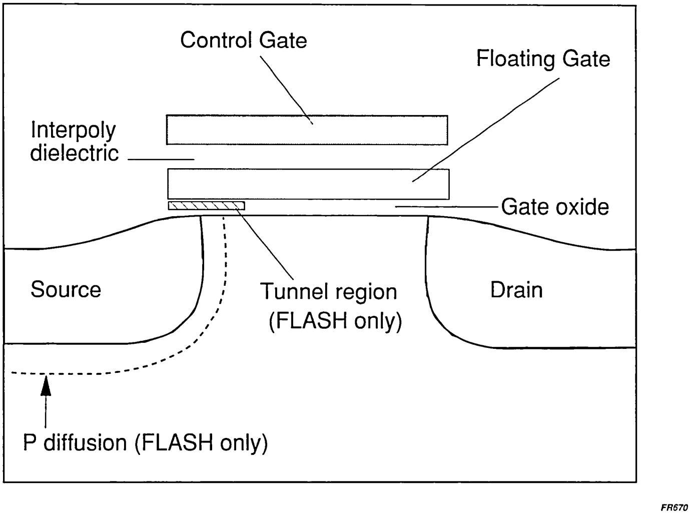

Control Gate
Floating Gate
Interpoly
dielectric
Gate oxide
Source
Tunnel region
(FLASH only)
Drain
P diffusion (FLASH only)
FR670

Figure 2C. Cross section along poly word line

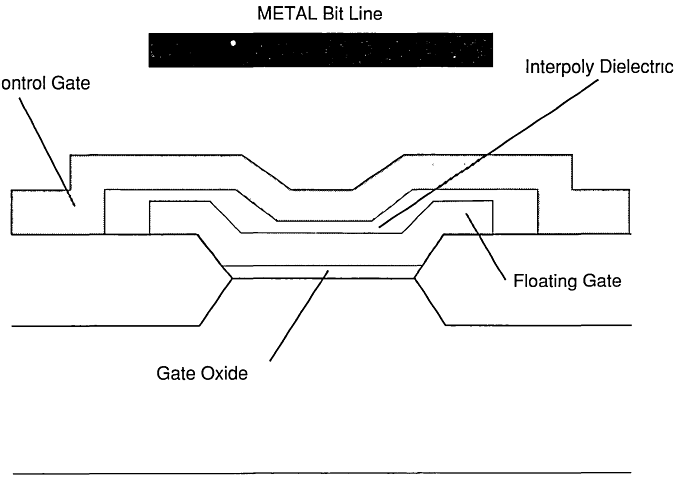
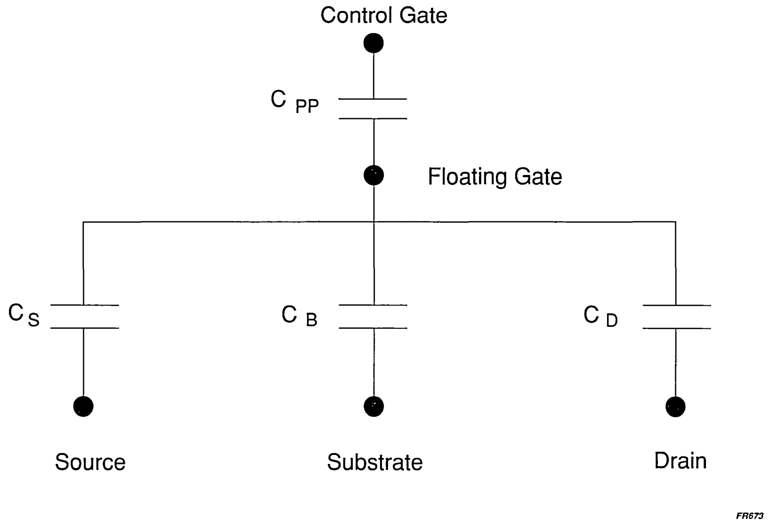

METAL Bit Line
Control Gate
Interpoly Dielectric
Floating Gate
Gate Oxide
FR671

Figure 2D. Electrical equivalent circuit


Control Gate
C_{PP}
Floating Gate
C_S
C_B
C_D
Source
Substrate
Drain
FR673

Programming

Hot channel electron injection, which is discouraged in normal transistors, is enhanced in the cell to improve the gate current Ig, or programming efficiency. Programming curves for an SGC are shown in Figure 3. The cell is programmed by applying positive voltage pulses to the control gate (11V) and the drain (6V). Curves are shown without and with source and drain resistances.

The curve of Figure 4 is derived from Figure 3 and shows the gate current versus the floating gate voltage during programming. Two separate regions are present. In the injection limited region Vfg > Vd the energy distribution of hot electrons is reduced by the low lateral electric field even though the vertical field is suitable for injection. The second region is the electrode limited region Vfg < Vd. Here the hot electron distribution is confined to the lateral field region where the potential barrier is higher. An important point is the knee of the curve where Vfg = Vd. At this point,

$$Vfg = Ag^*Vcg + Ad^*Vd - Ag^*(Vt-Vt0)(t) = Vd$$

where (vt-Vt0)(t) is time dependant and a critical parameter for the cell, 't' can be considered to represent the programming speed of the cell. Variations of the device parameters and applied voltages impact on the coupling ratios of the cell and so on the equation. As programming speed is a key issue for EPROM and FLASH MEMORY all effects depending on the array organisation and layout have to be understood. As can be seen from Figure 3, series resistance in the source and drain can dramatically affect programming.

Erasure

EPROM erasure is made by exposure to UV light. The electrons stored on the floating gate are excited by incident photons and escape from the potential well. Erase time depends on the tranparency of the dielectrics used, but is several minutes.

FLASH MEMORY erasure is made by applying a high positive voltage pulse to the source. This creates a high electric field across the thin gate oxide and electrons tunnel from the floating gate to the source. During erasure the drain is left floating to prevent a large channel current. Some substrate current occurs due to band- to-band tunneling because of the large electric field induced in the silicon surface, this leakage current can limit the erase speed and affect the endurance reliability. It can be avoided by the correct design organisation of the memory. FLASH MEMORY erase time varies from milliseconds to seconds.

Figure 3. Threshold shift against programming time

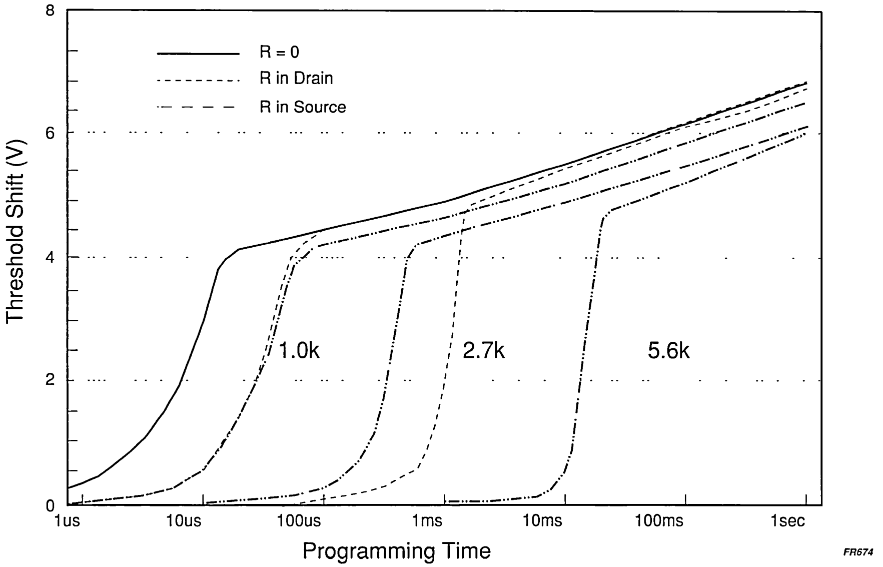


Figure 4. Gate current against floating gate voltage during programming

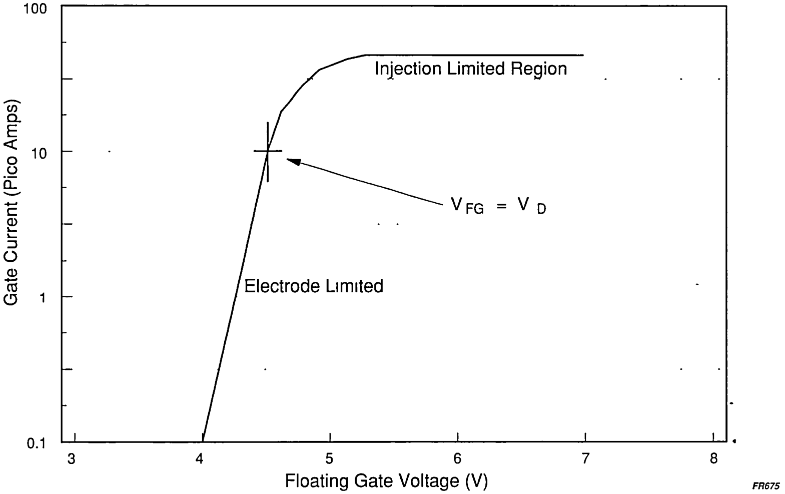
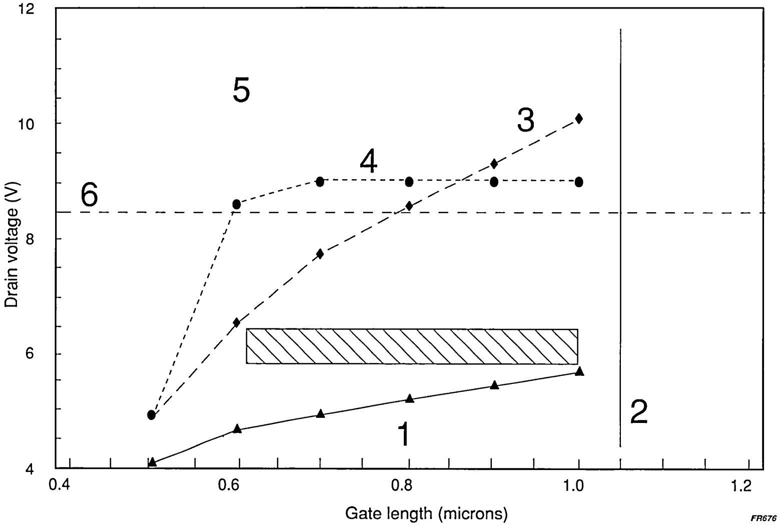


Figure 5. Working area of a 0.8 micron SGC



Cell working area

The good functionality of a cell is based not only on the writing efficiency, but on the robustness to parasitic effects and programming effects such as,

- Drain turn-on
- Snap back
- Soft programming during reading
- Soft erasure during writing

These effects can be clearly seen in a graph of Drain Voltage versus Gate Length as these are the main variables which determine the cell electric fields.

The cell working area is confined by several forbidden areas of active and parasitic effects as shown in Figure 5:

- 1: Programming speed
- 2: Reading current
- 3: Snap-back effect
- 4: Drain turn-on
- 5: Soft Programming
- 6: Soft erasure

Within these constraints a working area for the cell is defined by the box shown. Manufacturing tolerances must hold the cell within the limits of the box. The wider the box by design, the more the manufacturability of the memory.

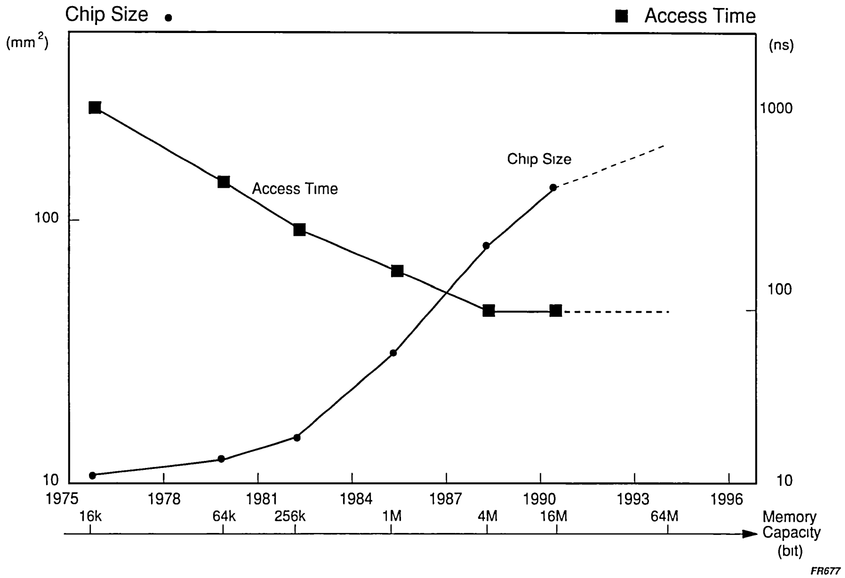
A similar diagram can be drawn for FLASH MEMORY where the disturbance of the memory during write is enhanced due to the thinner oxides used. In the FLASH MEMORY the endurance must also be taken into account, EPROM endurance is not a critical parameter and typically ranges around 100 cycles, but FLASH MEMORY endurance must exceed 100,000 cycles. During this life time the memory parameters should remain with a defined operating area without degradation of the electrical characteristics.

Scaling Down

In semiconductor memory tecnology there is always the constant effort to fit more memory cells on the wafer. EPROM density has quadrupled every three years - see Figure 6.

Through the development of high performance dielectrics and high voltage architectures, the

Figure 6. Evolution of EPROM density, chip size and access time



EPROM has served as a technology driver. The EPROM technologies have been adopted by many other products, like microprocessors with embedded (EPROM, EEPROM) memories on the chip.

To give some idea of what the reduction of chip area means, every three generations the whole EPROM cell size is reduced so that it would fit into the contact area of the original generation. As the process complexity increases, equipment requirements and process control become more severe. Economically however, scaling down is essential and allows redesign in new technologies of all sizes of memories, thus reducing costs and increasing profitability of products that have reached maturity on the market.

Scaling Down rules

Scaling down the transistor sizes, while maintaining the power supply at 5V and the capability handle high programming voltages, places greater stresses on the materials. Figure 7 shows the trend for scaling the gate length through the various generations of EPROM.

A scaling strategy between that of constant field and constant voltage could be adopted. Device dimensions and writing voltage follow a constant field path, while reading voltage follows the constant voltage path. When the programming voltage is properly scaled and oxides fabricated with increased integrity, the reading voltage becomes not so critical. Not scaling the reading voltage increases the reading current available and thus speeds up access time - see Figure 8.

The largest stresses due to electric fields occur in the gate oxides of the row decoder transistors which have to switch the high voltage during writing. In a FLASH MEMORY cell scaling of the gate oxide is limited by direct tunneling, high temperature bake retention and stress induced leakage current increase after repeated program/erase cycles. So a scaling that follows constant electric field across the gate oxide must be adopted.

Maintaining Reliability

Data retention is typically 20 years for a Non-Volatile memory. A programmed cell has only some tens of thousands of electrons on the floating gate. The oxides surrounding the floating gate must guarantee a leakage current of only a few electrons per day. Both electronic and ionic processes contribute to the leakage current.

Figure 7. Gate length versus memory size

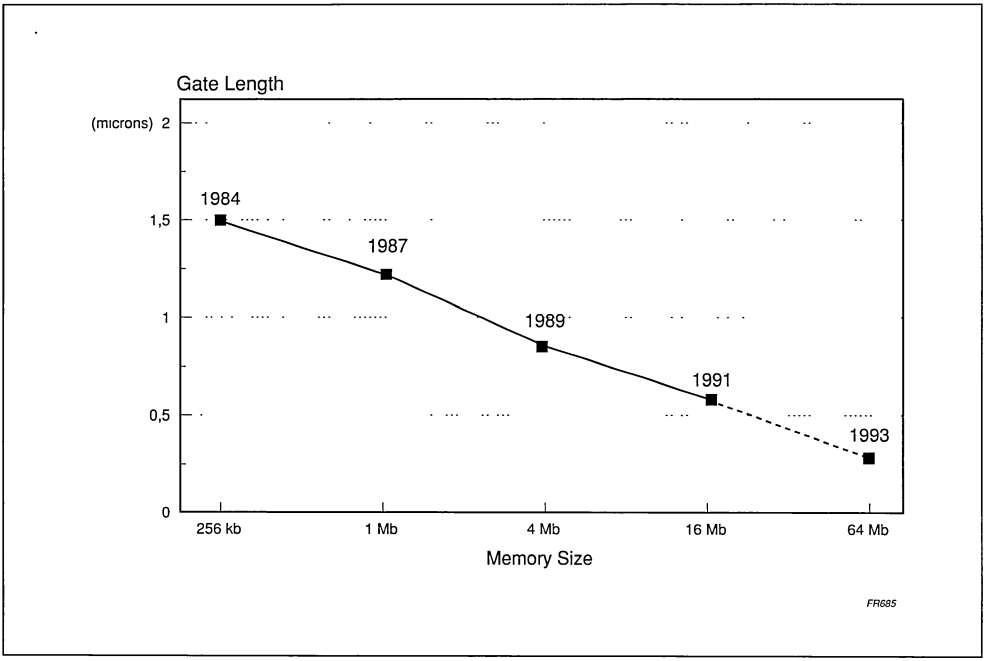
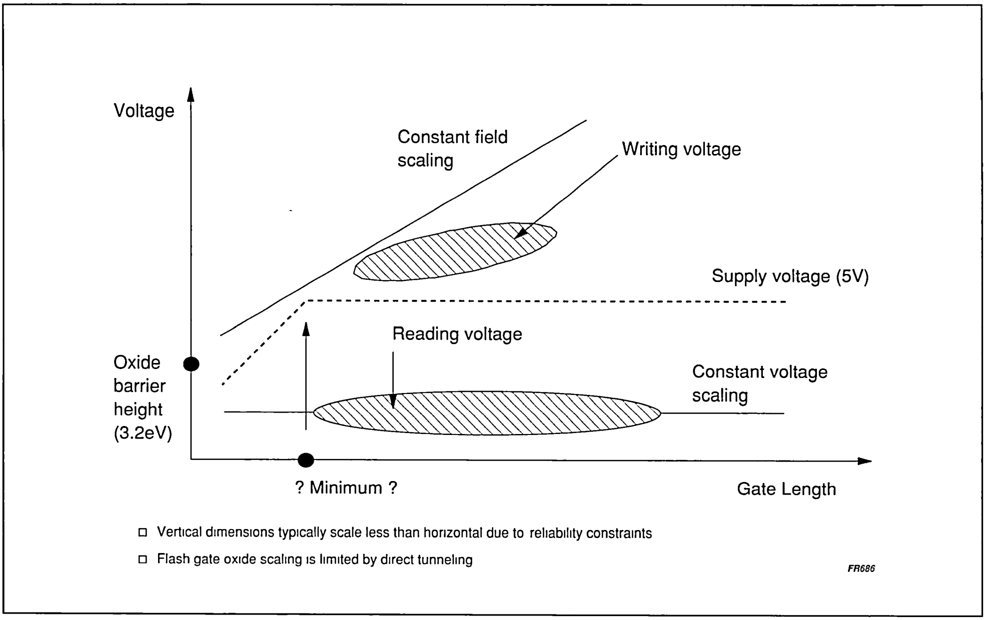


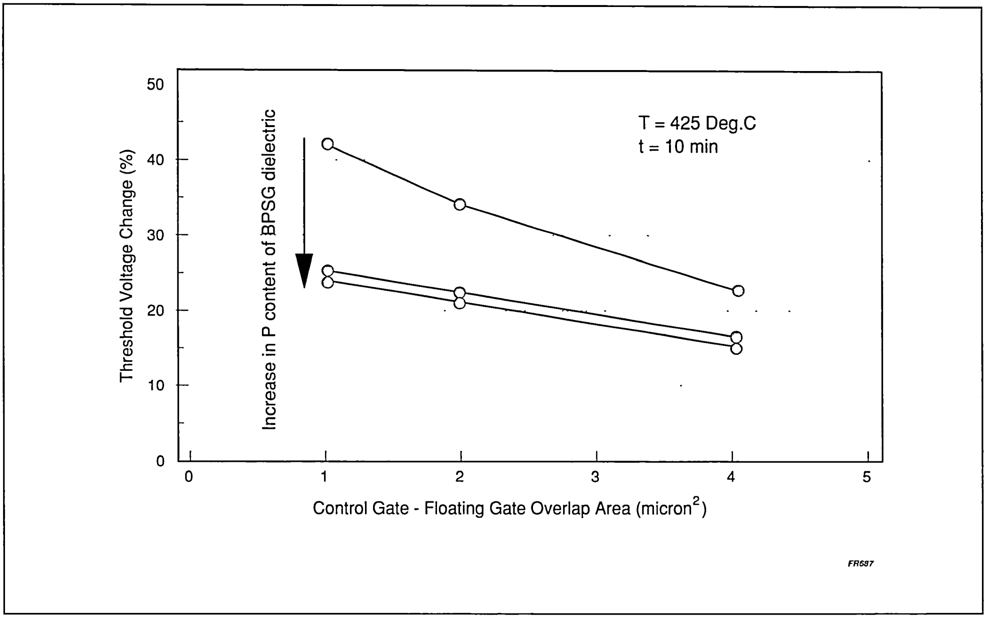
Figure 8. Scaling versus voltage


Voltage
Constant field scaling
Writing voltage
Supply voltage (5V)
Reading voltage
Oxide barrier height (3.2eV)
Constant voltage scaling
? Minimum ?
Gate Length
FR686

☐ Vertical dimensions typically scale less than horizontal due to reliability constraints

☐ Flash gate oxide scaling is limited by direct tunneling

Figure 9. Charge loss dependance on scaling cell size



Electronic processes include the escape of electrons from the floating gate through oxide defects. This mainly affects single bits, randomly scattered thoughout the memory array. The dependance on temperature indicates an activation energy of a few tenths of an eV, and the leakage current is an exponential function of the electric field.

Ionic processes affect the data retention by screening and compensation effects of the stored charge on the floating gate. Charge loss is also associated with alkali metal contamination. Activation energies found are greater than 1eV and a drift diffusion transport mechanism controls the mobile ion current.

Scaling down the cell means that the same change in threshold voltage between a programmed and erased cell is achieved by a smaller stored charge on the floating gate. This makes the memory more sensitive to ion contamination. Figure 9 shows the charge loss as a function of the Control Gate - Floating Gate overlap, with the same interpoly and gate oxides. Charge loss goes up with reducing dimensions and decreasing phosphorous content of the BPSG interlevel dielectric.

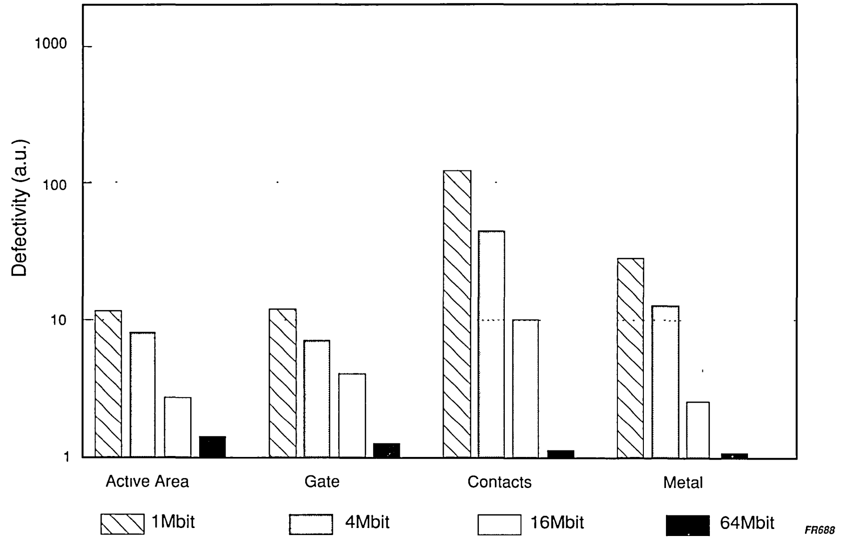
With geometry scaling, the defectivity becomes a dramatic issue. As an example Figure 10 shows the defectivity targets for the main critical layers. To meet these targets the technology has to be constantly tuned and process control tightened.

Reliability failure modes, such as electromigration, hot electrons, etc, must be controlled in the more severe environment of the non-volatile memory: high voltage programming and high temperature (250°C) bake testing for data retention.

Improving Speed

With increasing memory density, the bit line (metal interconnect) and the word line (second polysilicon) parasitic capacitance and resistance affect the speed of the memory. The delay times for array matrix access offset the improvement in the transistor driving capacity and cell read current. To achieve high speeds the memory array can be partitioned to reduce the minimum decoded array and the parasitic capacitance effects. Partitioning has to be paid for in terms of die size and a cost/performance trade off found.

Figure 10. Defectivity targets for main critical layers



Improvements in process can also contribute to improved matrix access time, one of these is the use of silicide to reduce resistance of the polysilicon word lines. Circuit design techniques such as Address Transition Detection, generating an internal clock to gate noise effects, are necessary to avoid memory designs with narrow operating Vcc ranges or even oscillation generated by feedback to address inputs from the high output switching currents - see Figure 11 and Figure 12.

An example of two state-of-the-art memory arrays made with the same technology, but one emphasising speed and the other chip size reduction, are shown in Figure 13.

In the future it is likely that we will see a split in the market demand into high density architectures, with speed limitations, and dedicated high speed designs.

Alternative cells and technologies

As design rules shrink, reliability problems are enhanced and manufacturing latitude is decreased. Many efforts are dedicated to finding new solutions to contain the increase in chips sizes and keep them within manufacturable limits. This can be achieved in two ways: innovative technology and alternative cell architecture.

Figure 11. Memory delays

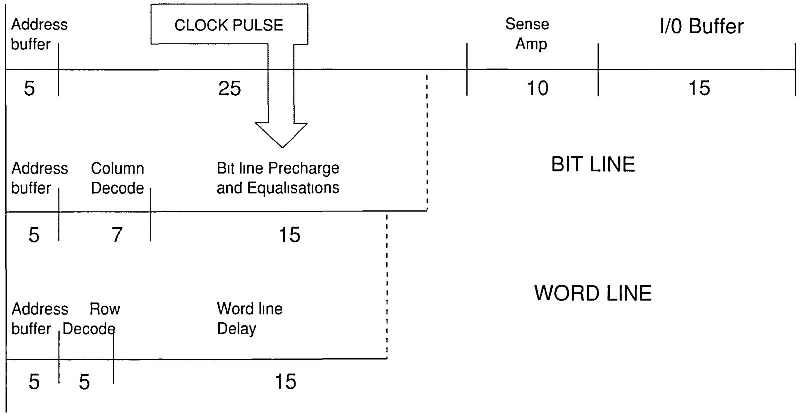
% Contribution	From
40 %	Access time delay of cell matrix
20 %	Time delay from pad → input buffer → address decode
20 %	Time delay of sense amp → output buffer
20 %	External load dependant, specification is 100 pF load

☐ Matrix delay reduced by :

- Silicide on poly word lines - reduced resistance
- Repeater amplifier in the word lines
- Matrix of maximum 512 cells per bit line - reduced capacitance
- Address Transition Detection - precharge/equalised bit lines

FR689

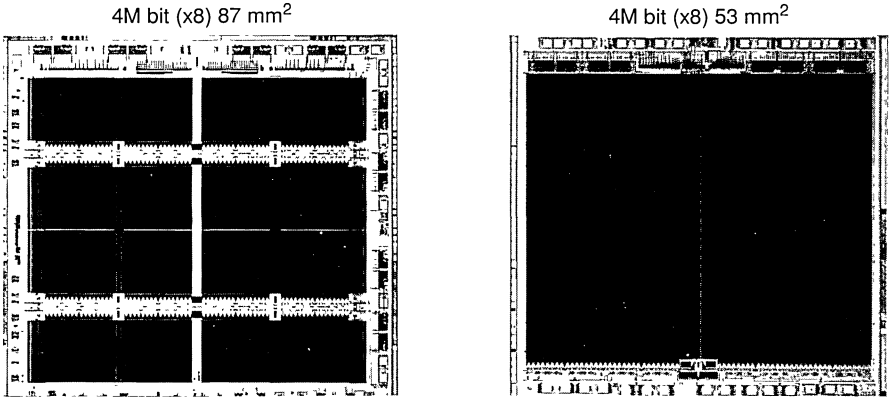
Figure 12. Address transition detection


Address buffer
CLOCK PULSE
Sense Amp
I/O Buffer
5
25
10
15
Address buffer
Column Decode
Bit line Precharge and Equalisations
BIT LINE
5
7
15
Address buffer
Row Decode
Word line Delay
WORD LINE
5
5
15

4 Megabit EPROM typical timing in nanoseconds, t_{acc} = 55ns (no load)

FR690

Figure 13. Two 4 Megabit EPROMs, for high speed and high density


4M bit (x8) 87 mm^2
4M bit (x8) 53 mm^2

Access time 80 ns
8R + 8C redundancy
Pads on 4 sides

Access time 100 ns
4R + 4C redundancy
Pads on 2 sides

SCALING CELL SIZE

Two possible alternatives:

1. use of innovative technologies (double metal, plugs, local interconnections, self alignment, ...)

   advantage: no inpact on device organiastion (conventional)

   drawback: cost and risk of new complex process steps

2. different cell array organiastion (contactless virtual ground approach)

   advantage: less severe technological requirements

   drawback: new circuit solutions, unknown characteristics

Improved Stacked Gate Cell designs have been proposed that self- align the source line, and/or the drain contact to the gate. The use of double metal interconnect is also beginning to appear on EPROM and FLASH MEMORY, allowing a chip size reduction in the peripheral circuits and a decrease of the array parasitic RC delays if it is used for array bit or word lines. The use of refractory materials has been proposed for local interconnect, but the drawbacks of these are the cost and risk of increasing the process complexity. Advantages are that the cell concept remains unchanged and array design organisation is easy, keeping the same logic as previous generations.

One alternative cell organisation in the array is known as "virtual ground". The purpose of this is to save space by eliminating many contacts and alignment tolerances - see Figure 14. The array is known as virtual ground because the source is not fixed and connected to ground.

Some other cell examples are the buried bit line cell, the ALDS cell, the SFOX cell and the FACE FLASH MEMORY cell - see Figure 15.

All these offer the advantage of a small cell size with more relaxed design rules than for a Stacked Gate Cell of the same size. The design modifications introduced however can affect speed performance. Higher resistance and capacitance of diffused bit lines also affect speed, especially on FLASH MEMORY. FLASH MEMORY compatibility is more critical as the same bit line is used alternatively as source and drain.

Concerns About Virtual Ground Architectures

- Design modifications can affect performance, limiting speed.
- Higher resistance and capacitance of diffused bit lines limit the reduction in contact number, and affect speed (particularly on FLASH MEMORY).
- FLASH MEMORY compatibility is more critical, as the same bit line is alternatively used as source and drain.
- Technological saving is questionable, as tight layout rules are required to match decoder pitch with reduced cell size.
- Array reduction obtained by smaller cell size is paritally compensated by larger decoders.
- Programming disturbance to adjacent cells are: careful charge/discharge of array bit lines (circuit solution) and asymetrical cell (technological solution).

The Virtual Ground type of cell design usually results in the cell layout that is square, rather than rectangular. This means it is critical to insert the decoders in the cell pitch or use more aggressive design rules in this sensitive, high voltage part of the circuit.

There is also the problem of programming disturbance to adjacent cells which has to be solved by careful charge and discharge of the bit lines or the use of an asymmetric cell.

Asymmetric cells, such as ALDS (Toshiba 88) and the split gate cell (WSI 88), allow the use of a less complex decoding organisation. But such cells are not FLASH MEMORY compatible without adding extra complexity as the source is not coupled to the floating gate (in the case of the split-gate cell) or is coupled by a region of low doping (in the ALDS cell) which induces a voltage drop during erase.Many alternative cell approaches have been proposed - for example Toshiba three poly layer and NAND cells but few have been transferred into true volume production.

Considering speed, cost-per-bit and FLASH MEMORY compatibility, the Stacked Gate Cell with some innovative processing steps and the use of double metal is likely to remain the best in the future and has been adopted for the SGS-THOMSON 16 Megabit EPROM and FLASH MEMORY developments.

Figure 14. Conventional and virtual ground array

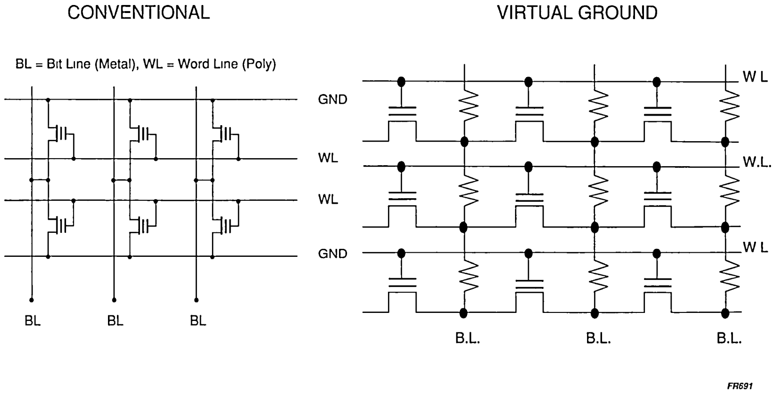
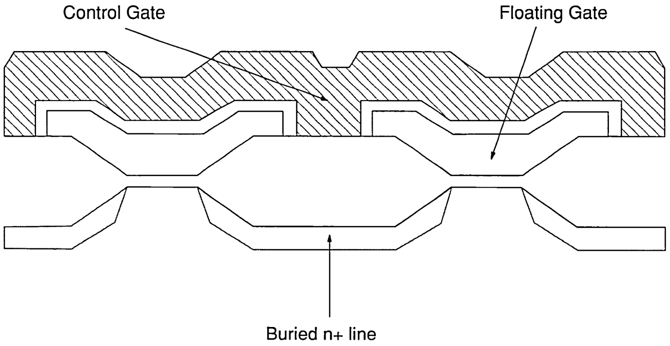

CONVENTIONAL
VIRTUAL GROUND
BL = Bit Line (Metal), WL = Word Line (Poly)
GND
WL
WL
GND
BL
BL
BL
W L
W.L.
W L
B.L.
B.L.
B.L.
FR691

Figure 15. Alternative cells


Control Gate
Floating Gate
Buried n+ line

Buried Bit Line Cell (Texas Instruments)

Other proposed virtual ground cells :

ALDS EPROM cell (Toshiba - IEDM 88)
SFOX EPROM cell (SGS-THOMSON - IEDM 89)
FACE FLASH EEPROM cell (Intel - IEDM 90)

FR692

Future emerging trends

The versatility of FLASH MEMORY which combines electrical erase capability with EPROM density raises the question of whether this device will substitute the EPROM. Direct execution of software stored in a FLASH MEMORY makes the replacement of both DRAM and disk storage possible.

The in-system re-programmability of the FLASH MEMORY shortens the time-to-market: code changes can be made in a short time and board updates done without disassembly. Executable software can be loaded and updated directly. This will stimulate a large growth in a number of applications such as the portable, lap top computers where FLASH MEMORY will save both space and power consumption by replacing both disk and DRAM.

A few years ago it seemed that EEPROM may reduce the EPROM market, but tunnel oxide defectivity, manufacturability of large memories, and larger cell sizes have prevented the EEPROM from taking over from the EPROM in cost-per-bit sensitive applications.

FLASH MEMORY are now in a better position to revolutionise memory usage, as high density is achieveable and cheaper plastic packaging - compared to EPROM - can be used. Balanced against this are the technology and manufacturing problems to be overcome, and the higher cost of the process and testing. Another constraint of the FLASH MEMORY is the requests for power supply reduction to single 5V devices: the electric field needed for tunneling does not scale and the tunnel oxide thickness itself cannot be scaled down because of direct tunneling effects.

The conclusion is that EPROMs will not be entirely superceeded, but that an entirely new market will arise, based on the Stacked Gate Cell to maintain low cost-per-bit and manufacturability, and leading to new computer architectures. Technology development will allow the production of future high density, 16 Megabit and beyond, memories for the future.

FLASH TREND

In-system reprogrammability:

- useful for storage of software updates

Direct execution of software code (XIP):

- replaces disk storage
- substitutes shadow DRAM

Future computers will potentially use:

- an MPU
- a very fast SRAM cache
- a small amount of DRAM for data storage and buffering
- a large amount of fast FLASH MEMORY
- disks, only for backword compatibility

Aknowledgement is given to the material presented by M. MELANOTTE, R. BEZ and G. CRESENZA in Microelectronic Engineering 15 (1991) which formed the basis for this review.

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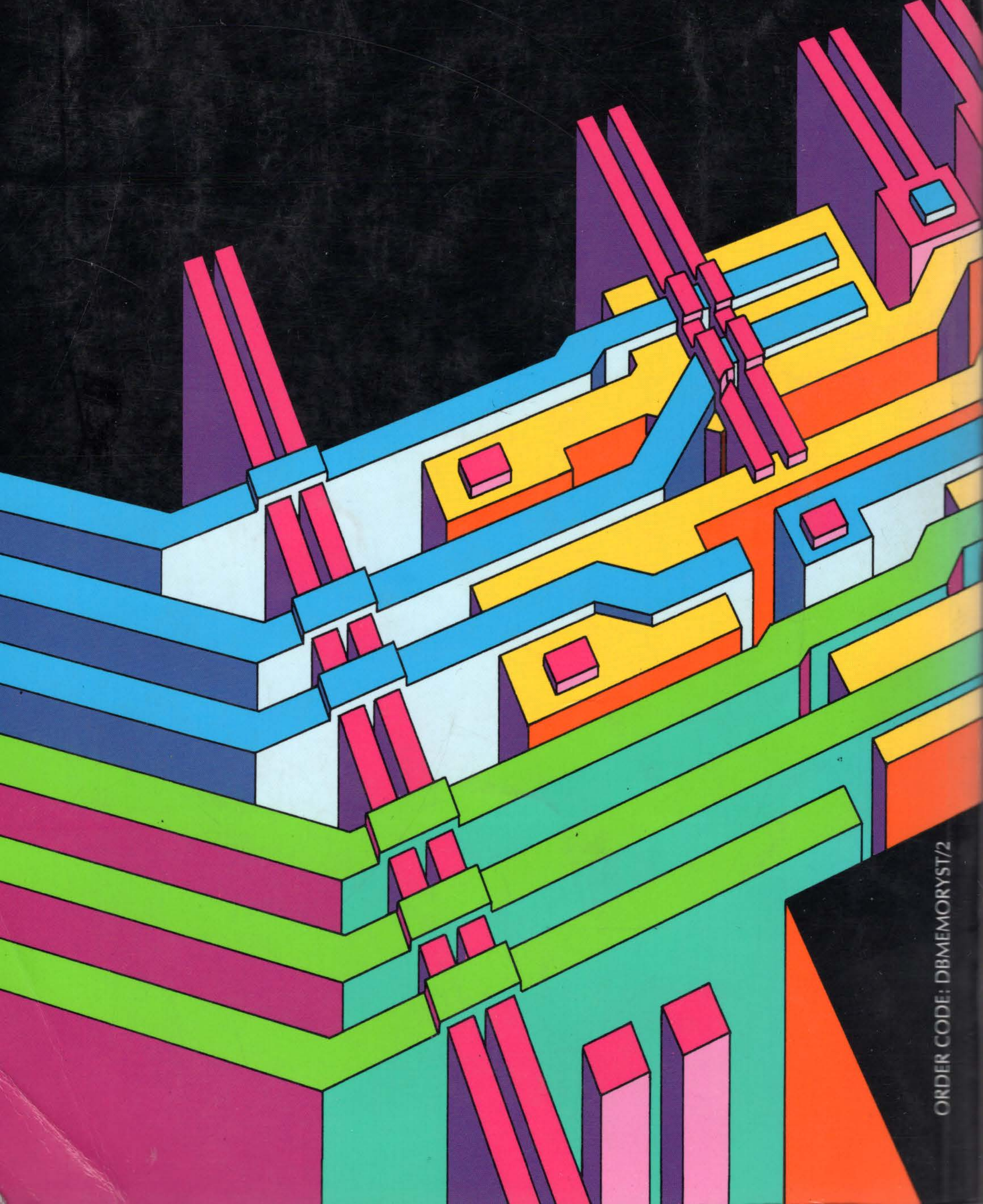

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