TELEPHONE SET ICs

DATABOOK

1st EDITION

SGS-THOMSON MICROELECTRONICS

TELEPHONE SET ICs

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1st EDITION

JULY 1989

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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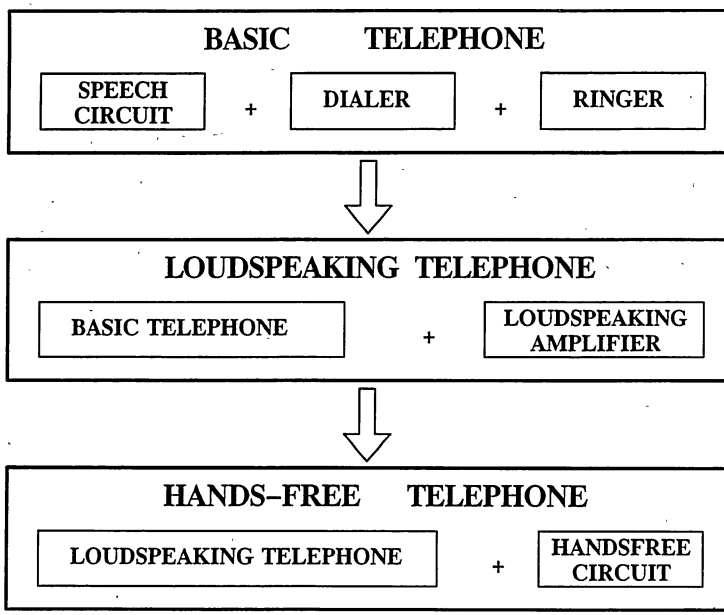
SGS-THOMSON TELEPHONE SET: THE BROADEST PRODUCT RANGE

SGS-THOMSON has been designing and producing dedicated telephone set products since the first voice circuits were introduced in the 1970s. Today, at the beginning of the nineties, the company offers the widest telephone product range in the world and ships more than 50 million dedicated ICs per year, plus some ten million protection devices.

This comprehensive product family covers not just all the telephone functions, but the various national standards, too. A complete kit solution for a basic telephone - speech circuit, dialer and ringer - is available for each country. Moreover, thanks to families of pin-compatible devices it is easy to adapt a design to different standards.

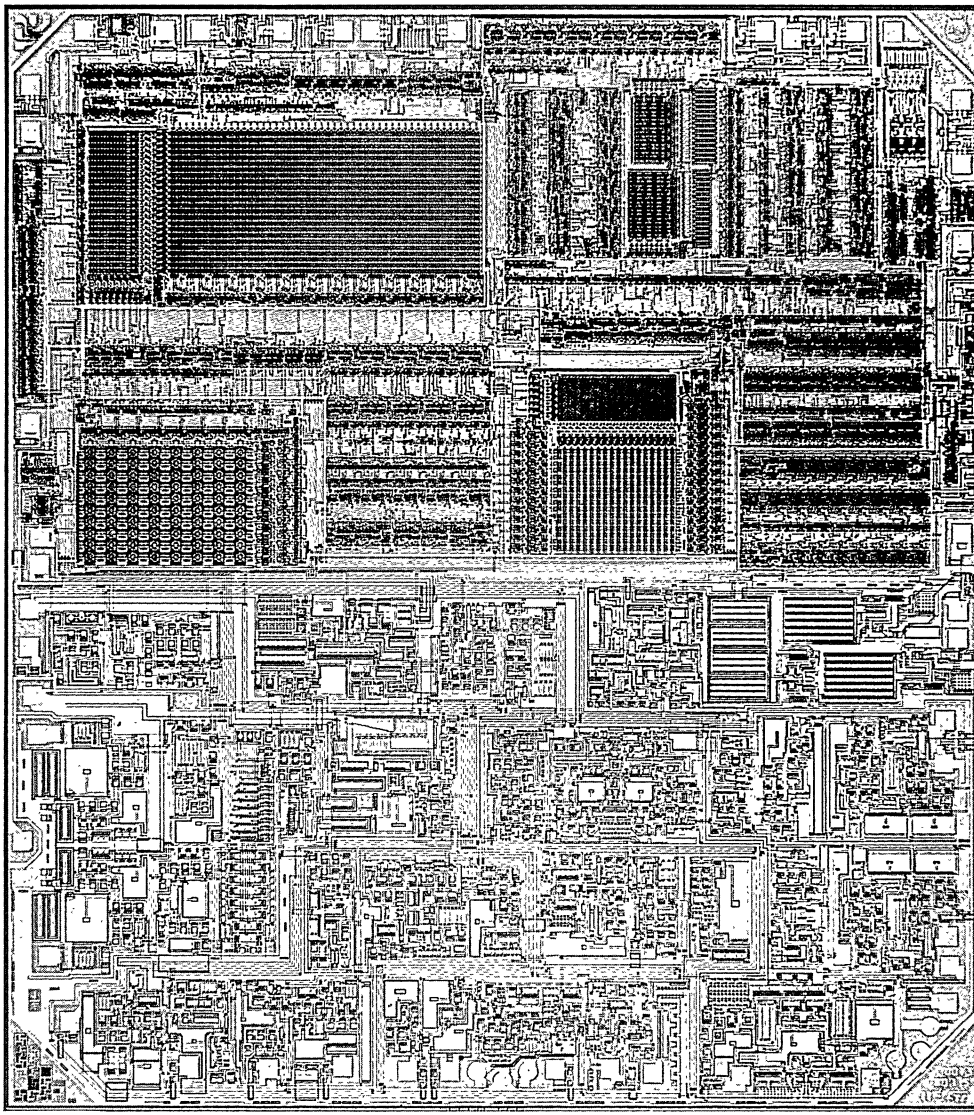
In addition to the basic telephone kits SGS-THOMSON provides circuits designed to allow modular expansion, adding features such as loudspeaking or handsfree capability.

For the early nineties SGS-THOMSON is readying advanced telephone components using advanced mixed technologies. By the time you read this note samples may be available. Stay in touch with SGS-THOMSON to keep up to date with the state of the art.



MODULAR APPROACH. The SGS-THOMSON telephone product range includes a basic, telephone kit for each national standard plus add-on function ICs that turn a basic phone into a feature phone.

INTRODUCTION



ADVANCED TECHNOLOGY. Using an advanced mixed technology SGS-THOMSON has already produced a custom single-chip telephone for a major telecom manufacturer.

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ALPHANUMERICAL INDEX

SELECTION GUIDE

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TONE RINGERS

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SPECIAL FUNCTIONS

CMOS COMPARATORS

Type	Configuration	Main Feature	Single Supply	Operating Voltage Range (V)	Supply Current (Max per Amplifier) (mA)	Input Offset Voltage (Max) (mV)	Responde Time (Typ) (with overdue= 5mV) (ns)	Page
TS372	Dual	Low Power	Yes	3 to 16	0.4	10	600	585
TS374	Quad	Low Power	Yes	3 to 16	0.4	10	600	589

Characteristics specified at V_{CC}= +10V

BIPOLAR OP-AMPs

Type	Configuration	Main Feature	Single Supply	Maximum Supply Voltage (V)	Supply Current (per Amplifier) (mA)	Input Offset Voltage (Max) (mV)	Gain-Bandwidth Product (Typ) (MHz)	Slew Rate (Typ) (V/μs)	Noise Voltage (nV/$\sqrt{Hz}$)	Page
TEB1033	Dual	High Stability	No	±18	0.75	1	2.5	1	6	535
TEB4033	Quad	High Stability	No	±18	0.75	1	2.5	1	6	545
LS204	Dual	High Stability	Yes	±18	0.6	2.5	2.5	1	8	513
LS404	Quad	High Stability	Yes	±18	0.5	2.5	2.5	1	8	523

Characteristics specified at V_{CC}= ±15V

CMOS OP-AMPS

Type	Configuration	Main Feature	Single Supply	Operating Voltage Range (V)	Supply Current (Max per Amplifier) (mA)	Input Offset Voltage (Max) (mV)	Gain-Bandwidth Product (Typ) (MHz)	Slew Rate (Typ) (ns)	Page
TS271	Single	Programmable	Yes	3 to 16	0.015 to 1.5	10	0.1 to 2.5	0.01 to 45	555
TS271A	Single	Programmable	Yes	3 to 16	0.015 to 1.5	5	0.1 to 2.5	0.01 to 45	555
TS271B	Single	Programmable	Yes	3 to 16	0.015 to 1.5	2	0.1 to 2.5	0.04 to 45	555
TS27L2	Dual	Very Low Power	Yes	3 to 16	0.015	10	0.1	1.04	565
TS27L2A	Dual	Very Low Power	Yes	3 to 16	0.015	5	0.1	1.04	565
TS27L2B	Dual	Very Low Power	Yes	3 to 16	0.015	2	0.1	1.04	565
TS27M2	Dual	Low Power	Yes	3 to 16	0.2	10	1	0.5	565
TS27M2A	Dual	Low Power	Yes	3 to 16	0.2	5	1	0.5	565
TS27M2B	Dual	Low Power	Yes	3 to 16	0.2	2	1	0.5	565
TS272	Dual	High Speed	Yes	3 to 16	1.5	10	3.5	5.5	565
TS272A	Dual	High Speed	Yes	3 to 16	1.5	5	3.5	5.5	565
TS272B	Dual	High Speed	Yes	3 to 16	1.5	2	3.5	5.5	565
TS27L4	Quad	Very Low Power	Yes	3 to 16	0.015	10	0.1	0.04	575
TS27L4A	Quad	Very Low Power	Yes	3 to 16	0.015	5	0.1	0.04	575
TS27L4B	Quad	Very Low Power	Yes	3 to 16	0.015	2	0.1	0.04	575
TS27M4	Quad	Low Power	Yes	3 to 16	0.2	10	1	0.6	575
TS27M4A	Quad	Low Power	Yes	3 to 16	0.2	5	1	0.6	575
TS27M4B	Quad	Low Power	Yes	3 to 16	0.2	2	1	0.6	575
TS274	Quad	High Speed	Yes	3 to 16	1.5	10	3.5	5.5	575
TS274A	Quad	High Speed	Yes	3 to 16	1.5	5	3.5	5.5	575
TS274B	Quad	High Speed	Yes	3 to 16	1.5	2	3.5	5.5	575

Characteristics specified at V_{CC} = +10V

TRANSIL PROTECTIONS

P_P (W)	V_{RM} (V)	Types		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.8 to 376	BZW04../BZW04P..	BZW04..B/BZW04P..B	F126	595
600/1 ms	5.8 to 376	P6KE.. P,A	P6KE..CP, CA	CB-417	601
700/1 ms	10 to 110	P7T...	P7T...B	CB-417	607
1500/1 ms	5.8 to 376	1.5KE...P,A	1.5KE...CP,CA	CB-429	613
5000/1 ms	10 to 180	BZW50...	BZW50...B	AG	619

TRISIL PROTECTIONS

I_{PP} (A)	V_{BR} (V)	Types	Case	Page
MONO FUNCTION				
100/8-20 us	58 to 270	TPA series	F126	637
150/8-20 us	58 to 270	TPB series	CB-429	641
500/8-20 us	17 to 120	LS5018B/LS5060B/LS5120B,B1	MINIDIP	645
TRIGGERED FUNCTION				
250/8-20 us	255	L3100B1	MINIDIP	649

SURFACE MOUNT TRANSIL PROTECTIONS

P_P (W)	V_{RM} (V)	Types		Case	Page
		Unidirectional	Bidirectional		
600/1 ms	5.5 to 188	SM6T...,A	—	CB-472	625
	5.5 to 171	—	SM6T...C,A	CB-472	
1500/1 ms	5.5 to 188	SM15T..., A	—	CB-473	631
	5.5 to 171	—	SM15T...C,A	CB-473	

DIALER CIRCUITS

SGS-THOMSON MICROELECTRONICS

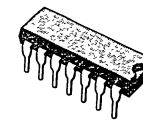
EFG7189
EFG71891

DTMF GENERATOR FOR BINARY CODED HEXADECIMAL DATA

- GENERATES 16 STANDARD DTMF TONE PAIRS
- USES LOW COST 3.579 MHz CRYSTAL
- DIRECT MICROPROCESSOR INTERFACE
- ACCEPTS 4 BIT DATA IN SERIAL OR PARALLEL FORMAT
- DATA IS STORED DURING TRANSMISSION PERIOD
- LOW HARMONIC DISTORTION
- HIGH GROUP PRE EMPHASIS
- LOW POWER CONSUMPTION IN STANDBY MODE
- PULL-UP TO V^+ ON ALL LOGIC INPUTS

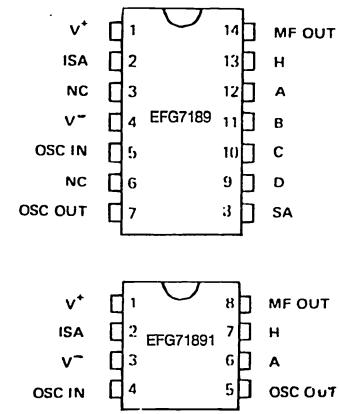
MINIDIP

DIP14



ORDER CODES : EFG71891PD (Minidip)
EFG7189PD (DIP14)

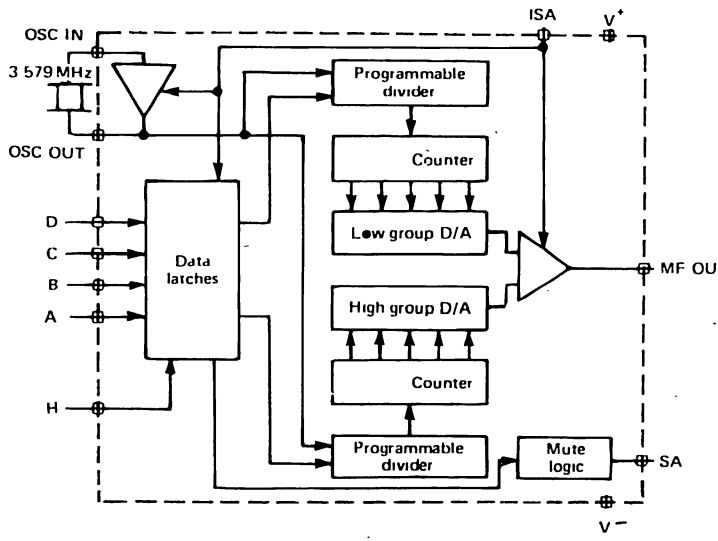
PIN CONNECTIONS (top view)



DESCRIPTION

This CMOS circuit is designed specifically to provide, with a minimum number of external components, a low cost DTMF dialer for microprocessor controlled telephone sets operating in accordance with existing standards. The 4 bits identifying the frequency pair to be generated may be supplied via either 5 connections between the EFG7189 and the microprocessor in parallel format or in serial format through 3 connections linking the EFG71891 to the microprocessor. This feature eliminates the necessity to simulate keyboard type inputs normally required by standard DTMF generators. Input data is stored on trailing edge of ISA signal. The tone pair selected by this code is generated while ISA remains low. With ISA high, the oscillator is inhibited and the device is in standby mode. SA pin is connected to V^- while device is outputting any tone pair.

BLOCK DIAGRAM



PIN DESCRIPTION

N°	Name	Function	Description
1 4	V^+ V^-	Supply Voltage Supply Voltage	Positive Supply 0 V
11 10 9	B C D	Logic Input Logic Input Logic Input	Parallel input for hexadecimal code allowing the selection of 2 frequencies constituting the DTMF signal (see attached table).
12	A	Logic Input	Serial or Parallel Input for Hexadecimal Code
13	H	Serial Input Clock	Clock Input for Hexadecimal Code Serial Input Register on Pin A Furthermore, it allows for the selection of the serial or parallel operating mode of this code. When ISA input goes low, the validated code is : • the parallel input code if input H is high. • the serial input code if input H is low.
2	ISA	Logic Input	This pin allows for the inhibition of the analog output MF OUT : • when ISA is high, output MF OUT is idle and connected to V^-. • when ISA is low, the hexadecimal code is validated and MF OUT output is activated.
8	SA	Logic Output	This pin indicates the state of the analog output : • if ISA is low, SA is a low impedance output at V^-. • if ISA is high, SA is a high impedance output.
14	MF OUT	Analog Output	This pin is the DTMF signal output.
5	OSC IN	Oscillator Input	This pin corresponds to the input of the inverter of the oscillator. The nominal frequency of the oscillator is 3.579 MHz.
7	OSC OUT	Oscillator Output	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	– 0.3 to + 5.5	V
V_{in}	Digital Input Range	– 0.3 to V^+ + 0.3	V
T_{stg}	Storage Temperature Range	– 55 to + 125	°C

ELECTRICAL OPERATING CHARACTERISTICS

All voltages referenced to V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	3	–	5.25	V
T_{oper}	Operating Temperature Range	– 25	–	70	°C
f_c	Crystal Frequency	–	3.579545	–	MHz

DC ELECTRICAL CHARACTERISTICS

T_{amb} = – 25 °C to 70 °C, V^+ = – 3 to 5.25 V, f_c = 3.579 MHz (all voltages are referenced to V^-)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{DD}	Operating Current in Transmission Mode (V^+ = 4 V, output not loaded)	–	0.6	1	mA
ISB	Standby Current (ISA, H, A, B, C, D open circuit or connected to V^+)	–	–	10	µA
V_{IL}	Input Low Voltage (ISA, H, A, B, C, D)	0	–	0.3 V^+	V
V_{IH}	Input High Voltage (ISA, H, A, B, C, D)	0.7 V^+	–	V^+	V
R_T	Pull up Resistor on Logic Inputs ISA, H, A, B, C, D	100	–	–	kΩ
I_{OLSA}	SA Output Current (V_{OLSA} = 0.5 V)	500	–	–	µA
I_{FSA}	SA Leakage Current, Open Current (V_{OHSA} = 5 V)	–	–	2	µA

A.C. ELECTRICAL CHARACTERISTICS

T_{amb} = – 25 °C to 70 °C, V^+ – 3 V to 5.25 V, f_c = 3.579 MHz

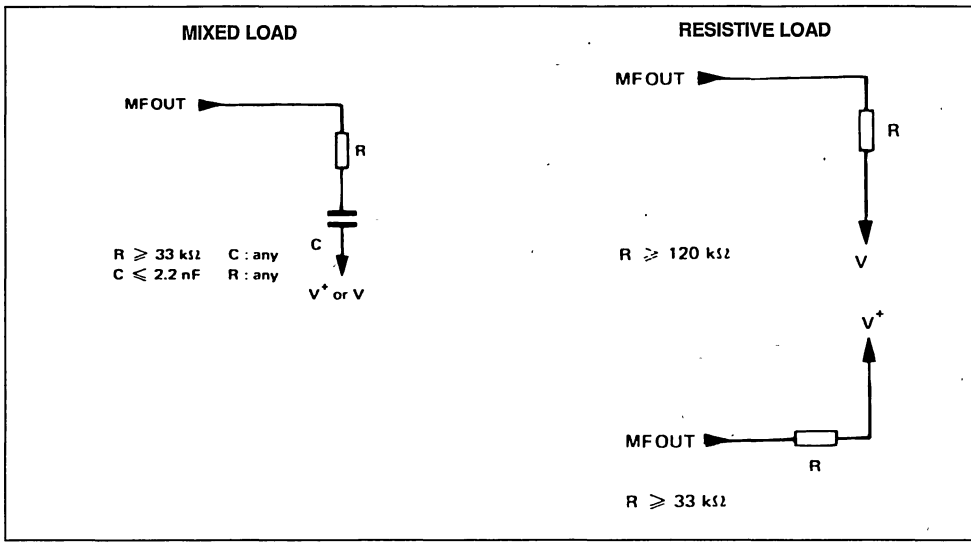
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_r t_f	Rise/Fall Time on Input Signals	–	–	50	ns
$TISA_{ON}$	Transmission Delay	–	–	5	ms
$TISA_{OFF}$	Blocking Delay	–	–	5	ms
T_H	Clock Period	10	–	–	µs
T_{HH}	High Level Clock Width	5	–	–	µs
T_{HL}	Low Level Clock Width	5	–	–	µs
T_{PH}	Set-up Time of A Related to Clock	1	–	–	µs
T_{MH}	Hold Time of A Related to Clock	7	–	–	µs
T_{PISA}	Set-up Time of the Code or Clock Related to ISA	1	–	–	µs
T_{MISA}	Hold Time of Code Related to ISA	2	–	–	µs

TRANSMISSION CHARACTERISTICS $T_{amb} = -25$ °C to 70 °C, V^+ 3 V to 5.25 V, $f_c = 3.579$

Symbol	Parameter	Min.	Typ.	Max.	Unit
DFH DFB	High and Low Frequency Precision	–	–	1	%
AFB	Low Frequency Transmission Level ($V^+ = 4$ V) - Note 1	– 8	– 7	– 6	dBm
GBH	High Band Pre-emphasis	2.3	2.7	3.1	dB
D	Output Distortion	–	–	– 20	dB

Note : 1. 0 dBm = 0.775 V_{rms}
These specifications are related to the following loads.

Figure 1.



FUNCTIONAL DESCRIPTION

With ISA input at logic level "1", the device is in low power mode. The oscillator is inhibited and analog output MF OUT is at ground level. DTMF input data is detected on trailing edge of ISA. This transition enables both the oscillator and the analog output then the data is stored and corresponding DTMF pair is generated during the low state interval of the ISA signal. Any modification to H, A, B, C and D signals during this period will not have any further effect on DTMF pair generated.

The device accepts input data in two different formats :

- Parallel format : this requires 4 connections (A, B, C, D) between the microprocessor and the circuit.
- Serial format : in this case data is supplied to the circuit by the microprocessor via 2 connections A and H (see typical application diagram).

Pre-emphasis is applied to high group tone and both tones of DTMF pair are supplied through analog output pin.

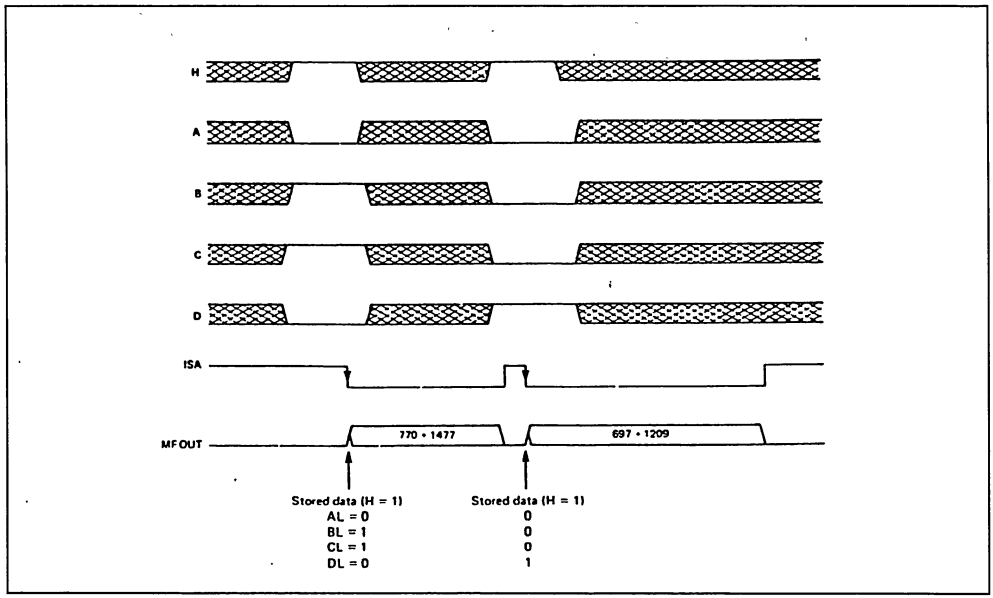
DATA ACQUISITION LOGIC

This section includes : A 4-bit shift register, an 8-line to 4-line multiplexer and a 4-bit storage register.

- The 4-bit shift register has its input connected to pin A and is enabled by the signal applied to pin H. Its outputs are AS, BS, CS and DS signals.
- The multiplexer is enabled by signal H and operates according to the following law : AI = H.AP + $\overline{H}$.AS.
- The 4-bit storage register operates on trailing edge of ISA signal. AI, BI, CI, DI and AL, BL, CL, DL are its inputs and outputs respectively.

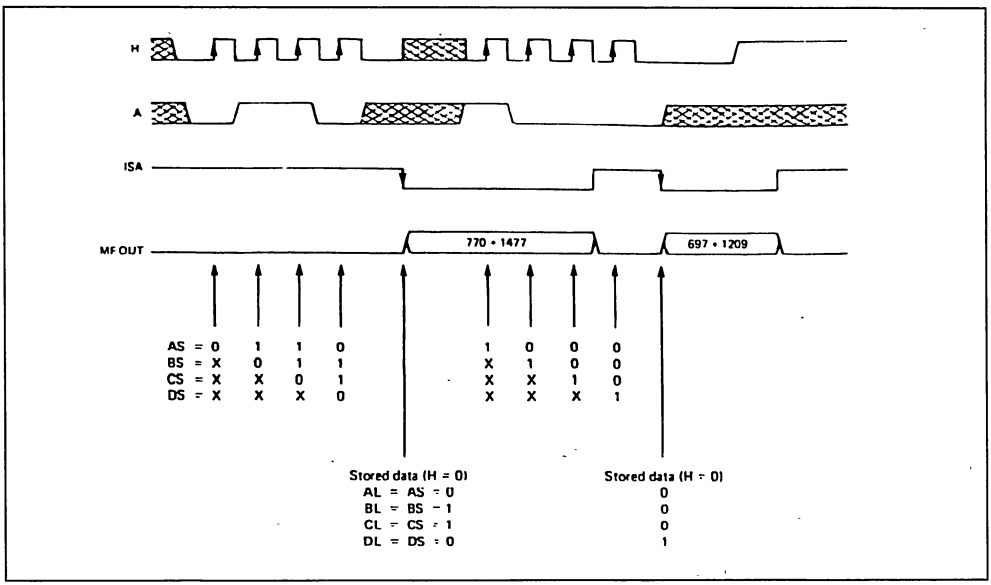
During the low state period of ISA input, AL, BL, CL and DL signals determine the DTMF pair to be generated.

Figure 2 : Example of Parallel Operating Mode.



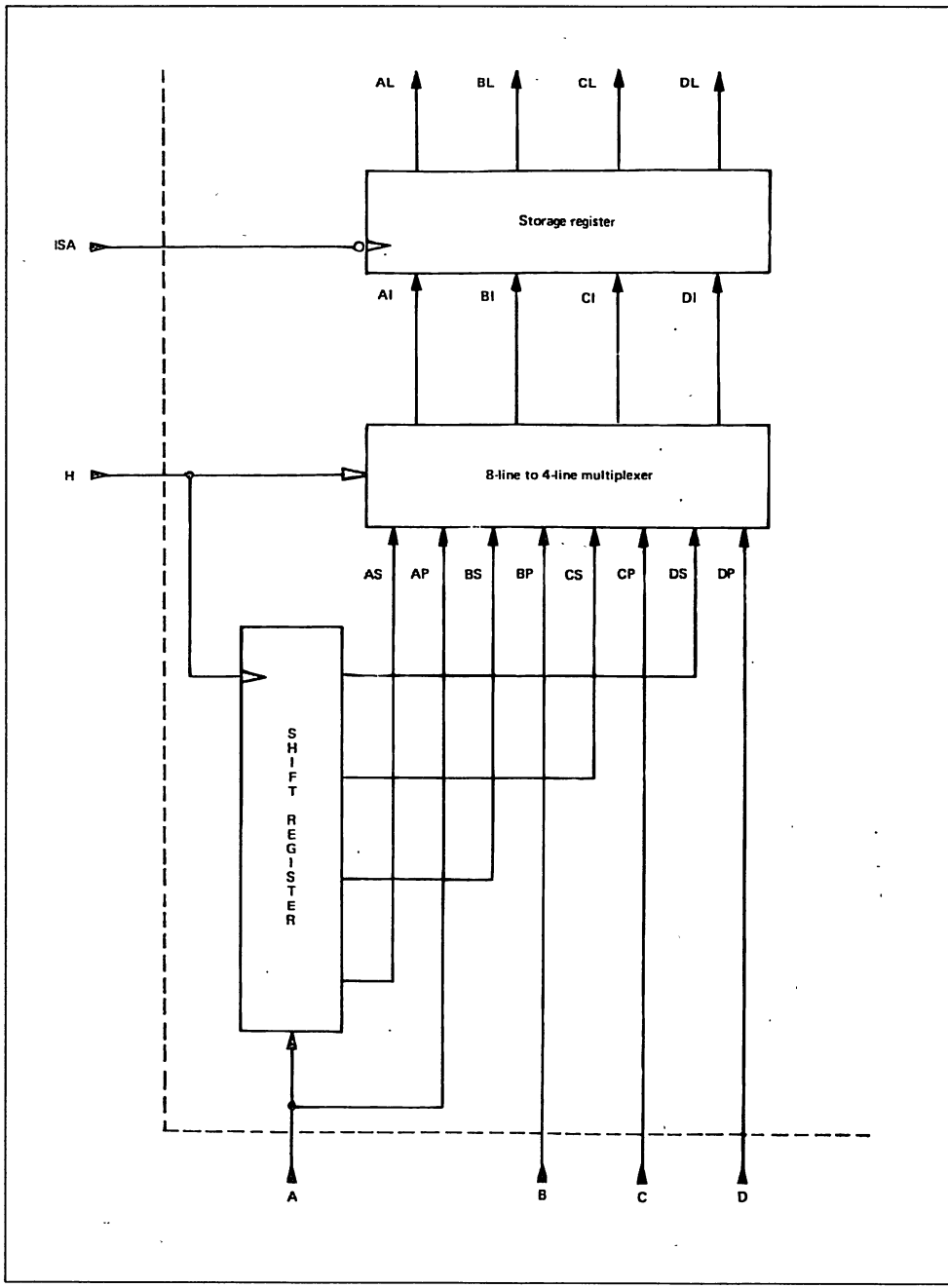
Note : If the circuit operates permanently in parallel mode, then the H input may be left floating (internally pulled-up to V*) or tied to logic 1. With ISA at logic 0, H,A,B,C, and D inputs cannot modify the generated DTMF pair.

Figure 3 : Example of Serial-Operating Mode.



Notes : 1. With ISA at logic 0, H, A, B, C and D signals cannot modify the generated DTMF pair. As a result, in serial operating mode, it is possible to enter AS, BS, CS and DS data while another DTMF pair is being generated.
2. First data to be entered is DS.

Figure 4 : Data Acquisition Logic.



TIMING DIAGRAM

Figure 5 : Rise/Fall Time on Input Signals.

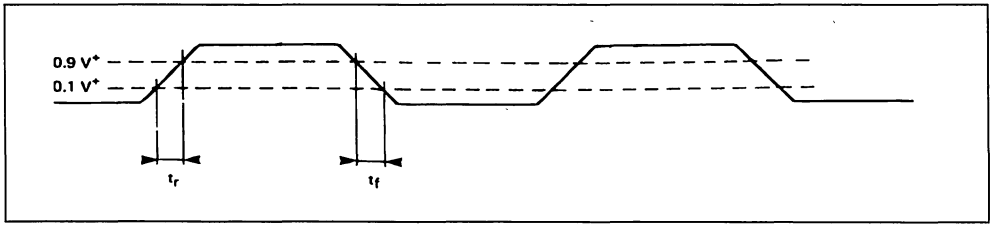


Figure 6 : Parallel Operating Mode (H = "1").

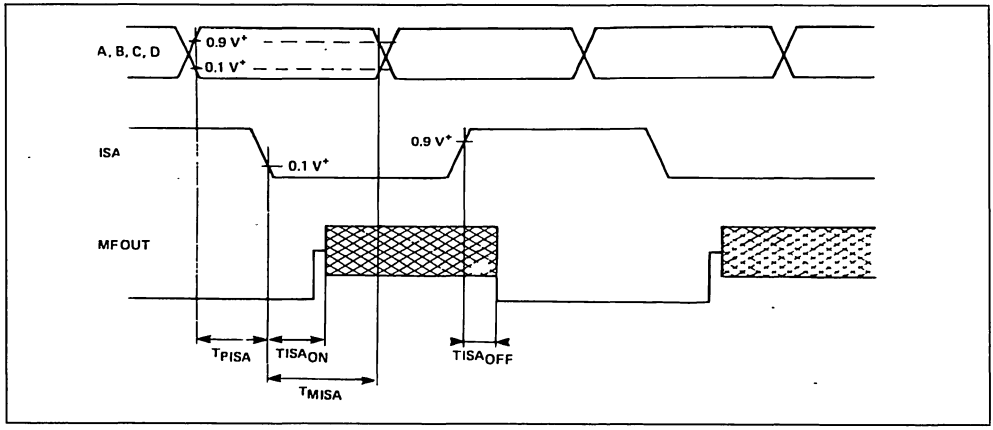


Figure 7 : Serial Operating Mode.

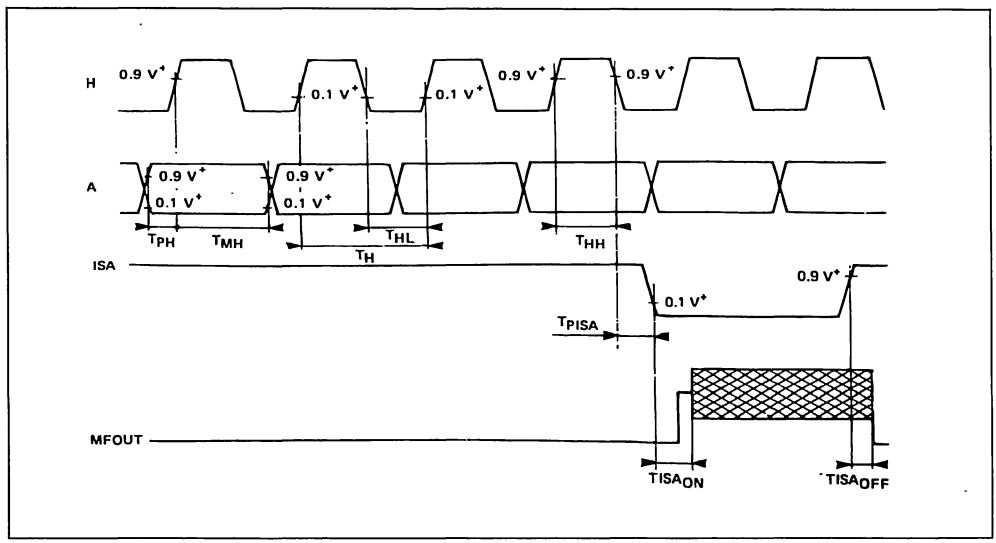


Table 1

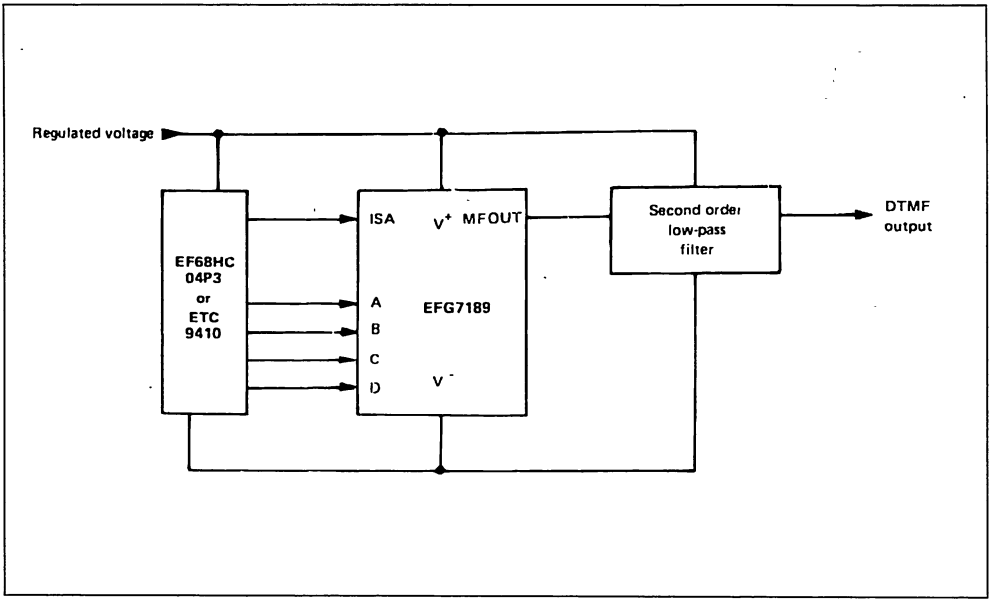
	DTMF Specification (Hz)	Frequencies Derived from a 3.579 MHz Quartz (Hz)	Division Rank	% Deviation from Standard
f1	697	701.3	5104	0.62
f2	770	771.4	4640	0.19
f3	852	857.2	4176	0.61
f4	941	935.1	3828	– 0.63
f5	1209	1215.9	2944	0.57
f6	1336	1331.7	2688	– 0.32
f7	1477	1471.9	2432	– 0.35
f8	1633	1645	2176	0.74

Table 2

Keyboard Code	Hexadecimal Code				ISA	Generated Frequencies	
	A	B	C	D		f(Hz)	f(Hz)
X	X	X	X	X	1		
1	0	0	0	1	⌟	697	1209
2	0	0	1	0	⌟	697	1336
3	0	0	1	1	⌟	697	1477
4	0	1	0	0	⌟	770	1209
5	0	1	1	1	⌟	770	1336
6	0	1	1	0	⌟	770	1477
7	0	1	0	1	⌟	852	1209
8	1	0	1	0	⌟	852	1336
9	1	0	1	1	⌟	852	1477
0	1	0	0	0	⌟	941	1336
•	1	0	1	1	⌟	941	1209
#	1	1	1	0	⌟	941	1477
A	1	1	0	1	⌟	697	1633
B	1	1	1	0	⌟	770	1633
C	1	1	1	1	⌟	852	1633
D	0	0	0	0	⌟	941	1633

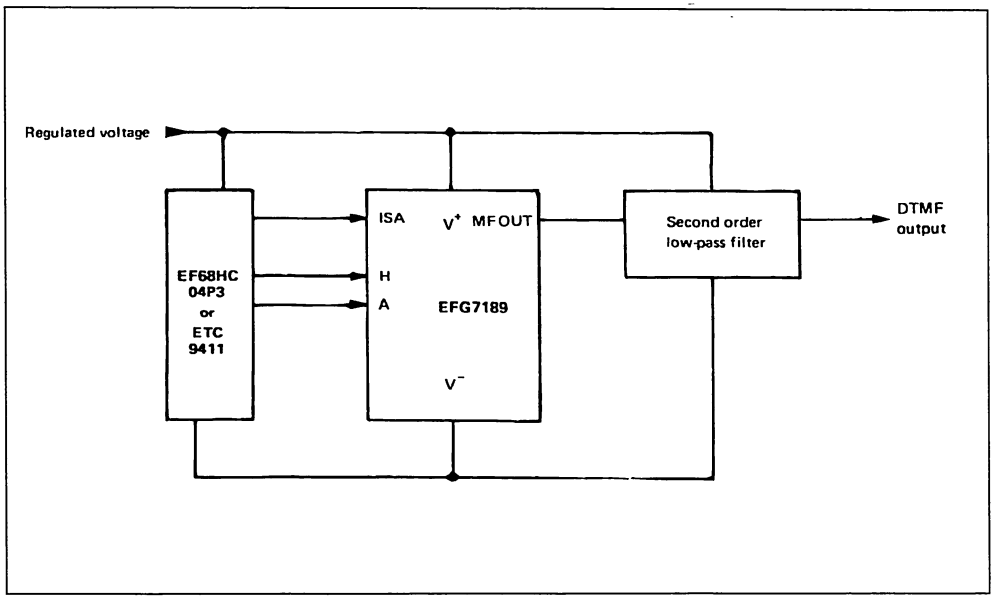
TYPICAL APPLICATION (european standards)

Figure 8 : Parallel Connection.



Note : H may be left open or connected to logic 1.

Figure 9 : Serial Connection.



Note : B, C and D may be left floating or connected to logic 1.

SECOND ORDER LOW-PASS FILTERS

Figure 10 : With Transistor (gain = 1).

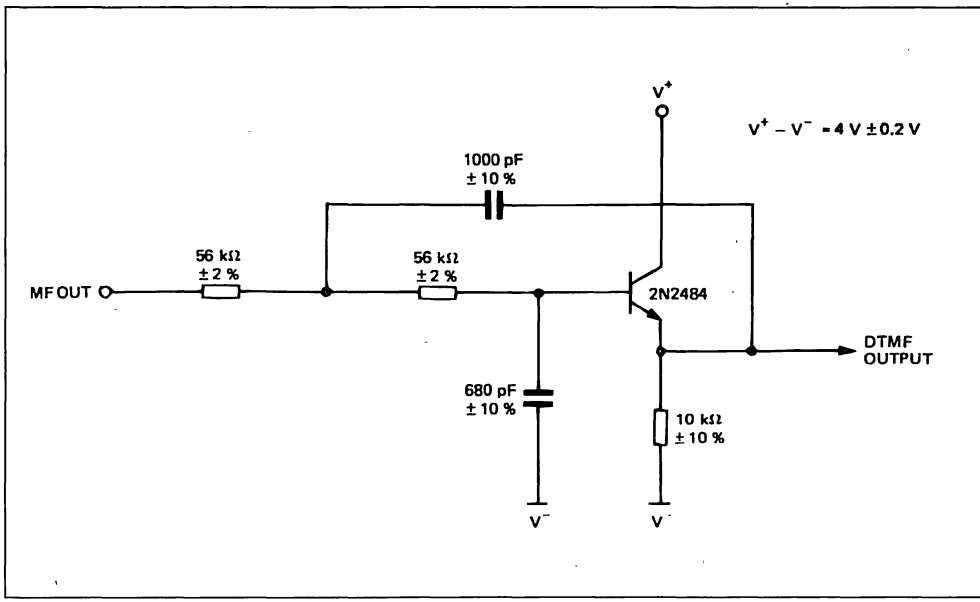
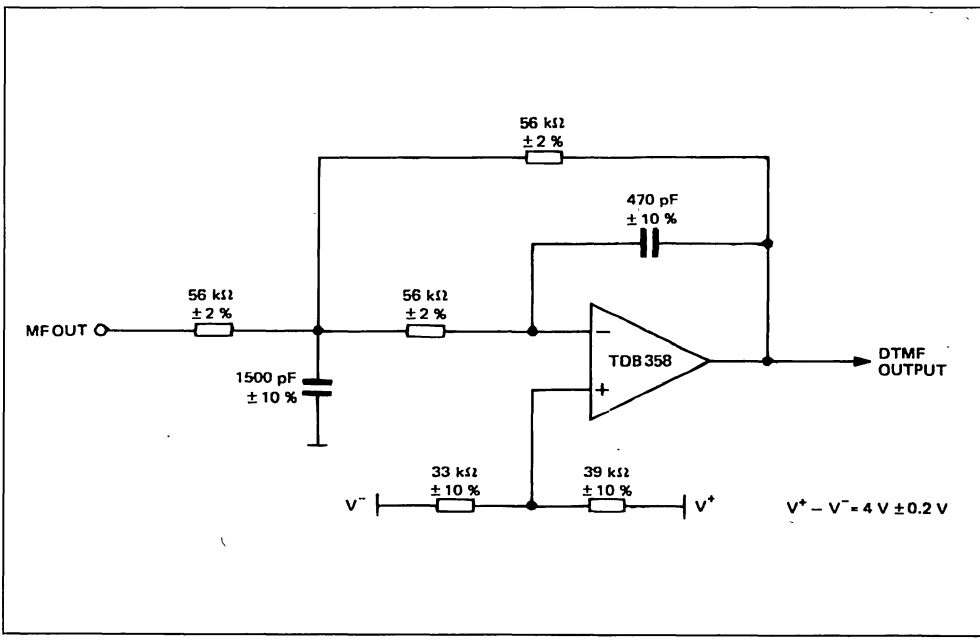


Figure 11 : With Op. Amp. (gain = 1).

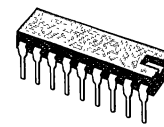


SGS-THOMSON MICROELECTRONICS

M761E

DUAL TONE MULTIFREQUENCY GENERATOR

- 2.4 TO 4 V SUPPLY RANGE
- VERY LOW POWER CONSUMPTION
- ON-CHIP CRYSTAL CONTROLLED OSCILLATOR (f_o = 4.433619 MHz) WITH INTEGRATED FEEDBACK RESISTOR AND LOAD CAPACITORS
- LOW HARMONIC DISTORTION (≤ 2 %)
- FIXED PRE-EMPHASIS ON HIGH-GROUP TONES
- FAST START-UP TIME
- LOW POWER CONSUMPTION IN STANDBY MODE
- MUTE OUTPUT
- ONE CONTACT PER KEY



DIP18

ORDER CODE : M761EB1

DESCRIPTION

The M761 provides all the tone frequency pairs required for a DTMF Dialling System. Tones are obtained from an inexpensive TV crystal (f_o = 4.433619 MHz) followed by two independent programmable dividers. The dividing ratio is controlled by the selected key. Keyboard format is 4 rows x 4 columns and a key is valid when a column and a row are connected together.

Internal logic prevents the transmission of illegal tones when more than one key is pressed. If no key is selected the oscillator turns off and the linear parts are strobed to decrease the total power consumption.

As any buttom is pressed row and column inputs are scanned internally, to identify the activated ones. Electrically, row and column inputs are activated on high level voltage.

Single tone output cannot be emitted by a "1" an a row or column only. For single tone emission see "Single tone procedure".

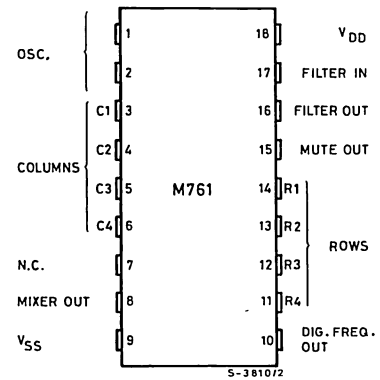
A debounce output is available to indicate that a key has been selected. D/A conversion is accomplished by a capacitive network allowing very low power consumption, very low distortion and an exceptional stability of tone level against temperature variations.

The tones are mixed in a resistive network ; a unity gain amplifier is provided to realize a two pole active filter with only four external passive components.

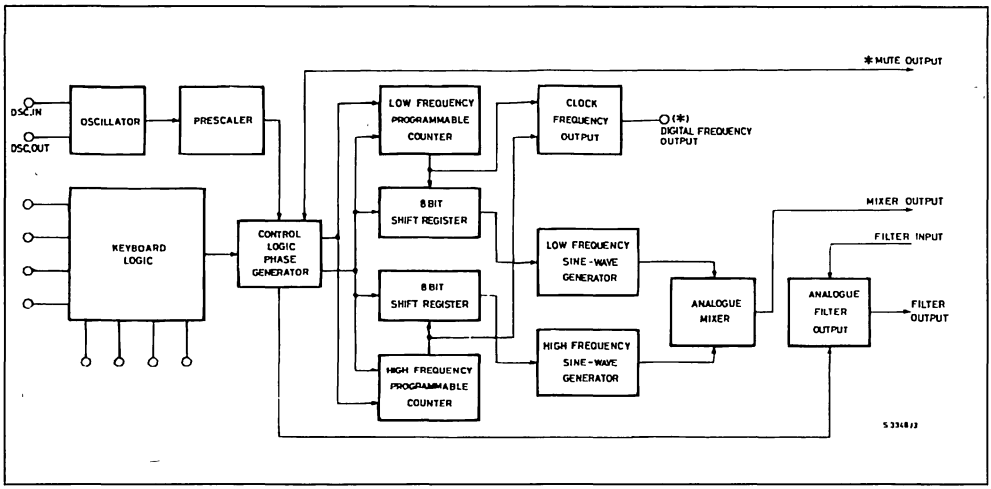
The M761 can be interfaced with the speech circuit family LS156, LS356, LS656 with MF interface avoiding the need of the common spring set.

The M761 utilizes low voltage CMOS technology and is available in 18 pin dual in-line plastic package.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.5 to + 5.5	V
V_I	Input Voltage	– 0.3 to V_{DD} + 0.5	V
P_{tot}	Power Dissipation	400	mW
T_{op}	Operating Temperature Range	– 25 to + 70	°C
T_{stg}	Storage Temperature Range	– 55 to + 125	°C

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (all parameters are tested at T_{amb} = 25 °C)

Parameter		Test Conditions (see note 1)	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
Supply	V_{DD} Voltage Supply Voltage		2.4	3	4	V
	I_{DD} Operating Supply Current	V_{DD} = 2.4 V			1.8	mA
	I_{DDO} Stand-by Supply Current	V_{DDO} = 2.55 V			0.3	mA
Row and Column Inputs	Input Voltage Levels					
	V_{IH} Logical "1"			80 % of (V_{DD}-V_{SS})	V_{DD} + 0.3	V
	V_{IL} Logical "0"			V_{SS} – 0.3 V	20 % of (V_{DD}-V_{SS})	V
	C_{IN} Input Capacitance Any Pin				7.5	pF
Oscillator	I_{IH} High Level Input Current	V_{DD} = 2.5 V V_{IN} = 2.5 V			1	µA
	I_{IL} Low Level Input Current	V_{DD} = 2.5 V V_{IL} = 0 V			1	µA
	I_{OH} High Level Output	V_{DD} = 2.5 V V_{OH} = 2 V	– 100	– 500		µA
	I_{OL} Low Level Output Current	V_{DD} = 2.5 V V_{OL} = 0.5 V	100	500		µA
Digit. Freq. Outp.	I_{OL} Low Level Output Current (open drain output)	V_{DD} = 2.5 V V_{OL} = 1 V	100			µA
Filter	V_O Output DC Voltage Without Tones	V_{DD} = 2.5 V			200	mV
	V_O Output DC + AC Voltage with 2 Tones	V_{DD} = 2.5 V (see note 2) (see fig. 1)	0.63	0.84	1.05	V
Mute Output	I_{OH} Output Drive Current	V_{DD} = 2.5 V V_{OH} = 1.5 V	– 100			µA
	I_{OL} Output Sink Current	V_{DD} = 2.5 V V_{OL} = 1 V	20			µA

Notes : 1. This device has been designed to be connected to the DTMF interface of the speech circuit family LS156, LS356, LS656 from which it takes a V_{DD} = 2.4 V min. Therefore many parameters are tested at this value.

2. The value of DC output component at two different conditions of supply voltage, with two tones activated, can be related as follows :

$$V_{DC'} = V_{DC} \frac{V_{DD'}}{V_{DD}}$$

3. The value of AC output components (V_{LF}, V_{HF}) at two different conditions of supply voltages can be related as follows :

$$V_{LF'} = V_{LF} \frac{V_{DD'}}{V_{DD}} \qquad V_{HF'} = V_{HF} \frac{V_{DD'}}{V_{DD}}$$

The values are measured with two tone at the output.

ELECTRICAL CHARACTERISTICS (all parameters are tested at T_{amb} = 25 °C)

Parameter		Test Conditions (see note 1)	Min.	Typ.	Max.	Unit
AC CHARACTERISTICS						
Oscillator	R_F Feedback Oscillator Resistance		1.5	4.5		MΩ
	C_I Input Capacitance to V_{DD}			9.5	10.5	pF
	C_O Output Capacitance to V_{DD}			10.5	11.5	pF
Mixer	Z_{01} Output Dynamic Impedance with 2 Tones	V_{DD} = 2.5 V		10		KΩ
Filter	Z_{02} Output Dynamic Impedance with 2 Tones	V_{DD} = 2.5 V		2.5		KΩ
Tone Characteristics	$\frac{\Delta F}{F}$ Max. Output Tone Derivation from Standard	At Crystal Frequency f = 4.433619 MHZ				
	R1 697 Hz				+ 0.5	%
	R2 770 Hz				− 0.2	%
	R3 852 Hz				+ 0.5	%
	R4 941 Hz				− 0.6	%
	C1 1209 Hz				+ 0.6	%
	C2 1336 Hz				− 0.4	%
	C3 1477 Hz				− 0.3	%
	C4 1633 Hz				+ 1.1	%
	V_{LF} Low Frequency Tones Amplitude at Filter Out	V_{DD} = 2.5 V (see note 3) (see fig. 2)	124		148	mV_{PP}
	V_{HF} High Frequency Tones Amplitude at Filter Out	V_{DD} = 2.5 V (see note 3) (see fig. 2)	157		187	mV_{PP}
	Pre-emphasis		1.25	2	2.75	dB
	Unwanted Frequency Components					
	at f = 3.4 KHz				− 33	dBm
	at f = 50 KHz				− 80	dBm
	Total Harminic Distortion for a Single Frequency	V_{DD} = 2.5 V			5	%
	t_s Start-up Time	V_{DD} + 2.5 V (see fig. 4) (see fig. 5)		3	5	ms
	t_r Supply Voltage Rise Time	V_{DD} = 2.5 V			250	ms

Notes : 1. This device has been designed to be connected to the DTMF interface of the speech circuit family LS156, LS356, LS656 from which it takes a V_{DD} = 2.4 V min. Therefore many parameters are tested at this value.

2. The value of DC output component at two different conditions of supply voltage, with two tones activated, can be related as follows :

$$V_{DC'} = V_{DC} \frac{V_{DD'}}{V_{DD}}$$

3. The value of AC output components (V_{LF}, V_{HF}) at two different conditions of supply voltages can be related as follows :

$$V_{LF'} = V_{LF} \frac{V_{DD'}}{V_{DD}} \qquad V_{HF'} = V_{HF} \frac{V_{DD'}}{V_{DD}}$$

The values are measured with two tone at the output.

FUNCTIONAL DESCRIPTION

OSCILLATOR (OSC. IN - OSC. OUT)

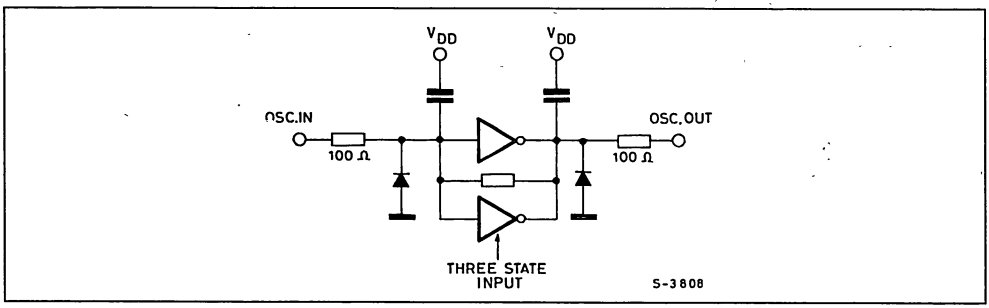
The oscillator circuit has been designed to work with a 4.433619 MHz crystal ensuring both fast start-up time and low current consumption.

When V_{DD} is applied and a key is activated two inverters are paralleled (see fig. below) to decrease the total r_{ON} resistance.

After oscillations have started one of the two buffers is switched off and the current consumption is reduced to 2/3 of the initial value.

Feedback resistance and load capacitances are integrated on the chip ensuring good temperature performance.

When the device is supplied but no key is activated, the oscillator is in the stand-by mode to minimize power consumption.



KEYBOARD INPUTS
(C1, C2, C3, C4 - R1, R2, R3, R4)

Each keyboard input has an internal protection circuit ; when a button is pressed, the oscillator starts and dynamic scanning of keyboard is realised.

This allows to the detection of which button has been pressed.

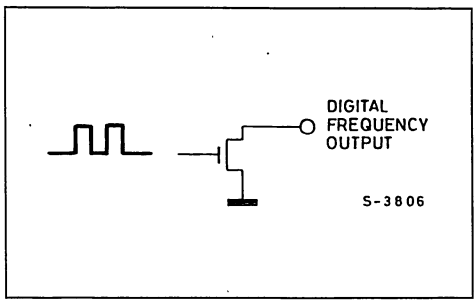
When two or more column or row inputs are activated no tone is generated.

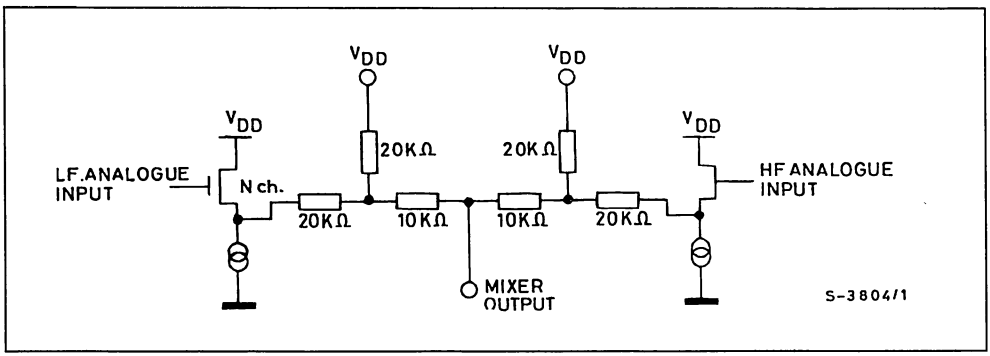
DIGITAL FREQUENCY OUTPUT

This output is intended for testing only ; when a single tone is activated, at this output is available a digital signal whose frequency is 16 times the selected output tone frequency. This output is an open collector N-channel transistor.

MIXER OUTPUT

The two reconstructed sine waves are buffered then mixed in a resistive array network that also restores the DC output level.



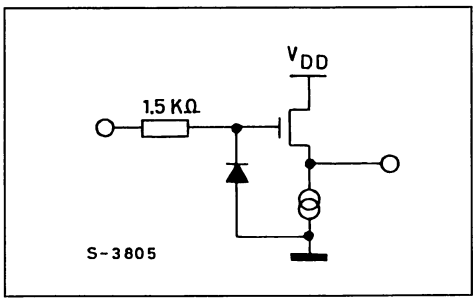


FILTER (Filter Input, Filter Output)

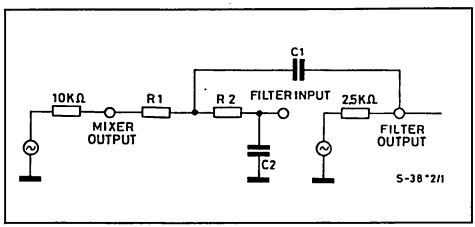
A unity gain amplifier is available to realize a two pole active filter (see fig. below). The output of this amplifier is held low until tones are valid, it than rises to about 0.85 V at V_{DD} = 2.5 V.
Tones are superimposed on this DC.

The output DC component is very precise and stable to allow DC coupling with the LS156 speech circuit with MF interface.

The output dynamic impedance of the filter is about 2.5 KΩ.



The following equivalent circuit should be applied during filter design :



It is evident that R1 and R2 should be kept high to avoid undue influence of Mixer and Filter output impedances.

The following values are suggested :

R1 = 56 KΩ ± 2 %
R2 = 33 KΩ ± 2 %
C1 = 2.2 nF ± 10 %
C2 = 0.56 nF ± 10 %

MUTE OUTPUT

Mute output becomes active when a key is activated eliminating keyboard bounces and remains active for all the duration of tone transmission.

If the key is released before the oscillator produces the correct control signals, mute output is disabled.

SINGLE TONE PROCEDURE

This is accomplished through the following steps :

1) Activate simultaneously R1, R4, C1, C4 inputs, appling logic 1'S. This implies the use of logic level sources. The single contact keyboard does not allow this procedure.
2) The device enters the "test mode" Now any single row or column frequency (or both) can be activated at output applying logic "1" to correspondant input (inputs).
3) To get out from "test mode" reply R1, R4, C1, C4, activation or power off/power on.

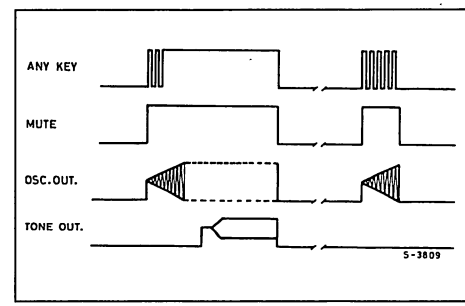
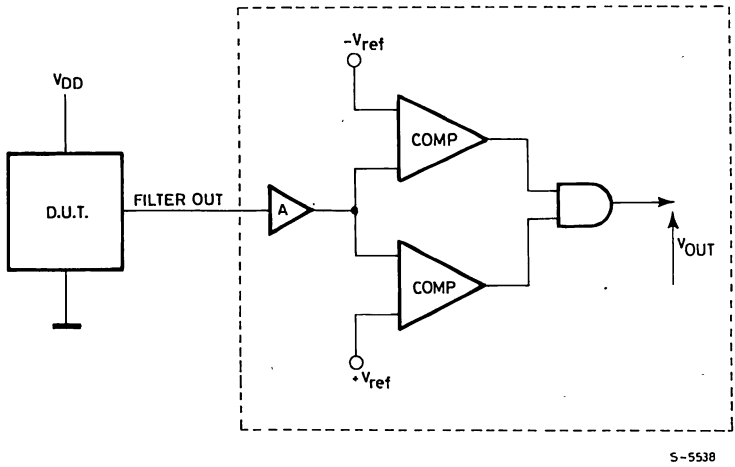
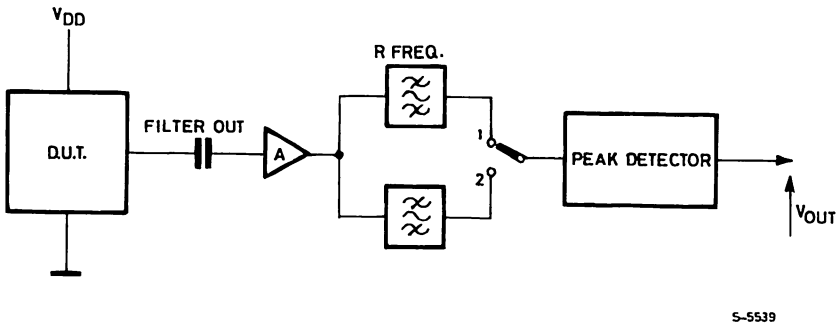


Figure 1 : DC + AC Out Level Measurement Test Set.



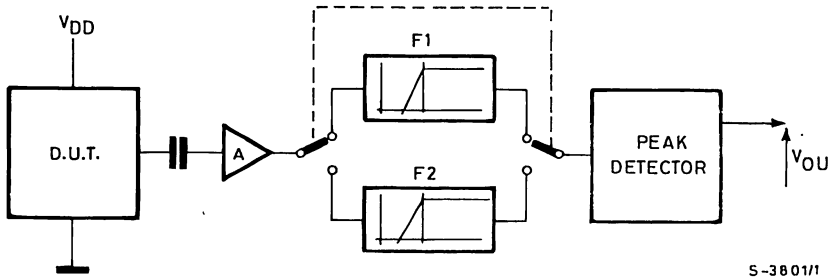
This measurement is performed with both row and column tones at output.

Figure 2 : Out Tone Level Measurement Test Set.



This measurement is performed with both row and column tones at output.

Figure 3 : THD Measurement Test Set.



High pass filters characteristics : F1 : f_0 = 1400 Hz 100 dB/dec
F2 : f_0 = 2500 Hz 100 dB/dec

THD measurement is made by sensing the level of harmonic components after suppression of the fundamental. Two different high pass filters are used for low and high frequency tones.

Figure 4 : Start-up time Measurement Test Set.

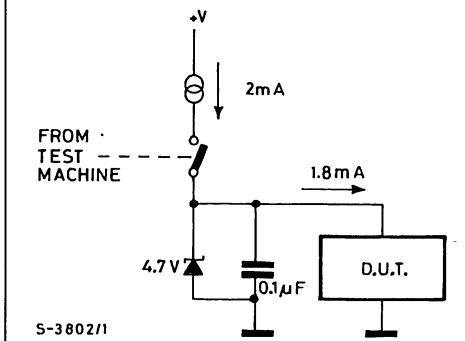
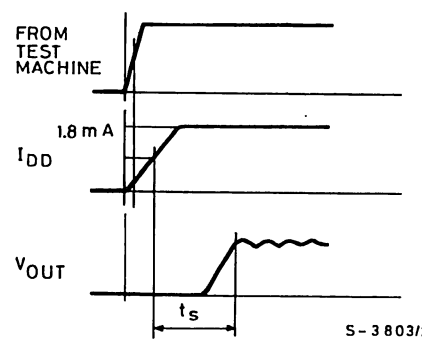
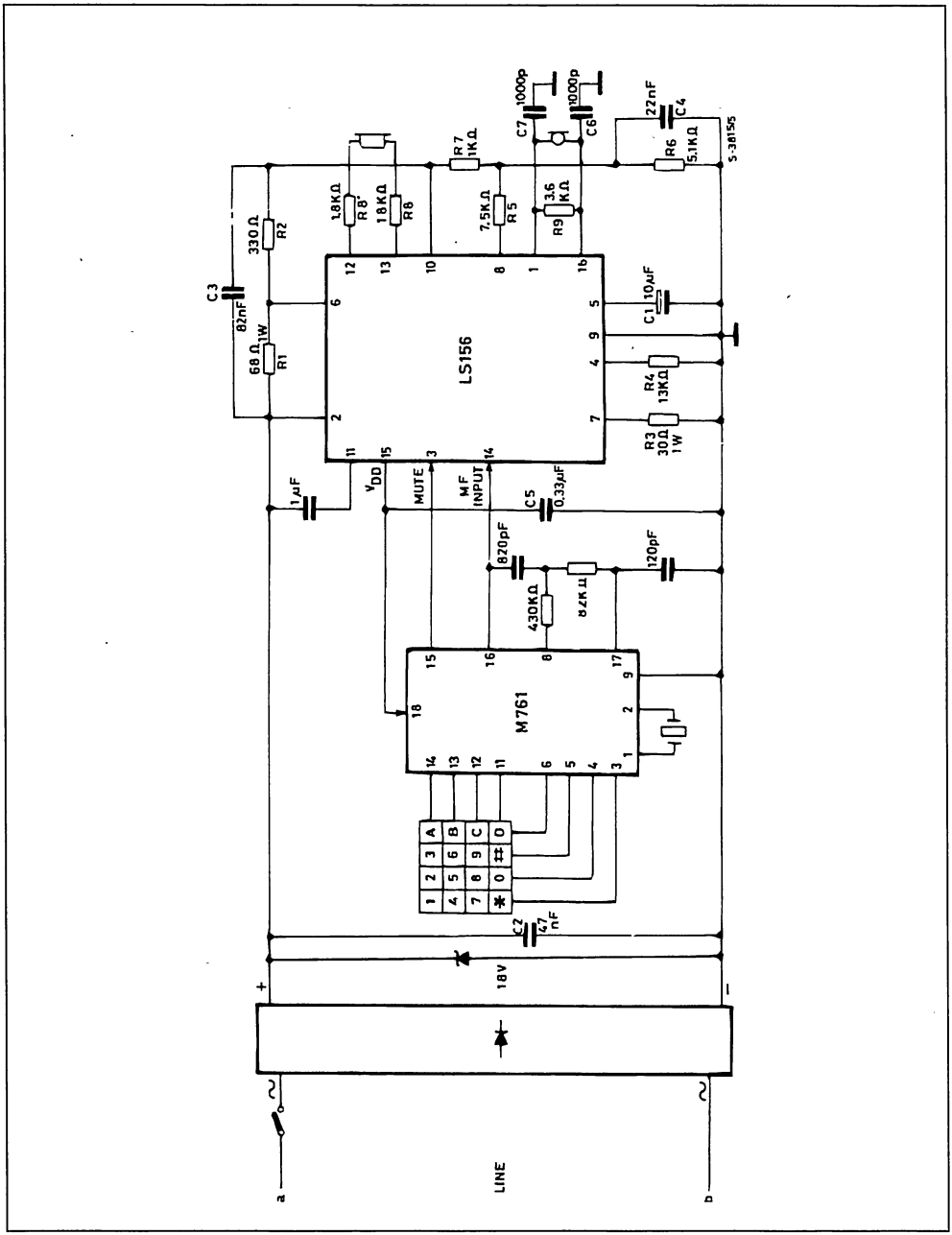


Figure 5 : Start-up time Definition.



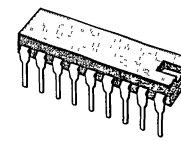
TYPICAL APPLICATIONS

Figure 6 : M761 application circuit with electronic speech circuit.



PULSE DIALER

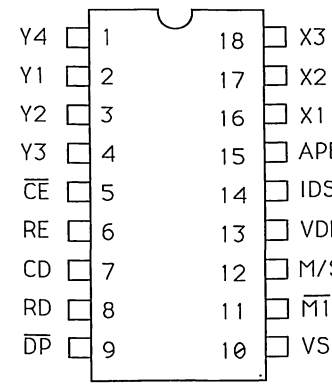
- OPERATION FROM 1.5V TO 5.5 SUPPLY
- STATIC STANDBY OPERATION DOWN TO 1V
- LOW CURRENT CONSUMPTION : 100uA, 1.5V
- LOW STATIC STANDBY CURRENT : MAX 500nA
- LAST NUMBER REDIAL FUNCTION
- 32 DIGIT CAPACITY, INCLUDING ACCESS PAUSES
- ON-CHIP RC OSCILLATOR USING THREE EXTERNAL COMPONENTS
- DIALING RATE CAN BE VARIED BY CHANGING THE DIAL RATE OSCILLATOR FREQUENCY
- DIALING PULSE MARK/SPACE RATIO SELECTABLE : 1.5 : 1 OR 2 : 1
- CIRCUIT RESET FOR LINE POWER BREAKS > 220ms
- ACCESS PAUSE GENERATION VIA THE KEYBOARD
- ACCESS PAUSE RESET VIA THE KEYBOARD



DIP18
(0,25mm)

ORDER CODE : M3561B

PIN CONNECTION



M89M3561-01

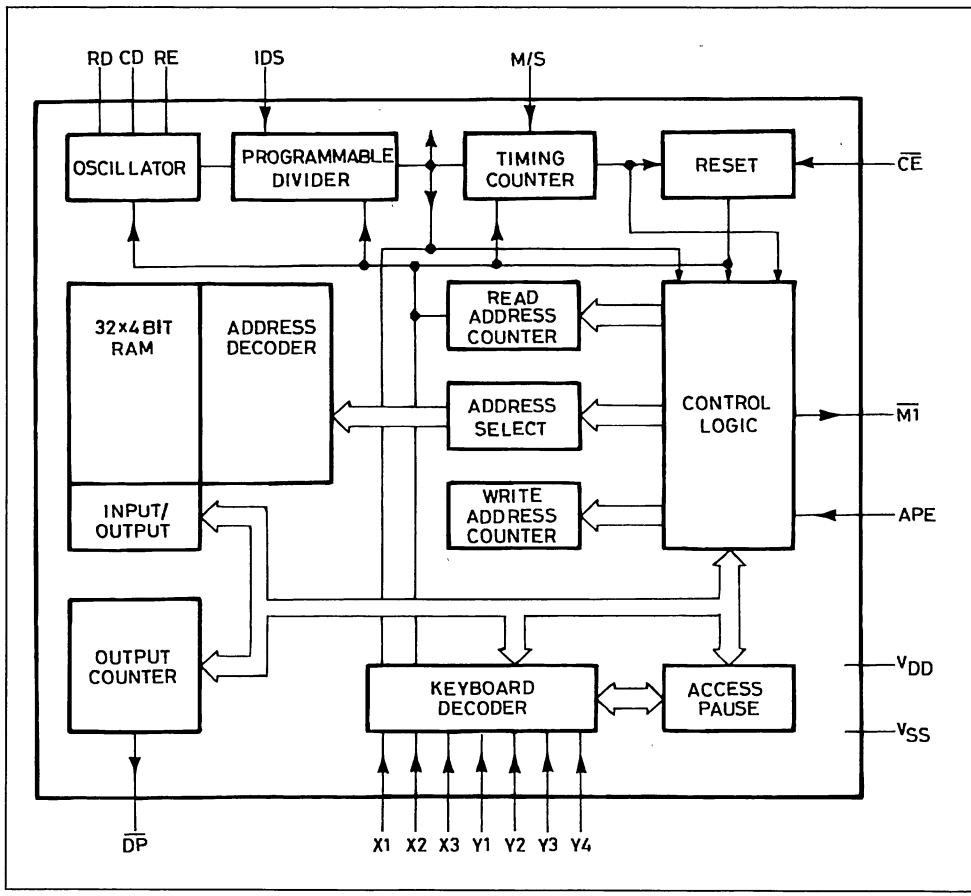
DESCRIPTION

The M3561 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert push button keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 push button matrix. Numbers with up to 32 digits can be retained in a RAM for redial. Access pause can be stored via the keyboard.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	+ 7	V
V_{IN}	Voltage on any Pin	(V_{SS} – 0.3) to (V_{DD} + 0.3)	V
T_{OP}	Operating Temperature	(– 25 to + 70)	°C
T_{ST}	Storage Temperature	(– 65 to + 150)	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V ; V_{SS} = 0V ; f_{OSC} = 2.4KHz ; T_{amb} = – 25°C to + 70°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Operating Supply Voltage		1.5		5.5	V
V_{DR}	Data Retention Voltage	$\overline{CE}$ = V_{DD}	1			V
I_{DD}	Operating Supply Current	$\overline{CE}$ = V_{SS} ; V_{DD} = 1.5 V $\overline{CE}$ = V_{SS} ; V_{DD} = 5.5 V T_{amb} = 25 °C			100 500	µA µA
I_{DDO}	Standby Supply Current	$\overline{CE}$ = V_{DD} ; V_{DD} = 1.5 V M/S = V_{DD} ; IDS = APE = V_{SS}			500	nA
V_{IL}	Input Voltage Low	1.5 V ≤ V_{DD} ≤ 5.5 V	V_{SS} – 0.3 V		20 % of V_{DD}	
V_{IH}	Input Voltage High	1.5 V ≤ V_{DD} ≤ 5.5 V	80 % of V_{DD}		V_{DD} + 0.3 V	
– I_{IL} I_{IH}	Input Leakage Current $\overline{CE}$ Low $\overline{CE}$ High	$\overline{CE}$ = V_{SS} $\overline{CE}$ = V_{DD}			100 100	nA nA
– I_{IL}	Pull-up Input Current M/S	V_I = V_{SS}	0.4		4	µA
R_{KON}	Keyboard "ON" Resistance	Contact ON			1	kΩ
R_{KOFF}	Keyboard "OFF" Resistance	Contact OFF	1			MΩ
I_{IH}	Input Current for Xn, "ON"	V_I = V_{DD}			30	µA
I_{IH}	Input Current for Yn, "ON"	V_I = V_{DD}			30	µA
– I_{IL}	Input Current for Xn "OFF"	V_I = V_{SS}			220	µA
– I_{IL}	Input Current for Yn "OFF"	V_I = V_{SS}			220	µA
I_{OL}	Outputs $\overline{M1}$, $\overline{DP}$: Sink Current	V_{OL} = 0.5 V	1	6		mA
– I_{OH}	Source Current	V_{OH} = 2.0 V	1	6		mA
f	Oscillator Frequency	V_{DD} = 1.5 V			10	KHz
Δf	Frequency Deviation (%) $\Delta f = \frac{\lvert f(1.5\ V) - f(3.5\ V)\rvert}{f(2.5\ V)}$	1.5 V ≤ V_{DD} ≤ 3.5 V fixed R_C Oscillator Components : R_d = 715 kΩ R_e = 750 kΩ C1 = 270 pF T_{amb} = 25 °C			4	%

TIMING CHARACTERISTICS

(V_{DD} = 1.5 to 5.5V ; V_{SS} = 0 ; fosc = 2.4KHz ; T_{amb} = 25°C)

Symbol	Parameter		Test Conditions	Value	Unit
f_{CL}	Clock Pulse Frequency	30 x f_{DP}		300	Hz
f_{DP}	Dialing Pulse Frequency	$1/T_{DP}$	IDS = V_{SS}	10	Hz
t_m t_m	Make Time	2/5 x T_{DP} 1/3 x T_{DP}	M/S = V_{DD} M/S = V_{SS}	40 33.3	ms ms
t_b t_b	Break Time	3/5 x T_{DP} 2/3 x T_{DP}	M/S = V_{DD} M/S = V_{SS}	60 66.6	ms ms
t_{id}	Inter Digit Pause	8 x T_{DP}	IDS = V_{SS}	800	ms
t_{pd}	Pre Digit Pause	8.4 x T_{DP}	IDS = V_{SS}	840	ms
t_{rd}	Reset Delay Time			223	ms
$t_{e\ min}$ $t_{e\ max}$	Debounce Time	Min. Max.		13.3 16.7	ms ms
$t_{en\ max}$	Clock Enable Time			1	ms
$t_{ON\ max}$	Clock Start-up Time			1	ms
$t_{i\ typ}$	Initial Data Entry Time	$t_{ON} + t_e$		16	ms

GENERAL DESCRIPTION

1. Pin Description

Y4 ; Y3 ; Y2 ; Y1 (pins 1 through 4)

Row keyboard input pins

$\overline{CE}$ (pin 5)

Chip Enable input pin. It is used to initialize the system, to select between the operational mode and the static standby mode, to handle line power breaks.

RE ; CD ; RD (pins 6 through 8)

Oscillator pins. These pins are used to connect external resistors RD, RE and capacitor CD to form a R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.

$\overline{DP}$ (pin 9)

Dial Pulse output pin. This signal is provided to drive the external line switching transistor or relay. The output will be "low" during "space" and "high" otherwise.

VSS (pin 10)

Negative supply input pin.

$\overline{M1}$ (pin 11)

Mute output pin. This signal can be used to mute the receiver during the dialling sequence.

M/S (pin 12)

Mark/Space selection input pin. This pin controls the mark to space ratio of the line pulses :

M/S = VSS (33.3/66.6) ; M/S = VDD (40/60).

M/S has an internal pull-up resistor.

VDD (pin 13)

Positive Supply input pin.

IDS (pin 14)

This pin must be connected to Vss.

APE (pin 15)

This pin must be connected to Vss.

X1 ; X2 ; X3 (pins 16 through 18)

Column keyboard input pins.

Table1 : Table for selecting oscillator component values for desired dialing rates and inter-digit pauses.

Osci. Freq. [KHz]	RD kΩ	RE kΩ	CD [pF]	Dial Rate (pps) IDS = V_{SS}	IDP (ms) IDS = V_{SS}
1.32	Select component in the ranges indicated in table of electrical specificatiion			5.5	1454
1.44				6	1334
1.56				6.5	1230
1.68				7	1142
1.80				7.5	1066
1.92				8	1000
2.04				8.5	942
2.16				9	888
2.28				9.5	842
2.40	715	750	270	10	800
f				f/0.24	1920/f

Table 2 : Input Pin Selection.

Function	Pin	Input Level	Selection
Mark/space Ratio	M/S	V_{SS} V_{DD}	1 : 2 1 : 1.5
Chip Enable	$\overline{CE}$	V_{SS} V_{DD}	Off-hook On-hook

2. Clock Oscillator

This device contains an oscillator circuit that requires three external components : two resistors (RD and RE) and one capacitor (CD). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times, including the "on hook" condition. For a dialing rate of 10 pps, the oscillator should be adjusted to 2400Hz. Typical values of external components for this are RD = 715Kohm and RE = 750Kohm and CD = 270pF.

It is recommended that the tolerance of resistors be 1%, and that of the capacitor be 5%, to insure a ± 10% tolerance of the dialing rate in the system.

3. Chip Enable ($\overline{CE}$)

The $\overline{CE}$ input is used to initialize the chip system.

$\overline{CE}$ = High provides the static standby condition. In this mode, the clock oscillator is off, and internal registers are clamped in reset, with the exception of WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When $\overline{CE}$ = Low, the clock oscillator is again off but the internal registers are enabled and data can be entered from the keyboard. After the first keyboard entry the clock oscillator starts.

If the $\overline{CE}$ input is taken to a High level for more than the time trd (see figures 3 and 4 and timing data), an internal reset pulse will be generated at the end of the trd period. The system is then is the static standby mode.

Short $\overline{CE}$ pulses of < trd will not affect the operation of the circuit. No reset pulses are then produced.

4. Debouncing Keyboard Entries

The column keyboard inputs to the integrated circuit (Xn) and the row keyboard inputs (Yn) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact), as shown in fig. 1, or to a double contact keyboard with a common connected to VDD (see figure 2). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input, or when one column input and one row input are set High. Any other input combinations will be judged to not be valid and will not be accepted.

Valid inputs are debounced on to the leading and trailing edges, as shown in figure 3 : Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period te). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Figure 1 : Single Contact Keyboard.

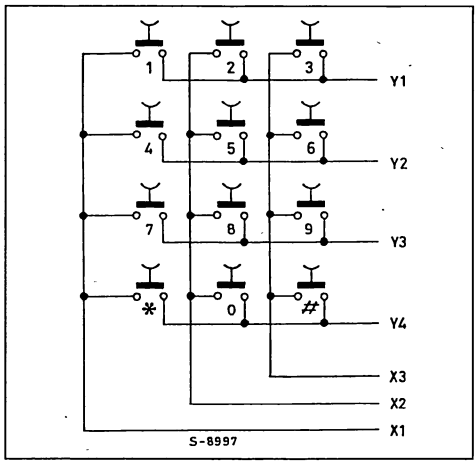
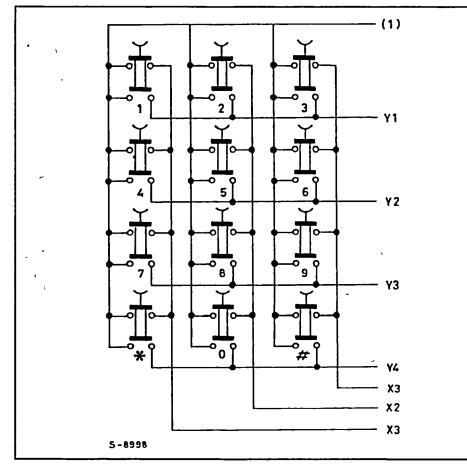


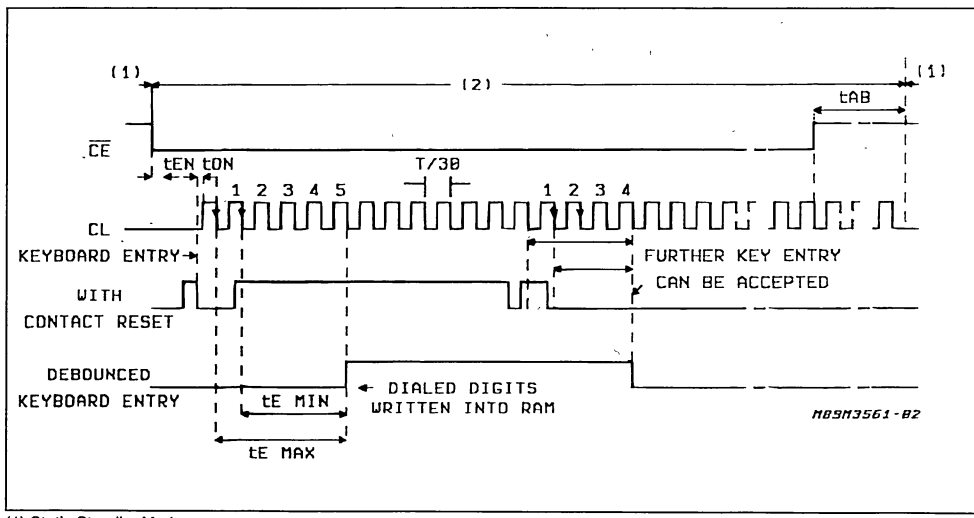
Figure 2 : Double Contact Keyboard.
(1) common (connected to VDD).



Key : Redial or Set/Reset Access Pause.

Figure 3.

Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply. to $\overline{CE}$ during the transmission of dialing pulses.



(1) Static Standby Mode.
(2) Dialing Mode.

5. Data Storage and Data Retrieval

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM, but not yet converted into line pulses.

If more than 32 keycodes are written into the RAM, memory overflow results and the excess keycodes replace the data in the lower-numbered RAM locations. In this event, since an erroneous number is stored, automatic redialing is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first push button to be pressed is not redial (#), the WAC is reset during entry time te, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one to select the next RAM location. Consequently, if the first push button pressed is not redial, the data stored previously in the RAM cannot be redialed anymore.

If the first push button is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialing pulses at output $\overline{DP}$. If the redial push button (#) is operated again during the redialling sequence, it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the M3561. During and after redial, new keyboard entries will be accepted, and converted into correctly timed dialing pulses. These new keyboard are not stored in RAM.

6. Dialing Sequence

The dialing sequence can be initiated under the following conditions :

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry) ; see fig. 4.

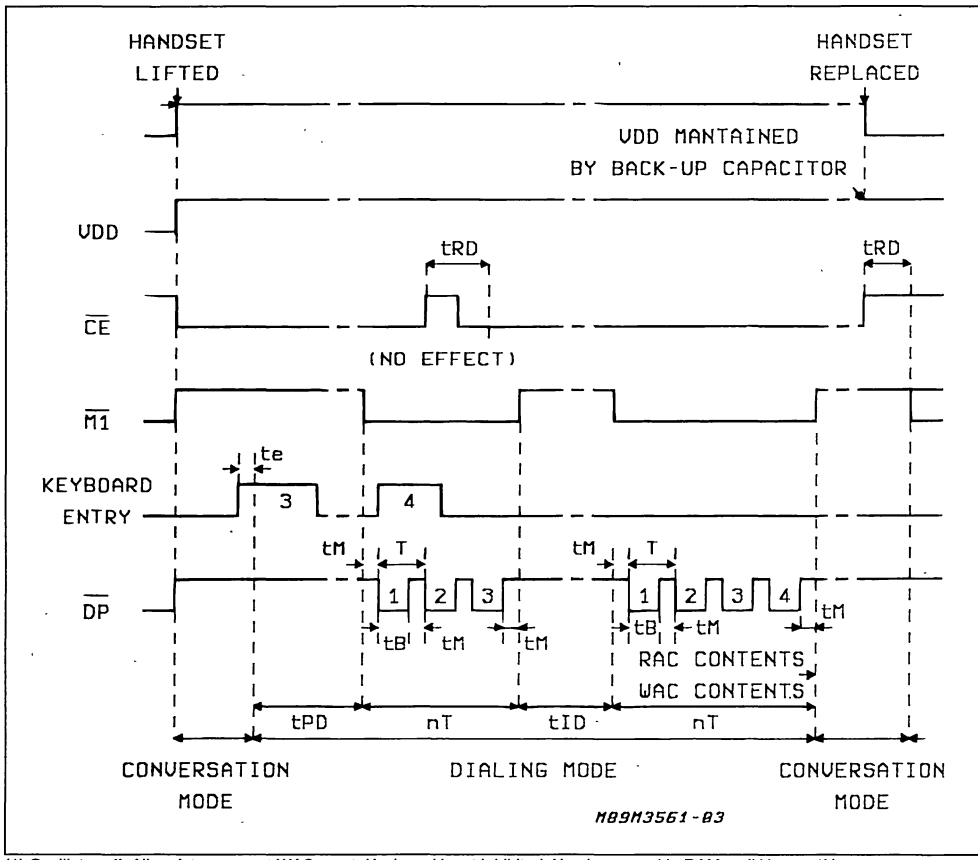
Then, approximately 1ms (ten) after $\overline{CE}$ goes Low, the clock pulse generator is enable, and the circuit is in the conversation mode, while the subscriver waits for the dialing tone. When the first digit of the required number is entered at the keyboard, the clock oscillator starts and data entry period te begins.

The further dialing sequence will be described with the aid of fig. 4. When the keyboard entry has been decoded and written into the RAM, $\overline{M1}$ goes LOW to mute the telephone with a delay of about one Inter Digit Pause time (1.1 *tid), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter, which generates the appropriate number of correctly timed dialing pulses at output $\overline{DP}$.

When the digit has been pulsed out, $\overline{M1}$ goes HIGH, at least for one IDP, the RAC is incremented by one, and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out).

When $\overline{M1}$ is High, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if $\overline{CE}$ goes High for more than the reset delay time (trd) at any time during the conversation or dialing mode (e.g., because the handset is replaced). $\overline{CE}$ remains High although VDD is maintained by a backup supply (e.g., because an external diode isolates $\overline{CE}$ from the back-up supply connected to VDD). The RAM retains its contents for subsequent automatic redialing as long as the back-up supply maintains VDD above VDR = 1V.

Figure 4.
Timing diagram of dialing sequence with V_{DD} and $\overline{CE}$ Low before keyboard entry (e.g., supply via the cradle contacts).



(1) Oscillator off. All registers except WAC reset. Keyboard input inhibited. Number stored in RAM until V_{DD} >= 1V.

7. Storage and Regeneration of Access Pauses

A dial sequence may require an extended Inter Digit Pause if it is necessary to wait for the dial tone. During the keyboard entry, whenever an access pause is needed, a pause code can be stored in the RAM, via the keyboard (# key) for a later redial sequence. When an access pause is regenerated during redialing, it can be terminated via keyboard (# key).

A pause code takes one position in the RAM like a digit. The number of digits plus the number of access pauses cna therefor bu up to 32.

7.1. MANUAL PAUSE. Access pause codes can be stored in the RAM at appropriate positions by pressing the access pause key (# key). A manual pause code can be stored after any digit. The maximum number of manual pause codes is not limited. Consecutive manual pause codes will generate a single pause during redial.

During the redial sequence the manually stored codes will automatically generate pauses. The duration of the manual pause is unlimited. Whenever a manual pause code is read from the RAM, the normal Inter Digit Pause is extended until it is terminated manually by presssing key #.

8. Summary of Special Keyboard Functions

Key # : Inserts a manual pause code, if activated after a number key, or terminates a manual pause, if activated during the pause.

Key # : Starts the redial sequence, if activated as first key after off-hook.

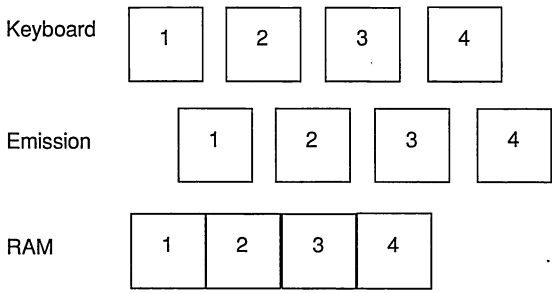
9. Statc Standby Operation

$\overline{CE}$: HIGH turns off the oscillator and resets all internal registers, with the exception of the WRITE ADDRESS COUNTER and the RAM. All input pull-up and pull-down devices are switched off. The current consumption is reduced in this condition such that the supply voltage required to hold the data stored in the RAM can be provided by a capacitor.

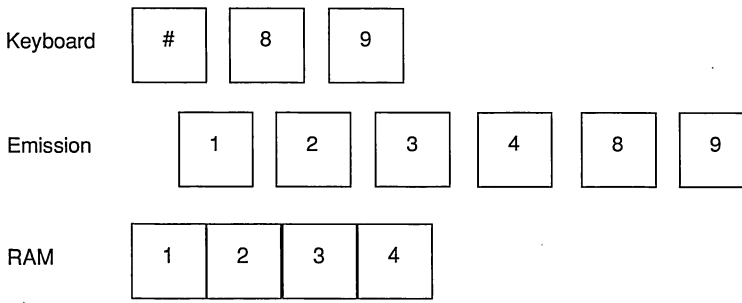
10. Selection of Extra Digits During or After Redial

Case 1

1th selection



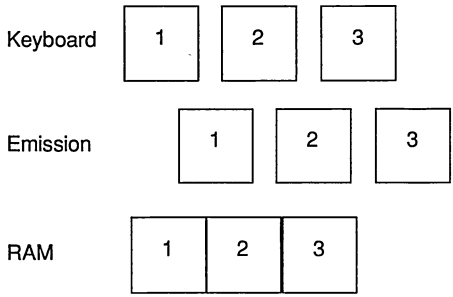
Redial



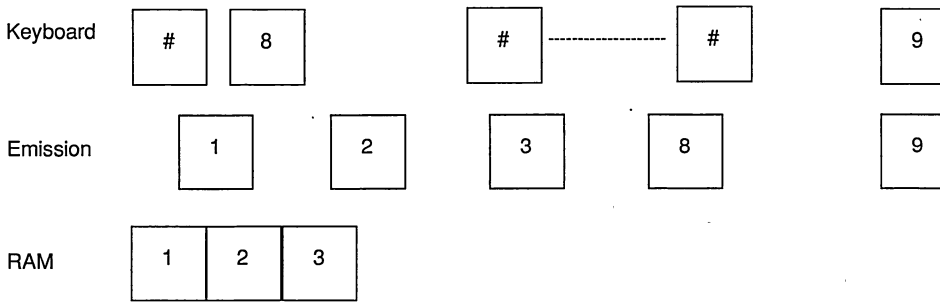
Comment : The key entries [8] and [9] after "Redial" are dialed buty not memorized.

Case 2

1st selection



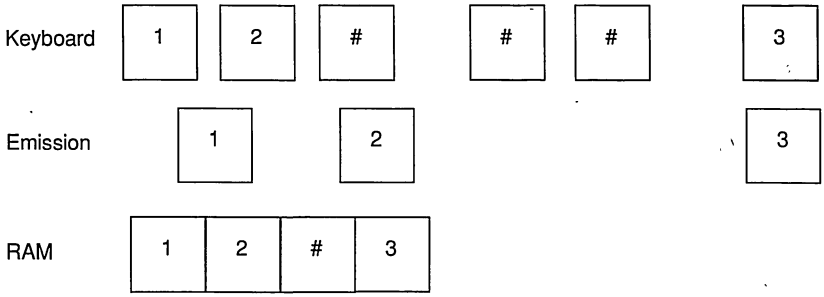
Redial



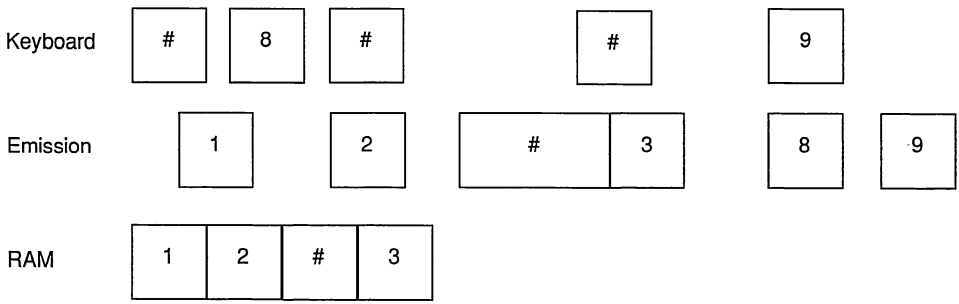
Comment : The first key [#] is used as "Redial", the other keys [#] are ignored because no manual pause was memorized during the first selection.

Case 3

1st selection



Redial

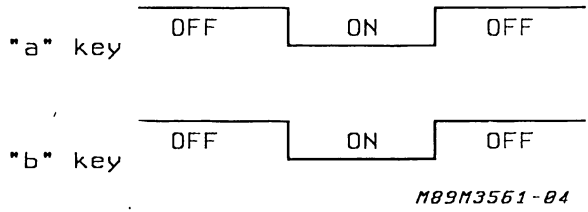


Comment : during the first selection if many keys [#] are pressed consecutively only one is memorized in the RAM. In the second selection the first [#] key is used as Redial, the second is ignored since the emission is still going and the third ends the manual pause inserted in the first selection.

11. Multiple Key Pressing

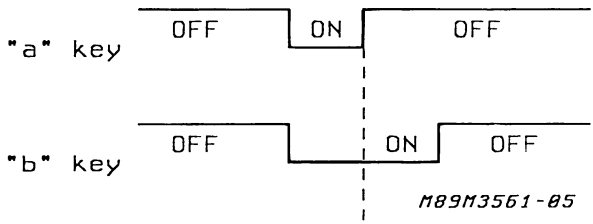
If two keys are pressed at the same time, the following operation will take place.

Case 1



These key inputs will be completely ignored.

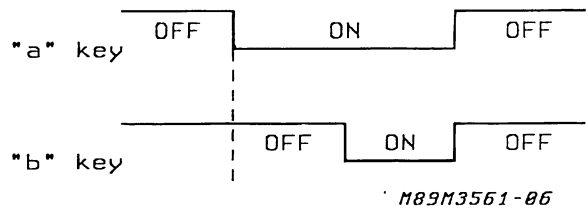
Case 2



The "a" key input wil be ignored.

The "b" key input will be read from this point (|)

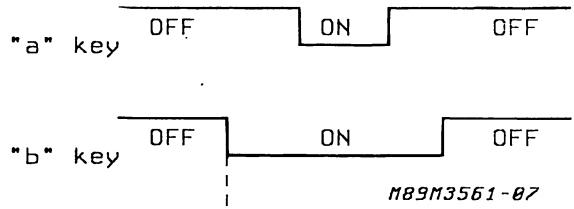
Case 3



The "a" key input will be read from this point (|)

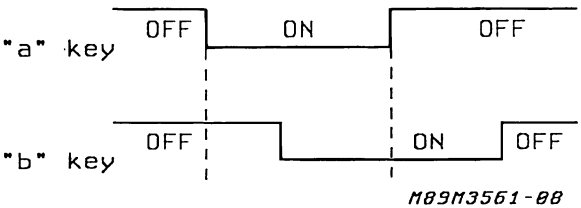
The "b" key input will be ignored.

Case 4



The "b" key input will be read from this point (|).
Consequently the "b" key is read once and the "a" key is ignored.

Case 5



The "a" key input wil be read from 1st point (|). The "b" key input will be read from 2nd point (|).
Consequently the "a" key and the "b" key are read once each.-

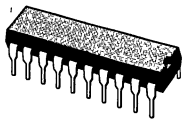
SGS-THOMSON MICROELECTRONICS

M3540

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER WITH SAVE FACILITY

PRELIMINARY DATA

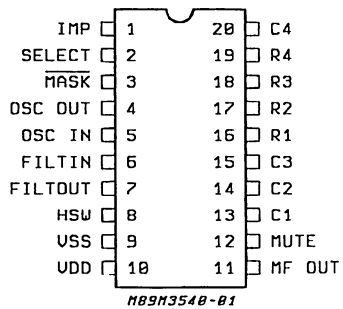
- SELECTABLE LOOP DISCONNECT OR DTMF DIALLING MODES
- ALLOWS USER TO SWITCH FROM LD TO DTMF DIALLING DURING A CALL
- LNR FACILITY ALLOWS UP TO 32 DIGITS TO BE RETAINED FOR REDIALLING
- SELECTABLE MAKE/BREAK RATIOS 2 : 1 AND 3 : 2
- SELECTABLE INTERDIGIT PAUSE 500ms OR 800ms
- USES INEXPENSIVE 560KHz RESONATOR
- TIMED BREAK RECALL (timed flash)
- OPERATES WITH INEXPENSIVE SINGLE CONTACT KEYPAD
- CAPABLE OF BATTERY-LESS OPERATION. LOW POWER CMOS PROCESS ALLOWS DIRECT OPERATION FROM TELEPHONE LINES



DIP20

ORDER CODE : M3540B

PIN CONNECTION



M89M3540-01

DESCRIPTION

The M3540 is a keypad switchable LD/DTMF dialer devices designed for use in low cost, dual dialing mode telephone instruments. It is suitable for sending telephone numbers without limit and an on-chip memory allows numbers of up 32 digits to be retained for redialling later. The low power CMOS design allows the number in the memory to be maintained indefinitely (until overwritten) by a minimal current leaked from the telephone line. A particular feature of this device is the facility for the user to switch dialling mode from LD to DTMF via the keypad during the course of a call. This is intended for uses such as home banking, access to long distance trunk service, credit card verifications and other applications which require data to be sent at low speed once a connection has been established.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
	Supply Voltage V_{DD} - V_{SS}	– 0.3		6.5	V
	Voltage on any Pin Except HSW Voltage on Pin HSW (current limited to < 100µA)	V_{SS} – 0.3 V_{SS} – 0.3		V_{DD} + 0.3	V V
	Current at any Pin Except FILTOUT and FILTIN Current at Pin FILTIN Current at Pin FILTOUT	– 1 0 – 5		+ 1 0.1 0	mA mA mA
	Operating Temperature Storage Temperature	– 10 – 55		+ 55 + 125	°C °C

* Stresses above the listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

D. C. ELECTRICAL CHARACTERISTICS

(at 2.5V, 25°C unless otherwise stated)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
	Supply Voltage - Off-hook Supply Voltage - On-hook	2.5 2.0		5.5 5.5	V V
	Supply Current - On-hook at 2.0V Supply Current - Off-hook (idle)		 1.5	1000 15.0	nA µA
	Supply Current - MF tone sending Supply Current - LD impulsing			1.0 200	mA µA
	Hookswitch Input - On-hook Hookswitch Input - Off-hook	 0.8 V_{DD}		0.2 V_{DD}	
	$\overline{MASK}$, MUTE and IMP Outputs, Load – 1mA MASK, MUTE and IMP Outputs, Load + 1mA	2.2		 0.3	V V
	MF OUT D.C. Level During Tone Sending		0.9 V_{DD}		
	MF OUT Output Resistance		3		kΩ
	Darlington Pair Current Gain at I_E = 100µA, V_{CE} = 2V	 600			

A.C. ELECTRICAL CHARACTERISTICS

(at V_{DD} = 2.5V, 25°C unless otherwise stated)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
	Tone Amplitude Low Group Tone Amplitude High Group } no Load	57	64 81	 91	mVrms mVrms
	Ratio of High to Low Group Amplitude	1.5	2	2.5	dB
	Total Harmonic Distortion : 0 - 4 kHz 0 - 10 kHz 0 - 50 kHz 0 - 200 kHz		2 2.5 5 6.5	 10	% % % %

PIN FUNCTIONS

Pin Name	Function
ROW 1 ROW 2 ROW 3 ROW 4 COL 1 COL 2 COL 3 COL 4	Connections for 16 Buttons, Single Contact Keyboard
V_{DD}	Positive Supply
V_{SS}	Negative Supply
SELECT	LD/MF Selection, IDP and B/M Ratio Programming
OSCIN OSCOUT	Oscillator Connection
HSW	Hookswitch. A logic '1' voltage at this pin is used to indicate 'off-hook'.
$\overline{MASK}$	Output to disable speech circuit during pulse dialling and recall (see note 1).
IMP	'Loop Disconnect' Dialling Output
MF OUT	Unfiltered, Dual Tone Output
FILTOUT FILTIN	Unity Gain Amplifier Input and Output for 2-pole Filter
MUTE	Output Active During Keying and Tone Transmission (see note 2)

Notes : 1. The $\overline{MASK}$ output may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook, during a TBR (timed flash) operation or for LD dialling.
2. The MUTE output is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

KEYPAD OPERATION

The device will accept keypad inputs only in the 'off-hook' condition when the key is pressed for more than 14ms. Any key pressed during the 'on-hook' condition will be ignored and the oscillator inhibited. This ensures that the current drain 'on-hook' is low and used only for memory retention.

KEYPAD FORMAT

	C1	C2	C3	C4
R1	1	2	3	TBR
R2	4	5	6	REDIAL
R3	7	8	9	SAVE
R4	*	0	#	TONE

n89m3548-02

TBR = Timed Break Recall (Timed Flash)
SAVE = Save digits dialled since going off-hook
REDIAL = Redial digits in 'save' store
TONE = Change dialling mode from LD to DTMF
* and # are available in DTMF mode only

LD/DTMF MODE SELECTION

The initial dialling mode after the telephone goes off-hook is determined as follows :

DTMF - Connect SELECT pin to V_{DD}

LD –

Option		Connect SELECT pin to :
IDP	B/M Ratio	
800ms	2:1	V_{SS}
500ms	2:1	COL 1
500ms	3:2	COL 2
800ms	3:2	COL 3

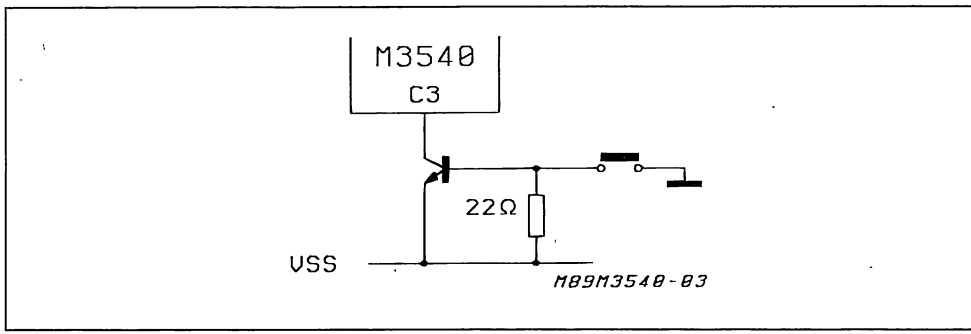
LD dialing is at 10 p.p.s. for all options

KEYPAD LD/DTMF MODE CHANGE

Pressing the TONE key at any time after going off-hook will cause subsequently entered digits to be dialled in DTMF. If the TBR (Timed Flash) key is Pressed, or an Earth Loop Recall operation is signalled to the chip, further dialling is set to the initial mode again.

In order to signal an ELR operation to the chip, the following configuration should be adopted :

Figure 1.



'SAVE' STORE OPERATION

The 'save' store is 31 digits long. If the user attempts to save a number of more than 31 digits the store is inhibited. The contents of the 'save' store are maintained until overwritten.

To load the 'save' store :

At any time whilst off-hook the SAVE key may be pressed. This action causes digits dialled since going off-hook to be retained, and the previous contents of the store are overwritten. Further digits may be dialled after pressing the SAVE key but these will not be retained.

To redial the number in the 'save' store :

Whilst in the speech mode, press REDIAL once.

However, if an LD to DTMF mode change was effected when the number was originally dialled, a marker* in the 'save' store will cause the redialling to pause at this point and the speech circuit will be reactivated. If the REDIAL key is then pressed again, the remaining digits in the store will be redialled in DTMF.

If the redial feature is invoked after going off-hook, the digits in the 'save' store will be redialled as described above. If the redial feature is not invoked after going off-hook, it is possible to first key in digits and then press REDIAL. If the digits keyed in correspond with the first digits in the 'save' store, the remaining digits will be automatically redialled (this feature is provided to allow manual keying of an access code followed by a pause before dialling out the rest of the number). If, however, a digit is keyed which differs from the corresponding digit in the store number, then redialling is inhibited.

* This marker requires one location of the 31 digit store

LAST NUMBER REDIAL

The function of the Last Number Redial store is to automatically retain the last number dialled so that it can be redialled later simply by pressing the LNR key. Either LD or MF numbers will be retained in the store. When numbers containing an LD part followed by an MF part are dialled, only the LD part will be retained in order that security codes, etc., dialled in MF are not automatically stored.

To redial a number, go off-hook and press LNR once. Alternatively, digits may be keyed manually before LNR is pressed. If the digits keyed correspond with the first digits in the LNR store, the remaining digits will be automatically redialled when LNR is pressed (this feature allows manual keying of an access code followed by a pause before dialling out the rest of the number). If, however, a digit is keyed which differs from the corresponding digit in the stored number, then redialling is inhibited.

HOOKSWITCH OPERATION

The hookswitch input is used to inform the M3540 of whether the telephone is on- or off-hook. When the telephone is on-hook the M3540 will adopt a static low power mode in which dialling functions are inhibited and only a minimal current is consumed to maintain the store contents.

The M3540 recognises the on-hook condition when the hookswitch input (HSW) goes from logic '1' (the off-hook condition) to logic '0' for greater than 300ms. Short line voltage interruptions of less than 200ms, such as those created by the exchange during connection, will not be recognised by the M3540 as an on-hook indication.

The MASK output will go to logic '0' instantly whenever, and for as long as, the hookswitch input is at logic '0' in order to disconnect the speech circuit. This conserves current so that the store contents are not lost.

POWER-ON RESET

A Power-on Reset is internally generated when power is applied to the chip and causes the number store to be cleared.

LOOP DISCONNECT MODE

In this mode the $\overline{\text{MASK}}$ output is used to disable the speech circuit during dialling. The $\overline{\text{MASK}}$ output is at logic '0' during impulsing and interdigit pauses.

The IMP output signals a break to line when at logic '0' (V_{SS}). Make periods and I.D.P. times are signalled by logic '1' on the output. During the non-dialling period the impulsing output is at logic '0'. Timing of the output is shown below.

Figure 2 : Timing Diagram.

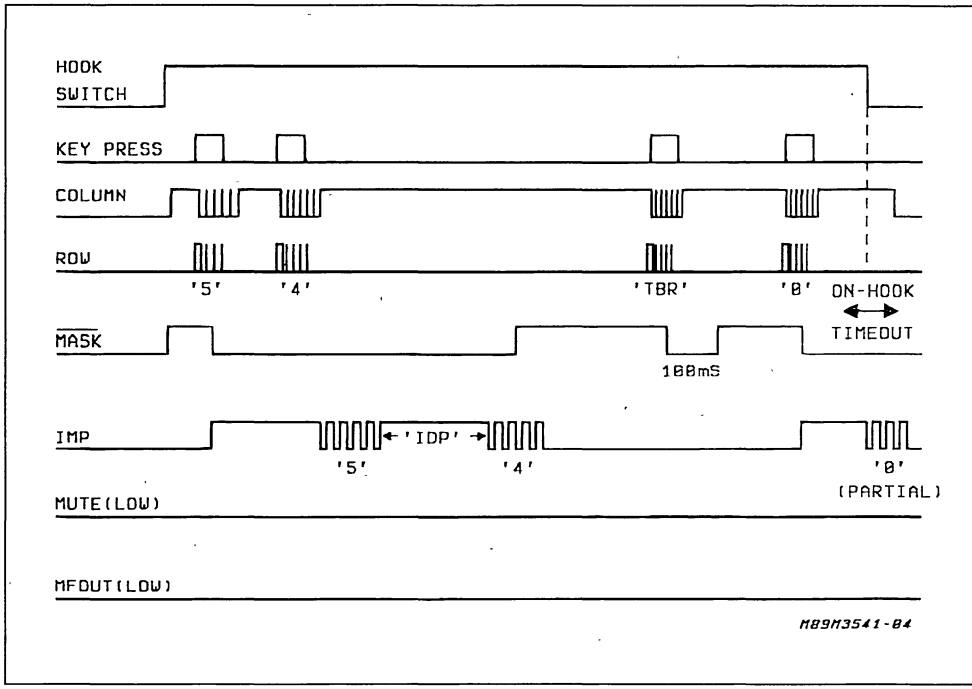
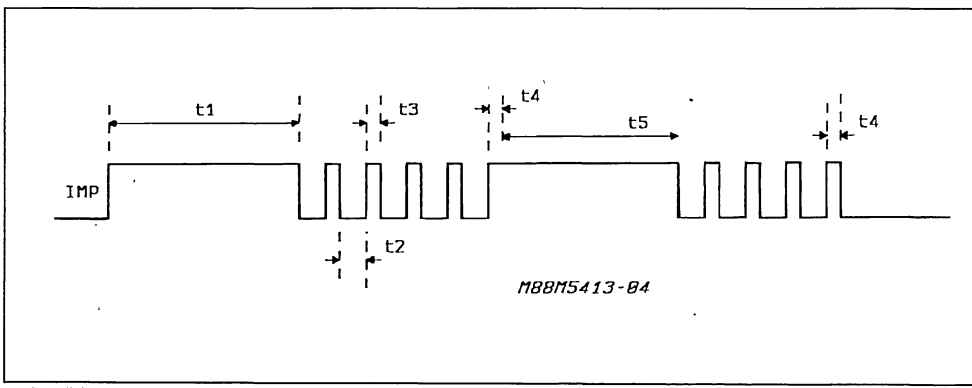


Figure 3 : Timing Data.



t_1 = Pre-digit pause (= t_5)
t_2 = Break period (60ms or 67ms)
t_3 = Make period (40ms or 33ms)
t_4 = Post-digit make (= t_3)
t_5 = Inter-digit pause (500 or 800ms)

DTMF MODE

The MUTE output goes to logic '1' when a key is activated and remains active for the duration of the tone transmission.

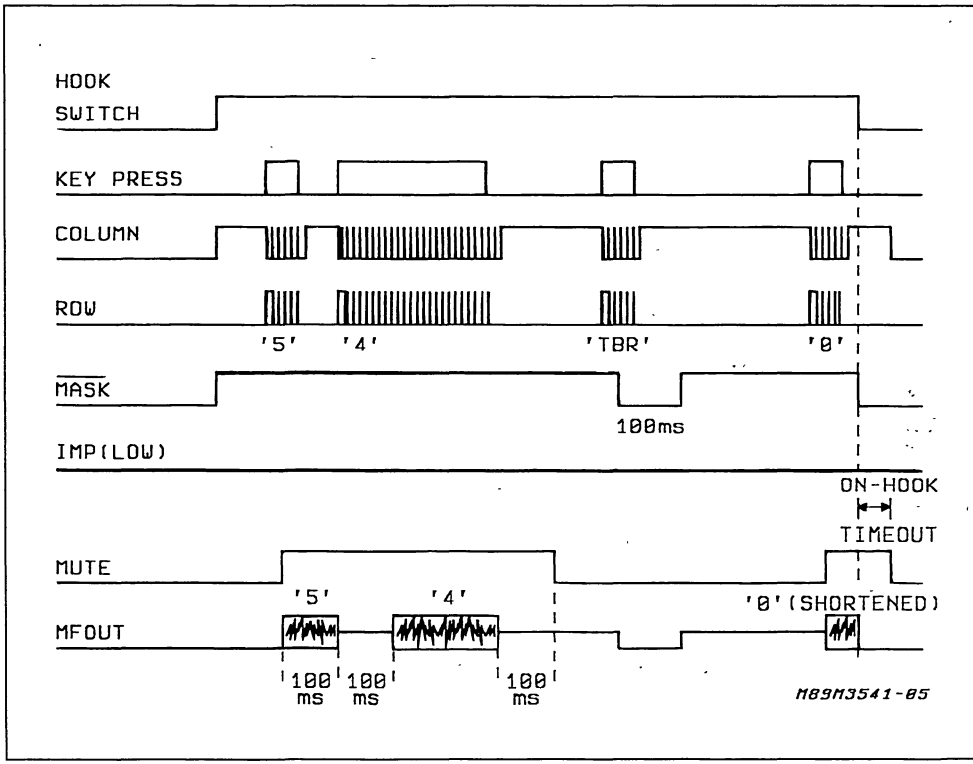
The tone rate will be 100ms on, 100ms off minimum.

TONE FREQUENCIES

Keypad	R1	R2	R3	R4	C1	C2	C3
Nominal Frequency (Hz)	697	770	852	941	1209	1336	1477
Deviation from Nominal (%)	– 0.07	– 0.10	– 0.19	– 0.15	– 0.17	– 0.20	– 0.22

There will be an additional error due to the deviation of the oscillator frequency from 560KHz.

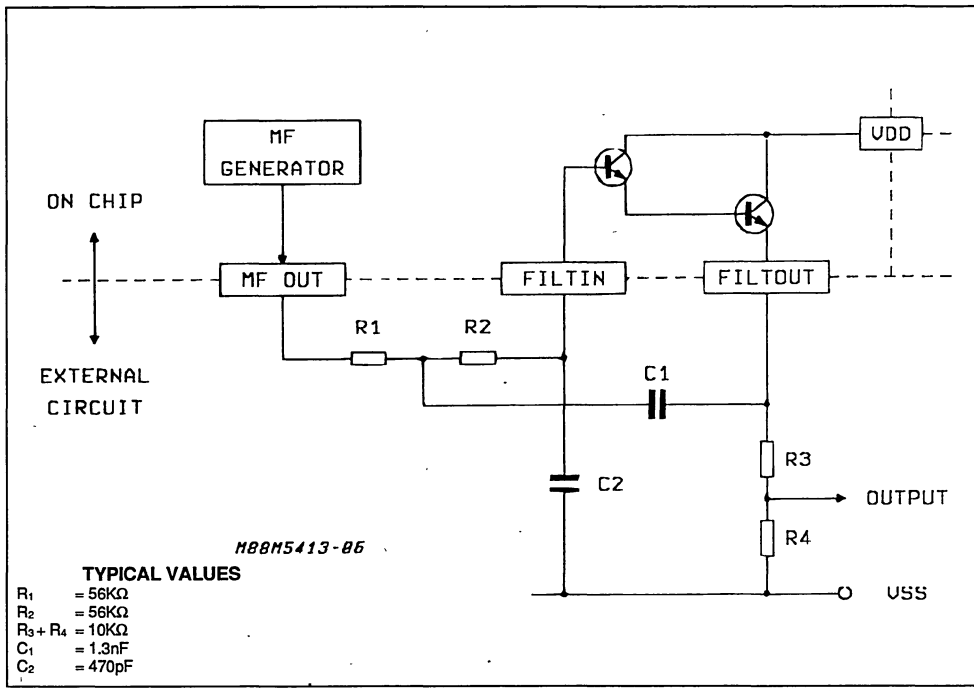
Figure 4 : Timing Diagram.



TONE OUTPUT

Facility has been made for tone filtering as shown below. This also allows the user to adjust tone amplitudes as required. The tone amplitude is proportional to the chip supply voltage, V_{DD}, and can be adjusted by changing the ratio of R_3 and R_4

Figure 5.



The filter components shown have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5KHz. The pass-band insertion loss is nominally 0.5dB.

DTMF APPLICATION CIRCUITS

The DTMF circuit in figure 2 uses a constant current supply and a 2.5V reference diode to produce the stabilised supply voltage which determines the MF tone level of the M3540. If the speech circuit provides a stabilised voltage, then figure 3 shows how it may be used to power the M3540 Diode D1 prevents the speech circuit from taking current whilst the telephone is on-hook, and D2 compensates for the voltage dropped across D1 when off-hook.

Figure 6.

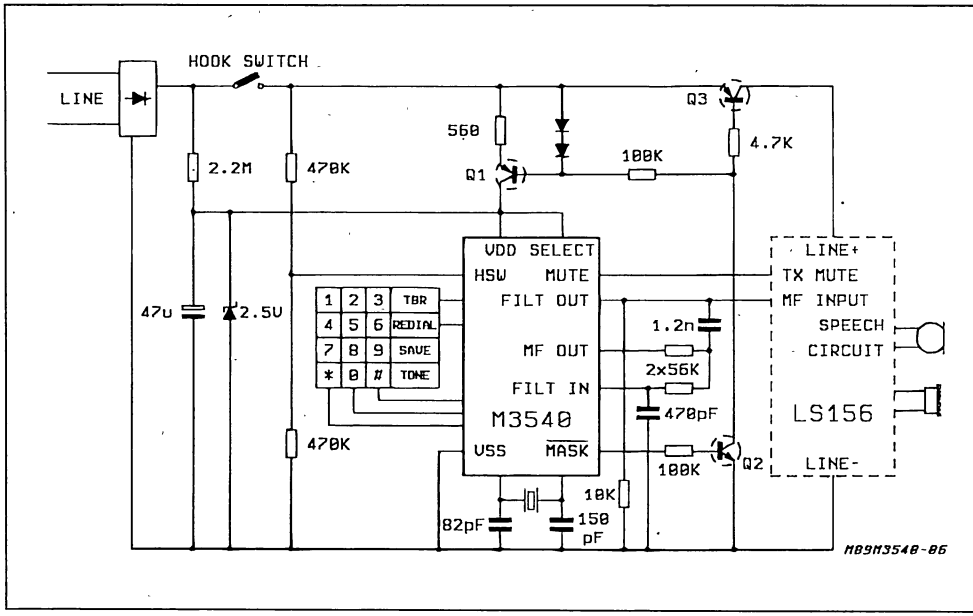
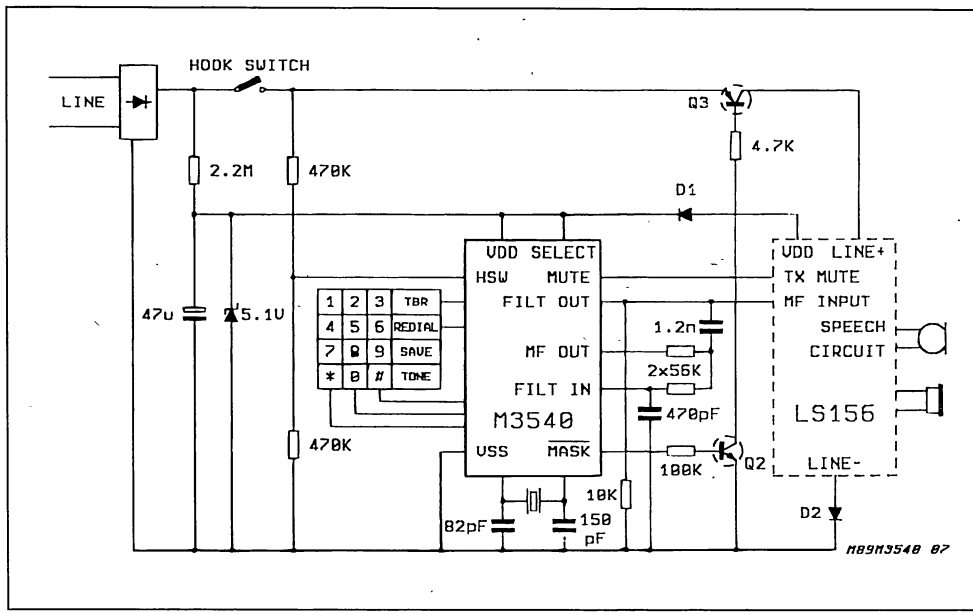


Figure 7.



SWITCHABLE LD/MF APPLICATION CIRCUITS

The circuit in figure 4 uses a constant current supply to take current from the telephone line which is used to power the M3540. The 2.5V reference diode produces a stabilised supply voltage which determines the MF tone level of the M3540.

In figure 5, a stabilising voltage from the speech cct is used to supply the M3540 during MF dialling to give accurate tone levels.

The M3540 is powered via the 150K resistor during TBR operations and LD dialling breaks, and via Q1 during dialling makes. This configuration minimises the component count at the expense of allowing a leakage current of about 450µA during dialling breaks. The 47µF reservoir capacitor maintains and smooths the supply to the chip.

Figure 8.

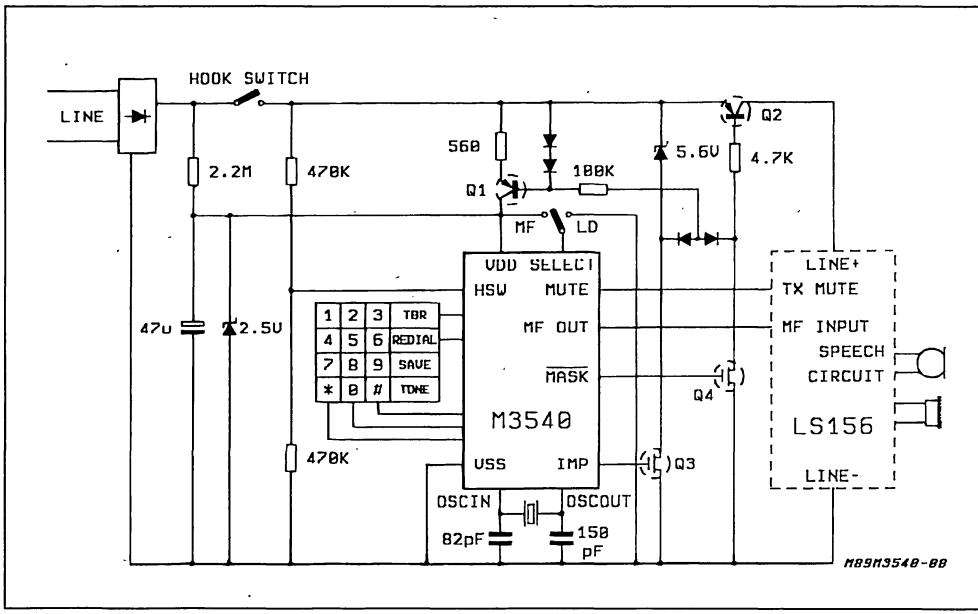
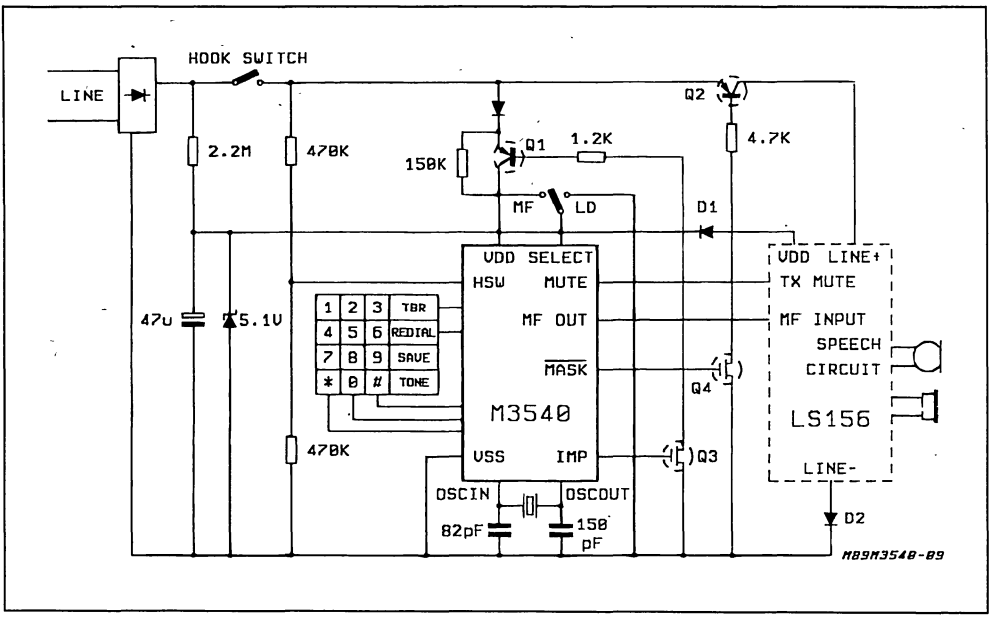


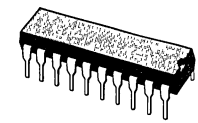
Figure 9.


HOOK SWITCH
LINE
2.2M
470K
150K
Q1
1.2K
Q2
4.7K
MF
LD
D1
VDD SELECT
HSW
MUTE
MF OUT
MASK
M3540
VSS
IMP
VDD LINE+
TX MUTE
MF INPUT
SPEECH
CIRCUIT
LS156
LINE-
Q4
Q3
D2
47u
5.1V
1 2 3 TBR
4 5 6 REDIAL
7 8 9 SAVE
* 0 # TONE
470K
OSCIN
OSCOUT
82pF
150 pF
MB9M3540-09

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

PRELIMINARY DATA

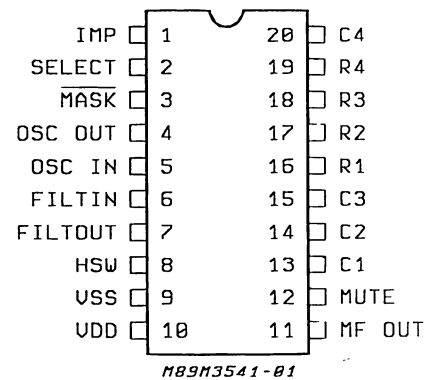
- SELECTABLE LOOP DISCONNECT OR DTMF DIALLING MODES
- ALLOWS USER TO SWITCH FROM LD TO DTMF DIALLING DURING A CALL
- LNR FACILITY ALLOWS UP TO 32 DIGITS TO BE RETAINED FOR REDIALLING
- SELECTABLE MAKE/BREAK RATIOS 2:1 AND 3:2
- SELECTABLE INTERDIGIT PAUSE 500ms OR 800ms
- USES INEXPENSIVE 560KHz RESONATOR
- TIMED BREAK RECALL (timed flash)
- OPERATES WITH INEXPENSIVE SINGLE CONTACT KEYPAD
- CAPABLE OF BATTERY-LESS OPERATION. LOW POWER CMOS PROCESS ALLOWS DIRECT OPERATION FROM TELEPHONE LINES



DIP20

ORDER CODE : M3541B

PIN CONNECTION



M89M3541-01

DESCRIPTION

The M3541 is a keypad switchable LD/DTMF dialer devices designed for use in low cost, dual dialing mode telephone instruments. It is suitable for sending telephone numbers without limit and an on-chip memory allows numbers of up 32 digits to be retained for redialling later. The low power CMOS design allows the number in the memory to be maintained indefinitely (until overwritten) by a minimal current leaked from the telephone line. A particular feature of this device is the facility for the user to switch dialling mode from LD to DTMF via the keypad during the course of a call. This is intended for uses such as home banking, access to long distance trunk service, credit card verificatios and other applications which require data to be sent at low speed once a connection has been established.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
	Supply Voltage V_{DD} - V_{SS}	– 0.3		6.5	V
	Voltage on any Pin Except HSW Voltage on any Pin HSW (current limited to < 100µA)	V_{SS} – 0.3 V_{SS} – 0.3		V_{DD} + 0.3	V V
	Current at any Pin Except FILTOUT and FILTIN Current at Pin FILTIN Current at Pin FILTOUT	– 1 0 – 5		+ 1 0.1 0	mA mA mA
	Operating Temperature Storage Temperature	– 10 – 55		+ 55 + 125	°C °C

* Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

D. C. ELECTRICAL CHARACTERISTICS

(at 2.5V, 25°C unless otherwise stated)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
	Supply Voltage - Off-hook Supply Voltage - On-hook	2.5 2.0		5.5 5.5	V V
	Supply Current - On-hook at 2.0V Supply Current - Off-hook (idle)		 1.5	1000 15.0	nA µA
	Supply Current - MF tone sending Supply Current - LD impulsing			1.0 200	mA µA
	Hookswitch Input - On-hook Hookswitch Input - Off-hook	 0.8 V_{DD}		0.2 V_{DD}	
	$\overline{MASK}$, MUTE and IMP Outputs, Load – 1mA $\overline{MASK}$, MUTE and IMP Outputs, Load + 1mA	2.2		 0.3	V V
	MF OUT D.C. Level During Tone Sending		0.9 V_{DD}		
	MF OUT Output Resistance		3		kΩ
	Darlington Pair Current Gain at I_E = 100µA, V_{CE} = 2V	 600			

A. C. ELECTRICAL CHARACTERISTICS

(at V_{DD} = 2.5V, 25°C unless otherwise stated)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
	Tone Amplitude Low Group Tone Amplitude High Group } no Load	57	64 81	 91	mVrms mVrms
	Ratio of High to Low Group Amplitude	1.5	2	2.5	dB
	Total Harmonic Distortion : 0 - 4 kHz 0 - 10 kHz 0 - 50 kHz 0 - 200 kHz		2 2.5 5 6.5	 10	% % % %

PIN FUNCTIONS

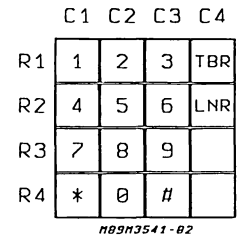
Pin Name	Function
ROW 1 ROW 2 ROW 3 ROW 4 COL 1 COL 2 COL 3 COL 4	Connections for 16 Buttons, Single Contact Keyboard
V_{DD}	Positive Supply
V_{SS}	Negative Supply
SELECT	LD/MF Selection, IDP and B/M Ratio Programming
OSCIN OSCOUT	Oscillator Connection
HSW	Hookswitch. A logic '1' voltage at this pin is used to indidcate 'off-hook'.
$\overline{MASK}$	Output to disable speech circuit during pulse dialling and recall (see note 1).
IMP	'Loop Disconnect' Dialling Output
MF OUT	Unfiltered, Dual Tone Output
FILTOUT FILTIN	Unity Gain Amplifier Input and Output for 2-pole Filter
MUTE	Output Active During Keying and Tone Transmission (see note 2)

Notes : 1. The $\overline{MASK}$ output may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook, during a TBR (Timed Flash) operation or for LD dialling.
2. The MUTE output is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

KEYPAD OPERATION

The device will accept keypad inputs only in the 'off-hook' condition when the key is pressed for more than 14ms. Any key pressed during the 'on-hook' condition will be ignored and the oscillator inhibited. This ensures that the current drain 'on-hook' is low and used only for memory retention.

KEYPAD FORMAT



LNR = Redial digits in "LNR"store

TBR = Timed Break Recall (timed flash)

LD/DTMF MODE SELECTION

The initial dialling mode after the telephone goes off-hook is determined as follows :

DTMF - Connect SELECT pin to V_{DD}

LD -

Option		Connect SELECT pin to :
IDP	B/M Ratio	
800ms	2:1	V_{SS}
500ms	2:1	COL 1
500ms	3:2	COL 2
800ms	3:2	COL 3

LD dialling is at 10 i.p.s. for all options

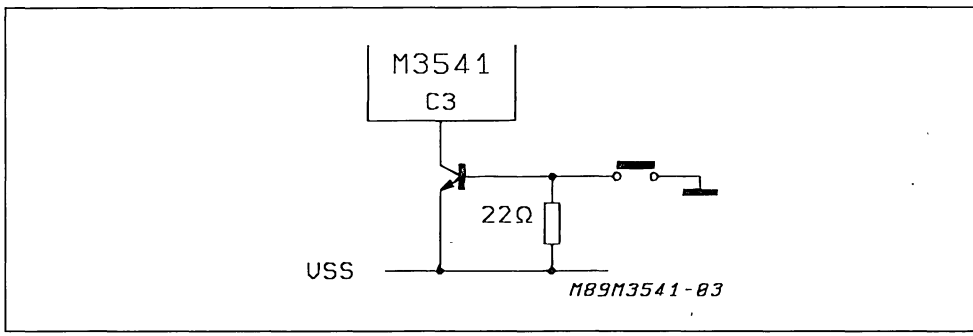
KEYPAD LD/DTMF MODE CHANGE

If the initial dialling mode is LD, pressing either the * or # key will cause all subsequently entered digits to be dialled in DTMF. The first press of either * or # will not cause a digit to be dialled, but once in MF mode, pressing * or # will cause the appropriate tone pair to be transmitted.

If the TBR (Timed Flash) key is pressed, or an Earth Loop Recall operation is signalled to the chip, further dialling is set to the initial mode.

In order to signal an ELR operation to the chip, the following configuration should be adopted :

Figure 1.



LAST NUMBER REDIAL

The function of the Last Number Redial store is to automatically retain the last number dialled so that it can be redialled later simply by pressing the LNR key. Either LD or MF numbers will be retained in the store. When numbers containing an LD part followed by an MF part are dialled, only the LD part will be retained in order that security codes, etc., dialled in MF are not automatically stored.

To redial a number, go off-hook and press LNR once. Alternatively, digits may be keyed manually before LNR is pressed. If the digits keyed correspond with the first digits in the LNR store, the remaining digits will be automatically redialled when LNR is pressed (this feature allows manual keying of an access code followed by a pause before dialling out the rest of the number). If, however, a digit is keyed which differs from the corresponding digit in the stored number, then redialling is inhibited.

HOOKSWITCH OPERATION

The hookswitch input is used to inform the M3541 of whether the telephone is on- or off-hook. When the telephone is on-hook the M3541 will adopt a static low power mode in which dialling functions are inhibited and only a minimal current is consumed to maintain the store contents.

The M3541 recognizes the on-hook condition when the hookswitch input (HSW) goes from logic '1' (the off-hook condition) to logic '0' for greater than 300ms. Short line voltage interruptions of less than 200ms, such as those created by the exchange during connection, will not be recognized by the M3541 as an on-hook indication.

The MASK output will go to logic '0' instantly whenever, and for as long as, the hookswitch input is at logic '0' in order to disconnect the speech circuit. This conserves current so that the store contents are not lost.

POWER-ON RESET

A Power-on Reset is internally generated when power is applied to the chip and causes the number store to be cleared.

LOOP DISCONNECT MODE

In this mode the $\overline{\text{MASK}}$ output is used to disable the speech circuit during dialling. The $\overline{\text{MASK}}$ output is logic '0' during impulsing and interdigit pauses.

The IMP output signals a break to line when at logic '0' (VSS). Make periods and I.D.P. times are signalled by logic '1' on the output. During the non-dialling period the impulsing output is at logic '0'. Timing of the output is shown below.

Figure 2. : Timing Diagram

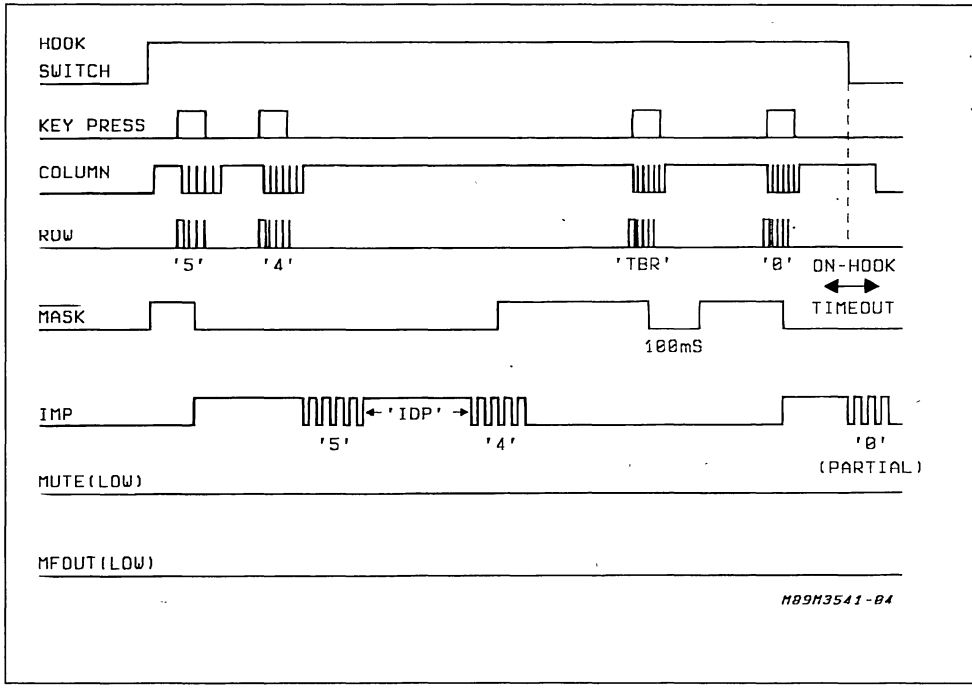
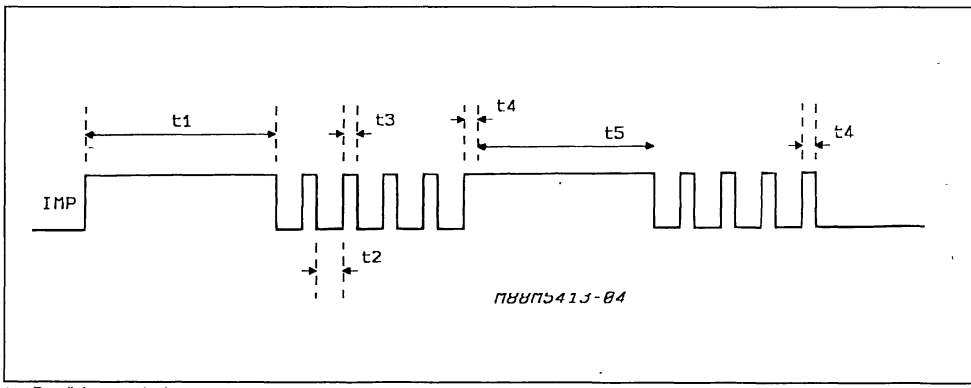


Figure 3. : Timing Data



t_1 = Pre-digit pause (=t_5)
t_2 = Break period (60ms or 67ms)
t_3 = Make period (40ms or 33ms)
t_4 = Post-digit make (= t_3)
t_5 = Inter-digit pause (500 or 800ms)

DTMF MODE

The MUTE output goes to logic '1' when a key is activated and remains active for the duration of the tone transmission.

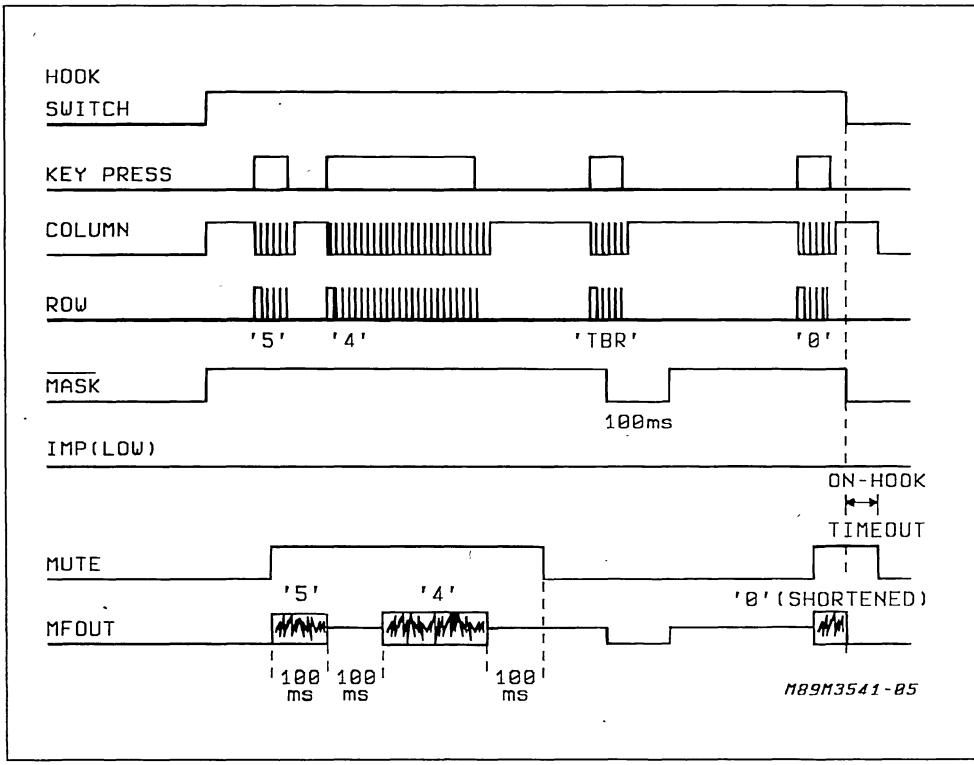
The tone rate will be 100ms on, 100ms off minimum.

TONE FREQUENCIES

Keypad	R1	R2	R3	R4	C1	C2	C3
Nominal Frequency (Hz)	697	770	852	941	1209	1336	1477
Deviation from Nominal (%)	– 0.07	– 0.10	– 0.19	– 0.15	– 0.17	– 0.20	– 0.22

There will be an additional error due to the deviation of the oscillator frequency from 560KHz.

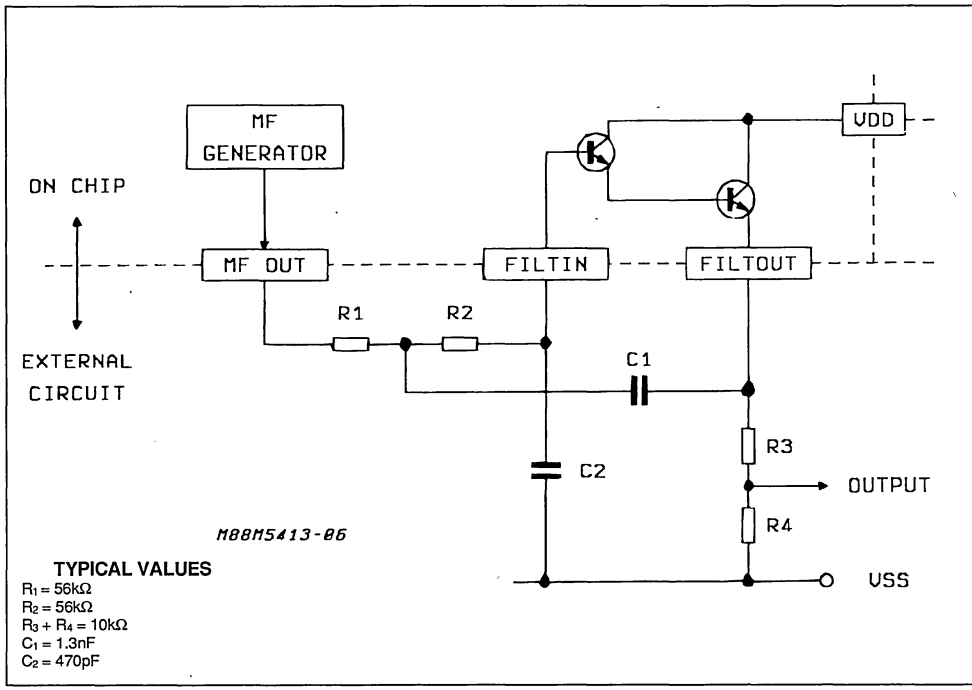
Figure 4 : Timing Diagram.



TONE OUTPUT

Facility has been made for tone filtering as shown below. This also allows the user to adjust tone amplitudes as required. The tone amplitude is proportional to the chip supply voltage, V_{DD}, and can be adjusted by changing the ratio of R3 and R4.

Figure 5.



The filter components shown have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5KHz. The pass-band insertion loss is nominally 0.5dB.

DTMF APPLICATION CIRCUITS

The DTMF circuit in figure 6 uses a constant current supply and a 2.5V reference diode to produce the stabilised supply voltage which determines the MF tone level of the M3541. If the speech circuit provides a stabilised voltage, then figure 7 shows how it may be used to power the M3541. Diode D1 prevents the speech circuit from taking current whilst the telephone is on-hook, and D2 compensates for the voltage dropped across D1 when off-hook.

Figure 6.

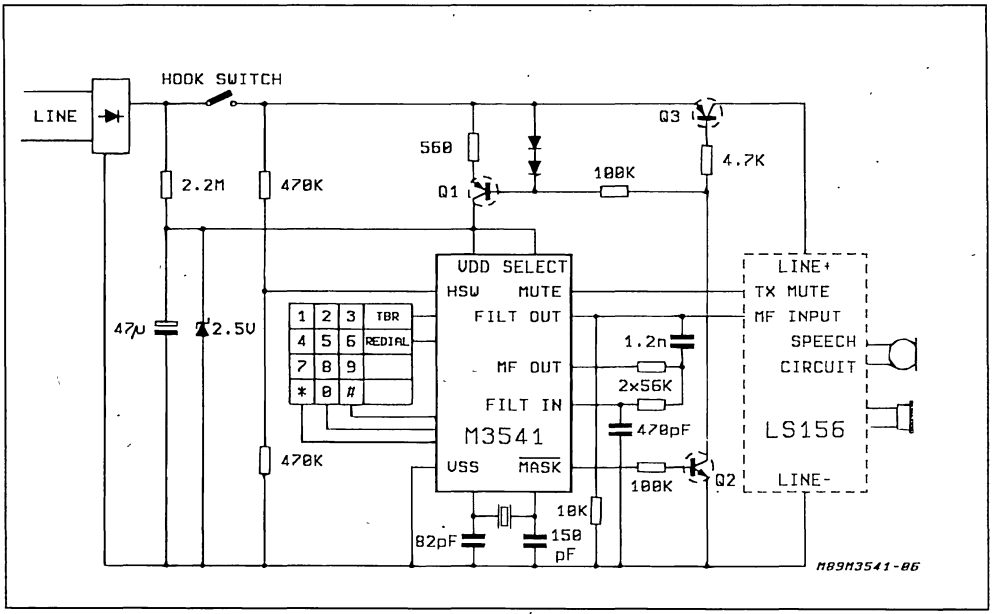
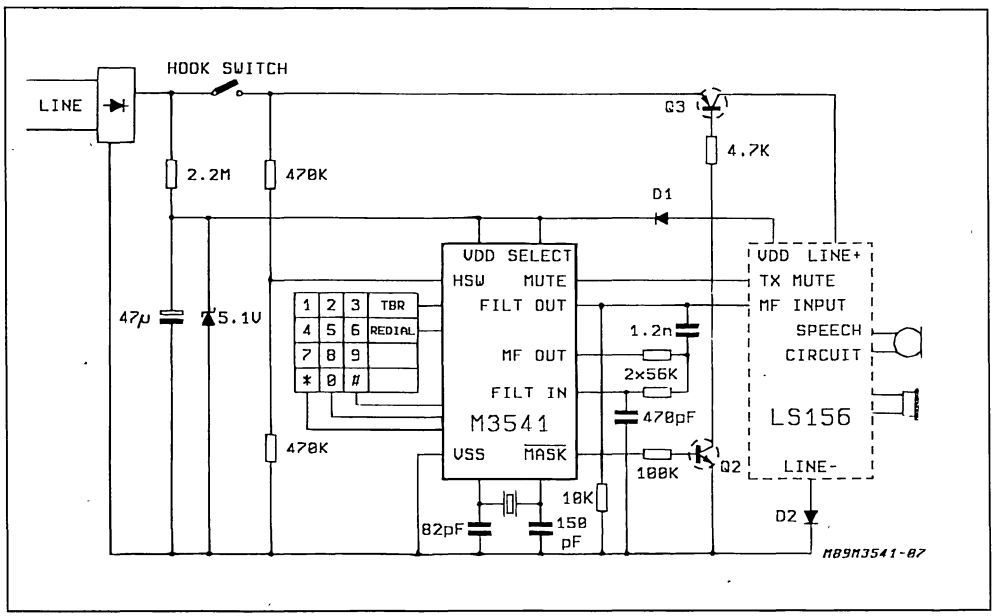


Figure 7.



SWITCHABLE LD/MF APPLICATION CIRCUITS

The circuit in figure 8 uses a constant current supply to take current from the telephone line which is used to power the M3541. The 2.5V reference diode produces a stabilised supply voltage which determines the MF tone level of the M3541.

In figure 9, a stabilising voltage from the speech is used to supply the M3541 during MF dialling to give accurate tone levels.

The M3541 is powered via the 150K resistor during TBR operations and LD dialling breaks, and via Q1 during dialling makes. This configuration minimises the component count at the expense of allowing a leakage current of about 450µA during dialling breaks. The 47µF reservoir capacitor maintains and smooths the supply to the chip.

Figure 8.

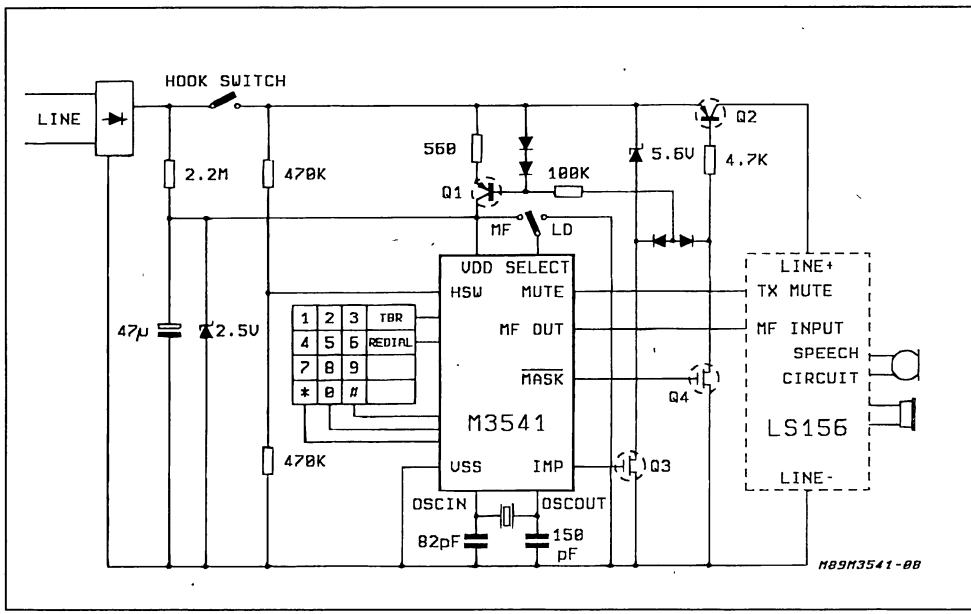
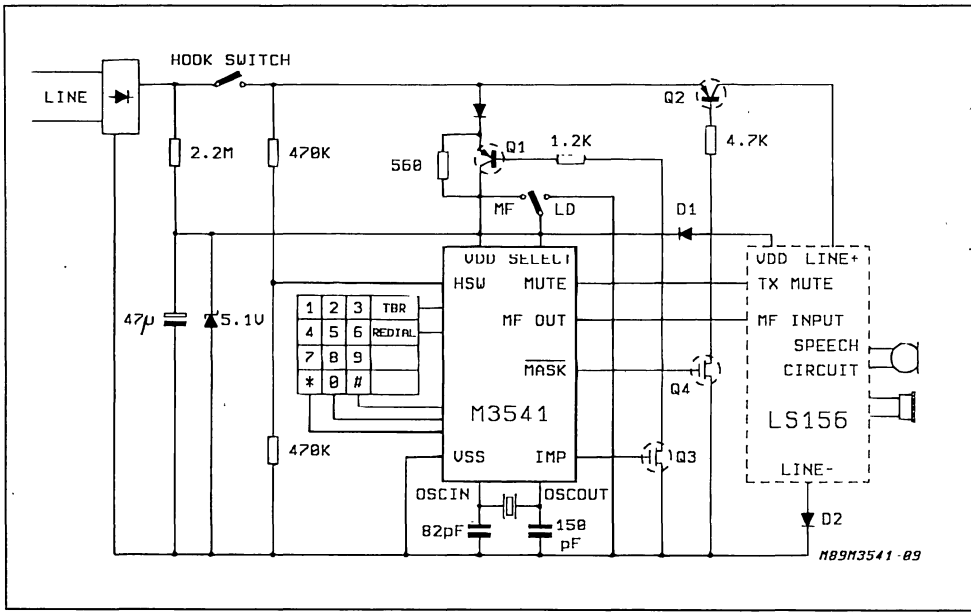
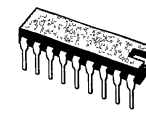


Figure 9.


HOOK SWITCH
LINE
2.2M
470K
560
Q1
1.2K
Q2
4.7K
MF
LD
D1
VDD SELECT
HSW
MUTE
MF OUT
MASK
M3541
VSS
IMP
OSCIN
OSCOUT
82pF
150 pF
47µ
5.1V
1 2 3 TBR
4 5 6 REDIAL
7 8 9
* 0 #
470K
Q4
Q3
VDD LINE+
TX MUTE
MF INPUT
SPEECH CIRCUIT
LS156
LINE-
D2
M89M3541-09

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

- STAND-ALONE DTMF AND PULSE SIGNALING
- RECALL OF LAST NUMBER DIALED (up to 28 digits long)
- FORM-A AND 2-of -7 KEYBOARD INTERFACE
- PACIFIER TONE
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS



DIP18

ORDER CODE : MK5370N00

DESCRIPTION

The MK5370 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK5370 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and redial them using either the *or # as the first key entry after going off-hook.

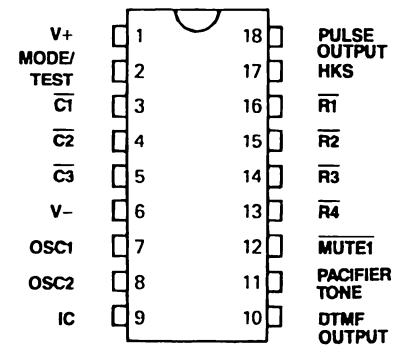
A *or # key input automatically redials the last number dialed if it is the first key entered after a transition from on-hook to off-hook (HKS input switched from a high to low logic level). Auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed, however these inputs are not stored into memory.

KEYPAD CONFIGURATION

1	2	3
4	5	6
7	8	9
* LND	0	# LND

M88MK5370-01

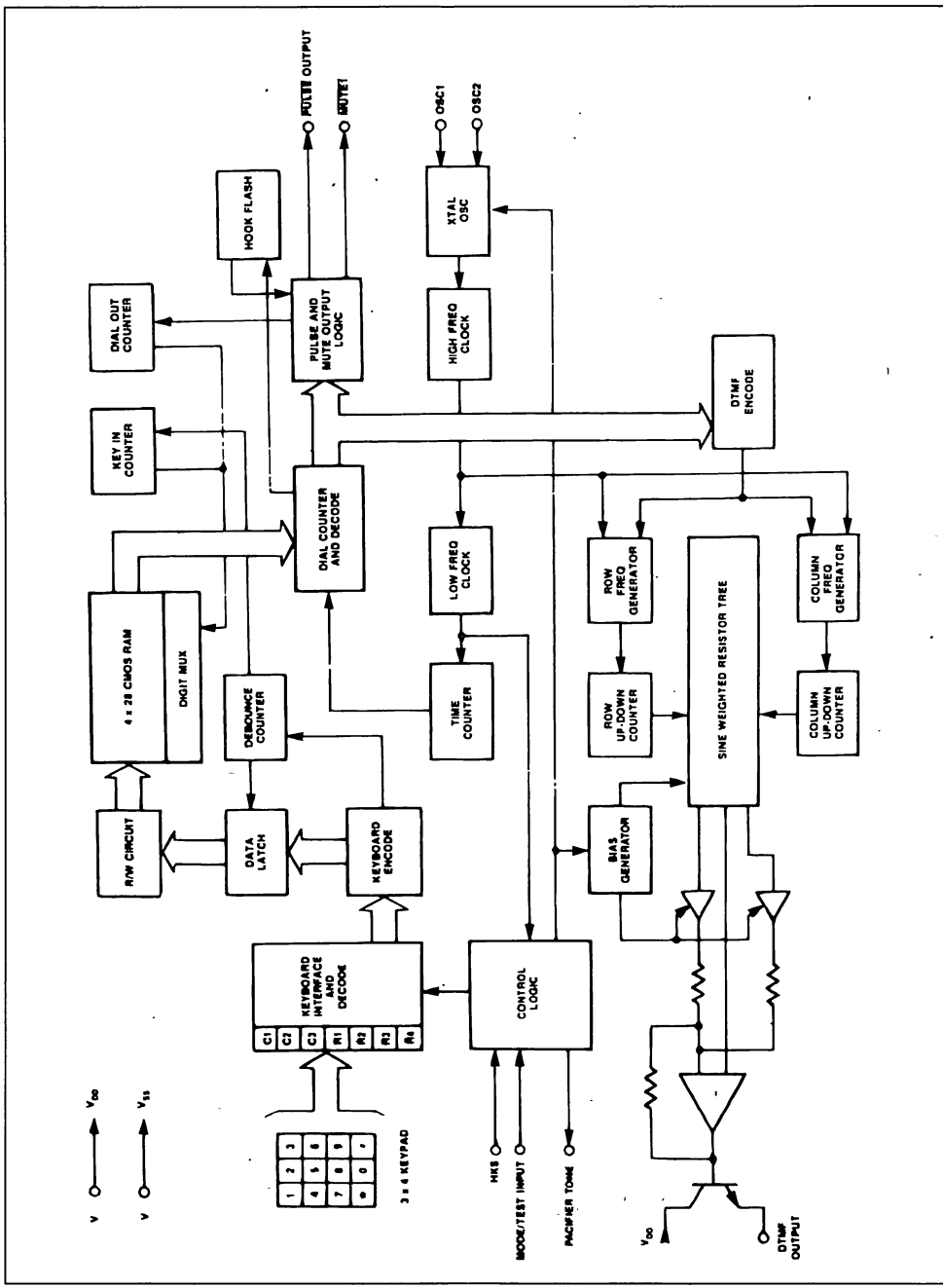
PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS *

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	0 to + 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	(V+) + 0.3, (V–) – 0.3	V

BLOCK DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwwise stated.

DC CHARACTERISTICS

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	V+	DC Operating Voltage (all functions)	2.5		6.0	V	
	V_{MR}	Memory Retention Voltage	1.5			V	1, 6
	I_S	Standby Current		0.2	1.0	µA	1
	I_{MR}	Memory Retention Current		0.1	0.75	µA	5, 6
	V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
	I_T	Operating Current (tone)		300	600	µA	2
	I_P	Operating Current (pulse)		225	350	µA	2
	I_{ML}	Mute Output Sink Current (V+ = 2.5 V)	1.0	2.0		mA	3
	I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
	I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
	K_{RU}	Keypad Pull-up Resistance		100		kΩ	
	K_{RD}	Keypad Pull-down Resistance		750		Ω	
	V_{IL}	Keypad Input Level-low	0		0.3 V+	V	
	V_{IH}	Keypad Input Level-High	0.7 V+		V+	V	

Notes :
1. All inputs unloaded Quiescent Mode (oscillator off).
2. All outputs unloaded single key input.
3. V_{OUT} = 0.4 Volts
4. Sink Current for V_{OUT} = 0.5 volts. Source Current for V_{OUT} = 20 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum supply voltage where activation of mute output with key entry is ensured.

AC CHARACTERISTICS – KEYDAP INPUTS, PACIFIER TONE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
3	T_{KD}	Keypad Debounce Time		32		ms	1
–	F_{KS}	Keypad Scan Frequency		250		Hz	1
–	T_{RL}	Two Key Rollover Time		4		ms	1
–	F_{PT}	Frequency pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1

Notes : 1. Crystal oscillator accuracy directly affects these times.

AC CHARACTERISTICS – PULSE MODE OPERATION

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
–	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		40		ms	2
6	IDP	Interdigital Pause		940		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2

Notes : 1. 10 PPS is the nominal rate.
2. Figure 5 illustrates this relationship.

ELECTRICAL OPERATING CHARACTERISTICS (continued)

AC CHARACTERISTICS – TONE MODE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
–	T_{NK}	Tone Output No Key Down			– 80	dBm	1
–	T_{0d}	Tone Output (dependent)	– 13 – 173	– 12 194	– 11 218	dBm mV_{rms}	1, 2 5
–	PE_d	Pre-emphasis, High Band	2.3	2.7	3.1	dB	
–	DC_d	Tone Output DC Bias (V+ = 2.5)	1.0	1.2		V	
–	R_E	Tone Output Load			10	kΩ	5
–	T_{RIS}	Tone Output Rise Time		0.1	1.0	ms	6
–	DIS	Output Distortion		5.0	8.0	%	3
–	T_X	Tone Signaling Rate		5.0		1/sec	
1	T_{PSD}	Pre-signal Delay		100		ms	7
2	T_{ISD}	Inter-signal Delay		100		ms	

Notes : 1. 0 dBm equals 1mW power into 600 ohms or 775 mVolts.
Important Note : The mk5370 is designed to drive a 10 Kohms load. The 600 ohms load is only for reference.
2. Single tone (low group). varies when used in subscriber set.
3. Supply voltage ? 2.5 to 6 Volts. R_E=10 kohms.
4. R_E = 10 Kohms.
5. Supply voltage = 2.5 Volts. These specifications are supply-dependent.
6. Time from beginning of tone output waveform to 90 % of final magnitude of either frequency Crystal parameters suggested for proper operation are R_S = 1000 ohms L_m = 96 mH C_m = 0.2 pF C_m= 5pF f = 3.579545 MHz and C_1 = 18 pF.
7. Time from initial key input until beginning of signaling.

FUNCTIONAL DESCRIPTION

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see Electrical Specifications).

MODE/TEST

Input. Pin 2. MODE/TEST determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook (V+) to off-hook (V–) the default determines the signaling mode. A V+ connection selects to pulse mode operation.

Pin 2 also forces the device into test mode.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard Input. Pins 3, 4, 5, 13, 14, 15, 16. The MK5370 interfaces with either the standard 2-of-7 with negative common or the inexpensive single-contract (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator to begin scanning the keypad. Scanning consists of Rows and Columns alternately switching high through on-chip pull-ups.

After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (Tdb) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs all pull high through on-chip pull-up resistors.

IC

Input. Pin 9 Internal connection. This pin should be left during for normal operation.

V–

Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Input/Output. Pins 7, 8. OSC1 and OSC2 are inputs to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions.

DTMF OUTPUT

Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 4 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 1. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK5370 is designed to operate from a regulated supply and the row (low group) TONE LEVEL is related to this supply by either of the following equations :

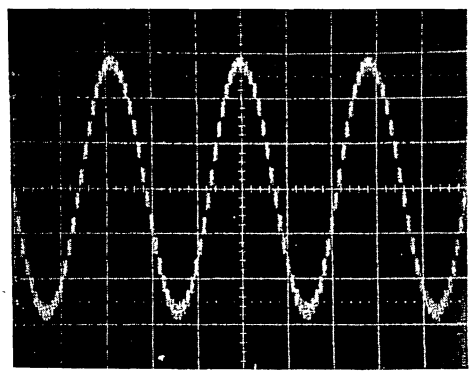
$T_{O1} = 20 \text{ LOG } [(0.0776 \text{ V+}) / 0.775] \text{ dBm}$

$T_{O1} = 0.0776 \text{ (V+) VRMS}$

The DC component of the DTMF output while active is described by the following equation :

$V_{DC1} = 0.66 \text{ V} + -0.6 \text{ Volts}$

Figure 1 : Single Tone.



PACIFIER TONE OUTPUT

Output. Pin 11. A 500 Hz square wave is activated on pin 11 upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, only a redial entry activates the pacifier tone. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted.

Figure 2 : Dual Tone.

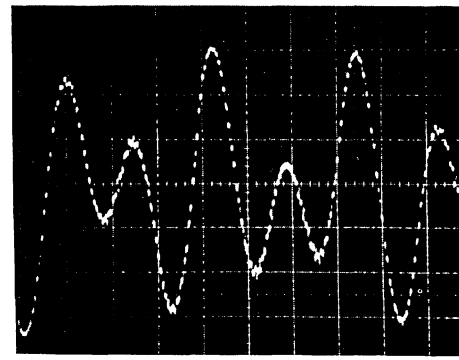
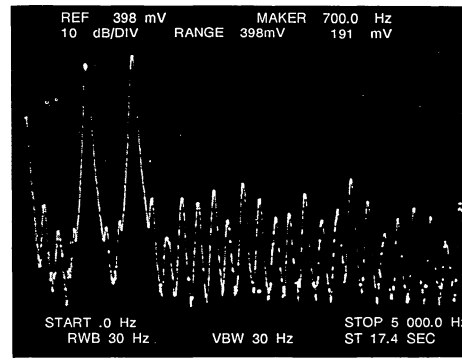


Figure 3 : Spectral Reponse.



MUTE1

Output. Pin 12. This pin is the Mute Output for both tone and pulse modes. Timing is dependent upon mode.

The output consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pull-up resistor to the positive supply.

In tone mode, $\overline{\text{MUTE1}}$ removes the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE1}}$ is active continuously until dialing is completed.

In pulse mode, $\overline{\text{MUTE1}}$ removes the receiver or the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE1}}$ timing is shown in Figure 5 for pulse mode signaling and Figure 4 for tone mode signaling.

HKS

Input. Pin 17. Pin 17 is the hookswitch input to the MK5370. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2.

$\overline{\text{PULSE}}$ OUTPUT

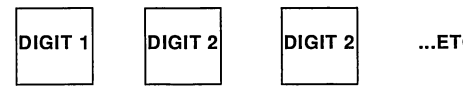
Output. Pin 18. This pin has a dual function determined by the dialing mode selected. In Pulse Mode, the pin is an output consisting of an open drain N-channel device with zener protection. The break timing at this output meets Bell Telephone and EIA specifications for loop disconnect signaling. Figure 4 shows this timing.

DEVICE OPERATION (tone mode)

When the MK5370 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are pulled high. Key entries are not recognized unless they utilize a keypad common connection to force the respective Row and Column inputs low. These inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of 100 ms. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an intersignal time of 102 ms.

One important feature of the dialer is its ability to buffer data into the RAM before signaling. This feature allows less expensive keyboards to be used because signal distortion and double digit entry caused by bouncing and bounding of the keypad are eliminated. This design also ensures that data stored in the buffer exactly matches the digits actually dialed.

NORMAL DIALING (off-hook)



Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the * or # key as the first entry after coming off-hook.

Table 1 : DTMF Output Frequency.

Key Input	Standard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+ 0.31
2	770	766.2	– 0.49
3	852	847.4	– 0.54
4	941	948.0	+ 0.74
COL 1	1209	1215.9	+ 0.57
2	1336	1331.7	– 0.32
3	1477	1471.9	– 0.35

Figure 4 : Tone Mode Timing.

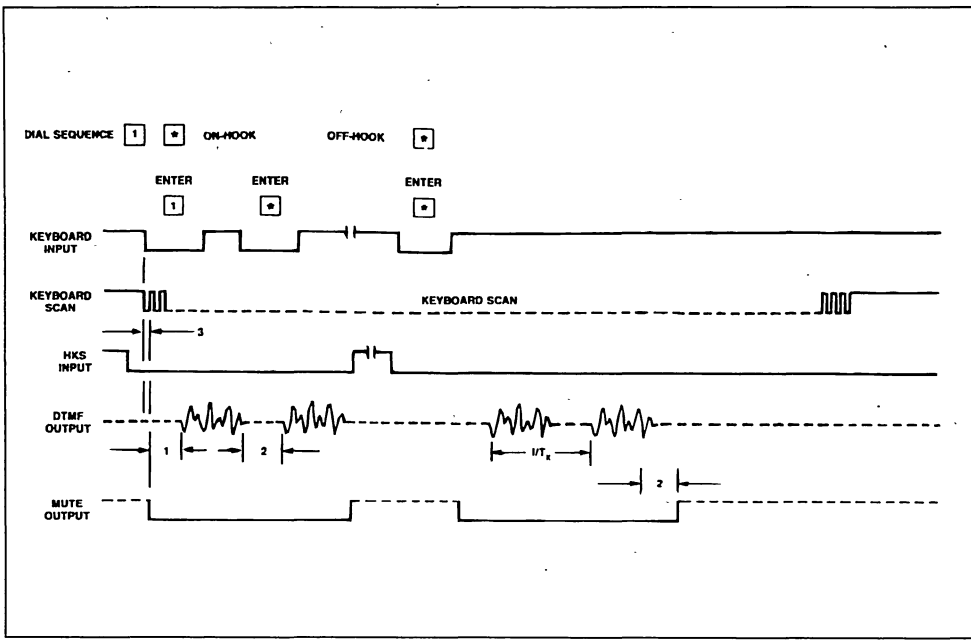


Figure 5 : Pulse Mode Timing.

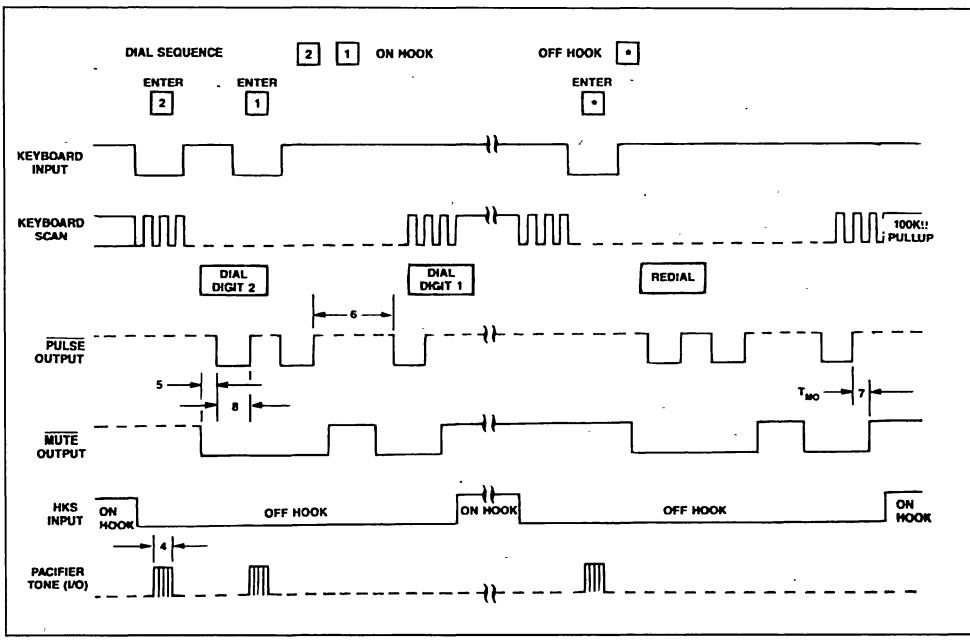
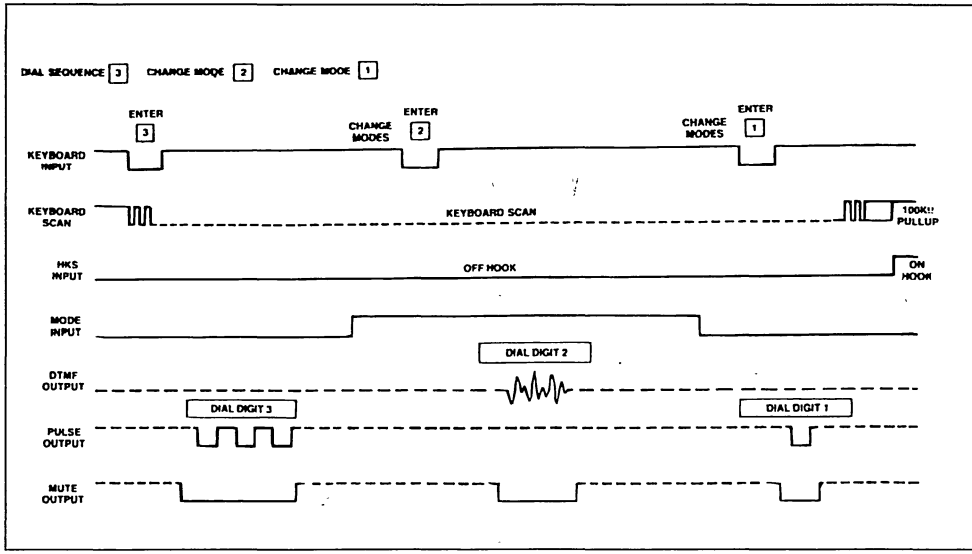


Figure 6 : Pulse and Tone Mode Timing.



TYPICAL APPLICATION

The MK5370 Pulse Tone dialer provides both cost-effective telephone-line interface and the logic required for DTMF (Tone) and Loop Disconnect (Pulse) signaling.

Pulse dialing originated with the rotary dial telephone. The MK5370 Pulse Tone dialer provides the same capability as the rotary dial telephone and the convenience of pushbutton entry. The subscriber set (telephone) is powered by loop current supplied by the telephone company. Signaling, in Pulse Mode, is accomplished by repeatedly interrupting the low current. The central office senses, times, and counts each line "break" ; the number of breaks corresponds to the digit dialed. The duration of the break period, the dialing rate, and the separation between consecutive digits (IDP time) are controlled by the Pulse Tone dialer IC. Loop disconnect dialing is nearly a world-standard concept.

DTMF signaling consists of modulating the telephone line with a signal comprised of two fundamental frequencies. Each frequency pair represents one of sixteen possible digit (or key) entries. Twelve of these frequency pairs are commonly used (0, 1, 2, ..., *, #). The MK5370 Pulse Tone dialer provides DTMF signalling capability controlling signal duration, separation, level, and rate.

The typical application circuit in Figure 7 illustrates one way the Pulse Tone dialer can be used. The pulse output provides the signal to break the line to transistor Q3. Q3 switches off, eliminating the base current to Q4, which also switches off. The majority of the loop current is then eliminated, resulting in a break condition. The IC dialer must be protected from large voltage fluctuations, such as that caused by interrupting the loop current. Transistor Q1 along with R2, C1, and Z1 regulate the voltage to the dialer. The Mute Output signal is active while signalling each digit to mute popping noises at the receiver (earpiece or speaker).

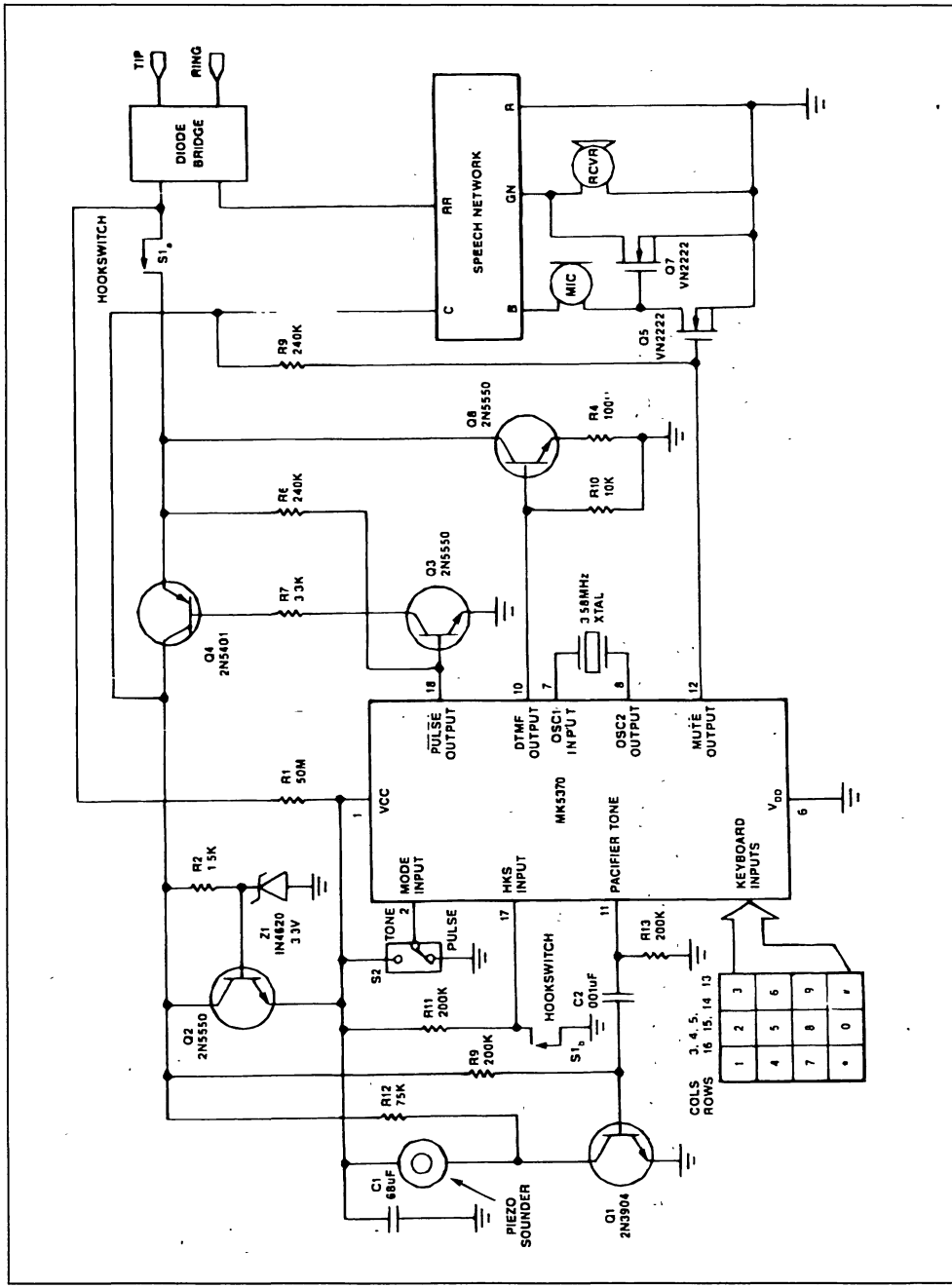
The DTMF tone output drives the base of Q8, which modulates the line. The tone level at tip and ring is determined by the effective impedance of the telephone line and the speech network.

Mode of operation is controlled by switch S1 (which sets the default dialing mode).

Resistor R1 provides a small memory-retention bias current to prevent the device from powering down while on hook. The current required for long term memory retention is less than 1μA.

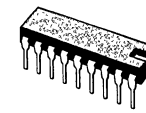
A ceramic sounder can also be interfaced to pin 11 (PACIFIER TONE) of the device. A pacifier tone signal is activated for each key entry in pulse mode. This feature provides an audible indication for each valid key entry. Keys may be entered faster than the maximum signalling rate allows. Audible feedback confirms proper key entry.

Figure 7 : MK5370 Typical Application.



SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

- STAND-ALONE DTMF AND PULSE SIGNALING
- SOFTSWITCH AUTOMATICALLY SWITCHES SIGNALING MODE
- RECALL OF LAST NUMBER DIALED (UP TO 28 DIGITS LONG)
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- MICROPROCESSOR INTERFACE (BDC INPUTS) FOR SMART TELEPHONES
- TIMED PABX PAUSE
- FORM-A AND 2-OF-8 KEYBOARD INTERFACE
- PACIFIER TONE
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS



DIP18

ORDER CODE : MK5371N00

KEYPAD CONFIGURATION

1	2	3	FLASH
4	5	6	MODE
/	8	9	PAUSE
*	0	#	LND

M88MK5371-01

DESCRIPTION

The MK5371 is a monolithic, integrated circuit manufactured using Silicon Gate CMOS process. These circuits provide necessary signals for either DTMF or loop disconnect (Pulse) dialing. The MK5371 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and access several unique special functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch (Mode), Flash, and Pause.

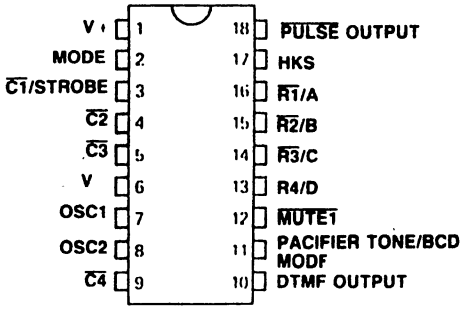
A LND key input automatically redials the last number dialed. Keys entered during auto-dialing sequence will not be stored or dialed. However, auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed.

The mode key simplifies the process of alternating dialing modes. This input automatically toggles the immediate dialing mode. The function is also stored in memory. During auto-redial, the signaling mode is toggled each time the Mode code appears in the digit sequence. The signaling mode always defaults to the mode selected (hardwire or switch) at Pin 2 (MODE) after a Power-Up-Clear initialization or a transition from on-hook to off-hook (HKS input switched from a high to low logic level). Switching modes through Pin 2 toggles the immediate dialing mode and changes the default, but it is not stored in memory.

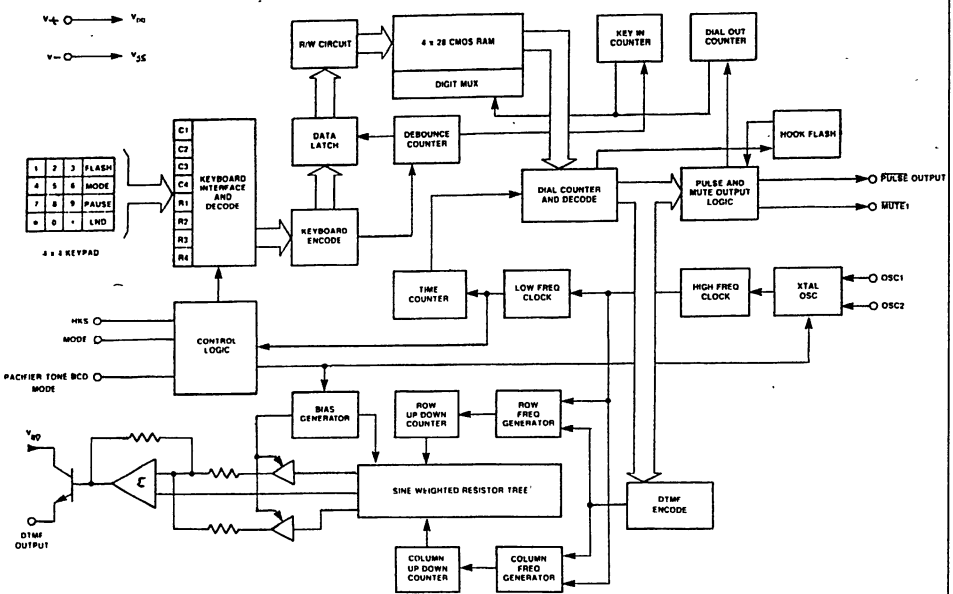
Two features simplify PABX dialing. The pause key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signaling resumes. The Flash key simulates a hook flash to transfer calls or to activate other special features provided by the PABX or a central office. The MK5371 ensures exact timing for the hook flash.

In addition to interfacing with standard keypads, the MK5371 also accepts parallel BCD inputs. This feature simplifies interfacing a microprocessor-based design to the telephone line. The MK5371 buffers 28 bytes of information, including special functions.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	– 30 to + 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on Any Pin	(V+) + 0.3, (V–) – 0.3	V

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device rehability.

ELECTRICAL OPERATING CHARACTERISTICS

(all specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated)

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+	DC Operating Voltage	2.5		6.0	V	
V_{MR}	Memory Retention Voltage	1.5			V	1, 6
I_S	Standby Current		0.2	0.750	µA	1
I_{MR}	Memory Retention Current		0,10	0.75	µA	5, 6
I_T	Operating Current (tone)		300	600	µA	2
I_P	Operating Current (pulse)		225	350	µA	2
I_{ML}	Mute Output Sink Current	1.0	2.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	keypad Pulldown Resistance		750		Ω	
V_{IL}	BCD/Keypad Input Level-low	0		0.2 V+	V	
V_{IH}	BCD/Keypad Input Level-high	0.7 V+		V+	V	

Notes : 1. All inputs unloaded. Quiescent Mode (oscillator off). V+ 2.5 V.
2. All outputs unloaded. Single key input.
3. V_{OUT} 0.5 Volts. V- 2.5 V.
4. Sink Current for V_{OUT} 0.5. Source Current for V_{OUT} 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.

AC CHARACTERISTICS - PULSE MODE OPERATION

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
P_R	Pulse Rate		10		PPS	
T_{PDP}	Predigital Pause		140		ms	1
T_{IDP}	Interdigital Pause		940		ms	1
T_{MO}	Mute Overlap Time		4		ms	1
T_B	Break Time		60		ms	1

Note : 1. Figure 6 illustrates this relationship.

ELECTRICAL OPERATING CHARACTERISTICS (continued)

AC CHARACTERISTICS - KEYPAD INPUTS, PACIFIER TONE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T_{KD}	Keypad Debounce Time		32		ms	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		ms	1
F_{PT}	Frequency Opacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone Duration		30		ms	1
T_{HFP}	Hookflash Timing		600		ms	1
F_{SR}	BCD Strobe Rate			124	1/sec	1
T_{DS}	Data Set up	2			µs	1
T_{DH}	Data Hold	1			µs	1
T_{ST}	Strobe Width	2		96000	µs	1
T_{SS}	Strobe Separation	9			ms	

Notes : 1. Crystal oscillator accuracy directly affects these times.
2. Figure 1 illustrates this timing relationship.

AC CHARACTERISTICS - TONE MODE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T_{NK}	Tone Output No Key Down			– 80	dBm	1
T_{Od}	Tone Output (dependent)	– 13 173	– 12 194	– 11 218	dBm mV_{rms}	1, 2 5
PE_d	Pre-Emphasis, High Band	2.3	2.7	3.1	dB	
DC_d	Tone Output DC Bias	1.0	1.2		V	4
R_E	Tone Output Load		10		KΩ	5
T_{RIS}	Tone Output Rise Time		0.1	1.0	ms	6
DIS	Output Distortion		5.0	8.0	%	3
TR	Tone Signaling Rate		5.0		1/sec	
T_{PSD}	Pre-signal Delay		100		ms	7
T_{ISD}	Inter-signal Delay		100		ms	

Notes : 1. O dBm equals 1 mW power into 600 ohms (775 mVolts). Important Note : The MK5371 is designed to drive a 10 kohm load. The 600 ohm load is only for reference.
2. Single tone (low group).
3. Supply voltage = 2.5 to 6 Volts. R_E = 10 kohms.
4. R_E = 10 k ohms. V+ = 2.5 Volts.
5. Supply voltage = 2.5 Volts. These specifications are supply-dependent.
6. Time from beginning of tone output waveform to 90 % of final magnitude of eitheir frequency. Crystal parameters suggested for proper operation are R_S < 100 Ω. L_m = 96 mH. C_m = 0.02 pF. C_h = 5 pF. f = 3.579545 MHz and C_L = 18 pF.
7. Time from Mute active to beginning of signaling.

FUNCTIONAL DESCRIPTION

The following pin descriptions are numbered according to the 24-pin package. Pin numbers for the 18-pin version are listed in parenthesis under each pin name.

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see Electrical Specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to Tone Mode operation and a V– connection defaults to Pulse Mode operation.

A Softswitch (Mode) code entered in a number sequence can temporarily modify the signaling mode. After encountering a first Softswitch code in a number sequence, the Signaling Mode toggles and is opposite the default determined by Pin 2. A second Softswitch toggles the Signaling Mode a second time, returning the mode back to the default condition. Note that the Softswitch code performs a toggle function on the default state ; switching the state of Pin 2 while dialing changes the default state as well as the immediate signaling mode.

$\overline{C1}$/STROBE, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard input. Pins 3, 4, 5, 9, 13, 14, 15, 16. The MK5371 interfaces with standard keypads as well as a microprocessor-driven 4-bit bus.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (boucing contacts, etc.) is ignored for a debounce period (Tdb) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information is valid, the information is buffered into the LND location. If switched on-hook, the keyboard inputs all pull high through on-chip pull-up resistors. Information may still be entered into memory but it is not signaled and the keyboard scan is disabled. If users desire to enter data while on-hook, a 2-of-8 keypad with negative common is required.

A key entry during LND interrupts the sequence when it reaches the redial period until the key is released. Dialing then resumes. The key entered is not stored or dialed.

The keyboard inputs become high impedance when the Binary Input Mode is selected. As shown in Table 1, Row pins become inputs for the Binary codes from a microprocessor in this mode. Table 1 equates the Binary Codes to the keyboard digits and special functions. The $\overline{C1}$ input pin now provides an input for a strobe strobe used to clock the valid codes into the LND buffer. Dialing proceeds at the specified rates. The strobe duration must be active for at least 2 µs to ensure proper acceptance of the information. If the strobe remains high for longer than 96 ms false dialing may occur. A minimum of 8 ms must separate each strobe. Figure 1 illustrates the required strobe/data timing. Valid encoded signaling information must be present until the strobe goes low. Information entered during an on-hook operation is stored but signaling is inhibited. Changing between BCD and keyboard mode can only occur when the HKS input is high, or upon power-up. Caution, a power supply transient may be interpreted as a power-up condition, and the logic level on pin 11 at that time will be interpreted as a valid BCD/Keyboard selection.

V–

Input. Pin 6. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Input/Output. Pins 7, 8. OSC1 and OSC2 are inputs to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions.

Table 1 : Binary Input Codes.

D	C	B	A	KEYBOARD FUNCTION	D	C	B	A	KEYBOARD FUNCTION
0	0	0	0	0	0	0	0	0	8
0	0	0	1	1	0	0	0	1	9
0	0	1	0	2	0	0	1	0	*
0	0	1	1	3	0	0	1	1	#
0	1	0	0	4	0	1	0	0	MODE
0	1	0	1	5	0	1	0	1	PAUSE
0	1	1	0	6	0	1	1	0	FLASH
0	1	1	1	7	0	1	1	1	LND

Figure 1 : BCD Mode Strobe Interface Timing.

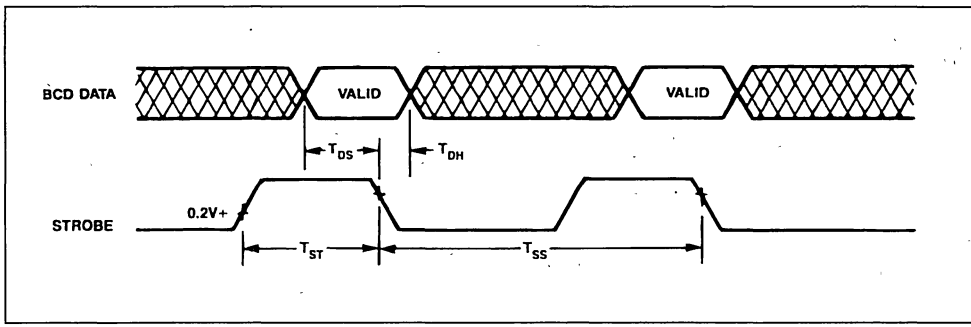


Table 2 : DTMF Output Frequency.

KEY INPUT	STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW 1	697	699.1	+ 0.31
2	770	766.2	– 0.49
3	852	847.4	– 0.54
4	941	948.0	+ 0.74
COL 1	1209	1215.9	+ 0.57
2	1336	1331.7	– 0.32
3	1477	1471.9	– 0.35

DTMF OUTPUT

Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column Tones together. Figure 4 shows the timing at this pin.

PACIFIER TONE OUTPUT/BCD MODE

Input/Output. Pin 11. A 500 Hz square wave is activated at this pin upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In the Pulse mode the PACIFIER TONE is activated for all key entries. The PACIFIER TONE provides audible feedback, confirming that the key has been properly entered and accepted. In Tone mode, only the LND key activates the PACIFIER TONE.

This pin is normally high impedance until a key is entered. Connecting this pin high through a resistor causes the circuit to accept BCD inputs through the

Figure 2 : Single Tone.

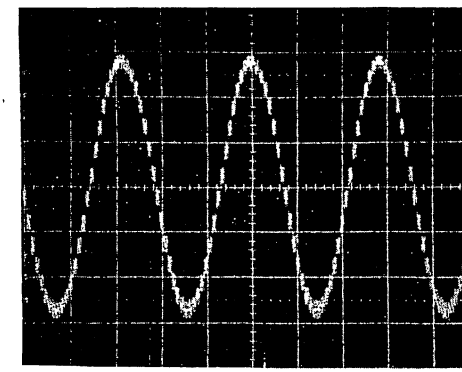


Figure 3 : Dual Tone.

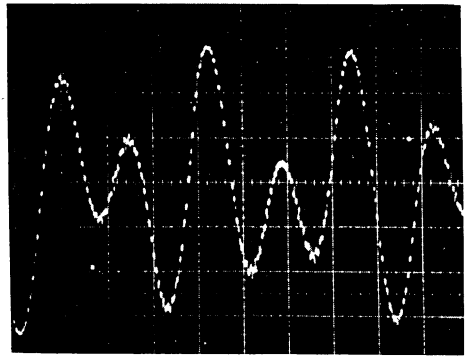


Figure 4 : Spectral Reponse.

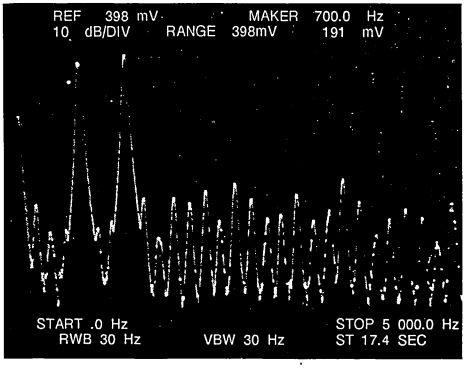
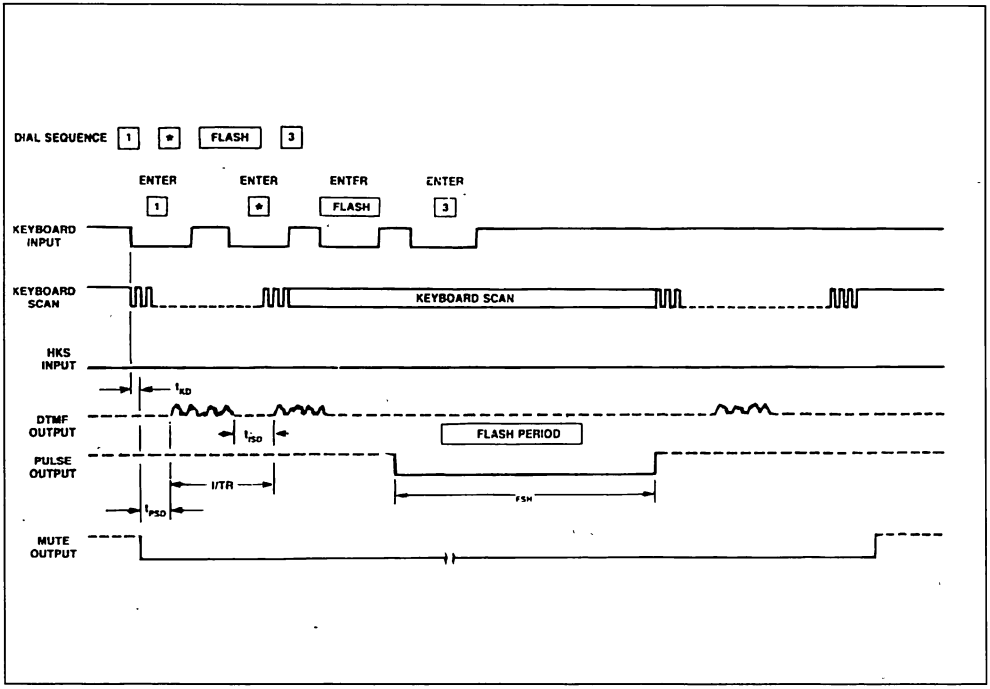


Figure 5 : Tone Mode Timing.



ROW pins. In Binary Mode, as mentioned in the keyboard interface description, the keyboard inputs are all high impedance. Keypad inputs in this mode are not recognized. Connecting this pin low enables the keyboard scan circuitry, which allows entries. The mode of operation is selected upon power-up, and thereafter may only occur when HKS pin 17 is high.

MUTE1

Output. Pin 12. This pin is the Mute Output for both Tone and Pulse Modes. Timing is dependent upon mode.

The output consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In Tone Mode, $\overline{\text{MUTE1}}$ removes the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE1}}$ is active continuously until dialing is completed.

In Pulse Mode, $\overline{\text{MUTE1}}$ removes the receiver or the network from the line. Different circuitry is required for Tone and Pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE1}}$ timing is shown in Figure 6 for Pulse Mode signaling and Figure 5 for Tone Mode signaling.

HKS

Input. Pin 17. Pin 17 is the hookswitch input to the MK5372. This is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at Pin 2.

$\overline{\text{PULSE}}$ OUTPUT

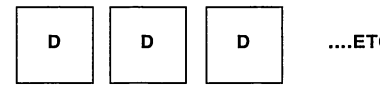
Output. Pin 18. This pin has a dual function determined by the dialing mode selected. In Pulse Mode, the pin is an output consisting of an open drain N-channel device with zener protection. The break timing at this output meets Bell Telephone and EIA specifications for loop disconnect signaling. The Make/Break ratio is not user selectable in the 18-pin version. $\overline{\text{PULSE}}$ OUTPUT also provides the break timing for the hook flash function. Figure 6 shows this timing.

DEVICE OPERATION (Tone Mode)

When the MK5371 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are pulled high. Key entries are not recognized unless they utilize a keypad common connection to force the respective Row and Column inputs low. These inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, the Mute Output is activated, and dialing begins after a pre-signal delay of 100 ms. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an intersignal time of 102 ms.

One important feature of the dialer is its ability to buffer data into the RAM before signaling. This feature allows less expensive keyboards to be used because signal distortion and double digit entry caused by bouncing and bounding of the keypad are eliminated. This design also ensures that data stored in the buffer exactly matches the digits actually dialed.

NORMAL DIALING (off-hoof)

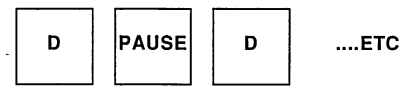


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last Number Dialing is accomplished by entering the LND key.

PABX PAUSE



A pause may be entered into the dialed sequence at any point by keying in the special function key, Pause. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 3.

HOOK FLASH

D	FLASH	D	....ETC

HOOK FLASH may be entered into the dialed sequence at any point by keying in the function key, Flash. The flash function is stored in the LND buffer just like any other digit, but it will not be redialed, and acts much like Pause. The MK5371 has a HOOK FLASH time of 600 ms.

SOFTSWITCH

D	MODE	D	....ETC

Softswitch allows the user to easily switch from Pulse to Tone Mode while dialing a number sequence. For example, the first digits may be entered in Pulse Mode. Signaling will proceed in Pulse Mode until a Softswitch (Mode) entry is encountered. Any subsequent digits are dialed using DTMF signals. A hookswitch transition or a second Softswitch entry returns dialing to the original Default Mode.

Each special function provides a built-in delay before auto-dialing resumes. The fixed delay introduced by the function is 1.1 seconds. In addition, the fixed delay is preceded and followed by the standard interdigital pause period that depends on the selected signaling mode. Table 3 lists the actual delays produced by each function.

Table 3 : Special Function Delay Periods.

Function	Delay	Pulse Mode	Tone Mode
PAUSE	IDP + 1.1 + IDP	+ IDP	1.5 sec
SOFTSWITCH	IDP + 1.1 + IDP	2.9 sec	1.3 sec
FLASH	.6	2.1 sec	2.1 sec

Figure 6 : Pulse Mode Timing.

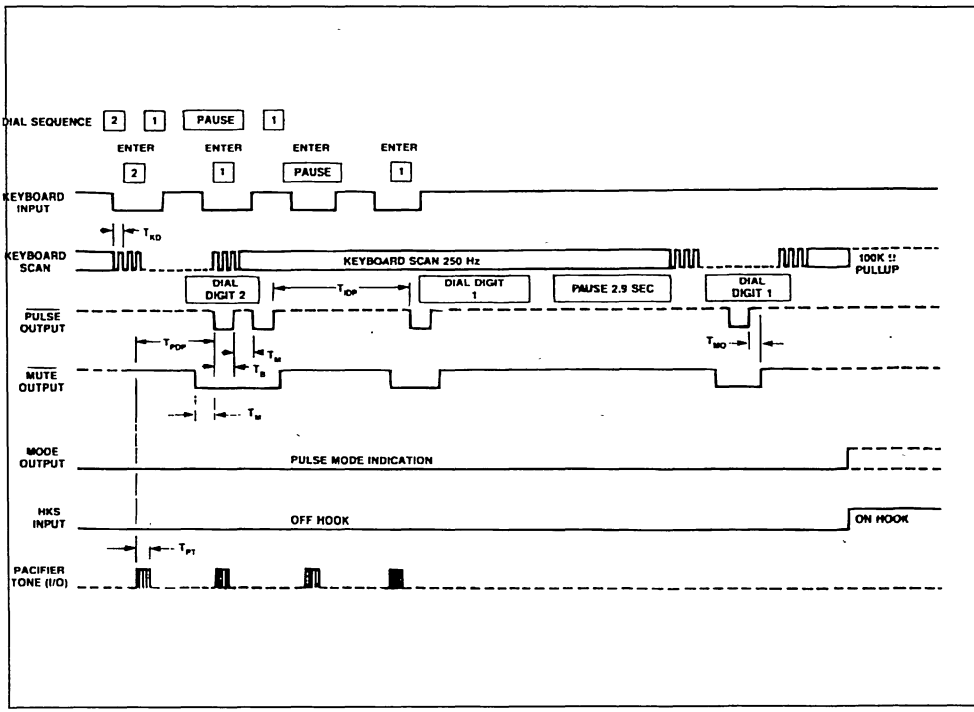
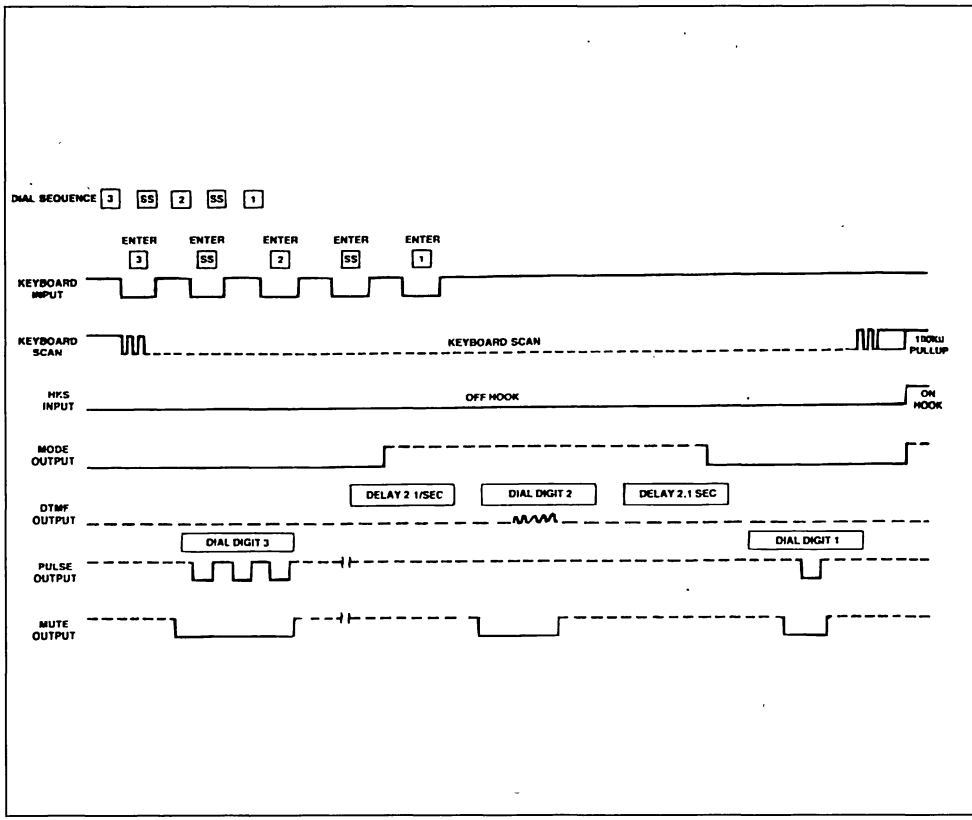


Figure 7 : Pulse And Tone Mode Timing.



TYPICAL APPLICATION

The MK5371 Pulse Tone dialer provides both cost-effective telephone-line interface and the logic required for DTMF (Tone) and Loop Disconnect (Pulse) signaling.

Pulse dialing originated with the rotary dial telephone. The MK5371 Pulse Tone dialer provides the same capability as the rotary dial telephone and the convenience of pushbutton entry. The subscriber set (telephone) is powered by loop current supplied by the telephone company. Signaling, in Pulse Mode, is accomplished by repeatedly interrupting the loop current. The central office senses, times, and counts each line "break" ; the number of breaks corresponds to the digit dialed. The duration of the break period, the dialing rate, and the separation between consecutive digits (IDP time) are controlled by the Pulse Tone dialer IC. Loop disconnect dialing is nearly a world-standard concept.

DTMF signalling consists of modulating the telephone line with a signal comprised of two fundamental frequencies. Each frequency pair represents one of sixteen possible digit (or key) entries. Twelve of these frequency pairs are commonly used (0, 1, 2, ...,*, #). The MK5371 Pulse Tone dialer provides DTMF signalling capability controlling signal duration, separation, level, and rate.

The typical application circuit in Figure 8 illustrates one way the Pulse Tone dialer can be used. The pulse output provides the signal to break the line to transistor Q3. Q3 switches off, eliminating the base current to Q4, which also switches off. The majority of the loop current is then eliminated, resulting in a break condition. The IC dialer must be protected from large voltage fluctuations, such as that caused by interrupting the loop current. Transistor Q1 along with R2, C1, and Z1 regulate the voltage to the dialer. The Mute Output signal is active while signalling each digit to mute popping noises at the receiver (earpiece or speaker).

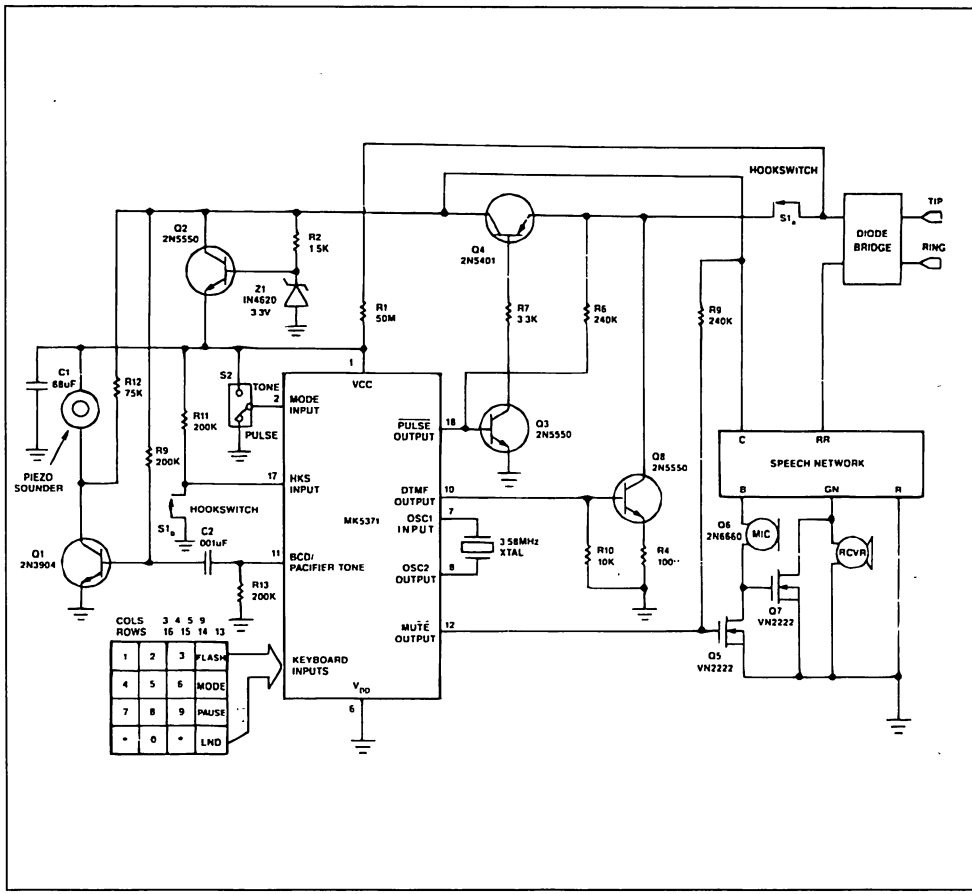
The DTMF tone output drives the base of Q8, which modulates the line. The tone level at tip and ring is determined by the effective impedance of the telephone line and the speech network.

Mode of operation is controlled by switch S1 (which sets the default dialing mode) and the keypad. A change of dialing mode with a Mode (Softswitch) key input is stored in memory and will be repeated when the LND (last number dialed) feature is activated.

Resistor R1 provides a small memory-retention bias current to prevent the device from powering down while on hook. The current required for long term memory retention is less than 1 µA.

A ceramic sounder can also be interfaced to pin 11 (BCD/PACIFIER TONE) of the device. A pacifier tone signal is activated for each key entry. This feature provides an audible indication for each valid key entry. Keys may be entered faster than the maximum signalling rate allows. Audible feedback confirms proper key entry.

Figure 8 : MK5371 Typical Application.



SGS-THOMSON MICROELECTRONICS

MK5375

TEN-NUMBER REPERTORY TONE/PULSE DIALER

- CMOS TECHNOLOGY PROVIDES LOW-VOLTAGE OPERATION
- CONVERTS PUSH-BUTTON INPUTS TO BOTH DTMF AND LOOP-DISCONNECT SIGNALS
- STORES TEN 16-DIGIT TELEPHONE NUMBERS, INCLUDING LAST NUMBER DIALED
- PACIFIER TONE AND PBX PAUSE
- LAST-NUMBER-DIALED (LND) PRIVACY
- MANUAL AND AUTO-DIALED DIGITS MAY BE CASCADED
- ABILITY TO STORE AND DIAL BOTH "*" AND "#" DTMF SIGNALS
- VARIABLE DIALING RATE
- ON-CHIP POWER-UP-CLEAR GUARANTEES DATA INTEGRITY

DESCRIPTION

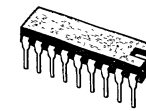
The MK5375 is a monolithic, integrated circuit manufactured using Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. It also allows for the storage of ten telephone numbers, including as many as 16 digits each, in on-chip memory.

The MK5375 accepts rapid keypad inputs (up to 25 key entries per second) and buffers these inputs in the FIFO (First-In-First-Out) LND (Last-Number-Dialed) register. Each digit entry is accompanied by a pacifer tone. Which is activated after the digit has been debounced, decoded, and properly stored. Signaling occurs at a rate determined by externally connected components, allowing the dialing rate to be adjusted for any system.

The flexibility of the dialer makes possible a variety of applications, such as "scratchpad" number storage. In "scratchpad" applications, the MK5375 inhibits signaling during entry, without interrupting a conversation.

Privacy is also an important feature. The MK5375 allows the LND (Last-Number-Dialed) buffer to be cleared following a call, without affecting data stored in other permanent memory locations. The memory in the permanent locations may be easily protected from inadvertent key entries with the addition of a simple "memory lock" switch to the application.

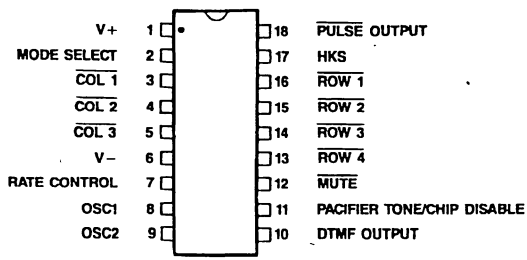
All of these options plus additional features are discussed in more detail in the following sections. the first section contains a brief detailed description of each pin function. The second section describes the device operation. This is followed by the DC and AC Electrical Specifications, and a few application suggestions.



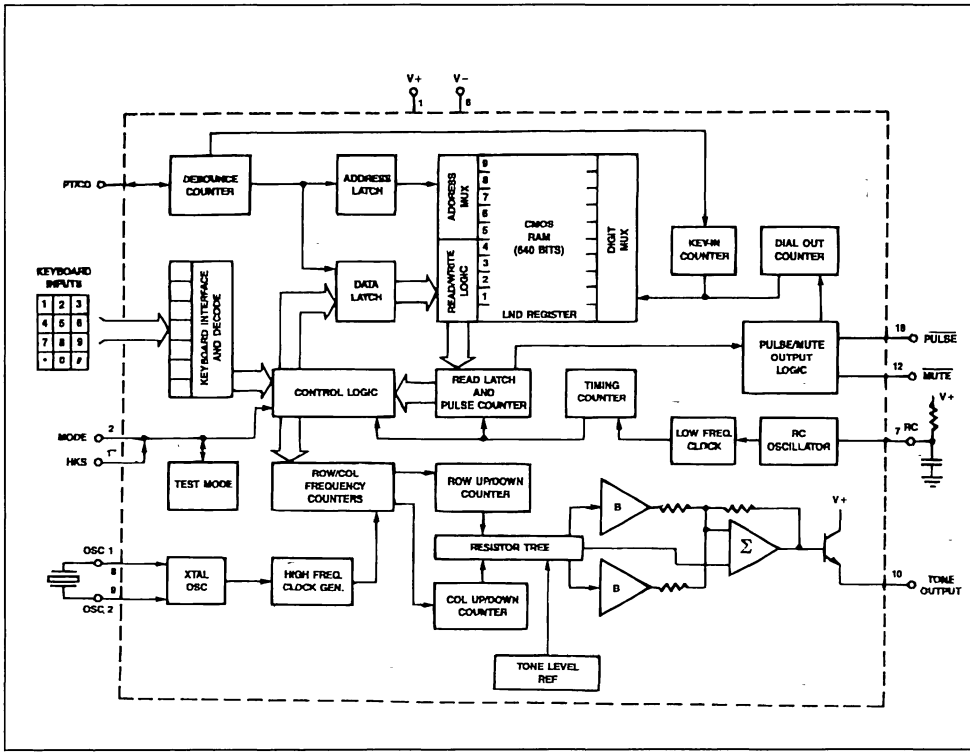
DIP18

ORDER CODE : MK5375N00

PIN CONNECTION



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

V+ (pin 1)

Pin 1 is the positive supply for the circuit and must meet the maximum and minimum voltage requirements as stated in the electrical specifications.

MODE SELECT (pin 2)

In normal operations. Pin 2 determines the signaling mode used : a logic level 1 (V+) selects Tone Mode operation. While a logic level 0 (V–) selects Pulse Mode operation. This input must be tied to one of the supplies to guarantee proper dialing.

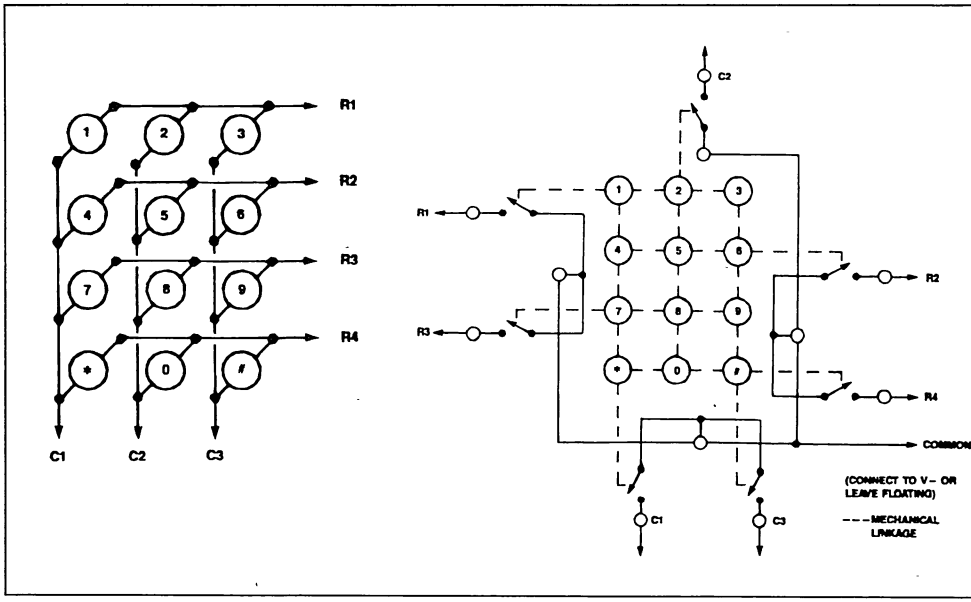
KEYBOARD INPUT : $\overline{COL1}$, $\overline{COL2}$, $\overline{COL3}$, $\overline{ROW4}$, ROW3, ROW2, ROW1 (pins 3, 4, 5, 13, 14, 15, 16)

The MK5375 keypad interface allows either the standard 2-of-7 keyboard with negative common or the in-expensive single-contact (FORM–A) keyboard to be used (Figure 1). A valid key entry is defined by either a single Row being connected to a single Column or by V™ being presented to both a single Row and Column. In standby mode either all the rows will be a logic 1 (V+) and all the columns will be a logic 0 (V–) or vice versa.

The keyboard interface logic detects when an input is pulled low and enables the RC (Rate Control) oscillator and keypad scan. Scanning consists of alternately strobing the rows and columns high through on-chip pullups. After both valid row and column key closures have been detected, the debounce counter is enabled.

Breaks in contact continuity (bouncing contacts, etc.) are ignored for a debounce period (T_{db}) of 32 ms. At this time the keypad is sampled, and if both row and column information is valid, this information is buffered into the LND location.

Figure 1 : Keypad Schematics.



RATE CONTROL (pin 7)

The Rate Control input is a single-pin RC oscillator. An external resistor and capacitor determine the rate at which signaling occurs is both Tone and Pulse modes. An 8 kHz oscillation provides the nominal signaling rates of 10 PPS (Pulses per second) in Pulse Mode and 50 TPS (Tones per second) in Tone Mode ; the Tone duty cycle is 98 ms on, 102 ms off. The RC values on this input can be adjusted to a maximum oscillation frequency of 16 kHz resulting in an effective Pulse rate of 20 PPS an a Tone rate or 10 TPS.

The frequency of oscillation is approximated by the following equation :

$$Fosc = 1/(1.49RC) \qquad (1.0)$$

The value suggested for the capacitor (C) should be a maximum of 410 pF to guarantee the accuray of the oscillator. The resistor is then selected for the desired signaling rate. Nominal frequency (8 kHz) is achieved with component values of 390 pF and 220 kohms. Parasitics must be taken into account.

OSCIN, OSCOUT (pins 8, 9)

Pins 8 and 9 are the input and output, respectively, of an on-chip inverter with sufficient loop gain to oscillate when used in conjunction with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz, and any deviation from this standard is directly reflected in the Tone Output frequencies.

This oscillator is under direct control of the repertory dialer and is enabled only when a tone signal is to be transmitted. During all other times it remains off, and the input has high impedance. The input OSCIN may be driven by an external source.

DTMF OUTPUT (pin 10)

The DTMF Output pin is connected internally to the emitter of an NPN transistor, which has its collector tied to V+, as shown on the functional block diagram.

The base of this transistor is the output of an on-chip operational amplifier that mixes the Row and Column Tones together.

The level of the DTMF Output is the sum of a single row frequency and a single column frequency. A typical single-tone sine wave is shown in Figure 2. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The tone level of the MK5375 is a function of the supply voltage. The voltage to the device may be regulated to achieve the desired tone level, which is related to the supply by either of the following equations :

$$T_{(0)} = 20 \text{ LOG } [(0.078V +)/0.775] \text{ dBm} \qquad (2.0)$$

$$T_{(0)} = 0.078(V+) \text{ VRMS. (row tones)} \qquad (2.1)$$

PACIFIER TONE OUTPUT / CHIP DISABLE (pin 11)

This pin normally has high impedance. Upon acceptance of a valid key input, and after the 32 ms debounce time, a 500 Hz square-wave will be output on this pin. The square-wave terminates after a maximum of 30 ms or when the valid key is no longer present. The purpose of this pacifier tone is to provide to the user audible feedback taht a valid key has been entered. This feature is useful particularly for on-hook storage and pulse-mode signaling.

The pacifier tone is not enabled when manually dialing in tone mode. this eliminates any confusion between the audible DTMF feedback and the pacifier tone, and prevents distortion of the DTMF signal by any of the pacifier tone frequency components. In both cases, the tone confirms that the key has been properly entered and accepted : whereas without the tone the user will not know if the keys have been properly entered.

IMPORTANT : This pin also serves as a chip-disable pin. pulling this input high through a resistor will disable the keypad (high impedance) and initialize all counters and flip-flops (memory remains undisturbed). Pulling the input low through the same resistor enables the circuit. For the device to function properly, the resistor to V- (pin) is required.

This feature is useful in several applications, as described in the application notes section.

MUTE OUTPUT (pin 12)

This pin is the Mute output for both Tone and Pulse modes of operation. The timing is dependent upon which mode is being used. The output consists of an open-frain, N-channel device. During stanby, the output has high impedance and generally requires an external pullup resistor to the positive supply.
In Tone Mode, the Mute output is used to remove the transmitter and the receiver from the network during DTMF signaling. The output will mute continuously while auto-dialing and during manual DTMF signaling until each digit entered has been signaled.
In Pulse Mode of operation, the Mute output is used to remove the receiver or even the entire network from the line. These timing relation ships are shown in Figure 4.

HKS INPUT (pin 17)

This pin is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input will cause the on-chip logic to initialize, terminating any operation in progress at the time. Signaling is inhibited while on-hook, but key inputs will be accepted and stored in the LND register. The information stored in the LND register may be copied into an alternate location only whil on-hook. A logic level may be presented to this input, independent of the position of the hook-switch, allowing on-hook operations, such as storage, to be performed off-hook.

Figure 2A : Typical Sine Wave Output - Single Tone.

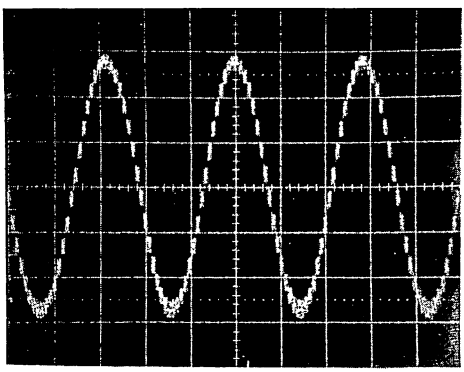


Figure 2B : Typical Dual-tone Waveform (Row 1, Col 1).

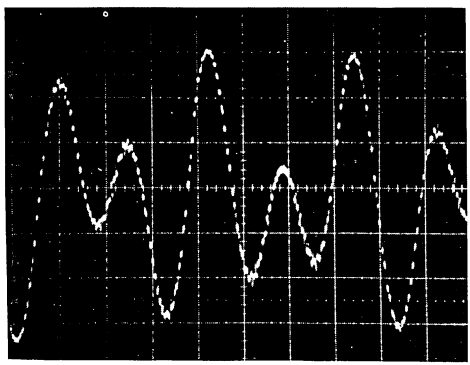


Figure 2C : Spectral Analysis of Waveform in Fig.5 (Vert.10 dB/div. Horizontal - 600 Hz/div.).

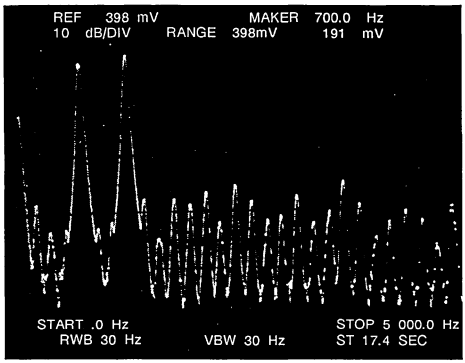


Table 1 : Output Frequency.

Key Input	Standard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+ 0.31
2	770	766.2	– 0.49
3	852	847.4	– 0.54
4	941	948.0	+ 0.74
COL 1	1209	1215.9	+ 0.57
2	1336	1331.7	– 0.32
3	1477	1471.9	– 0.35

PULSE (pin 18)

This is an output driven by an open-drain, N-channel device. In Pulse Mode operation, the timing at this output meets Bell Telephone and EIA specifications for loop-disconnect signaling. The Make/Brake ratio is set to 40/60 on the standard MK5375. The pulse rate is determined By the RC values selected for the Rate Control, Pin 7. Note : The standard make/break ratio may not be suitable if the Pulse dialing rate is accelerated.

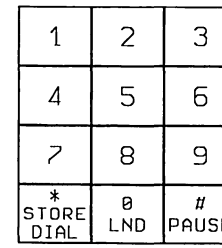
DEVICE OPERATION

The Mk5375 can be used in low-priced phones with basic 3x4 matrix keypads. the block diagram shows the data and control signal flow between the various functional blocks. The keypad entries are decoded, debounced, and if valid, they are stored into the LND (Last-Number-Dialed) buffer, which acts much like a FIFO (First-In-First-Out) register. Each subsequent entry is stacked in the buffer. Typically, the dialing sequence begins 172 ms after the first digit is accepted in Pulse Mode operation and 132 ms in Tone Mode operation. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an inter-signal time of 102 ms.

Buffering the data into the RAM prior to signaling is an important feature of the repertory dialer. It allows for the use of less expensive keypads, since the user cannot enter the digits too quickly for the system, and the pacifier tone can be used to provide audible feedback following each key entry not generating a DTMF signal. It also guarantees that the data stored in the RAM matches exactly the digits actually dialed.

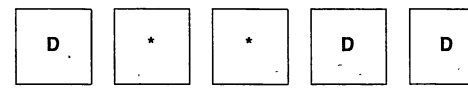
Manual dialing and auto-dialing can be executed in any order, consecutively or cascaded. The dialer must complete auto-dialing the previous entry before another key is entered. Digits should not be entered while the device is auto-dialing. Most digits would be ignored unless preceded by a control key : in which case, an error in dialing may occur.

Figure 3 : Keypad Configuration.



H88MK5376-01

NORMAL DIALING



The "*" (STAR) key is used as the modifier to control repertory functions. All numeric keys will signal normally unless preceded by a modifier. To signal either a "*" or "#", these keys must be entered twice in succession. The first entry is not signaled or stored.

LND PRIVACY

D	D	D	*	ON HOOK

A single "*" input prior to going on-hook or prior to coming off-hook will erase the information stored in the LND buffer.

AUTO DIALING (off-hook)

D	D	D	*	N
opt	opt	opt		

The key sequence "*" followed by any digit, will auto-dial the number sequence stored in the designated address location while off-hook.

STORAGE (on-hook)

D	D	D	*	N

D is any data (telephone numbers) being entered or dialed. N is the address (memory location) in which numbers are stored. The number sequence stored in the LND buffer can be transfered to one the other nine permanent locations whith the simple sequence "*" followed by the address. New digits may be written into the LND buffer while on-hook. To enter either a "*" or "#" signal the digit must be entered twice in succession.

PABX PAUSE (off-hook and on-hook)

D	D	*	#	D

An indefinite pause is stored in a number sequence by entering the "*" key modifier, followed by a "#" key input. When the number sequence is redialed, the dialer will pause when it encounters the "#" entry. A key input will cause it to continue.

PULSE DIALING

Most of the Pulse key operations are the same as they were in Tone Mode ; PABX Pause is the only exception. In Pulse Mode, the pause may be stored as in tone mode, "* #", or with a single "#" inputs will store two pauses.

The "*" key exercises the control function ; two "*" inputs will be the same as a single input (multiple inputs are not accepted).

Figure 4A : MK5375 Timing Diagram – Pulse Mode Off-hook Operation.

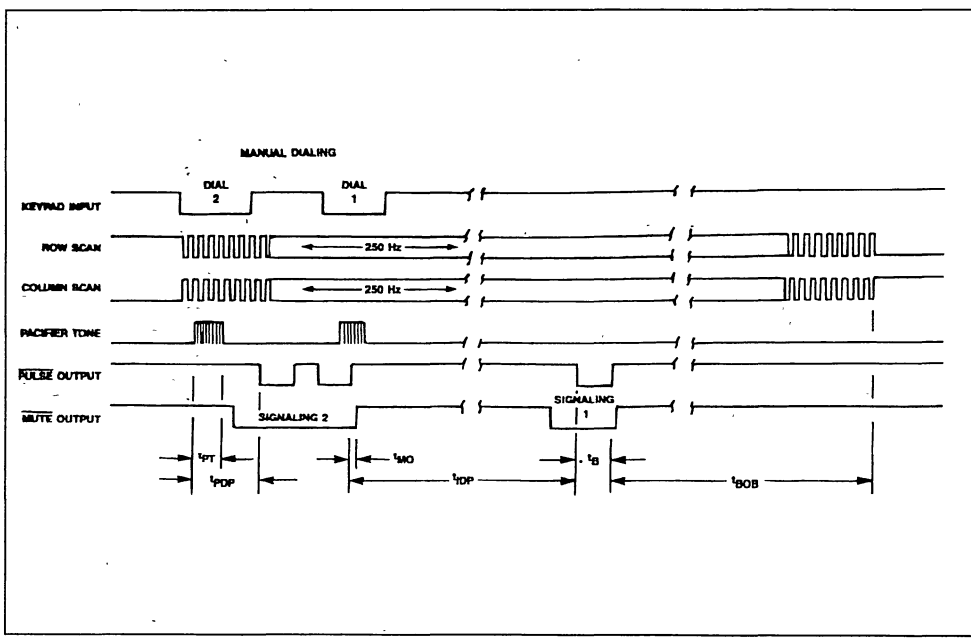
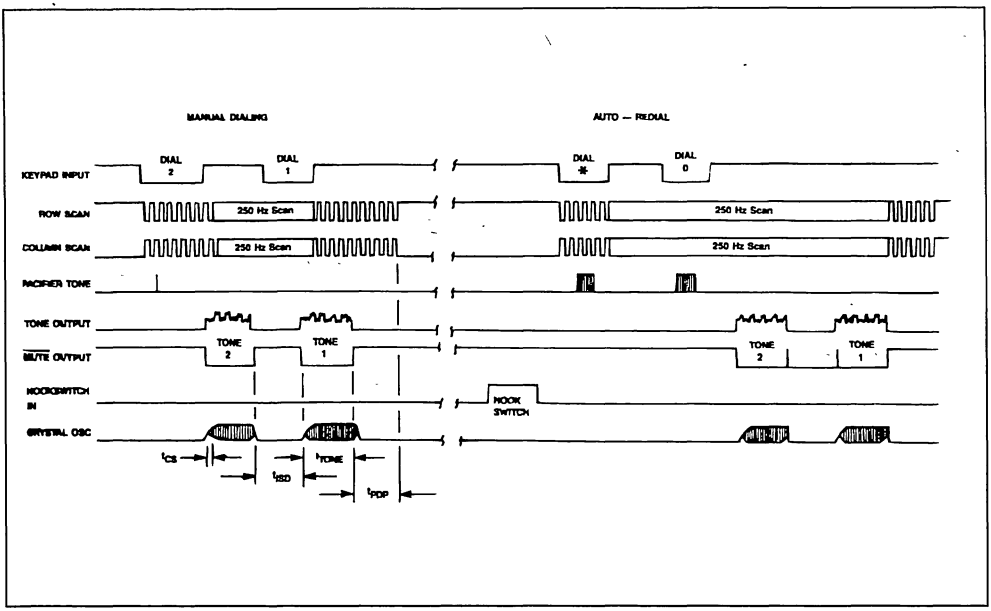


Figure 4B : MK5375 Timing Diagram – Tone Mode.



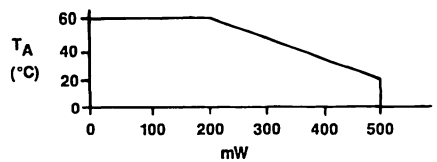
ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
DC Supply Voltage V^+	6.5	V
Operating Temperature	– 30 to + 60	°C
Storage Temperature	– 55 to + 85	°C
Maximum Voltage Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	$(V^+) + 0.3$, $(V^-) - 0.3$	V

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMANDED OPERATING CONDITIONS

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL OPERATING CHARACTERISTICS

DC CHARACTERISTICS – 30 °C ≤ T_A ≤ 60 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V^+	DC Operating Voltage	2.5		6.0	V	
I_{SB}	Standby Current		0.3	0.75	µA	1
V_{MR}	Memory Retention Voltage	1.5			V	2
I_{MR}	Memory Retention Current	750	200		nA	2
I_T	Operating Current (tone)		0.5	1.0	mA	3
I_P	Operating Current (pulse)		50	150	µA	3
I_{ML}	Mute Output Sink Current	1.0	3.0		mA	4
I_{PL}	Pulse Output Sink Current	1.0	3.0		mA	4
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	5
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	Keypad Pulldown Resistance		500		Ω	

(All specifications are for 2.5 Volt operation, unless otherwise stated Typical values are representative values at room temperature and are not tested or guaranteed parameters).

Notes : 1. All inputs unloaded. Quescient Mode (Oscillator off).
2. Meeting these minimum supply requirements will guarantee the rentention of data stored in memory.
3. All outputs unloaded single key input.
4. V_{OUT} = 0.5 Volts.
5. Sink current for V_{OUT} = 0.5, source current for V_{OUT} = 2.0 Volts.

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T_{KD}	Keypad Debounce Time		32		ms	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		ms	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone		30		ms	1
F_{RC}	Frequency RC Oscillator	– 7.0	± 2.5	+ 7.0	%	2

Notes : 1. Times based upon 8 kHz RC input for Rate Control.
2. Deviation of oscillator frequency takes into account all voltage (2.5 to + 60 Volts), temperature (30° to .60°C) and unit-to-unit variations. The tolerance of the external RC components or parasitic capacitance is not included.

AC CHARACTERISTICS – TONE MODE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T_{NK}	Tone Output no Key down			– 80	dBm	1
T_O	Tone Output (row tones)	– 13 173	– 12 194	– 11 218	dBm mV (RMS)	1
PE	Pre-emphasis, High Band	2.2	2.7	3.2	dB	1
V_{DC}	Average DC Bias Tone Out		1.7		V	
DIS	Output Distortion		5.0	8.0	%	1
TR	Tone Signaling Rate		5	10	1/SEC	2
PSD	Pre-signal Delay		132		mSEC	2
ISD	Inter-signal Delay		100		mSEC	

Notes : 1. Load 10 kΩ.
2. These values are directly related to the RC input to Pin 7 nominally 8 kHz.

ELECTRICAL OPERATING CHARACTERISTICS (continued)

AC CHARACTERISTICS – PULSE MODE OPERATION

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
P_R	Pulse Rate		10		PPS	1
PDP	Predigital Pause		172		ms	1
IDP	Interdigital Pause		940		ms	1
T_{MO}	Mute Overlap Time		2		ms	1

Notes : 1. Typical time assume nominal RC input frequency of 8 kHz. An increase in frequency results in an equal decrease in time values and an equal increase in rate values.

APPLICATION CIRCUIT

The MK5375 integrated circuit provides the ability to convert keypad inputs into either DTMF or loop-disconnect signals compatible with most telephone systems. Both modes of signaling utilise loop currents to transmit the desired signaling information to the central office.

The circuit schematic in Figure 5 illustrates a typical implementation of the MK5375 dialer IC along with the necessary components required to interface with the telephone line in a tone/pulse application.

In loop-disconnect signaling, each digit dialed consists of a series of momentary interruptions of loop current called "breaks" (i.e., a digit "1" consists of a single break, a digit "2" consists of two breaks, and so on. The Pulse output is dedicated to loop-disconnect signaling and controls the flow of loop current through the speech network switching transistors, Q4 and Q5. The Mute output, through transistors Q2 and Q3, removes the receiver and transmitter to eliminate loud pops in the receiver caused by switching current through the network. The Pulse and Mute output signals, as shown in Figure 4A, consist of make, break, and interdigital time intervals.

DTMF signaling requires that the loop current be modulated, producing an analog signal on the telephone line. Transistor Q1 modulates the loop current by amplifying the DTMF signal coupled to its base from the Tone Output. The Mute output removes the receiver and transmitter by switching transistors Q2 and Q3. This eliminates any interference with the DTMF signal from the transmitter and cuts down on the amplitude of the DTMF tone heard at the receiver. The timing diagram in Figure 4B illustrates the time relationship between key entries, Tone Output, and Mute Output.

The voltage regulator circuit comprising resistor R2, zener diode Z2, and transistor Q6 serves several purposes. In tone mode operation, it provides the regulated supply voltage to the MK5375 which determines the DTMF signal amplitude at the Tone Output. Varying the supply voltage will vary the DTMF output signal. In pulse mode, it helps provide some isolation from the transients caused by switching the speech network in and out.

During normal off-hook dialing, the MK5375 operates using current from the telephone line. On-hook number storage and memory retention current are supplied by the battery shown in Figure 5. Transistor Q6 prevents the flow of battery current to the speech network.

The rate at which dialing occurs is determined by the values chosen for resistor R1 and capacitor C1. These values can be predetermined using equation (1.0) described above. The 3.5795 MHz crystal is used as a reference for systhesizing the DTMF signals and is activated only for the short periods during which these tones are being generated.

The application circuit schematic in Figure 6 gives an example of the various features which can be utilized with the addition of several switches. the example also shows that multiple devices may be used to increase the effective storage capability of the telephone design.

Much of the circuity used to modulate and pulse the line, mute the speech network, and regulate the supply voltage is unchanged from the basic tone/pulse switchable telephone described above.

The two devices in Figure 6 are hooked up in parallel with on another except for their oscillator pins and the Chip Disable inputs. A DPDT switch is used to select between the two dialers through the Chip Disable pin ; one device is activated while the other is put on standby.

Some applications may include a memory lock switch to prevent any of the data stored to be changed inadvertently. This memory lock switch can take the form of a locking key switch, which would allow only the person with the key to alter data stored in memory.

A scratchpad feature may be implemented to allow off-hook programmming of the memory while inhibiting dialing. A switch is added in series with the telephone hook-switch to allow the dialer to be forced into its on)hook key entry mode while the telephone set is off-hook.

Figure 5 : MK5375 Circuit Schematic.

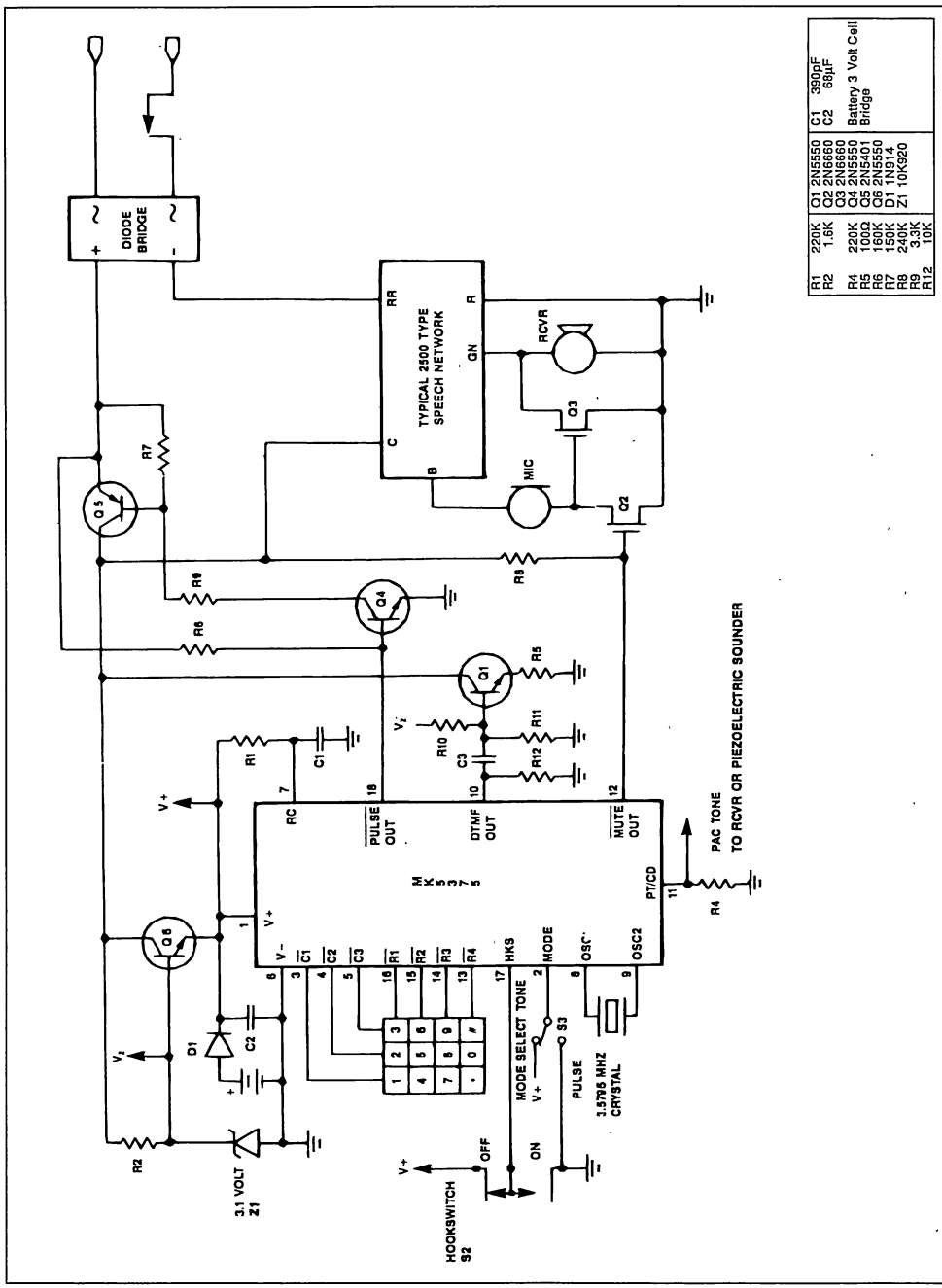
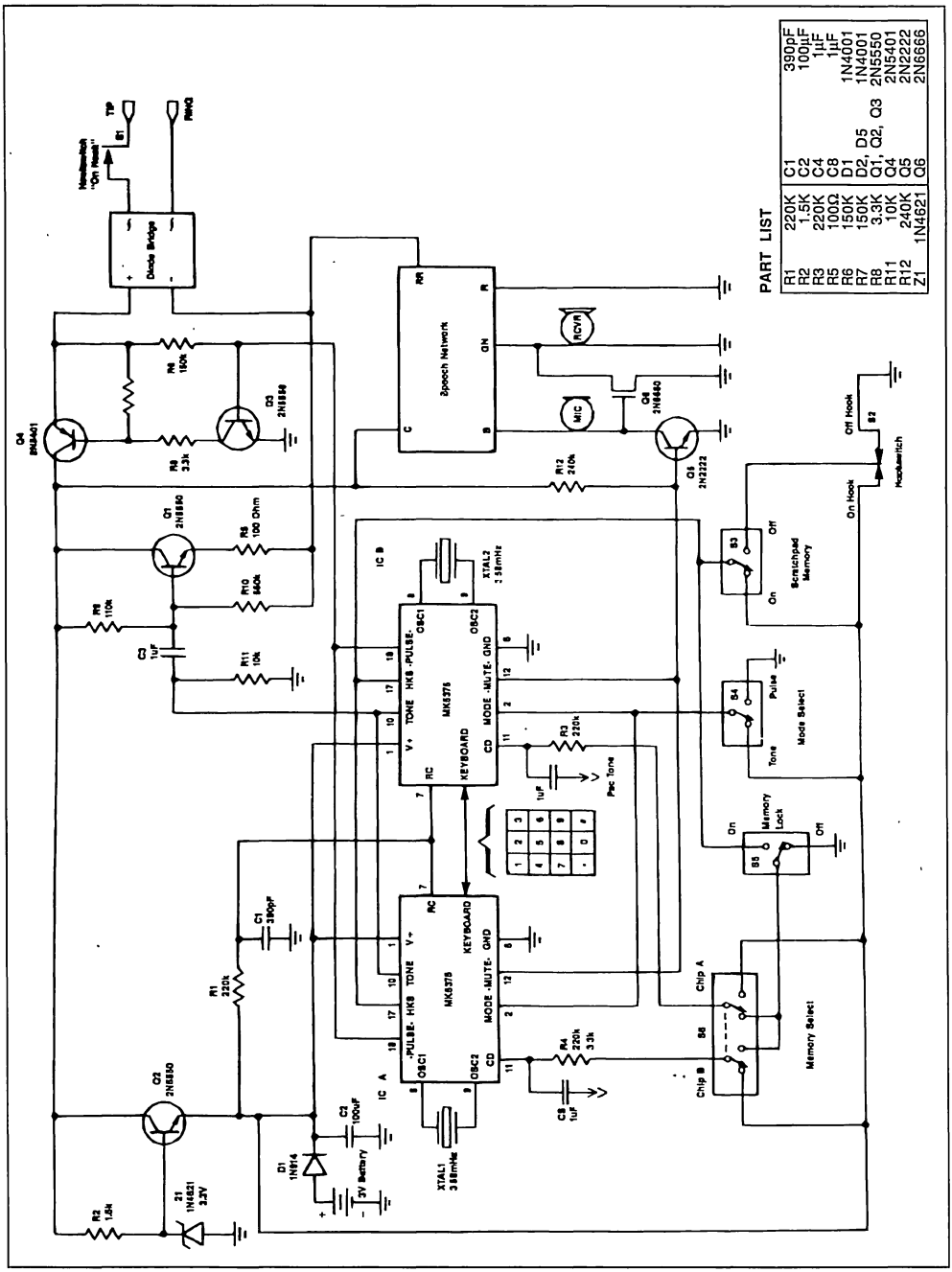


Figure 6 : MK5375 Application Circuit Schematic.

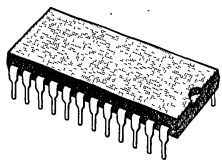


SGS-THOMSON MICROELECTRONICS

MK5376

TEN-NUMBER REPERTORY TONE/PULSE DIALER

- CONVERTS PUSH-BUTTON INPUTS TO BOTH DTMF AND PULSE SIGNALS
- STORES TEN 16-DIGIT TELEPHONE NUMBERS INCLUDING LAST NUMBER DIALED
- PACIFIER TONE AND PBX PAUSE
- LAST NUMBER DIALED (LND) PRIVACY
- MANUAL AND AUTO-DIALED DIGITS MAY BE CASCADED
- ABILITY TO STORE AND DIAL BOTH * AND # DTMF SIGNALS



DIP-24

ORDER CODE : MK5376N00

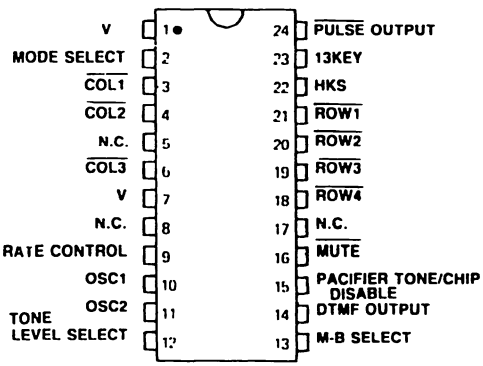
DESCRIPTION

The MK5376 is a monolithic, integrated circuit manufactured using Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. Ten telephone numbers of up to 16 digits each may be stored in the on-chip RAM. Manual and auto-dialed numbers may be cascaded in any order.

Additional functions available are a Pacifier Tone output, PABX pause, external control of the signaling rate, and total functional control with either a standard 3 x 4 matrix keypad (FORM-A) or a 2-of-7 keyboard. A 13th key option allows control of the dialer's repertory features. The telephone keypad then functions for signaling purposes only, independent of the repertory functions. The 13th key mode and the M-B (Make/Break) Ratio is user selectable.

The dialer's flexibility provides for many applications, for example, off-hook programming, the use of additional chips in parallel for 10, 20, and 30 number repertory phones, permanent memory protection and the option of a supply-independent or supply-dependent tone level.

PIN CONNECTION



FUNCTIONAL DESCRIPTION

V+

Pin 1. Pin 1 is the positive supply for the circuit and must meet the voltage requirements defined in the Electrical Specifications.

MODE SELECT

Input. Pin 2. In normal operation, Pin 2 determines the Signaling Mode ; a logic level 1 (V+) selects Tone Mode, while a logic level 0 (V–) selects Pulse Mode operation. To guarantee proper dialing, this input must be tied to one of the supplies.

$\overline{COL1}$, $\overline{COL2}$, $\overline{COL3}$, $\overline{ROW4}$, $\overline{ROW3}$, $\overline{ROW2}$, $\overline{ROW1}$

Keyboard Input. Pins 3, 4, 6, 18, 19, 20, 21. The MK5376 keypad interface allows users to add either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form-A) keyboard (see Figure 1). A valid key entry is either a single Row connected to a single column or V- presented to both a single Row and Column. In Standby Mode, either all the Rows pull to a logic 1 (V+) and all the Columns are a logic 0 or vice versa.

The keyboard interface logic detects an input being pulled low and enables the RC (RATE CONTROL) oscillator and keypad scan. Scanning consists of Rows and Columns alternately strobing high through on-chip pullups. After both a valid Row and Column key closure have been detected, the debounce counter is enabled Breaks in contact continuity (bouncing contacts, etc.) are ignored for a debounce period (Tdb) of 32 ms. At this time, the keypad is sampled. If both Row and Column information is valid, this information is buffered into the LND.

V–

Input. Pin 7. This pin is the negative supply input to the device. This is the voltage reference for all specifications.

RATE CONTROL

Input. Pin 9. RATE CONTROL is a single-pin RC oscillator. An external resistor and capacitor determine signaling rates in both Tone and Pulse Modes. An 8 KHz oscillation provides nominal signaling rates of 10 PPS (pulses per second) in Pulse Mode and

Figure 1A : Keyboard Schematics-Calculator Type Keypad.

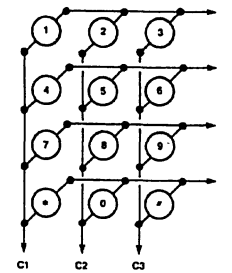
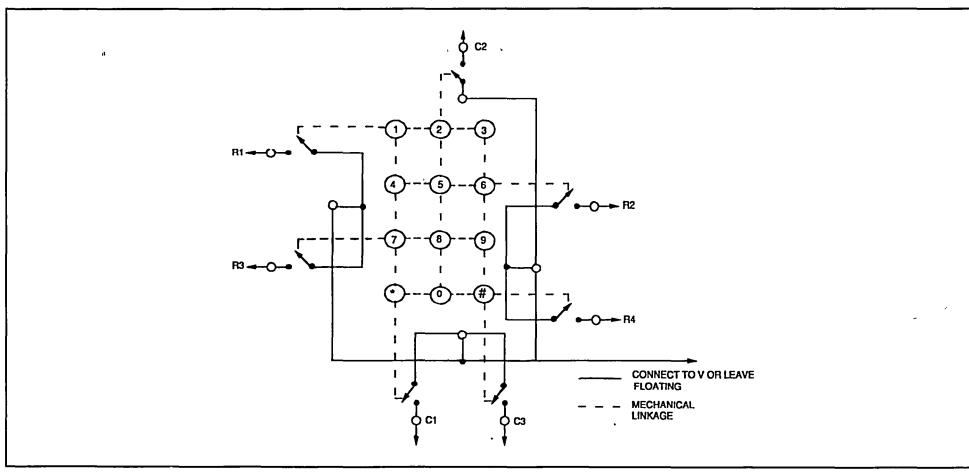


Figure 1B : Keyboard Schematics Standard Telephone Type Keypad.



5 TPS (tones per second) in Tone Mode ; the tone duty cycle is 98 ms on, 102 ms off. RC values on this input can be adjusted to a maximum oscillation frequency of 16 KHz, resulting in an effective Pulse rate of 20 PPS and Tone rate of 10 TPS.

The following equation approximates the oscillation frequency :

$$Fosc = 1/(1.49\ RC)$$

The capacitor's (C) suggested value should be a maximum of 410 pF to guarantee accuracy of the oscillator. The resistor (R) is then selected for the desired signaling rate. The nominal frequency of 8 kHz is achieved with component values of 390 pF and 220 K ohms.

OSC1, OSC2

Input/Output. Pins 10, 11. Pins 10 and 11 are the input and output, respectively, of an on-chip inverter. They have sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation is directly reflected in the Tone Output frequencies.

The repertory dialer directly controls the oscillator and is only enabled for tone signal transmission. It remains off at all other times and the input is high impedance. An external source may also drive the input.

TONE LEVEL SELECT

Input. Pin 12. The MK5376 has selectable tone levels with supply-independent or supply-dependent specifications. The tone levels available are similar to those provided on Mostek's industry standard MK5380 and MK5089 DTMF generators (see Table 1). The optimum tone scheme is application-dependent.

Table 1 : Tone Level Select.

Tone Level Select Input	Tone Reference	Compatible With
V – (method 1)	Supply	MK5089
V + (method 2)	On-chip Reference	MK5380

Method 1 operates from a regulated supply. The tone level is related to this supply by either of the following equations :

$$To = 20\ LOG\ [0.0776(V+)/0.775]\ dBm$$

$$To = 0.0776\ (V+)\ Vrms$$

Method 2 provides a constant tone output and modulates its own supply in a minimum parts count configuration. The tone level, when used in a subscriber set, is a function of the output resistor R_E and the telephone AC resistance R_L. The low-group single tone output amplitude is a function of R_E and R_L described by the equation :

$$Vo = \{1/[0.2+R_E)/R_L]\}To$$

where V_O is the tone amplitude at the phone line and T_O is the tone level at the DTMF OUTPUT pin. This version may also be operated on a regulated supply, but users must observe additional caution to prevent signal distortion (clipping) on longer loops.

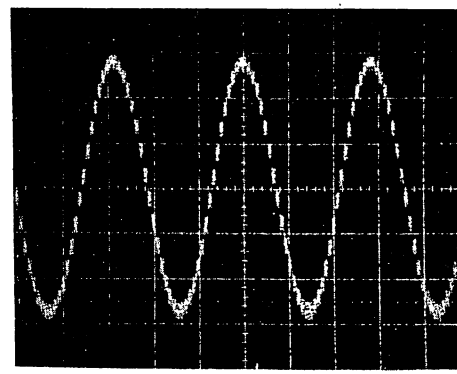
M/B SELECT

Input. Pin 13. In Pulse Mode, this pin selects the Make/Break ratio, or the percentage Break time per Pulse period (see Table 2).

Table 2 : Make/Break Ratio.

M-B Select Input	Break Time	Make Time
V +	68	32
V –	60	40

Figure 2 : Typical Sine Wave Output.



DTMF OUTPUT

Output. Pin 14. The DTMF OUTPUT pin is connected internally to an NPN transistor's emitter with a collector tied to V+. The transistor base is the output of an on-chip operational amplifier that mixes the Row and Column Tones together.

The DTMF OUTPUT level is the sum of a single Row single tone sine wave is shown in Figure 2. This waveform is synthesized using a resistor tree with sinusoidally weighted taps. DTMF output frequencies are defined by Table 3.

PACIFIER TONE OUTPUT/CHIP DISABLE

Input/Output. Pin 15. A 500 Hz square wave is output on this pin after acceptance of a valid key input

and after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. The PACIFIER TONE audibly signals a valid key entry. This feature is particularly useful for on-hook storage and Pulse Mode signaling. The PACIFIER TONE is not enabled when users manually dial in Tone Mode. This eliminates any confusion between the audible DTMF feedback and the PACIFIER TONE. In both cases, the tone confirms that the key has been properly entered and accepted. Without the tone, users do not know if the keys have been properly entered.

This pin is normally high impedance until a key is entered. It also serves as a CHIP DISABLE pin. Pulling this input high through a resistor disables the keypad (high impedance) and initializes all counters and flip flops (memory remains undisturbed). Pulling the input low through the same resistor enables the circuit.

This feature is useful in several applications. It provides a convenient way to lock memory by connecting this input through a resistor to HKS. When it is on-hook, the device is then disabled and key inputs are not recognized. The circuit will function normally off-hook. Information can only be entered into the permanent memory locations by switching to Program Mode. This requires that a switch and resistor be added to connect to V–.

$\overline{\text{MUTE}}$

Output. Pin 16. This pin is the mute output for both Tone and Pulse Modes. Timing depends on which mode is used.

The output consists of an open drain N-channel device and zener input protection. During standby, the output is high impedance and generally requires an external pullup resistor to the positive supply.

In Tone Mode, $\overline{\text{MUTE}}$ removes the transmitter and receiver from the network during DTMF signaling. The output then mutes continuously while auto-dialing and during manual DTMF signaling.

In Pulse Mode, the $\overline{\text{MUTE}}$ removes the receiver or even the entire network from the line. Timing is avai-

Table 3 : Output Frequency.

Key Input	Standard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+ 0.31
2	770	766.2	– 0.49
3	852	847.4	– 0.54
4	941	948.0	+ 0.74
COL 1	1209	1215.9	+ 0.57
2	1336	1331.7	– 0.32
3	1477	1471.9	– 0.35

Figure 3A : MK5376 Timing Diagram - Pulse Mode Off-Hook Operation.

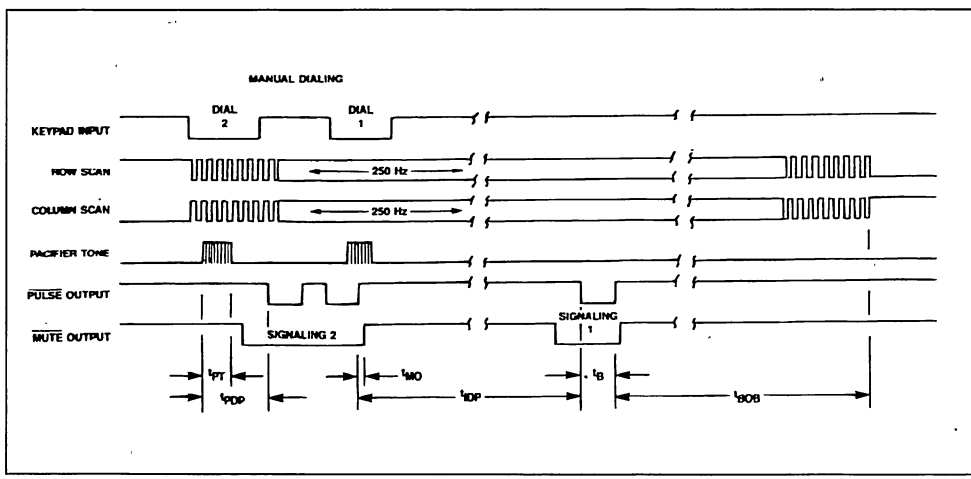
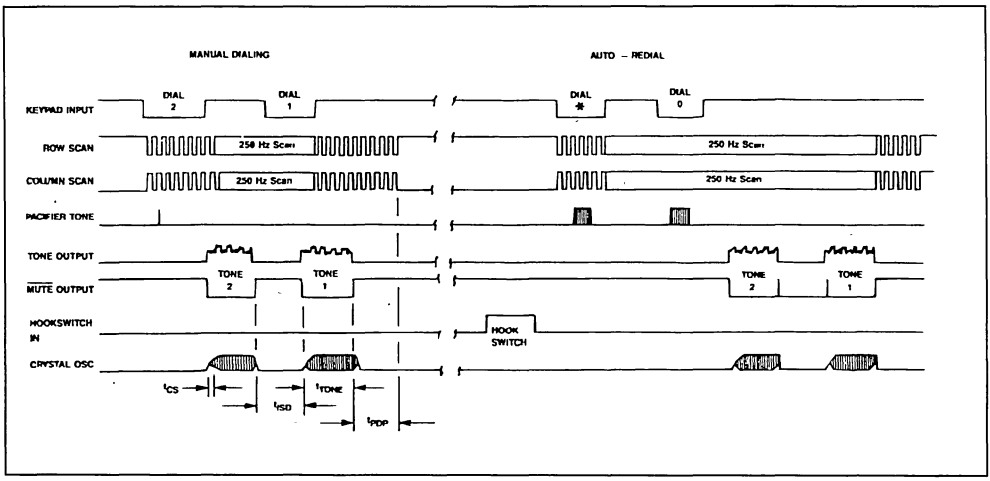


Figure 3B : MK5376 Timing Diagram - Tone Mode.



lable both as a continuous mute (provided by the MK5376) or a mute that is active only when actually pulsing the line. Figure 3 depicts these timing relationships.

HKS

Input. Pin 22. This pin is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input initializes the on-chip logic. This stops the current operation. A logic level independent of the hookswitch position may be presented to this input, which allows on-hook operations, such as storage, to be performed off-hook.

13KEY

Input. Pin 23. This pin is a high impedance input. When it is tied permanently low, it indicates 12KEY Mode. If users desire 13KEY operation, a switch to the negative supply is attached to this pin, along with an external pullup. This forces the repertory dialer into 13KEY Mode. The dialer switches to 12KEY mode if users depress the 13th key switch while simultaneously entering information through the keypad. The differences between these modes are presented in the Device Operation Section.

$\overline{\text{PULSE}}$ OUTPUT

Output. Pin 24. An open drain N-channel device drives this pin. In Pulse Mode, the timing meets Bell Telephone and EIA specifications for loop disconnect signaling. The Make/Break ratio is user-selectable. RATE CONTROL regulates the dialing rate.

DEVICE OPERATION

The MK5376 interfaces to two keypad configurations - the 12KEY and 13KEY Modes (see Figures 4 and 5). This flexibility simplifies interfacing to existing keypads and products. The MK5376 can be used in inexpensive telephones with basic 3x4 matrix keypads to give them repertory dialer features. In 13KEY Mode, the MK5376 allows the keypad to be used for standard signaling and the special repertory functions are only activated by using the "control" (13th) key.

In both modes, keypad entries are decoded, debounced, and (if valid) stored in the LND (Last Number Dialed) buffer that acts much like a FIFO (First-In-First-Out) register. Each subsequent entry is stacked in the buffer. The dialing sequence begins 100 ms after the first digit is accepted. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and a 102 ms intersignal time.

Figure 4 : Keypad Configuration 12Key Mode (tone mode).

1	2	3
4	5	6
7	8	9
* STORE DIAL	0 LND	# PAUSE

MBBMK5376-01

Buffering data into the RAM before signaling is an important feature. This allows less expensive keypads to be used since users cannot enter digits too quickly for the system and the PACIFIER TONE can provide audible feedback after each non-toned key entry. It also guarantees that data stored in the RAM exactly matches the digits actually dialed.

Users can perform consecutive manual and auto-dialing, if auto-dialing is used to accomplish only a part of the desired number sequence. However, manual and auto-dialing cannot be performed simultaneously.

NORMAL DIALING

D	*	*	D	D

In 12KEY Mode, the "*" (Star) key is the modifier used to control repertory functions. All numeric keys signal normally unless a modifier precedes them. To signal either a "*" or "#" users must enter these keys twice in succession. The first entry is not signaled or stored.

LND PRIVACY

D	D	ON-HOOK	*	#

A "*", # input after going on-hook or prior to coming off-hook with erase information stored in the LND buffer.

AUTO-DIALING (Off-hoof))

D	D	...	D	*	N
opt	opt		opt		

The key sequence "*" followed by any digit auto-dials the number sequence stored in the designated address location. Note auto-dial can take place following manual key inputs.

STORAGE (On-hook)

D	D	...	D	*	N
opt	opt		opt		

The number sequence stored in the LND buffer can be transferred to one of the nine other "permanent" locations with the simple sequence "*" followed by the address. New digits may be written into the LND buffer while on-hook. To enter a "*" signal, users enter the "*" key twice in succession as when dialed off-hook.

PABX PAUSE (Off-hook and On-hook)

D	D	*	#	N

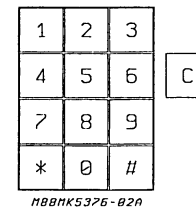
When users input "*" key followed by a "#", an indefinite pause is stored in a number sequence. Upon redialing the number sequence, the dialer will pause when it encounters "#". A key input makes it continue.

KEYPAD CONFIGURATION 12KEY MODE (pulse mode)

Most of the Pulse key operations are identical to those in the 12KEY Tone Mode ; PABX Pause is the only exception. In Pulse Mode, the pause is stored with a single "#" input. Two "#" inputs store two pauses.

The "*" key exercises the control function ; two "*" inputs are the same as a single input (multiple inputs are not accepted).

Figure 5 : Keypad Sequence 13Key Cofiguration.



NORMAL DIALING AND LND PRIVACY OPTION (Off-hook)

D	D	D	....ETC	C

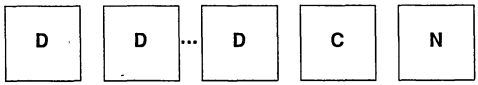
Normal dialing is straightforward ; all keypad entries are stored in the LND (Last Number Dialed) buffer and signaled as each is entered. All digits in the LND register are maintained unless the final key prior to going on-hook is "C". In the metal mask version, the LND buffer is cleared unless users make a Control entry before going on-hook.

AUTO-DIALING (Off-hook)

C	N	ADDRESS

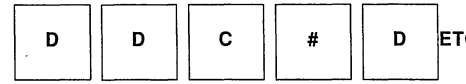
To auto-dial, users enter the control key "C", followed by the address key, (shown here as "N", representing memory location N). As soon as the address key is decoded and debounced, auto-dialing begins. Address zero is used to auto-dial LND.

STORAGE (On-hook)



To store data in a given location (LOC N) users simply enter digits into the LND buffer and copy them to "N" by entering a control key "C" followed by the desired address. Users can copy the last number dialed before going on-hook to another location if they make no entries before the copy operation.

PABX PAUSE



Users may inject a pause at any point in the dialed sequences by keying in "C" followed by "#". When this number sequence is redialed, the dialer pauses indefinitely and continues to dial when another key input is received.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	– 30 to + 60	°C
Storage Temperature	– 55 to + 85	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	(V+) + 0.3, (V–) – 0.3	V

* All specifications are for 2.5 V operation and full operating temperature range unless otherwise stated.

ELECTRICAL OPERATING CHARACTERISTICS

DC CHARACTERISTICS – 30 °C ≤ TA ≤ 60 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+	DC Operating Voltage	2.5		6.0	V	
I_{SB}	Standby Current		0.3	1.0	µA	1
V_{MR}	Memory Retention Voltage	1.5			V	5
I_{MR}	Memory Retention Current	750	200		nA	5
I_T	Operating Current (tone)		0.5	1.0	mA	2
I_P	Operating Current (pulse)		50	150	µA	2
I_{ML}	Mute Output Sink Current	1.0	3.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	3.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	Keypad Pulldown Resistance		500		kΩ	

Notes : 1. All inputs unloaded. Quiescent Mode (oscillator off).
2. All inputs unloaded. single key input.
3. V_{OUT} = 0.5 V.
4. Sink Current for V_{OUT} = 0.5 Source Current for V_{OUT} = 2.0 V.
5. Meeting these minimum supply requirements guarantees the retention of data stored in memory.

ELECTRICAL OPERATING CHARACTERISTICS (continued)

CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T_{KD}	Keypad Debounce Time		32		ms	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		ms	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone		30		ms	1
F_{RC}	Frequency RC Oscillator	– 7.0	+ 2.5	+ 7.0	%	2

Notes : 1. Times based upon 8 kHz RC input for RATE CONTROL.
2. Deviation of oscillator frequency takes into account all voltage, temperature and unit-to-unit variations, but does not include the tolerance of external components.

CHARACTERISTICS – TONE MODE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T_{NK}	Tone Output no Key Down			– 80	dBm	1
T_{Od}	Tone Output (dependent)	– 13 173	– 12 194	– 11 218	dBm mV(rms)	1, 2
P_{Ed}	Pre-emphasis, High Band		2.7		dB	
V_{DCd}	Average DC Bias Tone out (V+ = 2.5 V)		1.2		V	
T_{Oi}	Tone Output (independent)		– 12 194		dBm mV(rms)	2, 3
P_{Ei}	Pre-emphasis, High Band		2.0		dB	3
V_{DCi}	Average DC Bias Tone out		1.5		V	
DIS	Output Distortion		5.0	8.0	%	3
R_E	Tone Output Load			10	kΩ	4
TR	Tone Signaling Rate		5	10	1/sec	5
PSD	Pre-signal Delay		132		ms	5
ISD	Inter-signal Delay		100		ms	5

Notes : 1. ODBm equals 1 mWatt signal power into a 600 W load or 775 mV.
2. Single tone (low group) V = 2.5 V.
3. Supply voltage = 2.5 to 6 V. R_E = 10 KΩ.
4. Maximum load which can be connected externally to pin 10 and maintain proper tone levels.
5. These values are directly related to the RC component values connected to Pin 7, the rate control frequency is nominally 8 kHz.

AC CHARACTERISTICS – PULSE MODE OPERATION

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
P_R	Pulse Rate		10		PPS	1
PDP	Predigital Pause		172		ms	1
IDP	Interdigital Pause		940		ms	1
T_{MO}	Mute Overlap Time		2		ms	1

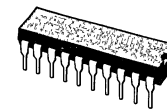
Note : 1. Typical times assume nominal RC input frequency of 8 kHz. An increase in frequency results in an equal decrease in time values and increase in rate values.

SGS-THOMSON MICROELECTRONICS

MK53721

TONE/PULSE WORLD DIALER WITH LNR

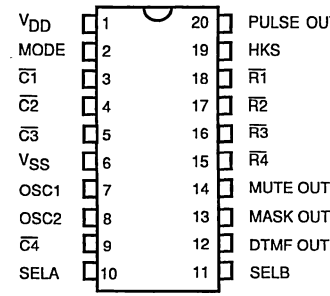
- TWO SELECT PINS ALLOW THE USER TO SELECT 16 DIFFERENT COUNTRY OPTIONS
- SINGLE CHIP MIXED MODE DIALER ALLOWS DIALING IN EITHER TONE OR PULSE MODES. A * OR "SOFTSWITCH" KEY INPUT CAN ALSO BE USED TO SWITCH FROM PULSE TO TONE MODE OPERATION AND IS STORED IN MEMORY
- 28 DIGIT STORAGE WITH LNR (last number redial)
- P.I.N. (personal identify number) PROTECTION METHOD
- SLIDING CURSOR METHOD TO SIMPLIFY PABX DIALING
- HOOKSWITCH DEBOUNCE, TRANSIENTS DUE TO LINE REVERSALS AND DROP-OUTS CAN BE MASKED FOR A PERIOD DETERMINED BY EXTERNAL RC
- POWERED FROM TELEPHONE LINE, LOW STANDBY CURRENT AND OPERATING VOLTAGE
- DTMF SIGNAL CONSISTENT WITH KEY ENTRY PERIOD
- MINIMUM DTMF SIGNAL DURATION/SEPARATION GUARANTEED
- TIMED PABX PAUSE MAY BE STORED IN MEMORY
- TIMED FLASH FOR EXTENDED TIMED BREAK RECALL



DIP20

ORDER CODE : MK53721N00

PIN CONNECTION



DESCRIPTION

The MK53721 is a 20 pin CMOS mixed mode dialer IC. This dialer provides signalling for both TONE (DTMF) and PULSE (LD) modes of operation. All digits entered are stored in a 28-digit buffer and can be recalled with a single LNR (last number redial) command entry.

The MK53721 can be switched from PULSE to TONE mode operation through the keypad with a */# key input or softswitch (SS) key input. All key inputs following a softswitch command will generate DTMF signals.

KEYPAD CONFIGURATION

1	2	3	FLASH
4	5	6	SS
7	8	9	PAUSE
★	0	#	LNR

DESCRIPTION (continued)

Two select pins (SELA, SELB) have been provided which allow the part to be customized for various markets. Rather than selecting and modifying individual parameters which would take many pins or mask options each select pin will select groups of options which have been identified for particular markets.

The MK53721 features a Sliding Cursor, Auto-Pause insertion (on some options), manual Pause, and Flash. The DTMF tone output has a guarenteed minimum duty cycle and extends to match the duration of key inputs.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	0 to 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25°C)	500	mW
Maximum Voltage on any Pin	(VDD) +.3, (VSS) –.3	V

DC ELECTRICAL CHARACTERISTICS(Ta = 25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
VDDT	DC Operating Voltage Tone Mode	2.5		6.0	V	
VDDP	DC Operating Voltage Pulse Mode	2.0		6.0	V	
VMR	Memory Retention Voltage	1.5	1.3		V	4,5
VMT	Mute Operation	1.8			V	
IDDP	Operating Current Pulse Mode		.800	1.2	mA	2
IDDT	Operating Current Tone Mode		.900	1.2	mA	2
ISS	Standby Current		0.4	1.0	µA	1
IMR	Memory Retention Current		0.2	0.8	µA	1,5
ISINK	Pulse/Mute/Mask Output Sink Current	1.0			mA	3
VOL	Output Low Voltage (ISINK = 1mAMP)			0.5	V	
KRU	Keyboard Pullup Resistance	50	100	200	kΩ	
KRD	Keyboard Pulldown Resistance	100	500	1000	Ω	
VIL	Input Level Low			.2VDD	V	
VIH	Input Level High	.8VDD			V	

Notes : 1. All inputs unloaded. Quiescent mode (oscillator off).
2. All outputs unloaded, single key input.
3. Vout = 0.4 Volts.
4. Memory retention voltage is the point where memory is guaranteed but circuit operation is not.
5. Proper memory retention is guaranteed if either the minimum Imr is provided or the minimum Vmr. Both are not needed simultaneously.

AC ELECTRICAL CHARACTERISTICS(TA = 25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
TNK	Tone Output no Key Down			– 80	dBm	6
TO	Tone Output (low group)	– 13 173	– 12 194	– 11 218	dBm mVrms	6, 7, 8
VPE	Pre-emphasis 20 log [VCOL/VROW]	2.0		2.75	dBm	
TDC	Tone DC Bias		1.6		V	
TLOAD	Tone Output Load			10	kΩ	
TRIS	Tone Output Rise Time		1.0		msec	9
TDIS	Tone Distortion		5.0	8.0	%	8

Notes : 6. 0 dBm equals 1mWatt into 600Ω or 775mV. The MK53721 is designed to drive a 10kOhm load. The 600Ω load is only for reference.
7. Single tone (low group), as measured at pin 12.
8. Supply voltage from 2.5 to 6.0V. Rload = 10kOhms.
9. Time from beginning of tone output waveform to 90% of final magnitude.

TIMING SPECIFICATIONS (TA = 25°C unless otherwise noted)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
TKD	Keyboard Debounce Time		24		mSEC	
FKS	Keyboard Scan Frequency		250		Hz	
TPSD	Tone Presignal Delay			40	mSEC	
THFP	Hookflash Break Period	See table "A-Options"			mSEC	
TISD	Tone Intersignal Delay				mSEC	10
TDUR	Tone Burst Duration				mSEC	10
PPS	Pulses per Second (pulse rate)				PPS	10
PDP	Predigital Pause				mSEC	10
IDP	Interdigital				mSEC	10
TMO	Mute Overlap Pulse		TM		mSEC	10/11

Notes : 10. The values of these parameters are dependent upon the option selected by SELA and SELB pins, see option tables A and B for timing values.
11. TM = Make Time ; 32 mS or 40 mS depending upon option selected.

PIN DESCRIPTIONS

Pin #	Pin Name	Description
1 6	VDD VSS	Positive Supply Negative Supply (ref for all voltages)
8 9	OSC1 OSC2	Oscillator Input for 3.579545MHz Crystal Oscillator Output
2 10 11 19	MODE SELA SELB HKS	Selects TONE or PULSE Default Operation Select Option Group A1-A16 by Connecting this Pin to the Appropriate Row or Col Selects Option Group B1-B8 Hookswitch Detect, Logic 1 = 'off-hook'
12 13 14 20	DTMF OUT MASK OUT MUTE OUT PULSE OUT	DTMF Output NPN Emitter Follower Mask Output for Pulse Mode Operation, Nch Open Drain,Active High Mute Output for Tone Mode Operation, Nch Open Drain, Active High PULSE Output for Precise Break Timing, Nch Open Drain, Active High
3 4 5 9	-COL1- -COL2- -COL3- -COL4-	Column Keypad Connections
18 17 16 15	-ROW4- -ROW3- -ROW2- -ROW1-	Row Keypad Connections

TIMING DIAGRAMS

Figure 1 : Tone Mode Timing.

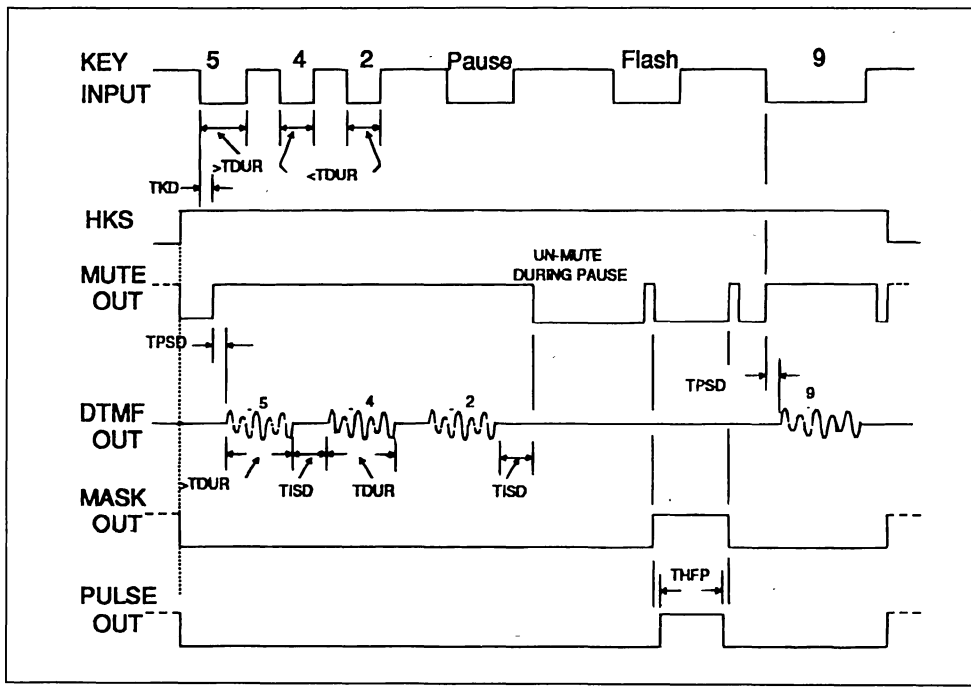
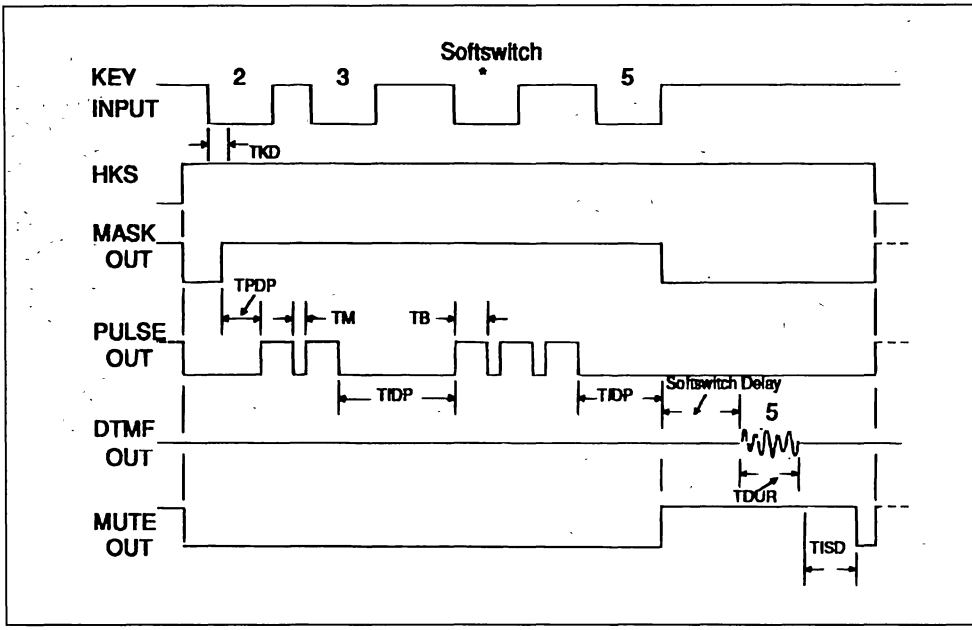


Figure 2 : Pulse Mode Timing.



GENERAL DESCRIPTION

A-OPTIONS

The SELA pin is used to select groups of parameters and modify the operation of some of the special features. These groups are tailored for specific users. A major benefit of this approach simplifies the design of telephones for the international market. The option groups are selected by connecting the SELA pin (number 10) to one of the row or column pins for a total of eight possible choices. The Sel-B option pin further defines an additional group of A-options by connecting the Sel-B pin to either a column, for options A1-A8, or to a row, for options A9-A16. Options can only be changed while "on-hook".

Table 1 : A Options.

OPT	PIN	PPS	M/B	PDP	IDP	FLSH	TONE	Functions
A1	-ROW4-	10	40/60	840	840	100	80/80	API, SS★SS, FT = True
A2	-ROW3-	10	32/68	240	840	100	98/98	FT = True
A3	-ROW2-	10	32/68	240	840	300	80/80	SS★# = True, ★#PIN = True
A4	-ROW1-	10	32/68	240	840	100	80/80	SS★# = True, ★#PIN = True
A5	-COL1-	16	40/60	240	840	600	98/98	
A6	-COL2-	10	32/68	240	840	100	80/80	New Zealand Style Keypad
A7	-COL3-	10	40/60	240	540	100	80/80	Swedish Style Keypad
A8	-COL4-	10	40/60	240	840	600	80/80	
A9	-ROW4-	10	40/60	240	840	100	80/80	
A10	-ROW3-	20	32/68	240	840	100	98/98	FT = True
A11	-ROW2-	10	32/68	540	540	100	70/140	DM, SS★#, ★#PIN = True
A12	-ROW1-	10	32/68	240	540	300	80/80	DM = True
A13	-COL1-	10	32/68	240	840	100	80/80	API, FT = T
A14	-COL2-	10	40/60	240	840	300	98/98	Flash Option = F2
A15	-COL3-	10	40/60	840	840	100	80/80	
A16	-COL4-	20	40/60	240	540	600	80/80	

The default settings for any group, unless specified otherwise in the FUNCTIONS column is :
API = False, DM = False, SS*# = False, PIN = True, FT = False, Flash Option = F1, D*#P = False,
Sweden keypad = False, New Zeland = False.

DEFINITIONS
TONE xx/yy : xx = Tone duration (TDUR), yy = Tone intersignal delay (TISD)
API = autopause insertion (True, False)
DM = data mode, memory bypassed and part xmits tones as simple DTMF generator.
SS*# = transmit * or # key on input, even in pulse mode (True, False).
SS*SS = Softswitch sequence [bi-directional] required by Germany (True, False).
PIN = personal id number protection (True, False)
*#PIN = PIN protection is ignored if * or # is the first digit (True, False).
FT = flash can only be used in Tone mode (True, False)
F1 = flash option 1, keys following a flash will begin new sequence
F2 = flash option 2, keys following flash will be appended to current sequence and cannot be recalled.

The first group of A-Options are selected by B-options B1 through B4.

A1 : OPEN
A2 : UK
A3 : FRANCE (PUBLIC)
A4 : FRANCE (PRIVATE)
A5 : PANAMA/COLOMBIA (S. AMERICAN COUN-TRIES)
A6 : NEW ZEALAND
A7 : SWEDEN/SOME OF NORWAY
A8 : USA - 10PPS

The second group of A-Options are selected by B-options B5 through B8.

A9 : HOLLAND/DENMARK
A10 : BELGIUM
A11 : SPAIN
A12 : FRANCE (Data mode)
A13 : AUSTRALIA
A14 : ISRAEL
A15 : ITALY
A16 : USA - 20PPS

B-OPTIONS

SELB pin is used to select a default pulse rate and also determine the fixed delay time used for the PAUSE command.

There are four alternatives to choose from. Options can be changed only when "on-hook".

Table 2 : B Options.

Option	Pin	A- OptionsGroup	Pause Duration(sec)
B1	-COL1-	A1-A8	IDP + 1.1 + IDP
B2	-COL2-		IDP + 3.1 + IDP
B3	-COL3-		IDP + 6.0 + IDP
B4	-COL4-		Indefinite
B5	-ROW1-	A9-A16	IDP + 1.1 + IDP
B6	-ROW2-		IDP + 3.1 + IDP
B7	-ROW3-		IDP + 6.0 + IDP
B8	-ROW4-		Indefinite

KEYBOARD INTERFACE

The MK53721 has eight keyboard interface pins which are to connected to a 4 x 4 keypad with FORM A (SPST) switches. A 2-of-8 keyboard with negative common may also be used.

The keyboard is disabled while "on-hook". Off-hook, the column and row keys assume opposite logical states. Keyboard scan is enabled when a valid input is detected. The scan frequency is 250Hz.

On hook, the keypad inputs are disabled eliminating possible current draw in this state. Off hook, the keypad inputs are enabled. A key entry, connecting a single column pin to a single row pin, is detected and the oscillator is activated. The keypad is scanned and debounced to verify the key input and the data is then stored into the LNR buffer (if storable).

HOOKSWITCH INPUT

The HKS INPUT (HOOKSWITCH) informs the MK53721 of the state of the telephone. A logic "1" (connected to VDD) indicates the telephone set is in the "off-hook" state and dialing is enabled. A logic "0" (connected to VSS) indicates the telephone set is "on-hook", dialing is disabled, and the chip will not draw extra current if keys are depressed. This ensures that only the memory retention current is required while on hook.

The HKS INPUT is level sensitive which simplifies the implementation of hookswitch debounce. Transients caused by interruptions in loop current during exchange operations will not cause inadvertant "on-hook" detection. The length of debounce is determined by the value of a the pullup resistor and capacitor connected externally. The suggested debounce periods range from 50msec to 500msec. A valid hookswitch transition will terminate signalling in progress and reset the dialing mode to the default mode determined by the MODE INPUT (pin 2). The HKS debounce time is determined by the following equation :

$$T(HSDB) = 0.75 \times REXT \times CEXT$$

EARTH LOOP RECALL (ELR OR GND KEY)

Earth loop recall is not generated by the MK53721 but can be detected by applying a logic "0" level directly to the hookswitch. The hookswitch debounce is bypassed by applying logic levels directly to the HKS pin (input not connected through external resistor). The ELR or GND KEY detect is identical to a hookswitch input without the debounce. Any digits dialed after ELR or GND key will reset the memory and be treated as a new number in the LNR buffer.

LAST NUMBER REDIAL

LNR (last number redial) command causes the contents of the LNR buffer to be dialed. Numbers which include a softswitch are limited by P.I.N. protection described below. LNR does not have to be the initial key input since the MK53721 features a "sliding cursor" dialing method.

The LNR buffer can store 28 digits but any number of digits may be dialed manually. The memory storage will wrap-around after the first 28 digits have been entered and the additional inputs will be stored beginning in the first memory location. After wrap-around has occured the LNR command will be disabled to prevent misdials.

FLASH

The FLASH command is stored in the LNR buffer and when signaled it initiates a timed break. This timing is determined by the options selected. Flash option F1 will reset the memory after a flash and additional inputs will begin a new number sequence. If this option is selected new digits will not be accepted until the FLASH is completed.

Flash option F2 will continue accepting inputs and storing these sequentially in the buffer. These digits cannot be redialed.

In both cases, signalling will revert to the default dialing mode determined by the MODE INPUT following the FLASH command execution and the FLASH itself is never redialed.

Mask out during Flash = Tpdp + Flash duration + Tidp.

Table 3 : Flash Key Options.

Mode	Key Input	Output	Description
T/P	1 2 3 F 4 5	1 2 3 F 4 5	Manual Dial, Flash Key
T/P	LND	4 5	Redial, Flash Option F1
T/P	LND	1 2 3	Redial, Flash Option F2
T/P	1 2 3 4 5	1 2 3 4 5	Normal Dial
T/P	F	F	Flash Dial
T/P	LND	1 2 3 4 5	Redial, Flash Option F1, F2
T/P	1 2 3 4 5 F	1 2 3	1 2 3 4 5
T/P	LND	1 2 3 4 5 F	Manual Dial, Flash Key Term

SLIDING CURSOR

The sliding cursor feature simplifies PABX access and redial. The MK53721 will compare all digits as they are entered to the previous memory contents.

If all digits entered equal the memory contents the LNR command can be activated at any point in the dialing sequence and the remaining data will be redialed. LNR is inhibited if there is a digit mismatch.

Table 4 : Sliding Cursor Operation.

Mode	Key Input	Output	Description
T/P	1 2 3 4 5	1 2 3 4 5	Normal Dial
T/P	LND	1 2 3 4 5	Redial
T/P	1 2 3 LND	1 2 3 4 5	Sliding Cursor
T/P	1 2 4 LND	1 2 4	Sliding Cursor, Invalid
T/P	12	1 2	Normal Dial
T/P	LNR	1 2	Redial of Last Number Dialed

SOFTSWITCH, P.I.N. PROTECTION

Softswitch feature allows the dialing mode of the dialer to be switched from Pulse Mode to Tone Mode operation with a key input. Two methods are available to accomplish this, first is the SS key and second is the * or # key while in Pulse mode.

The P.I.N. (PERSONAL IDENTIFY PROTECTION) feature of the MK53721 will protect numbers which are likely to be used in confidential transactions. Digits entered after a * or # key in TONE mode, or "softswitch" command (either a * input or SS input while in PULSE mode) are considered private. These digits cannot be redialed and therefore the users privacy is not compromised. The exception to this is a * or # key at the beginning of a sequence, in this case redial of the entire sequence is allowed.

Table 5 : Softswitch Operation.

Mode	Key Input	Output	Description
PULSE	1 2 3 ★ 4 5	1 2 3 <TDMF> 4 5	Softswitch, SS ★ # = False
PULSE	1 2 3 ★ 4 5	1 2 3 <TDMF>★ 4 5	Softswitch, SS ★ # = True
PULSE	1 2 3 SS 4 5	1 2 3 <TDMF> 4 5	Softswitch
PULSE	LNR	1 2 3	PIN = True
PULSE	★ 1 2 3 ★ 4 5	<TDMF> 1 2 3 ★ 4 5	Softswitch, SS ★ # = False
PULSE	LNR	<TDMF> 1 2 3	PIN invalid for ★ key first, SS★ # = False
PULSE	★ 1 2 3 ★ 4 5	<TDMF>★ 1 2 3 ★ 4 5	Softswitch, SS ★ # = True
PULSE	LNR	<TDMF>★ 1 2 3 ★ 4 5	PIN invalid for ★ key first, SS★ # = True
TONE	1 2 3 ★ 4 5	1 2 3 ★ 4 5	Manual Dial ★ Key
TONE	LNR	1 2 3	PIN =True
TONE	★ 1 2 3 ★ 4 5	★ 1 2 3 ★ 4 5	If firest key is ★ or # , then ★ , # is redialed
TONE	LNR	★ 1 2 3 ★ 4 5	SS★ # = True
TONE	LNR	★ 1 2 3	SS★ # = False

PAUSE

The PAUSE command is used to insert a fixed time delay into a number sequence. The dialer will delay a fixed time when redialing the number. The delay is programmable with the SELB option pin. If an indeterminate delay is selected the dialer will stop during redial at the point where the PAUSE function was entered. Auto-dialing is resumed by entering the PAUSE key.

An AUTO-PAUSE INSERTION (API) feature is also available as an option. The pause is inserted automatically into a number sequence if manual dialing is interrupted by a delay of more than one second following the signaling of the last digit entered if in tone mode operation. In Pulse mode operation, the delay will be inserted automatically if a manual digit has not been entered within an IDP time following the completion of the previous digit. Not more than two APIs' will be entered for each number sequence.

Table 6 : Pause Operation.

Mode	Key Input	Output	Description
T/P	1 2 3 ... 4 5	1 2 3 4 5	Manual Dial with Delay
T/P	LNR	1 2 3 ... 4 5	Redial, Pause Inserted if Autopause = True
T/P	1 2 3 P 4 5	1 2 3 P 4 5	Manual Dial, Pause Key Input
T/P	LNR	1 2 3 P 4 5	Redial, PAUSE <> Ind
T/P	LNR	1 2 3	Redial, PAUSE = Ind
T/P	PAUSE	4 5	Complete Redial

DATA MODE

The DATA MODE feature allows the MK53721 to be put into a mode where it operates just like a simple tone dialer, for entering long sequences of tones to a remote service without disturbing the LNR buffer. If the DM option is selected, all digits entered after a * or # key will be toned out with no minimum tone duration, and will not clear the LNR buffer regardless of how many digits are output.

Table 7 : Data Mode Option.

Mode	Key Input	Output	Description
T	1 2 3 ★ 4 5 ... N	1 2 3 ★ 4 5 ... N	Data Mode (DM) Active After ★ or #
T	LNR	1 2 3	Digits before DM are redialed.
T	★ 1 2 3 ★ 4 5 ... N	★ 1 2 3 ★ 4 5 ... N	DM activated on first ★ entry.
	LNR	★	Only ★ is redialed.
P	1 2 3 ★ 4 5 ... N	1 2 3 <T> ★ 4 5 ... N	Softswitch to DM on ★ or #, SS ★ # = True
P	1 2 3 ★ 4 5 ... N	1 2 3 <T> 4 5 ... N	Softswitch to DM, SS ★ # = False
P	LNR	1 2 3	Digits before DM are redialed.
P	★ 1 2 3 ★ 4 5 ... N	<T> 1 2 3 ★ 4 5 ... N	SS ★# = False
P	LNR	<T>	SS ★ # = False, softswitches but nothing redialed.
P	★ 1 2 3 ★ 4 5 ... N	<T> ★ 1 2 3 ★ 4 5 ... N	SS ★ # = True
P	LNR	<T> ★	SS ★ # = True

DTMF OPERATION

The DTMF OUTPUT is driven by a bipolar (NPN) emitter follower with the collector tied to VDD. The DTMF OUT signal is a summation of the keyboard selected High group (column) and Low group (row) tones. The amplitude of these tones is determined internal to the chip and is independent of supply.

The tones are synthesized using a resistor tree with sinusoidally weighted taps. The frequency and accuracy of the synthesized tones is listed in the table 8. Note, variations in the oscillator frequency (using the 3.579545MHz crystal) will be reflected in the frequency of the synthesized tones.

Single tone may be generated when using options A8 or A16, by symultaneously pressing two buttons in the same row or column.

Table 8 : DTMF Output Frequencies.

Key Input	Standard Frequency	Actual Frequency	% Deviation from Standard
-ROW1-	697	699.1	+ 0.31
-ROW2-	770	766.2	− 0.49
-ROW3-	852	847.4	− 0.54
-ROW4-	941	948.0	+ 0.74
-COL1-	1209	1215.9	+ 0.57
-COL2-	1336	1331.7	− 0.32
-COL3-	1477	1471.9	− 0.35

PULSE OPERATION

In Pulse operation the MK53721 converts keypad inputs into a series of pulses to simulate a rotary dialer. The Pulse Output becomes active following the debounce period and a short predigital pause period. A Mask Output is provided to remove the speech network form the line or to attenuate the current spikes which reach the receiver when Pulse dialing. The Mask output goes active a predigital pause prior to the first break and remains active until an IDP period following the output of the last digit from the buffer. The nominal pulse output rate is 10pps although this is selectable by the Select Option pins.

In pulse mode operation the number of pulses associated with each key can be modified to meet standards of nations such as Sweden, some of Norway, and New Zealand. These options are available through the SELA and SELB input pins.

Table 9 : Pulse Output Options.

Normal		Sweden		New Zealand	
0 . . .	10 Pulses	0 . . .	1 Pulse	0 . . .	10 Pulses
1 . . .	1 Pulse	1 . . .	2 Pulses	1 . . .	9 Pulse
2 . . .	2 Pulses	2 . . .	3 Pulses	2 . . .	8 Pulses
3 . . .	3 Pulses	3 . . .	4 Pulses	3 . . .	7 Pulses
4 . . .	4 Pulses	4 . . .	5 Pulses	4 . . .	6 Pulses
5 . . .	5 Pulses	5 . . .	6 Pulses	5 . . .	5 Pulses
6 . . .	6 Pulses	6 . . .	7 Pulses	6 . . .	4 Pulses
7 . . .	7 Pulses	7 . . .	8 Pulses	7 . . .	3 Pulses
8 . . .	8 Pulses	8 . . .	9 Pulses	8 . . .	2 Pulses
9 . . .	9 Pulses	9 . . .	10 Pulses	9 . . .	1 Pulses
★ . . .	Softswitch	★ . . .	Softswitch	★ . . .	Softswitch
# . . .	Ignored	# . . .	Ignored	# . . .	Ignored

TYPICAL APPLICATIONS

The MK53721 is a single chip Tone Pulse World Dialer with 28-digit last number redial, which provides the necessary signals for DTMF (tone) or loop disconnect (pulse) dialing. The typical application circuit shown in figure 3 illustrates one way the MK53721 Tone Pulse dialer can be used with an integrated speech circuit to produce a multi-standard telephone. The circuit is connected to the telephone line through a polarity guard integrated circuit that assures proper voltage polarity to the circuit, regardless of telephone line polarity, as well as limiting the voltage at the polarized side. The 2-to-4 wire conversion, muting of the transmitter and receiver, and provision of regulated supply voltage to the MK53721 is accomplished using an SGS-THOMSON L3280 integrated speech circuit. The L3280 also takes the MK53721 DTMF output and modulates the line with that signal. Because of the various World Dialer timing options selectable with the MK53721, the application can be easily adapted to meet the standards of almost any country.

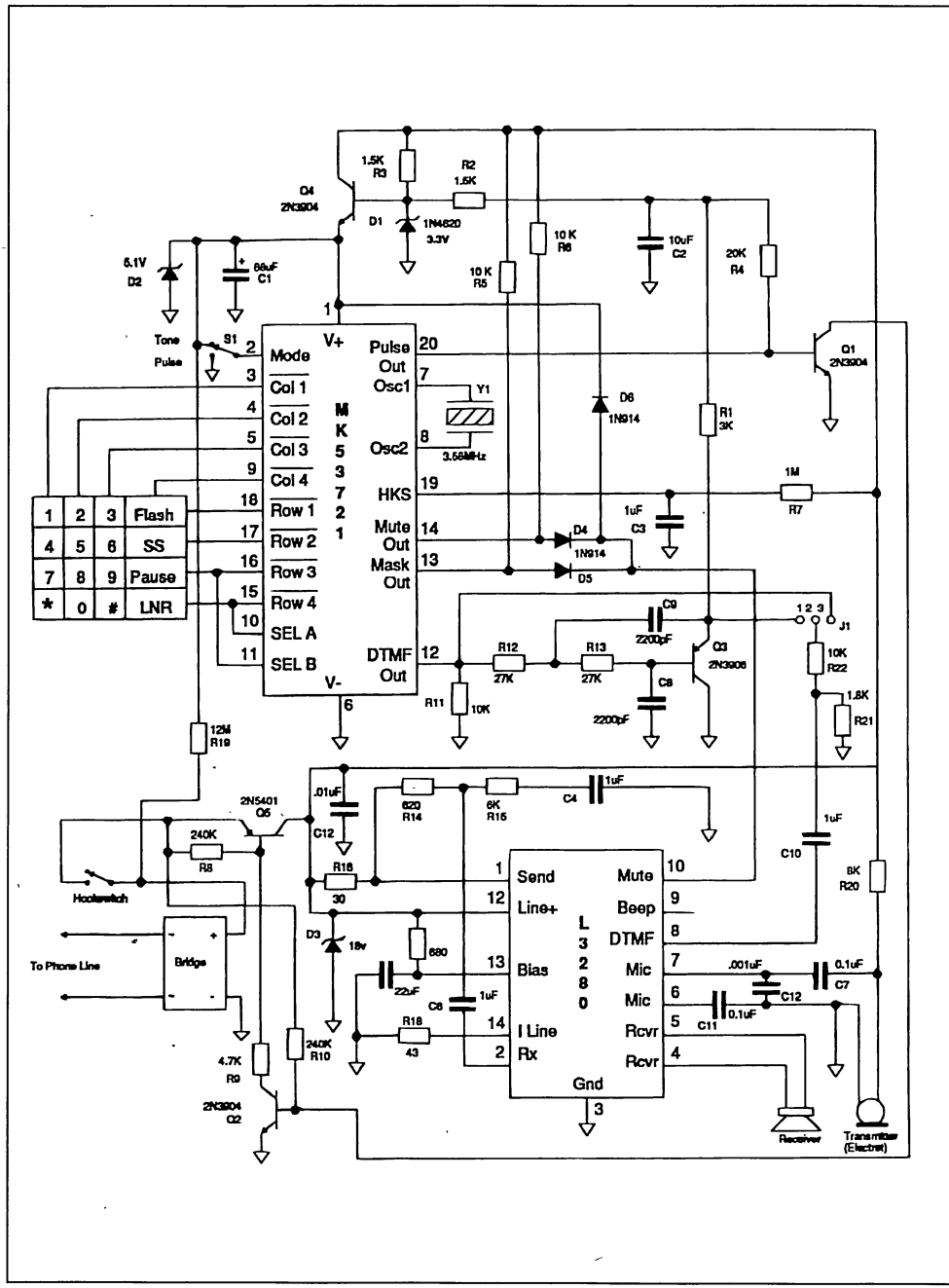
In this circuit, Pulse dialing (which consists of a series of momentary interruptions of loop current) is achieved by the Pulse output of the MK53721 controlling transistor Q1,Q2 and Q5 to break and make the loop current through the speech network. The MK53721 MASK output provides the logic level to the L3280 MUTE input to cause muting of the loud pops which would otherwise be heard at the receiver due to the pulsing of the loop current through the speech network.

Tone signalling requires that the loop current be modulated with the appropriate DTMF signal. The DTMF output of the MK53721 is coupled to the DTMF driver circuitry of the L3280 via a filter network comprised of C8, C9, R12, R13 and Q3. The jumper J1 allows the user to select whether or not to use the filter network required to meet some country specifications. The MK53721 MUTE output provides the logic level to the L3280 MUTE input to mute the transmitter and reduce to an acceptable level the tone heard at the receiver.

The mode of operation (Tone or Pulse) is controlled by switch S1. In Pulse Mode, the Softswitch key (SS or * key) can be used to change from Pulse to Tone Mode. Going on-hook and back off-hook will cause the MK53721 to revert to the mode selected by the S1, but the Softswitch function can be redialed. The signalling mode may be changed at any time, so as to allow mixed Pulse and Tone dialing.

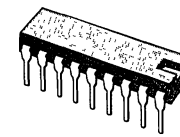
The current required for long term memory retention with the MK53721 is typically 0.3uA. A battery is therefore not required if a resistor is used to provide the small amount of memory retention from the line when on-hook.

Figure 3 : MK53721 Typical Application.



SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

- SINGLE CHIP DTMF AND PULSE DIALER
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- RECALL OF LAST NUMBER DIALED (up to 28 digits long)
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- TIMED PABX PAUSE
- 8 TONES PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION GUARANTEED (74/54 ms)
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS



DIP18

ORDER CODE : MK53731N00

Figure 1 : Pin Connection (top view).

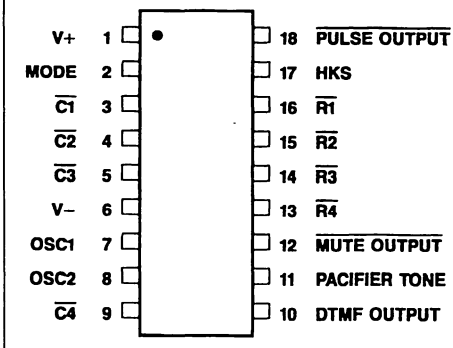


Figure 2 : Keypad Configuration.

1	2	3	FLASH
4	5	6	SOFT SWITCH
7	8	9	PAUSE
* SOFT SWITCH	0	#	LND

M88MK53731-01

DESCRIPTION

The MK53731 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53731 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch, Flash, and Pause. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed.

Two features simplify PABX dialing. The pause key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signalling resumes. The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

FUNCTIONAL PIN DESCRIPTION

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see Electrical Specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V– connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard inputs. The MK53731 interfaces with either the standard 2-of-8 with negative common or the single-contact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs are pull high through on-chip pull-up resistors.

In the tone mode, if 2 or more keys in the same row or if 2 or more keys in the same column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes, and single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table 1.

Table 1. Output Tone Duration.

Key – Push Time, T*	Tone Output*
$T \leq 32$ ms	No Output. Ignored by MK53731.
32 ms $\leq T \leq$ 75 ms + T_{DK}	75 ms Duration Output.
$T \geq 75$ ms + T_{KD}	Output Duration = $T - T_{KD}$

* **Note :** T_{KD} is the keypad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75 ms duration, and the tone separation (intersignal delay) is 50 ms.

V–

Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Pin 7 (input), pin 8 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ±0.25 % may also be used.

DTMF OUTPUT

Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53731 is designed to operate from an unregulated supply ; the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{01} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation :

$$V_{DC1} = 0.3 \text{ V+} + 0.5 \text{ Volts}$$

Figure 3 : MK53731 Block Diagram.

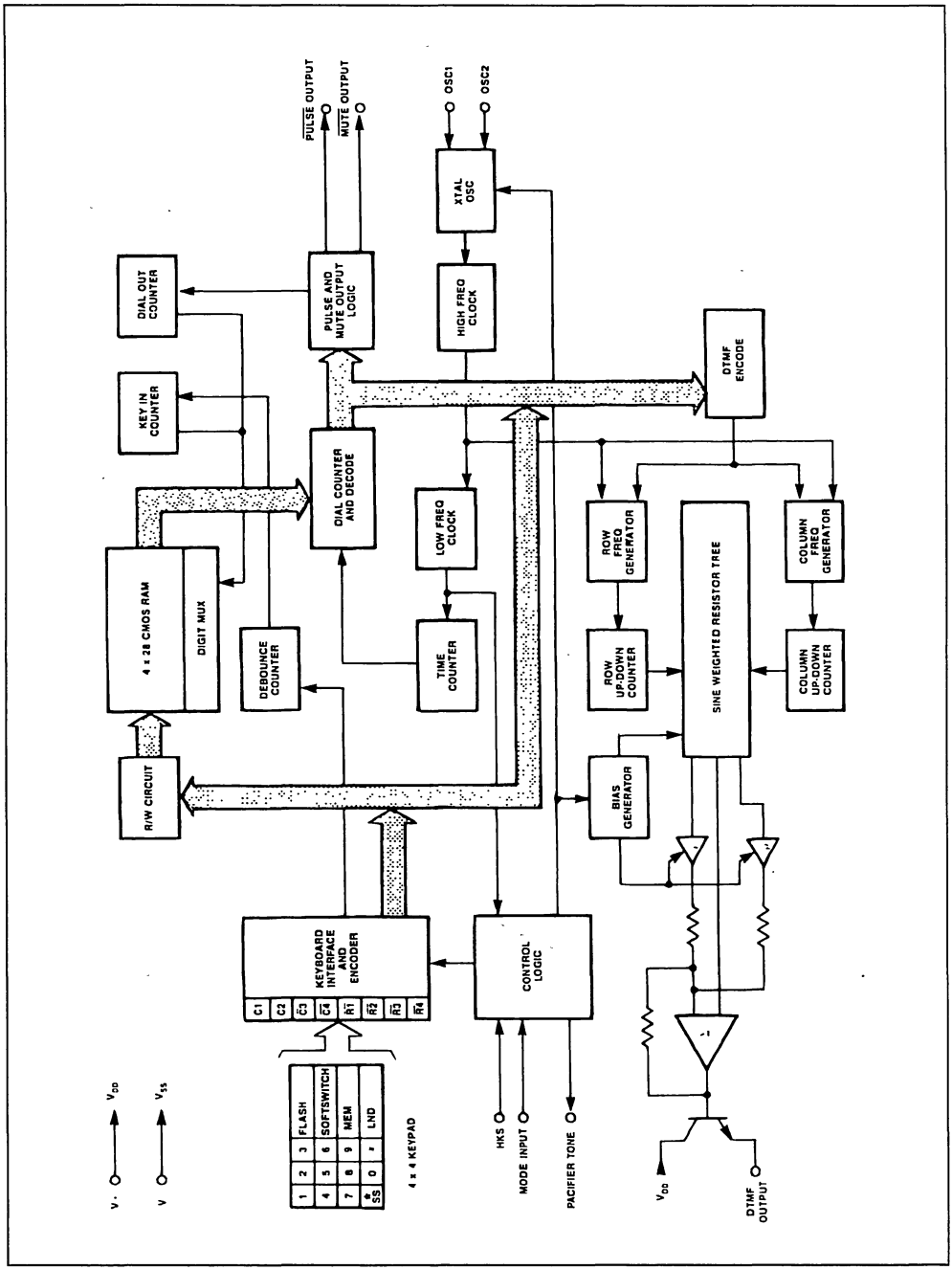


Figure 4 : Typical Single Tone.

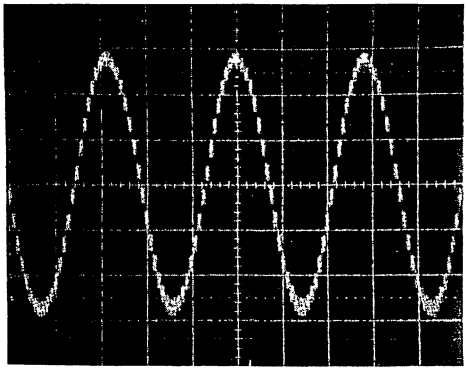


Figure 5 : Typical Dual Tone.

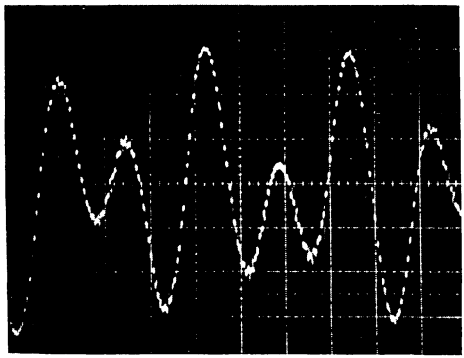
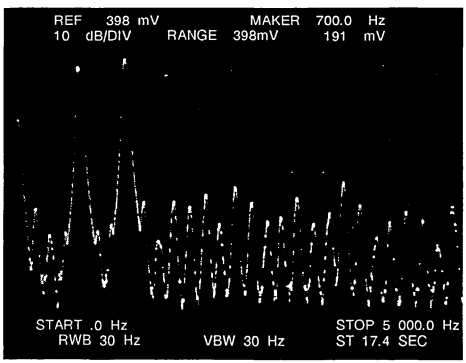


Figure 6 : Typical Spectral Response.



PACIFIER TONE

Output. Pin 11. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all valid key entries activate the pacifier tone. In tone mode, any non-DTMF (FLASH, PAUSE, LND, SOFTSWITCH) entry activates the pacifier tone. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted.

MUTE OUTPUT

Output. Pin 12. This pin is the MUTE OUTPUT for both tone and pulse modes. Timing is dependent upon mode.

The MUTE OUTPUT consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, MUTE OUTPUT is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, MUTE OUTPUT is active continuously until dialing is completed. MUTE OUTPUT goes active when any key is pushed.

In the pulse mode, MUTE OUTPUT is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. MUTE OUTPUT timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. MUTE OUTPUT is active during each digit, and not active during the interdigit time. In both tone and pulse modes, MUTE OUTPUT goes active 40 ms before PULSE OUTPUT for a FLASH.

HKS

Input. Pin 17. Pin 17 is the hookswitch input to the MK53731. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

PULSE OUTPUT

Output. Pin 18. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 18.

DEVICE OPERATION (Tone Mode)

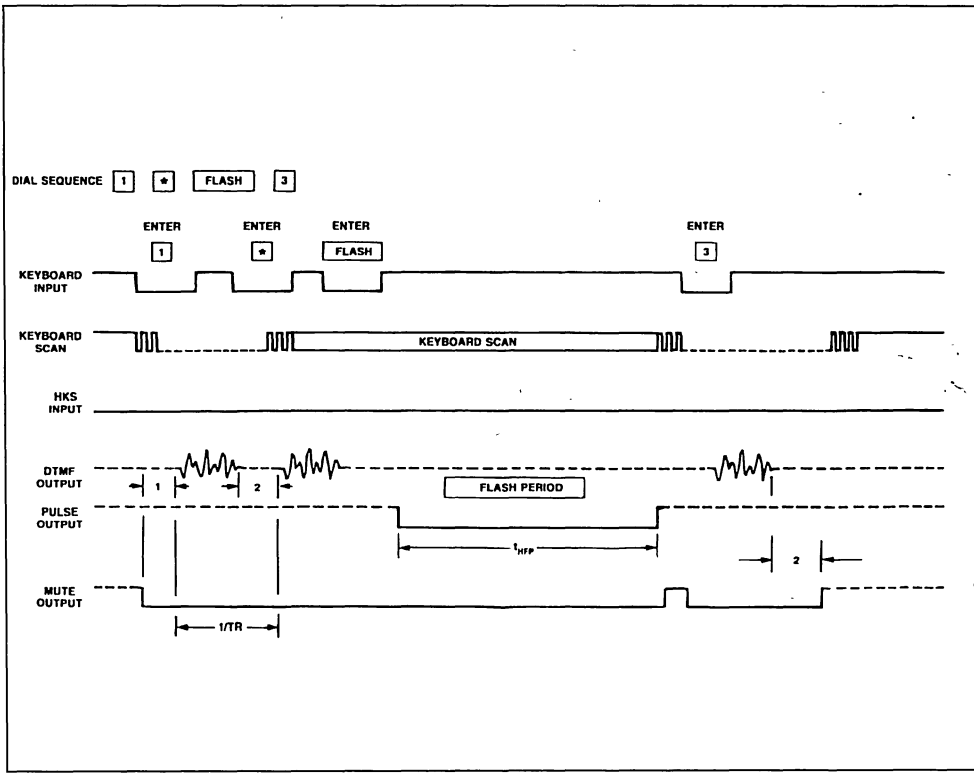
When the MK53731 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are internally pulled high. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53731 allows manual dialing of an indefinite number of digits, but if more than 28 digits are dialed, the 53731 will "wrap around". That is, the extra digits beyond 28 will be stored at the beginning of the LND buffer, and the first 28 digits will no longer be available for redial.

Table 2 : DTMF Output Frequency.

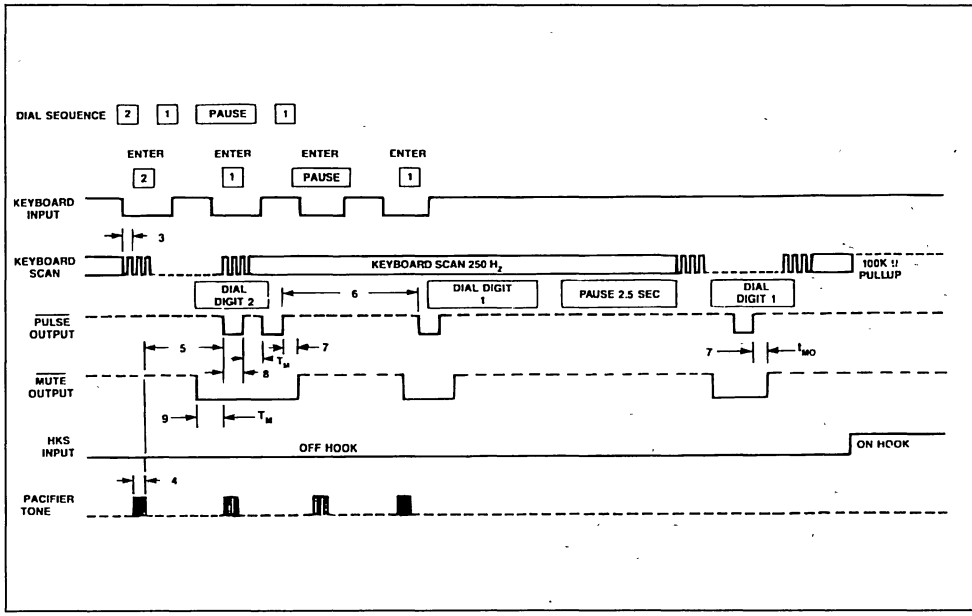
Key Input	Standard Frequency	Actual Frequency	% Deviation
ROW 1	697	699.1	+ 0.31
2	770	766.2	− 0.49
3	852	847.4	− 0.54
4	941	948.0	+ 0.74
COL 1	1209	1215.9	+ 0.57
2	1336	1331.7	− 0.32
3	1477	1471.9	− 0.35

Figure 7 : Tone Mode Timing.

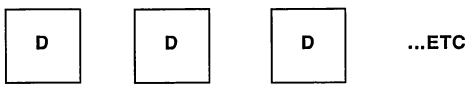


Note : For this example, key entries are ≤ 75 ms, but ≥ 32 ms.

Figure 8 : Pulse Mode Timing.



NORMAL DIALING (off-hook)

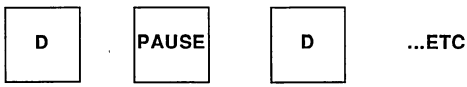


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

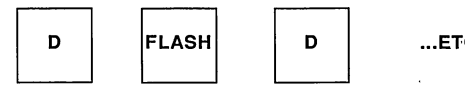
Last number dialing is accomplished by entering the LND key.

PAUSE



A pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 3.

HOOK FLASH



Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560 ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hook-flash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, MUTE OUTPUT will remain active during the flash delay period.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever

the * key, or SOFTSWITCH, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

Table 3 : Spécial Function Delays.

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse	Tone
SOFTSWITCH	FIRST AUTO	1.15 1.85	
PAUSE	FIRST AUTO	1.84 2.50	1.15 1.20

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	0 to + 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	(V+) + 3, (V–) – 3	

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS DC Characteristics

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	V+ TONE	DC Operating Voltage (tone mode)	2.5		6.0	V	
	V_{MR}	Memory Retention Voltage	1.5			V	1, 6
	I_s	Standby Current		0.4	1.0	µA	1
	I_{MR}	Memory Retention Current		0.15	0.75	µA	5, 6
	V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
	I_T	Operating Current (tone)		300	600	µA	2
	I_P	Operating Current (pulse)		150	250	µA	2
	I_{ML}	Mute Output (2.5 V) Sink Current (4.0 V)	1.0 3.0			mA mA	3
	I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
	I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
	K_{RU}	Keypad Pullup Resistance		100		kΩ	
	K_{RD}	Keypad Pulldown Resistance		500		Ω	
	V_{IL}	Keypad Input Level-low	0		0.3 V+	V	
	V_{IH}	Keypad Input Level-high	0.7 V+		V+	V	
	V_{PULSE}	Operating Voltage (pulse mode)	1.8		6.0	V	

Notes :
1. All inputs unloaded. Quiescent Mode (Oscillator off).
2. All outputs unloaded. Single key input.
3. V_{OUT} = 0.4 Volts.
4. Sink Current for V_{OUT} = −0.5 Volts. Source Current for V_{OUT} = 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

AC CHARACTERISTICS - TONE MODE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	T_{NK}	Tone Output No Key Down			80	dBm	1
	T_{OI}	Tone Output (independent)	13 173	12 194	11 218	dBm mV_{rms}	1, 2 3
	P_{Ei}	Pre-emphasis, High Band	1.6	2.0	2.4	dB	
	DC_i	Tone Output DC Bias (V+ – 2.5) (V+ 3.5)	 1.5	1.25		V V	
	R_E	Tone Output Load		10		kΩ	4
	T_{RIS}	Tone Output Rise Time		1.0		ms	5
	DIS	Output Distortion		5.0	8.0	%	3
	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-signal Delay	40			ms	6
2	T_{ISD}	Inter-signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

Notes : 1. O dBm equals 1 mW power into 600 Ω or 775 mVolts Important Note. The MK53731 is designed to drive a 10 kΩ load. The 600 Ω load is only for reference.
2. Single tone (low group) as measured at pin 10 T_A = 25 °C.
3. Supply voltage = 2.5 to 6 Volts R_E = 10 kΩ.
4. Supply voltage = 2.5 Volts.
5. Time from beginning of tone output waveform to 90 % of final magnitude of either frequency Crystal parameters suggested for proper operation are R_S < 100 Ω, L_m = 96 mH, C_m 0.02 pF, C_h = 5pF, f = 3.579545 MHz and C_L = 18 pF.
6. Time from initial key input until beginning of signaling.

AC CHARACTERISTICS - KEYDAP INPUTS, PACIFIER TONE
(numbers in left hand column refer to the limiting diagrams)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
3	T_{KD}	Keypad Debounce Time		32		ms	1
	F_{KS}	Keypad Scan Frequency		250		Hz	1
	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
	T_{HFP}	Hookflash Timing		560		ms	1

Note : 1. Crystal oscillator accuracy directly affects these times.

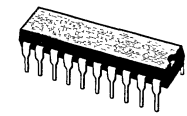
AC CHARACTERISTICS - PULSE MODE OPERATION

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	P_R	Pulse Rate		10		PPS	1
5	PDP	Pedigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

Notes : 1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship.

DIALER WITH FOUR EMERGENCY NUMBERS

- SINGLE CHIP DTMF AND PULSE DIALER
- STORES 5 18-DIGIT TELEPHONE NUMBERS, INCLUDING LAST NUMBER DIALED
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- SINGLE BUTTON REDIAL OF ALL 5 MEMORIES
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- 8 TONES PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION GUARANTEED (74/54ms)
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF A VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS



DIP20

ORDER CODE : MK53760 N00

Figure 1 : Pin Connection.

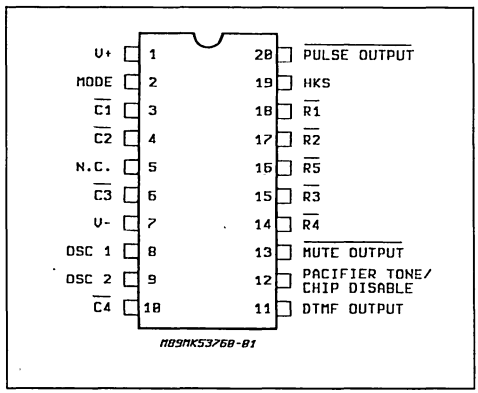
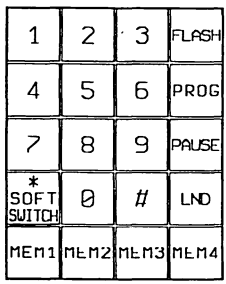


Figure 2 : Keypad Configuration.



DESCRIPTION

The MK53760 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53760 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to 4 repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch, Flash, and 4 memories. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed, and the MEM keys provide single key access to all memory locations for auto-dialing.

The FLASH key simulates a 560ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

The PAUSE key allows the user to insert a delay in dialing for functions such as the pause in accessing an outside line when reading from a PABX.

The PROG key provides an easy way to program a number into any memory location (MEM1 - MEM4) whether on-hook or off-hook.

FUNCTIONAL PIN DESCRIPTION

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements (see Electrical Specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V-), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V- connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the *key, or softswitch, is depressed. Subsequent *key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R5}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard inputs. The MK53760 interfaces with either the standard 2-of-9 with negative common or the single-contact (Form A) keyboard.

A valid keypad and entry is either a single Row connected to a single Column or V- simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternatively switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 19 to pin 1), the keyboard inputs all pull high through on-chip pullup resistors.

In the tone mode, if 2 or more keys in the same row or column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes.

Single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table below :

Table 1 : Output Tone Duration.

Key-Push Time, T*	Tone Output*
$T \leq 32ms$	No Output Ignored by MK53760.
$32ms \leq T \leq .75ms + T_{KD}$	75ms Duration Output.
$T \geq 75ms + T_{KD}$	Output Duration = $T - T_{KD}$

***Note :** T_{KD} is the key pad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75ms duration, and the tone separation (intersignal delay) is 50ns.

V-

Input. Pin 7 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Pin 8 (input), pin 9 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has have sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ± 0.25% may also be used.

DTMF OUTPUT

Output. Pin 11. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency and a single Column frequency. A typical single tone sine wave is shown in figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53760 is designed to operate from an unregulated supply : the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{oi} = -12dBm \pm 1dB$$

The DC component of the DTMF output while active is described by the following equation :

$$VDC_1 = 0.3V + + 0.5 \text{ Volts}$$

Figure 3 : MK53760 Functional Block Diagram.

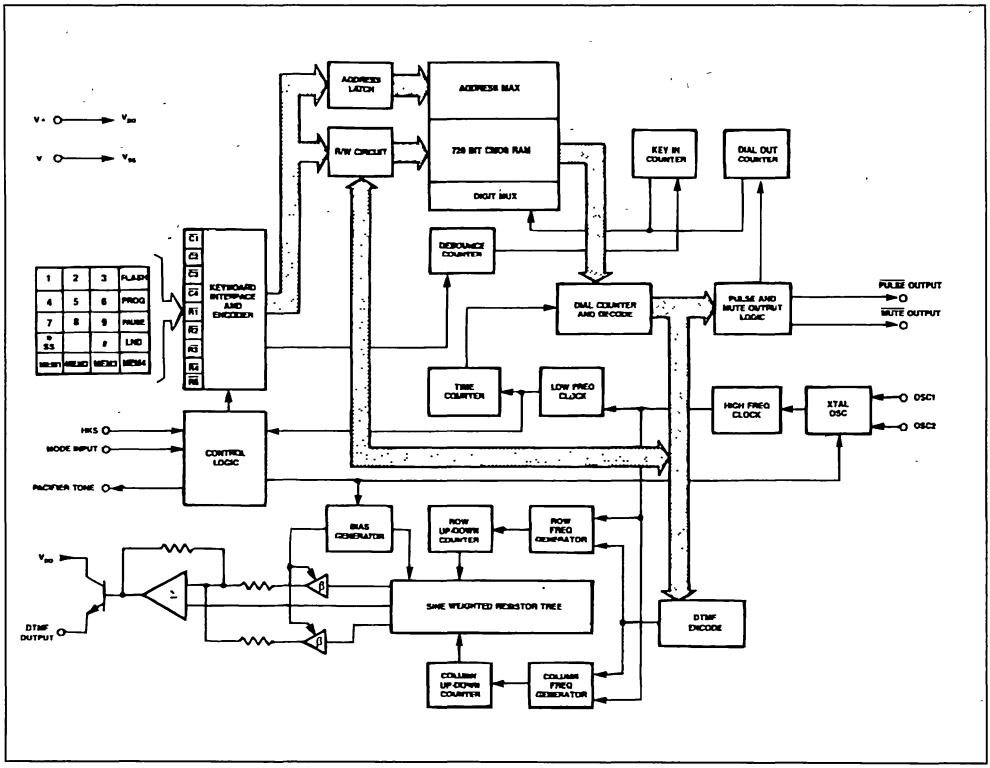


Figure 4 : Typical Single Tone.

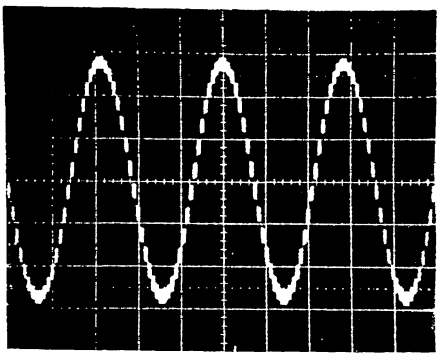
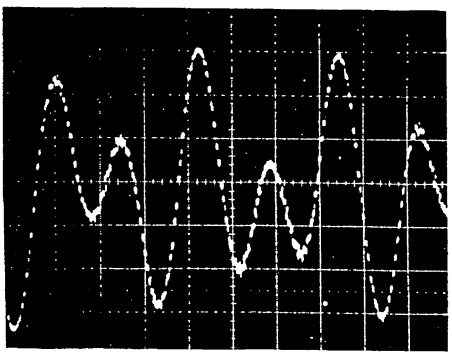


Figure 5 : Typical Dual Tone.



PACIFIER TONE OUTPUT/CHIP DISABLE INPUT

Pin 12. PAC tone is an output. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted. A 500Hz square wave is activated upon acceptance of a valid key input, after the 32ms debounce time. The square wave terminates after a maximum of 30ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, any non-DTMF key (LND, FLASH, MEM, PROG) entry activates the pacifier tone. When programming the chip, all valid key entries activate the pacifier tone in either pullse or tone mode.

The CHIP DISABLE is an input. When pin 12 is switched low, through a resistor (10K to 100K), the MK53760 is enabled. When pin 12 is switched to V+ through the resistor, all keypad inputs are pulled high, and the MK53760 will ignore all keypad inputs. When the chip is disabled, it will not dial, and it cannot be programmed. The chip will only be disabled when the circuit is inactive (not dialing) and Pin 12 is switched high.

Figure 6 : Typical Spectral Response.

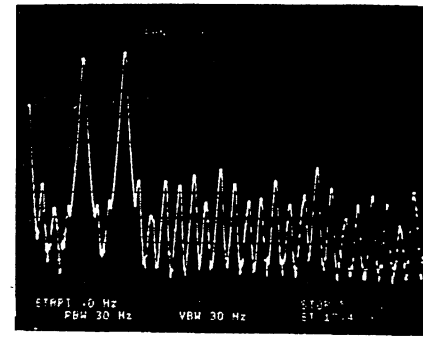
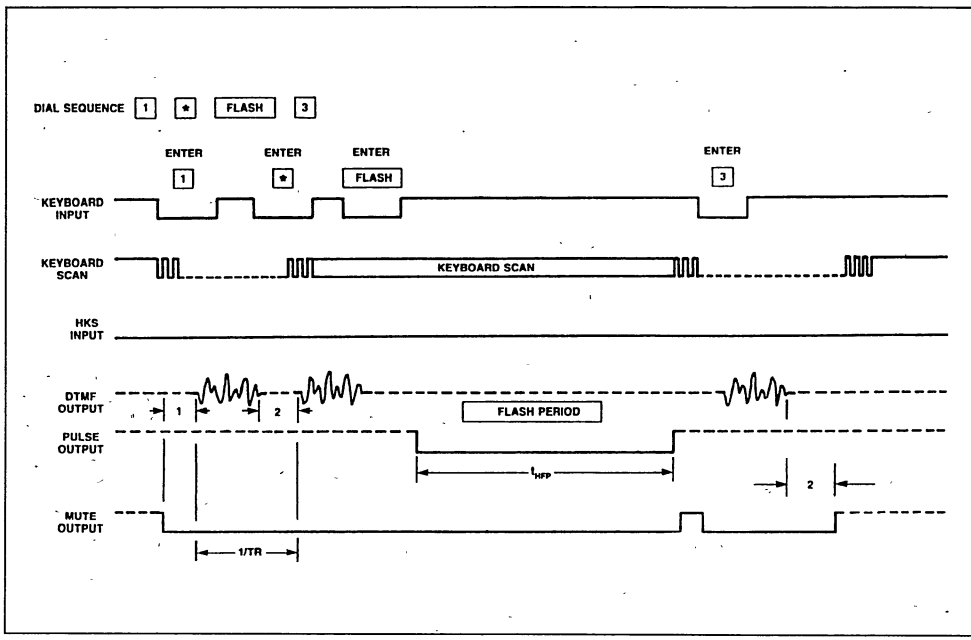


Figure 7 : Tone Mode Timing.



Notes : 1. For this example, key entries are ≤ 75 ms, but ≥ 32 ms.
2. MUTE goes active after any key is depressed.

Figure 8 : Pulse Mode Timing.

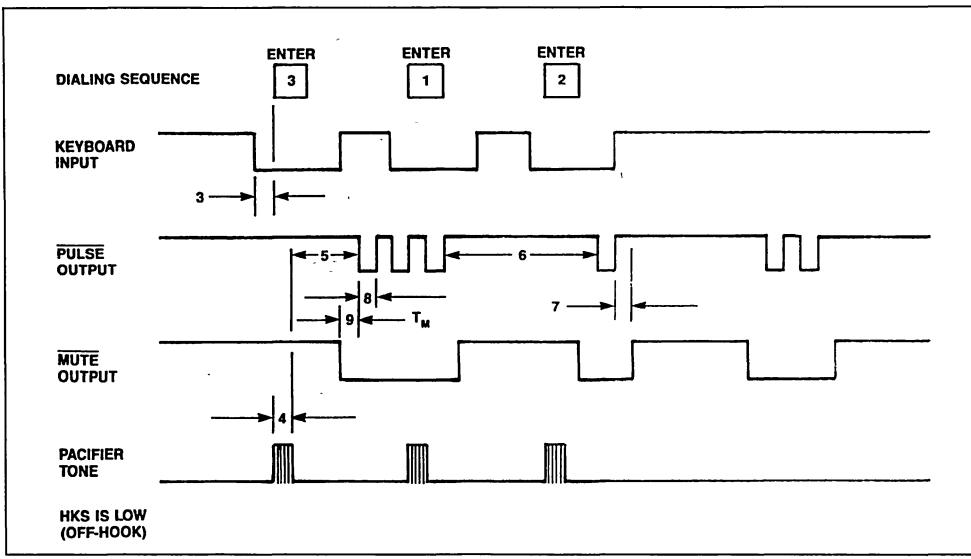


Table 2 : DTMF Output Frequency.

Key Input		Standard Frequency	Actual Frequency	% Deviation
ROW	1	697	699.1	+ 0.31
	2	770	766.2	− 0.49
	3	852	847.4	− 0.54
	4	941	948.0	+ 0.74
COL	1	1209	1215.9	+ 0.57
	2	1336	1331.7	− 0.32
	3	1477	1471.9	− 0.35

MUTE OUTPUT

Output. Pin 13. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in figure 8 for pulse mode signaling and figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH.

HKS

Input Pin 19. Pin 19 is the hookswitch input to the MK53760. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

PULSE OUTPUT

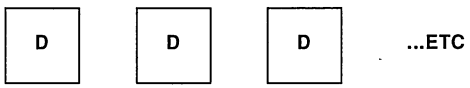
Output. Pin 20. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560ms output pulse at pin 20.

DEVICE OPERATION

When the MK53760 is not actively dialing, it consumes very little current. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40ms (measured from initial key closure). Output tone duration is shown in table 1.

The MK53760 allows manual dialing of an indefinite number or digits, but if more than 18 digits are dialed per number, the MK53760 "wrap around". That is, the extra digits beyond 18 will be stored at the beginning of the LND buffer, and the first 18 digits will no longer be available for redial. During autodial from LND or any MEM location, key inputs are not accepted, but they will suspend dialing until released.

NORMAL DIALING (off-hook)



Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

HOOK FLASH

Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, MUTE OUTPUT will remain active during the flash delay period.

PAUSE

A Pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in table 3.

PROGRAMMING AND REPERTORY DIALING

PROGRAMMING AND REPERTORY DIALING

Programming is independent of HKS (pin 19) and MODE (pin 2).

To program, enter the following :

PROG, Digit 1, Digit 2, ..., MEM (Location 1-4). When programming, dialing is inhibited.

To dial a number from repertory memory (HKS must be low) enter the single key :

MEM (location 1 - 4)
To save the last number dialed : PROG, MEM (location 1 - 4)

Table 3 : Special Function Delays.

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse	Tone
SOFTSWITCH	FIRST AUTO	0.40 1.10	
PAUSE	FIRST AUTO	1.84 2.50	1.15 1.20

ABSOLUTE MAXIMUM RATINGS *

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	0 to + 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25°C)	500	mW
Maximum Voltage on any Pin	(V +) + 3, (V –) – 3	

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
V + TONE	DC Operating Voltage (tone mode)	2.5		6.0	V	
V_{MR}	Memory Retention Voltage	1.5			V	1, 6
I_S	Standby Current		0.4	1.0	µA	1
I_{MR}	Memory Retention Current		0.15	0.75	µA	5, 6
V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
I_T	Operating Current (tone)		300	600	µA	2
I_P	Operating Current (pulse)		150	250	µA	2
	Operating Current On-Hook Program Mode Key Operated No-Key Operated			 200 1	 µA µA	

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS (continued)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
I_{ML}	Mute Output (2.5V) Sink Current (4.0V)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
K_{RU}	Keypad Pullup Resistance		100		KΩ	
K_{RD}	Keypad Pulldown Resistance		500		Ω	
V_{IL}	Keypad Input Level-Low	0		0.3 V+	V	
V_{IH}	Keypad Input Level-High	0.7 V+		V+	V	
V_{PULSE}	Operating Voltage (pulse mode)	1.8		6.0	V	

Notes : 1. All inputs unloaded. Quiescent Mode (oscillator off).
2. All outputs unloaded, single key input.
3. V_{OUT} = 0.4 Volts.
4. Sink Current for V_{OUT} = 0.5 volts, Source Current for V_{OUT} = 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

AC CHARACTERISTICS - TONE MODE

N°	Symbol	Parameter	Value			Unit	Note
			Min.	Typ.	Max.		
	T_{NK}	Tone Output No Key Down			– 80	dBm	1
	T_{Oi}	Tone Output (independent)	– 13 173	– 12 194	– 11 218	dBm mV_{rms}	1, 2 3
	PEi	Pre-Emphasis, High Band	1.6	2.0	2.4	dB	
	D_{Ci}	Tone Output DC Bias (V + = 2.5) (V + = 3.5)	 1.5	1.25		V V	
	R_E	Tone Output Load		10		kΩ	4
	T_{RIS}	Tone Output Rise Time		1.0		ms	5
	DIS	Output Distortion		5.0	8.0	%	3
	TR	Tone Signaling Ratte		8.0		1/sec	
1	T_{PSD}	Pre-Signal Delay	40			ms	6
2	T_{ISD}	Inter-Signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

Notes : 1. O dBm equals 1mW power into 600 ohms or 775mV. Important Note : The MK53760 is designed to drive a 10 kΩ load. The 600Ω load is only for reference.
2. Single tone (low group) as measured at pin 10, T_A = 25°C.
3. Supply voltage = 2.5 to 6V, R_E = 10 kΩ.
4. Supply voltage = 2.5V. These specifications are supply-dependent
5. Time from beginning of tone output waveform to 90 % of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_S < 100 ohms, L_m = 96mH, C_m = 0.02pF, C_h = 5pF, f = 3.579545MHz, and C_L = 18pF
6. Time from initial key input until beginning of signaling.

ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE
(numbers in left hand column refer to the timing diagrams.)

N°	Symbol	Parameter	Value			Unit	Note
			Min.	Typ.	Max.		
3	T_{KD}	Keypad Debounce Time		32		ms	1
	F_{KS}	Keypad Scan Frequency		250		Hz	1
	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
	T_{HFP}	Hookflash Timing		560		ms	1

Notes : 1. Crystal oscillator accuracy directly affects these times.

AC CHARACTERISTICS – PULSE MODE OPERATION

N°	Symbol	Parameter	Value			Unit	Note
			Min.	Typ.	Max.		
	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

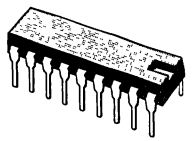
Notes : 1. 10 PPS is the nominal rate
2. Figure 8 illustrates this relationship.

SGS-THOMSON MICROELECTRONICS

MK53761

REPERTORY DIALER

- SINGLE CHIP DTMF AND PULSE DIALER
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- NINE NUMBER REPERTORY PLUS RECALL OF LAST NUMBER DIALED (18 digits each)
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- 8 TONE PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION GUARANTEED (74/54 ms)
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS



DIP18

ORDER CODE : MK53761N01

Figure 1 : Pin Connection.

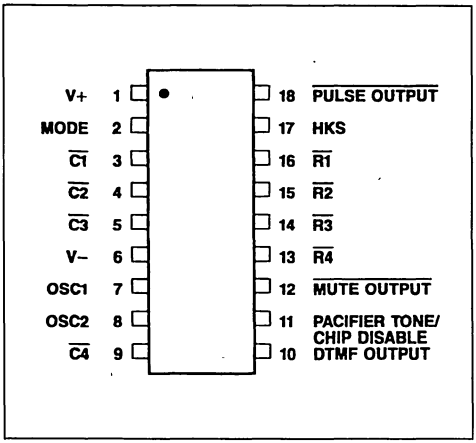


Figure 2 : Keypad Configuration.

1	2	3	FLASH
4	5	6	PROG
7	8	9	MEM
* SOFT SWITCH	0	#	LND

M88MK53761-01A

DESCRIPTION

The MK53761 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53761 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch, and Flash. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed. The PROG key provides an easy way to program a number into any memory location (1-9) whether on-hook on off-hook. The MEM key allows easy redialing of the number stored in memory locations (1-9).

The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

FUNCTIONAL PIN DESCRIPTION

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see electrical specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V– connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard inputs. The MK53761 interfaces with either the standard 2-of-8 with negative common or the singlecontact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs all pull high through on-chip pullup resistors.

In the tone mode, if 2 or more keys in the same row or if 2 or more keys in the same column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes, and single tones will not be redialed.

Also in the tone mode, the output tone is continuous is manual dialing as long as the key is pushed. The output tone duration follows the table 1.

Table 1 : Output Tone Duration.

Key-Push Time, T*	Tone Output*
$T \leq 32$ ms	No Output Ignored by MK53761
32 ms $\leq T \leq$ 75 ms + T_{KD}	75 ms Duration Output
$T \geq 75$ ms + T_{KD}	Output Duration = $T - T_{KD}$

* TKD is the key pad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75 ms duration, and the tone separation (intersignal delay) is 50 ms.

V–

Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Pin 7 (input), pin 8 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ± 0.25 % may also be used.

DTMF OUTPUT

Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53761 is designed to operate from an unregulated supply ; the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{oi} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation :

$$VDC_1 = 0.3 \text{ V+} + 0.5 \text{ Volts}$$

Figure 3 : MK53761 Functional Block Diagram.

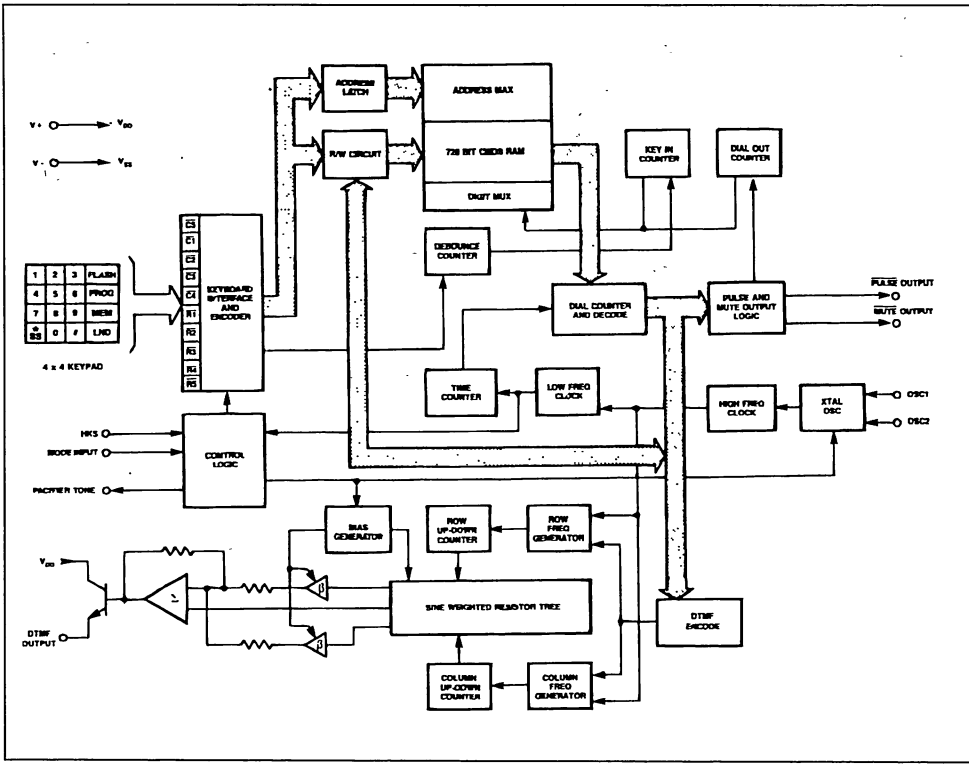


Figure 4 : Typical Single Tone.

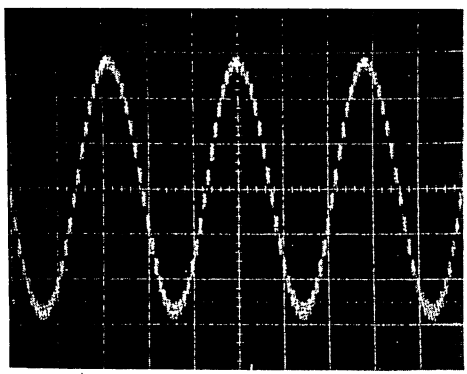


Figure 5 : Typical Dual Tone.

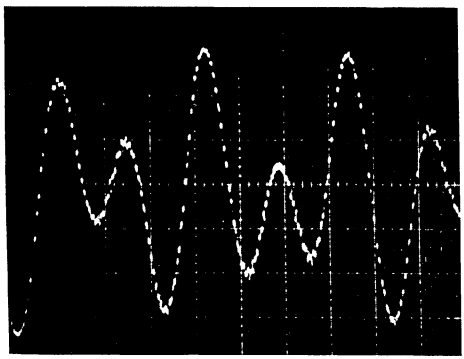
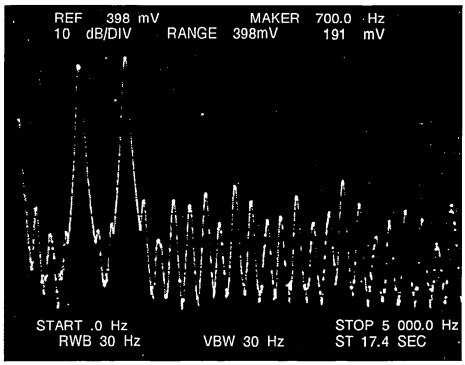


Figure 6 : Typical Spectral Response.



PACIFIER TONE OUTPUT/CHIP DISABLE INPUT

Output. Pin 11. The pacifier tone provides audible feed-back, confirming that the key has been properly entered and accepted. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, any non-DTMF key (LND, FLASH, MEM, PROG) entry activates the pacifier tone. When programming the chip, all valid key entries activate the pacifier tone in either pulse or tone mode.

The CHIP DISABLE is an input. When pin 11 is switched low through a resistor (10 K to 100 K), the MK53761 is enabled. When pin 11 is switched to V+ through the resistor, all keypad inputs are pulled high, and the MK53761 will ignore all keypad inputs. When the chip is disabled, it will not dial, and it cannot be programmed. The chip can only be disabled when the circuit is inactive (not dialing) and Pin 12 is switched high.

Table 2 : DTMF Output Frequency.

Key Input		Standard Frequency	Actual Frequency	% Deviation
ROW	1	697	699.1	+ 0.31
	2	770	766.2	– 0.49
	3	852	847.4	– 0.54
	4	941	948.0	+ 0.74
COL	1	1209	1215.9	+ 0.57
	2	1336	1331.7	– 0.32
	3	1477	1471.9	– 0.35

MUTE OUTPUT

Output. Pin 12. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH. Figure 8 illustrates the timing for this pin.

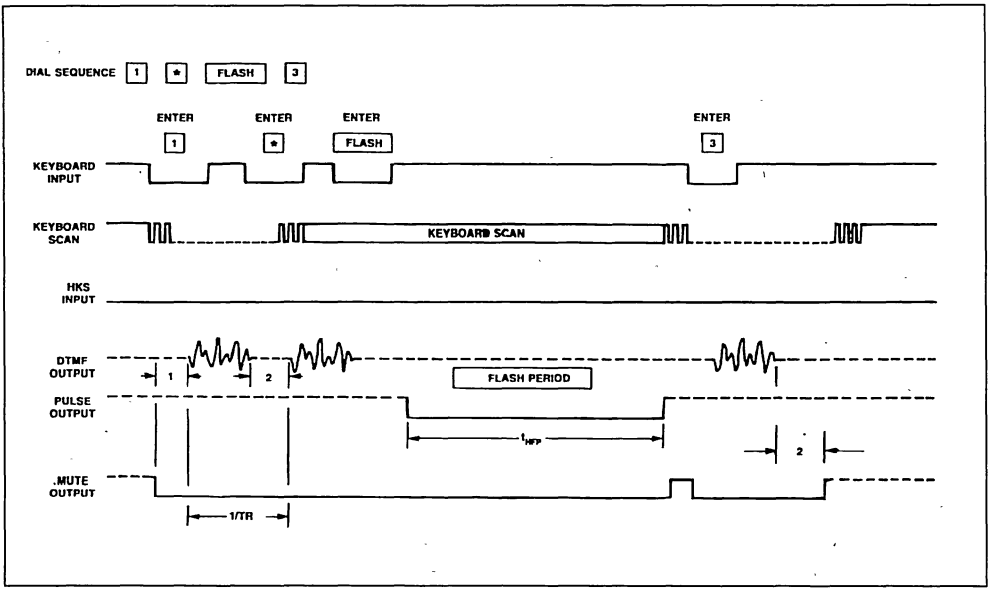
HKS

Input. Pin 17. Pin 17 is the hookswitch input to the MK53761. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2.

$\overline{\text{PULSE OUTPUT}}$

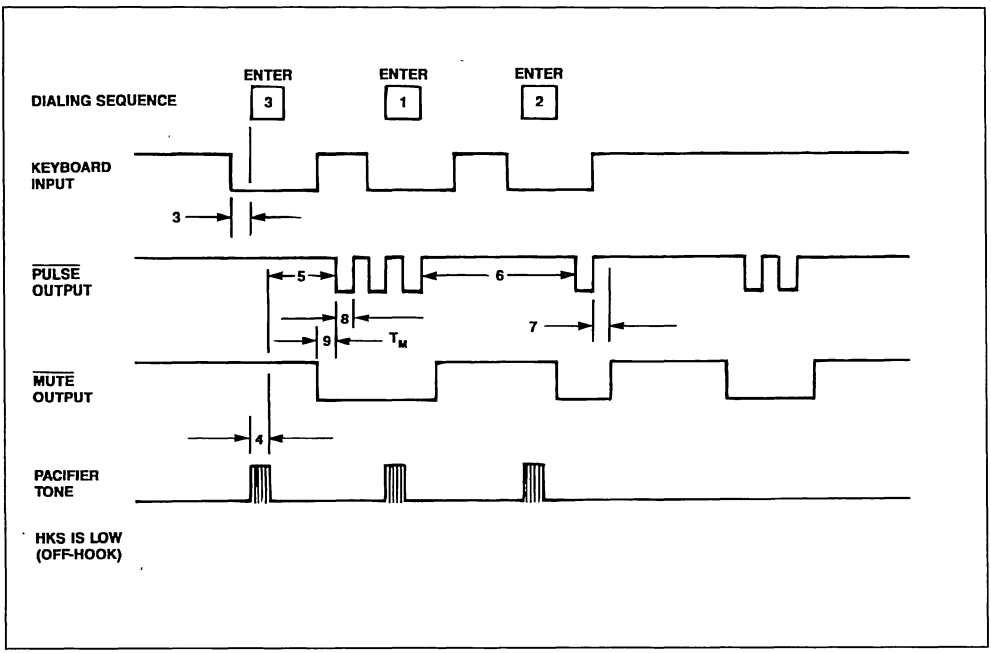
Output. Pin 18. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 18.

Figure 7 : Tone Mode Timing.



Notes : 1. For this example, key entries are ≤ 75 ms, but ≥ 32 ms.
2. MUTE goes active after any key is depressed.

Figure 8 : Pulse Mode Timing..

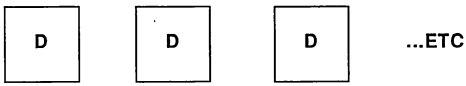


DEVICE OPERATION

When the MK53761 is not actively dialing, it consumes very little current. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53761 allows manual dialing of an indefinite number of digits, but if more than 18 digits are dialed per number, the 53761 will "wrap around". That is, the extra digits beyond 18 will be stored at the beginning of the LND buffer, and the first 18 digits will no longer be available for redial. During autodial from LND or any memory location, key inputs are not accepted, but they will suspend dialing until released.

NORMAL DIALING (off-hook)

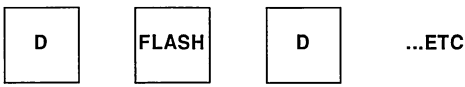


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

HOOK FLASH



Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560 ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, $\overline{\text{MUTE OUTPUT}}$ will remain active during the flash delay period.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

PROGRAMMING AND REPERTORY DIALING

Programming is independent of HKS (pin 17) and MODE (pin 2).

To program, enter the following :

PROG, Digit 1, Digit 2, ..., MEM, Location (1-9).

When programming, dialing in inhibited.

To dail a number from repertory memory (HKS must be low) enter the following :

MEM, Location (1-9).

To save the last number dialed : PROG, MEM, Location (1-9).

Table 3 : Special Function Delays.

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.
The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or previous dialing is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse	Tone
SOFTSWITCH	FIRST AUTO	0.40 1.10	

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	0 to + 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	(V^+) + .3 ; (V^-) – .3	V

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V+ TONE	DC Operating Voltage (tone mode)	2.5		6.0	V	
V_{MR}	Memory Retention Voltage	1.5			V	1. 6
I_S	Standby Current		0.4	1.0	µA	1
I_{MR}	Memory Retention Current		0.15	0.75	µA	5. 6
V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
I_T	Operating Current (tone)		300	600	µA	2
I_P	Operating Current (pulse)		150	250	µA	2
	Operating Current On-hook Program Mode Key Operated No-key Operated			 200 1	 µA µA	
I_{ML}	Mute Output (2.5 Volts) Sink Current (4.0 Volts)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	Keypad Pulldown Resistance		500		Ω	
V_{IL}	Keypad Input Level-low	0		0.3 V +	V	
V_{IH}	Keypad Input Level-high	0.7 V +		V +	V	
V_{PULSE}	Operating Voltage (pulse mode)	1.8		6.0	V	

Notes : 1. All inputs unloaded. Quiescent mode (oscillator off).
2. All outputs unloaded, single key input.
3. V_{OUT} = 0.4 Volts.
4. Sink current for V_{OUT} = 0.5 Volts, Source Current for V_{OUT} = 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS – TONE MODE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	T_{NK}	Tone Output no Key Down			– 80	dBm	1
	T_{Oi}	Tone Output (independent)	– 13 173	– 12 194	– 11 218	dBm mV_{rms}	1, 2 3
	PE_i	Pre-emphasis, High Band	1.6	2.0	2.4	dB	
	DC_i	Tone Output DC Bias (V + = 2.5) (V + = 3.5)	 1.5	1.25		V V	
	R_E	Tone Output Load		10		kΩ	4
	T_{RIS}	Tone Output Rise Time		1.0		ms	5
	DIS	Output Distortion		5.0	8.0	%	3
	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-signal Delay	40			ms	6
2	T_{ISD}	Inter-signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

Notes : 1. O dBm equals 1 mW power into 600 Ω or 775 mVolts.Important note : the MK53761 is designed to drive a 10 kΩ load. The 600 Ω load is only for reference.
2. Single tone (low group), as measured at pin 10, $T_A = 25°C$.
3. Supply voltage = 2.5 to 6 volts, $R_E = 10$ kΩ.
4. Supply voltage = 2.5 volts.
5. Time from beginning of tone output waveform to 90 % of final magnitude of either frequency. Crystal parameters suggested for proper operation are $R_s < 100$ Ω, $L_m = 96$ mH, $C_m = 0.02$ pF, $C_h = 5$ pF, f = 3.579545 MHz, and $C_L = 18$ pF.
6. Time from initial key input until beginnig of signaling.

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE
(numbers in left hand column refer to the timing diagrams.)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
3	T_{KD}	Keypad Debounce Time		32		ms	1
	F_{KS}	Keypad Scan Frequency		250		Hz	1
	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
	T_{HFP}	Hookflash Timing		560		ms	1

Note : 1. Crystal oscillator accuracy directly affects these times

AC CHARACTERISTICS – PULSE MODE OPERATION

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

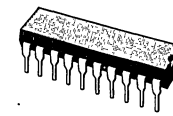
Notes : 1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship.

SGS-THOMSON MICROELECTRONICS

MK53762

REPERTORY DIALER

- SINGLE CHIP DTMF AND PULSE DIALER
- STORES 10 18-DIGIT TELEPHONE NUMBERS, INCLUDING LAST NUMBER DIALED
- SOFTSWITCH CHANGES SIGNALING MODE FROM PULSE TO TONE
- SINGLE BUTTON REDIAL OF ALL TEN MEMORIES
- FLASH KEY INPUT INITIATES TIMED HOOK FLASH
- 8 TONES PER SECOND DIALING IN TONE MODE AND 10 PPS IN PULSE MODE
- DTMF ACTIVE UNTIL KEY RELEASE
- MINIMUM DTMF DURATION/SEPARATION GUARANTEED (74/54 ms)
- PACIFIER TONE PROVIDES AUDIBLE INDICATION OF A VALID KEY INPUT FOR NON-DTMF KEY ENTRIES
- POWERED FROM TELEPHONE LINE, LOW OPERATING VOLTAGE FOR LONG LOOP APPLICATIONS



DIP20

ORDER CODE : MK53762N01

Figure 1 : Pin Connection.

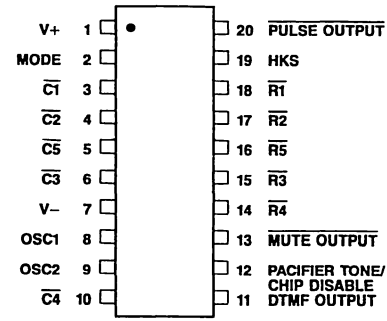


Figure 2 : Keypad Configuration.

1	2	3	FLASH	MEM9
4	5	6	PROG	MEM8
7	8	9	PAUSE	MEM7
* SOFT SWITCH	0	#	LND	MEM6
MEM1	MEM2	MEM3	MEM4	MEM5

M88MK53762-01

DESCRIPTION

The MK53762 is a Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53762 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch, Flash, and 9 memories. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed, and the MEM keys provide single key access to all memory locations for auto-dialing.

The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

The PAUSE key allows the user to insert a delay in dialing for functions such as the pause in accessing an outside line when redialing from a PABX.

The PROG key provides an easy way to program a number into any memory location (MEM 1 - MEM 9) whether on-hook or off-hook.

FUNCTIONAL PIN DESCRIPTION

V+

Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (see Electrical Specifications).

MODE

Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V–), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V– connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{C5}$, $\overline{R5}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$

Keyboard inputs. The MK53762 interfaces with either the standard 2-of-10 with negative common or the single-contact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V– simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 19 to pin 1), the keyboard inputs all pull high through on-chip pullup resistors.

In the tone mode, if 2 or more keys in the same row or column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes.

Single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table below :

Table 1 : Output Tone Duration.

Key-Push Time, T*	Tone Output*
$T \leq 32$ ms	No output. Ignored by MK53762.
$32\text{ ms} \leq T \leq 75\text{ ms} + T_{KD}$	75 ms Duration Output.
$T \geq 75\text{ ms} + T_{KD}$	Output Duration = $T - T_{KD}$

***Note :** T_{KD} is the key pad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75 ms duration, and the tone separation (intersignal delay) is 50 ms.

V –

Input. Pin 7 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2

Pin 8 (input), pin 9 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has have sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ± 0.25 % may also be used.

DTMF OUTPUT

Output. Pin 11. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53762 is designed to operate from an unregulated supply ; the TONE LEVEL is supply independent, and the single row tone output level will be typically :

$$T_{oi} = -12\text{ dBm} \pm 1\text{ dB}$$

The DC component of the DTMF output while active is described by the following equation :

$$VDC_1 = 0.3\ V+ + 0.5\text{ Volts}$$

Figure 3 : MK53762 Functional Block Diagram.

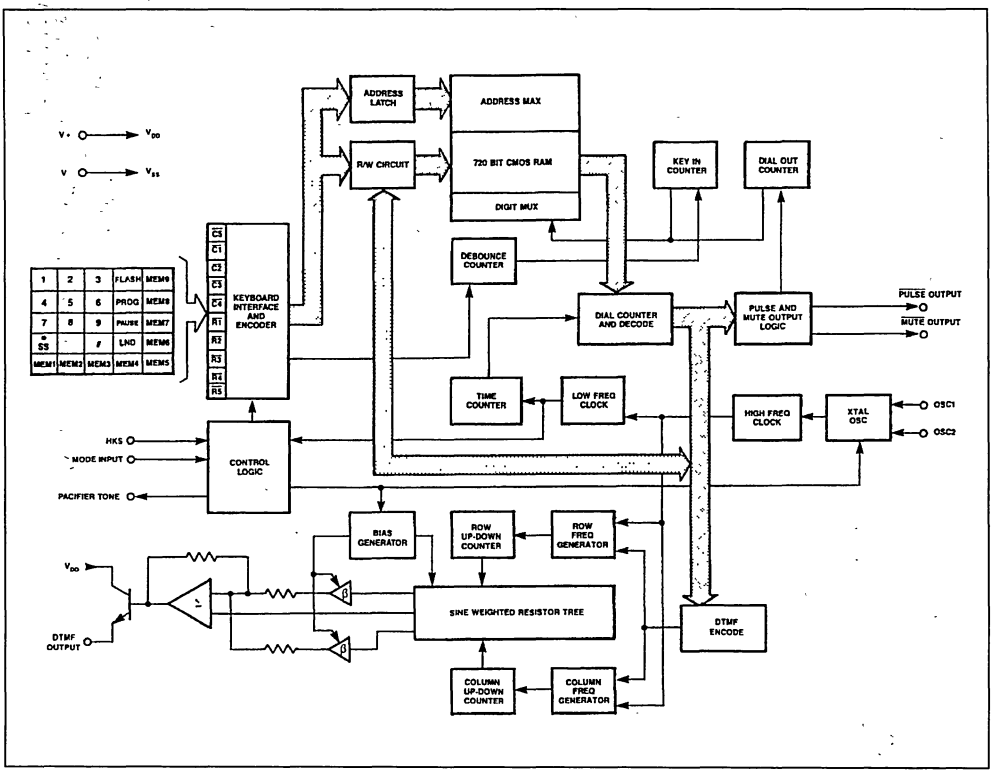


Figure 4 : Typical Single Tone.

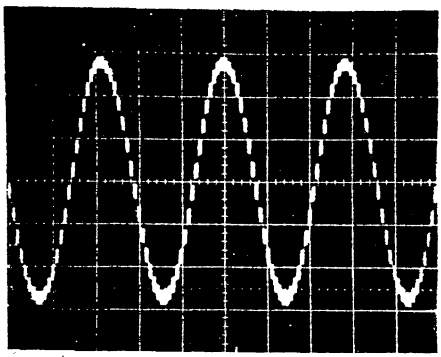
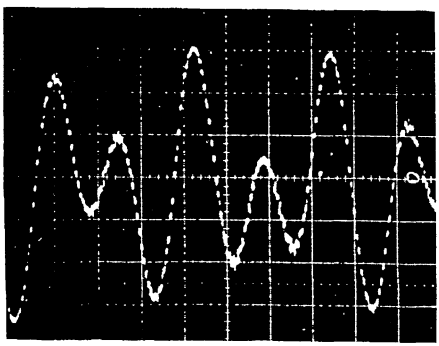


Figure 5 : Typical Dual Tone.



PACIFIER TONE OUTPUT/CHIP DISABLE INPUT

Pin 12. PAC tone is an output. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, any non-DTMF key (LND, FLASH, MEM, PROG) entry activates the pacifier tone. When programming the chip, all valid key entries activate the pacifier tone in either pullse or tone mode.

The CHIP DISABLE is an input. When pin 12 is switched low through a resistor (10 K to 100 K), the MK53762 is enabled. When pin 12 is switched to V+ through the resistor, all keypad inputs are pulled high, and the MK53762 will ignore all keypad inputs. When the chip is disabled, it will not dial, and it cannot be programmed. The chip will only be disabled when the circuit is inactive (not dialing) and Pin 12 is switched high.

Figure 6 : Typical Spectral Response.

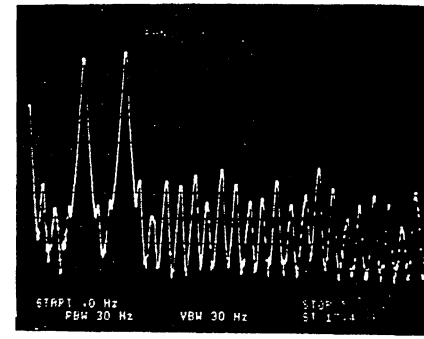
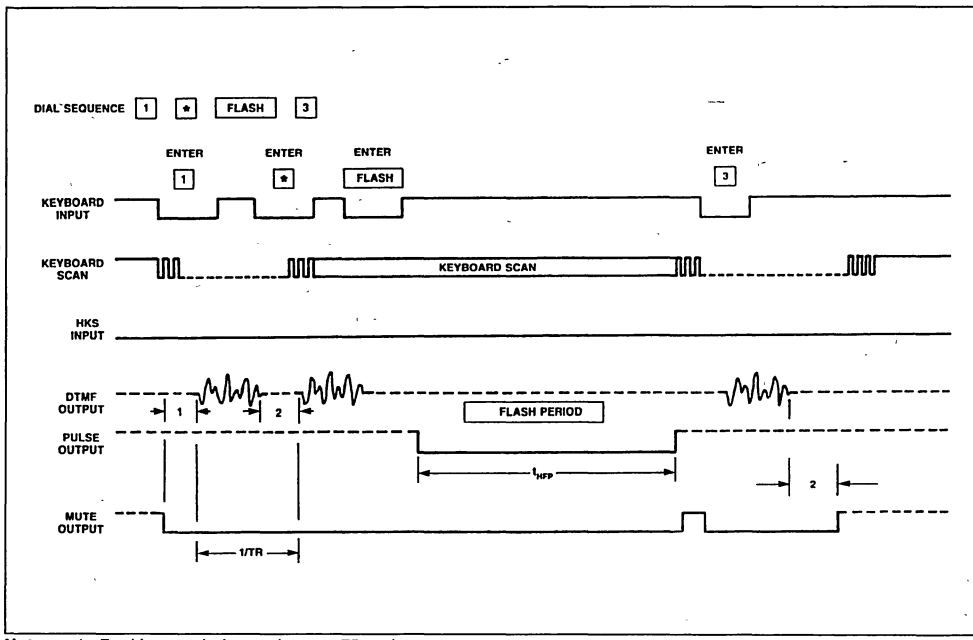


Figure 7 : Tone Mode Timing.



Notes : 1. For this example, key entries are ≤ 75 ms, but ≥ 32 ms.
2. MUTE goes active after any key is depressed.

Figure 8 : Pulse Mode Timing.

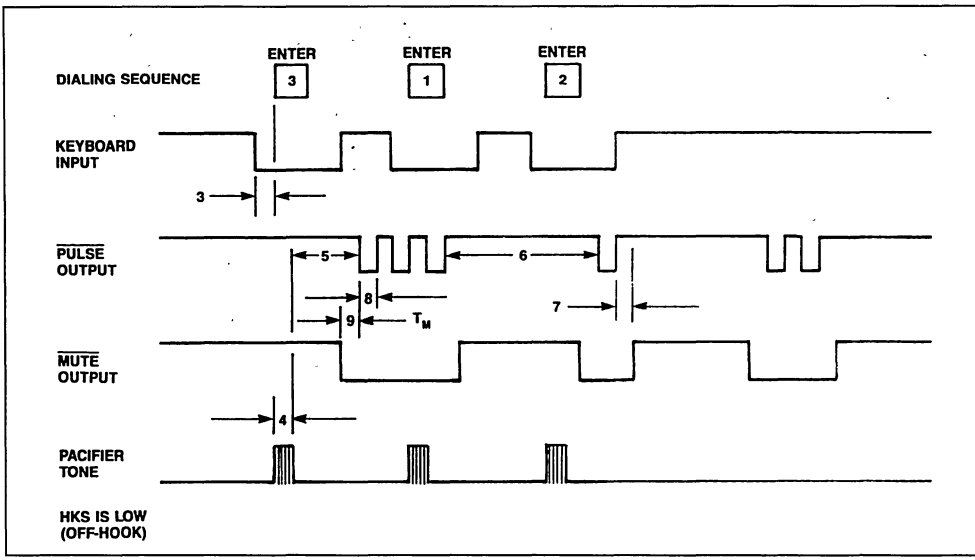


Table 2 : DTMF Output Frequency.

Key Input		Standard Frequency	Actual Frequency	% Deviation
ROW	1	697	699.1	+ 0.31
	2	770	766.2	– 0.49
	3	852	847.4	– 0.54
	4	941	948.0	+ 0.74
COL	1	1209	1215.9	+ 0.57
	2	1336	1331.7	– 0.32
	3	1477	1471.9	– 0.35

MUTE OUTPUT

Output. Pin 13. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH.

HKS

Input. Pin 19. Pin 19 is the hookswitch input to the MK53762. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

PULSE OUTPUT

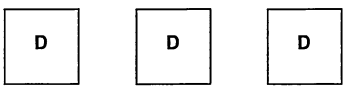
Output. Pin 20. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 20.

DEVICE OPERATION

When the MK53762 is not actively dialing, it consumes very little current. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53762 allows manual dialing of an indefinite number of digits, but if more than 18 digits are dialed per number, the 53762 will "wrap around". That is, the extra digits beyond 18 will be stored at the beginning of the LND buffer, and the first 18 digits will no longer be available for redial. During autodial from LND or any MEM location, key inputs are not accepted, but they will suspend dialing until released.

NORMAL DIALING (off-hook)



Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

HOOK FLASH

Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560 ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, MUTE OUTPUT will remain active during the flash delay period.

PAUSE

A Pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 3.

PROGRAMMING AND REPERTORY DIALING

PROGRAMMING AND REPERTORY DIALING

Programming is independent of HKS (pin 19) and MODE (pin 2).

To program, enter the following :

PROG, Digit 1, Digit 2, ..., MEM (Location 1-9). When programming, dialing is inhibited.

To dial a number from repertory memory (HKS must be low) enter the single key :

MEM (Location 1-9)

To save the last number dialed : PROG, MEM (Location 1-9).

Table 3 : Special Function Delays.

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

Function	First/Auto	Delay (seconds)	
		Pulse	Tone
SOFTSWITCH	FIRST AUTO	0.40 1.10	– –
PAUSE	FIRST AUTO	1.84 2.50	1.15 1.20

ABSOLUTE MAXIMUM RATINGS *

Parameter	Value	Unit
DC Supply Voltage	6.5	V
Operating Temperature	0 to + 60	°C
Storage Temperature	– 55 to + 125	°C
Maximum Power Dissipation (25 °C)	500	mW
Maximum Voltage on any Pin	(V +) + 3, (V –) – 3	

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V + TONE	DC Operating Voltage (tone mode)	2.5		6.0	V	
V_{MR}	Memory Retention Voltage	1.5			V	1, 6
I_S	Standby Current		0.4	1.0	µA	1
I_{MR}	Memory Retention Current		0.15	0.75	µA	5, 6
V_{MUTE}	Mute Output Operating Voltage	1.8			V	7
I_T	Operating Current (tone)		300	600	µA	2
I_P	Operating Current (pulse)		150	250	µA	2
	Operating Current On-Hook Program Mode Key Operated No-Key Operated			 200 1	 µA µA	
I_{ML}	Mute Output (2.5 V) Sink Current (4.0 V)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		µA	4
K_{RU}	Keypad Pullup Resistance		100		KΩ	
K_{RD}	Keypad Pulldown Resistance		500		Ω	
V_{IL}	Keypad Input Level-Low	0		0.3 V+	V	
V_{IH}	Keypad Input Level-High	0.7 V+		V+	V	
V_{PULSE}	Operating Voltage (pulse mode)	1.8		6.0	V	

Notes : 1. All inputs unloaded. Quiescent Mode (oscillator off).
2. All outputs unloaded, single key input.
3. V_{OUT} = 0.4 Volts.
4. Sink Current for V_{OUT} = 0.5 volts, Source Current for V_{OUT} = 2.0 Volts.
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS – TONE MODE

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
–	T_{NK}	Tone Output No Key Down			– 80	dBm	1
–	T_{OI}	Tone Output (independent)	– 13 173	– 12 194	– 11 218	dBm mV_{rms}	1, 2 3
–	PE_i	Pre-Emphasis, High Band	1.6	2.0	2.4	dB	
–	DC_i	Tone Output DC Bias (V + = 2.5) (V + = 3.5)	 1.5	1.25		V V	
–	R_E	Tone Output Load		10		KΩ	4
–	T_{RIS}	Tone Output Rise Time		1.0		ms	5
–	DIS	Output Distortion		5.0	8.0	%	3
–	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-Signal Delay	40			ms	6
2	T_{ISD}	Inter-Signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

Notes : 1. O dBm equals 1 mW power into 600 ohms or 775 mVolts. Important Note : The MK53762 is designed to drive a 10 kohm load. The 600 ohm load is only for reference.
2. Single tone (low group) as measured at pin 10, $T_A = 25$ °C.
3. Supply voltage = 2.5 to 6 Volts, $R_E = 10$ kohms.
4. Supply voltage = 2.5 Volts. These specifications are supply-dependent
5. Time from beginning of tone output waveform to 90 % of final magnitude of either frequency. Crystal parameters suggested for proper operation are $R_S < 100$ ohms, $L_m = 96$ mH, $C_m = 0.02$ pF, $C_h = 5$ pF, f = 3.579545 MHz, and $C_L = 18$ pF
6. Time from initial key input until beginning of signaling.

AC CHARACTERISTICS – KEYPAD INPUTS, PACIFIER TONE
(Numbers in left hand column refer to the timing diagrams.)

N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
3	T_{KD}	Keypad Debounce Time		32		ms	1
–	F_{KS}	Keypad Scan Frequency		250		Hz	1
–	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
–	T_{HFP}	Hookflash Timing		560		ms	1

Notes : 1. Crystal oscillator accuracy directly affects these times.

AC CHARACTERISTICS – PULSE MODE OPERATION

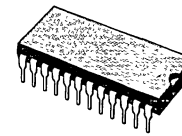
N°	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
–	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

Notes : 1. 10 PPS is the nominal rate
2. Figure 8 illustrates this relationship.

REPERTORY WORLD DIALER™

ADVANCE DATA

- STORAGE OF THIRTEEN 18-DIGIT NUMBERS : 3 EMERGENCY LOCATIONS, AND 10 ADDITIONAL LOCATIONS INCLUDING LNR (last number redial)
- ALL LOCATIONS CAN BE ACCESSED WITH SINGLE KEY INPUTS ALTHOUGH THE OPTION IS AVAILABLE TO ACCESS 3 EMERGENCY LOCATIONS PLUS LNR DIRECTLY AND TWO KEYS (MEM key plus key 1-9) TO ACCESS THE 9 OTHER MEMORIES
- TWO SELECT PINS ALLOW USER TO SELECT 16 DIFFERENT COUNTRY OPTIONS
- SINGLE CHIP, MIXED MODE DIALER ALLOWS DIALING IN EITHER TONE OR PULSE MODES. A * OR "SOFTSWITCH" KEY INPUT CAN ALSO BE USED TO SWITCH FROM PULSE TO TONE MODE OPERATION AND IS STORED IN MEMORY
- P.I.N. (personal identity number) PROTECTION METHOD
- SLIDING CURSOR METHOD TO SIMPLIFY PABX DIALING
- HOOKSWITCH DEBOUNCE, TRANSIENTS DUE TO LINE REVERSALS AND DROP-OUTS CAN BE MASKED FOR A PERIOD DETERMINED BY EXTERNAL RC
- POWERED FROM TELEPHONE LINE, LOW STANDBY CURRENT AND OPERATING VOLTAGE
- DTMF SIGNAL CONSISTENT WITH KEY ENTRY PERIOD
- MINIMUM DTMF SIGNAL DURATION/SEPARATION GUARANTEED
- TIMED PABX PAUSE MAY BE STORED IN MEMORY
- TIMED FLASH FOR EXTENDED TIMED BREAK



DIP24

ORDER CODE: MK53763N01

DESCRIPTION

The MK53763 is a 24 pin CMOS mixed mode dialer IC. This dialer provides signalling for both TONE (DTMF) and PULSE (LD) modes of operation and it stores up to 13 18-digit numbers including the last number dialed. The user can store all 12 signalling digits plus access several unique functions with single key entries. These functions include : Last Number Dialed (LND), Softswitch, Flash, Pause and 12 memories (M1 - M9 and E1 - E3).

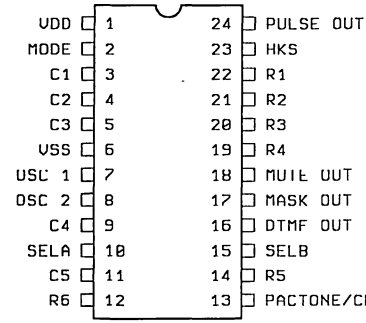
The MK53763 can be switched from PULSE to TONE mode operation through the keypad with a * key input or softswitch (SS) key input. All key inputs following a softswitch command will generate DTMF signals.

Two select pins (SELA, SELB) have been provided which allow the part to be customized for various markets. Rather than selecting and modifying individual parameters which would take many pins or mask options each select pin will select groups of options which have been identified for particular markets.

The MK53763 features a sliding cursor, auto-pause insertion (on some options), manual Pause, and Flash. The DTMF tone output has a guarenteed minimum duty cycle and extends to match the duration of key inputs.

The MK53763 structure and specification are the same of the MK53721 LND world dialer, expanded with 3 emergency and 9 repertory numbers.

PIN CONNECTION (top view)



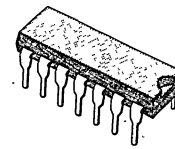
KEYPAD CONFIGURATION

SPEECH CIRCUITS

LOW VOLTAGE TELEPHONE SPEECH CIRCUIT

ADVANCE DATA

- OPERATION DOWN TO 1.3 V/5 mA
- DTMF & BEEP TONE INPUTS
- EXTERNAL MUTING FOR EARPHONE AND MICROPHONE
- MUTE TURNS ON BEEP TONE & DTMF INPUTS AND TURNS OFF EARPHONE & MICROPHONE
- SUITABLE FOR DYNAMIC OR PIEZO EARPHONES AND PIEZO, DYNAMIC OR ELECTRET MICROPHONES



DIP14 Plastic (0.25)

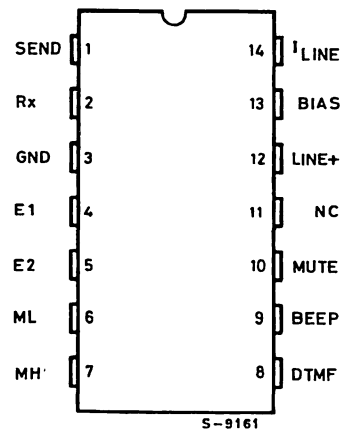
ORDER CODES : L3280B
L3280AB

DESCRIPTION

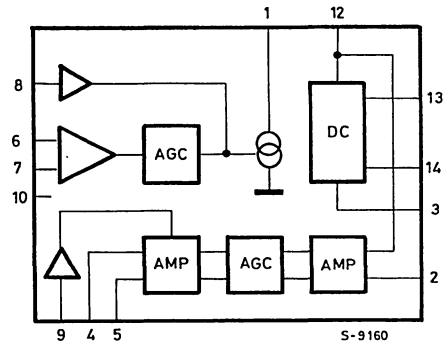
The L3280 is a brand new low voltage speech circuit designed to replace hybrid circuits in telephone sets. It is designed for sets that may be operated in parallel. It features both DTMF input and Beep tone input ; ALC on send and receive and muting input.

Various DC - characteristics can be programmed at pin 14 replacing testing resistor (43 Ω) with proper network value.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse)	20	V
I_L	Line Current	150	mA
P_{tot}	Total Power Dissipation, T_{amb} = 70 °C	1	W
T_{op}	Operating Temperature	– 20 to 55	°C
T_j	Junction Temperature	– 65 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

Figure 1 : Test Circuits.

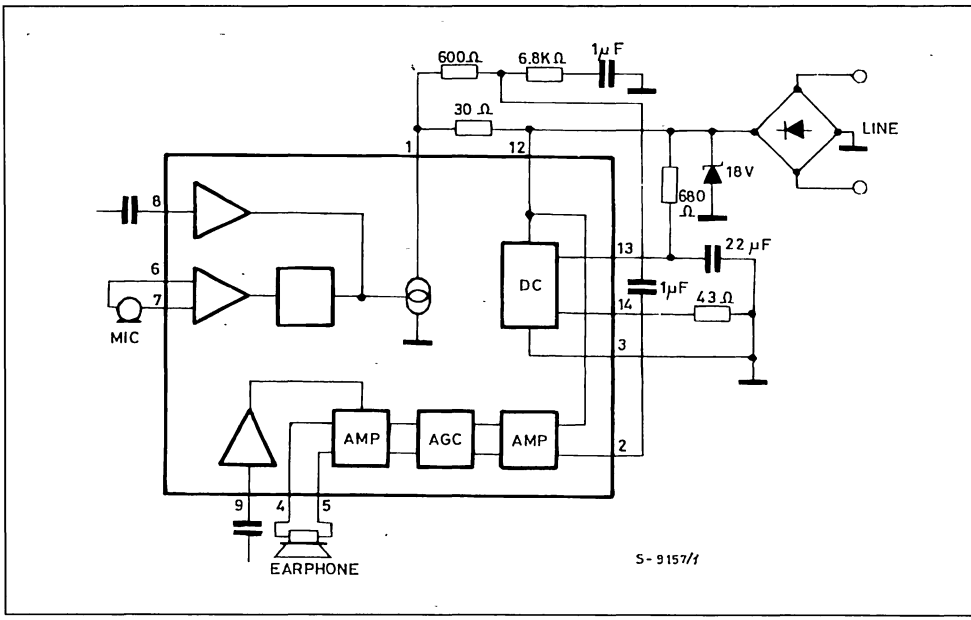
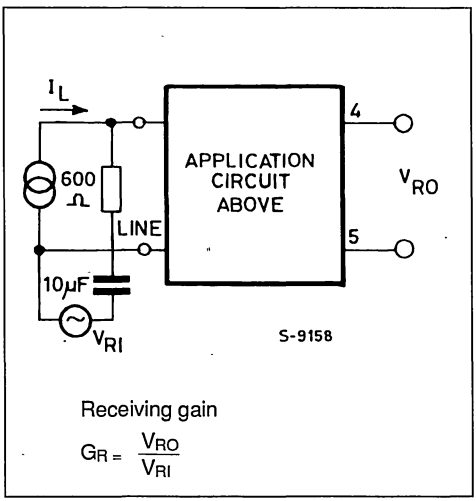


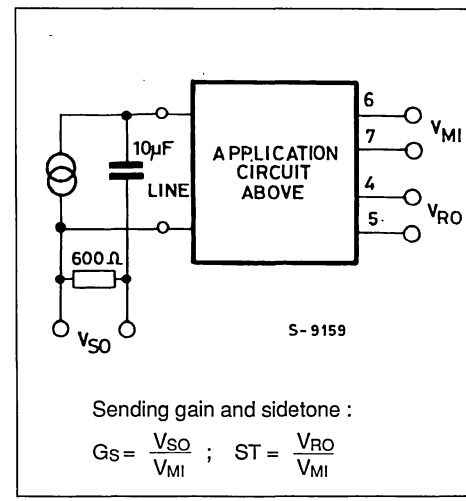
Figure 2 .



Receiving gain

$$G_R = \frac{V_{RO}}{V_{RI}}$$

Figure 3.



Sending gain and sidetone :

$$G_S = \frac{V_{SO}}{V_{MI}} \quad ; \quad ST = \frac{V_{RO}}{V_{MI}}$$

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C ; frequency = 1 Khz ; I_l = 20 mA : mute low ; R1 (pin 14) = 43 Ω unless otherwise spec.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_L	Line Voltage	I_L = 20 mA		2.9	3.2	V
V_L	Line Voltage	I_L = 50 mA		5.8	6.2	V
V_L	Line Voltage	I_L = 80 mA		8.5	10	V
C_{MRR}	Common Mode Rej. Ratio		50			dB
G_S	Sending Gain for B Type	V_{MI} = 2 mV, I_L = 20 mA	47.5	48.5	49.5	dB
G_S	Sending Gain for AB Type	V_{MI} = 2 mV, I_L = 20 mA	47	48.5	50	dB
D_{GS}	Delta Sending Gain	I_L = 70 mA V_{MI} = 2 mV	– 7	– 5.5	– 4	dB
T_{HDS}	Sending Distortion (B type)	V_{SO} = 700 mV			2	%
T_{HDS}	Sending Distortion (AB type)	V_{SO} = 700 mV			5	%
N_{TX}	Sending Noise	I_L = 50 mA V_{MI} = 0 V		– 71		dBm
Z_{MI}	Mic. Input Impedance	V_{MI} = 2 mV	40			KΩ
G_R	Receiving Gain (B type)	I_L = 20 mA V_{RI} = 0.2 V	7.5	8.5	9.5	dB
G_R	Receiving Gain (AB type)	I_L = 20 mA V_{RI} = 0.2 V	7	8.5	10	dB
D_{GR}	Delta Receiving Gain	I_L = 70 mA V_{RI} = 0.2 V	– 7	– 5.5	– 4	dB
T_{HDR}	Receiving Distortion (B type)	V_{RO} = 350 mV ; R_{LOAD} = 350 Ω			2	%
T_{HDR}	Receiving Distortion (AB type)	V_{RO} = 350 mV ; R_{LOAD} = 350 Ω			5	%
N_{RX}	Receiving Noise	V_{RI} = 0 V		300		μV
Z_{RO}	Receiving Output Imped.	R_{LOAD} = 200 Ω V_{RO} = 50 mV		10		Ω
	Sidetone	V_{MI} = 2 mV		40		dB
Z_{ML}	Line Match. Impedance	V_{RI} = 0.2 V	500	600	700	Ω
V_L	Line Voltage	I_L = 5.5 mA		1.3	1.6	V
V_{SO}	Sending Output Voltage	I_L = 5.5 mA, T_{HD} = 5 %	100			mV
I_{RO}	Rec. Output Current	I_L = 5.5 mA, T_{HD} = 5 %	0.7			mA
OPERATION @ I_L = 16 mA						
MULO	Mute Input Low	(Speech)			1	V
MUHI	Mute Input High	(Dial Mode)	2			V
GMF	DTMF Gain (B type)	Vin = 2 mV ; Mute = 2 V	25.5	26.5	27.5	dB
GMF	DTMF Gain (AB type)	Vin = 2 mV ; Mute = 2 V	25	26.5	28	dB
RMF	DTMF Input Impedance	Mute = 2 V	6	8.5		KΩ
THDMF	DTMF distortion (B type)	Mute = 2 V ; Vin = 25 mV			2	%
THDTMF	DTMF Distortion (AB type)	Mute = 2 V ; V_{in} = 25 mV			5	%
G_{beep}	Beeptone Gain	Mute = 2 V ; V_{in} = 25 mV		8.5		dB
R_{beep}	Beeptone Input Imped.	Mute = 2 V ; V_{Bt} = 100 mV	12			KΩ
THD	Beeptone Distortion	Mute = 2 V ; V_{Bt} = 100 mV			5	%
D_{VL}	Delta V_{LINE}	Mute = 2 V ; I_L = 20 mA	0.5		1.2	V

CHARACTERISTIC AT 1 KHz

Figure 4 : Receive Characteristic and Max Output at 2 % THD.

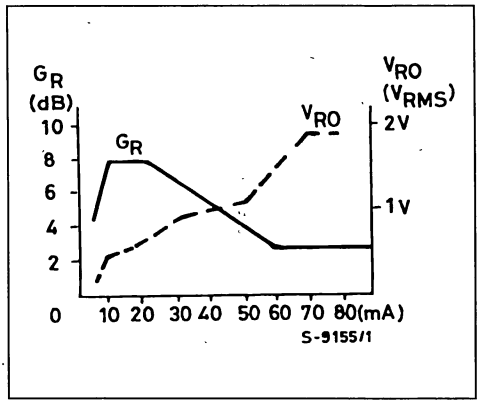


Figure 5 : Sending ALC Characteristic and Max Output at 2 % THD.

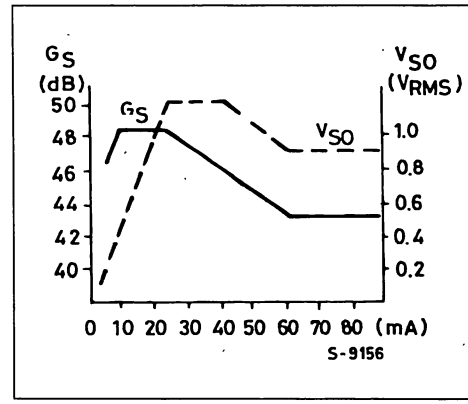
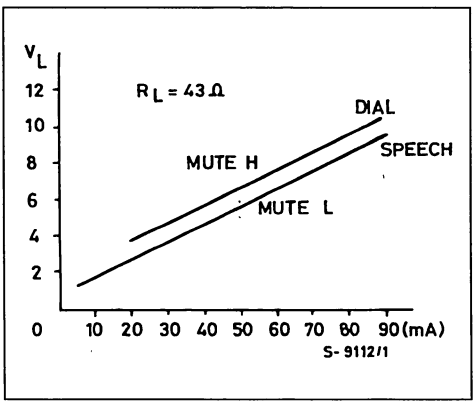


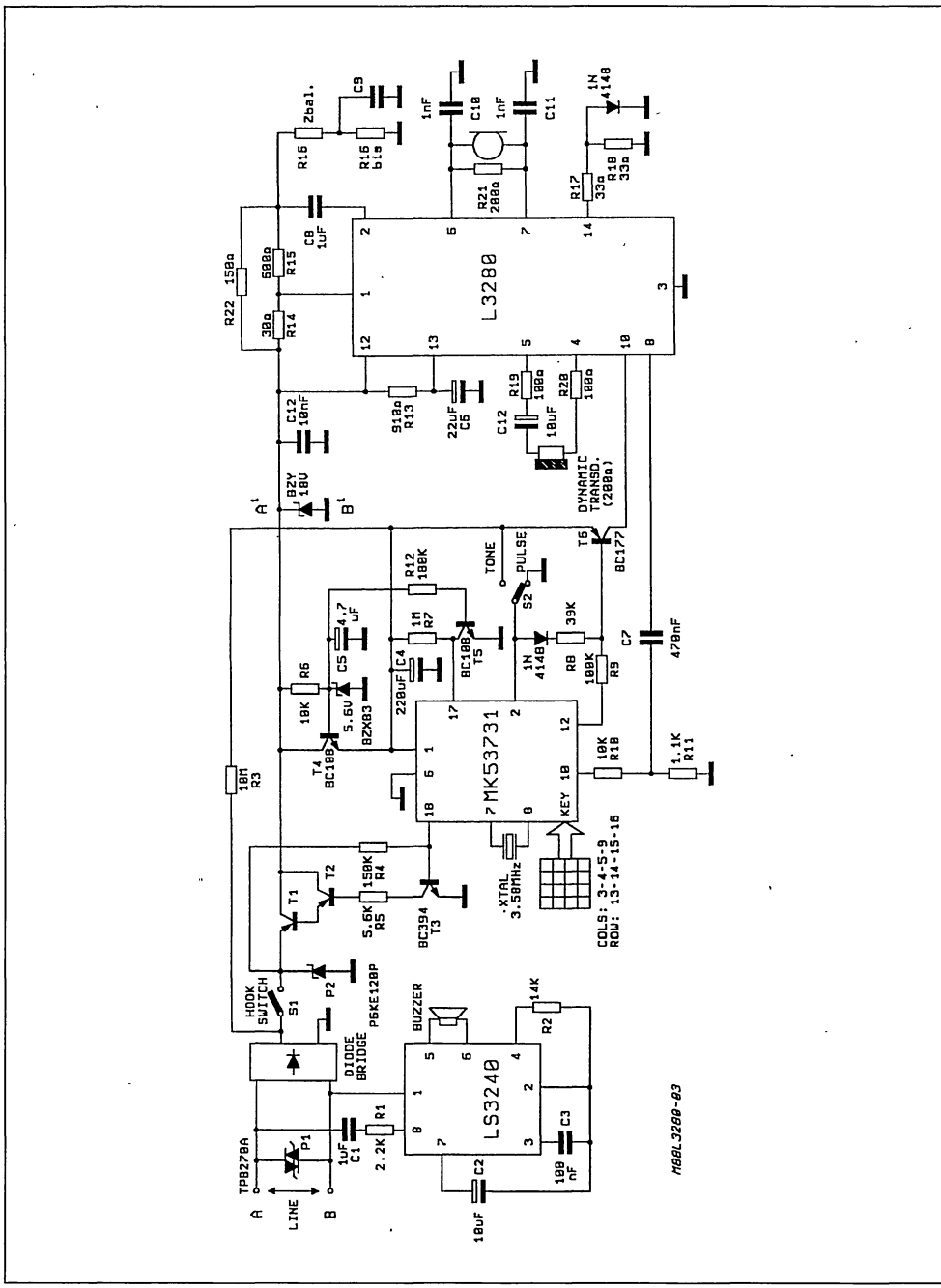
Figure 6 : DC Characteristic Measured between Line and GND.



LOGIC OF MUTE SWITCHING

	DTMF	BEEP	MIC INPUT	RECEIVE INPUT
MUTE H	ACTIVE TO LINE OUTPUT	ACTIVE TO EARPHONE OUTPUT	MUTED	MUTED
MUTE L	MUTED	MUTED	ACTIVE	ACTIVE

Figure 7 : Application Circuit for Dynamic Transducer.



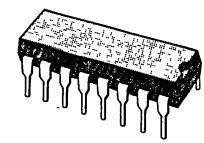
SGS-THOMSON MICROELECTRONICS

LS156

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

- PRESENTS THE PROPER DC PATH FOR THE LINE CURRENT.
- HANDLES THE VOICE SIGNAL, PERFORMING THE 2/4 WIRES INTERFACE AND CHANGING THE GAIN ON BOTH SENDING AND RECEIVING AMPLIFIERS TO COMPENSATE FOR LINE ATTENUATION BY SENSING THE LINE LENGTH THROUGH THE LINE CURRENT.
- ACTS AS LINEAR INTERFACE FOR MF, SUPPLYING A STABILIZED TO THE DIGITAL CHIP AND DELIVERING TO THE LINE THE MF TONES GENERATED BY THE M761.

DIP16



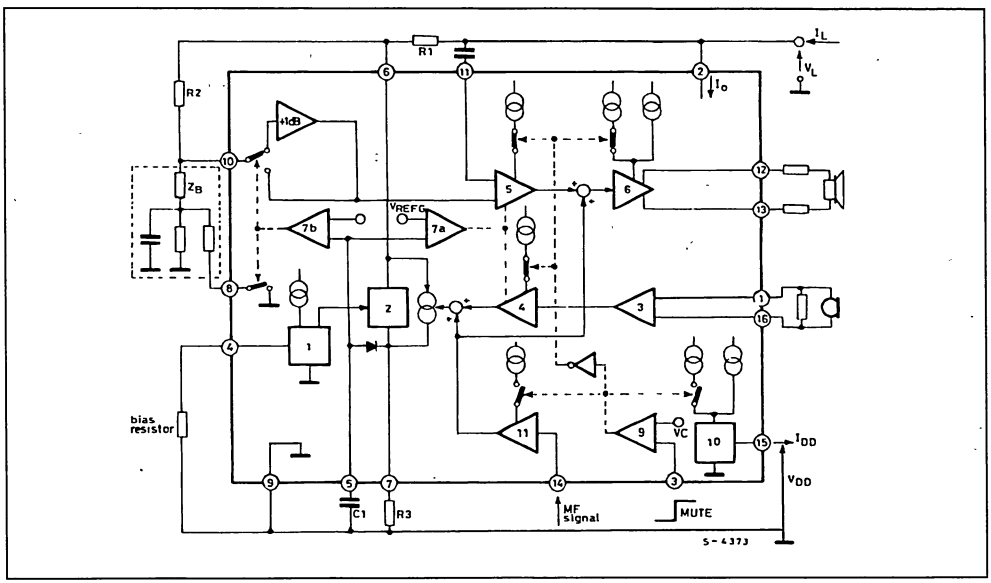
ORDER CODE : LS156B/1

DESCRIPTION

The LS156 is a monolithic integrated circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically piezoceramic capsules, but the device can work also with dynamic ones). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.

In addition to the speech operation, the LS156 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer).

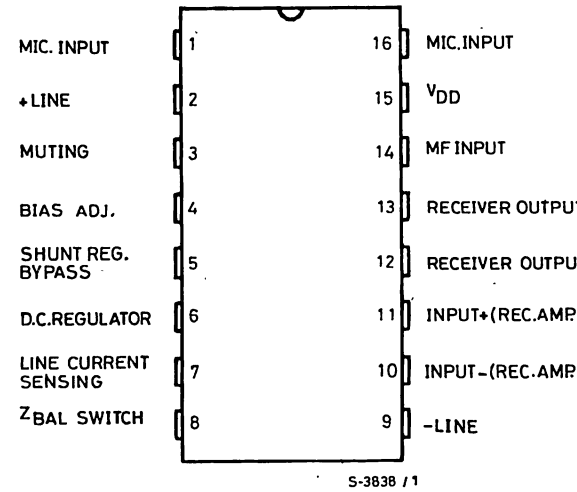
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Line Voltage (3 ms pulse duration)	22	V
	Forward Line Current	150	mA
	Reverse Line Current	– 150	mA
	Total Power Dissipation at T_{amb} = 70 °C	1	W
	Operating Temperature	– 45 to 70	°C
T_j	Storage and Junction Temperature	– 65 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

TEST CIRCUITS

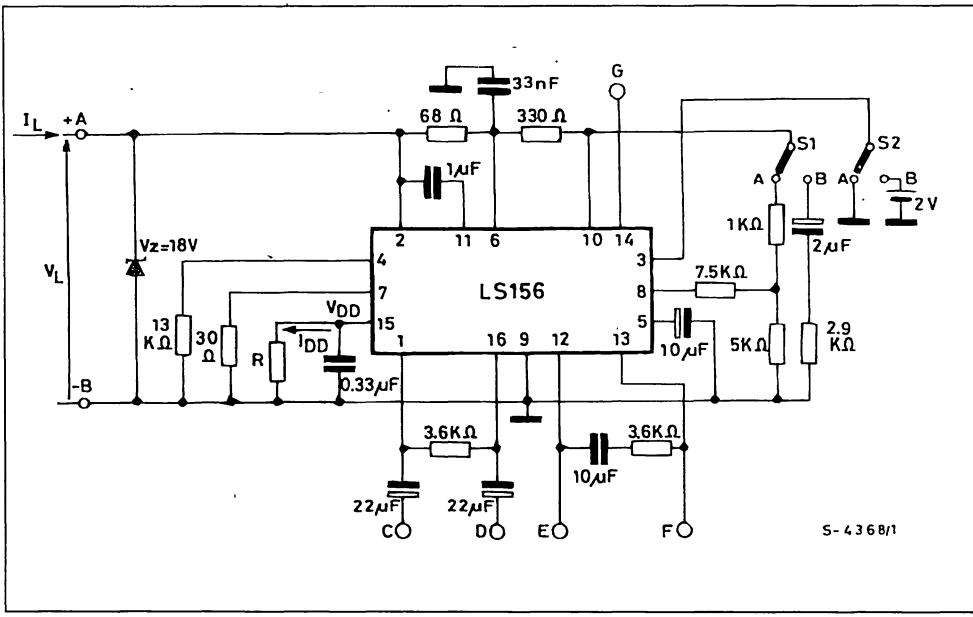
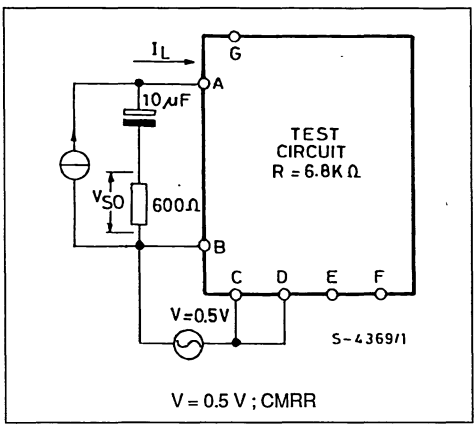
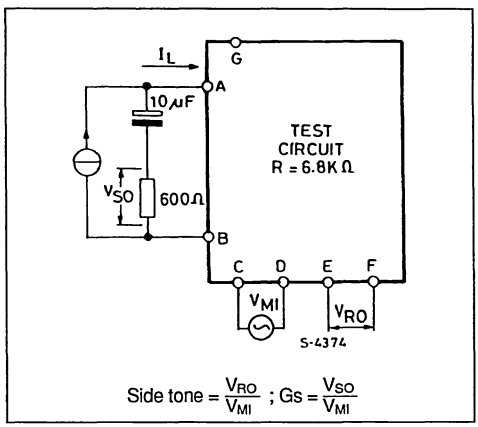


Figure 1.



V = 0.5 V ; CMRR

Figure 2.



Side tone = $\frac{V_{RO}}{V_{MI}}$; Gs = $\frac{V_{SO}}{V_{MI}}$

Figure 3.

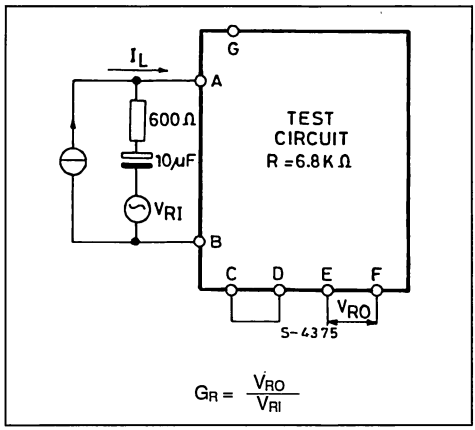
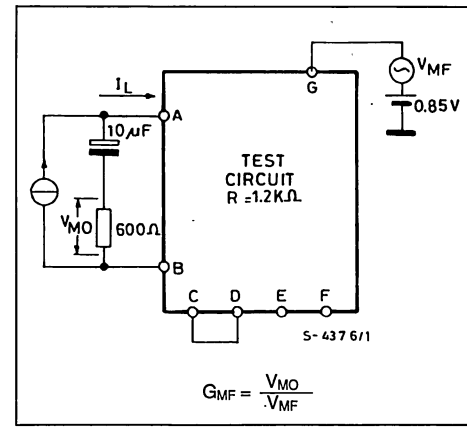


Figure 4.



ELECTRICAL CHARACTERISTICS (refer to the test circuits, S1 and S2 in (a), T_{amb} = – 25 to + 50 °C, f = 200 to 3400 Hz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION							
V_L	Line Voltage	T_{amb} = 25 °C I_L = 12 mA I_L = 20 mA I_L = 80 mA	3.9		4.7 5.5 12.2	V	
CMRR	Common Mode Rejection	f = 1 kHz IL = 12 to 80 mA	50			dB	1
G_s	Sending Gain	T_{amb} = 25 °C f = 1 kHz I_L = 52 mA V_{MI} = 2 mV I_L = 25 mA	44 48	45 49	46 50	dB	2
	Sending Gain Flatness	V_{MI} = 2 mV f_{ref} = 1 kHz I_L = 12 to 80 mA			± 1	dB	2
	Sending Distortion	f = 1 kHz V_{so} = 1 V I_L = 16 to 80 mA V_{so} = 1.3 V			2 10	%	2
	Sending Noise	V_{MI} = 0 V I_L = 40 mA		– 70		dBmp	2
	Microphone Input Impedance Pin 1-16	V_{MI} = 2 mV I_L = 12 to 80 mA	40			kΩ	
	Sending Loss in MF Operation	V_{MI} = 2 mV I_L = 52 mA S_2 in (b) I_L = 25 mA	– 30 – 30			dB	2
G_R	Receiving Gain	V_{RI} = 0.3 V I_L = 52 mA f = 1 kHz I_L = 25 mA T_{amb} = 25 °C	3 7	4 8	5 9	dB	3
	Receiving Gain Flatness	V_{RI} = 0.3 V f_{ref} = 1 kHz I_L = 12 to 80 mA			± 1	dB	3

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION (continued)							
	Receiving Distortion	f = 1 kHz I_L = 12 mA V_{RO} = 1.6 V I_L = 12 mA V_{RO} = 1.9 V I_L = 50 mA V_{RO} = 1.8 V I_L = 50 mA V_{RO} = 2.1 V			2 10 2 10	%	3
	Receiving Noise	V_{RI} = 0 V I_L = 12 to 80 mA		150		µV	3
	Receiver Output Impedance Pin 12-13	V_{RO} = 50 mV I_L = 40 mA			100	Ω	
	Sidetone	f = 1 kHz I_L = 52 mA T_{amb} = 25 °C S_1 in (b) I_L = 25 mA			36 36	dB	2
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3 V f = 1 kHz I_L = 12 to 80 mA	500	600	700	Ω	3
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF Supply Voltage (standby and operation)	I_L = 12 to 80 mA	2.4	2.5		V	
I_{DD}	MF Supply Current Stand by Operation	 I_L = 12 to 80 mA I_L = 12 to 80 mA; S_2 in (b)	 0.5 2			 mA	
	MF Amplifier Gain	I_L = 12 to 80 mA $f_{MF\ in}$ = 1 kHz $V_{MF\ in}$ = 80 mV	15		17	dB	4
V_I	DC Input Voltage Level (pin 14)	$V_{M\ Fin}$ = 80 mV		V_{DD} x 0.3		V	
R_I	Input Impedance (pin 14)	$V_{M\ Fin}$ = 80 mV	40			kΩ	
d	Distortion	$V_{M\ Fin}$ = 110 mV I_L = 12 to 80 mA			2	%	4
	Starting Delay Time	I_L = 12 to 80 mA			5	ms	
	Muting Threshold Voltage (pin 3)	Speech Operation			1	V	
		MF Operation	1.6			V	
	Muting Stand by Current (pin 3))	I_L = 12 to 80 mA			− 10	µA	
	Muting Operating Current (pin 3)	I_L = 12 to 80 mA S_2 in (b)			+ 10	µA	

CIRCUIT DESCRIPTION

1. DC CHARACTERISTIC

In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristics V_L, I_L.

The DC characteristic of the LS156 it is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3. The equivalent circuit of the total system is shown in fig. 5.

A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).

The recommended minimum of I_o is 7.5 mA.

The voltage Vo ≅ 3.8 V of the shunt regulator is independent of the line current.

The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).

Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

The difference I_L - I_o flows through the shunt regulator being I_b negligible.

I_a is an internal constant current generator ; hence $V_o = V_{BED1} + I_a \cdot R_a \cong 3.8$ V. The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.

It is important to note that the DC voltage at pin 5 is proportional to line current ($V_5 = V_7 + V_{BED1} \cong (I_L \cdot I_o) R_3 + V_{BED1}$).

Figure 5 : Equivalent DC Load to the Line.

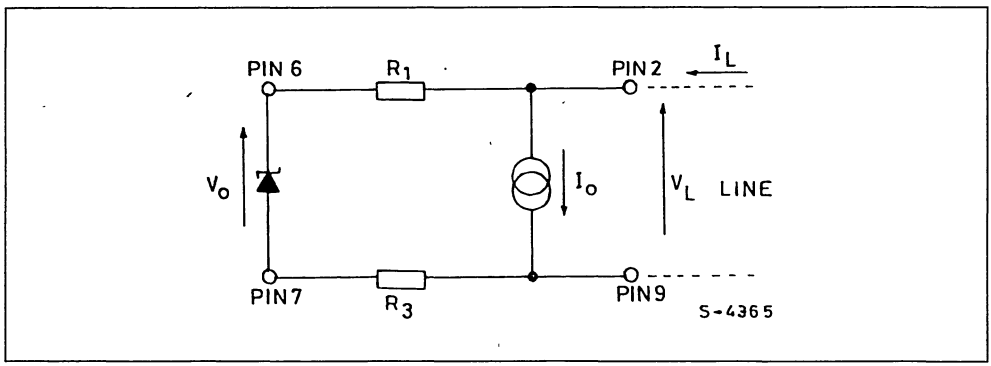
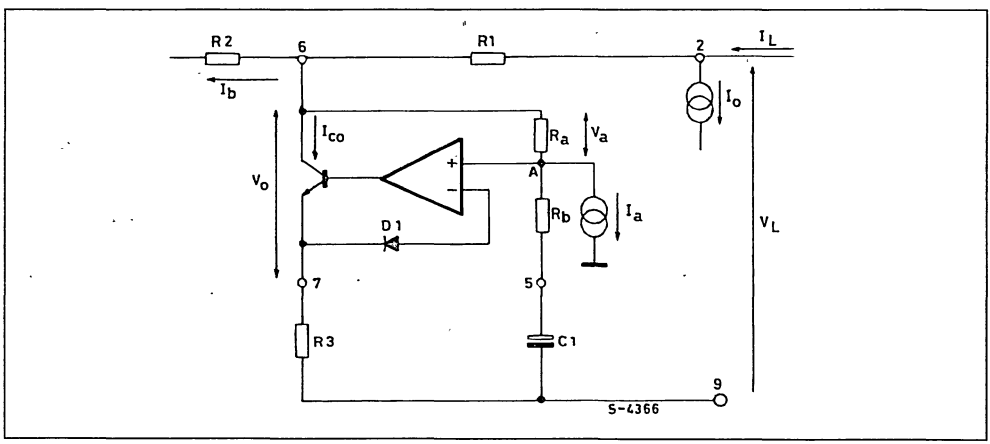


Figure 6 : Circuit Configuration of the Shunt Regulator.



2. 2/4 WIRES CONVERSION

The LS156 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 7).

For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$) ; the main part is sent to the line via R_1.

In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.

The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6\text{-}9}}{\Delta I_{6\text{-}9}}$.

From fig. 6, considering C_1 as a short circuit for AC signal, any variation ΔV_6 generates a variation.

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R_3}$$

Therefore

$$Z_M = \frac{V_6}{DI} = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R_1 + Z_M \,//\, (R_2 + Z_B)$$

By choosing $Z_M >> R_1$ and $Z_B \geq Z_M$

$$Z_{ML} \cong Z_M = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

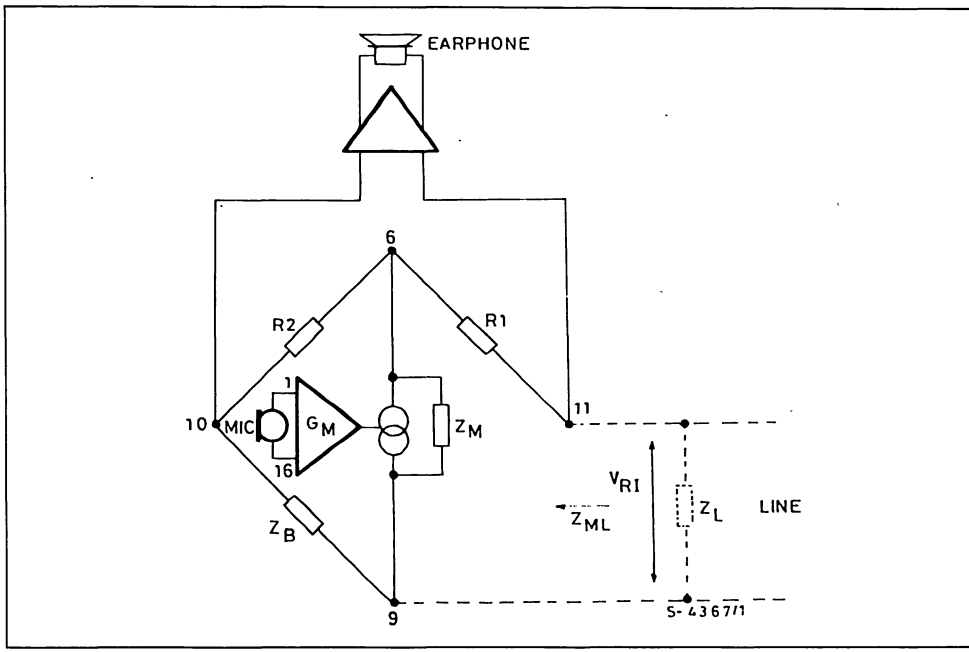
The received signal amplitude across pin 11 and 10 can be changed using different values of R_1 (of course the relationship $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$ must be always valid).

The received signal is related to R_1 value according to the approximated relationship

$$V_R = 2 \cdot V_{RI} \quad \frac{R_1}{R_1 + Z_M}$$

Note that by changing the value of R_1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

Figure 7 : Two to Four Wires Conversion.



3. AUTOMATIC GAIN CONTROL

The LS156 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation by sensing the line length through the line current.

The line current is sensed across R_3 (see fig. 6) and transferred to pin 5 by the regulator.

$$V_5 = V_{BED1} + V_7 \cong V_{BED1} + (I_L - I_o) \cdot R_3.$$

The pin 5 V_5 voltage, after a comparison with an internal reference V_{REFG} (see the block diagram) is used to modify the gain of the amplifiers (4) and (5) on both the sending and receiving path.

The starting point of the automatic level control is obtained at I_L = 25 mA when the drain current I_o = 7.5 mA.

Minimum gain is reached for a line current of about 52 mA for the same drain current I_o = 7.5 mA.

When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly :

Automatic switching of the balance network Z_B for a better sidetone is performed by the LS156 through V_5 information. This information, proportional to the line length, drives the comparator (7 b) (see the block diagram).

For long lines, the impedance level of Z_B is high (pin 8 open) and the additional + 1 dB gain is added to the receiving amplifier chain.

For short lines, the impedance level of Z_B is automatically switched to a lower value (pin 8 shorted to ground) and the additional + 1 dB block is bypassed by the received signal.

A built in hysteresis circuit avoids uncertain operation of the comparator.

4. TRANSDUCERS INTERFACING

The microphone amplifier (3) has a differential input stage with high impedance ($\cong$ 40 kΩ) so allowing a good matching to the microphone by means of external resistors without affecting the sending gain.

The receiving output stage (6) is particularly intended to drive piezoceramic capsules. [Low output impedance (100 Ω max) ; high voltage swing (close to V_L) ; current capability of 1.8 mAp].

When a dynamic capsule is used, it is useful to decrease the receiving gain by decreasing R_1 value (see the relationship for V_R).

With very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. MULTIFREQUENCY INTERFACING

The LS156 acts a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.

When no key of the keyboard is pressed the mute state is low and the LS156 feeds the M761 through pin 15 with low current (standby operation of the M761). The oscillator of the M761 is not operating. When one key is pressed, the M761 sends a "high state" mute condition to the LS156. A voltage comparator (9) of LS156 drives internal electronic switches : the current delivered by the voltage supply (10) is increased to allow the operation of the oscillator. This extra current is diverted by the receiving and sending section of the LS156 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.

A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber ; the MF amplifier (11) delivers the dial tones to the sending paths.

The application circuit shown in fig. 9 fulfils the EUROPE II standard (– 6, – 8 dBm). If the EUROPE I levels are required (– 9, – 11 dBm), an external divider must be used (fig. 11).

The mute function can be used also when a temporary inhibition of the output signal is requested.

APPLICATION INFORMATION

The circuits shown in fig. 8 and fig. 11 are referred to the Italian standard. The fig. 10 shows the connection for mute function (inhibition of the output stage when it is requested) by using an external switch at pin 3.

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
R_1	68 Ω	Bridge Resistors	R_1 controls the receiving gain. The Ratio R_2/R_1 fixes the amount of signal delivered to the line. R_1 helps in fixing the DC characteristic (see R_3 note).
R_2	330 Ω		
R_3	30 Ω	Line Current Sensing. Fixing DC Characteristics	The relationships involving R_3 are : • $Z_{ML} = (20\ R_3 \,//\, Z_B) + R_1$ • $G_S = K \cdot \frac{Z_L \,//\, Z_{ML}}{R_3}$ • $V_L = (I_L - I_o)(R_3 + R_1) + V_o$; $V_o = 3.8$ V. Without any problem it is possible to have a Z_{ML} ranging from 500 up to 900 Ω.
R_4	13 kΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R_4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point. (see fig. 12).
R_5	7.5 kΩ	Balance Network	The balance network has two possible impedance levels, selected by the circuit referring to the line current (i.e. to the line length) in order to optimize the sidetone. It's possible to change R_5, R_6, R_7 values in order to improve the matching to different lines; in any case : $\frac{Z_B}{Z_L} = \frac{R_2}{R_1}$ with the two possible values for Z_B : $Z_{B(1)} = R_7 + R_6 \,//\, C_4$ (long lines) $Z_{B(2)} = R_7 + (R_6 \,//\, R_5) \,//\, C_4$ (short lines) (see fig. 13).
R_6	5.1 kΩ		
R_7	1 kΩ		
$R_8 - R_8'$	1.8 kΩ	Receiver Impedance Matching	R_8 and R_8' must be equal; the suggested value is good for matching to piezoceramic capsule; there is no problem in increasing and decreasing (down to 0 Ω) this value, but when low resistance levels are used a DC decoupling must be inserted to stop the current due to the receiver output offset voltage (max 400 mV).
R_9	3.6 kΩ	Microphone Impedance Matching	The suggested value is typical for a piezoceramic microphone, but it is possible to choose R_9 in a wide range.
C_1	10 µF	Regulator AC Bypass	A value greater than 10 µF gives a system start time too high for low current line during MF operation; a lower value gives an alteration of the AC line impedance at low frequency
C_2	47 nF	Matching to a Capacitive Line	C_2 changes with the characteristics of the transmission line.
C_3	82 nF	Receiving Gain Flatness	C_3 depends on balancing and line impedance versus frequency.
C_4	22 nF	Balance Network	See Note for R_7, R_6, R_5.
C_5	0.33 µF	DC Filtering	The C_5 range is from 0.1 µF to 0.47 µF. The lowest value is ripple limited, the higher value is starting up time limited.
$C_6 - C_7$	1000 pF	RF Bypass	
C_8	1 µF	Dc Decoupling for Receiving Input	The DC offset is very low. An electrolitic capacitor can be used.

Figure 8 : Application Circuit with Multifrequency (EUROPE II std.).

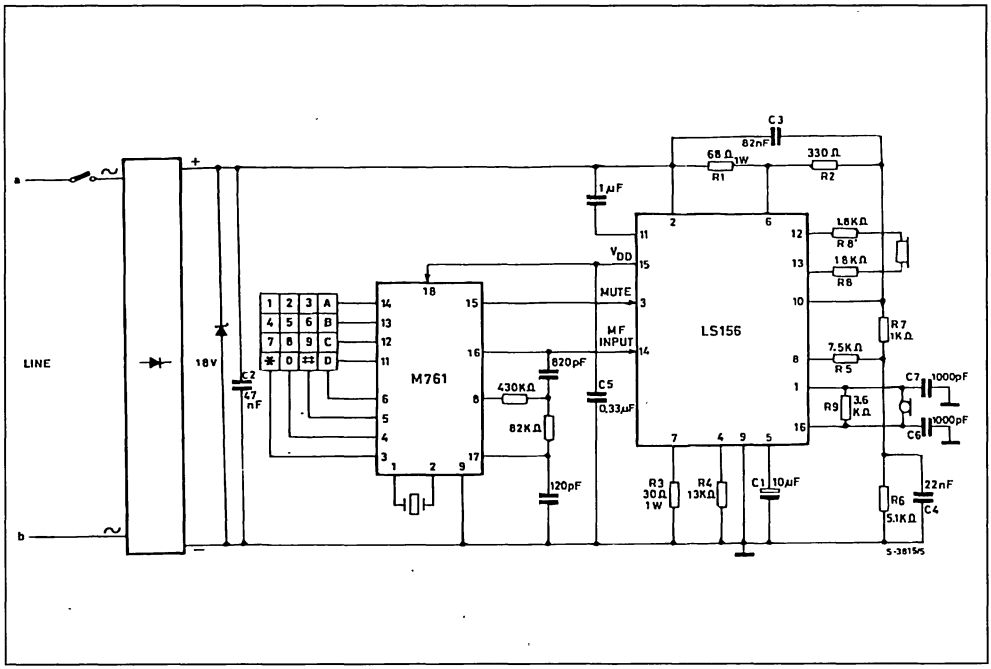


Figure 9 : Application Circuit with Multifrequency (EUROP I std.).

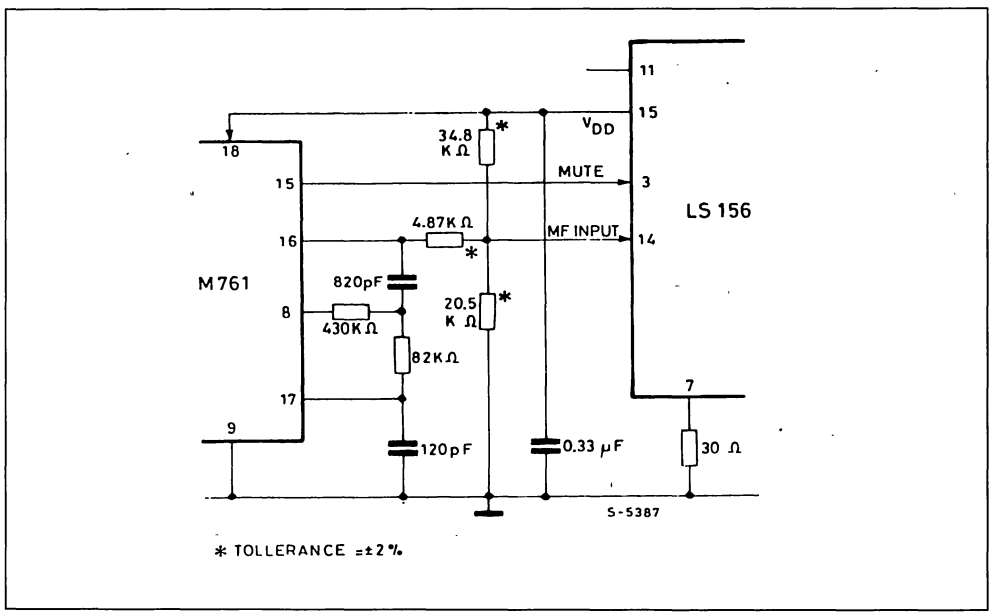


Figure 10 : External Mute Function.

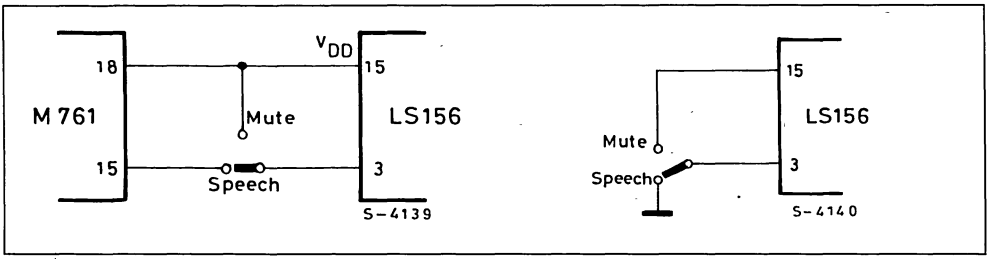


Figure 11 : Application Circuit without Multifrequency.

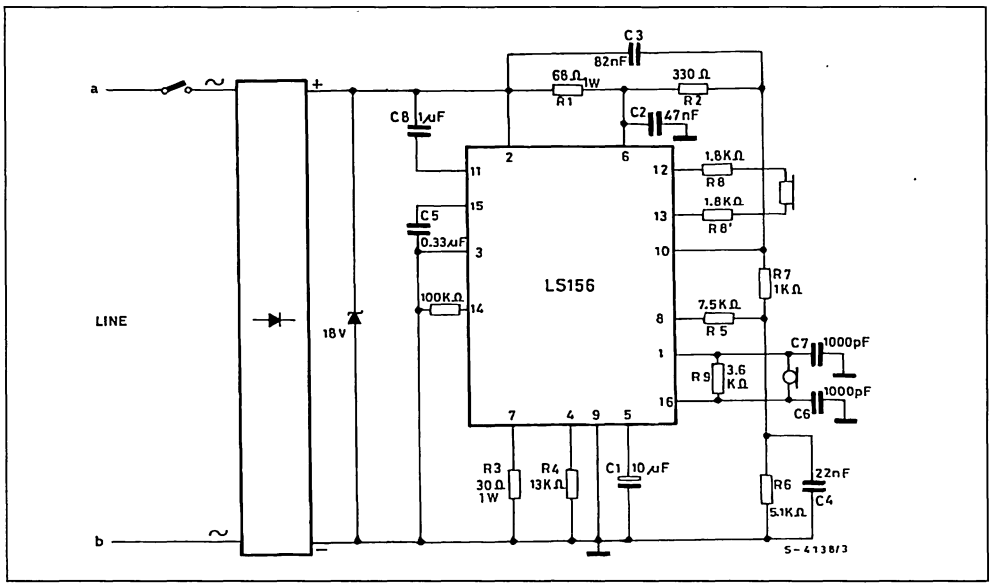


Figure 12 : Sending and Receiving Gain vs. Line Current.

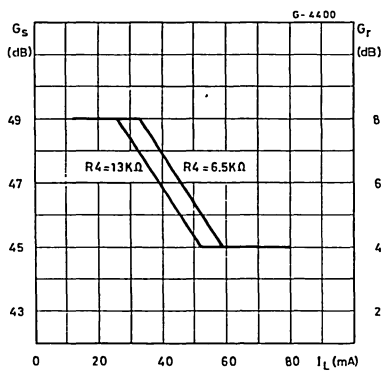
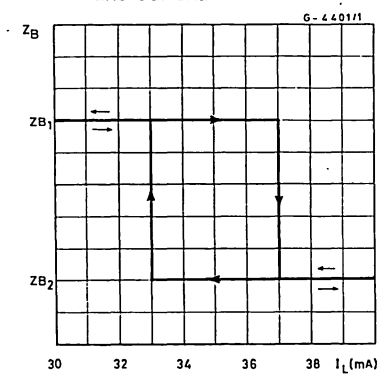


Figure 13 : Balance Network Impedance vs. Line Current.



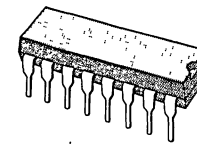
SGS-THOMSON MICROELECTRONICS

LS256

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

ADVANCE DATA

- PRESENTS THE PROPER DC PATH FOR THE LINE CURRENT
- HANDLES THE VOICE SIGNAL, PERFORMING THE 2/4 WIRES INTERFACE AND CHANGING THE GAIN ON BOTH SENDING AND RECEIVING AMPLIFIERS TO COMPENSATE FOR LINE ATTENUATION BY SENSING THE LINE LENGTH THROUGH THE LINE CURRENT
- ACTS AS LINEAR INTERFACE FOR MF, SUPPLYING A STABILIZED TO THE DIGITAL CHIP AND DELIVERING TO THE LINE THE MF TONE GENERATED BY THE DIALER



DIP16
(Plastic 0.25)

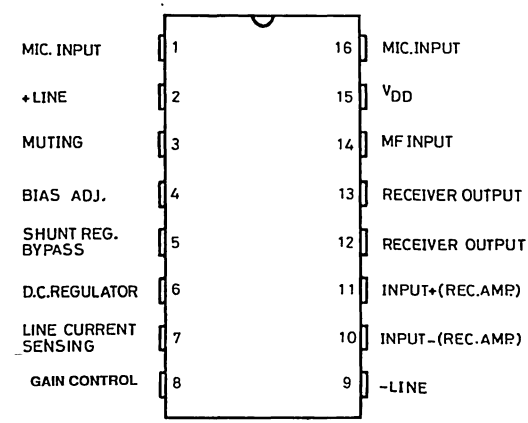
ORDER CODE : LS256B

DESCRIPTION

The LS256 is a monolithic integrated circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically piezoceramic capsules, but the device can work also with dynamic ones). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.

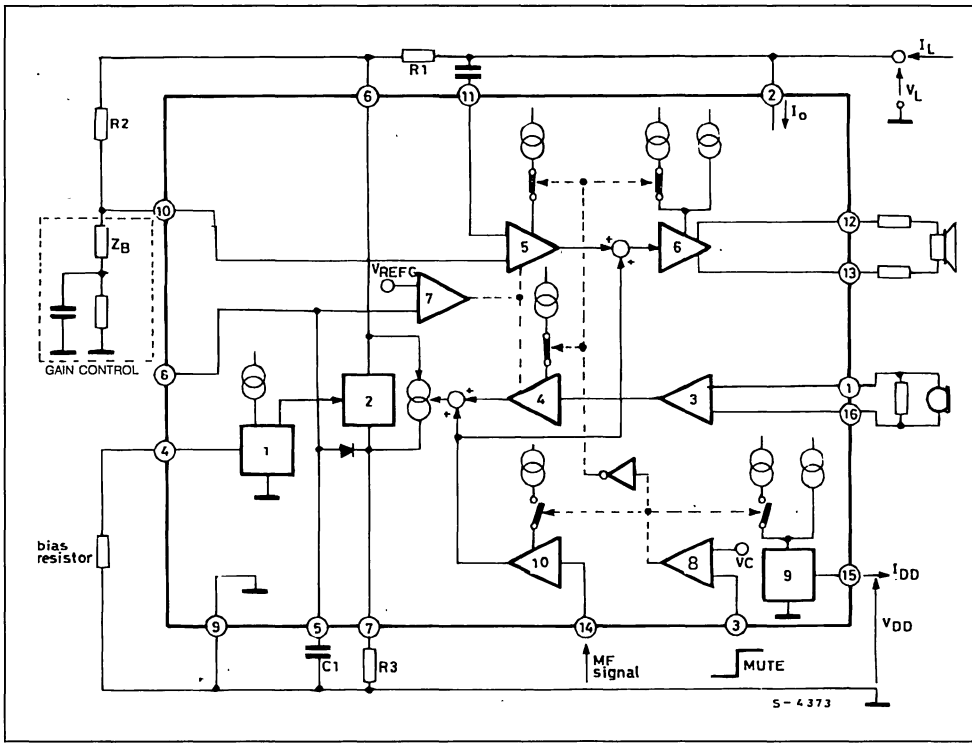
In addition to the speech operation, the LS256 acts as an interface for the MF tone signal.

PIN CONNECTION (top view)



S-4919

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3ms pulse duration)	22	V
I_L	Forward Line Current	150	mA
I_L	Reverse Line Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70°C	1	W
T_{op}	Operating Temperature	– 45 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 65 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

TEST CIRCUITS

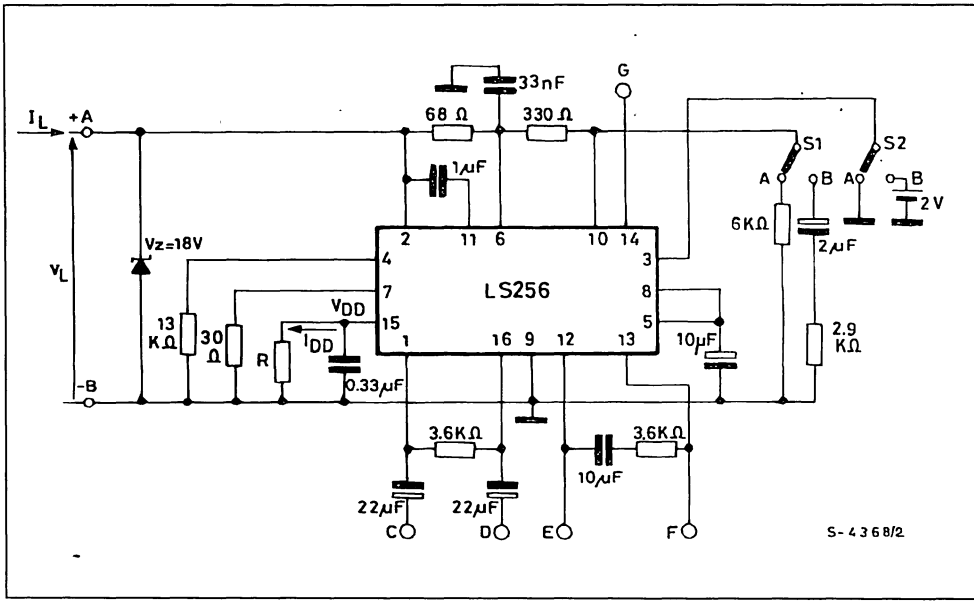


Figure 1.

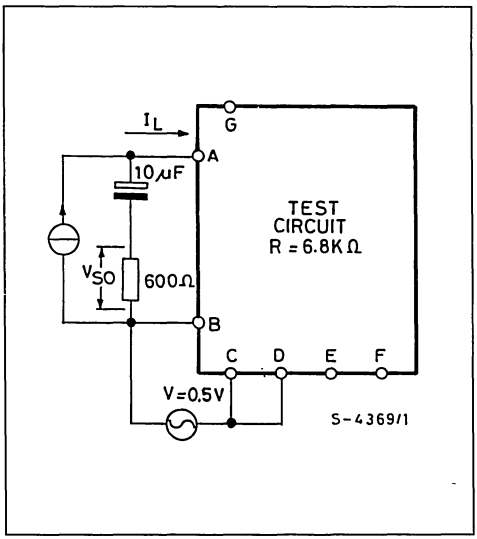


Figure 2.

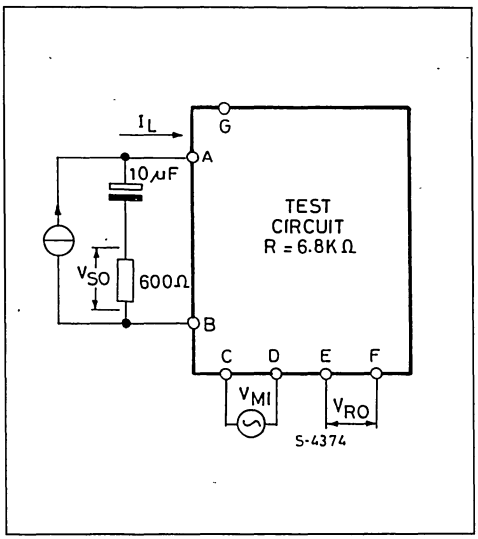
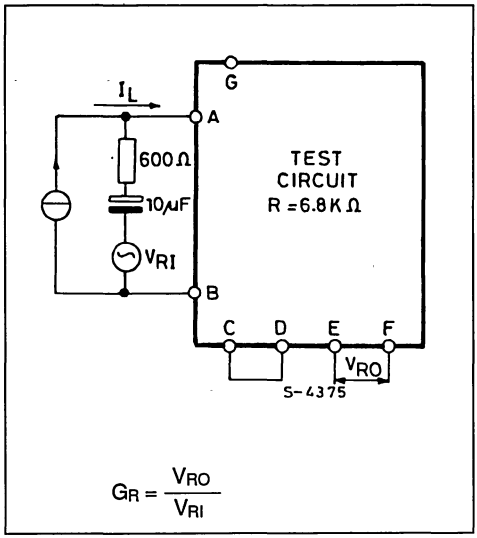
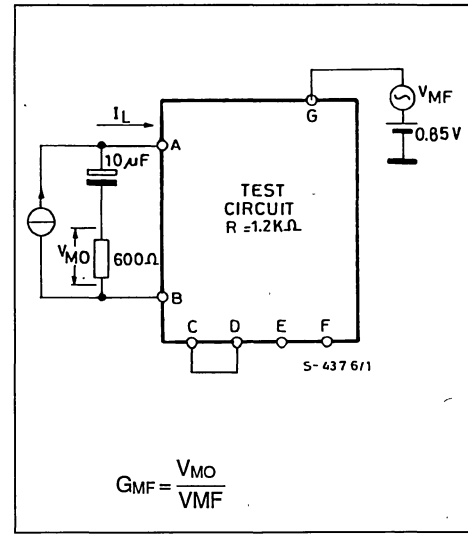


Figure 3.



$$G_R = \frac{V_{RO}}{V_{RI}}$$

Figure 4.



$$G_{MF} = \frac{V_{MO}}{VMF}$$

ELECTRICAL CHARACTERISTICS

(refer to the test circuits, S1, S2 in (a), T_{amb} = – 25 to + 50°C, f = 200 to 3400Hz, unless otherwise specified)

SPEECH OPERATION

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
V_L	Line Voltage	T_{amb} = 25°C	I_L = 12mA I_L = 20mA I_L = 80mA	3.9		4.7 5.5 12.2	V	
CMRR	Common Mode Rejection	f = 1KHz	I_L = 12 to 80mA	50			dB	1
G_S	Sending Gain	T_{amb} = 25°C f = 1KHz V_{MI} = 2mV	I_L = 52mA I_L = 25mA	44 48	45 49	46 50	dB	2
	Sending Gain Flatness	V_{MI} = 2mV	f_{ref} = 1KHz I_L = 12 to 80mA			± 1	dB	2
	Sending Distortion	f = 1KHz I_L = 16 to 80mA	V_{SO} = 1V V_{SO} = 1.3V			2 10	%	2
	Sending Noise	V_{MI} = 0V	I_L = 40mA			– 68.5	dBmp	2
	Microphone Input Impedance Pin 1-16	V_{MI} = 2mV	I_L = 12 to 80mA	40			KΩ	
	Sending Loss in MF Operation	V_{MI} = 2mV S_2 in (b)	I_L = 52mA I_L = 25mA	– 30 – 30			dB	2

ELECTRICAL CHARACTERISTICS (continued)

SPEECH OPERATION (continued)

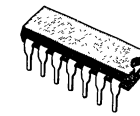
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
G_R	Receiving Gain	V_{R1} = 0.3V I_L = 52mA f = 1KHz I_L = 25mA T_{amb} = 25°C	2.5 7	3.5 8	4.5 9	dB	3
	Receiving Gain Flatness	V_{RI} = 0.3V f_{ref} = 1KHz I_L = 12 to 80mA			± 1	dB	3
	Receiving Distortion	f = 1KHz I_L = 12mA V_{RO} = 1.6V I_L = 12mA V_{RO} = 1.9V I_L = 50mA V_{RO} = 1.8V I_L = 50mA V_{RO} = 2.1V			2 10 2 10	%	3
	Receiving Noise	V_{RI} = 0V I_L = 12 to 80mA		100	500	µV	3
	Receiver Output Impedance Pin 12-13	V_{RO} = 50mV I_L = 40mA			100	Ω	
	Sidetone	F = 1KHZ I_L = 52mA T_{amb} = 25°C S_1 in (b) I_L = 25mA			36 36	dB	2
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3V f = 1KHz I_L = 12 to 80mA	500	600	700	Ω	3

MULTIFREQUENCY SYNTHESIZER INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{DD}	MF Supply Voltage (standby and operation)	I_L = 12 to 80mA	2.35	2.5		V	
I_{DD}	MF Supply Current Stand by Operation	I_L = 12 to 80mA I_L = 12 to 80mA ; S_2 in (b)	 0.5 2			mA	
	MF Amplifier Gain	I_L = 12 to 80mA f_{MF} in = 1KHz V_{MF} in = 80mV	15		17	dB	4
V_I	DC Input Voltage Level (pin 14)	$V_{M\,Fin}$ = 80mV		.3V_{DD}		V	
R_I	Input Impedance (pin 14)	$V_{M\,Fin}$ = 80mV	40			KΩ	
d	Distortion	$V_{M\,Fin}$ = 110mV I_L = 16 to 80mA			2	%	4
	Starting Delay Time	I_L = 12 to 80mA			5	ms	
	Muting Threshold Voltage (pin 3)	Speech Operation			1	V	
		MF Operation	1.6			V	
	Muting Stand by Current (pin 3)	I_L = 12 to 80mA			− 10	µA	
	Muting Operating Current (pin 3)	I_L = 12 to 80mA S_2 in (b)			+ 10	µA	

TELEPHONE SPEECH CIRCUITS

- 2/4 WIRE INTERFACE
- OPERATES DOWN TO 4 mA
- 3.5 V_{pp} DYNAMIC IN SENDING AT 25 mA



DIP14
(Plastic)

ORDER CODE : LS285AB1

DESCRIPTION

The LS285 is monolithic integrated circuits for replacement of the hybrid circuit (2-4 wire interface) in conventional telephones interfacing the two transducers to the line and providing a controlled amount of sidetone.

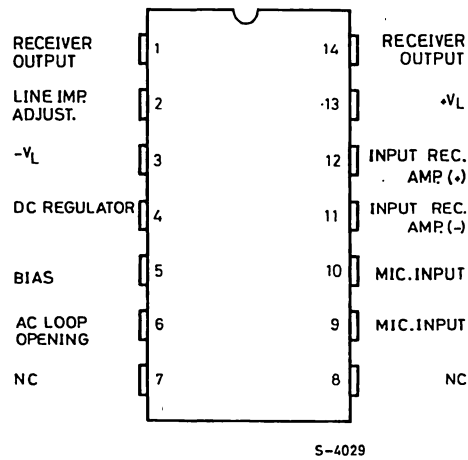
The same type of transducer can be used for both transmitter and receiver, usually a 350 Ω dynamic type.

By sensing the line current, LS285 adjusts the gain in both directions to compensate for line attenuation.

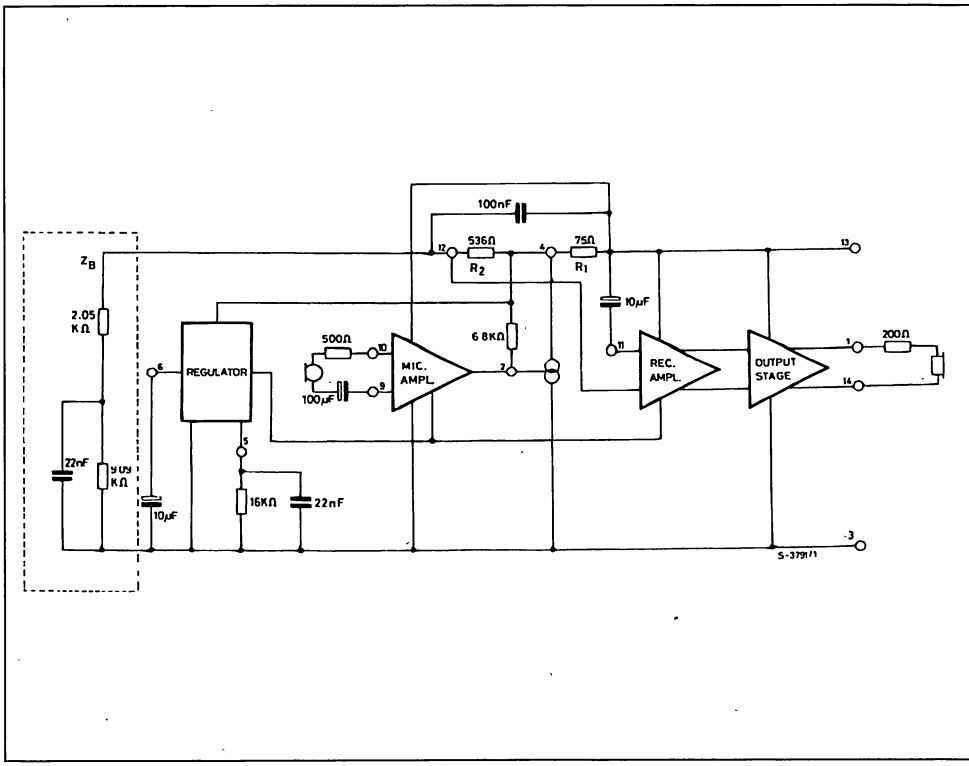
Output impedance can be matched to the line, independent of transducer impedance.

The LS285 is packaged in a 14 lead dual in–line plastic package.

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse duration)	22	V
I_L	Forward Current	120	mA
I_L	Reverse Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{stg}	Storage and Junction Temperature	– 55 to 150	°C
T_{op}	Operating Temperature	– 40 to 70	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

DESCRIPTION

The LS285 is based on a bridge configuration.

They contain a regulator block, a sending amplifier and a receiver amplifier.

The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length. It provides DC characteristics in line with CEPT standards.

The transmit/receiver amplifiers are connected to the line via an external bridge to provide sidetone attenuation.

The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line lenght. When he is hearing, the signal level on the receiver capsule is constant.

The amplifiers can also be matched to different transducers simply by varying external components. Gain variation over the operating temperature range is less than ± 1 dB.

The impedance to the line can be adjusted ; without any change in circuit parameters ; by changing an external resistor (6.8 KΩ at pin 2).

BASIC CIRCUIT CONFIGURATION.

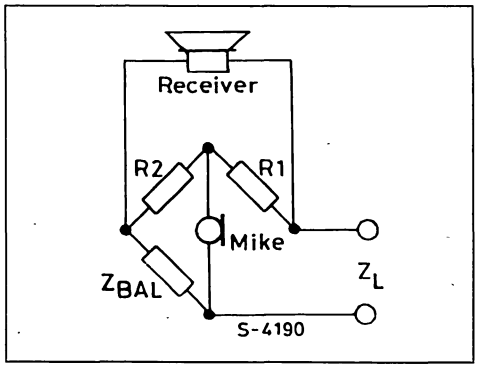


Figure 1 : Test Circuit.

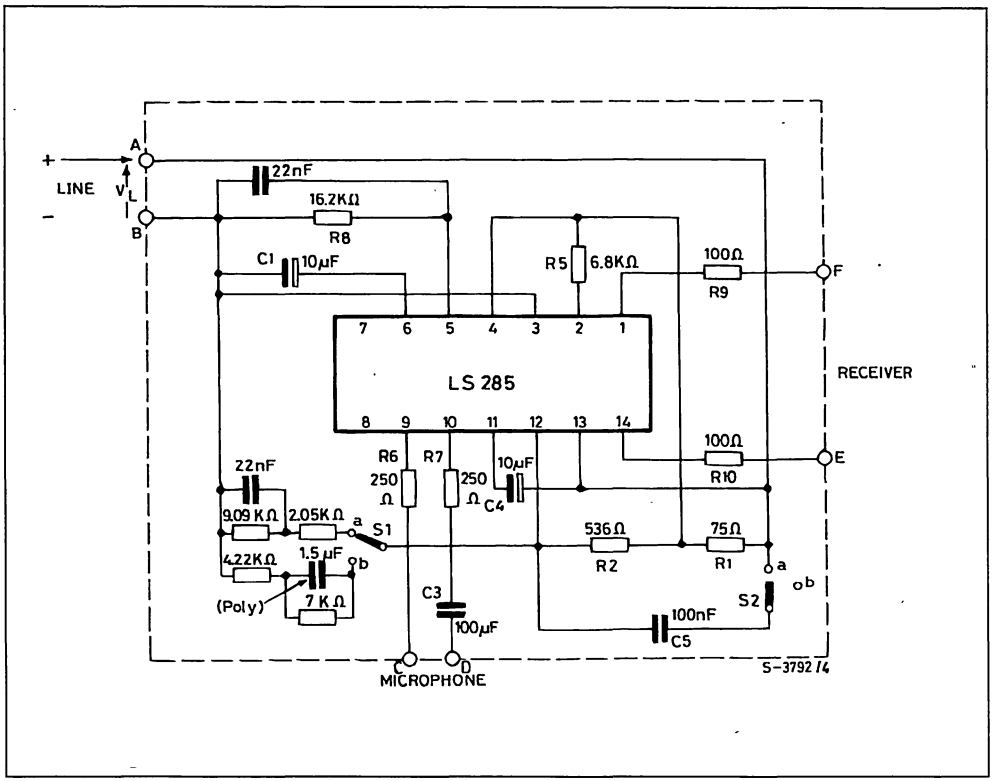
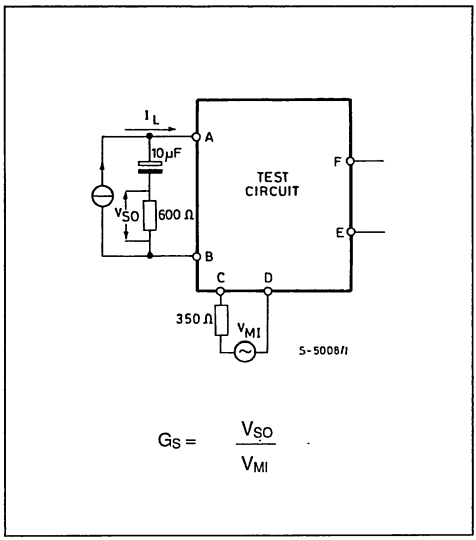
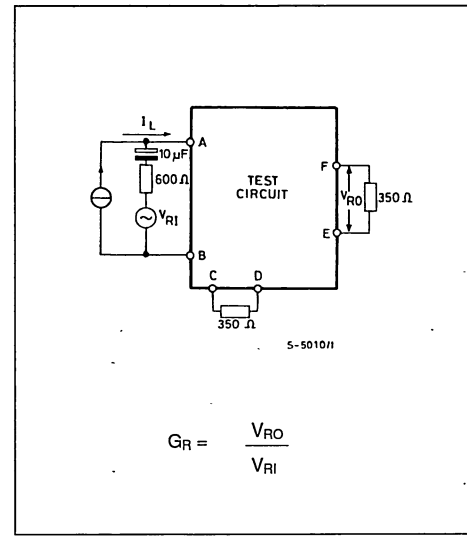


Figure 2 : Sending Gain.



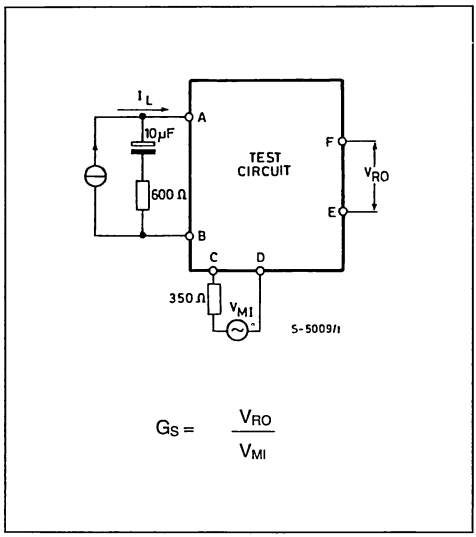
$$G_S = \frac{V_{SO}}{V_{MI}}$$

Figure 3 : Receiving Gain.



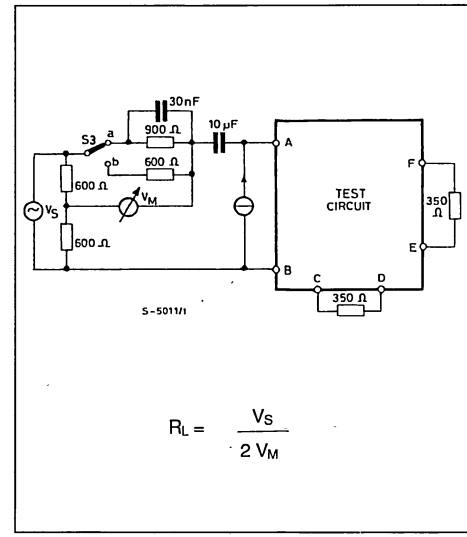
$$G_R = \frac{V_{RO}}{V_{RI}}$$

Figure 4 : Sidetone.



$$G_S = \frac{V_{RO}}{V_{MI}}$$

Figure 5 : Return Loss.



$$R_L = \frac{V_S}{2\,V_M}$$

ELECTRICAL CHARACTERISTIC (refer to the test circuit, T_{amb} = 25 °C, f = 300 Hz to 3400 Hz, S1, S2 in "a" unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_L	Line Voltage	– 15 °C < T_{amb} < + 45 °C I_L = 80 mA I_L = 20 mA I_L = 10 mA	 9.5 4.8 3.6		 11.5 5.8 1.6	V	1
G_s	Sending Gain	f = 1 KHz I_L = 15 mA ; V_{MI} = 1.0 V_{RMS} I_L = 30 mA ; V_{MI} = 2.5 V_{RMS} I_L = 60 mA ; V_{MI} = 3.7 V_{RMS} I_L = 80 mA ; V_{MI} = 4.5 V_{RMS}	 48.5 47.4 42.7 42.0		 52.5 51.5 46.1 45.3	dB	2
G_s	Sending Gain Variation vs. Temp.	– 15 °C < T_{amb} < + 45 °C		0.8		dB	2
	Sending Gain Flatness	I_L = 10 to 80 mA f_{ref} = 1 KHz S1, S2 in (b)		- 0.5	+ 0.5	dB	2
	Sending Distortion	I_L = 10 to 15 mA ; V_{so} = 0.7 V_p			2	%	2
		I_L = 16 to 24 mA ; V_{so} = 1.3 V_p			2	%	
		I_L = 25 to 80 mA ; V_{so} = 1.7 V_p			10	%	
	Sending Noise	V_{MI} = 0 V I_L = 60 mA		– 73		dBmp	2
	Microphone Amplifier Impedance (pin 9-10)			95		Ω	1
	Max Sending Output (*)	I_L = 10 to 80 mA V_{MI} = 1 V			3	V_p	2
G_R	Receiving Gain	f = 1 KHz I_L = 15 mA ; V_{RI} = 0.8 V_{RMS} I_L = 30 mA ; V_{RI} = 1.0 V_{RMS} I_L = 60 mA ; V_{RI} = 1.8 V_{RMS} I_L = 80 mA ; V_{RI} = 10 V_{RMS}	 – 13.3 – 13.5 – 18 – 19		 – 9.6 – 10.5 – 14.9 – 16	dB	3
ΔG_R	Receiving Gain Variation vs. Temperature	– 15 °C < Tamb < + 45 °C		0.25		dB	3
	Receiving Gain Flatness	f_{ref} = 1 KHz I_L = 10 to 80 mA S1, S2 in (b)	– 0.5		+ 0.5	dB	3
	Receiving Distortion	I_L = 10 to 15 mA V_{RO} = 300 mV_p			2	%	3
		I_L = 15 to 80 mA V_{RO} = 500 mV_p			2		
	Receiving Amplifier Output Impedance (pin 1-4)			110		Ω	1
	Receiving Noise	V_{RI} = 0 V I_L = 60 mA psophometric		80		µV	3
	Max receiving Output Current	I_L = 80 mA V_{RI} = 10 V			3.6	mAp	3

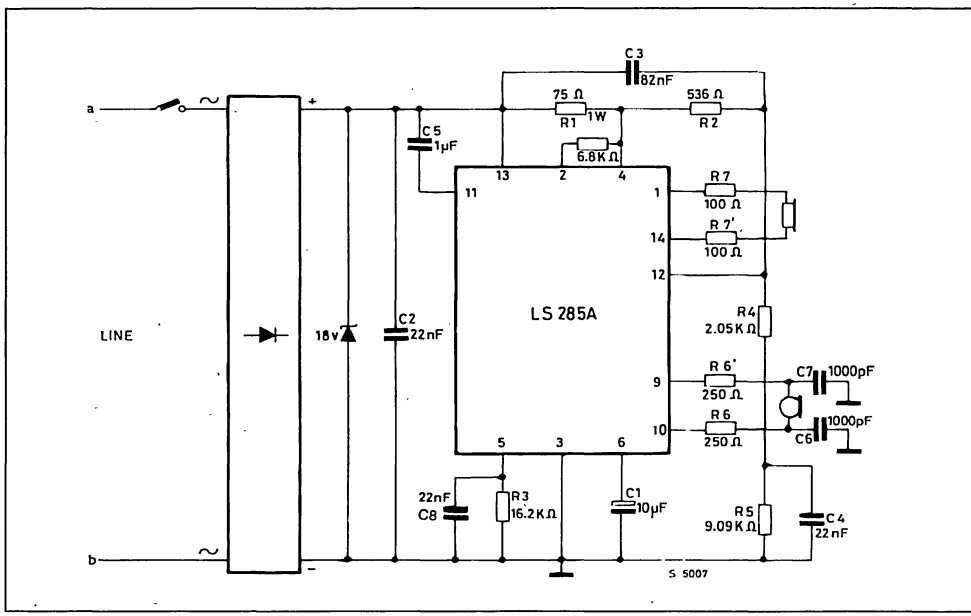
(*) This output is limited to allow for input overvoltages.

ELECTRICAL CHARACTERISTIC (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
	Sidetone	f = 1 KHz	I_L = 20 mA		7		dB	4
			I_L = 80 mA		0		dB	
	Return Loss	S3 in (a)			14		dB	5
		S3 in (b)			14		dB	

(*) This output is limited to allow for input overvoltages.

Figure 6 : Typical Application Circuit.



APPLICATION INFORMATION

The following table shows the recommended values for the typical application circuit of fig. 6. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R1	75 Ω	Bridge Resistors	The ratio R2/R1 fixes the amount of the signal delivered to the line. (see fig. 7)
R2	536 Ω		
R3	16.2 KΩ	Bias Resistor	Changing R3 value it is possible to shift the gain characteristics. The value can be chosen from 15 KΩ to 20 KΩ. The recommended value assures the maximum swing (see fig. 9).
R4	2.05 KΩ	Balance Network	In order to optimize the sidetone it is possible to change R4 and R5 values. In any case : $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ where Z_B = R4 + R5//C4.
R 5	9.09 KΩ		
R6 and R6'	250 Ω	Microphone Impedance Matching	R6 and R6' must be equal ; 250 Ω is a typical value for dynamic capsules. Furthermore, they determine a sending gain variation according to : $\Delta G_s = 20 \log \frac{Rx}{850\ \Omega}$ where Rx = R6 + R6' + R_{mike}. The trend of ΔG_s as a function of Rx value is shown in fig. 8.
R7 and R7'	100 Ω	Receive Impedance Matching	R7 and R7' must be equal ; 100 Ω is a typical value for dynamic capsules.
C1	10 µF	AC Loop Opening	Ensures a high regulator impedance for AC signals (≈ 20 KΩ). This capacitor should not be higher than 10 µF in order to have a short response time of the system.
C2	22 nF	Matching to a Capacitive Line	C2 changes with the characteristics of the transmission line.
C3	82 nF	High Frequency Roll-off	C3 determines the high frequency response of the circuit. it also acts as RF bypass.
C4	22 nF	Balance Network	See Note for R4 and R5.
C5	1 µF	DC decoupling for Receiving Input	
C6 and C7	1000 pF	RF Bypass	
C8	22 nF	Filter Capacitor	

Figure 7 : Receiving Gain Variation vs. R1 Value (with fixed R1/R2 ratio).

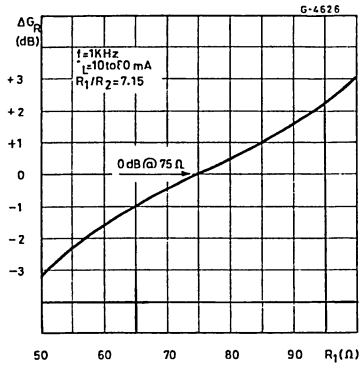


Figure 8 : Sending Gain Variation vs. Rx Value (see note for R6 and R6').

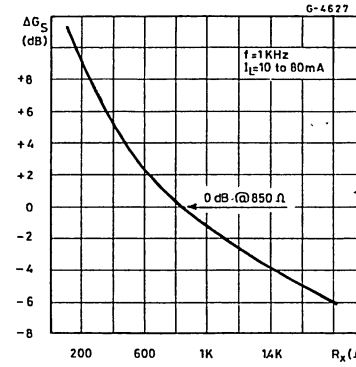
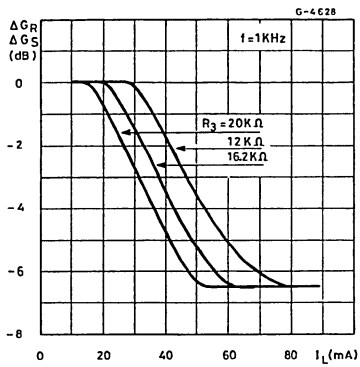


Figure 9 : Sending and receiving Gain Variation vs. Line Current.

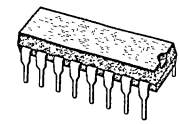


SGS-THOMSON MICROELECTRONICS

LS356

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

- PRESENTS THE PROPER DC PATH FOR THE LINE CURRENT
- HANDLES THE VOICE SIGNAL, PERFORMING THE 2/4 WIRES INTERFACE AND CHANGING THE GAIN ON BOTH SENDING AND RECEIVING AMPLIFIERS TO COMPENSATE FOR LINE ATTENUATION BY SENSING EITHER THE LINE CURRENT OR THE LINE VOLTAGE. **IN ADDITION, THE LS356 CAN ALSO WORK IN FIXED GAIN MODE**
- ACTS AS LINEAR INTERFACE FOR MF, SUPPLYING A STABILIZED VOLTAGE TO THE DIGITAL CHIP AND DELIVERING TO THE LINE THE MF TONES GENERATED BY THE M761



DIP16

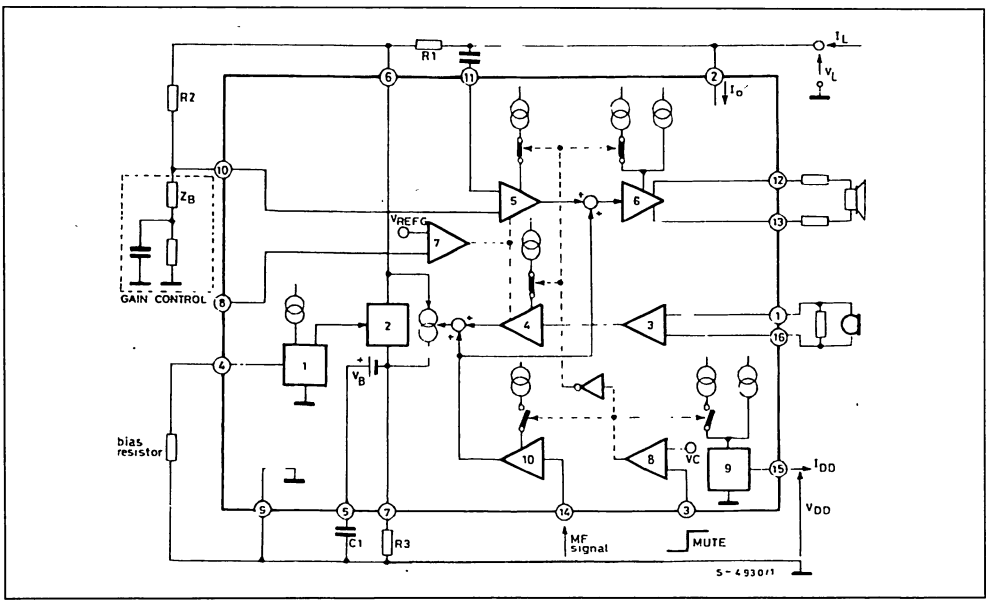
ORDER CODES : LS356B
LS356AB

DESCRIPTION

The LS356 is a monolithic circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typical dynamic capsules, but the device can also work with **piezoceramic ones**). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.

In addition to the speech operation, the LS356 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer).

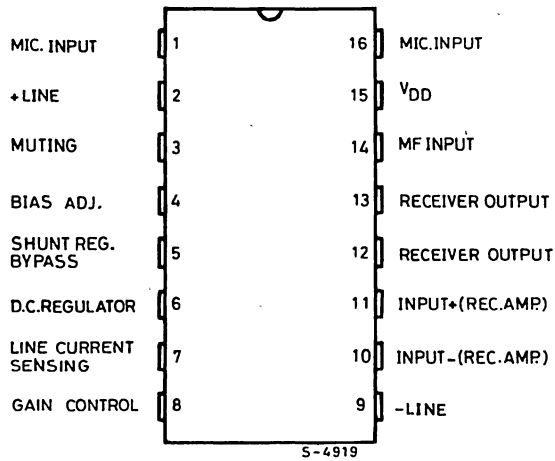
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse duration)	22	V
I_L	Forward Line Current	150	mA
I_L	Reverse Line Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{op}	Operating Temperature	– 45 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 65 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

TEST CIRCUITS

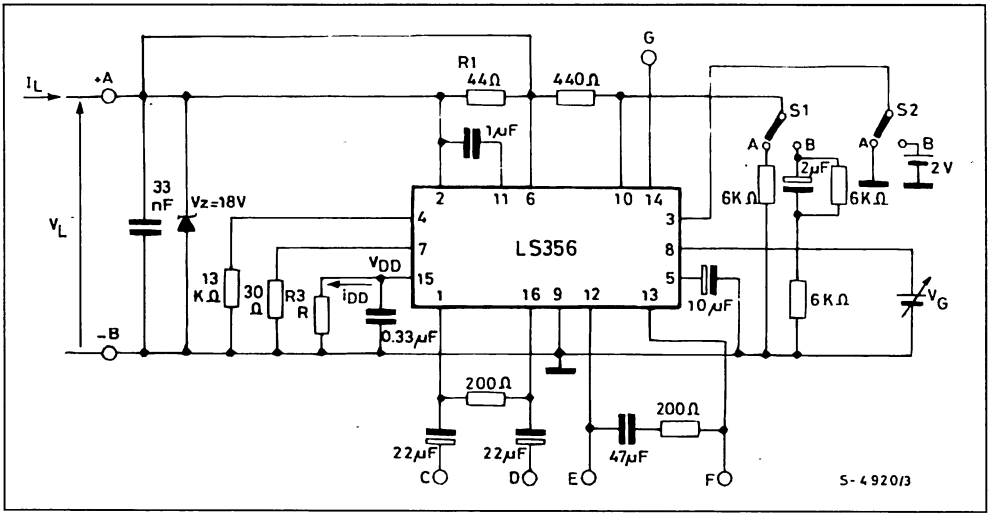


Figure 1.

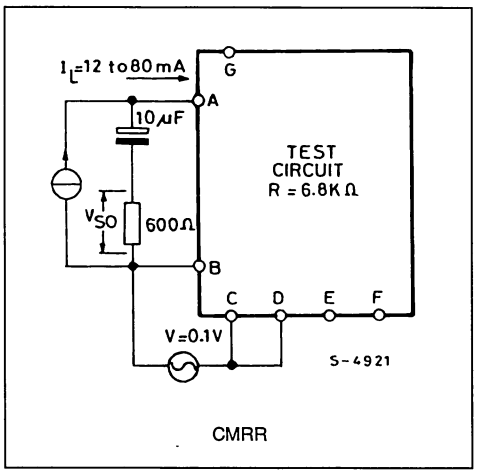


Figure 2.

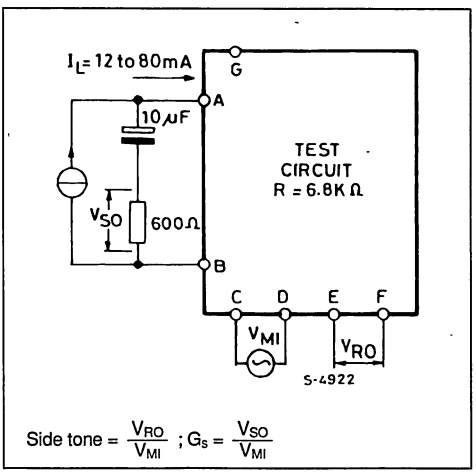
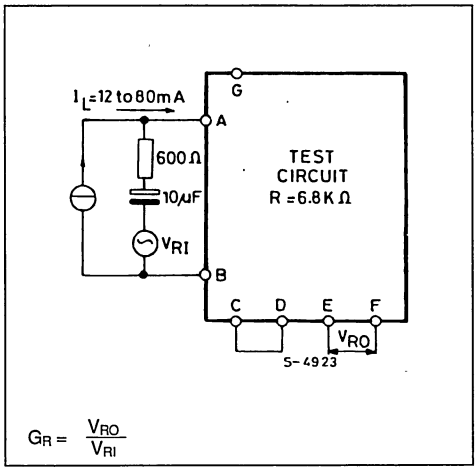
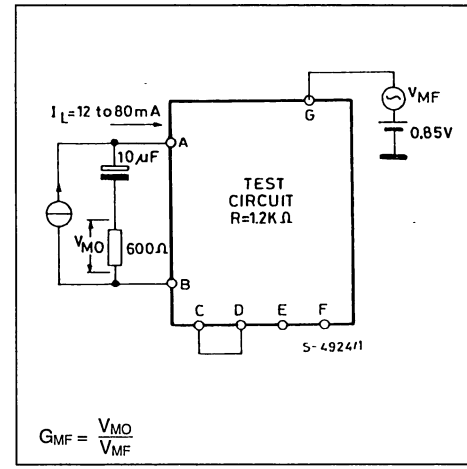


Figure 3.



$G_R = \frac{V_{RO}}{V_{RI}}$

Figure 4.



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_G= 1 to 2 V, I_L = 12 to 80 mA, S1 and S2 in (a), T_{amb} = – 25 to + 50 °C, f = 200 to 3400 Hz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION							
V_L	Line Voltage	T_{amb} = 25 °C I_L = 12 mA I_L = 20 mA I_L = 80 mA	3.65		4.5 5 10	V	–
CMR	Common Mode Rejection	f = 1 KHz	50			dB	1
G_S	Sending Gain for B Type	T_{amb} = 25 °C f = 1 KHz V_G = 2 V V_{MI} = 2 mV V_G = 1 V	44.5 48.5		46.5 50.5	dB	2
G_S	Sending Gain for AB Type	T_{amb} = 25 °C f = 1 KHz V_G = 2 V V_{MI} = 2 mV V_G = 1 V	44 48		47 51	dB	2
	Sending Gain Flatness (vs. frequency)	V_{MI} = 2 mV f_{ref} = 1 KHz	– 1		+ 1	dB	2
	(*) Sending Gain Flatness for B Type (vs. current)	V_G = 2 V I_{ref} = 50 mA	– 0.5		+ 0.5	dB	2
	(*) Sending Gain Flatness for AB Type (vs. current)	V_G = 2 V I_{ref} = 50 mA	– 1		+ 1	dB	2
	Sending Distortion for B Type	f = 1 KHz V_{so} = 775 mV I_L = 16 mA V_{so} = 900 mV			2 10	%	2
	Sending Distortion for AB Type	f = 1 KHz V_{so} = 775 mV I_L = 16 mA V_{so} = 900 mV			3 10	%	2
	Sending Noise	V_{MI} = 0 V V_G = 1 V		– 71		dBmp	2
	Microphone Input Impedance (pin 1-16)	V_{MI} = 2 mV	40			KΩ	–

* Fixed gain mode.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
	Sending Gain in MF Operation	V_{MI} = 2 mV S2 in (b)		– 30			dB	2
G_R	Receiving Gain for B Type	V_{RI} = 0.3 V f = 1 KHz T_{amb} = 25 °C	V_G = 2 V V_G = 1 V	– 5 – 0.5		– 3 + 1.5	dB	3
G_R	Receiving Gain for AB Type	V_{RI} = 0.3 V f = 1 KHz T_{amb} = 25 ° C	V_G = 2 V V_G = 1 V	– 5.5 – 1.0		– 2.5 + 2.0	dB	3
	Receiving Gain Flatness (vs. frequency)	V_{RI} = 0.3 V	f_{ref} = 1 KHz	– 1		+ 1	dB	3
	(*) Receiving Gain Flatness for B Type (vs. current)	V_G = 2 V	I_{ref} = 50 mA	– 0.5		+ 0.5	dB	3
	Receiving Gain Flatness for AB Type (vs. current)	V_G = 2 V	I_{ref} = 50 mA	– 1		+ 1	dB	3
	Receving Distortion for B Type	f = 1 KHz	V_{RO} = 400 mV V_{RO} = 450 mV			2 5	%	3
	Receiving Distortion for AB Type	f = 1 KHz	V_{RO} = 400 mA V_{RO} = 450 mA			3 5	%	3
	Receiving Noise	V_{RI} = 0 V			100		µV	3
	Receiver Output Impedance (pin 12-13)	V_{RO} = 50 mV			30		Ω	–
	Sidetone	f = 1 KHz S1 in (b)	T_{amb} = 25 °C			36	dB	2
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3 V	f = 1KHz	500	600	700	Ω	3
I_8	Input Current for Gain Control (pin 8)					– 10	µA	–

* Fixed gain mode.

ELECTRICAL CHARACTERISTICS (continued)

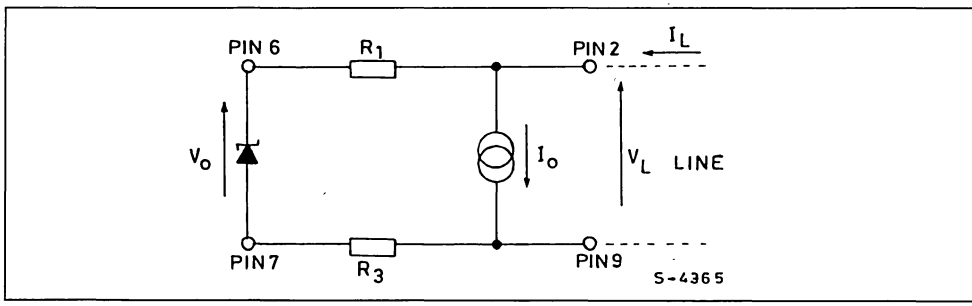
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF Supply Voltage (standby and operation)	S2 in (b)	2.4	2.5	2.7	V	–
I_{DD}	MF Supply Current Standby Operation	S2 in (b)	0.5 2			mA	–
	MF Amplifier Gain	$f_{MF\ in}$ = 1 KHz $V_{MF\ in}$ = 80 mV	15		17	dB	4
V_I	DC Input Voltage Level (pin 14)	$V_{MF\ in}$ = 80 mV		0.3 V_{DD}		V	–
R_I	Input Impedance (pin14)	$V_{MF\ in}$ = 80 mV	60			KΩ	–
d	Distortion for B Type	$V_{MF\ in}$ = 110 mV			2	%	4
d	Distortion for AB Type	$V_{MF\ in}$ = 110 mV			4	%	4
	Starting Delay Time Muting Threshold Voltage (pin 3)				5	ms	–
		Speech Operation			1	V	–
		MF Operation	1.6			V	–
	Muting Standby Current (pin 3)				– 10	µA	–
	Muting Operating Current (pin 3)	S2 in (b)			+ 10	µA	–

CIRCUIT DESCRIPTION

1. DC CHARACTERISTIC

The fig. 5 shows the DC equivalent circuit of the LS356.

Figure 5 : Equivalent DC Load to the Line.



A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit.

The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).

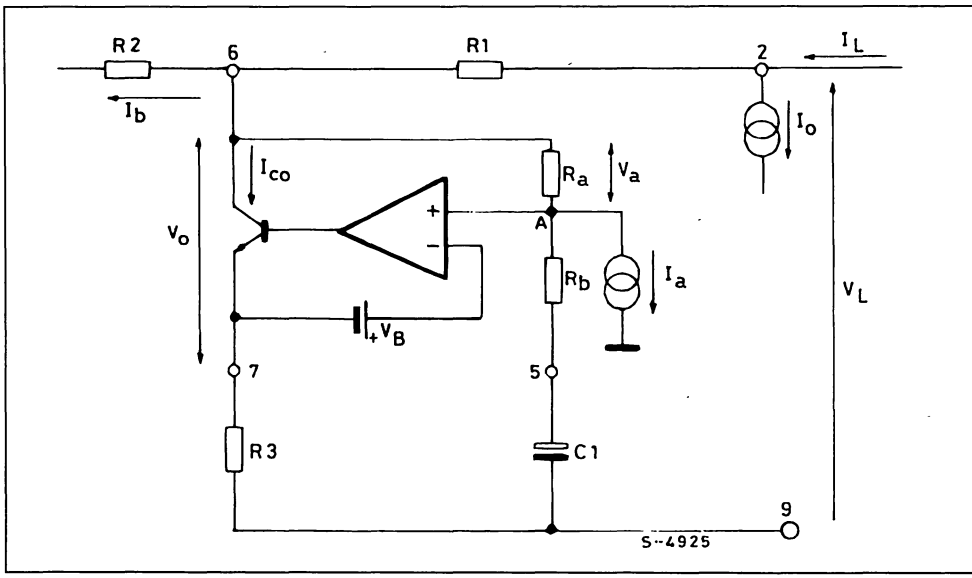
The minimum value of I_o is 7.5 mA.

The voltage V_o = 3.8 V of the shunt regulator is independent of the line current.

The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).

Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

Figure 6 : Circuit Configuration of the Shunt Regulator.



The difference $I_L - I_o$ flows through the shunt regulator being I_b negligible.

I_a is an internal constant current generator ; hence $V_o = V_B + I_a \cdot R_a = 3.8$ V.

The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.

It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_B = (I_L - I_o)\ R3 + V_B$).

2. TWO TO FOUR WIRES CONVERSION

The LS356 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 7).

For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R1}{R2}$.

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$) ; the main part is sent to the line via R1.

In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.

The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$.

From fig. 6 considering C1 as a short circuit for AC signal, any variation ΔV_6 generates a variation :

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R3\ (1 + \frac{R_a}{R_b})$$

The total impedance across the line connections (pin 11 and 9) is given by

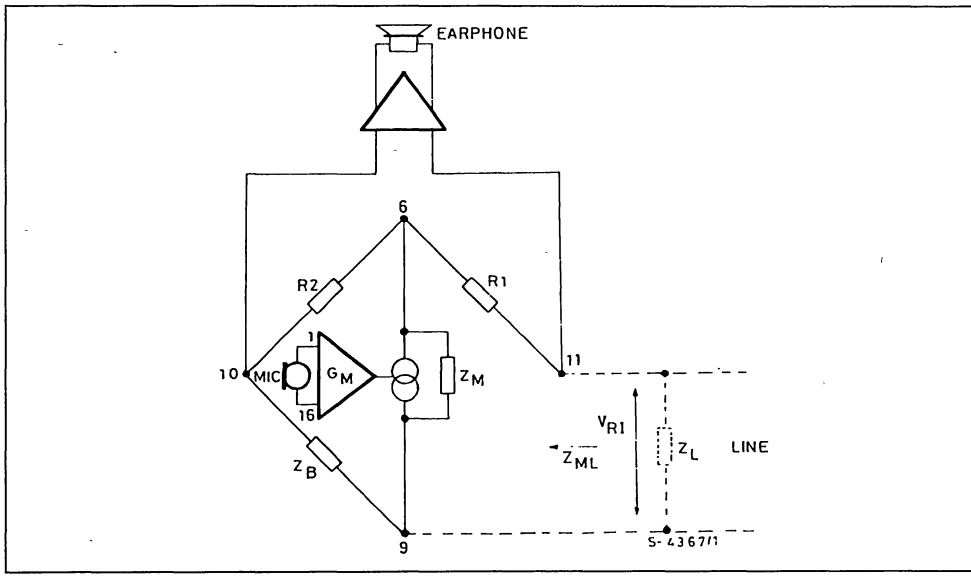
$$Z_{ML} = R1 + Z_M \,//\, (R2 + Z_B)$$

By choosing $Z_M >> R1$ and $Z_B >> Z_M$

$$Z_{ML} \cong Z_M = R3\ (1 + \frac{R_a}{R_b})$$

The received signal amplitude across pin 11 and 10 can be changed using different values of R1 (of course the relationship $Z_L/Z_B = R1/R2$ must be always valid).

Figure 7 : Two to Four Wires Conversion.



The received signal is related to R1 value according to the approximated relationship :

$$V_R = 2\ V_{RI}\ \frac{R1}{R1 + Z_M}$$

Note that by changing the value of R1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. AUTOMATIC GAIN CONTROL

The LS356 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.

This function is performed by the circuit of fig. 8.

The differential stage is progressively unbalanced by changing V_G in the range 1 to 2 V (V_{REFG} is an internal reference voltage, temperature compensated).

It changes the current I_G, and this current is used as a control quantity for the variable gain stages (amplifier (4) and (5) in the block diagram). The voltage V_G can be taken :

a) from the LS356 itself (both in variable and in fixed mode) and

b) from a resistive divider, directly at the end of the line.

a) In the first case, connecting V_G (pin 8) to the regulator bypass (pin 5) it is possible to obtain a gain charcteristic depending on the current. In fact (see fig. 6) :

$$V_5 = V_B + V_7 \cong V_B + (I_L - I_o)\ R3$$

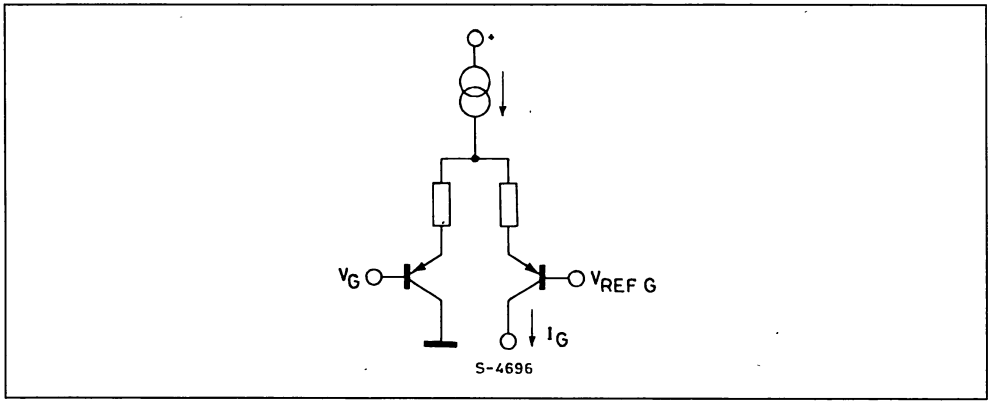
The starting point of the automatic level control is obtained at I_L = 25 mA when the drain current I_o = 7.5 mA.

Minimum gain is reached for a line current of about 52 mA for the same drain current I_o = 7.5 mA. When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.

It is also possible to change the starting point without changing I_o by connecting pin 8 to the centre of a resistive divider placed between pin 5 and ground (the total resistance seen by pin 5 must be at least 100 KΩ). In this case, the AGC range increases too ; for example using a division 1 : 1 (50 K/50 K) the AGC starting point shifts to about I_L = 40 mA, and the minimum gain is obtained at I_L = 95 mA. In addition to this operation mode, the V_G voltage can be maintained constant thus fixing the gain values (Rx, Tx) independently of the line conditions.

For this purpose the V_{DD} voltage, available for supplying the MF generator, can be used.

Figure 8.



b) When gains have to be related to the voltage at the line terminals of the telephone set, it is necessary to obtain V_G from a resistive divider directly connected to the end of the line.

This type of operation meets for instance the requirements of the French standard. (see the application circuit of fig. 12).

4. TRANSDUCERS INTERFACING

The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistor without affecting the sending gain. The receiving output stage (6) is particularly intended to drive dynamic capsules. (Low output impedance, 100 Ω max ; high current capability, 3 mAp).

When a piezoceramic capsule is used, it is useful to increase the receiving gain by increasing R1 value (see the relationship for V_R).

With very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. MULTIFREQUENCY INTERFACING

The LS356 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.

When no key of the keyboard is pressed the mute state is low and the LS356 feeds the M761 through pin 15 with low voltage and low current (standby operation of the M761). The oscillator of the M761 is not operating.

When one key is pressed, the M761 sends a "high state" mute condition to the LS356. A voltage comparator (8) of LS356 drives internal electronic switches : the voltage and the current delivered by the voltage supply (9) are increased to allow the operation of the oscillator.

This extra current is diverted by the receiving and sending section of the LS356 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.

A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber ; the MF amplifier (10) delivers the dial tones to the sending paths.

The application circuit shown in fig. 9 fulfils the EUROPE II standard (– 6, – 8 dBm). If the EUROPE I levels are required (– 9, – 11 dBm) an external divider must be used (fig. 10).

The mute function can be used also when a temporary inhibition of the output signal is requested.

APPLICATION INFORMATION

Figure 9 : Application Circuit with Multifrequency (EUROPE II STD).

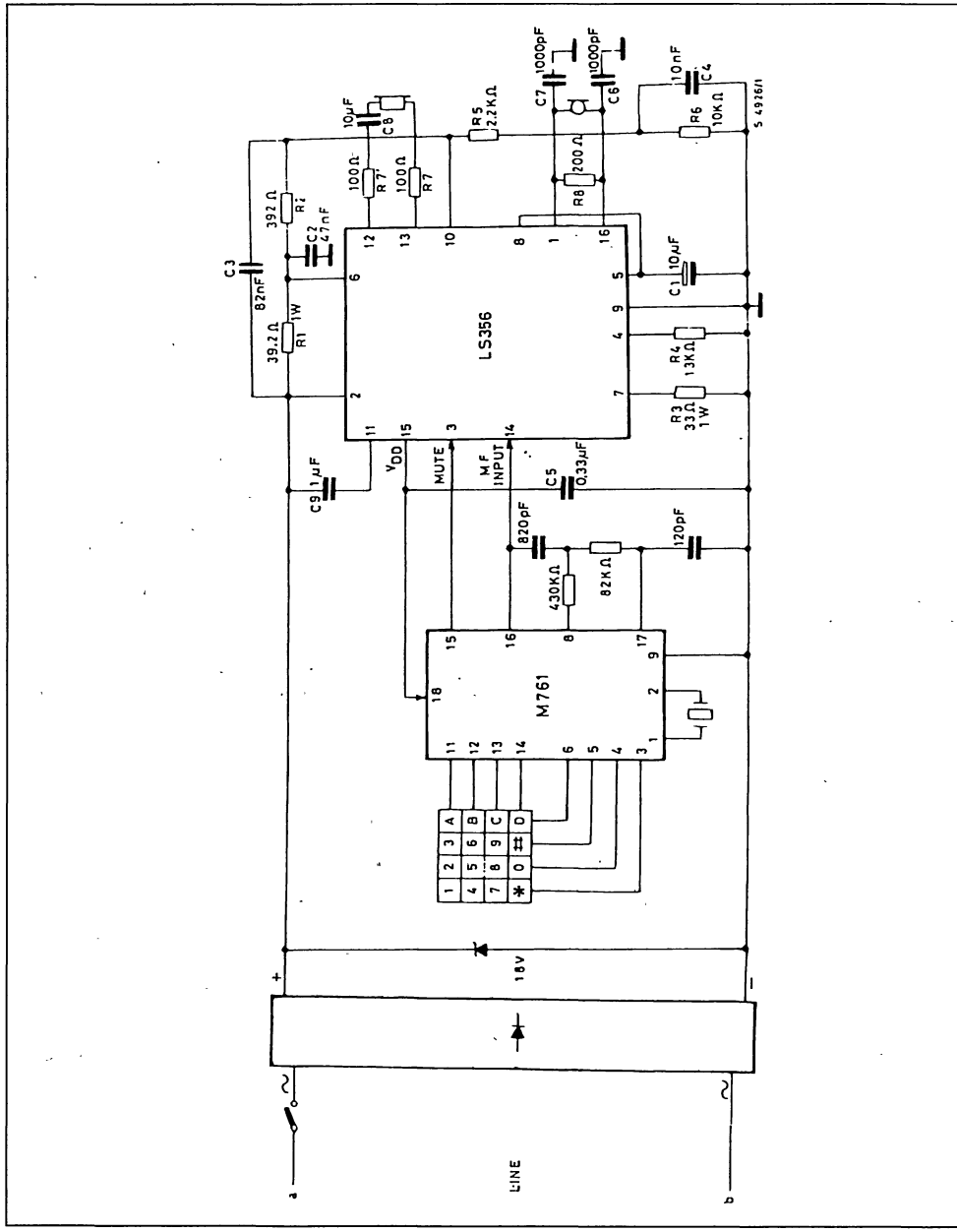


Figure 10 : Application Circuit with Multifrequency (EUROPE I).

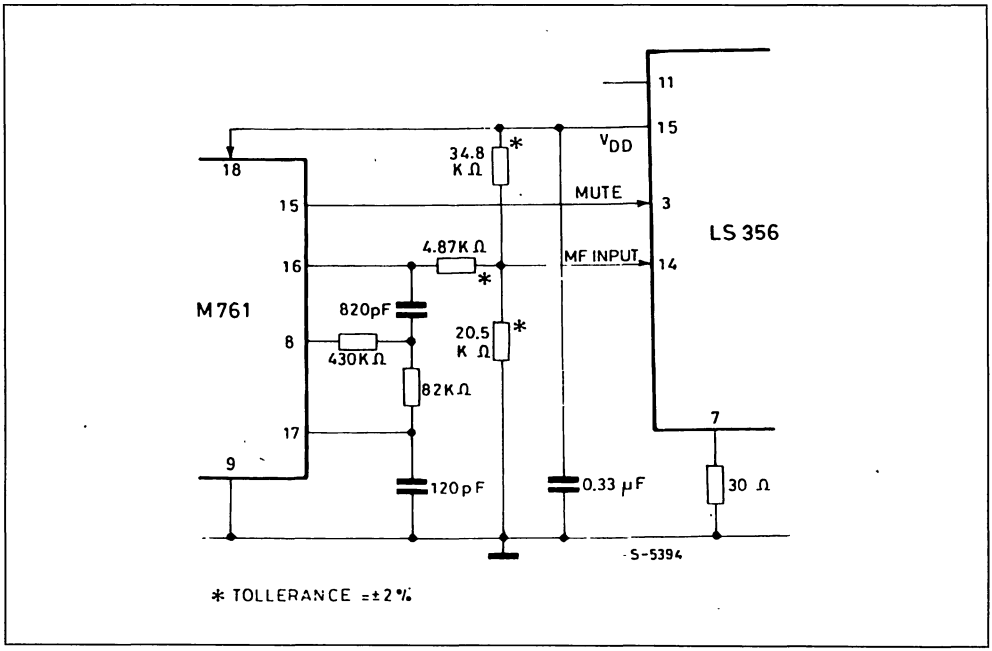


Figure 11 : Sending and Receiving Gain vs. Line Current (application circuit of fig. 13).

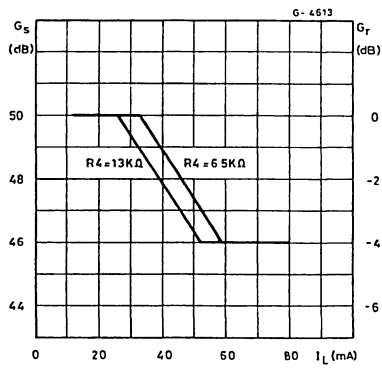


Figure 12 : Application Circuit without Multifrequency.

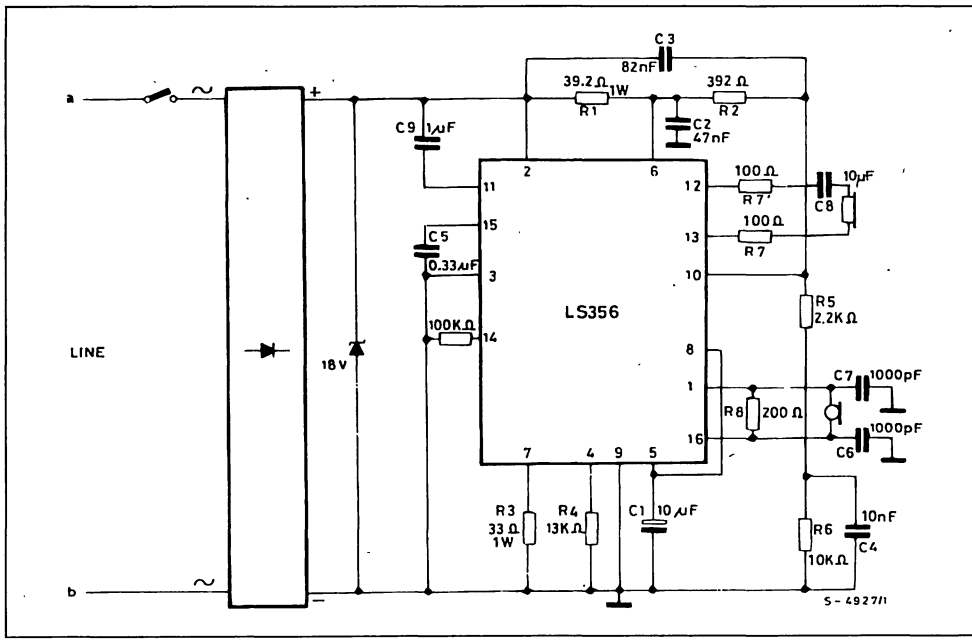


Figure 13 : Application Circuit with Gain Controlled by Line Voltage (French standard).

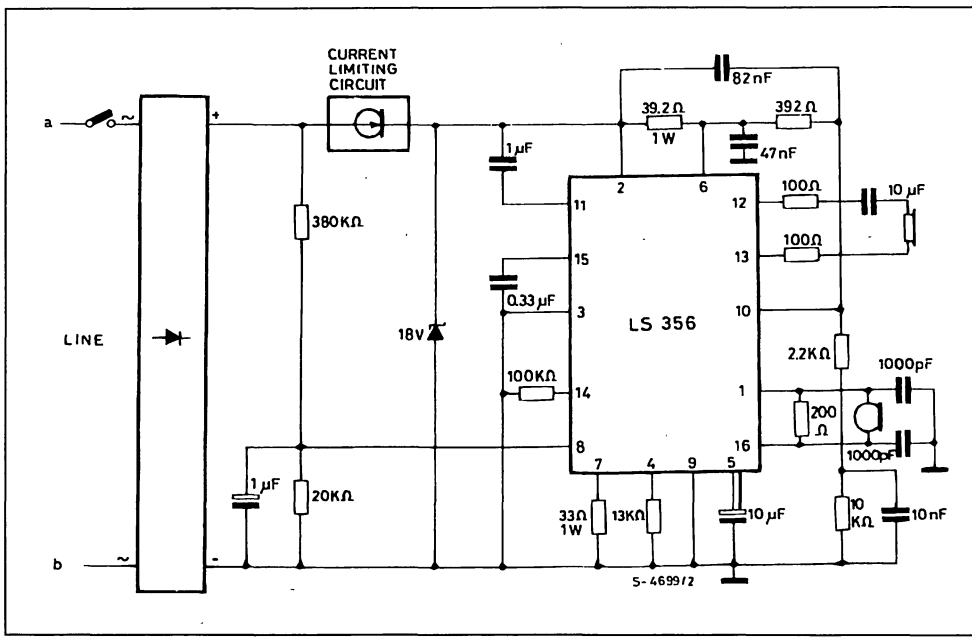
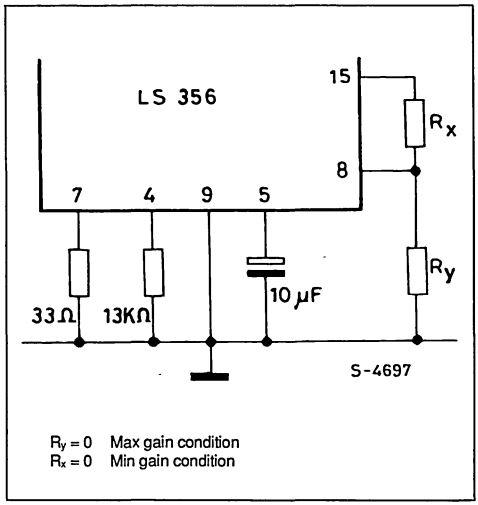
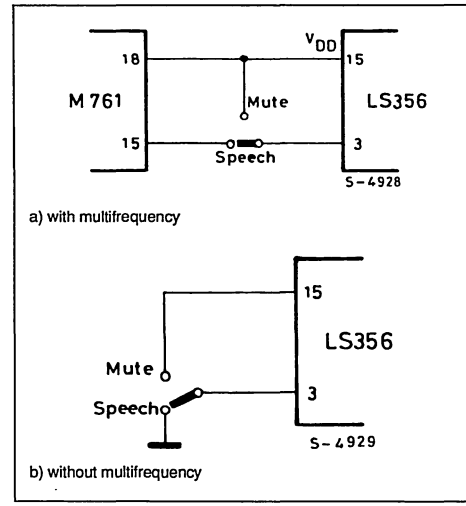


Figure 14 : Application Circuit with Fixed Gain Operation.



In addition to the above mentioned applications, different values for the external components can be used in order to satisfy different requirements.

Figure 15 : External Mute Function.



The following table (refer to the application circuit of fig. 9) can help the designers.

APPLICATION INFORMATION

Component	Value	Purpose	Note
R1	39.2 Ω	Bridge Resistors	R1 controls the receiving gain. When high current values are allowed, R1 must be able to dissipate up to 1 W. The Ratio R2/R1 fixes the amount of signal delivered to the line. R1 helps in fixing the DC characteristic (see R3 note).
R2	392 Ω		
R3	33 Ω	Line Current Sensing. Fixing DC Characteristic	The relationships involving R3 are : – $Z_{ML} = (20\ R3//ZB) + R1$ – $G_s = K \cdot \frac{Z_L//Z_{ML}}{R3}$ – $V_L = (I_L - I_O)\ (R3 + R1) + V_O$; $V_O = 3.8$ V. Without any problem it is possible to have a Z_{ML} ranging from 600 up to 900 Ω. As far as the power dissipation is concerned, see R1 note.
R4	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point.
R5	2.2 KΩ	Balance Network	It it possible to change R5 and R6 values in order to improve the matching to different lines ; in any case : $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ $Z_B = R5 + R6//X_{C4}$
R6	10 KΩ		

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
R7-R7'	100 Ω	Receiver Impedance Matching	R7 and R7' must be equal ; the suggested value is good for matching to dynamic capsule ; there is no problem in increasing and decreasing (down to 0 Ω) this value. A DC decoupling must be inserted when low resistance levels are used to stop the current due to the receiver output offset voltage (max 200 mV).
R8	200 Ω	Microphone Impedance Matching	The suggested value is typical for a dynamic microphone, but it is possible to choose R8 in a wide range.
C1	10 µF	Regulator AC Bypass	A value greater than 10 µF gives a system start time to high for low current line during MF operation ; a lower value gives an alteration of the AC line impedance at low frequency.
C2	47 nF	Matching to a Capacitive Line	C2 changes with the characteristics of the transmission line.
C3	82 nF	Receiving Gain Flatness	C3 depends on balancing and line impedance versus frequency.
C4	10 nF	Balance Network	See note for R5, R6.
C5	0.33 µF	DC Filtering	The C5 range is from 0.1 µF to 0.47 µF. The lowest value is ripple limited, the higher value is starting up time limited.
C6-C7	1000 pF	RF Bypass	
C8	10 µF	Receiving Output DC Decoupling	See note for R7, R7'.
C9	1 µF	Receiving Input DC Decoupling	

PROGRAMMABLE TELEPHONE SPEECH CIRCUIT

DESCRIPTION

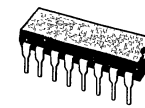
The LS588 is a monolithic integrated circuit in 16 lead dual in-line plastic package. Designed as a replacement for the hybrid circuit in telephone sets it performs all the functions previously carried out by this circuit.

With the LS588 it is possible to select the operating mode (fixed or variable gain). The device works with both piezoceramic and dynamic transducers and therefore its gain, both in sending and receiving paths, can be present by means of two external resistors. This feature can also be obtained in AGC operating mode, when the device automatically adjusts the Rx/Tx gains to compensate for the line attenuation by sensing the line current.

The LS588 can supply the decoupling FET when working with an electret microphone. Output impedance can be matched to the line independently of transducer impedance.

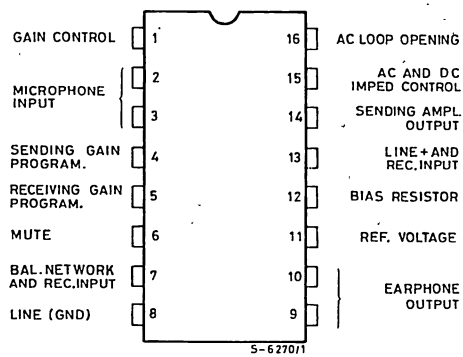
In addition, the LS588 can be set in power down state, where the device displays a strow decrease of the current consumption (about 8 mA), still maintains DC and AC impedances to the line (for parallel operation with a DTMF generator).

DIP16
(Plastic 0.25)



ORDER CODE : LS588N1

PIN CONNECTION (top view)



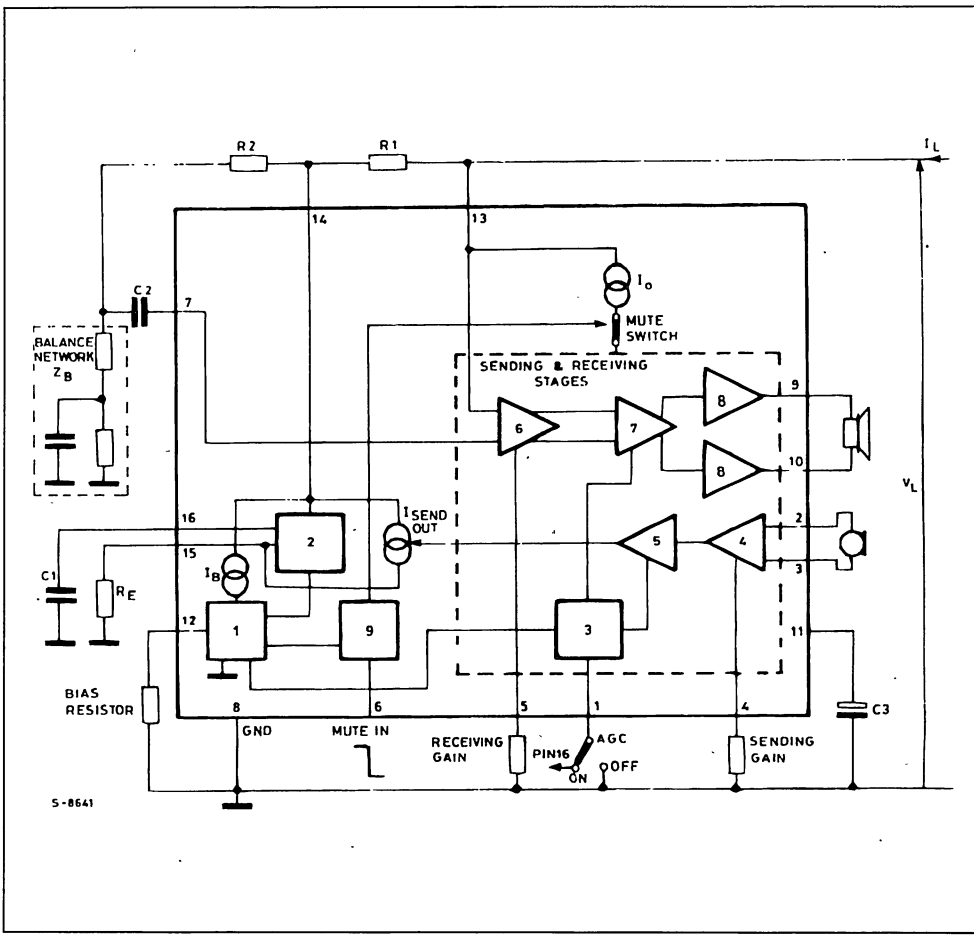
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Line Voltage (3 ms pulse duration)	22	V
I_L	Forward Line Current	150	mA
I_L	Reverse Line Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{op}	Operating Temperature	– 45 to + 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction–ambient	Max	80	°C/W

BLOCK DIAGRAM



TEST CIRCUITS

Figure 1.

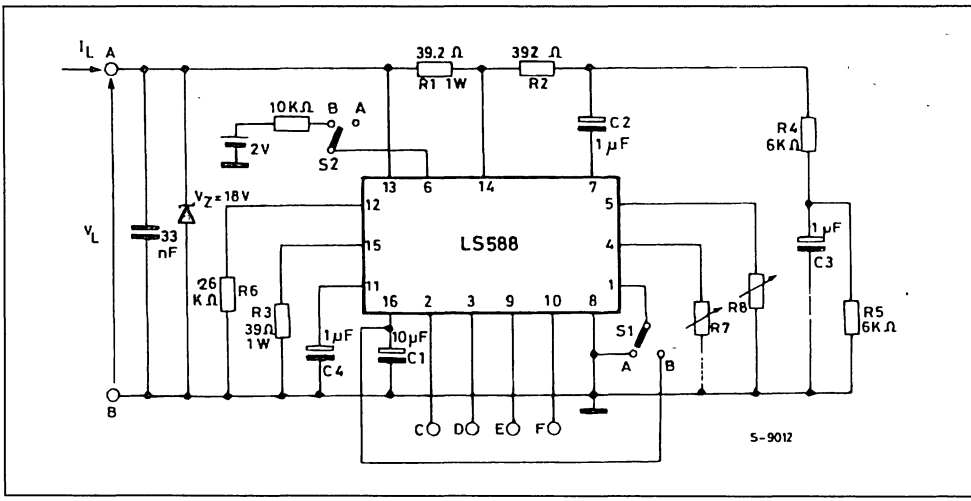


Figure 2.

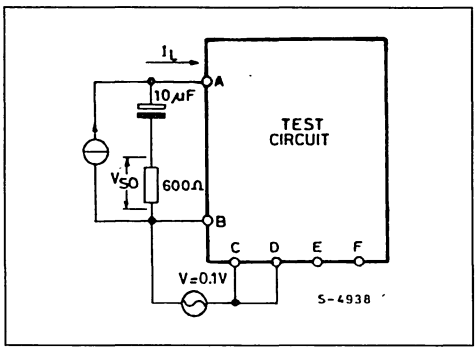


Figure 3.

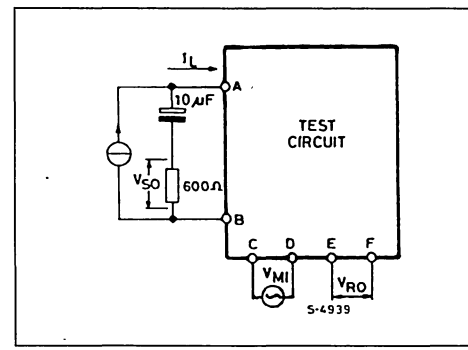
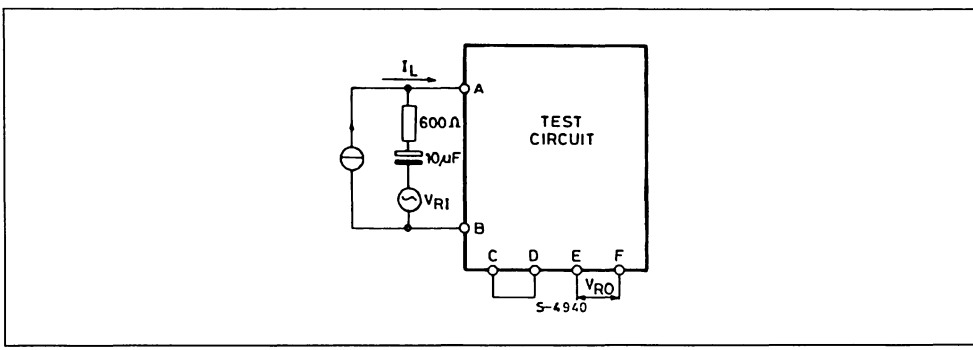


Figure 4.



ELECTRICAL CHARACTERISTICS (Refer to test circuits, T_{amb} = - 25 to + 50 °C, f = 200 to 3400 Hz, I_L = 15 to 100 mA, R_7 = 17.3 kΩ, R_8 = 17.1 kΩ, S1 in A, S2 in A, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
A.G.C. On								
V_L	Line Voltage	I_L = 15 mA I_L = 25 mA I_L = 50 mA I_L = 120 mA	T_{amb} = 25 °C	4.1	4.5 5.2 7	4.9 5.6 7.8 14	V	1
CMR	Common Mode Rejection	f = 1 kHz		50			dB	2
G_S	Sending Gain	I_L = 50 mA f = 1 kHz T_{amb} = 25 °C V_{MI} = 2 mV	R_7 = 17.3 kΩ	39.0		41.0	dB	3
			R_7 = 22.0 kΩ	43.8		46.2	dB	3
ΔG_S	Sending Gain Variation vs. Current	I_{ref} = 50 mA T_{amb} = 25 °C		− 0.5		+ 0.5	dB	3
	vs. Current (S1 in B)	I_{ref} = 50 mA T_{amb} = 25 °C	I_L = 25 mA	4.0		6	dB	3
			I_L = 100 mA	− 2.0		0	dB	
	vs. Frequency	f_{ref} = 1 kHz		− 0.5		0.5	dB	3
THD_S	Sending Distortion	I_L = 15 to 25 mA V_{so} = 450 mV	f = 1 kHz			2	%	3
		I_L = 25 to 100 mA V_{so} = 1.6 V	f = 1 kHz			5	%	
N_S	Sending Noise	V_{MI} = 0 mV			− 74		dBm	3
Z_{MI}	Microphone Impedance	V_{MI} = 3 mV		11	15		kΩ	3
G_R	Receiving Gain	I_L = 50 mA f = 1 kHz T_{amb} = 25 °C V_{RI} = 570 mV	R_8 = 17.1 kΩ	2.3		4.7	dB	4
			R_8 = 14.7 kΩ	− 0.1		1.9	dB	4
ΔG_R	Receiving Gain Variation vs. Current	I_{ref} = 50 mA T_{amb} = 25 °C		− 0.5		+ 0.5	dB	4
	vs. Current (S1 in B)	I_{ref} = 50 mA T_{amb} = 25 °C	I_L = 25 mA	4.0		6	dB	4
			IL = 100 mA	− 2.0		0		
	vs. Frequency	f_{ref} = 1 kHz		− 0.5		0.5		
THD_R	Receiving Distortion	V_{RI} = 570 mV				2	%	4
		V_{RI} = 775 mV				5		
N_R	Receiving Noise	V_{RI} = 0 mV			150		µV	4
Z_{RO}	Receiving Output Impedance	V_{RO} = 50 mV			50		Ω	4
	Sidetone	f = 1 kHz			15		dB	3
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3 V	f = 1 kHz	650		850	Ω	4
	Max Receiving Output (click suppression)	V_{RI} = 2 V		3.9	4.4		V_{PP}	4
V_{SM}	Microphone Supply	R_{load} = 2.2 kΩ		1.9		2.2	V	1

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
MUTE OPERATION							
	Mute Threshold Voltage (pin 6)	Speech Condition			0.8	V	–
		Mute Condition	1.5			V	–
	Muting Operation Curr. (pin 6) (S2 in B)		50			µA	–
	Line Dynamic in Mute Condition (S2 in B) THD = 2 %	I_L = 3.5 mA I_L = 4 mA	600 850			mV	–
	Line Voltage in Mute Condition (S2 in B)	I_L = 3.5 mA I_L = 4 mA		3.6 4.2		V	–

CIRCUIT DESCRIPTION

1. DC CHARACTERISTIC

In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristic V_L, I_L.
The DC characteristics of the LS588 is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3 (see the block diagram). The equivalent circuit is shown in fig. 5.
A fixed amount, I_o, of the total available current, I_L, is drained to allow the circuit to operate correctly. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 12.
The recommended minimum value of I_o is 7.5 mA with R pin 12 = 26 KΩ.
The voltage $V_o \cong 3.8$ V of the shunt regulator is independent of the line current.
The shunt regulator (block 2) is controlled by a temperature compensated voltage reference (block 1). Fig. 6 shows a more detailed circuit configuration of the shunt regulator.
The difference I_L-I_o flows through the shunt regulator since I_b is negligible.
I_a is an internal constant current generator ; hence $V_o = V_B + Ia \cdot R_a = 3.8$ V.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series with a battery.
It is important to note that the DC voltage at pin 16 is proportional to the line current $V_{16} = V_{15} + V_B = (I_L - I_o) R_3 + V_B$.

2. TWO TO FOUR WIRES CONVERSION

The LS588 performs the two wire (line) to four wire (microphone, earphone) conversion by means of a Wheatstone bridge configuration thus obtaining the proper decoupling between sending and receiving signals (see fig. 7).

For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$

The AC signal from the microphone is sent to one diagonal of the bridge (pin 8 and 14). A small percentage of the signal power is lost on Z_B (since $Z_B >> Z_L$) ; the main part is sent to the line via R_1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 7 and 13). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator which also acts as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{(14\text{-}8)}}{\Delta I_{(14\text{-}8)}}$

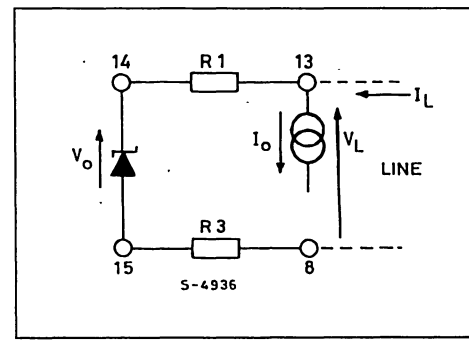
From fig. 6, considering C_1 as a short circuit to the AC signal, any variation in V_{14} generates a variation as follows :

$$V_{15} = V_A = V_{14} \frac{R_b}{R_a + R_b}$$

the corresponding current change is :

$$\Delta I = \frac{\Delta V_{15}}{R_3}$$

Figure 5 : Equivalent DC Load to the Line.



therefore

$$Z_M = \frac{\Delta V_{14}}{\Delta I} = R_3 (1 + \frac{R_a}{R_b})$$

The total impedance across the line connections (pin 13 and 8) is given by

$$Z_{ML} = R_1 + Z_M // (R_2 + Z_B)$$

By choosing Z_M R_1 and Z_B Z_M

$$Z_{ML} \cong Z_M = R_3 (1 + \frac{R_a}{R_b})$$

The amplitude of the signal received across pins 13 and 7 can be changed using different values of R_1.

(Of course the relationship $\frac{Z_I}{Z_B} = \frac{R_1}{R_2}$ must always be valid.

The received signal is related to the value of R_1 according to the approximated relationship :

$$V_R = V_{RI} 2 \quad \frac{R_1}{R_1 + Z_M}$$

Note that if the value of R_1 is changed the transmission signal current is not changed, since the microphone amplifier is a transconductance amplifier.

3. INPUT AND OUTPUT AMPLIFIERS

The microphone amplifier (4) has a differential input stage with high impedance (min 11 K) so allowing a good matching to the microphone by means of an external resistor without affecting the sending gain.

The receiving output stage (8) is intended to drive both piezoceramic and dynamic capsules. It has low output impedance, a maximum voltage swing greater than 2 V_p and a peak current of 2 mA.

With very low impedance transducers, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

4. GAIN CONTROL

It is possible to set the LS588 gain characteristics by means of one pin (pin 1).

When the pin 1 is grounded, the gains of the sending and receiving amplifiers do not depend on the line current (AGC off). When the pin 1 is connected to pin 15 the LS588 automatically changes the gain to compensate for line attenuation (AGC on).

4.1. AGC OFF :In this conditions, as already mentioned, both the sending and the receiving gain are fixed. Their values are determined, independently for the two paths, by the two external resistors R_7 (for T_x, between pin 4 and ground) and R_8 (for R_x, between pin 5 and ground), in a wide range (see fig. 8 and 9).

4.2. AGC ON : Starting from any couple of gain values, fixed by the appropriate values of R_7 and R_8, the LS588 can automatically change the sending and receiving gains depending on the line current. The line current is sensed across R_3 (see fig. 7) and transferred to pin 16 by the regulator.

$$V_{16} = V_B + V_{15} = V_B + (I_L - I_o) \cdot R_3$$

Following comparison with an internal reference (block 1) the voltage at pin 1 is used to modify (block 3) the gain of the amplifiers (5) and (7) on both the sending and receiving paths.

The starting point of the automatic level control is obtained at I_L = 25 mA when the drain current I_o = 7.5 mA.

The external resistors R_7 and R_8 fix the maximum value for the gains.

Minimum gain is reached for a line current of about 100 mA when the same drain current I_o of 7.5 mA is used.

5. DC SHUNT REGULATOR

The LS588 has built into the chip a DC shunt regulator intended to supply (pin 11) the coupling FET when an electret microphone is used. It delivers 1 mAp current with a voltage of 2 Volts (typ) regardless of the line current.

6. MUTE CONDITION AND MUTIFREQUENCY INTERFACING

- A logical control (mute) at pin 6 allows operation in parallel with a proper DTMF generator connectable to the line.
- When pin 6 is set high (more than 1.8 Volt) the mute logic circuit (block 9) switches off both sending and receiving stages (mute switch) and reduces (1) the bias current, to sabe about 10 mA, available for the paralleled DTMF generator.

In this condition the LS588 still shows to the line the specified AC impedance (650 to 850 Ω) not provided by the DTMF generator which acts as a current generator.

7. ANTICLIPPING APPLICATION

It is possible to avoid distortion of the sending signal limiting the sending gain with an external control at pin 4 (gain programming).

The maximum level to the line will be :

$$V_S = \frac{0.6\ V}{\sqrt{2}} \times \frac{R_{AC1} + R_{AC2}}{R_{AC2}}$$

The following table can be helpful to the designer when choosing different values for the external components, it refers to the typical application circuit of fig. 10.

Figure 6 : Circuit Configuration of the Shunt Regulator.

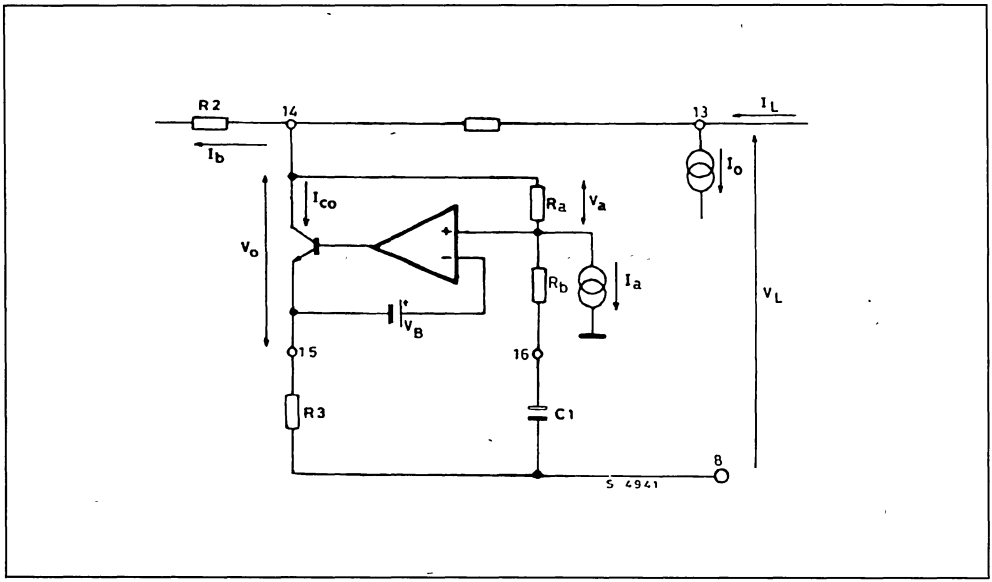


Figure 7 : Two to four Wires Conversion.

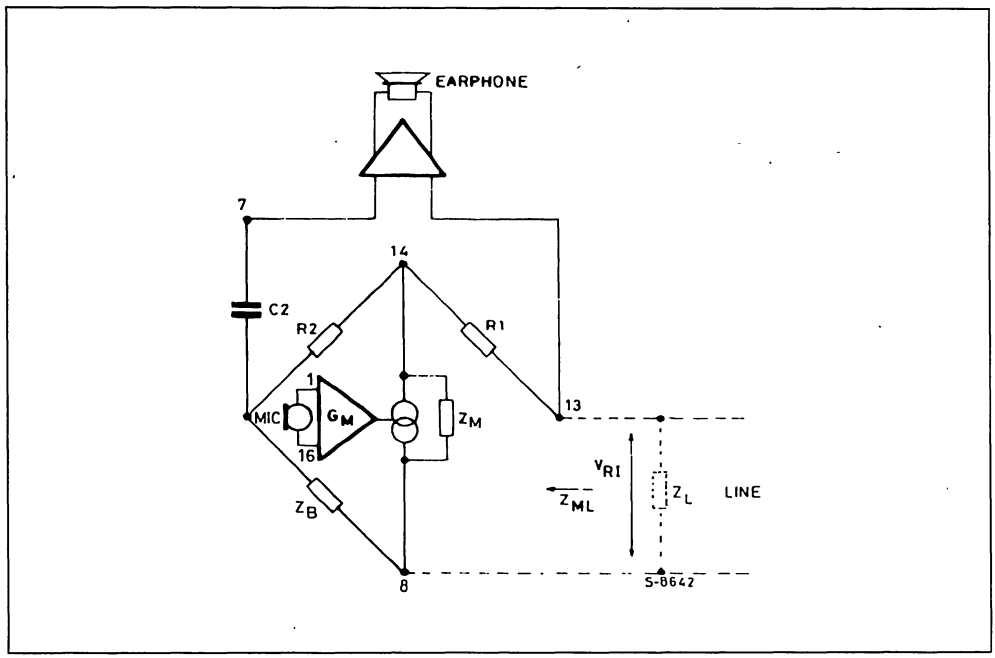


Figure 8 : Sending Gain vs. R_7 Value (AGC OFF).

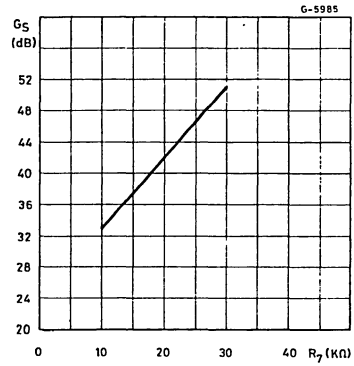


Figure 9 : Receiving Gain vs. R_8 Value (AGC OFF).

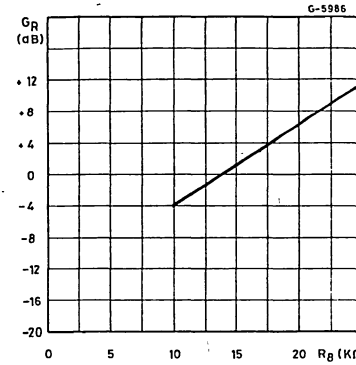


Figure 10 : Typical Application Circuit (piezoceramic transducers).

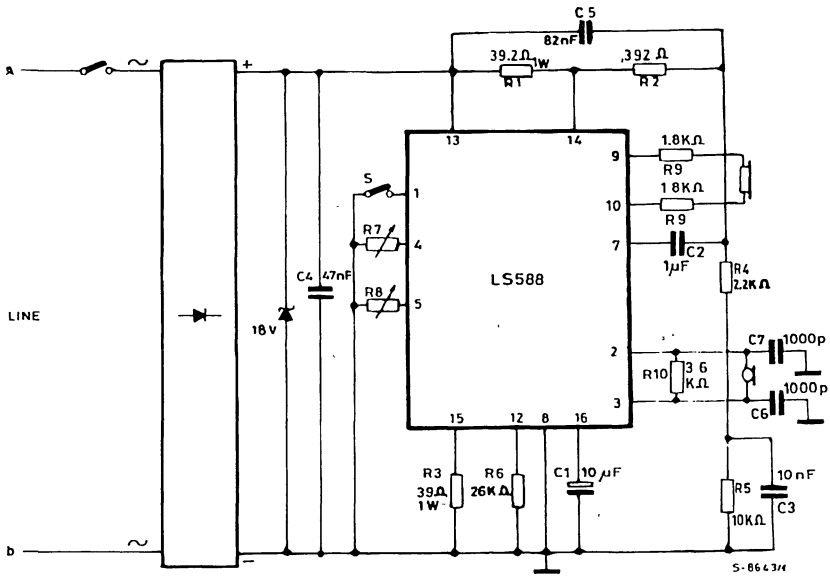
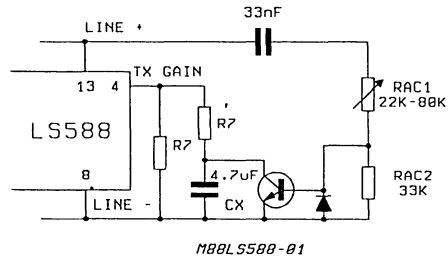
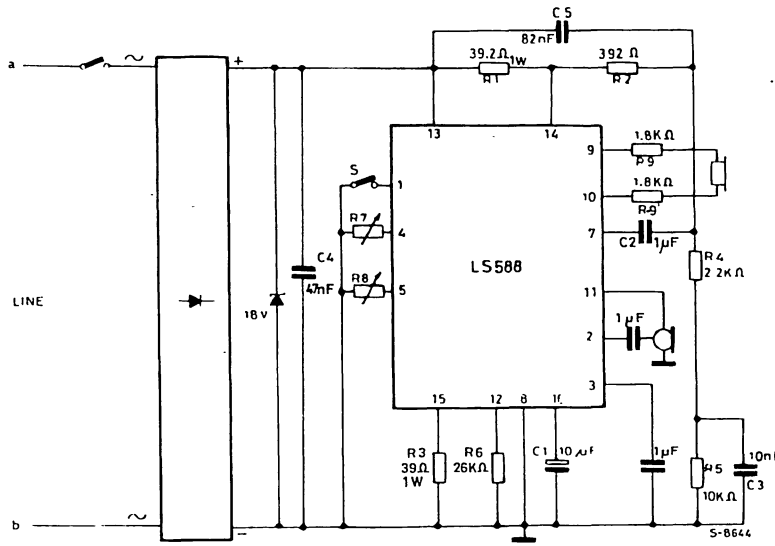


Figure 11 : Anticlipping Application.



APPLICATION INFORMATION

Figure 12 : Application Circuit with Electret Microphone.



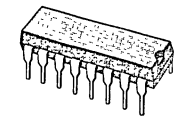
SGS-THOMSON MICROELECTRONICS

LS656

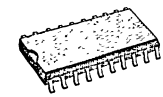
TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

- PRESENTS THE PROPER DC PATH FOR THE LINE CURRENT, PARTICULAR CARE BEING PAID TO HAVE LOW VOLTAGE DROP
- HANDLES THE VOICE SIGNAL, PERFORMING THE 2/4 WIRES INTERFACE AND CHANGING THE GAIN ON BOTH SENDING AND RECEIVING AMPLIFIERS TO COMPENSATE FOR LINE ATTENUATION BY SENSING EITHER THE LINE CURRENT OR THE LINE VOLTAGE. IN ADDITION, THE LS656 CAN ALSO WORK IN FIXED GAIN MODE
- ACTS AS LINEAR INTERFACE FOR MF, SUPPLYING A STABILIZED VOLTAGE TO THE DIGITAL CHIP AND DELIVERING TO THE LINE THE MF TONES GENERATED BY THE M761

DIP16
(Plastic 0.4)



SO-20L

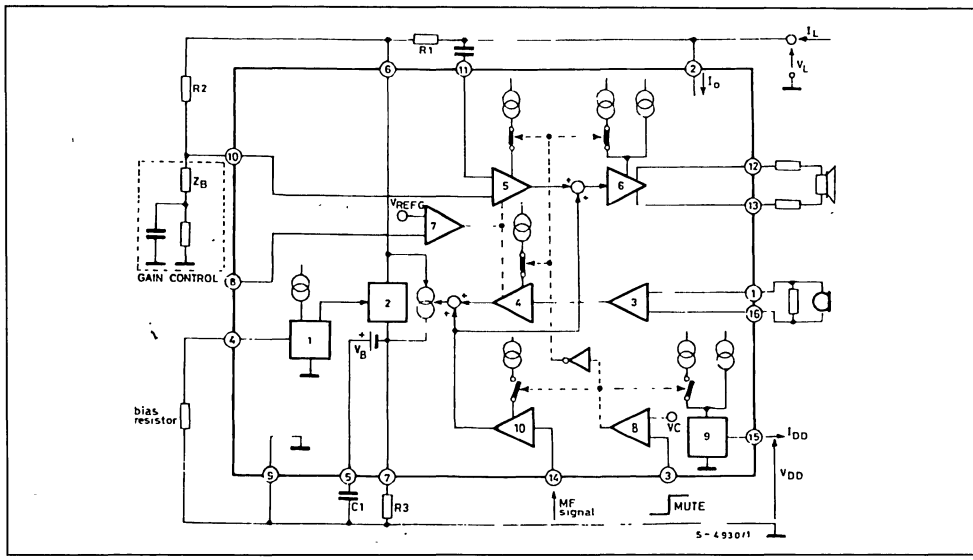


ORDER CODES : LS656B - LS656AB (DIP16)
LS656D1 - LS656AD1 (SO-20)

DESCRIPTION

The LS656 is a monolithic integrated circuit in 16-lead plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically dynamic capsules). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.
In addition to the speech operation, the LS656 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer).

BLOCK DIAGRAM (DIP16)



ABSOLUTE MAXIMUM RATINGS

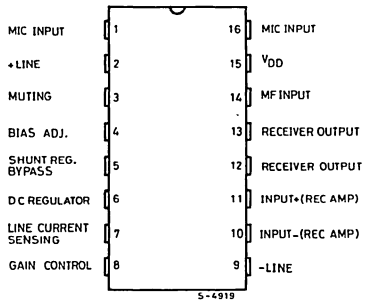
Symbol	Parameter	Test Conditions	Unit
V_L	Line Voltage (3 ms pulse duration)	22	V
I_L	Forward Line Current	150	mA
I_L	Reverse Line Current	– 150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1	W
T_{op}	Operating Temperature	– 45 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 65 to 150	°C

THERMAL DATA

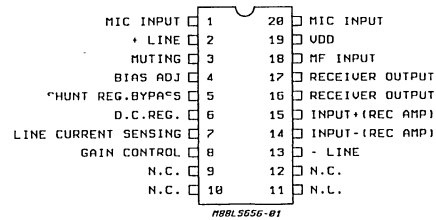
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

PIN CONNECTIONS (top view)

DIP-16



SO-20L



TEST CIRCUITS

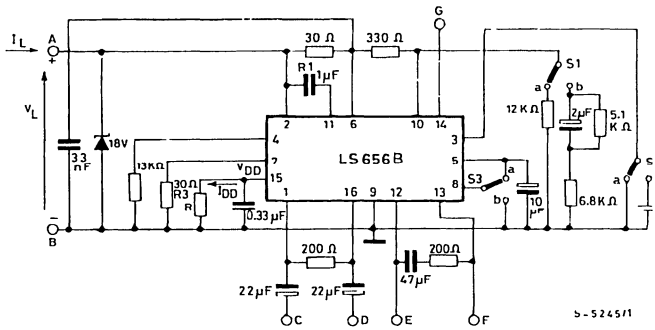
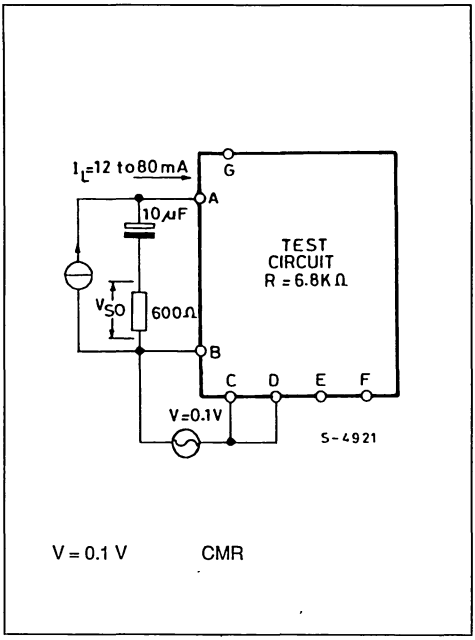
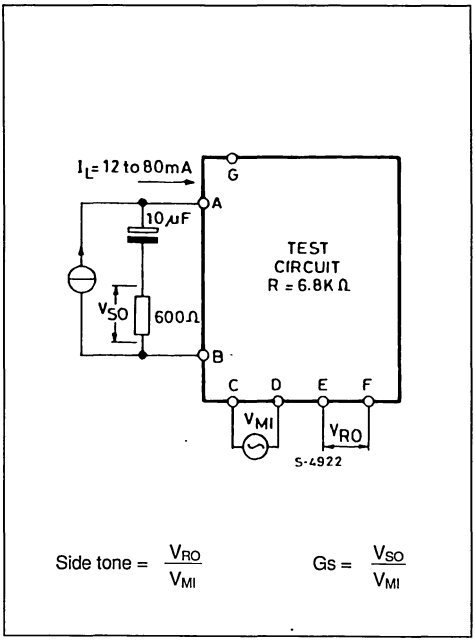


Figure 1.



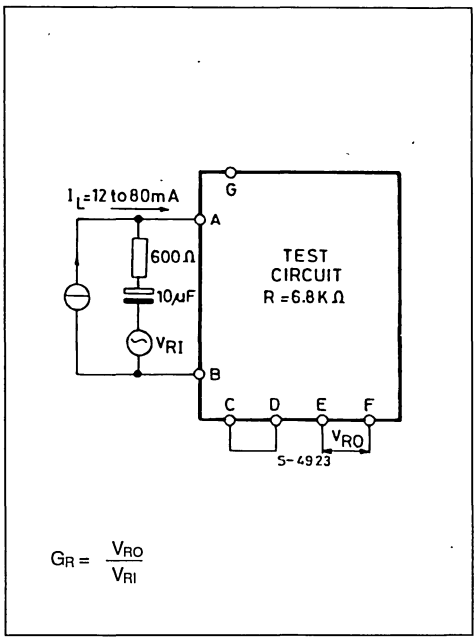
V = 0.1 V CMR

Figure 2.



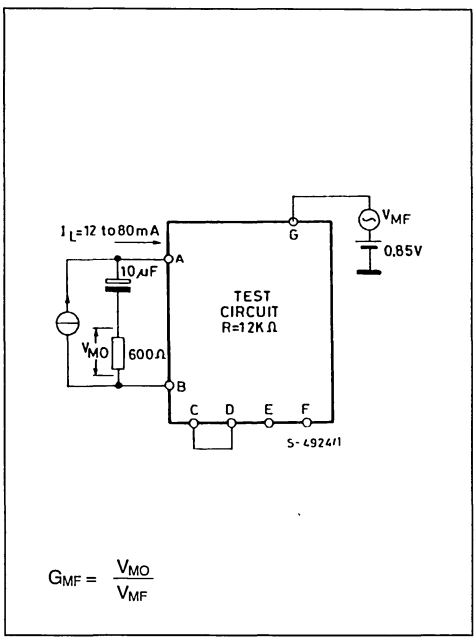
Side tone = $\frac{V_{RO}}{V_{MI}}$ Gs = $\frac{V_{SO}}{V_{MI}}$

Figure 3.



$G_R = \frac{V_{RO}}{V_{RI}}$

Figure 4.



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_G = 1 to 2 V, I_L = 12 to 80 mA, S1, S2 and S3 in (a), T_{amb} = – 25 to + 50 °C, f = 200 to 3400 Hz, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION								
V_L	Line Voltage	T_{amb} = 25 °C	I_L = 12 mA I_L = 30 mA I_L = 60 mA	3.4		3.9 5.1 6.9	V	–
CMR	Common Mode Rejection	f = 1 kHz		50			dB	1
G_S	Sending Gain for B and D1 Types	T_{amb} = 25 °C f = 1 kHz V_{MI} = 2 mV	I_L = 25 mA I_L = 50 mA	48.5 44.5		50.5 46.5	dB	2
G_S	Sending Gain for AB and AD1 Types	T_{amb} = 25 °C f = 1 kHz V_{MI} = 2 mV	I_L = 25 mA I_L = 50 mA	48 44		51 47	dB	2
	Sending Gain Flatness for B and D1 Types (vs. freq.)	V_{MI} = 2 mV	f_{ref} = 1 kHz	– 0.5		+ 0.5	dB	2
	Sending Gain Flatness for AB and AD1 Types (vs. freq.)	V_{MI} = 2 mV	f_{ref} = 1 kHz	– 1		+ 1	dB	2
(*)	Sending Gain Flatness for B and D1 Types (vs. current)	V_{MI} = 3 mV S3 in (b)	I_{ref} = 50 mA	– 0.5		+ 0.5	dB	2
	Sending Gain Flatness for AB and AD1 Types (vs. current)	V_{MI} = 3 mV S3 in (b)	I_{ref} = 50 mA	– 1		+ 1	dB	2
	Sending Distortion for B and D1 Types	f = 1 kHz I_L = 16 mA	V_{so} = 775 mV V_{so} = 900 mV			2 10	% %	2
	Sending Distortion for AB and AD1 Types	f = 1 kHz I_L = 16 mA	V_{so} = 775 mV V_{so} = 900 mV			3 10	% %	2
	Sending Noise	V_{MI} = 0 V ; V_G = 1 V			– 71		dBmp	2
	Microphone Input Impedance (pin 1-16)	V_{MI} = 2 mV		40			kΩ	–
	Sending Gain in MF Operation	V_{MI} = 2 mV S2 in (b)		– 30			dB	2

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
G_R	Receiving for B and D1 Types	V_{RI} = 0.3 V f = 1 kHz T_{amb} = 25 °C	I_L = 25 mA I_L = 50 mA	– 5.5 – 10.5		– 3.5 – 8.5	dB	3
GR	Receiving for AB and AD1 Types	V_{RI} = 0.3 V f = 1 kHz T_{amb} = 25 °C	I_L = 25 mA I_L = 50 mA	– 6 – 11		– 3 – 8	dB	3
	Receiving Gain Flatness for B and D1 Types (vs. freq.)	V_{RI} = 0.3 V	f_{ref} = 1 kHz	– 0.5		+ 0.5	dB	3
	Receiving Gain Flatness for AB and AD1 Types (vs. freq.)	V_{RI} = 0.3 V	f_{ref} = 1 kHz	– 1		+ 1	dB	3
	Receiving Gain Flatness for B and D1 Types (vs. current)	V_{RI} = 0.3 V S3 in (b)	I_{ref} = 50 mA	– 0.5		+ 0.5	dB	3
	Receiving Gain Flatness for AB and AD1 Types (vs. current)	V_{RI} = 0.3 V S3 in (b)	I_{ref} = 50 mA	– 1		+ 1	dB	3
	Receiving Distortion for B and D1 Types	f = 1 kHz I_L = 15 mA	V_{RO} = 400 mV V_{RO} = 450 mV			2 10	% %	3
	Receiving Distortion for AB and AD1 Types	f = 1 kHz I_L = 15 mA	V_{RO} = 400 mV V_{RO} = 450 mV			3 10	% %	3
	Receiving Noise	V_{RI} = 0 V ; V_G = 1 V			150		µV	3
	Receiving Ouptut Impedance (pin 12-13)	V_{RO} = 50 mV			30		Ω	–
	Sidetone	f = 1 kHz T_{amb} = 25 °C S1 in (b)				36	dB	2
Z_{ML}	Line Matching Impedance	V_{RI} = 0.3 V	f = 1 kHz	500	600	700	Ω	3
I_8	Input Current for Gain Control (pin 8)					– 10	µA	–

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF Supply Voltage Stand by and Operation	S2 in (b)	2.4	2.5	2.7	V	–
I_{DD}	MF Supply Current Stand by Operation	S2 in (b)	0.5 2			mA mA	– –
	MF Amplifier Gain	$f_{MF\,in}$ = 1 kHz $V_{MF\,in}$ = 80 mV	15		17	dB	4
V_I	DC Input Voltage Level (pin 14)	$V_{MF\,in}$ = 80 mV		V_{DD} x 0.3		V	–
R_I	Input Impedance (pin 14)	$V_{MF\,in}$ = 80 mV	60			kΩ	–
d	Distortion for B and D1 Types	$V_{MF\,in}$ = 150 mVp I_L > 17 mA			2	%	4
d	Distortion for AB and AD1 Types	$V_{MF\,in}$ = 150 mVp I_L > 17 mA			4	%	4
	Starting Delay Time				5	ms	–
	Muting Threshold Voltage (pin3)	Speech Operation			1	V	–
		MF Operation	1.6			V	–
	Muting Stand by Current (pin 3))				– 10	µA	–
	Muting Operating Current (pin 3)	S2 in (b)			+ 10	µA	–

CIRCUIT DESCRIPTION

1. DC CHARACTERISTIC

The fig. 5 shows the DC equivalent circuit of the LS656.

A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).

The minimum value of I_o is 7.5 mA.

The voltage V_o = 37 V of the shunt regulator is independent of the line current.

The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).

Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

The difference I_L-I_o flows through the shunt regulator being I_b negligible. I_a is an internal constant current generator ; hence $V_o = V_B + I_a \cdot R_a = 3.7$ V.

The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.

Figure 5 : Equivalent DC Load to the Line.

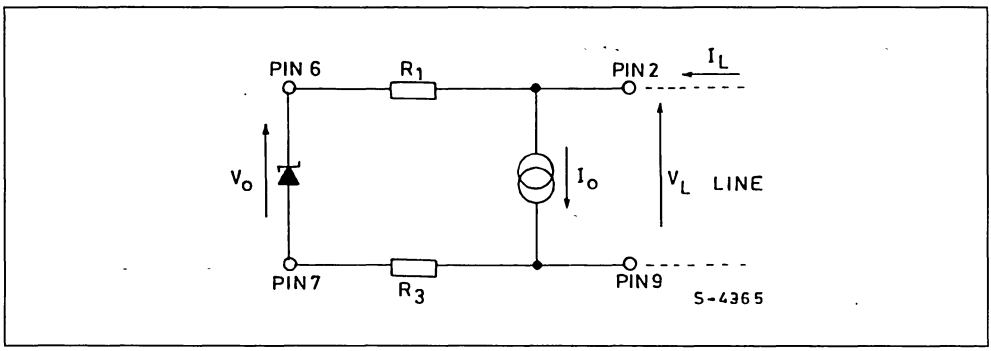
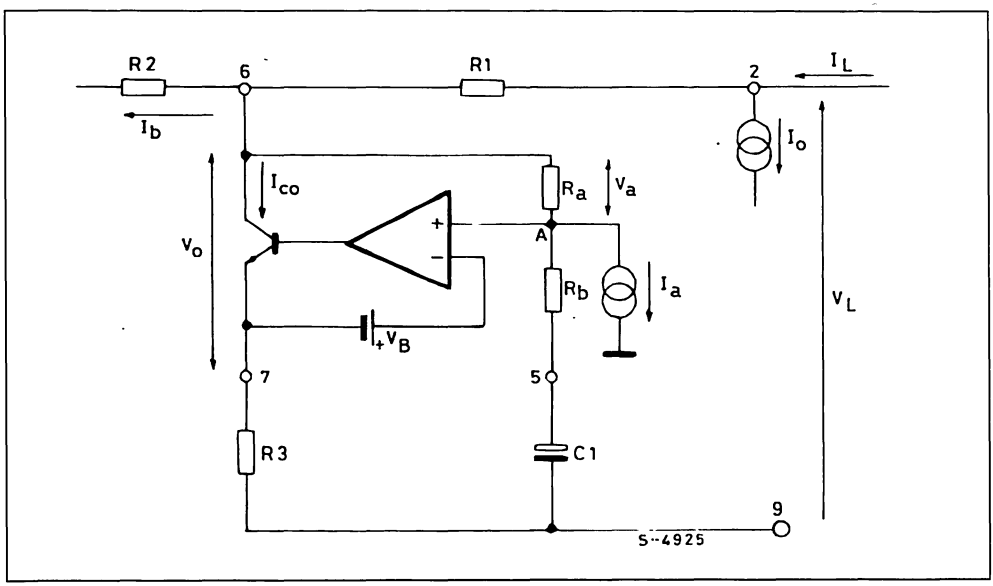


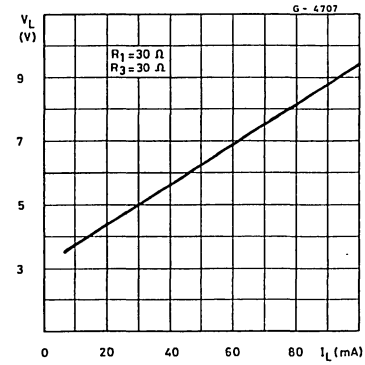
Figure 6 : Circuit Configuration of the Shunt Regulator.



It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_B = (I_L - I_o)\ R3 + V_B$).

The DC characteristic of the LS656 is shown in fig. 7.

Figure 7 : DC Characteristic.



2. TWO TO FOUR WIRES CONVERSION

The LS656 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 8).

For a perfect balancing of the bridge $\frac{ZL}{ZB} = \frac{R1}{R2}$

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$) ; the main part is sent to the line via R1. In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.

The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$

From fig. 6 considering C1 as a short circuit for AC signal, any variation ΔV_6 generates a variation :

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current is

$$\Delta I = \frac{\Delta V_7}{R3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R3\ (1 + \frac{R_a}{R_b})$$

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R1 + Z_M//(R2 + Z_B)$$

By choosing $Z_M \geq R1$ and $Z_B \geq Z_M$

$$Z_{ML} \cong Z_M = R3\ (1 + \frac{R_a}{R_b})$$

The received signal amplitude across pin 11 and 10 can be changed using different value of R1 (of course the relationship $Z_L/Z_B = R1/R2$ must be always valid).

The received signal is related to R1 value according to the approximated relationship :

$$V_R = 2\ V_{RI}\ \frac{R1}{R1 + Z_M}$$

Note that by changing the value of R1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. AUTOMATIC GAIN CONTROL

The LS656 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.

This function is performed by the circuit of fig. 9.

The differential stage is progressively unbalanced by changing V_G in the range 1 to 2 V (V_{REFG} is an internal reference voltage, temperature compensated).

It changes the current I_G, and this current is used as a control quantity for the variable gain stages (amplifier (4) and (5) in the block diagram). The voltage V_G can be taken :

a) from the LS656 itself (both in variable and in fixed mode) and.

b) from a resistive divider, directly at the end of the line.

a) In the first case, connecting V_G (pin 8) to the regulator bypass (pin 5) it is possible to obtain a gain characteristic depending on the current.
In fact (see fig. 6)

$$V_5 = V_B + V_7 \cong V_B = (I_L - I_o)\ R3$$

The starting point of the automatic level control is obtained at I_L = 25 mA when the drain current I_o = 7.5 mA.

Minimum gain is reached for a line current of about 50 mA for the same drain current I_o = 7.5 mA. When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.

It is also possible to change the starting point without changing I_o by connecting pin 8 to the centre of a resistive divider placed between pin 5 and ground (the total resistance seen by pin 5 must be at least 100 KΩ). In this case, the AGC range increases too; for example using a division 1 : 1 (50 K/50 K) the AGC starting point shifts to about I_L = 40 mA, and the minimum gain is obtained at I_L = 95 mA. In addition to this operation mode, the V_G voltage can be maintained constant thus fixing the gain value (Rx, Tx) independently of the line conditions.

For this purpose the V_{DD} voltage, available for supplying the MF generator, can be used.

b) When gains have to be related to the voltage at the line terminals of the telephone set, it is necessary to obtain V_G from a resistive divider directly connected to the end of the line.

This type of operation meets the requirements of the French standard. (See the application circuit of fig. 13).

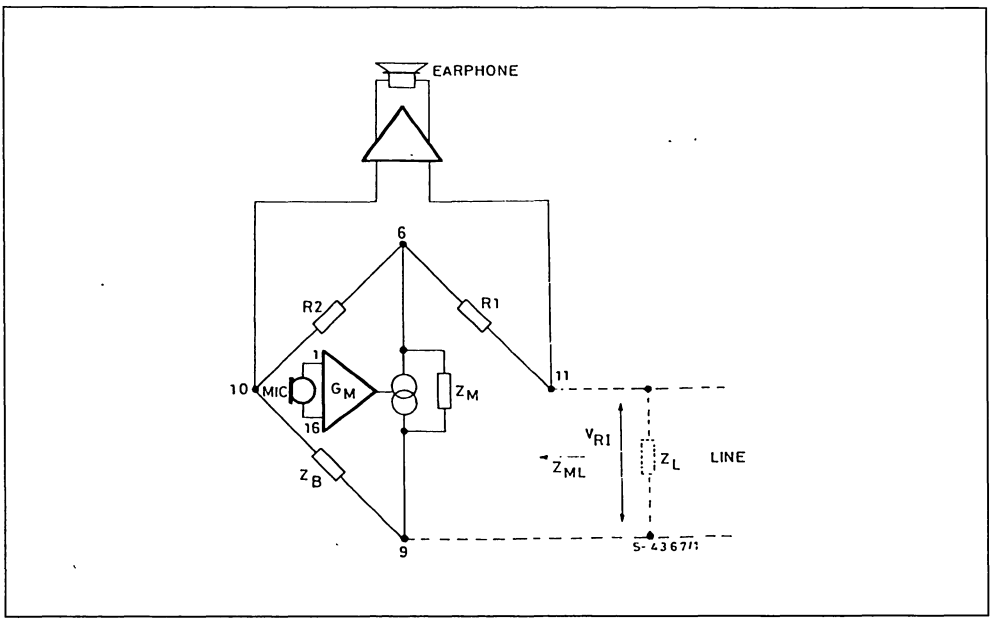
4. TRANSDUCER INTERFACING

The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistor without affecting the sending gain. The receiving output stage (6) is particularly intended to drive dynamic capsules. (Low output impedance (100 Ω max) ; high current capability 3 mAp).

When a piezoceramic capsule is used, it is useful to increase the receiving gain by increasing R1 value (see the relationship for V_R).

Whit very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

Figure 8 : Two to Four Wires Conversion.



5. MULTIFREQUENCY INTERFACING

The LS656 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.

When no key of the keyboard is pressed the mute state is low and the LS656 feeds the M761 through pin 15 with low voltage and low current (standby operation of the M761). The oscillator of the M761 is not operating.

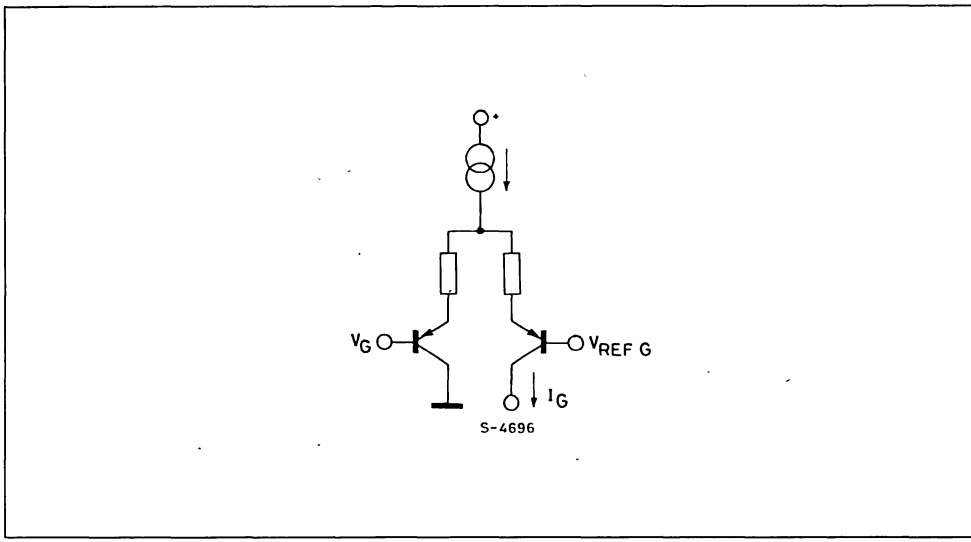
When one key is pressed, the M761 sends a "high state" mute condition to the LS656. A voltage comparator (8) of LS656 drives internal electronic switches ; the voltage and the current delivered by the voltage supply (9) are increased to allow the operation of the oscillator.

This extra current is diverted by the receiving and sending section of the LS656 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.

A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber ; the MF amplifier (10) delivers the dial tones to the sending paths.

The mute function can be used also when a temporary inhibition of the output signal is requested. The application circuit shown in fig. 10 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm) an external divider must be used (see fig. 11).

Figure 9.



APPLICATION INFORMATION

Figure 10 : Application Circuit with Multifrequency (Europe II STD).

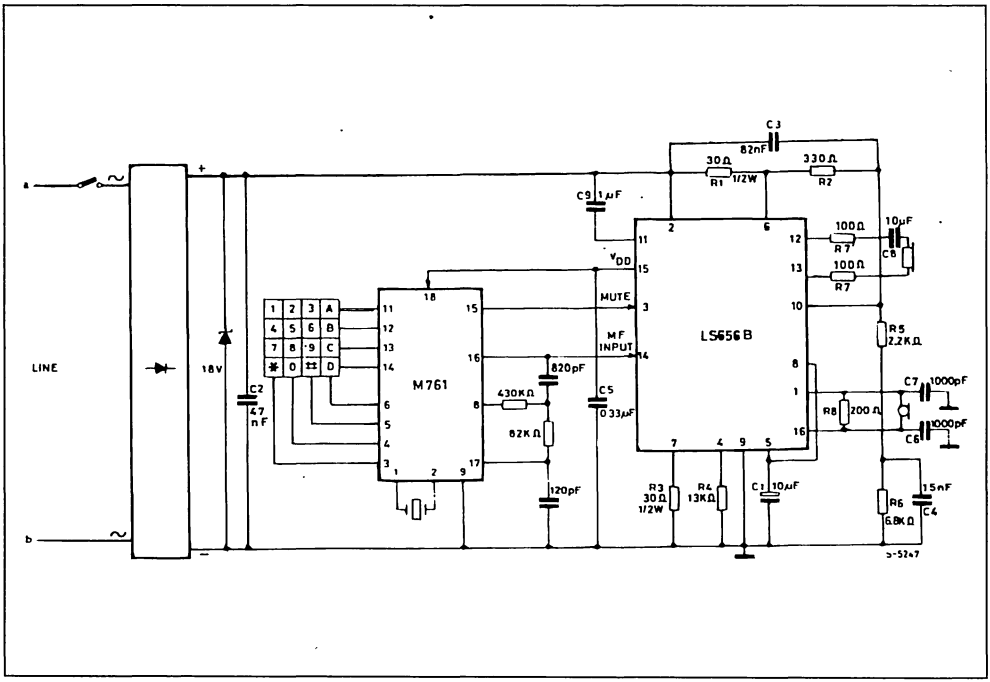


Figure 11 : Application Circuit with Multifrequency (Europe I STD).

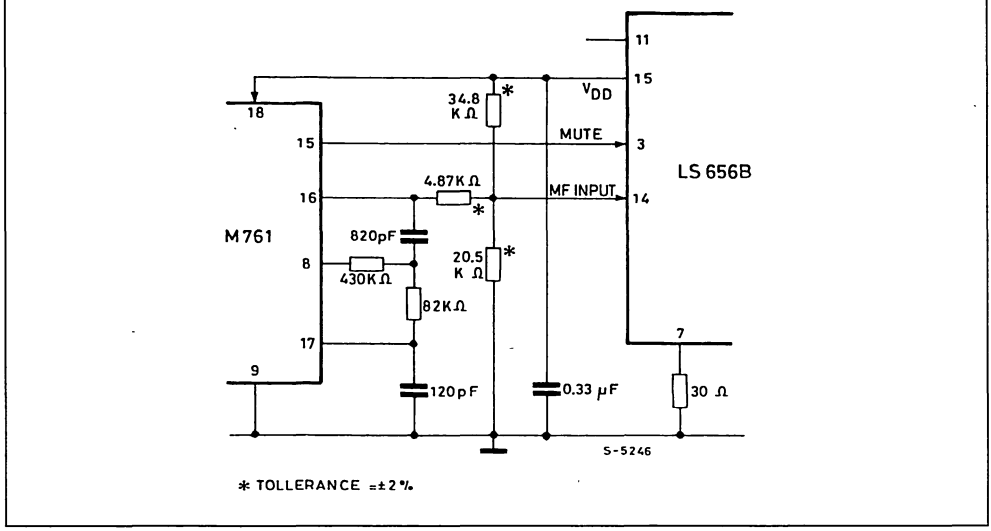


Figure 12 : Sending and Receiving Gain vs. Line Current (application circuit of fig. 10).

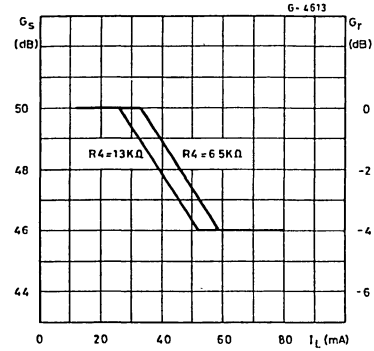


Figure 13 : Application Circuit without Multifrequency.

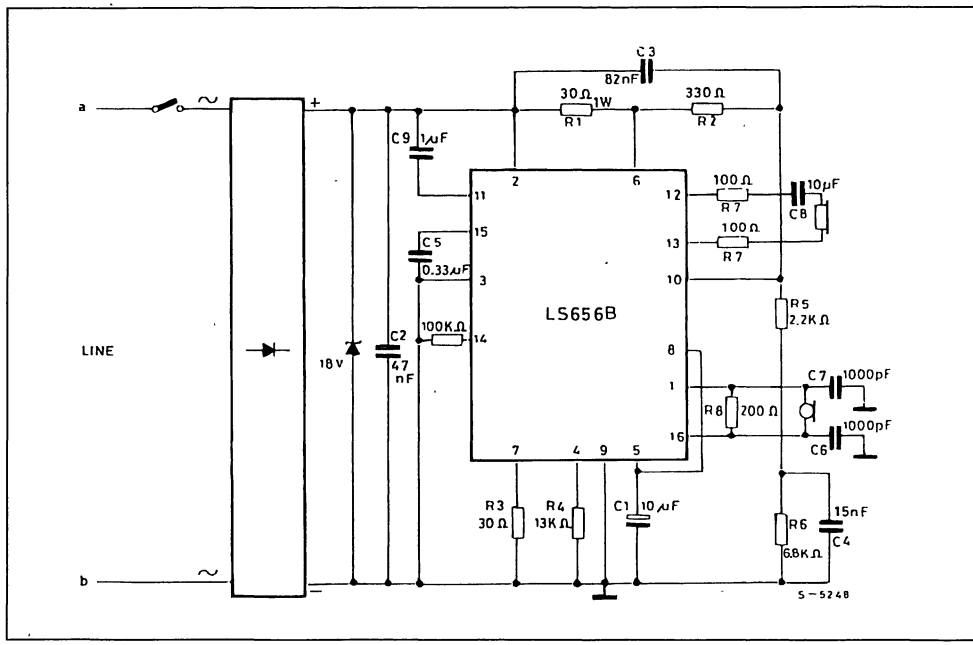


Figure 14 : Application Circuit with Gain Controlled by Line Voltage (french standard).

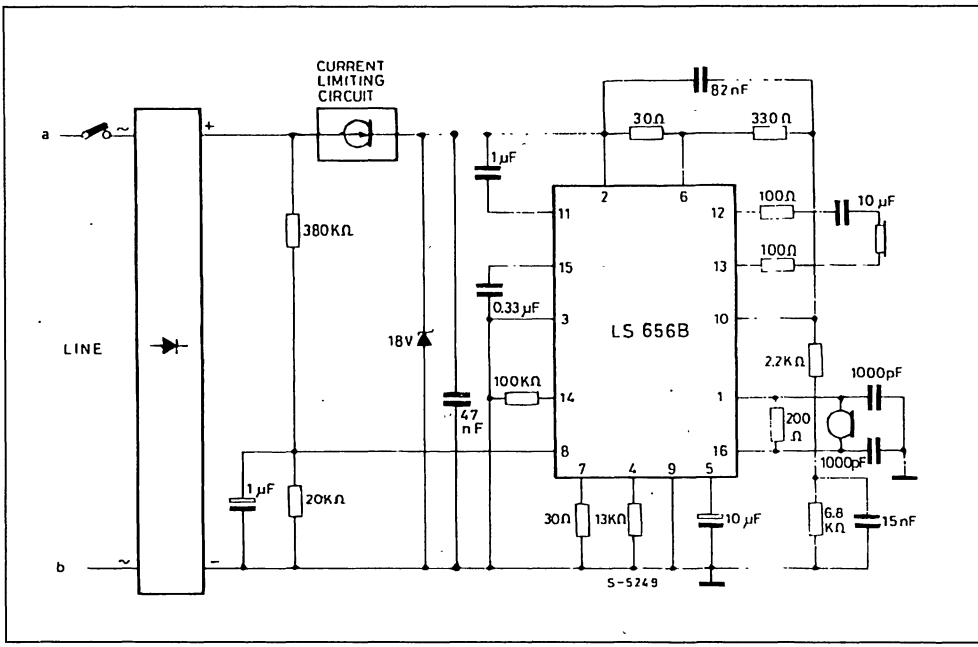
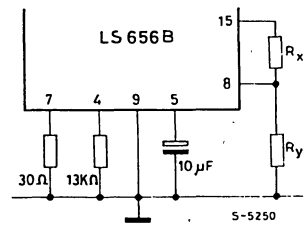
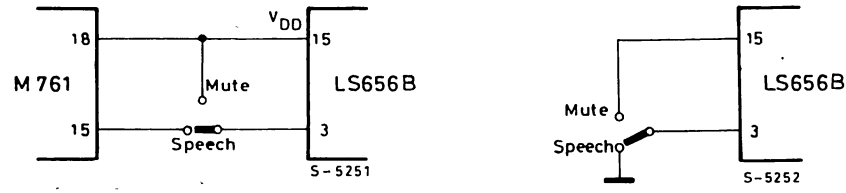


Figure 15 : Application Circuit with Fixed Gain Operation.



Ry = 0 Main gain condition
Rx = 0 Main gain condition

Figure 16 : External Mute Function.



a) with multifrequency

b) without multifrequency

In addition to the above mentioned applications, different values for the external components can be used in order to satisfy different requirements.
The following table (refer to the application circuit of fig. 10) can help the designers.

Component	Value	Purpose	Note
R1	30 Ω	Bridge Resistors	R1 controls the receiving gain. When high current values are allowed, R1 must be able to dissipate up to 1 W. The Ratio R2/R1 fixes the amount of signal delivered to the line. R1 helps in fixing the DC characteristics (see R3 note).
R2	330 Ω		
R3	30 Ω	Line Current Sensing Fixing DC Characteristic	The relationships involving R3 are : - $Z_{ML} = (20\ R3 // Z_B) + R1$ - $G_S = K \cdot \frac{Z_L // Z_{ML}}{R3}$ - $V_L = (I_L - I_O)(R3 + R1) + V_O$; $V_O = 3.7$ V Without any problem it is possible to have a Z_{ML} ranging from 600 up to 900 Ω. As far as the power dissipation is concerned, see R1 note.
R4	13 kΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point. (see fig. 16). After R4 changement, some variations could be found also in other parameters, i.e. line voltage.
R5	2.2 kΩ	Balance Network	It's possible to change R5 and R6 values in order to improve the matching to different lines ; in any case : $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ $Z_B = R5 + R6 // X_{C4}$
R6	6.8 kΩ		
R7-R7'	100 Ω	Receiver Impedance Matching	R7 and R7', must be equal ; the suggested value is good for matching to dynamic capsule ; there is no problem in increasing and decreasing (down to 0 Ω) this value. A DC decoupling must be inserted when low resistance levels are used to stop the current due to the receiver output offset voltage (max 200 mV).
R8	200 Ω	Microphone Impedance Matchin	

Component	Value	Purpose	Note
C1	10 µF	Regulator AC byPass	A value greater than 10 µF gives a system start time too high for low current line during MF operation ; a lower value gives an alteration of the AC line impedance at low frequency.
C2	47 nF	Matching to a Capacitive Line	C2 changes with the characteristics of the transmission line.
C3	82 nF	Receiving Gain Flatness	C3 depends on balancing and line impedance versus frequency.
C4	15 nF	Balance Network	See note for R5, R6.
C5	0.33 µF	DC Filtering	The C5 range is from 0.1 µF to 0.47 µF. The lowest value is ripple limited, the higher value is starting up time limited.
C6-C7	1000 pF	RF byPass	
C8	100 µF	Receiving Output DC Decoupling	See note for R7, R7.
C9	1 µF	Receiving Input DC Decoupling	

MASK - PROGRAMMABLE SPEECH CIRCUITS

ADVANCE DATA

Key Options

- MICROPHONE TYPES SUCH AS ELECTRODYNAMIC/MAGNETIC, ELECTRET OR CERAMIC
- POWER SUPPLY FOR EXTERNAL CIRCUITRY
- AGC CIRCUIT
- LINE REGULATION OF TRANSMIT/RECEIVE GAIN FOR CERTAIN TELEPHONE STATION POWER SUPPLIES
- EXTRA POWER SUPPLY INPUTS FOR OUTPUT AMPLIFIER TO BE USED IN HAND-FREE TELEPHONES
- SPECIAL IMPEDANCE/GAIN REQUIREMENTS
- MUTE OR TRANSMIT/RECEIVE AMPLIFIERS WITH OR WITHOUT CONFIRMATION TONE
- ACOUSTIC SHOCK ARRESTORS
- SIDETONE CANCELLATION CIRCUITRY

Pin Options

- MUTE/NO MUTE FUNCTION
- REGULATION OF SIDETONE WITH LINE LENGTH
- CUT OFF OF ALL LINE REGULATION

External Components (step by step)

- DC CHARACTERISTICS
- IMPEDANCE
- TRANSMIT GAIN
- TRANSMIT LINEARITY
- RECEIVE GAIN
- RECEIVE LINEARITY
- SIDETONE
- LOW VOLTAGE OPERATION

DESCRIPTION

PBL3726 is a family of mask-programmable speech circuits intended for various telephone applications. The flexibility of these circuits allows use of versions of PBL3726 in all telecom markets, whether it be in an ordinary telephone, a hands-free multi-function phone or even as a trunk interface. The versatility is based on three levels :

- Mask options for special requirements
- Pin options on certain functions
- Step-by-step design possibility on the basic telephone functions making it possible to cut down design time to a minimum. This is done by changing the values of a small number of external components.

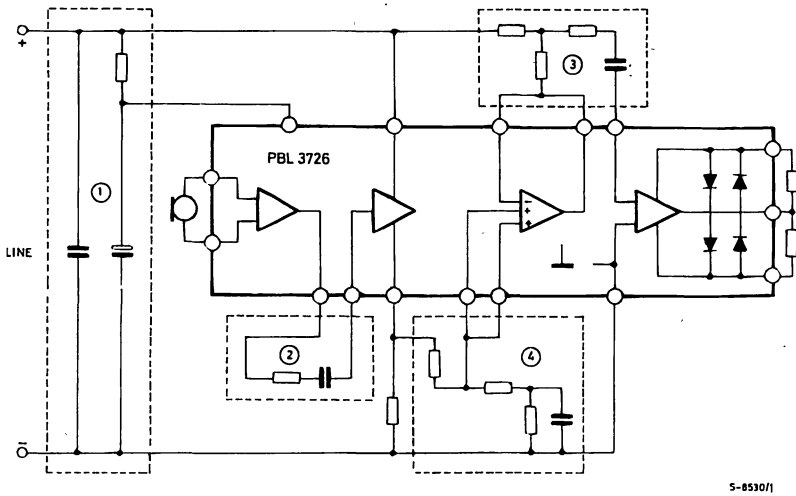
ABSOLUTE MAXIMUM RATINGS

Maximum Ratings over Operating Free-air Temperature Range (unless otherwise stated)

Symbol	Parameter	Test Conditions	Unit
V_{DC}	Line Voltage, $t_p = 2$ s	22	V
I_{DC}	Continuous Operating Line Current (*)	100	mA
T_j	Junction Temperature	+ 150	°C
T_{amb}	Operating Ambient Temperature	− 40 to + 70	°C
T_{stg}	Storage Temperature	− 55 to + 150	°C

(*) Max current increases linearly up to 130mA with max operating temperature lowered to + 55°C.

Figure 1 : Block Diagram and Typical Application.



External RC-networks
1) Line impedance and radio interference suppression
2) Transmitting amplifier, gain set and frequency adjustment
3) Receiver amplifier, gain set and frequency adjustment
4) Side tone adjustment

For recommended operating conditions see specific data sheets for different versions of PBL3726

FUNCTIONAL DESCRIPTION

The gains of the transmitting and receiving amplifiers are continuously and equally changed with the line length. The gain regulation can be cut off externally, and the gain will then be the maximum gain normally used at long lines.

The outputs of the transmitting and receiving amplifiers have internal limitations as to the output amplitudes.

The circuit includes a temperature independent voltage reference used for regulating the DC line current and for regulating the transmitting and receiving gain. The DC voltage quickly settles to its final value with a minimum of overshoot.

The circuit needs few external components. In a normal practical case there are only 5 external capacitors, one of which is an electrolytic/tantalum filter capacitor. The other capacitors are needed for radio interference suppression, to function in the sidetone balancing network, and to provide low frequency cut-off in each of the transmitting and receiving amplifiers.

The circuit has an excellent return loss characteristic against both purely resistive lines such as 600 Ω and against complex networks such as 900 Ω in parallel with 30 nF.

The microphone input is balanced to provide a good CMRR.

It is possible to add a push-button controlled cut-off of the transmitting amplifier of the circuit without disturbing any of the other circuit functions.

A mute input is included to :

1) Cut off the transmitting amplifier (F_1)
2) Reduce gain in the receiving amplifier
3) Reduce current consumption to lower power loss

The DC regulation works independently of the mute function and is not influenced by the mute signal. External mute-control of the circuit from a DTMF generator is then possible.

The receiver amplifier is equipped with a high impedance input stage, allowing a less expensive RC network on the input.

Only resistive elements are used to set the receiving gain.

A push-pull power stage in the receiving amplifier provides a high output swing.

The sidetone balance can be set by an RC network without influencing other parameters. An inexpensive solution requires only one capacitor whereas more capacitors may provide better performance. The sidetone can be regulated with respect to line length.

A separate amplifier stage (F_3) can be used in several different ways, for instance.

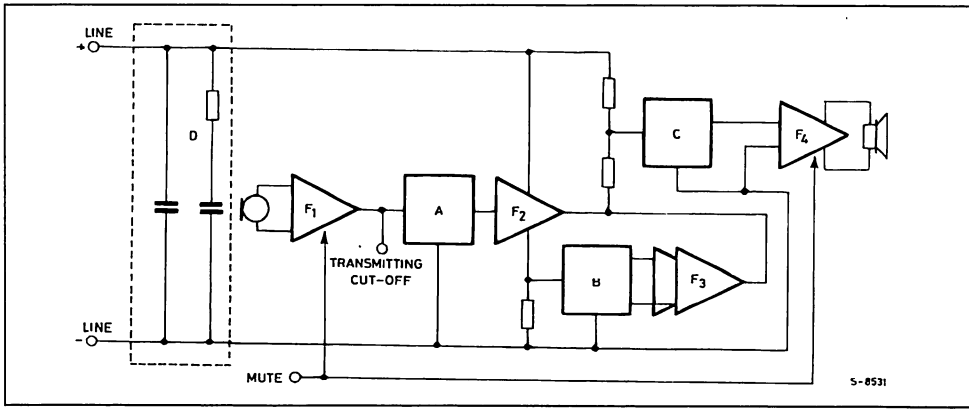
1) Separating the sidetone balance network

2) Compensating sidetone level for line length

3) Providing an extra 20dB gain for volume control of the receiving amplifier, etc.

This amplifier has many uses. In the following part only two examples of its use are given.

Figure 2.



A, B, C and D are RC links with the following functions :

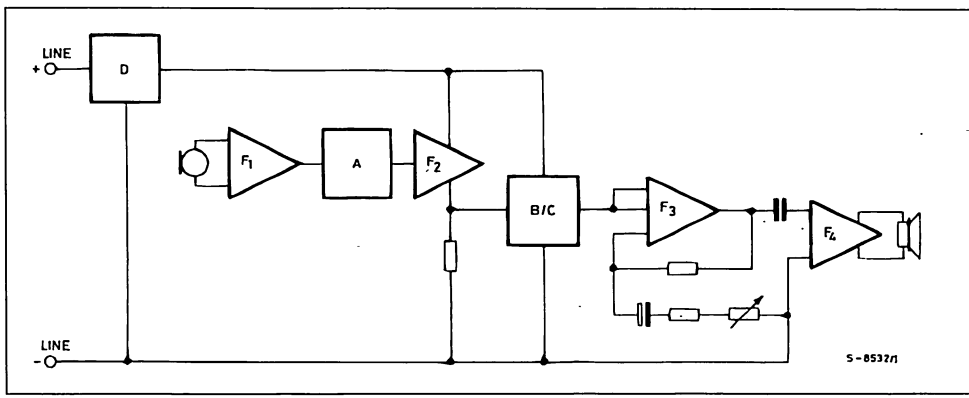
A : To set the gain and frequency response for transmitting

B : To set the sidetone level (regulation with line length is possible)

C : To set the gain and frequency response for receiving

D : For radio interference suppression and to give the correct return loss behaviour

Figure 3.



In this case an extra 20 dB amplification is added to the receiving part. A potentiometer provides the possibility of adjusting the gain to the required level.

BASIC EXTERNAL COMPONENTS

R1, R2.

These resistors set the starting point for the gain and sidetone regulation.

Input impedance on the regulator is about 52KΩ ± 2%. Only universal versions of PBL 3726 like PBL3726/6, 3726/9 etc. are equipped with this option. In the data sheets for these versions there is a table showing the R1, R2 values for different central office power supplies. The regulation can also be cut off by leaving R1 open and shorting R2 to-LINE voltage.

For other PBL 3726 versions the regulation is set internally for a specific power supply type.

C1, C2, R3.

C1 in series with R3 and these in parallel with C2 determine the impedance to the line from the set.

C2 is normally inserted for radio interference suppression.

The network is optimized with regard to the return loss.

The R3, C1 combination forms a low-pass filter in the DC-feedback loop of the transmitting amplifier. If the R3 C1 time constant is too low there may be distortion at low frequencies.

If R3 is changed this will change the DC characteristics too which is set by the voltage at V_{DD}. The input current at V_{DD} is about 1mA.

R4, R5, C3, C4.

The network gives the amplification and frequency response for the transmitter. R5 is used when a greater reduction of the gain is wanted. Input impedance at F_2 is about 17KΩ with typical variation ± 20%. The DC load on F_1 must be greater than 40KΩ.

Figure 4 : The PBL3726 and External RC Networks.

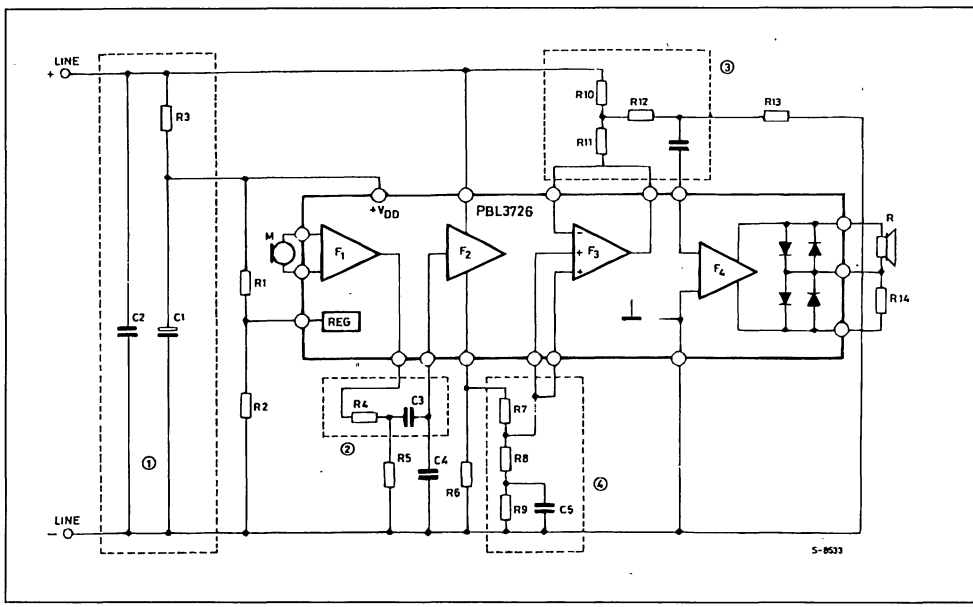
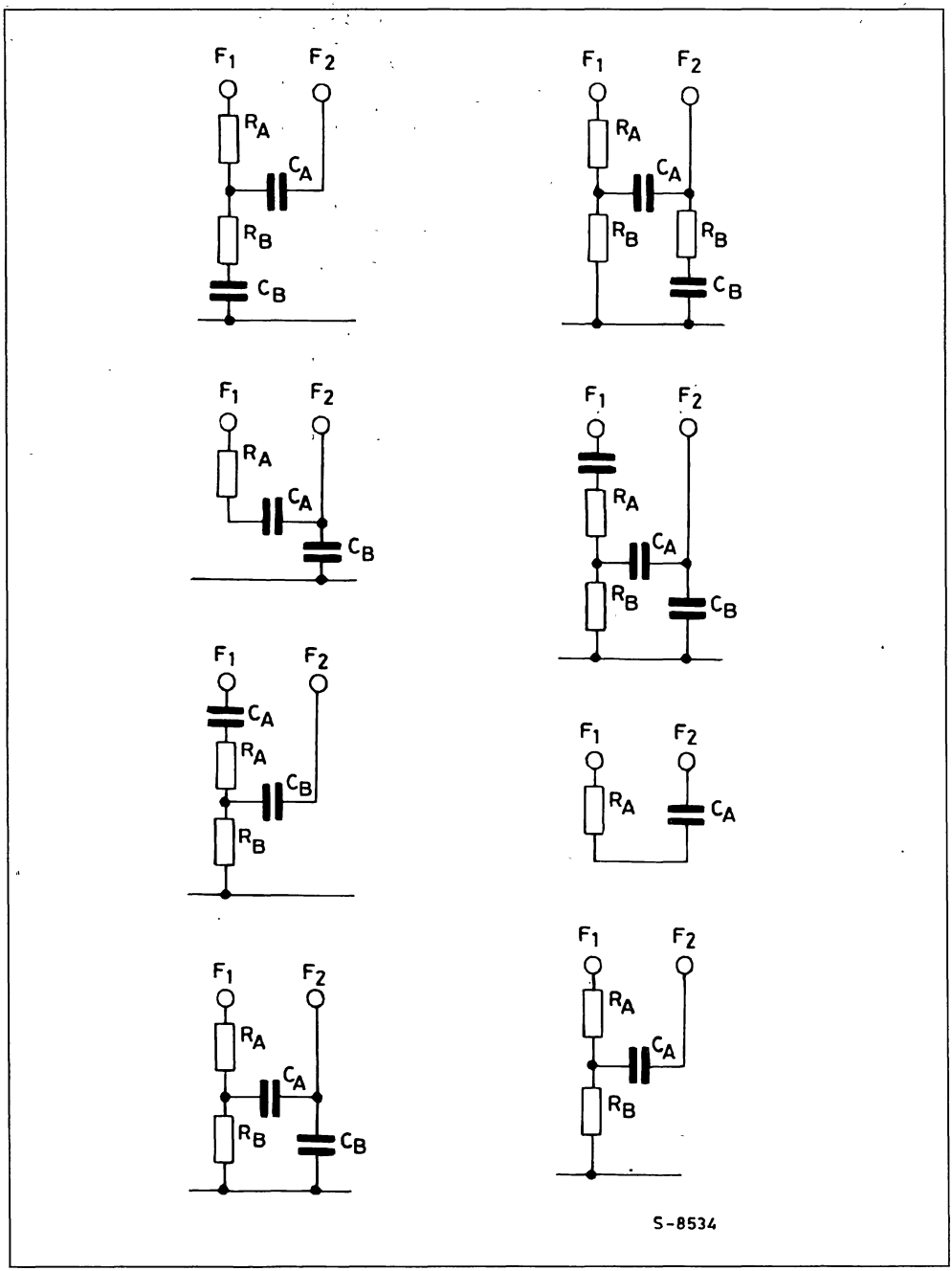


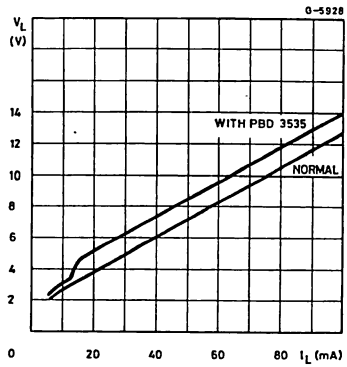
Figure 5 : Typical Filters.



R6.

Sets the DC Characteristics and dissipates some of the supplied power. The resistor also affects, the transmitter gain, the output amplitude from the transmitter, the gain regulation and the sidetone. Common values are 68Ω to 82Ω .

Figure 6 : Typical DC Characteristics.



R7, R8, R9, R10, R11, C5.

This network sets the sidetone balance. The network in the application is one of many possibilities.

R10 an R11 together balance the signals that exit two different ways from the transmitter output stage, one from pin 1 and the other from pin 2. The balance network consists of R8, R9 and C5.

Examples given in the data sheets for different versions of PBL3726 are not optimized to any specified line : they are given only to show the principle.

Amplifier F_3 has a high input impedance.

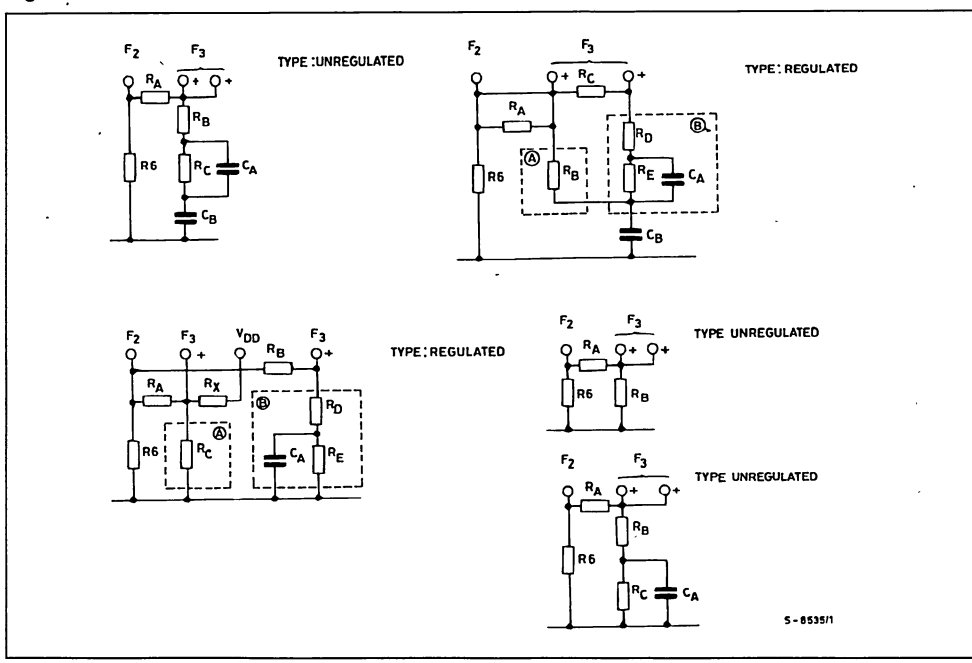
Shown in fig. 7 are some different sidetone networks.

Construction of a sidetone network with regulation according to the above can be done as follows :

The balance impedance A is optimized at a short line where the regulation starts. The balance impedance B is optimized at a long line where the regulation stops. The circuit generates a continuous change between the two balance impedances. R_X insures that no DC voltage shall be between F_3's double positive inputs at the change.

By breaking up between the negative input and output of F_3 it can be used as an amplifier with amplification greater than unit. In fig. 8 two balance networks without F_3 are shown. F_3 can then be used in other applications.

Figure 7 : Sidetone Network.



In fig. 9 a circuit is shown, where F_3 is used as an amplifier with an extra 20dB gain at receiving and with a volume control.

R12, R13, C6 (R10, R11).

The network gives the gain and frequency response for the receiver.

R13 is used when a greater reduction of the gain is wanted. Input impedance F_4 is about 35KΩ with typical variation ± 20%. For different possibilities for the design of the network, see the network for the transmitter (R4, R5, C3) in fig. 5.

R14.

Generates the output impedance to the magnetic earphone.

If a dynamic earphone is used it should be placed between outer connections. The middle connection is then not used.

This will give about a double output (for the same output current).

Rectifier. Rectifier bridge and over-voltage protector. The zener voltage at fig. 10 should be as low as possible. Common values are between 12V and 16V.

Figure 8 : Sidetone Netrwork without F_3.

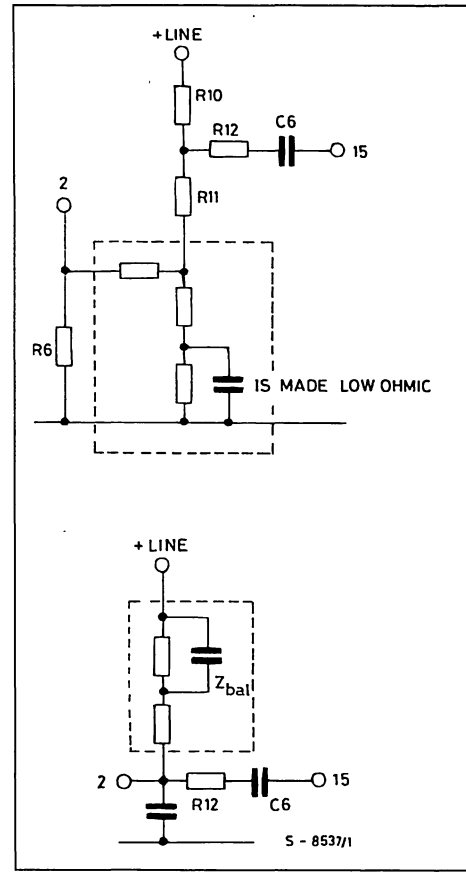


Figure 9 : 20dB Extra Amplifier (cannot be used in all version).

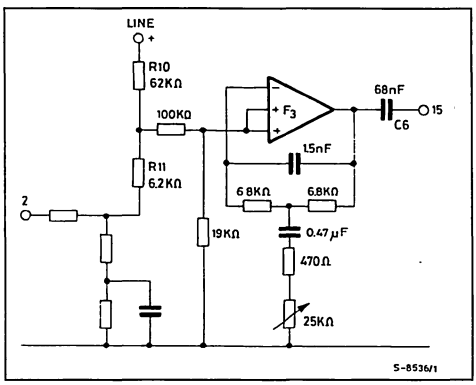
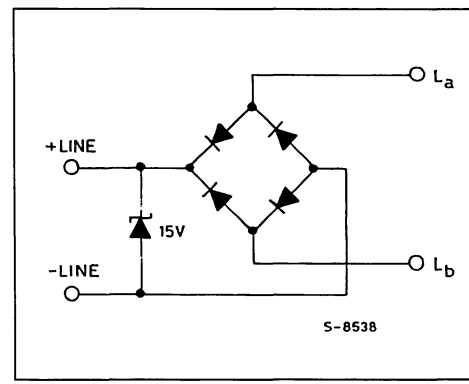


Figure 10 : Rectifier Bridge and Overvoltage Protection.



DESIGN RULES

The following order should always be used when designing telephone parameters.

1) The circuit impedance to the line
2) DC characteristics
3) Gain regulation
4) Transmitter gain and frequency response
5) Receiver gain and frequency response
6) Sidetone

Components usually have to be added to surpress radio interference, especially from the wires up to the handset.

(The circuit can be placed either in the telephone or in the handset).

IMPEDANCE.

This is determined with the components C1, C2, and R3 in most cases. In fig. 11 a few examples of this are shown. If a more complex impedance is desired as in the example for British Telecom (fig. 12), this can also be achieved by copying the mathematical model of the desired impedance.

Examples of line impedance matching :

Impedance	R3	C1	C2
600 Ω	600 Ω	47 µF	15 nF
900 Ω, 30 nF	900 Ω	47 µF	15 nF
1.2 kΩ, 60 nF	1.2 kΩ	47 µF	47 nF

Figure 12 : Example of complex Impedance Matching.

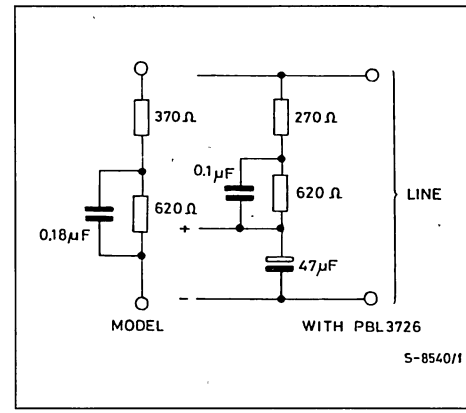
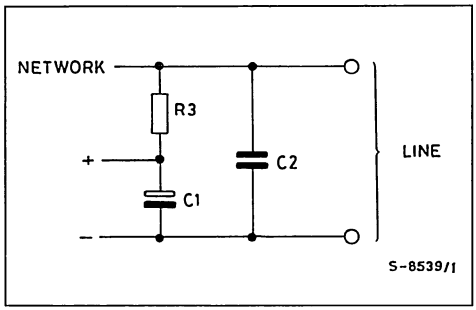


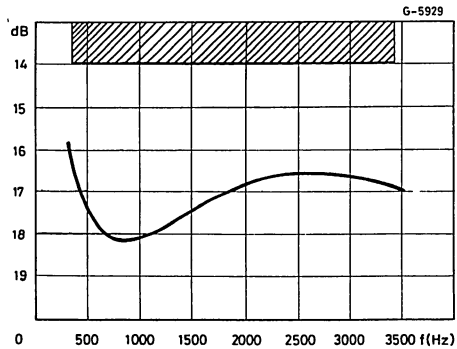
Figure 11 : Typical Return Loss Against 600Ω.

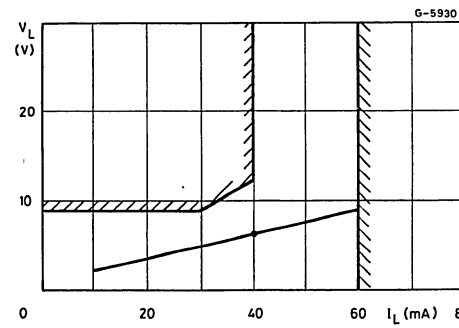


DC CHARACTERISTICS.

The slope of the DC characteristics is set by the resistor R6 (fig. 13). The lower value of R6, the flatter the slope. With the steaper slope the minimum DC

Figure 13 : Typical DC Characteristics.



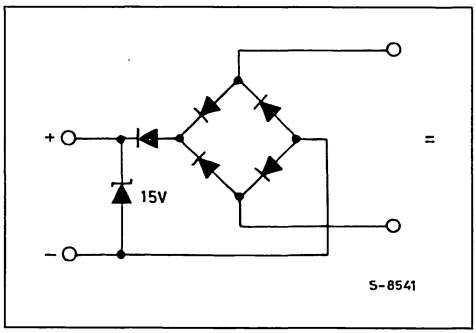


voltage also will go down. It is not recommended, though, to set the PBL3726 to DC voltages below 2.5V. If in some circumstances the DC characteristics of PBL3726 is too low, they can be raised by inserting an extra diode in series with the rectifier bridge as in fig. 14.

GAIN REGULATION.

When regulation with line length is used on send and receive gain, this can be set with the resistors R1 and R2. Note that not all versions are equipped with this function. By changing the values of these, the regulation attack can be set to fit any particular need.

Figure 14 : Rectifier Bridge with Extra Diode.



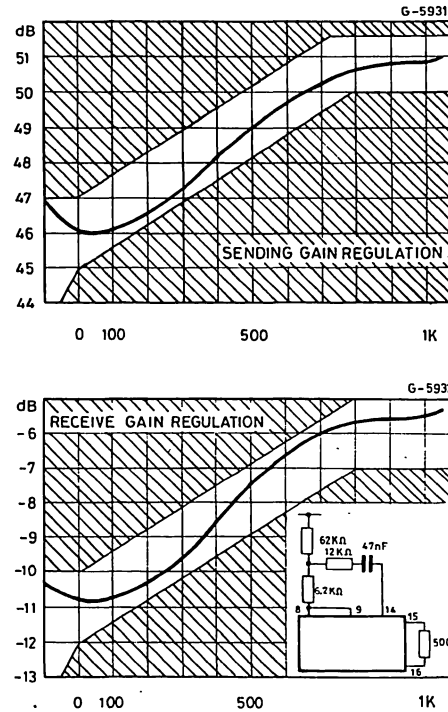
A table in the data sheets shows what values to use for some standard power supply systems. See example in fig. 15.

Figure 15 : Examples of Line-regulation Setting.

Line	R1	R2
50 V, 2 x 200 Ω	18 kΩ	47 kΩ
50 v, 2 x 400 Ω	9.1 kΩ	47 kΩ
50 V, 2 x 800 Ω	0	∞
Unregulated (all lines)	∞	0

Regulation input (pin 6 on PBL3726/6)

Figure 16 : Typical Gain Regulation with Line Lenght.



TRANSMITTER GAIN.

The resistor R4 sets the gain by attenuating the signal from amplifier F_1. If greater attenuation is needed a resistor (R5) can be connected to the minus line.

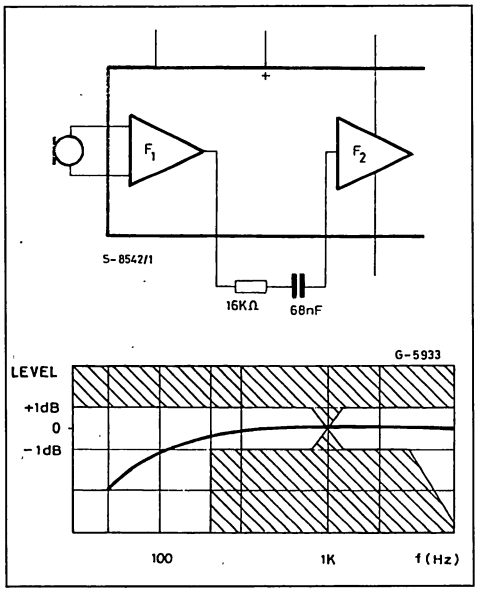
To get a frequency response appropriate for the microphone used a filter function as in fig. 5 can be used. These filters were previously described in this document.

The circuit can be provided with an unbalanced input as in fig. 18.

Cut off of the transmitter can be done at F_1 without interfering other functions of the circuit as in fig. 19.

Also signals other than DTMF signals can be added at input of F_2.

Figure 17 : Typical Response of PBL3726 Using Simple Filter.



For the version originally developed for electrodynamic/magnetic microphones it is also possible to use electret microphones as shown in fig. 20.

RECEIVER GAIN

In order to get the correct gain on the receive side, resistors R10 - R13 are used. Remember that R10 and R11 also set the rough ratio of the sidetone. R13 is used only in extreme circumstances, where a very

Figure 18 : Unbalanced Input.

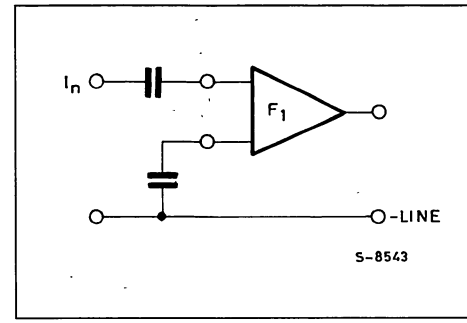


Figure 19 : Special Function.

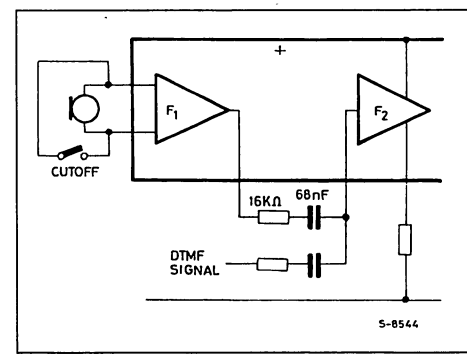
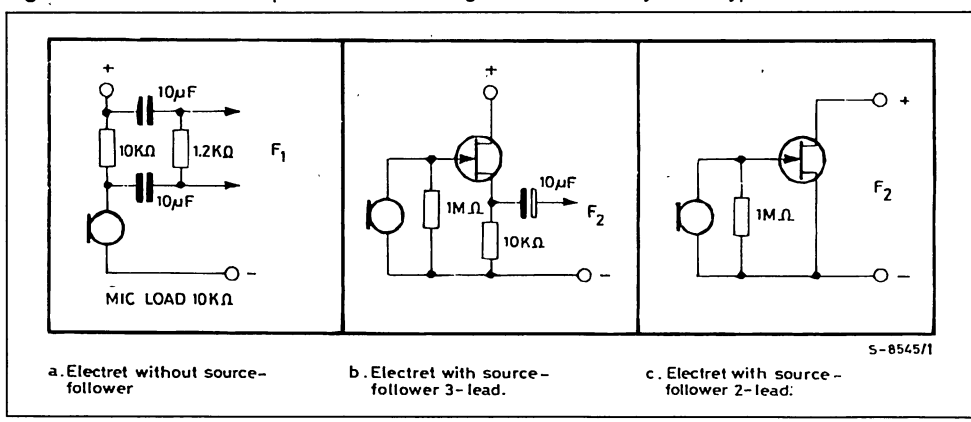


Figure 20 : Alternative Microphones of Electromagnetic and Electrodynamic Types for PBL3726.



a. Electret without source-follower

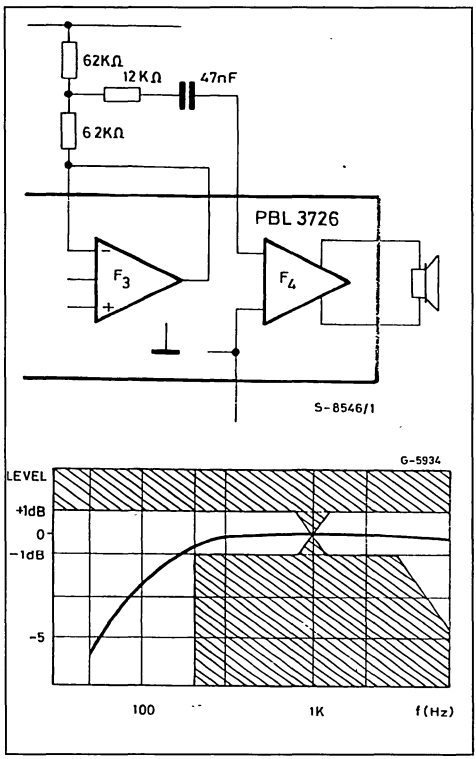
b. Electret with source-follower 3-lead.

c. Electret with source-follower 2-lead.

high receive gain attenuation is needed. The frequency response can be altered with the same filters used for the send gain (see fig. 5). To get protection against acoustic shock the diodes provided on some versions after the output of F_4 can be used.

One or two diode pairs can be used. Should this not be enough a resistor can be connected after the diodes (in series). This should be done before the setting of the receive gain.

Figure 21 : Typical Receive Gain.



SIDETONE

$$STMR = -\frac{10}{m} \times 10_{log}\{14 - \frac{m}{\sum_{i=1} 10^{10}} (W_{ST} + L_E\ S_S + S_R + A_{rst})\}$$

The most difficult part of the design work is always to define the sidetone. This should always be done last when designing with PBL3726. The sidetone is the sound of your own voice fed back into the ear by the handset.

The subjective effect of this is best seen in the formula above for "Side Tone Masking Rating".

Summed at the frequencies f_I = 0.2,

0.25.....4KHz (see fig. 22)

W_{ST} = Weighing factor

L_E = Leakage at receiver capsule

S_S = Send sensitivity

S_R = Receive sensitivity

A_{rst} = Hybrid-loss balance

The part that can be alteren by the speech circuit is the A_{rst} value that can be determined by the formula :

$$A_{rst} = 20\ 10_{log}\left[\frac{Z_C + Z_{SO}}{2\,Z_C} \times \frac{Z + Z_C}{Z - Z_{SO}}\right]$$

Where :

Z = Impedance of the connected telephone line

Z_{SO} = The balance impedance of the central office (PABX)

Z_C = Impedance of the speech circuit

The sum of Z and Z_{SO} can be called Z_{line}

The principle of the traditional so called active speech circuit has been the wheatstone bridge (fig. 23). The formula for the minimum sidetone is to balance until :

$$\frac{Z_2}{Z_1} = \frac{Z_{bal}}{Z_{line}}$$

Figure 22 : CCITT Factors.

f_I kHz	W_{ST} dB	L_E dB
0.2	86.4	8.4
0.25	81.9	4.9
0.315	78.5	1
0.4	78.2	– 0.7
0.5	72.8	– 2.2
0.63	67.6	– 2.6
0.8	58.4	– 3.2
1	49.7	– 2.3
1.25	48.0	– 1.2
1.6	48.7	– 0.1
2	50.7	3.6
2.5	49.8	7.4
3.15	48.4	6.7
4	49.2	8.8

The principle of PBL3726 is more complicated (even if calculation with the bridge in fig. 23 is possible). With the all-active bridge a method of cancelling the sidetone is a summing amplifier makes it possible to get not only one but two different sidetone optimums for different line lengths (see fig. 25). The function of the external components in fig. 7 have previously been described in this document. Fig. 26 shows an example of a sidetone network using the Wheatstone principle with PBL3726.

Figure 23 : Balance Bridge.

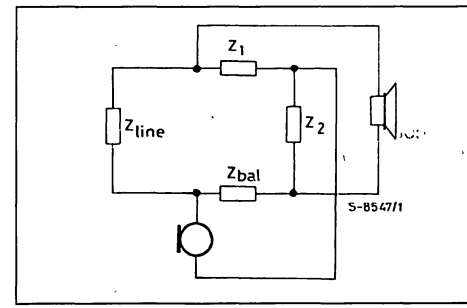


Figure 24 : Unregulated Sidetone Network.

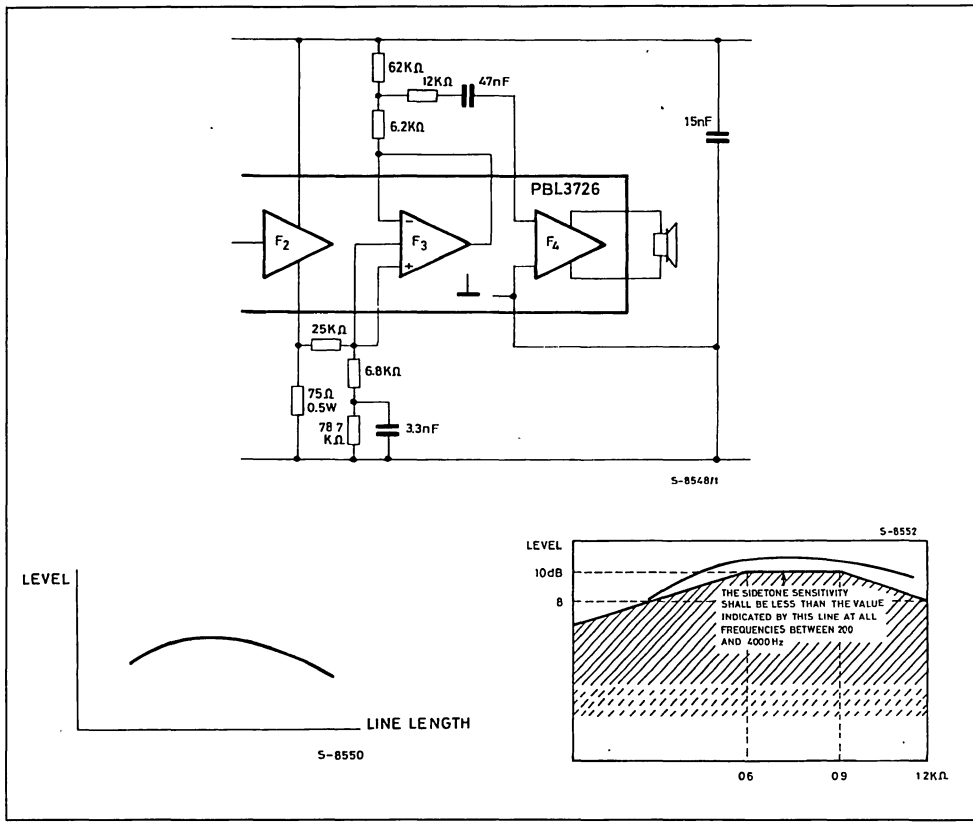


Figure 25 : Regulated Sidetone Network.

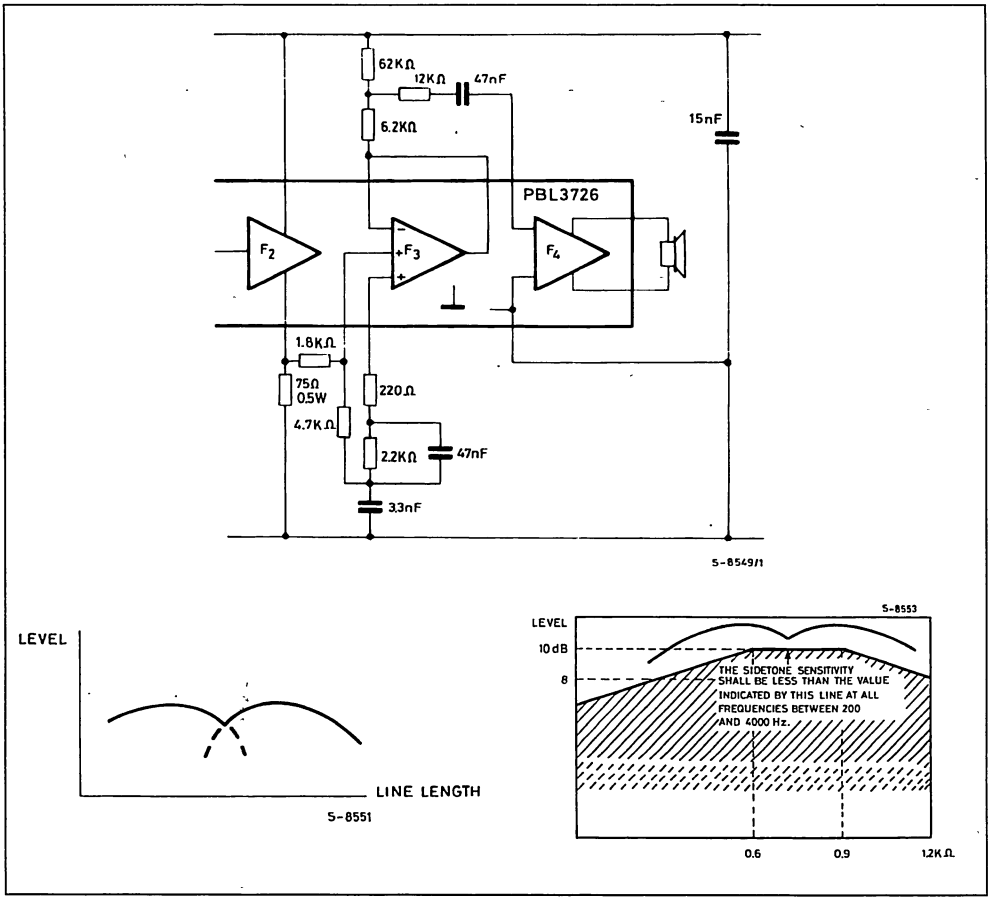
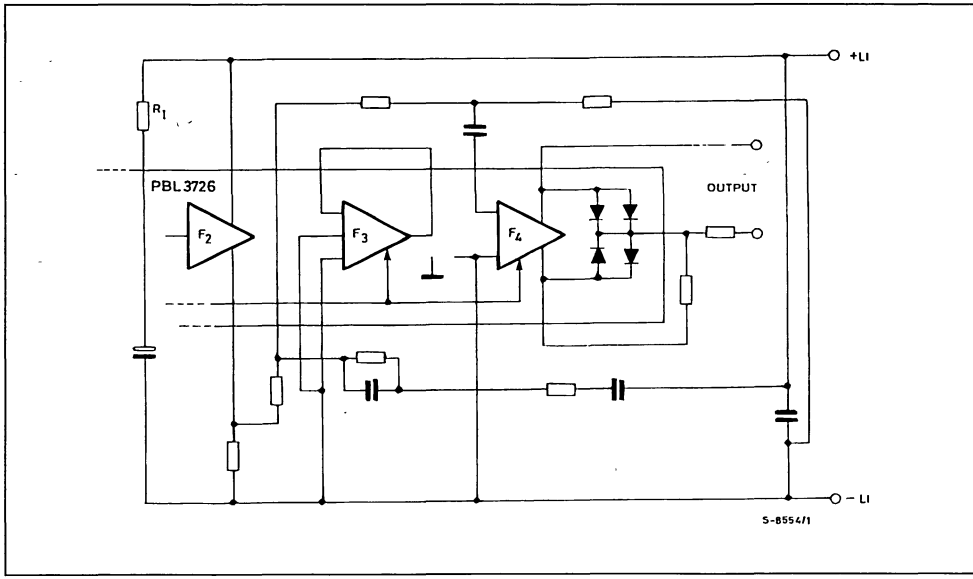


Figure 26 : Wheatstone Type Sidetone Network.



PRODUCT SUMMARY

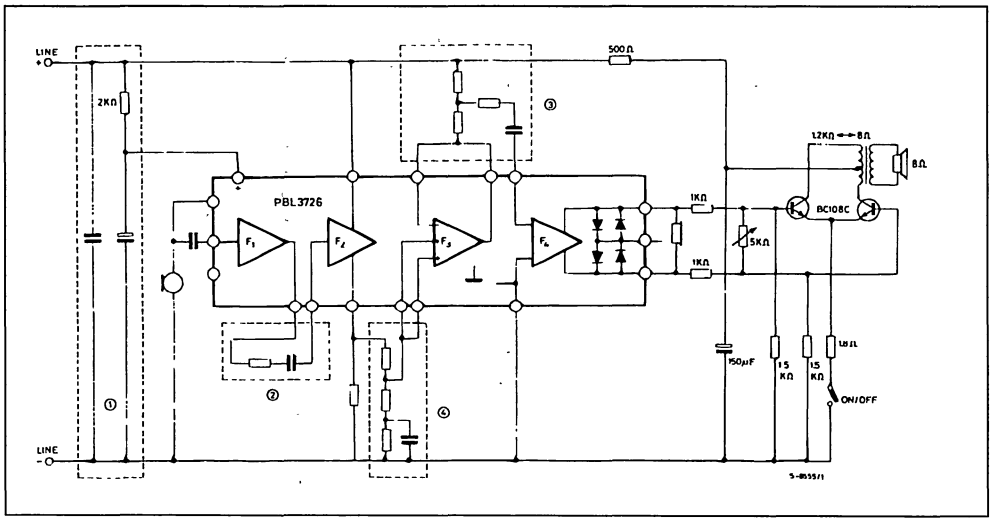
Speech Circuit	Microphone				Line	Regulated Side tone	Extra Receive Amp	Low Cost Speak Phone	Click Suppressor	Split Power Supply for Output Amp
	Carbon	Electro Magnetic	Electro Dynamic	Electret						
PBL3726/6		•	•		Adjustable	•	•	•	•	
PBL3726/8	•			•	36 V, 2 x 500 Ω 50 v, 2 x 800 Ω	•	•	•	•	
PBL3726/9	•			•	Adjustable	•	•	•	•	
PBL3726/11		•	•			•	•	•	•	
PBL3726/12		•	•		Adjustable	•	•	•	•	•

APPLICATIONS

To use PBL3726 in a hands-free telephone with a monitor function the schematics in fig. 27 can be used. The transformer should be rather efficient. Ordinary transistors can be used.

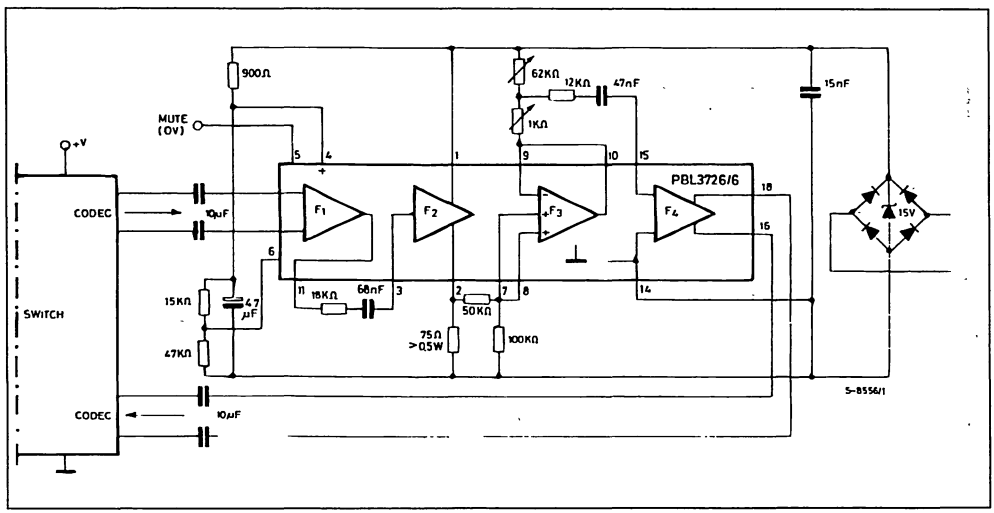
PBL3726 can also be used as trunk interface in modems, PABX, key systems etc where an analog interface against the telephone line is needed. The balanced inputs and outputs make this possible together with the possibility of regulated sidetone. Examples of both one-way and two-way data/signal communication with PBL3726/6 are shown in fig. 28.

Figure 27 : Monitor Loudspeaker.



TWO - WAY COMMUNICATION (SEND/RECEIVE)

Figure 28 : Trunk Interface Applications.

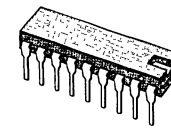


NOTES

MASK - PROGRAMMABLE SPEECH CIRCUITS

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 5 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATING WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATING, DOWN TO 3.3V
- VERY SHORT START-UP TIME



DIP-18
(Plastic)

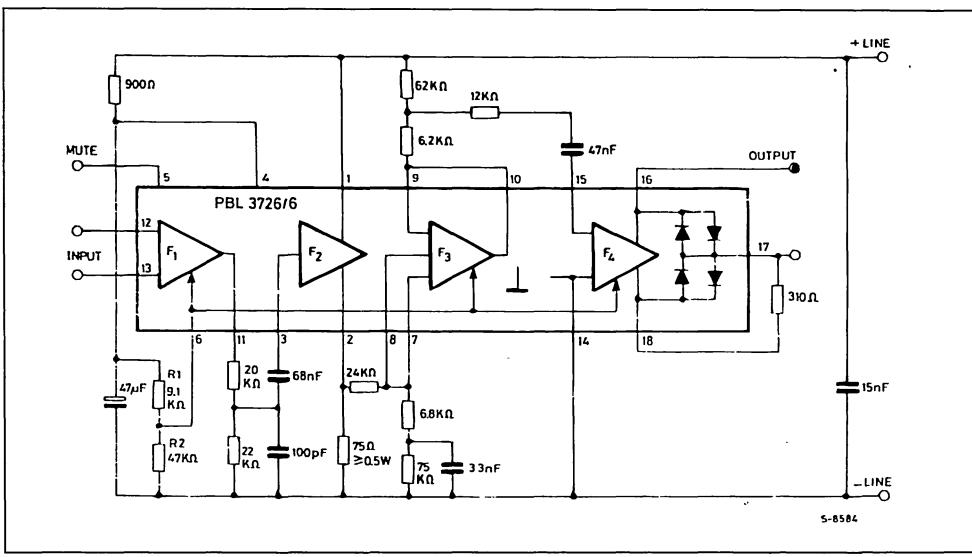
ORDER CODE : PBL3726/6

DESCRIPTON

PBL3726/6 is standard version of the PBL3726 family of the mask-programmable, monolithic integrated speech circuits for use with a low impedance microphone. Sending and receiving gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained with external resistor or totally cut off. Typical current feeds as 48V 2 x 200Ω 2 x 400Ω and 36V 2 x 250Ω can be handled.

Application-dependent paremeters as line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra 20dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Maximum Ratings over Operating Free-air Temperature Range (unless otherwise stated)

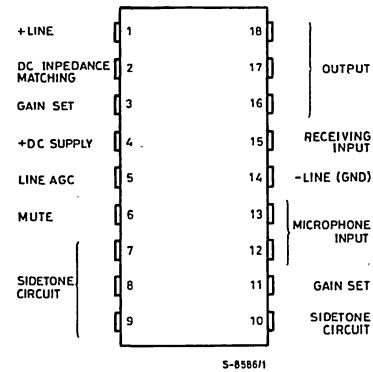
Symbol	Parameter	Test Conditions	Unit
V_{DC}	Line Voltage, t_p = 2 s	22	V
I_{DC} (*)	Continuous Operating Line Current	100	mA
T_j	Junction Temperature	+ 150	°C
T_{amb}	Operating Ambient Temperature	– 40 to + 70	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

(*) Max current increases linearly up to 130mA with max operating temperature lowered to + 55°C.

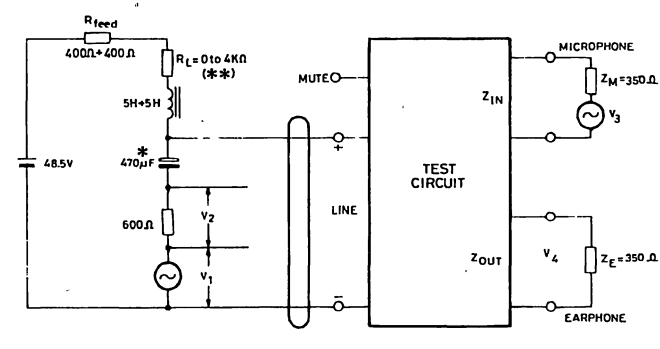
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current	15		100	mA

CONNECTION DIAGRAM



TEST SET-UP



THERMAL DATA

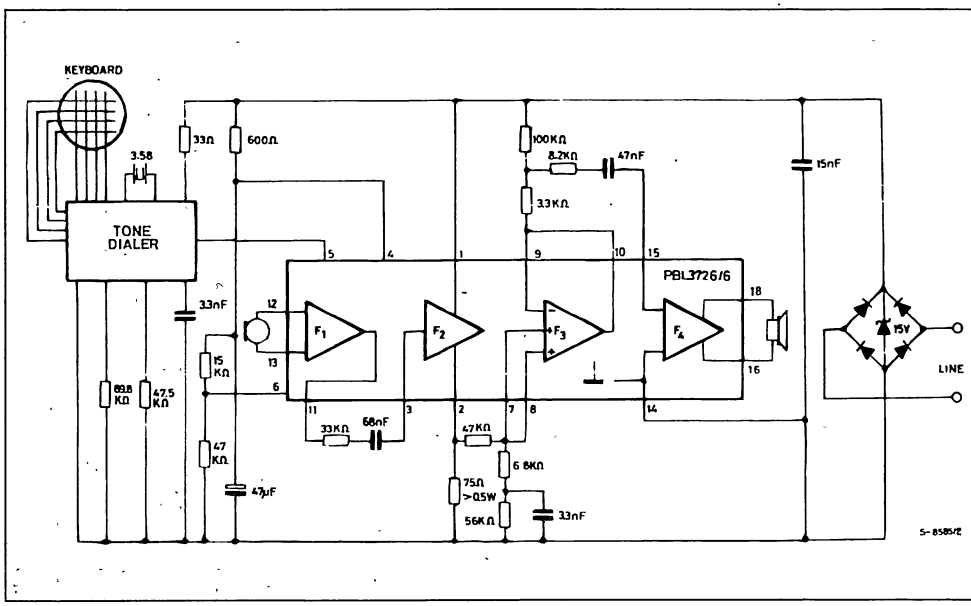
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (electrical characteristics over recommended operating conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DC}	Terminal Voltage	I_{DC} = 15 mA I_{DC} = 100 mA	3.3 11	3.7 13	4.1 15	V V
G_T	Transmitting Gain (*)	$20 . \log10 (\frac{V_2}{V_3})$ 1 kHz R_L = 0 E = E + 10 % R_L = 400 Ω R_L = 900 Ω – 2.2 kHz	 41 43.5 46	 43 45.5 48	 45 47.5 50	 dB dB dB
REG_T	Transmitting Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_T	Transmitting Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
G_R	Receiving Gain (*)	$20 . \log10 (\frac{V_4}{V_1})$ 1 kHz R_L = 0 Ω E = E + 10 % R_L = 400 Ω R_L = 900 Ω – 2.2 kΩ	 – 18.5 – 16 – 13.5	 – 16.5 – 14 – 11.5	 – 14.5 – 12 – 9.5	 dB dB dB
REG_R	Receiving Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_R	Receiving Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
Z_{IN}	Transmitter Input Impedance	1 kHz		1.1		kΩ
V_T	Transmitter Dynamic Output	200 Hz – 3.4 kHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA		1.5		V_p
V_T	Transmitter Max Output	200 Hz – 3.4 kHz I_{DC} = 0 – 100 mA V_3 = 0 – 1 V		3		V_p
Z_{OUT}	Receiver Output Impedance	1 kHz		3 + 310		Ω
	Receiver Dynamic Output **	200 Hz – 3.4 kHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA	0.5	0.55		V_p
V_R	Receiver Max Output	Measured with Line Rectifier 200 Hz – 3.4 kHz I_{DC} = 0 – 100 mA V_1 = 0 – 50 V		0.9		V_p
NT	Transmitter Output Noise	P_{sof}-weighted, REL 1 V R_L 0		– 75		dB_{psof}
N_R	Receiver Output Noise	A-weighted, REL 1 V, with Cable 0-5 Km Ø 0.5 mm ; 0-3 Km Ø 0.4 mm		– 85		dB_A
I_M	Mute Input Current		0.1			mA
I_{DC}	Extra Available Current when Muted at the Same DC-voltage	I_{DC} = 15 – 100 mA		10		mA

* Adjustable to both higher and lower values with external components.
** The dynamic output can be doubled. See application notes at R14.

Figure 1 : Typical Application.



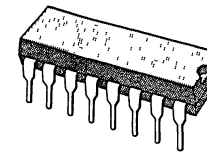
Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table.

Type	R1	R2
No Regulation all Feeding Systems	∞	0
48 V, 2 x 200 Ω	16 KΩ	47 KΩ
48 V, 2 x 400 Ω	9.1 KΩ	47 KΩ
36 v, 2x 500 Ω	0	∞

MASK - PROGRAMMABLE SPEECH CIRCUITS

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 6 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3V
- VERY SHORT START-UP TIME
- CURRENT-SOURCE GENERATOR FOR ACTIVE MICROPHONES



DIP-16
(Plastic)

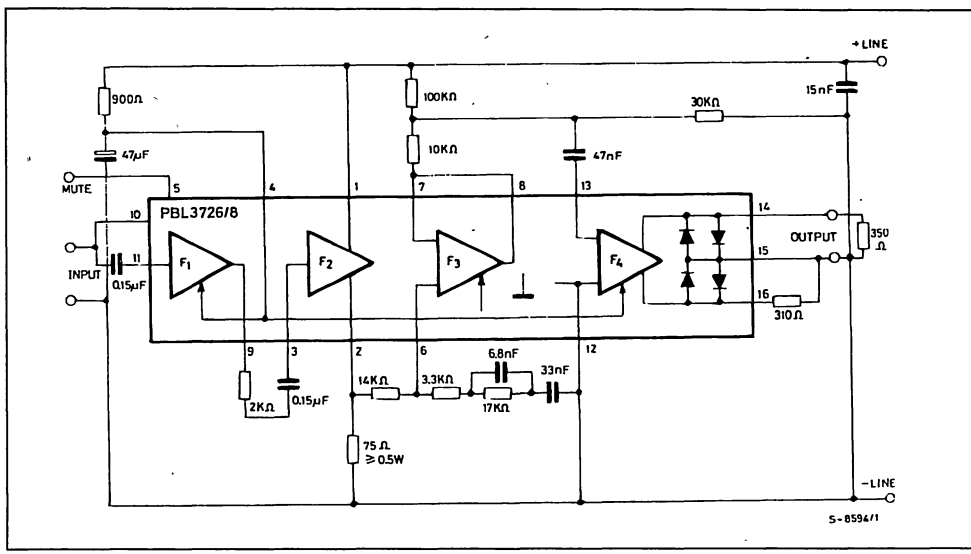
ORDER CODE : PBL3726/6

DESCRIPTON

PBL3726/8 is a standard version of the PBL3726 family of the mask-programmable, monolithic integrated speech circuits for use in electronic telephones. It is designed for use with a low impedance microphone. Sending and receiving gain is regulated with the line length. Different ranges of amplifier regulation for various current feeds can be obtained by mask programming. Typical current feeds such as 48V 2 x 800 , and 36V 2 x 500 can be handled.

Application-dependent parameters are line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra 20dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

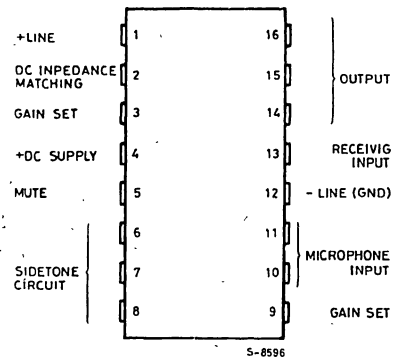
Maximum Ratings over Operating Free-air Temperature Range (unless otherwise stated)

Symbol	Parameter	Test Conditions	Unit
V_{DC}	Line Voltage, $t_p = 2$ s	22	V
I_{DC}	Continuous Operating Line Current	100	mA
T_j	Junction Temperature	150	°C
T_{amb}	Operating Ambient Temperature	– 40 to + 70	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

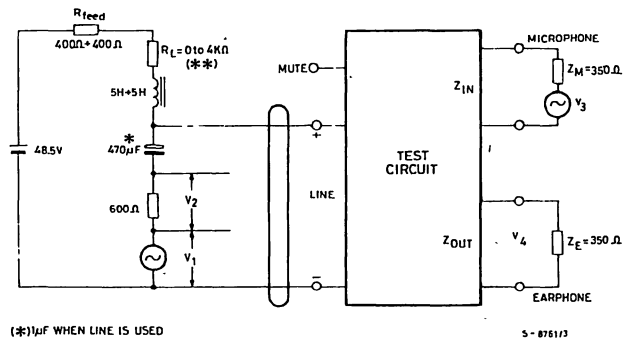
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current	10		60	mA
T_{amb}	Ambient Temperature	– 15		45	°C

CONNECTION DIAGRAM



TEST SET-UP



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (electrical characteristics over recommended operating conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DC}	Terminal Voltage	I_{DC} = 10 mA I_{DC} = 60 mA	3.0 7	3.5 9	4.0 10.5	V V
G_T	Transmitting Gain *	$20 . \log10 (\frac{V_2}{V_3})$ 1 kHz R_L = 0 E = E + 10 % R_L = 400 Ω R_L = 900 Ω – 2.2 kHz	 33 35.5 38	 34 36.5 39	 35 37.5 40	 dB dB dB
REG_T	Transmitting Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_T	Transmitting Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
G_R	Receiving Gain (*)	$20 . \log10 (\frac{V_4}{V_1})$ 1 kHz R_L = 0 Ω E = E + 10 %	 – 17.9	 – 16.5	 – 15.1	 dB
REG_R	Receiving Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_R	Receiving Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
Z_{IN}	Transmitter Input Impedance	1 kHz	17	20		kΩ
V_T	Transmitter Dynamic Output	200 Hz – 3.4 kHz ≤ 2 % Distortion I_{DC} = 11.25 – 50 mA	1.1			V_p
V_T	Transmitter Max Output	200 Hz – 3.4 kHz I_{DC} = 0 – 50 mA V_3 = 0 – 1 V			3	V_p
Z_{OUT}	Receiver Output Impedance	1 kHz		3 + 310		Ω
V_R	Receiver Dynamic Output **	200 Hz – 3.4 kHz ≤ 3 % Distortion I_{DC} = 11.25 – 50 mA	0.4			V_p
V_R	Receiver Max Output	Measured with Line Rectifier 200 Hz – 3.4 kHz I_{DC} = 0 – 50 mA V_1 = 0 – 50 V			0.9	V_p
N_T	Transmitter Output Noise	P_{sof}-weighted, REL 1 V R_L = 0		– 75		

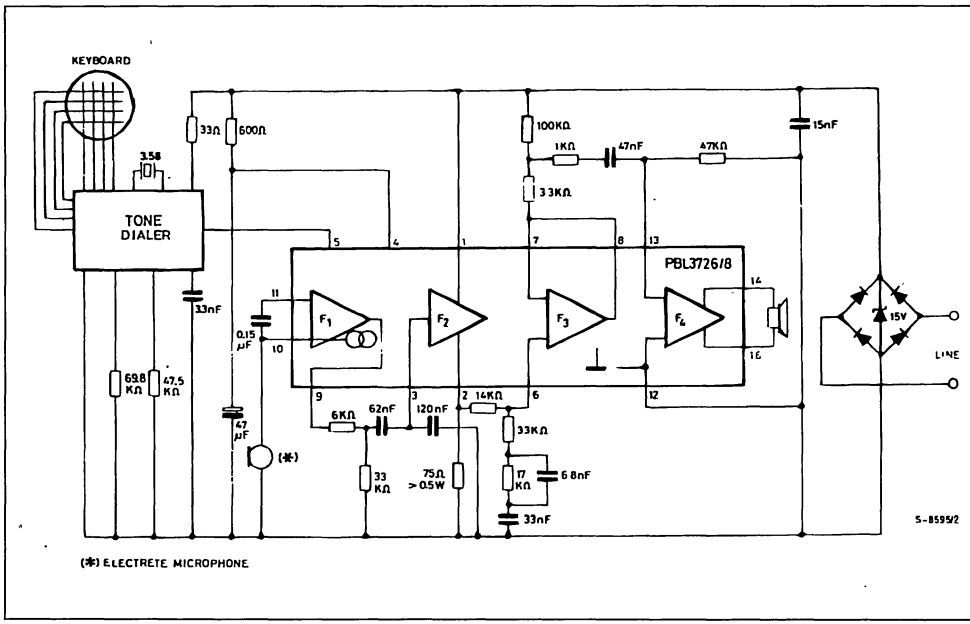
* Adjustable to both higher and lower values with external components.
** The dynamic output can be doubled. See application notes at R14.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_R	Receiver Output Noise	A-weighted, REL 1 V, with Cable 0-5 Km ∅ 0.5 mm ; 0-3 Km ∅ 0.4 mm		– 85		dB_A
I_M	Mute Input Current		0.1			mA
V_{DC}	Minimum DC-line Voltage when Muted	I_{DC} = 2.5 mA I_M = 0.1 mA	3.0			V
I_S	Supply Current for Microphone Amplifier	I_{DC} = 11.25 – 50 mA	300			µA
I_{DC}	DC Voltage for Microphone Amplifier	I_{DC} = 11.25 – 50 mA			2	V

* Adjustable to both higher and lower values with external components.
** The dynamic output can be doubled. See application notes at R14.

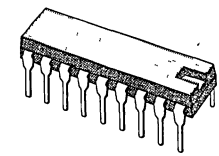
Figure 1 : Typical Application.



MASK - PROGRAMMABLE SPEECH CIRCUITS

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 6 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3V
- VERY SHORT START-UP TIME
- INTERNAL CURRENT-SOURCE GENERATOR FOR BUFFER AMPLIFIER OR A SIMILAR DEVICE



DIP-18
(Plastic)

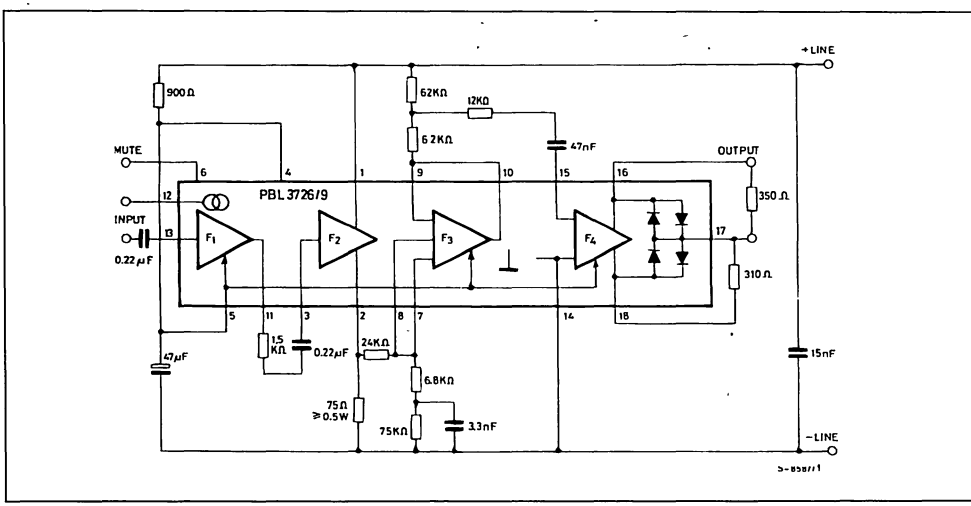
ORDER CODE : PBL3726/9

DESCRIPTON

PBL3726/9 is a standard version of the PBL3726 family of the mask-programmable, monolithic integrated speech circuit for use in electronic telephones. It is designed for use with electret microphone with a buffer amplifier. Sending and receiving gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained. Typical current feeds as 48V
2 x 200Ω, 2 x 400Ω and 36V 2 x 25Ω can be handled.

Application-dependent paremeters such as line balance, sidetone level and frequency response are set by external components. Parameters are set indpendently which means easy adaptationfor various market needs. An extra 20dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Maximum Ratings over Operating Free-air Temperature Range (unless otherwise stated)

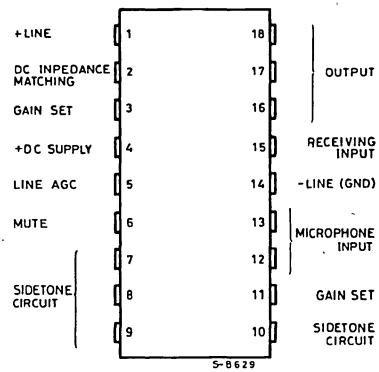
Symbol	Parameter	Test Conditions	Unit
V_{DC}	Line Voltage, $t_p = 2$ s	22	V
I_{DC} (*)	Continuous Operating Line Current	100	mA
T_j	Junction Temperature	150	°C
T_{amb}	Operating Ambient Temperature	– 40 to + 70	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

(*) Max. current increases linearly up to 130mA with max operating temperature lowered to + 55°C.

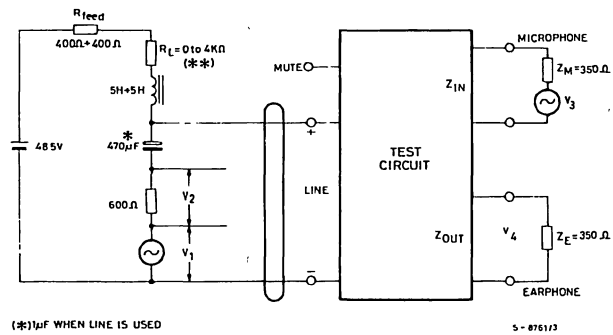
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current	15		100	mA

CONNECTION DIAGRAM



TEST SET-UP



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (electrical characteristics over recommended operating conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DC}	Terminal Voltage	I_{DC} = 15 mA I_{DC} = 100 mA	3.5 11	3.9 13	4.3 15	V V
G_T	Transmitting Gain *	$20 . \log10 (\frac{V_2}{V_3})$ 1 kHz R_L = 0 E = E + 10 % R_L = 400 Ω R_L = 900 Ω – 2.2 kHz	 24 26.5 28	 26 28.5 31	 28 30.5 33	 dB dB dB
REG_T	Transmitting Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_T	Transmitting Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
G_R	Receiving Gain *	$20 . \log10 (\frac{V_4}{V_1})$ 1 kHz R_L = 0 Ω E = E + 10 % R_L = 400 Ω R_L = 900 Ω – 2.2 kΩ	 – 18.5 – 16 – 13.5	 – 16.5 – 14 – 11.5	 – 14.5 – 12 – 9.5	 dB dB dB
REG_R	Receiving Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_R	Receiving Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
Z_{IN}	Transmitter Input Impedance	1 kHz		19		kΩ
V_T	Transmitter Dynamic Output	200 Hz – 3.4 kHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA		1.5		V_p
V_T	Transmitter Max Output	200 Hz – 3.4 kHz I_{DC} = 0 – 100 mA V_3 = 0 – 1 V		3		V_p
Z_{OUT}	Receiver Output Impedance	1 kHz		3 + 310		Ω
V_R	Receiver Dynamic Output **	200 Hz – 3.4 kHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA	0.5	0.55		V_p
V_R	Receiver Max Output	Measured with Line Rectifier 200 Hz – 3.4 kHz I_{DC} = 0 – 100 mA V_1 = 0 – 50 V		0.9		V_p
N_T	Transmitter Output Noise	P_{sof}-weighted, REL 1 V R_L = 0		– 75		dB_{psof}

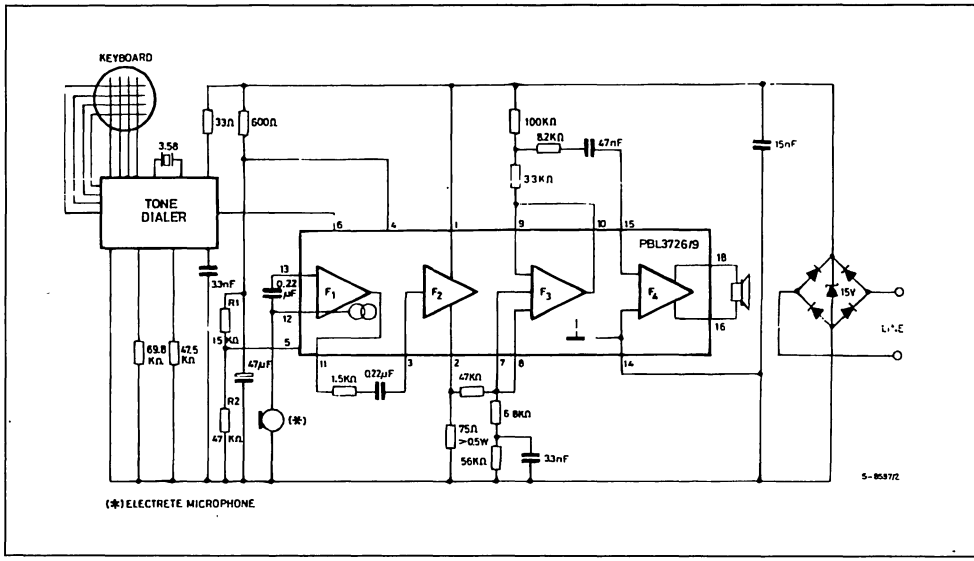
* Adjustable to both higher and lower values with external components.
** The dynamic output can be doubled. See application notes at R14.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_T	Transmitter Output Noise	P_{sof}-weighted, REL 1 V $R_L = 0$		– 75		dB_{psof}
N_R	Receiver Output Noise	A-weighted, REL 1 V, with Cable 0-5 km Ø 0.5 mm ; 0-3 km Ø 0.4 mm		– 85		dB_A
I_M	Mute Input Current		0.1			mA
I_{DC}	Extra Available Current when Muted at the Same DC-voltage	I_{DC} = 15 – 100 mA		10		mA
I_S	Supply Current for the Microphone	R_L = 0 – 800	310			µA

* Adjustable to both higher and lower values with external components.
** The dynamic output can be doubled. See application notes at R14.

Figure 1 : Typical Application.



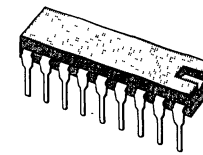
Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table.

Type	R1	R2
No Regulation, all Feeding Systems	∞	0
48 V, 2 x 400 Ω	14.5 KΩ	47 KΩ
48 V, 2 x 200 Ω	18 KΩ	47 KΩ

MASK - PROGRAMMABLE SPEECH CIRCUITS

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 5 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3V
- VERY SHORT START-UP TIME
- SIDETONE DISTORTION CANCELLATION



DIP-18
(Plastic)

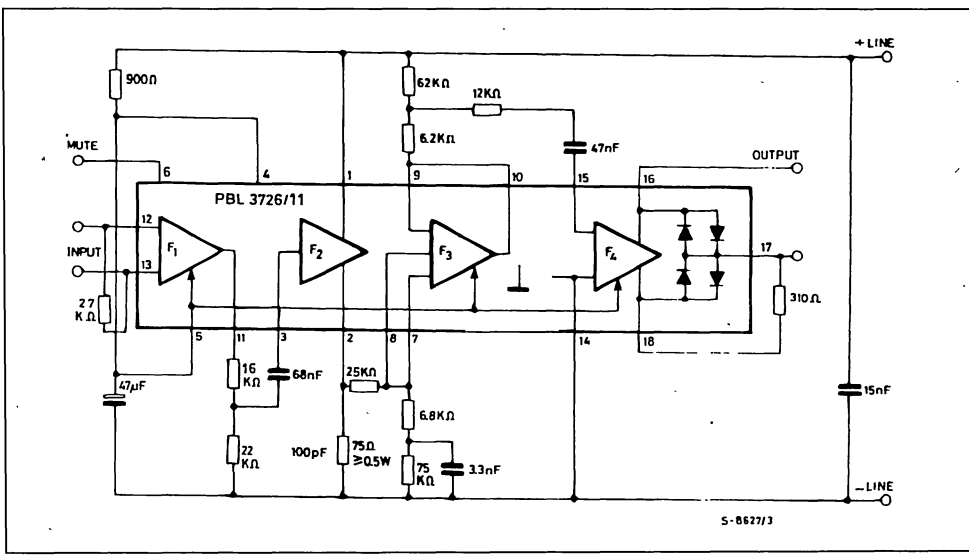
ORDER CODE : PBL3726/11

DESCRIPTON

PBL3726/11 is a standard version of the PBL3726 family of the mask-programmable, monolithic integrated speech circuits for use in electronic telephones. It is designed for use with a low impedance microphone. Sending and receiving gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained with external resistor or totally cur off. Typical current feeds such as 48V 2 x 200Ω, 2 x 400Ω and 36V 2 x 250Ω can be handled.

Application-dependent parameters such as line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra amplifier can be used for various purposes such as active sidetone balance.

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Maximum Ratings over Operating Free-air Temperature Range (unless otherwise stated)

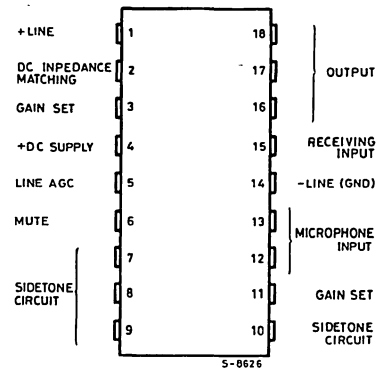
Symbol	Parameter	Test Conditions	Unit
V_{DC}	Line Voltage, t_p = 2 s	22	V
I_{DC} (*)	Continuous Operating Line Current	100	mA
T_j	Junction Temperature	150	°C
T_{amb}	Operating Ambient Temperature	– 40 to + 70	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

(*) Max. current increases linearly up to 130mA with max operating temperature lowered to + 55°C.

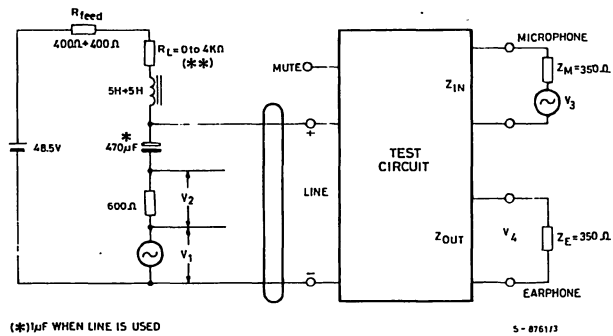
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current	15		100	mA

CONNECTION DIAGRAM



TEST SET-UP



SGS-THOMSON MICROELECTRONICS

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (electrical characteristics over recommended operating conditions)

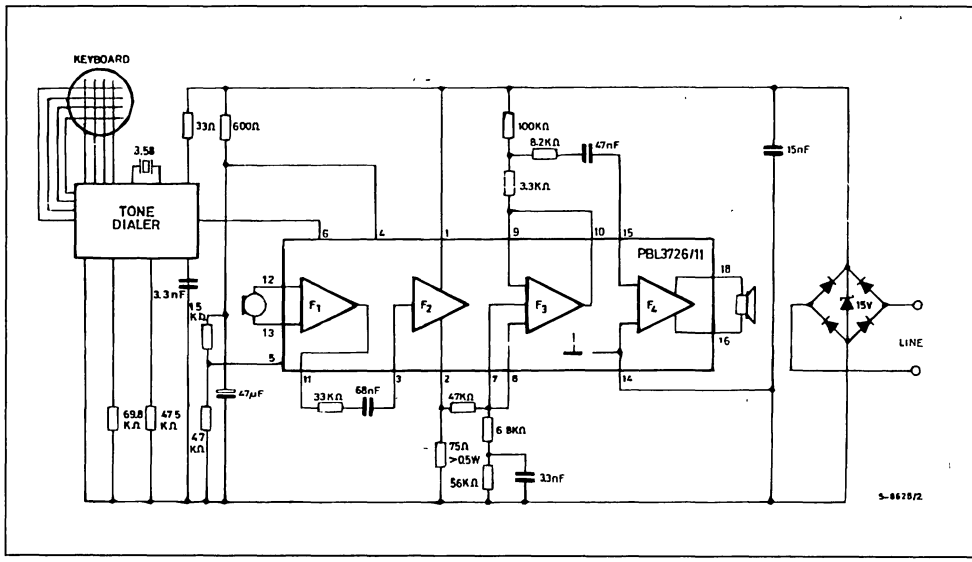
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_D	Terminal Voltage	I_{DC} = 15 mA I_{DC} = 100 mA	3.3 11	3.7 13	4.1 15	V V
G_T	Transmitting Gain *	$20 . \log10 (\frac{V_2}{V_3})$ 1 kHz R_L = 0 E = E + 10 % R_L = 400 Ω R_L = 900 Ω – 2.2 kHz	 41 43.5 46	 43 45.5 48	 45 47.5 50	 dB dB dB
REG_T	Transmitting Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_T	Transmitting Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
G_R	Receiving Gain *	$20 . \log10 (\frac{V_4}{V_1})$ 1 kHz R_L = 0 Ω E = E + 10 % R_L = 400 Ω R_L = 900 Ω – 2.2 kΩ	 – 18.5 – 16 – 13.5	 – 16.5 – 14 – 11.5	 – 14.5 – 12 – 9.5	 dB dB dB
REG_R	Receiving Range of Regulation	1 kHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_R	Receiving Frequency Response	200 Hz to 3.4 kHz	– 1		1	dB
Z_{IN}	Transmitter Input Impedance	1 kHz		1050		Ω
V_T	Transmitter Dynamic Output	200 Hz – 3.4 kHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA		1.5		V_p
V_T	Transmitter Max Output	200 Hz – 3.4 kHz I_{DC} = 0 – 100 mA V_3 = 0 – 1 V		3		V_p
Z_{OUT}	Receiver Output Impedance	1 kHz		3 + 310		Ω
	Receiver Dynamic Output **	200 Hz – 3.4 kHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA V_1 = 0 – 50 V		0.5		V_p

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_R	Receiver Max Output	Measured with Line Rectifier 200 Hz – 3.4 kHz I_{DC} = 0 – 100 mA V_1 = 0 – 50 V		0.9		V_p
N_T	Transmitter Output Noise	P_{sof}-weighted, REL 1 V R_L = 0		– 75		dB_{psof}
N_R	Receiver Output Noise	A-weighted, REL 1 V, with Cable 0-5 km Ø 0.5 mm ; 0-3 km Ø 0.4 mm		– 85		dB_A
I_M	Mute Input Current		0.1			mA
I_{DC}	Extra Available Current when Muted at the Same DC-voltage	I_{DC} = 15 – 100 mA		10		mA

* Adjustable to both higher and lower values with external components.
** The Dynamic output can be doubled. See application notes at R14.

Figure 1 : Typical Application.



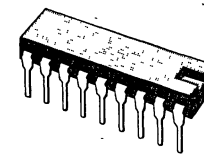
Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table.

Type	R1	R2
No Regulation, all Feeding Systems	∞	0
48 V, 2 x 200 Ω	16 KΩ	47 KΩ
48 V, 2 x 400 Ω	9.1 K	47 KΩ

MASK - PROGRAMMABLE SPEECH CIRCUITS

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 5 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3 V
- VERY SHORT START-UP TIME
- SEPARATE POWER SUPPLY POSSIBLE FOR OUTPUT AMPLIFIER



DIP-18
(Plastic)

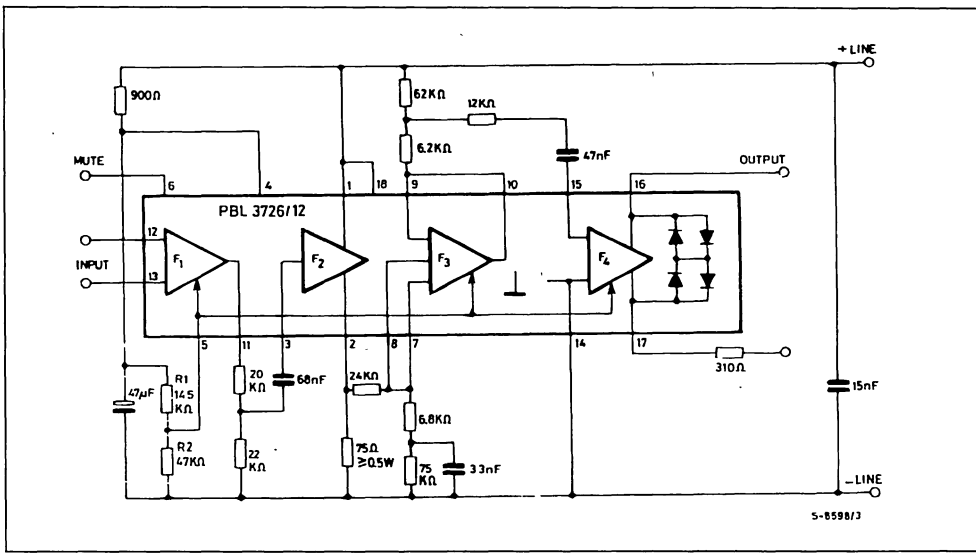
ORDER CODE : PBL3726/12

DESCRIPTON

PBL3726/12 is a standard version of the PBL3726 family of the mask-programmable, monolithic integrated speech circuits for use in electronic telephones. It is designed for use with a low impedance microphone. Sending and receiving gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained. Typical current feeds as 48 V 2 x 250 Ω 2 x 400 Ω and 36 V 2 x 250 Ω can be handled.

Application-dependent parameters such as line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra 20 dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

(Maximum Ratings over Operating Free-air Temperature Range unless otherwise stated)

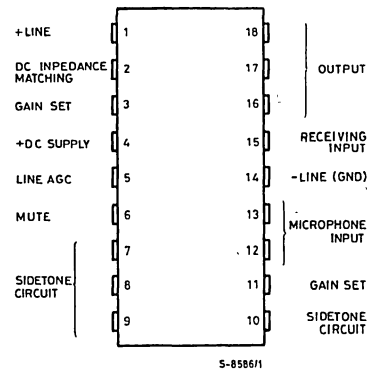
Symbol	Parameter	Test Conditions	Unit
V_{DC}	Line Voltage, t_p = 2 s	22	V
I_{DC} (*)	Continuous Operating Line Current	100	mA
T_j	Junction Temperature	150	°C
T_{amb}	Operating Ambient Temperature	– 40 to + 70	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

(*) Max. current increases linearly up to 130 mA with max operating temperature lowered to + 55 °C.

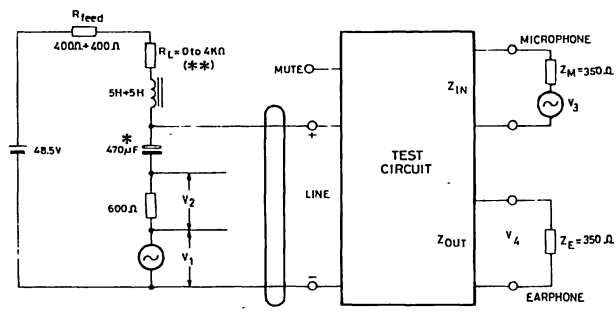
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current	15		100	mA

CONNECTION DIAGRAM



TEST SET-UP



THERMAL DATA

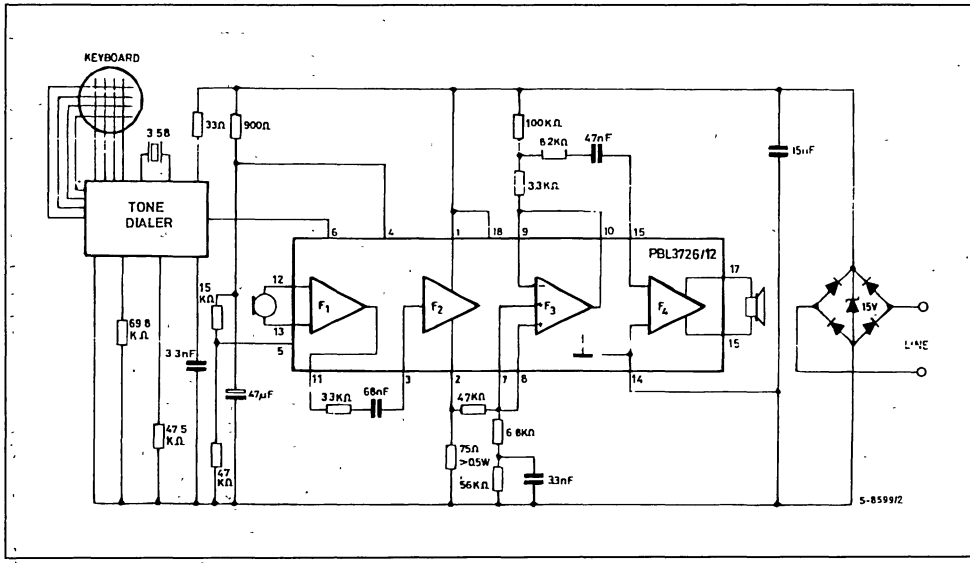
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (electrical characteristics over recommended operating conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_D	Terminal Voltage	I_{DC} = 15 mA I_{DC} = 100 mA	3.3 11	3.7 13	4.1 15	V V
G_T	Transmitting Gain *	20 . log10 ($\frac{V_2}{V3}$) 1 KHz R_L = 0 E = E + 10 % R_L = 900 Ω – 2.2 KHz	 38 43	 40 45	 42 47	 dB dB
REG_T	Transmitting Range of Regulation	1 KHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_T	Transmitting Frequency Response	200 Hz to 3.4 KHz	– 1		1	dB
G_R	Receiving Gain *	20 . log10 ($\frac{V_4}{V1}$) 1 KHz R_L = 0 Ω E = E + 10 % R_L = 900 Ω – 2.2 KΩ	 – 18.5 – 13.5	 – 16.5 – 11.5	 – 14.5 – 9.5	 dB dB
REG_R	Receiving Range of Regulation	1 KHz R_L = 0 Ω E = E + 10 % to R_L = 900 Ω	3	5	7	dB
Lin_R	Receiving Frequency Response	200 Hz to 3.4 KHz	– 1		1	dB
Z_{IN}	Transmitter Input Impedance	1 KHz		2.5		KΩ
V_T	Transmitter Dynamic Output	200 Hz – 3.4 KHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA		1.4		V_p
V_T	Transmitter Max Output	200 Hz – 3.4 KHz I_{DC} = 0 – 100 mA V_3 = 0 – 1 V		3		V_p
Z_{OUT}	Receiver Output Impedance	1 KHz		3 + 310		Ω
V_R	Receiver Dynamic Output **	200 Hz – 3.4 KHz ≤ 2 % Distortion I_{DC} = 20 – 100 mA		0.4		V_p
V_R	Receiver Max Output	Measured with Line Rectifier 200 Hz – 3.4 KHz I_{DC} = 0 – 100 mA V_1 = 0 – 50 V		0.9		V_p
N_T	Transmitter Output Noise	P_{sof}-weighted, REL 1 V R_L = 0		– 75		dB_{psof}
N_R	Receiver Output Noise	A-weighted, REL 1 V, with Cable 0-5 Km Ø 0.5 mm ; 0-3 Km Ø 0.4 mm		– 85		dB_A
I_M	Mute Input Current		0.1			mA
I_{DC}	Extra Available Current when Muted at the Same DC-voltage	I_{DC} = 15 – 100 mA		10		mA

* Adjustable to both higher and lower values with external components.

Figure 1 : Typical Application.



Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table.

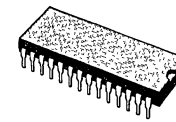
Type	R1	R2
No Regulation, all Feeding Systems	∞	0
48 V, 2 x 400 Ω	14.5 kΩ	47 kΩ
48 V, 2 x 200 Ω	18 kΩ	47 kΩ

SGS-THOMSON MICROELECTRONICS

TEA7037

SPEECH AND TONE CIRCUIT

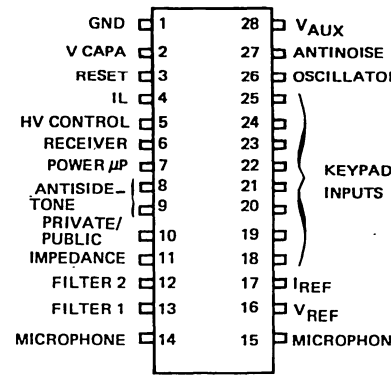
- AUTOMATIC LINE LENGTH RECEIVING AND SENDING GAIN CONTROL
- AUTOMATIC LINE LENGTH TRACKING ANTI-SIDETONE SYSTEM
- ADJUSTABLE MICROPHONE AND EAR-PHONE AMPLIFIER GAIN
- MEETS FRENCH VOLTAGE/CURRENT LIMI-TATIONS IN SPEECH AND RING MODE
- ADAPTED TO EVERY KIND OF EARPHONE TRANSDUCER
- MUTE IN EMISSION AND RECEPTION
- PABX POSITION
- TWO KEYS ROLL OVER PROVIDED
- ADJUSTABLE OUTPUT TONE LEVEL
- CLICK FREE SWITCH OVER FROM SPEECH TO DIALING MODE & VICE-VERSA



DIP-28

ORDER CODE : TEA7037DP

PIN CONNECTION



DESCRIPTION

Specially designed for telephone set applications this 28 pins IC provides :

a) Transmission and line adaptation

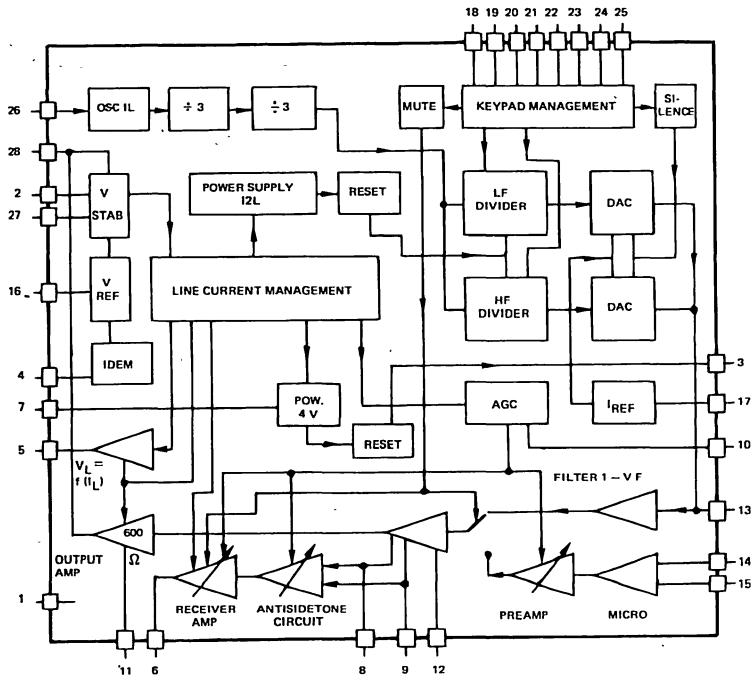
b) F.V. generation

c) Power supply for peripherals

d) Interface with MCU

It meets the French Specifications for handset ho-mologation level 1.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{cse}	Supply Voltage	8.5	V
P_{tot}	Power Dissipation	800	mW
T_{oper}	Operating Temperature Range	– 25 to 65	°C
T_{stg}	Sorage Temperature Range	– 55 to 150	°C

PIN DESCRIPTION

N°	Name	Description
1	G_{ND}	Ground
2	V_{capa}	C7 : Voltage Stabilizer Filtering Capacity
3	Reset	Microprocessor Reset
4	I_L	R17/C6 Sets Call Frame Width
5	H_V Control	Output Controlling HV Stage
6	Receiver	Receiver Output
7	Power Up	Stabilized Power for Peripheral Circuits
8	Antisidetone	Antisedone Network Input for Long Lines (3.5km)
9		Antisedone Network Input for Short Lines (0.5km)
10	Private/Public	Gain Control Inhibition with Respect to line Length
11	Impedance	R7 Sets Dynamic Impedance
12	Filter 2	Second Filter Input for Voice Frequencies
13	Filter 1	First Filter Input for Voice Frequencies
14-15	Microphone	Microphone
16	V_{ref}	Reference Voltage
17	I_{ref}	R9 Sets Internal Source Reference Current
18	Keypad Inputs	" D " 941 Hz Logic Input
19		" C " 852 Hz Logic Input
20		" B " 770 Hz Logic Input
21		" A " 697 Hz Logic Input
22		" E " 1209 Hz Logic Input
23		" F " 1336 Hz Logic Input
24		" G " 1477 Hz Logic Input
25		" H " 1633 Hz Logic Input
26	Oscillator	Oscillator Input
27	Antinoise	C8 Decreases Line Noise Level
28	V_{aux}	V_{CC} : Low Voltage LIne

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_C	Stabilized Voltage (pin 2)	I_L = 28mA (see figs. 9, 10)	2.6	2.8	2.95	V
I_{DEM}	Charging Current(pin 2)			2.6		mA
I_r	Line Current Regulation for HV Control (pin 5)	Pin 4 = Pin 2 = GND I_L = 150mA I_L = 105mA	150		 5	µA
		Pin 4 ON ; Pin 2 = GND I_L = 75mA	150			µA
		Pin 4 ON ; Pin 2 ON I_L = 60mA I_L = 16mA	150		 100	µA nA
I_r/I_L		28mA < I_L < 50mA	0.9	1.0	1.1	µA/mA
I_{int}	Internal Bias Current (pin 28)	I_L = 28mA ; (see figs. 9, 10) R9 = 16.2KΩ (V_{28} = R6 * I_{int} + V_C)	470	510	550	µA
V_{ref}	Reference Voltage	I_L = 28mA	1.35	1.42	1.49	V
I_{ref}	Current at V_{ref}		− 10		100	µA
V_{MP}	Stabilized Supply at Pin 7	(see fig. 11)	3.7	4	4.2	V
I_{CMP}/I_{LI}	Charging Current at Pin 7	Pin 4 = Pin 2 = GND I_{L1} = I_L − I_{dem} (note 2)	0.7			mA/mA
I_{SMP}	Static Current at Pin 7	I_L = 6 mA I_L > 25 mA I_L > 25 mA + AC	0.5 3.15 1.6	– 3.5 1.75	– – –	mA mA mA
I_{IMP}	Internal Consumption	(see fig. 11)	90	110	130	µA

RESET MICROPROCESSOR (see fig. 12)

V_{RH}	High Threshold		0.82 x V_{PM}			V
V_{RB}	Low Threshold		2.83		0.805 x V_{PM}	V
V_{RSH}	Output High	Reset = 1	0.9 x V_{PM}			V
V_{RSB}	Output Low	Reset = 0			0.1 x V_{PM}	V

AC CHARACTERISTICS (see figs. 12, 13, 14 and 15)

G_{EL} G_{EC}	Tx Gain at Long Line Tx Gain at Short Line	I_L = 28 mA I_L = 44 mA	54 47	55 49	56 51	dB dB
DE	Distortion in I_x	I_L = 28 to 44 mA V_L = 1.5 dBm V_L = 4 dBm			 3 10	 % %
Z_E	Microphone Input Impedance	Symmetric Mode	1.82	2.15	2.47	KΩ
B_{EP}	Tx Psophometric Noise	Z_{IN} = 2 K ; I_L > 28 mA		− 69		dBmp
R_E	Tx Attenuation M.F. and Silence Modes	I_L > 28 mA	60			dB
CM_{RR}	Common Mode Rejection Ratio			60		dB

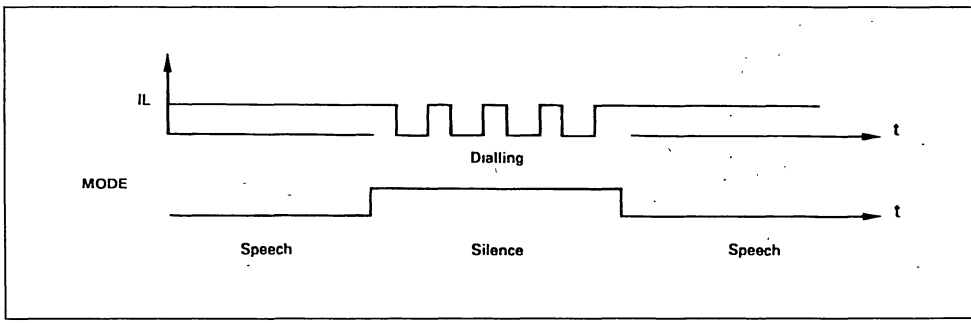
ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Unit
G_{RL} G_{RC}	Rx Gain at Long Line Rx Gain at Short Line	I_L = 28mA I_L = 44mA	28.5 27.5	29.5 23.5	30.5 25.5	dB dB
D_R	Distortion in R_x	I_L = 28 to 44mA V_{EC} = 440mV V_{EC} = 790mV			 3 10	 % %
B_{RP}	R_x Noise	I_L > 28mA ; R_{EC} = 600Ω		– 74		dB mp
G_{AL}	Side Tone at Long Line	I_L = 28mA	22			dB
G_{AC}	Side Tone at Short Line	I_L = 44mA	26			dB
Z_{AC}	AC Impedance	I_L > 28mA	500	600	700	Ω

DTMF GENERATOR (see fig. 16)

D_{FV}	Frequency Dispersion		– 0.5	–	+ 0.5	%
N_{FB}	Low Frequency Group		– 10	–	– 6	dBm
N_{FH}	High Frequency Group		– 8	–	– 4	dBm
P_{FV}	Pre-Emphasis		1	2	3	dB
C_{FV}	Voice Frequency Monitoring		28	35	42	dB

In pulse dialling the receiver mute is the silence mode.



FUNCTIONAL DESCRIPTION

- Logic inputs equivalent diagrams

LOGIC TABLE - KEYBORD MODE

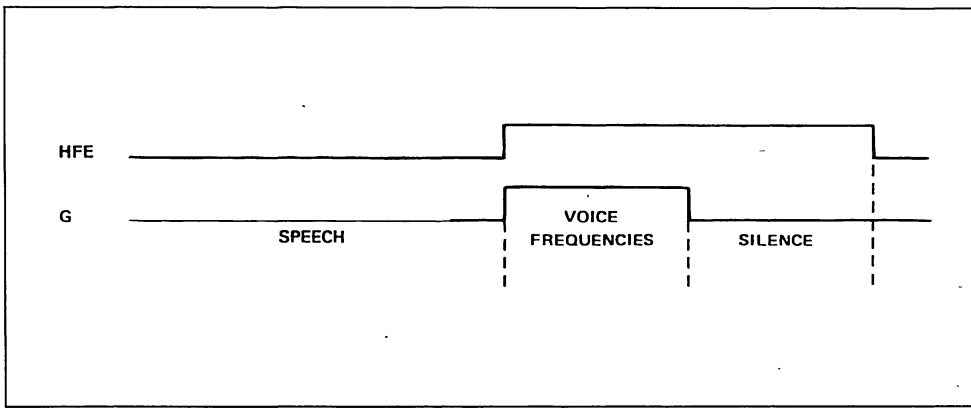
Symbol	Inputs								Voice Frequencies (Hz)	Mute	Notes
	A	B	C	D	E	F	G	H			
–	H	H	H	H	L	L	L	L	–	Off	a
–	L	H	H	H	L	L	L	L	697	On	b
–	H	L	H	H	L	L	L	L	770	On	
–	H	H	L	H	L	L	L	L	852	On	
–	H	H	H	L	L	L	L	L	941	On	
–	H	H	H	H	H	L	L	L	1209	On	c
–	H	H	H	H	L	H	L	L	1336	On	
–	H	H	H	H	L	L	H	L	1447	On	
–	H	H	H	H	L	L	L	H	1633	On	
"1"	L				H				697 + 1208	On	d
"2"	L					H			697 + 1336	On	
"3"	L						H		697 + 1477	On	
"A"	L							H	697 + 1633	On	
"4"		L			H				770 + 1209	On	
"5"		L				H			770 + 1336	On	
"6"		L					H		770 + 1477	On	
"B"		L						H	770 + 1633	On	
"7"			L		H				852 + 1209	On	
"8"			L			H			852 + 1336	On	
"9"			L				H		852 + 1477	On	
"C"			L					H	852 + 1633	On	
"*"				L	H				941 + 1209	On	
"0"				L		H			941 + 1336	On	
"#"				L			H		941 + 1477	On	
"D"				L				H	941 + 1633		

Notes : a. Conversation mode.
b. Test mode.
Low frequencies.
c. Test mode.
High frequencies.
d. If one of inputs E, F, G, H, is high, the others are low.
If one of inputs A, B, C, D, is low, the other are ligh.

LOGIC TABLE - MICROPROCESSOR MODE

Symbol	Inputs								Voice Frequencies (Hz)	Mute	Notes
	A	B	C	D	E	F	H	G			
–	H	H	H	H		L		L	–	Off	e
–	X	X	X	X		H		L	–	On	f
" 1 "	H	H	H	H		H		H	697 + 1209	On	
" 2 "	H	H	H	L		H		H	697 + 1336	On	
" 3 "	H	H	L	H		H		H	697 + 1477	On	
" A "	H	H	L	L		H		H	697 + 1633	On	
" 4 "	H	L	H	H		H		H	770 + 1209	On	
" 5 "	H	L	H	L		H		H	770 + 1336	On	
" 6 "	H	L	L	H		H		H	770 + 1477	On	
" B "	H	L	L	L		H		H	770 + 1633	On	
" 7 "	L	H	H	H		H		H	852 + 1209	On	
" 8 "	L	H	H	L		H		H	852 + 1336	On	
" C "	L	H	L	L		H		H	852 + 1477	On	
"C"	L	H	L	L		H		H	852 + 1633	On	
" * "	L	L	H	H		H		H	941 + 1209	On	
" 0 "	L	L	H	L		H		H	941 + 1336	On	
" # "	L	L	L	H		H		H	941 + 1477	On	
" D "	L	L	L	L		H		H	941 + 1633	On	

Notes : e. Conversion mode.
f. Silence setting.



PUBLIC / PRIVATE

When a resistor is inserted between pin 10 and ground, the transmission and receiving efficiency control and antisidetone variation are inhibited with respect to line current.

The transmission and receiving gains may vary from G_{max}(gel) to G_{max} 6 dB (Gec) with respect to the resistance value.

The equivalent antisidetone is related to the gain set by RI_p

Figure 1 : Transmission and Receiving Gain Attenuation.

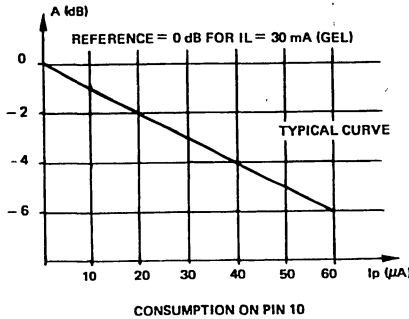


Figure 2 : Equivalent Antilocal Network.

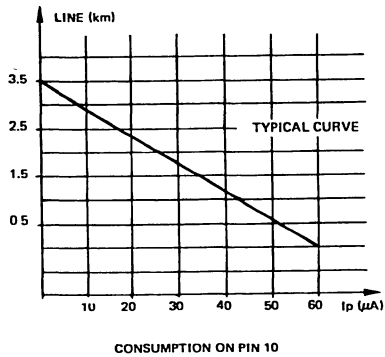
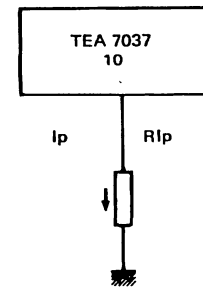


Figure 3 .



$$RIp \text{ In MW} = \frac{7.8}{Ip\mu A}$$

For RIp = 390K to 1%
DG = – 2dB ± 0.4dB

Figure 4.

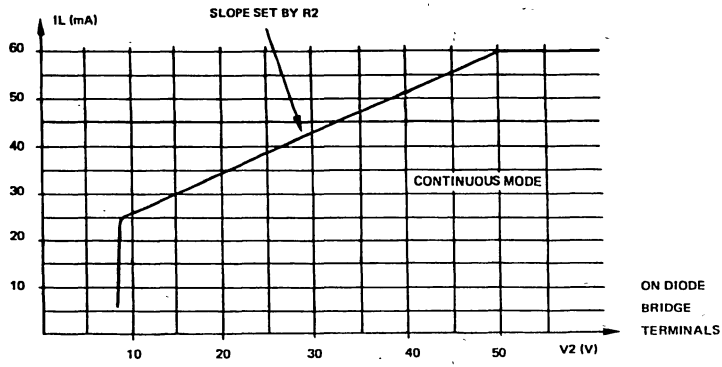


Figure 5.

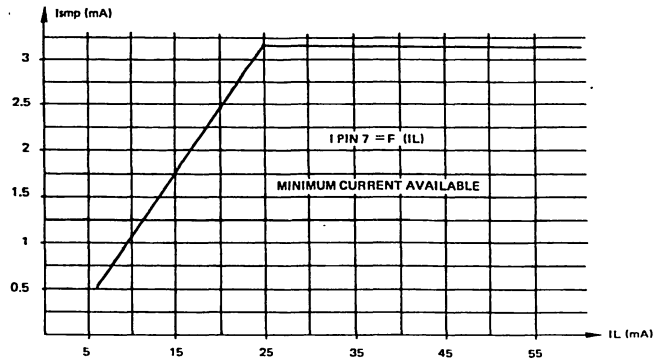


Figure 6.

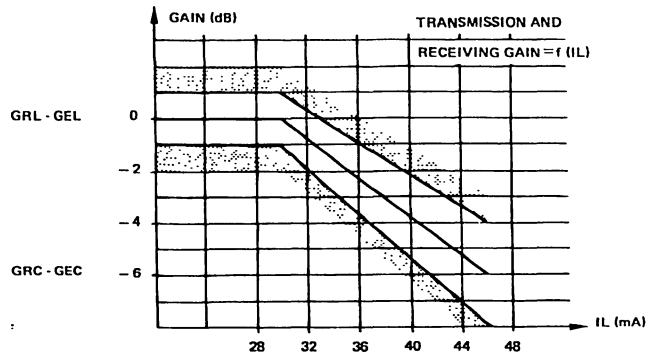
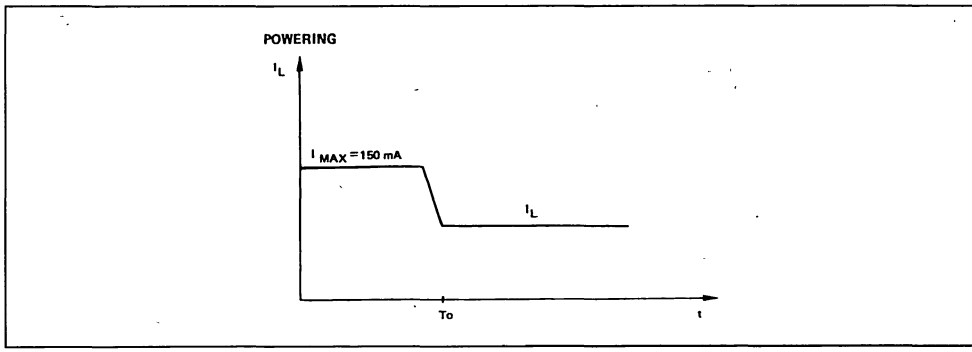


Figure 7 : To it set by : R17 · C6 (pin 4) or C7 (pin 2).

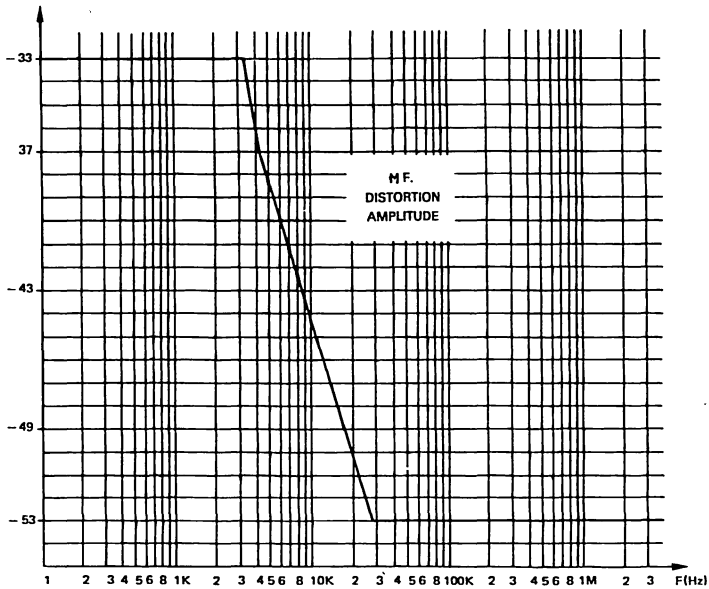


The TEA can stand the capacitive loads an all its pins, except pin 26 (oscillator).

It is obvious that these capacites can change the circuits alterning and/or transient behavior.

Pin	Name	Max. Value (grounded)	Comments
1	Ground		
2	V_{capa}	220µF	
3	Reset	470µF	
4	I_L = 120 or 60ms	2.2µF	
5	H_V Control	Few nF Max.	In parallel with the capacitor across pin 28 and pin 1, hence changes impedance & circuit time constants.
6	Receiver	100nF Max.	In Parallel on the Receiver
7	Pow µP	470µF	
8 9	Anti Local	10nF	Receiver Signal Filter
10	Private/Public	47nF	
11	Impedance	33 pF Max.	Provides a high pass, hence increases DTMF harmonics & noise above cut-out frequency.
12	Filter 2	Few pF Max.	Changes Refilter Impedance & Time CS[t]
13	Filter 1	82nF	Should not be changed (preephasis).
14 15	Microphone	100nF	
16	V_{REF}	10µF	
17	I_{REF}	680pF Max.	
18 19 20 21 22 23 24 25	Keyboard Inputs	10nF Max.	Bear Time Constants in Mind
26	Oscillator	NO	
27	Antinoise	2.2nF	
28	Vaux	Few nF	Cf. Comment Pin 5

Figure 8 : DTMF Harmonic Distortion vs. Frequency.



COMPONENTS VALUES (for figures 9 to 16)

R1	10Ω	C1	2.2nF
R2	12MΩ	C2	4.7nF
R3	100kΩ	C3	1nF
R4	4.7MΩ	C4	100µF
R5	220kΩ	C5	.
R6	5.9kΩ	C6	.
R7	.	C7	.
R8	.	C8	.
R9	16.2kΩ	C9	/ 1µF
R10	.	C10	/ 1µF (depending on µP)
R11	.	C11	68nF
R12	.	C12	1µF
R13	.	C13	= 6.8nF
R14	220kΩ	C14	– 3.3µF
R15	845Ω	C15	– 2.2nF
R16	220Ω	C16	– 2.2nF
R17	820kΩ	C17	= 10µF
R18	75Ω	C18	= 2.2µF
RIP	390kΩ	C19	= 470nF
RuP	5.6kΩ		
Zec	– 220Ω	D1	ZENER 15V
		D2	BAT43
T1	MJE340	D3	BAT43
T2	PBF259		
T3	PBF493S	QUARTZ	3.58MHz

- ZL = 600W

- R7	= 0	- C5	= 27pF
- R8	= 124kΩ	-C6	= 1nF
- R10	= 0	-C7	= 27pF
- R11	= 124kΩ	-C8	= 1nF
- R12	= 3.9kΩ		
- R13	= 3.9kΩ		

- 0.4mm France cable varying between 0km and 3.5km.

- R7	56kΩ	- C5	= 560pF
- R8	124kΩ	- C6	= 4.7nF
- R10	10kΩ	- C7	= 100pF
- R11	115kΩ	- C8	= 2.2nF
- R12	4.99kΩ		
- R13	3.6kΩ		

- R12 and R13 enable reception gain adjustment for adaptation to various transducers/
- R16 enable transmission gain equipment for adaptation to various transducers.

Figure 9 : V_C. I_{int}. V_{ref}.

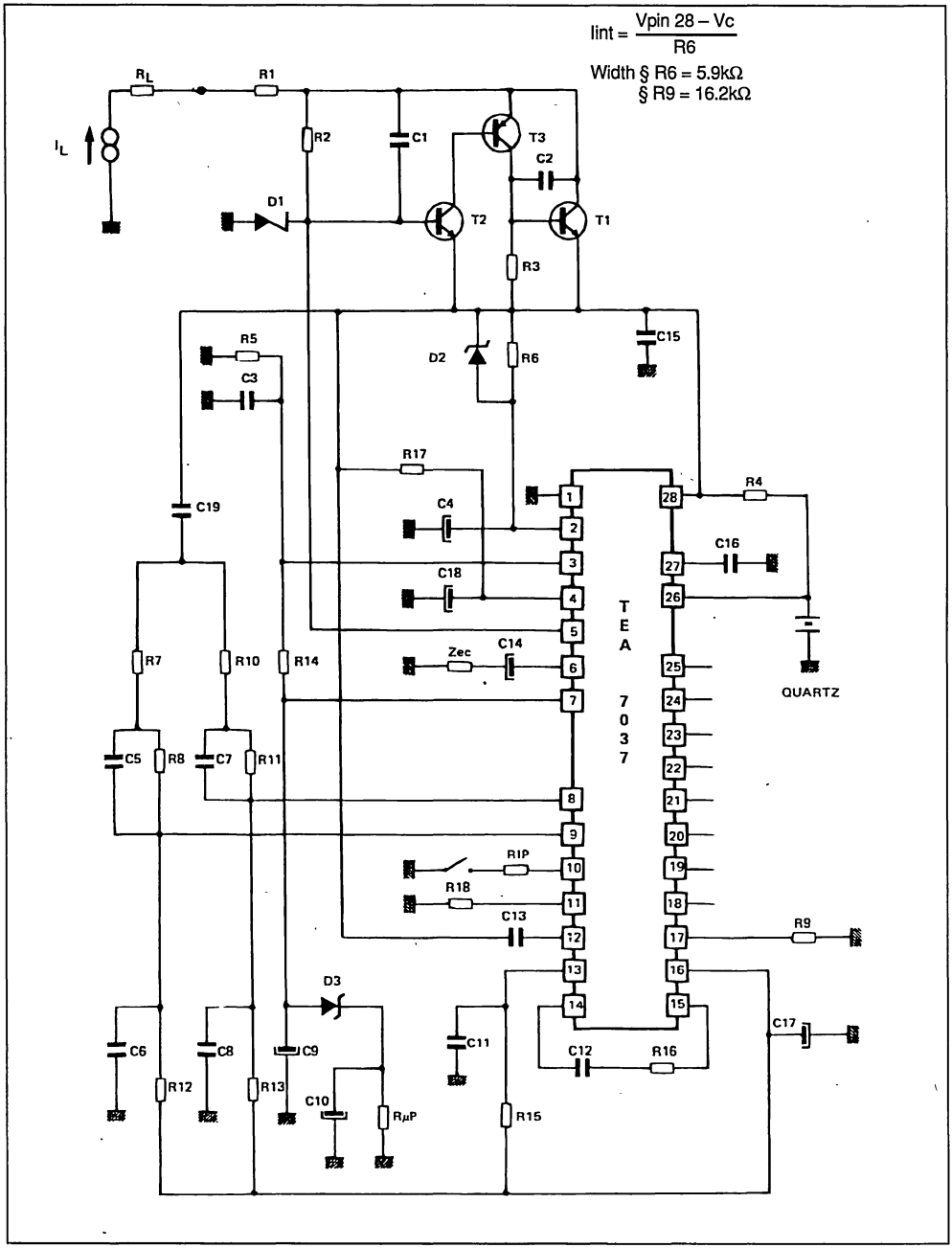


Figure 10 : Idem I_r.

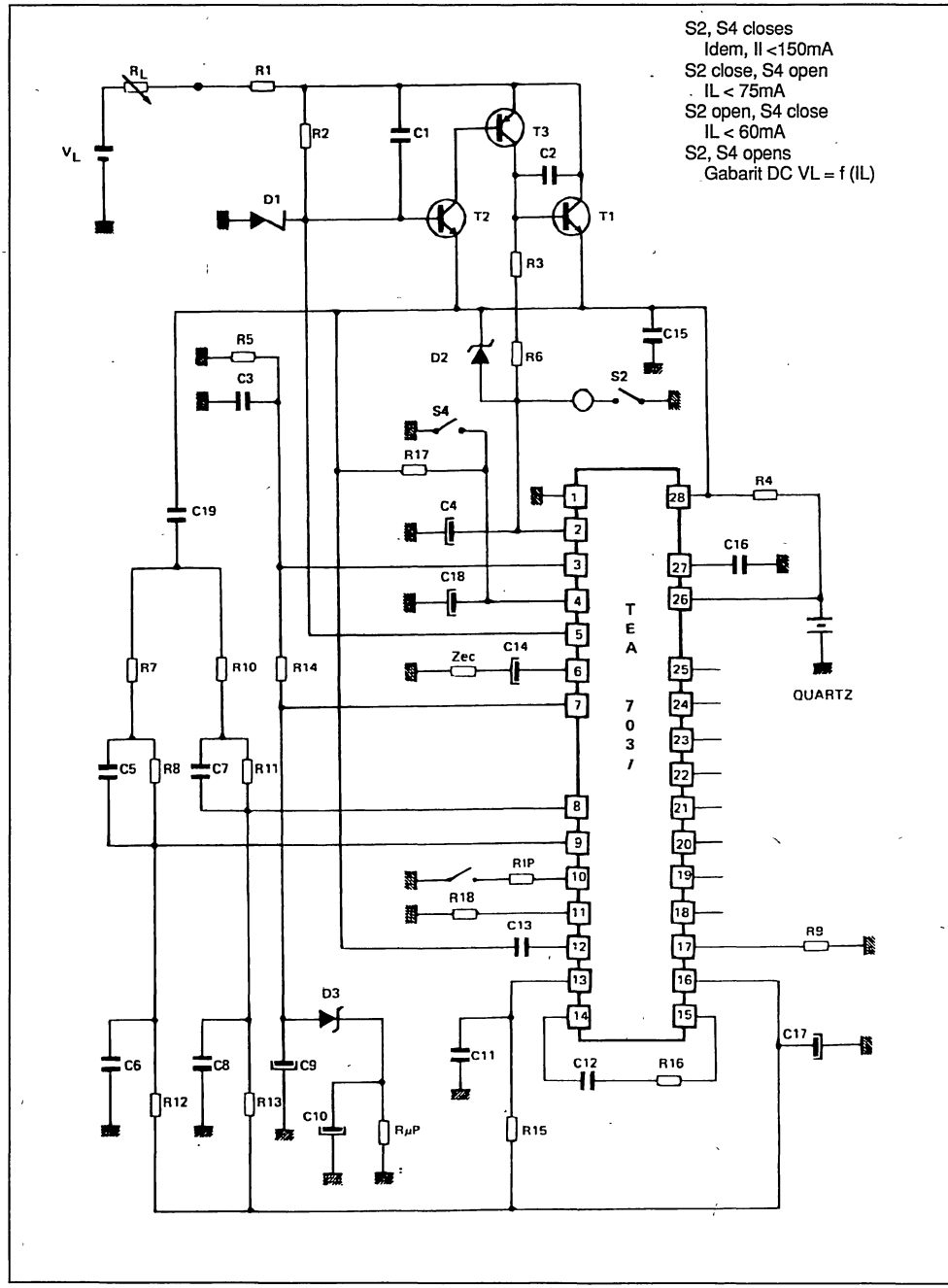


Figure 11.

Icmp, Vmp, Ismp, Iimp,
Vrh, Vrb, Vrsh, Vrsb.
S2, S4, S7 closes
Icmp
S2, S4, S7 opens
Vmp, Ismp
Limp by the time discharge of C9
when the line power is cut off.

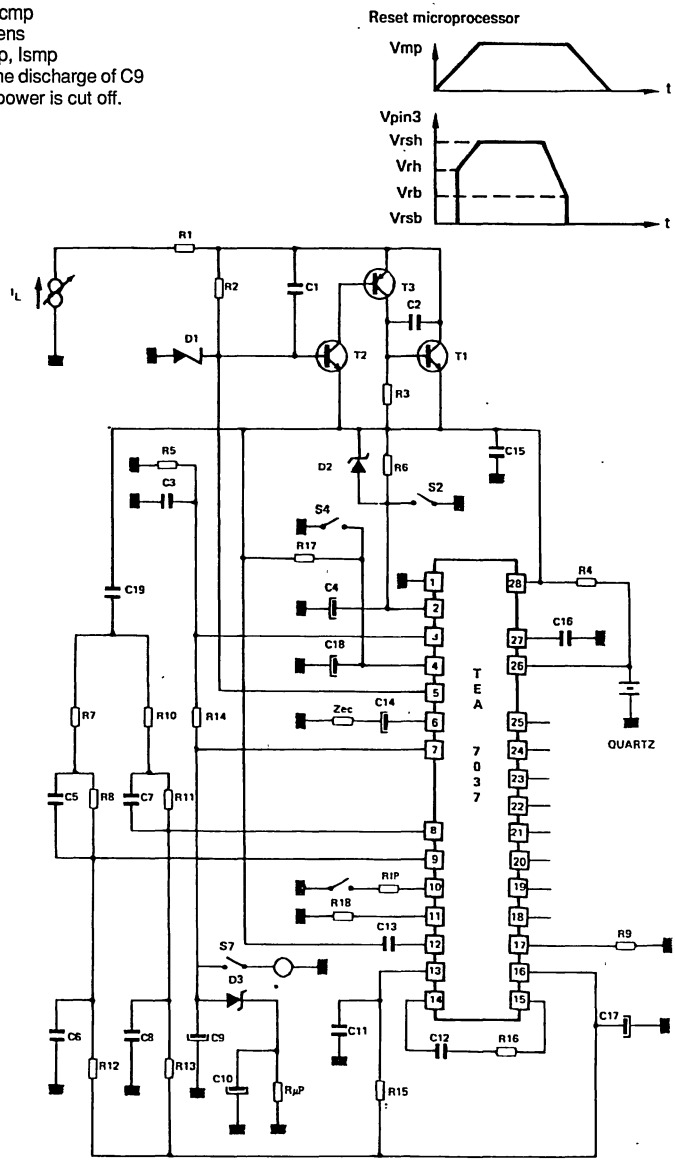


Figure 12 .

Gel. Gec. Re. De. Bep.

S1 open

$$(Gel, Gec) = 20 \log \frac{VL}{VM}$$

$$Re = 20 \log \frac{VL\ (S1\ open)}{VL\ (S1\ close)}$$

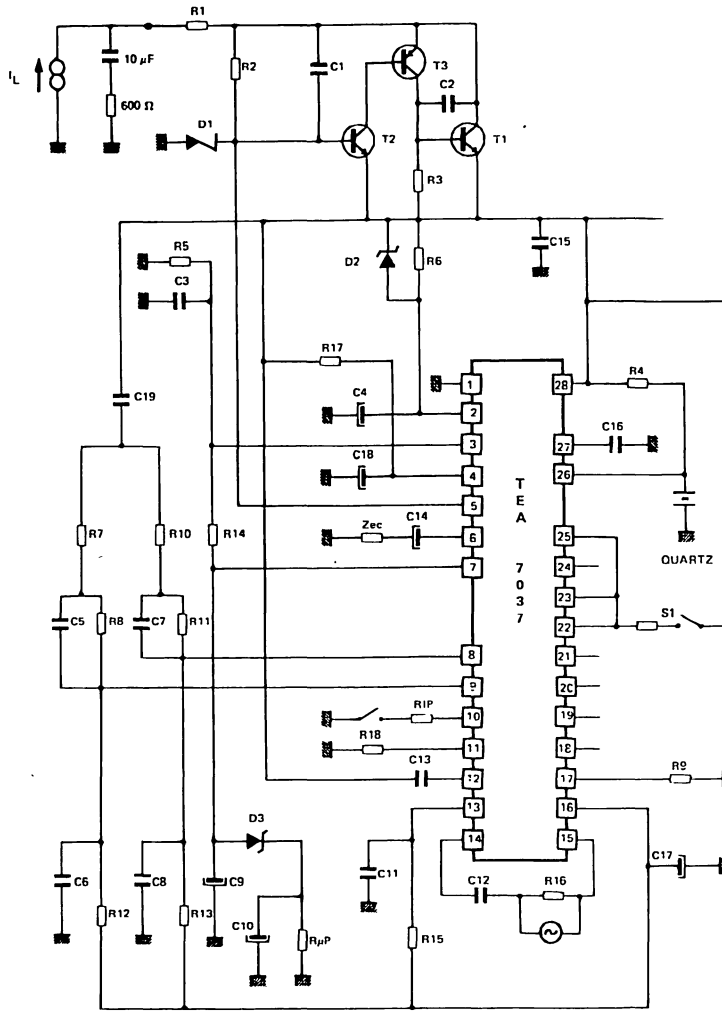


Figure 13 .

Grl, Grc, Dr, Brp,

$GRL = 20 \log \frac{Vpin6}{Vpin8}$

$Grc = 20 \log \frac{Vpin6}{Vpin9}$

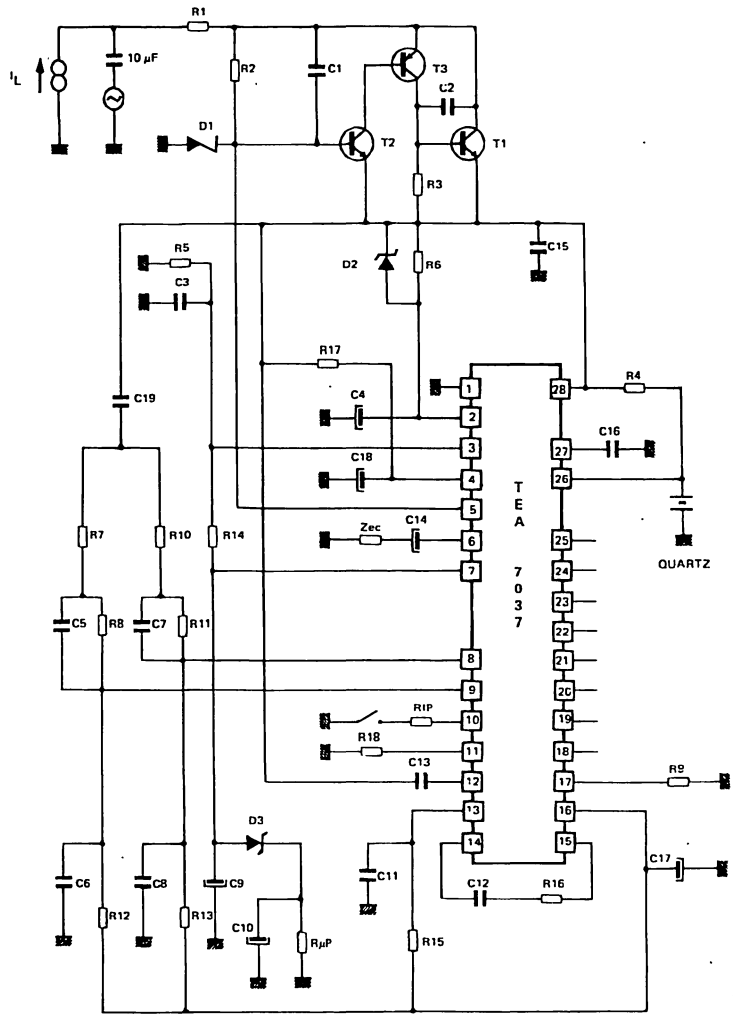


Figure 14 .

Gal, Gac

$$(Gal, Gac) = 20 \log \frac{Vpin28}{Vpin6}$$

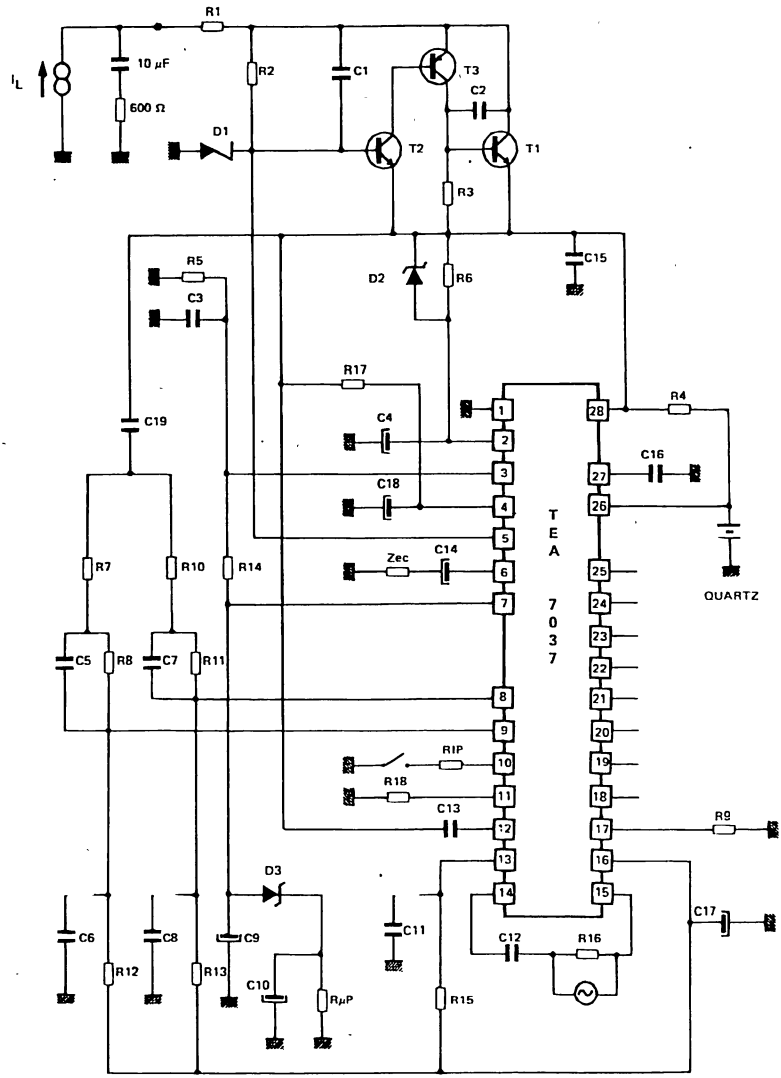


Figure 15 .

Zac

$$Zac = RL1 \times RL2 \frac{VL2 - VL1}{VL1 \times RL2 - VL2 \times RL1}$$

VL1 for RL1 = 300Ω
VL2 for RL2 = 600Ω

$$Zac = 600 \times \frac{VL2 - VL1}{2VL1 - VL2}$$

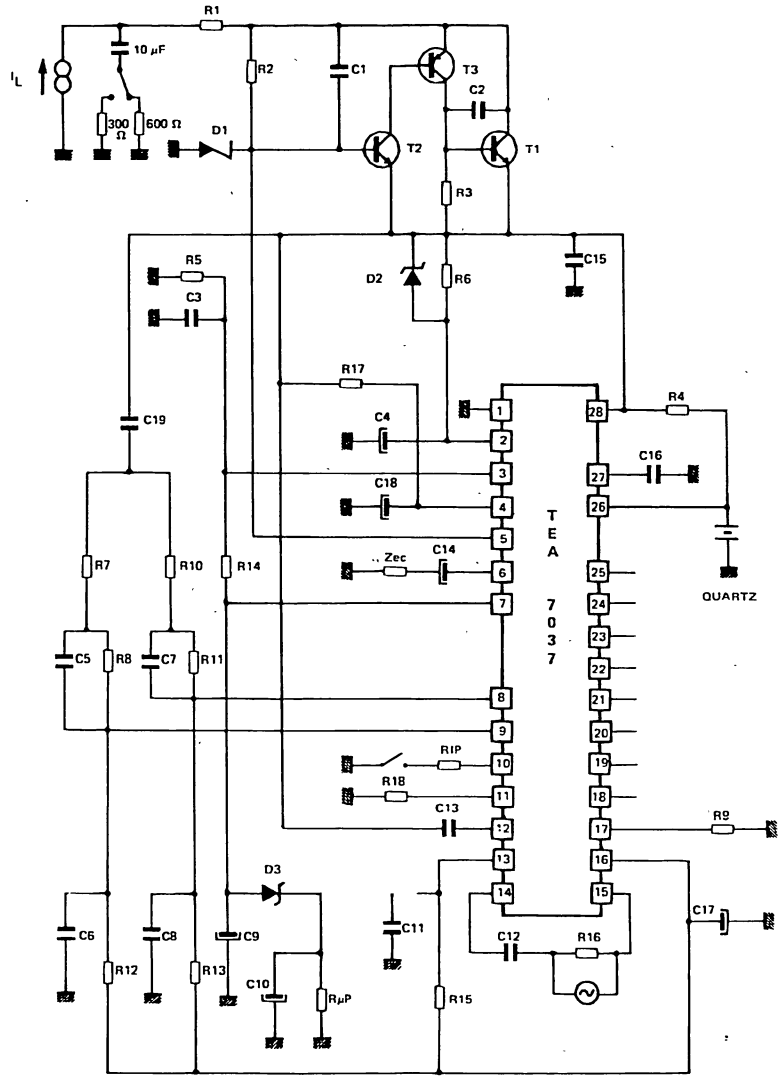
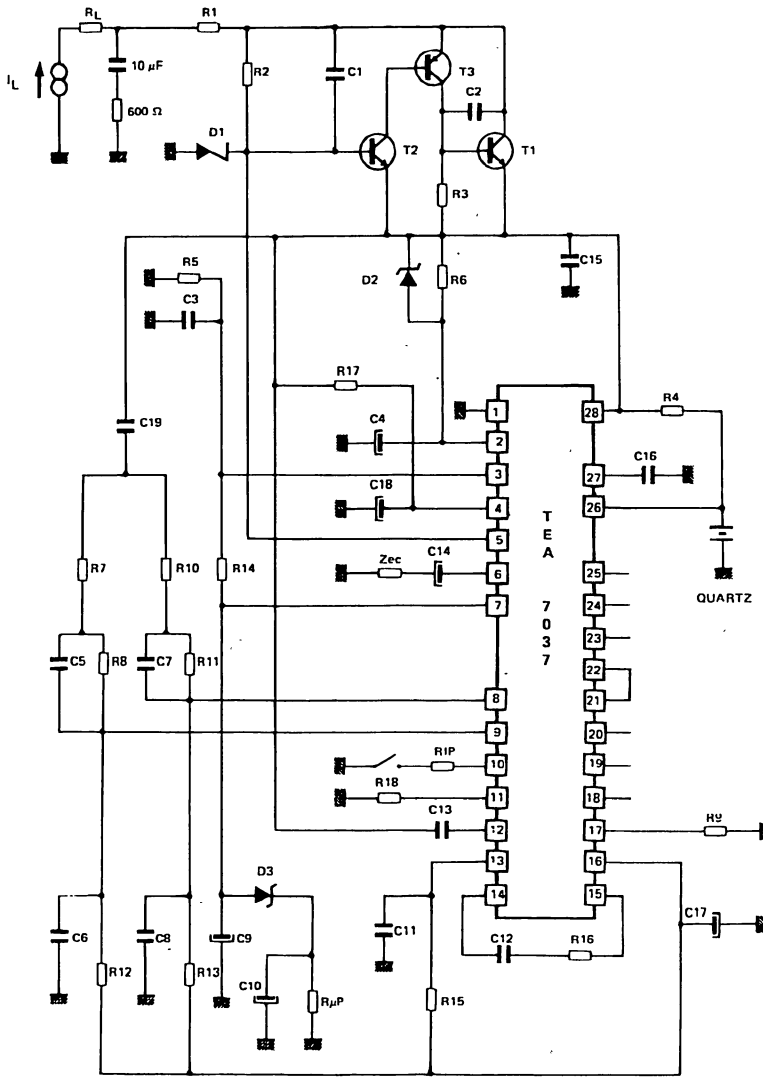


Figure 16 .

Nfb, Nfh, Pfv, Cfv,

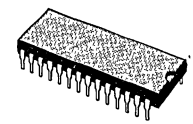
697Hz + 1 209Hz
Level and preemphasis are measured on pin 28

$$Cfv = 20 \log \frac{Vpin28}{Vpin6}$$

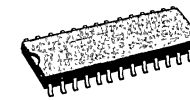


HIGH RANGE SPEECH CIRCUIT WITH SQUELCH FUNCTION

- 2/4 WIRES INTERFACE WITH
  - DOUBLE ANTISIDETONE NETWORK
  - MICROPHONE NOISE THRESHOLD (squelch)
  - RX GAIN AND AC IMPEDANCE EXTERNALLY PROGRAMMABLE
- DTMF INTERFACE
- PULSE DIAL INTERFACE
- 3.25 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- RESET TO MICROPROCESSOR
- CURRENT SUPPLY FOR LOUDSPEAKER
- HANDS-FREE INTERFACE
- DC CHARACTERISTIC AND ON/OFF HOOK FOR FRANCE
- CONTROL AGAINST HIGH VOLTAGE TRANSIENTS



DIP28



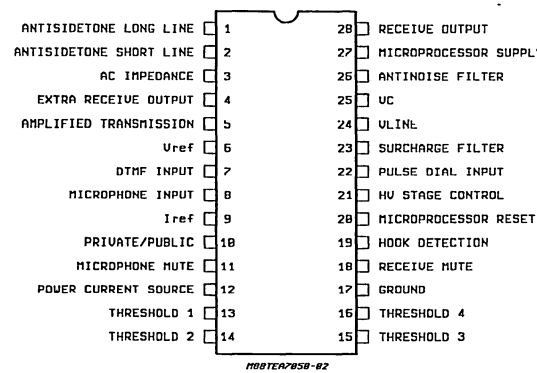
SO-28

ORDER CODES : TEA7050DP (DIP28)
TEA7050D (SO-28)

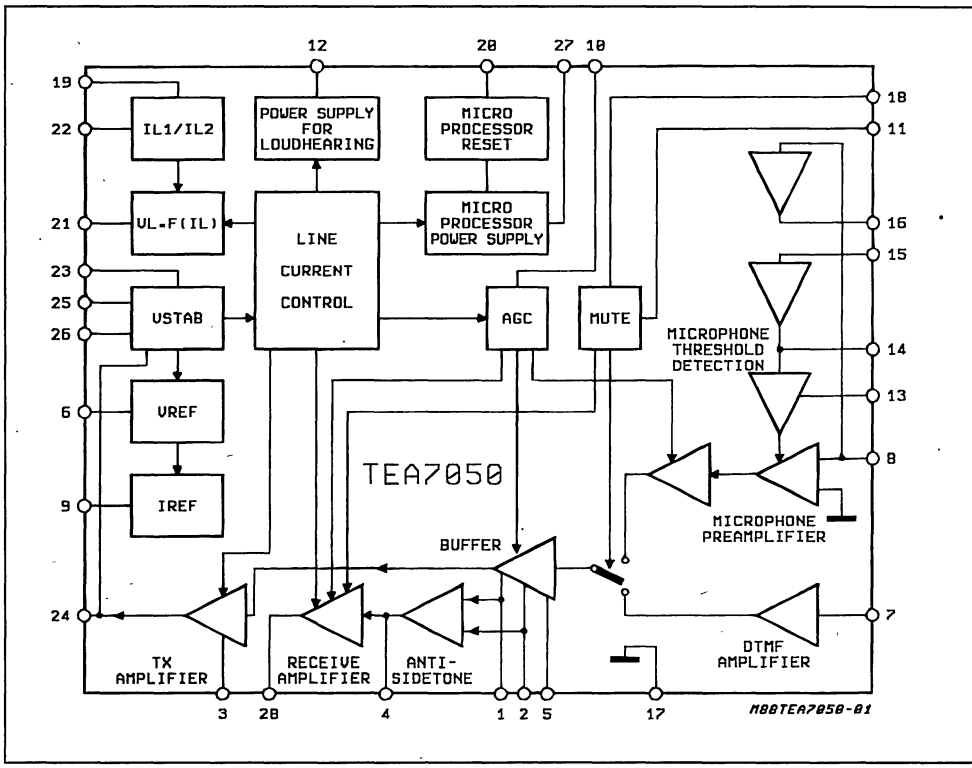
DESCRIPTION

The TEA7050 is expressely designed to meet the french specification for telephone set in high range equipments.

PIN CONNECTION (top view)



BLOCK DIAGRAM



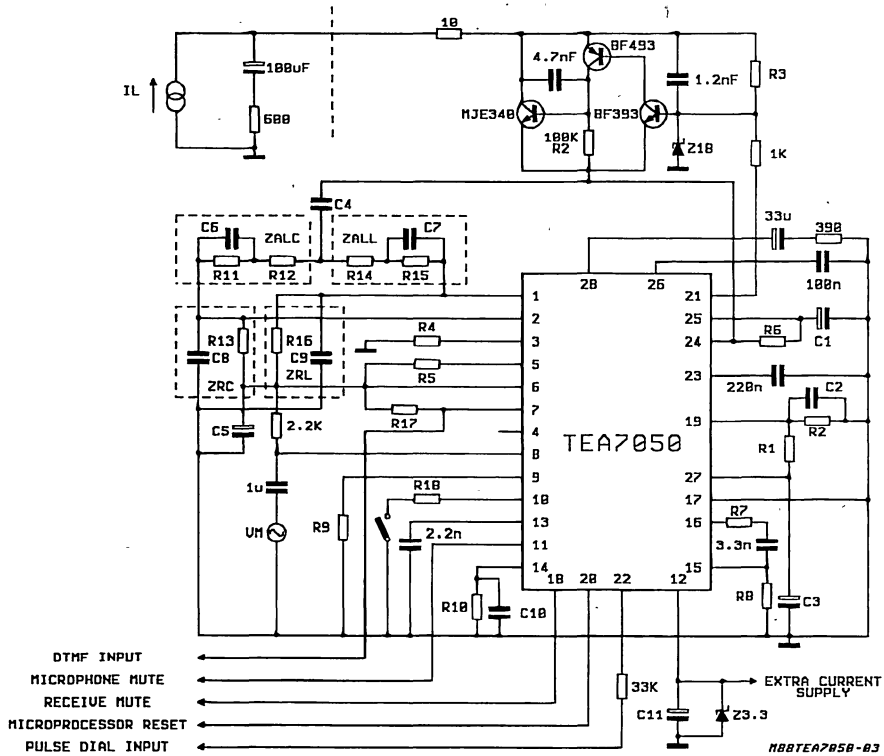
ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vc	Stabilized Voltage (pin 25)	II = 27mA	2.6	2.8	2.95	V
Idem	Charging Current (pin 25)	II = 27mA		2.6		mA
Ir	Line Current Regulation for HV Control (pin 21)	Pin 19 = Pin 25 = GND II = 150mA II = 100mA	150		 5	µA
		Pin 19 ON ; Pin 25 = GND II = 75mA	150			µA
		Pins 19 and 25 ON II = 60mA II = 16mA	150		 100	µA nA
Ir/II		27mA < II < 50mA	0.8	0.9	1.0	µA/mA
Iint	Internal Bias Current (pin 25)	II = 27mA ; R9 = 26.7 Kohms ; (V24 = R6*Iint + Vc)	410	460	510	µA
Vref	Reference Voltage	II = 27mA	1.32	1.38	1.47	V
Iref	Current at Vref		– 10		100	µA
Vmp	Stabilized Supply at Pin 27		3.1	3.3	3.5	V
Icmp	Charging Current at Pin 27	Pin 19 = Pin 25 = GND IL1 = II – Idem	0.7 x x IL1			mA
Ispm	Static Current at Pin 27	II = 6mA II > 25mA	0.5 2.5	 2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Iea	Supply Current for Parallel Circuits (pin 12)	R9 = 26.7Kohm II = 10mA II = 27mA II = 42mA	 8 21	 3 9.5 23.5	 11 26	 mA mA mA
Vrh Vrb Vrsh Vrsb	Microprocessor Reset High Treshold Low Treshold Output High Output Low	 Reset = 1 Reset = 0	 0.845 0.76 0.9	 0.89 0.8	 0.84 0.1	 Vmp (pin 27)

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vmh Vmb	Mute Microphone (pin 11)	ON OFF	1.6		 0.8	V V
Vmh Vmb	Mute Earphone (pin 18)	ON OFF	2.7		 2.1	V V
Gel Gec	Tx Gain Long Line Tx Gain Short Line	Il = 27mA Il = 42mA	48.5 41.5	49.5 43.5	50.5 45.5	dB
DGe	Squelch Attenuation			– 9		dB
Vse	Squelch Switch-off Level on the Line	Il = 27mA	– 44	– 39	– 34	dBm
Gmf	DTMF Gain	Il = 27mA Pin 11 > 1.6V	33.5	34.5	35.5	dB
De	Tx Distortion	Il = 27 to 42mA Vl = 0dBm Vl = 3dBm			 3 10	 % %
Ze	Microphone Impedance		9.6	12	14.5	Kohm
Bep	Tx Noise (psophometric)	Il > 27mA 2K at Pins 6-8		– 71		dBmp
Re	Tx Attenuation in Mute Mode	Il = 27mA Pin 11 > 1.6V	60			dB
Grl Grc	Rx Gain Long Line Rx Gain Short Line	Il = 27mA Il = 42mA	29 22	30 24	31 26	dB
Dr	Rx Distortion	Il = 27 to 42mA Vec = 500mV Vec = 700mV			 3 10	 % %
Brp	Rx Noise	Il > 27mA		– 74		dBmp
Rc	Rx Attenuation in Mute Mode	Il = 27mA Pin 18 > 2.7V	60			dB
Gal	Antisidetone	Il = 27 to 42mA	– 22			dB
Zac	AC Impedance	Il > 27mA	500	650	800	ohm
Grs	Confidence Level Vrec/Vmf	Pin 11 > 1.6V ; Pin 14 > 2.7V	28	31	34	dB

TEST CIRCUIT



R1 = 920KΩ
R2 = 820KΩ
R3 = 1.5MΩ
R4 = 75Ω
R5 = 5.1KΩ
R8 = 13KΩ
R9 = 26.7KΩ
R11 = 140KΩ
R12 = 8Ω
R13 = 2.7KΩ
R14 = 8Ω
R15 = 140KΩ
R16 = 2.7KΩ
R17 = 1.2 KΩ
R18 = 680KΩ for private complex

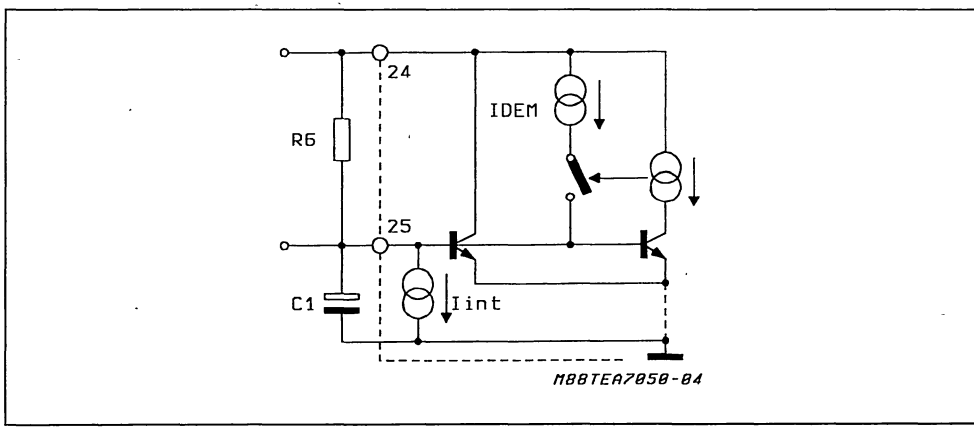
C1 = 188µF
C2 = 4.7µF
C3 = 10µF
C4 = 1µF
C5 = 100µF
C6 = 27pF
C7 = 27pF
C8 = 2.2nF
C9 = 2.2nF
C10 = 2.2µF
C11 = 220µF

CIRCUIT DESCRIPTION

1. DC-CHARACTERISTICS

1.1. VC (PIN 25). The stabilized voltage Vc is connected to Vline (pin 24) through an internal shunt regulator which presents to the line a high AC impedance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 25) must be not lower than 47 microFarad.

Figure 1.



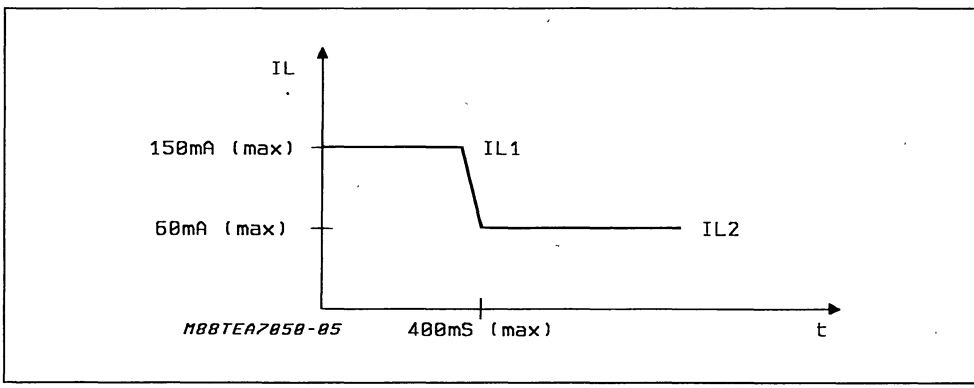
At "Off-hook", with only DC voltage applied to the line terminals, C1 fixes the timing of the line current profile at :

- 150mA max for a time shorter than 400msec (T-charge)
- 60mA max in steady state (conversation)

T-charge of 240msec (typ) is obtained with C1 = 220µF.

$$\text{T-charge} = \frac{Vc \times C1}{Idem} \text{ typically.}$$

Figure 2.



1.2. HOOK DETECTION (in ring mode) (pin 19). The DC-characteristic requested to allow off-hook detection by the exchange during ring call may be accomplished :

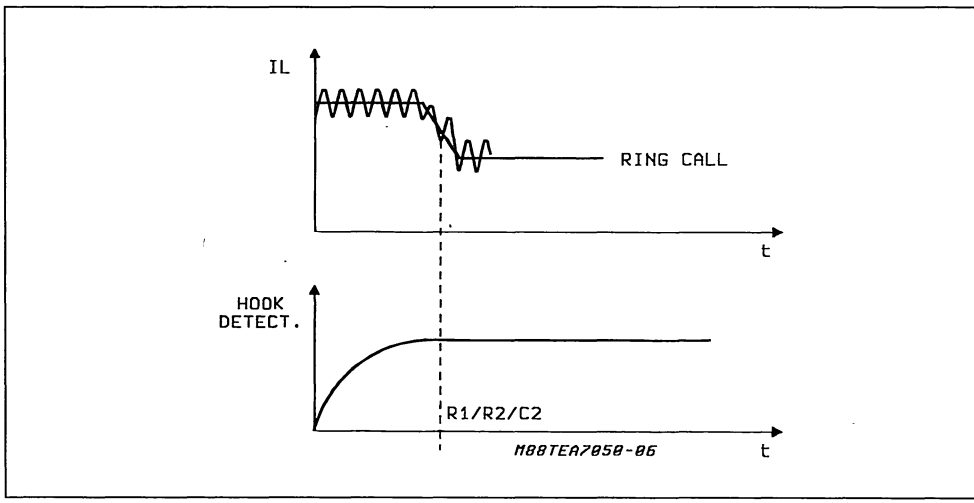
a) through an analog control (R-C) or
b) by a microprocessor.

a) Application with standard dialer (analog control) The components R1, R2 and C2 define the timing of the DC characteristic and also limit at 75mA-peak the line current during decadic dialing.

Optimum values are : - R1 x C2 = 1.8sec ; R2 x C2 = 0.8sec.

To reduce the minimum time between a "on-hook / off-hook" sequence, R2 may be replaced by a switch to ground.

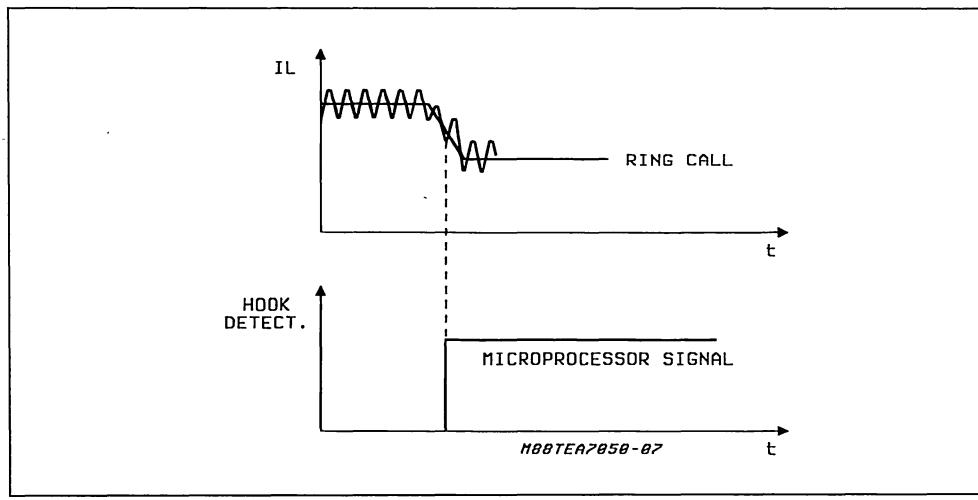
Figure 3.



b) Application with a microprocessor

Pin 19 may be controlled directly by the micro-controller, through a resistor R1b which replaces R1, R2 and C2.

Figure 4.



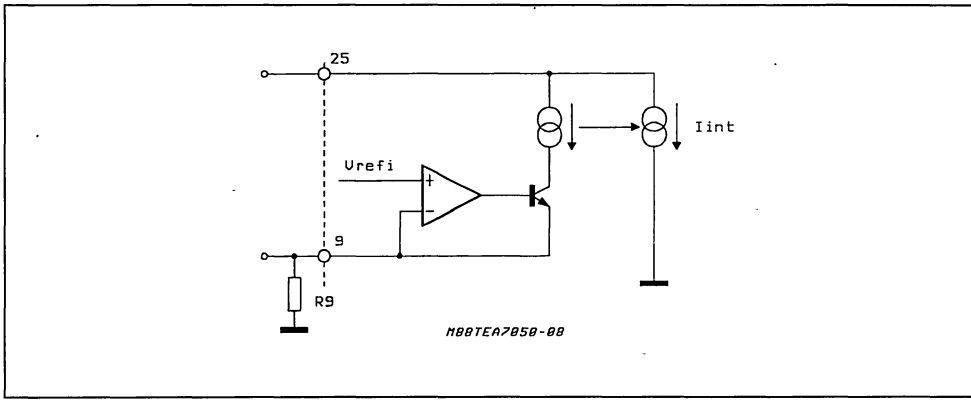
1.3. VLINE (PIN 24). The line voltage (pin 24) is determined by the value of the external resistor R6 and by the internal current, Iint, flowing between Vc (pin 25) and Ground (see also paragr. 1.1.) :

Vline = Vc + R6 x Iint.

Vc is fixed by design at about 2.8 volts.

Iint is reversely related to R9 (Iint = 12V / R9 at Iline = 27mA).

Figure 5.



Vline must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the french standards. At this purpose it is suggested that Vline equals 5.6 volts at Iline = 16mA. This typical value is obtained with R6 = 7.5Kohm.

1.4. HIGH VOLTAGE CONTROL STAGE (PIN 21). The behaviour of "HV control" is determined by several conditions, both internal (Iline sensor) and external (pins 19 and 25) with the purpose to accomplish the different DC characteristics and transitory conditions imposed by the French specification :

a) steady DC-characteristic and lightnings (pins 19 and 25 ON)

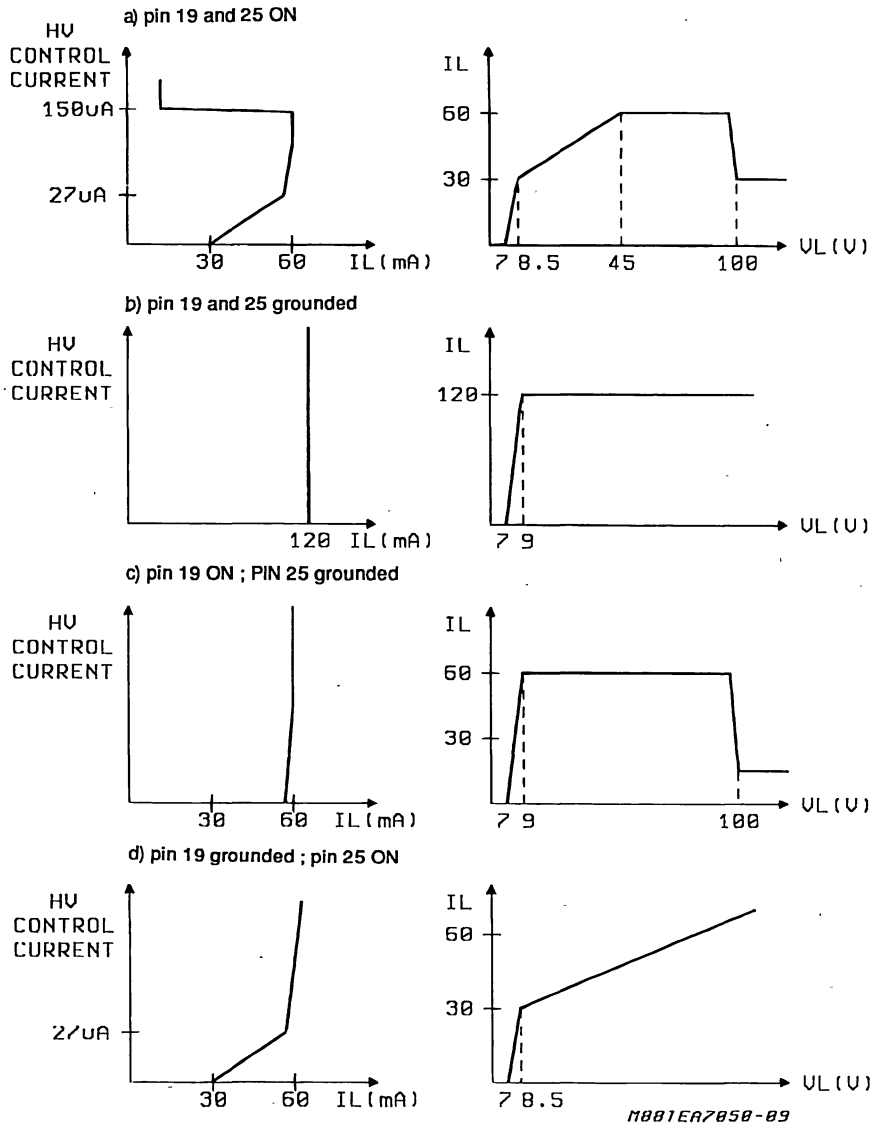
b) DC-characteristic at off-hook (pin 19 and 25 grounded)

c) DC-characteristic during decadic dialing (pin 25 grounded)

d) DC-characteristic after off-hook in ringing (pin 19 grounded)

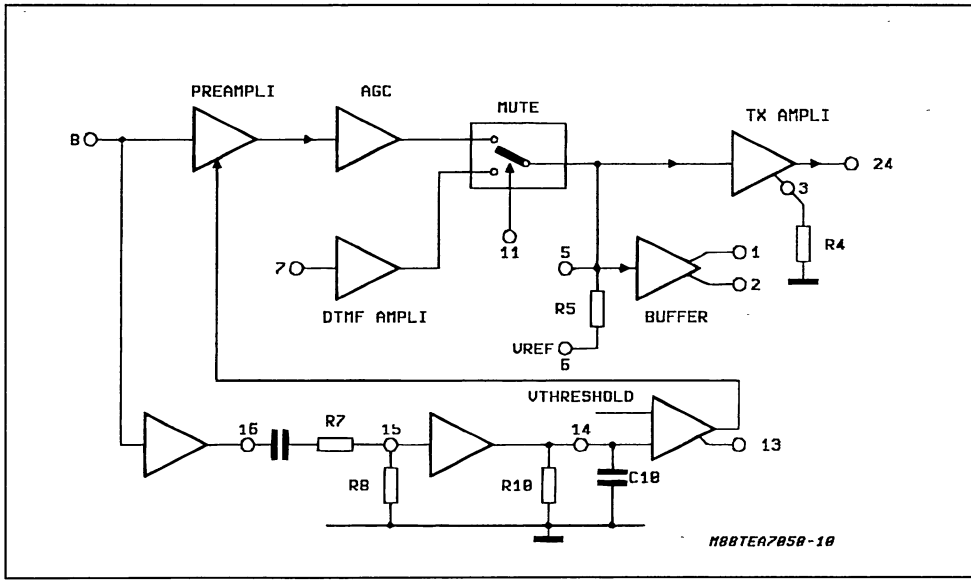
To do that, HV control pin regulates the current injected into the external high voltage transistor stage, requested by the French specification.

Figure 6.


a) pin 19 and 25 ON
HV CONTROL CURRENT
150uA
27uA
30
60
IL(mA)
IL
60
30
7
8.5
45
100
VL(V)
b) pin 19 and 25 grounded
HV CONTROL CURRENT
120
IL(mA)
IL
120
7
9
VL(V)
c) pin 19 ON ; PIN 25 grounded
HV CONTROL CURRENT
30
60
IL(mA)
IL
60
30
7
9
100
VL(V)
d) pin 19 grounded ; pin 25 ON
HV CONTROL CURRENT
27uA
30
60
IL(mA)
IL
60
30
7
8.5
VL(V)
M881EA7850-89

2. TRANSMISSION CHAIN

Figure 7.



2.1. A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 8) and Vline (pin 24) is internally decreased of 6dB when the line current varies from 27mA to 42mA with a constant AC load of 600ohms.

2.2. SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 at pin 3.

$$Zout = 10.65 \times Z4.$$

The total AC impedance shown to the line is the parallel

$$Zpar = Zout//Zint//Zext$$

where :

- Zint = 10kohm // 8.5nF (internal)
- Zext = R6 // C4 (at pin 24)

2.3. SENDING MUTE. In normal speech operation (Vmute 0.8V), the signal at Microphone Input (pin 8) is amplified to Vline (pin 24) with the gains Gec (short line), Gel (long line) or intermediate, depending on Iline.

In sending mute condition (Vmute 1.6V) these gains are reduced of at least 60 dB. In the same condition DTMF input (pin 7) is activated, with gain Gmf to the line independent from Iline.

2.4. ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented at pin 5 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2.).

2.5. NOISE THRESHOLD (SQUELCH). The microphone signal is highly amplified (46dB) at pin 16, then peak detected and compared with an internal threshold at pin 14.

If the peak so detected does not exceed the internal threshold, the comparator reduces of about 9dB the sending gain Ge, acting at the preamplifier level.

In this way a strong attenuation is obtained, both of the speech noise (about 4dB) and of the ambient noise (9dB).

The equivalent thresholds on the line are :

- minus 39dBm to switch from squelch to normal gain,
- minus 32dBm to switch from normal gain to squelch,

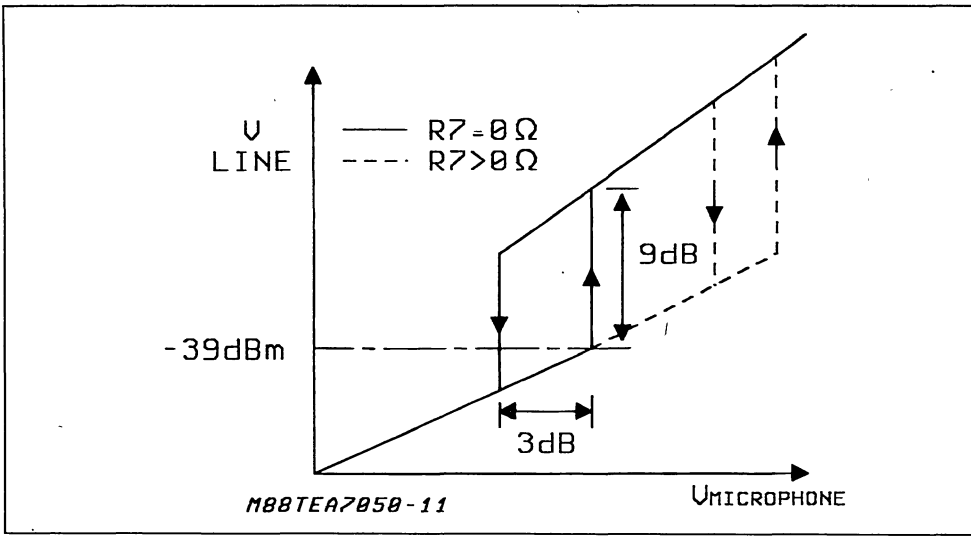
with R8=150KΩ from pin 15 to gnd and C=3.3nF from pin 16 to 15.

These thresholds can be increased inserting also a resistor (R7) in series to C between pin 16 and 15.

The variation is given by the formula : (R8 + R7)/R8.

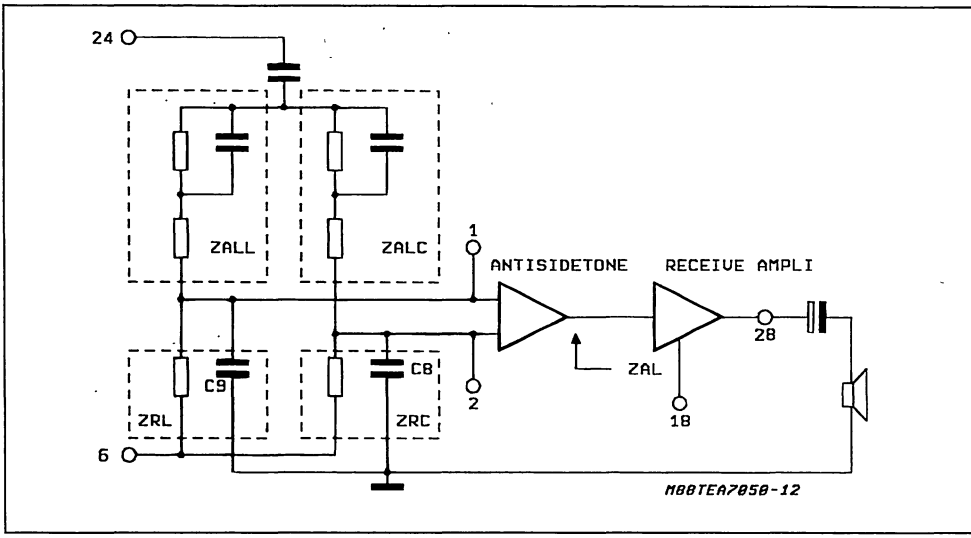
A hysteresis of about 3dB is defined to avoid continuous switch between squelch and normal gain.

Figure 8.



3. RECEIVE CHAIN

Figure 9.



3.1. A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 28, have a reduction of 6dB when Iline moves from 27mA to 42mA.

3.2. SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize sidetone both at long and short lines.

Before entering pins 1 and 2, the received signal is attenuated by two attenuating networks :

- Zall / Zrl to pin 1 for long lines sidetone compensation,
- Zalc / Zrc to pin 2 for short lines sidetone compensation.

Zrl and Zrc define the total receive gains :

a) $\frac{V\,28}{V24} = Grl \times \frac{Zrl}{Zrl + Zall}$ for long lines

b) $\frac{V\,28}{V24} = Grc \times \frac{Zrc}{Zrc + Zalc}$ for short lines

Zall and Zalc define the sidetone compensation of the circuit.

The equivalent balancing impedance is given by the formula :

$$Zal = K \times Zalc + (1\ K) \times Zall$$

where K = 0 at Iline = 27mA or lower (long line)

K varies from 0 to 1 with Iline between 27mA and 42mA,

K=1 at Iline=42mA or higher (short line).

Calculations to define Zall and Zalc are :

a) $Zall = 70 \times R5 \times \frac{Zline(long) \,//\, Zext \,//\, Zint \,//\, Zout}{Zout}$

b) $Zalc = 70 \times R5 \times \frac{Zline(short) \,//\, Zext \,//\, Zint \,//\, Zout}{Zout}$

where :

- Zext = R6 // C4 // (Zelectret) (at pin 24)
- Zint = 10Kohms // 8.5nF (internal impedance)
- Zout = 10.65 x Z4 (at pin 3 ; see paragr. 2.2.)
- Zline(short) and (long) are the impedances of the line at 0Km and 3.5Km.
- R5 = 5.1Kohm ± 1%

3.3. AC IMPEDANCE. The total AC impedance of the circuit to the line is :

Zpar = Zout//Zint//Zext//Zalc//Zall (see par. 2.2. and 3.2.)
= Zout//Zint//Zext (Zalc, Zall Zpar)

3.4. RECEIVE MUTE (and confidence level). When the receive channel is muted (Vpin 18 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from DTMF input (pin 7) to Receive Output (pin 28) with a gain Gmf = 31dB to provide acoustic feedback of the DTMF transmission.

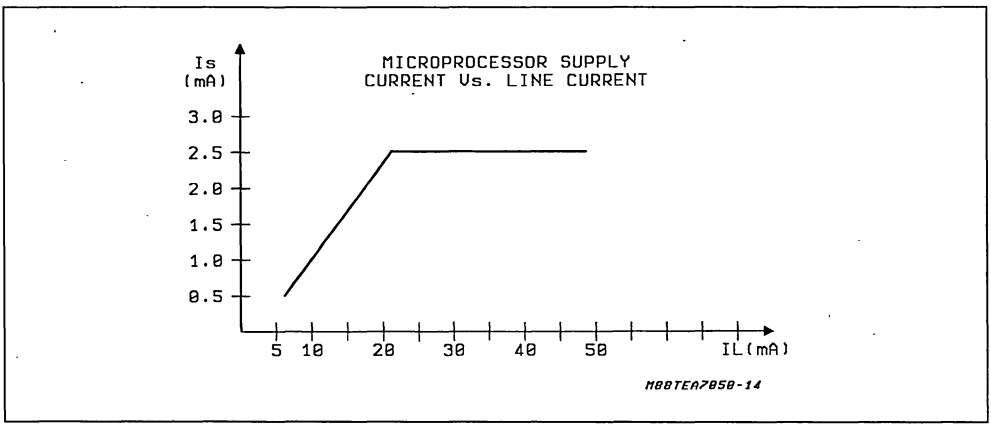
4. MICROPROCESSOR INTERFACE

4.1. MICROPROCESSOR SUPPLY (PIN 27). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 27) to charge quickly the external capacitor C3.

This charging current is : Icpm = 0.7 x (Iline - Idem), where Idem = 2.6mA is the current charging C1.

Vmp = 3.3V in normal operation and current increases linearly from 0.5mA min, at Iline = 6mA, to 2.5mA min, at Iline = 27mA, remaining stable for higher values of Iline.

Figure 10.

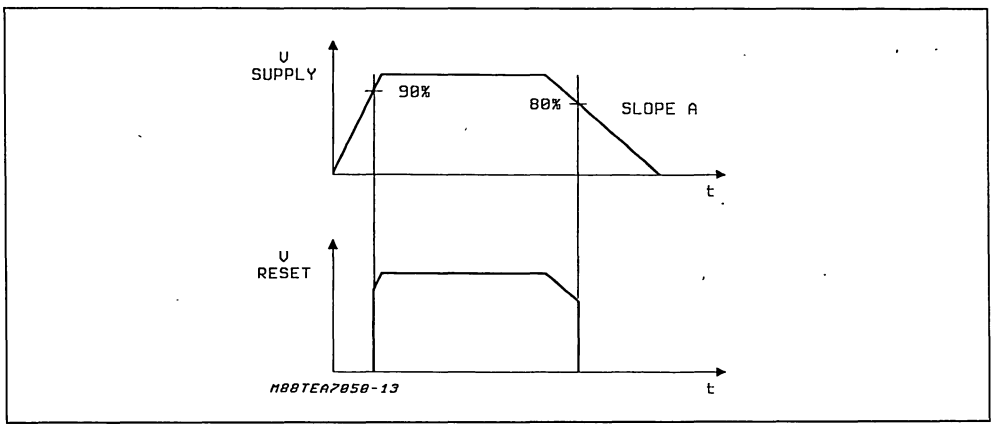


4.2. MICROPROCESSOR RESET (pin 20). The Microprocessor Reset becomes active when Vmp overcomes 85% of its nominal level.

It becomes low when Vmp undergoes 84%.

Slope A is related to C3, Iimp (internal consumption) and to the external load (microprocessor or dialer).

Figure 11.

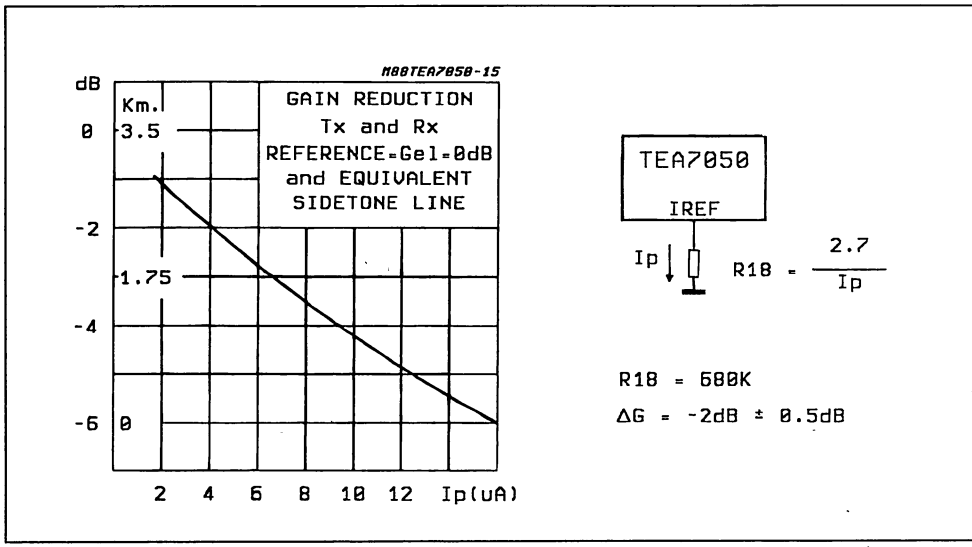


5. PUBLIC / PRIVATE

5.1. A.G.C. OFF (PIN 10). An external resistor, R18, applied between pin 10 and ground disconnects the AGC control.

Sending, receiving gain and sidetone compensation are now independent of the line length and the value of the current Ip, flowing through R18, defines the length of the line for which sidetone is optimized (Ip = 2.7V / R18).

Figure 12.



5.2. SECRET FUNCTION FOR PRIVATE (PINS 11 & 18). The two separate Mute pins allow "Secret Function" (only microphone muted).

As the two controls have different threshold levels, they can be operated :

a) separately through two different control logic,

b) connected in short circuit with a three levels logic (Vm = 0V speech mode ; Vm = 1.8V microph mute ; Vm = 3V all mute).

6. POWER MANAGEMEN AND HANDS-FREE INTERFACE

6.1. POWER MANAGEMENT (PIN 12). Most of the DC current available from the line will be delivered by the speech circuit at the output Isource (pin 12) through an internal current generator.

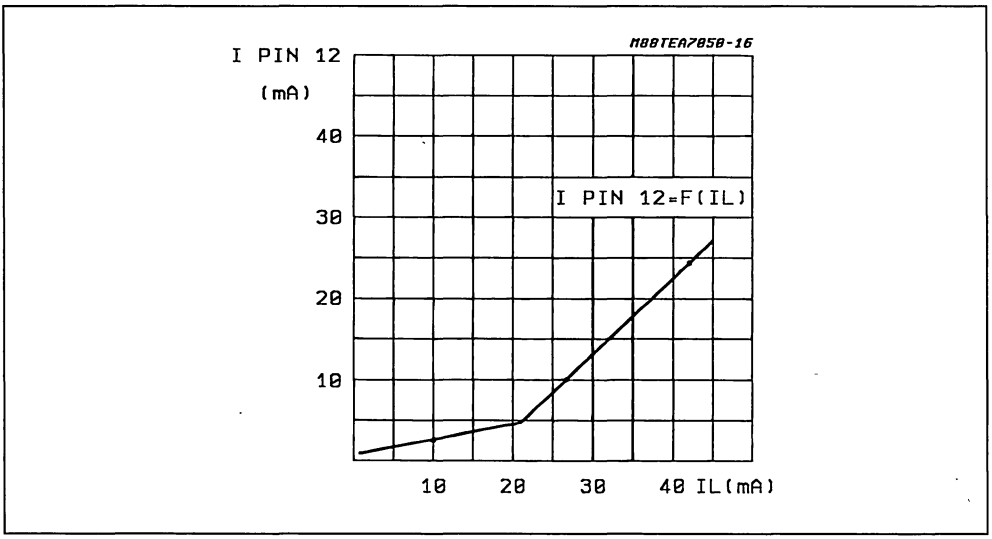
Typical values of this current, Iea, are :
- Iea = (0.3 x Iline) for Iline < 22mA
- Iea = (0.9 x Iline 13mA) for Iline > 22mA

(ex : Iline=16mA then Iea=4.8mA
Iline=30mA then Iea=14.0mA
Iline=60mA then Iea=41.0m)

The voltage level at pin 12 must be defined by an external regulator (i.e. : zener) and, if necessary, filtered with a capacitor (47 to 220 µF).

In case Vline (at pin 24) approaches V at pin 12, then the internal current source switches off and its DC current is shunt to ground through an internal complementary generator, thus avoiding any negative effect on the Ac and DC impedances of the telephone set application.

Figure 13.



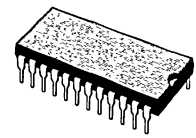
6.2. EXTRA RECEIVE OUTPUT (PIN 4). The Extra Receive Signal is active also in Receive Mute condition, so allowing the transit of the receive signal from the speech circuit to the Hands-Free system even when the earpiece is muted.

The gain at this pin is 30dB lower than standard Receive Output (pin 28).

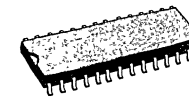
SPEECH CIRCUIT WITH POWER MANAGEMENT

ADVANCE DATA

- 2/4 WIRES INTERFACE WITH
  - Double antisidetone network
  - Rx gain and AC impedance externally programmable
- DTMF INTERFACE
- PULSE DIAL INTERFACE
- 4.0 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- RESET TO MICROPROCESSOR
- CURRENT SUPPLY FOR LOUDSPEAKER
- HANDS-FREE INTERFACE
- DC CHARACTERISTIC AND ON/OFF HOOK FOR FRANCE
- CONTROL AGAINST HIGH VOLTAGE TRANSIENTS



DIP24



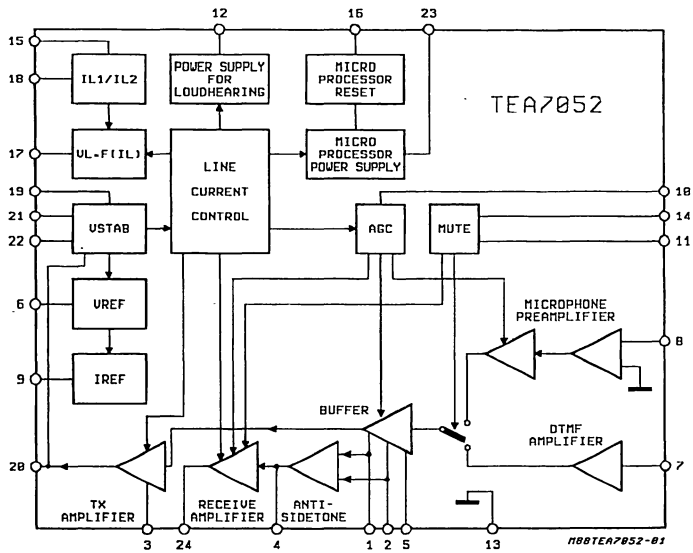
SO-28

ORDER CODES : TEA7052DP (DIP24)
TEA7052D (SO-28)

DESCRIPTION

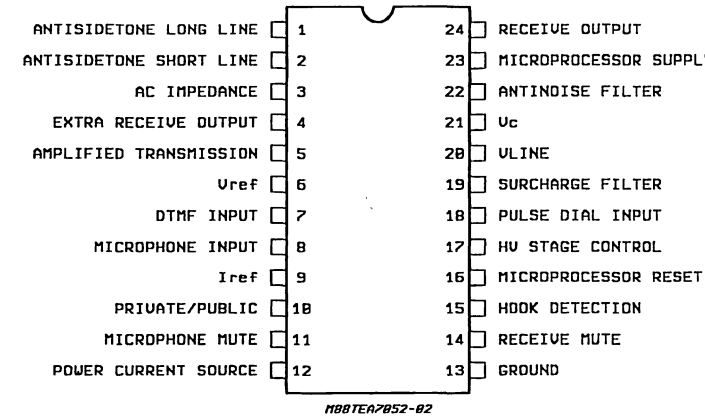
The TEA7052 is expressely designed to meet the french specification for telephone set in medium and high range equipments.

BLOCK DIAGRAM



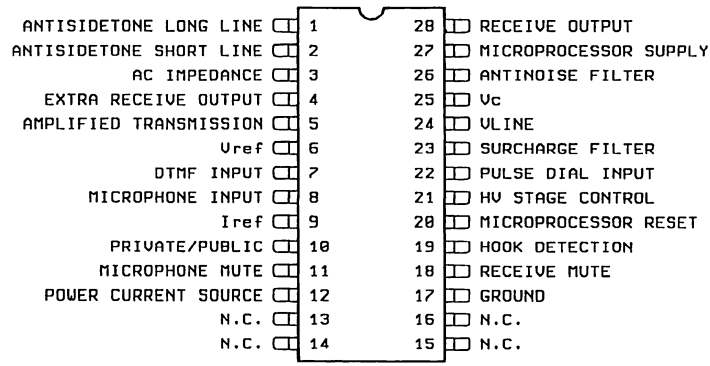
PIN CONNECTIONS (top view)

DIP24



MB8TEA7052-02

SO-28



MB8TEA7052-17

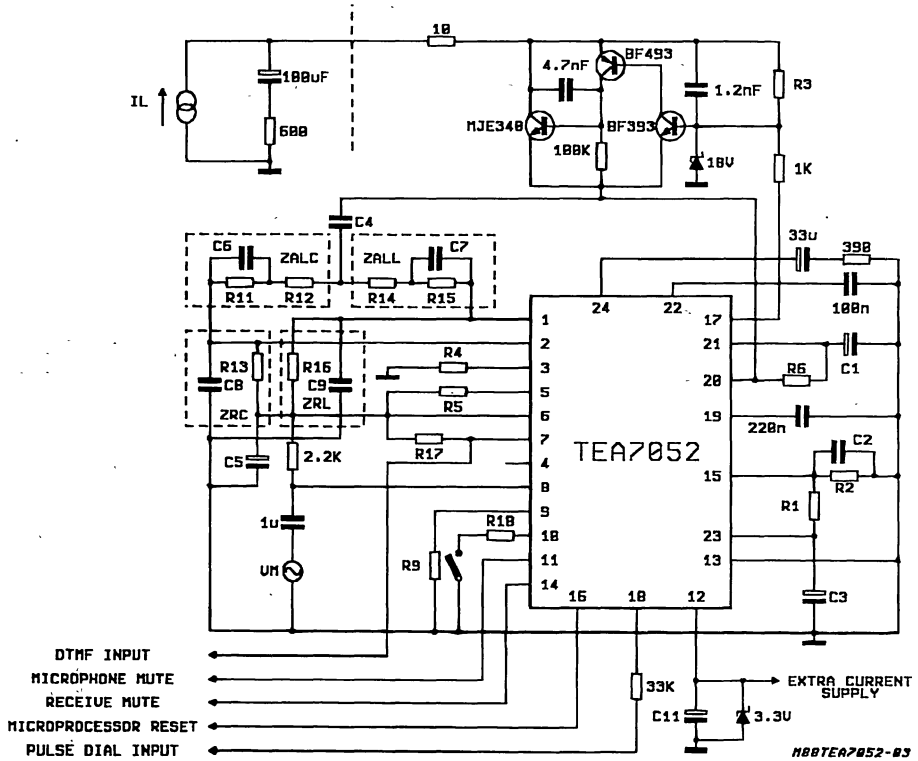
ELECTRICAL CHARACTERISTICS (Ta = 25°C ; PIN identification related to DIP–24 configuration)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vc	Stabilized Voltage (pin 21)	II = 27mA	2.35	2.6	2.85	V
Idem	Charging Current (pin 21)	II = 27mA		2.6		mA
Ir	Line Current Regulation for HV Control (pin17)	Pin 15 = Pin 21 = GND II = 150mA II = 100mA	 150		 5	µA
		Pin 15 ON ; Pin 21 = GND II = 75mA	 150			µA
		Pins 15 and 21 ON II = 60mA II = 16mA	 150		 100	µA nA
Ir/II		27mA < II < 50mA	0.8	0.9	1.0	µA/mA
Iint	Internal Bias Current (pin 21)	II = 27mA ; R9 = 26.7 Kohms ; (V20 = R6 x Iint + Vc)	250	280	310	µA
Vref	Reference Voltage	II = 27mA	1.32	1.38	1.47	V
Iref	Current at Vref		– 10		100	µA
Vmp	Stabilized Supply at Pin 23		3.7	4.0		V
Icmp	Charging Current at Pin 23	Pin 15 = Pin 21 = GND IL1 = II – Idem	0.7 x x IL1			mA
Ispm	Static Current at Pin 23	II = 6mA II > 25mA	0.5 2.5	 2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Iea	Supply Current for Parallel Circuits (pin 12)	R9 = 26.7Kohm II = 10mA II = 27mA II = 42mA	 8 21	 3 9.5 23.5	 11 26	 mA mA mA
	Microprocessor Reset					
Vrh	High Treshold		0.845	0.89		Vmp
Vrb	Low Treshold		0.76	0.8	0.84	(pin 23)
Vrsh	Output High	Reset = 1	0.9			
Vrsb	Output Low	Reset = 0			0.1	

ELECTRICAL CHARACTERISTICS (Ta = 25°C ; PIN identification related to DIP–24 configuration)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vmh Vmb	Mute Microphone (pin 11)	ON OFF	1.6		 0.8	V V
Vmh Vmb	Mute Earphone (pin 14)	ON OFF	2.7		 2.1	V V
Gel Gec	Tx Gain Long Line Tx Gain Short Line	Il = 27mA Il = 42mA	41 34	42 36	43 38	dB
Gmf	DTMF Gain	Il = 27mA Pin 11 > 1.6V	41	42	43	dB
De	Tx Distorsion	Il = 27 to 42mA Vl = 0dBm Vl = 3dBm			 3 10	 % %
Ze	Microphone Impedance		20			Kohm
Bep	Tx Noise (psophometric)	Il > 27mA 2K at Pins 6-8		– 73		dBmp
Re	Tx Attenuation in Mute Mode	Il = 27mA Pin 11 > 1.6V	60			dB
Grl Grc	Rx Gain Long Line Rx Gain Short Line	Il = 27mA Il = 42mA	29 22	30 24	31 26	dB
Dr	Rx Distorsion	Il = 27 to 42mA Vec = 500mV Vec = 700mV			 3 10	 % %
Brp	Rx Noise	Il > 27mA		– 74		dBmp
Rc	Rx Attenuation in Mute Mode	Il = 27mA Pin 14 > 2.7V	60			dB
Gal	Antisidetone	Il = 27 to 42mA	– 22			dB
Zac	AC Impedance	Il > 27mA	500	650	800	ohm
Grs	Confidence Level Vrec/Vmf	Pin 11 > 1.6V ; Pin 14 > 2.7V	35.5	38.5	41.5	dB

TEST CIRCUIT



R1 = 920KΩ
R2 = 820KΩ
R3 = 1.5MΩ
R4 = 75Ω
R5 = 5.1KΩ
R8 = 13KΩ
R9 = 26.7KΩ
R11 = 140KΩ
R12 = 0Ω
R13 = 2.7KΩ
R14 = 0Ω
R15 = 140KΩ
R16 = 2.7KΩ
R17 = 1.2 KΩ
R18 = 680KΩ for private complex

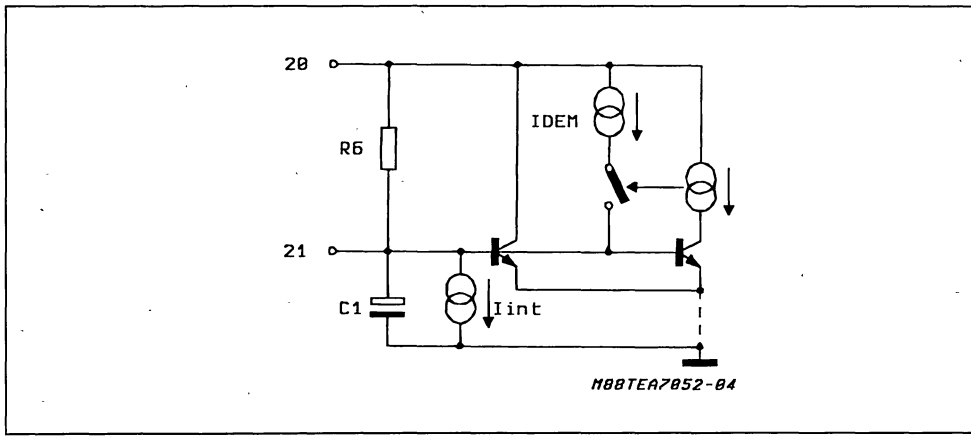
C1 = 100µF
C2 = 4.7µF
C3 = 10µF
C4 = 1µF
C5 = 100µF
C6 = 27pF
C7 = 27pF
C8 = 2.2nF
C9 = 2.2nF
C11 = 220µF

CIRCUIT DESCRIPTION

1. DC-CHARACTERISTICS

1.1. VC (pin 21). The stabilized voltage Vc is connected to Vline (pin 20) through an internal shunt regulator which presents to the line a high AC impedance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 21) must be not lower than 47 microFarad.

Figure 1.



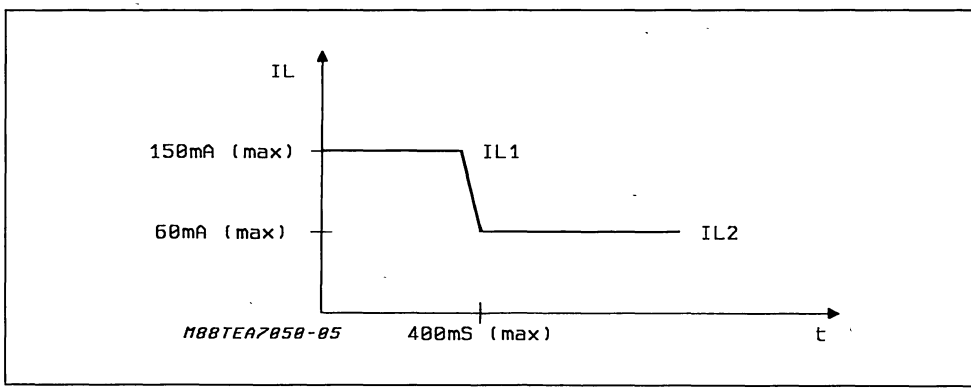
At "Off-hook", with only DC voltage applied to the line terminals, C1 fixes the timing of the line current profile at :

- 150mA max for a time shorter than 400msec (T-charge)
- 60mA max in steady state (conversation)

T-charge of 240msec (typ) is obtained with C1= 220µF.

$$\text{T-charge} = \frac{Vc \times C1}{Idem} \text{ typically.}$$

Figure 2.



1.2. HOOK DETECTION (in ring mode) (pin 15).
The DC-characteristic requested to allow off-hook detection by the exchange during ring call may be accomplished :
a) through an analog control (R-C) or
b) by a microprocessor.

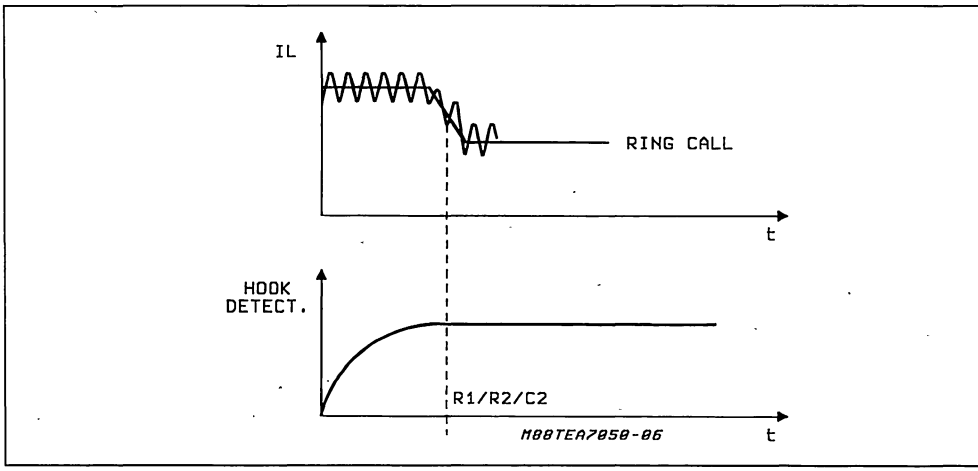
a) Application with standard dialer (analog control)

The components R1, R2 and C2 define the timing of the DC characteristic and also limit at 75mA-peak the line current during decadic dialing.

Optimum values are : - R1 x C2 = 1.8 sec ;
R2 x C2 = 0.8 sec.

To reduce the minimum time between a "on-hook / off-hook" sequence, R2 may be replaced by a switch to ground.

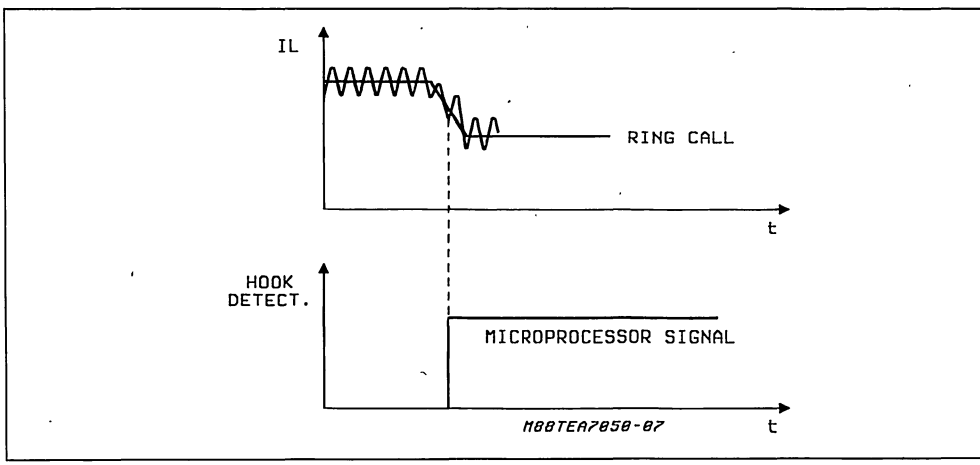
Figure 3.



b) Application with a microprocessor

Pin 15 may be controlled directly by the micro-controller, through a resistor R1b which replaces R1, R2 and C2.

Figure 4.



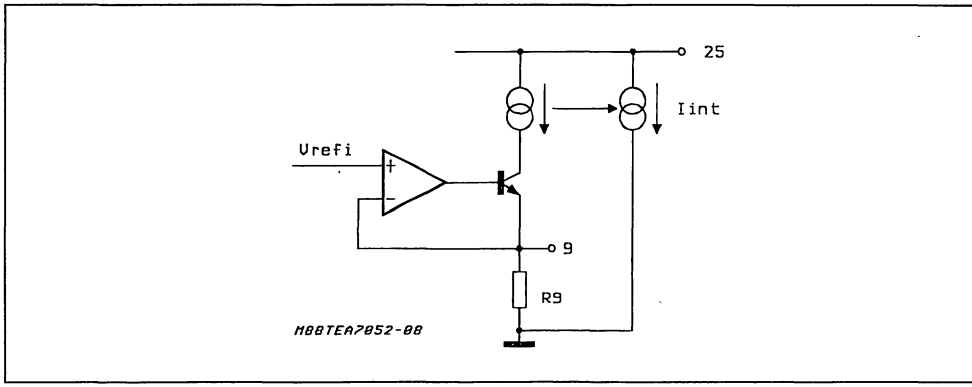
1.3. VLINE (pin 20). The line voltage (pin 20) is determined by the value of the external resistor R6 and by the internal current, Iint, flowing between Vc (pin 21) and Ground (see also paragr. 1.1.) :

$$Vline = Vc + R6 \times Iint.$$

Vc is fixed by design at about 2.6 volts.

Lint is reversely related to R9 (Lint = 7.5V/R9 at Iline = 27mA).

Figure 5.



Vline must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the french standards. At this purpose it is suggested that Vline equals 5.6 volts at Iline = 16mA. This typical value is obtained with R6 = 13Kohm.

1.4. HIGH VOLTAGE CONTROL STAGE (pin 17). The behaviour of "HV control" is determined by several conditions, both internal (Iline sensor) and external (pins 15 and 21) with the purpose to accomplish the different DC characteristics and transitory conditions imposed by the French specification :

a) steady DC-characteristic and lightnings (pins 15 and 21 ON)

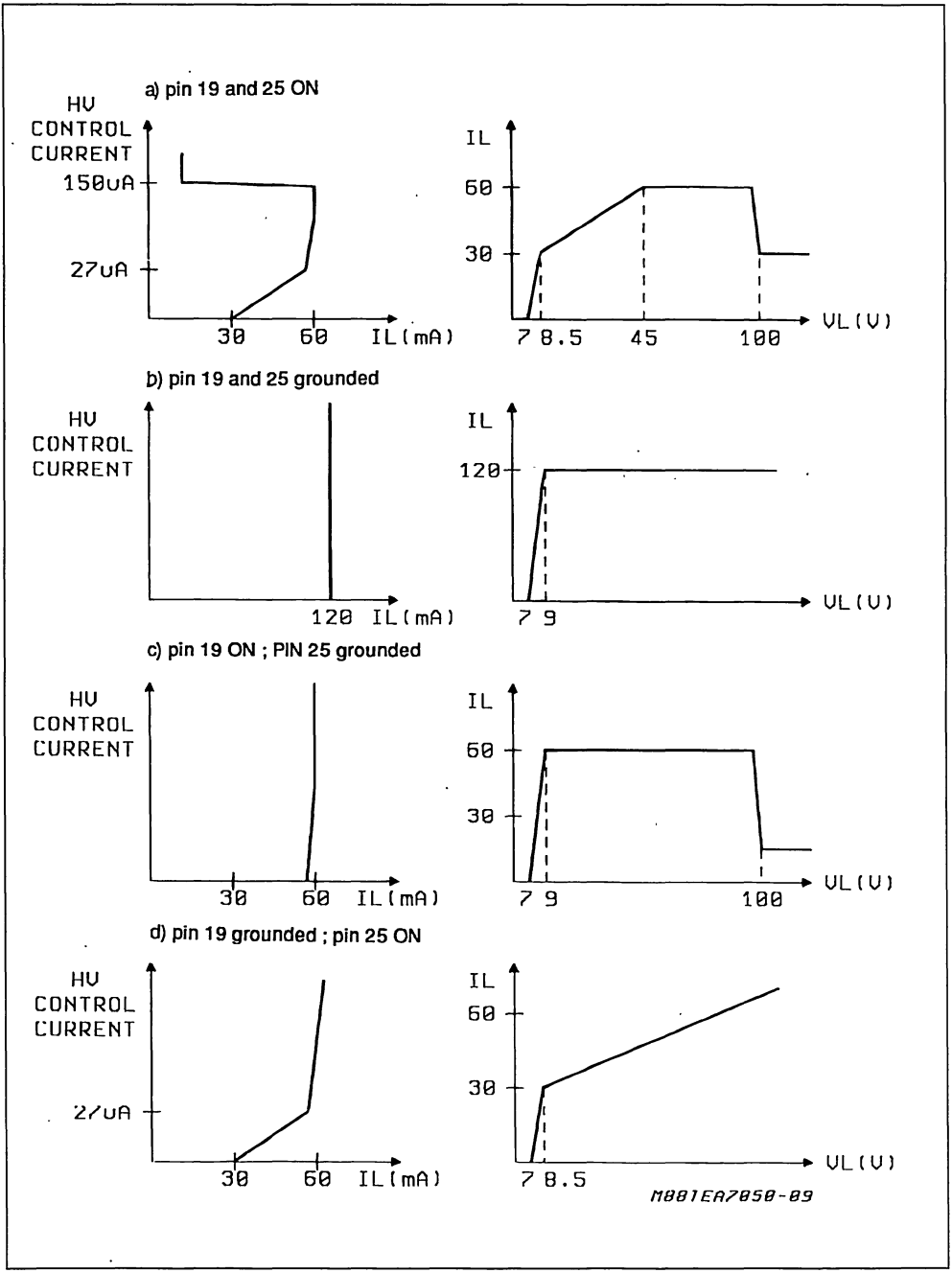
b) DC-characteristic at off-hook (pin 15 and 21 grounded)

c) DC-characteristic during decadic dialing (pin 21 grounded)

d) DC-characteristic after off-hook in ringing (pin 15 grounded)

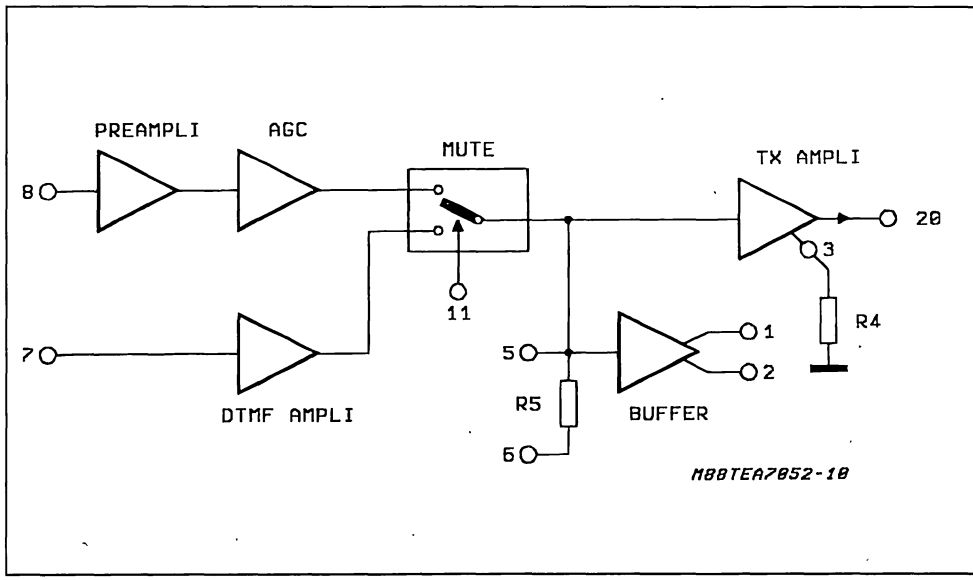
To do that, HV control pin regulates the current injected into the external high voltage transistor stage, requested by the French specification.

Figure 6.


a) pin 19 and 25 ON
HV CONTROL CURRENT
150uA
27uA
30
60
IL(mA)
IL
60
30
7
8.5
45
100
VL(V)
b) pin 19 and 25 grounded
HV CONTROL CURRENT
120
IL(mA)
IL
120
7
9
VL(V)
c) pin 19 ON ; PIN 25 grounded
HV CONTROL CURRENT
30
60
IL(mA)
IL
60
30
7
9
100
VL(V)
d) pin 19 grounded ; pin 25 ON
HV CONTROL CURRENT
27uA
30
60
IL(mA)
IL
60
30
7
8.5
VL(V)
M881EA7050-09

2. TRANSMISSION CHAIN

Figure 7.



2.1. A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 8) and Vline (pin 20) is internally decreased of 6dB when the line current varies from 27mA to 42mA with a constant AC load of 600 ohms.

2.2. SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 (at pin 3).

$$Zout = 10.65 \times Z4.$$

The total AC impedance shown to the line is the parallel

$$Zpar = Zout//Zint//Zext$$

where :

- Zint = 10kohm // 8.5nF (internal)
- Zext = R6 // C4 (at pin 20)

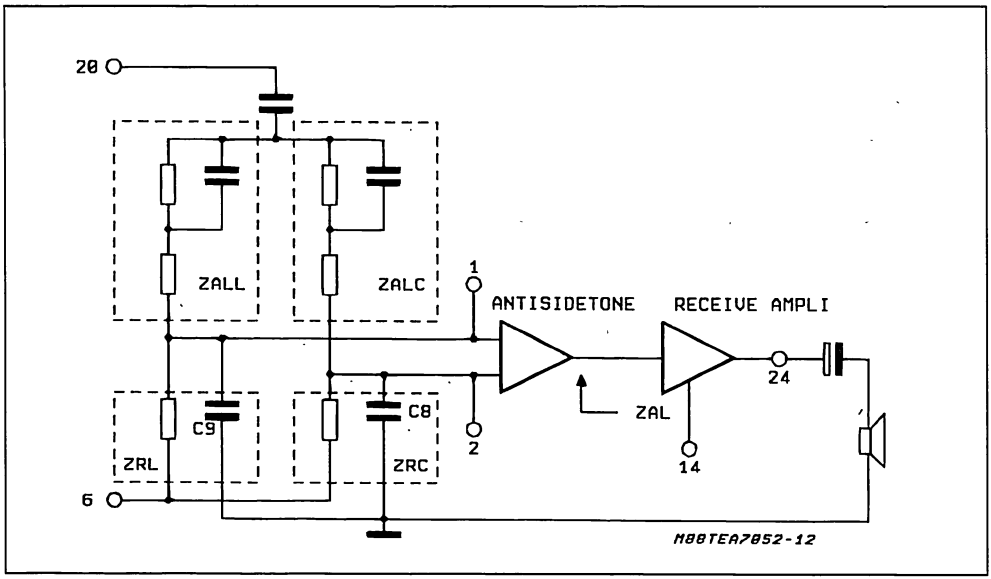
2.3. SENDING MUTE. In normal speech operation (Vmute < 0.8V), the signal at Microphone Input (pin 8) is amplified to Vline (pin 20) with the gains Gec (short line), Gel (long line) or intermediate, depending on Iline.

In sending mute condition (Vmute > 1.6V) these gains are reduced of at least 60dB. In the same condition DTMF input (pin 7) is activated, with gain Gmf to the line independent from Iline.

2.4. ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented at pin 5 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2.).

3. RECEIVE CHAIN

Figure 8.



3.1. A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 24, have a reduction of 6dB when Iline moves from 27mA to 42mA.

3.2. SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize sidetone both at long and short lines.

Before entering pins 1 and 2, the received signal is attenuated by two attenuating networks :

- Zall / Zrl to pin 1 for long lines sidetone compensation,
- Zalc / Zrc to pin 2 for short lines sidetone compensation.

Zrl and Zrc define the total receive gains :

$$a)\ \frac{V\,24}{V\,20} = Grl \times \frac{Zrc}{Zrl + Zall} \quad \text{for long lines}$$

$$b)\ \frac{V\,20}{V\,24} = Grc \times \frac{Zrc}{Zrc + Zalc} \quad \text{for short lines}$$

Zall and Zalc define the sidetone compensation of the circuit.

The equivalent balancing impedance is given by the formula :

$$Zal = K \times Zalc + (1 - K) \times Zall$$

where K = 0 at Iline = 27mA or lower (long line)

K varies from 0 to 1 with Iline between 27mA and 42mA,

K = 1 at Iline = 42mA or higher (short line).

Calculations to define Zall and Zalc are :

$$a)\ Zall = 70 \times R5 \times \frac{Zline(long)\ //\ Zext\ //\ Zint\ //\ Zout}{Zout}$$

$$b)\ Zalc = 70 \times R5 \times \frac{Zline(short)\ //\ Zext\ //\ Zint\ //\ Zout}{Zout}$$

where :

- Zext = R6 // C4 // (Zelectret) (at pin 20)
- Zint = 10Kohms // 8.5nF (internal impedance)
- Zout = 10.65 x Z4 (at pin 3 ; see paragr. 2.2.)
- Zline (short) and (long) are the impedances of the line at 0Km and 3.5Km.
- R5 = 5.1Kohm ± 1 %

3.3. AC Impedance. The total AC impedance of the circuit to the line is :

Zpar = Zout//Zint//Zext//Zalc//Zall (see par. 2.2. and 3.2.)
= Zout//Zint//Zext (Zalc, Zall Zpar)

3.4. RECEIVE MUTE (and confidence level). When the receive channel is muted (Vpin 14 > 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from DTMF input (pin 7) to Receive Output (pin 24) with a gain Gmf = 38.5dB to provide acoustic feedback of the DTMF transmission.

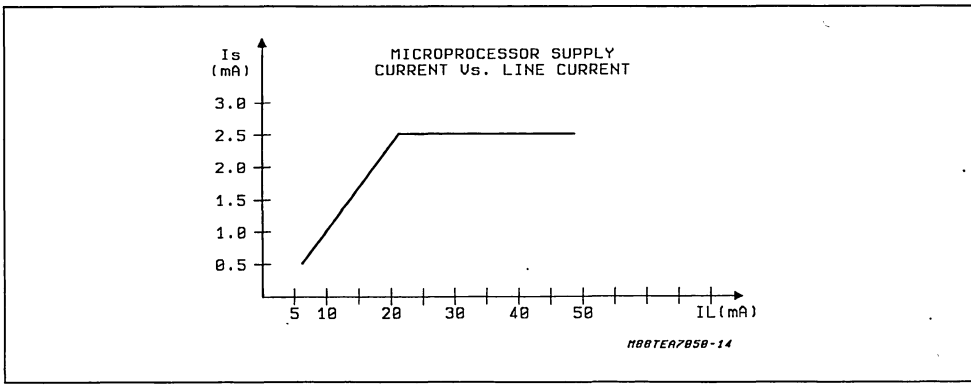
4. MICROPROCESSOR INTERFACE

4.1. MICROPROCESSOR SUPPLY (pin 23). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 23) to charge quickly the external capacitor C3.

This charging current is : Icpm = 0.7 x (Iline - Idem), where Idem = 2.6mA is the current charging C1.

Vmp = 3.95V in normal operation and current increases linearly from 0.5mA min, at Iline=6mA, to 2.5mA min, at Iline = 27mA, remaining stable for higher values of Iline.

Figure 9 : Microprocessor Supply Current vs. Line Current.

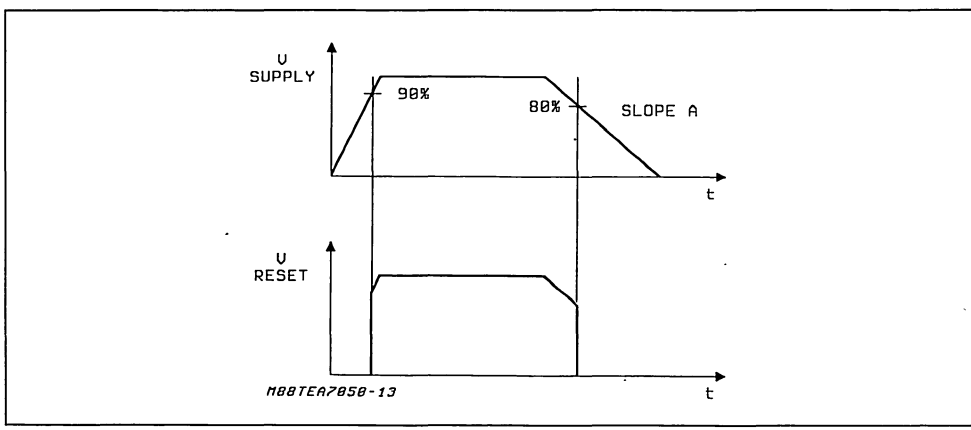


4.2. MICROPROCESSOR RESET (pin 16). The Microprocessor Reset becomes active when Vmp overcomes 85 % of its nominal level.

It becomes low when Vmp undergoes 84 %.

Slope A is related to C3, I1mp (internal consumption) and to the external load (microprocessor or dialer).

Figure 10.

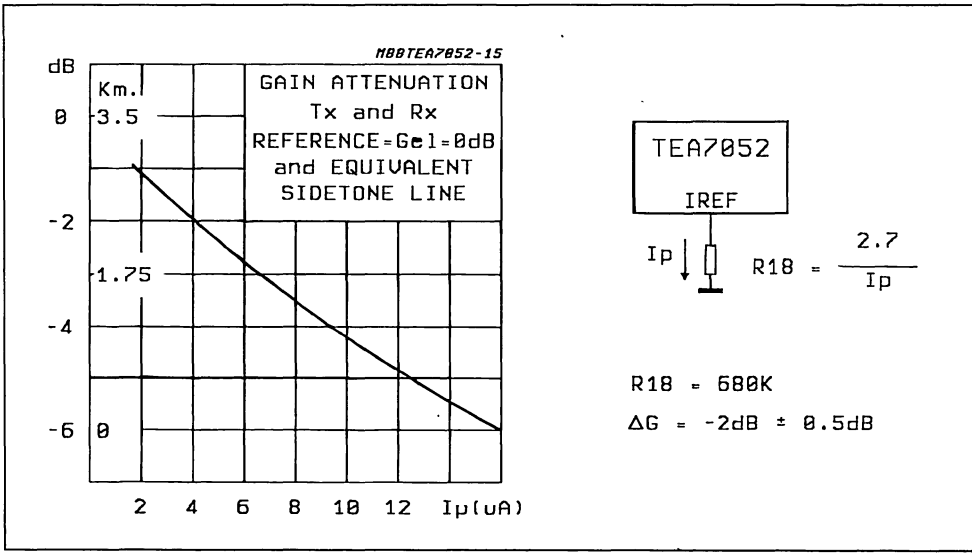


5. PUBLIC / PRIVATE

5.1. A.G.C. OFF (pin 10). An external resistor, R18, applied between pin 10 and ground disconnects the AGC control.

Sending, receiving gain and sidetone compensation are now independent of the line length and the value of the current Ip, flowing through R18, defines the length of the line for which sidetone is optimized (Ip = 2.7V / R18).

Figure 11.



5.2. SECRET FUNCTION FOR PRIVATE (pins 11 & 14). The two separate Mute pins allow "Secret Function" (only microphone muted).

As the two controls have different threshold levels, they can be operated :

a) separately through two different control logic,

b) connected in short circuit with a three levels logic (Vm = 0V speech mode ; Vm = 1.8V microph mute ;
Vm = 3V all mute).

6. POWER MANAGEMEN AND HANDS-FREE INTERFACE

6.1. Power Management (pin 12). Most of the DC current available from the line will be delivered by the speech circuit at the output Isource (pin 12) through an internal current generator.

Typical values of this current, Iea, are :

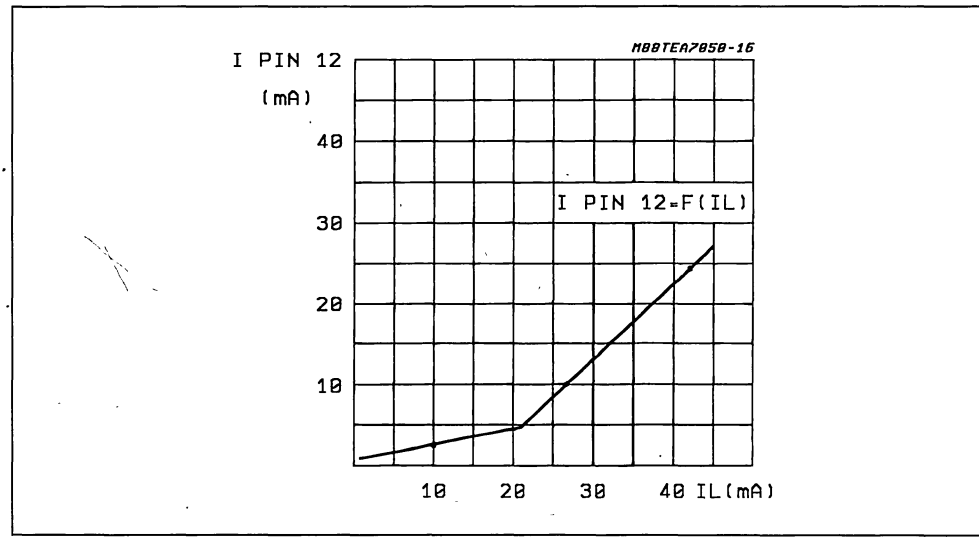
- Iea = (0.3 x Iline) for Iline < 22mA
- Iea = (0.9 x Iline 13mA) for Iline > 22mA

(ex : Iline = 16mA then Iea = 4.8mA
Iline = 30mA then Iea = 14.0mA
Iline = 60mA then Iea = 41.0mA

The voltage level at pin 12 must be defined by an external regulator (i.e. : zener) and, if necessary, filtered with a capacitor (47 to 220 microF).

In case Vline (at pin 20) approaches V at pin 12, then the internal current source switches off and its DC current is shunt to ground through an internal complementary generator, thus avoiding and negative effect on the AC and DC impedances of the telephone set application.

Figure 12.



6.2. EXTRA RECEIVE OUTPUT (pin 4). The Extra Receive Signal is active also in Receive Mute condition, so allowing the transit of the receive signal from the speech circuit to an external hands-free system even when the earpiece is muted.

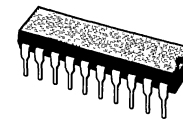
The gain at this pin is 30dB lower than standard Receive Output (pin 24).

SGS-THOMSON MICROELECTRONICS

TEA7053

SPEECH CIRCUIT

- 2/4 WIRES INTERFACE WITH
  - DOUBLE ANTISIDETONE NETWORK
  - RX GAIN AND AC IMPEDANCE EXTERNALLY PROGRAMMABLE
- DTMF INTERFACE
- PULSE DIAL INTERFACE
- 3.25 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- DC CHARACTERISTIC AND ON/OFF HOOK FOR FRANCE
- CONTROL AGAINST HIGH VOLTAGE TRANSIENTS



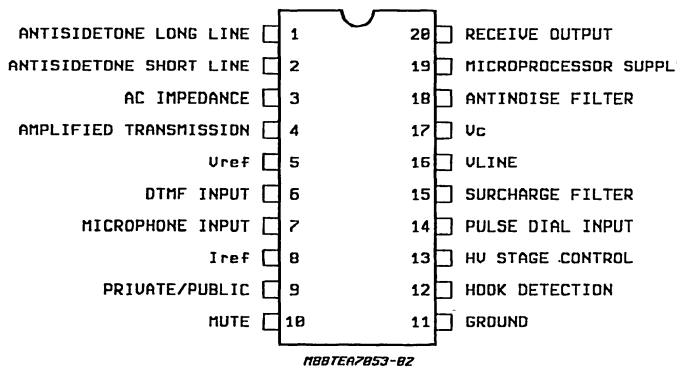
DIP20

ORDER CODE : TEA7053DP

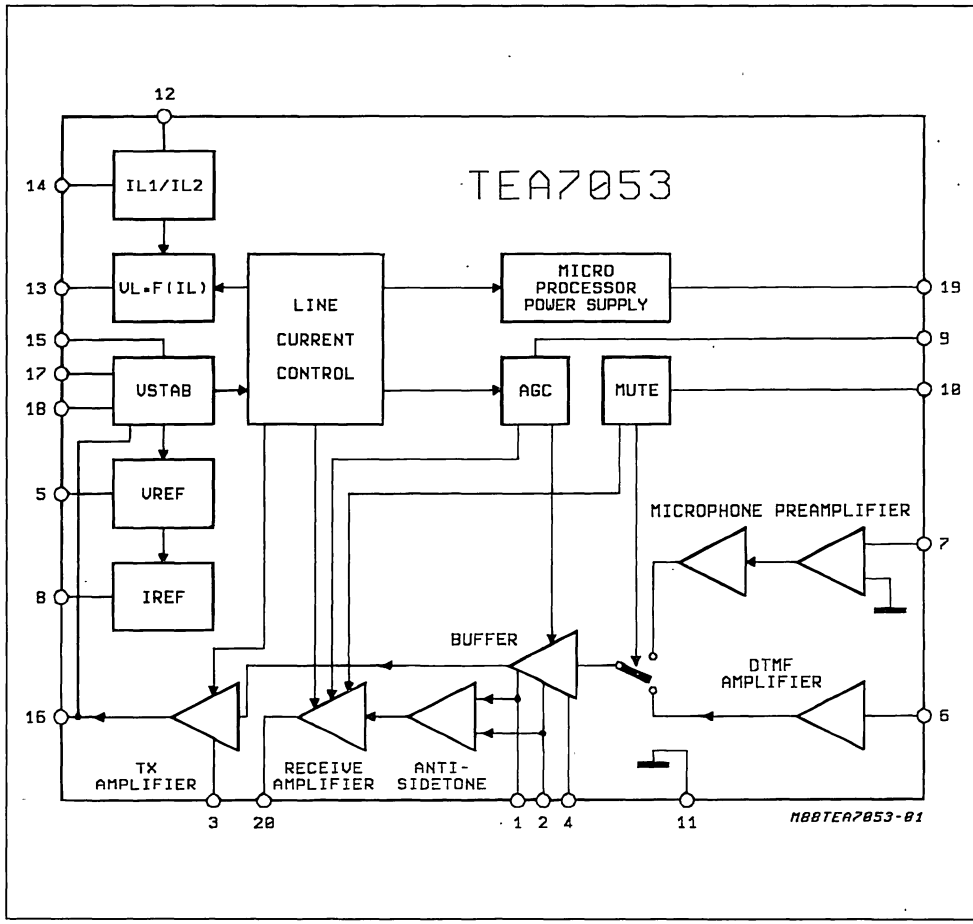
DESCRIPTION

The TEA7053 is expressely designed to meet the french specification for basic telephone set.

PIN CONNECTION (top view)



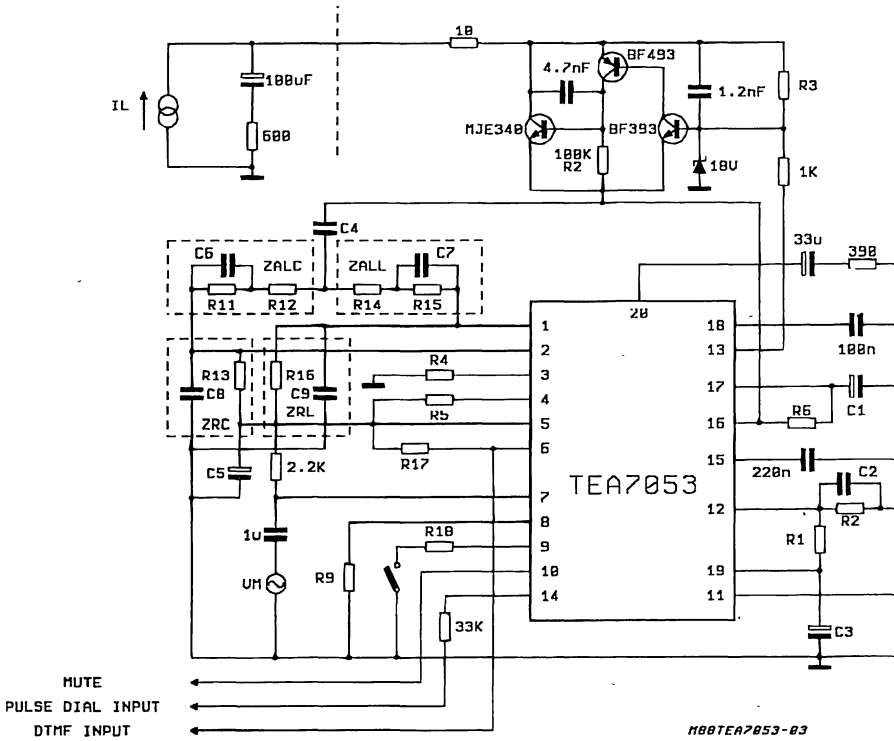
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Vc	Stabilized Voltage (pin 17)	II = 27mA	2.35	2.6	2.85	V
Idem	Charging Current (pin 17)	II = 27mA		2.6		mA
Ir	Line Current Regulation for HV Control (pin 17)	Pin 12 = Pin 17 = GND II = 150mA II = 100mA	150		 5	µA
		Pin 12 ON ; Pin 17 = GND II = 75mA	150			µA
		Pins 12 and 17 ON II = 60mA II = 16mA	150		 100	µA nA
Ir/II		27mA < II < 50mA	0.8	0.9	1.0	µA/mA
Iint	Internal Bias Current (pin 17)	II = 27mA ; R9 = 26.7 KΩ ; (V16 = R6·Iint + Vc)	250	280	310	µA
Vref	Reference Voltage	II = 27mA	1.32	1.38	1.47	V
Iref	Current at Vref		– 10		100	µA
Vmp	Stabilized Supply at Pin 19		3.1	3.3		V
Icmp	Charging Current at Pin 19	Pin 12 = Pin 17 = GND IL1 = II – Idem	0.7 x x IL1			mA
Ispm	Static Current at Pin 19	II = 6mA II > 25mA	0.5 2.5	 2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Vmh Vmb	Mute Microphone (pin 10)	ON OFF	1.6		 0.8	V V
Vmh Vmb	Mute Earphone (pin 10)	ON OFF	2.7		 2.1	V V
Gel Gec	Tx Gain Long Line Tx Gain Short Line	II = 27mA II = 42mA	41 34	42 36	43 38	dB
Gmf	DTMF Gain	II = 27mA Pin 10 > 1.6V	41	42	43	dB
De	Tx Distortion	II = 27 to 42mA Vl = 0dBm Vl = 3dBm			 3 10	 % %
Ze	Microphone Impedance		20			Kohm
Bep	Tx Noise (psophometric)	II > 27mA ; 2K at Pins 5-7		– 713		dBmp
Re	Tx Attenuation in Mute Mode	II = 27mA ; Pin 10 > 1.6V	60			dB
Grl Grc	Rx Gain Long Line Rx Gain Short Line	II = 27mA II = 42mA	29 22	30 24	31 26	dB
Dr	Rx Distortion	II = 27 to 42mA Vec = 500mV Vec = 700mV			 3 10	 % %
Brp	Rx Noise	II > 27mA		– 74		dBmp
Rc	Rx Attenuation in Mute Mode	II = 27mA ; Pin 10 > 2.7V	60			dB
Gal	Antisidetone	II = 27 to 42mA	– 22			dB
Zac	AC Impedance	II > 27mA	500	650	800	Ω
Grs	Confidence Level V_{LINE} / V_{REC} (DTMF)	Pin 10 > 2.7V	35.5	38.5	41.5	dB

Figure 1 : Test Circuit.



R1 = 820KΩ
R2 = 820KΩ
R3 = 1.5MΩ
R4 = 75Ω
R5 = 5.1KΩ
R8 = 13KΩ
R9 = 26.7KΩ
R11 = 140KΩ
R12 = 0Ω
R13 = 2.7KΩ
R14 = 0Ω
R15 = 140KΩ
R16 = 2.7KΩ
R17 = 1.2 KΩ
R18 = 680KΩ for private complex

C1 = 100µF
C2 = 4.7µF
C3 = 10µF
C4 = 1µF
C5 = 100µF

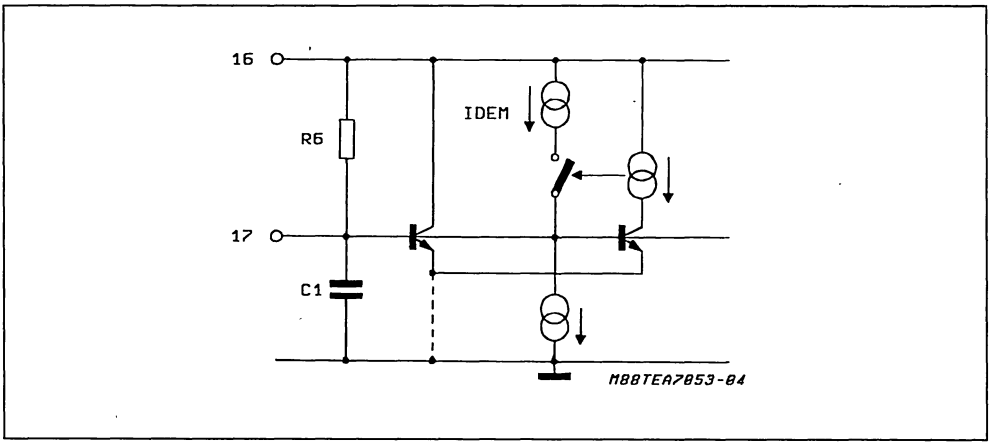
C6 = 27pF
C7 = 27pF
C8 = 2.2nF
C9 = 2.2nF
C11 = 220µF

CIRCUIT DESCRIPTION

1. DC-Characteristics

1.1. VC (pin 17). The stabilized voltage Vc is connected to Vline (pin 16) through an internal shunt regulator which presents to the line a high AC impedance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 17) must be not lower than 47 microFarad.

Figure 2.



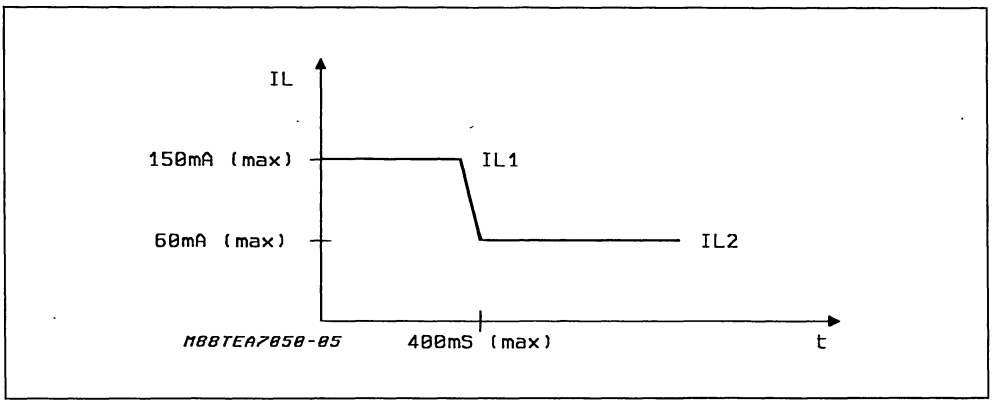
At "Off-hook", with only DC voltage applied to the line terminals, C1 fixes the timing of the line current profile at :

- - 150mA max for a time shorter than 400msec (T-charge)
- - 60mA max in steady state (conversation)

T-charge of 240msec (typ) is obtained with C1=220µF

$$\text{T-charge} = \frac{Vc \times C1}{Idem} \text{ typically.}$$

Figure 3.



1.2. HOOK DETECTION (in ring mode) (pin 12). The DC-characteristic requested to allow off-hook detection by the exchange during ring call may be accomplished :

a) through an analog control (R-C) or

b) by a microprocessor.

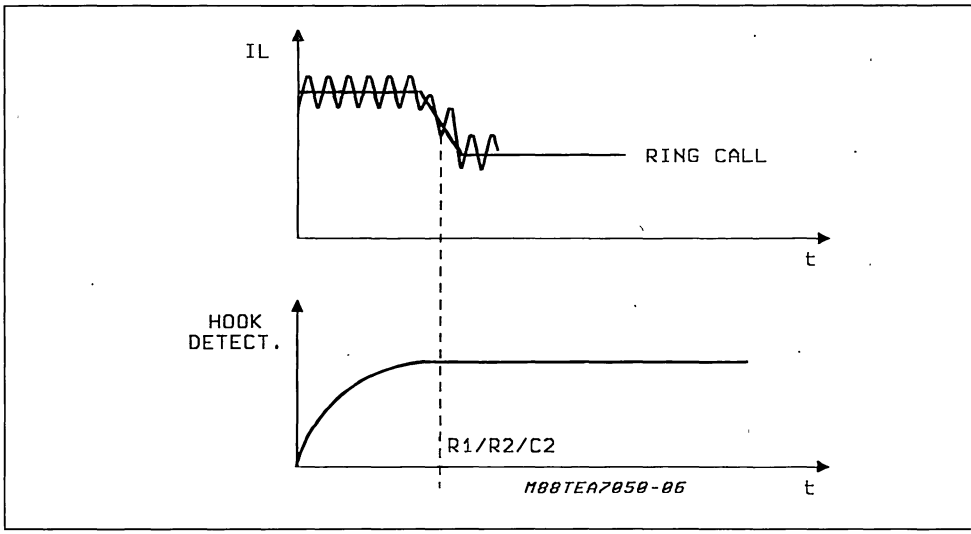
a) Application with standard dialer (analog control)

The components R1, R2 and C2 define the timing of the DC characteristic and also limit at 75mA-peak the line current during decadic dialing.

Optimum values are : - R1 x C2 = 1.8sec ; R2 x C2 = 0.8sec.

To reduce the minimum time between a "on-hook / off-hook" sequence, R2 may be replaced by a switch to ground.

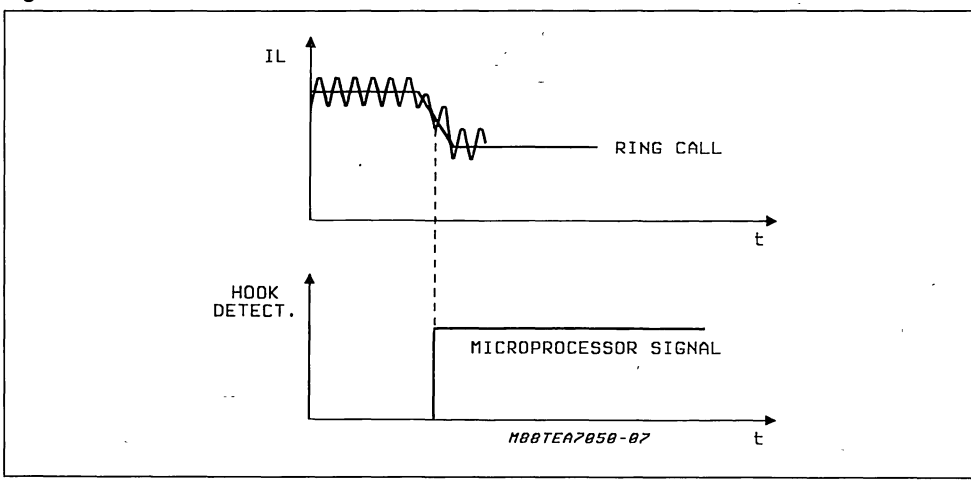
Figure 4.



b) Application with a microprocessor

Pin 12 may be controlled directly by the micro-controller, through a resistor R1b which replaces R1, R2 and C2.

Figure 5.



1.3. V_{LINE} (pin 16). The line voltage (pin 16) is determined by the value of the external resistor R6 and by the internal current, Iint, flowing between Vc (pin 17) and Ground (see also parag. 1.1.) :

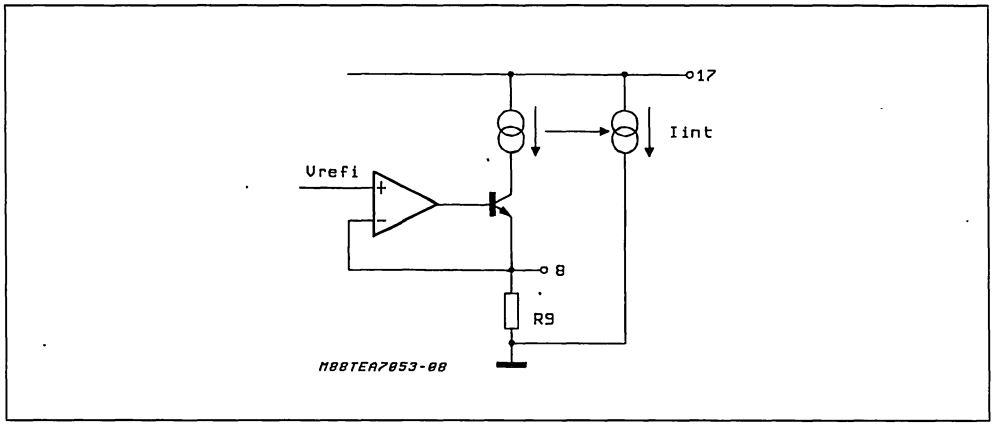
$$V_{LINE} = Vc + R6 * Iint.$$

Vc is fixed by design at about 2.6 volts.

Iint is reversely related to R9 (Iint = 7.5V/R9 at I_{LINE} = 27mA).

V_{LINE} must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the french standards. At this purpose it is suggested that Vline equals 5.6 volts at Iline = 16mA. This typical value is obtained with R6 = 13Kohm.

Figure 6.



1.4. HIGH VOLTAGE CONTROL STAGE (pin 13). The behaviour of "HV control" is determined by several conditions, both internal (Iline sensor) and external (pins 12 and 17) with the purpose to accomplish the different DC characteristics and transitory conditions imposed by the French specification :

a) steady DC-characteristic and lightnings (pins 12 and 17 0N)

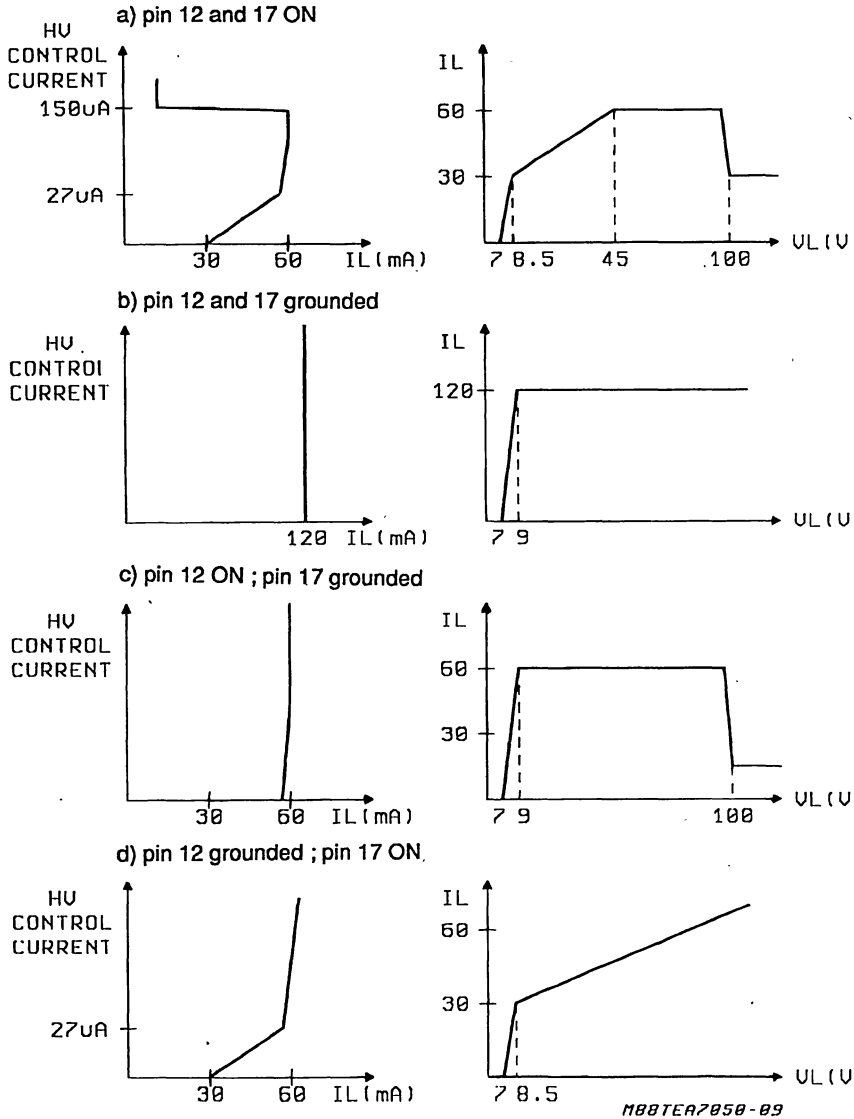
b) DC-characteristic at off-hook (pin 12 and 17 grounded)

c) DC-characteristic during decadic dialing (pin 17 grounded)

d) DC-characteristic after off-hook in ringing (pin 12 grounded)

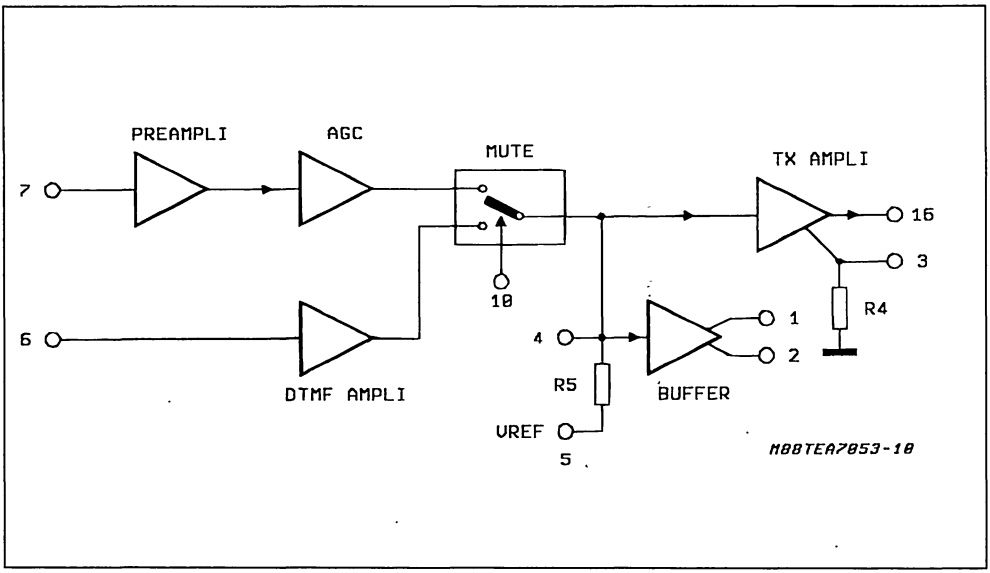
To do that, HV control pin regulates the current injected into the external high voltage transistor stage, requested by the French specification.

Figure 7.


a) pin 12 and 17 ON
HV CONTROL CURRENT
150uA
27uA
30
60
IL(mA)
IL
60
30
7
8.5
45
100
VL(V)
b) pin 12 and 17 grounded
HV CONTROL CURRENT
120
IL(mA)
IL
120
7
9
VL(V)
c) pin 12 ON ; pin 17 grounded
HV CONTROL CURRENT
30
60
IL(mA)
IL
60
30
7
9
100
VL(V)
d) pin 12 grounded ; pin 17 ON
HV CONTROL CURRENT
27uA
30
60
IL(mA)
IL
60
30
7
8.5
VL(V)
MBBTEA7050-09

2. Transmission Chain

Figure 8 .



2.1. A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 7) and Vline (pin 16) is internally decreased of 6dB when the line current varies from 27mA to 42mA with a constant AC load of 600ohms.

2.2. SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 at pin 3.

$$Zout = 10.65 \times Z4.$$

The total AC impedance shown to the line is the parallel

$$Zpar = Zout//Zint//Zext$$

where :

- Zint = 10kohm // 8.5nF (internal)
- Zext = R6 // C4 (at pin 16)

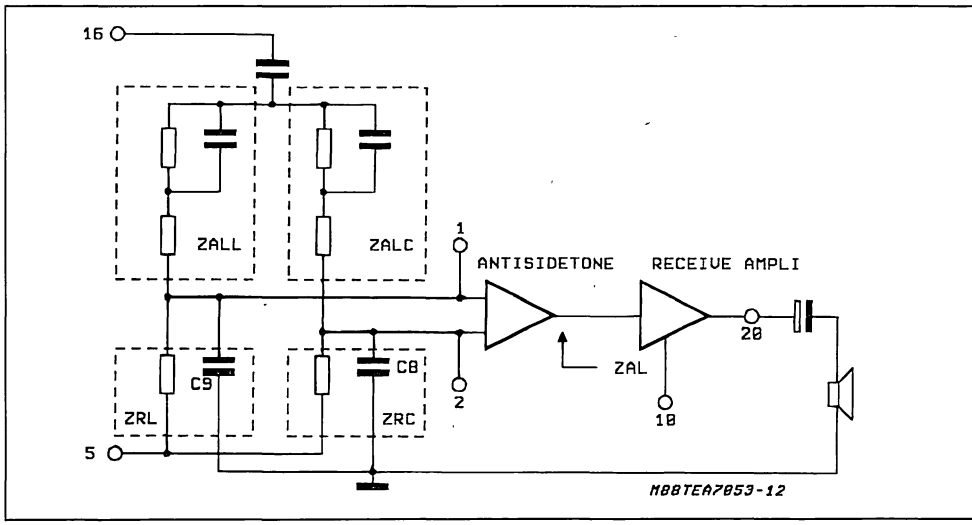
2.3. SENDING MUTE. In normal speech operation (Vmute at pin 10 0.8V), the signal at Microphone Input (pin 7) is amplified to Vline (pin 16) with the gains Gec (short line), Gel (long line) or intermediate, depending on Iline.

In sending mute condition (Vmute 1.6V) these gains are reduced of at least 60dB. In the same condition DTMF input (pin 6) is activated, with gain Gmf to the line independent from Iline.

2.4. ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented at pin 4 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2.).

3. Receive Chain

Figure 9.



3.1. A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 20, have a reduction of 6dB when Iline moves from 27mA to 42mA.

3.2. SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize sidetone both at long and short lines.

Before entering pins 1 and 2, the received signal is attenuated by two attenuating networks :

Zall / Zrl to pin 1 for long lines sidetone compensation,
Zalc / Zrc to pin 2 for short lines sidetone compensation.
Zrl and Zrc define the total receive gains :

a) $\frac{V\,20}{V\,16} = Grl \times \frac{Zrl}{Zrl + Zall}$ for long lines

b) $\frac{V\,20}{V\,16} = Grc \times \frac{Zrc}{Zrc + Zalc}$ for short lines

Zall and Zalc define the sidetone compensation of the circuit.
The equivalent balancing impedance is given by the formula :

$$Zal = K * Zalc + (1-K) * Zall$$

where :

- K = 0 at Iline = 27mA or lower (long line)
- K varies from 0 to 1 with Iline between 27mA and 42mA,
- K = 1 at Iline = 42mA or higher (short line).

Calculations to define Zall and Zalc are :

a) $Zall = 70 \times R5 \times \frac{Zline(long) \,//\, Zext \,//\, Zint \,//\, Zout}{Zout}$

b) $Zalc = 70 \times R5 \times \frac{Zline(short) \,//\, Zext \,//\, Zint \,//\, Zout}{Zout}$

where :

- Zext = R6 // C4 // (Zelectret) (at pin 16)
- Zint = 10Kohms // 8.5nF (internal impedance)
- Zout = 10.65 * Z4 (at pin 3 ; see paragr. 2.2.)
- Zline (short) and (long) are the impedances of the line at 0Km and 3.5 Km.
- R5 = 5.1 Kohm ± 1 %

3.3. AC IMPEDANCE. The total AC impedance of the circuit to the line is :

Zpar = Zout//Zint//Zext//Zalc//Zall (see par. 2.2. and 3.2.)
= Zout//Zint//Zext (Zalc, Zall >> Zpar)

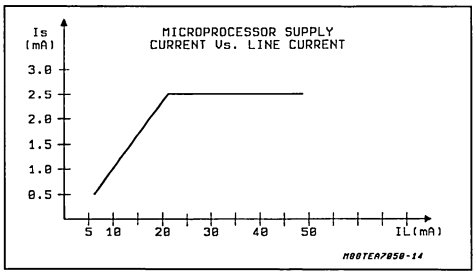
3.4. RECEIVE MUTE (AND CONFIDENCE LEVEL). When the receive channel is muted (Vmute at pin 10 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from line DTMF output (pin 16) to Receive Output (pin 20) with a gain Gmf = 38.5dB to provide acoustic feedback of the DTMF transmission.

4. Microprocessor Interface

4.1. MICROPROCESSOR SUPPLY (PIN 19). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 19) to charge quickly the external capacitor C3.

Figure 10.



This charging current is : Icpm = 0.7 * (Iline - Idem), where Idem = 2.6mA is the current charging C1.

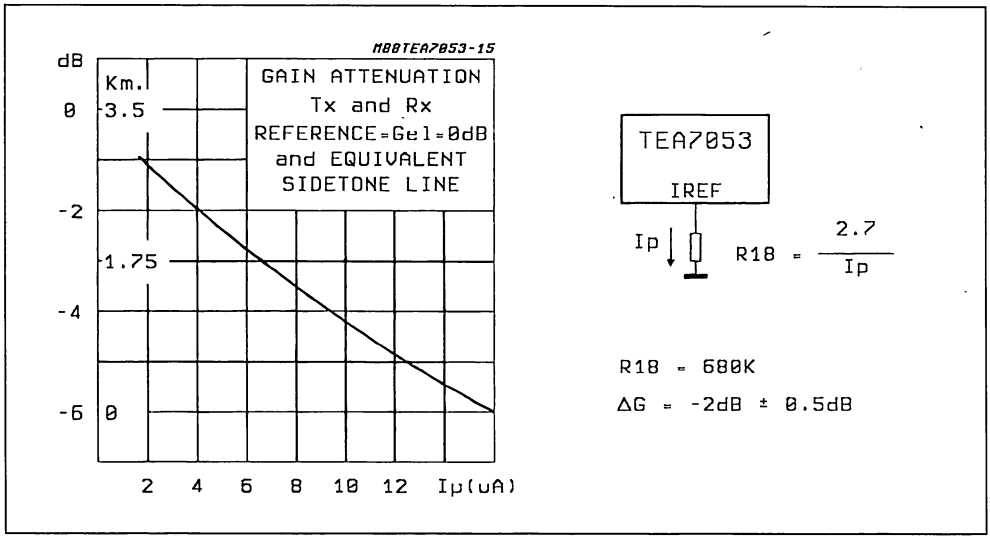
Vmp = 3.25V in normal operation and current increases linearly from 0.5mA min, at Iline = 6mA, to 2.5mA min, at Iline = 27mA, remaining stable for higher values of Iline.

5. Public/Private

5.1. A.G.C. OFF (PIN 9). An external resistor, R18, applied between pin 9 and ground disconnects the AGC control.

Sending, receiving gain and sidetone compensation are now independent of the line lenght and the value of the current Ip, flowing through R18, defines the lenght of the line for which sidetone is optimized (Ip = 2.7V/R18).

Figure 11.



5.2. SECRET FUNCTION (PIN 10). The Mute pin allows "Secret Function" (only microphone muted), when the circuit is used for private market.

As the control of sending and receiving must have different threshold levels, it can be operated with a three levels logic :

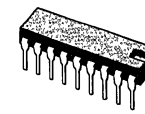
a) Vm = 0V speech mode ;
b) Vm = 1.8V microphone muted ;
c) Vm = 3.0V all speech muted.

SGS-THOMSON MICROELECTRONICS

TEA7062

SPEECH CIRCUIT WITH POWER MANAGEMENT

- 2/4 WIRES INTERFACE WITH
  - double antisidetone network
  - Rx gain and AC impedance externally programmable
  - AGC attack/disconnect points programmable
- DTMF INTERFACE
- 3.3 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- CURRENT SUPPLY FOR LOUDSPEAKER



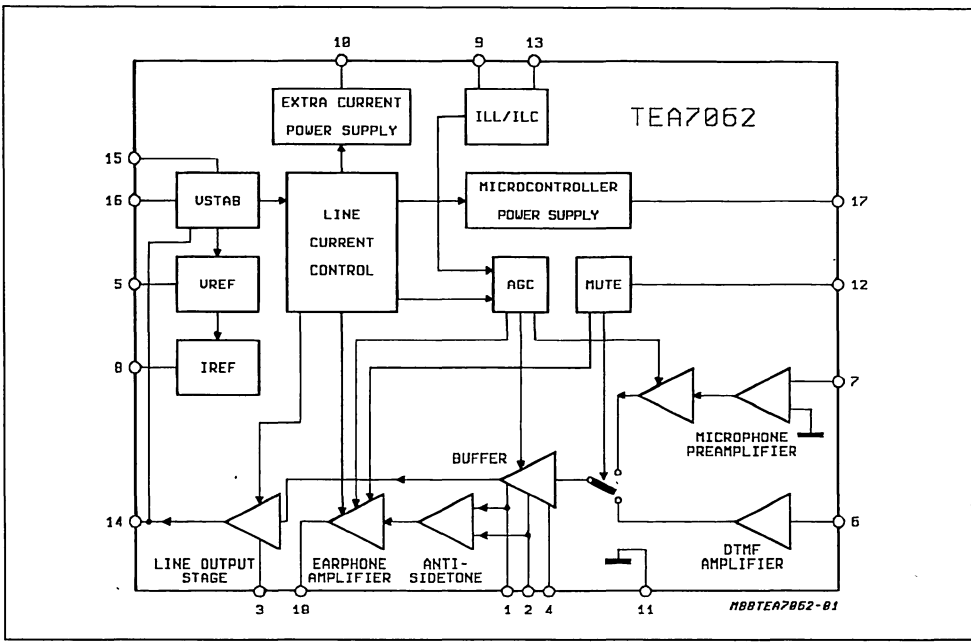
DIP18

ORDER CODE : TEA7062DP

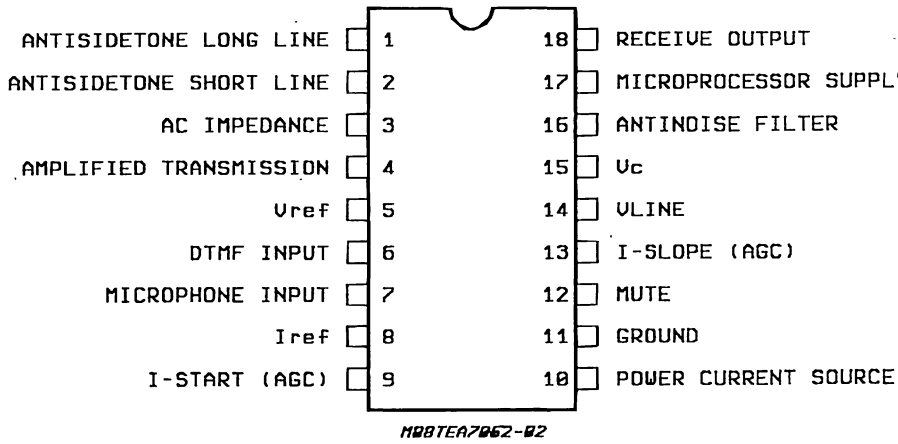
DESCRIPTION

The TEA7062 is designed to meet the different european specifications for telephone set in medium and high range equipments.

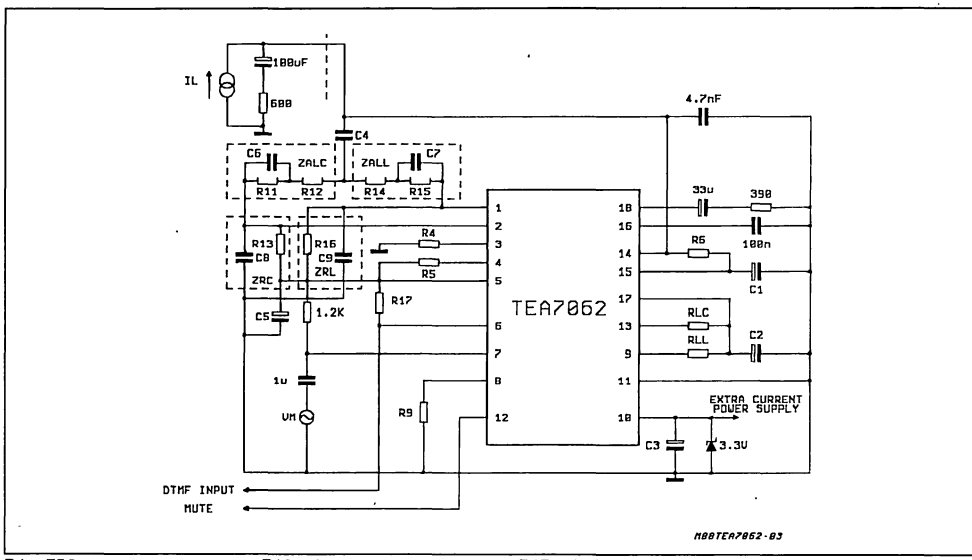
BLOCK DIAGRAM



PIN CONNECTIONS (top view)



TEST CIRCUIT



R4 = 75Ω	R12 = 0Ω	R17 = 1.2KΩ	C5 = 100µF
R5 = 5.1KΩ	R13 = 2.7KΩ	C1 = 47µF	C6 = 27pF
R6 = 18KΩ	R14 = 0Ω	C2 = 4.7µF	C7 = 27pF
R9 = 100KΩ	R15 = 140KΩ	C3 = 220µF	C8 = 1.5nF
R11 = 140 KΩ	R16 = 2.7KΩ	C4 = 1µF	C9 = 1.5nF

ELECTRICAL CHARACTERISTICS

(R_9 = 100KΩ ; T_a = 25°C ; identification of the pins related to DIP-18 unless otherwise noted)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
VC	Stabilized Voltage (pin 15)	I_L = 25mA	2.3	2.5	2.7	V
Iint	Internal Bias Current (pin 15)	I_L = 25mA I_L = 6mA (V14 = R6*Iint + VC)		210 145		µA
Vref	Reference Voltage	I_L = 25mA	1.05	1.2	1.35	V
Iref	Current at Vref		– 10		100	µA
Vmp	Stabilized Supply at Pin 17		3.1	3.3	3.5	V
Icmp mA	Charging Current at Pin 17	Pin 15 = GND	0.6 X I_{line}			mA
Ispm	Static Current at Pin 17	I_L = 6mA I_L > 25 mA	0.5 1.4	1.6		mA
		I_L > 25mA ; R9 = 68K		2.8		mA
Iimp	Internal Consumption		90	120	160	µA
Iea	Supply Current for Parallel Circuits (pin 10)	I_L = 16mA I_L = 30mA I_L = 60mA		5.0 13.0 40.0		mA mA mA
Vmh Vmb	Mute Microphone (pin 12)	ON OFF	1.6		 0.8	V V
Vmh Vmb	Mute Earphone (pin 12)	ON OFF	2.7		 2.1	V V
Gs AGCs	Tx Gain Long Line Line Lenght Control	I_L = 20mA	50 – 7	51 – 6	52 – 5	dB dB
Gmf	DTMF Gain	Pin 12 > 1.6V	34.5	35.5	36.5	dB
THDs	Tx Distortion	I_L > 25mA Vl = 0dBm Vl = 3dBm			 3 10	 % %
Ze	Microphone Impedance		9	12	15	KΩ
Nep	Tx Noise (psophometric)	I_L > 25mA 2KΩ at Pins 5-7		– 70		dBmp
Rs	Tx Attenuation in Mute Mode	I_L > 25mA Pin 12 > 1.6V	60			dB
Gr AGCr	Rx Gain Long Line Line Lenght Control	I_L = 20mA	29 – 7	30 – 6	31 – 5	dB dB
THDr	Rx Distortion	I_L > 25mA Vro = 500mV Vro = 630mV			 3 10	 % %
Nrp	Rx Noise	I_L > 25mA		– 72		dBmp
Rr	Rx Attenuation in Mute Mode	I_L = 25mA Pin 12 > 2.7V	60			dB
Gas	Antisidetone	I_L = 20mA	– 22			dB
Zac	AC Impedance	I_L > 25mA	500	650	800	Ω
Grs	Confidence Level V_{LINE}/V_{REC} in DTMF	Pin 12 > 2.7V	29	32	35	dB

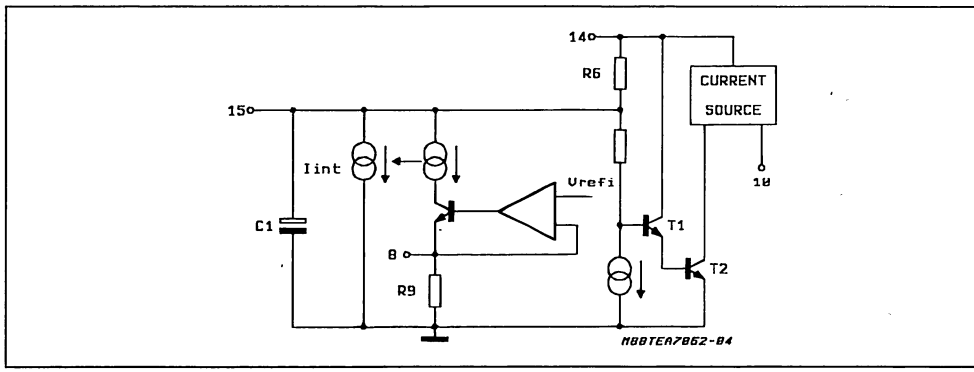
CIRCUIT DESCRIPTION

1. DC Characteristics

1.1 Vc (pin 15). The stabilized voltage Vc is connected to Vline (pin 14) througth an internal shunt regulator T1, T2, which presents to the line a high AC impedance at frequencies higher than 200Hz. At this purpose the value of C1 (at pin 15) must be not lower than 47 microFarad (suggested value is 100µF).

The shunt regulator, T1 and T2, also controls the extra current source, or power management, at pin 10 (see also paragraph 6).

Figure 1.



1.2 V_{LINE} (pin 14). The line voltage (pin 14) is determined by the value of the external resistor R6 and by the internal current, I_{int}, flowing between Vc (pin 15) and Ground (see also paragr. 1.1) :

$V_{LINE} = Vc + R6 \times I_{int}$.

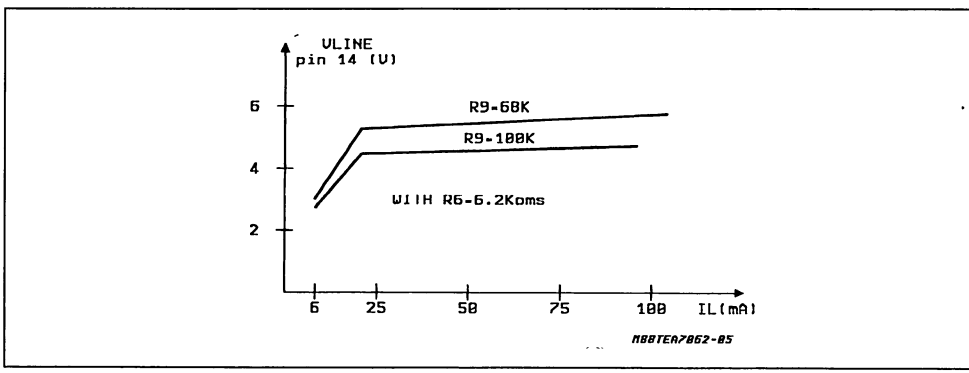
Vc is fixed by design at about 2.5V.

I_{int} is reversely related to R9 (I_{int} = 16V/R9 + 60µA at I_{LINE} > 25mA).

V_{LINE} must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the specific standard of the different administrations.

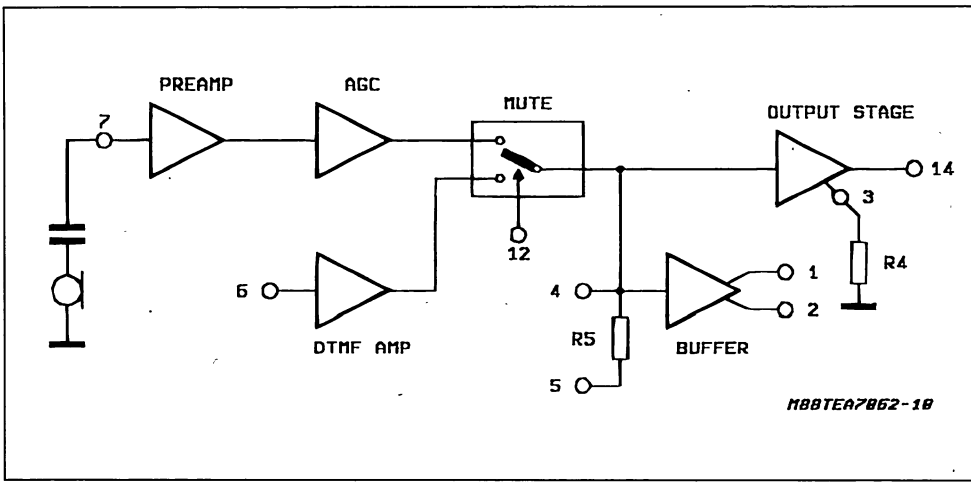
Another adjustment of the DC characteristic is possible with R9. Increasing the value of R9 causes a decrease of I_{int} and consequently a reduction of the product I_{int} x R9.

Figure 2.



2. Transmission Chain

Figure 3.



2.1 A.G.C. IN TRANSMISSION. The transmission gain between Microphone Input (pin 7) and Vline (pin 14) is internally decreased of 6dB when the line current varies from ILL to ILS with a constant AC load of 600Ω.

The values of ILL (long line current) and ILS (short line current) are programmable through I-start (pin 9) and I-slope (pin 13) (see also paragr. 4).

2.2 SENDING IMPEDANCE. The impedance of the Output Stage Amplifier, Zout, is determined by the impedance Z4 (at pin 3).

$$Zout = 10.65 \times Z4.$$

The total AC impedance shown to the line is the parallel

$$Zpar = Zout//Zint//Zext$$

where :

- Zint = 10kΩ//8.5nF (internal)
- Zext = R6//C4 (at pin 14)

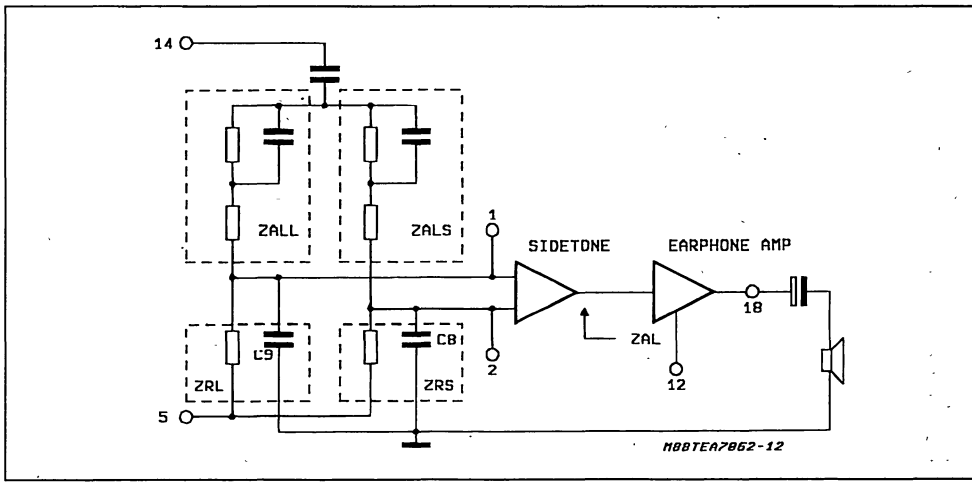
2.3 SENDING MUTE. In normal speech operation (Vmute at pin 12 < 0.8V), the signal at Microphone Input (pin 7) is amplified to Vline (pin 14) with the gain Gs (long line) or up to 6dB lower (shorter lines) depending on AGC control (see paragr. 4).

In sending mute condition (V12 > 1.6V) these gains are reduced of at least 60dB. In the same condition, DTMF input (pin 6) is activated, with gain Gmf to the line independent from Iline.

2.4 ANTISIDETONE BUFFER. The signal coming from the sending preamplifier is internally presented at pin 4 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2).

3.Receive Chain

Figure 4.



3.1 A.G.C. IN RECEIVE. As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 24, have a reduction of 6dB when Iline moves from ILL to ILS (see also paragr. 4).

3.2 SIDETONE COMPENSATION. The circuit is provided with a double anti-sidetone network to optimize both at long and short lines.

In case double antisidetone network is not requested by the application needs, pins 1 and 2 can be connected to each other and 5 external passive components can be saved (ZALL and ZRL).

Before entering pins 1 and 2, the received signal is areduced by the two attenuating networks :

-ZALL/ZRL to pin 1 for long lines sidetone compensation,

-ZALS/ZALS to pin 2 for short lines sidetone compensation.

ZRL and ZRC define the total receive gains :

a) $\frac{V18}{V14} = Gr \times \frac{ZRL}{ZRL+ZALL}$ for long lines

b) $\frac{V18}{V14} = (Gr - 6dB) \times \frac{ZRS}{ZRS+ZALS}$ for short lines

ZALL and ZALS define the sidetone compenstaion of the circuit.

The equivalent balancing impedance is given by the formula :

ZAL = K x ZALS + (1 - K) x ZALL

where :

-K = 0 at Iline = ILL or lower (long line)

-K varies from 0 to 1 with Iline between ILL and ILS

-K = 1 at Iline = ILS or higher (short line).

Calculations to define ZALL and ZALS are :

a)
$$ZALL = 70 \times R5 \times \frac{Zline\ (long)//Zext//Zint//Zout}{Zout}$$

b)
$$ZALS = 70 \times R5 \times \frac{Zline\ (short)//Zext//Zint//Zout}{Zout}$$

where :

- Zext = R6//C4//(Zelectret) (at pin 11)
- Zint = 10Kohms//8.5nF (internal impedance)
- Zout = 10.65 * Z4 (at pin 3 ; see paragr. 2.2)
- Zline (short) and (long) are the impedances of the line at minimum and maximum line length
- R5 = 5.1Kohm ± 1%

3.3 AC IMPEDANCE. The total AC impedance of the circuit to the line is :

ZAC = Zout//Zint//Zext//ZALS//ZALL (see par. 2.2 and 3.2)

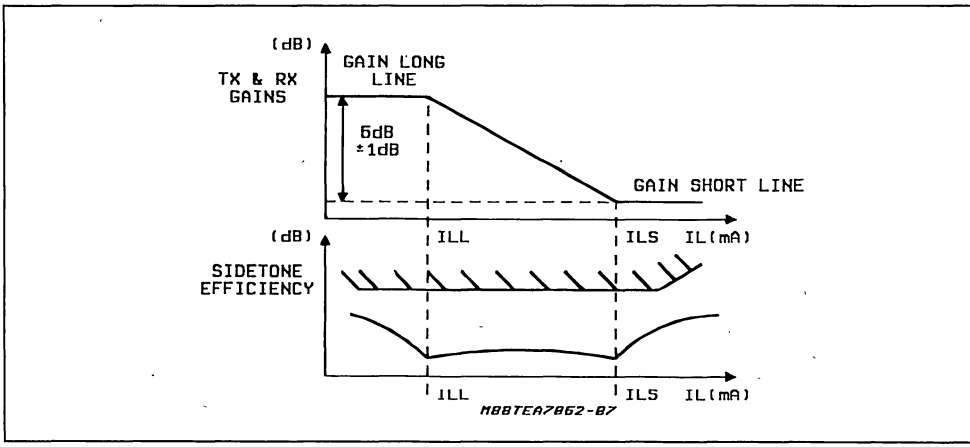
ZAC = Zout//Zint//Zext (ZALS, ZALL>>ZAC)

3.4 RECEIVE MUTE (and confidence level). When the receive channel is muted (Vpin 12 > 2.7V) the receive gain is reduced of 60dB minimum.

In this condition an internal connection is activated from line DTMF output (pin 16) to Receive Output (pin 18) with a gain Gmf = 32dBto provide acoustic feedback of the DTMF transmission.

4. A.G.C. and Sidetone Programming

Figure 5.



4.1 PROGRAMMABLE CONTROLS. AGC and sidetone attack and disonnect points (or currents) are programmable externally through two independents pins, I-start (pin 19) and I-slope (pin 13).

4.2 I-START (pin 9). An external resistor RLL connected between I-start (pin 9) and Microprocessor Supply (pin 17) controls the attack point of AGC and ZAL (antisedetone Z).

ILL is the line current at which the control starts. Formulas for ILL and RLL with R9 = 100K are :

$$ILL \frac{2880}{RLL} + 11mA$$

$$RLL \frac{2880}{(ILL - 11mA)}$$

4.3 I-SLOPE (pin 13)

An external resistor RLS connected between I-slope (pin 13) and Microprocessor Supply (pin 17) controls the disconnect point of AGC and ZAL (antisidetone Z). ILS is the line current at which the control stops. Formulas for ILS and RLS with R9 = 100K are :

$$ILS = \frac{4680}{RLS} + ILL;$$

$$RLS = \frac{4680}{(ILS - ILL)}$$

4.4 A.G.C. OFF (pin 9 and 13). Programming ILL and ILS respectively higher than 70mA and 450mA is forcing the IC in AGC OFF Condition.

Suggested external components are : RLL = 51kohm and RLS = 10Kohm.

Sending, receiving gain and sidetone compensation are so independent of the line lenght. Pins 1 and 2 can be connected to each other saving 5 passive external components at pin 2.

4.5 SECRET FUNCTION FOR PRIVATE (pin 12). The two separate thresholds for sending and Receiving Mute (pin 12) allow "Secret Function" (only microphone muted).

Pin 12 can be set :

a) between 0V and 0.8V for speech mode,

b) between 1.6V and 2.1V for "secret" mode (micro phone muted),

c) between 2.7V and 3.3V for "all muted" mode

5. Microprocessor Interface

5.1 MICROPROCESSOR SUPPLY (pin 17). At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 17) to charge quicly the external capacitor C2.

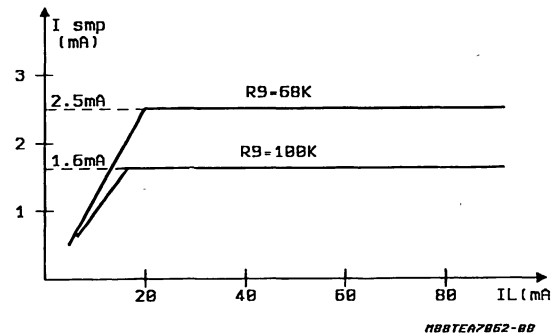
This charging current is Icpm = 0.6 x I_{LINE}.

T-charge of about 1 msec is necessary, with C2 = 4.7/µF, to charge pin 17 at the specified value of 3.3V typical :

$$T\text{-charge} = \frac{3.3V \times C2}{0.6 \times I_{LINE}} \text{ typically.}$$

Vmp = 3.3V in normal operation and current increases linearly from 0.5 mA min, at I_{LINE} = 6mA, to 2.5mA, at I_{LINE} = 25mA, remaining stable for higher values of I_{LINE}.

Figure 6.



6. Power Management

6.1 POWER MANAGEMENT(pin 10). Most of the DC current available from the line be delivered by the speech circuit at the output Isource (pin 10) through an internal current generator.

Typical values of this current, Iea with R9 = 100K, are :

Iea = (0.3 xI_{LINE}) for I_{LINE} < 16.5mA

Iea = (0.9 x I_{LINE} - 10mA) for I_{LINE} >16.5mA

(ex : I_{LINE} = 16mA then I_{ea} = 5mA

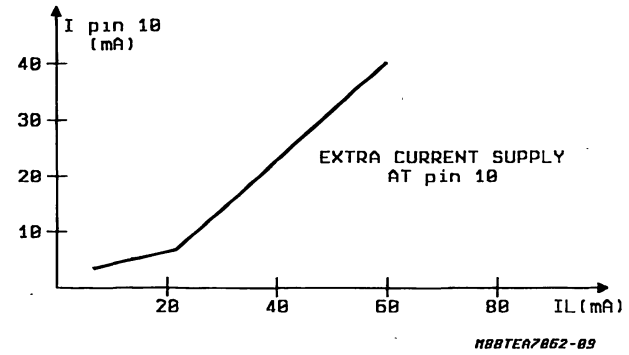
I_{LINE} = 30mA then Iea = 17mA

I_{LINE} = 60mA then Iea = 11mA).

The voltage level at pin 10 must be defined by an external regulator (i.e. : zener) and, if necessary, filtered with a capacitor (47 to 220 microF).

In case V_{LINE} (at pin 14) approaches voltage at pin 10, then the internal current source switches off and its DC current is shunt to ground through an internal complmentary generator, thus avoiding any negative effect on the AC and DC impedances of the telephone set application.

Figure 7.

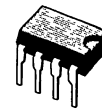

I pin 10
(mA)
40
30
20
10
EXTRA CURRENT SUPPLY
AT pin 10
20
40
60
80
IL(mA)
MBBTEA7062-09

TONE RINGERS

ML8204
ML8205

TONE RINGER

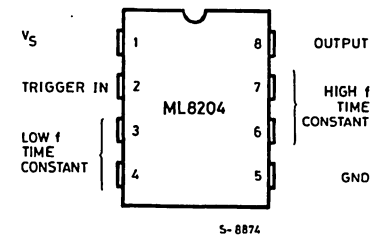
- DESIGNED FOR TELEPHONE BELL REPLACEMENT
- LOW CURRENT DRAIN
- SMALL SIZE "MINIDIP" PACKAGE
- ADJUSTABLE 2-FREQUENCY TONE
- ADJUSTABLE WARBLING RATE
- BUILT-IN HYSTERESIS PREVENTS FALSE TRIGGERING AND ROTARY DIAL "CHIRPS"
- EXTERNAL TRIGGERING OR RINGER DISABLE (ML8204)
- ADJUSTABLE FOR REDUCED SUPPLY INITIATION CURRENT (ML8205)
- TELEPHONE SET TONE RINGERS
- EXTENSION TONE RINGER MODULES
- ALARMS OR OTHER ALERTING DEVICES



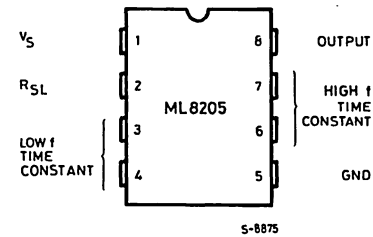
MINIDIP

ORDER CODE : ML8204
ML8205

PIN CONNECTIONS (top view)



S-8874

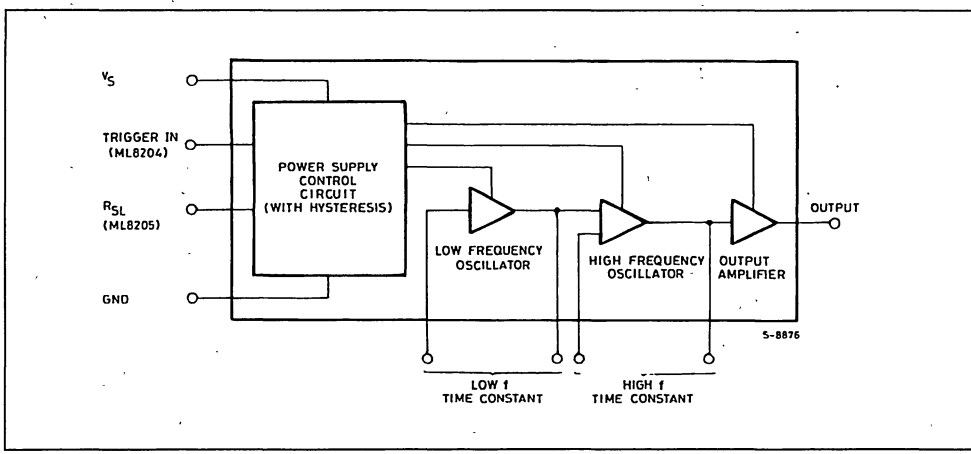


S-8875

DESCRIPTION

The ML8204/ML8205 tone ringers are monolithic devices, each incorporating two oscillators, an output amplifier and a power supply control circuit. The oscillator frequencies can be adjusted over a wide range by selection of external components. One oscillator, normally operated at a low frequency (f_L), causes the second oscillator to alternate between its nominal frequency (f_{H1}), and a related higher frequency (f_{H2}). The resulting output is a distinctive "warbling" tone. The output amplifier will drive either a transformer coupled loudspeaker or a piezo-ceramic transducer. The device can be powered from a telephone line or a fixed d.c. supply. The power supply control circuit has built-in hysteresis to prevent false triggering and rotary dial "chirps". The ML8204 can be triggered externally under logic control. The ML8205 has provision for adjustment of the power supply initiation current.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_S	Supply Voltage - GND	30	V
T_{op}	Operating Temperature	– 45 to + 65	°C
T_{stg}	Storage Temperature (E package)	– 65 to + 150	°C
P_{tot}	Total Power Dissipation (E package)*	400	mW

Stresses in excess of thos listed unter "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	6.3	mW/°C

ELECTRICAL CHARACTERISTICS (all voltages referenced to GND unless otherwise noted T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage				29	V
V_{si}	Supply Initiation Voltage(1)	Trigger in Open Circuit (ML8204)	17	19	21	V
V_{sus}	Sustaining Voltage(2)		9.7	11	12	V
I_{si}	Supply Initiation Current	No Load $V_s = V_{si}$ R_{SL} = 6.8 kΩ (ML8205)	1.4	2.5	4.2	mA
I_{sus}	Sustaining Current	No Load $V_s = V_{sus}$	0.7	1.2		mA
V_{TR}	Trigger Voltage(3)		10.5			V
I_{TR}	Trigger Current(3)		40		1000(5)	µA
V_{DIS}	Disable Voltage(4)				0.8	V
I_{DIS}	Disable Current(4)		– 50			µA
V_o	Output Voltage	No Load V_s = 21 V	17	19	21	V
f_o	Oscillator Frequency Tolerance	Component Tolerance Excluded			± 7	%

Notes : 1. V_{si} is the value of supply voltage which must be exceeded to trigger oscillation.
2. V_{sus} is the value of supply voltage required to maintain oscillation.
3. V_{TR} and I_{TR} are the conditions applied to Trigger In to start oscillation for $V_{SUS} \leq V_S \leq V_{SI}$.
4. V_{DIS} and I_{DIS} are the conditions applied to Trigger In to inhibit oscillation for $V_{SI} < V_S$.
5. Trigger Current must be limited to this value externally.

Figure 1a : Supply Current vs. Supply Voltage (no lead).

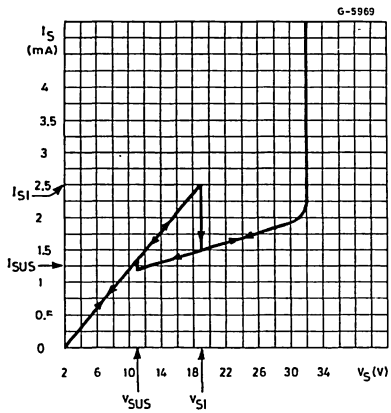
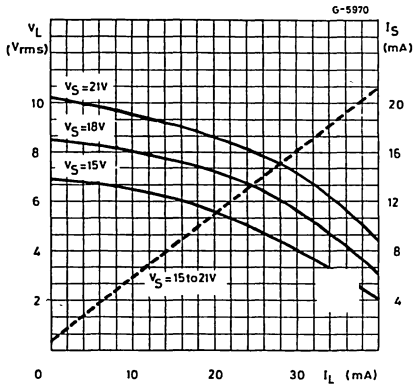


Figure 1b : Load Voltage and Supply Current vs. Load Current.



FUNCTIONAL DESCRIPTION

The M8204/ML8205 Tone Ringers are primarily intended for use as replacements for the mechanical bell in telephone sets. Each incorporates two oscillators, an output amplifier and a power supply control circuit. The devices can be powered directly from the telephone line using the a.c. ringing voltage, or they may be powered from a separate d.c. supply. The output amplifier is capable of driving a wide range of load impedances when powered from a low impedance supply. The power supply control circuit provides the hysteresis required to ensure positive triggering of the device and to prevent transient triggering due to dial pulsing.

As the power supply voltage to the ML8204/ML8205 is increased up to the supply initiation voltage (V_{SI}), the supply current also increases up to (I_{si}). When V_{SI} is exceeded, oscillation begins and the static power supply current decreases (see fig. 2a). The low frequency oscillator (LFO) oscillates at a rate (f_L) controlled by an external resistor and capacitor. The frequency can be determined using the relation $f_L = 1/(1.234RC)$ where R is the value of the resistor connected between pins 3 and 4, and C is the value of the capacitor connected between pin 3 and ground.

The output of the LFO is internally connected to the switching threshold circuitry of the high frequency (HFO). When the output of the LFO is high, HFO oscillates at its nominal rate (f_{H1}), described by the relation $f_{H1} = 1/(1.515RC)$ where R is the value of the resistor connected between pins 6 and 7, and C is the value of the capacitor connected between pin 6 and ground. When the output of the LFO is low, the HFO oscillates at a higher rate (f_{H2}) described by the relation $f_{H2} = 1.25\ f_{H1}$. Thus the LFO sets the warbling rate : the rate at which the HFO switches between the two tone frequencies f_{H1} and f_{H2}. Oscillation continues until the supply voltage decreases below the sustaining voltage (V_{sus}). At this point, the power supply current undergoes a step increase (from I_{sus}), and then ramps down in accoardance with the supply voltage.

In normal applications, Trigger in (pin 2) of the ML8204 is left open circuit. This pin allows external triggering of oscillation of the ML8204 at supply voltages in the range $V_{sus} \leq V_s \leq V_{si}$. To do so, a voltage at least equal to the minimum trigger voltage (V_{TR}) must be applied to pin 2.

Triggering the device is accomplished by sourcing a minimum current (I_{TR}) into pin 2. This current must be limited to prevent damage to the triggering circuit. Tone ringer oscillation may also be inhibited at supply voltages in the range $V_{si} < V_s \leq V_{s(max)}$ by applying a maximum disable voltage (V_{DIS}) to pin 2. Disabling is accomplished by sinking a minimum current (I_{DIS}) out of pin 2. (See Applications Section for details on the operation and use of the Trigger in pin).

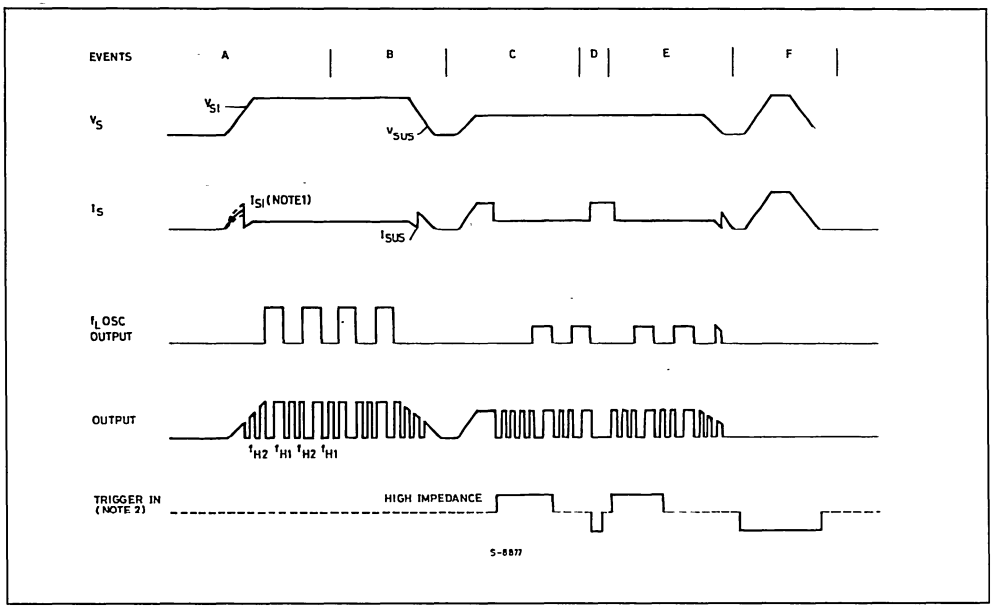
The ML8205 requires the connection of a resistor, R_{SL}, to program the slope of its supply current versus supply voltage characteristic prior to triggering ($V_s \leq V_{si}$). This in turn determines the maximum supply initiation current (I_{si} drawn at the initiation voltage (V_{si})). Programming is accomplished by connecting a slope determining resistor, R_{SL}, between pin 2 and ground. The value of I_{si} varies inversely with the value of R_{SL}. This feature can be used to control effective impedance presented to the telephone line by the ringer circuit. (See Applications section for detailed description on the operation and use of the R_{SL} pin).

The output amplifier of the ML8204/ML8205 is capable of driving a wide range of load impedances when driven from a low source impedance power supply. When the device is powered from a telephone line, load impedance should be kept fairly high (800 or greater) to prevent power supply regulation problems. A transformer is thus required for driving loudspeakers as is an output coupling capacitor. Piezo-ceramic transducers may be driven directly. However, the tone frequencies f_{H1} and f_{H2} must normally be set higher (around 2 KHz) to ensure that the transducer delivers sufficient acoustic power. (Suitable piezo-ceramic transducers typically have maximum efficiency around 2 KHz). It is also necessary to connect a zener diode in parallel with the transducer to limit voltage surges generated by the transducer during mechanical shocks.

Table 1.

N°	Pin function	Description
1	V_{SS}	Positive Power Supply
2	Trigger in	ML8204 - Oscillator External Trigger/Inhibit pin (must be connected through a current limiting resistor when used)
	R_{SL}	ML8205 - Initiation Current (I_{SI}) Programmming Pin. (must be connected)
3	Low f Time Constant	Low Frequency Time Constant Adjustement Pins. Used to Set Frequency Oscillator Switches f1 (by connection of appropriate resistor and capacitor. see fig. 3)
5	GND	Negative Power Supply
6	High f Time Constant	High Frequency Time Constant Adjustement Pins Used to Set Nominal Tone Output Frequency (f_{H1}) (by connection of appropriate resistor and capacitor. see fig. 3)
8	Output	Tone Output. (must be capacitively coupled for transformer coupled or resistive loads)

Figure 2 : ML8204/ML8205 Timing Diagram.



1. I_{SI} varies with R_{SL} on ML8205.
2. Trigger in on ML8204 connected through current limiting resistor.

A) Oscillation triggered by $V_s > V_{si}$.
B) Oscillation maintained until $V_s < V_{sus}$.
C) Oscillation triggered by trigger in high for $V_{sus} \leq V_s \leq V_{si}$.
D) Oscillation stopped by trigger in low for $Vs \geq V_{sus}$.
E) Oscillation triggered by trigger in high, maintained until $V_s < V_{sus}$.
F) Oscillation inhibited by trigger in low for $V_s > V_{si}$.

APPLICATIONS

TYPICAL TELEPHONE OR EXTENSION TONE RINGER CIRCUIT

The circuit shown in fig. 3 illustrates the use of the ML8204/8205 devices in a typical telephone or extension tone ringer application. The a.c. ringing voltage appears across the TIP and RING inputs of the circuit and is attenuated by capacitor C_1 and resistor R_1. C_1 also provides isolation from d.c. voltages on the line. After full wave rectification by the diode bridge BR_1, the waveform is filtered by capacitor C_4 to provide a d.c. supply for the tone ringer chip. As this voltage exceeds the initiation voltage, V_{si}, oscillation starts. With the components shown, the output frequency chops between 512 Hz (f_{H1}) and 640 Hz (f_{H2}) at a 10 Hz (f_L) rate. The loudspeaker load is coupled through a 1300 Ω to 8 Ω transformer. While the output impedance of the ML8204 is quite low, the load impedance must be kept fairly high. This is to prevent d.c. power supply regulation problems due to high source impedance of the telephone line and coupling components C_1 and R_1. The output coupling capacitor C_5 is required with transformer coupled loads. The value shown (0.22 µF) presents a high enough impedance at the nominal ringing frequency to allow connection of fairly low impedance loads without upsetting the supply regulation. If the load impedance is large enough, then the value of this capacitor can be increased to couple more power to the load without upsetting the power supply to the ML8204. Potentiometer P_1, is used to adjust the audio amplitude and resistor R_4 is a current limiting resistor. Resistor R_5 is a quenching resistor used to limit back emf generated by the inductive load when ringing stops. When driving a piezo-ceramic transducer type load, the coupling capacitor C_5 is not required. However, a current limiting resistor is required as is a 29 V zener diode in parallel with the transducer. This diode limits the voltage transients than can generated by mechanical shocking of a piezo-ceramic transducer. The electrical characteristics shown in Table 2 indicate typical performance of this circuit. The incoming ringing voltage and frequency are determined by the telephone system.

Figure 3 : Typical Tone Ringer Circuit.

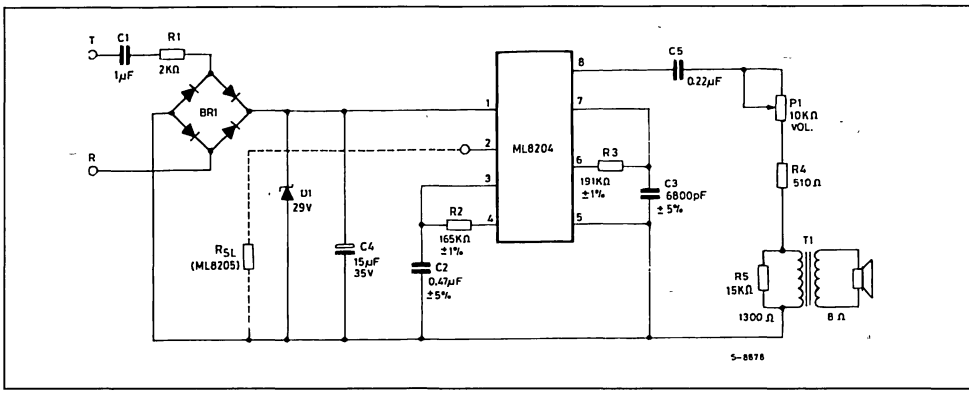


Table 2 : Typical Electrical Characteristics of Tone Ringer Circuit (fig. 3).

Parameter	Min.	Typ.	Max.	Unit	Parameter	Min.	Typ.	Max.	Unit
Input Voltage	75	88	120	V_{rms}	Output Frequencies				
Input Frequency	16	20	60	Hz	f_L f_{H1} f_{H2}	9 461 576	10 512 640	11 563 704	Hz Hz Hz
Input Current (when ringing)	–	8	11	mA_{rms}	Output Voltage (Pin 8 '0' loop)	–	25	–	V_{PP}
Output power (into 8 transformer coupled load)	–	40	–	mW	Output Sound Pressure	80	85	90	dBA

USE OF TRIGGER IN (pin 2 ML8204)

Pin 2 of the ML8204 may be used to a) externally trigger oscillation for voltages in the range $V_{sus} \leq V_S \leq V_{si}$, or b) disable ringer operation. The equivalent circuit at pin 2 is shown in Fig. 5. The ringer circuit can only oscillate when Q_1 is conducting. Normally when supply voltage V_S exceeds the supply initiation voltage (V_{si}), base current flows into Q_1, via D_2 and D_1 causing Q_1 to conduct. This continues until V_S is taken below the minimum sustaining voltage (V_{sus}).

The ML8204 can be made to oscillate when powered from supply voltages in the range $V_{sus} \leq V_S \leq V_{si}$.

Oscillation is ensured by forcing a current I_{TR} (10 µA $\leq I_{TR} \leq$ 1 mA) into pin 2 to provide base current to Q_1. This requires the voltage applied to pin 2 to exceed V_{TR} where V_{TR} is the sum of the zener voltage of D_3, the forward voltage drop of D_2 and the V_{BE} of Q_1 (typically 11 V). The required current drive can be provided by connecting a resistor R_E between pin 1 and V_S (Fig. 5a) ; where : 20 KΩ ≤ R_E ≤ (V_S - 11)/10 MΩ. To operate the ML8204 from a d.c. 12 V supply, R_E should be typically 50 K. This mode of operation can also be used to reduce the effective value of the V_{si}, by inserting a zener diode in series with R_E (fig. 5b). This modifies the initiating voltage to $V_{si\ (Eff)} = V_{TR} + V_E + 10\ R_E$ (R_E is in MΩ).

Figure 4 : Pin 2 Input Equivalent Circuit.

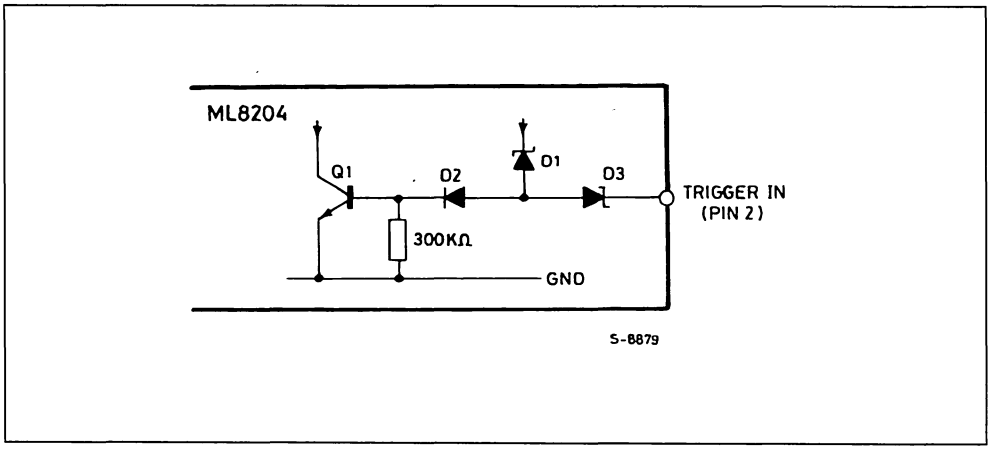
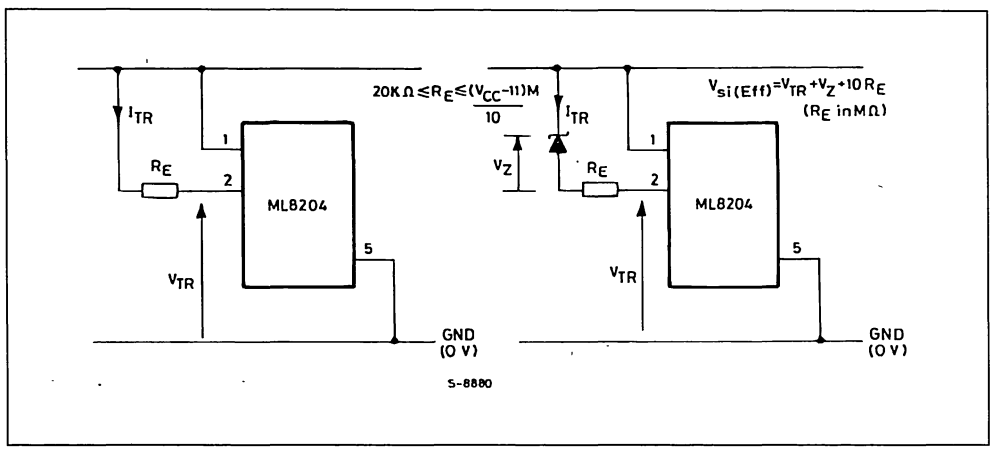


Figure 5a : Enabling Oscillation of the ML8204 for Supply Voltages less than V_{si}.

Figure 5b : Reducing the Effective Value of V_{si} for the ML8204



Oscillation of the ML8204 may be inhibited for voltages in the range $V_{si} < Vs \leq V_{s(max)}$ by sinking the current from D_1, starving Q_1 of base current. This is achieved by either a) grounding pin 2 (fig. 6a), or b) applying a voltage V_{INH} via a resistor R_1 to pin 2 (fig. 6b) to ensure that :

V_{DIS} 0.8 V, and $I_{DIS} = \frac{V_{DIS} - V_{INH}}{R_1} \geq 40\ \mu A.$

When driven from a fixed d.c. supply, oscillation of the ML8204 may be gated on or off by CMOS or TTL logic as shown in Fig. 7a and Fig. 7b respectively.

Figure 6 : Inhibiting Oscillation of the ML8204.

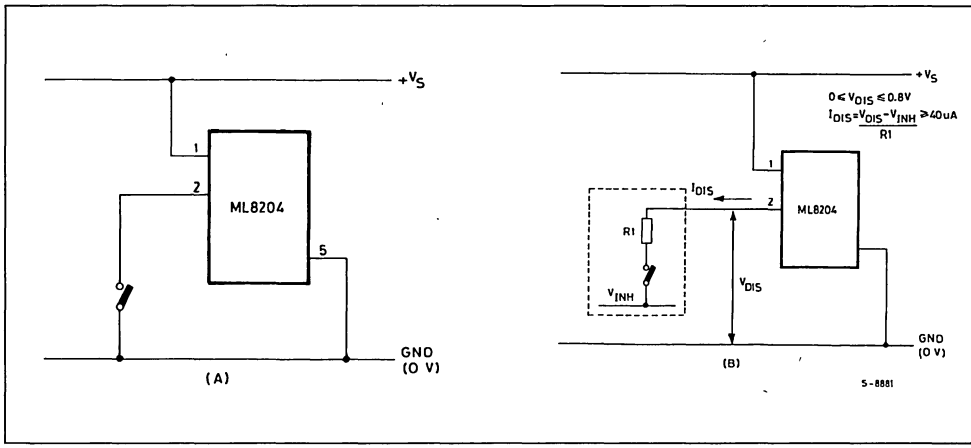


Figure 7a : Gating the ML8204 from CMOS.

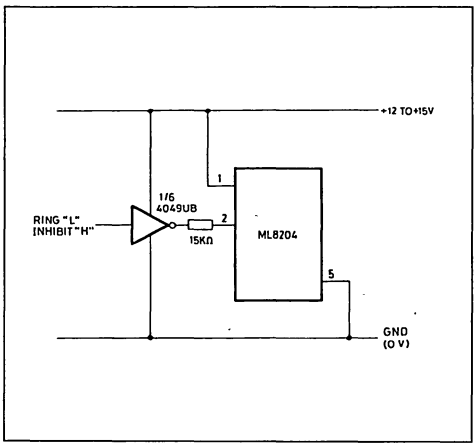
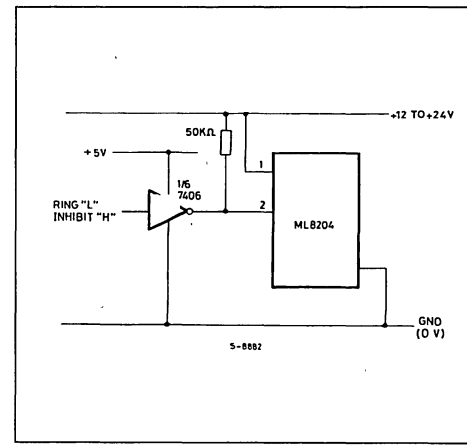


Figure 7b : Gating the ML8204 from TTL.



PROGRAMMING THE ML8205 INITIATION CURRENT

Pin 2 of the ML8205 requires connection of an external resistor R_{SL} (fig. 8), which is used to program the slope of the supply current vs, supply voltage characteristic, and hence the supply current up to the initiation voltage (V_{si}). This initiation voltage remains constant independent of R_{SL}. The supply initiation current (I_{si}) varies inversely with R_{SL}, decreasing for increasing values of resistance. Thus, increasing the value of R_{SL} will decrease the amount of a.c. ringing current required to trigger the device, As such, longer subscriber loops are possible since less voltage is dropped per unit length of loop wire due to the lower current level. R_{SL} can also be used to compensate for smaller a.c. line coupling capacitors (providing higher impedance) which can be used alter the ringer equivalence number of a tone ringer circuit.

The graph in fig. 9a illustrates the variation of supply current with supply voltage of the ML8205. Three curves are drawn to show the change in the slope of the I-V characteristic with R_{SL}. Curve B (R_{SL} = 6.8 KΩ) shows the I-V characteristic for the ML8204 tone ringer. Curve A is a plot with R_{SL} = 5.0 KΩ and shows an increase in the current drawn up to the initiation voltage V_{si}. The I-V characteristic after initiation remains unchanged. Curve C illustrates the effect of increasing R_{SL} to 13.0 KΩ. Initiation current decreases but again current after trigging is unchanged. The variation of I_{si}, with R_{SL} is illustrated in fig. 9b.

Figure 8 : Adjusting I_{si} by Varying R_{SL}.

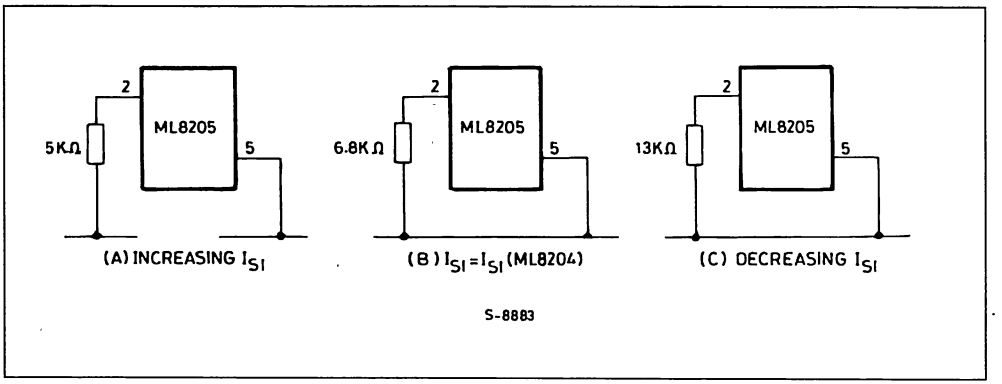


Figure 9a : I-V Slope Change Due to R_{SL}.

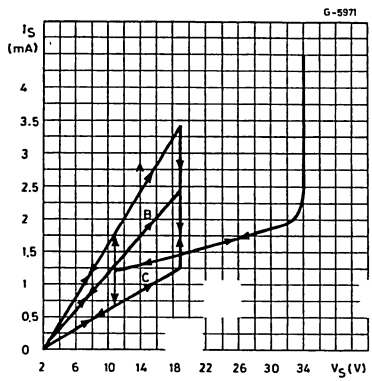
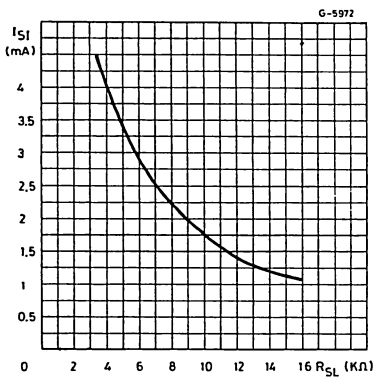


Figure 9b : Supply Initiation Current. (I_{si}) vs. R_{SL}.



MITEL F.C.C. APPROVED TONE RINGER MODULE USING ML8205

The Mitel tone ringer module (CM3215) using the Mitel ML8205 tone ringer chip in the circuit below (fig. 10) has been approved by the F.C.C. (F.C.C. reg. number BN285B673550TN). The circuit has been given a ringer equivalence of 0.7 B. This accomplished by increasing the value of R_{SL} to 13 KΩ which reduces the supply initiation current (I_{si}). This reduction in I_{si} allows the use of higher line coupling components (R_1 = 8.2 KΩ) while ensuring sufficient voltage drop between pins 1 and 5 of the ML8205 for triggering. The 5.1 V zener diode D_1 presents a high impedance to low level signals on the telephone line while allowing tone ringer powering from high level rigging voltages.

TRANSIENT OVERVOLTAGE TESTING OF THE ML8204 TONE RINGER

The following tests were performed to investigate the ability of the ML8204 to withstand transients on its power supply rails. All tests were performed using the circuit shown in fig. 11 with transient voltage pulses of the form shown in fig. 12. After each application of a transient pulse, functionality of the device was checked by switching S_1, S_2, and S_3 to the configuration shown in fig. 11.

Figure 10 : F.C.C. Approved Tone Ringer Circuit.

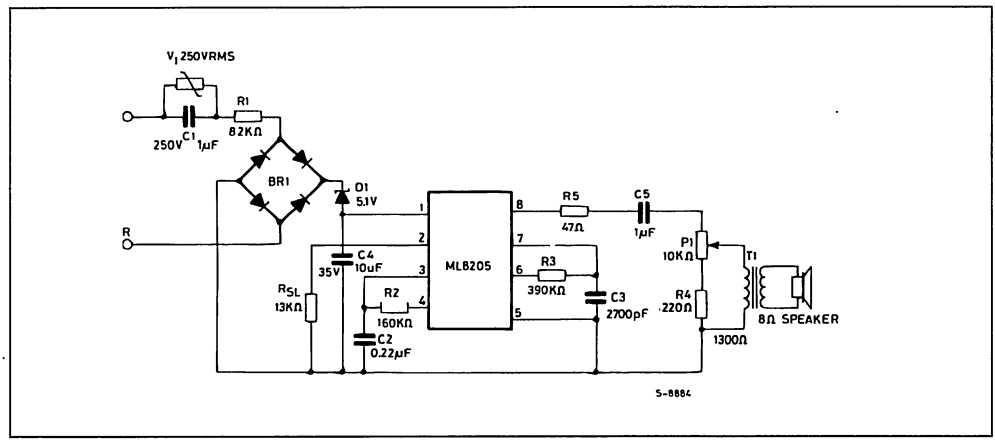
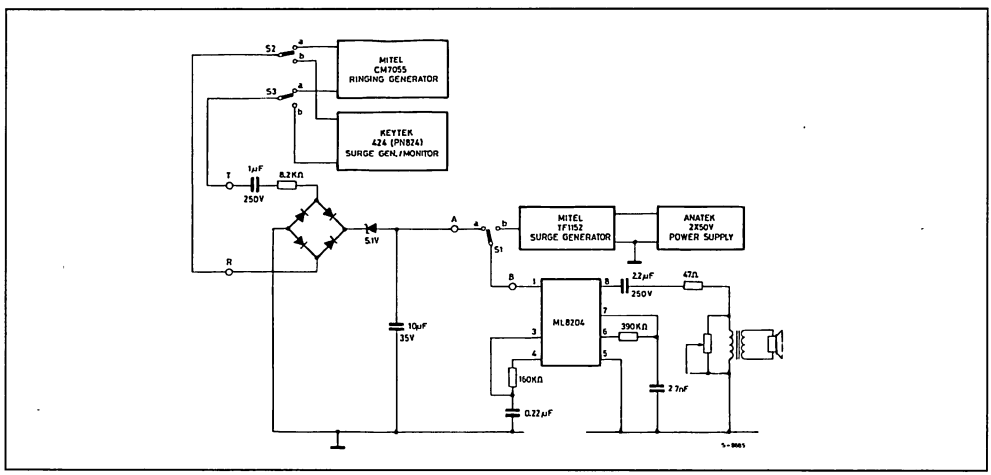


Figure 11 : ML8204 Test Circuit (power supply transient).



The device was tested in two ways by applying pulses : 1) directly into the ML8204 power supply pins, and 2) to the complete ringer circuit TIP and RING inputs. In the first case with S_1 in position "b", a series of pulses with magnitudes (V) from 30 V upwards applied from the TF152 until the ML8204 falled to operate. This was repeated for 10 devices. The unloaded value of V at which the devices ceased to operate varied from 84 to 88 V (V_{BK}). Subsequently a number of devices were tested by applying 70 V pulses to each device. Instability was noted in some devices after 100 pulse applications. All devices ceased to function after 172 to 203 pulse applications. A further set of devices were tested with 64 V pulses. All devices withstood 300 pulse applications without any sign of degradation. In the second test, with switches S_2 and S_3 in position "b" and S_1 in position "a", 800 and 1500 V pulses were repeatedly applied to the TIP and RING inputs of the circuit. No degradation of the devices' operation was observed.

SINGLE TONE OPERATION OF THE ML8204/ML8205

The ML8204/ML8205 can be made to oscillate at one or the other of its output tone frequencies f_{H1} or f_{H2}. To do so, the tone frequency determining components are connected to pins 6 and 7 as normally done. Pin 3 is used as a control input. When pin 3 is connected to V_s, the output (pin 6) will oscillate at the f_{H1} frequency. Conversely, when pin 3 is at ground, the output will oscillate at the f_{H2} frequency. The output can thus be switched between f_{H1} and f_{H2} externally by applying a control signal to pin 3. The low frequency oscillator may also be used separately by connecting the frequency determining components between pins 3 and 4 as normally done. The output is taken from pin 4. However, this is a fairly high impedance output.

Figure 12 : Typical Transient Tset Waveform.

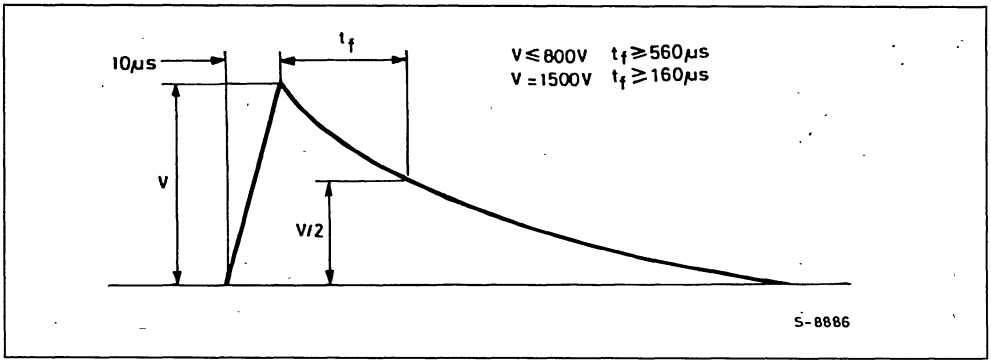
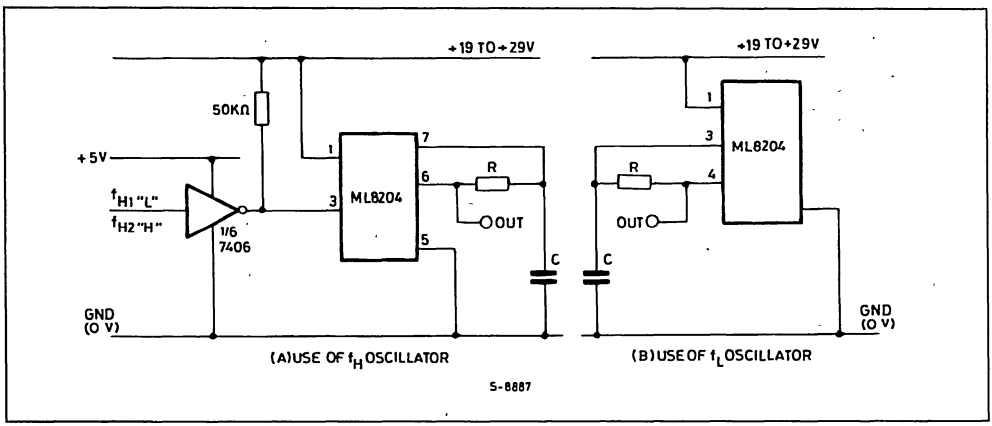


Figure 13 : Single Tone Operating of ML8204/ML8205.



TYPICAL APPLICATION CIRCUITS FOR USE WITH A PIEZO-ELECTRIC TRANSDUCER

Feedback from a piezo-electric transducer can cause spurious oscillations on the output of a ML8204/5 tone ringer. These oscillations corrupt the normal two-tone output and change as the ringer switches off.

The oscillations occur because the piezo electric transducer resonates at its characteristic frequency. If the resonant amplitude is sufficient to pull pin 8 one bipolar threshold below pin 5 then the tone ringer may give a short spurious pulse.

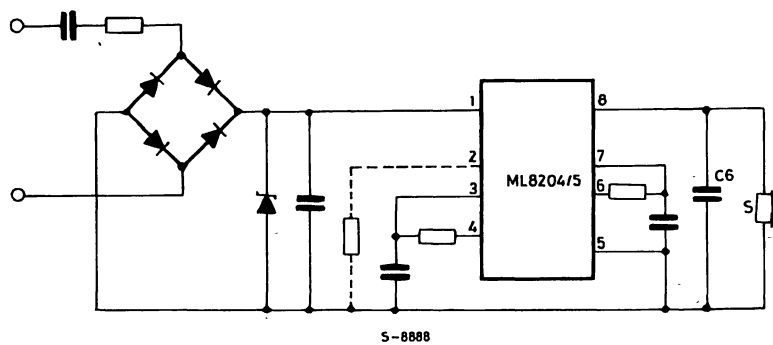
This effect can be eliminated by using a bypass capacitor across the transducer as shown in fig. 14. The size of this capacitor is obviously dependent on the piezo-electric transducer used, but a value of 0.1 µF is usually sufficient.

It is possible under specific conditions for a ML8204/5 tone ringer with a piezo-electric load to continue oscillating after the ringing voltage stops. The ringer can be powered by the smoothing capacitor which is across pins 1 and 5 (see fig. 14). This causes the device to switch off slowly and since the output frequencies shift by about a musical semitone before oscillation stops, the output can have an unpleasant tail-off.

To eliminate this, a simple monitor can be used which switches the output off when ringing stops. fig. 16 shows a circuit which works with an ML8204. When ringing voltage is applied from the line, pin 2 is held between 2 and 10 V and the device functions normally. When ringing stops, pin 2 is pulled to ground and the ML8204 switches off.

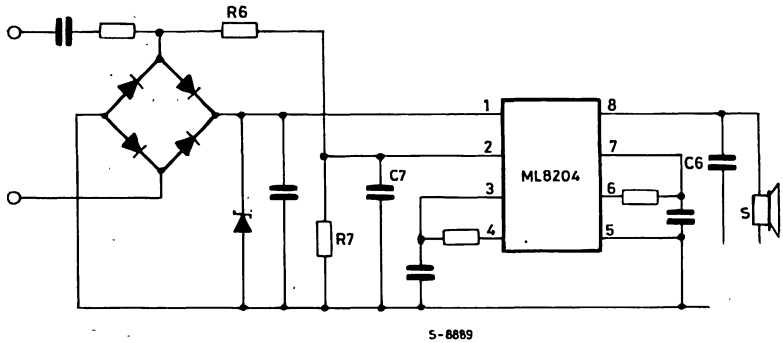
There is no enable on the ML8205 corresponding to pin 2 on the ML8204. Fig. 16 shows a circuit which does not require the enable pin. The output is switched through an NPN transistor instead. During ringing the base of the transistor is forward biased and the load is enabled. When ringing stops the transistor switches off and deactivates the load.

Figure 14 : Typical Application Circuit for Use with a Piezo-electric Transducer..



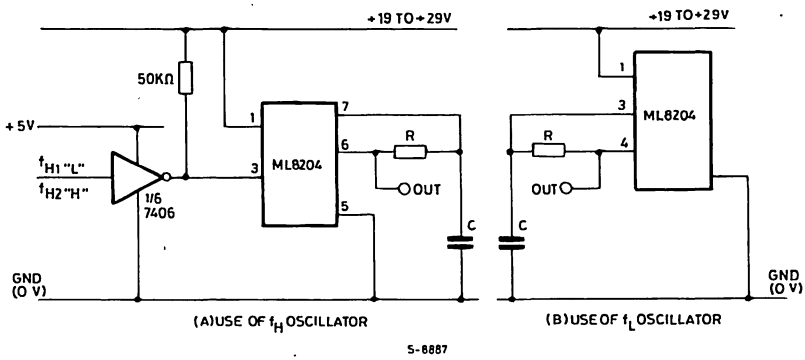
C6 = 01 µF
S = Piezo-electric transducer
Other components same as figure 3

Figure 15 : ML 8204 Circuit to Eliminate Tail-off.



C6 = 0.1 µF
C7 = 4.7 µF
R6 = 51 KΩ
R7 = 22 KΩ
S = Piezo-electric Transducer
Other Components Same as fig. 3

Figure 16 : ML8204/5 Circuit to eliminate Tail-off.

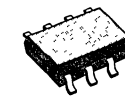


C6 = 0.1 µF
C7 = 4.7 µF
R6 = 51 KΩ
R7 = 22 KΩ
S = Piezo-electric Transducer
Other Components Same as fig. 3

ELECTRONIC TWO-TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF 4 DEVICES
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVERVOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS
- BRIDGE OUTPUT CONFIGURATION

Minidip



SO-8J

ORDER CODES : L3240B (Minidip)
L3240D1 (SO-8)

DESCRIPTION

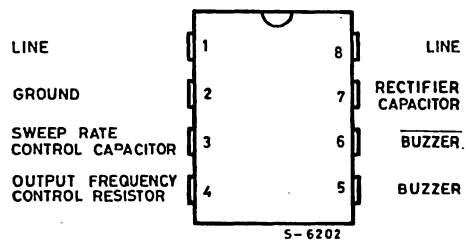
L3240 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The device can drive either directly a piezo ceramic converter (buzzer) or a small loudspeaker. In this case a transformer is needed. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across output amplifiers in the transducer ; both tone frequencies and the switching frequency can be externally adjusted.

The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect the correct operation of the devices.

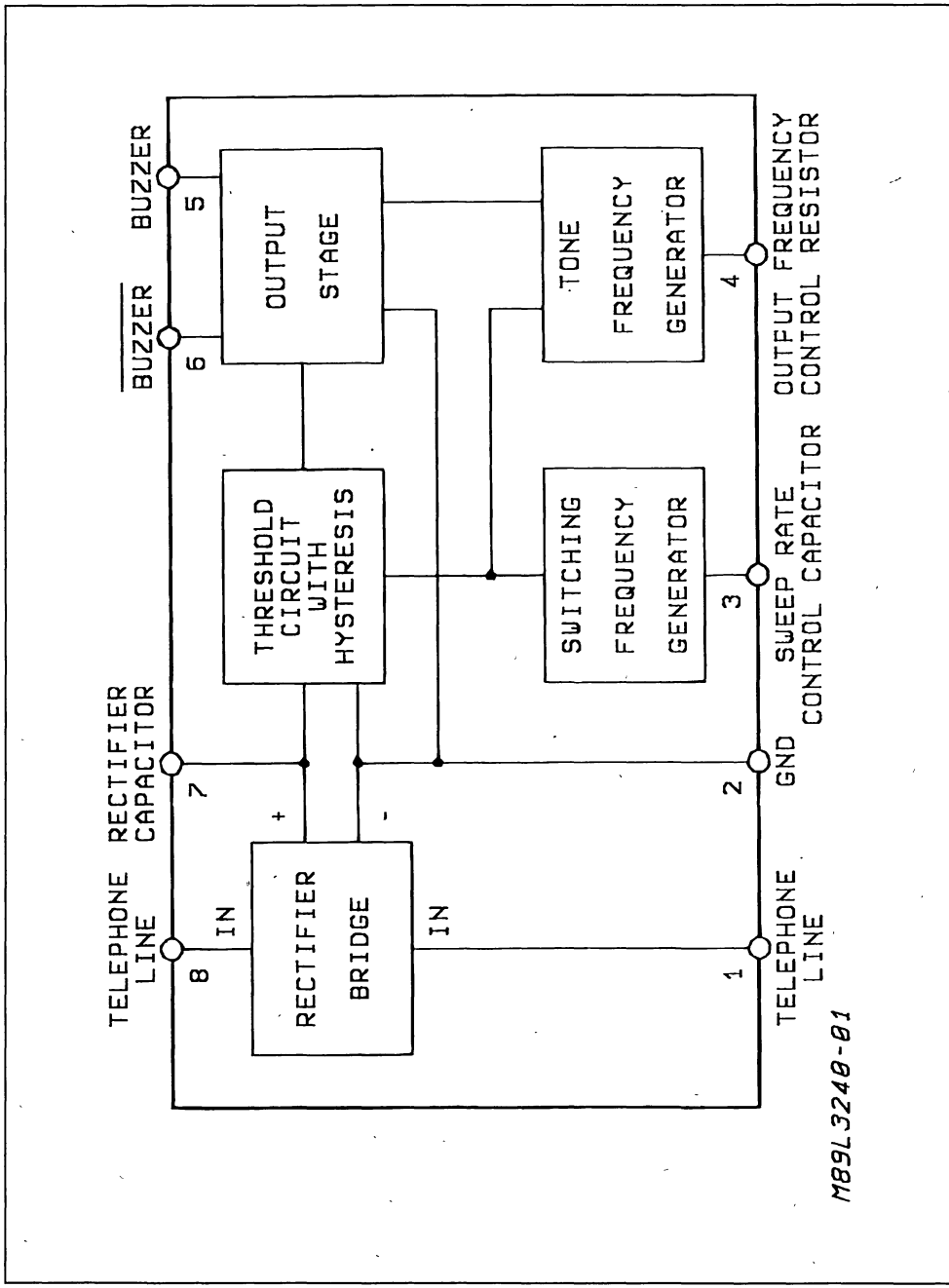
The output bridge configuration allows to use a high impedance transducer with acoustical results much better than in a single ended configuration.

The two outputs can also be connected independently to different converters or actuators (acoustical, opto, logic).

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{AB}	Calling Voltage (f = 50 Hz) Continuous	120	V_{rms}
V_{AB}	Calling Voltage (f = 50 Hz) 5s N/10s OFF	200	V_{rms}
DC	Supply Current	30	mA
T_{op}	Operating Temperature	– 20 to + 70	°C
T_{stg}	Storage and Junction Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

Figure 1 : Test Circuit.

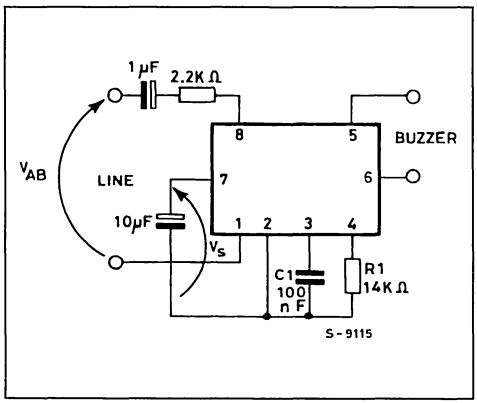


Figure 2 : Typical Application with Balanced Output.

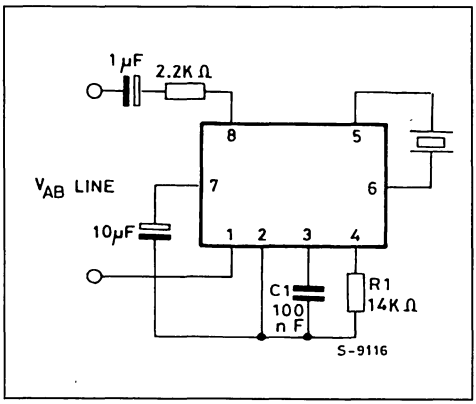


Figure 3 : Application Compatible with LS1240 (single ended output).

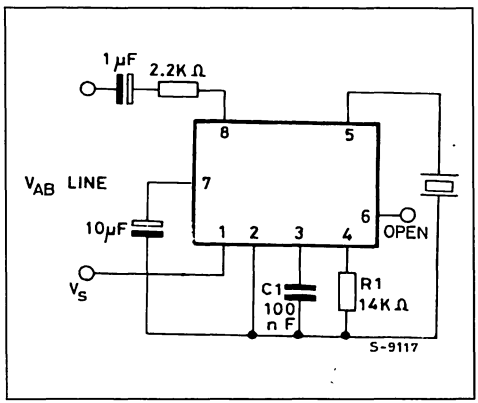
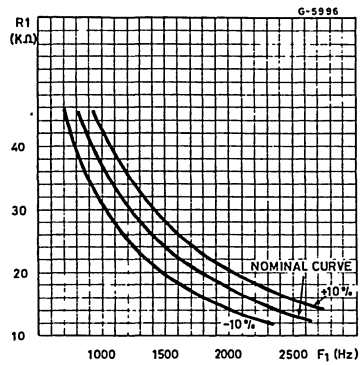


Figure 4 : F_1 Out vs. R_1.



$$R_1 \approx \frac{3.56 \times 10^4}{F_1\ (HZ)} \times \left(1 - 0.16 \times \ln \frac{F_1}{2543}\right) \qquad f_2 = 0.725\ f_1 \qquad f_{SWEEP} = \frac{750}{C1\ (nF)}$$

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C ; V_s = applied between pins 7-2 ; otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage				26	V
I_B	Current Consumption Without Load (pins 8-1)	V_s = 16.5 to 29.5 V		1.5	1.8	mA
V_{ON}	Activation Voltage		12		13.5	V
V_{OFF}	Sustaining Voltage		7.8		9.3	V
R_D	Differential Resistance in OFF Condition (pins 8-1)		6.4			KΩ
V_{OUT}	Output Voltage Swing			V_s – 5		V
I_{OUT}	Short Circuit Current (pins 5-6)	V_s = 20 V		35		mA
V_s	Voltage Drop Between Pins 8-1 and Pins 7-2			3		V

AC OPERATION

	Output Frequencies Fout 1 Fout 2	V_s = 26 V R_1 = 14 KΩ V_s = 0 V V_s = 6 V	 2,29 1.6		 2,8 2.1	KHz
	$\frac{\text{Fout 1}}{\text{Fout 2}}$		1.33		1.43	
	Programming Resistor Range		8		56	KΩ
	Sweep Frequency	R_1 = 14 KΩ C1 = 100 nF	5.25	7,5	9.75	Hz

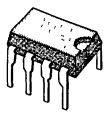
SGS-THOMSON MICROELECTRONICS

LS1240
LS1240A

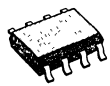
ELECTRONIC TWO - TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF 4 DEVICES
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVERVOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS

MINIDIP



SO-8J



ORDER CODES :

Minidip	SO-8
LS1240	LS1240D1
LS1240A	LS1240AD1

DESCRIPTION

LS1240 and LS1240A are monolithic integrated circuits designed to replace the mechanical bell in telephone sets in connection with an electro-acoustical converter. Both devices can drive directly a piezoceramic converter (buzzer).

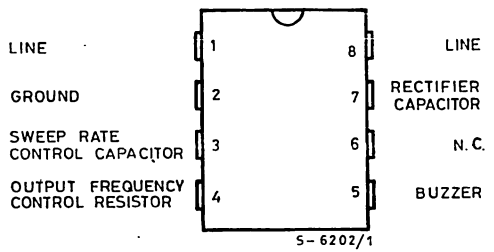
The output current capability of LS1240A is higher than LS1240. For driving a dynamic loudspeaker LS1240 needs a transformer, while LS1240A, needs a decoupling capacitor.

No current limitation is provided on the output stage of LS1240A, so a minimum load DC of 50 Ω is adviced.

The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker, both tone frequencies and the switching frequency can be externally adjusted.

The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect correct operation of the device.

PIN CONNECTION (top view)



BLOCK DIAGRAM

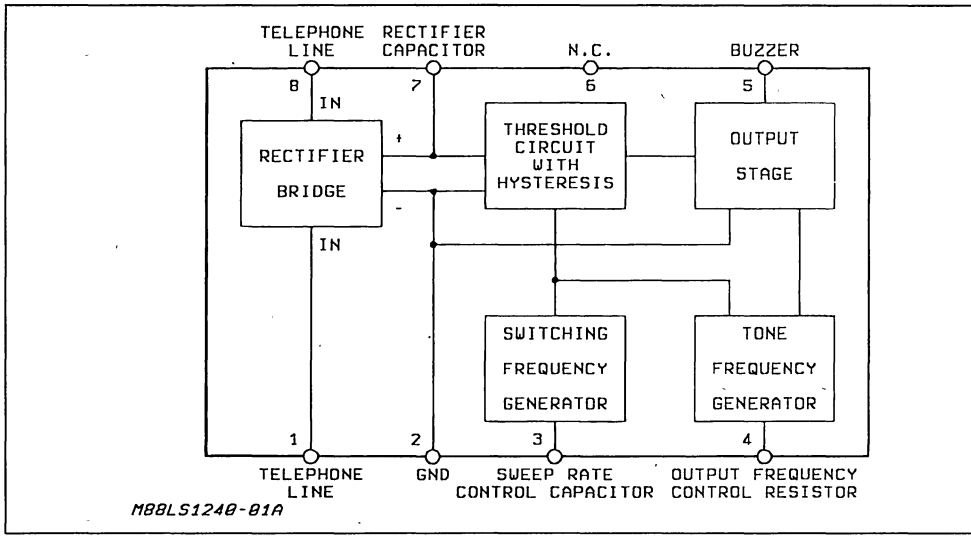
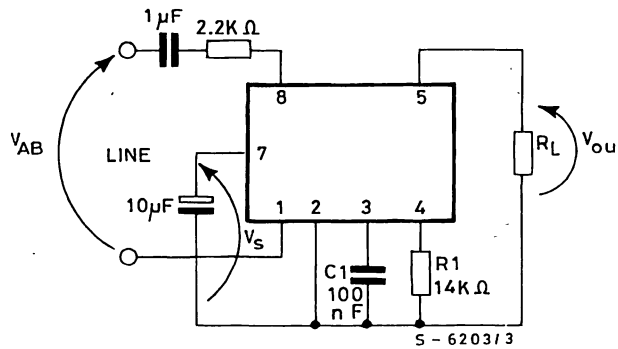


Figure 1 : Test Circuit.



$$f_1 = \frac{2.72 \cdot 10^4}{R\ (K\Omega)} \qquad f_2 = 0.725\ f_1 \qquad f_{SWEEP} = \frac{750}{C1\ (nF)}$$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{AB}	Calling Voltage (f = 50 Hz) Continuous	120	V_{rms}
V_{AB}	Calling Voltage (f = 50 Hz) 5s ON/10s OFF	200	V_{rms}
DC	Supply Current	30	mA
T_{op}	Operating Temperature	– 20 to + 70	°C
T_{stg}	Storage and Junction Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C; V_s = applied between pins 7-2 unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage				26	V
I_B	Current Consumption without Load (pins 8-1)	V_s = 9.3 to 25 V		1.5	1.8	mA
V_{ON}	Activation Voltage **LS1240**		12.2		13.2	V
	LS1240A		12		13.5	V
V_{OFF}	Sustaining Voltage **LS1240**		8		9	V
	LS1240A		7.8		9.3	V
R_D	Differential Resistance in OFF Condition (pins 8-1)		6.4			KΩ
V_{OUT}	Output Voltage Swing			V_s – 5		V
I_{OUT}	Short Circuit Current (pins 5-2) **LS1240**	V_s = 20 V R_L = 0 Ω		35		mA
	LS1240A	R_L = 250 Ω		70		mA

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Output Frequencies	V_s = 26 V R_1 = 14 KΩ				
f_1	f_{out1}	V_s = 0 V	1.74		2.14	KHz
f_2	f_{out2}	V_s = 6 V	1.22		1.6	
	$\frac{f_{out1}}{f_{out2}}$		1.33		1.43	
	Programming Resistor Range		8		56	KΩ
f_{SWEEP}	Sweep Frequency	R_1 = 14 KΩ C_1 = 100 nF	5.25	7.5	9.75	Hz

Figure 2 : Typical Application for LS1240.

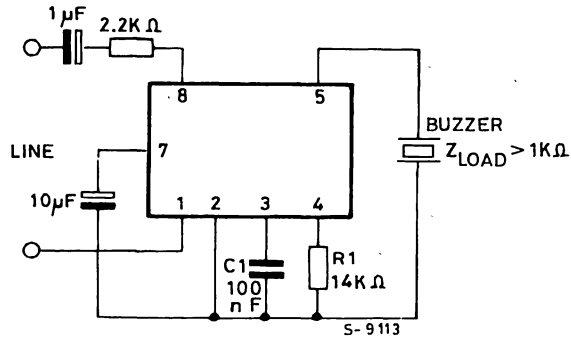
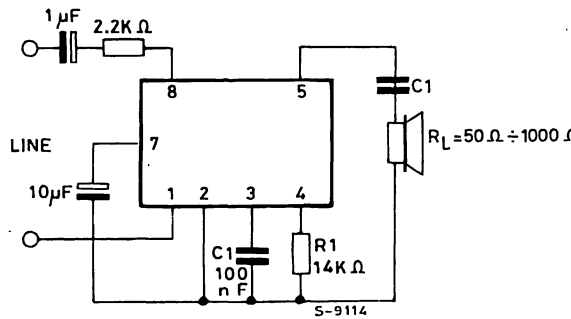


Figure 3 : Typical Application for LS1240A.



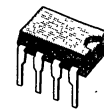
C_1 such that $|Z_{LOAD}| > 1\ K\Omega$

ELECTRONIC TWO - TONE RINGER

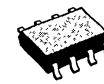
- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF A DEVICE
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVER VOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS

The supply voltage is obtained from the AC ring signal and the circuit is designed to that noise on the line or variations of the ringing signal cannot affect correct operation of the device.

MINIDIP



SO-8J

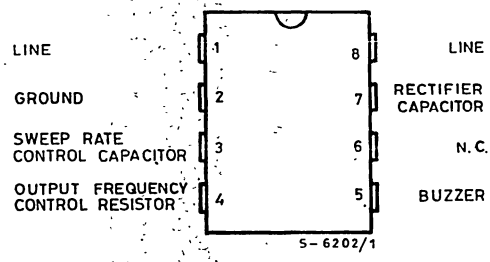


ORDER CODE : LS1241 (Minidip)
LS1241D1 (SO-8J)

DESCRIPTION

LS1241 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The device can drive either directly a piezo ceramic converter (buzzer) or a small loudspeaker. In this case a transformer is needed. The two tone frequencies generated are switched by an output amplifier in the loudspeaker ; both tone frequencies and the switching frequency can be externally adjusted.

PIN CONNECTION (top view)



BLOCK DIAGRAM

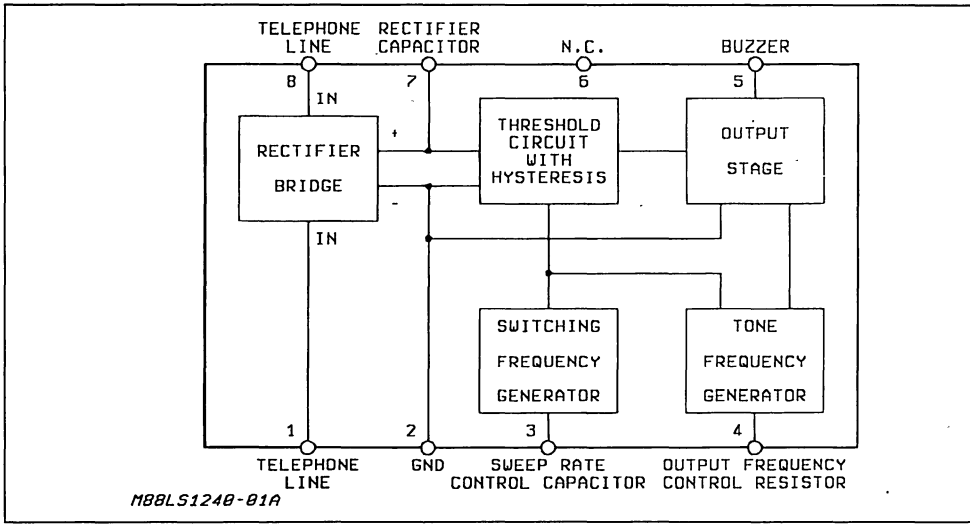
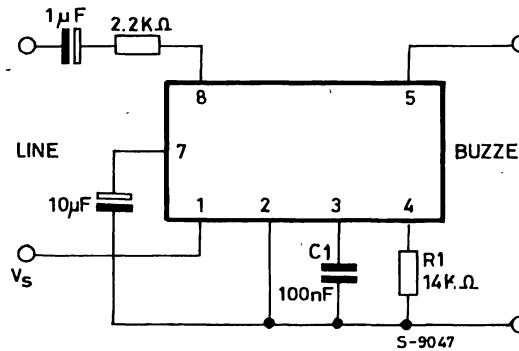


Figure 1 : Test Circuit.



$$f_1 = \frac{1.90 \cdot 10^4}{R\ (K\Omega)} \qquad f_2 = \frac{4}{5} f_1 \pm 4\,\% \qquad f_{SWEEP} = \frac{750}{C1\ (nF)}$$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{AB}*	Calling Voltage (f = 50 Hz) Continuous	120	V_{rms}
V_{AB}*	Calling Voltage (f = 50 Hz) 1.8s ON/3.6s OFF	200	V_{rms}
DC	Supply Current	30	mA
T_{op}	Operating Temperature	– 20 to + 70	°C
T_{stg}	Storage and Junction Temperature	– 65 to + 150	°C

* See test circuit of figure 1.

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C; V_s = applied between pins 7-2 unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage				26	V
I_B	Current Consumption without Load (pins 8-1)	V_s = 9 to 25 V		1.5	1.8	mA
V_{ON}	Activation Voltage		12.2		13.2	V
V_{OFF}	Sustaining Voltage		8		9	V
R_D	Differential Resistance in OFF Condition (pins 8-1)		6.4			KΩ
V_{OUT}	Output Voltage Swing			V_s – 5		V
I_{OUT}	Short Circuit Current (pins 5-2)	V_s = 20 V		35		mA

AC OPERATION

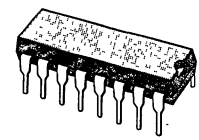
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_1 f_2	Output Frequencies f_{out1} f_{out2}	V_s = 26 V R_1 = 14 KΩ V_3 = 0 V V_3 = 6 V	1.21 0.93		1.5 1.25	KHz
	$\frac{f_{out1}}{f_{out2}}$		1.2		1.3	
	Programming Resistor Range		5		50	KΩ
F_{SWEEP}	Sweep Frequency	R_1 = 14 KΩ C_1 = 100 nF	5.25	7.5	9.75	Hz

SGS-THOMSON MICROELECTRONICS

M764A

THREE TONE RINGER

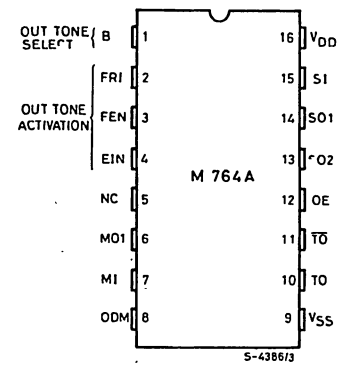
- WIDE OUTPUT TONE SELECTION
- DIRECT DRIVE FOR PIEZOCERAMIC OR DYNAMIC TRANSDUCERS
- BUILT IN BAND PASS FILTER (20 TO 60 Hz)
- µP CONTROL INPUT
- CMOS TECHNOLOGY



DIP16
(Plastic Package 0.25)

ORDER CODE : M764A B1

PIN CONNECTION



DESCRIPTION

The M764A is a high performance electronic ringer suitable for application in standard and parallel connection telephones ; it can also be used as an alarm indicator. An incorporated bandpass filter prevents spurious ringing caused by transients and dialling pulses. Pin-selectable options permit three, two and single tone sequences.

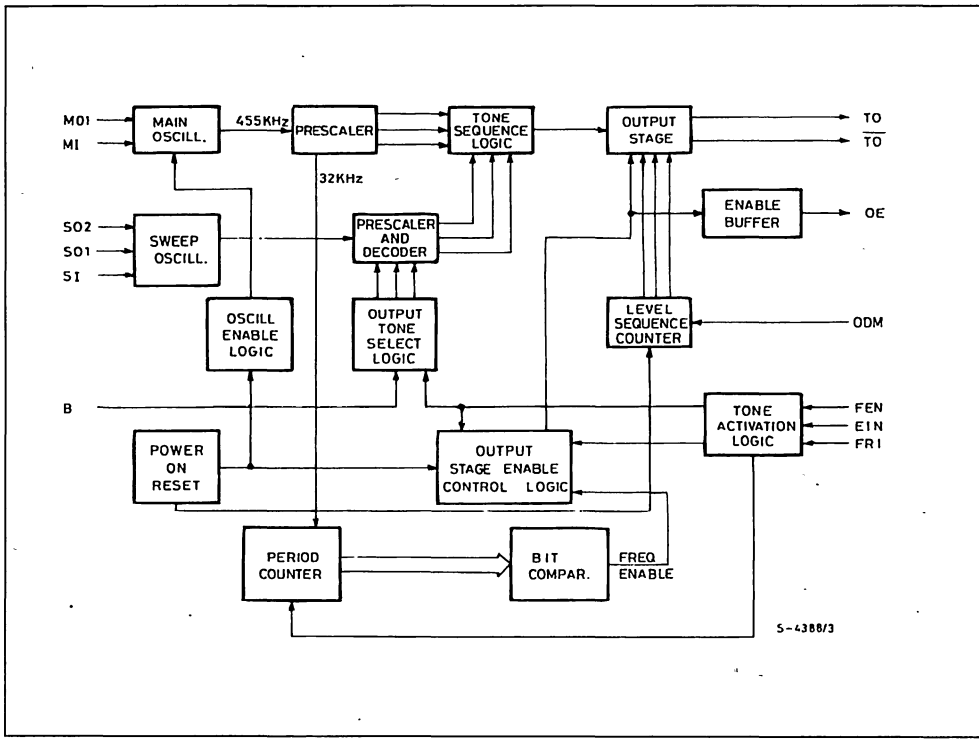
The output stage allows direct drive of both piezoceramic and dynamic transducers. The output tone level can be externally programmed to increase gradually during the first three bursts. Output tone stability and the bandpass filter corner frequencies are guaranteed by a crystal controlled oscillator.

The M764A is available in 16 pin dual in-line plastic.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.5 V to + 17	V
V_I	Input Voltage	– 0.3 to V_{DD} + 0.5	V
P_{tot}	Power Dissipation	400	mW
T_{op}	Operating Temperature Range	– 25 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 125	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (all parameters are tested at T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
Supply						
V_{DD}	Voltage Supply		6		17	V
V_{TH}	Power on/off Reset Threshold		4.5		5.5	V
V_{TH}	Sequence Logic Power on/off Reset		1.8		2.8	V
I_{DD}	Operating Supply Current	V_{DD} = 15 V OE = 1			0.75	mA
I_{DDO}	Stand-by Supply Current	V_{DD} = 15 V			0.15	mA
Main Oscillator						
MI	Main Oscillator Input	I_{IH} V_{IH} = 15 V; V_{DD} = 15 V			+ 5	µA
		I_{IL} V_{IL} = 0 V; V_{DD} = 15 V			− 1	µA
MO1	Main Oscillator Output 1	I_{OH} V_{OH} = 13 V; V_{DD} = 15 V	− 250			µA
		I_{OL} V_{OL} = 1 V; V_{DD} = 15 V	+ 250			µA
Sweep Oscillator						
SI	Sweep Oscillator Input	I_{IH} V_{IH} = 15 V; VDD = 15 V			+ 1	µA
		I_{IL} V_{IL} = 0 V; VDD = 15 V			− 1	µA
SO1	Sweep Oscillator Output 1	I_{OH} V_{OH} = V_{DD} − 1 V; V_{DD} = 15 V	− 90			µA
		I_{OL} V_{OL} = V_{DD} 13 V; V_{DD} = 15 V	+ 90			µA
SO2	Sweep Oscillator Output 2	I_{OH} V_{OH} = V_{DD} − 1 V; V_{DD} = 15 V	− 90			µA
		I_{OL} V_{OL} = V_{DD} 13 V; V_{DD} = 15 V	+ 90			µA
Control Pins						
EIN FEN ODM	Enable Input Filter Enable Input Output Drive Mode	I_{IH} V_{IH} = 15 V		0.1	+ 1	µA
		I_{IL} V_{IL} = 0 V		− 0.1	− 1	µA
A B C*	Output Sequence Selection Pins	I_{IH} V_{IH} = 15 V		0.1	5	µA
		I_{IL} V_{IL} = 2 V		1		mA
Frequency Input						
FRI	Frequency Input	I_{IL} V_{IL} = 0 V			1	µA
		I_{IH} V_{IH} = 4 V	4	20	40	µA
		V_{TH}	2		4	V
Output Enable						
OE		I_{OH} V_{DD} = 15 V V_O = 13 V	10			mA
		I_{OL} V_{DD} = 15 V V_O = 1 V	1			mA

* Input resistor of 1.5 KΩ is active until V_{TR} of input inverter is reached.

ELECTRICAL CHARACTERISTIC (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Tone Outputs							
TO	Output	I_{OH} V_{DD} = 15 V V_O = 13 V		10			mA
		I_{OL} V_{DD} = 15 V V_O = 1 V		10			
$\overline{TO}$	Inverted Output	I_{OH} V_{DD} = 15 V V_O = 13 V		10			mA
		I_{OL} V_{DD} = 15 V V_O = 1 V		10			

* Input resistor of 1.5 KΩ is active until V_{TR} of input inverter is reached.

AC CHARACTERISTICS

Main Oscillator							
t_{SM}	Start up Time	V_{DD} = 6 V fo = 455 KHz R_F = 1 MΩ $C_I = C_O$ = 100 pF			10		ms
			See Tables 1-2				
Sweep Oscillator							
t_{SS}	Start up Time	V_{DD} = 6 V f = 1140 to 11400 Hz (*)			5		ms

(*) R > 50 kΩ
C > 100 pF

FUNCTIONAL DESCRIPTION

MAIN OSCILLATOR

The main oscillator has been designed to be driven either by an external RC network or by a ceramic resonator (see fig. 1) :

The accuracy of the output tones and of the band-pass filter characteristics are determined by the accuracy of the main oscillator frequency.

The crystal guarantees good performance over the whole temperature range with no external trimmer. The main oscillator as well as the sweep oscillator are maintained in a stand-by condition or forced to run according to table 1.

SWEEP OSCILLATOR

The sweep oscillator (fig. 2) controls the repetition rate of the output tone sequence. The output repetition period is given by

$$T_{rep} = \frac{384}{F_{sweep\ oscill.}}$$

OUTPUT TONE ACTIVATION (pins FEN, EIN, FRI)

The output stage is enabled by the signal OE (output enable) under control of pins FEN, EIN, FRI as shown in table 1, and fig. 3.

Pin FEN and EIN are standard C-MOS inputs.

Pin FRI has a pull-down resistor of approximately 300 KΩ.

OUTPUT ENABLE (OE)

The output enable pin (OE) can be used in special application to drive a LED or any external circuit to indicate that an incoming ringing signal has been detected by the tone ringer as in automatic responders.

OE timing diagrams are shown in table 1.

The OE output stage configuration is shown in fig.4.

Figure 1 : a) Crystal Controlled Oscillator.

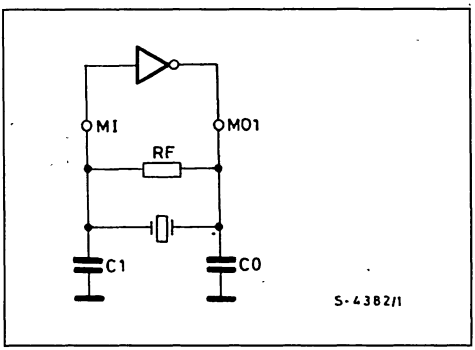


Figure 2.

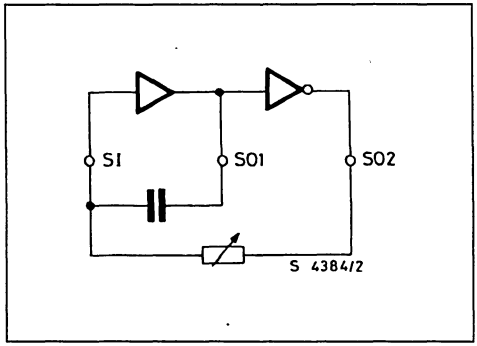


Figure 3 : Timing Diagram.

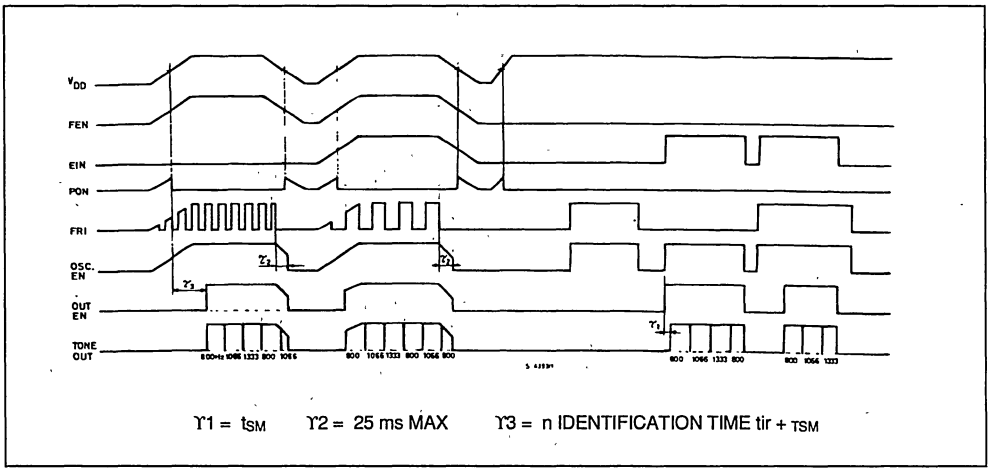


Figure 4.

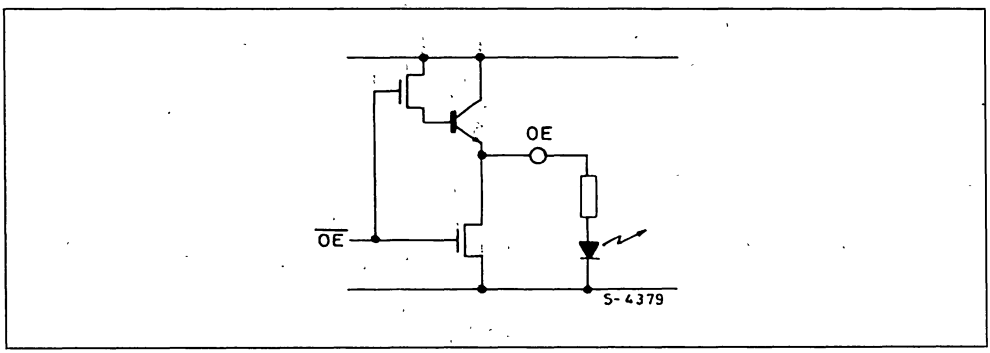
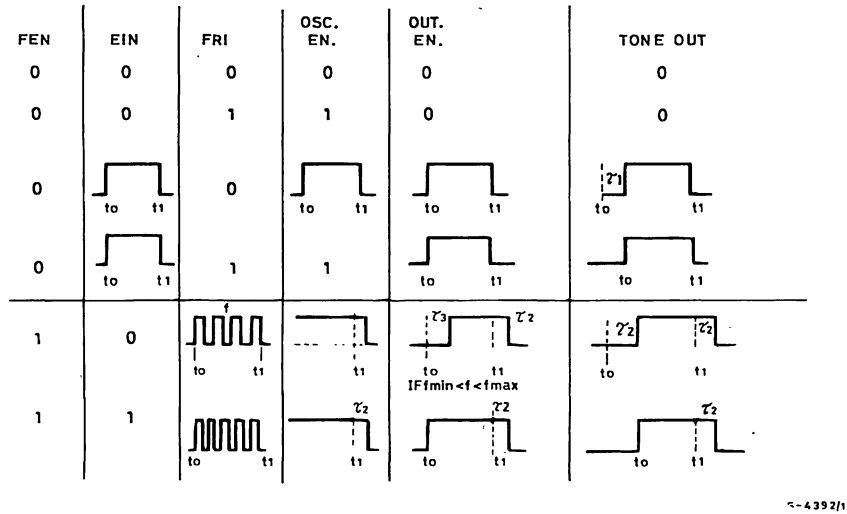


Table 1.



$\Upsilon 1 = t_{SM}$ $\Upsilon 2 = 25$ ms MAX $\Upsilon 3 =$ n IDENTIFICATION TIME tir + T_{SM}

TONE OUTPUTS (TO, TO)

Two complementary outputs are provided to drive in a bridge configuration both piezoceramic and dynamic transducers (see fig. 5).

The configuration of the output buffer is shown in fig. 6.

The output waveform is a square wave with 50 % duty cycle.

The generated tone level can be constant or can be gradually increased up to the max. level during the detection of the first three ring signals.

This function has been implemented controlling the output voltage swing that can be V_{DD} for max. output level, 0.4 V_{DD} for the intermediate output level and 0.1 V_{DD} for the lowest output level.

OUTPUT DRIVE MODE (ODM)

The output level is constant if this pin is a logical 0 : it gradually increases to the max. level if this pin is a logical 1 : the sequence can take place if after the first ring signal during the ring tone pause period the supply does not fail below the power on reset threshold (5.5 V) and always starts from the lowest level.

OUTPUT TONE SELECTION (B)

Table 2.

B	Output Tone Sequences and Frequencies $f_{max\ oscill.}$ = 455 KHz		
0	800	1066	1333
1	800	1066	

Figure 5.

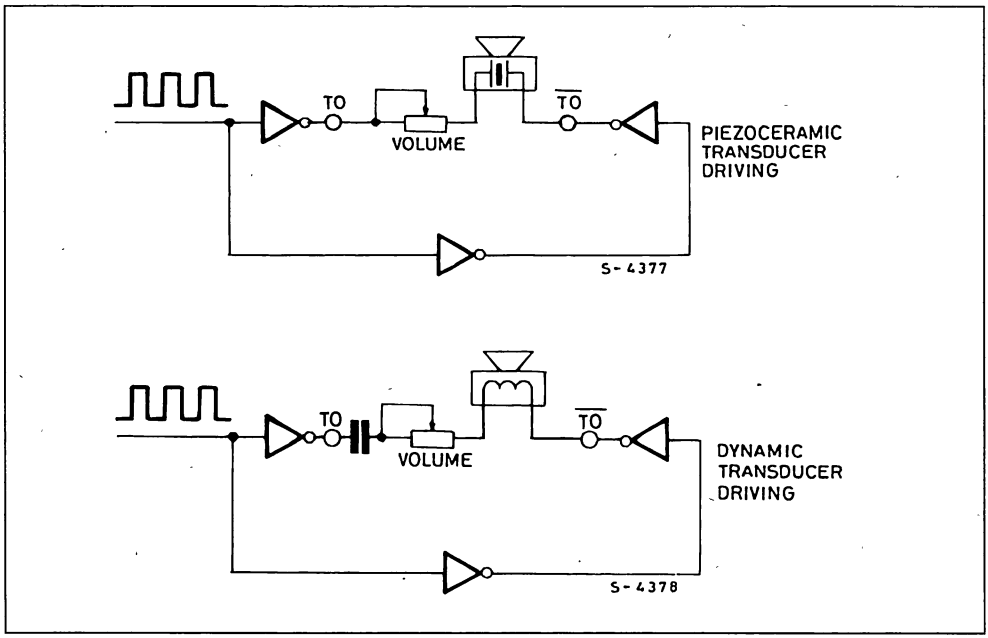
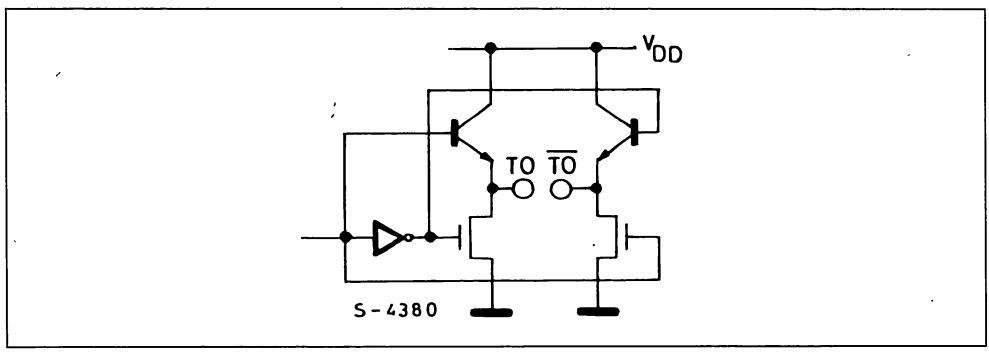
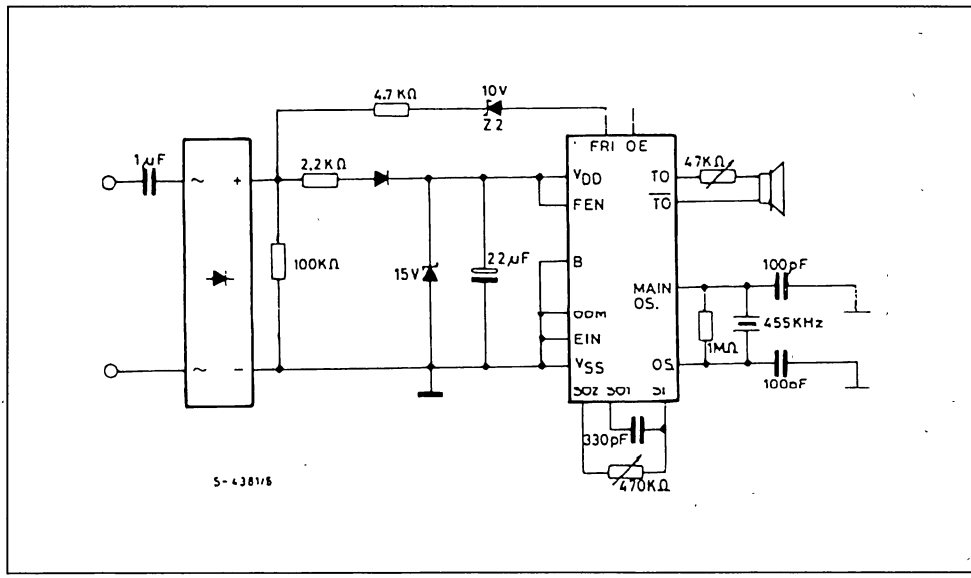


Figure 6.



TYPICAL APPLICATIONS

Figure a : Tone Ringer for Standard telephone Applications.

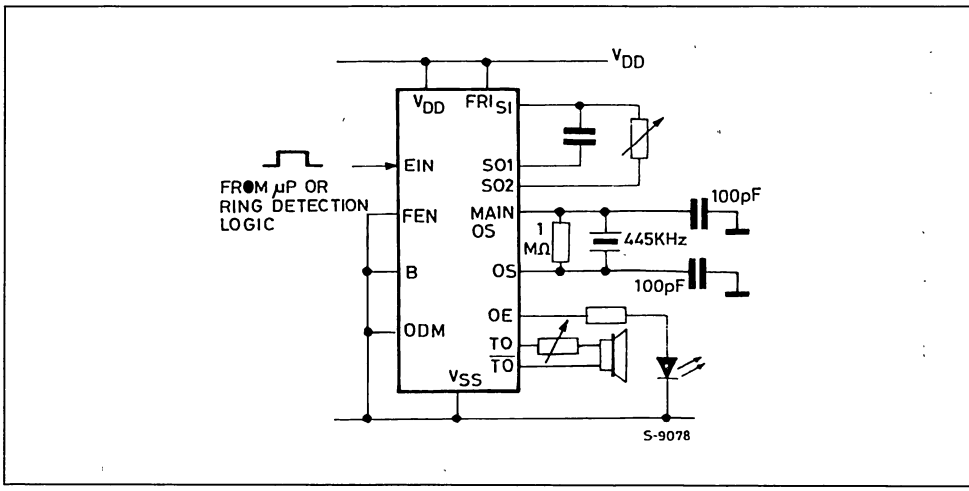


If pin EIN is connected to V_{DD} the ringer is activated by frequencies upper than 20 Hz.

- In both cases the volume potentiometer can be avoided connecting the ODM to V_{DD} allowing the gradually increase of the ringer volume in three steps.

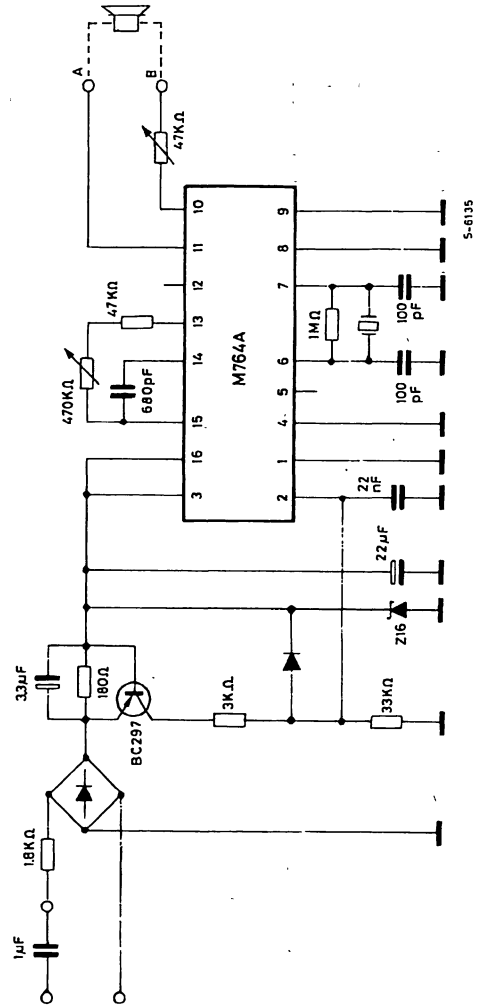
- The number of the output available tones and their frequencies are controlled by ABC pins according to table 2.

Figure b : Tone Ringer for Alarm,Buzzer or Ring Tone Detection in Centralized Equipments.



ANTI TAPPING APPLICATION

In the anti-tapping application an input current threshold is established.



SGS-THOMSON MICROELECTRONICS

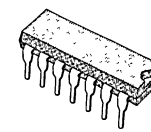
SAA1094

THREE-TONE RINGER

ADVANCE DATA

- ON-CHIP RECTIFIER BRIDGE AND TRANSIENT PROTECTION
- DIRECT DRIVE OF PIEZOCERAMIC OR DYNAMIC TRANSDUCERS
- NOISE SUPPRESSION BY DIGITAL FREQUENCY FILTER AND LEVEL DETECTOR
- USES LOW COST CERAMIC RESONATOR FOR MAIN OSCILLATOR
- REPETITION RATE OF TONE SEQUENCE ADJUSTABLE BY RC TIME CONSTANT

DIP14



ORDER CODE : SAA1094-2

DESCRIPTION

The SAA1094 replaces the electromechanical telephone bell and calls the subscriber by a melodic tone sequence. It derives its power supply by rectifying the ac ringing signal, requires only a minimum of additional components and is compatible with the conventional telephone network.

PIN CONNECTION

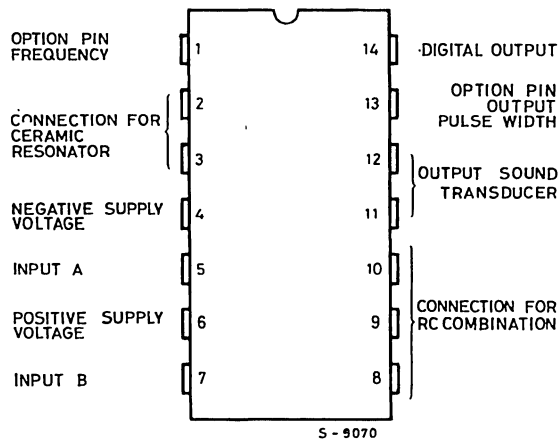
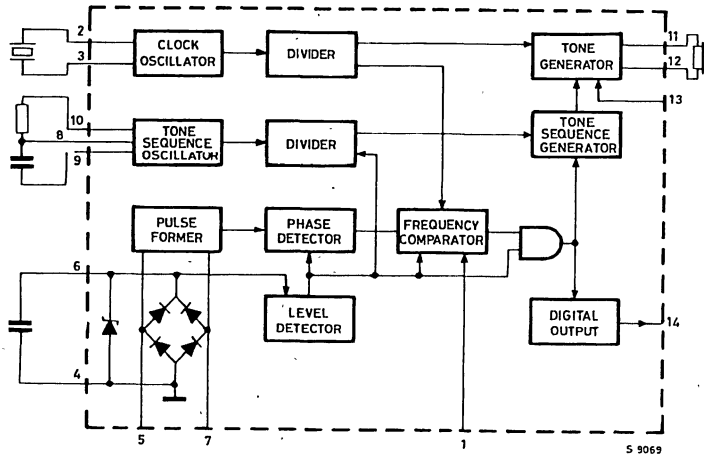


Figure 1 : Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Supply Current	I5, I7 = ± 25	V
V_I	Input Voltage	V_I V_{SS} − 0.3 to V_{DD} + 0.3	V
	Output Current	I11, I12, I14 = ± 10	mA
T_{op}	Operating Ambient Temperature	− 25 to + 60	°C
T_{stg}	Storage Temperature Furthermore, the Conditions of Section 9 are Applicable	− 40 to + 125	°C

Stresses in excess of thos listed unter "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_C	Clock Oscillator Frequency		455		kHz
	Power Supply (see functional description)				

ELECTRICAL CHARACTERISTICS (at V6-4 = 10 V ; f_C = 455 KHz ; T_{amb} = 25 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I5, I7	Current Consumption, Outputs whithout Load		1.4	2.2	mA
f_{IN}	Frequency range of the ac input current into pins 5 and 7 which gives an output signal at pins 11 and 12 ; (test circuit - fig. 7).				
	a) Pin 1 unconnected	23		54	Hz
	b) Pin 1 connected to Pin 4 = V_{SS}	12		54	Hz
	c) Pin 1 connected to Pin 6 = V_{AD} dc Operation (see section 3)				
f_{IN}	Frequency ranges of the ac input current into pins 5 and 7 which do no produce output signals at pins 11 and 12 ; (test circuit - fig. 8)				
	a) Pin 1 is unconnected	0		18	Hz
		60		∞	Hz
R_{ON}	On-resistance of Outputs :				
	Pin 11, Pin 12, at I_{OL} = 5 mA or I_{OH} = – 5 mA			90	Ω
	Pin 14, at I_{OL} = 5 mA			500	Ω
	Pin 14, at I_{OH} = – 5 mA			300	Ω
f_{01}	Frequency of the Output Signal at Pin 11, Pin 12		813		
f_{02}			1083		
f_{03}			1354		
	Start-up Time of Clock Oscillator			10	ms
V6-4	Internal Supply Voltage Limitation at I5, I7 = 10 mA	15		22	V
	Switching Levels of Voltage Level Detector :				
V6-4 ON	Turn-on Level	6		7.5	V
V6-4 OFF	Turn-off Level	3		4.5	V

GENERAL DESCRIPTION

The SAA1094 replaces the customary electromechanical telephone bell and calls the subscriber by a melodic tone sequence, using a small magnetic or piezo-ceramic sound transducer. The melody ringer circuit, together with its transducer is powered by the ringing current from the enge. This makes it compatible with the conventional telephone network and, in addition, no battery or mains connections are needed (fig. 2). It is also possible to apply a DC signal instead of the AC ringing signal (fig. 3). As shown in fig. 2 and 3 the amount of additional components is reduced to a minimum.

FUNCTIONAL DESCRIPTION OF THE TONE RINGER CIRCUIT

POWER SUPPLY

The tone ringer circuit (fig. 2) derives the power required for its operation from the ringing AC supplied by the exchange via linea a and b. Together with the loop resistance, the specified 1 µF isolating capacitor and a 2.2 kΩ resistor is needed to ensure a minimum impedance.

The supplied alternating current is fed to pins 5 and 7 of the tone ringer and is rectified by means of an integrated bridge circuit in the SAA1094. The rectified current charges the electrolytic capacitor at pin 4 and 6. The direct voltage V 6-4 generated across this capacitor is the supply for the internal circuit. It mainly depends on the loop resistance and on the ringing frequency. Its maximum value is limited by an internal Zener diode to about 20 V.

CLOCK SIGNAL GENERATION

The clock oscillator, integrated in the SAA1094 tone ringer Ic requires only an inexpensive ceramic resonator connected to pins 2 and 3, for example the 455 KHz type Murata CSB 455E. The frequency of this oscillator is used to derive the three input tone frequencies and the clocks for the output frequency comparator.

MONITORING THE INPUT RINGING FREQUENCY

The frequency f_{IN} of the ringing AC supplied to the inputs pins 5 and 7 is monitored in the SAA1094 by a frequency comparator. The result of the frequency comparison is used as one criterion for activiting the tone generator (see section 4 for the other crite-

rion). The circuit generates output tones only if the input ringing signal is inside a specified frequency band. Three different modes can be selected by the option pin 1.

a) Pin 1 unconnected :

In this mode a frequency f_{IN} from 23 to 54 Hz will be accepted for producing the output tone sequence.

b) Pin 1 connected to pin 4 = 0

In this mode a frequency f_{IN} from 12 to 54 Hz will be accepted. Due to this option, the SAA1094 can also be employed in telephone systems having a ringing frequency below 20 Hz.

c) Pin 1 connected to pin 6 = 1

In this mode the result of the frequency comparison has no influence. A DC signal can be applied to the SAA1094 at pins 4 and 6 or pin 5 and 7 for producing the output tone sequence.

A digital noise suppression circuit in the SAA1094 ensures that noise signals in the range from 0 Hz to 20 KHz and with a maximum amplitude of 9 V RMS will not affect the correct function of the SAA1094 if the input ringing signal applied to the terminal a and b fig. 2 has an amplitude of 50 V RMS and a frequency in the range specified for producing an output signal.

VOLTAGE LEVEL DETECTOR

The voltage level V 6-4 is monitored in the SAA1094 and used as another criterion for activiting the tone generator. The tone sequence will be started when V 6-4 increases to a level around 6 V. The tone sequence will be ended when V 6-4 decays to a level around 3 V.

TONE SEQUENCER

The ringing signal produced by the SAA1094 is a sequence which is determined by the external RC network of the tone sequence oscillator and by the ratio of the frequency divider. the relationship between repetition rate f_R and oscillator frequency f_{OS} is :

$$f_R = \frac{f_{OS}}{3 \cdot 32}$$

The repetition frequency can be adjusted from 2.4 Hz ± 0.2 Hz to 25 Hz ± 3.5 Hz using the connection scheme of Fig. 4 and the following component values :

C = 4.7 nF
R3 = 43 kW
R4 = 0 to 600 kW

The repetition frequency can be calculated using the formula :

$$f_R\,(\text{Hz}) = \frac{10^6}{134.4 \cdot C \cdot (20 + R)}$$

with C (nF) = capacitance between pins 8 and 9, R (KΩ) = resitance between pins 8 and 10.

The repetion frequency depends slightly on the supply voltage V 6-4. The variation is equal of less than + 4 % per 1 V.

TONE GENERATOR

The ringing signal is a sequence of three tones. their frequencies are derived from the clock frequency at division rates of 560, 420 and 336. Depending of the clock frequency f_C the tone frequencies are

813 Hz, 1083 Hz, 1354 Hz for f_C = 455 kHz or

800 Hz, 1067 Hz, 1333 Hz for f_C = 448 kHz

This is a harmonic ratio of 3 : 4 : 5. the sequence will be started if two conditions are fulfilled : the input ringing signl f_{IN} has to be inside a specified frequency band and the supply voltage V 6-4 has to be increased to the turn-on level. The sequence always starts with the lowest tone. The sequence ends, if f_{IN} departs from the specified frequency band or if V 6-4 is lowered to the turn-off level.

TONE OUTPUT

The output amplifier of the SAA1094 tone ringer is a push pull bridge circuit. It supplies two square wave signals of opposite phase at pin 11 and pin 12. The high value of the signal equals the potential of pin 6 and the low value equals the potential of pin 4, if no load is connected to the outputs. Optionally, the pulsewidth of the squarewave output signal can be limited to 0.2 ms internally, in order to save the components of an external limiting circuit containing a capacitor. The shorter pulse-width is of advantage in the case of an electromagnetic transducer being used which will operate with increased efficiency in this case. The connection of pin 13 determines the mode : when connected to pin 4, the pulsewidth is not affected. If pin 13 is left unconnected, the pulsewidth will be 0.2 ms. The waveform of the current through the load is shown for both cases in Fig. 5.

DIGITAL OUTPUT

The digital output pin 14 can be used for connecting a supplementary load to the supply terminals pins 4 and 6 when the tone generation is deactivated. Without the supplementary load the voltage V 6-4 may decrease significantly upon activation of the tone generation.

The digital output is at the voltage level of pin 6 as long as the two conditions (f_{IN} and V 6-4) for the tone generation are not fulfilled. A supplementary load current can then be drawn through an external resistor between pins 14 and 4. As soon as the conditions for the tone generation are fultilled, the digital output switches to the voltage level of pin 4.

OVERLOAD PROTECTION

The SAA1094 can withstand an alternating voltage of 110 V at a frequency of 50 Hz across terminals a and b fig. 2 for 15 seconds.

The circuit will not be damaged by a transient voltage test with the following test conditions :

Voltage across the charge capacitor	2 kV
Pulse tinming	10/700 µs
Pulse sequence	30 s
Number of transients	16
Polarity change after	5 transients
Test circuit	Fig. 6

Figure 2 : SAA1094 with Power Supplied by the AC Ringing Signal..

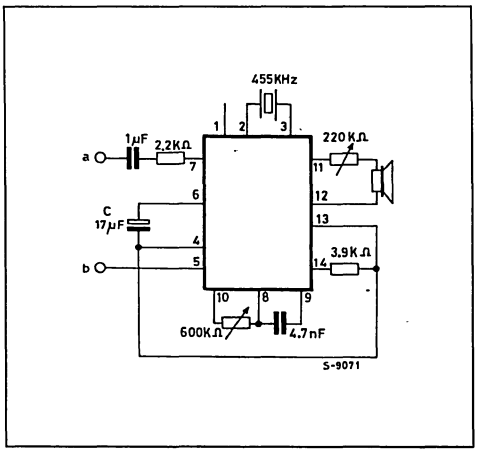


Figure 3 : SAA1094 with Power Supplied by DC.

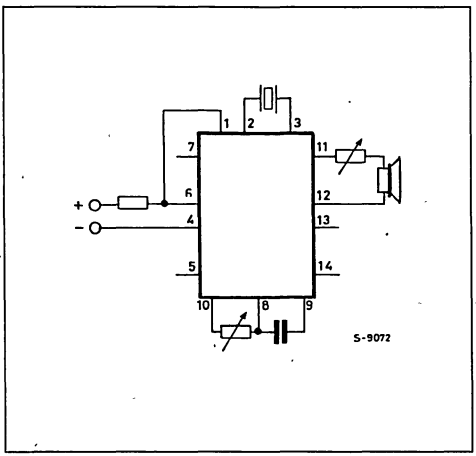


Figure 4 : Circuit Connection Scheme for Repetition Frequency Adjustement Described in Section 5.

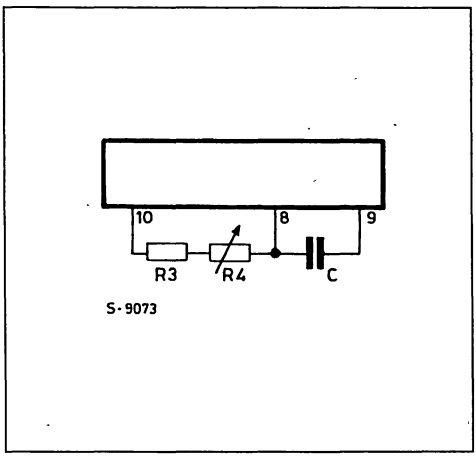


Figure 5a/5b : Diagram of Output Current through a Load between Pins 11 and 12.

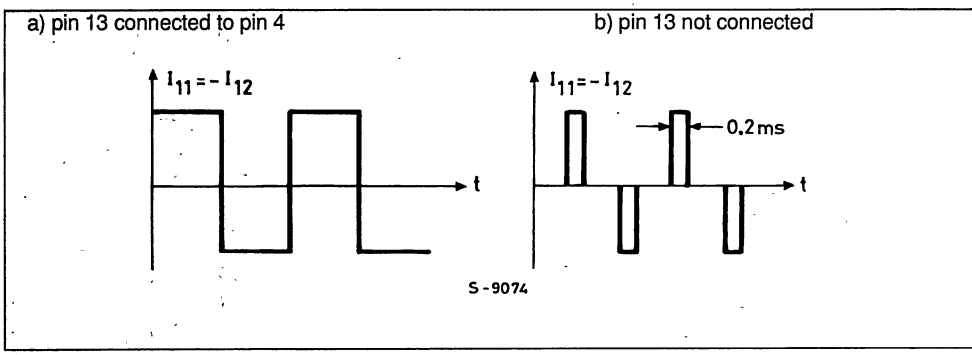


Figure 6 : Circuit for Transient Voltage Test Described in Section 9.

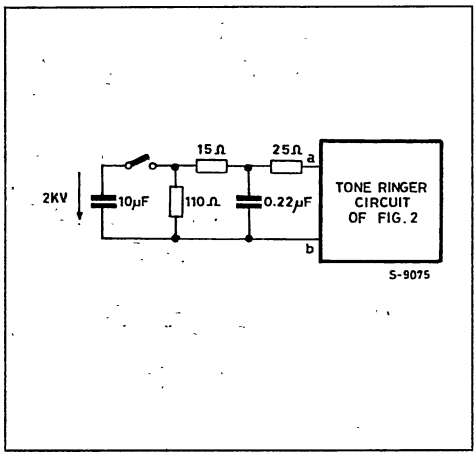


Figure 7 : Test Circuit which Activates the Output Signal Generator (see also frequency specification).

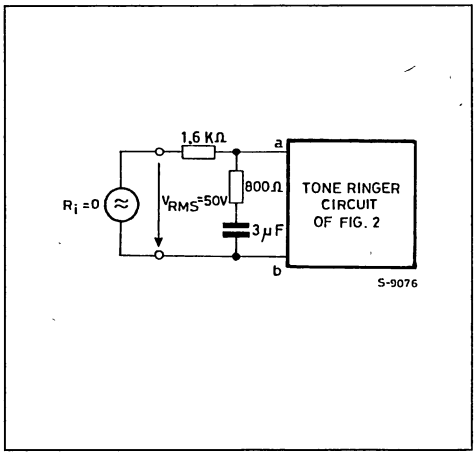
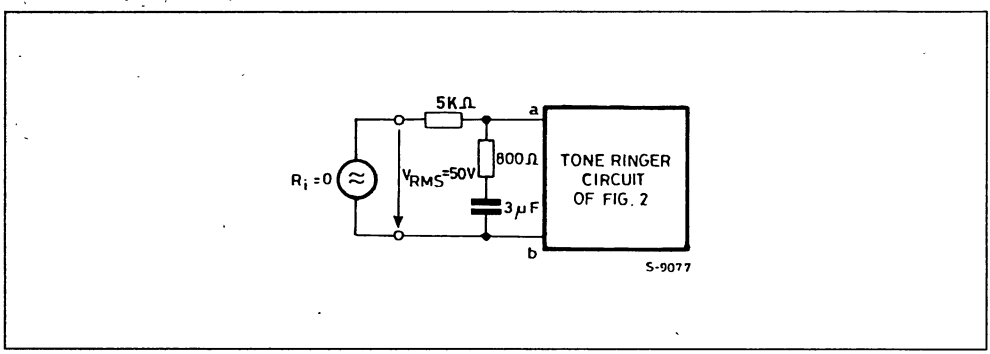


Figure 8 : Test Circuit which does not Activate the Output Signal Generator (see also frequency specification).



SGS-THOMSON MICROELECTRONICS

LB1006

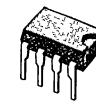
TELEPHONE RINGING DETECTOR

AN AT & T PRODUCT

PRELIMINARY DATA

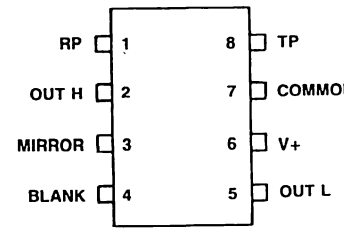
- MEETS BOTH TYPE A AND B RINGING REQUIREMENTS (40 $V_{RMS} \leq VIN \leq 150\ V_{RMS}$, 15 Hz $\leq F_{IN} \leq$ 68 Hz
- OPERATES ON LESS THAN 1 mA FROM THE TELEPHONE LOOP
- INTERNAL POLARITY GUARD PROVIDES 1500 V LIGHTNING SURGE PROTECTION WHEN CONNECTED AS IN FIG. 11 AND 12
- IMMUNE TO ROTARY DIAL PULSING (BELL TAP)

MINIDIP A



ORDER CODE : LB 1006AB

PIN CONNECTION

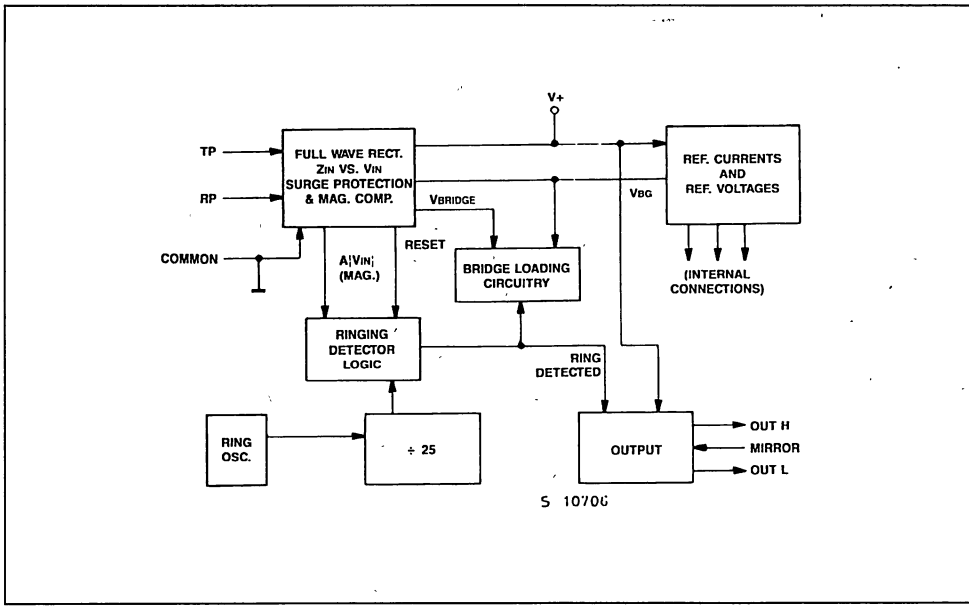


S-10707

DESCRIPTION

The LB1006 provides ringing detection functions from the Tip-ring pair of a telephone loop. This device provides approximately 1 mA output current for two types of output drivers. The output can be connected to either an opto-isolator device or to a logic interface with a microprocessor.

Figure 1 : Functional Diagram.



PIN DESCRIPTION

N°	Symbol	Description
8	TIP	AC Input Signal from Telephone Line
1	RING	AC Input Signal from Telephone Line
2	OUTH	Sources Current when ringing is detected
3	MIRROR	Mirror Current from OUTH to Activate Pin OUTL
5	OUTL	Sinks Current when ringing is detected
6	V^+	Internal Supply Voltage. This voltage is usually derived from the AC signal which is present on the Tip-ring pair. This pin must have a 10 µF capacitor to common for energy storage and «smoothing» purposes. For «stand alone application», an external voltage may be used to bias this pin.
7	GND	Ground
4	NC	No Connection

ABSOLUTE MAXIMUN RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage (ref to GND)	30	V
OUTH	Supply Voltage (ref to GND)	30	V
OUTL	Supply Voltage (ref to GND)	30	V
TIP	Voltage (tip-ring)	± 30	V
I_O	Operating Current (tip-ring)	± 100	mA
I_{MIR}	Mirror Current	2.0	mA
T_A	Ambient Operating Temperature Range	– 20 to + 75	°C
T_{stg}	Storage Temperature Range	– 40 to + 125	°c
–	Pin Temperature (soldering 15 sec)	300	°C
P_D	Power Dissipation (package limitation)	600	mW

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS(at 25 °C unless otherwise specified)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Power Supply Current	$V^+ = 28$ V	(see fig. 2)	200	365	900	µA
Power Supply Current	$V^+ = 15$ V	(see fig. 2)	200	360	800	
Tip-ring Current	$V_{TIP-RING} = 4.5$ V	(see fig. 3)	–	30.4	65	
OUTH Current	$V_{TIP} = V^+ = 15$ V	(see fig. 5)	540	900	1040	
OUTL Current	$V_{TIP} = V^+ = 15$ V	(see fig. 4)	750	–	1400	
Mirror Current	$I_{MIRROR} = 1.0$ mA, $V_{OUTL} = 5.0$ V	(see fig. 8)	750	1245	1400	
Tip Current, No Load	$V_{TIP-RING} = 20$ V	(see fig. 7)	0.25	1.410	1.8	mA
Ring Current, No Load	$V_{TIP-RING} = -20$ V	(see fig. 7)	– 0.25	– 1.41	– 1.8	
Input Threshold Voltage, Tip-ring	$V^+ = 10$ V	(see fig. 6)	6.0	7.2	8.0	V
Clamp Voltage	$I_{TP} = 20$ mA	(see fig. 9)	22.5	25.5	30	
	$I_{TP} = -20$ mA	(see fig. 9)	– 22.5	– 25.5	– 30	
	$I_{TP} = 100$ mA	(see fig. 9)	–	3.6	5.5	
	$I_{TP} = -100$ mA	(see fig. 9)	–	– 3.6	– 5.5	

TEST CIRCUITS

Figure 2.

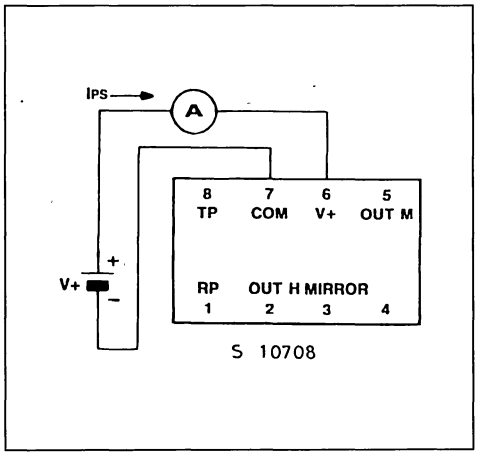


Figure 3.

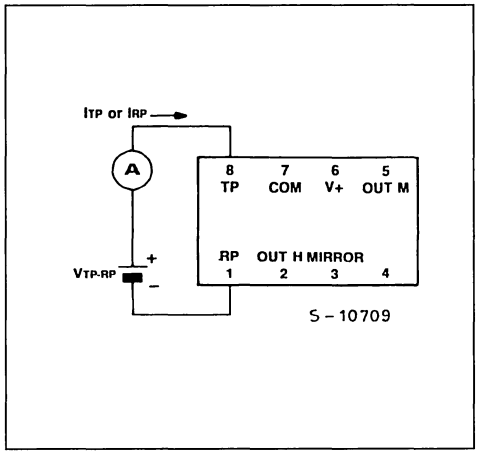


Figure 4.

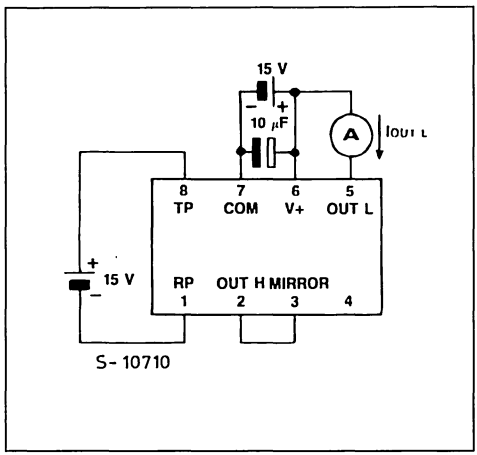


Figure 5.

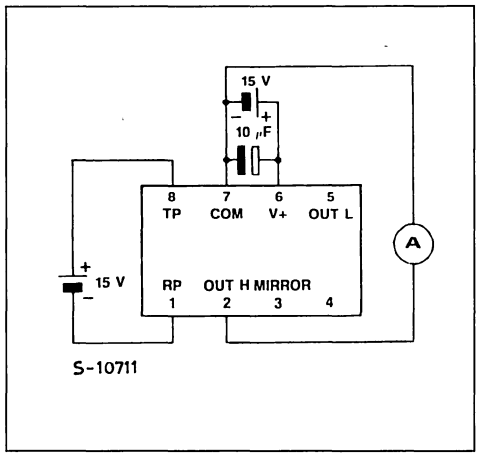


Figure 6

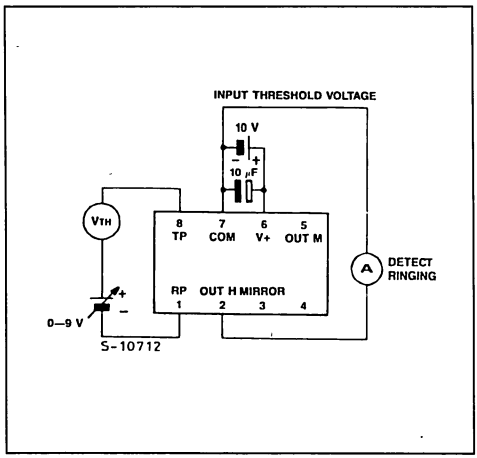


Figure 7

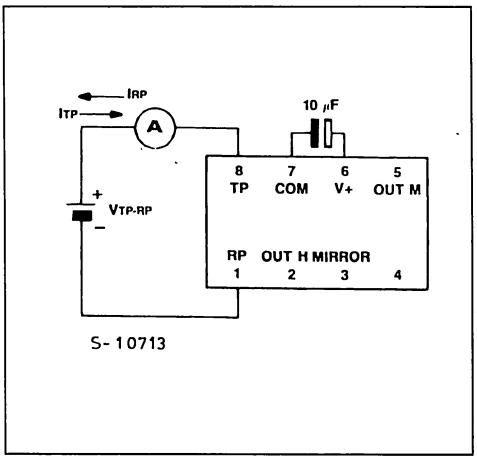


Figure 8

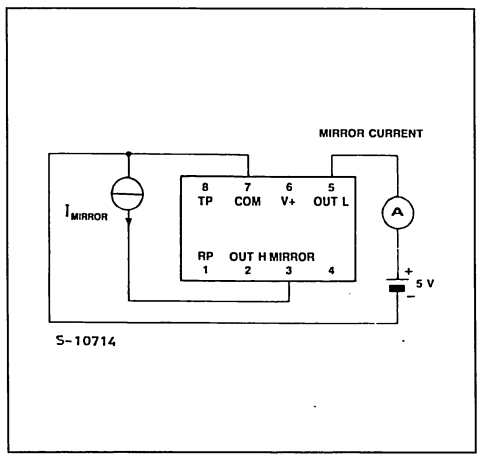
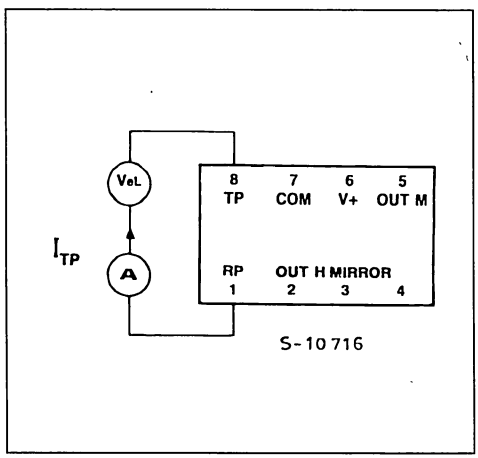


Figure 9



APPLICATION

The LB1006 detector derives its power by rectifying the AC ringing signal from the Tip-Ring pair of a telephone loop. It operates over widely varying waveforms (15 to 68 Hz at 40 to 150 V_{RMS}). It uses this derived power to activate ringing detector logic, and then transfers most of this power to an output current driver. There is essentially no loading under non-ringing conditions. This device has two outputs, OUTH and OUTL. The OUTH output is used to source output current when ringing is detected. The OUTL output will sink output current when the OUTH output is connected to the mirror input and when ringing is detected (see application diagram figure 11 and 12). The device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V+ will also allow the device to operate in what is described as "Stand Alone Applications".

Figure 10 : Simplified Output Diagram.

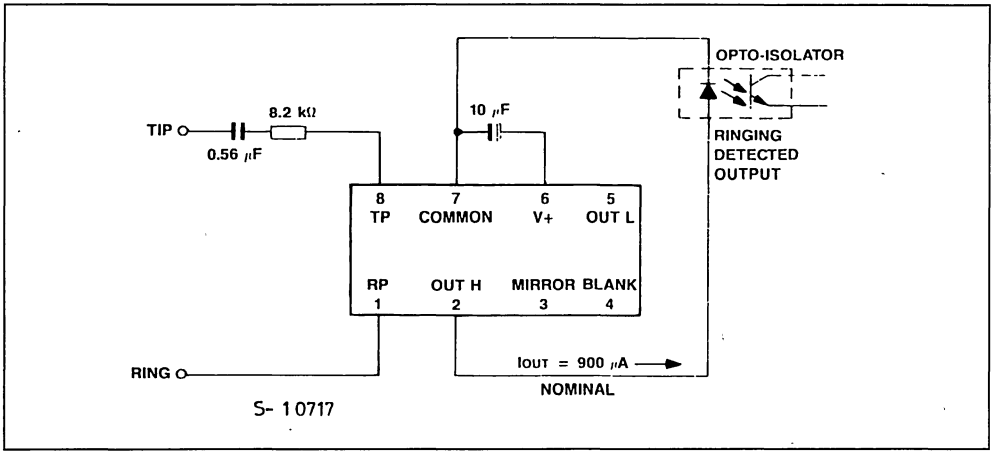


Figure 11 : Typical Application for Opto-isolator Drive.

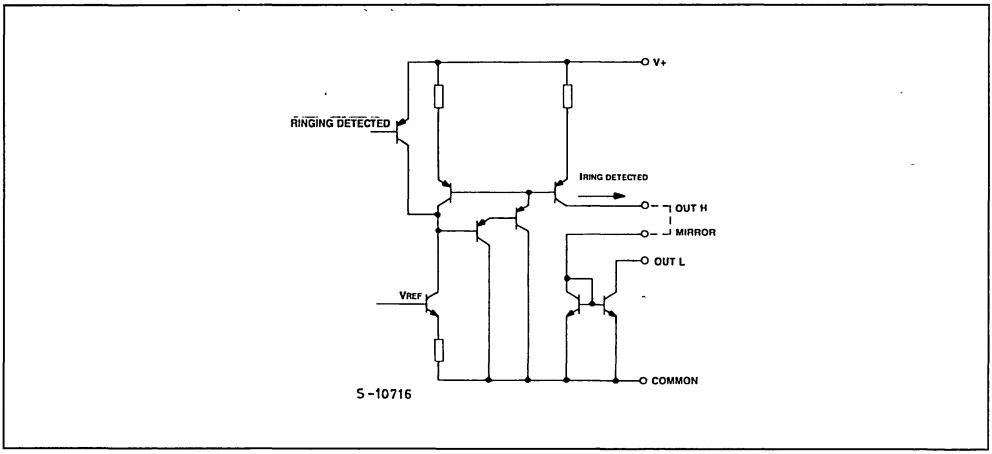
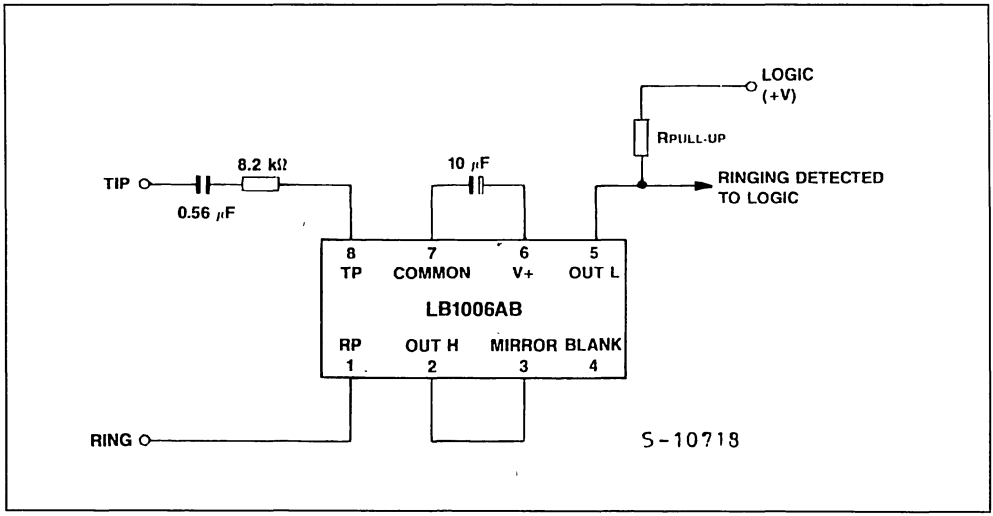


Figure 12 : Typical Application for Interface Direct to Logic.

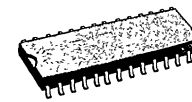


SPEAKERPHONE CIRCUITS

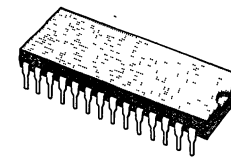
MONITOR AMPLIFIER AND RINGER

LOUDSPEAKER AMPLIFIER
- ANTI-ACOUSTIC FEEDBACK (antilarsen)
- ANTIDISTORSION BY AUTOMATIC GAIN ADAPTATION
- PROGRAMMABLE GAIN IN STEPS OF 6 dB OR LINEARLY
- ON/OFF POSITION
- LOW VOLTAGE
- POWER : 100 mW AT 5 V

RINGER
- SWITCHING REGULATOR TO TRANSFORM HIGH INTO LOW VOLTAGE IN RING MODE
- MICROCOMPUTER SUPPLY WITH RESET, HALT AND RING DETECTION SIGNAL
- TUNE GENERATION BY MCU AND RINGING BY LOUDSPEAKER



SO-28



DIP28

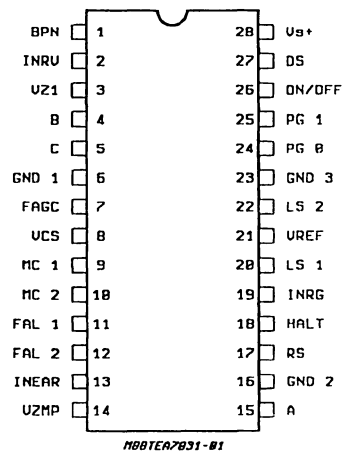
ORDER CODES : TEA7031DP (DIP28)
TEA7031FP (SO-28)

DESCRIPTION

TEA7031 is a 28-pin DIL integrated circuit providing the following facilities :
- Loudspeaker amplifier
- Anti-acoustic feed-back system (anti-Larsen system)
- Microprocessor supply and control
- Switching regulator control

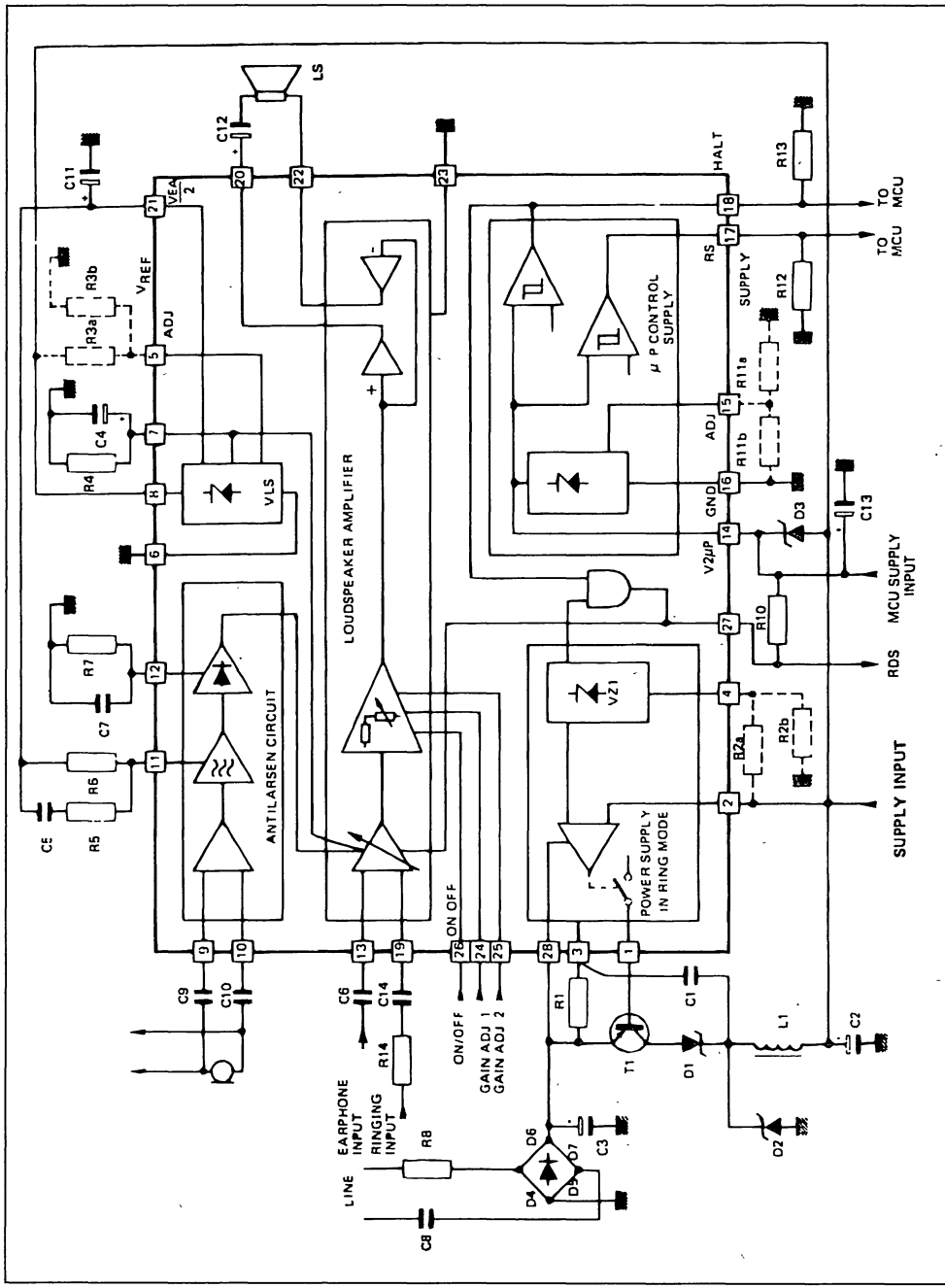
These facilities are generally electrically separated ; hence selective use of the functions provided is possible.

PIN CONNECTION (top view)



MBBTEA7031-01

BLOCK DIAGRAM



PIN DESCRIPTION

Name	N°	Description
BPN	1	Base Drive to External Transistor of the Switchmode Power Supply
INRV	2	Switchmode Power Supply Regulation Input
VZ1	3	3.5 V Reference Voltage to Switchmode Power Supply
B	4	Adjust VZ1
C	5	Adjust VLS
GND 1	6	Ground
FAGC	7	Gain Control Filter
VCS	8	Supply Voltage
MC 1	9	Microphone Input 1
MC 2	10	Microphone Input 2
FAL 1	11	Antilarsen Filter 1
FAL 2	12	Antilarsen Filter 2
INEAR	13	Earphone Input
V_{ZMP}	14	Microprocessor Supply Voltage, Internally Zener Stabilized (3.3 V)
A	15	Adjust VZMP
GND 2	16	Ground
RS	17	Microprocessor Reset Output
Halt	18	Microprocessor Halt Output
INRG	19	Input Ringing Signal
LS 1	20	Loudspeaker Output
VREF	21	Internal Reference
LS 2	22	Loudspeaker Output
GND 3	23	Ground
PG 0 PG 1	24 25	Gain Level Programming
ON/OFF	26	Loudspeaker ON/OFF
DS	27	Ring Signal Indication
V_S +	28	Rectified Ring Signal Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{LS}	Supply Voltage (adjustable)	6	V
V_{S+}	Input Voltage Rectified Ring Signal	22	V
I_{LS}	Supply Current	90	mA
P_{tot}	Power Dissipation	360	mW
V_{ZMP}	Microprocessor Short Regulator Voltage	6	V
I_{ZMP}	Microprocessor Short Regulator Current	30	mA
T_{oper}	Operating Temperature Range	– 5 to + 45	°C
T_{STO}	Storage Temperature Range	– 55 to + 125	°C

ELECTRICAL CHARACTERISTIC (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
V_{LS}	Shunt Voltage Regulator	I_{LS} = 2 mA			2.65	2.8	3.2	V
		I_{LS} = 30 mA			2.7	2.9	3.4	V
V_1	Voltage Pin 1	I_{LS} = 2 mA to 30 mA				1.25		V
$I_{AGC\ off}$	Gain Control Current	I_{LS} = 30 mA (fig. 1)					1	µA
$I_{AGC\ on}$		V_{LS} = 2.6 V (fig. 2)				− 4	− 2.5	µA
G	Loudspeaker Amplifier GAIN = $\frac{V_{22} - V_{20}}{V_{13}}$	f = 300 Hz V_{OUT} = 0.8 V_{RMS} (fig. 3)						
		ON/OFF	P_{G0}	P_{G1}				
		GND	GND	GND	12	14	16	dB
		GND	GND	V_{LS}	18	20	22	dB
		GND	V_{LS}	GND	24	26	28	dB
		GND	V_{LS}	V_{LS}	30	32	34	dB
		V_{LS}	GND	GND		− 30	− 20	dB
THD	Distortion	I_{LS} = 30 mA ; V_{OUT} = 0.8 V_{RMS} f = 300 Hz to 10 kHz (fig. 3)						
		ON/OFF	P_{G0}	P_{G1}				
		GND	V_{LS}	V_{LS}			2	%
G_{RING}	Ringing Gain GAIN = $\frac{V_{22} - V_{20}}{V_{19}}$	(fig. 4)						
		ON/OFF	P_{G0}	P_{G1}				
		V_{LS}	GND	GND	12	19	16	dB
		V_{LS}	GND	V_{LS}	18	20	22	dB
		V_{LS}	V_{LS}	GND	24	26	28	dB
		V_{LS}	V_{LS}	V_{LS}	30	32	34	dB
$Z_{MIC\ IN}$	Microphone Input	Symetrical (pins 9 - 10)				4.5		kΩ
		Asymetrical (pin 10)				36		kΩ
$Z_{EAR\ IN}$	Earphone Input					2.8		kΩ
$Z_{RING\ IN}$	Ringing Input					1.2		kΩ
I_{PG0} I_{PG1} $I_{ON/OFF}$	Input Current ON State	I_{LS} = 30 mA (fig. 3) V_{21} = V_{25} = V_{26} = GND			− 10 − 10 − 10	− 5 − 5 − 5		µA µA µA
I_{PG0} I_{PG1} $I_{ON/OFF}$	Input Current OFF State	I_{LS} = 30 mA (fig. 3) V_{21} = V_{25} = V_{26} = V_{LS}					1 1 1	µA µA µA
G_{MIC}	Microphone Gain = $\frac{V_{11}}{(V_9 - V_{10})}$	I_{LS} = 30 mA (fig. 5)			18	22	26	dB
$A_{NT\ RMS}$	Antilarsen Control = $\frac{(V_{22} - V_{20})}{V_{13}}$	I_{LS} = 30 mA (fig. 6) V_{13} = 20 mV_{RMS} V_{12} = 0.3 V_{DC} V_{12} = 0.6 V_{DC}			 20		 − 20	 dB dB

ELECTRICAL CHARACTERISTIC (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
MICROCOMPUTER SUPPLY SECTION						
V_{ZMP1}	Supply Voltage	I_{ZMP1} = 3 mA (fig. 9)	3	3.3	3.6	V
I_{ZMP}	Supply Current	V_{ZMP} = 0.8 V_{ZMP1} (fig. 10)		0,3		mA
I_{RESET}	Reset ON	V_{17} = 0 V ; V_{14} = V_{ZMP1}			1	µA
	Reset OFF	V_{17} = 0 V ; V_{14} = 0.8 V_{ZMP1}		– 150	– 75	µA
I_{HALT}	Halt ON	V_{18} = 0 V ; V_{14} = V_{ZMP1}			1	µs
	Halt Off	V_{18} = 0 V ; V_{14} = 0.8 V_{ZMP1}		– 150	– 75	µA
SWITCH MODE SUPPLY SECTION						
V_{SA}	Maximum Input Voltage	I_{VS} = 1 mA, (fig. 7)	22			V
V_{21}	Voltage Reference	V_{S+} = 22 V ; V_{LS} = 2,8 V (fig. 7)	3,2	3,5	3,8	V
$I_{BPN\ ON}$ $I_{BPN\ OFF}$	PNP Base ON PNP Base OFF	V_{14} = 0 V ; V_2 = 3 V (fig. 8) V_{14} = 0 V ; V_2 = 4 V (fig. 8)	1	2	 1	mA µA
$V_{Z1\ ADJ}$	Adjust VZ1	V_{14} = 0 V ; V_2 = 4 V (fig. 8)		1.1		V
$I_{DS\ ON}$ $I_{DS\ OFF}$	Ring Detection ON Ring Detection OFF	V_{14} = 3.5 V (fig. 8) V_{14} = 0.8 X V_{ZMP1} (fig. 8)	0,8	14		mA µA

Figure 1 : Test VLS, VREF, I AGC, V (5).

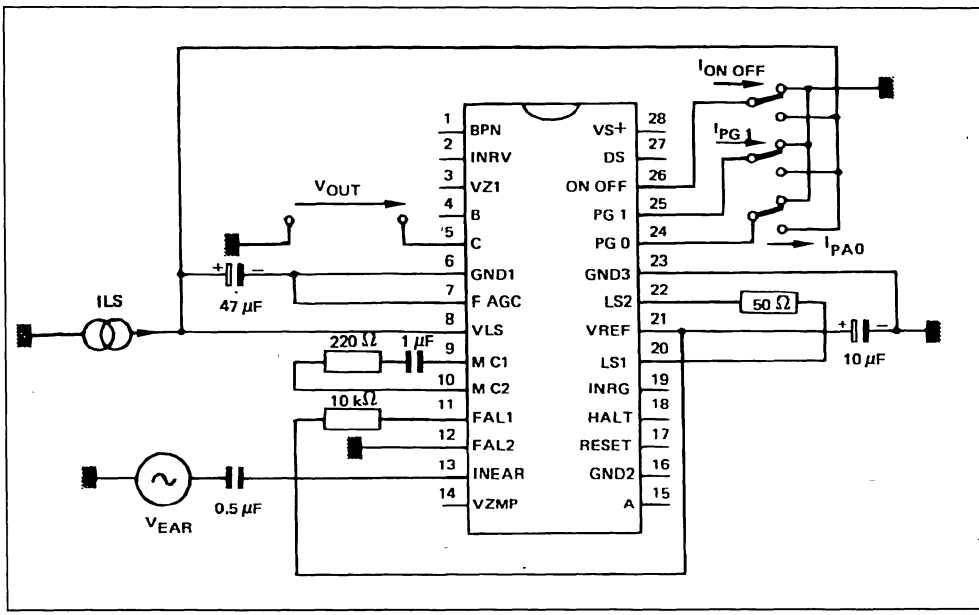


Figure 2 : Test Power Supply - ILS - I AGC.

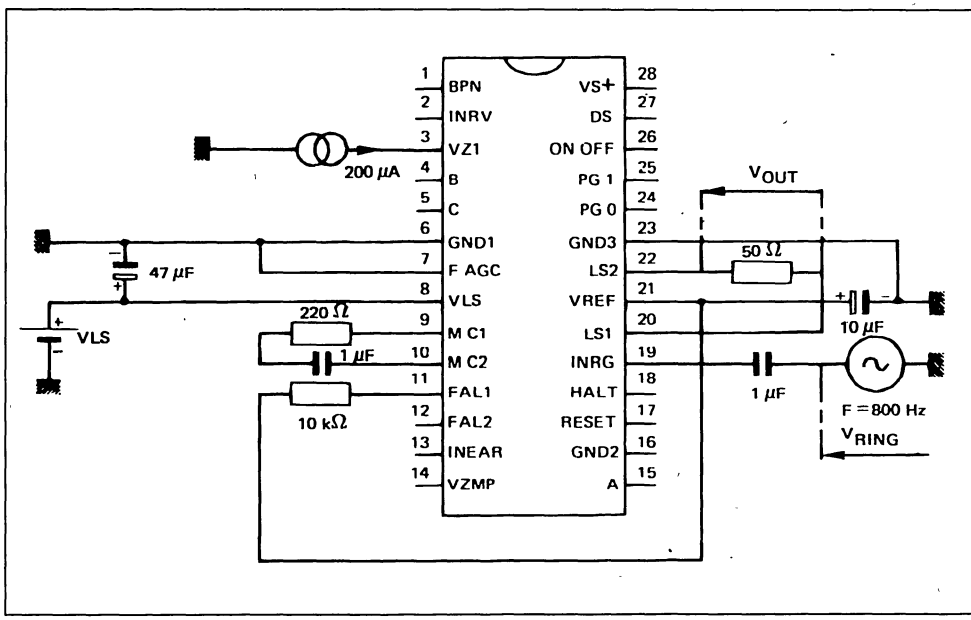


Figure 3 : Test Loudspeaker Amplifier - Gain - Distortion - ILS.

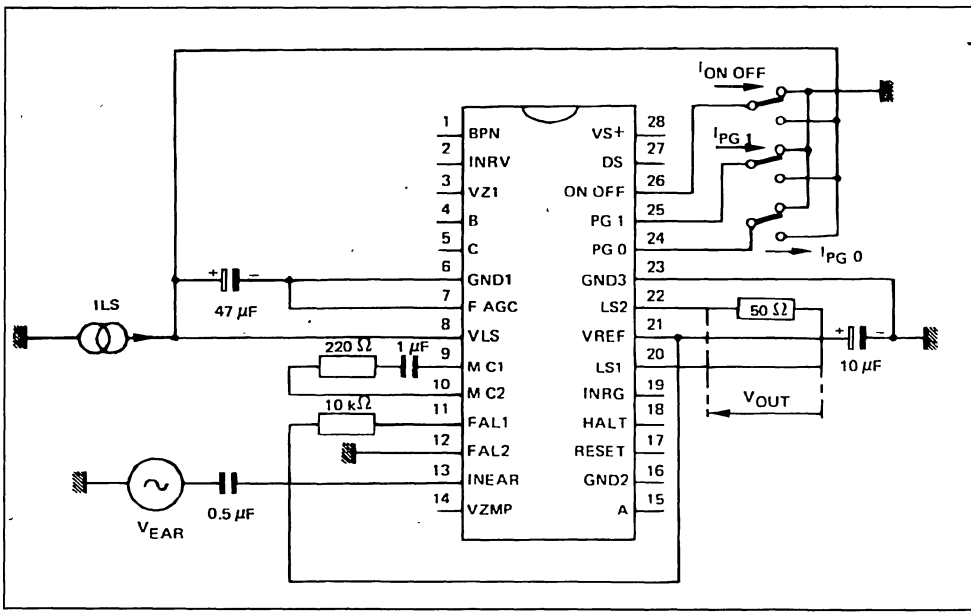


Figure 4 : Test Amplifier.

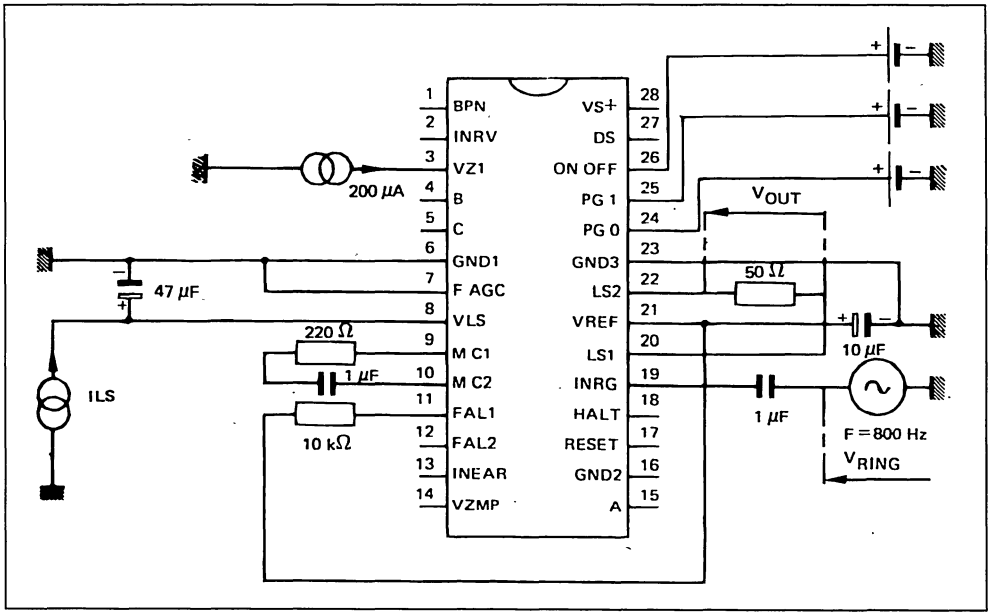


Figure 5 : Test Antiacoustic System Efficiency.

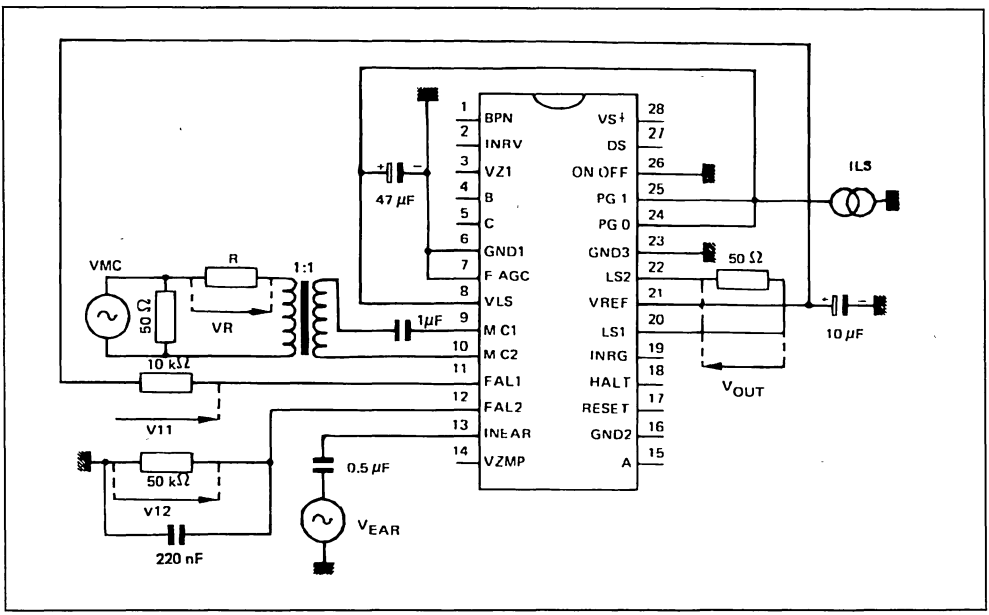


Figure 6 : Test Antiacoustic System Efficiency.

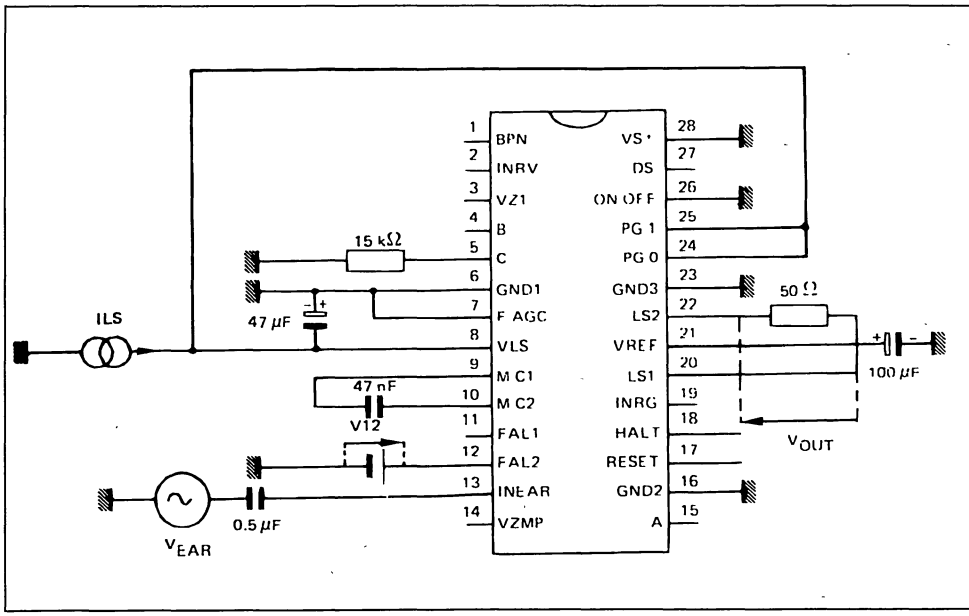


Figure 7 : Test Power Supply in Ring Mode - VZ1 - IBPN - IDS.

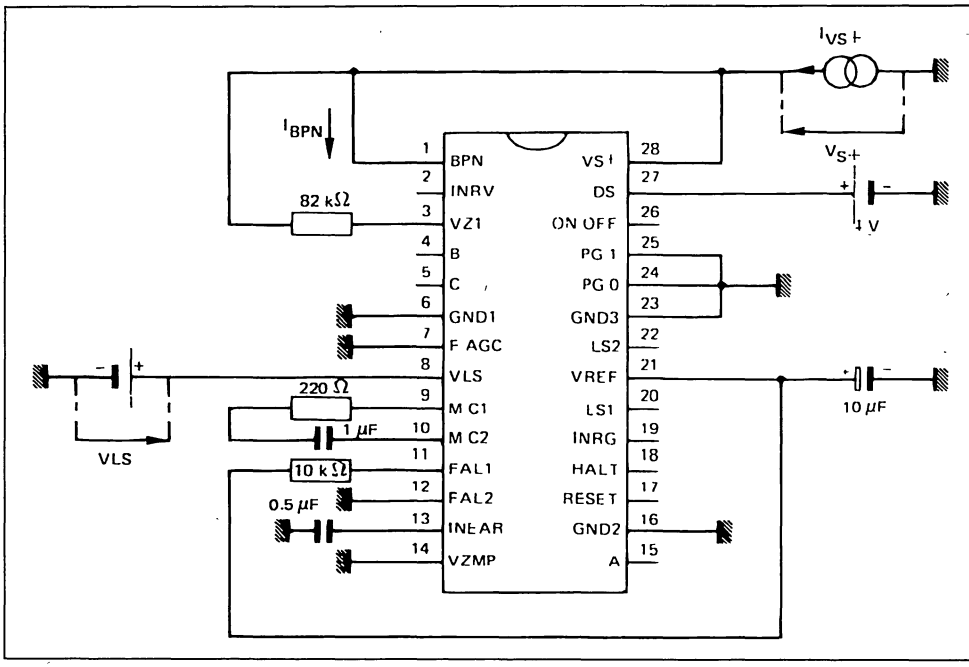
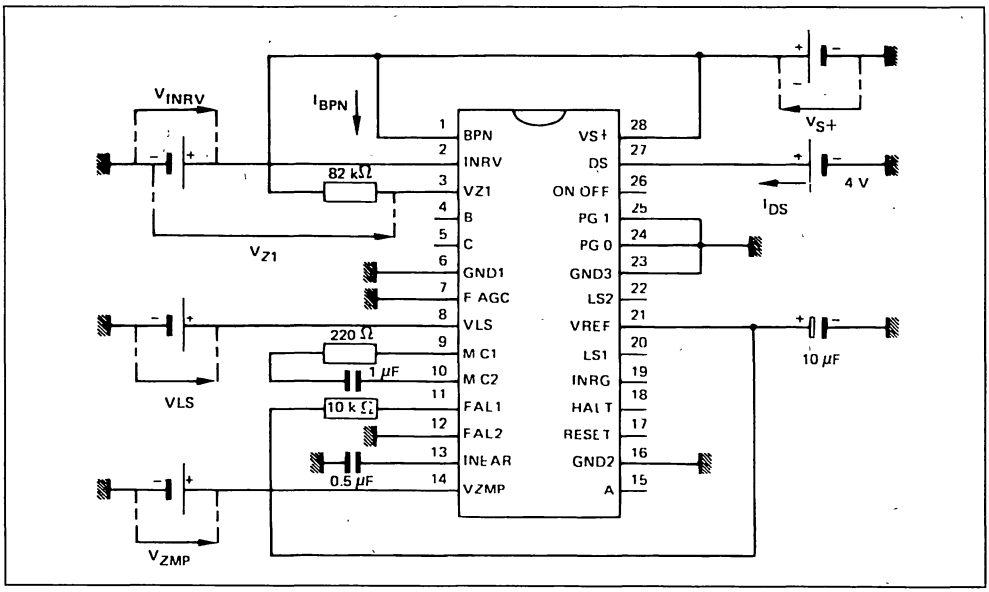


Figure 8 : Test Power Supply in Ring Mode - VB + MAX.



CIRCUIT DESCRIPTION

TEA7031 is a 28-pin DIL integrated circuit providing the following facilities :

- Loudspeaker amplifier
- Anti-acoustic feed-back system (anti-Larsen system)
- Microprocessor supply and control
- Switching regulator control

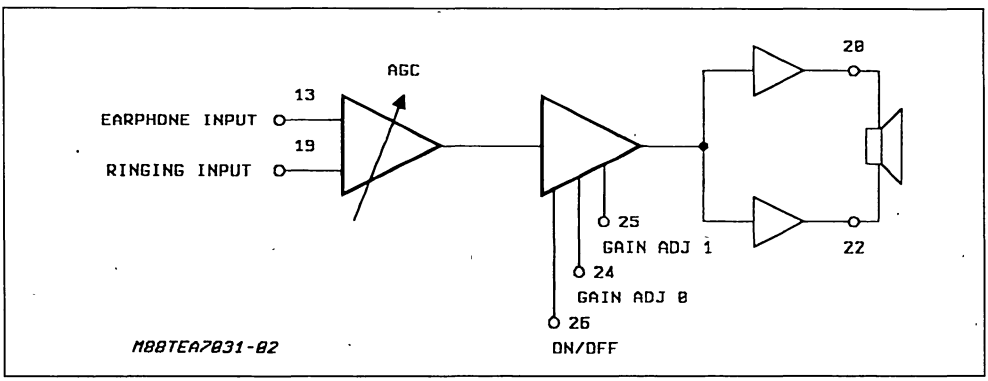
These facilities are generally electrically separated ; hence selective use of the functions provided is possible.

1.1 LOUDSPEAKER AMPLIFIER

The amplifier is divided into 3 main sections :

a) Automatic Gain Control (AGC)
b) Preamplifier
c) Push-pull amplifier (bridge structure).

Figure 9 : Loudspeaker Amplifier.



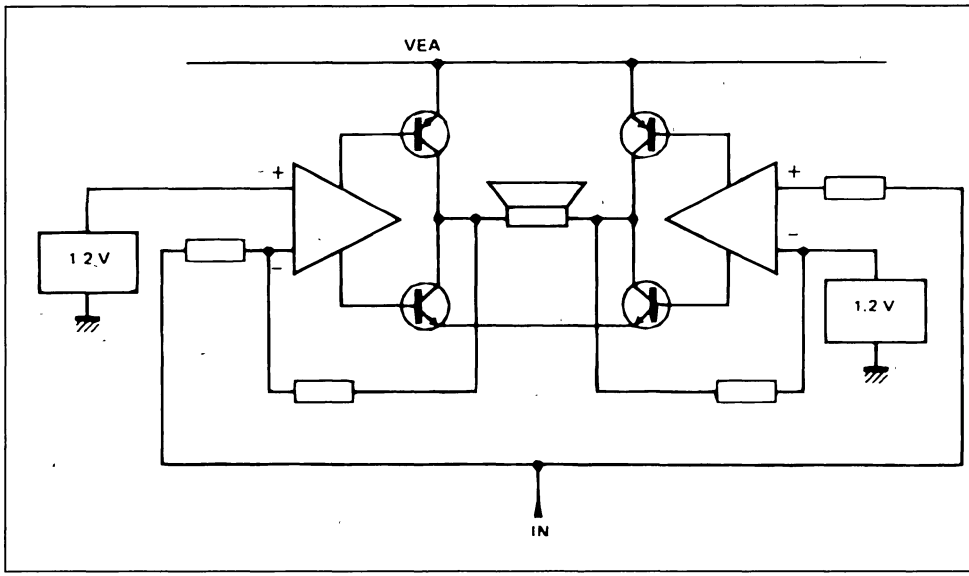
a) The AGC section is used for the anti-Larsen and anti-distortion system.

- When used in a telephone set to avoid Larsen effect the AGC automatically decreases loudspeaker amplifier gain.
- When the required output level exceeds the capabilities of the available current, the AGC decreases the loudspeaker amplifier gain to avoid distorsion.

b) The preamplifier permits step control of amplifier gain in steps of 6 dB, using pins GAIN ADJ 1 and 2, which may be controlled using switches or by a microprocessor.
The amplifier may be muted using the ON/OFF control signal (pin 26).

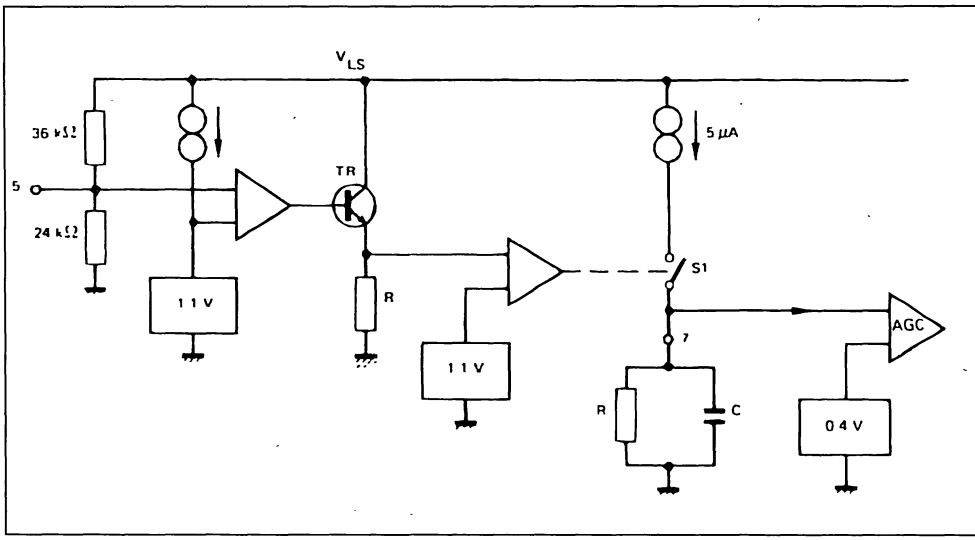
c) The output amplifier uses a double push-pull configuration (H bridge) to get maximum dynamic range under limited supply conditions.

Figure 10 : Output Stage.



Amplifier DC Supply.
In transmission mode, the supply voltage is controlled by the internal shunt DC regulator. For this reason, the TEA7031 should be supplied from a current source (see : supply considerations).
An anti-distortion system is embodied which provides AGC control to avoid loudspeaker distortion under current-limited conditions.

Figure 11.



Circuit action.

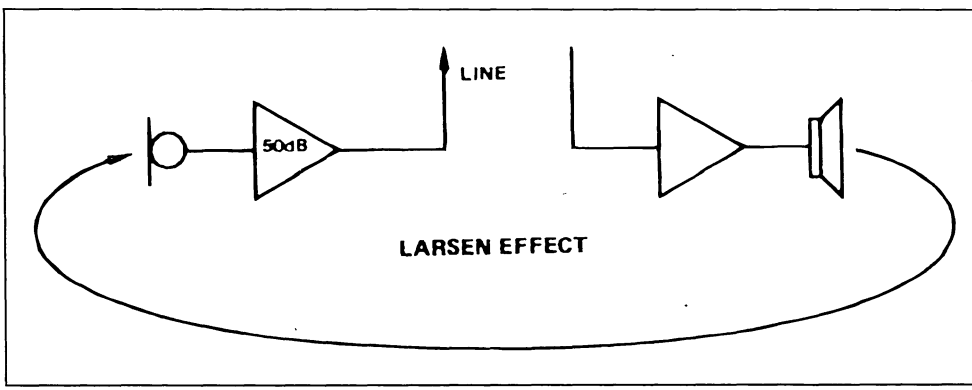
When the supply voltage is unsufficient, the voltage at pin 5, falls below the reference voltage 1.1 V, resulting in transistor (TR) being switched off, resulting in zero current flow in resistor R. This state enables the gain control system. Under these conditions, the shunt DC supply will switch at a rate determined by the time constant of the RC network on pin 7.

This switching action accomodates normal speech characteristics under low supply conditions.

1.2 . ANTIACOUSTIC FEEDBACK SYSTEM (antilarsen system).

The purpose of this system is to control AGC action, in order to avoid acoustic feedback between the loudspeaker and the microphone, when used in a telephone set.

Figure 12.



Principle of Operation.

When examining, the spectral density of the voice area and the Larsen area, it may be seen that the dominant features of each exist in different frequency bands.

To extract the Larsen component, the microphone signal is first filtered by a second order filter (formed by two first order filters), then amplified and rectified in order to produce the AGC control signal.

Figure 13.

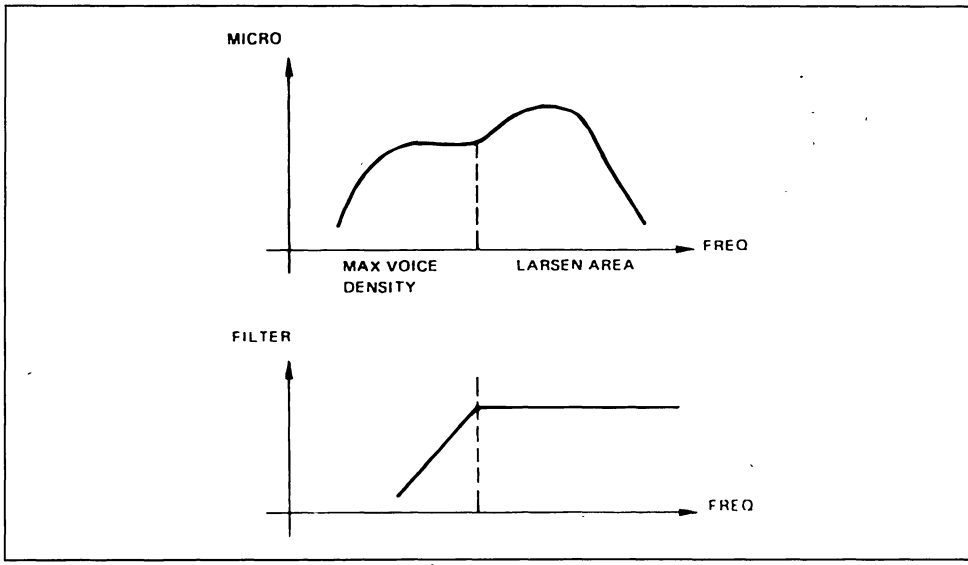
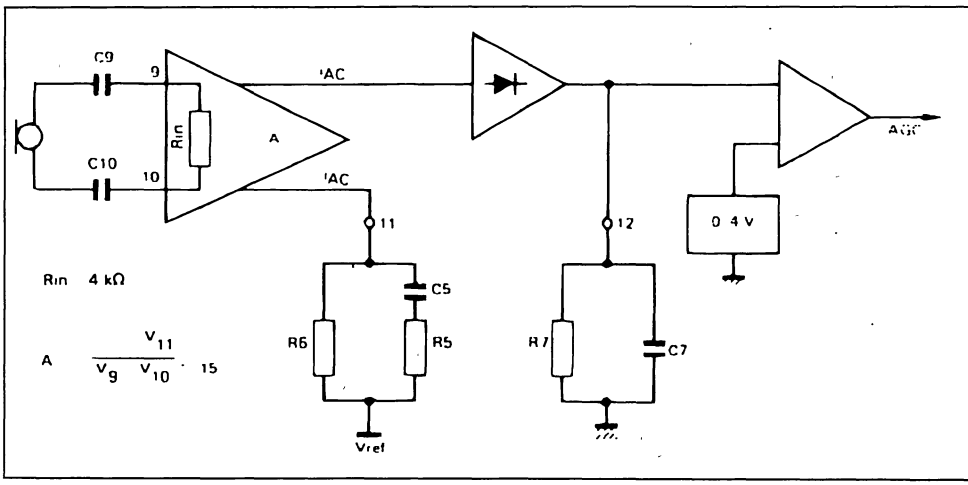


Figure 14.

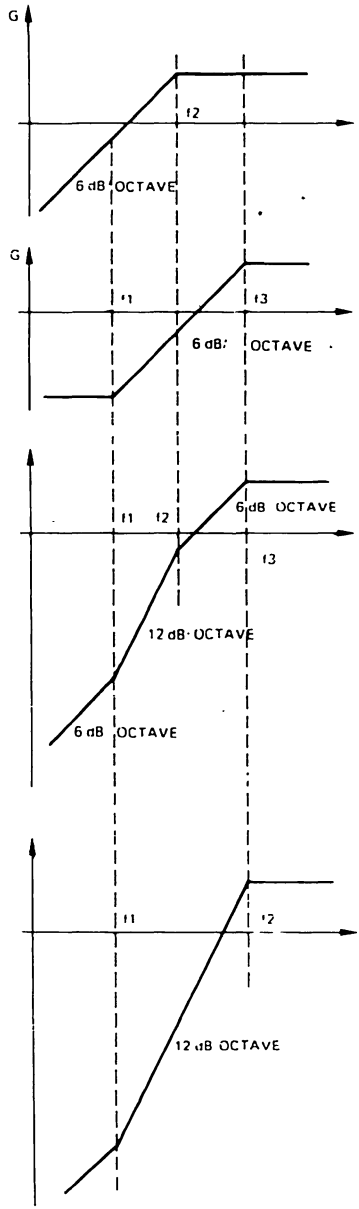


$$i_{AC} = \frac{V_{pin\ 11}}{Z_{pin\ 11}} \quad \text{with} \quad \frac{1}{Z_{pin\ 11}} = \frac{1}{R6} + \frac{1}{R5 + \dfrac{1}{C5j\omega}}$$

$$V_{DC\ pin\ 12} = \frac{i_{AC}\ (RMS) \cdot 2\sqrt{2}}{\pi} R7$$

The first filter is generated by the capacitors on pins 9 and 10 and the input resistor Rin ; the second filter by the RC network on pin 11.

Figure 15.



- Filter on pins 9-10 :

$$f2 = \frac{C9 + C10}{2\pi \,.\, Zin.C9.C10}$$

- Filter on pin 11 :

$$f1 = \frac{1}{2\pi\,(R6 + R5)\,C5}$$

$$f2 = \frac{1}{2\,R5\,C5}$$

- Anti-Larsen system filter response.

- Theoretical result.

If f2 = f3 the anti-Larsen system filter is equivalent to a second order filter.

f2 = f3

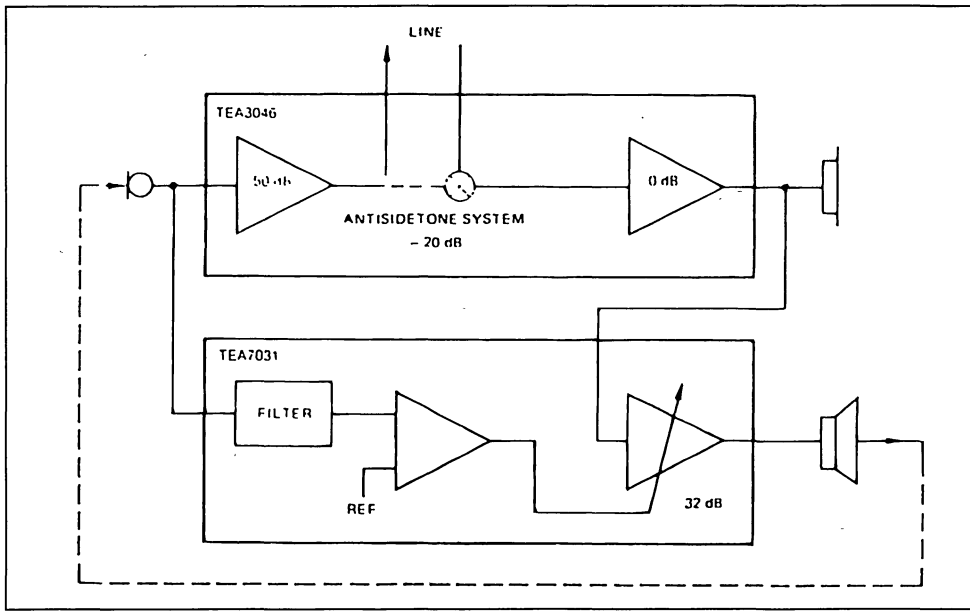
$$\frac{C9 + C10}{2\,\pi\,.\,Zim.C9.C10} = \frac{1}{2\,\pi\,R5\,C5}$$

A complete telephone set has two anti-Larsen systems :

- one in the transmission circuit (for example : TEA7050) antisidetone network ;
- one in the loudspeaker amplifier (for example: TEA7031).

Together these form a high efficiency anti-Larsen system.

Figure 16.



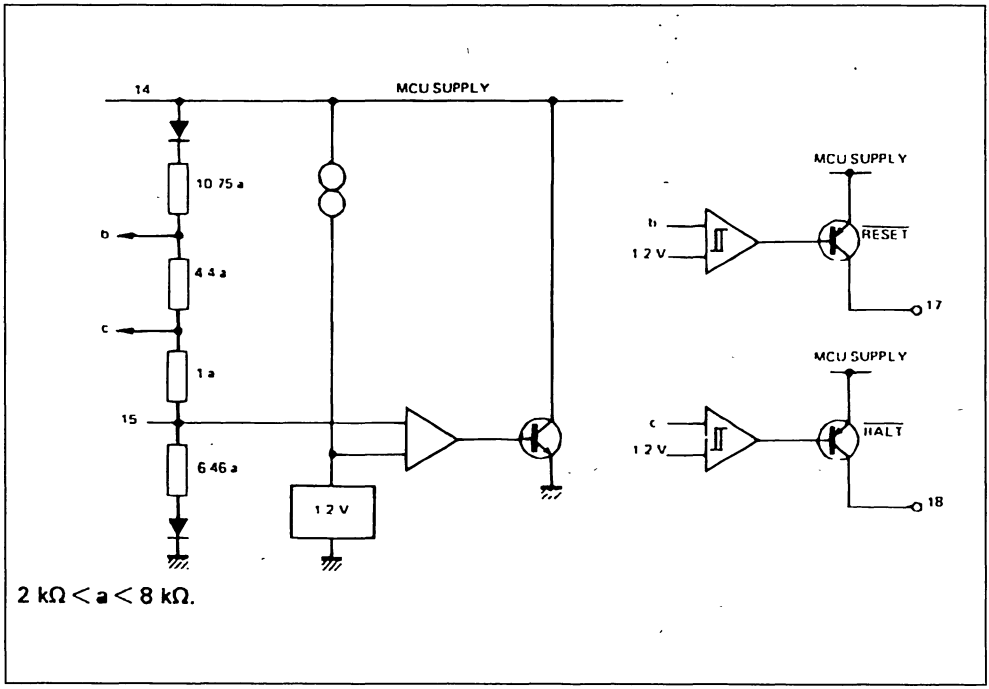
1.3 . MICROPROCESSOR CONTROL.

TEA7031 provides the following signals for an associated microprocessor :

- halt and reset signal,
- a regulated supply.

The MCU shunt supply voltage is internally fixed at 3.2 V but can be adjusted via pin 15.

Figure 17.

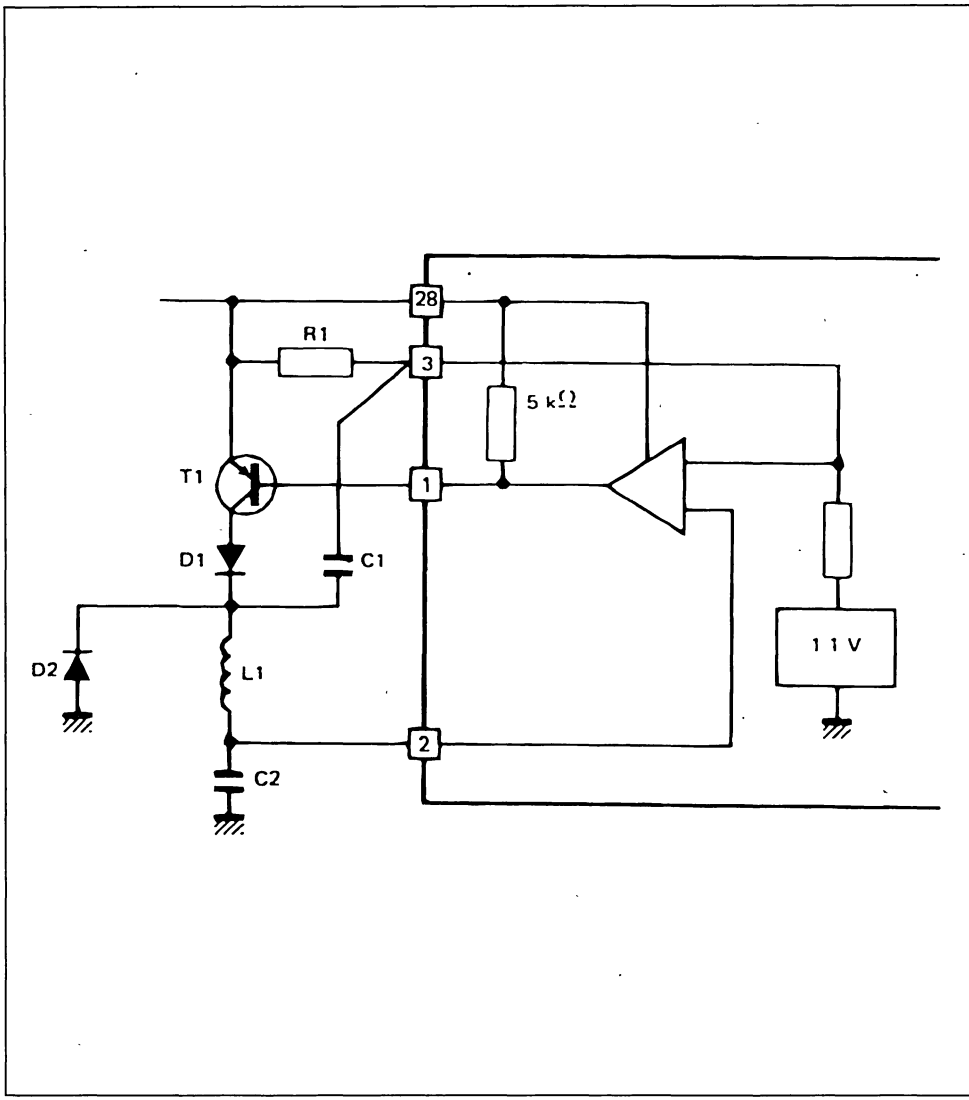


Note : Reset and Halt outputs, which are open collector outputs, require external resistors to zero volt.

1.4 . SWITCHING CONVERTER.

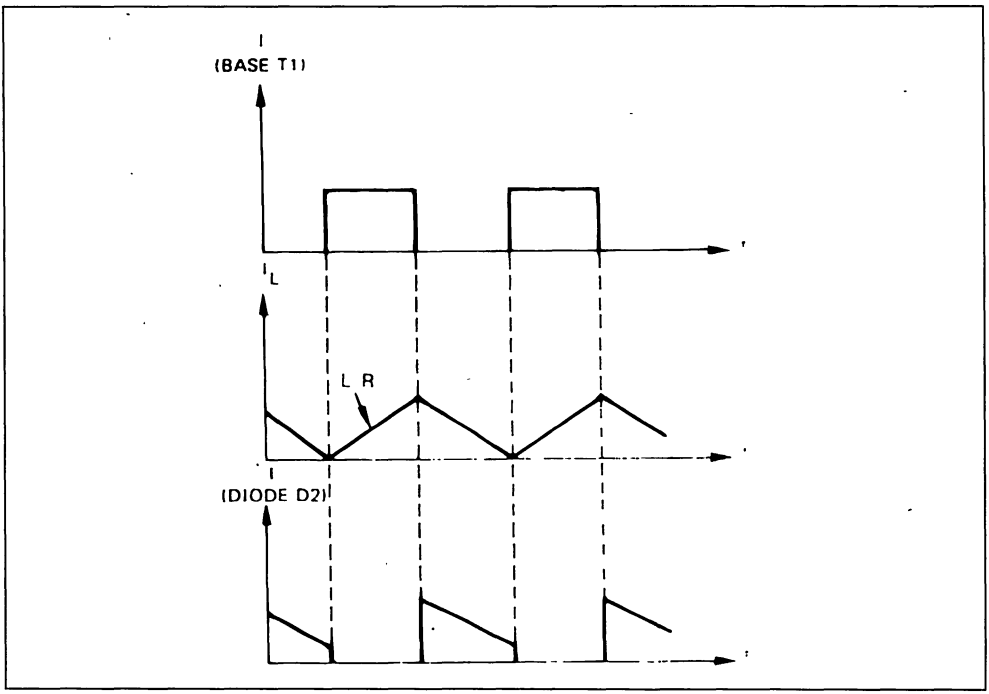
Under ringing conditions the line supply available has a high voltage (~ 22 V), low current (~ 6 mA) characteristic. In order to be used by the I.C., this supply has to be converted to a low voltage (~ 3.5 V) and higher current (15 – 20 mA), using a switching converter.

Figure 18.



Transistor T1 is switched either ON/OFF via pin 1 in accordance with the result of a comparison between an internal reference voltage and the I.C. supply voltage (pin 2). When transistor T1 is off, the diode D2 provides a return current path for L1.
Under speech conditions, the switching converter has to be isolated from the main supply VLS by D1, to prevent reverse current.

Figure 19.



Internal conditions during switching converter operation :

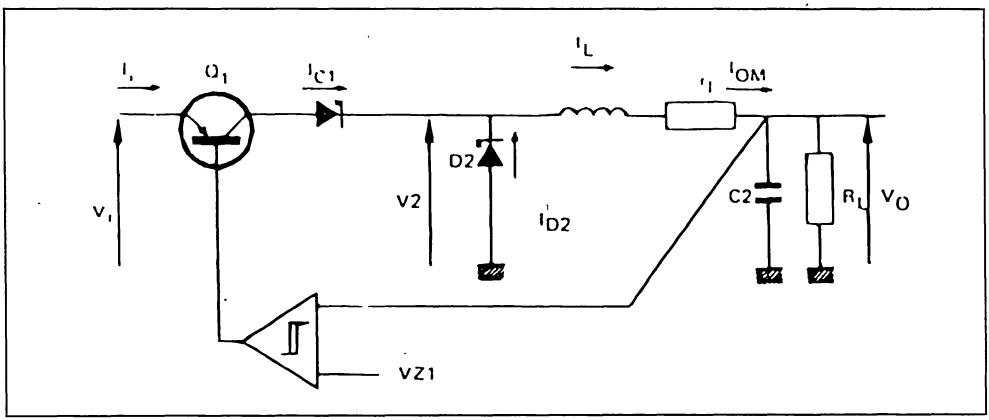
- the internal zener diodes VLS, MCU supply are automatically disconnected,
- the Earphone input is OFF and ringing input is ON.

Note : For better converter efficiency, it is advisable to use schottky diodes for D1 and D2.

SWITCHING POWER SUPPLY EFFICIENCY.

Contribution of external components

Figure 20.

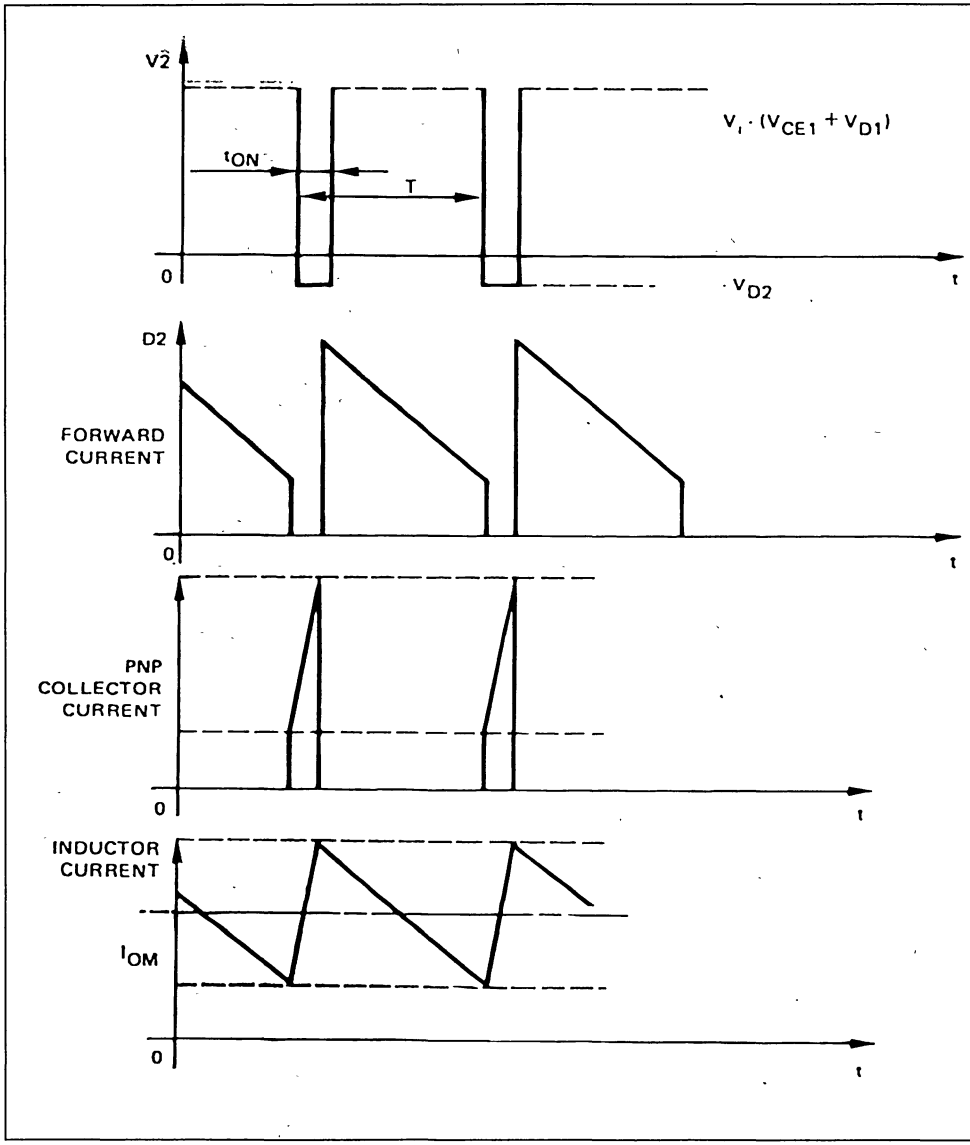


EQUIVALENT DRAWING :

Efficiency calculation hypotheses :

- I_{OM} average output current
- $R_L \cdot C_2 > T.T$ = switching period
- Duty cycle $\tau r = \frac{t_{on}}{T}$
- Be careful that resonance frequency of $L.C_2$ must be lower than switching frequency.

Figure 21.



If Po = load output power
Pe = input power

If Ppo = dissipated power in D2 and L
Ppe = dissipated power in Q1 and D1
Po = Pe – Ppo – Ppe

The efficiency is $o = \frac{Po}{Pe} = 1 - \frac{Ppo + Ppe}{Pe}$

Dissipated power in D2 and L
$Ppo . (V_{D2} + r o . I_{OM}) . I_{OM} (1 - \tau_r)$
V_{D2} = forward voltage of D2

Dissipated power in Q1 and D1
$Ppe = (V_{D1} + V_{CES1}) . I_{OM} . \tau_r$
V_{D1} = forward voltage of D1

V_{CES1} = Saturation voltage (at $I_C = I_{OM}$) of Q1

Relation between o and τ_r

$$\tau_r = \frac{Vo}{Vi} \cdot \frac{1}{e} \text{ detail } \begin{cases} Po = o \cdot Po \\ Vo, I_{OM} = o \cdot I_{OM} V_i \cdot \tau_r \end{cases}$$

$$\rho = \frac{Vo}{Vi} = \frac{Vi - (V_{D1} + V_{CES1}) + V_{D2} + r o \cdot I_{OM}}{Vo + V_{D2} + ro \cdot I_{OM}}$$

2 . PIN FUNCTIONS

PIN 1 : SWITCHING CONVERTER DRIVE OUTPUT :

Base drive output for the external PNP switching transistor in the switching converter. This switching transistor should have the following characteristics :

$V_{CEO} > 30$ V ; $I_C > 200$ mA ; $G_{min} > 100$; $f_T \geq 1$ MHz.

PIN 2 : SWITCHMODE POWER SUPPLY REGULATION INPUT :

This input provides the voltage sensing feedback input to the switching converter.

PIN 3 : VZ1 : REF. VOLTAGE TO SWITCHING CONVERTER COMPARATOR :

With pin 4 open circuit, VZ1 is internally stabilized at 3.5 V.

PIN 4 : ADJUST VZ1 :

This pin is used to adjust the switching converter power supply reference voltage.

PIN 5 : ADJUST VLS :

This pin is used to adjust the I.C. supply voltage.

PINS 6 - 16 - 23 : GROUND :

These pins have to be connected together.

PIN 7 : AUTOMATIC GAIN CONTROL FILTER :

The anti-distortion system response is adjusted by the RC network on this pin.

PIN 8 : CIRCUIT SUPPLY VOLTAGE :

With pin 5 open circuit, VLS is internally stabilized at 2.8 V.

When the TEA7031 is under AGC control, the voltage on this pin varies slightly (due to AGC action).

PIN 9/10 : MICROPHONE INPUTS :

These are used for anti-Larsen control.

PIN 11 : ANTI-LARSEN FILTER 1

The second filter of the anti-Larsen system (1 st filter : pins 9-10) is formed by the RC network R5C5. In order to obtain a second order filter for the anti-Larsen system, the cut-off frequency defined at this pin, should be the same as that chosen for the first filter.

For correct TEA7031 operation R6 and R5 should be fixed at 10 kΩ and 1 kΩ respectively.

PIN 12 : ANTI-LARSEN FILTER 2 :

The gain and the response of the anti-Larsen system can be adjusted respectively by the resistor and the capacitor on this pin, according to the acoustic characteristics of the telephone set.

The value of the resistor should not exceed 390 kΩ. When the voltage on this pin exceeds the threshold voltage of 0.4 V, the AGC system is enable.

PIN 13 : EARPHONE INPUT.

Input for loudspeaker signal. This input is only active in transmission mode, but not in ringing mode ; in ringing mode, input pin 19 should be used for amplification of ringing tones. In transmission mode no signal should applied on pin 19, for a proper working of the I.C.

PIN 14 : MICROPROCESSOR SUPPLY VOLTAGE.

With pin 15, open circuit, MCU supply is internally stabilized at 3.3 V, and is available for microprocessor supply purposes.

PIN 15 : MCU SUPPLY ADJUST.

This pin is used to adjust the microprocessor supply voltage.

PIN 17 : MICROPROCESSOR RESET OUTPUT.

This output is an open collector output which delivers a reset signal for a microprocessor.

PIN 18 : MICROPROCESSOR HALT OUTPUT.

This output is an open collector output with delivers a halt signal for a microprocessor.

PIN 19 : SQUARE WAVE RINGING MELODY SIGNAL INPUT.

Input for loudspeaker signal.

This input is only active in ringing mode (when supplied by the switching supply). In transmission mode (when supplied by the shunt DC supply), input 13 should be used and no signal should be applied on pin 19. In ringing mode, it could be used, for example, to generate the microprocessor melody.

PINS 20-22 : LOUDSPEAKER OUTPUTS.

Outputs to be connected to a 50 Ω impedance loudspeaker.
Output voltage : Vpp = 2 VLS – 2.5 Volts (with a gain of 32 dB).
Maximum current : depending of the supply voltage.

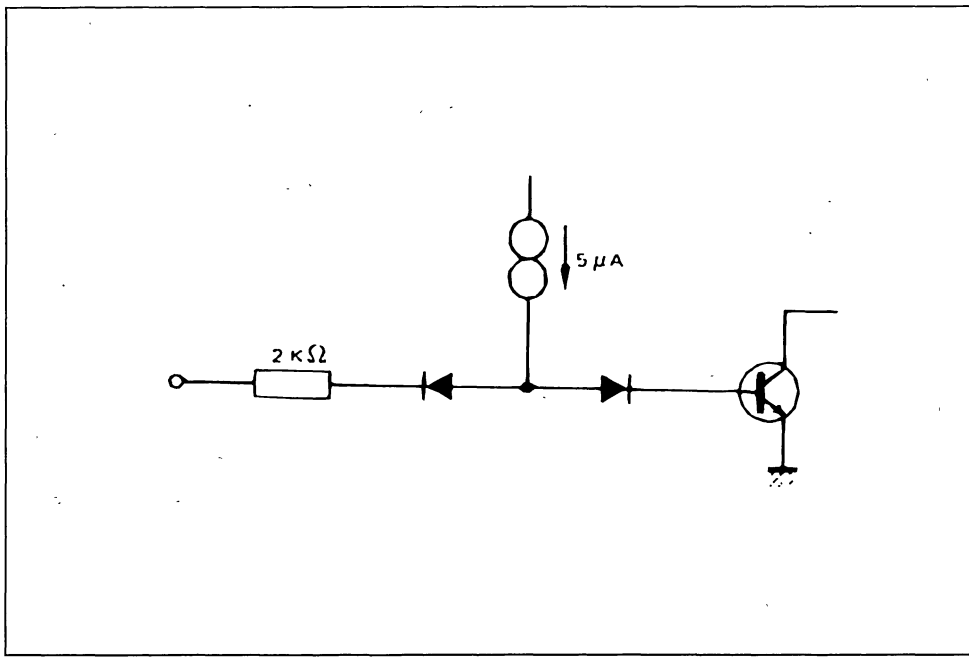
PIN 21 : V_{ref} : INTERNAL REFERENCE.

Output which provides an internally regulated reference voltage.
V_{ref} : 1.1 V typical.

Maximum available current : 5 µA.

PINS 24-25 : GAIN ADJUSTMENT INPUTS.

These pins are used to adjust the loudspeaker amplifier gain. Four steps of 6 dB/step are available (pin open circuit = high level).



GAIN ADJUSTEMENT INPUTS

GAIN ADJ 0	GAIN ADJ 1	
1	1	G_{MAX}
1	Ø	G_{MAX} – 6 dB
Ø	1	G_{MAX} – 12 dB
Ø	Ø	G_{MAX} – 18 dB

PIN 26 : LOUDSPEAKER MUTING.

This pin is used to mute the loudspeaker. Pin open-circuit = high level = loudspeaker muted. Pin low level = loudspeaker enabled.

PIN 27 : RING SIGNAL INDICATION.

This NPN open collector output provides ready status when in ringing condition.

DS is ON (low-level) when the switching converter is established in the running state and when the microprocessor supplies are stabilized. The DS signal is validated by "Halt".

It may be used to cause an associated microprocessor to generate the ringing tones.

PIN 28 : RECTIFIED RING SIGNAL INPUT.

High voltage input for the switching converter.

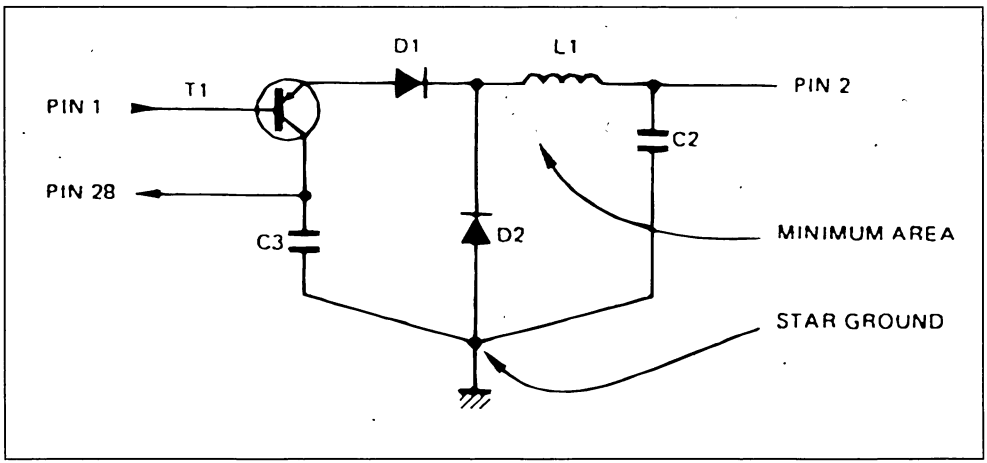
Maximum voltage : 22 V.

3 . SUPPLY CONSIDERATIONS

3.1 . SWITCHING SUPPLY LAY-OUT.

To avoid switching-noise, C2, C3, D2 should be tied together as close as possible.

Figure 23.



3.2 . TEA7031 SUPPLY.

As the I.C. has a zener characteristic, it should be supplied by a current source.

Constant voltage supply :

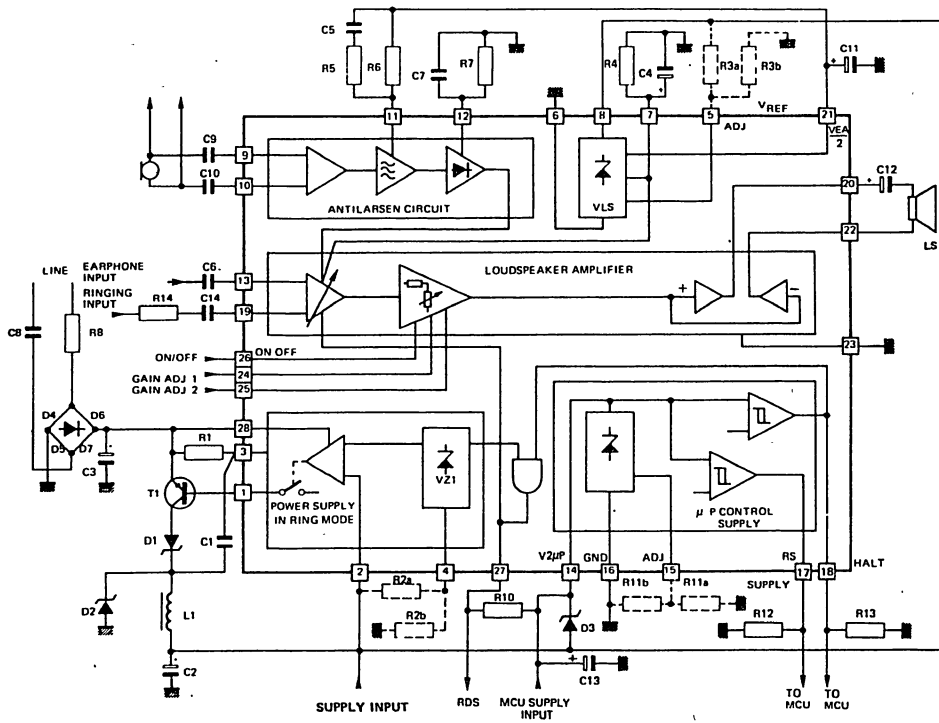
The TEA7031 can be supplied by an external constant voltage on condition :

To set the zener voltages at a level higher than the supply voltage.

To tie the automatic gain control pin (pin 7) to the ground (otherwise the I.C. will always be in AGC mode).

Note : The maximum loudspeaker level is depending of the supply voltage.

Figure 24 : Typical Application.



LIST OF COMPONENTS

RESISTORS :

R1 : 22 kΩ
R2 :
R3 :
R4 : 470 kΩ
R5 : 1 kΩ
R6 : 10 kΩ
R7 : 330 kΩ
R8 : 1 kΩ/1 W
R9 : (5 kΩ)
R10 : 100 kΩ
R11 :
R12 : 100 kΩ
R13 : 100 kΩ
R14 : 47 kΩ

CAPACITORS :

C1 : 22 pF
C2 : 220 μF/10 V
C3 : 10 μF/35 V
C4 : 10 μF/10 V
C5 : 68 nF
C6 : 220 nF
C7 : 470 nF
C8 : 1 μF/250 V
C9 : 33 nF
C10 : 33 nF
C11 : 33 μF/10 V
C12 : 22 μF
C13 : 33 μF/10 V
C14 : 1.5 nF

DIODES :

D1 : BAT43
D2 : BAT43
D3 : BAT43
D4 : 1N4004
D5 : 1N4004
D6 : 1N4748-BZX 85C (22 V)
D7 : 1N4748-BZX 85C (22 V)

INDUCTOR :

L1 : 470H - 680 H

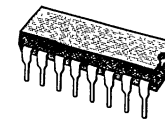
TRANSISTOR :

T1 : BCW93 - BCW92

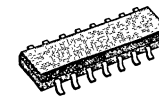
TEA7531

MONITOR AMPLIFIER

- PROGRAMMABLE GAIN IN STEPS OF 6dB OR LINEARLY
- ON/OFF POSITION
- LOW VOLTAGE
- POWER : 100mW AT 5V



DIP-16
(Plastic 0.25)



SO-16J

ORDER CODES : TEA7531DP (DIP16)
TEA7531FP (SO-16J)

DESCRIPTION

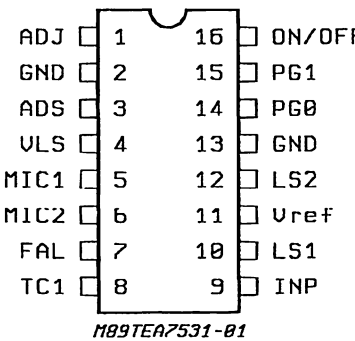
This 16 pins IC is designed for monitor (loudspeaker) telephone set and provides :

a) Signal amplification for monitoring (loudspeaker)

b) Antiacoustic feedback (antilarsen)

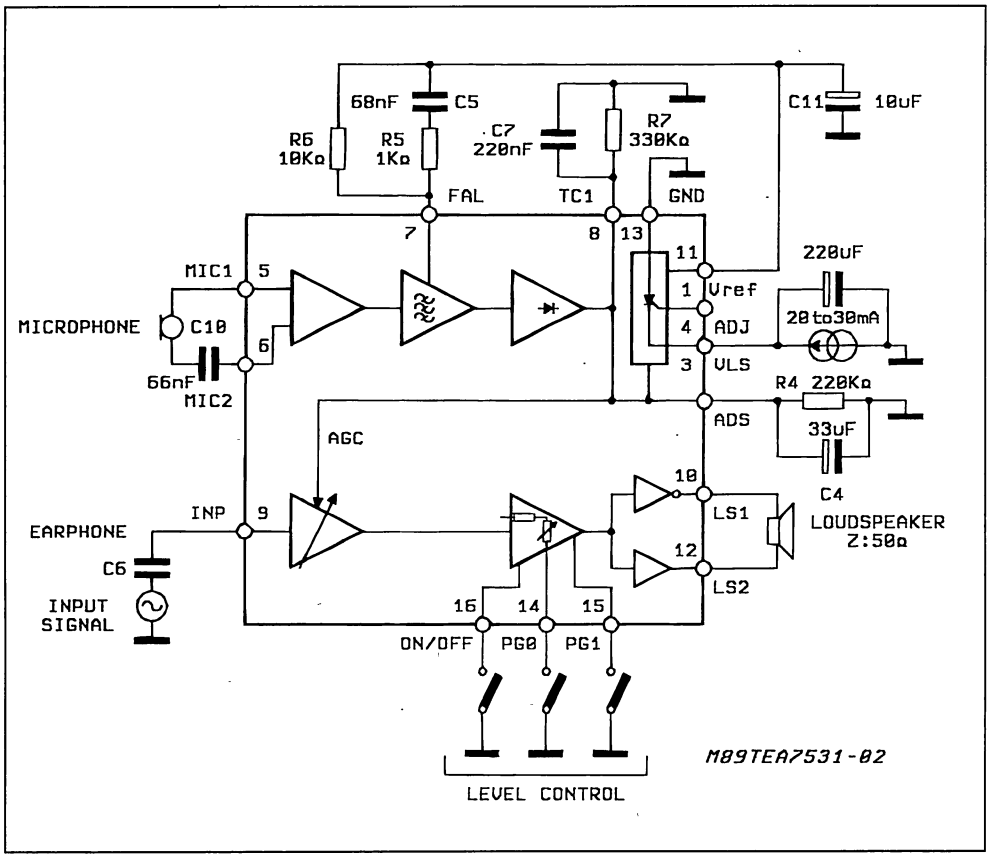
c) Antidistortion by automatic gain adaptation

PIN CONNECTION (top view)



M89TEA7531-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{op}	Temperature Range	– 5 to + 45	°C
V_{LS}	Supply Voltage	6	V
I_{LS}	Supply Current for T > 300ms for T ≤ 300ms	90 150	mA mA
V_L	Voltage Level (pins, PG0, PG1, ON/OFF)	– 0.6 > to V_{LS} + 0.6	V

PIN DESCRIPTION

N°	Symbol	Description
1	ADJ	Adjust Internal Reference V_{LS}
2	GND	Ground
3	ADS	Antidistortion
4	V_{LS}	Supply
5	MIC1	Microphone Input
6	MIC2	Microphone input
7	FAL	Antilarsen Filter
8	TC1	Antilarsen Time Constant
9	INP	Input Signal
10	LS1	Output Loudspeaker 2
11	V_{REF}	Internal Resistance
12	LS2	Output Loudspeaker 2
13	GND	Ground
14 15 16	PG0 PG1 ON/OFF	Inputs Program Level to Loudspeaker

FUNCTIONAL DESCRIPTION

TEA7531 performs the following functions :

The circuit amplifies the incoming signal and feeds it to the loudspeaker. PG0 and PG1 inputs are used to set the loudspeaker gain in a range of 32dB to 14dB in 6dB steps.

The TEA7531 inputs (PG0, PG1, ON/OFF) permit the loudspeaker to be cut-off thus ensuring privacy of communication.

- The antilarsen (antiacoustic feedback) system is incorporated.
- The maximum power available on a 50 ohms impedance loudspeaker is 25mW at 3 volts and 100mW at 5 volts.

Limit values for external components :

R3 min = 5 kohms (R3 adjust VLS).

R7 max = 390 kohms.

R6 min = R7/35.

R max between pin 5 and 6 = 10 kohms + C min = 10nf.

ELECTRICAL CHARACTERISTICS : (T_{amb} = 25°C, I_{LS} = 30mA unless otherwise specified)

Symbol	Parameter	Test Conditions			Value			Unit
					Min.	Typ.	Max.	
V_{LS1}	V_{LS} Supply	I_{LS} = 2mA (fig. 6)			2.8	3.0	3.2	V
		I_{LS} = 30mA (fig. 6)				3.15	3.4	
V_{LSM}	V_{LS} Maximum	$I_{pin\,1}$ = 40µA (fig. 6, SO = closed)					5.5	V
V_{ADJ}	Voltage Pin 1	I_{LS} = 2mA to 30mA (fig. 6)			1.1	1.25	1.4	V
G	Loudspeaker Amplifier Gain = $\frac{V_{(10)} - V_{(12)}}{V_{(9)}}$	f = 800Hz (fig. 7) $V_{(10)} - V_{(12)}$ = 0.8V_{rms}						
		ON/OFF	PG0	PG1				
G000		GND	GND	GND	12	14	16	dB
G001		GND	GND	V_{LS}	18	20	22	dB
G010		GND	V_{LS}	GND	24	26	28	dB
G011		GND	V_{LS}	V_{LS}	30	32	34	dB
G100		V_{LS}	X	X		– 30	– 20	dB
THD	Distortion	f = 300Hz to 2kHz $V_{(10)} - V_{(12)}$ = 0.8Vrms G = G011 ; (fig. 7)					2	%
Z_{MICIN}	Microphone Input	Symetrical at (pins 5-6) fig. 8				4.5		kΩ
		Asymetrical at (pin 6) fig. 8			28.5	36.0	43.5	kΩ
Z_{INPIN}	Earphone Input	(fig. 8)			2.2	2.8	3.4	kΩ
V_{OFFS}	Ouput Offset $[V_{(10)} - V_{(12)}]$	G011 ; (fig. 7)			– 50		50	mV
$I_{ON/OFF}$	Input Current ON State	V_{PGI} = 0V ; (fig. 7)			– 10	– 5		µA
I_{PG0}					– 10	– 5		
I_{PG1}					– 10	– 5		
$I_{ON/OFF}$	Input Current OFF State	$V_{PGI} = V_{LS}$; (fig. 7)					1	µA
I_{PG0}							1	
I_{PG1}							1	
$V_{IL\ ON/OFF}$	Input Voltage ON State						0.45	V
$V_{IL\ PG0}$							0.45	V
$V_{IL\ PG1}$							0.45	V
$V_{IH\ ON/OFF}$	Input Voltage OFF State				1.5			V
$V_{IH\ PG0}$					1.5			V
$V_{IH\ PG1}$					1.5			V
G_{MIC}	Microphone Gain = $V_{(7)}/[V_{(5)} - V_{(6)}]$	V_{MIC} = 10m Vrms f = 2kHz ; (fig. 9)			21.5	23.0	24.5	dB
V_8	Voltage Pin 8				0.48	0.67	0.90	V
G_{ATT}	Loudspeaker Attenuated Gain = $[V_{(10)} - V_{(12)}]/V_{(9)}$	G011 ; $V_{(8)}$ = 0.6V ; (fig. 9)				– 30	– 20	dB
		G011 ; $V_{(8)}$ = 0.4V ; (fig. 9)			20	30		dB

Figure 1 : Loudspeaker Gain versus Voltage on Pin(3) - (8) with Pin 2 Open.

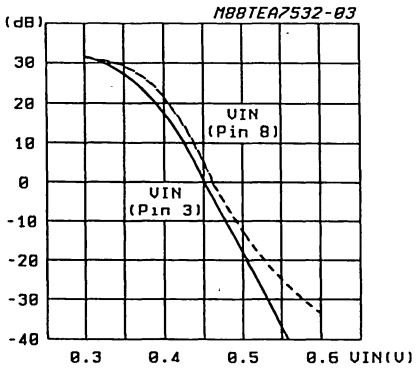


Figure 2 : AC Output Voltage versus Amplifier Gain.

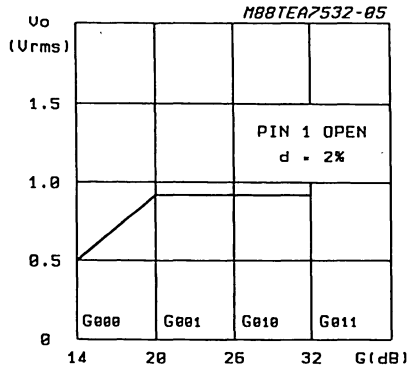


Figure 3 : Power Available on Loudspeaker versus V_{LS} Typical Curve.

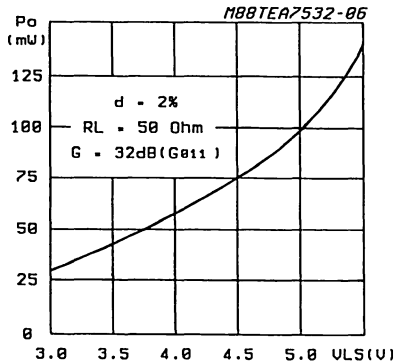


Figure 4 : Distortion versus Output Power.

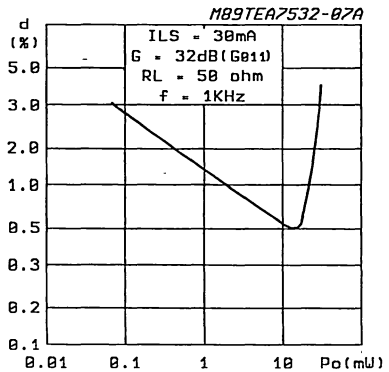
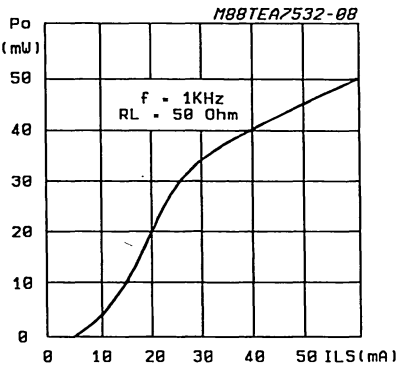
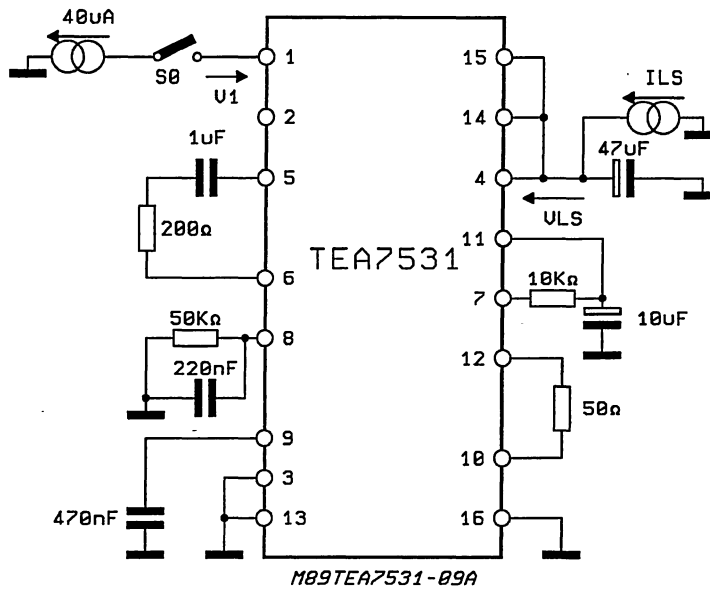


Figure 5 : Output Power versus Supply Current.



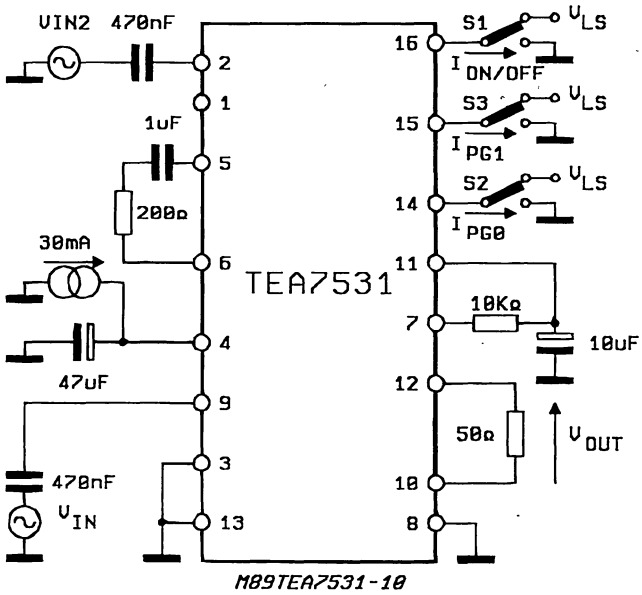
TEST CIRCUIT

Figure 6 : Shuntvoltage Regulator/Reference Voltage at Pin 1.



Note : S0 open for VLS 1.
S0 close for VLSM.

Figure 7 : Loudspeaker Amplifier : Gain/Distortion/Output Offset.

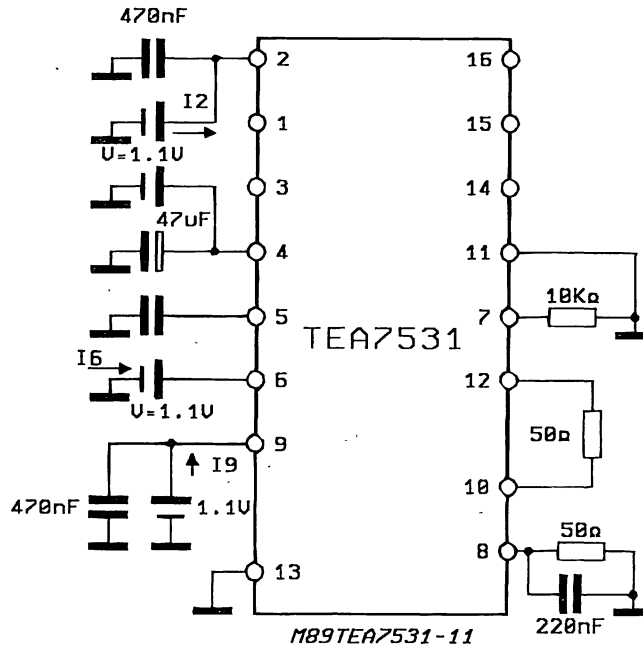


	S1	S2	S3
G1XX	1	X	X
G000	0	0	0
G010	0	1	0
G001	0	0	1
G011	0	1	1

- $G = \frac{V(10) - V(12)}{V(9)} = \frac{V_{out}}{V(9)}$
- V_{OFFS} with Vin = 0

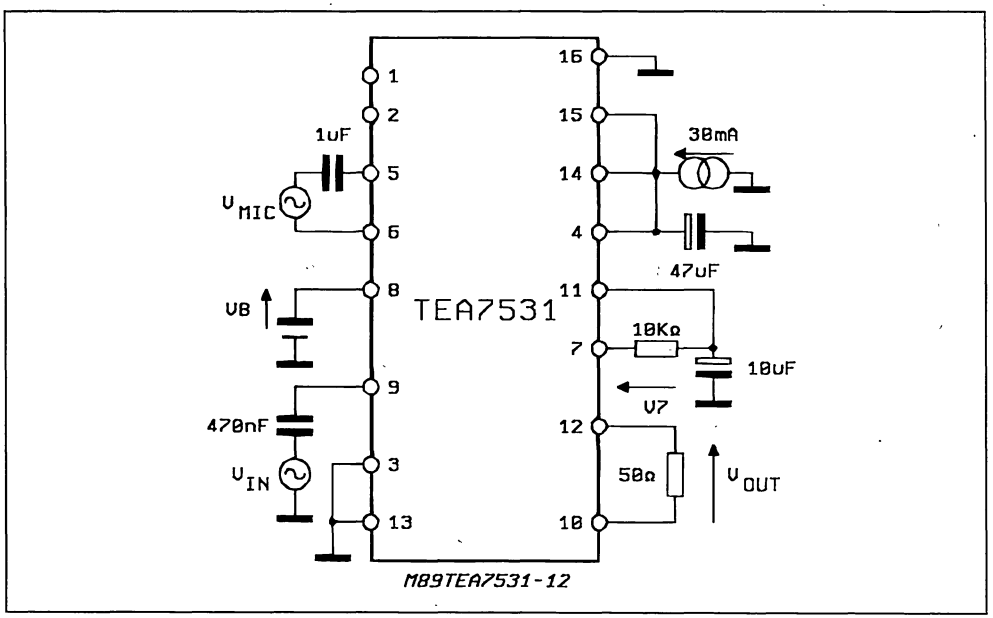
S_1 : $V_{LS} = 1$
$G_{ND} = 0$

Figure 8 : Impedance ZMIC, ZINP and Zin2.



$$Zmic = \frac{1.1V}{16} \quad ; Zinp = \frac{1.1V}{19} \quad ; Zin2 = \frac{1.1V}{12}$$

Figure 9 : Antiacoustic Feedback System at G011.



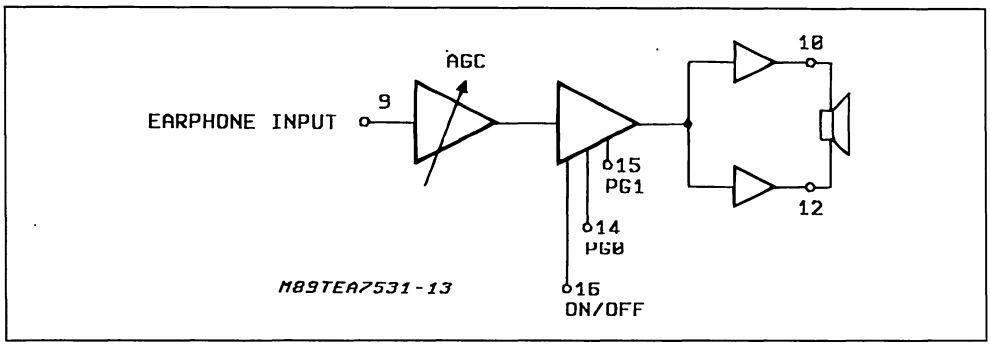
CIRCUIT DESCRIPTION

TEA7531 is a 16 pin DIL integrated circuit providing the following facilities :

- Loudspeaker amplifier.
- Antiacoustic feed-back system (antilarsen system).

1.1. LOUDSPEAKER AMPLIFIER.

Figure 10.



The amplifier is divided into 3 main sections.

- Automatic Gain Control (AGC)
- Preamplifier
- Push-pull amplifier (bridge structure)

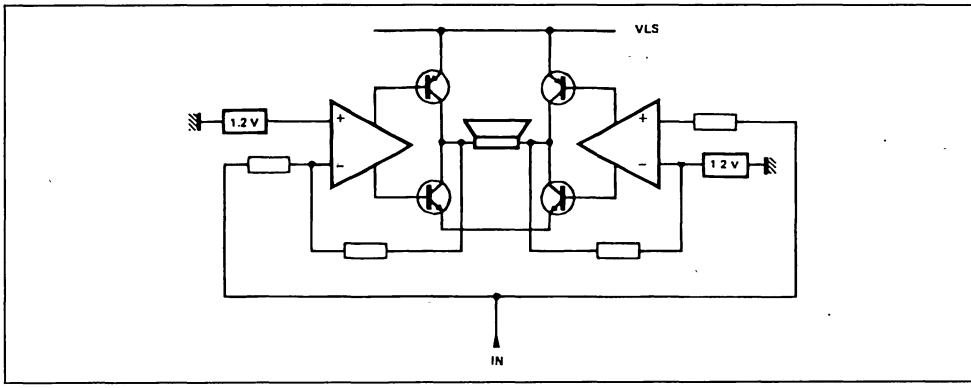
a) The AGC section is used for the antilarsen and antidistortion system.

- When used in a telephone set to avoid larsen effect the AGC automatically decreases loudspeaker amplifier gain.
- When the required output level exceeds the capabilities of the available current, the AGC decreases the loudspeaker amplifier gain to avoid distortion.

b) The preamplifier permits step control of amplifier gain in steps of 6dB, using pins PG0 and PG1, which may be controlled using switches or by a microprocessor. The amplifier may be muted using the ON/OFF control signal (pin 16).

c) The output amplifier uses a double push-pull configuration (H bridge) to get maximum dynamic range under limited supply conditions.

Figure 11.



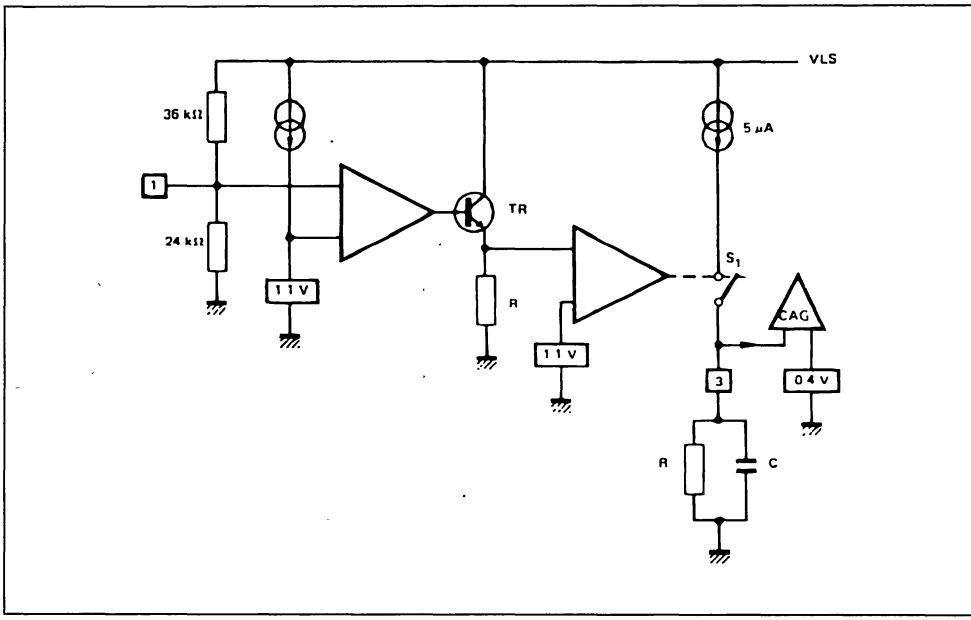
Amplifier dc supply.

In transmission mode, the supply voltage is controlled by the internal shunt DC regulator. For this reason, the TEA7531 should be supplied from a current source.

(see : supply considerations).

An antidistortion system is embodied which provides AGC control to avoid loudspeaker distortion under current-limited conditions.

Figure 12.



Circuit action.

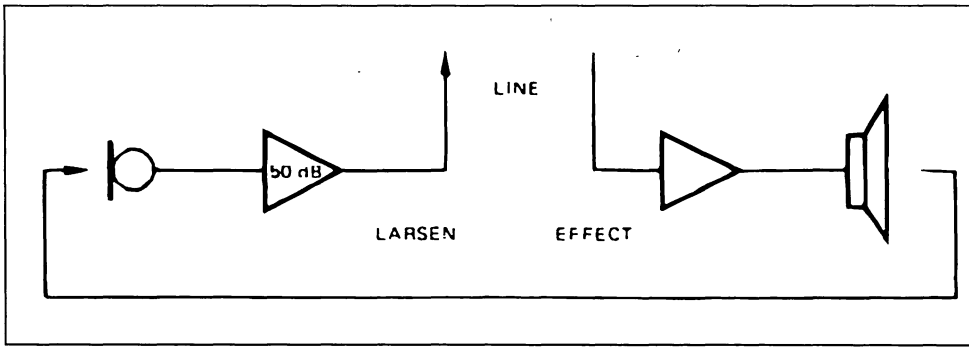
When the supply voltage is insufficient, the voltage at pin 1, falls below the reference voltage 1.1V, resulting in transistor (TR) being switched off, resulting in zero current flow in resistor R. This state enables the gain control system. Under these conditions, the shunt DC supply will switch at a rate determined by the time constant of the RC network on pin 3.

This switching action accomodates normal speech characteristics under low supply conditions.

1.2. ANTIACOUSTIC FEED-BACK SYSTEM (antilarsen system)

The purpose of this system is to control AGC action in order to avoid acoustic feed-back between the loudspeaker and the microphone, when used in a telephone set.

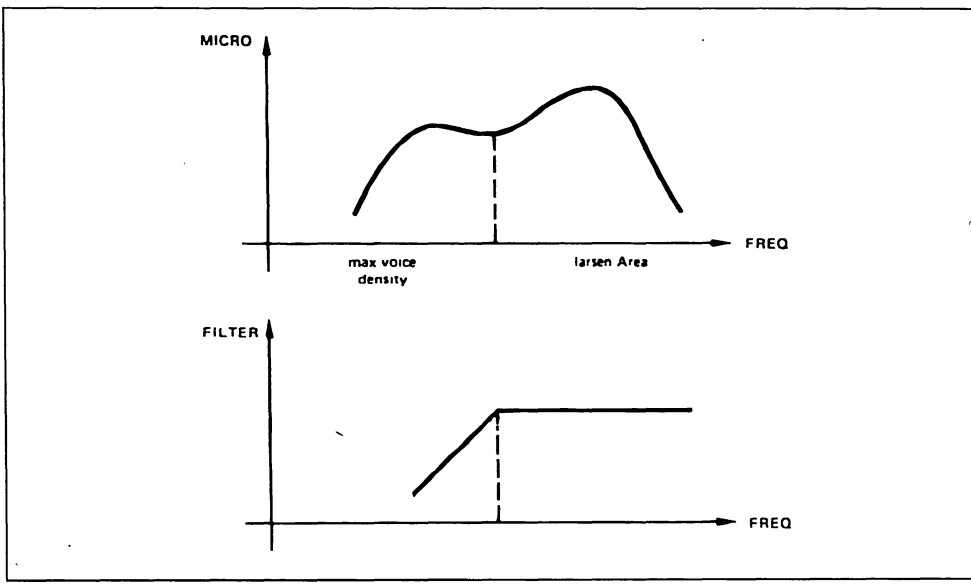
Figure 13.



Principle of operation.

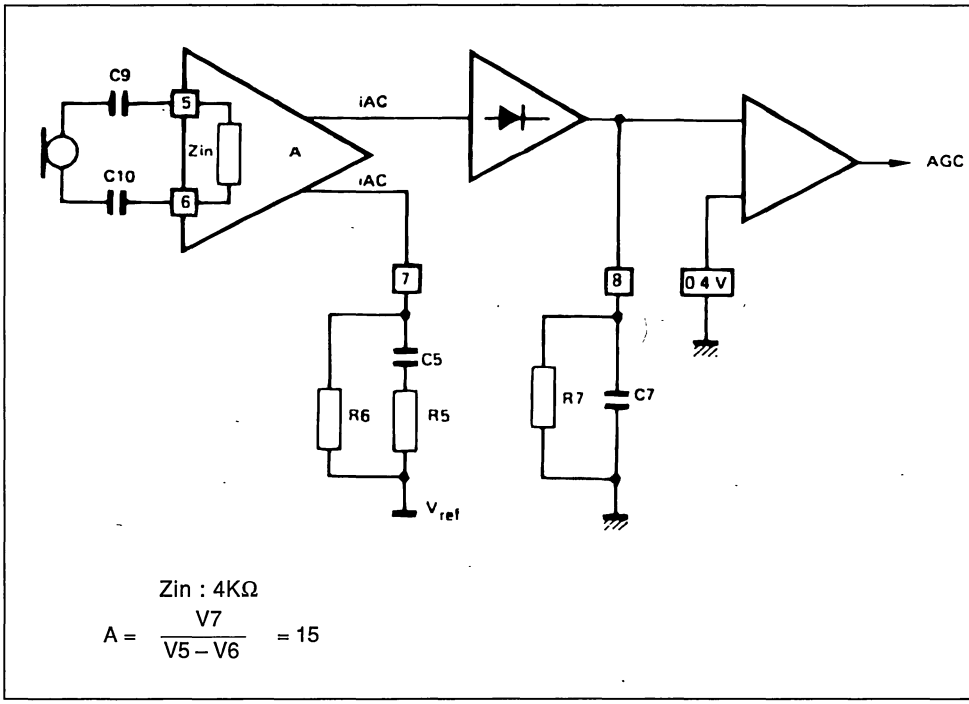
When examining the spectral density of the voice area and the larsen area, it can be seen that the dominant features of each exist in different frequency bands.

Figure 14.



To extract the larsen component, the microphone signal is first filtered by a second order filter (formed by two first order filters), then amplified and rectified in order to produce the AGC control signal.

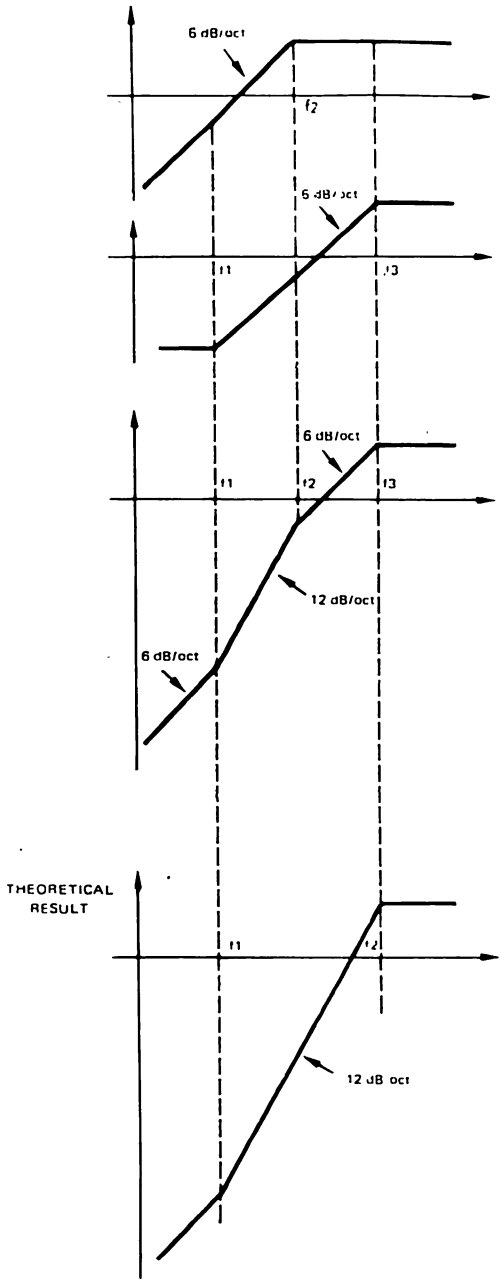
Figure 15.



$$A = \frac{Zin : 4K\Omega}{\frac{V7}{V5 - V6}} = 15$$

The first filter is generated by the capacitors on pins 5 and 6 ; the second filter by the R-C network on pin 7.

Figure 16 : Antilarsen System Filter Response.



Filter on pins 5 & 6

$$f2 = \frac{C9 + C10}{2\pi \, Zin \, C9 \, C10}$$

Filer on pin 7

$$f1 = \frac{1}{2\pi \, (R5 + R6) \, C5}$$

$$f3 = \frac{1}{2\pi \, R5 \, C5}$$

Antilarsen system
Filter response

If f2 = f3 the Antilarsen system filter is equivalent to a second order filter.

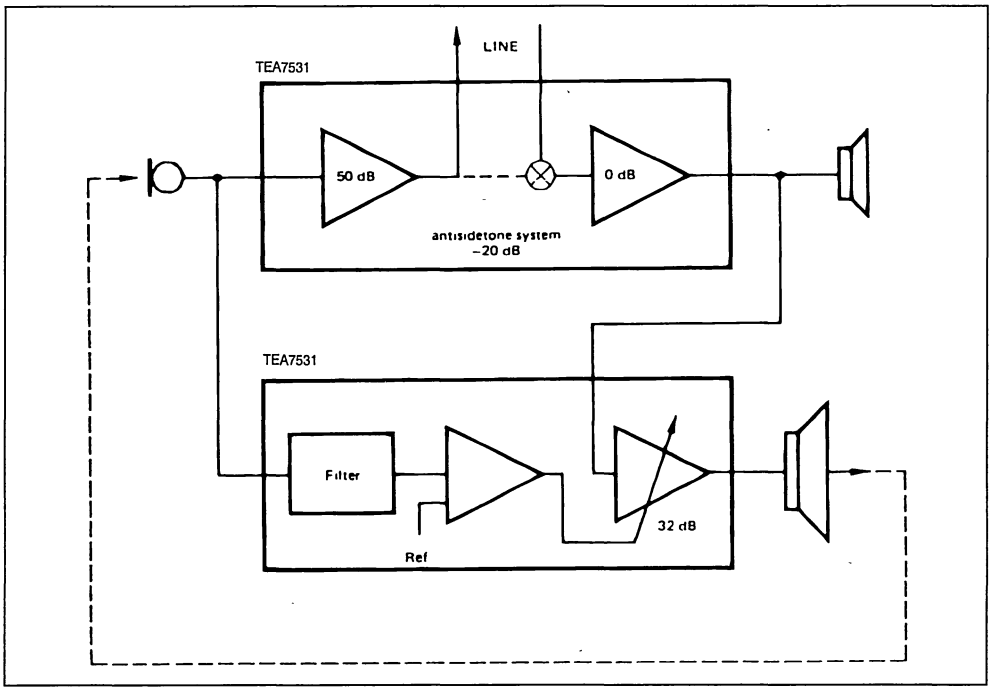
$$\frac{C9 + C10}{2\pi \, Zin \, C9 \, C10} = \frac{1}{2\pi \, R5 \, C5}$$

A complete telephone set has two antilarsen systems :

- one in the transmission circuit (for example : TEA7051) antisidetone network ;
- one in the loudspeaker amplifier (for example : TEA7531).

Together these form a high efficiency antilarsen system.

Figure 17.



PIN FUNCTIONS

PIN 1 : ADJUST VLS

This pin is used to adjust the IC supply voltage.

PINS 2-13 Ground :

These pins have to be connected together.

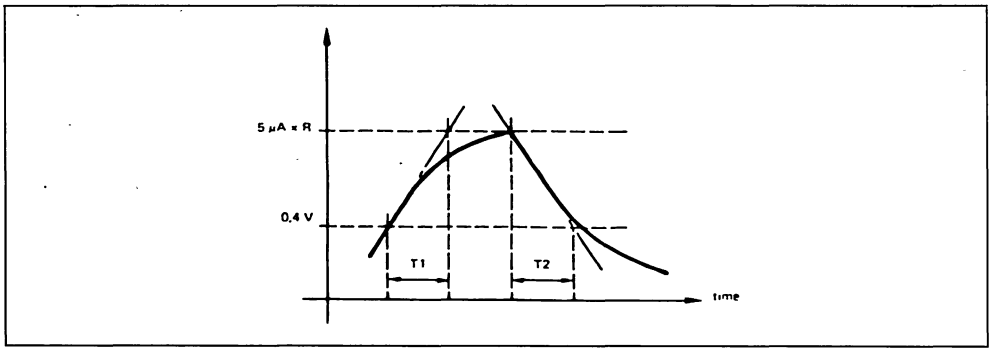
PIN 3 : AUTOMATIC GAIN CONTROL FILTER

The antidistortion system response is adjusted by the R-C network on this pin.

The AGC will be switched ON when the level on pin 3 is greater than the reference voltage (0.4V), the RC-network charges (current source ON) or discharges (current source OFF) according to the supply voltage.

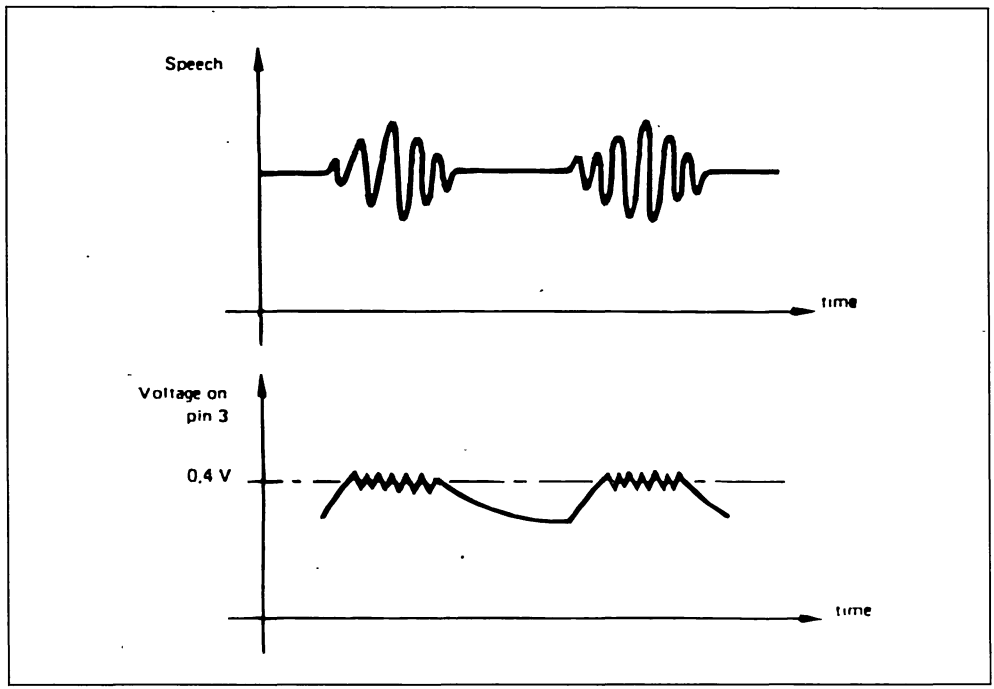
THEORETICAL VOLTAGE ON PIN 3

Figure 18.



- The value of R affects the system time constant and the charge/discharge duty cycle.
- The value of C only affects the system time constant.
- R should be greater or equal than 150kΩ for correct AGC operation.

Figure 19.



PIN 4 : CIRCUIT SUPPLY VOLTAGE
With pin 1 open circuit, VLS is internally stabilized at 2.8V.

When the TEA7531 is under AGC control, the voltage on this pin varies slightly (due to AGC action).

PIN 5/6 : MICROPHONE INPUTS

These are used for antilarsen control.

PIN 7 : ANTILARSEN FILTER 1

The second filter of the antilarsen system (1 st filter : pins 5-6) is formed by the RC network R5C5. In order to obtain a second order filter for the antilarsen system, the cut-off frequency defined at this pin, should be the same as that chosen for the first filter.

For correct TEA7531 operation R6 and R5 should be fixed at 10kΩ and 1kΩ respectively.

PIN 8 : ANTILARSEN FILTER 2

The gain and the response of the antilarsen system can be adjusted respectively by the resistor and the capacitor on this pin, according to the acoustic characteristics of the telephone set.

The value of the resistor should not exceed 390kΩ. When the voltage on this pin exceeds the threshold voltage of 0.4V, the AGC system is enabled.

PIN 9 : EARPHONE INPUT

Input for loudspeaker signal.

PIN 10-12 : LOUDSPEAKER OUTPUTS

Maximum output voltage : $V_{pp} = 2\ V_{LS} - 2.5V$ (with a gain of 32dB).

Maximum output current : depending of the supply current.

Two loudspeaker connection methods are possible, using the amplifier in either "H" mode or "B" mode.

Note : It is advisable to connect a 47nF capacitor in parallel with the loudspeaker (between pins 10 and 12).

- **"H" Mode**

This is for low voltage working, but at a higher supply current. The highest output power is available in this mode, due to the 5.5V maximum supply voltage restriction, imposed by the TEA7531.

Loudspeaker impedance recommended value : 50Ω.

Maximum gain available between earphone input and loudspeaker output : 32dB.

- **"B" Mode**

This allows higher voltage operation, but at a lower supply current.

Loudspeaker impedance recommended value : 25Ω.

Maximum gain available between earphone input and loudspeaker output : 32 – 6 = 26dB.

PIN 11 : Vref : INTERNAL REFERENCE

Output which provides an internally regulated reference voltage.

$V_{ref} = 1.1V$ typical

MAXIMUM AVAILABLE CURRENT : 5µA.

Figure 20.

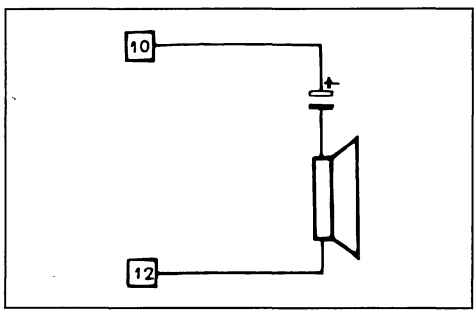
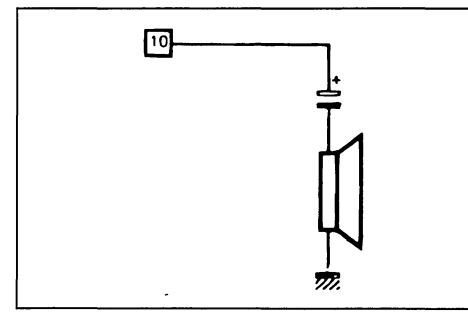
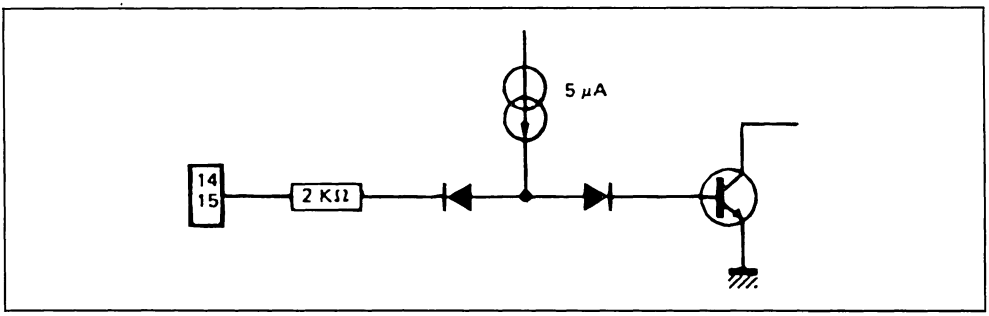


Figure 21.



PIN 14-15 : GAIN ADJUSTMENT INPUTS

Figure 22.



PIN 16 : LOUDSPEAKER MUTING.

PG0	PG1	
1	1	Gmax
1	0	Gmax - 6dB
0	1	Gmax - 12dB
0	0	Gmax - 18dB

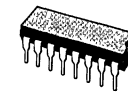
These pins are used to adjust the loudspeaker.
Pin open circuit : high level = loudspeaker muted.
Pin low level : loudspeaker enabled.
See connection of Pins 14 and 15.

SGS-THOMSON MICROELECTRONICS

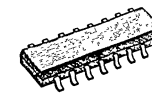
TEA7532

MONITOR AMPLIFIER

- PROGRAMMABLE GAIN IN STEPS OF 6 dB OR LINEARLY
- ON/OFF POSITION
- LOW VOLTAGE
- POWER : 100 mW AT 5 V



DIP16
(Plastic 0.25)



SO-16J

ORDER CODES : TEA7532DP (DIP16)
TEA7532FP (SO-16J)

DESCRIPTION

This 16 pins IC is designed for monitor (loudspeaker) telephone set and provides :

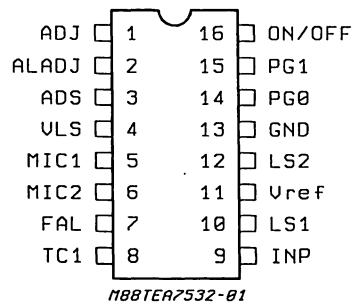
a) Signal amplification for monitoring (loudspeaker)

b) Antiacoustic feedback (antilarsen)

c) Antidistortion by automatic gain adaptation

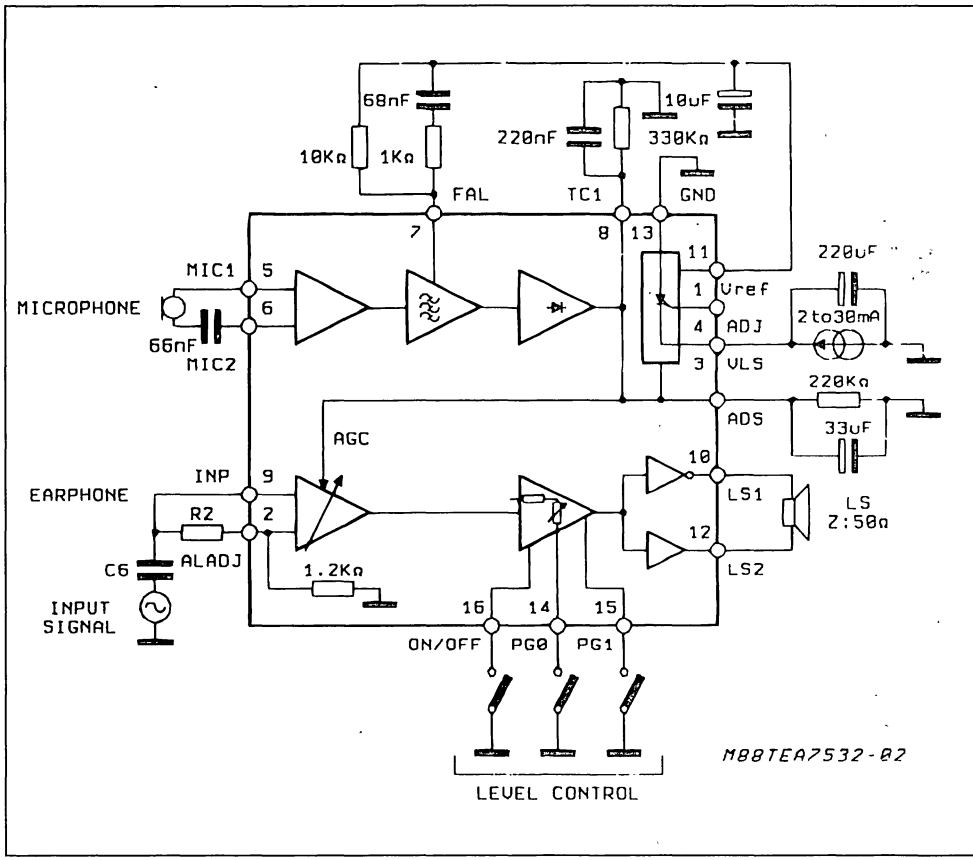
d) Antilarsen adjustment (full duplex)

PIN CONNECTION



M88TEA7532-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{op}	Temperature Range	–5 to + 45	°C
V_{LS}	Supply Voltage	6	V
I_{LS}	Supply Current for T > 300 ms for T ≤ 300 ms	90 150	mA mA
V_L	Voltage Level (pins, PG0, PG1, on/off)	0.6 > to V_S + 0.6	V

PIN DESCRIPTION

N°	Symbol	Description
1	ADJ	Adjust Internal Reference V_{LS}
2	ALADJ	Antilarsen Adjustement
3	ADS	Antidistortion
4	V_{LS}	Supply
5	MIC1	Microphone Input
6	MIC2	Microphone input
7	FAL	Antilarsen Filter
8	TC1	Antilarsen Time Constant
9	INP	Input Signal
10	LS1	Output Loudspeaker 2
11	V_{REF}	Internal Resistance
12	LS2	Output Loudspeaker 2
13	GND	Ground
14 15 16	PG0 PG1 ON/OFF	Inputs Program Level to Loudspeaker

FUNCTIONAL DESCRIPTION

TEA7532 performs the following functions :
The circuit amplifies the incoming signal and feeds it to the loudspeaker. PG0 and PG1 inputs are used to set the loudspeaker gain in a range of 32 dB to 14 dB in 6 dB steps.
The TEA7532 inputs (PG0, PG1, ON/OFF) permit the loudspeaker to be cut-off thus ensuring privacy of communication.

- The antilarsen (antiacoustic feedback) system is incorporated.
- The maximum power available on a 50 ohms impedance loudspeaker is 25 mW at 3 volts and 100 mW at 5 volts.

Limit values for external components :

R3 min = 5 kohms (R3 adjust V_{LS})

R7 max = 390 kohms

R6 min = R7/35

R max between pin 5 and 6 = 10 kohms + C min = 10 nF.

ELECTRICAL CHARACTERISTICS : (T_{amb} = 25 °C, I_{LS} = 30 mA unless otherwise Specified)

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
V_{LS1}	V_{LS} Supply	I_{LS} = 2 mA (fig. 7)			2.8	3.0	3.2	V
		I_{LS} = 30 mA (fig. 7)				3.15	3.4	
V_{LSM}	V_{LS} Maximum	$I_{pin\ 1}$ = 40 µA (fig. 7; So = closed)					5.5	V
V_{ADJ}	Voltage Pin 1	I_{LS} = 2 mA to 30 mA (fig. 7)			1.1	1.25	1.4	V
G	Loudspeaker Amplifier Gain = $\frac{V_{(10)} - V_{(12)}}{V_{(9)}}$							
		ON/OFF	PG0	PG1				
G000		GND	GND	GND	12	14	16	dB
G001		GND	GND	V_{LS}	18	20	22	dB
G010		GND	V_{LS}	GND	24	26	28	dB
G011		GND	V_{LS}	V_{LS}	30	32	34	dB
G100		V_{LS}	X	X		– 30	– 20	dB
THD	Distortion	f = 300 Hz to 2 kHz $V_{(10)} - V_{(12)}$ = 0,8 Vrms G = G011 ; (fig. 8)					2	%
G2	[V(10) – V(12)]/V2	$P_{G0} = P_{G1} = V_{LS}$; $V_{(8)}$ = 0.8 V (fig. 8)			30	32	39	dB
Z_{MICIN}	Microphone Input	Symetrical at (pins 5-6) Asymetrical at (pin 6) fig. 9			 28,5	4.5 36,0	 43,5	kΩ kΩ
Z_{INPIN}	Earphone Input	(fig. 9)			2.2	2.8	3.4	kΩ
Z_{IN2}	Antilarsen Adjustment Input				1	1.2	1.45	kΩ
V_{OFFS}	Ouput Offset $[V_{(10)} - V_{(12)}]$	G011 ; (fig. 8)			– 50		50	mV
$I_{ON/OFF}$ I_{PG0} I_{PG1}	Input Current ON State	V_{PG1} = 0 V ; (fig. 8)			– 10 – 10 – 10	– 5 – 5 – 5		µA
$I_{ON/OFF}$ I_{PG0} I_{PG1}	Input Current OFF State	$V_{PG1} = V_{LS}$; (fig. 8)					1 1 1	µA
$V_{IL\ ON/OFF}$ $V_{IL\ PG0}$ $V_{IL\ PG1}$	Input Voltage ON State						0.45 0.45 0.45	V V V
$V_{IH\ ON/OFF}$ $V_{IH\ PG0}$ $V_{IH\ PG1}$	Input Voltage OFF State				1.5 1.5 1.5			V V V
G_{MIC}	Microphone Gain = $V_{(7)}/[V_{(5)} - V_{(6)}]$	V_{MIC} = 10 m Vrms f = 2 kHz ; (fig. 10)			21,5	23.5	24.5	dB
Vg	Voltage Pin 8				0.48	0.67	0.90	V
G_{ATT}	Loudspeaker Attenuated Gain = $[V_{(10)} - V_{(12)}]/V_{(9)}$	G011 ; $V_{(8)}$ = 0.6 V ; (fig. 10)				– 30	– 20	dB
		G011 ; $V_{(8)}$ = 0.4 V ; (fig. 10)			20	30		dB

Figure 1 : Loudspeaker Gain Versus Voltage on Pin (3) - (8) with Pin 2 Open.

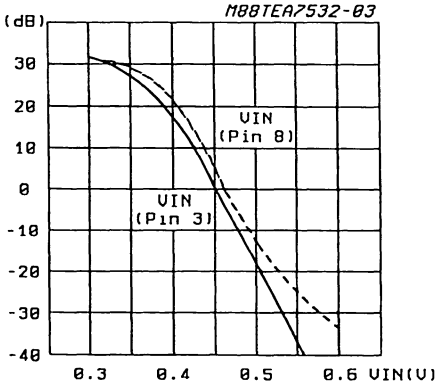
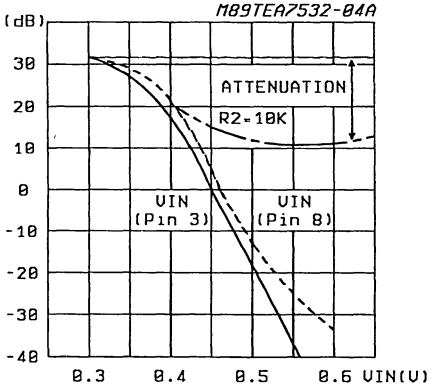


Figure 2 : Loudspeaker Gain Versus Voltage on Pin (3) - (8) and Versus R_2.



$$\text{ATTENUATION} = \frac{Zin_2\,(1.2\,K)}{Zin_2\,(1.2\,K) + R_2\,(E\,X\,T)}$$

$R_2 = 10\,K \Rightarrow ATT = 20\,dB$
$R_2 = 3\ K \Rightarrow ATT \approx 10\,dB$

Figure 3 : AC Output Voltage Versus Amplifier Gain.

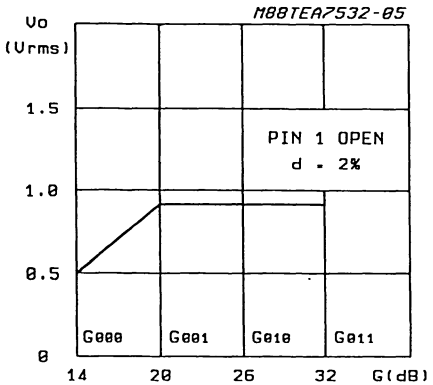


Figure 4 : Power Available on Loudspeaker Versus V_{LS} Typical Curve.

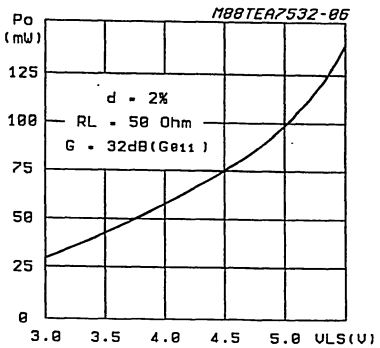


Figure 5 : Distortion Versus Output Power.

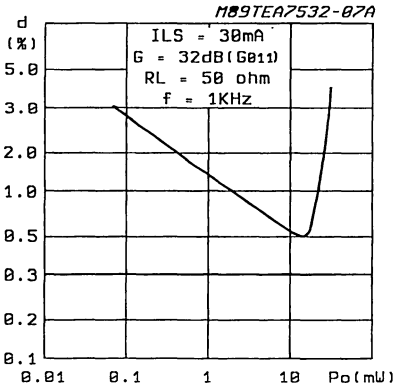
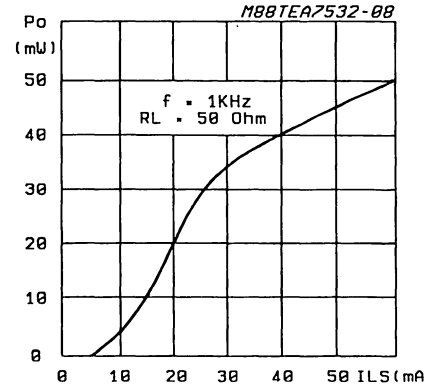
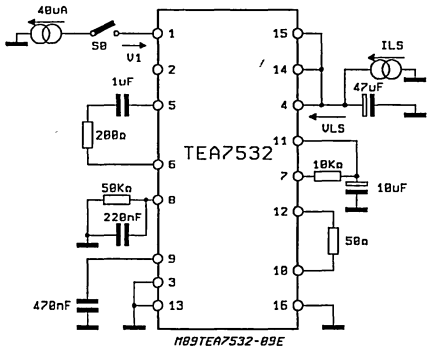


Figure 6 : Output Power Versus Supply Current.



TEST CIRCUITS

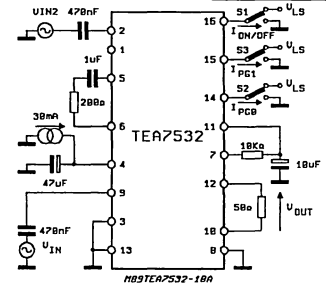
Figure 7 : Shuntvoltage Regulator/ Reference Voltage at Pin 1.



Note : S0 open for VLS 1
S0 close for VLSM.

Figure 8 : Loudspeaker Amplifier : Gain/Distortion/Output Offset.

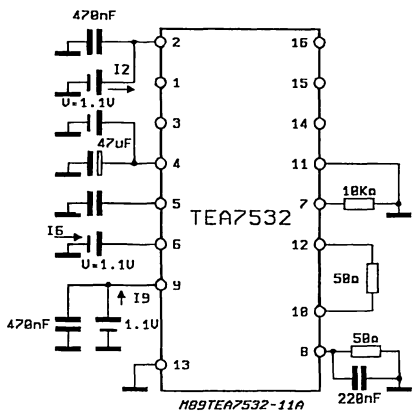
	S1	S2	S3
G1XX	1	X	X
G000	0	0	0
G010	0	1	0
G001	0	0	1
G011	0	1	1



- $G = \frac{V(10) - V(12)}{V(9)} = \frac{Vout}{V(9)}$
- VOFFS with Vin = 0.

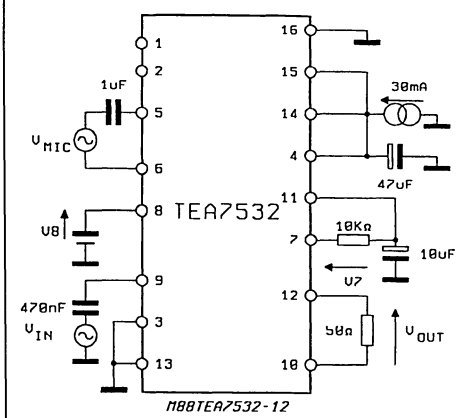
$V_{LS} = 1$
$G_{ND} = 0$

Figure 9 : Impedance ZMIC, ZINP and Zin2.



$$Zmic = \frac{1.1\ V}{I6} \quad ; Zinp = \frac{1.1\ V}{I9} \quad ; Zin2 = \frac{1.1\ V}{I2}$$

Figure 10 : Antiacoustic Feedback System at G011.



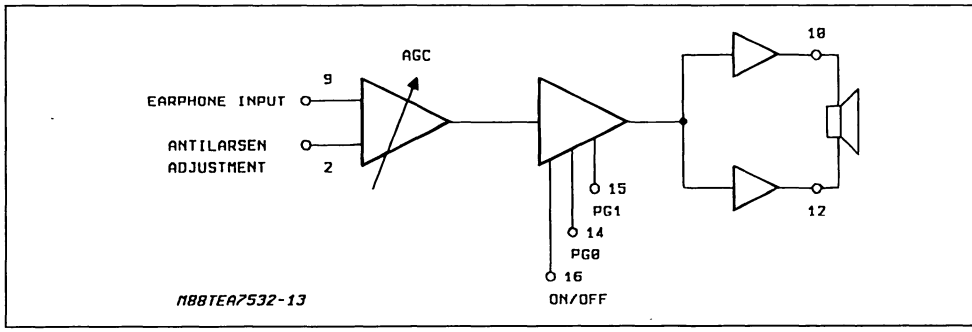
CIRCUIT DESCRIPTION

TEA7532 is a 16 pin DIL integrated circuit providing the following facilities :

- Loudspeaker amplifier
- Antiacoustic feed-back system (antilarsen system)

1.1. LOUDSPEAKER AMPLIFIER

Figure 11.



The amplifier is divided into 3 main sections.

- Automatic Gain Control (AGC)
- Preamplifier
- Push-pull amplifier (bridge structure)

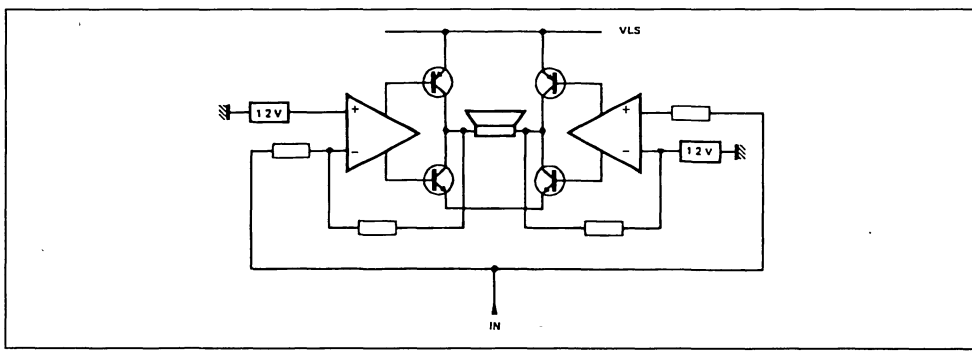
a) The AGC section is used for the antilarsen and antidistortion system.

- When used in a telephone set to avoid larsen effect the AGC automatically decreases loudspeaker amplifier gain.
- When the required output level exceeds the capabilities of the available current, the AGC decreases the loudspeaker amplifier gain to avoid distortion.

b) The preamplifier permits step control of amplifier gain in steps of 6 dB, using pins PG0 and PG1, which may be controlled using switches or by a microprocessor. The amplifier may be muted using the ON/OFF control signal (pin 16).

c) The output amplifier uses a double push-pull configuration (H bridge) to get maximum dynamic range under limited supply conditions.

Figure 12.

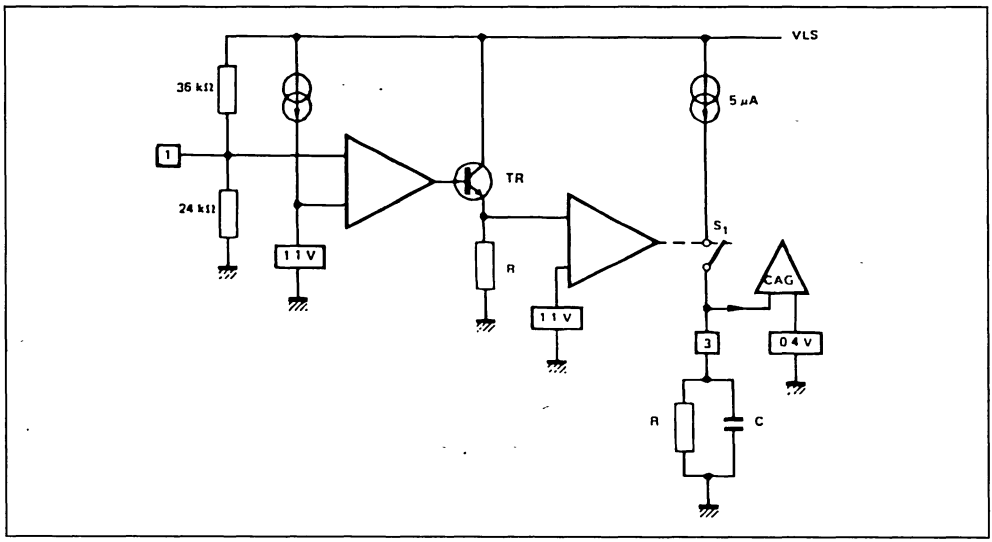


Amplifier dc supply.

In transmission mode, the supply voltage is controlled by the internal shunt DC regulator. For this reason, the TEA7532 should be supplied from a current source (see : supply considerations).

An antidistortion system is embodied which provides AGC control to avoid loudspeaker distortion under current-limited conditions.

Figure 13.



Circuit action.

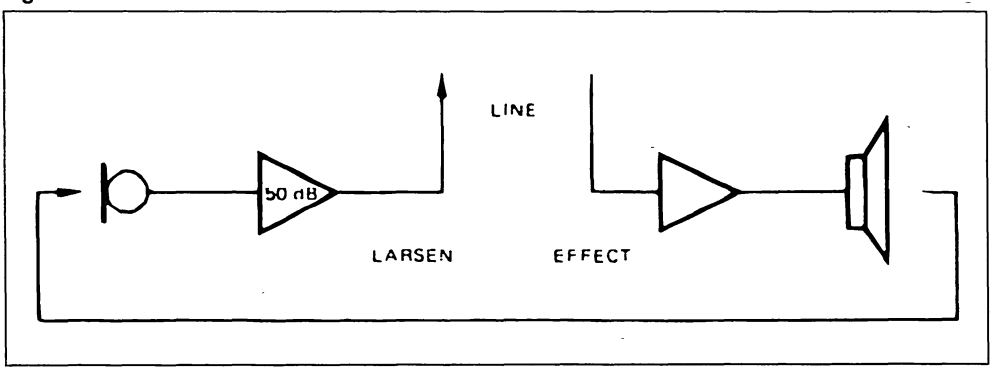
When the supply voltage is insufficient, the voltage at pin 1, falls below the reference voltage 1.1 V, resulting in transistor (TR) being switched off, resulting in zero current flow in resistor R. This state enables the gain control system. Under these conditions, the shunt DC supply will switch at a rate determined by the time constant of the RC network on pin 3.

This switching action accomodates normal speech characteristics under low supply conditions.

1.2. ANTIACOUSTIC FEED-BACK SYSTEM (ANTILARSEN SYSTEM)

The purpose of this system is to control AGC action in order to avoid acoustic feed-back between the loudspeaker and the microphone, when used in a telephone set.

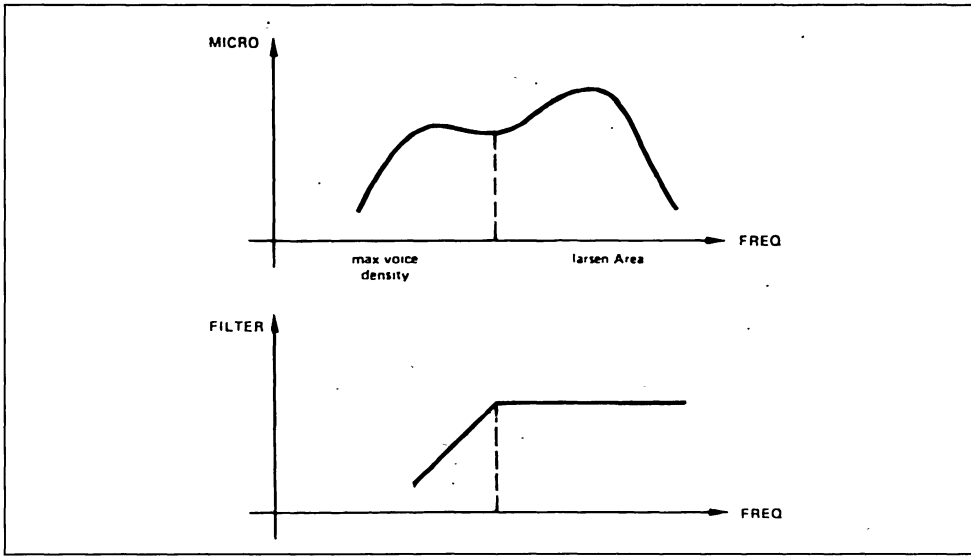
Figure 14 .



Principle of operation.

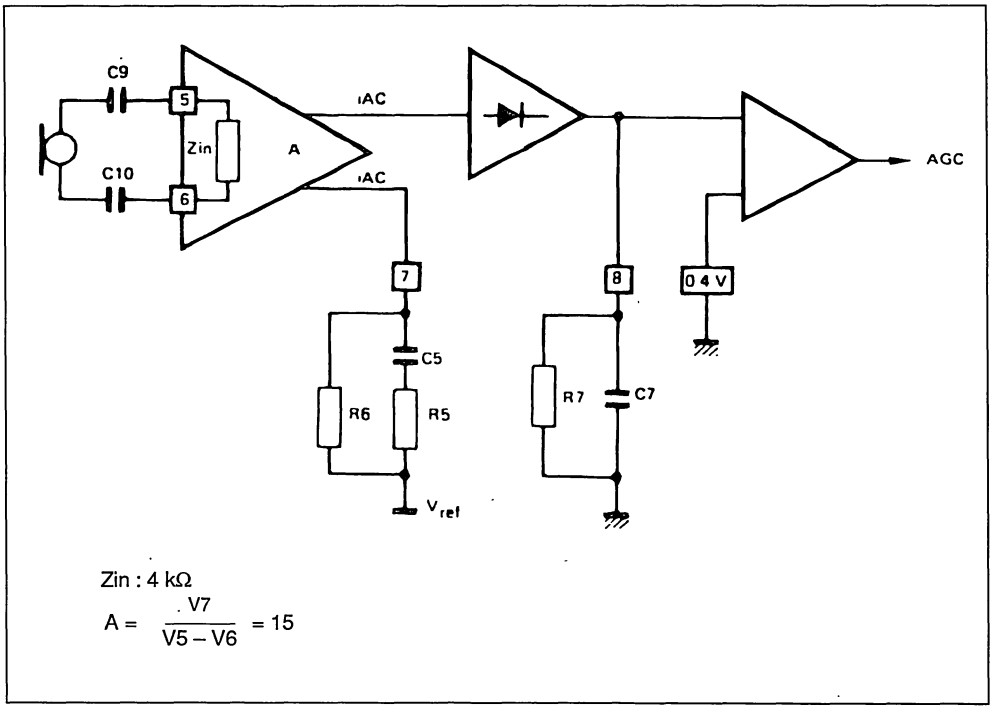
When examining the spectral density of the voice area and the larsen area, it can be seen that the dominant features of each exist in different frequency bands.

Figure 15.



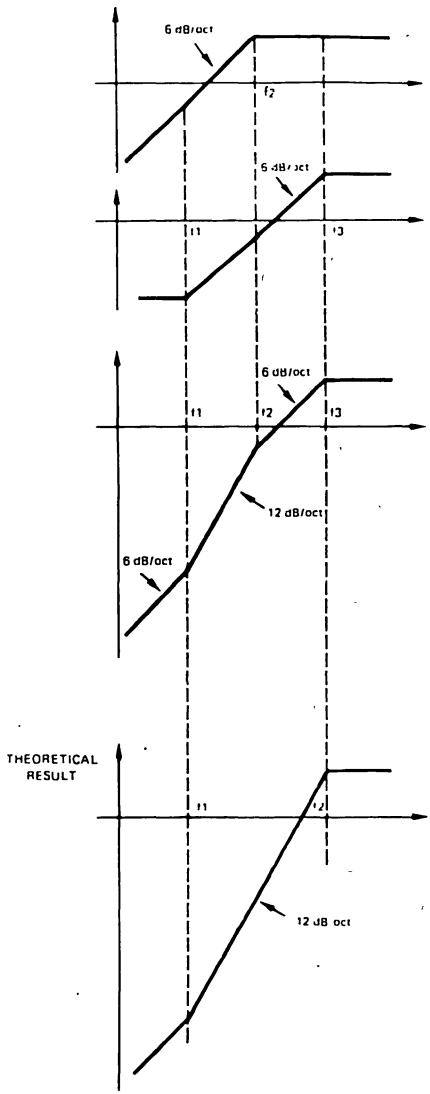
To extract the larsen component, the microphone signal is first filtered by a second order filter (formed by two first order filters), then amplified and rectified in order to produce the AGC control signal.

Figure 16.



The first filter is generated by the capacitors on pins 5 and 6 ; the second filter by the R-C network on pin 7.

Figure 17 : Antilarsen System Filter Response.



Filter on pins 5 & 6

$$f2 = \frac{C9 + C10}{2\pi \, Zin \, C9 \, C10}$$

Filter on pin 7

$$f1 = \frac{1}{2\pi \, (R5 + R6) \, C5}$$

$$f3 = \frac{1}{2\pi \, R5 \, C5}$$

Antilarsen system
Filter response

If f2 = f3 the Antilarsen system filter is equivalent to a second order filter.

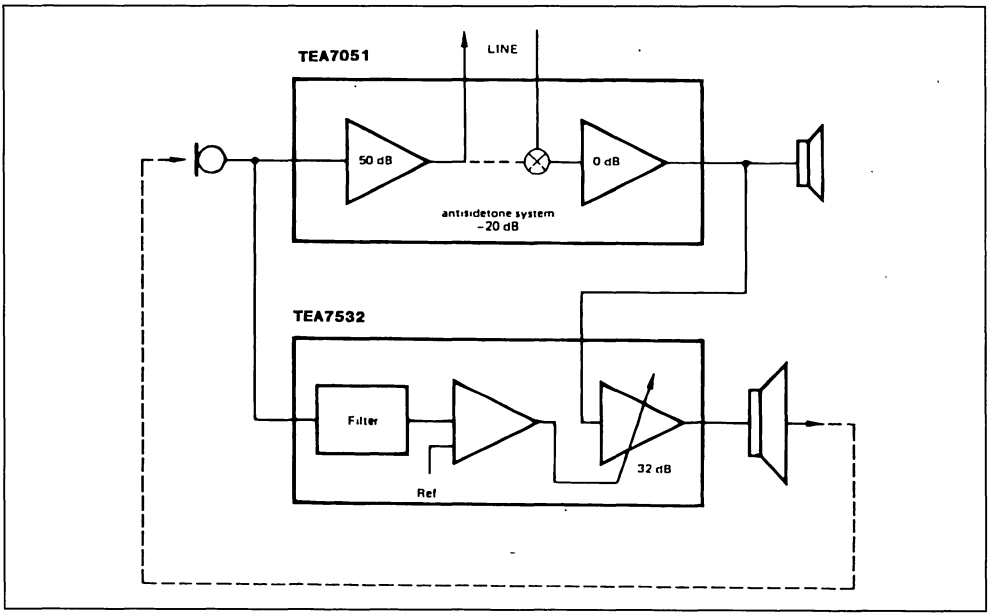
$$\frac{C9 + C10}{2\pi \, Zin \, C9 \, C10} = \frac{1}{2\pi \, R5 \, C5}$$

A complete telephone set has two antilarsen systems :

- one in the transmission circuit (for example : TEA7051) antisidetone network ;
- one in the loudspeaker amplifier (for example : TEA7532).

Together these form a high efficiency antilarsen system.

Figure 18.



PIN FUNCTIONS

PIN 1 : ADJUST V_{LS}

This pin is used to adjust the IC supply voltage.

PIN 2 : ANTILARSEN ADJUSTMENT

The AC signal at this pin is amplified to the loudspeaker without AGC attenuation.

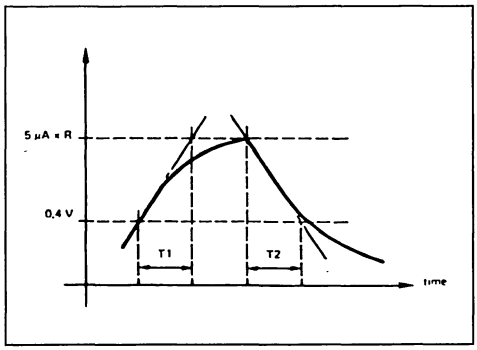
PIN 3 : AUTOMATIC GAIN CONTROL FILTER

The antidistortion system response is adjusted by the R-C network on this pin.

The AGC will be switched ON when the level on pin 3 is greater than the reference voltage (0.4 V), the RC-network charges (current source ON) or discharges (current source OFF) according to the supply voltage.

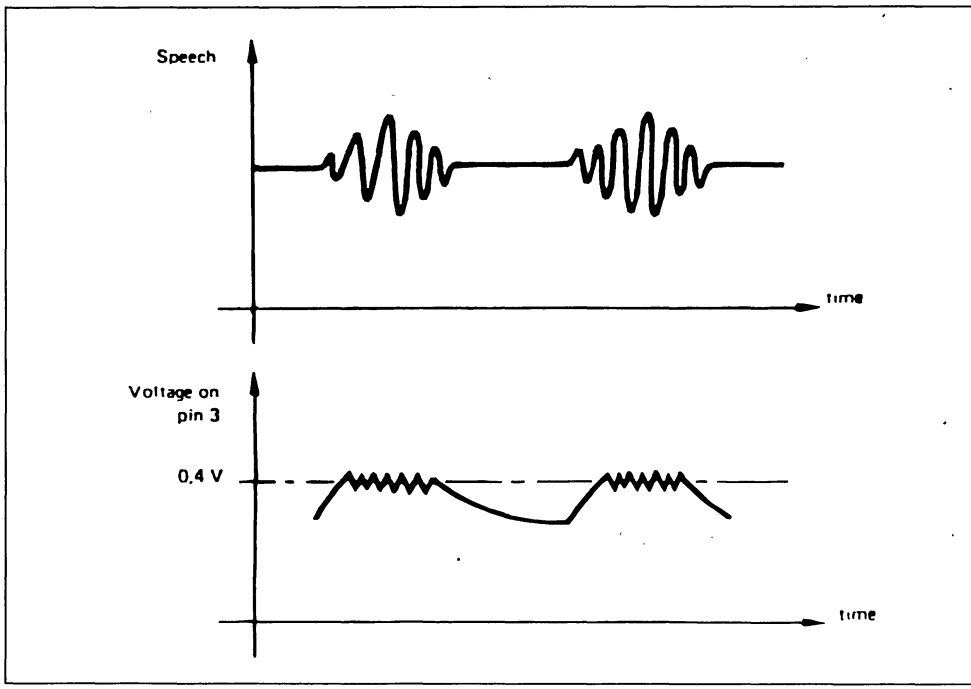
THEORETICAL VOLTAGE ON PIN 3

Figure 19 :



- The value of R affects the system time constant and the charge/discharge duty cycle.
- The value of C only affects the system time constant.
- R should be greater or equal than 150 kΩ for correct AGC operation.

Figure 20.



PIN 4 : CIRCUIT SUPPLY VOLTAGE
With pin 1 open circuit, VLS is internally stabilized at 2.8 V.

When the TEA7532 is under AGC control, the voltage on this pin varies slightly (due to AGC action).

PIN 5/6 : MICROPHONE INPUTS

These are used for antilarsen control.

PIN 7 : ANTILARSEN FILTER 1

The second filter of the antilarsen system (1 st filter : pins 5-6) is formed by the RC network R5C5.
In order to obtain a second order filter for the antilarsen system, the cut-off frequency defined at this pin, should be the same as that chosen for the first filter.

For correct TEA7532 operation R6 and R5 should be fixed at 10 kΩ and 1 kΩ respectively.

PIN 8 : ANTILARSEN FILTER 2

The gain and the response of the antilarsen system can be adjusted respectively by the resistor and the capacitor on this pin, according to the acoustic characteristics of the telephone set.

The value of the resistor should not exceed 390 kΩ. When the voltage on this pin exceeds the threshold voltage of 0.4 V, the AGC system is enabled.

PIN 9 : EARPHONE INPUT

Input for loudspeaker signal.

PIN 10-12 : LOUDSPEAKER OUTPUTS

Maximum output voltage : $V_{pp} = 2\ V_{LS} - 2.5$ V (with a gain of 32 dB).

Maximum output current : depending of the supply current.

Two loudspeaker connection methods are possible, using the amplifier in either "H" mode or "B" mode.

Note : It is advisable to connect a 47 nF capacitor in parallel with the loudspeaker (between pins 10 and 12).

- "H" Mode

This is for low voltage working, but at a higher supply current. The highest output power is available in this mode, due to the 5.5 V maximum supply voltage restriction, imposed by the TEA7532.
Loudspeaker impedance recommended value : 50 Ω.
Maximum gain available between earphone input and loudspeaker output : 32 dB.

Figure 21.

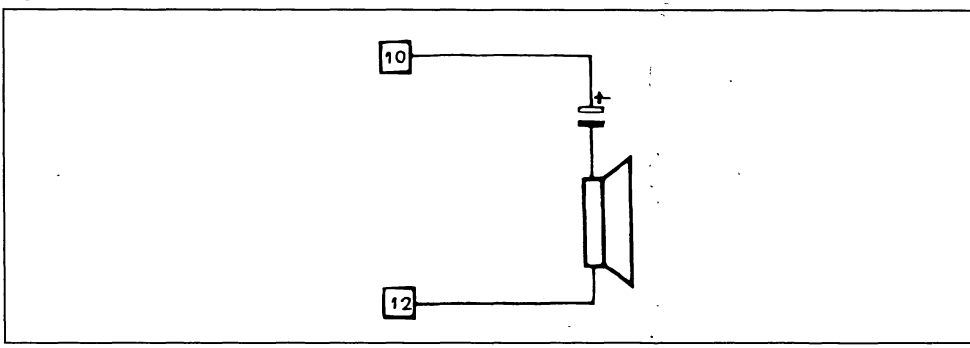
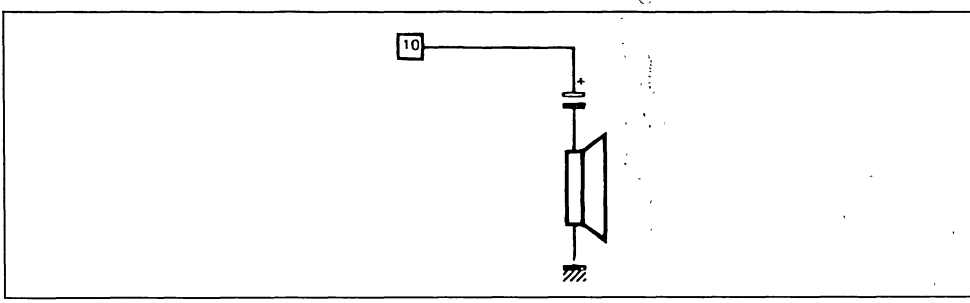


Figure 22.



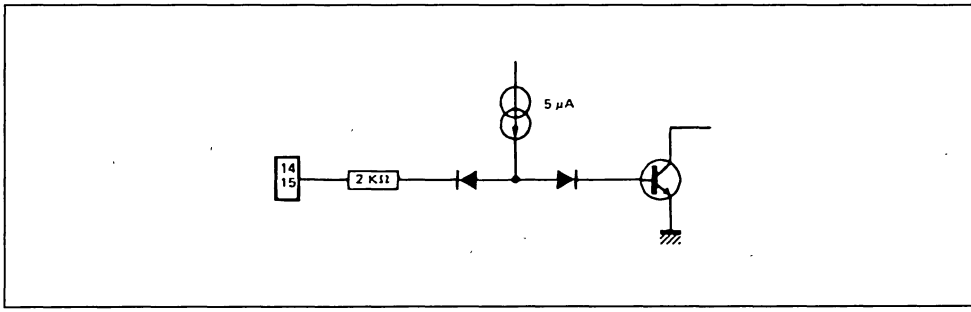
- "B" Mode
This allows higher voltage operation, but at a lower supply current.
Loudspeaker impedance recommended value : 25 Ω.
Maximum gain available between earphone input and loudspeaker output : 32 - 6 = 26 dB.

PIN 11 : Vref : INTERNAL REFERENCE
Output which provides an internally regulated reference voltage.

Vref = 1.1 V typical

MAXIMUM AVAILABLE CURRENT : 5 µA

Figure 23.



PIN 13 : GROUND

PIN 14-15 : GAIN ADJUSTMENT INPUTS

These pins are used to adjust the loudspeaker amplifier gain. Four steps of 6 dB/step are available (pin open circuit = high level).

PG0	PG1	
1	1	Gmax
1	0	Gmax - 6 dB
0	1	Gmax - 12 dB
0	0	Gmax - 18 dB

PIN 16 : LOUDSPEAKER MUTING.

This pin is used to mute the loudspeaker. Pin open-circuit : high level = loudspeaker muted.

Pin low level : louspeaker enabled (see connection of pins 14 and 15).

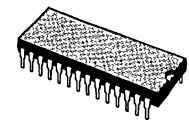
SGS-THOMSON MICROELECTRONICS

TEA7540

HANDSFREE

ADVANCE DATA

- NOISE/SPEECH DISCRIMINATION IN EMISSION AND RECEPTION
- INTEGRATED SIGNAL GAIN COMPRESSOR IN BOTH MODES
- PROGRAMMABLE ATTENUATORS IN BOTH MODES
- ADAPTED TO ACOUSTIC PARAMETERS OF ALL CABINETS
- LOW OPERATING VOLTAGE 2.5V
- LOW OPERATING CURRENT 2.1mA
- CHIP SELECT BETWEEN HANDSFREE AND MONITORING MODES



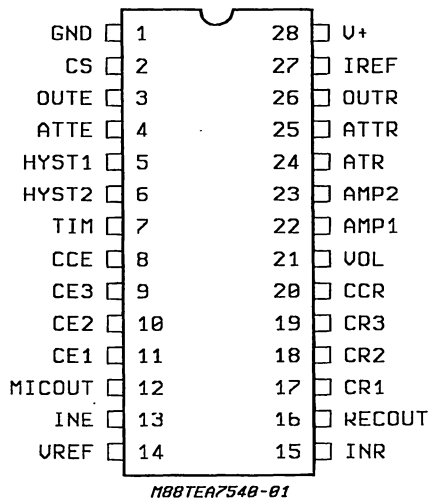
DIP28

ORDER CODE : TEA7540DP

DESCRIPTION

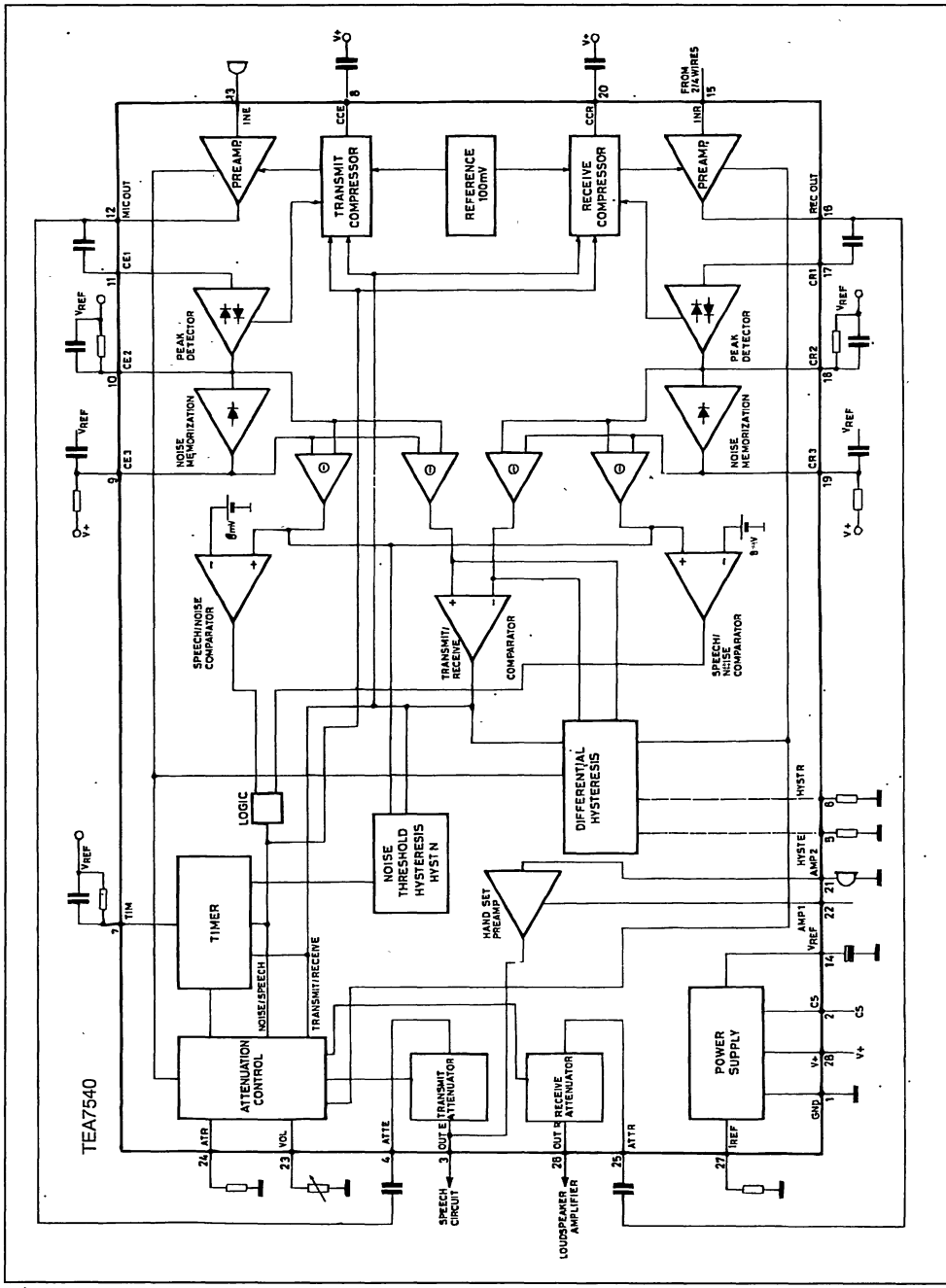
This 28 pins IC is an innovative approach to quality handsfree telephone sets. It results from an extensive research on speech signal.

PIN CONNECTION (top view)



M88TEA7540-01

BLOCK DIAGRAM



PIN FUNCTION

N°	Name	Function
1	GND	Ground
2	CS	Chip Select
3	OUTE	Transmit Attenuator Output
4	ATTE	Transmit Attenuator Input
5	HYST1	Transmit Channel Hysteresis
6	HYST2	Receive Channel Hysteresis
7	TIM	RC Timer
8	CCE	Time Constant of the Transmit Signal Compressor
9	CE3	Transmit Noise Memorisation
10	CE2	Transmit Peak Detector
11	CE1	Transmit Rectifier Input
12	MICOUT	Transmit Signal Compressor Output
13	INE	Transmit Signal Compressor Input
14	VREF	V+/2
15	INR	Receive Signal Compressor Input
16	RECOUT	Receive Signal Compressor Output
17	CR1	Receive Rectifier Input
18	CR2	Receive Peak Detector
19	CR3	Receive Noise Memorisation
20	CCR	Time Constant of the Receive Signal Compressor
21	VOL	Volume Control
22	AMP1	Handset Preamplifier Power Supply
23	AMP2	Handset Preamplifier Input
24	ATR	Attenuation Value
25	ATTR	Receive Attenuator Input
26	OUTR	Receive Attenuator Output
27	IREF	Reference Current Source
28	V+	

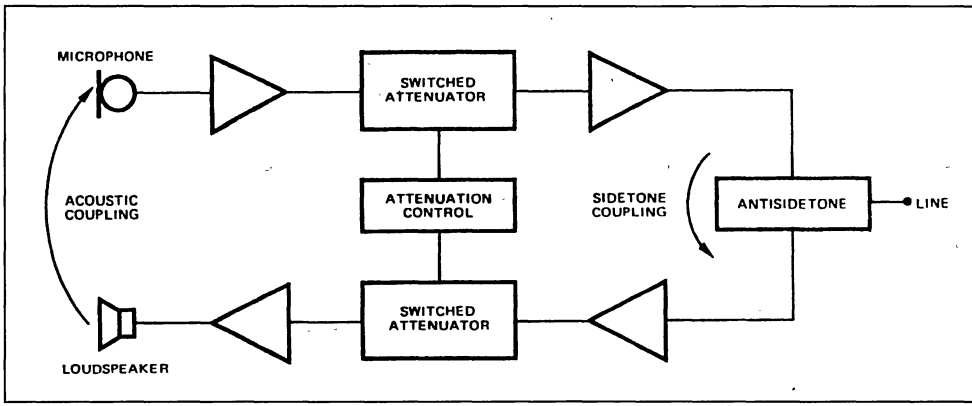
FUNCTIONAL DESCRIPTION

SWITCHED ATTENUATORS

Fig. 1 represents a block diagram of a handsfree subset with attenuators in signal mode. To prevent the system from howling, the total loop gain, including acoustic feedback through the housing and sidetone coupling, must be less than 0dB. For this purpose, two switched attenuators are inserted in each mode (emission and reception). The attenuation is shifted from one mode to the other, resulting from the speech level comparison between each way.

To prevent the circuit to switch continuously in one way, the operation of the IC must be fully symetrical in both ways. This involves signal comparison, attenuation value.

Figure 1.



GAIN COMPRESSORS

In TEA7540, two signal compressors are inserted in each mode before the signal comparison, so the signal coming from each end has the same level (100mV peak), the losses in each way (for instance losses resulting from the line lenght in receiving mode) are compensated and the signal comparison is fully symetrical. The time constant of each signal compressor is fixed by an external capacitor, but the gain of the compressor decreases 100 times more quickly than it increases to prevent from noise increasing between words. The compressing depth is 38dB.

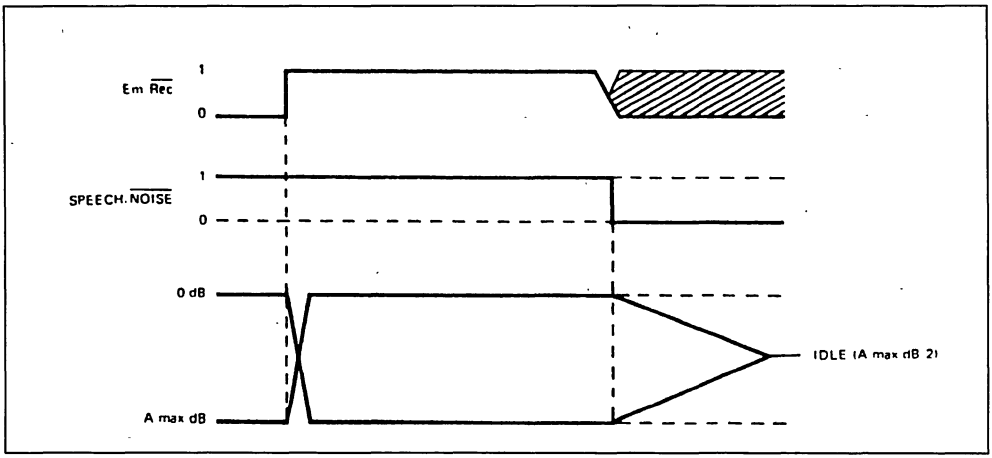
BACKGROUND NOISE DISCRIMINATION

An additional feature provided in TEA7540 is background noise level discrimination in each way. The IC stores the background sound level with a long time constant (3 to 5 seconds depending on an external RC) and compares it with the incoming signal in order to distinguish a usefull signal (speech) from the background noise. This background noise memorisation is also used to compensate the noise in each mode before signal comparison : the noise level in each mode is substracted from the incoming signal before the comparison. So a very high noise level in one mode cannot trouble the comparison between the usefull signals.

The result of the comparison manages the attenuators in the following way :

- The maximum attenuation is switched on the mode where the speech signal is the lowest. The maximum attenuation is fixed by two external resistors (maximum 52dB). The time constant of the switch is fixed by the timer via an external capacitor.
- When neither party is talking both attenuators are set to a medium attenuation. Thus each mode is in idle mode. The time constant of the switch from active mode to idle mode must be long enough to prevent from switching to idle mode between two words (see fig 2). This time constant is fixed by an external RC.

Figure 2.



TEA7540 OPERATION

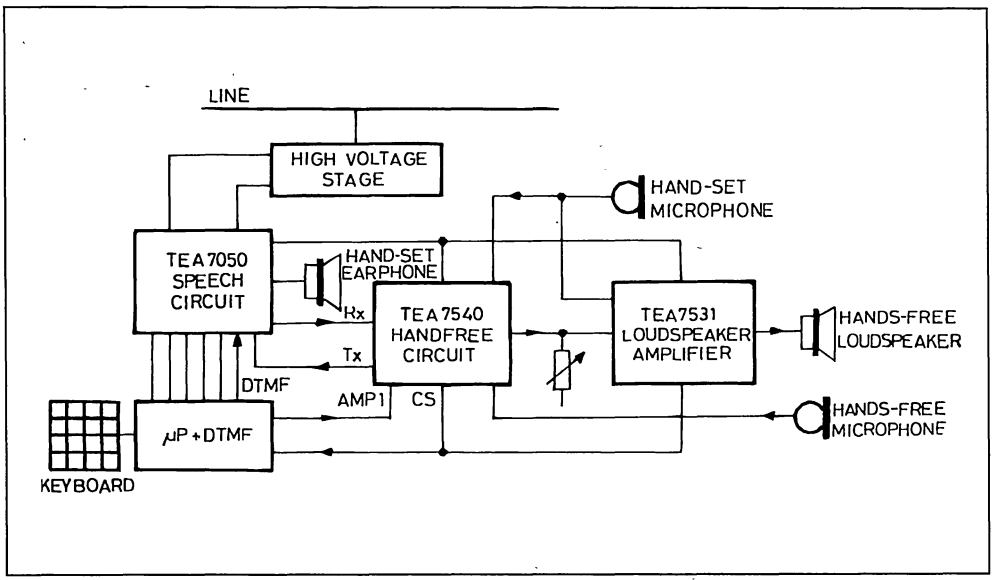
TEA7540 is powered through an external shunt regulator (for instance the shunt regulator of the monitor amplifier TEA7531) or an external zener diode. It can work at a very low voltage (2.5volts) over the circuit and it has a low current consumption (2.1mA).

It's also possible via the chip select pin (CS) to put the handsfree function in standby to use the circuit in monitoring mode with the handset microphone.

TEA7540 is designed to work with all kinds of microphones, including Electret.

TEA7540 also handles the handset microphone signal (AMP2) when the system is set to normal conversation mode (AMP1).

Figure 3 : Application Diagram.
Example of high range telephone set using TEA7540.



SPECIAL FUNCTIONS

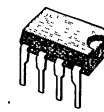
MICROPHONE AMPLIFIER

- VERY FEW EXTERNAL COMPONENTS
- BUILT IN PARTIAL BRIDGE
- HIGH IMMUNITY AGAINST EMI
- ACCURATE GAIN CONTROL
- NO CAPACITOR REQUIRED
- WIDE OPERATING VOLTAGE AND CURRENT RANGE
- PROGRAMMABLE DC CHARACTERISTICS

DESCRIPTION

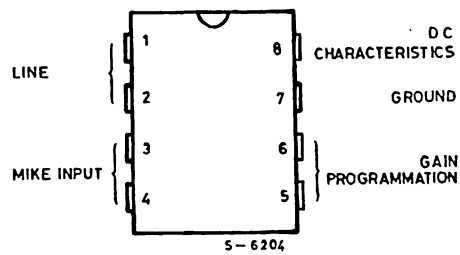
The LS188 is a monolithic microphone amplifier designed to be used with several kinds of transducers. It can replace the carbon microphone in telephones and may also be used in cassette recorder, walky talkies, or infrared receiver applications. The circuit is assembled in a 8-pin Dual in Line Package. The LS188 consists of a differential input amplifier, internal reference and a current modulator stage enabling the device to send the amplifier speech to the line.

MINIDIP

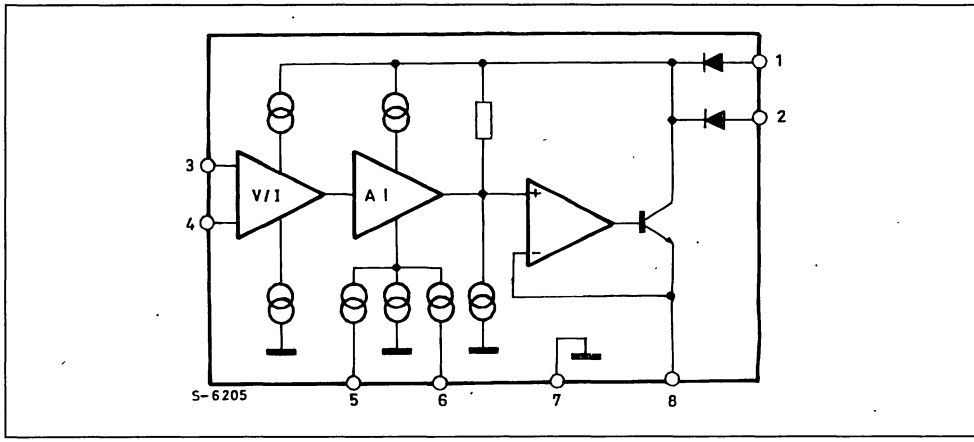


ORDER CODE : LS188CB

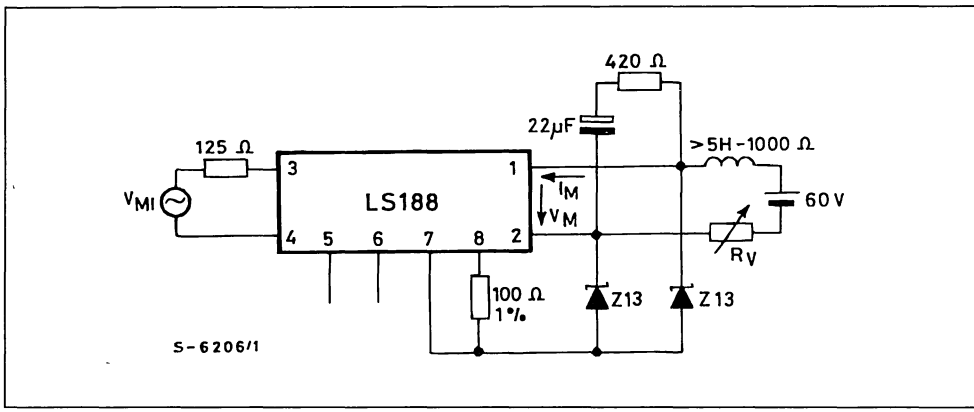
PIN CONNECTION (top view)



BLOCK DIAGRAM



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_M	Microphone Voltage (3ms duration)	20	V
I_M	Microphone Current	150	mA
P_{tot}	Power Dissipation	600	mW
T_{op}	Operating Temperature	– 30 to 70	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit at 25 °C with f = 300 Hz to 3400 Hz (pins 5-6 floating), unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_s	Sending Gain	V_{MI} = 1 mV f = 1 KHz I_M = 15 mA	39.5	40.5	41.5	dB
G	Gain Spread vs. Temperature	− 25 °C T_{amb} = + 60 °C			± 1	dB
G	Gain Spread vs. Polarity	I_M = ± 15 mA			± 0.3	dB
G	Gain Spread vs. Line Current	V_{MI} = 1 mV f = 1 KHz I_M = 7 to 60 mA I_{ref} = 15 mA			± 1	dB
V_{1-7}	Microphone Voltage	I_M = 7 mA I_M = 15 mA I_M = 40 mA		4.5	 5.9 8.65	V V V
	Differential Resistance and Output Impedance	I_M = 7 to 60 mA		120	200	Ω
	Frequency Response	I_M = 15 mA			± 1	dB
	Sending Noise	V_{MI} = 0			− 67	dBmp
	Input Impedance	I_M = 7 to 60 mA	7.3	9.75	12.2	KΩ
	Distortion	f_{ref} = 1 KHz I_M = 7 to 15 mA V_o = 0.4 V I_M = 15 to 60 mA V_o = 1.25 V			 2 7	 % %
I_q	Quiescent Current			1		mA

TYPICAL GAIN VERSUS PIN 5 - 6 CONNECTION

Pin 5	Pin 6	
	Floating	Grounded
Floating	40.5 dB	47 dB
Grounded	45.5 dB	49.5 dB

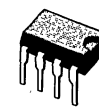
Intermediate values of G_S are obtained by right resistors from pins 5 or 6 to ground.

TRUNK INTERFACE

PRELIMINARY DATA

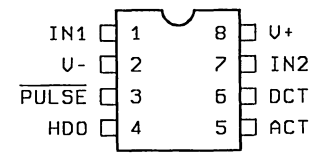
- ON CHIP POLARITY GUARD
- MEETS DC LINE CHARACTERISTICS OF EITHER CCITT AND EIA RS 464 SPECS
- PULSE FUNCTION
- HIGH AC IMPEDANCE
- OFF HOOK-STATUS DETECTION OUTPUT
- LOW EXTERNAL COMPONENT COUNT

MINIDIP



ORDER CODE : L3845

PIN CONNECTION
(top view)



M88L3845-02A

DESCRIPTION

The circuit provides DC loop termination for analog trunk lines.

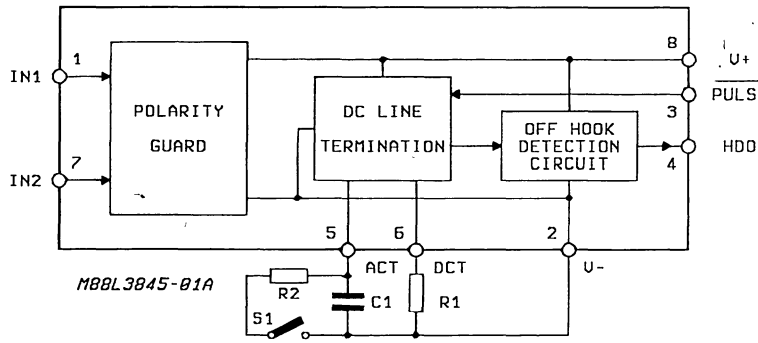
The V-I characteristics is equivalent to a fixed voltage drop (zener like characteristic) in series with an external resistance that determines the slope of the DC characteristic.

An external low voltage electrolytic capacitor causes the circuit to exhibit a very high impedance to all AC signal above a minimum frequency that is determined by the capacitor itself and by a 20 K nominal resistor integrated on the chip.

The Off-Hook status is detected all the time a typic of 8 mA is flowing into the circuit. In this condition a constant current generator is activated to supply an external device (typically an optocoupler) without affecting the AC characteristic of the circuit.

When Pulse Dialing is required the $\overline{\text{PULSE}}$ input (pin 3) connected to V- causes the device to reduce the fixed DC voltage drop and to exhibit a pure resistive impedance equal to the external resistor.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Max Line Voltage (pulse duration 10 ms max)	20	V
I_L	Max Line Current	150	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	800	mW
T_{op}	Operating Temperature	– 40 to + 70	°C
T_{srg}, T_j	Storage and Junction Temperature	– 55 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	120	°C

DC ELECTRICAL CHARACTERISTICS

(I_L = 10 mA to 100 mA, R_1 = 56 Ω, R_2 = 150 KΩ, S_1 = Open, T_{amb} = + 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_L	Line Voltage (normal mode)	PULSE = Open I_L = 10 mA I_L = 20 mA I_L = 100 mA			 5 5.5 12	 V V V
V_{LP}	Line Voltage (pulse mode)	PULSE = V^- I_L = 20 mA I_L = 35 mA I_L = 80 mA			 4 5.5 9.5	 V V V
I_{hn}	ON/OFF-Hook Line Current Detection Threshold		6.5		9.5	mA
I_{hf}	OFF/ON-Hook Line Current Detection Threshold		5		8	mA
I_{OUT}	OFF-Hook Output Drive Current at Pin HDO	I_L = 10 mA $I_L \geq$ 20 mA	1.5 2			mA mA
V_{PM}	Pulse Input Low Voltage				0.8	V
I_{PM}	Pull-up Input Current at Pin PULSE (pulse mode)	I_L = 100 mA Pulse = V^-			20	µA
I_{NM}	Imput Current at Pin Pulse (normal mode)				3	µA

AC ELECTRICAL CHARACTERISTICS

(I_L = 10 mA to 100 mA, R_1 = 56 Ω, R_2 = 470 KΩ, S_1 = Open, T_{amb} = + 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_L	AC Line Impedance	C_1 = 2.2 µF F = 1 KHz		 20		 KΩ
	Sending/Receiving Distortion	F = 1 KHz V_S = 775 mV_{RMS} I_L = 15 to 100 mA			 2	 %
	Sending/Receiving Distortion	S_1 = Closed ; V_S = 1.3 V_{RMS}		2		%

APPLICATION INFORMATION

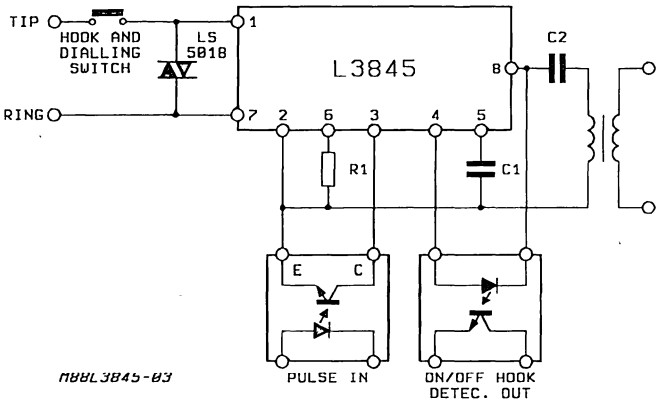
With the use of this circuit it is possible to terminate an analog trunk so that all the DC current component is flowing in the TRUNK TERMINATION CIRCUIT while the AC component is decoupled with a low voltage capacitor and can be used with a small and low cost audio coupler transformer to provide the AC balancing termination and two to four wire conversion.

Therefore it is usefull both for MODEM and PABX systems.

Figure 1 gives the typical application circuit ; it is worth to note that the TRUNK TERMINATION CIRCUIT, together with the LS5018 transient suppressor provides a compact and low cost module fully protected against lightning or overvoltages frequently present on telephone lines.

The $\overline{\text{PULSE}}$ input when connected to V- allows the device to reduce the Line Voltage and to show a resistive impedance equal to R1 to the line. When $\overline{\text{PULSE}}$ input is left open, this function is disable.

Figure 1 : Typical Application.



SGS-THOMSON MICROELECTRONICS

TEA7868

LINE INTERFACE

Designed to interface an equipment with the telephone line, this 8 pin IC provides :

- LINE ADAPTATION
- RING DETECTION

It is particularly convenient for modem applications and fulfills a wide range of international specifications.

Line adaptation : (DC characteristics)

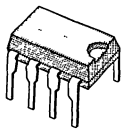
- ZENER CHARACTERISTIC WITH ADJUSTABLE SLOPE
- ADJUSTABLE DYNAMIC IMPEDANCE
- ADJUSTABLE MAXIMUM AMPLITUDE OF THE SIGNAL
- USE ONLY A LOW COST DRY TRANSFORMER
- NEED NO DIALLING RELAY

Ring detection :

- ADJUSTABLE DETECTION LEVEL
- ADJUSTABLE AC IMPEDANCE
- VERY LOW LINE DISTORTION
- LOGIC SIGNAL OUTPUT

Other :

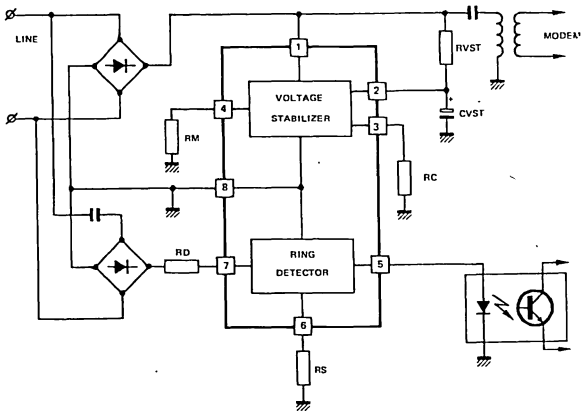
- LOW WORKING VOLTAGE
- WIDE OPERATING CURRENT RANGE



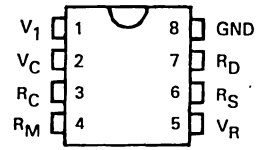
MINIDIP

ORDER CODE : TEA7868DP

BLOCK DIAGRAM



PIN CONNECTION (top view)



PIN DESCRIPTION

VOLTAGE STABILIZER

Name	N°.	Description
V_1	1	Voltage Over the IC
V_C	2	C_{VST} decouples the voltage stabilizer and R_{VST} fixes the impedance.
R_C	3	R_C fixes the voltage through R_{VST}.
R_M	4	R_M fixes the slope of the DC characteristic.
GND	8	Ground

RING DETECTOR

Name	N°.	Description
V_R	5	Ring detection output connected to an optocoupling device.
R_S	6	R_S fixes the ring detection level.
R_D	7	Ring Detection Input. R_D fixes the impedance of the ring detector.

OUTLINES

Specially designed for the modem applications, this 8 pins IC provides line adaptation, ring detection and easy pulse dialling. It is a Direct Connect Circuit (DCC) which has been designed to fulfill a wide range of AC and DC specifications for various countries.

RING DETECTION

This circuit detects the incoming ringing signal and generates a logic signal to the microcomputer via an optocoupling device. The detection level can be fixed by an external resistor. The dynamic impedance of the ring detector is also fixed by an external resistor. The line distortion of the ringing signal is very low compared to the distortion introduced by a zener detector.

LINE ADAPTATION

The DC characteristic can fulfill a wide range of DC specifications :

- zener characteristic with adjustable slope fixed by an external resistor
- line current limitation using an external CTP.

The dynamic impedance is fixed by an external resistor R_{VST} so as to match with different line impedances.

The maximum amplitude of the signal is fixed by two external resistors R_{VST} and R_C.

This circuit has been designed to be connected to a low cost dry transformer.

The application has been studied to avoid the use of dialling relay.

With its possibility of ring detection, off-hook are dialling this circuit is adapted to the application in smart modems. It also satisfies the FCC Rules Part 68.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_1 V_7	Supply Voltage	16 16	V V
P_{tot}	Power Dissipation	600	mW
T_{oper}	Operating Temperature	– 25 to 65	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

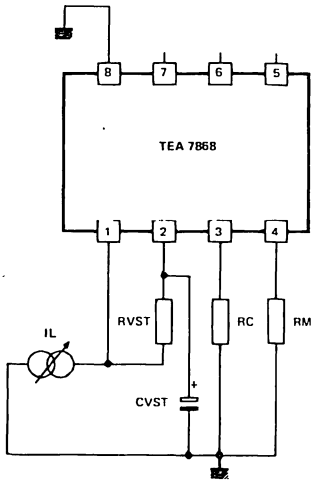
STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current (pin 1)	10		120	mA
V_1 V_1	Voltage over the IC (pin 1) (see fig. 1) I_L = 10 mA I_L = 100 mA	 3.0 4.3	 3.2 4.5	 3.4 4.7	 V V
V_C V_C	Voltage Stabilizer (pin 2) (see fig.1) I_L = 10 mA I_L = 100 mA	 1.9 3.2	 2.1 3.4	 2.3 3.6	 V V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

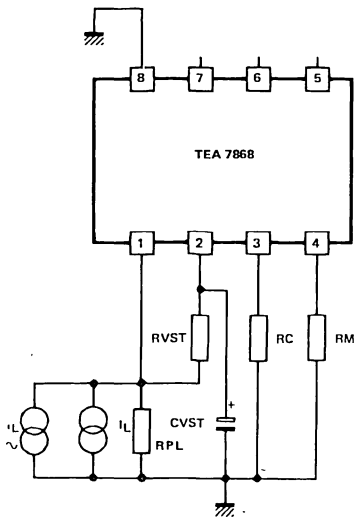
Symbol	Parameter	Min.	Typ.	Max.	Unit
R.L.	Impedance of the Transmission Part. (see fig. 2) Return loss compared to 600 Ω : 300 Hz < f < 5 kHz ; I_L = 20 mA	15			dB
V_R	Ring Detection Level (see fig. 3) for a Low Level on Pin 5 (< 0.3 V) : no Detection for a High Level on Pin 5 (> 0.8 V) : Ring Detection	19	20 20	 24	V_{pp}
Z_R	Impedance of the Ring Detection Part : Typically $R_S + R_D/13$ (see fig. 3)	9.5	10.5	11.5	kΩ
	Distortion in Ring Mode : f_{Ring} = 50 Hz (see note 4)				

Figure 1 : Static Electrical Characteristic Test Diagram.



External components :
C_{VST} = 100µF R_{VST} = 1.2kΩ
R_C = 2.7kΩ R_M = 12Ω.

Figure 2 : Impedance Measurement.



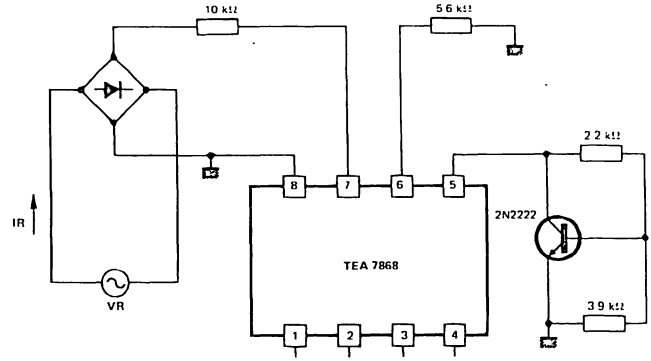
External components :
C_{VST} = 100µF R_{VST} = 1200Ω
R_C = 2.7kΩ R_M = 12Ω
RPL = 1200Ω

Return loss is defined by :

$$R.L. = 20\log\left(\frac{|Z_{out} + 600|}{|Z_{out} - 600|}\right)$$

$$Z_{out} = \frac{V_1}{i_L}$$

Figure 3 : Ring Detection Level and Impedance.

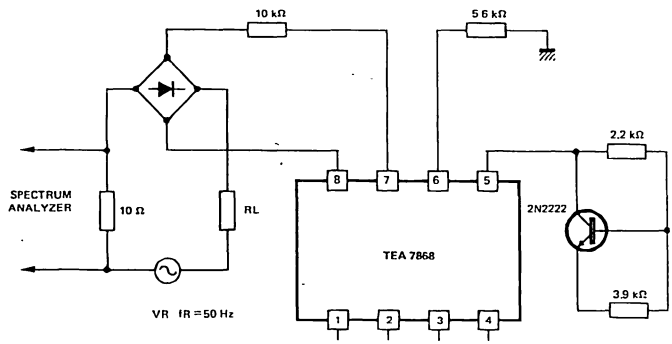


- Ring detection level
  for : $V_R = 19Vpp$ $V(5) < 0.3V$
  for : $V_R = 21Vpp$ $V(5) > 0.8V$
- Impedance of the ring detection part :

$$Z_R = \frac{V_R}{I_R}$$

Figure 4 : Ring Detection Distortion.

a)

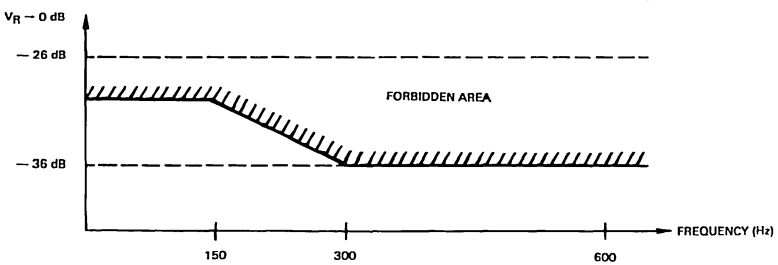


Test conditions :
$V_R = 90\ V_{RMS}$

$300\Omega < R_L < 1400\Omega$

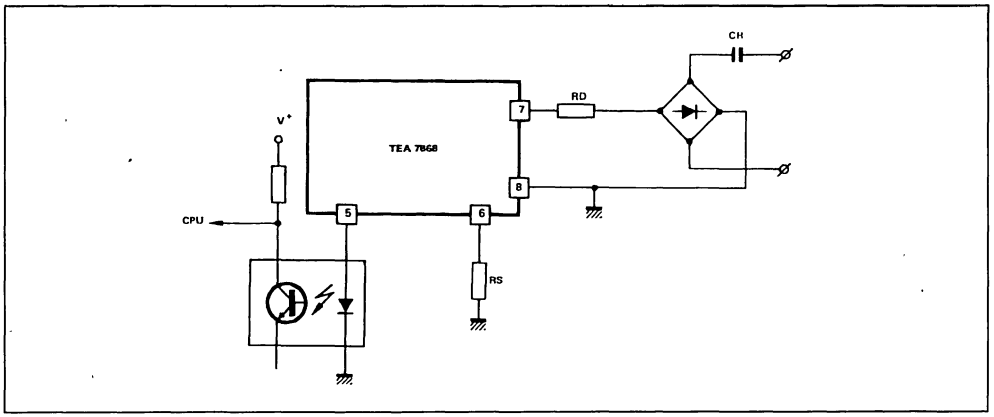
No distortion peaks appear in the forbidden area of the following shape :

b)



APPLICATIONS INFORMATION

Figure 5 : Ring Detection.



The ringing signal coming from the line is rectified by the diode bridge ; the circuit compares the peak amplitude of the signal to a predeterminated detection level fixed by R_S. On the output transistor of the optocoupling device a logic signal is generated which frequency is twice the frequency of the ringing signal.

"0" = the amplitude of the ringing signal is greater than the detection level.

"1" = the amplitude of the ringing signal is lower than the detection level.

The ring detection circuit is fully linear ; so the distortion on the line is very low compared to the distorsion introduced by a zener detector as usually used.

Three external components affect the characteristic of the ring detection circuit. The capacitor C_R provides the DC solation from the line.

The AC impedance of the circuit at the ringing frequency is given by the formula :

$$Z_{AC} = Z_{CR}(f) + R_D + R_S/13$$

Z_{CR} is the impedance of the capacitor C_R at the ringing frequency.

The ring detection level is fixed by the external resistor R_S with the following formula :

$$R_S = \frac{11 \text{ volts}}{V_R - V_D - 3 \text{ volts}} R_D$$

V_R is the peak amplitude of the ringing signal at the detection level.

V_D is the voltage over the diode bridge and the capacitor C_R at the ringing frequency.

The DC characteristic is a zener characteristic which slope is fixed by R_M (see fig.8). The voltage over the circuit (pin 1) is fixed via a current source driven through R_{VST}. The value of this current source is fixed by the external resistor R_C with the formula :

$$V(R_{VSI}) = V(pin1) - V(pin2) = \frac{R_{VSI}}{R_C} \times 2.46 \text{ volts}$$

Note that the voltage through R_{VST} also limits the amplitude of the emitted signal.

The external resistor R_{VST} also defines the AC impedance of the circuit :

$Z_{AC} = R_{VST}$ / / impedance seen from the transformer (see hybrid system)

* When a current limitation is required for the DC characteristic (as for the French specification), an external TPE is connected between the telephone line and the circuit (see application diagram).

PULSE DIALLING

Pulse dialling is easily done using a high voltage optocoupling device and a high voltage PNP transistor as shown on the typical application diagram.

HYBRID SYSTEM

This system uses an operational amplifier to prevent from injecting the emitted signal in the receiving path of the modem IC. A typical diagram is given at fig. 9.

R_L represents the impedance of the telephone line Z_L in parallel with R_{VST}. Typically we take Z_L = 600 ohms.

Figure 6 : AC/DC Line Adaptation.

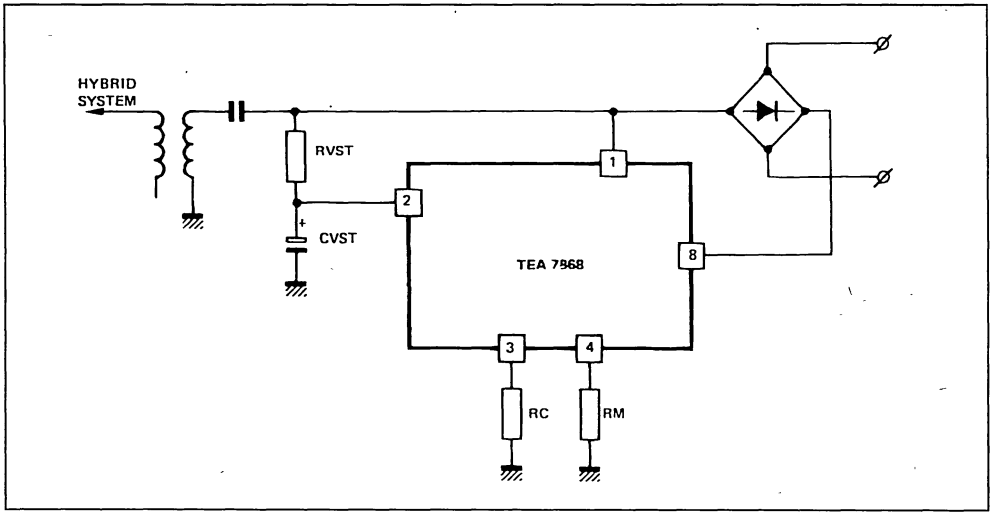


Figure 7 : This part of the TEA7868 is used for line adaptation.

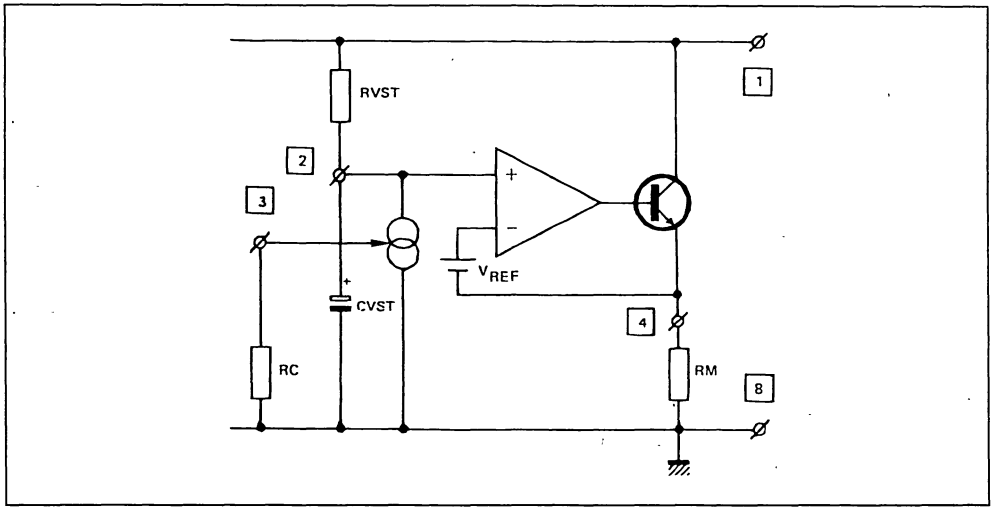
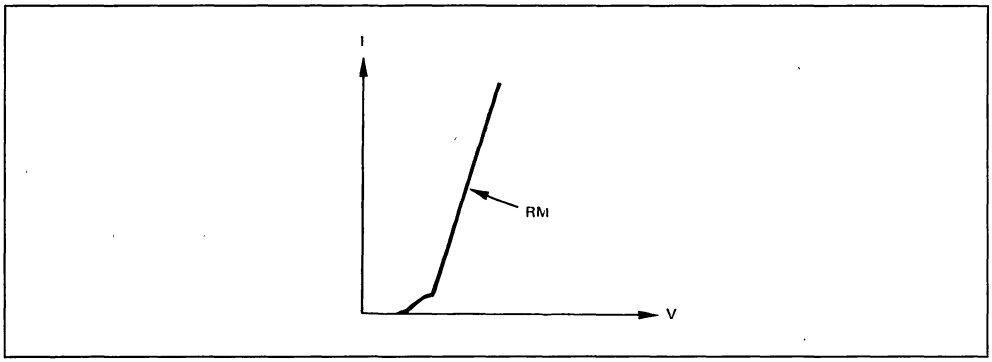


Figure 8 : An Equivalent Diagram of the Circuit is given at fig. 7.



The hybrid gain of the system is given by :

$$G_D = \frac{V_S}{V_E} = 1 - \frac{R_2 + R_3}{R_2} \cdot \frac{R_1}{R_1 + R_L}$$

For a maximum efficiency you must have $G_D = 0$ and this gives :

$$\frac{R_3}{R_2} = \frac{R_L}{R_1}$$

The impedance seen from the line must be 600 ohms, this impedance is given by :

$Z_{out} = R_1 // R_{VST}$

So, if R_{VST} is fixed, R_1 is also fixed by Z_{out} = 600 ohms.

The gain between the online signal and the modem input is :

$$G_E = \frac{R_L}{R_1 + R_L}$$

The gain between the line and the modem input is :

$$G_R = 1 + \frac{R_3}{R_2}$$

Those calculations are purely theoretical ; really the line impedance has a complex component, so there will be little changes in the value of R_1, R_2, R_3 to adapt the hybrid system.

Figure 9.

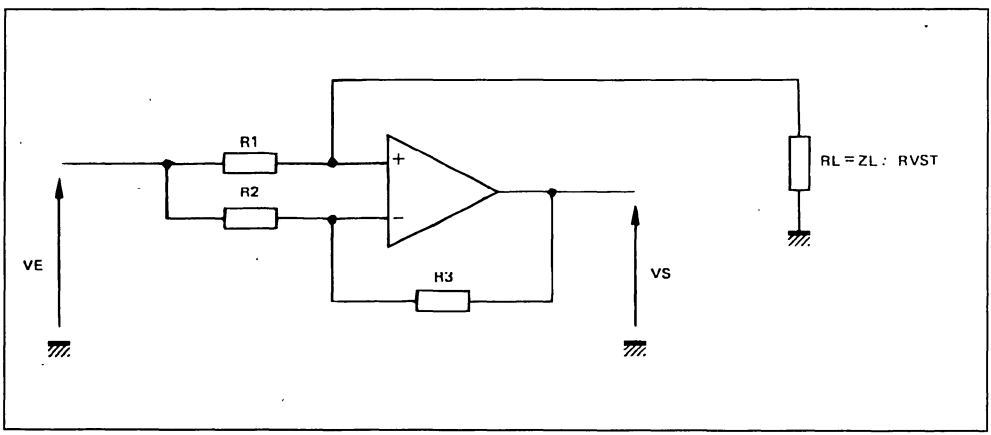


Figure 10 : Complete DAA Interface Circuit with TEA7868.

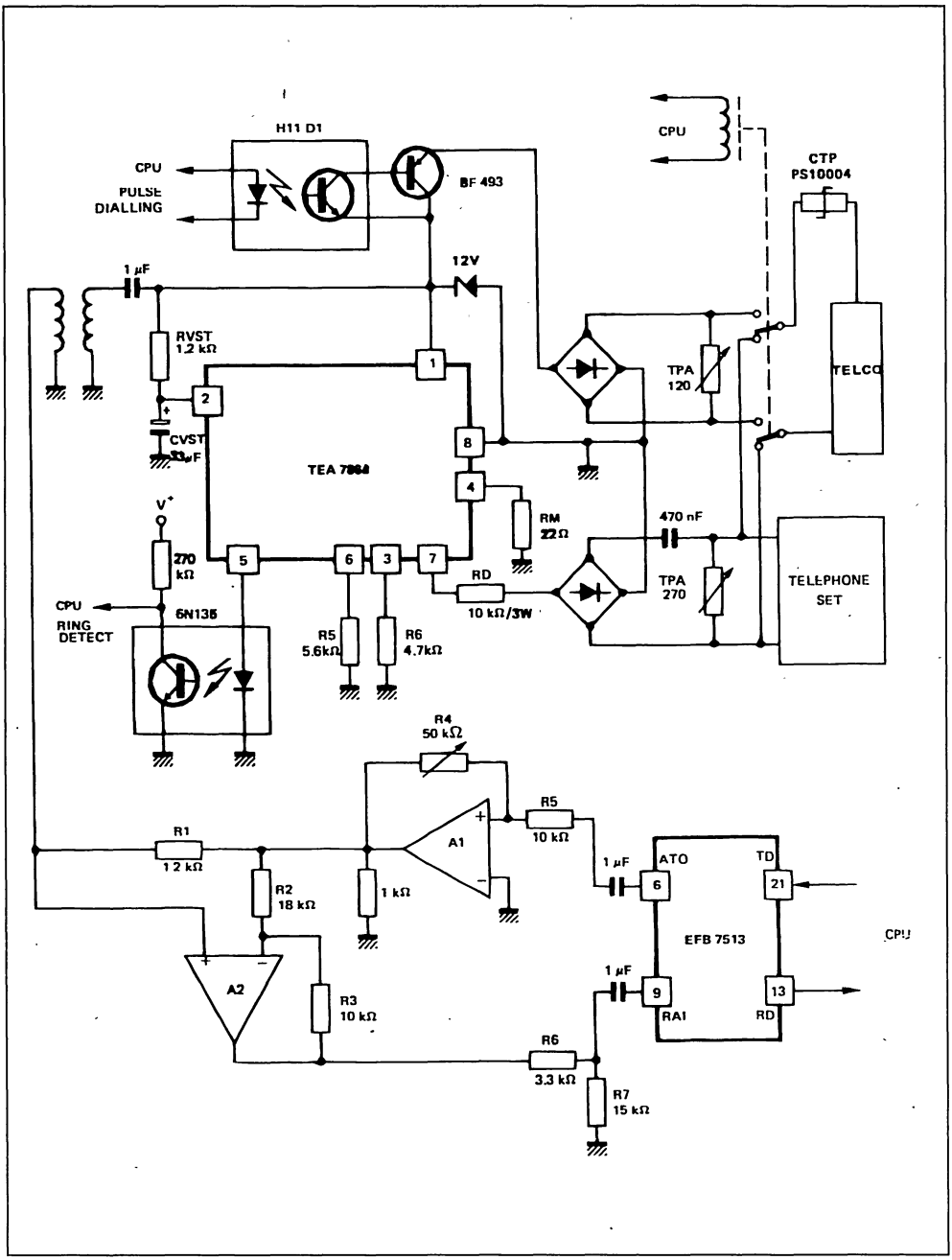
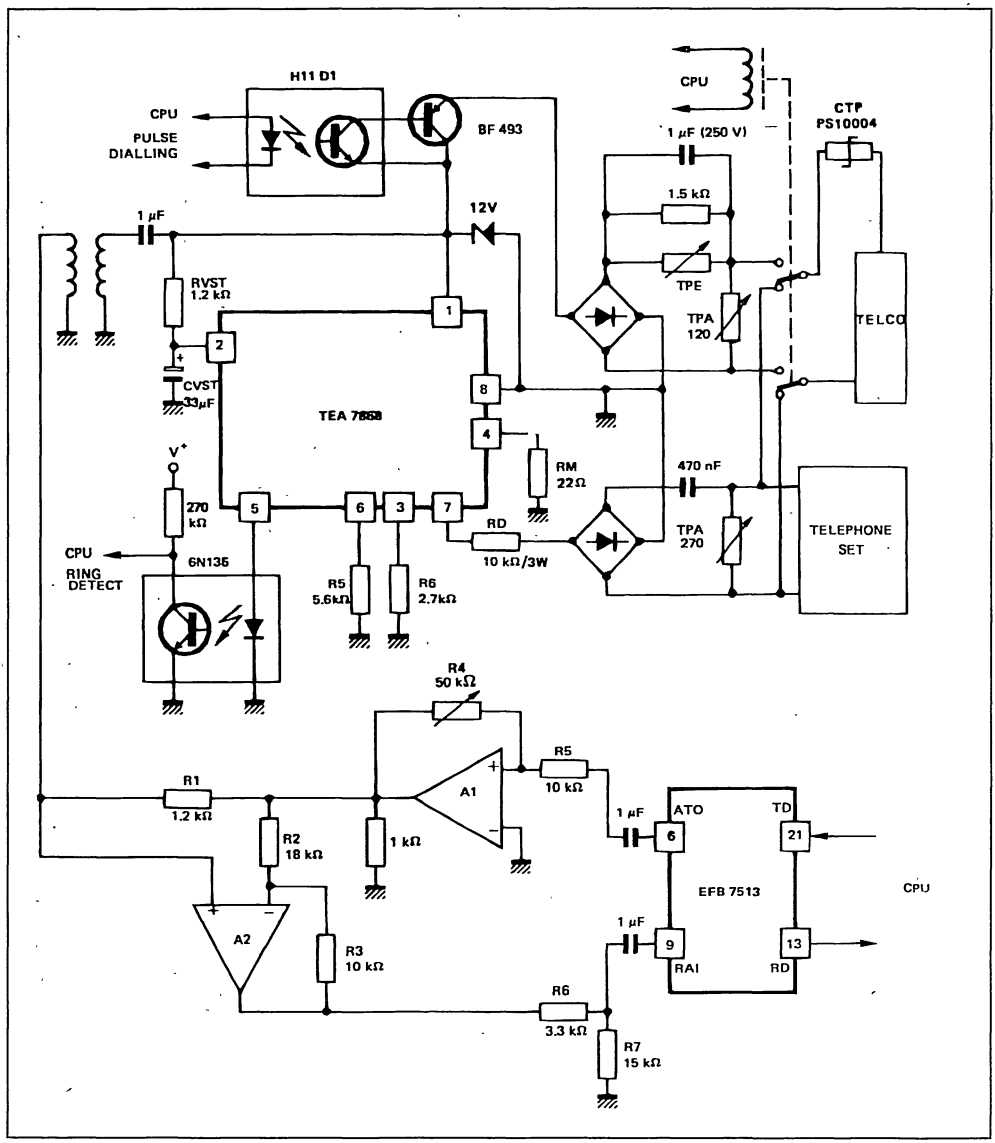


Figure 11 : Complete DAA Interface Circuit with Current Limitation.



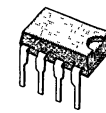
TELEPHONE INTERFACE CIRCUIT

AN AT&T PRODUCT

ADVANCE DATA

- WITHSTANDS TELEPHONE LOOP VOLTAGES TO 150 V DC AND 200 V PULSED
- OPERATES AT LOW TIP-RING VOLTAGES (typically as low as 2.7 V)
- POLARITY GUARD HAS LOW INTERNAL VOLTAGE DROPS
- MONOLITHIC SOLID-STATE CONSTRUCTION GIVES COMPETITIVE EDGE IN PHYSICAL AREA CONSERVATION AND RELIABILITY

MINIDIP

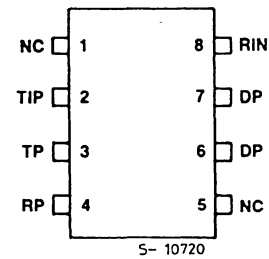


ORDER CODE : LH1028BB

DESCRIPTION

Dielectric isolation and a monolithic high-voltage DMOS technology are used to fabricate the LH1028 Telephone Interface Circuit (TIC). This integrated circuit performs the following basic functions : high-voltage dial pulse switching, protection against reversal of Tip-Ring polarity from the Central Office, and overvoltage/overcurrent protection of telephone circuits.

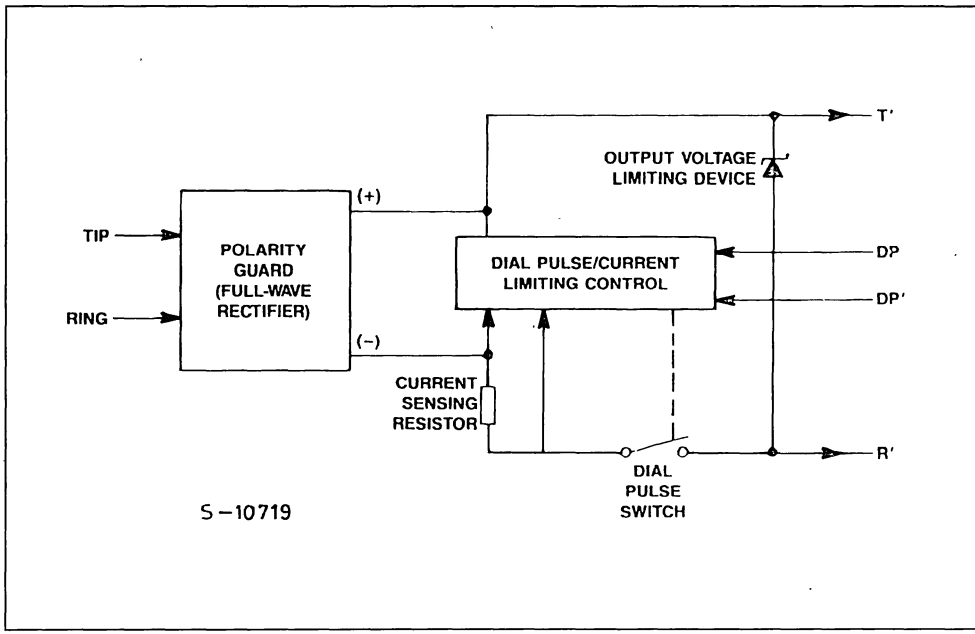
PIN CONNECTION (top view)



PIN DESCRIPTION

Pin	Symbol	Description
2	Tip	Tip Input
8	Ring	Ring Input
3	T Prime (T')	Positive Output of Polarity Guard
7	DP	Control for Internal Dial Pulse Switch
6	DP Prime (DP')	Control for Internal Dial Pulse Switch
4	R Prime (RP')	Negative Output of Polarity Guard
1,5	NC	No Connection Allowed Reserved Pins

Figure 1 : Functional Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{TRD}	Dialling Voltage (tip-ring) (t_{ON}= 2 ms ; f = 10 Hz)	180	V
V_{IMP}	Pulse Voltage (tip-ring) (t_{ON} = 2 µs ; t_{OFF} = 30 sec)	200	V
T_A	Ambient Operating Temperature Range	0 to 50	°C
T_{stg}	Storage Temperature Range	– 40 to + 125	°C
	Pin Temperature (soldering, 15 sec)	300	°C
P_D	Power Dissipation (package limitation)	750	mW

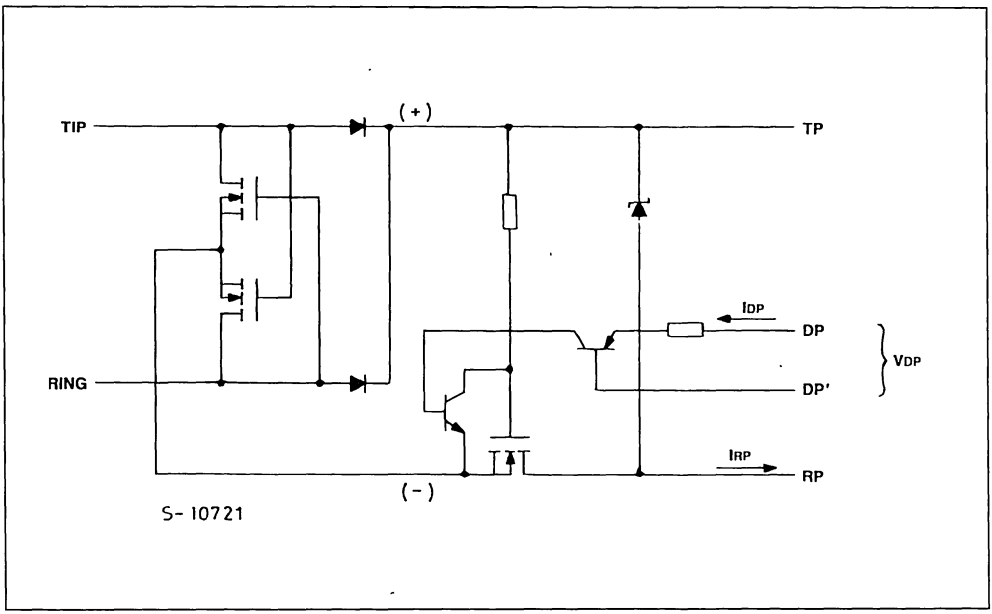
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction–ambient	Max	120	°C/W

ELECTRICAL CHARACTERISTICS (see figure 2)
(T_A = 4 to 49 °C for min. and max. value) (T_A = 25 °C for typical value)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Breakdown Voltage (tip-ring)	V_{DP} = 2 V ; R_L = 1000 Ω Increase V_{TR} until I_{TR} = 3 mA (see fig. 3)	155	175	–	V
Dial Pulse Control Voltage, V_{DP}	V_{TR} = 48 V ; R_L = 200 Ω I_{DP} = 5 µA (see fig. 4)	–	1.7	2	
Dial Pulse Control Current	V_{TR} = 48 V ; V_{DP} = 2 V ; R_L = 200 Ω (see fig. 3)	–	–	20	µA
Off-state Leakage Current	VTR = 48 V ; VDP = 2 V ; RL = 200 Ω (see fig. 3)	–	–	400	µA
Tip-ring Operating Voltage	Increase V_{TR} until V_{OUT} = .1.6 V (see fig. 4) R = 400 Ω I_{RP} = – 4 mA	–	2.7	2.9	V
On-state Voltage V_{TR} = 6 V	R = 235 Ω ; I_{RP} = – 20 mA ; V_{DP}= 0.65 V Measure V_{TR} – V_{OUT} (see fig. 4)	–	1.05	1.3	
Output Voltage, V_{TR} = 140 V peak	Measure V_{OUT} peak (see fig. 5)	–	26	30	
Turn-on Time	DP Initially at + 2 V (see fig. 6)	–	20	500	µs
Turn-off Time	DP Initially shorted to DP' (see fig. 7)	–	20	500	
Current Limiting	R_L = 40 Ω ; V_{DP} = 0.65 V (see fig. 8)	155	–	–	mA

Figure 2 : Simplified Schematic Illustrating Characteristic Symbology.



TEST CIRCUITS

Figure 3.

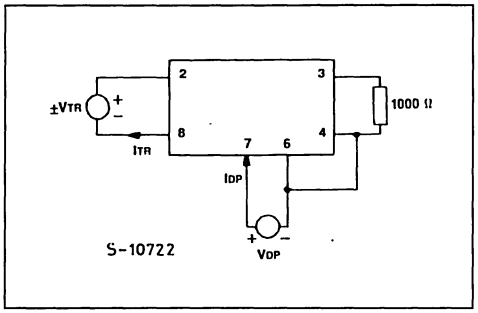


Figure 4.

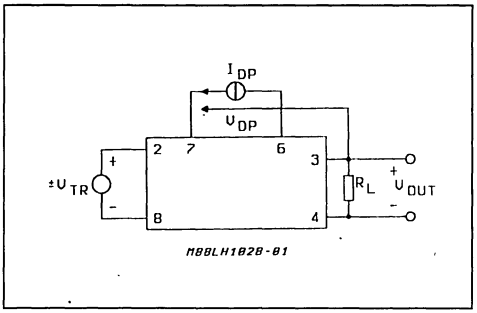
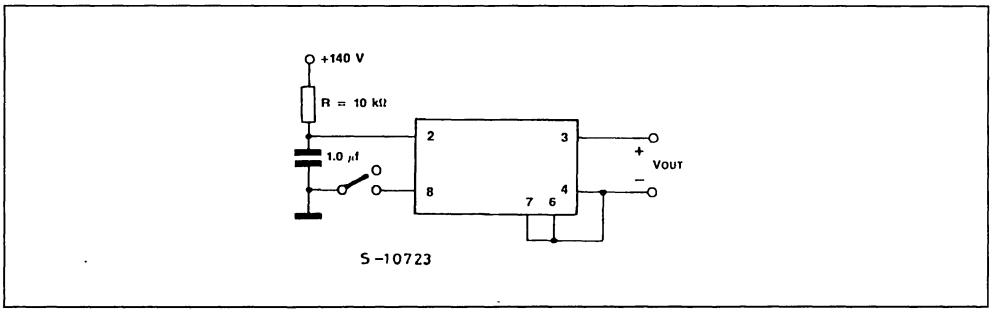


Figure 5.



CHARACTERISTIC TIMINGS

Figure 6 : Turn-on Time Test Method.

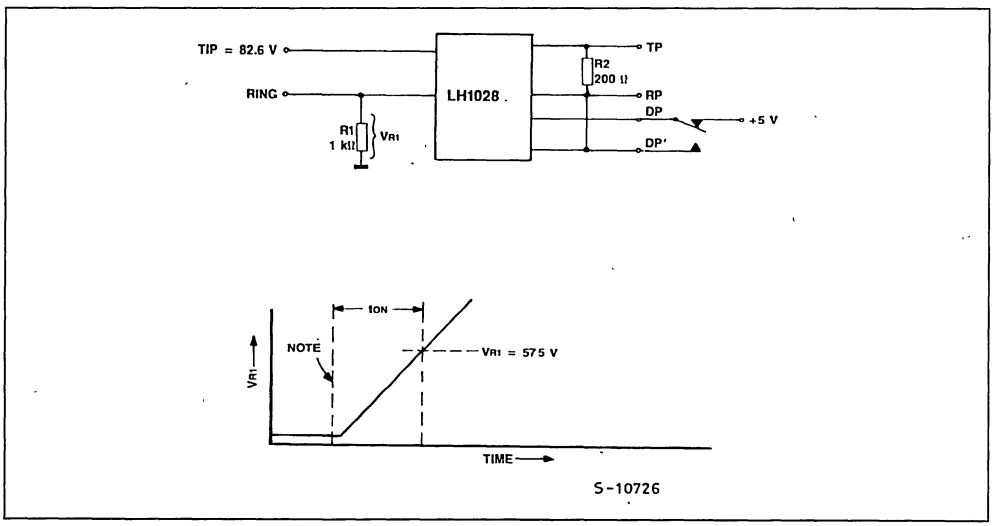


Figure 7 : Turn-off Time Test Method.

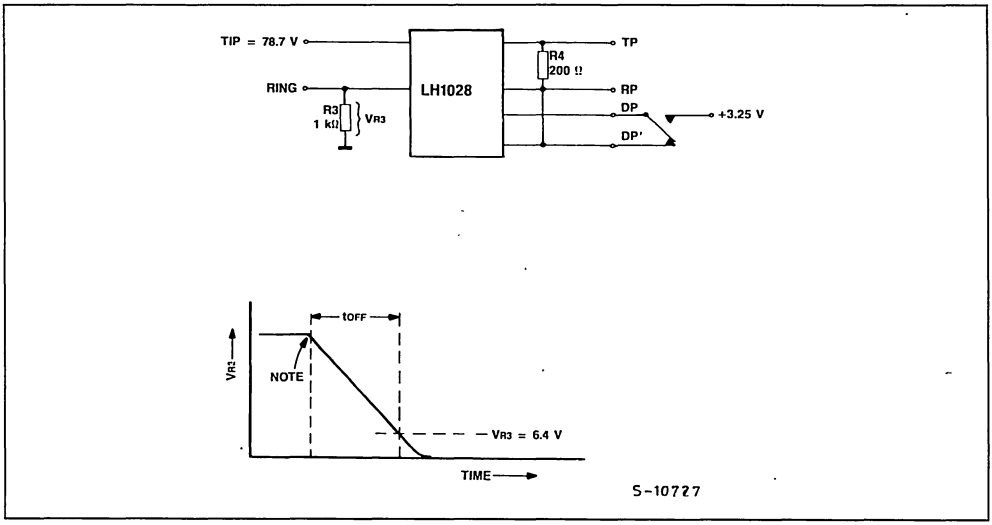
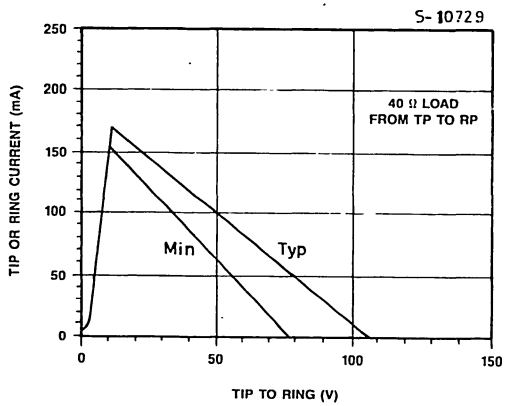


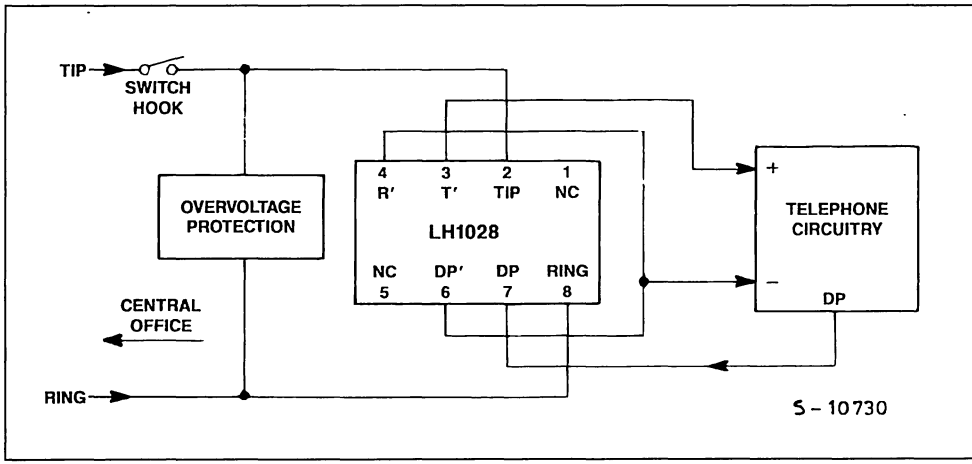
Figure 8 : Current Limiting Characteristics.



APPLICATION

The LH1028 device can be connected in the following manner to perform telephone interface functions. An overvoltage metal-oxide-varistor or other similar type of device shunts the Tip-Ring input terminal of the LH1028 TIC and limits the voltage across these terminals to less than 200 V (the maximum voltage rating of the LH1028). The output terminals of the LH1028 TIC are TPRIME (T') and RPRIME (R'). T' and R' are the positive and negative sides of the TIC polarity guard, respectively. R' is connected to the telephone circuitry through a switch which is internal to the LH1028 TIC. This internal switch opens when a dial pulse voltageis applied between terminal DP (Dial Pulse) and DP' (Dial Pulse Prime).

Figure 9 : Typical Telephone Set Configurations.



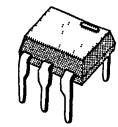
SGS-THOMSON MICROELECTRONICS

LH1056

SINGLE POLE HIGH-VOLTAGE SOLID-STATE RELAY

AN AT &T PRODUCT

- HIGH VOLTAGE IC FABRICATED IN A DIELECTRIC ISOLATION PROCESS
- OPTICAL COUPLING BETWEEN INPUT AND OUTPUT
- CAN SWITCH LOADS UP TO 350V AT CURRENTS UP TO 100mA
- LOW ON-RESISTANCE
- CLEAN, BOUNCE-FREE SWITCHING
- HIGH CURRENT SURGE CAPABILITY
- LOW-POWER CONSUMPTION
- NO ELECTROMAGNETIC INTERFERENCE



DIP6
(Plastic Package)

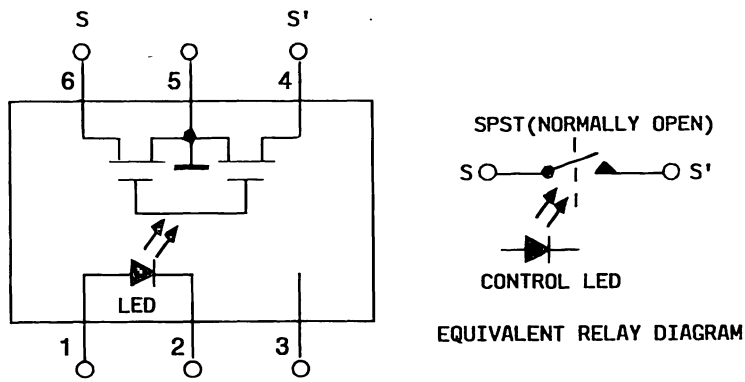
ORDER CODE : LH1056AT

DESCRIPTION

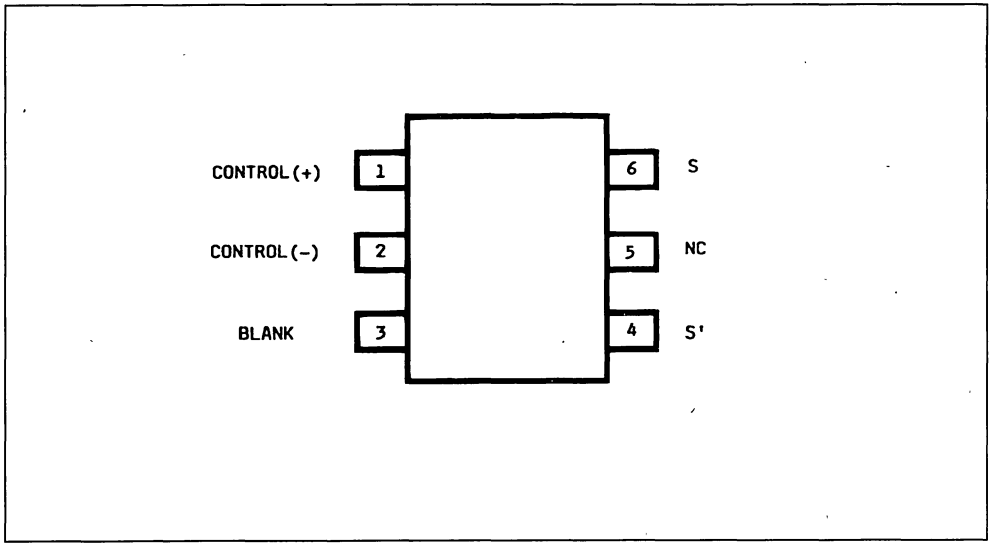
The LH1056 (Multipurpose Solid-State Relay) is a low-cost, bi-directional, SPST designed to switch both AC and DC loads. Output is rated at 350 volts and can handle loads up to 100mA. It is packaged in a special 6-pin plastic DIP.

Each device consists of one GaAlAs LED to optically couple the control signal to a high-voltage integrated circuit. The typical ON-Resistance is 30 ohms at 25mA, and is exceptionally linear up to 50mA. Beyond 50mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The LH1056 also has internal current limiting which clamps the load current at 150mA to insure that the device will survive during current surges.

Figure 1 : Functional and Equivalent Relay Diagrams.



PIN CONNECTION (top view)



PIN DESCRIPTION

Name	Description
Control + Control –	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
S-S'	These pins are the outputs. The pin pair S-S' represents one normally open relay pole.
Blank	This pin may be used as a tie-point for external components. Voltage on this pin should not exceed 300V.
NC	This pin is connected to internal circuitry. It should not be used as a tie-point for external circuitry.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	– 40 to + 85	°C
Storage Temperature Range	– 40 to + 100	°C
Pin Temperature (soldering time =15s)	300	°C
LED Input Ratings : Continuous Forward Current Reverse Voltage	20 10	mA V
Recommeded Maximum Output Operation : Operating Voltage Load Current	350 100	V mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
* LED Forward Current for Turn-on	I_{LOAD} = 100mA		1.5	2.5	mA
	I_{LOAD} = 80mA, 70°C		2.5	5.0	
LED ON Voltage	I_{LED} = 10mA	1.15	1.30	1.45	V
ON Resistance : $R_{ON} = V_M/25mA$	I_{LED} = 2.5mA ; I_{LOAD} = 25mA	20	30	50	Ω
Breakdown Voltage	I_{LED} = 0μA ; I_{LOAD} = 50μA	350	380		V
Output Off-state Leakage Current	100V, I_{LED} = 0μA		1.0	200	nA
	100V, I_{LED} = 200μA		0.1	2.0	μA
	300V, I_{LED} = 200μA		0.1	5.0	μA
Turn-on Time	R_{LOAD} = 10kΩ ; I_{LED} = 5mA		1.0	2.0	ms
Turn-off Time			0.5	2.0	
Feedthrough Capacitance, Pin 4 to 6 ($4V_{p-p}$, 1kHz)			24		pF

* Supply a minimum of 6mA LED current to insure proper operation over the full operating temperature range.

TEST CIRCUITS

Figure 2 : R_{ON}, ON Voltage and Breakdown Voltage.

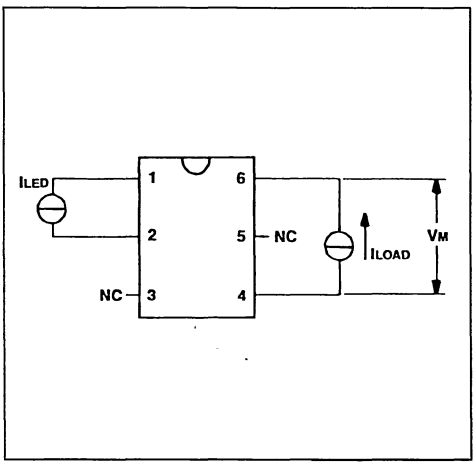


Figure 3 : Leakage Current.

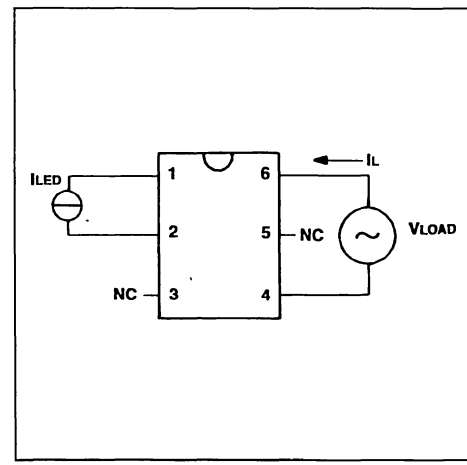
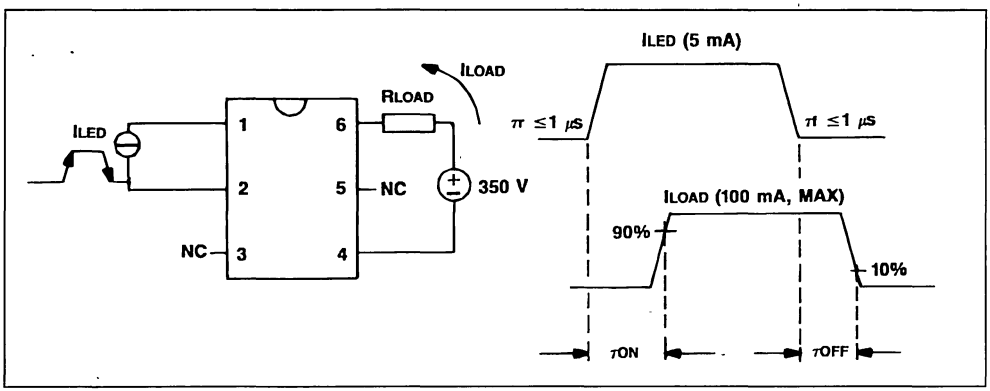


Figure 4 : τ_{ON}/τ_{OFF} Test Circuit and Waveform.



CHARACTERISTIC CURVES

Figure 5 : Solid-state Relay Typical ON Characteristics.

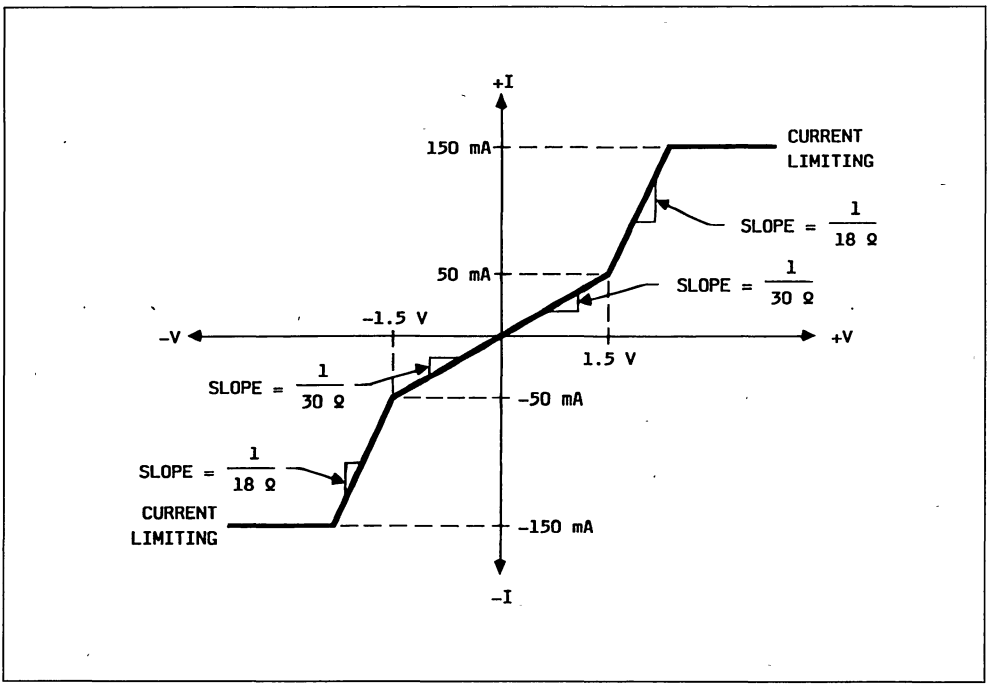


Figure 6 : Normalized Turn-on Time vs. Temperature.

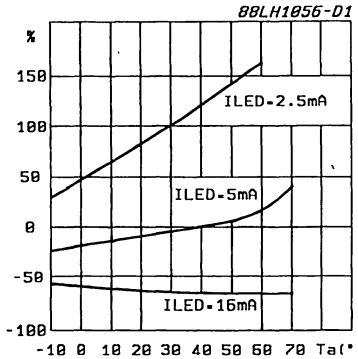


Figure 7 : Normalized Turn-off Time vs. Temperature.

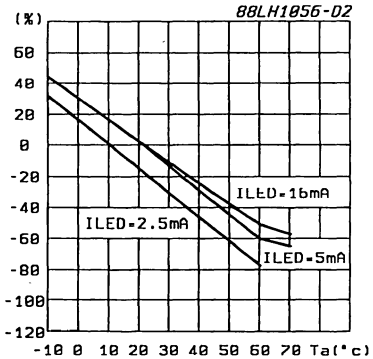


Figure 8 : Normalized Switching Time vs. Load Voltage.

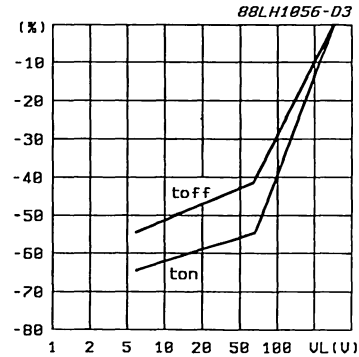


Figure 9 : Normalized On-resistance vs. Temperature.

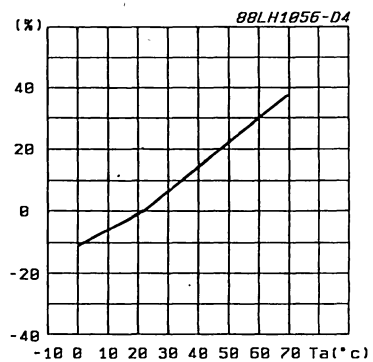


Figure 10 : Normalized Threshold Current vs. Temperature.

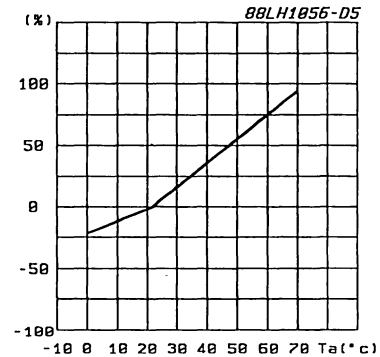
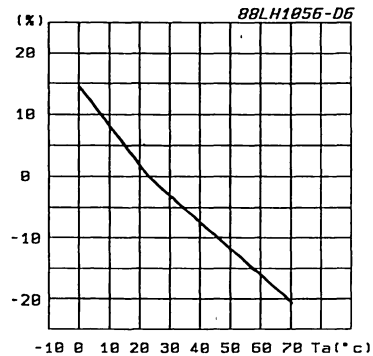


Figure 11 : Normalized Current Limit vs. Temperature.



INPUT/OUTPUT ISOLATION

The optical coupling between input and output provides a great degree of isolation between the low-voltage control and the high voltage output. Each device meets the 1500Vrms U/L (Underwriters Laboratories) test, which requires the product to withstand 1500Vrms for a time of one minute. For throughput purposes, U/L allows reduction of the test time to 1 second if the stress is increased to 1800Vrms.

In order to further assure long term reliability, each device is tested with an additional 600Vrms of guardband, bringing the total test stress to 2400Vrms for one second. During the test, less than 100nA of leakage is required. After passing this test, the part is subjected to the parameters specified by the data sheet.

LOAD PROTECTION

The LH1056 has been designed to protect the switching load by quick transient suppression and by output current limitation. These features can be illustrated by evaluation of the step response of the closed contact.

The circuit used for evaluation is shown in figure 12. First, a control signal is applied in order to activate the switch. Then transistor TR1 is turned on, which activates a 50V step through 100Ω across the closed switch. The switch reacts to the leading edge of the step by quickly deactivating, stopping current flow in the load. The resultant load current is shown in figure 13. After 250µs, the switch recloses, allowing current to flow in the load, up to the current limit of the device, if necessary. This clamping can be seen in figure 14 which also shows the fast shutoff at the leading edge of the step.

Figure 12 : Circuit used for Measurements of figures 13, 14.

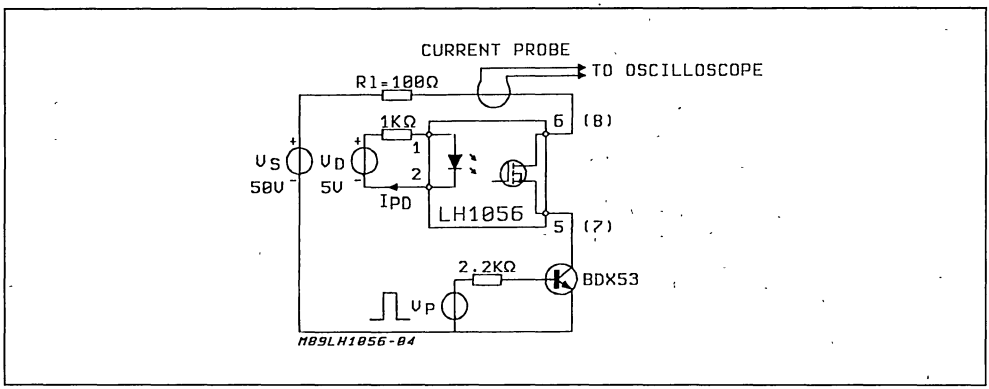


Figure 13 : Current Spike (R_L = 100Ω, V_S = 22V).
X = 0.5µs/div.
Y = 30mA/div.
Upper Trace : load current.
Lower Trace : command pulse.

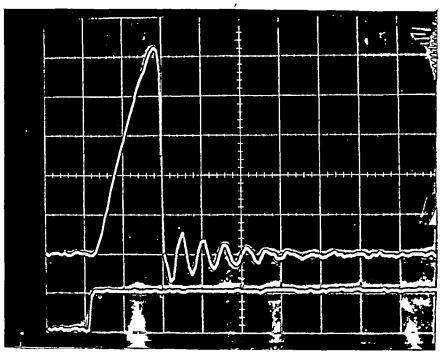
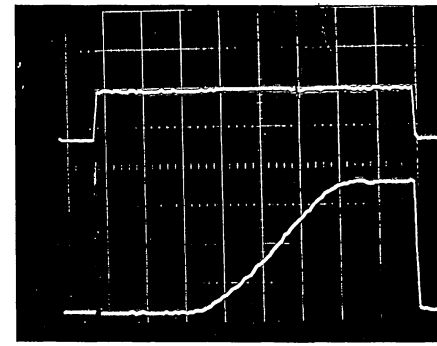


Figure 14 : Current limiting (V_S = 22V, R_L = 100Ω).
X = 0.2ms/div.
Y = 40mA/div.
Upper Trace : command pulse.
Lower Trace : load current.



APPLICATION

This device has been optimized to meet the demands of switching high voltages at moderate current levels in applications such as telecommunications, instrumentation, and medium-power switching. It is ideally suited for applications where high performance, noise-free switching of ac and dc signals is desirable.

The operational range of this device includes low-power commercial voltage applications where milampere control signals and low ON-resistance are required. The speed, reliability, and linearity of this switch makes it well suited for those applications which are beyond the range of mechanical relays, thyristors, and triacs. For lower ON resistance, higher voltages, or greater current capability, the LH1056 can be easily combined in parallel or series arrangements, as required, with their control LEDs simply driven in series.

The low ON-resistance and low-noise features are beneficial in instrumentation applications. The optical coupling provides isolation of the switch from the control signal in high-voltage and high-frequency applications.

The fabrication of high-voltage, monolithic ICs in a unique dielectric isolation process provides high reliability and the solid-state construction eliminates problems associated with mechanical relays such as sensitivity to shock and vibration.

Figure 15 : Triac Predriver.

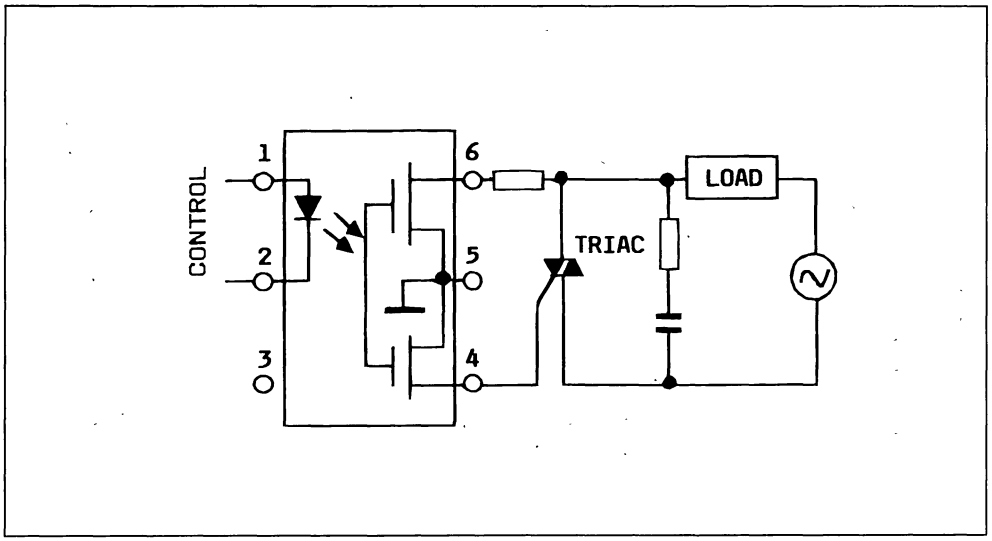
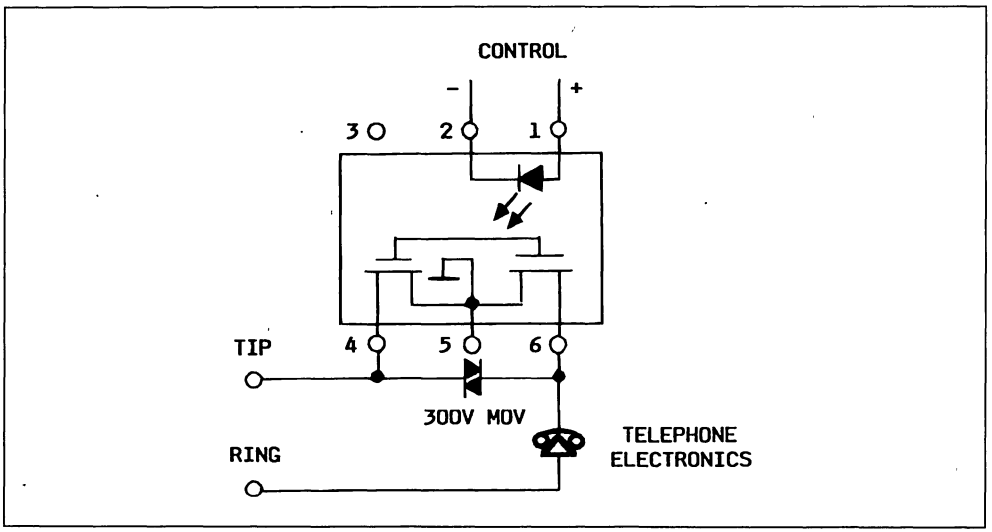


Figure 16 : Telephone Switchhook.



SGS-THOMSON MICROELECTRONICS

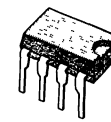
LH1061

DOUBLE POLE HIGH-VOLTAGE SOLID-STATE RELAY

ADVANCE DATA

AN AT & T PRODUCT

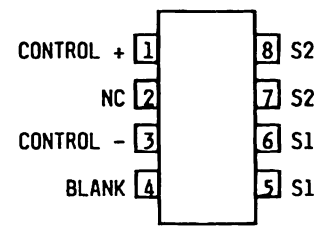
- HIGH VOLTAGE IC FABRICATED IN A DIELECTRIC ISOLATION PROCESS
- OPTICAL COUPLING BETWEEN INPUT AND OUTPUT
- CAN SWITCH TWO SEPARATE LOADS UP TO 200V EACH AT CURRENTS UP TO 200mA
- LOW ON-RESISTANCE
- CLEAN, BOUNCE-FREE SWITCHING
- HIGH CURRENT SURGE CAPABILITY
- LOW-POWER CONSUMPTION
- NO ELECTROMAGNETIC INTERFERENCE



Minidip

ORDER CODE : LH1061AB

PIN CONNECTION

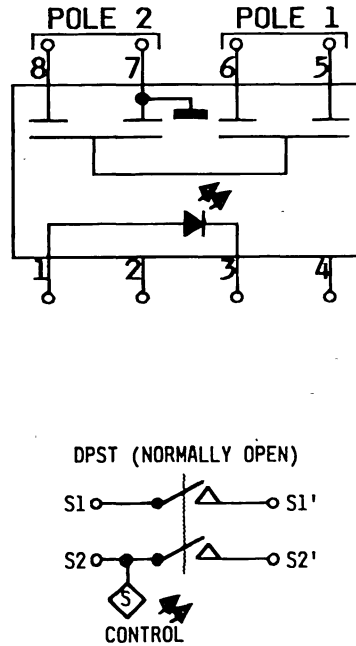


DESCRIPTION

The LH1061 (Multipurpose Solid-State Relay) is a low-cost, bi-directional, SPDT designed to switch both AC and DC loads. Outputs are rated at 200V and can handle contemporarily two loads up to 200mA. It is packaged in a special 8-pin plastic DIP.

Each device consists of one GaAlAs LED to optically couple the control signal to two high-voltage integrated switches. The typical ON-Resistance is 15Ω at 25mA, and is exceptionally linear up to 100mA. Beyond 100mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The LH1061 also has internal current limiting which clamps the load current at 300mA to insure that the device will survive during current surges.

Figure 1 : Functional and Equivalent Diagram.



PIN DESCRIPTION

Name	Description
Control + Control –	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
S1, S1' S2, S2'	These pins are the outputs. The pins designated as S represents one side of a relay pole. The pins designated as S' are the complementary side of a relay pole. Note that S2 is connected to the substrate.
NC	This pin is connected internally for test purposes. It should NOT be used as a tie-point for external components.
Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should no exceed 150V.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	– 40 to + 85	°C
Storage Temperature Range	– 40 to + 100	°C
Pin Soldering Temperature (t = 15s max)	300	°C
LED INPUT : Continuous Forward Current Reverse Voltage	 20 10	 mA V
Operating Voltage	200	V
One Pole (S1, S1' or S2, S2')	300	mA
Each Pole (two poles operating simultaneously)	200	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LED Forward Current for Turn-on*	I_{LOAD} = 200mA		1.5	2.5	mA
	I_{LOAD} = 160mA, 70°C		2.5	5.0	mA
LED ON Voltage @ 10mA	I_{LED} = 10mA	1.15	1.30	1.45	V
ON Resistance : $R_{ON} = V_M/50mA$	I_{LED} = 2.5mA ; I_{LOAD} = 50mA	8	12	15	Ω
ON Voltage	I_{LED} = 2.5mA ; I_{LOAD} = 200mA		2.0	2.5	V
Output Off-state Leakage Current	100V, I_{LED} = 0µA		1.0		nA
	100V, I_{LED} = 200µA		0.1	2.0	µA
Breakdown Voltage @ 50µA (figure 2)	I_{LED} = 0µA ; I_{LOAD} = 50µA	200	230		V
Turn-on Time	R_L = 15kΩ I_{LED} = 5mA		2.0		ms
Turn-off Time			1.0		
Feedthrough Capacitance, Pin 4 to 6 ($4V_{pp}$, 1kHz)			35		pF
Pole to pole Capacitance ($4V_{pp}$, 1kHz)			20		pF

* Supply a minimum of 6mA LED current to insure proper operation over the full operating temperature range.

TEST CIRCUITS

Figure 2 : R_{ON}, ON Voltage and Breakdown Voltage.

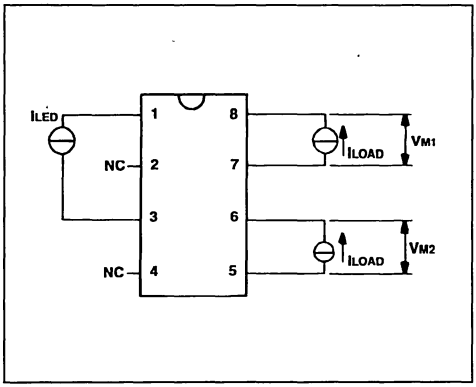


Figure 3 : Leakage Current.

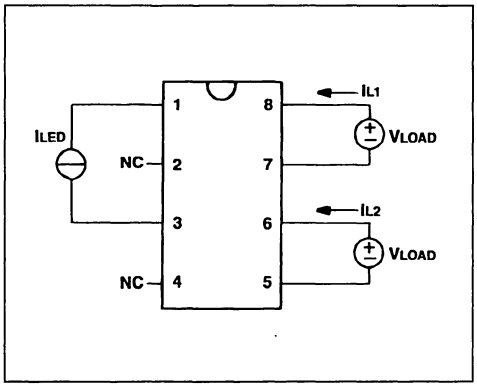
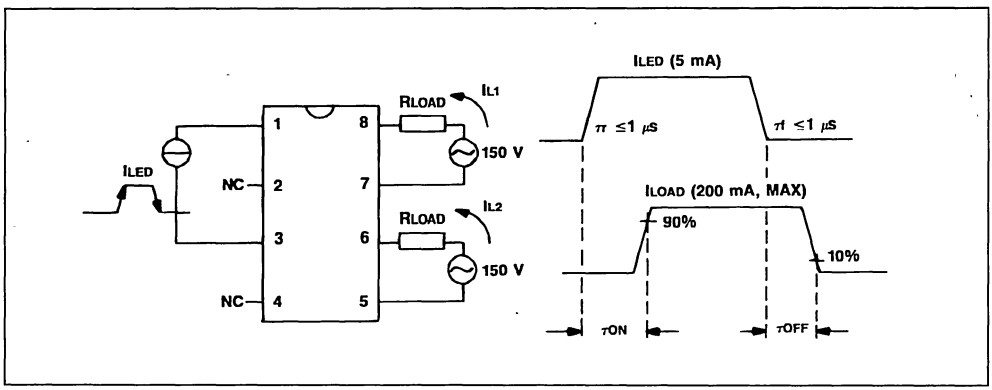


Figure 4 : τ_{ON}/τ_{OFF} Test Circuit and Waveform.



CHARACTERISTICS CURVES

Figure 5 : Solid-state Relay Typical ON Characteristics.

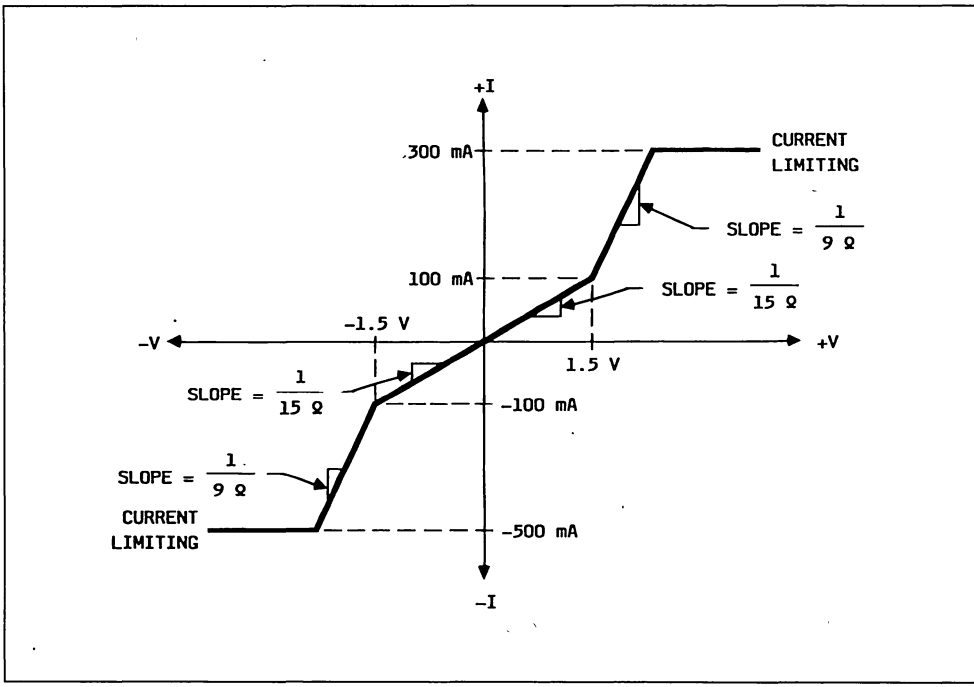


Figure 6 : Normalized Turn-on Time vs. Temperature.

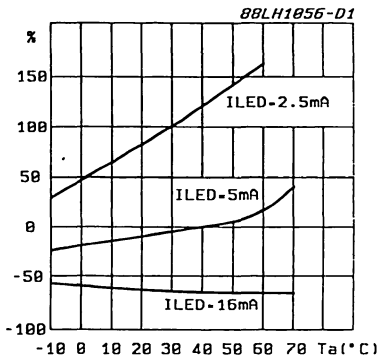


Figure 7 : Normalized Turn-off Time vs. Temperature.

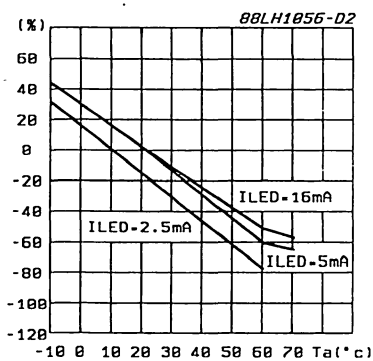


Figure 8 : Normalized Switching Time vs. Load Voltage.

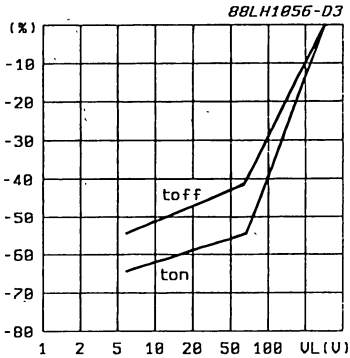


Figure 9 : Normalized On-resistance vs. Temperature.

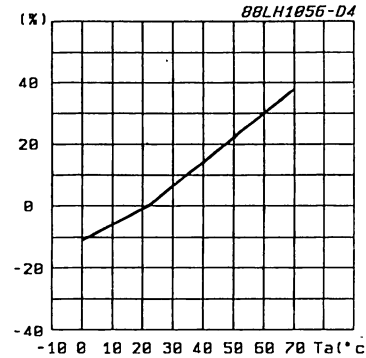


Figure 10 : Normalized Threshold Current vs. Temperature.

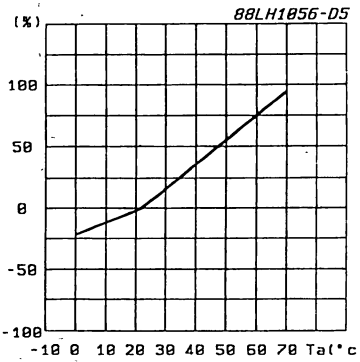
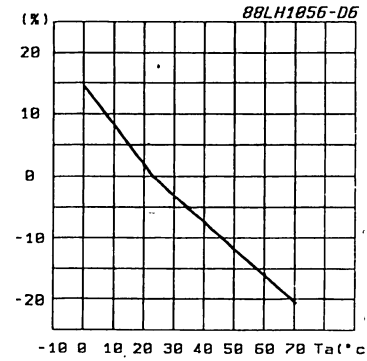


Figure 11 : Normalized Current Limit vs. Temperature.



INPUT/OUTPUT ISOLATION

The optical coupling between input and output provides a great degree of isolation between the low-voltage control and the high-voltage output. Each device meets the 1500Vrms U/L (Underwriters Laboratories) test, which requires the product to withstand 1500Vrms for a time of one minute. For throughput purposes, U/L allows reduction of the test time to 1 second if the stress is increased to 1800Vrms.

In order to further assure long term reliability, each device is tested with an additional 600Vrms of guardband, bringing the total test stress to 2400Vrms for one second. During the test, less than 100nA of leakage is required. After passing this test, the part is subjected to the parameters specified by the data sheet.

LOAD PROTECTION

The LH1061 has been designed to protect the switched load by quick transient suppression and by output current limitation. These features can be illustrated by evaluation of the step response of the closed contact.

The circuit used for evaluation is shown in figure 12. First, a control signal is applied in order to activate the switch. Then transistor TR1 is turned on, which activates a 50V step through 100Ω across the closed switch. The switch reacts to the leading edge of the step by quickly deactivating, stopping current flow in the load. The resultant load current is shown in figure 13. After 250µs, the switch recloses, allowing current to flow in the load, up to the current limit of the device, if necessary. This clamping can be seen in figure 14 which also shows the fast shutoff at the leading edge of the step.

Figure 12 : Circuit used for Measurements of figures 13, 14.

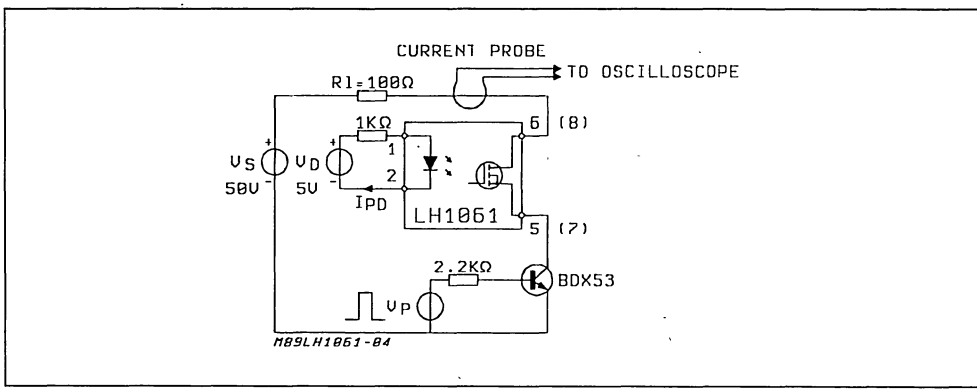


Figure 13 : Current spike (R_L = 100Ω, V_S = 50V).
X = 0.5µs/div.
Y = 60mA/div.
Upper Trace : load current.
Lower Trace : command pulse.

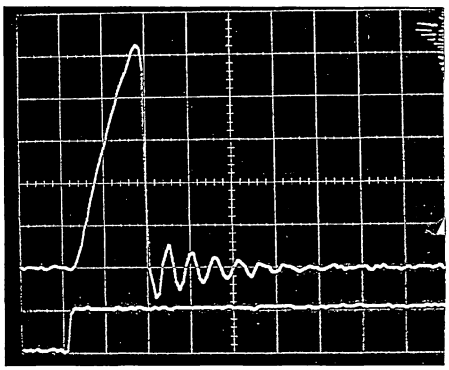
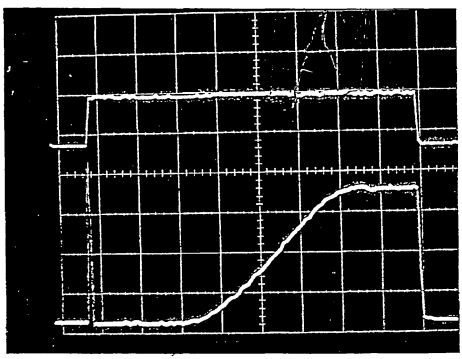


Figure 14 : Current limiting (V_S = 50V, R_L = 100Ω).
X = 0.2ms/div.
Y = 80mA/div.
Upper Trace : command pulse.
Lower Trace : load current.



APPLICATION

This device has been optimized to meet the demands of switching high voltages at moderate current levels in applications such as telecommunications, instrumentation, and medium-power switching. It is ideally suited for applications where high performance, noise-free switching of ac and dc signals is desirable.

The operational range of this device includes low-power commercial voltage applications where milampere control signals and low ON-resistance are required. The speed, reliability, and linearity of this switch makes it well suited for those applications which are beyond the range of mechanical relays, thyristors, and triacs. For lower ON resistance, higher voltages, or greater current capability, the LH1061 can be easily combined in parallel or series arrangements, as required, with their control LEDs simply driven in series.

The low ON-resistance and low-noise features are beneficial in instrumentation applications. The optical coupling provides isolation of the switch from the control signals in high-voltage and high-frequency applications.

The fabrication of high-voltage, monolithic ICs in a unique dielectric isolation process provides high reliability and the solid-state construction eliminates problems associated with mechanical relays such as sensitivity to shock and vibration.

Figure 15 : Balanced Switchhook Application.

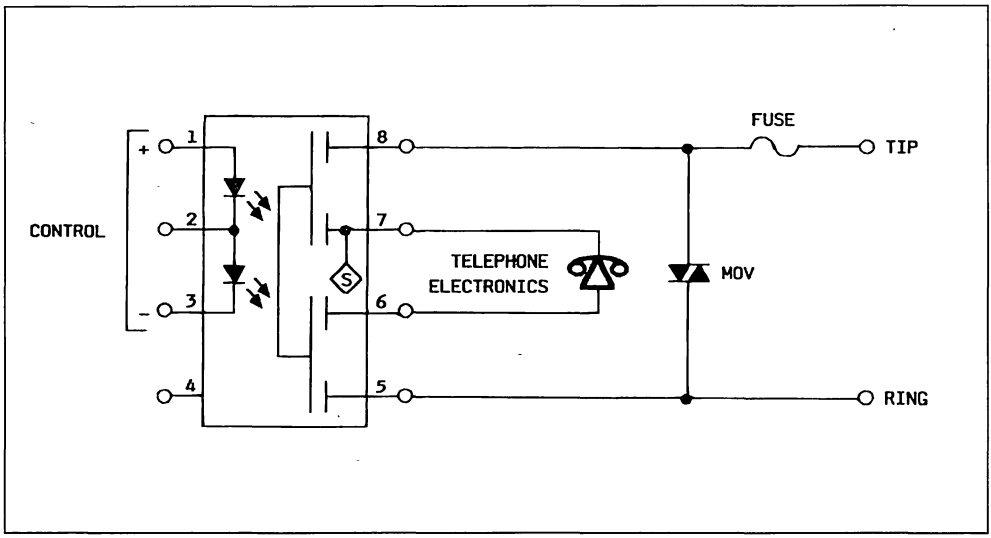
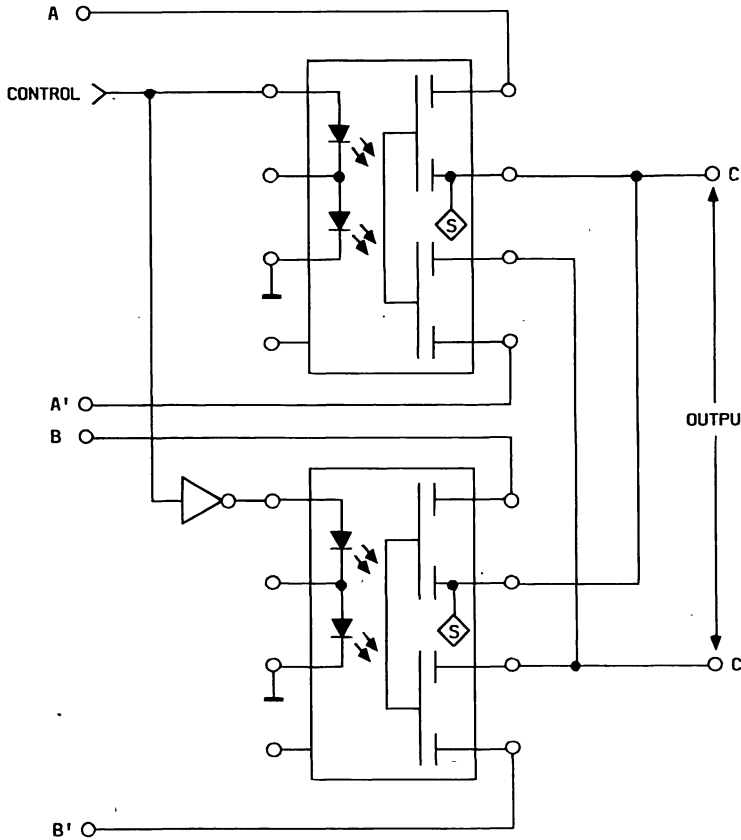


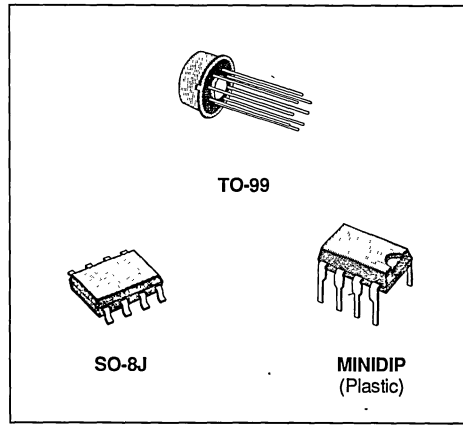
Figure 16 : Balanced Two-line Multiplexer Application.



OP-AMPs COMPARATORS

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



TO-99

SO-8J

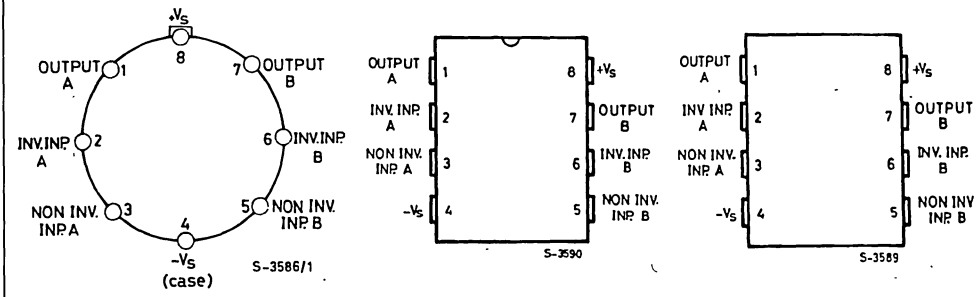
MINIDIP
(Plastic)

DESCRIPTION

The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

PIN CONNECTIONS (top views)

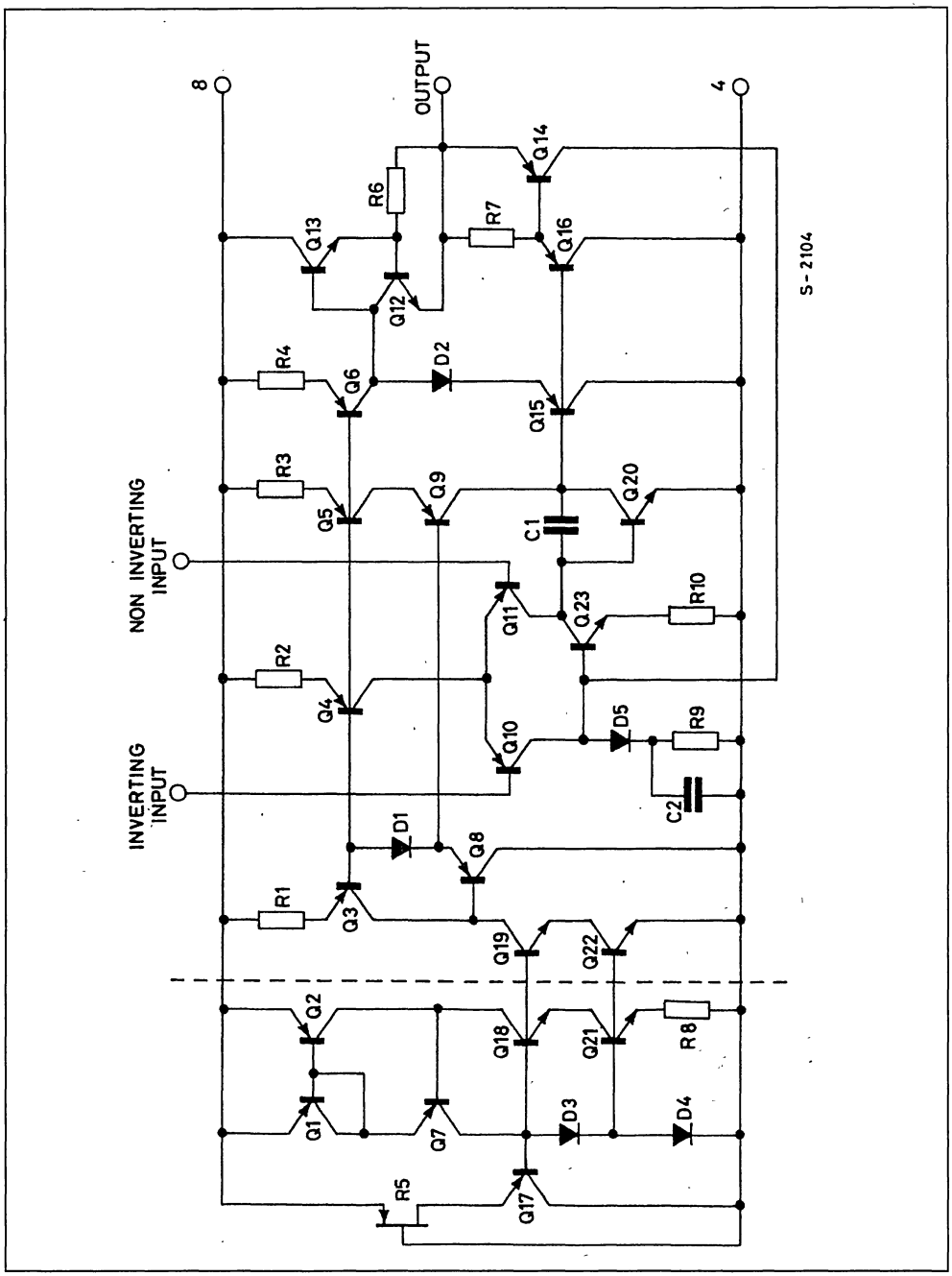


TO-99 Minidip SO-8

ORDER CODES

Type	TO-99	Minidip	SO-8
LS204	LS204TB	–	LS204M
LS204A	LS204ATB	–	–
LS204C	LS204CTB	LS204CB	LS204CM

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		TO-99	Minidip	µPackage
V_s	Supply Voltage		± 18V		
V_i	Input Voltage		± V_s		
V_i	Differential Input Voltage		± (V_s – 1)		
T_{op}	Operating Temperature for	**LS204** **LS204A** **LS204C**	– 25 to 85°C – 55 to 125°C 0 to 70°C		
P_{tot}	Power Dissipation at T_{amb} = 70°C		520mW	665mW	400mW
T_j	Junction Temperature		150°C	150°C	150°C
T_{stg}	Storage Temperature		– 65 to 150°C	– 55 to 150°C	– 55 to 150°C

THERMAL DATA

			TO-99	Minidip	SO-8J
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	155°C/W	120°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply Current			0.7	1.2		0.8	1.5	mA
I_b	Input Bias Current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input Resistance	f = 1KHz		1			0.5		MΩ
V_{os}	Input Offset Voltage	$R_g \leq 10K\Omega$		0.5	2.5		0.5	3.5	mV
		$R_g \leq 10K\Omega$ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	R_g = 10KΩ $T_{min} < T_{op} < T_{max}$		5			5		µV/°C
I_{os}	Input Offset Current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output Short Circuit Current			23			23		mA
G_v	Large Signal Open Loop Voltage Gain	$T_{min} < T_{op} < T_{max}$ R_L = 2KΩ V_s = ± 15V V_s = ± 4V	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS204/LS204A			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
d	Distortion	G_V = 20dB R_L = 2KΩ V_o = 2V_{PP} f = 1KHZ		0.03	0.1		0.03	0.1	%
V_o	DC Output Voltage Swing	R_L = 2KΩ V_s = ± 15V V_s = ± 4V	± 13	± 3		± 13	± 3		V
V_o	Large Signal Voltage Swing	R_L = 10KΩ f = 10KHz		28			28		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2KΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection	V_i = 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply Voltage Rejection	V_i = 1V f = 100Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel Separation	f = 1KHz 100	120			120			dB

Note :

Temp.	LS204	LS204A	LS204C
$T_{min.}$	– 25°C	– 55°C	0°C
$T_{max.}$	+ 85°C	+ 125°C	+ 70°C

Figure 1: Supply Current vs. Supply Voltage.

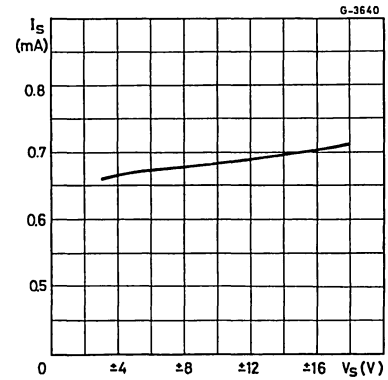


Figure 2 : Supply Current vs. Ambient Temperature.

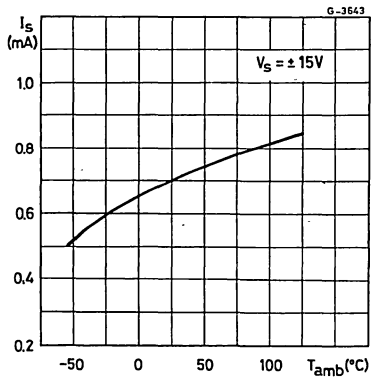


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

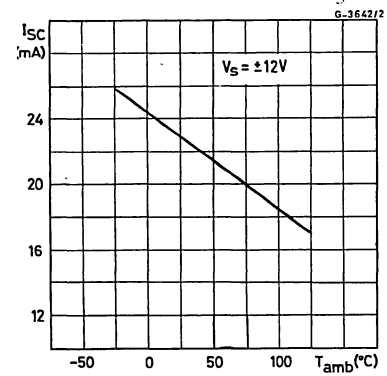


Figure 4: Open Loop Frequency and Phase Response.

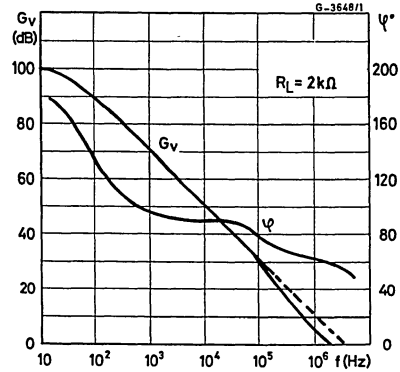


Figure 5: Open Loop Gain vs. Ambient Temperature.

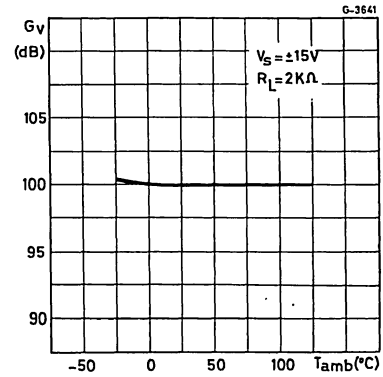


Figure 6 : Supply Voltage Rejection vs. Frequency.

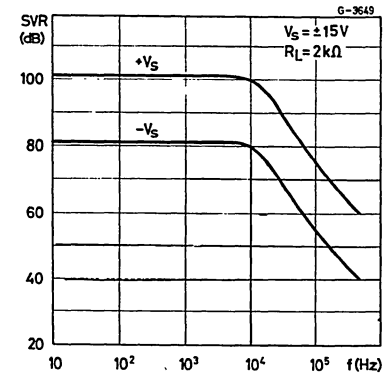


Figure 7 : Large Signal Frequency Response.

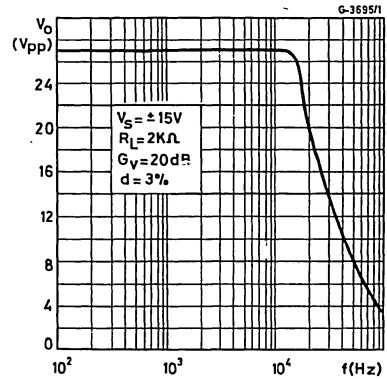


Figure 8 : Output Voltage Swing vs. Load Resistance.

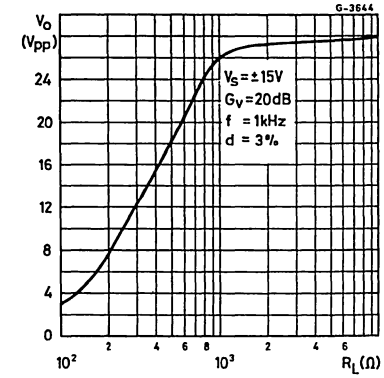
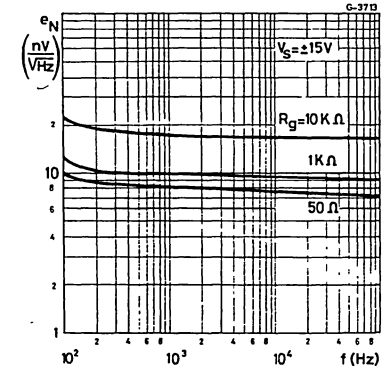


Figure 9 : Total Input Noise vs. Frequency.



APPLICATION INFORMATION

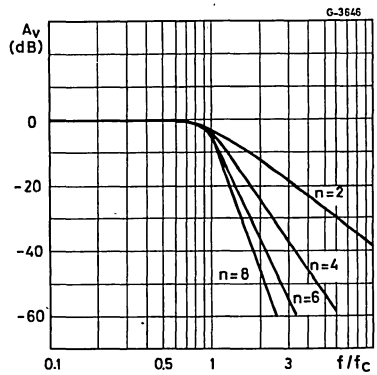
Active low-pass filter :

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

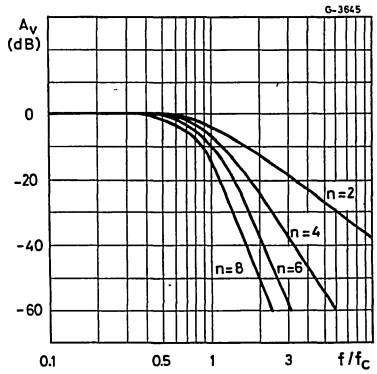
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3dB frequency of the filter

	2 pole	4 Pole	6 Pole	8 Pole
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

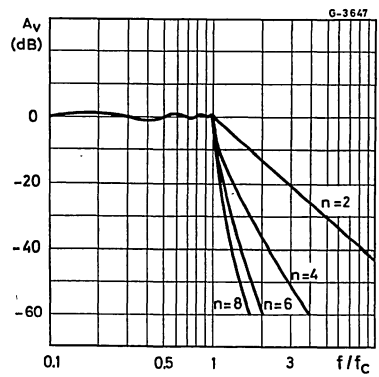
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

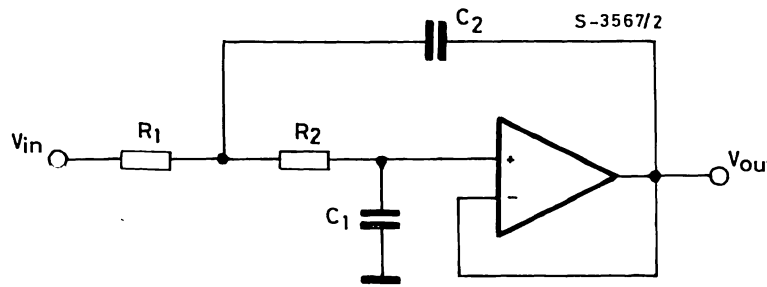
Other characteristics :
- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0 .1%	± 0.01%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ± 0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ± 1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_C} + \frac{S^2}{\omega_C^2}}$$

Where :

$\omega_c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter : the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

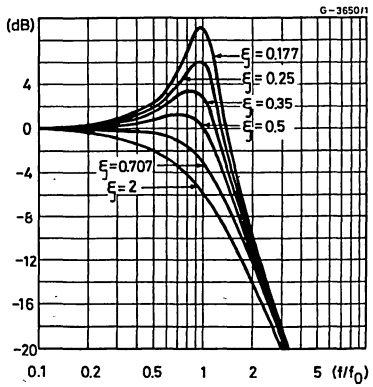
The higher order responses are obtained wit a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at Which G_v = – 3dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed R = R1 = R2, we have (see fig. 13)

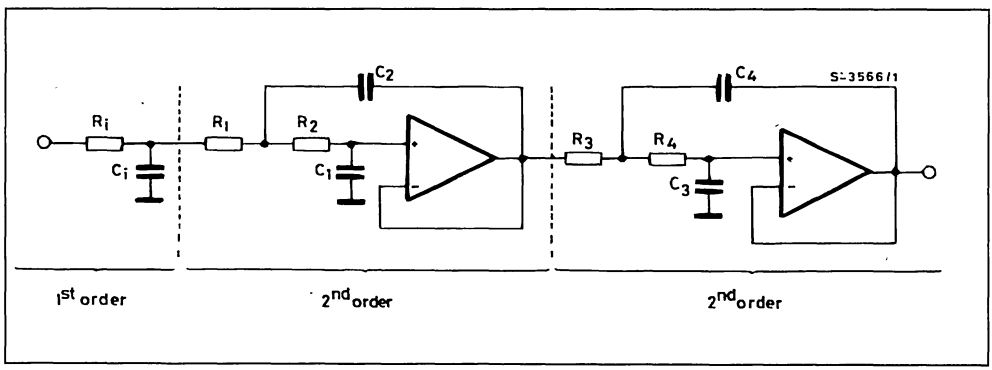
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4$ =10 KΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5 KHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1 nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5K\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2K\Omega$$

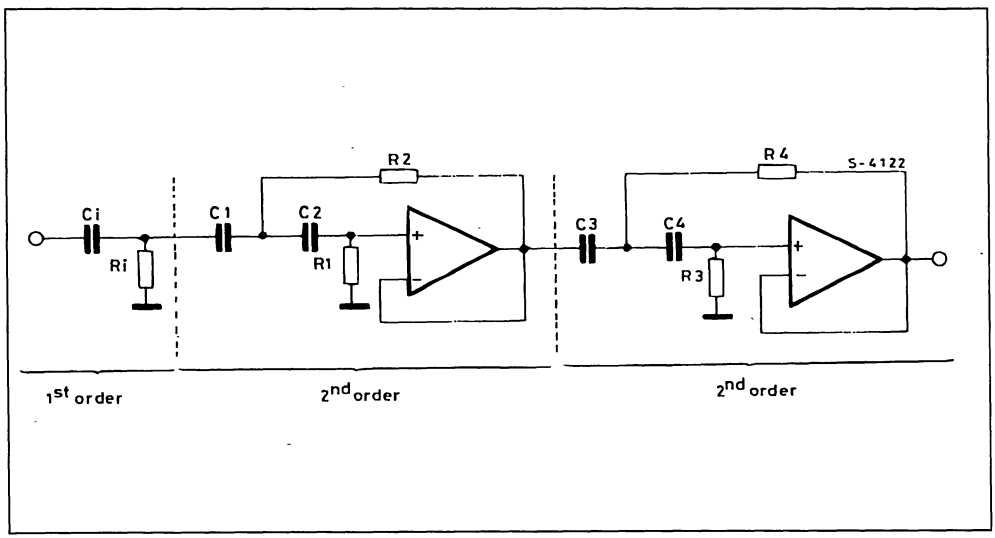
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103K\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6K\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters.

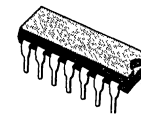
Order	C_I	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration.

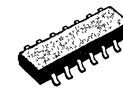


HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



DIP14
(Plastic 0.25)



SO-14J

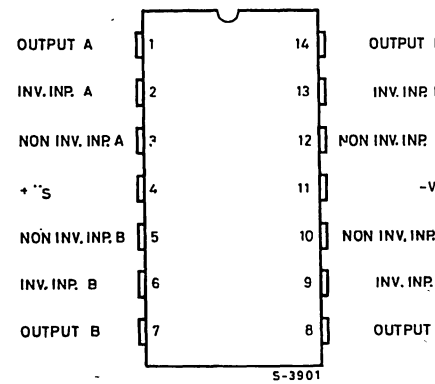
DESCRIPTION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.).

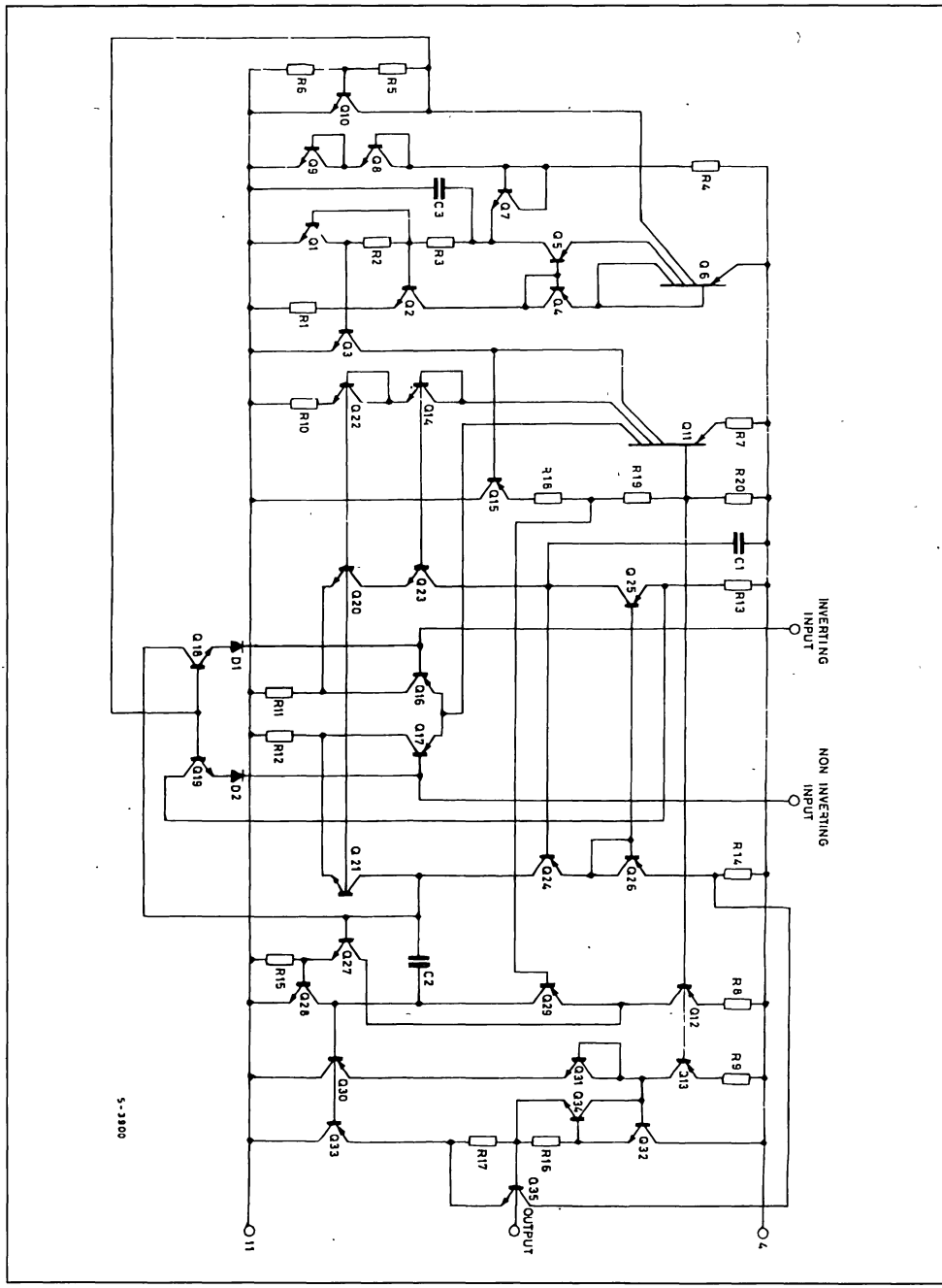
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

Type	DIP 14	SO-14
LS404	–	LS404D1
LS404C	LS404CB	LS404CD1



SCHEMATIC DIAGRAM (one section)



SGS-THOMSON MICROELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_s	Supply Voltage		± 18	V
V_i	Input Voltage	(positive) (negative)	+ V_s − V_s − 0.5	V
V_i	Differential Input Voltage		± (V_s − 1)	
T_{op}	Operating Temperature	**LS404** **LS404C**	− 25 to + 85 0 to + 70	°C °C
P_{tot}	Power Dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage Temperature		− 55 to + 150	°C

THERMAL DATA

			DIP 14	SO−14 J
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200°C/W	200°C/W

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = ± 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions		LS404			LS404C			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply Current				1.3	2		1.5	3	mA
I_b	Input Bias Current				50	200		100	300	nA
R_i	Input Resistance	f = 1 KHz			0.7	2.5		0.5	5	MΩ
V_{os}	Input Offset Voltage	R_g = 10 KΩ			1			1		mV
$\frac{\Delta V_{os}}{\Delta T}$	Input Offset Voltage Drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$			5			5		µV/°C
I_{os}	Input Offset Current				10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input Offset Current Drift	$T_{min} < T_{op} < T_{max}$			0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output Short Circuit Current				23			23		mA
G_v	Large Signal Open Loop Voltage Gain	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	90	100 95		86	100 95		dB
B	Gain-bandwidth Product	f = 20 KHz		1.8	3		1.5	2.5		MHz
e_N	Total Input Noise Voltage	f = 1 KHz R_g = 50 Ω R_g = 1 KΩ R_g = 10 KΩ			8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	Unity Gain R_L = 2 KΩ V_o = 2 V_{PP}	f = 1 KHz f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC Output Voltage Swing	R_L = 2 KΩ	V_s = ± 12 V V_s = ± 4 V	± 10	± 3		± 10	± 3		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	LS404			LS404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Large Signal Voltage Swing	f = 10 KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		V_{pp}
SR	Slew Rate	Unity Gain R_L = 2 KΩ	0.8	1.5			1		V/μs
CMR	Common Mode Rejection	V_i = 10 V	90	94		80	90		dB
SVR	Supply Voltage Rejection	V_i = 1 V f = 100 Hz	90	94		86	90		dB
CS	Channel Separation	f = 1 KHz	100	120			120		dB

Figure 1: Supply Current vs. Supply Voltage.

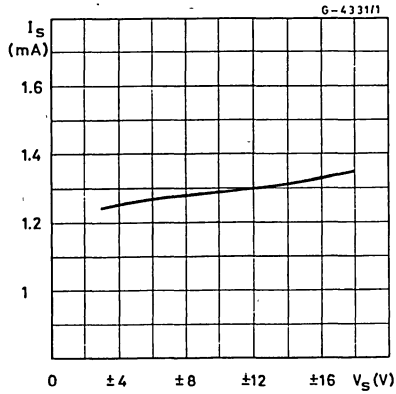


Figure 2 : Supply Current vs. Ambient Temperature.

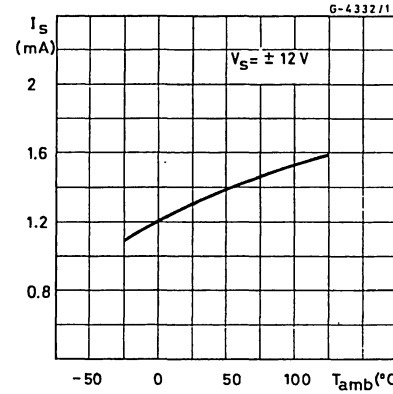


Figure 3 : Output Short Circuit Current vs. Ambient Temperature.

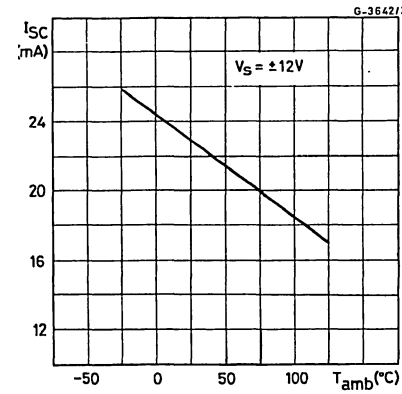


Figure 4: Open Loop Frequency and Phase Response.

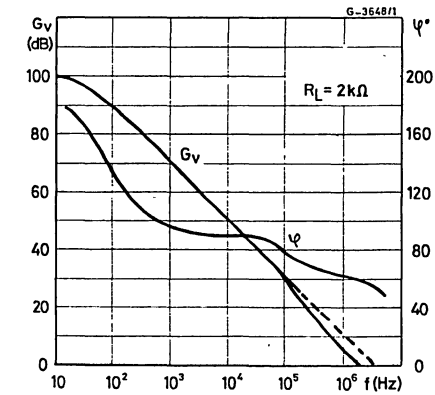


Figure 5: Open Loop Gain vs. Ambient Temperature.

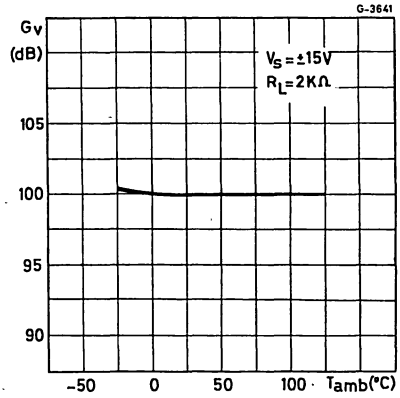


Figure 6 : Supply Voltage Rejection vs. Frequency.

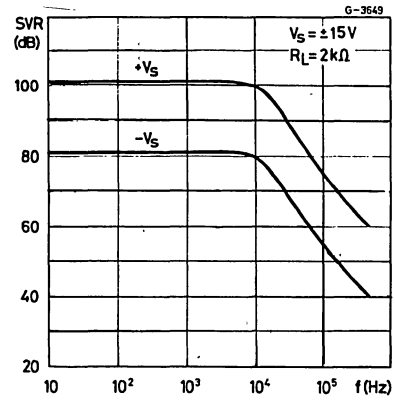


Figure 7 : Large Signal Frequency Response.

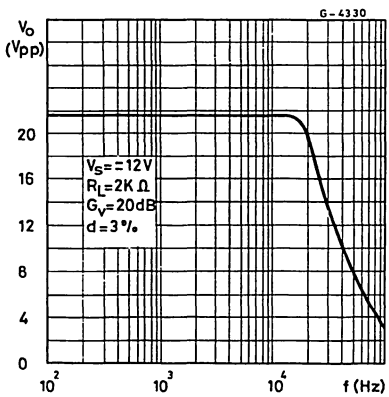


Figure 8 : Output Voltage Swing vs. Load Resistance.

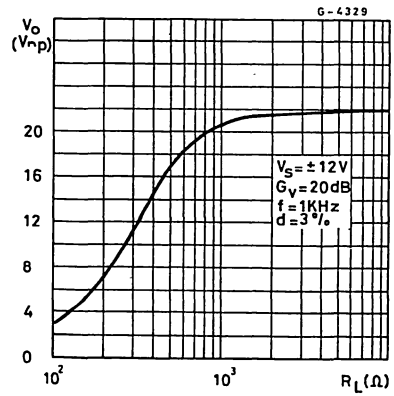
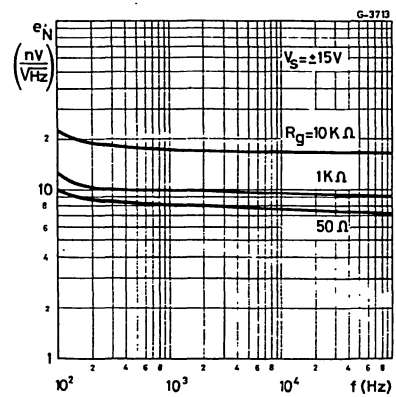


Figure 9 : Total Input Noise vs. Frequency.



APPLICATION INFORMATION

Active low-pass filter :

BUTTERWORTH

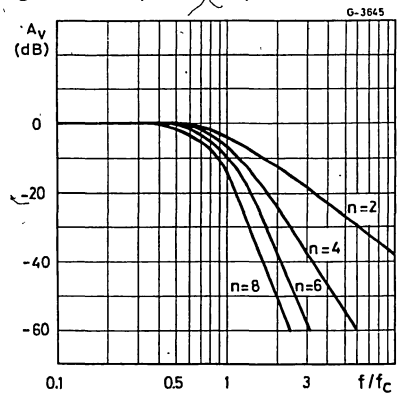
The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is - n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Figure 10 : Amplitude Response.



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

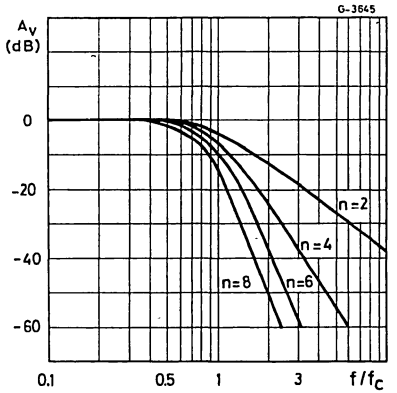
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the – 3 dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
– 3dB Frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs.
- Fast rise time.

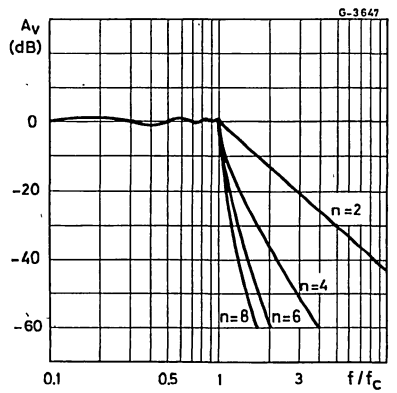
Figure 11 : Amplitude Response.



CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Figure 12 : Amplitude Response (± 1 dB ripple).



APPLICATION INFORMATION (continued)

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.

Increased ripple in the passband allows increased attenuation above the cutoff frequency.

The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

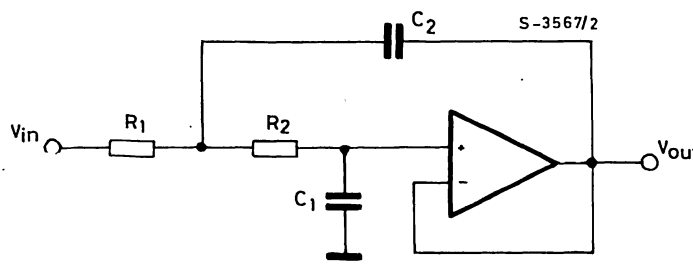
Other characteristics :
- Greater selectivity.
- Very nonlinear phase response.
- High overshoot response to step inputs.

The table below shows the typical overshoot and setting time response of the low pass filter to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
Butterworth	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	0.8/fc	1.4/fc	1.7/fc
	4	0.8	1.0/fc	1.8/fc	2.4/fc
	6	0.6	1.3/fc	2.1/fc	2.7/fc
	8	0.3	1.6/fc	2.3/fc	3.2/fc
Chebyschev (ripple ± 0.25dB)	2	11	1.1/fc	1.6/fc	–
	4	18	3.0/fc	5.4/fc	–
	6	21	5.9/fc	10.4/fc	–
	8	23	8.4/fc	16.4/fc	–
Chebyschev (ripple ± 1dB)	2	21	1.6/fc	2.7/fc	–
	4	28	4.8/fc	8.4/fc	–
	6	32	8.2/fc	16.3/fc	–
	8	34	11.6/fc	24.8/fc	–

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain op-amp).

Figure 13 : Filter Configuration.



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

Where :

$\omega c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

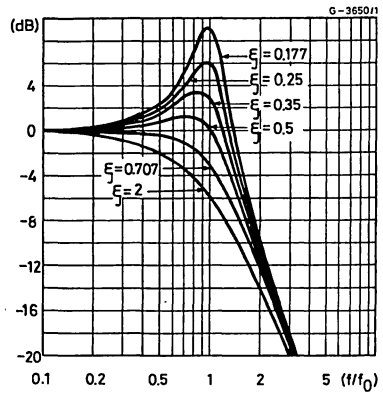
Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c). The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Table 1.

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which Phase Shift is – 90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which $G_V = -$ 3dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

Figure 14 : Filter Response vs. Damping Factor.



Fixed $R = R_1 = R_2$, we have (see fig. 13)

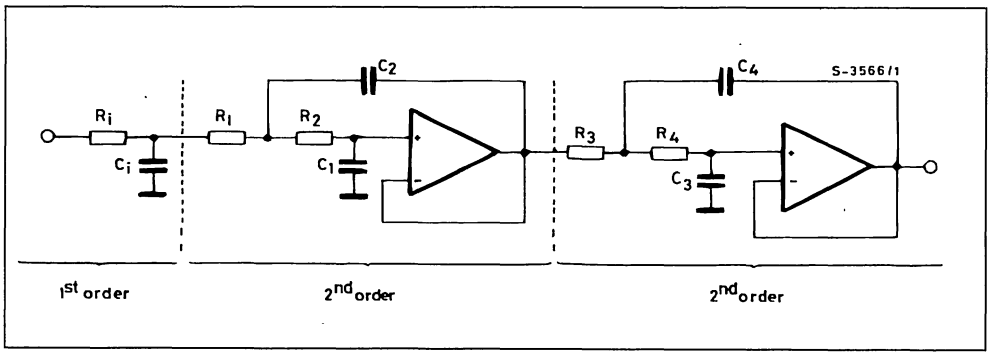
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE

Figure 15 : 5th Order Low Pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for $f_c = 3.4$ KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10$ KΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\text{nF}$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\text{ nF}$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\text{ nF}$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\text{ nF}$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\text{ nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For $f_c = 5$ KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1$ nF we obtain :

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\text{ KΩ}$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\text{ KΩ}$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\text{ KΩ}$$

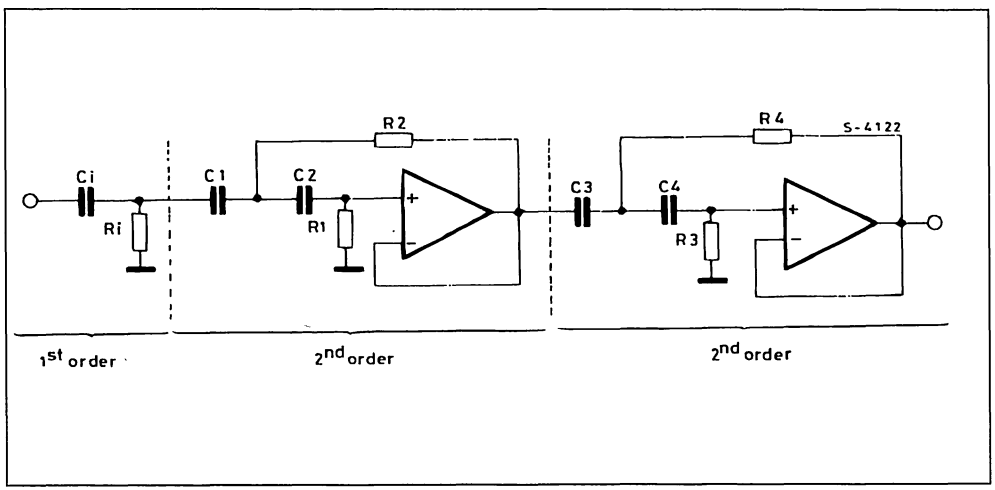
$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\text{ KΩ}$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\text{ KΩ}$$

Table II : Damping Factor for Low-pass Butterworth Filters.

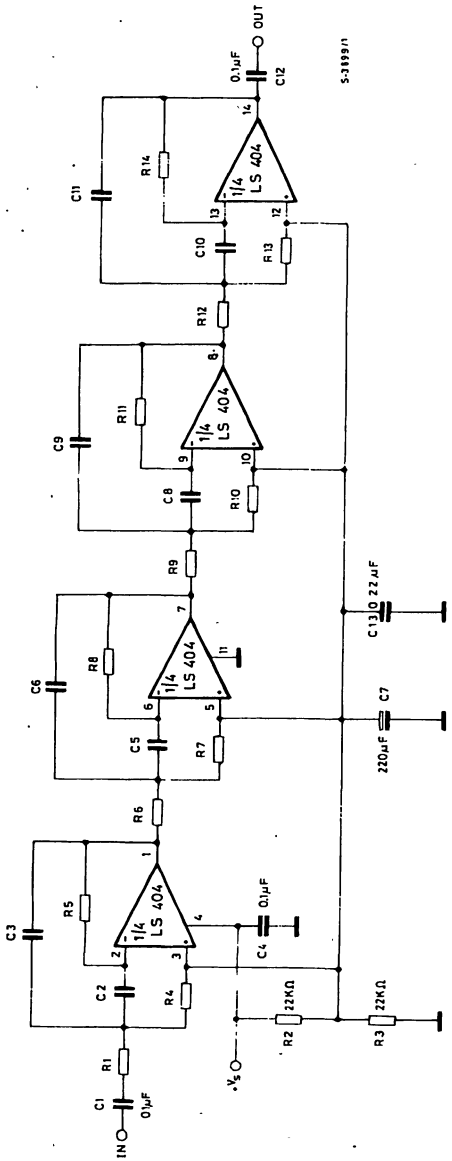
Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration.



APPLICATION INFORMATION (continued)

Figure 17 : Multiple Feedback 8-pole Bandpass Filter.



f_c = 1.180 Hz ; A = 1 ; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF ;
$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ ; $R_5 = R_8 = R_{11} = R_{14}$ = 330 KΩ ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3 KΩ

Figure 18 : Frequency Response of Band-pass Filter.

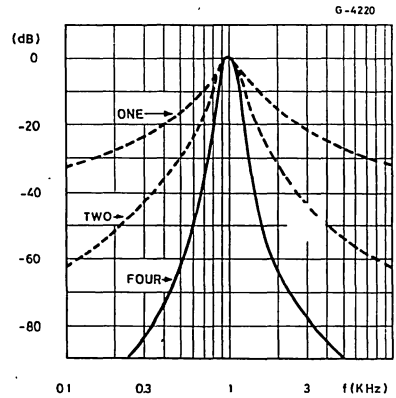


Figure 19 : Bandwidth of Band-pass Filter.

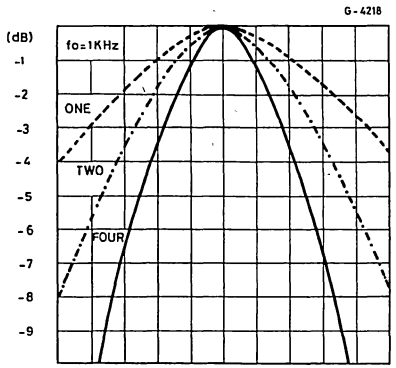
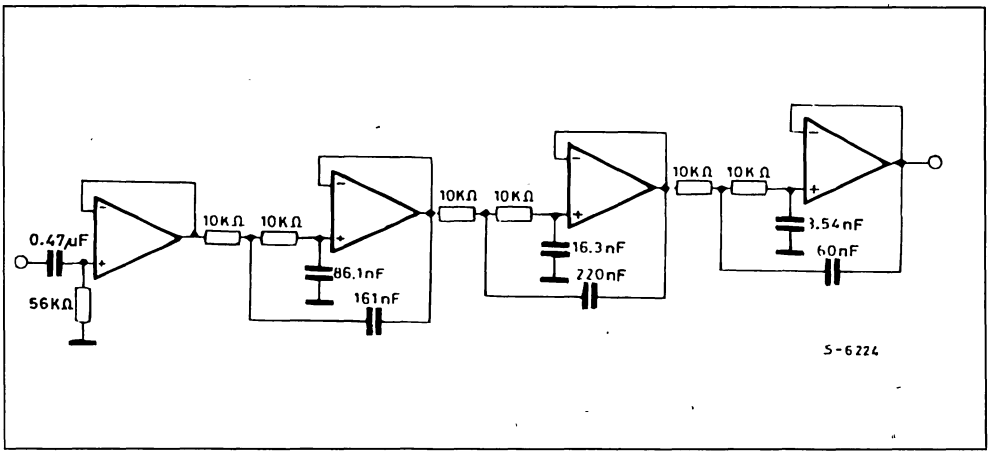
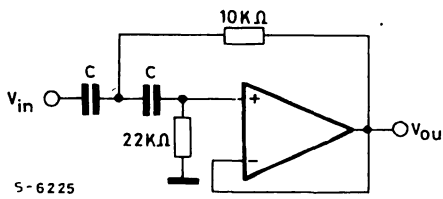


Figure 20 : Six-pole 355 Hz Low-pass Filter (chebychev type).



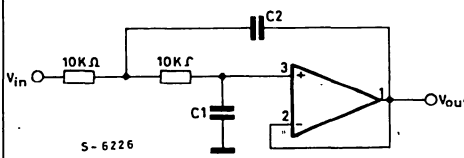
This is a 6-pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Figure 21 : Subsonic Filter (G_V = 0 dB).



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Figure 22 : High Cut Filter (G_V = 0 dB).



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

SGS-THOMSON MICROELECTRONICS

TEB1033
TEF1033 - TEC1033

BIPOLAR DUAL OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 µV/°C
- LONG TERM STABILITY : 8 µV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB1033 AND TEF1033 ARE PIN TO PIN REPLACEMENT OF THE LS204C AND LS204 RESPECTIVELY

N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB1033, TEF1033 and TEC1033 are high performance dual-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

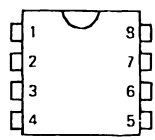
The circuits present very stable electrical characteristics over the entire supply voltage range.

ORDERING INFORMATION

Part Number	Temperature Range	Package		
		N	D	GC
TEB1033	0 °C to + 70 °C	•	•	
TEF1033	– 40 °C to + 105 °C	•	•	
TEC1033	– 55 °C to + 125 °C			•
Examples : TEB1033N, TEC1033GC				

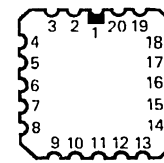
PIN CONNECTIONS (top views)

DIP8/SO8



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

LCC20

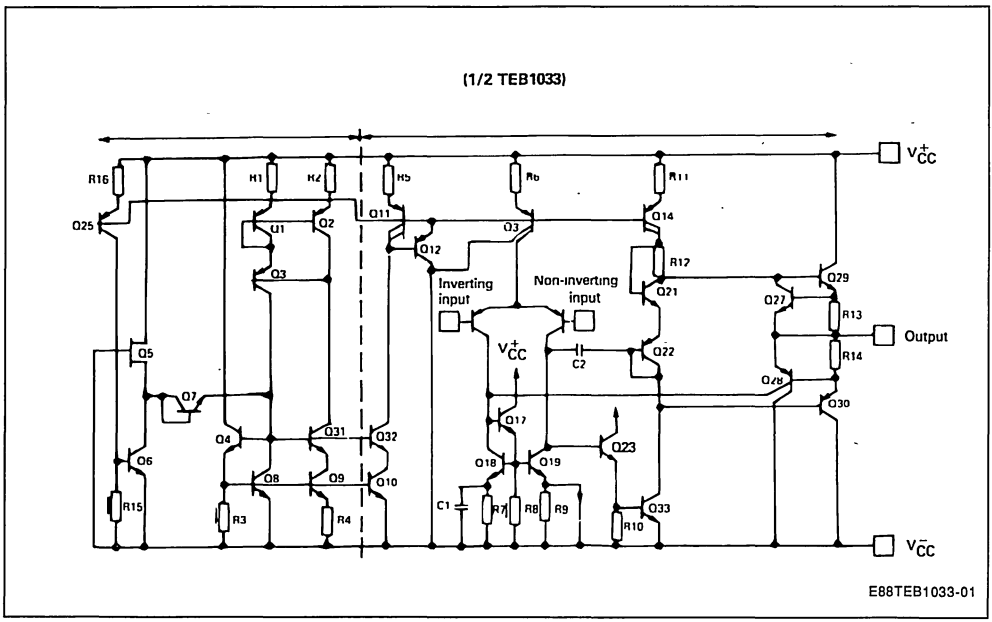


1 - NC
2 - Output 1
3 - NC
4 - NC
5 - Inverting input 1
6 - NC
7 - Non-inverting input 1
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Non-Inverting input 2
13 - NC
14 - NC
15 - Inverting Input 2
16 - NC
17 - Output 2
18 - NC
19 - NC
20 - V_{CC}^+

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		± 18	V
V_I	Input Voltage		± V_{CC}	V
V_{ID}	Differential Input Voltage		± (V_{CC} –1)	V
P_{tot}	Power Dissipation			mW
		TEB1033D, TEF1033D	400	
		TEB1033N	665	
		TEC1033GC	665	
T_{oper}	Operating Free-air Temperature Range			°C
		TEB1033	0 to + 70	
		TEF1033	– 40 to + 105	
		TEC1033	– 55 to + 125	
T_{stg}	Storage Temperature Range		– 55 to + 150	°C

BLOCK DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^+	V_{CC}^-	N. C.
DIP8 SO8	1, 7	2, 6	3, 5	8	4	
LCC20	2, 17	5, 15	7, 12	20	10	*

* **LCC20 :** Other pins are not connected.

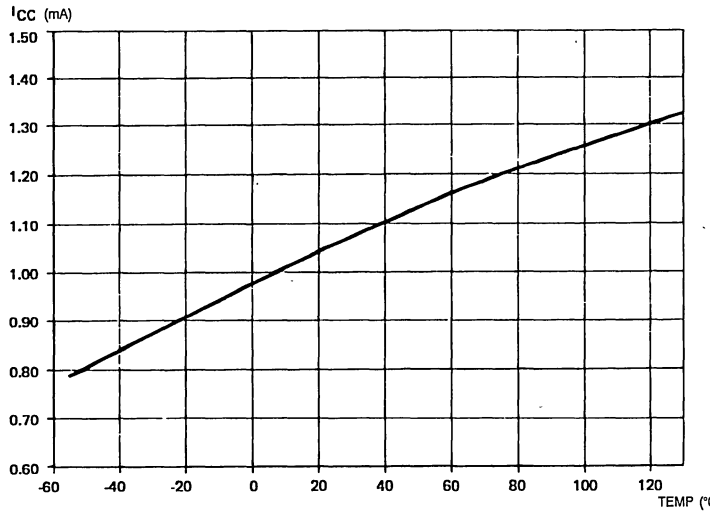
ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TEC 1033 : $-55 \leq T_{amb} \leq +125$ °C
TEF 1033 : $-40 \leq T_{amb} \leq +105$ °C
TEB 1033 : $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage T_{amb} = 25 °C (RS ≤ 10 kΩ) $T_{min} \leq T_{amb} \leq T_{max}$		0.3	1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		µV/°C
I_{IO}	Input Offset Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		5	20 40	nA
I_{IB}	Input Bias Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2 kΩ, $V_O = \pm 10$ V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 110		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$		1	1.5 2	mA
V_I	Input Voltage Range T_{amb} = 25 °C	− 12		+ 12	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ, $V_I = \pm 10$ V) T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 110		dB
I_{os}	Output Short-circuit Current T_{amb} = 25 °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10	 23	 40 40	mA
± V_{opp}	Output Voltage Swing T_{amb} = 25 °C R_L = 2 kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2 kΩ $V_{CC} = \pm 4$ V, R_L = 2 KΩ $V_{CC} = \pm 6$ V, R_L = 600 Ω	 13 12 2.8 4.6	 14 3		V
S_{vo}	Slew-rate ($V_I = \pm 10$ V, R_L = 2 kΩ, $C_L \leq 100$ pF, T_{amb} = 25 °C, unity gain)	0.6	1	3	V/µs
GBP	Gain Bandwidth Product (f = 100 KHz, T_{amb} = 25 °C, V_{IN} = 10 mV, R_L = 2 kΩ, C_L = 100 pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance (T_{amb} = 25 °C)		1		MΩ

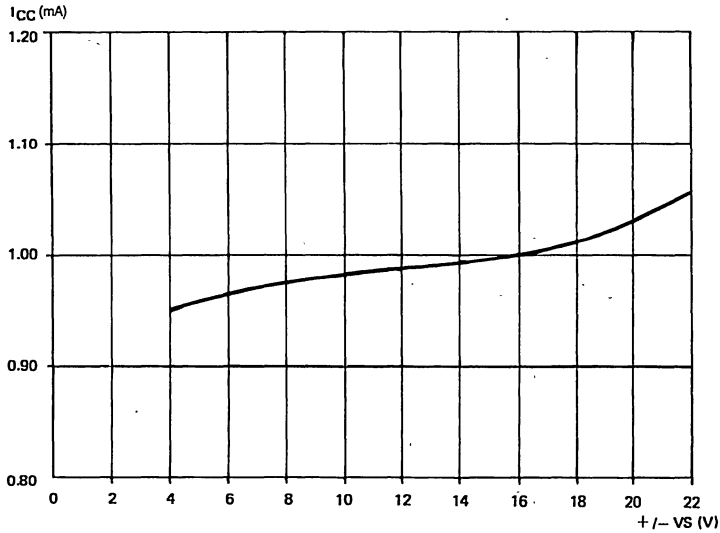
ELECTRICAL CHARACTERISTICS(continued)

Symbol	Parameter	TEB 1033 TEF 1033 TEC 1033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion (f = 1KHz, A_V = 20 dB, R_L = 2 kΩ $C_L \leq$ 100 pF, T_{amb} = 25 °C, V_o = 2 V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage (f = 1 KHz) R_S = 50 Ω R_S = 1 kΩ R_S = 10 kΩ		 8 10 18	15	nV/√Hz
V_{OPP}	Large Signal Voltage Swing R_L =10 kΩ, f = 10 KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



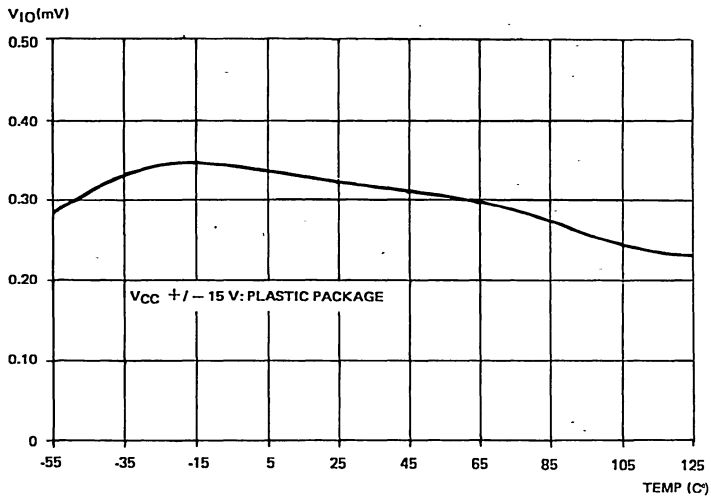
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB1033-02



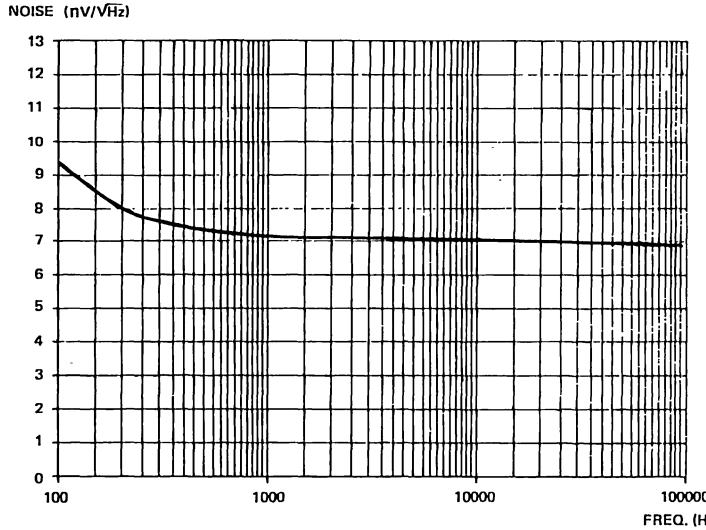
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB1033-03



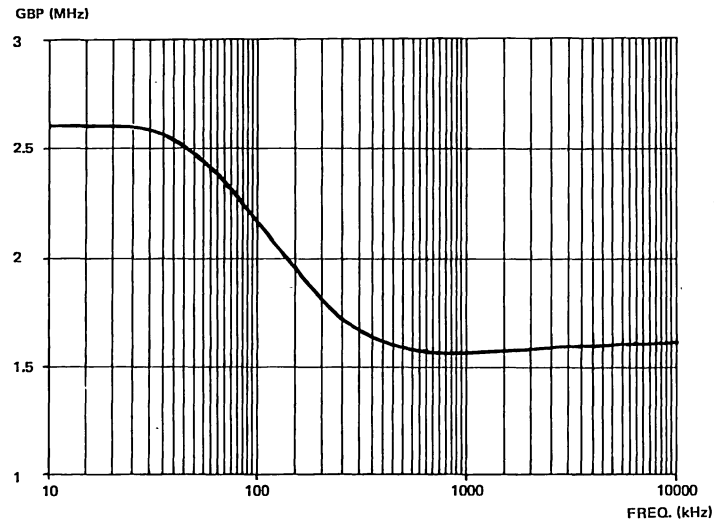
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB1033-04



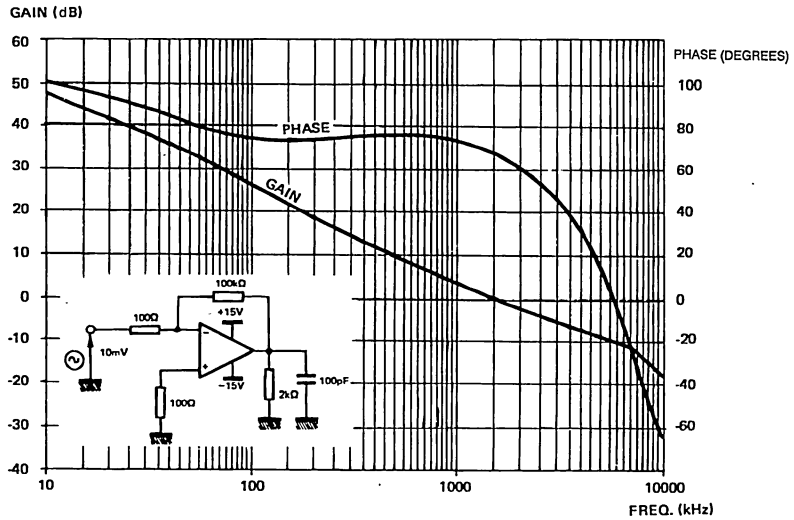
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB1033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

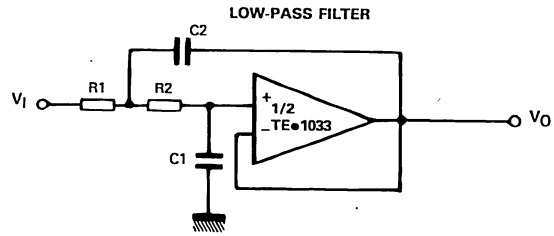
E88TEB1033-06



BODE PLOT

E88TEB1033-07

TYPICAL APPLICATION



E88TEB1033-08

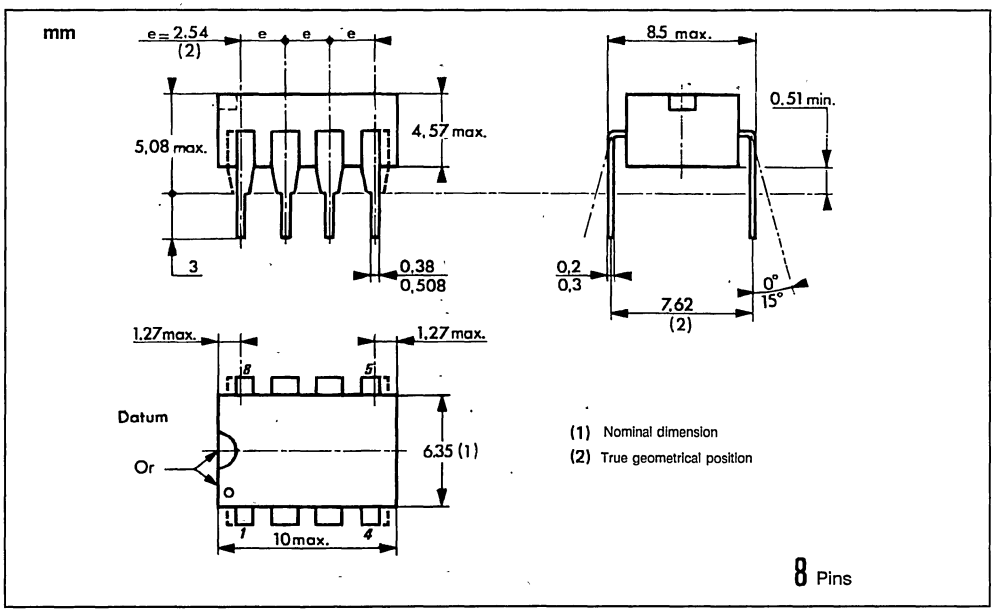
$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi \frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\omega_c = 2\pi f_c$, with f_c = cutt-off frequency

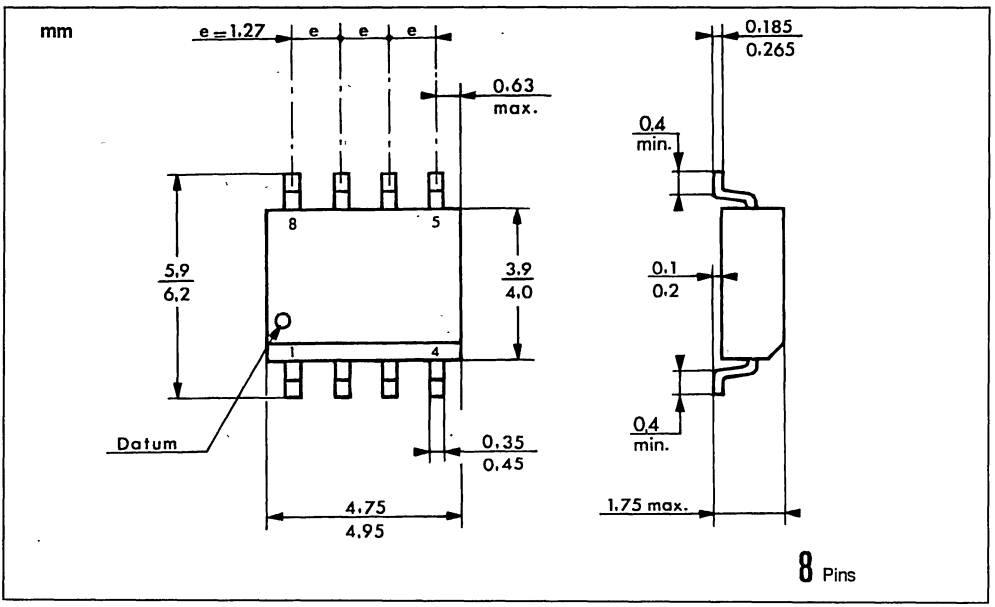
ξ = damping factor

PACKAGE MECHANICAL DATA

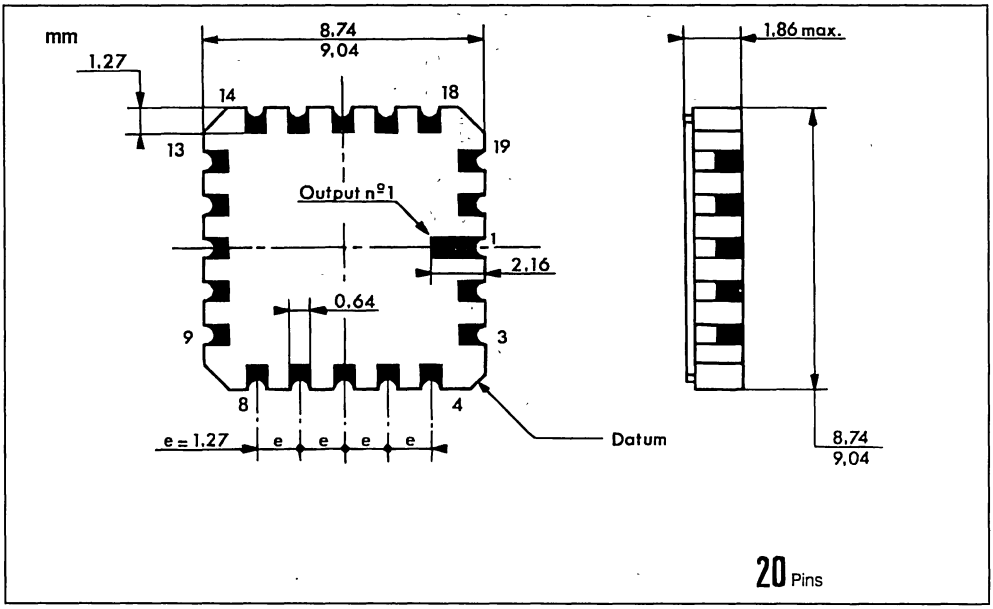
8 PINS – PLASTIC DIP



8 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)

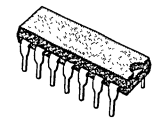


SGS-THOMSON MICROELECTRONICS

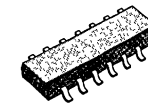
TEB4033
TEF4033 - TEC4033

BIPOLAR QUAD OPERATIONAL AMPLIFIERS

- LOW DISTORTION RATIO
- LOW NOISE
- VERY LOW SUPPLY CURRENT
- LOW INPUT OFFSET CURRENT
- VERY LOW INPUT OFFSET VOLTAGE
- LARGE COMMON-MODE RANGE
- HIGH GAIN
- HIGH OUTPUT CURRENT
- GAIN-BANDWIDTH PRODUCT : 2.5 MHz
- TEMPERATURE DRIFT : 2 µV/°C
- LONG TERM STABILITY : 8 µV/YEAR (for $T_{amb} \leq 50$ °C)
- THE TEB4033 AND TEF4033 ARE PIN TO PIN REPLACEMENT OF THE LS404C AND LS404 RESPECTIVELY



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

J
CERDIP14
(Cerdip Package)

GC
LCC20
(Tricecop (LCC))

DESCRIPTION

The TEB4033, TEF4033 and TEC4033 are high performance quad-operational amplifiers intended for active filter applications. The internal phase compensation allows stable operation as voltage follower in spite of their high gain-bandwidth products.

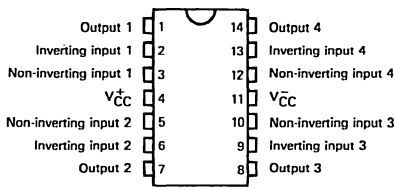
The circuits present very stable electrical characteristics over the entire supply voltage range.

ORDERING INFORMATION

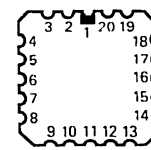
Part Number	Temperature Range	Package		
		N	D	GC
TEB4033	0 °C to + 70 °C	•	•	
TEF4033	– 40 °C to + 105 °C	•	•	
TEC4033	– 55 °C to + 125 °C			•
Examples : TEB4033N, TEC4033GC				

PIN CONNECTIONS (top views)

DIP14/CERDIP14
SO14



LCC20

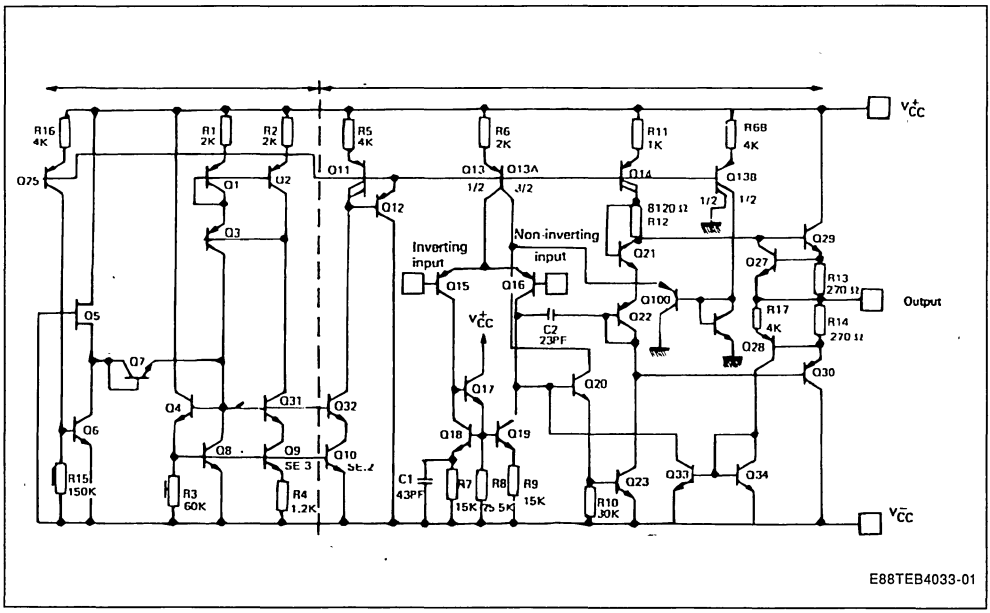


1 - NC
2 - Output 1
3 - Inverting input 1
4 - Non-inverting input 1
5 - NC
6 - V_{CC}^{-}
7 - NC
8 - Non-inverting input 2
9 - Inverting input 2
10 - Output 2
11 - NC
12 - Output 3
13 - Inverting input 3
14 - Non-inverting input 3
15 - NC
16 - V_{CC}^{+}
17 - NC
18 - Non-inverting input 4
19 - Inverting input 4
20 - Output 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 18	V
V_I	Input Voltage	± V_{CC}	V
V_{ID}	Differential Input Voltage	± (V_{CC} –1)	V
P_{tot}	Power Dissipation		mW
	TEB4033D, TEF4033D	400	
	TEB4033N, TEF4033N	665	
	TEC4033GC	665	
T_{oper}	Operating Free-air Temperature Range		°C
	TEB4033	0 to + 70	
	TEF4033	– 40 to + 105	
	TEC4033	– 55 to + 125	
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

BLOCK DIAGRAM



Case	Outputs	Inverting Inputs	Non-inverting Inputs	V_{CC}^{+}	V_{CC}^{-}	N. C.
DIP14 CERDIP14 SO14	1, 7 8, 14	2, 6 9, 13	3, 5 10, 12	4	11	
LCC20	2, 10 12, 20	3, 9 13, 19	4, 8 14, 18	6	16	*

* **LCC20 :** Other pins are not connected.

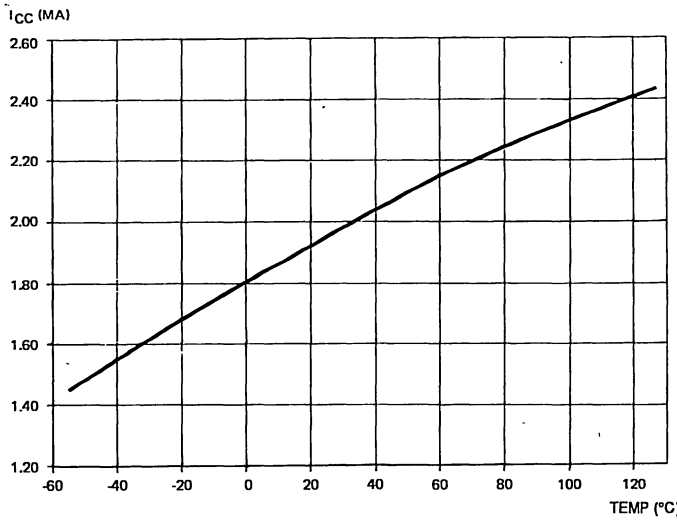
ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15$ V (unless otherwise specified)
TEC 4033 : $-55 \leq T_{amb} \leq +125$ °C
TEF 4033 : $-40 \leq T_{amb} \leq +105$ °C
TEB 4033 : $0 \leq T_{amb} \leq +70$ °C

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage $T_{amb} = 25$ °C ($R_S \leq 10$ kΩ) $T_{min} \leq T_{amb} \leq T_{max}$		0.3	1 3	mV
DV_{IO}	Input Offset Voltage Drift		2		µV/°C
I_{IO}	Input Offset Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		5	20 40	nA
I_{IB}	Input Bias Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		50	100 200	nA
A_{vd}	Large Signal Voltage Gain ($R_L = 2$ kΩ, $V_O = \pm 10$ V) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 300		V/mV
SVR	Supply Voltage Rejection Ratio DV_{CC} from ± 15 V to ± 4 V $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 110		dB
I_{CC}	Supply Current, all Amp, no Load $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$		2	3 4	mA
V_I	Input Voltage Range $T_{amb} = 25$ °C	− 12		+ 12	V
CMR	Common Mode Rejection Ratio ($R_S \leq 10$ kΩ, $V_I = \pm 10$ V) $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 100 100	 110		dB
Ios	Output Short-circuit Current $T_{amb} = 25$ °C $T_{min} \leq T_{amb} \leq T_{max}$	 10 10	 23	 40 40	mA
$\pm V_{opp}$	Output Voltage Swing $T_{amb} = 25$ °C $R_L = 2$ kΩ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 2$ kΩ $V_{CC} = \pm 4$ V, $R_L = 2$ kΩ $V_{CC} = \pm 6$ V, $R_L = 600$ Ω	 13 12 2.8 4.6	 14 3		V
S_{vo}	Slew-rate ($V_I = \pm 10$ V, $R_L = 2$ kΩ $C_L \leq 100$ pF, $T_{amb} = 25$°C, unity gain)	0.6	1	3	V/µs
GBP	Gain Bandwidth Product (f = 100 KHz, $T_{amb} = 25$ °C, $V_{IN} = 10$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF)	1.8	2.5	3.2	MHz
R_I	Input Resistance ($T_{amb} = 25$ °C)		1		MΩ

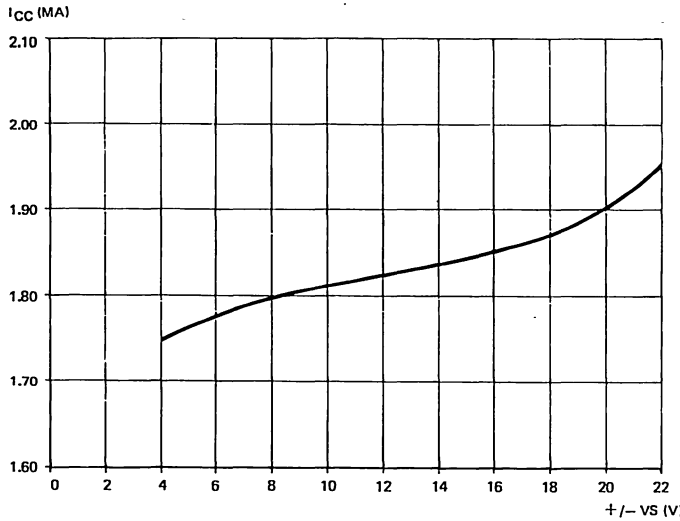
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	TEB 4033 TEF 4033 TEC 4033			Unit
		Min.	Typ.	Max.	
THD	Total Harmonic Distortion ($f = 1KHz$, $A_v = 20$ dB, $R_L = 2$ kΩ $C_L \leq 100$ pF, $T_{amb} = 25$ °C, $V_o = 2$ V_{pp})		0.008	0.05	%
V_n	Equivalent Input Noise Voltage ($f = 1$ KHz) $R_S = 50$ Ω $R_S = 1$ kΩ $R_S = 10$ kΩ		 8 10 18	 15	 $nV/\sqrt{Hz}$
V_{OPP}	Large Signal Voltage Swing $R_L = 10$ kΩ, $f = 10$ KHz	26	28		V
φM	Phase Margin		45		Degrees
V_{o1}/V_{o2}	Channel Separation	100	120		dB



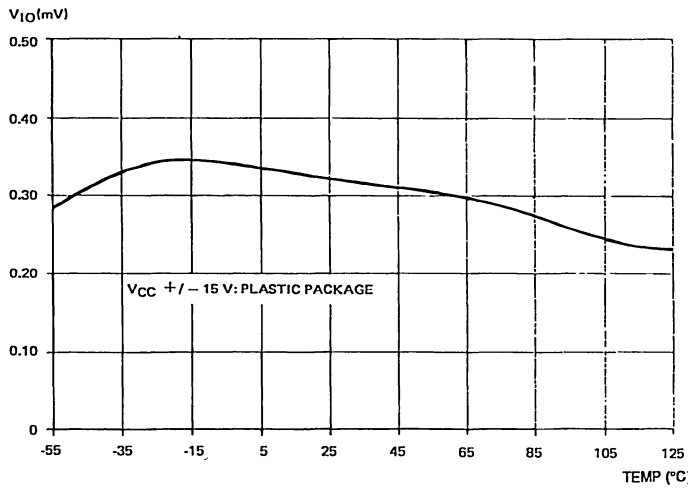
SUPPLY CURRENT VS. AMBIENT TEMPERATURE

E88TEB4033-02



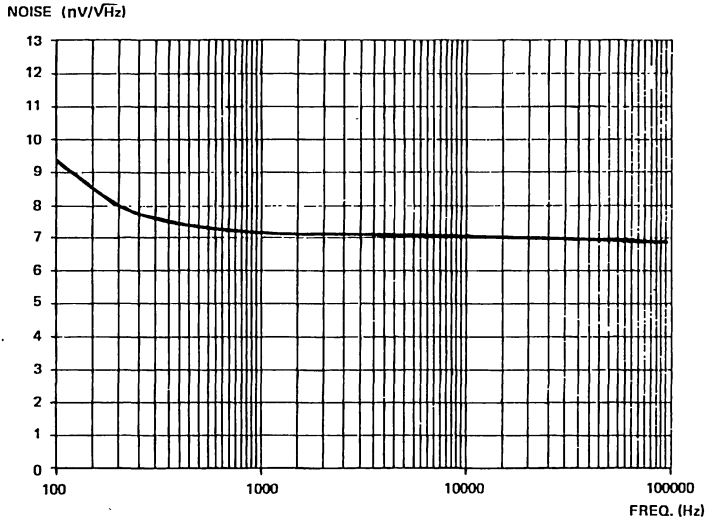
SUPPLY CURRENT VS. SUPPLY VOLTAGE

E88TEB4033-03



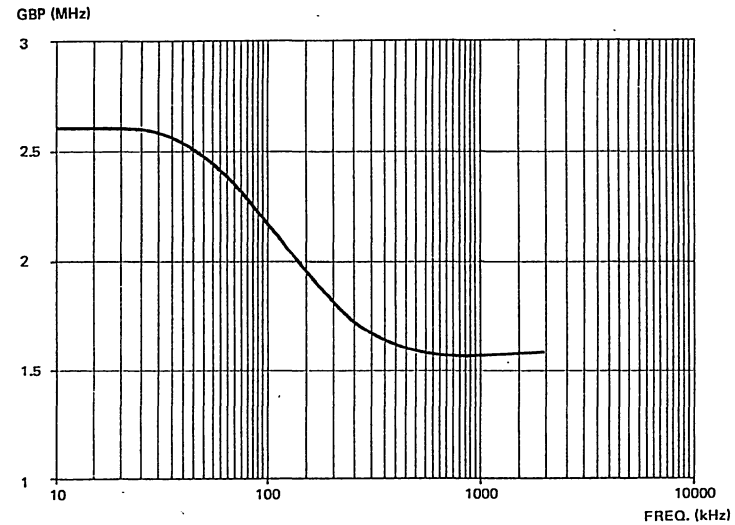
OFFSET VOLTAGE VS. AMBIENT TEMPERATURE

E88TEB4033-04



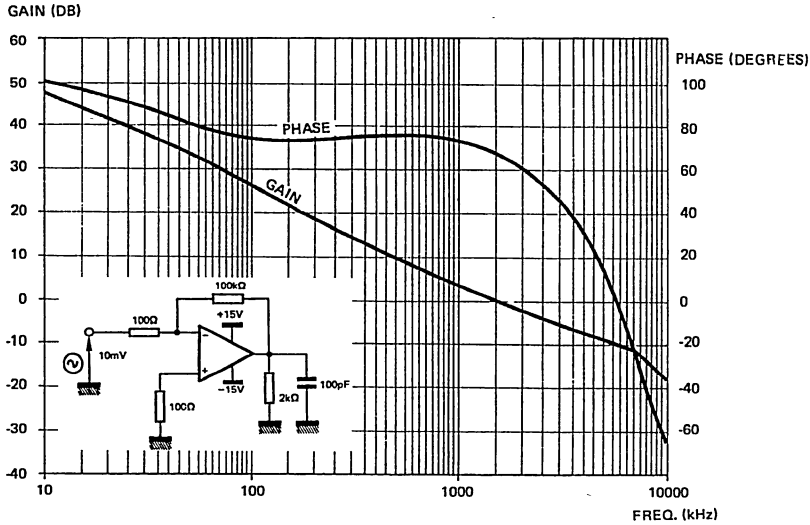
TOTAL INPUT NOISE VS. FREQUENCY

E88TEB4033-05



GAIN BANDWIDTH PRODUCT VS. FREQUENCY

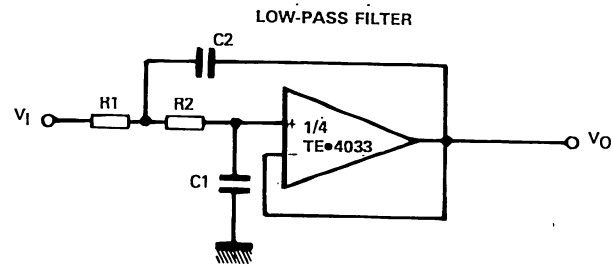
E88TEB4033-06



BODE PLOT

E88TEB4033-07

TYPICAL APPLICATION



E88TEB4033-08

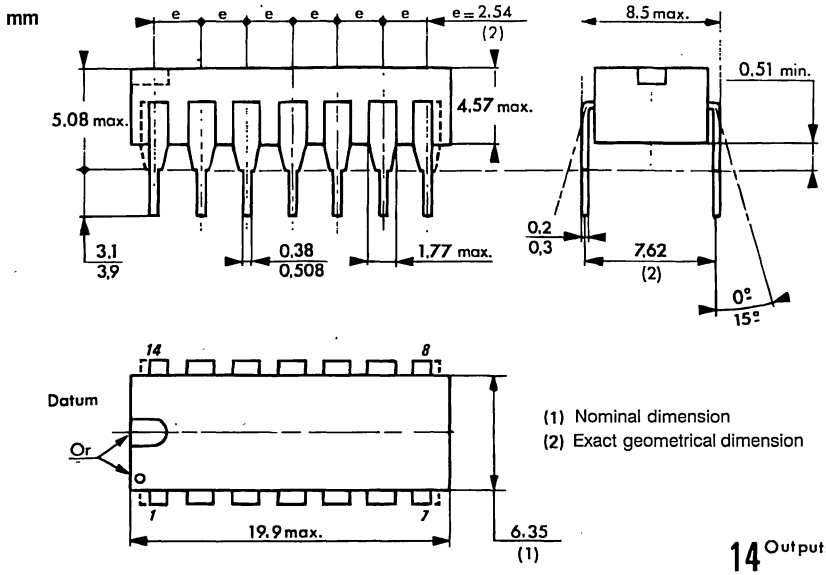
$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

$\omega_c = 2\pi f_c$, with f_c = cutt-off frequency

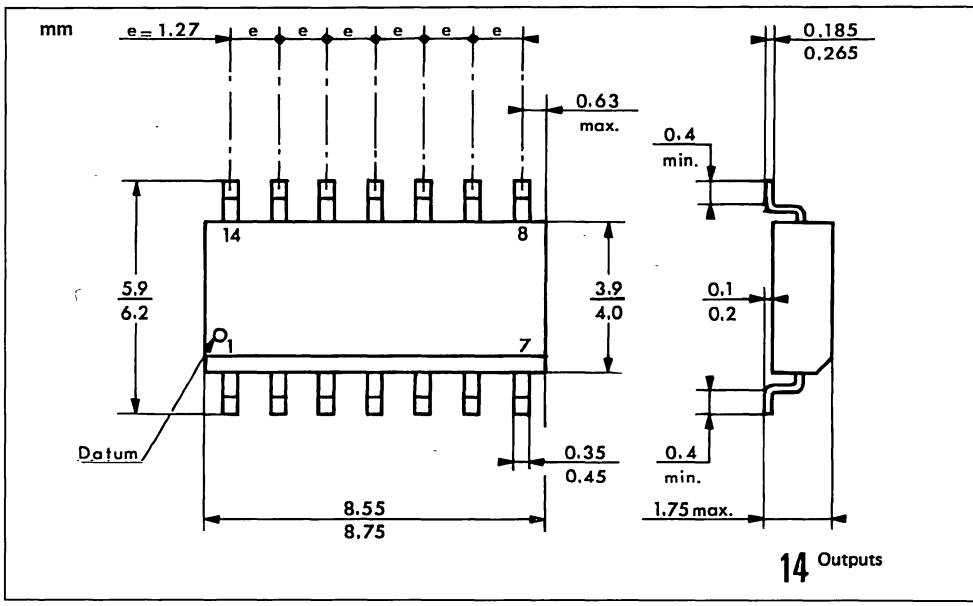
ξ = damping factor

PACKAGE MECHANICAL DATA

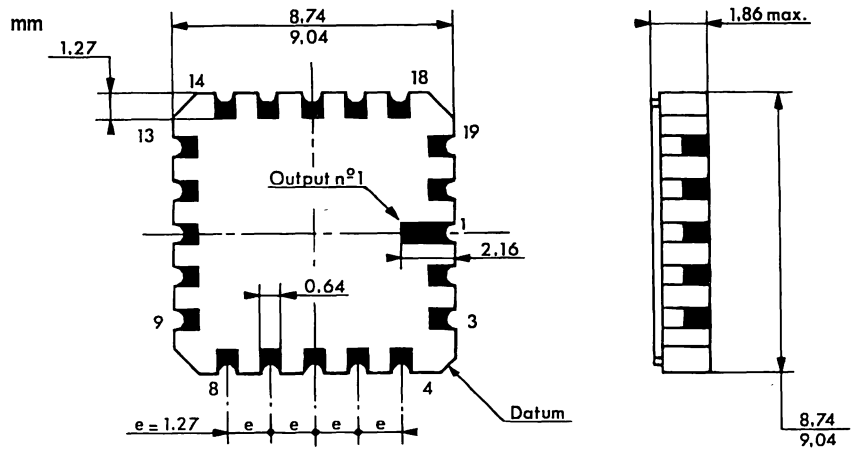
14 PINS – PLASTIC DIP OR CERDIP



14 PINS – PLASTIC MICROPACKAGE (SO)



20 PINS – TRICECOP (LCC)

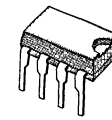


SGS-THOMSON MICROELECTRONICS

TS271

CMOS SINGLE OPERATIONAL AMPLIFIERS

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{set}
- VERY LARGE I_{set} RANGE
- PIN COMPATIBLE TO SINGLE OPERATIONAL AMPLIFIER (UA776)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



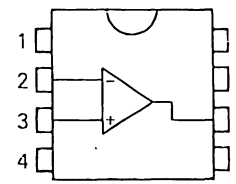
N
DIP8
(Plastic Package)

J
CERDIP8
(Cerdip Package)

D
SO8
(Plastic Micropackage)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS271-01

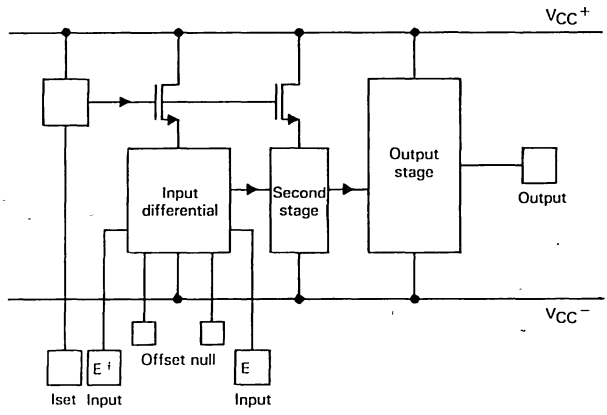
1 – Offset null 1
2 – Inverting input
3 – Non-inverting input
4 – V_{CC}^-
5 – Offset null 2
6 – Output
7 – V_{CC}^+
8 – I_{set}

DESCRIPTION

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.
The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and the consumption can be minimized according to the needed speed. These devices are specified for the following I_{set} current values : 1.5 µA, 25 µA, 130 µA.

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

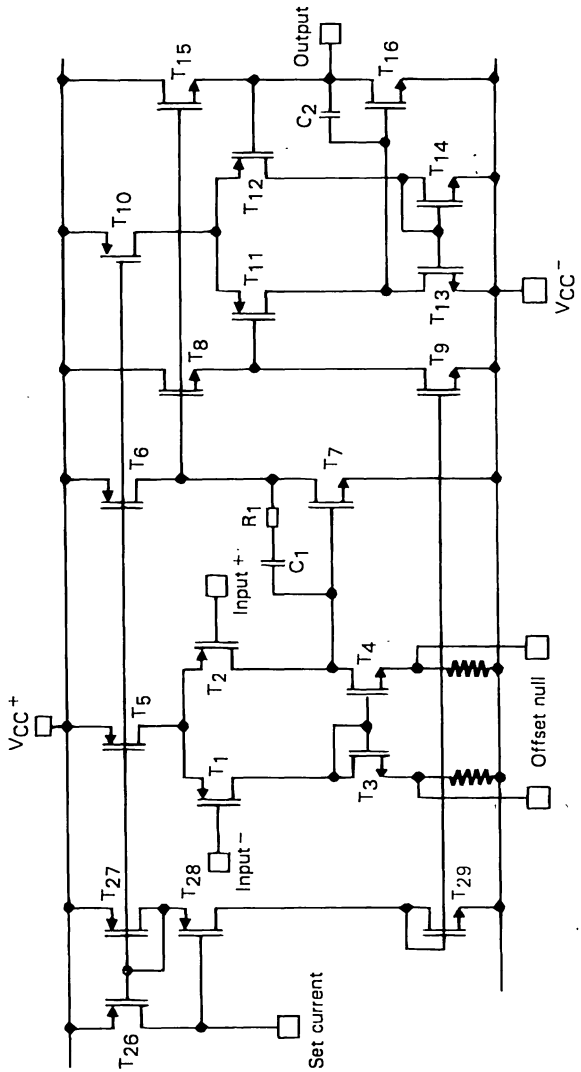
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	12	V
V_{id}	Differential Input Voltage (note 2).	± 12	V
V_i	Input Voltage (note 3)	- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature TS271C TS271I TS271M	0 to 70 - 40 to 105 - 55 to 125	°C
T_{stg}	Storage Temperature	- 65 to 150	°C
I_{set}	I_{set} Range	1 to 200	µA

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

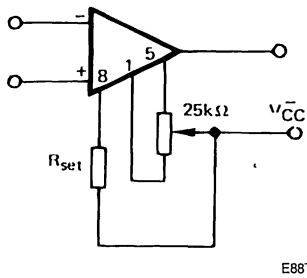
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common-mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM



E88TS271-03

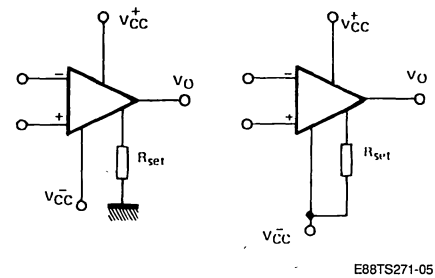
OFFSET VOLTAGE NULL CIRCUIT



E88TS271-04

OFFSET COMPENSATION GUARANTEED FOR TS271BCX (I_{set} > 25 µA), TS271ACX (I_{set} > 90 µA)

RESISTOR BIASING

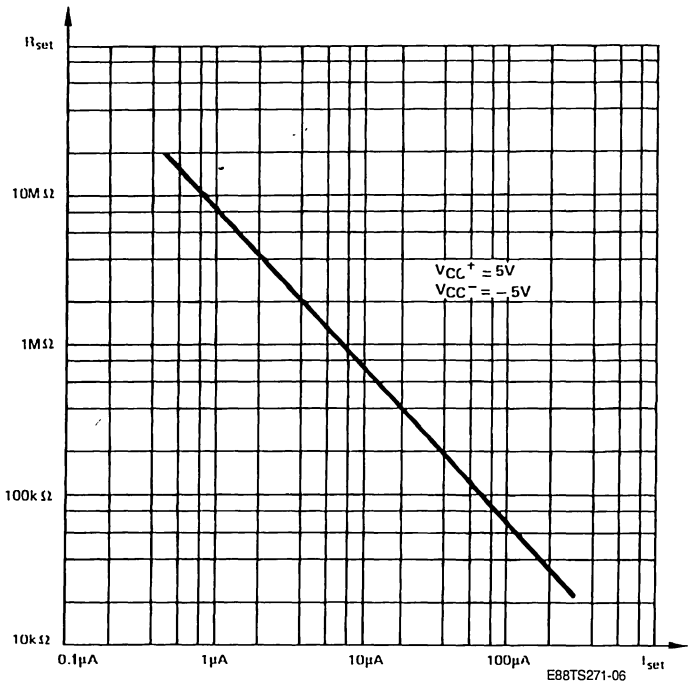


E88TS271-05

R_{set} CONNECTED TO GROUND

R_{set} CONNECTED TO V_{CC}^- (R_{set} VALUE : SEE FIG. 1)

Figure 1 : R_{set} Connected to V_{CC}^-.



E88TS271-06

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 1.5 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 mΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 1 mΩ $T_{min} < T < T_{max}$	30 20	100		30 20	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V, V_i = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 10 pF C_L = 100 pF		 35 10			 35 10		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 40 70			 40 70		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S = 10 Ω		70			70		nV/√Hz

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 25 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100KΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 100 KΩ $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 KΩ C_L = 100 pF fin = 100 KHz		0.7			0.7		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V , V_i = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 KΩ C_L = 10 pF C_L = 100 pF		 50 30			 50 30		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 30 50			 30 50		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S =10 Ω		38			38		nV/√Hz

Note : 1. Low output voltage is less than 50mV.

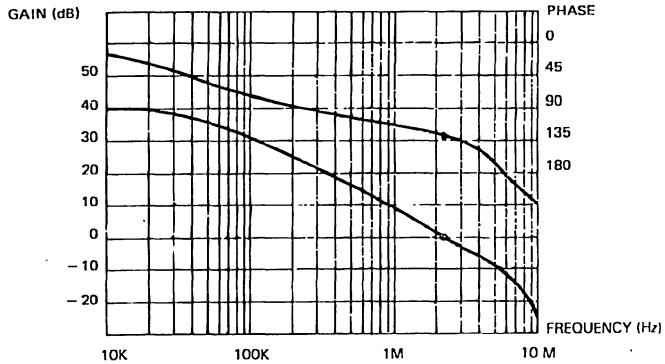
ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 130 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 KΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 KΩ C_L = 100 pF fin = 200 KHz		2.3			2.3		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V, V_i = 5 V $T_{min} < T < T_{max}$		800	1300 1400		800	1300 1500	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		4.5			4.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 KΩ C_L = 10 pF C_L = 100 pF		 56 56			 56 56		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 30 30			 30 30		%
V_n	Input Equivalent Noise Voltage F =1 KHz R_S = 10 Ω		30			30		nV/√Hz

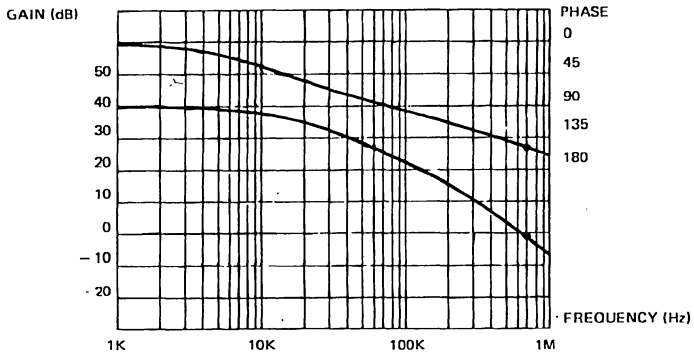
Note : 1. Low output voltage is less than 50mV.

I_{set} = 130 µA



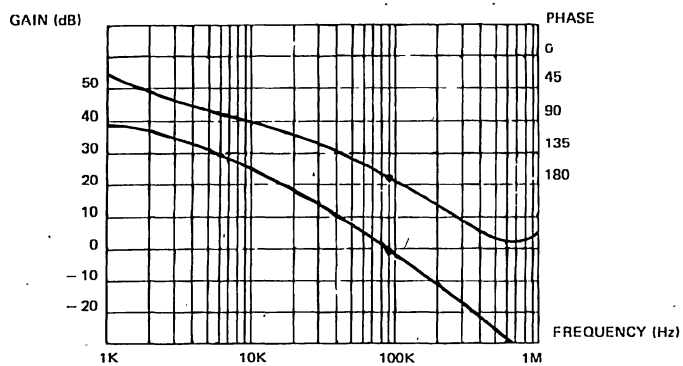
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 10$ KΩ, $C_L = 100$ pF, $T_{amb} = 25°C$ E88TS271-07

I_{set} = 25 µA



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 100$ KΩ, $C_L = 100$ pF, $T_{amb} = 25°C$ E88TS271-08

I_{set} = 1.5 µA



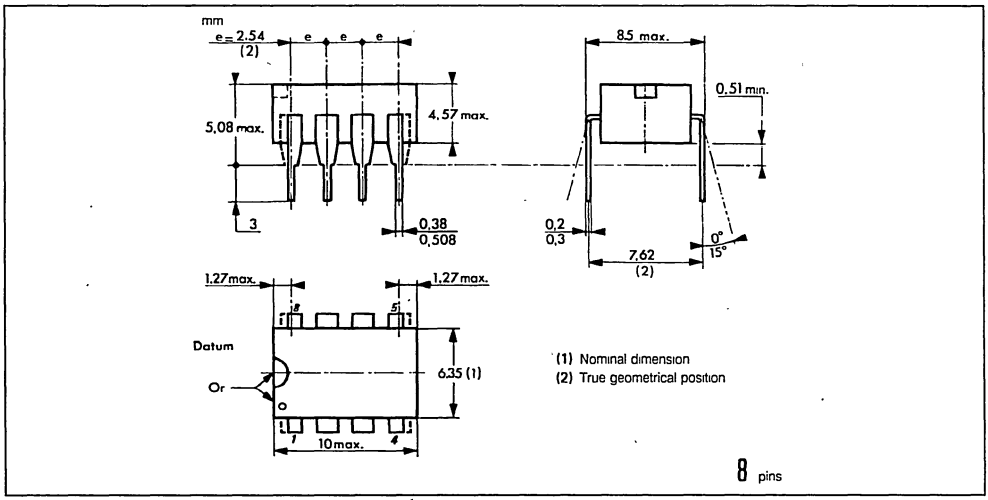
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 1$ MΩ, $C_L = 100$ pF, $T_{amb} = 25°C$ E88TS271-09

ORDERING INFORMATION

Part Number	Temperature Range °C	Package		
		N	D	J
TS271C	0 to + 70	•	•	
TS271AC	0 to + 70	•	•	
TS271BC	0 to + 70	•	•	
TS271I	- 40 to + 105	•	•	
TS271M	- 55 to + 125			•
TS271AI	- 40 to + 105	•	•	
TS271AM	- 55 to + 125			•
TS271BI	- 40 to + 105	•	•	
TS271BM	- 55 to + 125			•
Examples : TS271 ACN, TS271 CD				

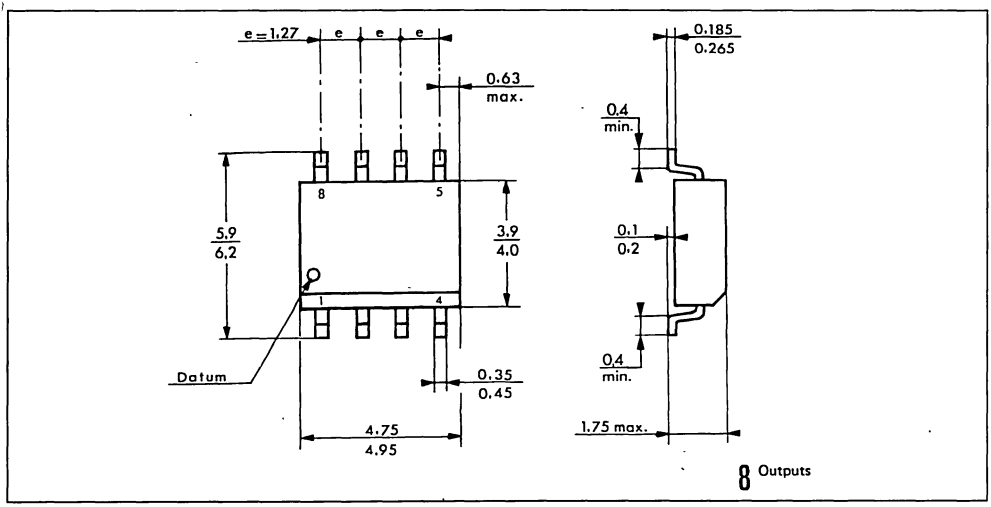
PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

8 PINS – PLASTIC MICROPACKAGE SO

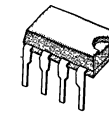


SGS-THOMSON MICROELECTRONICS

TS272
TS27M2/TS27L2

CMOS DUAL OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITANCE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS272
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD DUAL OPERATIONAL AMPLIFIERS (TL082 - LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



N
DIP8
(Plastic package)

J
CERDIP8
(Cerdip package)

D
SO8
(Plastic micropackage)

(Ordering Information at the end of the datasheet)

DESCRIPTION

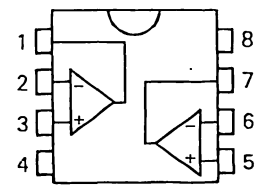
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- I_{CC} = **10 µA** per amplifier : TS27L2 (Low bias versions)
- I_{CC} = **150 µA** per amplifier : TS27M2 (Medium bias versions)
- I_{CC} = **1 mA** per amplifier : TS272 (High bias versions)

The input impedance is similar to the J-FET input impedance. Very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

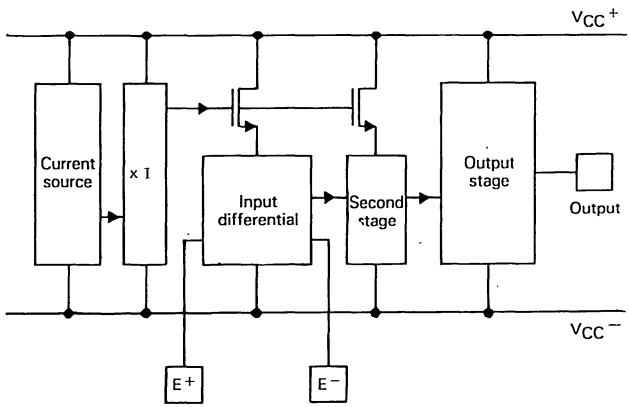
PIN CONNECTIONS (top view)



E88TS272-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

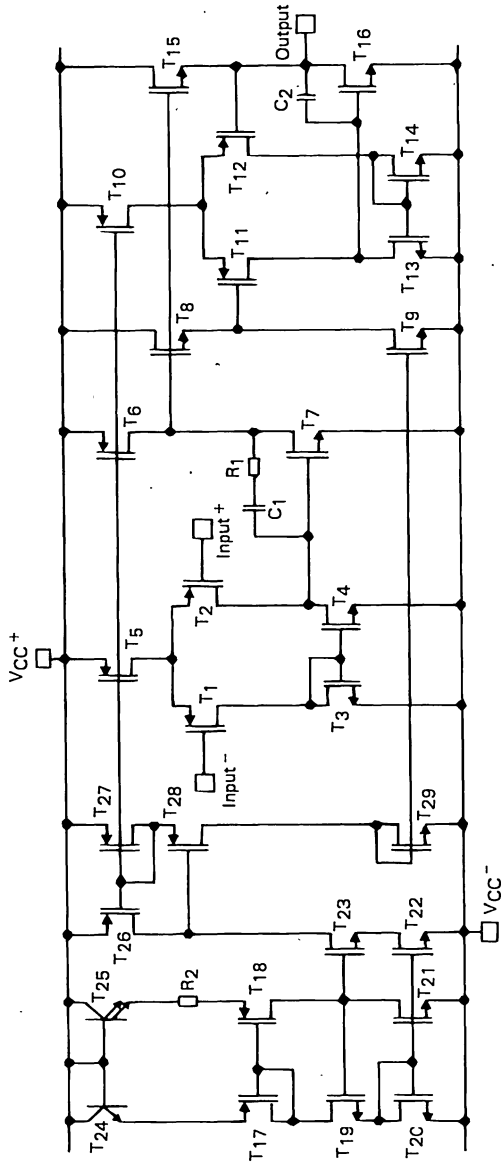
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	12	V
V_{id}	Differential Input Voltage (note 2)	± 12	V
V_i	Input Voltage (note 3)	− 0.3 to 12	V
T_{oper}	Operating Free-air Temperature TS272C TS272I TS272M TS27M2C TS27M2I TS27M2M TS27L2C TS27L2I TS27L2M	 0 to 70 − 40 to 105 − 55 to 125 0 to 70 − 40 to 105 − 55 to 125 0 to 70 − 40 to 105 − 55 to 125	°C
T_{stg}	Storage Temperature	− 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal respect to the terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (For 1/2 TS27×2)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS272

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} —

Symbol	Parameter	TS272C			TS272I/TS272M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS272 $T_{min} < T < T_{max}$ TS272A $T_{min} < T < T_{max}$ TS272B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 kΩ C_L = 100 pF Fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_O = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_O = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = − 10 mV, V_O = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} —

Symbol	Parameter	TS27M2C			TS27M2I/TS27M2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M2 $T_{min} < T < T_{max}$ TS27M2A $T_{min} < T < T_{max}$ TS27M2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF Fin = 100 KHz		1			1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

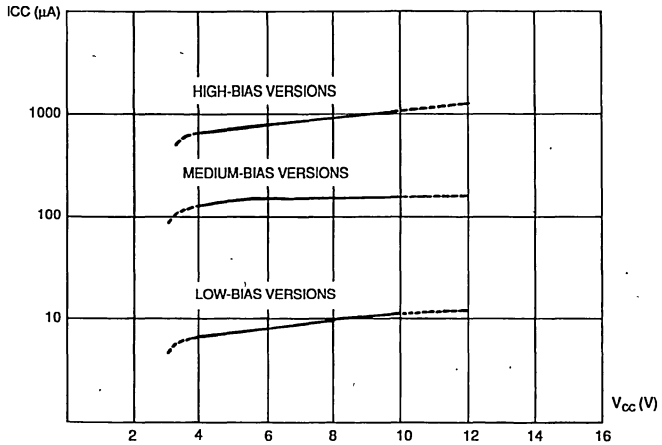
Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27L2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} —

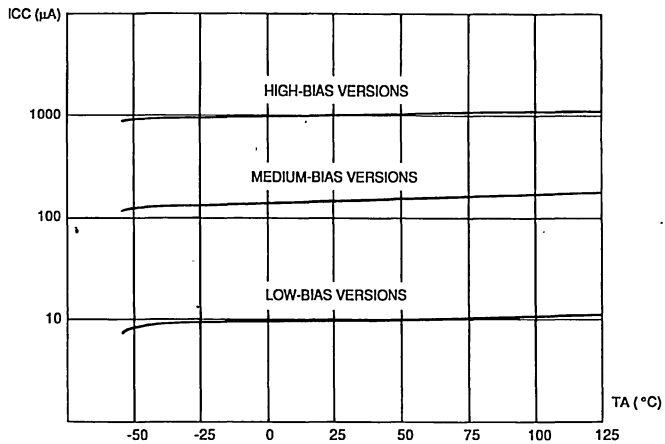
Symbol	Parameter	TS27L2C			TS27L2I/TS27L2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L2 $T_{min} < T < T_{max}$ TS27L2A $T_{min} < T < T_{max}$ TS27L2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	 8.8 8.7	 9		 8.8 8.6	 9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 1 MΩ V_i = 5 V $T_{min} < T < T_{max}$	 60 45	 100		 60 40	 100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF Fin = 100 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25$ °C, NO LOAD

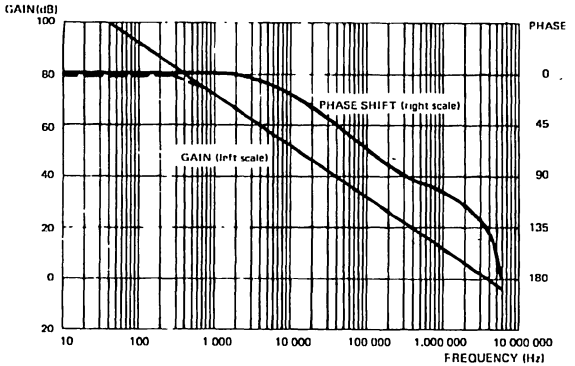
E88TS272-04



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10$ V, $V_{IC} = 5$ V, $V_O = 5$ V, NO LOAD

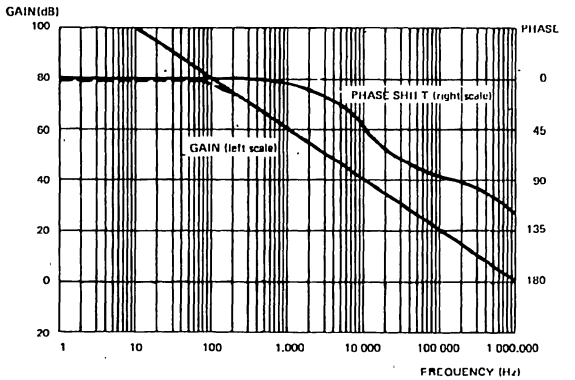
E88TS272-05

TS272



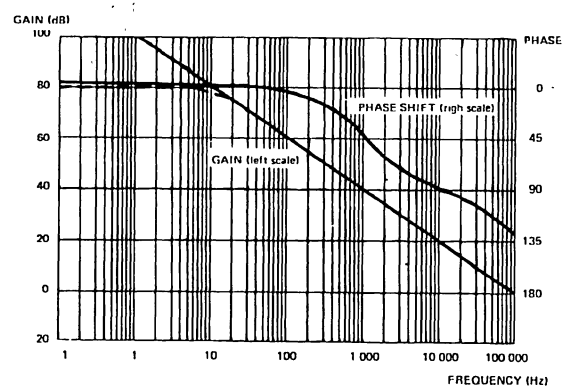
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-06

TS27M2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-07

TS27L2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-08

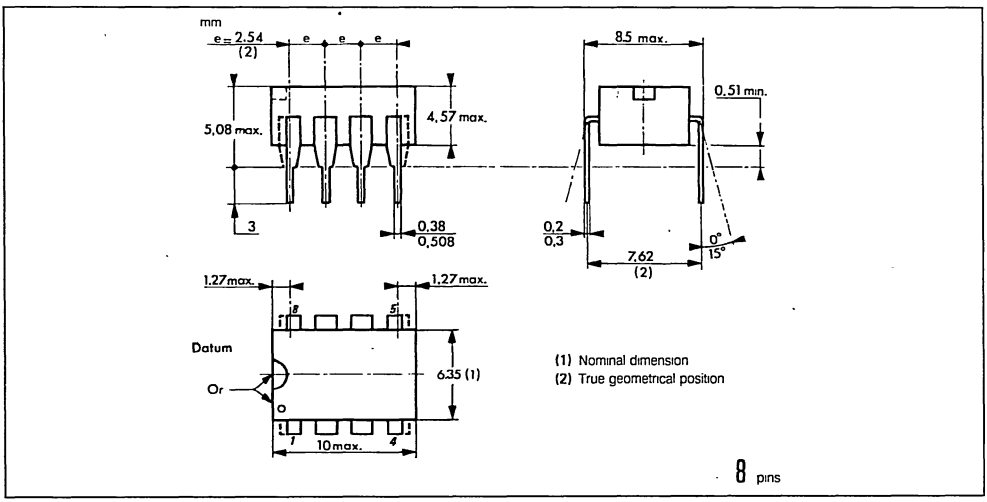
ORDERING INFORMATION

Part Number	Temperature Range °C	Package		
		N	D	J
TS272C	0 to 70	•	•	
TS272AC	0 to 70	•	•	
TS272BC	0 to 70	•	•	
TS272I	– 40 to 105	•	•	
TS272M	– 55 to 125			•
TS27M2C	0 to 70	•	•	
TS27M2AC	0 to 70	•	•	
TS27M2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27M2M	– 55 to 125			•
TS27L2C	0 to 70	•	•	
TS27L2AC	0 to 70	•	•	
TS27L2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27L2M	– 55 to 125			•
TS272AI	– 40 to 105	•	•	
TS272BI	– 40 to 105	•	•	
TS272AM	– 55 to 125			•
TS272BM	– 55 to 125			•
TS27M2AI	– 40 to 105	•	•	
TS27M2BI	– 40 to 105	•	•	
TS27L2AI	– 40 to 105	•	•	
TS27L2BI	– 40 to 105	•	•	
TS27M2AM	– 55 to 125			•
TS27M2BM	– 55 to 125			•
TS27L2AM	– 55 to 125			•
TS27L2BM	– 55 to 125			•

Examples : TS27L2ACN, TS272CD

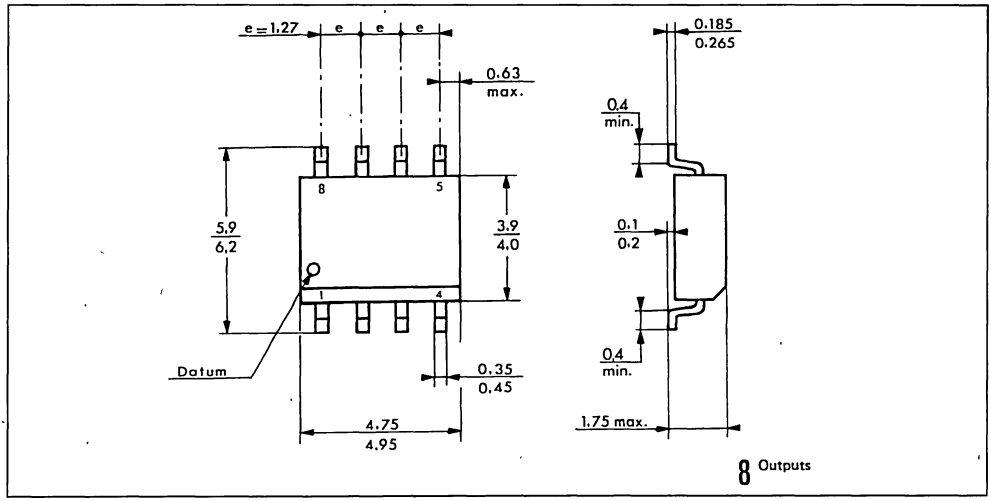
PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

8 PINS - PLASTIC MICROPACKAGE SO

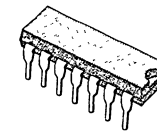


SGS-THOMSON MICROELECTRONICS

TS274
TS27M4/TS27L4

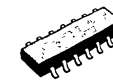
CMOS QUAD OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS274
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD QUAD OPERATIONAL AMPLIFIERS (TL084-LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



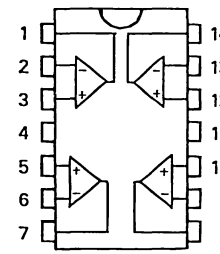
N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)
(Ordering Information at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS274-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^+
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^-
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

DESCRIPTION

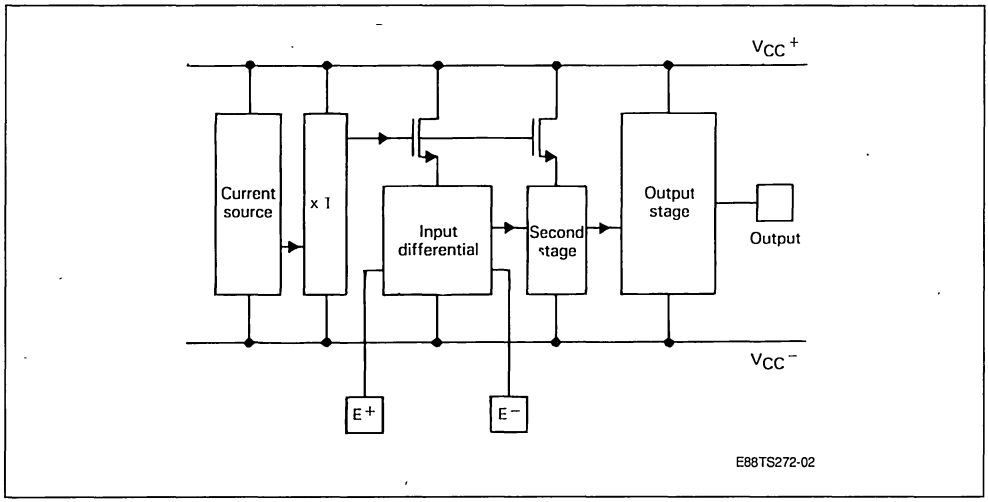
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- **I_{CC} = 10 µA** per amplifier : TS27L4 (Low bias versions)
- **I_{CC} = 150 µA** per amplifier : TS27M4 (Medium bias versions)
- **I_{CC} = 1 mA** per amplifier : TS274 (High bias versions)

The input impedance is similar to the J-FET input impedance : very high input inpedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

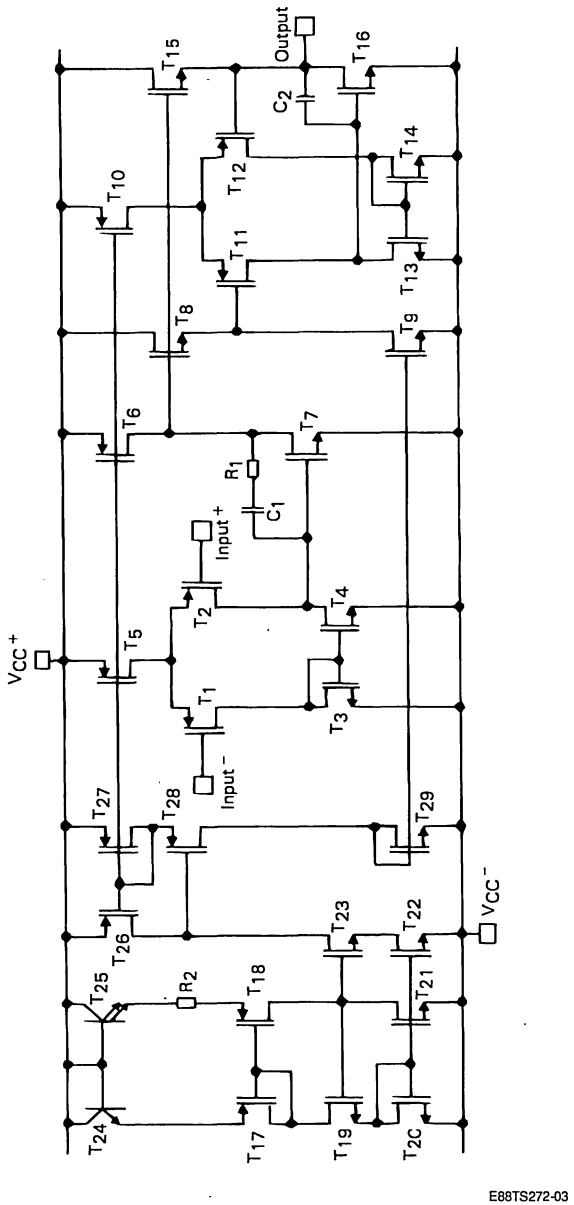
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	12	V
V_{id}	Differential Input Voltage (note 2)	± 12	V
V_i	Input Voltage (note 3)	- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature		
	TS274C	0 to 70	°C
	TS274I	- 40 to 105	
	TS274M	- 55 to 125	
	TS27M4C	0 to 70	
	TS27M4I	- 40 to 105	
	TS27M4M	- 55 to 125	
	TS27L4C	0 to 70	
	TS27L4I	- 40 to 105	
	TS27L4M	- 55 to 125	
T_{stg}	Storage Temperature	- 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (for 1/4 TS27 x 4)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS274

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS274C			TS274I/TS274M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS274 $T_{min} < T < T_{max}$ TS274A $T_{min} < T < T_{max}$ TS274B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	 8.2 8.1	 8.4		 8.2 8	 8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 10 kΩ V_i = 5 V $T_{min} < T < T_{max}$	 10 7	 15		 10 6	 15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 kΩ C_L = 100 pF fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS27M4C			TS27M4I/TS27M4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M4 $T_{min} < T < T_{max}$ TS27M4A $T_{min} < T < T_{max}$ TS27M4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	 8.7 8.6	 8.9		 8.7 8.5	 8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	 30 20	 50		 30 10	 50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF f_{in} = 100 KHz		1			1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
$S_{V\,O}$	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{01}/V_{02}	Cross Talk Attenuation		120			120		dB

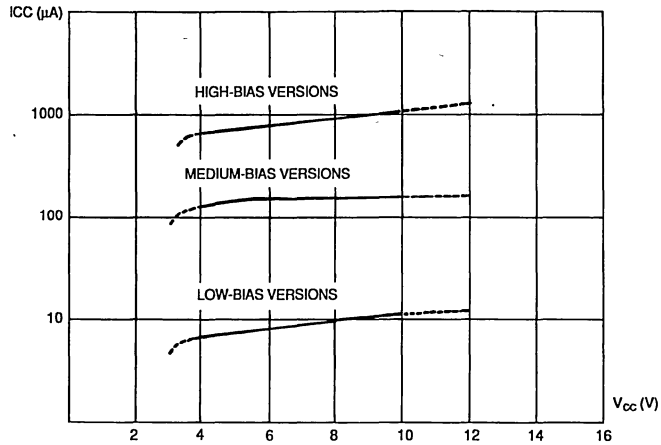
Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27L4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

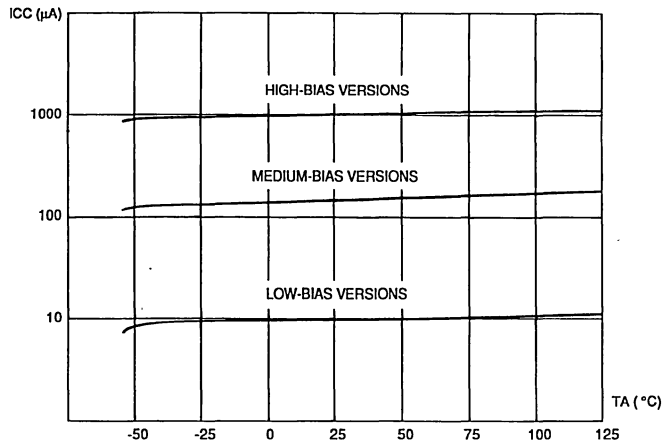
Symbol	Parameter	TS27L4C			TS27L4I/TS27L4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L4 $T_{min} < T < T_{max}$ TS27L4A $T_{min} < T < T_{max}$ TS27L4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	60 45	100		60 40	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
$\lvert V_{O1} / V_{O2} \rvert$	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25$ °C, NO LOAD

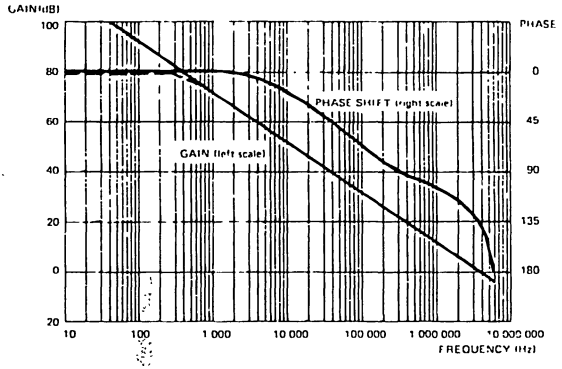
E88TS274-02



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10$ V, $V_{IC} = 5$ V, $V_O = 5$ V, NO LOAD

E88TS274-03

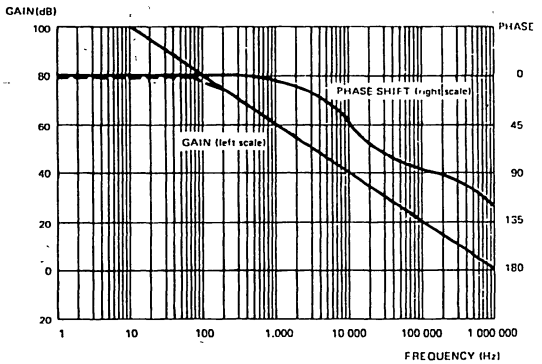
TS274



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-04

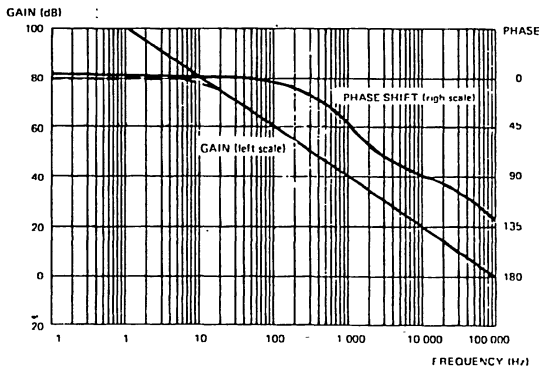
TS27M4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25 °C

E88TS274-05

TS27L4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-06

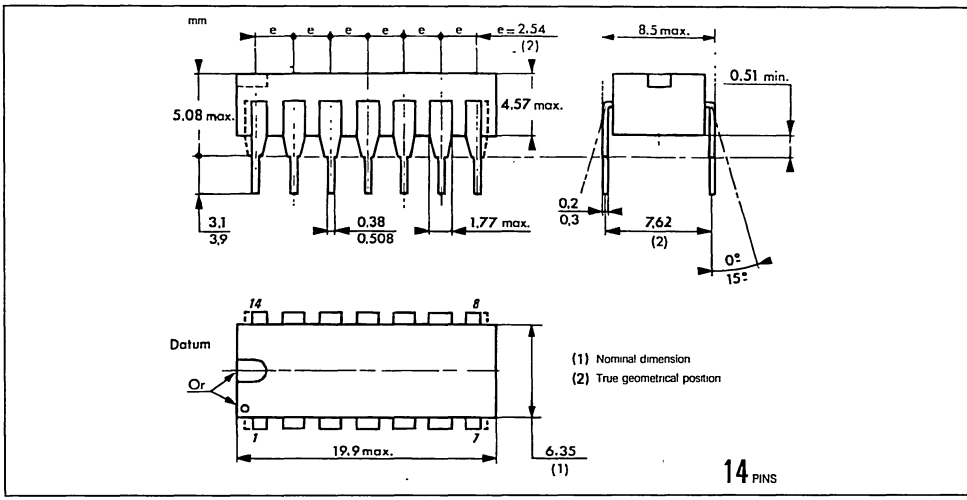
ORDERING INFORMATION

Part Number	Temperature Range °C	Package		
		N	D	J
TS274C	0 to + 70	•	•	
TS274AC	0 to + 70	•	•	
TS274BC	0 to + 70	•	•	
TS274I	- 40 to + 105	•	•	
TS274M	- 55 to + 125			•
TS27M4C	0 to + 70	•	•	
TS27M4AC	0 to + 70	•	•	
TS27M4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27M4M	- 55 to + 125			•
TS27L4C	0 to + 70	•	•	
TS27L4AC	0 to + 70	•	•	
TS27L4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27L4M	- 55 to + 125			•
TS27M4AI	- 40 to + 105	•	•	
TS27M4AM	- 55 to + 125			•
TS27M4BI	- 40 to + 105	•	•	
TS27M4BM	- 55 to + 125			•
TS27L4AI	- 40 to + 105	•	•	
TS27L4AM	- 55 to + 125			•
TS27L4BI	- 40 to + 105	•	•	
TS27L4BM	- 55 to ± 125			•

Examples : TS27L4ACN, TS274CD

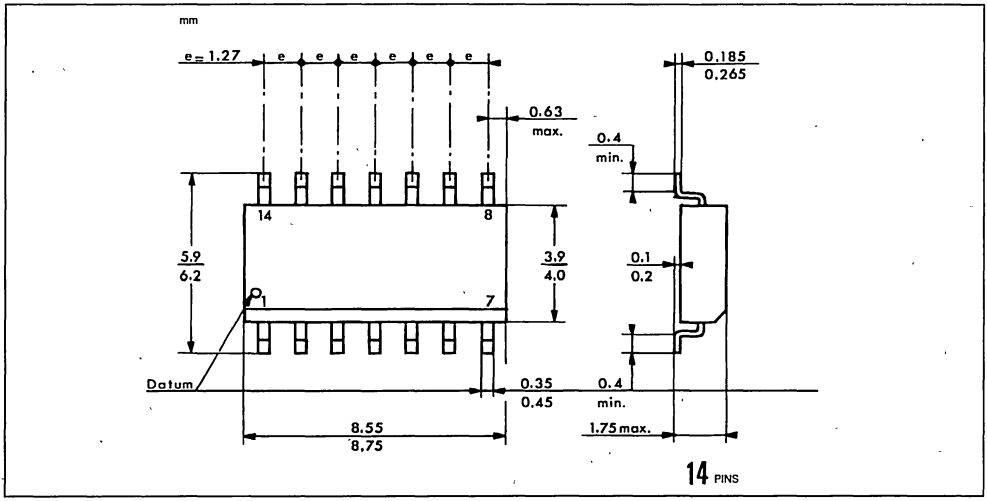
PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

14 PINS - PLASTIC MICROPACKAGE SO



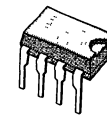
SGS-THOMSON MICROELECTRONICS

TS372

CMOS DUAL DIFFERENTIAL COMPARATOR

ADVANCE DATA

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 4V TO 10V OR ± 2V TO ± 5V
- VERY LOW SUPPLY CURRENT : 0.4 mA INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1 pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1 pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150 mV TYP
- OUTPUT COMPATIBLE WITH TTL.MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE 10^{12} ΩTYP
- FAST REPONSE TIME : 200 NS TYP FOR TTL LEVEL INPUT STEP



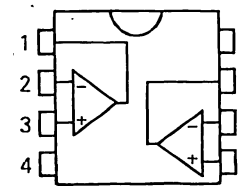
N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)

D
SO14
(Plastic Micropackage)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

DESCRIPTION

These devices consist of two independent precision voltage comparators, designed to operate with single or dual supplies.

These differential comparators use the SGS THOMSON Microelectronics silicon lin MOS process giving them an excellent consumption-speed ratio.

These devices are ideally suited for low consumption applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		12	V
V_O	Output Voltage		12	V
I_O	Output Current		20	mA
	Duration of Output Short-circuit to GND (note 4)		Unlimited	
T_{oper}	Operating Free-air Temperature	TS372C TS372I TS372M	0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature		– 65 to 150	°C

Notes : 1. All voltage values, except differential voltages are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	4 to 10	V
V_{CC}	Min Supply Voltage (for selected devices)	3	V
V_{CC}	Max Supply Voltage	12	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5 V, T = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage for $V_{IC} = V_{ICR\ Min}$ (note 1)		2	10	mV
I_{io}	Input Offset Current (note 1)		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Mode Voltage Range	0 to V_{CC} – 1.5 V			V
A_{vd}	Large Signal Voltage Gain V_{CC} = 10 V ; R_L > 15 KΩ at V_{CC}		200		V/mV
I_{oh}	High Level Output Current V_{id} = 1 V ; V_{oh} = + 5 V		0.1		nA
V_{ol}	Low Level Output Voltage V_{id} = 1 V ; I_{ol} = 4 mA		150	400	mV
I_{CC}	Supply Current (4 comparators) V_{id} = – 1 V ; R_L = ∞		0.4	1	mA
I_{ol}	Low Level Output Current V_{id} = – 1 V ; V_{OL} = 1.5 V	6	16		mA
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF Overdrive 5 mV (note 2)		600		ns
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF TTL Input (note 2)		200		ns

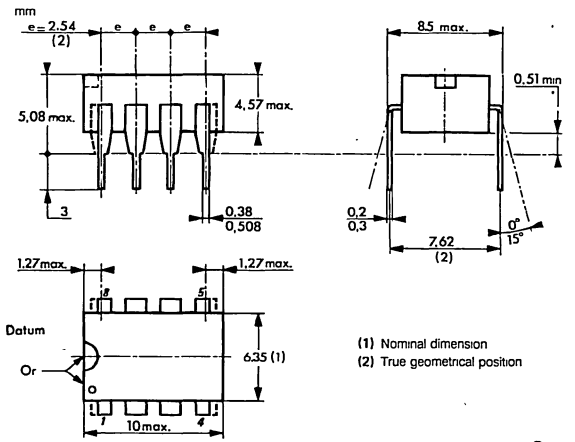
Notes : 1. The offset voltage and offset current which are given are the maximum values required to drive the output down to 400 mV or up to 4 V with R_L = 2.5 KΩ to V_{CC}.
2. The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4 V.

ORDERING INFORMATION

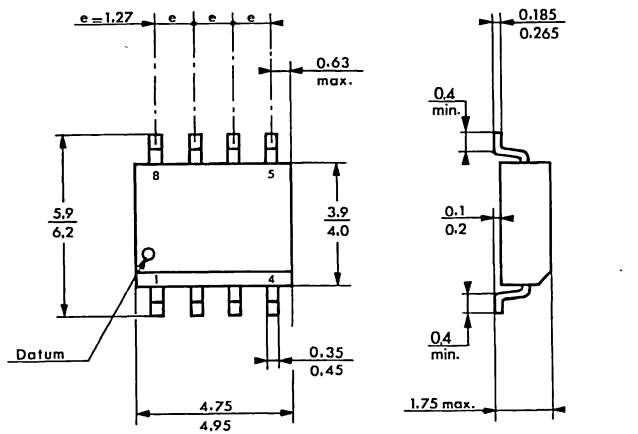
Part Number	Temperature Range	Package		
		N	D	J
TS372	0 to 70	•	•	
TS372I	– 40 to 105	•	•	
TS372M	– 55 to 125			•
Examples : TS372ID				

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



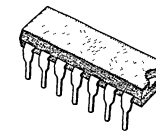
8 PINS - PLASTIC MICROPACKAGE SO



CMOS QUAD DIFFERENTIAL COMPARATOR

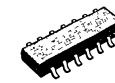
ADVANCED DATA

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 4V TO 10V OR ± 2V TO ± 5V
- VERY LOW SUPPLY CURRENT : 0.4 mA INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1 pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1 pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150 mV TYP
- OUTPUT COMPATIBLE WITH TTL.MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE 10^{12} ΩTYP
- FAST REPONSE TIME : 200 NS TYP FOR TTL LEVEL INPUT STEP



N
DIP14
(Plastic Package)

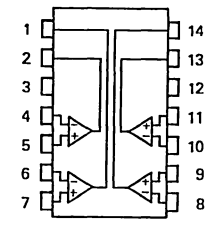
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS (top view)



1 - Output 2
2 - Output 1
3 - V_{CC}^{+}
4 - Inverting input 1
5 - Non-inverting input 1
6 - Inverting input 2
7 - Non-inverting input 2
8 - Inverting input 3
9 - Non-inverting input 3
10 - Inverting input 4
11 - Non-inverting input 4
12 - V_{CC}^{-}
13 - Output 4
14 - Output 3

DESCRIPTION

These devices consist of four independent precision voltage comparators, designed to operate with single or dual supplies.

These differential comparators use the SGS THOMSON Microelectronics silicon lin MOS process giving them an excellent consumption-speed ratio.

These devices are ideally suited for low consumption applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		12	V
V_O	Output Voltage		12	V
I_O	Output Current		20	mA
	Duration of Output Short-circuit to GND (note 4)		Unlimited	
T_{oper}	Operating Free-air Temperature	TS374C TS374I TS374M	0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature		– 65 to 150	°C

Notes : 1. All voltage values, except differential voltages are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	4 to 10	V
V_{CC}	Min Supply Voltage (for selected devices)	3	V
V_{CC}	Max Supply Voltage	12	V

ELECTRICAL CHARACTERISTICS ($V_{CC.}$ = + 5 V, T = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage for $V_{IC} = V_{ICR\ Min}$ (note 1)		2	10	mV
I_{io}	Input Offset Current (note 1)		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Mode Voltage Range	0 to V_{CC} – 1.5 V			V
A_{vd}	Large Signal Voltage Gain V_{CC} = 10 V ; R_L > 15 KΩ at V_{CC}		200		V/mV
I_{oh}	High Level Output Current V_{id} = 1 V ; V_{oh} = + 5 V		0.1		nA
V_{ol}	Low Level Output Voltage V_{id} = 1 V ; I_{ol} = 4 mA		150	400	mV
I_{CC}	Supply Current (4 comparators) V_{id} = – 1 V ; R_L = ∞		0.4	1	mA
I_{ol}	Low Level Output Current V_{id} = – 1 V ; V_{OL} = 1.5 V	6	16		mA
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF Overdrive 5 mV (note 2)		600		ns
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF TTL Input (note 2)		200		ns

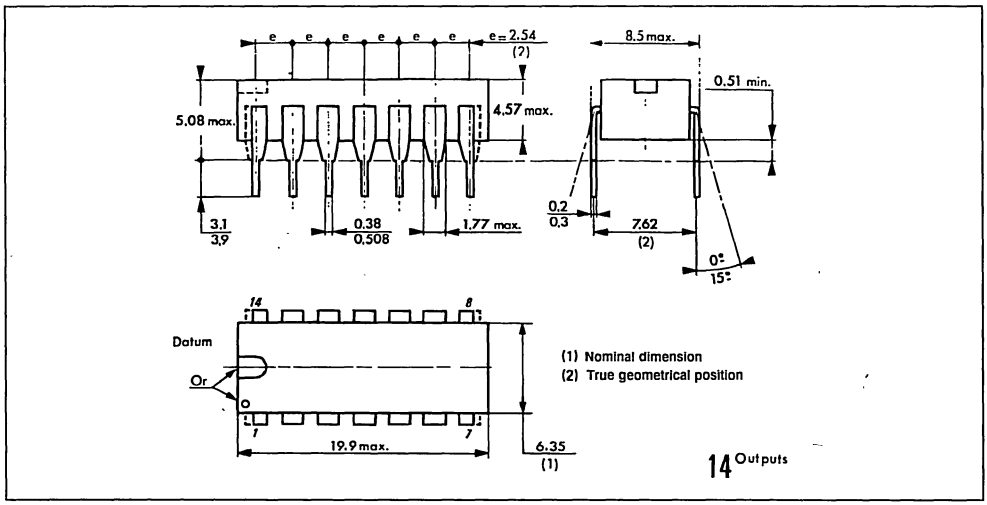
Notes : 1. The offset voltage and offset current which are given are the maximum values required to drive the output down to 400 mV or up to 4 V with R_L = 2.5 KΩ to V_{CC}.
2. The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4 V.

ORDERING INFORMATION

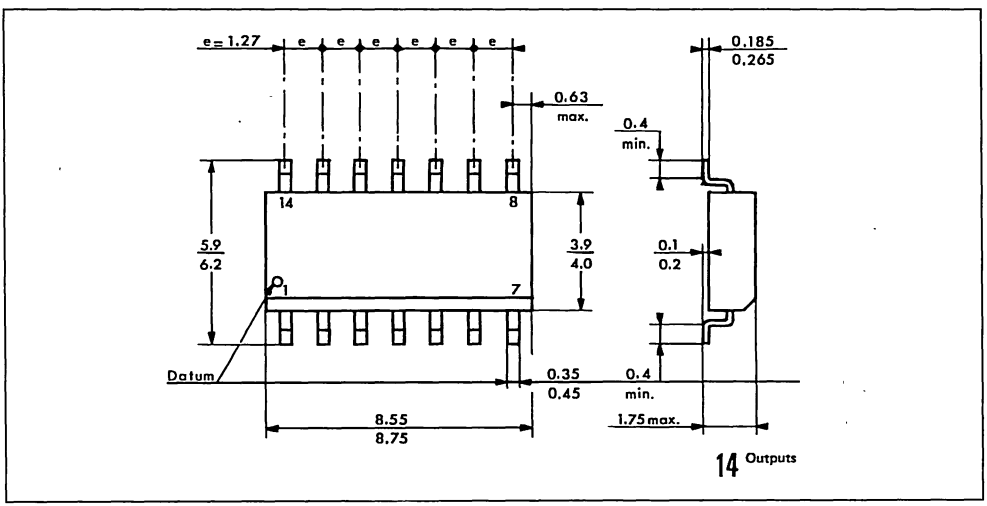
Part Number	Temperature Range	Package		
		N	D	J
TS374	0 to 70	•	•	
TS374I	– 40 to 105	•	•	
TS374M	– 55 to 125			•
Examples : TS374ID				

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



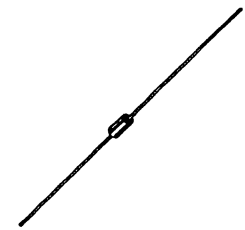
14 PINS - PLASTIC MICROPACKAGE SO



PROTECTION CIRCUITS

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY :
  400 W / 1 ms EXPO
- VERY FAST CLAMPING TIME :
  1 ps FOR UNIDIRECTIONAL TYPES
  5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE :
  5.8 V → 376 V
- ORDER CODE :
  TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES



F 126
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

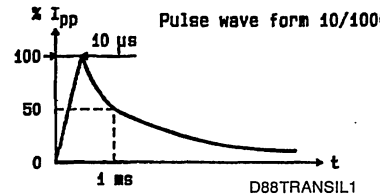
ABSOLUTE MAXIMUM RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	400	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	1.7	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	60	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P BZW04P5V8	P BZW04P5V8B	1000	5.8	6.45	6.8	7.48	10	10.5	38	13.4	174	5.7	3500
BZW04-5V8	BZW04-5V8B	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
BZW04P6V4	P BZW04P6V4B	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
BZW04-6V4	BZW04-6V4B	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
BZW04P7V0	P BZW04P7V0B	200	7.02	7.79	8.2	9.02	10	12.1	33	15.5	148	6.5	2700
BZW04-7V0	BZW04-7V0B	200	7.02	7.79	8.2	8.61	10	12.1	33	15.5	148	6.5	2700
BZW04P7V8	BZW04P7V8B	50	7.78	8.65	9.1	10.0	1	13.4	30	17.1	134	6.8	2300
BZW04-7V8	BZW04-7V8B	50	7.78	8.65	9.1	9.55	1	13.4	30	17.1	134	6.8	2300
BZW04P8V5	BZW04P8V5B	10	8.55	9.50	10	11.0	1	14.5	27.6	18.6	258	7.3	2000
BZW04-8V5	BZW04-8V5B	10	8.55	9.50	10	10.50	1	14.5	27.6	18.6	258	7.3	2000
P BZW04P9V4	P BZW04P9V4B	5	9.4	10.5	11	12.1	1	15.6	25.7	20.3	236	7.5	1750
BZW04-9V4	BZW04-9V4B	5	9.4	10.5	11	11.6	1	15.6	25.7	20.3	236	7.5	1750
BZW04P10	BZW04P10B	5	10.2	11.4	12	13.2	1	16.7	24	21.7	221	7.8	1550
BZW04-10	BZW04-10B	5	10.2	11.4	12	12.6	1	16.7	24	21.7	221	7.8	1550
P BZW04P11	P BZW04P11B	5	11.1	12.4	13	14.3	1	18.2	22	23.6	203	8.1	1450
BZW04-11	BZW04-11B	5	11.1	12.4	13	13.7	1	18.2	22	23.6	203	8.1	1450
P BZW04P13	P BZW04P13B	5	12.8	14.3	15	16.5	1	21.2	19	27.2	176	8.4	1200
BZW04-13	BZW04-13B	5	12.8	14.3	15	15.8	1	21.2	19	27.2	176	8.4	1200
P BZW04P14	P BZW04P14B	5	13.6	15.2	16	17.6	1	22.5	17.8	28.9	166	8.6	1100
BZW04-14	BZW04-14B	5	13.6	15.2	16	16.8	1	22.5	17.8	28.9	166	8.6	1100
P BZW04P15	P BZW04P15B	5	15.3	17.1	18	19.8	1	25.2	16	32.5	148	8.8	975
BZW04-15	BZW04-15B	5	15.3	17.1	18	18.9	1	25.2	16	32.5	148	8.8	975
BZW04P17	BZW04P17B	5	17.1	19	20	22	1	27.7	14.5	36.1	133	9.0	850
BZW04-17	BZW04-17B	5	17.1	19	20	21	1	27.7	14.5	36.1	133	9.0	850
BZW04P19	BZW04P19B	5	18.8	20.9	22	24.2	1	30.6	13	39.3	122	9.2	800
BZW04-19	BZW04-19B	5	18.8	20.9	22	23.1	1	30.6	13	39.3	122	9.2	800
BZW04P20	P BZW04P20B	5	20.5	22.8	24	26.4	1	33.2	12	42.8	112	9.4	725
BZW04-20	BZW04-20B	5	20.5	22.8	24	25.2	1	33.2	12	42.8	112	9.4	725
P BZW04P23	BZW04P23B	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	99	9.6	625
BZW04-23	BZW04-23B	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	99	9.6	625
P BZW04P26	P BZW04P26B	5	25.6	28.5	30	33	1	41.5	9.6	53.5	90	9.7	575
BZW04-26	BZW04-26B	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	90	9.7	575
BZW04P28	P BZW04P28B	5	28.2	31.4	33	36.3	1	45.7	8.8	59	81.5	9.8	510
BZW04-28	BZW04-28B	5	28.2	31.4	33	34.7	1	45.7	8.8	59	81.5	9.8	510
P BZW04P31	P BZW04P31B	5	30.8	34.2	36	39.6	1	49.9	8	64.3	74.5	9.9	480
BZW04-31	BZW04-31B	5	30.8	34.2	36	37.8	1	49.9	8	64.3	74.5	9.9	480
P BZW04P33	BZW04P33B	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	69	10.0	450

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

Types			I_{RM} @ V_{RM} max.		$V_{(BR)}$* (V) @ I_R				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional		(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
BZW04-33	BZW04-33B		5	33.3	37.1	39	41	1	53.9	7.4	69.7	69	10.0	450
BZW04P37	BZW04P37B	P	5	36.8	40.9	43	47.3	1	59.3	6.7	76.8	62.5	10.1	400
BZW04-37	BZW04-37B		5	36.8	40.9	43	45.2	1	59.3	6.7	76.8	62.5	10.1	400
BZW04P40	BZW04P40B		5	40.2	44.7	47	51.7	1	64.8	6.2	84	57	10.1	370
BZW04-40	BZW04-40B		5	40.2	44.7	47	49.4	1	64.8	6.2	84	57	10.1	370
BZW04P44	BZW04P44B		5	43.6	48.5	51	56.1	1	70.1	5.7	91	52.5	10.2	350
BZW04-44	BZW04-44B		5	43.6	48.5	51	53.6	1	70.1	5.7	91	52.5	10.2	350
BZW04P48	BZW04P48B		5	47.8	53.2	56	61.6	1	77	5.2	100	48	10.3	320
BZW04-48	BZW04-48B		5	47.8	53.2	56	58.8	1	77	5.2	100	48	10.3	320
BZW04P53	BZW04P53B		5	53	58.9	62	68.2	1	85	4.7	111	43	10.4	290
BZW04-53	BZW04-53B		5	53	58.9	62	65.1	1	85	4.7	111	43	10.4	290
BZW04P58	BZW04P58B		5	58.1	64.6	68	74.8	1	92	4.3	121	39.5	10.4	270
BZW04-58	BZW04-58B		5	58.1	64.6	68	71.4	1	92	4.3	121	39.5	10.4	270
BZW04P64	BZW04P64B		5	64.1	71.3	75	82.5	1	103	3.9	134	36	10.5	250
BZW04-64	BZW04-64B		5	64.1	71.3	75	78.8	1	103	3.9	134	36	10.5	250
BZW04P70	BZW04P70B	P	5	70.1	77.9	82	90.2	1	113	3.5	146	33	10.5	230
BZW04-70	BZW04-70B		5	70.1	77.9	82	86.1	1	113	3.5	146	33	10.5	230
BZW04P78	BZW04P78B		5	77.8	86.5	91	100	1	125	3.2	162	29.5	10.6	210
BZW04-78	BZW04-78B		5	77.8	86.5	91	95.5	1	125	3.2	162	29.5	10.6	210
BZW04P85	BZW04P85B	P	5	85.5	95	100	110	1	137	2.9	178	27	10.6	200
BZW04-85	BZW04-85B		5	85.5	95	100	105	1	137	2.9	178	27	10.6	200
BZW04P94	BZW04P94B		5	94	105	110	121	1	152	2.6	195	24.5	10.7	185
BZW04-94	BZW04-94B		5	94	105	110	116	1	152	2.6	195	24.5	10.7	185
BZW04P102	BZW04P102B		5	102	114	120	132	1	165	2.4	212	22.5	10.7	170
BZW04-102	BZW04-102B		5	102	114	120	126	1	165	2.4	212	22.5	10.7	170
BZW04P111	BZW04P111B	P	5	111	124	130	143	1	179	2.2	230	20.8	10.7	165
BZW04-111	BZW04-111B		5	111	124	130	137	1	179	2.2	230	20.8	10.7	165
BZW04P128	BZW04P128B	P	5	128	143	150	165	1	207	2.0	265	18.1	10.8	145
BZW04-128	BZW04-128B		5	128	143	150	158	1	207	2.0	265	18.1	10.8	145
BZW04P136	BZW04P136B	P	5	136	152	160	176	1	219	1.8	282	17	10.8	140
BZW04-136	BZW04-136B		5	136	152	160	168	1	219	1.8	282	17	10.8	140
BZW04P145	BZW04P145B		5	145	161	170	187	1	234	1.7	301	16	10.8	135
BZW04-145	BZW04-145B		5	145	161	170	179	1	234	1.7	301	16	10.8	135
BZW04P154	BZW04P154B		5	154	171	180	198	1	246	1.6	317	15.1	10.8	125
BZW04-154	BZW04-154B		5	154	171	180	189	1	246	1.6	317	15.1	10.8	125
BZW04P171	BZW04P171B		5	171	190	200	220	1	274	1.5	353	13.6	10.8	120
BZW04-171	BZW04-171B		5	171	190	200	210	1	274	1.5	353	13.6	10.8	120
BZW04P188	BZW04P188B	P	5	188	209	220	242	1	301	1.4	388	12.4	10.8	110
BZW04-188	BZW04-188B		5	188	209	220	231	1	301	1.4	388	12.4	10.8	110
BZW04P213	BZW04P213B		5	213	237	250	275	1	344	1.5	442	12	11	100
BZW04-213	BZW04-213B		5	213	237	250	263	1	344	1.5	442	12	11	100
BZW04P239	BZW04P239B		5	239	266	280	308	1	384	1.5	494	12	11	95
BZW04-239	BZW04-239B		5	239	266	280	294	1	384	1.5	494	12	11	95
BZW04P256	BZW04P256B		5	256	285	300	330	1	414	1.2	529	10	11	90
BZW04-256	BZW04-256B		5	256	285	300	315	1	414	1.2	529	10	11	90
BZW04P273	BZW04P273B		5	273	304	320	352	1	438	1.2	564	10	11	85
BZW04-273	BZW04-273B		5	273	304	320	336	1	438	1.2	564	10	11	85
BZW04P299	BZW04P299B	P	5	299	332	350	385	1	482	0.9	618	9	11	80
BZW04-299	BZW04-299B		5	299	332	350	368	1	482	0.9	618	9	11	80
BZW04P342	BZW04P342B		5	342	380	400	440	1	548	0.9	706	8	11	75
BZW04-342	BZW04-342B		5	342	380	400	420	1	548	0.9	706	8	11	75
BZW04P376	BZW04P376B		5	376	418	440	484	1	603	0.8	776	8	11	70
BZW04-376	BZW04-376B		5	376	418	440	462	1	603	0.8	776	8	11	70

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

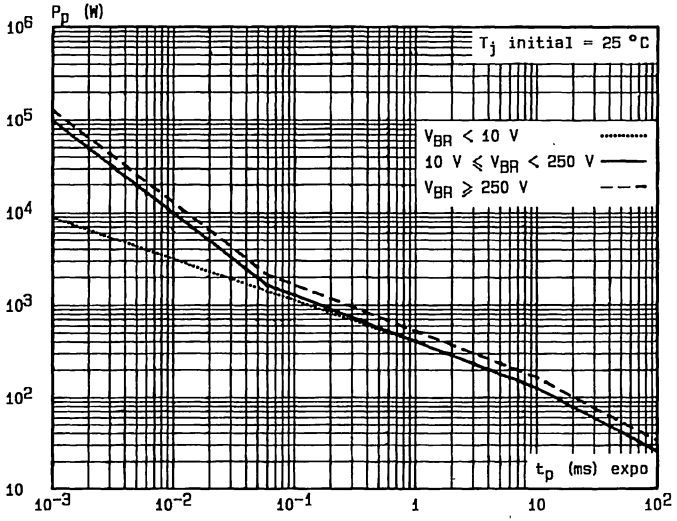


Fig.1 - Peak pulse power versus exponential pulse duration.

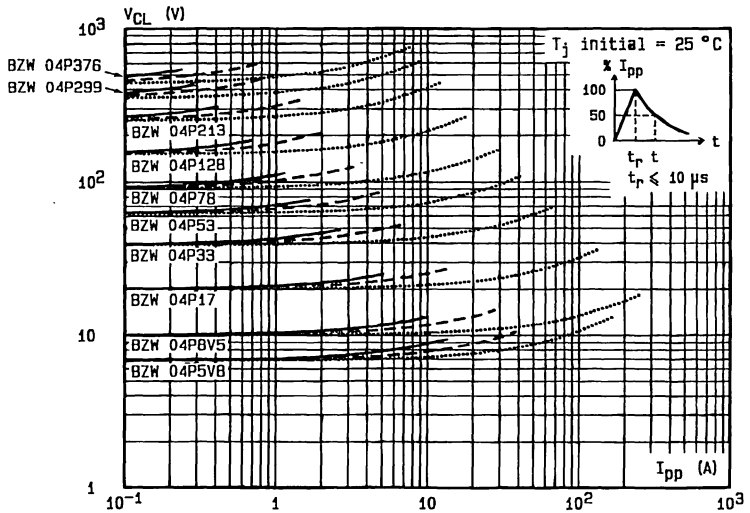


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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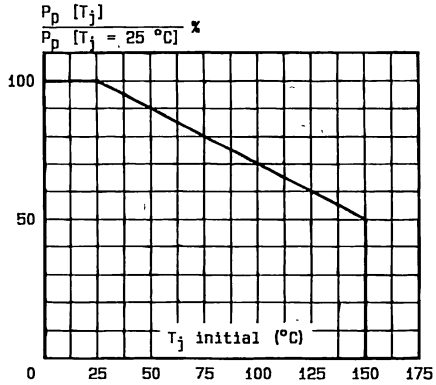


Fig.3 - Allowable power dissipation versus junction temperature.

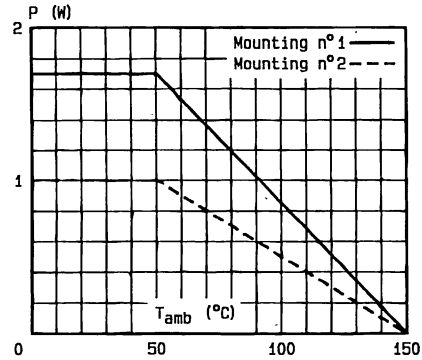


Fig.4 - Power dissipation versus ambient temperature.

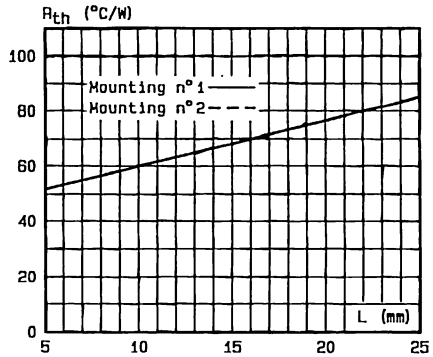
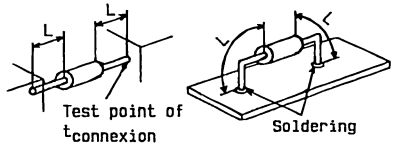


Fig.5 - Thermal resistance versus lead length.

Mounting n°1
INFINITE HEATSINK

Mounting n°2
PRINTED CIRCUIT



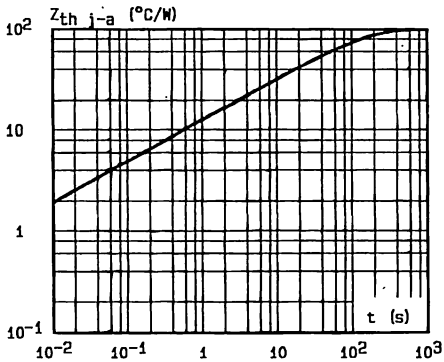


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

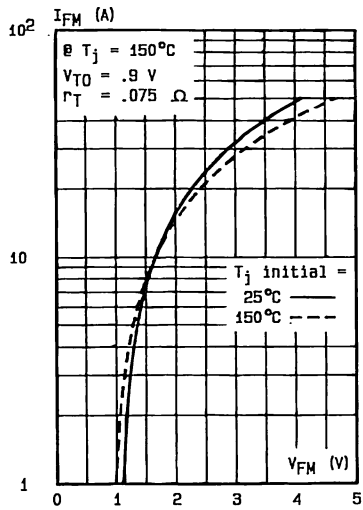


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

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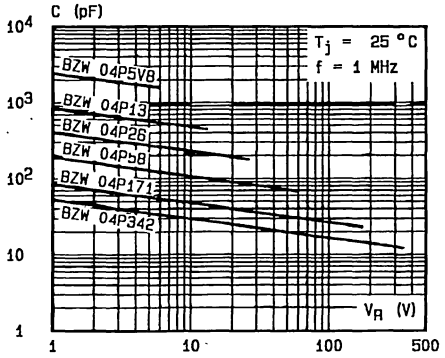

Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

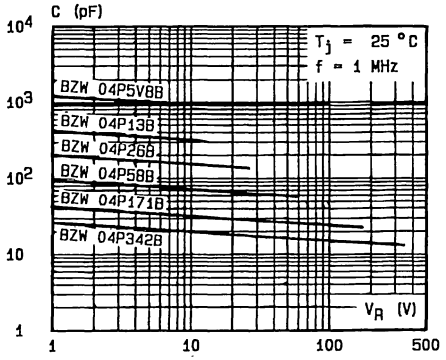

Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

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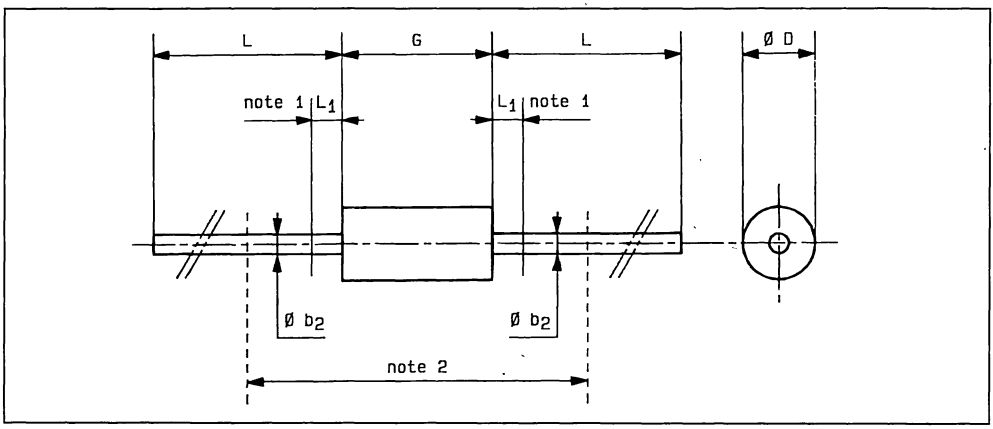
PACKAGE MECHANICAL DATA

F 126 Plastic



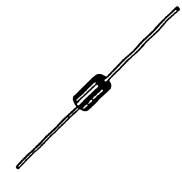
Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	0.76	0.86	0.029	0.034	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	2.95	3.05	0.116	0.120	
G	6.05	6.35	0.238	0.250	
L	26	–	1.024	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.4 g.

P6KE6V8P, A → 440P, A
P6KE6V8CP, CA → 440CP, CA

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY :
  600 W / 1 ms EXPO
- VERY FAST CLAMPING TIME :
  1 ps FOR UNIDIRECTIONAL TYPES
  5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE :
  5.8 V → 376 V
- ORDER CODE :
  TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES



CB-417
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

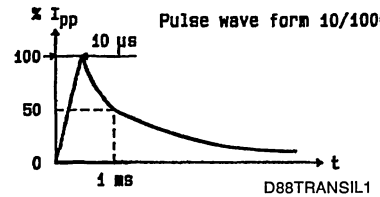
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	600	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	100	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 175 175	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.
V_{FM}	Forward Voltage Drop for Unidirectional Types (I_{FM} = 50 A)		3.5 V max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P P6KE6V8P	P P6KE6V8CP	1000§	5.8	6.45	6.8	7.48	10	10.5	57	13.4	261	5.7	4000
P6KE6V8A	P6KE6V8CA	1000§	5.8	6.45	6.8	7.14	10	10.5	57	13.4	261	5.7	4000
P P6KE7V5P	P P6KE7V5CP	500§	6.4	7.13	7.5	8.25	10	11.3	53	14.5	241	6.1	3700
P6KE7V5A	P6KE7V5CA	500§	6.4	7.13	7.5	7.88	10	11.3	53	14.5	241	6.1	3700
P P6KE8V2P	P6KE8V2CP	200§	7.02	7.79	8.2	9.02	10	12.1	50	15.5	226	6.5	3400
P6KE8V2A	P6KE8V2CA	200§	7.02	7.79	8.2	8.61	10	12.1	50	15.5	226	6.5	3400
P6KE9V1P	P6KE9V1CP	50§	7.78	8.65	9.1	10	1	13.4	45	17.1	205	6.8	3100
P6KE9V1A	P6KE9V1CA	50§	7.78	8.65	9.1	9.55	1	13.4	45	17.1	205	6.8	3100
P6KE10P	P6KE10CP	10§	8.55	9.5	10	11	1	14.5	41	18.6	387	7.3	2800
P6KE10A	P6KE10CA	10§	8.55	9.5	10	10.5	1	14.5	41	18.6	387	7.3	2800
P6KE11P	P6KE11CP	5§	9.4	10.5	11	12.1	1	15.6	38	20.3	355	7.5	2500
P6KE11A	P6KE11CA	5§	9.4	10.5	11	11.6	1	15.6	38	20.3	355	7.5	2500
P P6KE12P	P P6KE12CP	5	10.2	11.4	12	13.2	1	16.7	36	21.7	332	7.8	2300
P6KE12A	P6KE12CA	5	10.2	11.4	12	12.6	1	16.7	36	21.7	332	7.8	2300
P P6KE13P	P P6KE13CP	5	11.1	12.4	13	14.3	1	18.2	33	23.6	305	8.1	2150
P6KE13A	P6KE13CA	5	11.1	12.4	13	13.7	1	18.2	33	23.6	305	8.1	2150
P P6KE15P	P P6KE15CP	5	12.8	14.3	15	16.5	1	21.2	28	27.2	265	8.4	1900
P6KE15A	P6KE15CA	5	12.8	14.3	15	15.8	1	21.2	28	27.2	265	8.4	1900
P6KE16P	P6KE16CP	5	13.6	15.2	16	17.6	1	22.5	27	28.9	249	8.6	1800
P6KE16A	P6KE16CA	5	13.6	15.2	16	16.8	1	22.5	27	28.9	249	8.6	1800
P P6KE18P	P P6KE18CP	5	15.3	17.1	18	19.8	1	25.2	24	32.5	222	8.8	1600
P6KE18A	P6KE18CA	5	15.3	17.1	18	18.9	1	25.2	24	32.5	222	8.8	1600
P P6KE20P	P6KE20CP	5	17.1	19	20	22	1	27.7	22	36.1	199	9.0	1500
P6KE20A	P6KE20CA	5	17.1	19	20	21	1	27.7	22	36.1	199	9.0	1500
P6KE22P	P P6KE22CP	5	18.8	20.9	22	24.2	1	30.6	20	39.3	183	9.2	1350
P6KE22A	P6KE22CA	5	18.8	20.9	22	23.1	1	30.6	20	39.3	183	9.2	1350
P6KE24P	P6KE24CP	5	20.5	22.8	24	26.4	1	33.2	18	42.8	168	9.4	1250
P6KE24A	P6KE24CA	5	20.5	22.8	24	25.2	1	33.2	18	42.8	168	9.4	1250
P P6KE27P	P6KE27CP	5	23.1	25.7	27	29.7	1	37.5	16	48.3	149	9.6	1150
P6KE27A	P6KE27CA	5	23.1	25.7	27	28.4	1	37.5	16	48.3	149	9.6	1150
P P6KE30P	P6KE30CP	5	25.6	28.5	30	33	1	41.5	14.5	53.5	134	9.7	1075
P6KE30A	P6KE30CA	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	134	9.7	1075
P P6KE33P	P P6KE33CP	5	28.2	31.4	33	36.3	1	45.7	13.1	59	122	9.8	1000
P6KE33A	P6KE33CA	5	28.2	31.4	33	34.7	1	45.7	13.1	59	122	9.8	1000
P P6KE36P	P6KE36CP	5	30.8	34.2	36	39.6	1	49.9	12	64.3	112	9.9	950
P6KE36A	P6KE36CA	5	30.8	34.2	36	37.8	1	49.9	12	64.3	112	9.9	950

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types P6KE6V8CP → 11CA, IRM must be double that specified for unidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		V_{CL} @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P P6KE39P	P P6KE39CP	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	103	10.0	900
P6KE39A	P6KE39CA	5	33.3	37.1	39	41	1	53.9	11.1	69.7	103	10.0	900
P6KE43P	P6KE43CP	5	36.8	40.9	43	47.3	1	59.3	10.1	76.8	94	10.1	850
P6KE43A	P6KE43CA	5	36.8	40.9	43	45.2	1	59.3	10.1	76.8	94	10.1	850
P6KE47P	P P6KE47CP	5	40.2	44.7	47	51.7	1	64.8	9.3	84	86	10.1	800
P6KE47A	P6KE47CA	5	40.2	44.7	47	49.4	1	64.8	9.3	84	86	10.1	800
P P6KE51P	P6KE51CP	5	43.6	48.5	51	56.1	1	70.1	8.6	91	79	10.2	750
P6KE51A	P6KE51CA	5	43.6	48.5	51	53.6	1	70.1	8.6	91	79	10.2	750
P P6KE56P	P6KE56CP	5	47.8	53.2	56	61.6	1	77	7.8	100	72	10.3	700
P6KE56A	P6KE56CA	5	47.8	53.2	56	58.8	1	77	7.8	100	72	10.3	700
P6KE62P	P6KE62CP	5	53	58.9	62	68.2	1	85	7.1	111	65	10.4	650
P6KE62A	P6KE62CA	5	53	58.9	62	65.1	1	85	7.1	111	65	10.4	650
P P6KE68P	P6KE68CP	5	58.1	64.6	68	74.8	1	92	6.5	121	59.5	10.4	625
P6KE68A	P6KE68CA	5	58.1	64.6	68	71.4	1	92	6.5	121	59.5	10.4	625
P6KE75P	P6KE75CP	5	64.1	71.3	75	82.5	1	103	5.8	134	53.5	10.5	575
P6KE75A	P6KE75CA	5	64.1	71.3	75	78.8	1	103	5.8	134	53.5	10.5	575
P P6KE82P	P6KE82CP	5	70.1	77.9	82	90.2	1	113	5.3	146	49	10.5	550
P6KE82A	P6KE82CA	5	70.1	77.9	82	86.1	1	113	5.3	146	49	10.5	550
P6KE91P	P6KE91CP	5	77.8	86.5	91	100	1	125	4.8	162	44.5	10.6	525
P6KE91A	P6KE91CA	5	77.8	86.5	91	95.5	1	125	4.8	162	44.5	10.6	525
P6KE100P	P6KE100CP	5	85.5	95	100	110	1	137	4.4	178	40.5	10.6	500
P6KE100A	P6KE100CA	5	85.5	95	100	105	1	137	4.4	178	40.5	10.6	500
P6KE110P	P6KE110CP	5	94	105	110	121	1	152	3.9	195	37	10.7	470
P6KE110A	P6KE110CA	5	94	105	110	116	1	152	3.9	195	37	10.7	470
P6KE120P	P6KE120CP	5	102	114	120	132	1	165	3.6	212	34	10.7	450
P6KE120A	P6KE120CA	5	102	114	120	126	1	165	3.6	212	34	10.7	450
P P6KE130P	P6KE130CP	5	111	124	130	143	1	179	3.4	230	31.5	10.7	420
P6KE130A	P6KE130CA	5	111	124	130	137	1	179	3.4	230	31.5	10.7	420
P6KE150P	P6KE150CP	5	128	143	150	165	1	207	2.9	265	27.2	10.8	400
P6KE150A	P6KE150CA	5	128	143	150	158	1	207	2.9	265	27.2	10.8	400
P6KE160P	P P6KE160CP	5	136	152	160	176	1	219	2.7	282	25.5	10.8	380
P6KE160A	P6KE160CA	5	136	152	160	168	1	219	2.7	282	25.5	10.8	380
P6KE170P	P6KE170CP	5	145	161	170	187	1	234	2.6	301	24	10.8	370
P6KE170A	P6KE170CA	5	145	161	170	179	1	234	2.6	301	24	10.8	370
P P6KE180P	P6KE180CP	5	154	171	180	198	1	246	2.4	317	22.7	10.8	360
P6KE180A	P6KE180CA	5	154	171	180	189	1	246	2.4	317	22.7	10.8	360
P P6KE200P	P6KE200CP	5	171	190	200	220	1	274	2.2	353	20.4	10.8	350
P6KE200A	P6KE200CA	5	171	190	200	210	1	274	2.2	353	20.4	10.8	350
P6KE220P	P6KE220CP	5	188	209	220	242	1	301	2	388	18.6	10.8	330
P6KE220A	P6KE220CA	5	188	209	220	231	1	301	2	388	18.6	10.8	330
P P6KE250P	P6KE250CP	5	213	237	250	275	1	344	2	442	19	11	310
P6KE250A	P6KE250CA	5	213	237	250	263	1	344	2	442	19	11	310
P6KE280P	P6KE280CP	5	239	266	280	308	1	384	2	494	18	11	300
P6KE280A	P6KE280CA	5	239	266	280	294	1	384	2	494	18	11	300
P6KE300P	P6KE300CP	5	256	285	300	330	1	414	1.6	529	14	11	290
P6KE300A	P6KE300CA	5	256	285	300	315	1	414	1.6	529	14	11	290
P6KE320P	P6KE320CP	5	273	304	320	352	1	438	1.6	564	14	11	280
P6KE320A	P6KE320CA	5	273	304	320	336	1	438	1.6	564	14	11	280
P6KE350P	P6KE350CP	5	299	332	350	385	1	482	1.6	618	14	11	270
P6KE350A	P6KE350CA	5	299	332	350	368	1	482	1.6	618	14	11	270
P P6KE400P	P P6KE400CP	5	342	380	400	440	1	548	1.3	706	11	11	360
P6KE400A	P6KE400CA	5	342	380	400	420	1	548	1.3	706	11	11	360
P P6KE440P	P6KE440CP	5	376	418	440	484	1	603	1.3	776	11	11	350
P6KE440A	P6KE440CA	5	376	418	440	462	1	603	1.3	776	11	11	350

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

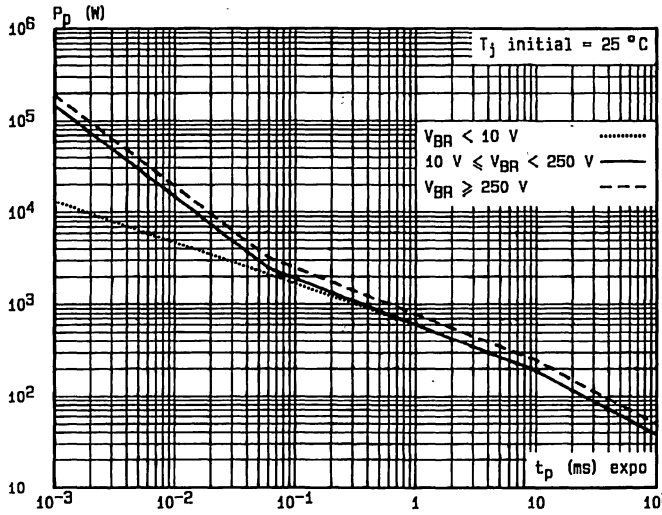


Fig.1 - Peak pulse power versus exponential pulse duration.

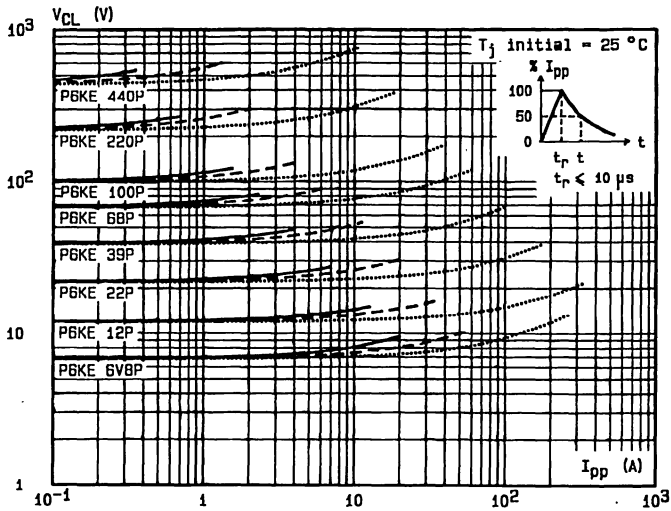


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms - - -
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

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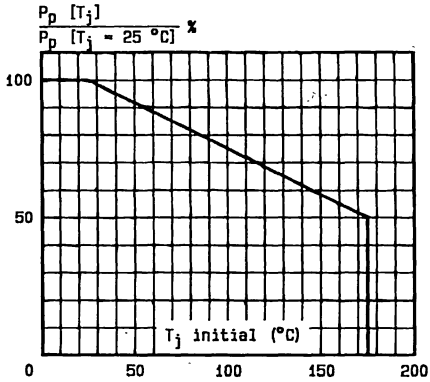


Fig.3 - Allowable power dissipation versus junction temperature.

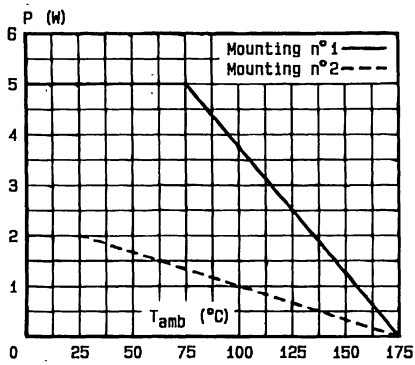


Fig.4 - Power dissipation versus ambient temperature.

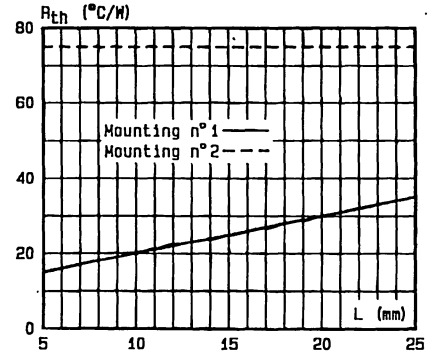
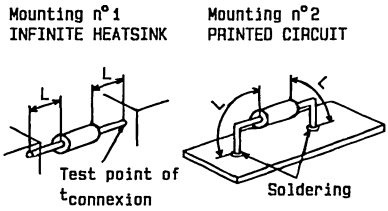


Fig.5 - Thermal resistance versus lead length.



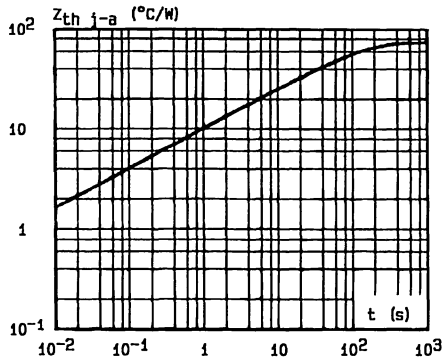


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

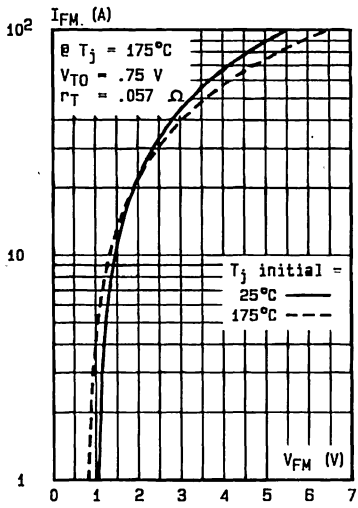


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88P6KEP5

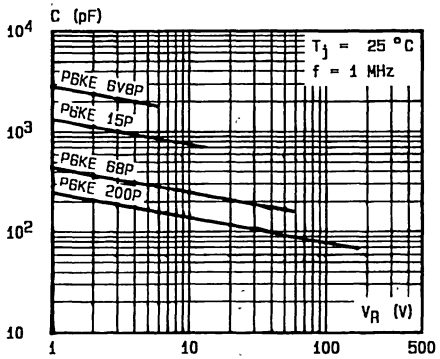


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

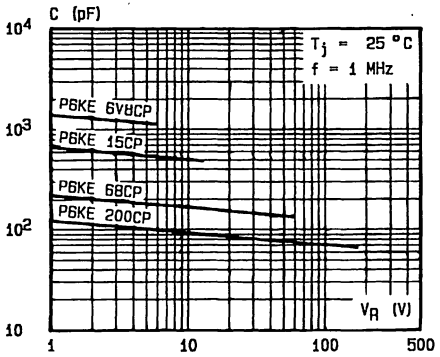
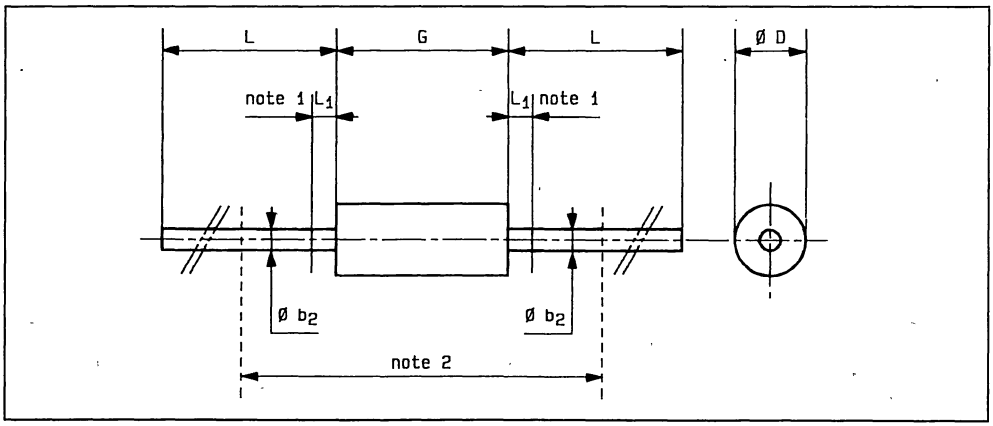


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88P6KEP6

PACKAGE MECHANICAL DATA

CB-417 Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.092	–	0.043	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	–	3.683	–	0.145	
G	–	8.89	–	0.350	
L	25.4	–	1.000	–	
L_1	–	1.25	–	0.049	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.6 g.

SGS-THOMSON MICROELECTRONICS

P7T-10, B → 110, B

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 700 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 10 V → 110 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES

CB-417
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

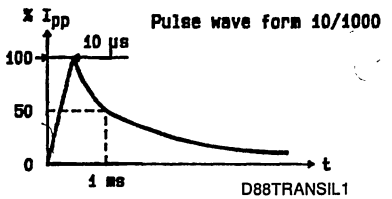
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	700	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	120	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 55 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P7T-10	P7T-10B	5	10	13	18	20	5	25	30	32	265	8.4	2600
P7T-27	P7T-27B	5	27	29.6	36	43.5	5	53	13	68	125	9.6	1100
P7T-43	P7T-43B	5	43	50	62	75	5	90	8	115	74	10.3	620
P7T-110	P7T-110B	5	110	130	160	200	5	235	3	300	28	10.8	370

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

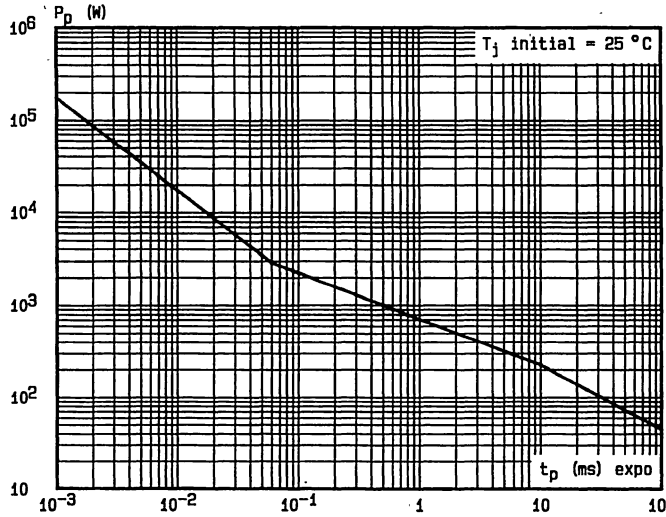


Fig.1 - Peak pulse power versus exponential pulse duration.

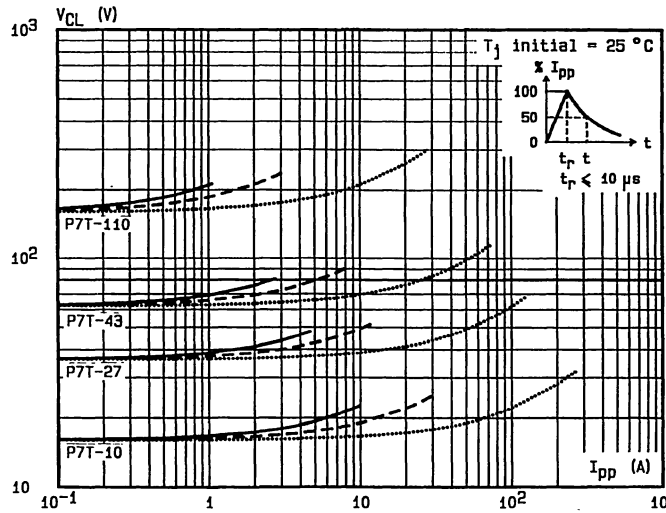


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88P7TP3

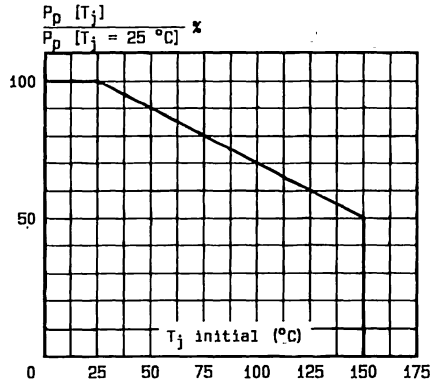


Fig.3 - Allowable power dissipation versus junction temperature.

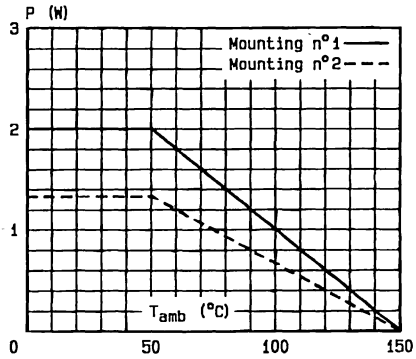


Fig.4 - Power dissipation versus ambient temperature.

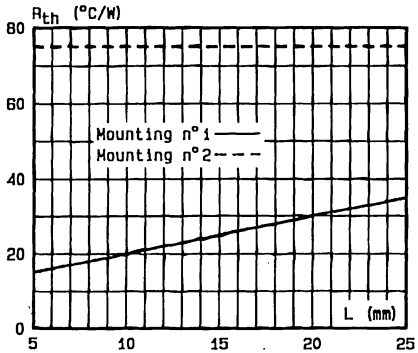
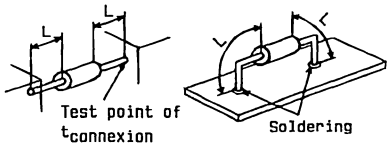


Fig.5 - Thermal resistance versus lead length.

Mounting n°1
INFINITE HEATSINK

Mounting n°2
PRINTED CIRCUIT



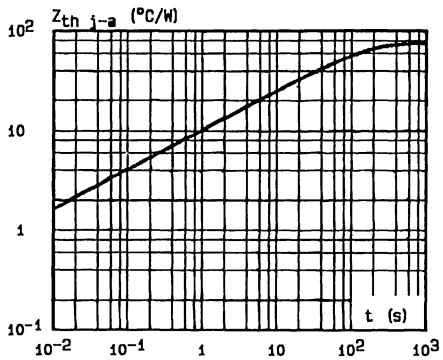


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

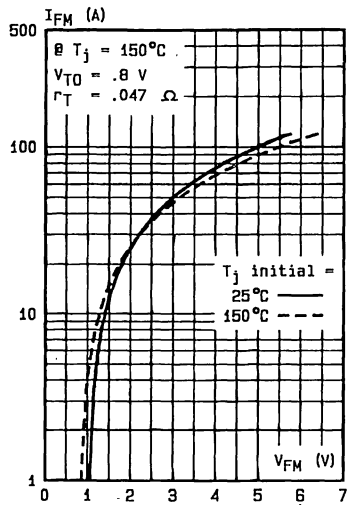


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88P7TP4

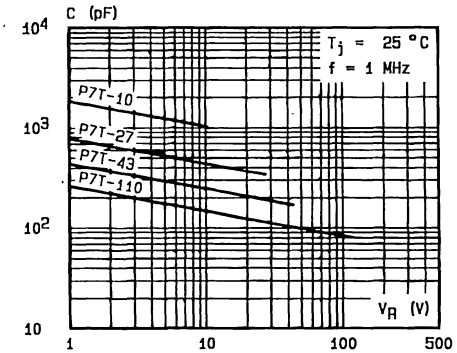


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

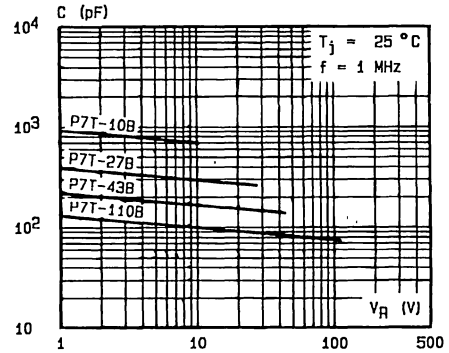
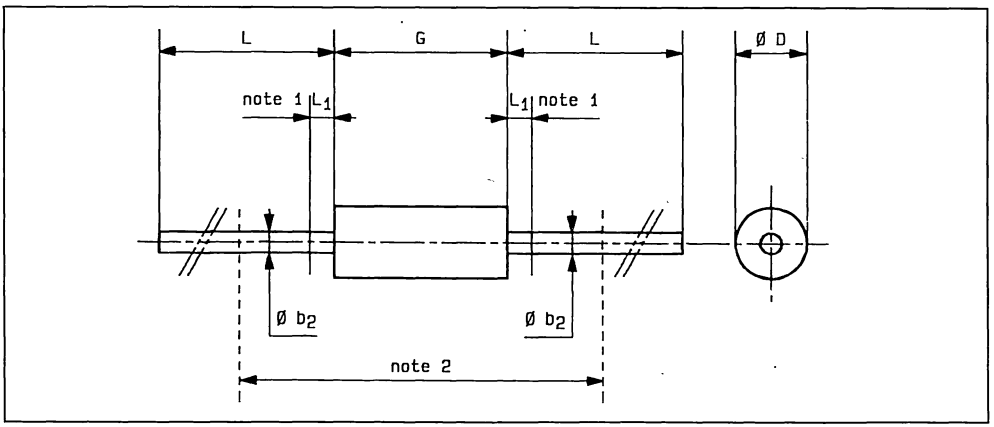


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88P7TP5

PACKAGE MECHANICAL DATA

CB-417 Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.092	–	0.043	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.59" (15 mm).
Ø D	–	3.683	–	0.145	
G	–	8.89	–	0.350	
L	25.4	–	1.000	–	
L_1	–	1.25	–	0.049	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.6 g.

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY :
  1.5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME :
  1 ps FOR UNIDIRECTIONAL TYPES
  5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE :
  5.8 V → 376 V
- ORDER CODE :
  TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

CB-429
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

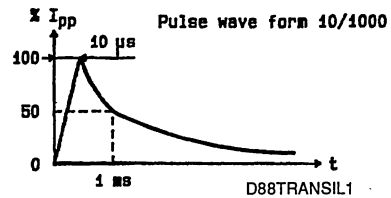
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	1.5	kW
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	250	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 175	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
P 1.5KE6V8P	P 1.5KE6V8CP	1000§	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
1.5KE6V8A	1.5KE6V8CA	1000§	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
P 1.5KE7V5P	1.5KE7V5CP	500§	6.4	7.13	7.5	8.25	10	11.3	132	14.5	690	6.1	8500
1.5KE7V5A	1.5KE7V5CA	500§	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
1.5KE8V2P	1.5KE8V2CP	200§	7.02	7.79	8.2	9.02	10	12.1	124	15.5	645	6.5	8000
1.5KE8V2A	1.5KE8V2CA	200§	7.02	7.79	8.2	8.61	10	12.1	124	15.5	645	6.5	8000
1.5KE9V1P	1.5KE9V1CP	50§	7.78	8.65	9.1	10	1	13.4	112	17.1	585	6.8	7500
1.5KE9V1A	1.5KE9V1CA	50§	7.78	8.65	9.1	9.55	1	13.4	112	17.1	585	6.8	7500
P 1.5KE10P	1.5KE10CP	10§	8.55	9.5	10	11	1	14.5	103	18.6	968	7.3	7000
1.5KE10A	1.5KE10CA	10§	8.55	9.5	10	10.5	1	14.5	103	18.6	968	7.3	7000
1.5KE11P	1.5KE11CP	5§	9.4	10.5	11	12.1	1	15.6	96	20.3	887	7.5	6400
1.5KE11A	1.5KE11CA	5§	9.4	10.5	11	11.6	1	15.6	96	20.3	887	7.5	6400
P 1.5KE12P	P 1.5KE12CP	5	10.2	11.4	12	13.2	1	16.7	90	21.7	829	7.8	6000
1.5KE12A	1.5KE12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	829	7.8	6000
P 1.5KE13P	1.5KE13CP	5	11.1	12.4	13	14.3	1	18.2	82	23.6	763	8.1	5500
1.5KE13A	1.5KE13CA	5	11.1	12.4	13	13.7	1	18.2	82	23.6	763	8.1	5500
1.5KE15P	1.5KE15CP	5	12.8	14.3	15	16.5	1	21.2	71	27.2	662	8.4	5000
1.5KE15A	1.5KE15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	662	8.4	5000
P 1.5KE16P	1.5KE16CP	5	13.6	15.2	16	17.6	1	22.5	67	28.9	623	8.6	4700
1.5KE16A	1.5KE16CA	5	13.6	15.2	16	16.8	1	22.5	67	28.9	623	8.6	4700
P 1.5KE18P	P 1.5KE18CP	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	554	8.8	4300
1.5KE18A	1.5KE18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	554	8.8	4300
P 1.5KE20P	P 1.5KE20CP	5	17.1	19	20	22	1	27.7	54	36.1	498	9.0	4000
1.5KE20A	1.5KE20CA	5	17.1	19	20	21	1	27.7	54	36.1	498	9.0	4000
P 1.5KE22P	1.5KE22CP	5	18.8	20.9	22	24.2	1	30.6	49	39.3	458	9.2	3700
1.5KE22A	1.5KE22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	458	9.2	3700
1.5KE24P	1.5KE24CP	5	20.5	22.8	24	26.4	1	33.2	45	42.8	421	9.4	3500
1.5KE24A	1.5KE24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	421	9.4	3500
P 1.5KE27P	1.5KE27CP	5	23.1	25.7	27	29.7	1	37.5	40	48.3	373	9.6	3200
1.5KE27A	1.5KE27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	373	9.6	3200
P 1.5KE30P	P 1.5KE30CP	5	25.6	28.5	30	33	1	41.5	36	53.5	336	9.7	2900
1.5KE30A	1.5KE30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	336	9.7	2900
P 1.5KE33P	P 1.5KE33CP	5	28.2	31.4	33	36.3	1	45.7	33	59	305	9.8	2700
1.5KE33A	1.5KE33CA	5	28.2	31.4	33	34.7	1	45.7	33	59	305	9.8	2700
P 1.5KE36P	P 1.5KE36CP	5	30.8	34.2	36	39.6	1	49.9	30	64.3	280	9.9	2500
1.5KE36A	1.5KE36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	280	9.9	2500
P 1.5KE39P	P 1.5KE39CP	5	33.3	37.1	39	42.9	1	53.9	28	69.7	258	10.0	2400

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
§ For bidirectional types 1.5KE6V8CP → 11CA, I_{RM} must be double that specified for unidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
1.5KE39A	1.5KE39CA	5	33.3	37.1	39	41	1	53.9	28	69.7	258	10.0	2400
P 1.5KE43P	1.5KE43CP	5	36.8	40.9	43	47.3	1	59.3	25.3	76.8	234	10.1	2200
1.5KE43A	1.5KE43CA	5	36.8	40.9	43	45.2	1	59.3	25.3	76.8	234	10.1	2200
P 1.5KE47P	P 1.5KE47CP	5	40.2	44.7	47	51.7	1	64.8	23.2	84	214	10.1	2050
1.5KE47A	1.5KE47CA	5	40.2	44.7	47	49.4	1	64.8	23.2	84	214	10.1	2050
P 1.5KE51P	1.5KE51CP	5	43.6	48.5	51	56.1	1	70.1	21.4	91	198	10.2	1950
1.5KE51A	1.5KE51CA	5	43.6	48.5	51	53.6	1	70.1	21.4	91	198	10.2	1950
1.5KE56P	1.5KE56CP	5	47.8	53.2	56	61.6	1	77	19.5	100	180	10.3	1800
1.5KE56A	1.5KE56CA	5	47.8	53.2	56	58.8	1	77	19.5	100	180	10.3	1800
1.5KE62P	1.5KE62CP	5	53	58.9	62	68.2	1	85	17.7	111	162	10.4	1700
1.5KE62A	1.5KE62CA	5	53	58.9	62	65.1	1	85	17.7	111	162	10.4	1700
P 1.5KE68P	P 1.5KE68CP	5	58.1	64.6	68	74.8	1	92	16.3	121	148	10.4	1550
1.5KE68A	1.5KE68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	148	10.4	1550
1.5KE75P	1.5KE75CP	5	64.1	71.3	75	82.5	1	103	14.6	134	134	10.5	1450
1.5KE75A	1.5KE75CA	5	64.1	71.3	75	78.8	1	103	14.6	134	134	10.5	1450
P 1.5KE82P	P 1.5KE82CP	5	70.1	77.9	82	90.2	1	113	13.3	146	123	10.5	1350
1.5KE82A	1.5KE82CA	5	70.1	77.9	82	86.1	1	113	13.3	146	123	10.5	1350
1.5KE91P	1.5KE91CP	5	77.8	86.5	91	100	1	125	12	162	111	10.6	1250
1.5KE91A	1.5KE91CA	5	77.8	86.5	91	95.5	1	125	12	162	111	10.6	1250
1.5KE100P	1.5KE100CP	5	85.5	95	100	110	1	137	11	178	101	10.6	1150
1.5KE100A	1.5KE100CA	5	85.5	95	100	105	1	137	11	178	101	10.6	1150
1.5KE110P	P 1.5KE110CP	5	94	105	110	121	1	152	9.9	195	92	10.7	1050
1.5KE110A	1.5KE110CA	5	94	105	110	116	1	152	9.9	195	92	10.7	1050
1.5KE120P	1.5KE120CP	5	102	114	120	132	1	165	9.1	212	85	10.7	1000
1.5KE120A	1.5KE120CA	5	102	114	120	126	1	165	9.1	212	85	10.7	1000
1.5KE130P	P 1.5KE130CP	5	111	124	130	143	1	179	8.4	230	78	10.7	950
1.5KE130A	1.5KE130CA	5	111	124	130	137	1	179	8.4	230	78	10.7	950
1.5KE150P	1.5KE150CP	5	128	143	150	165	1	207	7.2	265	68	10.8	850
1.5KE150A	1.5KE150CA	5	128	143	150	158	1	207	7.2	265	68	10.8	850
1.5KE160P	1.5KE160CP	5	136	152	160	176	1	219	6.8	282	64	10.8	800
1.5KE160A	1.5KE160CA	5	136	152	160	168	1	219	6.8	282	64	10.8	800
P 1.5KE170P	1.5KE170CP	5	145	161	170	187	1	234	6.4	301	60	10.8	750
1.5KE170A	1.5KE170CA	5	145	161	170	179	1	234	6.4	301	60	10.8	750
P 1.5KE180P	P 1.5KE180CP	5	154	171	180	198	1	246	6.1	317	57	10.8	725
1.5KE180A	1.5KE180CA	5	154	171	180	189	1	246	6.1	317	57	10.8	725
P 1.5KE200P	P 1.5KE200CP	5	171	190	200	220	1	274	5.5	353	51	10.8	675
1.5KE200A	1.5KE200CA	5	171	190	200	210	1	274	5.5	353	51	10.8	675
1.5KE220P	P 1.5KE220CP	5	188	209	220	242	1	328	4.6	388	46.5	10.8	625
1.5KE220A	1.5KE220CA	5	188	209	220	231	1	328	4.6	388	46.5	10.8	625
P 1.5KE250P	P 1.5KE250CP	5	213	237	250	275	1	344	5.0	442	47	11	560
1.5KE250A	1.5KE250CA	5	213	237	250	263	1	344	5.0	442	47	11	560
1.5KE280P	1.5KE280CP	5	239	266	280	308	1	384	5.0	494	47	11	520
1.5KE280A	1.5KE280CA	5	239	266	280	294	1	384	5.0	494	47	11	520
P 1.5KE300P	P 1.5KE300CP	5	256	285	300	330	1	414	5.0	529	47	11	500
1.5KE300A	1.5KE300CA	5	256	285	300	315	1	414	5.0	529	47	11	500
1.5KE320P	1.5KE320CP	5	273	304	320	352	1	438	4.5	564	42	11	460
1.5KE320A	1.5KE320CA	5	273	304	320	336	1	438	4.5	564	42	11	460
P 1.5KE350P	P 1.5KE350CP	5	299	332	350	385	1	482	4.0	618	37	11	430
1.5KE350A	1.5KE350CA	5	299	332	350	368	1	482	4.0	618	37	11	430
P 1.5KE400P	P 1.5KE400CP	5	342	380	400	440	1	548	4.0	706	37	11	390
1.5KE400A	1.5KE400CA	5	342	380	400	420	1	548	4.0	706	37	11	390
P 1.5KE440P	P 1.5KE440CP	5	376	418	440	484	1	603	3.5	776	33	11	360
1.5KE440A	1.5KE440CA	5	376	418	440	462	1	603	3.5	776	33	11	360

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.
P : Preferred device.

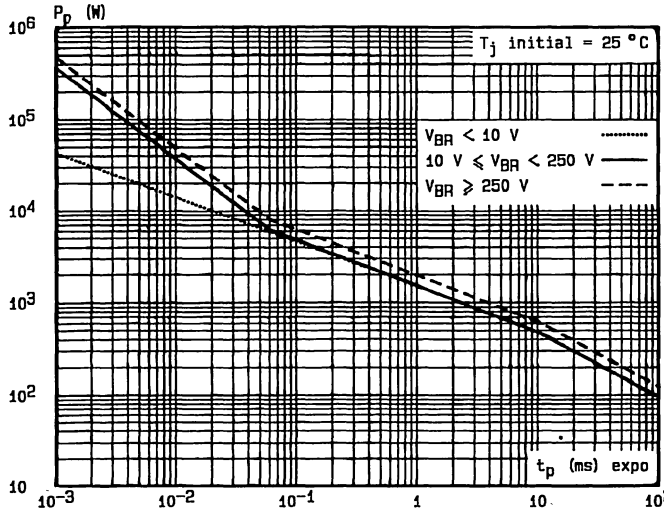


Fig.1 - Peak pulse power versus exponential pulse duration.

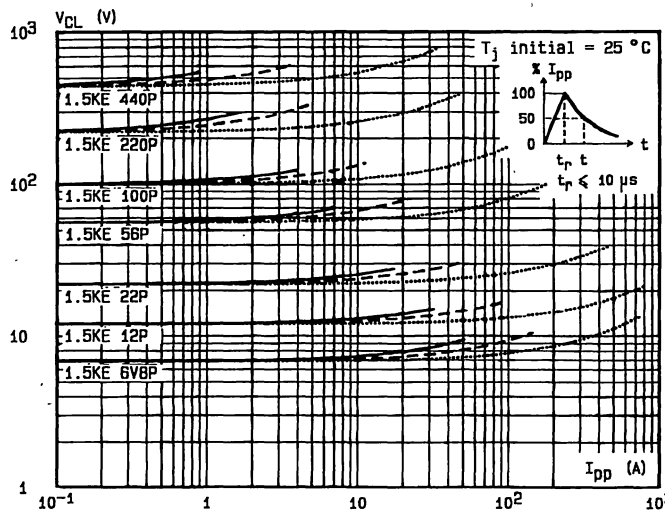


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms - - -
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D881.5KEP4

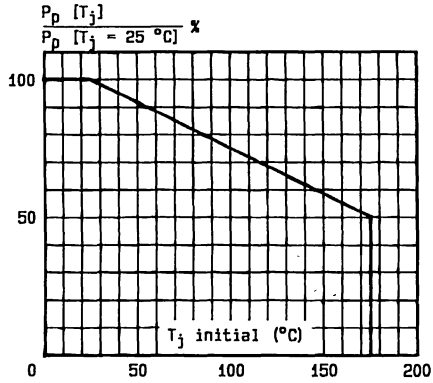


Fig.3 - Allowable power dissipation versus junction temperature.

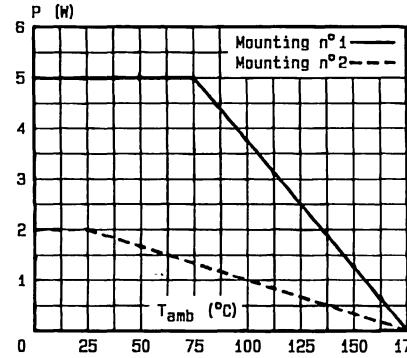


Fig.4 - Power dissipation versus ambient temperature.

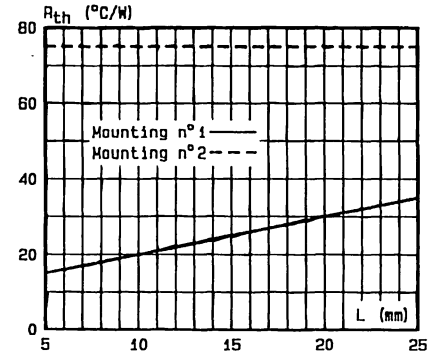
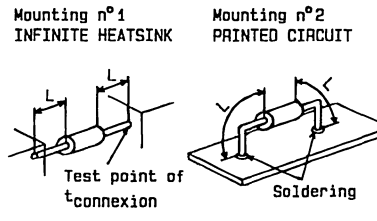


Fig.5 - Thermal resistance versus lead length.



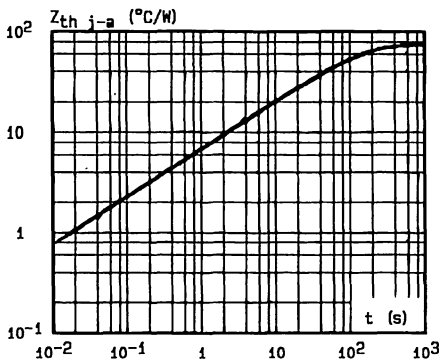


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

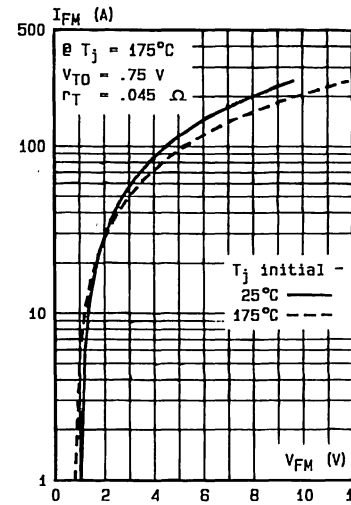


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D881.5KEP5

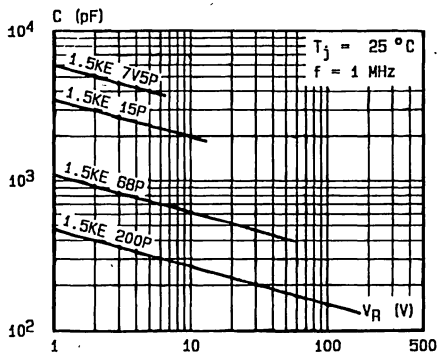


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

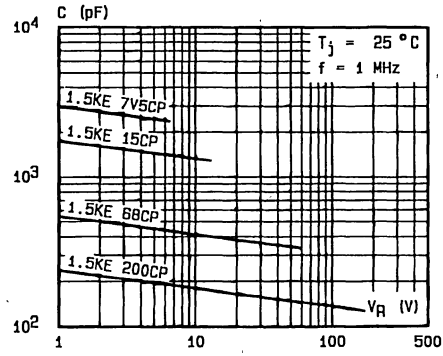
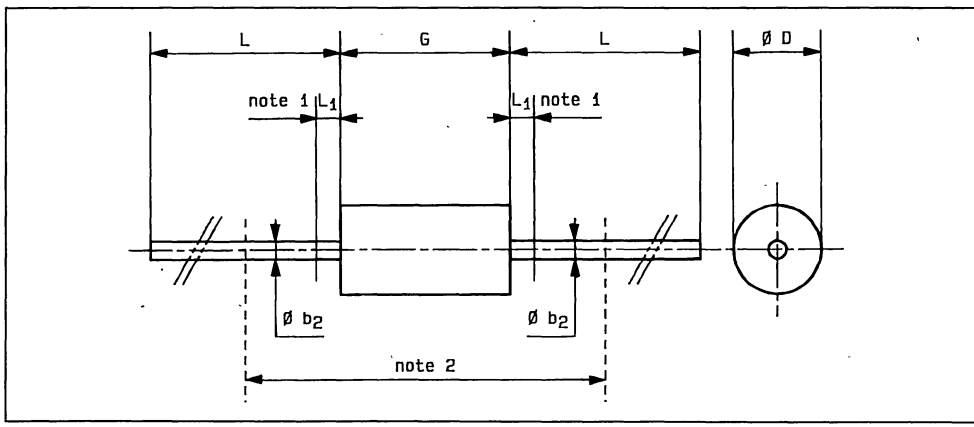


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D881.5KEP6

PACKAGE MECHANICAL DATA

CB-429 Plastic



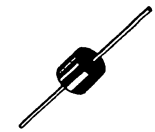
Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	–	1.06	–	0.042	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.70" (18 mm).
Ø D	–	5.1	–	0.20	
G	–	9.8	–	0.386	
L	26	–	1.024	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 0.9 g.

BZW50-10,B → 180, B

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 10 V → 180 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX B FOR BIDIRECTIONAL TYPES



AG
(Plastic)

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

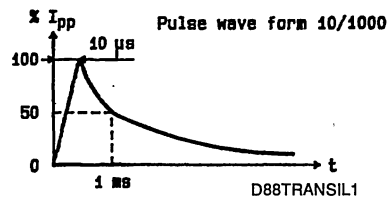
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	5	kW
P	Power Dissipation on Infinite Heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	500	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink for L_{lead} = 10 mm	15	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1 ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20 µs expo		α_T max.	C** typ. V_R=0 f=1 MHz
Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
BZW50-10	BZW50-10B	5	10	11.1	12.4	13.6	1	18.8	266	23.4	2564	7.8	24000
BZW50-12	BZW50-12B	5	12	13.3	14.8	16.3	1	22	227	28	2143	8.4	18500
BZW50-15	BZW50-15B	5	15	16.6	18.5	20.4	1	26.9	186	35	1714	8.8	13500
BZW50-18	BZW50-18B	5	18	20	22.2	24.4	1	32.2	155	41.5	1446	9.2	11500
BZW50-22	BZW50-22B	5	22	24.4	27.1	29.8	1	39.4	127	51	1177	9.6	8500
BZW50-27	BZW50-27B	5	27	30	33.3	36.6	1	48.3	103	62	968	9.8	7000
BZW50-33	BZW50-33B	5	33	36.6	40.7	44.7	1	59	85	76	789	10	5750
BZW50-39	BZW50-39B	5	39	43.3	48.1	53	1	69.4	72	90	667	10.1	4800
BZW50-47	BZW50-47B	5	47	52	57.8	63.6	1	83.2	60.1	108	556	10.3	4100
BZW50-56	BZW50-56B	5	56	62.2	69.1	76	1	99.6	50	129	465	10.4	3400
BZW50-68	BZW50-68B	5	68	75.6	84	92.4	1	121	41	157	382	10.5	3000
BZW50-82	BZW50-82B	5	82	91	101.2	111	1	145	34	189	317	10.6	2600
BZW50-100	BZW50-100B	5	100	111	123.5	136	1	179	28	228	263	10.7	2300
BZW50-120	BZW50-120B	5	120	133	148.1	163	1	215	23	274	219	10.8	1900
BZW50-150	BZW50-150B	5	150	166	185.2	204	1	269	19	343	175	10.8	1700
BZW50-180	BZW50-180B	5	180	200	222	244	1	322	16	410	146	10.8	1500

* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

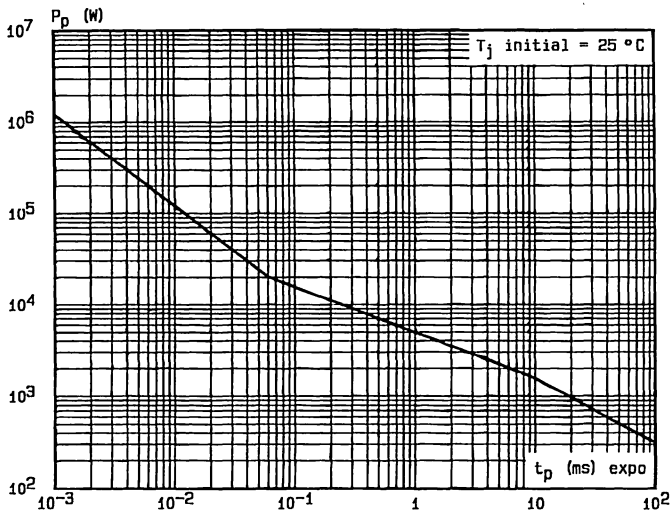


Fig.1 - Peak pulse power versus exponential pulse duration.

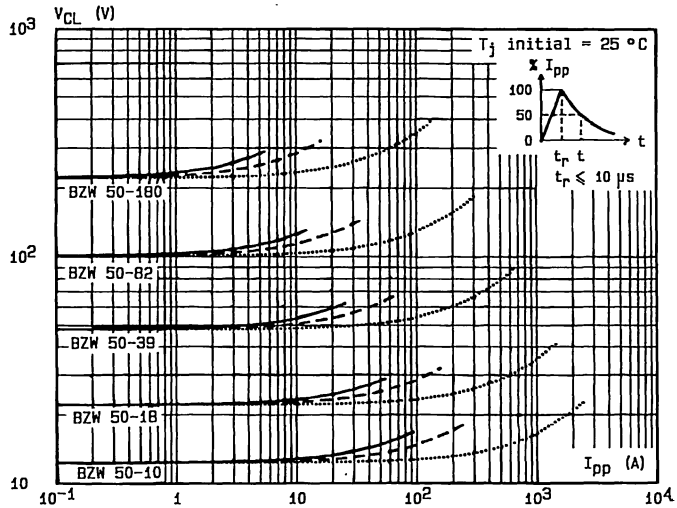


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·
t = 1 ms - - - -
t = 10 ms ———

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88BZW50P3

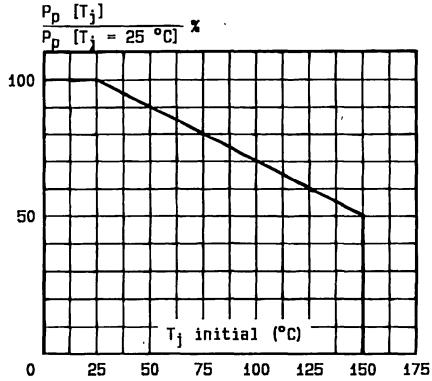


Fig.3 - Allowable power dissipation versus junction temperature.

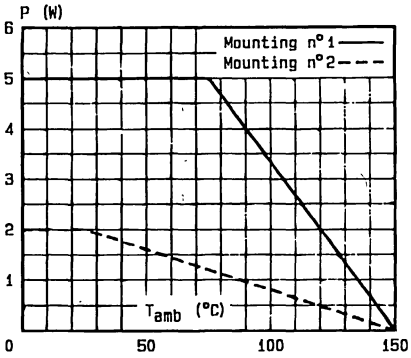


Fig.4 - Power dissipation versus ambient temperature.

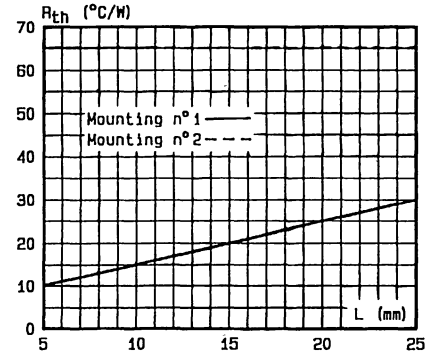
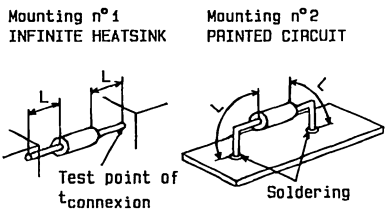


Fig.5 - Thermal resistance versus lead length.



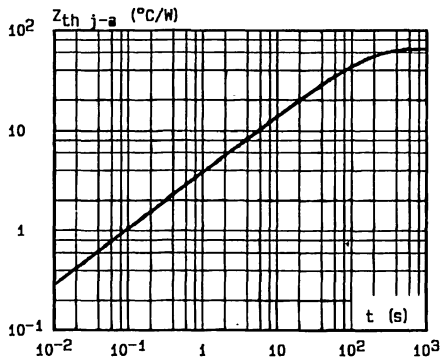


Fig.6 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).

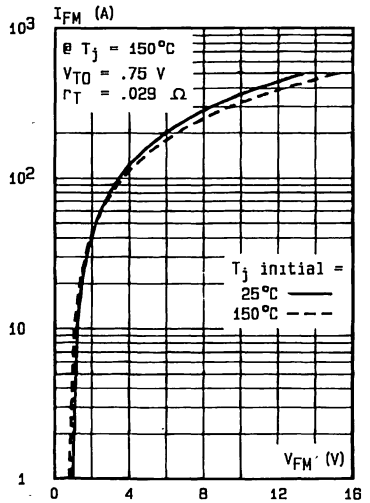


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88BZW50P4

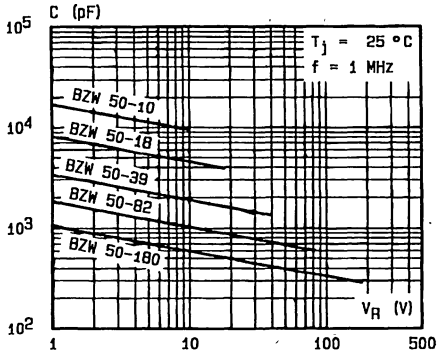


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

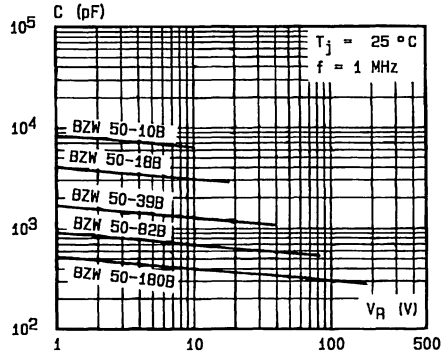
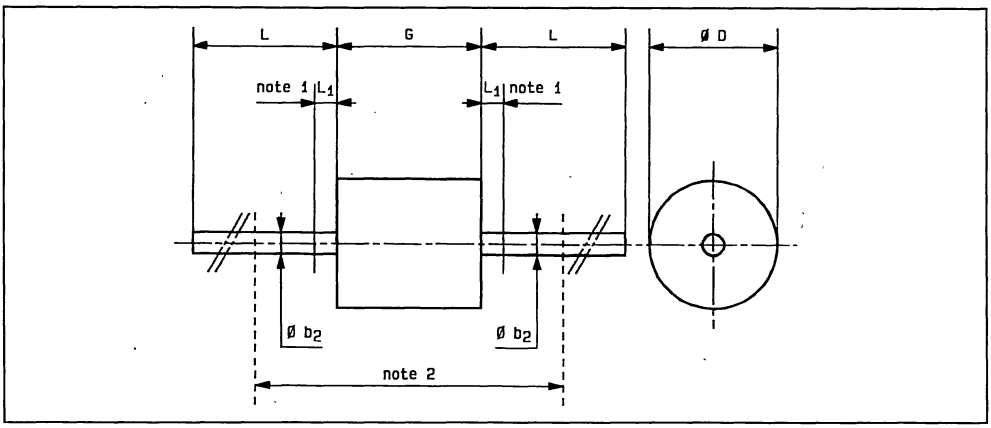


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88BZW50P5

PACKAGE MECHANICAL DATA

AG Plastic



Ref.	Millimeters		Inches		Notes
	Min.	Max.	Min.	Max.	
Ø b_2	1.35	1.45	0.053	0.057	1 - The lead diameter Ø b_2 is not controlled over zone L_1. 2 - The minimum axial lengh within which the device may be placed with its leads bent at right angles is 0.79" (20 mm).
Ø D	–	8	–	0.315	
G	–	9	–	0.354	
L	20	–	0.787	–	
L_1	–	1.27	–	0.050	

Cooling method : by convection (method A).
Marking : type number ; white band indicates cathode for unidirectional types.
Weight : 1 g.

SGS-THOMSON MICROELECTRONICS

SM6T6V8, A → 220, A
SM6T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY : 600 W / 1 ms EXPO
- VERY FAST CLAMPING TIME : 1 ps FOR UNIDIRECTIONAL TYPES 5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE : 5.5 V → 188 V
- ORDER CODE : TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 6
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

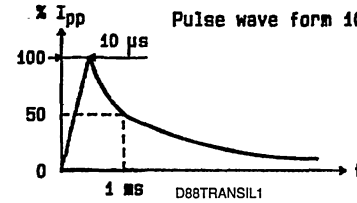
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	600	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.2	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	50	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	20	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



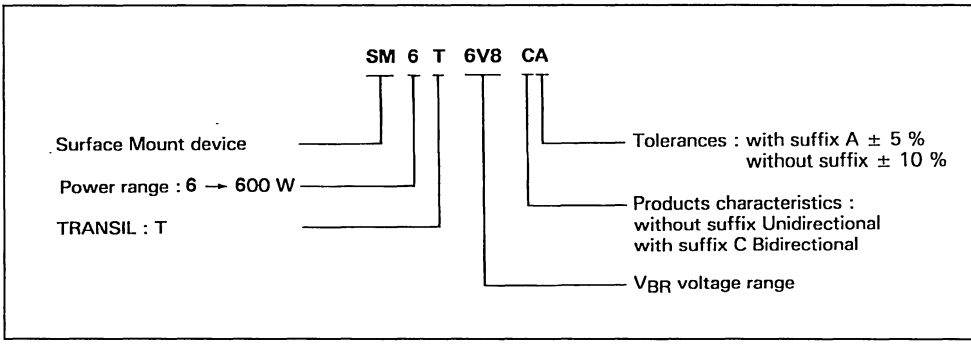
ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM6T6V8	SM6T6V8C	DD	LD	1000	5.5	6.12	6.8	7.48	10	10.8	55	14	250	5.7	4000
SM6T6V8A	SM6T6V8CA	DE	LE	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	261	5.7	4000
SM6T7V5	SM6T7V5C	DF	LF	500	6.05	6.75	7.5	8.25	10	11.7	51	15.2	230	6.1	3700
SM6T7V5A	SM6T7V5CA	DG	LG	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	241	6.1	3700
SM6T10	SM6T10C	DN	LN	10	8.1	9.0	10	11	1	15	40	19.5	369	7.3	2800
SM6T10A	SM6T10CA	DP	LP	10	8.55	9.5	10	10.5	1	14.5	41	18.6	387	7.3	2800
SM6T12	SM6T12C	DS	LS	5	9.72	10.8	12	13.2	1	17.3	35	22.7	317	7.8	2300
SM6T12A	SM6T12CA	DT	LT	5	10.2	11.4	12	12.6	1	16.7	36	21.7	332	7.8	2300
SM6T15	SM6T15C	DW	LW	5	12.1	13.5	15	16.5	1	22	27.5	28.4	254	8.4	1900
SM6T15A	SM6T15CA	DX	LX	5	12.8	14.3	15	15.8	1	21.2	28	27.2	265	8.4	1900
SM6T18	SM6T18C	ED	MD	5	14.5	16.2	18	19.8	1	26.5	22.5	34	212	8.8	1600
SM6T18A	SM6T18CA	EE	ME	5	15.3	17.1	18	18.9	1	25.2	24	32.5	222	8.8	1600
SM6T22	SM6T22C	EH	MH	5	17.8	19.8	22	24.2	1	31.9	18.5	41.2	175	9.2	1350
SM6T22A	SM6T22CA	EK	MK	5	18.8	20.9	22	23.1	1	30.6	20	39.3	183	9.2	1350
SM6T24	SM6T24C	EL	ML	5	19.4	21.6	24	26.4	1	34.7	17.5	44.9	160	9.4	1250
SM6T24A	SM6T24CA	EM	MM	5	20.5	22.8	24	25.2	1	33.2	18	42.8	168	9.4	1250
SM6T27	SM6T27C	EN	MN	5	21.8	24.3	27	29.7	1	39.1	15.5	50.5	143	9.6	1150
SM6T27A	SM6T27CA	EP	MP	5	23.1	25.7	27	28.4	1	37.5	16	48.3	149	9.6	1150
SM6T30	SM6T30C	EQ	MQ	5	24.3	27	30	33	1	43.5	13.5	56.1	128	9.7	1075
SM6T30A	SM6T30CA	ER	MR	5	25.6	28.5	30	31.5	1	41.4	14.5	53.5	134	9.7	1075
SM6T33	SM6T33C	ES	MS	5	26.8	29.7	33	36.3	1	47.7	12.5	61.7	117	9.8	1000
SM6T33A	SM6T33CA	ET	MT	5	28.2	31.4	33	34.7	1	45.7	13.1	59	122	9.8	1000
SM6T36	SM6T36C	EU	MU	5	29.1	32.4	36	39.6	1	52	11.5	67.3	107	9.9	950
SM6T36A	SM6T36CA	EV	MV	5	30.8	34.2	36	37.8	1	49.9	12	64.3	112	9.9	950
SM6T39	SM6T39C	EW	MW	5	31.6	35.1	39	42.9	1	56.4	10.6	73	99	10.0	900
SM6T39A	SM6T39CA	EX	MX	5	33.3	37.1	39	41	1	53.9	11.1	69.7	103	10.0	900
SM6T68	SM6T68C	FP	NP	5	55.1	61.2	68	74.8	1	98	6.1	127	57	10.4	625
SM6T68A	SM6T68CA	FQ	NQ	5	58.1	64.6	68	71.4	1	92	6.5	121	59.5	10.4	625
SM6T100	SM6T100C	FX	NX	5	81	90	100	110	1	144	4.2	187	38.5	10.6	500
SM6T100A	SM6T100CA	FY	NY	5	85.5	95	100	105	1	137	4.4	178	40.5	10.6	500
SM6T150	SM6T150C	GK	OK	5	121	135	150	165	1	215	2.8	277	26	10.8	400
SM6T150A	SM6T150CA	GL	OL	5	128	143	150	158	1	207	2.9	265	27.2	10.8	400
SM6T200	SM6T200C	GT	OT	5	162	180	200	220	1	287	2.1	370	19.4	10.8	350
SM6T200A	SM6T200CA	GU	OU	5	171	190	200	210	1	274	2.2	353	20 4	10.8	350
SM6T220		GV		5	178	198	220	242	1	316	1.9	406	17.7	10.8	330
SM6T220A		GW		5	188	209	220	231	1	301	2	388	18.6	10.8	330

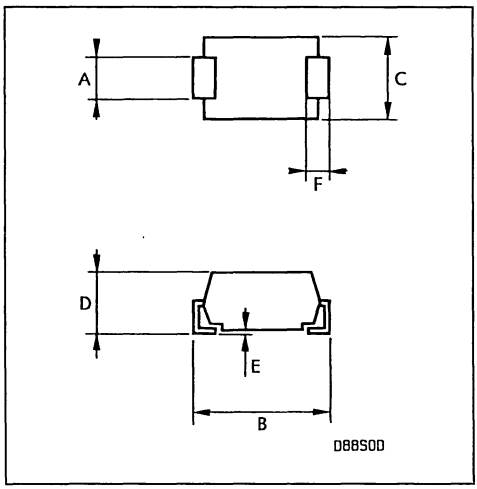
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

ORDER CODE



PACKAGE MECHANICAL DATA

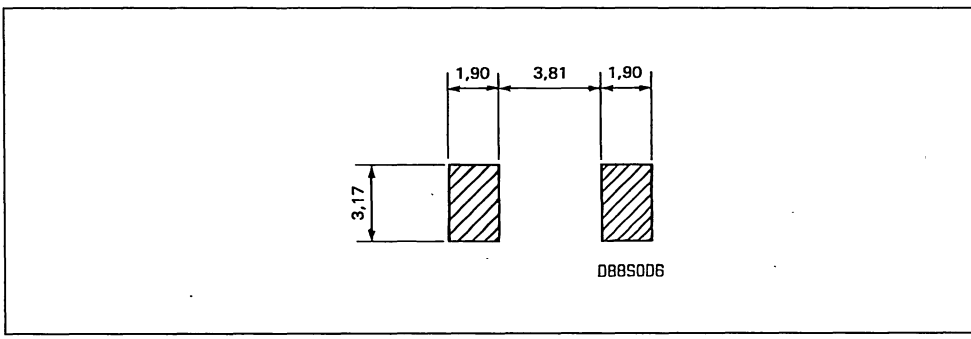
SOD 6 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	6.0	6.4	0.236	0.252
C	3.8	4.2	0.150	0.165
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	0.9	1.3	0.035	0.051

Laser marking.
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



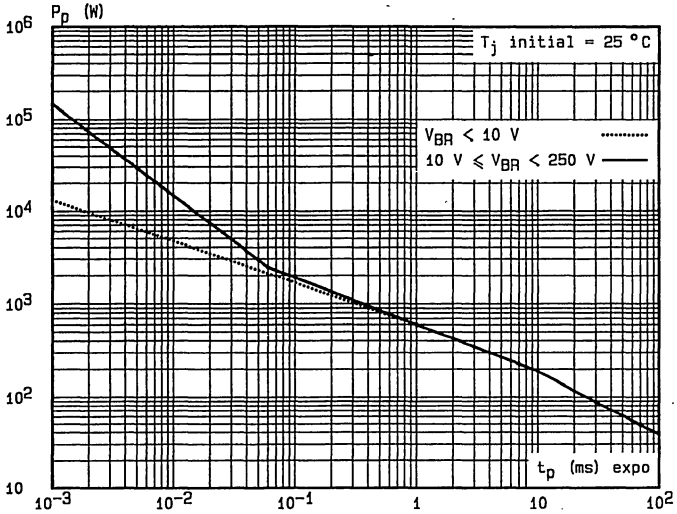


Fig.1 - Peak pulse power versus exponential pulse duration.

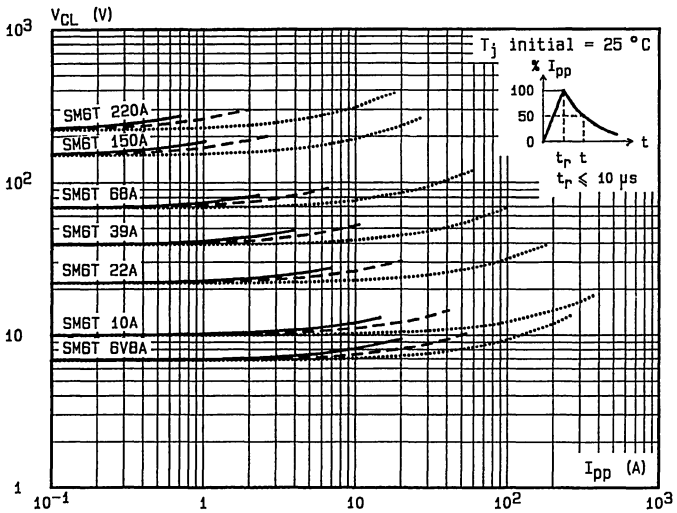


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms - - -
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88SM6TP4

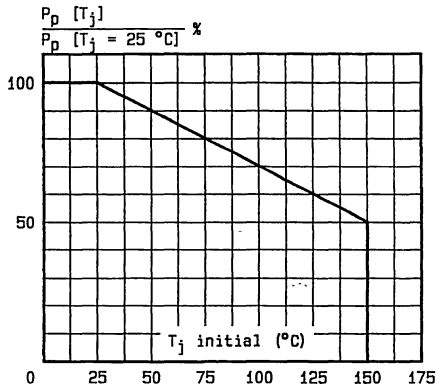


Fig.3 - Allowable power dissipation versus junction temperature.

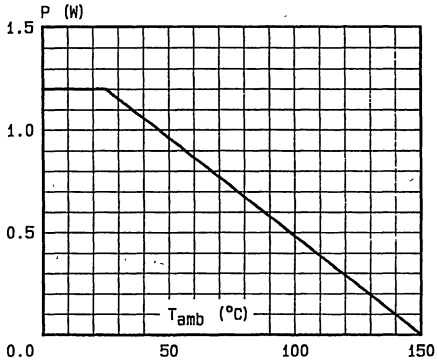


Fig.4 - Power dissipation versus ambient temperature.

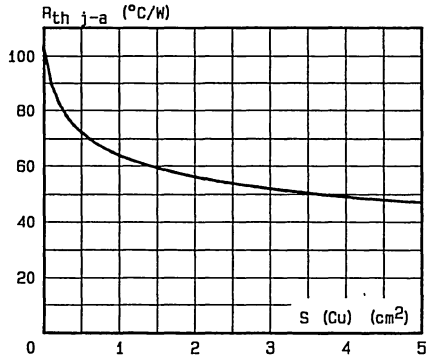


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

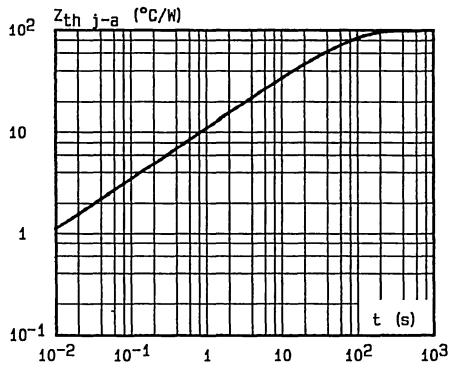


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

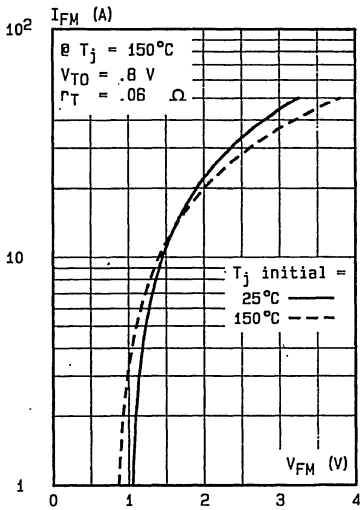


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

D88SM6TP5

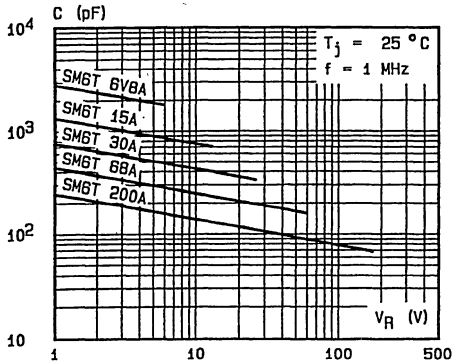


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

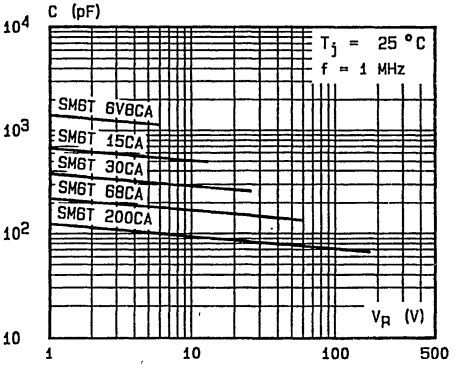


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88SM6TP6

SM15T6V8, A → 220, A
SM15T6V8C, A → 200C, A

UNI-AND BIDIRECTIONAL TRANSIENT VOLTAGE SUPPRESSORS

- HIGH SURGE CAPABILITY :
  1.5 kW / 1 ms EXPO
- VERY FAST CLAMPING TIME :
  1 ps FOR UNIDIRECTIONAL TYPES
  5 ns FOR BIDIRECTIONAL TYPES
- LARGE VOLTAGE RANGE :
  5.5 V → 188 V
- ORDER CODE :
  TYPE NUMBER FOR UNIDIRECTIONAL TYPES, TYPE NUMBER + SUFFIX C FOR BIDIRECTIONAL TYPES

SOD 15
(Plastic)

SURFACE MOUNT TRANSIL FEATURES

- A PERFECT PICK AND PLACE BEHAVIOUR
- AN EXCELLENT ON BOARD STABILITY
- A FULL COMPATIBILITY WITH BOTH GLUING AND PASTE SOLDERING TECHNOLOGIES
- BODY MARKED WITH TYPE CODE AND LOGO
- STANDARD PACKAGING : 12 mm TAPE (EIA STD. RS481)
- TINNED COPPER LEADS
- HIGH TEMPERATURE RESISTANT RESIN

DESCRIPTION

Transient voltage suppressor diodes especially useful in protecting integrated circuits, MOS, hybrids and other voltage-sensitive semiconductors and components.

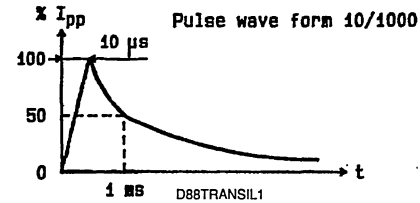
ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak Pulse Power for 1 ms Exponential Pulse	T_j Initial = 25 °C See note 1	1500	W
P	Power Dissipation on Infinite Heatsink	T_{amb} = 25 °C	1.7	W
I_{FSM}	Non Repetitive Surge Peak Forward Current for Unidirectional Types	T_j Initial = 25 °C t = 10 ms	150	A
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 65 to 175 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s		260	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction-leads	10	°C/W

Note : 1. For surges upper than the maximum values, the diode will present a short-circuit anode-cathode.



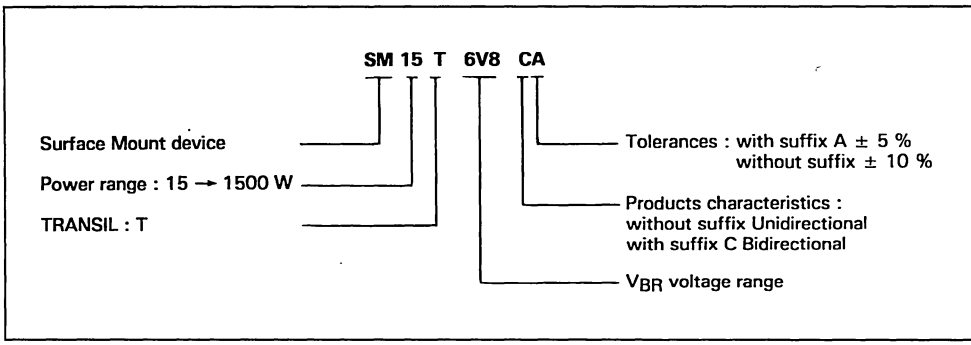
ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

Symbol	Parameter		Value
V_{RM}	Stand-off Voltage		See tables
$V_{(BR)}$	Breakdown Voltage		
$V_{(CL)}$	Clamping Voltage		
I_{pp}	Peak Pulse Current		
α_T	Temperature Coefficient of $V_{(BR)}$		
C	Capacitance		
$t_{clamping}$	Clamping Time (0 volt to $V_{(BR)}$)	Unidirectional Types	1 ps max.
		Bidirectional Types	5 ns max.

Types		Marking		I_{RM} @ V_{RM} max.		$V_{(BR)}$* @ I_R (V)				$V_{(CL)}$ @ I_{pp} max. 1ms expo		$V_{(CL)}$ @ I_{pp} max. 8-20µs expo		α_T max.	C** typ. V_R=0 f=1MHz
Unidirectional	Bidirectional	Unidirectional	Bidirectional	(µA)	(V)	min.	nom.	max.	(mA)	(V)	(A)	(V)	(A)	(10^{-4}/°C)	(pF)
SM15T6V8	SM15T6V8C	MDD	BDD	1000	5.5	6.12	6.8	7.48	10	10.8	139	14	714	5.7	9500
SM15T6V8A	SM15T6V8CA	MDE	BDE	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
SM15T7V5	SM15T7V5C	MDF	BDF	1000	6.05	6.75	7.5	8.25	10	11.7	128	15.2	660	6.1	8500
SM15T7V5A	SM15T7V5CA	MDG	BDG	1000	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
SM15T10	SM15T10C	MDN	BDN	10	8.1	9.0	10	11	1	15	100	19.5	928	7.3	7000
SM15T10A	SM15T10CA	MDP	BDP	10	8.55	9.5	10	10.5	1	14.5	103	18.6	968	7.3	7000
SM15T12	SM15T12C	MDS	BDS	5	9.72	10.8	12	13.2	1	17.3	87	22.7	793	7.8	6000
SM15T12A	SM15T12CA	MDT	BDT	5	10.2	11.4	12	12.6	1	16.7	90	21.7	829	7.8	6000
SM15T15	SM15T15C	MDW	BDW	5	12.1	13.5	15	16.5	1	22	68	28.4	634	8.4	5000
SM15T15A	SM15T15CA	MDX	BDX	5	12.8	14.3	15	15.8	1	21.2	71	27.2	662	8.4	5000
SM15T18	SM15T18C	MED	BED	5	14.5	16.2	18	19.8	1	26.5	56.5	34	529	8.8	4300
SM15T18A	SM15T18CA	MEE	BEE	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	554	8.8	4300
SM15T22	SM15T22C	MEH	BEH	5	17.8	19.8	22	24.2	1	31.9	47	41.2	437	9.2	3700
SM15T22A	SM15T22CA	MEK	BEK	5	18.8	20.9	22	23.1	1	30.6	49	39.3	458	9.2	3700
SM15T24	SM15T24C	MEL	BEL	5	19.4	21.6	24	26.4	1	34.7	43	44.9	401	9.4	3500
SM15T24A	SM15T24CA	MEM	BEM	5	20.5	22.8	24	25.2	1	33.2	45	42.8	421	9.4	3500
SM15T27	SM15T27C	MEN	BEN	5	21.8	24.3	27	29.7	1	39.1	38.5	50.5	356	9.6	3200
SM15T27A	SM15T27CA	MEP	BEP	5	23.1	25.7	27	28.4	1	37.5	40	48.3	373	9.6	3200
SM15T30	SM15T30C	MEQ	BEQ	5	24.3	27	30	33	1	43.5	34.5	56.1	321	9.7	2900
SM15T30A	SM15T30CA	MER	BER	5	25.6	28.5	30	31.5	1	41.4	36	53.5	336	9.7	2900
SM15T33	SM15T33C	MES	BES	5	26.8	29.7	33	36.3	1	47.7	31.5	61.5	292	9.8	2700
SM15T33A	SM15T33CA	MET	BET	5	28.2	31.4	33	34.7	1	45.7	33	59	305	9.8	2700
SM15T36	SM15T36C	MEU	BEU	5	29.1	32.4	36	39.6	1	52	29	67.3	267	9.9	2500
SM15T36A	SM15T36CA	MEV	BEV	5	30.8	34.2	36	37.8	1	49.9	30	64.3	280	9.9	2500
SM15T39	SM15T39C	MEW	BEW	5	31.6	35.1	39	42.9	1	56.4	26.5	73	246	10.0	2400
SM15T39A	SM15T39CA	MEX	BEX	5	33.3	37.1	39	41	1	53.9	28	69.7	258	10.0	2400
SM15T68	SM15T68C	MFN	BFN	5	55.1	61.2	68	74.8	1	98	15.3	127	142	10.4	1550
SM15T68A	SM15T68CA	MFP	BFP	5	58.1	64.6	68	71.4	1	92	16.3	121	148	10.4	1550
SM15T100	SM15T100C	MFW	BFW	5	81	90	100	110	1	144	10.4	187	96	10.6	1150
SM15T100A	SM15T100CA	MFX	BFX	5	85.5	95	100	105	1	137	11	178	101	10.6	1150
SM15T150	SM15T150C	MGH	BGH	5	121	135	150	165	1	215	7	277	65	10.8	850
SM15T150A	SM15T150CA	MGK	BGK	5	128	143	150	158	1	207	7.2	265	68	10.8	850
SM15T200	SM15T200C	MGU	BGU	5	162	180	200	220	1	287	5.2	370	48.5	10.8	675
SM15T200A	SM15T200CA	MGV	BGV	5	171	190	200	210	1	274	5.5	353	51	10.8	675
SM15T220		MGW		5	175	198	220	242	1	344	4.3	406	44.5	10.8	625
SM15T220A		MGX		5	185	209	220	231	1	328	4.6	388	46.5	10.8	625

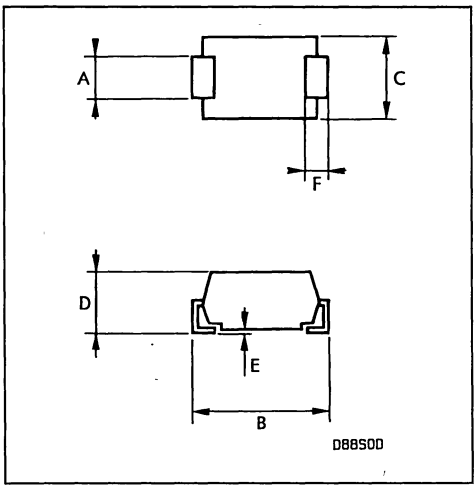
* Pulse test $t_p \leq 50$ ms $\delta < 2$ %.
** Divide these values by 2 for bidirectional types.
For bidirectional types, electrical characteristics apply in both directions.

ORDER CODE



PACKAGE MECHANICAL DATA

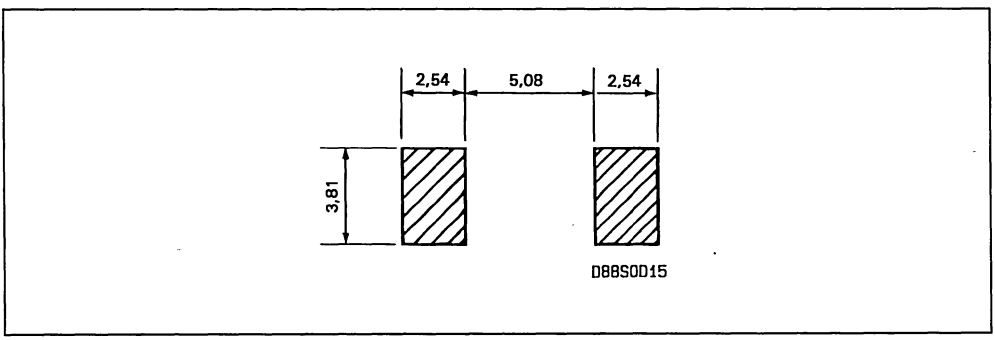
SOD 15 Plastic



Ref.	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	2.8	3.2	0.110	0.126
B	7.6	8.0	0.300	0.315
C	4.8	5.2	0.190	0.200
D	2.5	3.1	0.098	0.122
E	–	0.1	–	0.004
F	1.3	1.7	0.051	0.067

Laser marking.
The logo indicates cathode for unidirectional types.

FOOT PRINT DIMENSIONS (Millimeters)



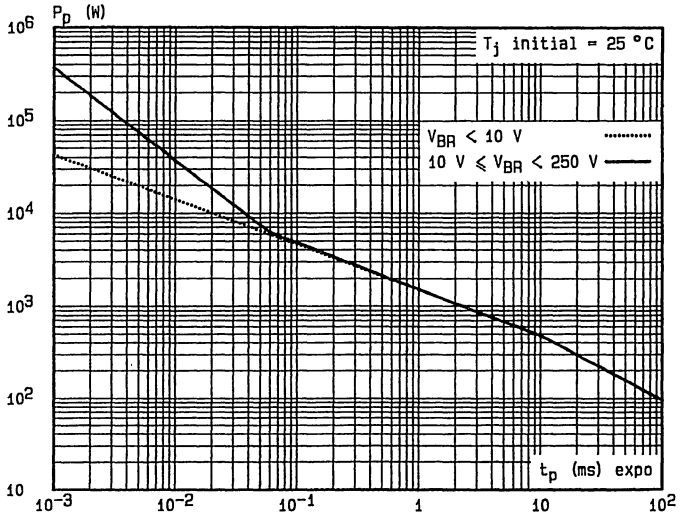


Fig.1 - Peak pulse power versus exponential pulse duration.

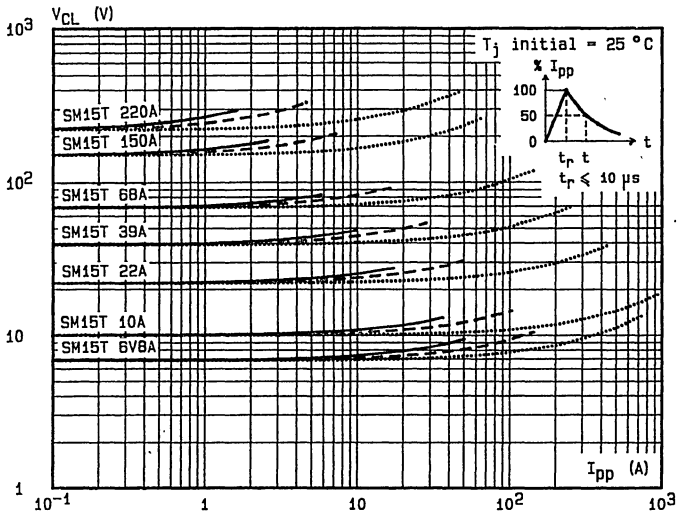


Fig.2 - Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs ·····
t = 1 ms – – –
t = 10 ms ——

Note : The curves of the figure 2 are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula : $\Delta V_{(BR)} = \alpha_{T(V(BR))} \times [T_j - 25] \times V_{(BR)}$
For intermediate voltages, extrapolate the given results.

D88SM15TP4

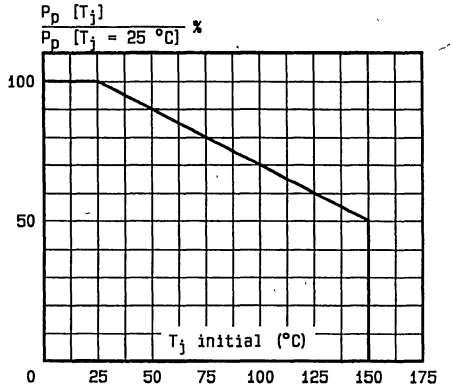


Fig.3 - Allowable power dissipation versus junction temperature.

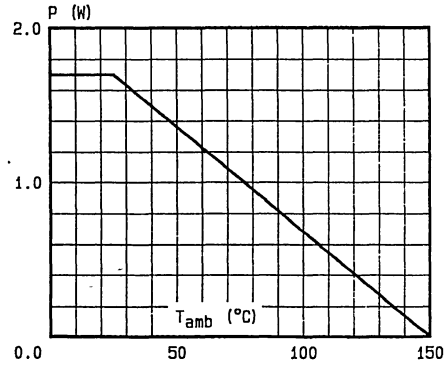


Fig.4 - Power dissipation versus ambient temperature.

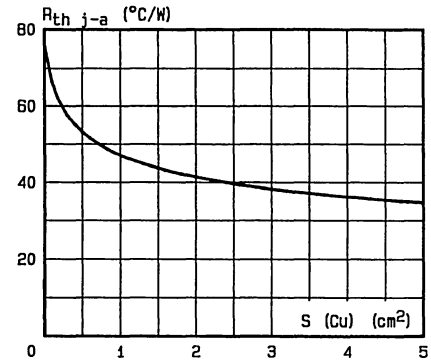


Fig.5 - Thermal resistance junction-ambient versus Cu surface (printed circuit).

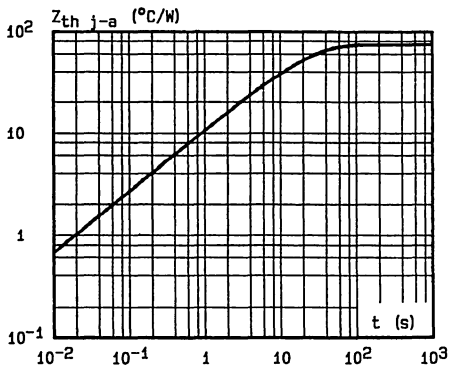


Fig.6 - Transient thermal impedance junction-ambient versus pulse duration.

D88SM15TP5

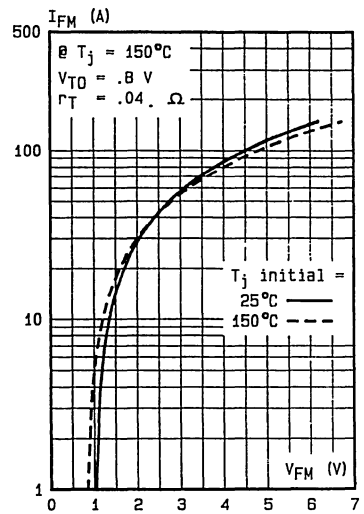


Fig.7 - Peak forward current versus peak forward voltage drop (typical values for unidirectional types).

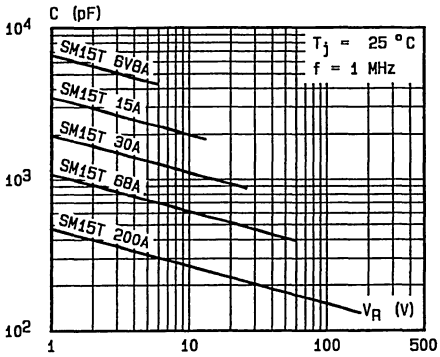


Fig.8a - Capacitance versus reverse applied voltage for unidirectional types (typical values).

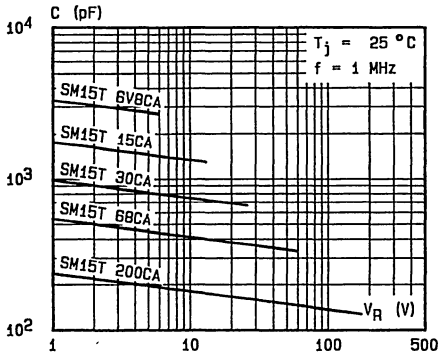
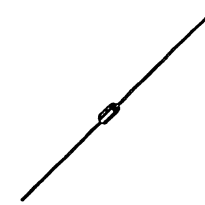


Fig.8b - Capacitance versus reverse applied voltage for bidirectional types (typical values).

D88SM15TP6

TRISIL

- BIDIRECTIONAL DEVICE USED TO **TELEPHONE PROTECTION**
- CHARACTERISTIC OF STAND-OFF AND BREAKDOWN VOLTAGE SIMILAR TO A TRANSIL (V_{off})
- HIGH FLOWOUT CAPABILITY BECAUSE OF ITS BREAKOVER CHARACTERISTIC (V_{on})



F 126
(Plastic)

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C - L = 10 mm)

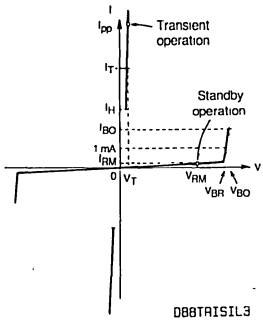
Symbol	Parameter		Value	Unit
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	1.7	W
I_{pp}	Peak Pulse Current	1 ms expo	50	A
		8-20 µs expo	100	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms	30	A
di/dt	Critical Rate of Rise of on-state Current	Non Repetitive	100	A/µs
dv/dt	Critical Rate of Rise of off-state Voltage	67 % $V_{(BR)}$ min	5	kV/µs
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 40 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-l)}$	Junction-leads on Infinite Heatsink	L = 10 mm	60	°C/W
$R_{th(j-a)}$	Junction-ambient on Printed Circuit		100	°C/W

ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage : 2.5 V typ. @ I_T = 1 A (t_p = 300 µs)



Types	I_{RM} @ V_{RM} max.		$V_{(BR)}$ @ I_R min.		V_{BO} max.	I_{BO} max.	I_H min.
	(µA)	(V)	(V)	(mA)	(V)	(mA)	(mA)
TPA62A - 12 or 18	2	56	62	1	82	800	
(1) TPA62B - 12 or 18	2	56	62	1	75	800	
TPA68A - 12 or 18	2	61	68	1	90	800	
(1) TPA68B - 12 or 18	2	61	68	1	82	800	
(1) TPA75A - 12 or 18	2	67	75	1	100	800	
(1) TPA75B - 12 or 18	2	67	75	1	91	800	
(1) TPA82A - 12 or 18	2	74	82	1	109	300	
(1) TPA82B - 12 or 18	2	74	82	1	99	300	
(1) TPA91A - 12 or 18	2	82	91	1	121	300	
(1) TPA91B - 12 or 18	2	82	91	1	110	300	
P TPA100A - 12 or 18	2	90	100	1	133	300	12 Suffix for 120 mA
TPA100B - 12 or 18	2	90	100	1	121	300	
TPA110A - 12 or 18	2	99	110	1	147	300	
TPA110B - 12 or 18	2	99	110	1	133	300	
P TPA120A - 12 or 18	2	108	120	1	160	300	
TPA120B - 12 or 18	2	108	120	1	145	300	
P TPA130A - 12 or 18	2	117	130	1	173	300	
TPA130B - 12 or 18	2	117	130	1	157	300	
(1) TPA150A - 12 or 18	2	135	150	1	200	300	
(1) TPA150B - 12 or 18	2	135	150	1	181	300	18 Suffix for 180 mA
(1) TPA160A - 12 or 18	2	144	160	1	213	300	
(1) TPA160B - 12 or 18	2	144	160	1	193	300	
(1) TPA180A - 12 or 18	2	162	180	1	240	300	
(1) TPA180B - 12 or 18	2	162	180	1	217	300	
(1) TPA200A - 12 or 18	2	180	200	1	267	300	
(1) TPA200B - 12 or 18	2	180	200	1	241	300	
P TPA220A - 12 or 18	2	198	220	1	293	300	
TPA220B - 12 or 18	2	198	220	1	265	300	
P TPA240A - 12 or 18	2	216	240	1	320	300	
TPA240B - 12 or 18	2	216	240	1	289	300	
P TPA270A - 12 or 18	2	243	270	1	360	300	
TPA270B - 12 or 18	2	243	270	1	325	300	

P : Preferred device.
(1) : These volages are on request. Consult us.

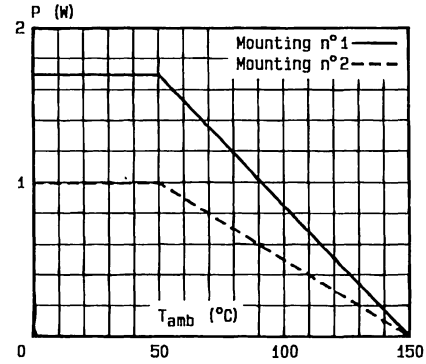


Fig.1 - Power dissipation versus ambient temperature.

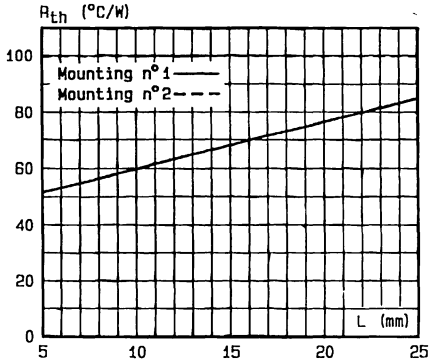


Fig.2 - Thermal resistance versus lead length.

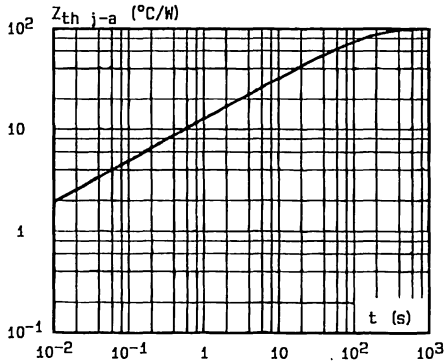
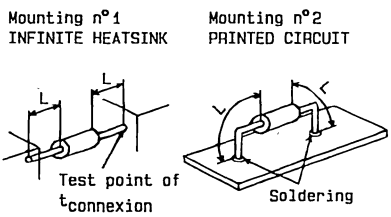


Fig.3 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).



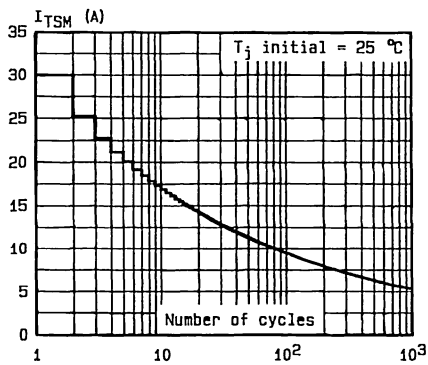


Fig.4 - Non repetitive surge peak on-state current versus number of cycles.

DB8TPAP3

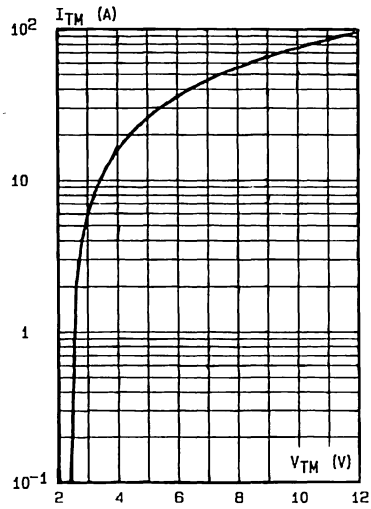


Fig.5 - Peak forward current versus peak forward voltage drop (typical values).

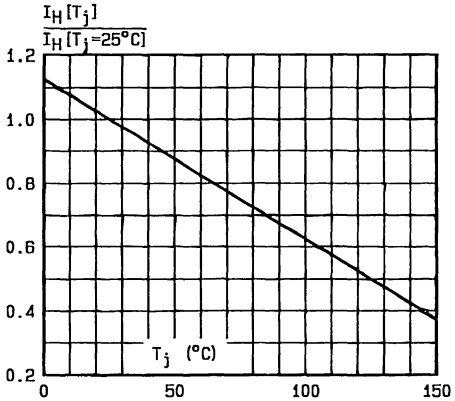


Fig.6 - Relative variation of holding current versus junction temperature.

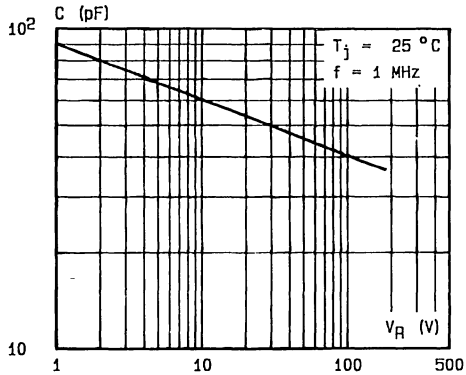
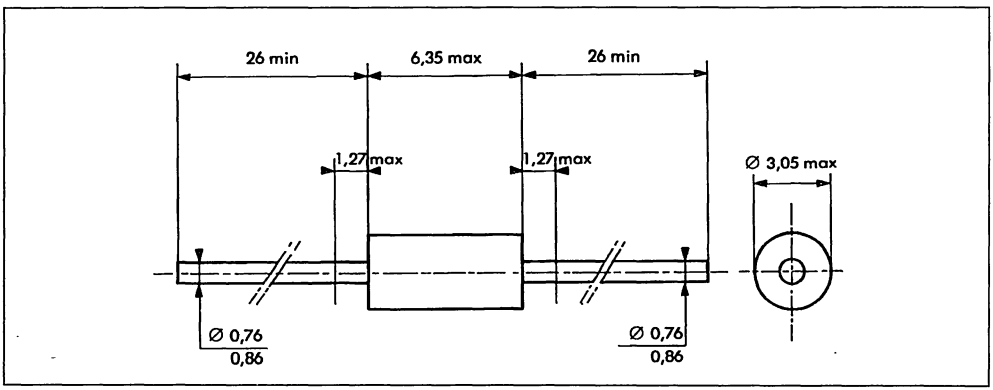


Fig.7 - Capacitance versus reverse applied voltage.

DB8TPAP4

PACKAGE MECHANICAL DATA

F 126 Plastic



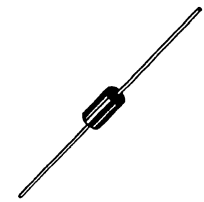
Cooling method : by conduction (method A)
Marking : type number
Weight : 0.4 g

SGS-THOMSON MICROELECTRONICS

TPB SERIES

TRISIL

- BIDIRECTIONAL DEVICE USED TO **TELEPHONE PROTECTION**
- CHARACTERISTIC OF STAND-OFF AND BREAKDOWN VOLTAGE SIMILAR TO A TRANSIL (V_{off})
- HIGH FLOWOUT CAPABILITY BECAUSE OF ITS BREAKOVER CHARACTERISTIC (V_{on})



CB 429
(Plastic)

ABSOLUTE RATINGS (limiting values) (T_{amb} = 25 °C - L = 10 mm)

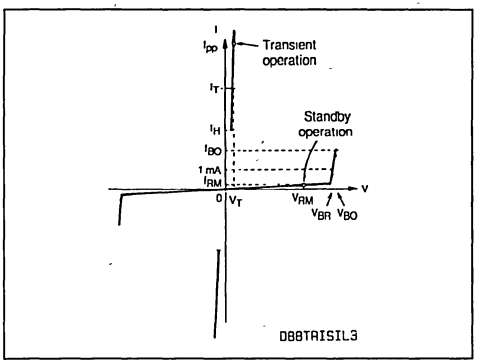
Symbol	Parameter		Value	Unit
P	Power Dissipation on Infinite Heatsink	T_{amb} = 50 °C	5	W
I_{pp}	Peak Pulse Current	1 ms expo	100	A
		8-20 µs expo*	150	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms	50	A
di/dt	Critical Rate of Rise of on-state Current	Non Repetitive	100	A/µs
dv/dt	Critical Rate of Rise of off-state Voltage	67 % $V_{(BR)}$ min	5	kV/µs
T_{stg} T_j	Storage and Operating Junction Temperature Range		– 40 to 150 150	°C °C
T_L	Maximum Lead Temperature for Soldering During 10 s at 4 mm from Case		230	°C

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-l)}$ $R_{th(j-a)}$	Junction-leads on Infinite Heatsink Junction-ambient on Printed Circuit	L = 10 mm	20 75	°C/W °C/W

ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage : 1.6 V typ. @ I_T = 1 A (t_p = 300 µs)



Types	I_{RM} @ V_{RM} max.		$V_{(BR)}$ @ I_R min.		V_{BO} max.	I_{BO} max.	I_H min.
	(µA)	(V)	(V)	(mA)	(V)	(mA)	(mA)
TPB62A - 12 or 18	2	56	62	1	82	800	
(1) TPB62B - 12 or 18	2	56	62	1	75	800	
TPB68A - 12 or 18	2	61	68	1	90	800	
(1) TPB68B - 12 or 18	2	61	68	1	82	800	
(1) TPB75A - 12 or 18	2	67	75	1	100	800	
(1) TPB75B - 12 or 18	2	67	75	1	91	800	
(1) TPB82A - 12 or 18	2	74	82	1	109	300	
(1) TPB82B - 12 or 18	2	74	82	1	99	300	
(1) TPB91A - 12 or 18	2	82	91	1	121	300	
(1) TPB91B - 12 or 18	2	82	91	1	110	300	
P TPB100A - 12 or 18	2	90	100	1	133	300	12 Suffix for 120 mA
TPB100B - 12 or 18	2	90	100	1	121	300	
TPB110A - 12 or 18	2	99	110	1	147	300	
TPB110B - 12 or 18	2	99	110	1	133	300	
P TPB120A - 12 or 18	2	108	120	1	160	300	
TPB120B - 12 or 18	2	108	120	1	145	300	
P TPB130A - 12 or 18	2	117	130	1	173	300	
TPB130B - 12 or 18	2	117	130	1	157	300	
(1) TPB150A - 12 or 18	2	135	150	1	200	300	
(1) TPB150B - 12 or 18	2	135	150	1	181	300	18 Suffix for 180 mA
(1) TPB160A - 12 or 18	2	144	160	1	213	300	
(1) TPB160B - 12 or 18	2	144	160	1	193	300	
(1) TPB180A - 12 or 18	2	162	180	1	240	300	
(1) TPB180B - 12 or 18	2	162	180	1	217	300	
(1) TPB200A - 12 or 18	2	180	200	1	267	300	
(1) TPB200B - 12 or 18	2	180	200	1	241	300	
P TPB220A - 12 or 18	2	198	220	1	293	300	
TPB220B - 12 or 18	2	198	220	1	265	300	
P TPB240A - 12 or 18	2	216	240	1	320	300	
TPB240B - 12 or 18	2	216	240	1	289	300	
P TPB270A - 12 or 18	2	243	270	1	360	300	
TPB270B - 12 or 18	2	243	270	1	325	300	

P : Preferred device.
(1) : These voltages are on request. Consult us.

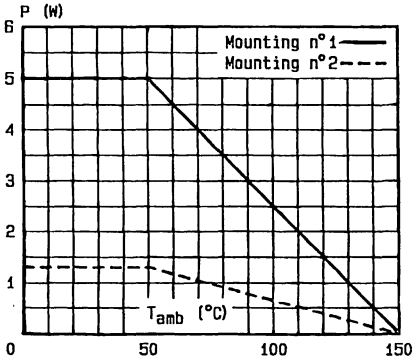


Fig.1 - Power dissipation versus ambient temperature.

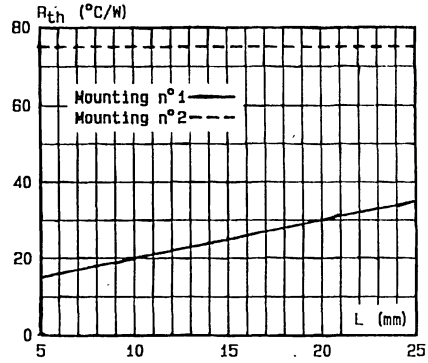


Fig.2 - Thermal resistance versus lead length.

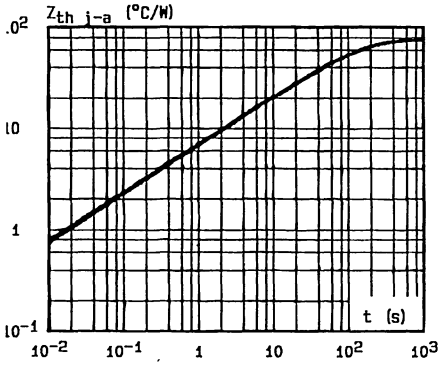
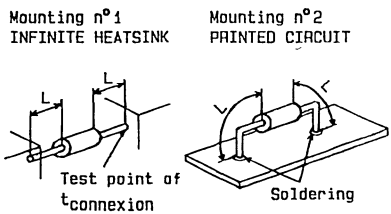


Fig.3 - Transient thermal impedance junction-ambient for mounting n°2 versus pulse duration (L = 10 mm).



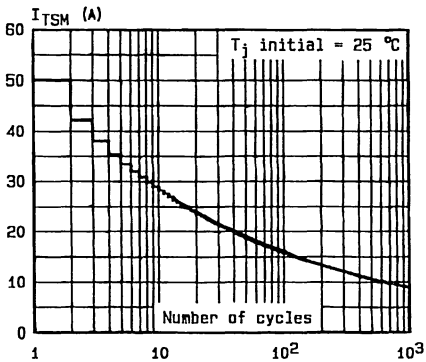


Fig.4 - Non repetitive surge peak on-state current versus number of cycles.

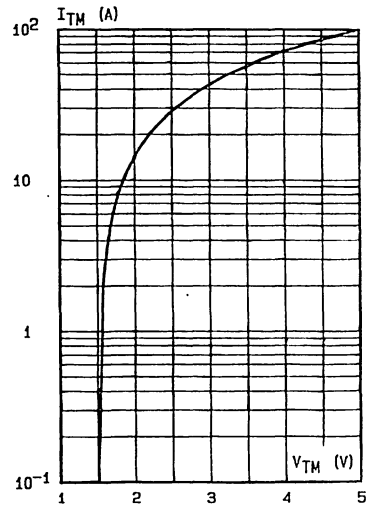


Fig.5 - Peak forward current versus peak forward voltage drop (typical values).

D88TPBP3

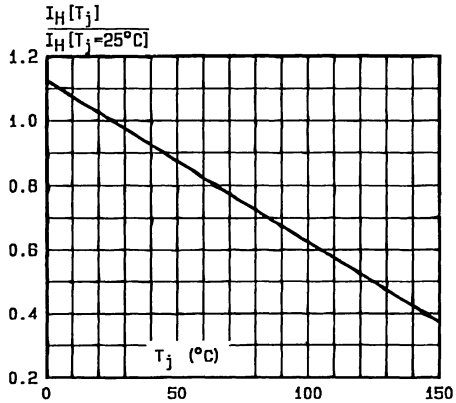


Fig.6 - Relative variation of holding current versus junction temperature

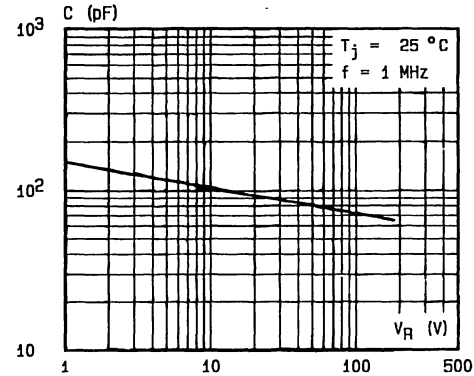
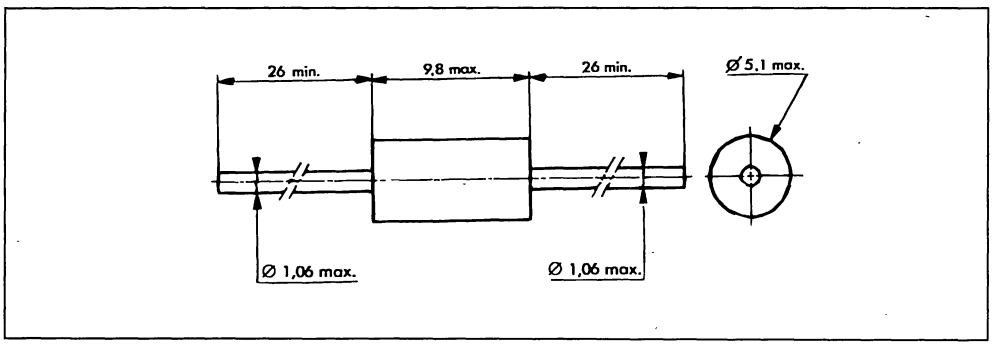


Fig.7 - Capacitance versus reverse applied voltage.

DBBTPBP4

PACKAGE MECHANICAL DATA

CB 429 Plastic



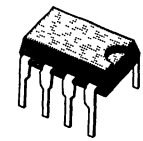
Cooling method : by conduction (method A)
Marking : type number
Weight : 0.9 g

SGS-THOMSON MICROELECTRONICS

LS5018B/LS5060B LS5120B/LS5120B1

BIDIRECTIONAL TRISIL

- CHARACTERISTIC OF STAND-OFF AND BREAKDOWN VOLTAGE SIMILAR TO A TRANSIL (V_{off})
- HIGH FLOWOUT CAPABILITY BECAUSE OF ITS BREAKOVER CHARACTERISTICS (V_{on})
- AUTOMATIC RECOVERY AFTER SURGE



Minidip
(Plastic)

DESCRIPTION

The LS5018B, LS5060B and LS5120B/B1 are bidirectional transient overvoltage suppressor designed to protect sensitive components in electronic telephones and telecommunication equipments against transient caused by lightning, induction from power lines, etc.

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C)

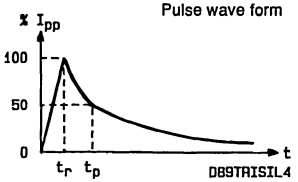
Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Current	1 ms expo	100	A
		8-20 µs expo*	500	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 20 ms – Sinus	50	A
di/dt	Critical Rate of Rise of on-state Current	Non repetitive	100	A/µs
T_{stg} T_j	Storage and Junction Temperature Range		– 40 to 150 150	°C °C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to Ambient	80	°C/W

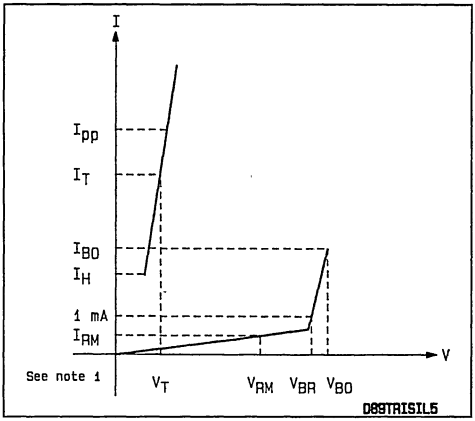
* ANSI STD C62.

Pulse wave form



ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage @ I_T
I_{BO}	Breakover Current
I_{pp}	Peak-pulse Current

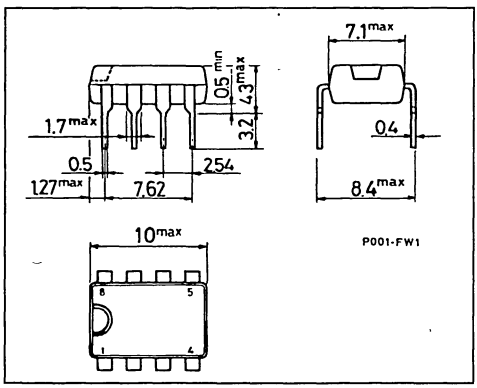


Type	I_{RM} @ V_{RM} max.		$V_{(BR)}$ @ I_R min.		V_{BO} @ max.	I_{BO} min.	I_{BO} typ.	I_{BO} max. See note 2	I_H min.	V_T typ. I_T = 1 A	C max. V_R = 5 V F = 1 MHz
	(µA)	(V)	(V)	(mA)	(V)	(mA)	(mA)	(mA)	(mA)	(V)	(pF)
LS5018B	5	16	17	1	22		1300		200	2	150
LS5060B	10	50	60	1	85		1000		200	2	150
LS5120B	20	100	120	1	180	500		1250	250	2	150
LS5120B1	20	100	120	1	180	500		1250	200	2	150

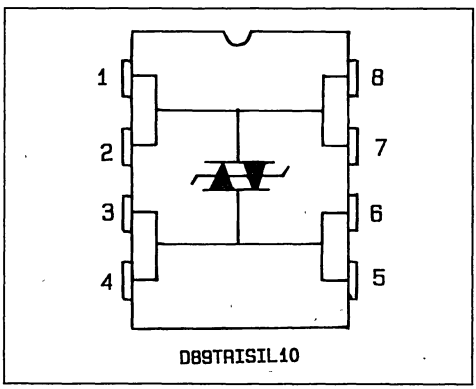
Notes : 1. Same characteristic both sides.
2. These devices are not designed to function as zeners ; continuous operation between 1 mA and I_{BO} will damage them.

PACKAGE MECHANICAL DATA

MINIDIP Plastic



CONNECTION DIAGRAM



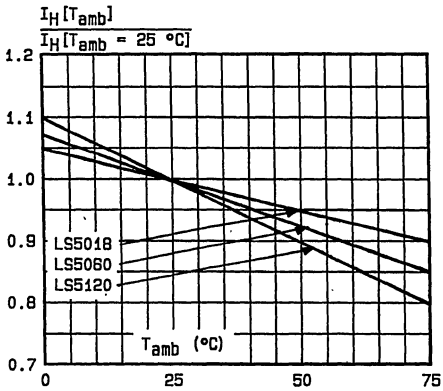


Fig.1 - Relative variation of holding current versus ambient temperature.

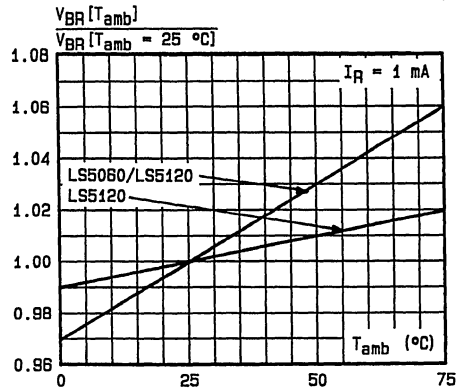


Fig.2 - Relative variation of breakdown voltage versus ambient temperature.

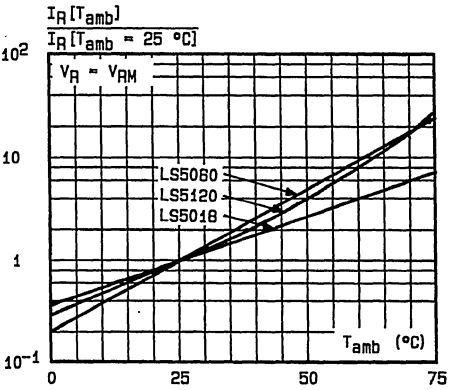


Fig.3 - Relative variation of leakage current versus ambient temperature.

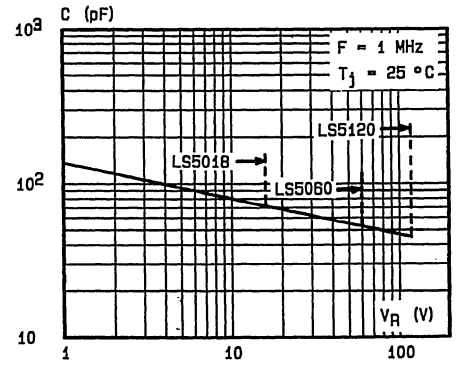


Fig.4 - Junction capacitance versus reverse applied voltage.

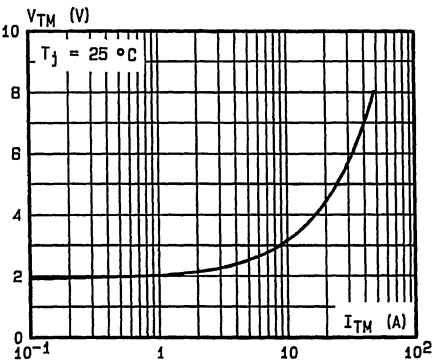


Fig.5 - On-state voltage versus on-state current (typical values).

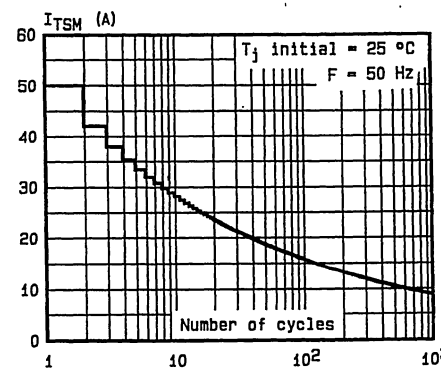


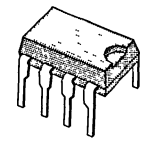
Fig.6 - Non repetitive surge peak on-state current versus number of cycles.

SGS-THOMSON MICROELECTRONICS

L3100B
L3100B1

TRISIL
UNIDIRECTIONAL PROGRAMMABLE VOLTAGE AND CURRENT SUPPRESSOR

- HIGH CURRENT CAPABILITY
- PROGRAMMABILITY BOTH IN VOLTAGE AND CURRENT
- AUTOMATIC RECOVERY



Minidip
(Plastic)

DESCRIPTION

The L3100B/B1 is a transient overvoltage suppressor/overcurrent arrester designed to protect sensitive components in electronic telephones and telecommunication equipments against transients caused by lightning, induction from power lines, etc.

The L3100B/B1 characteristic, that is its firing voltage and current, can be easily programmed by means of inexpensive external components ; more over, since this device recoveres automatically when the surge current falls below a fixed holding current, it may be used on remotely supplied lines. Finally, if destroyed, it becomes a permanent short circuit.

ABSOLUTE RATINGS (limiting values) (T_j = 25 °C)

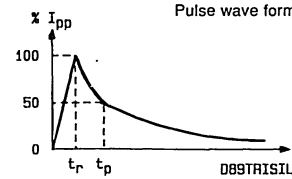
Symbol	Parameter		Value	Unit
I_{pp}	Peak Pulse Current	1 ms expo	150	A
		8-20 µs expo*	250	
I_{TSM}	Non Repetitive Surge Peak on-state Current	t_p = 10 ms – Sinus	50	A
di/dt	Critical Rate of Rise of on-state Current	Non repetitive	100	A/µs
T_{stg}	Storage and Junction Temperature Range		– 40 to 150	°C
T_j			150	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to Ambient	80	°C/W

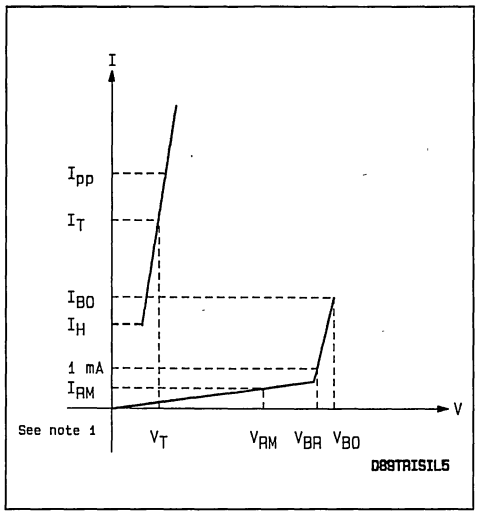
* ANSI STD C62.

Pulse wave form



ELECTRICAL CHARACTERISTICS
(T_j = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Clamping Voltage
I_H	Holding Current
V_T	On-state Voltage @ I_T
I_{BO}	Breakover Current
I_{pp}	Peak-pulse Current
V_{GN}	Gate Voltage
I_{GN}	Firing Gate N Current
V_{RGN}	Reverse Gate N Voltage
I_{GP}	Firing Gate P Current



OPERATION WITHOUT GATE

Type	I_{RM} @ V_{RM} max.		V_{BR} @ I_R min.		max.	V_{BO} @ I_{BO} max.	min.	max. See note 2	I_H min.	V_T typ. I_T = 1 A	C max. V_R = 5 V F = 1 MHz
	(µA)	(V)	(V)	(V)	(mA)	(V)	(mA)	(mA)	(mA)	(V)	(pF)
L3100B/B1	6 40	60 250	255 (3) 265 (4)		1	350	200	500	210 (3) 280 (4)	2	100

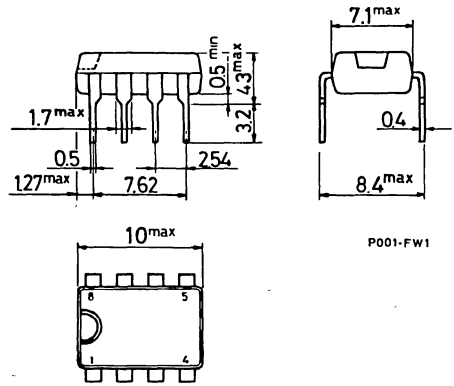
OPERATION WITH GATES

Type	V_{GN} (V) I_G = 200 mA		I_{GN} (mA) $V_A - C$ = 100 V		V_{RGN} (V) I_G = − 1 mA		I_{GP} (mA) $V_A - C$ = 100 V	
	min.	max.	min.	max.	min.	max.	min.	max.
L3100B/B1	0.6	1.8	30	200	0.7			150

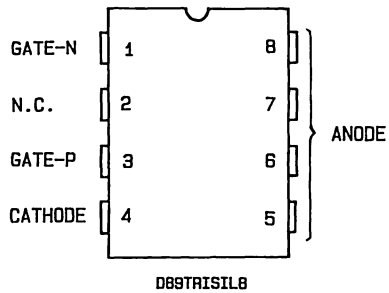
Notes : 1. Reverse characteristic : I_R < 1 mA @ V_R = 0.7V.
2. These devices are not designed to function as zeners ; continuous operation between 1 mA and I_{BO} will damage them.
3. L3100B1
4. L3100B

PACKAGE MECHANICAL DATA

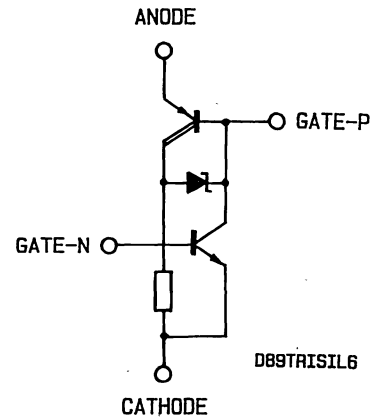
MINIDIP Plastic



CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



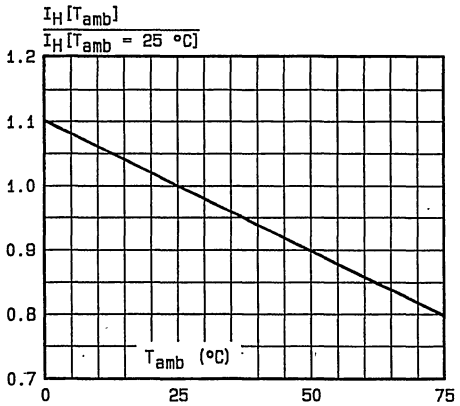


Fig.1 - Relative variation of holding current versus ambient temperature.

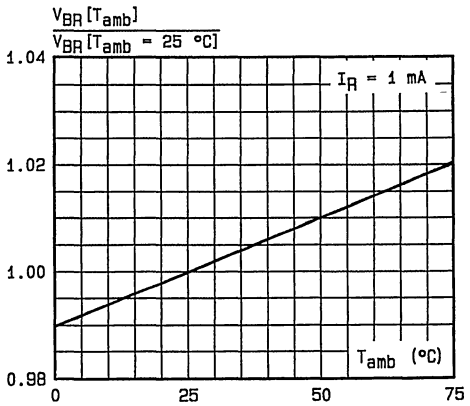


Fig.2 - Relative variation of breakdown voltage versus ambient temperature.

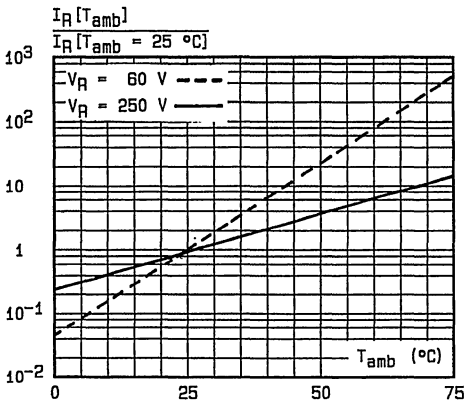


Fig.3 - Relative variation of leakage current versus ambient temperature.

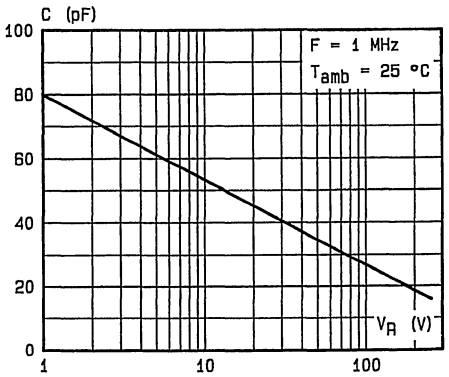
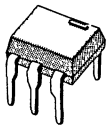


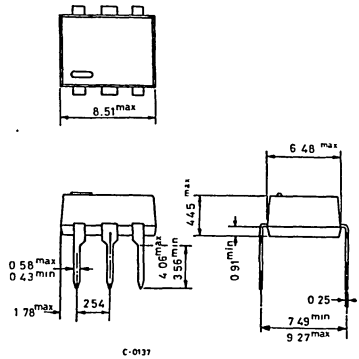
Fig.4 - Junction capacitance versus reverse applied voltage.

D89L3100B1P4

PACKAGES

DIP-6 H





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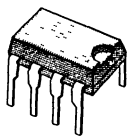
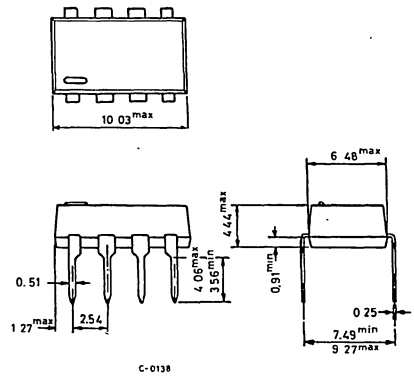
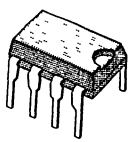
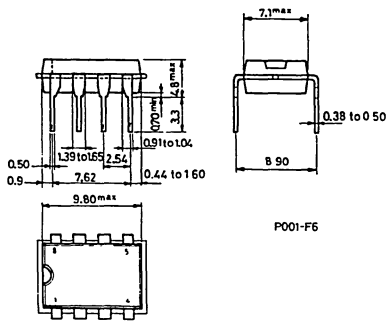


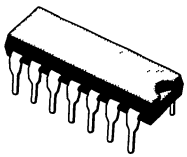


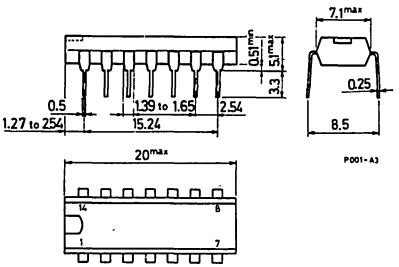
8 LEAD PLASTIC MINIDIP



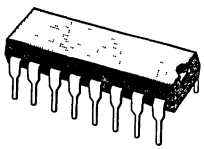


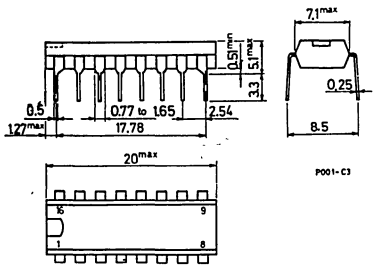
14 LEAD PLASTIC DIP





16 LEAD PLASTIC DIP





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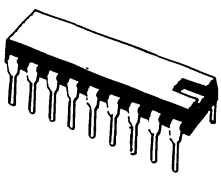
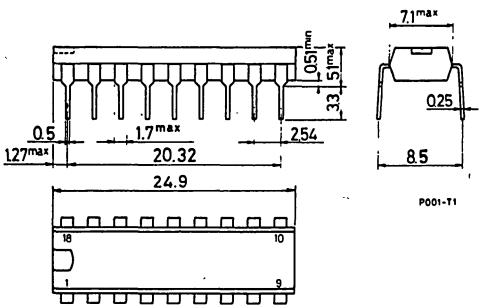
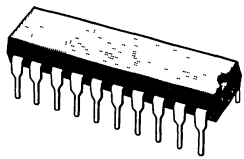
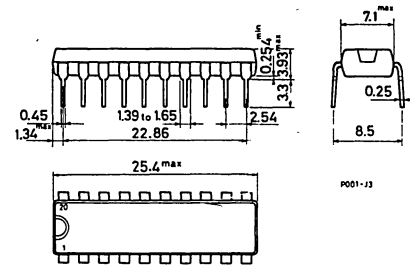


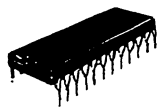


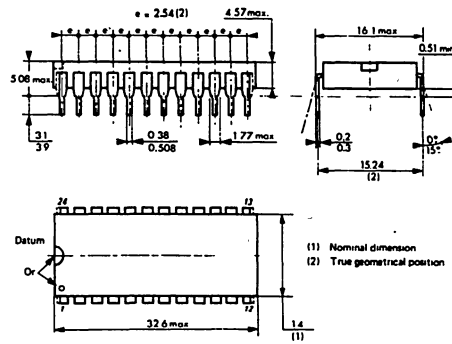
20 LEAD PLASTIC DIP





DIP-24 PLASTIC





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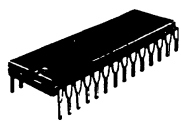
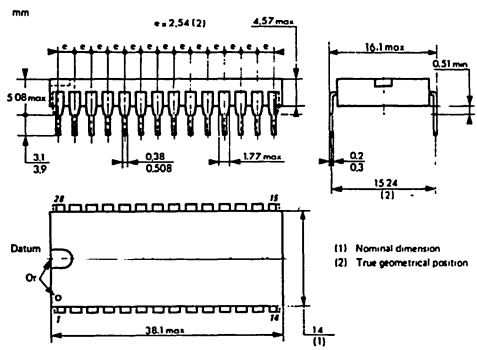
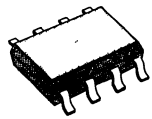
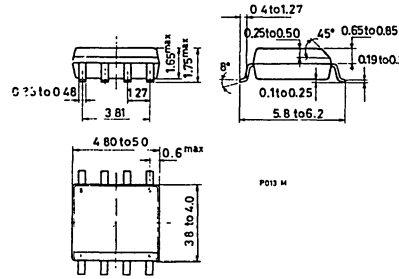


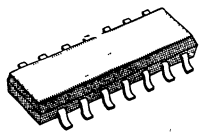


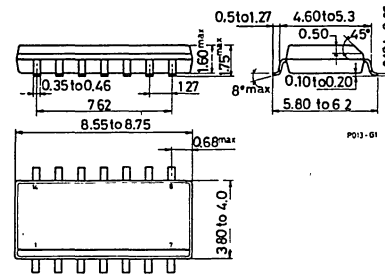
SO-8J





SO-14J





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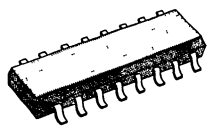

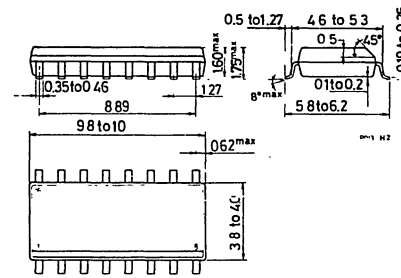

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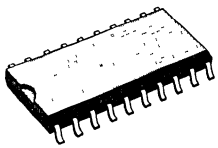

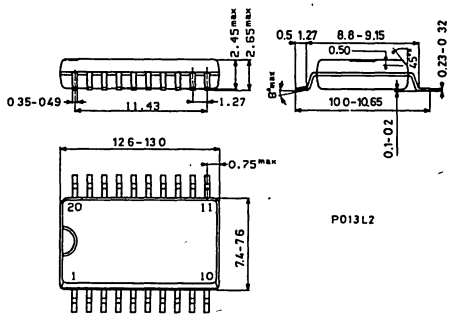

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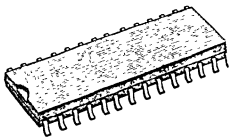
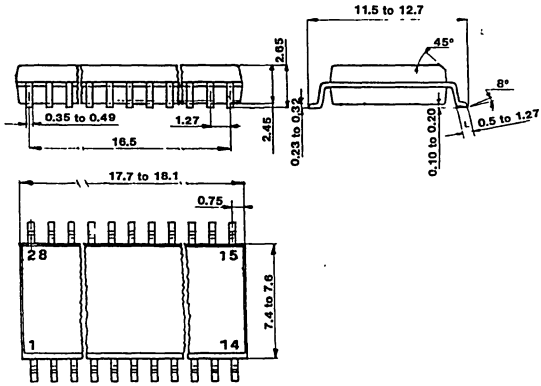
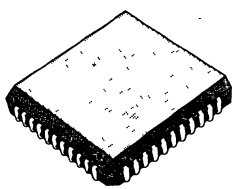
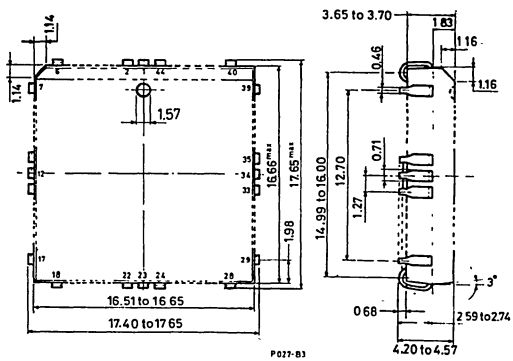




PLCC - 44 PLASTIC CHIP CARRIER





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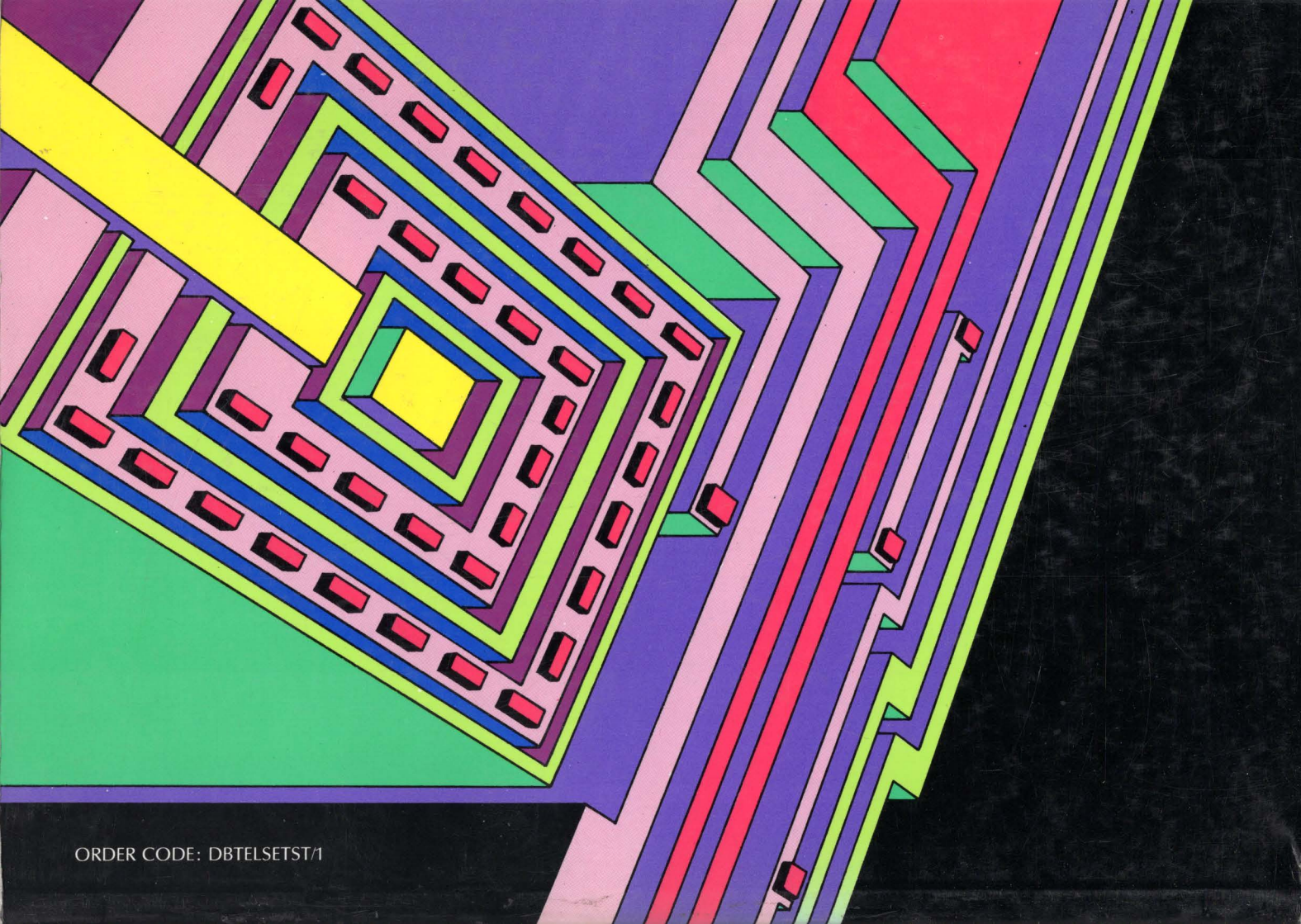

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