Functions
Fully CAV compatible CD-DSP function, CD-ROM function, built-in ATAPI (IDE) I/F, built-in DVD-RAM IF

Features
CD-ROM decoder, ATAPI (IDE) I/F block
• 24x speed fully CAV compatible
• Built-in ATAPI (IDE) I/F
• 16-bit DRAM (FPM, EDO) connectable (8-bit DRAM connectable)
• Up to 32 Mbits of buffer RAM connectable (when using DVD I/F) (CD-ROM connectable up to 4 Mbits)
• CD main channel and C2 flag areas in buffer RAM can be freely set by user
• Built-in batch transfer function (function for sending CD main channel, C2 flag, etc. at one time)
• Built-in multi block transfer function (function for sending several blocks at one time)
• Built-in DVD-ECC I/F
• Built-in intelligent functions
• Inter-memory transfer function
• Fixed data embedding function

CD-DSP Block
• Slices the interface input signal at precision levels, converts the result to the EFM signal, and compares the phase with the built-in Vage-controlled oscillator.
• Generates the standard clock and other internal timing signals necessary from an external 16.9344-MHz crystal oscillator.
• Detects, protects, and inserts frame synchronization signals to ensure stable data readout
• Demodulates the EFM signal to derive 8-bit symbol data
• Checks the CRC of the subcode Q signal and communicates with the microcontroller using parallel I/O
• Descrambles and de-interleaves by rearranging the demodulated EFM signal in the specified order
• Detects and corrects error signals and processes flags (C1: dual error correction, C2: quadruple error correction)
• Derives the C2 flag from the C1 flag and C2 check and uses it to interpolate the signal for muting. The interpolation circuit uses binary interpolation so that the C2 flag converges to the muting level at least two points.
• Uses 8-bit parallel input to receive commands from the microcontroller for jumping tracks, starting/stopping the disc motor, enabling/disabling muting, determining the track count, etc
• Supports arbitrary track count
• Built-in CAV-AUDIO support
• Uses zero cross muting
• Built-in eightfold oversampling and digital filter
• Built-in digital-to-analog converter (PWM output)
• Separate built-in digital attenuators (with 8-bit precision) for left and right channels
• Built-in digital de-emphasis
• Bilingual support

Package Dimensions
unit: mm
3220-SQFP176
## Specifications

### Absolute Maximum Ratings at $V_{SS} = 0 \, V$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum supply voltage</td>
<td>$V_{DD\ max}$</td>
<td>$T_a = 25^\circ C$</td>
<td>$-0.3$</td>
<td>$7.0$</td>
</tr>
<tr>
<td>Input/output voltage</td>
<td>$V_{I/O}$</td>
<td>$T_a = 25^\circ C$</td>
<td>$-0.3$</td>
<td>$V_{DD} +0.3$</td>
</tr>
<tr>
<td>Allowable power dissipation</td>
<td>$P_{d \ max}$</td>
<td>$T_a \leq 70^\circ C$</td>
<td>$500^\circ 2$</td>
<td>mW</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>$T_{opr}$</td>
<td></td>
<td>$-30$</td>
<td>$70$</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td></td>
<td>$-55$</td>
<td>$+125$</td>
</tr>
<tr>
<td>Soldering temperature (pin part only)</td>
<td>$T_{10s}$</td>
<td>$10s$</td>
<td>$235$</td>
<td>°C</td>
</tr>
<tr>
<td>Input/output current</td>
<td>$I_{I/O}$</td>
<td>$10s$</td>
<td>$20 \times 10^{-6}$</td>
<td>mA</td>
</tr>
</tbody>
</table>

Note: *1 Per 1 input/output reference cell
*2 Implement heat dissipation measures, for example by inserting a radiating sheet.
For details, contact a SANYO sales representative.

### Allowable Operating Ranges at $T_a = -30$ to $+70^\circ C$, $V_{SS} = 0 \, V$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$V_{DD}$</td>
<td></td>
<td>$4.75$</td>
<td>$5.0$</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>$V_{IN}$</td>
<td></td>
<td>$0$</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>[Internal Cell Power Supply]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage</td>
<td>$V_{DD}$</td>
<td></td>
<td>$3.9$</td>
<td>$4.1$</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>$V_{IN}$</td>
<td></td>
<td>$0$</td>
<td>$V_{DD}$</td>
</tr>
</tbody>
</table>
### DC Characteristics at Ta = -30 to +70°C, VSS = 0 V, VDD = 4.75 to 5.25 V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
<th>Applicable pins*</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-level input voltage</td>
<td>V1H</td>
<td>TTL levels</td>
<td>2.2</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>10, 13</td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>V1L</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>—</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>V1H</td>
<td>TTL levels</td>
<td>2.2</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>15</td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>V1L</td>
<td>with pull-up resistor</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>V1H</td>
<td>TTL levels</td>
<td>2.2</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>2, 3</td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>V1L</td>
<td>with pull-down resistor</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>V1H</td>
<td>CMOS levels</td>
<td>0.7 VDD</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>14</td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>V1L</td>
<td>—</td>
<td>—</td>
<td>0.3 VDD</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>V1H</td>
<td>CMOS levels</td>
<td>0.8 VDD</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>V1L</td>
<td>Schmitt</td>
<td>—</td>
<td>—</td>
<td>0.2 VDD</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>VOH</td>
<td>IQH = -2 mA</td>
<td>VOH - 2.1</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>5, 1, 9</td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>VOL</td>
<td>IQL = 2 mA</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>10, 15</td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>VOH</td>
<td>IQH = -4 mA</td>
<td>VOH - 2.1</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>3, 6</td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>VOL</td>
<td>IQL = 24 mA</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>7, 11</td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>VOH</td>
<td>IQH = 2 mA</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>12</td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>VOL</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Input leak current</td>
<td>IL</td>
<td>V1 = VSS, VDD</td>
<td>-10</td>
<td>—</td>
<td>+10</td>
<td>μA</td>
<td>2, 3, 4, 10, 15</td>
</tr>
<tr>
<td>Output leak current</td>
<td>IOZ</td>
<td>During high-impedance output</td>
<td>-10</td>
<td>—</td>
<td>+10</td>
<td>μA</td>
<td>3, 6, 7, 10, 12, 15</td>
</tr>
<tr>
<td>Pull-up resistance</td>
<td>RUP</td>
<td>40</td>
<td>80</td>
<td>160</td>
<td>kΩ</td>
<td>1, 11</td>
<td></td>
</tr>
<tr>
<td>Pull-down resistance</td>
<td>RDN</td>
<td>40</td>
<td>80</td>
<td>160</td>
<td>kΩ</td>
<td>10, 15</td>
<td></td>
</tr>
</tbody>
</table>

Note: *Applicable pin sets are as follows.

**INPUT**
- 2: ZRESET, ZDMACK, ZHRST, DA0 to DA2, ZCS1FX, ZCSSFX, ZDIO, ZDIOW, FG
- 4: ZCSCTRL, ZCS, ZRD, ZWR, HFL, TES
- 14: DEFI
- 13: SUAO to SUA6

**OUTPUT**
- 6: DMARQ, HINTRO
- 5: RA0 to RA8, ZIASO, ZCASO, ZOE, ZUE, ZLWE, C2F, ROMXA, FSX, EFLG, PCK, FSEQ, TOFF, TGL, 4.2M, WRQ, RWC, C2S, ROMX, RCHN, LCHP, LCHN
- 7: ZRSTCPU, ZRSTIC
- 9: JP+, JP-, SPO
- 11: ZINTO, ZINT1, ZSWAIT
- 12: IORDY, ZOCS16

**INPUT/OUTPUT**
- 1: DO to D7, IO0 to IO15
- 3: D00 to D15, ZDASP, ZPDIAG
- 10: IO0 to IOP7
- 15: DRESP, DREQ

Note: Pins XTAL, XTALCK, RO, VCNT0, PDO0, R1, VCNT1, P011, P021, BSN1, R2, VCNT2, P012, P022, and BSN2 are not included in DC characteristics. For 1-bit DAC, measurement was made using only a logic tester, and analog measurement was not performed.
Block Diagram

- DVD-ECC
- ASP
- Audio Circuit
- HOST
- Micro controller
- PLL Clock generator
- HOST
- Micro controller
- Each Block, Bus arbiter & RAM controller
- Each Block Bus control signal
- External Buffer
- RAM
- Buffer
- IDE I/F
- Each Block Register R0 to R94
- Data output input I/F
- Address generator
- IDE I/F based HISIDE **1
- ECC & EDC
- Address generator
- Sub-code SYNC Detector
- Address generator
- Sync Detector
- CD-DSP I/F & SYNC Detector
- Reset Controller
- ZRESET ZRTC
- ZRCPU
- ZINT1 ZINT0
- WRQ
- Each Block Register R0 to R94
- Decoder
- Microcontroller RAM access
- Address generator
- Microcontroller RAM access
- Address generator
- Data bus [0:7]
- Data bus [0:15] Address bus [0:16]
- Data bus [0:7]
- Each Block

*1 DEF, EFMI, HFL, TES
*2 4.2MHz, EFMO, PCK, FSEQ, TOFF, TGL, JP+, JP-, RWC, COIN, ZCLOCK
*3 RCCHP, RCCHN, LCHP, LCHN
*4 DD0 to DD15, ZDASP, ZDIAG
*5 ZCS1FX, ZCS3FX, DA0 to DA2, ZDIO, ZDIO, ZDMACK, ZHRST
*6 DMARQ, HINTIQ, ZIOCS16, IORDY
*7 ZPD, ZWR, ZCS, ZCSCTRL, SUA0 to 6
*8 D0 to D7
*9 I/O0 to I/O15
*10 RAID to RA9 (RA9), ZRAS0 (ZRAS1), ZCAS0, ZOE, ZUWE, ZLWE
*11 IOP0 to IOP7 (HD80 to HD87), DREQ, DRESP
*12 (HD8DIR)
*13 RO, VCH0, PDO0
**1 HISIDE (WD25C32) is made by WESTERN DIGITAL.