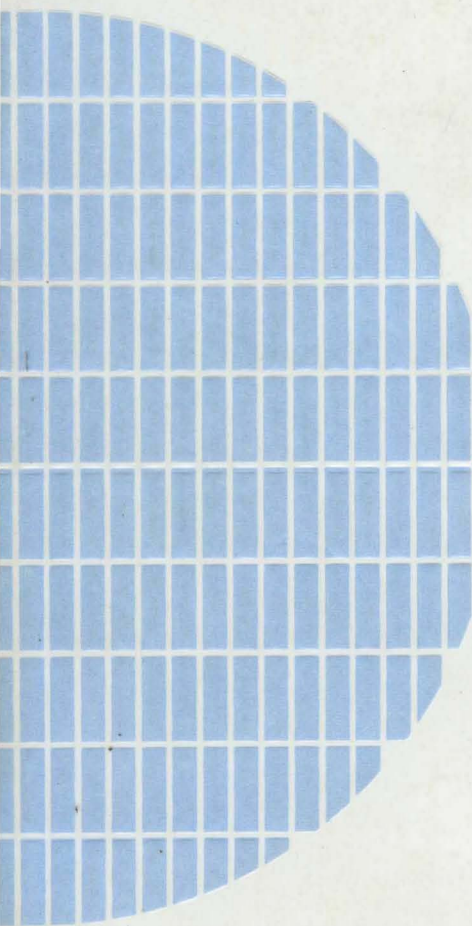


# SAMSUNG

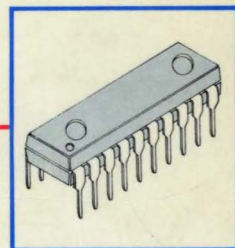
Data Book



## AHCT/HCTLS

(High Speed CMOS Logic IC)

1990



## INTRODUCTION

Samsung Semiconductor is a broad-line manufacturer of semiconductors that range from VLSI circuits such as memories (DRAM, SRAM, EPROM and EEPROM), microprocessors, gate arrays and programmable logic to transistors, linear circuits and telecommunications products.

The KS54/74AHCT and the KS54/74HCTLS high-performance CMOS logic families are Samsung's entry into the general purpose digital logic area.

The KS54/74AHCT advanced high-speed CMOS family is designed to provide performance equivalent to or better than that of the bipolar 54/74ALS (Advanced Low-power Schottky) family with the additional CMOS advantages of low power dissipation and high noise immunity. The AHCT parts can therefore be used as direct plug-in replacements for their ALS counterparts (and in most applications for FAST and Schottky) and improve the system performance.

The 54/74HCTLS high-speed CMOS family offers similar benefits as a replacement for industry-standard 54/74LS (Low-power Schottky), 54/74HCT and 54/74HC. While meeting all of the HCT electrical specifications, it also provides improved speed and drive capability, so that LS parts can be replaced with no performance degradation.

**PRINTED IN KOREA**

Circuit diagrams utilizing SAMSUNG products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of SAMSUNG or others. SAMSUNG reserve the right to change device specifications.

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# **High Performance CMOS Logic Data Book**

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**KS54/74AHCT**  
**Advanced High-Speed CMOS**

**KS54/74HCTLS**  
**High-Speed CMOS**

# **SAMSUNG DATA BOOK LIST**

- I. Semiconductor Product Guide
- II. Transistor Data Book
  - Vol. 1: Small Signal TR
  - Vol. 2: Bipolar Power TR
  - Vol. 3: TR Pellet
- III. Linear IC Data Book
  - Vol. 1: Audio/Video
  - Vol. 2: Telecom/Industrial/TOY
  - Vol. 3: Data Converter IC
- IV. CMOS Consumer IC Data Book
- V. High Speed CMOS Logic Data Book
- VI. MOS Memory Data Book
- VII. SFET Data Book
- VIII. MPR Data Book
- IX. CPL Data Book
- X. Dot Matrix Data Book

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## 1. Alphanumeric Index

### 1) KS54/74AHCT Family

Device	Function
KS54/74AHCT00	Quad 2-Input NAND Gates
KS54/74AHCT01	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT02	Quad 2-Input NOR Gates
KS54/74AHCT03	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT04	Hex Inverters
KS54/74AHCT05	Hex Inverters with Open-Drain Outputs
KS54/74AHCT08	Quad 2-Input AND Gates
KS54/74AHCT09	Quad 2-Input AND Gates with Open-Drain Outputs
KS54/74AHCT10	Triple 3-Input NAND Gates
KS54/74AHCT11	Triple 3-Input AND Gates
KS54/74AHCT12	Triple 3-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT14	Hex Schmitt-Trigger Inverters
KS54/74AHCT20	Dual 4-Input NAND Gates
KS54/74AHCT21	Dual 4-Input AND Gates
KS54/74AHCT22	Dual 4-Input NAND Gates with Open-Drain Outputs
KS54/74AHCT27	Triple 3-Input NOR Gates
KS54/74AHCT30	8-Input NAND Gate
KS54/74AHCT32	Quad 2-Input OR Gates
KS54/74AHCT42	BCD-to-Decimal Decoder
KS54/74AHCT51	Dual AND-OR-Invert Gates
KS54/74AHCT58	Dual AND-OR Gates
KS54/74AHCT73	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear
KS54/74AHCT74	Dual D-Type Positive-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74AHCT75	Quad Bistable Transparent Latches
KS54/74AHCT76	Dual J-K Negative-Edge-Triggered Filp Flops with Preset and Clear
KS54/74AHCT77	Quad D-Type Latches
KS54/74AHCT78	Dual J-K Negative-Edge-Triggered Filp-Flops with Preset, Common Clear and Common Clock
KS54/74AHCT86	Quad 2-Input Exclusive-OR Gates
KS54/74AHCT90	Decade Counters
KS54/74AHCT92	Divide-by-Twelve Counter
KS54/74AHCT93	4 Bit Binary Counter Divide by Two and Divide by Eight
KS54/74AHCT107	Dual J-K Negative-Edge-Triggered Filp-Flops with Clear
KS54/74AHCT109	Dual J-K Positive-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74AHCT112	Dual J-K Negative-Edge-Triggered Filp-Flops with Preset and Clear
KS54/74AHCT123	Dual Retriggerable Monostable Multivibrators
KS54/74AHCT125	Quad Buffers with 3-State Outputs
KS54/74AHCT126	Quad Buffers with 3-State Outputs
KS54/74AHCT132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs
KS54/74AHCT133	13-Input NAND Gate
KS54/74AHCT138	3-Line to 8-Line Decoders/Demultiplexers
KS54/74AHCT139	Dual 1 of 4 Decoders/Demultiplexers
KS54/74AHCT148	8-Line to 3-Line Priority Encoders
KS54/74AHCT151	1 of 8 Data Selectors/Multiplexers
KS54/74AHCT153	Dual 1 of 4 Data Selectors/Multiplexers
KS54/74AHCT154	4-Line to 16-Line Decoders/Demultiplexers
KS54/74AHCT155	Dual 2 to 4 Line Decoders/Demultiplexers
KS54/74AHCT157	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74AHCT158	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74AHCT160	Synchronous 4-Bit Decade Counters
KS54/74AHCT161	Synchronous 4-Bit Binary Counters
KS54/74AHCT162	Synchronous 4-Bit Decade Counters
KS54/74AHCT163	Synchronous 4-Bit Binary Counters
KS54/74AHCT164	8-Bit Serial-In/Parallel-Out Shift Registers
KS54/74AHCT165	8-Bit Parallel-In/Serial-Out Shift Registers
KS54/74AHCT166	8-Bit Parallel-In/Serial-Out Shift Registers with Clear

## KS54/74AHCT Family (continued)

Device	Function
KS54/74AHCT168	Synchronous 4-Bit Up/Down Decade Counters
KS54/74AHCT169	Synchronous 4-Bit Up/Down Binary Counters
KS54/74AHCT173	4-Bit D-Type Registers with 3-State Outputs
KS54/74AHCT174	Hex D-Type Flip-Flops with Clear
KS54/74AHCT175	Quad D-Type Flip-Flops with Clear
KS54/74AHCT181	4-Bit Arithmetic Logic Unit
KS54/74AHCT182	Look-Ahead Carry Generator
KS54/74AHCT183	Dual High Speed Adder
KS54/74AHCT190	Presetable Synchronous BCD Decade Up/Down Counter
KS54/74AHCT191	Synchronous 4-Bit Up/Down Binary Counters
KS54/74AHCT192	Presetable Synchronous BCD Decade Up/Down Counter
KS54/74AHCT193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock
KS54/74AHCT194	4-Bit Bidirectional Universal Shift Registers
KS54/74AHCT195	4-Bit Bidirectional Universal Shift Registers
KS54/74AHCT210	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT238	3-Line to 8-Line Decoders/Demultiplexers
KS54/74AHCT239	Dual 1-of-4 Decoders/Demultiplexers
KS54/74AHCT240	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT241	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT242	Quad Bus Transceivers with 3-State Outputs
KS54/74AHCT243	Quad Bus Transceivers with 3-State Outputs
KS54/74AHCT244	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT245	Octal Bus Transceivers with 3-State Outputs
KS54/74AHCT251	1 of 8 Data Selectors/Multiplexers with 3-State Outputs
KS54/74AHCT253	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs
KS54/74AHCT257	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs
KS54/74AHCT258	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs
KS54/74AHCT259	8-Bit Addressable Latches
KS54/74AHCT266	Quad Exclusive-NOR Gates with Open-Drain Outputs
KS54/74AHCT273	Octal D-Type Flip-Flops
KS54/74AHCT280	9-Bit Parity Generators/Checkers with Clear
KS54/74AHCT299	8-Bit Universal Shift/Storage Registers with 3-State Outputs
KS54/74AHCT322	8-Bit Shift Registers with Sign Extend
KS54/74AHCT352	Dual 4-Line to 1-Line Data Selectors/Multiplexers
KS54/74AHCT353	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs
KS54/74AHCT365	Hex Bus-Drivers with 3-State Outputs
KS54/74AHCT366	Hex Bus-Drivers with 3-State Outputs
KS54/74AHCT367	Hex Bus-Drivers with 3-State Outputs
KS54/74AHCT368	Hex Bus-Drivers with 3-State Outputs
KS54/74AHCT373	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74AHCT374	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74AHCT377	Octal D-Type Flip-Flops with Clock Enable
KS54/74AHCT390	Dual 4-Bit Decade Counters
KS54/74AHCT393	Dual 4-Bit Binary Counters
KS54/74AHCT399	Quad 2-Port Registers
KS54/74AHCT423	Dual Retriggerable Monostable Multivibrators
KS54/74AHCT465	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT466	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT467	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT468	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT518	8-Bit Identity Comparators
KS54/74AHCT519	8-Bit Identity Comparators
KS54/74AHCT520	8-Bit Identity Comparators
KS54/74AHCT521	8-Bit Identity Comparators
KS54/74AHCT522	8-Bit Identity Comparators
KS54/74AHCT533	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74AHCT534	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74AHCT540	Octal Buffers and Line Drivers with 3-State Outputs

## KS54/74AHCT Family (continued)

Device	Function
KS54/74AHCT541	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74AHCT563	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74AHCT564	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74AHCT573	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74AHCT574	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74AHCT590	8-Bit Binary Counters with 3-State Output Register
KS54/74AHCT591	8-Bit Binary Counters with 3-State Output Register
KS54/74AHCT592	8-Bit Binary Counters with Input Register
KS54/74AHCT593	8-Bit Binary Counters with Bidirectional Input Register Counter Output
KS54/74AHCT595	8-Bit Shift Registers with Output Latches
KS54/74AHCT596	8-Bit Shift Registers with Output Latches
KS54/74AHCT597	8-Bit Shift Registers with Input Latches
KS54/74AHCT640	Octal Bus Transceivers with 3-State Outputs
KS54/74AHCT643	Octal Bus Transceivers with 3-State Outputs
KS54/74AHCT645	Octal Bus Transceivers with 3-State Outputs
KS54/74AHCT646	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT648	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT651	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT652	Octal 3-State Bus Transceivers with Registers
KS54/74AHCT658	Octal Bus Transceivers with Parity
KS54/74AHCT659	Octal Bus Transceivers with Parity
KS54/74AHCT664	Octal Bus Transceivers with Parity
KS54/74AHCT665	Octal Bus Transceivers with Parity
KS54/74AHCT670	4-By-4 Register Files with 3-State Outputs
KS54/74AHCT679	12-Bit Address Comparators
KS54/74AHCT680	12-Bit Address Comparators
KS54/74AHCT682	8-Bit Magnitude Comparators
KS54/74AHCT684	8-Bit Magnitude Comparators
KS54/74AHCT686	8-Bit Magnitude Comparators
KS54/74AHCT688	8-Bit Identity Comparators
KS54/74AHCT689	8-Bit Identity Comparators with Open-Drain Outputs
KS54/74AHCT793	Octal Latches with Readback
KS54/74AHCT794	Octal Registers with Readback
KS54/74AHCT821	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT822	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT823	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT824	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT825	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT826	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74AHCT841	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT842	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT843	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT844	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT845	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT846	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74AHCT4049	Hex Inverting Logic Level Down Converters
KS54/74AHCT4050	Hex Logic Level Down Converters

## 2) KS54/74HCTLS Family (continued)

Device	Function
KS54/74HCTLS00	Quad 2-Input NAND Gates
KS54/74HCTLS01	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS02	Quad 2-Input NOR Gates
KS54/74HCTLS03	Quad 2-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS04	Hex Inverters
KS54/74HCTLS05	Hex Inverters with Open-Drain Outputs
KS54/74HCTLS08	Quad 2-Input AND Gates
KS54/74HCTLS09	Quad 2-Input AND Gates with Open-Drain Outputs
KS54/74HCTLS10	Triple 3-Input NAND Gates
KS54/74HCTLS11	Triple 3-Input AND Gates
KS54/74HCTLS12	Triple 3-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS14	Hex Schmitt-Trigger Inverters
KS54/74HCTLS20	Dual 4-Input NAND Gates
KS54/74HCTLS21	Dual 4-Input AND Gates
KS54/74HCTLS22	Dual 4-Input NAND Gates with Open-Drain Outputs
KS54/74HCTLS27	Triple 3-Input NOR Gates
KS54/74HCTLS30	8-Input NAND Gate
KS54/74HCTLS32	Quad 2-Input OR Gates
KS54/74HCTLS42	BCD-to-Decimal Decoder
KS54/74HCTLS51	Dual AND-OR-Invert Gates
KS54/74HCTLS58	Dual AND-OR Gates
KS54/74HCTLS73A	Dual J-K Negative-Edge-Triggered Flip-Flops with Clear
KS54/74HCTLS74A	Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear
KS54/74HCTLS75	Quad Bistable Transparent Latches
KS54/74HCTLS76A	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear
KS54/74HCTLS77	Quad D-Type Latches
KS54/74HCTLS78A	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear and Common Clock
KS54/74HCTLS86	Quad 2-Input Exclusive-OR Gates
KS54/74HCTLS90	Decade Counters
KS54/74HCTLS92	Divide-by-Twelve Counter
KS54/74HCTLS93	4 Bit Binary Counter Divide by Two and Divide by Eight
KS54/74HCTLS107A	Dual J-K Negative-Edge-Triggered Flip-Flops with Clear
KS54/74HCTLS109A	Dual J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear
KS54/74HCTLS112A	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear
KS54/74HCTLS123	Dual Retriggerable Monostable Multivibrators
KS54/74HCTLS125	Quad Buffers with 3-State Outputs
KS54/74HCTLS126	Quad Buffers with 3-State Outputs
KS54/74HCTLS132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs
KS54/74HCTLS133	13-Input NAND Gate
KS54/74HCTLS138	3-Line to 8-Line Decoders/Demultiplexers
KS54/74HCTLS139	Dual 1 of 4 Decoders/Demultiplexers
KS54/74HCTLS148	8-Line to 3-Line Priority Encoders
KS54/74HCTLS151	1 of 8 Data Selectors/Multiplexers
KS54/74HCTLS153	Dual 1 of 4 Data Selectors/Multiplexers
KS54/74HCTLS154	4-Line to 16-Line Decoders/Demultiplexers
KS54/74HCTLS155	Dual 2 to 4 Line Decoders/Demultiplexers
KS54/74HCTLS157	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74HCTLS158	Quad 2-Line to 1-Line Data Selectors/Multiplexers
KS54/74HCTLS160A	Synchronous 4-Bit Decade Counters
KS54/74HCTLS161A	Synchronous 4-Bit Binary Counters
KS54/74HCTLS162A	Synchronous 4-Bit Decade Counters
KS54/74HCTLS163A	Synchronous 4-Bit Binary Counters
KS54/74HCTLS164	8-Bit Serial-In/Parallel-Out Shift Registers
KS54/74HCTLS165	8-Bit Parallel-In/Serial-Out Shift Registers
KS54/74HCTLS166	8-Bit Parallel-In/Serial-Out Shift Registers with Clear
KS54/74HCTLS168	Synchronous 4-Bit Up/Down Decade Counters

## KS54/74HCTLS Family (continued)

Device	Function
KS54/74HCTLS169	Synchronous 4-Bit Up/Down Binary Counters
KS54/74HCTLS173	4-Bit D-Type Registers with 3-State Outputs
KS54/74HCTLS174	Hex D-Type Filp-Flops with Clear
KS54/74HCTLS175	Quad D-Type Filp-Flops with Clear
KS54/74HCTLS181	4-Bit Arithmetic Logic Unit
KS54/74HCTLS182	Look-Ahead Carry Generator
KS54/74HCTLS183	Dual High Speed Adder
KS54/74HCTLS190	Presettable Synchronous BCD Decade Up/Down Counter
KS54/74HCTLS191	Synchronous 4-Bit Up/Down Binary Counters
KS54/74HCTLS192	Presettable Synchronous BCD Decade Up/Down Counter
KS54/74HCTLS193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock
KS54/74HCTLS194	4-Bit Bidirectional Universal Shift Registers
KS54/74HCTLS195	4-Bit Bidirectional Universal Shift Registers
KS54/74HCTLS210	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS238	3-Line to 8-Line Decoders/Demultiplexers
KS54/74HCTLS239	Dual 1-of-4 Decoders/Demultiplexers
KS54/74HCTLS240	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS241	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS242	Quad Bus Transceivers with 3-State Outputs
KS54/74HCTLS243	Quad Bus Transceivers with 3-State Outputs
KS54/74HCTLS244	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS245	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS251	1 of 8 Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS253	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS257	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS258	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS259	8-Bit Addressable Latches
KS54/74HCTLS266	Quad Exclusive-NOR Gages with Open-Drain Outputs
KS54/74HCTLS273	Octal D-Type Filp-Flops
KS54/74HCTLS280	9-Bit Parity Generators/Checkers with Clear
KS54/74HCTLS299 A	8-Bit Universal Shift/Storage Registers with 3-State Outputs
KS54/74HCTLS322	8-Bit Shift Registers with Sign Extend
KS54/74HCTLS352	Dual 4-Line to 1-Line Data Selectors/Multiplexers
KS54/74HCTLS353	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs
KS54/74HCTLS365A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS366A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS367A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS368A	Hex Bus-Drivers with 3-State Outputs
KS54/74HCTLS373	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS374	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS377	Octal D-Type Flip-Flops with Clock Enable
KS54/74HCTLS390	Dual 4-Bit Decade Counters
KS54/74HCTLS393	Dual 4-Bit Binary Counters
KS54/74HCTLS399	Quad 2-Port Registers
KS54/74HCTLS423	Dual Retriggerable Monostable Multivibrators
KS54/74HCTLS465	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS466	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS467	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS468	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS518	8-Bit Identity Comparators
KS54/74HCTLS519	8-Bit Identity Comparators
KS54/74HCTLS520	8-Bit Identity Comparators
KS54/74HCTLS521	8-Bit Identity Comparators
KS54/74HCTLS522	8-Bit Identity Comparators
KS54/74HCTLS533	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS534	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS540	Octal Buffers and Line Drivers with 3-State Outputs
KS54/74HCTLS541	Octal Buffers and Line Drivers with 3-State Outputs



## KS54/74HCTLS Family (continued)

Device	Function
KS54/74HCTLS563	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS564	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS573	Octal D-Type Transparent Latches with 3-State Outputs
KS54/74HCTLS574	Octal D-Type Flip-Flops with 3-State Outputs
KS54/74HCTLS590	8-Bit Binary Counters with 3-State Output Register
KS54/74HCTLS591	8-Bit Binary Counters with 3-State Output Register
KS54/74HCTLS592	8-Bit Binary Counters with Input Register
KS54/74HCTLS593	8-Bit Binary Counters with Bidirectional Input Register Counter Output
KS54/74HCTLS595	8-Bit Shift Registers with Output Latches
KS54/74HCTLS596	8-Bit Shift Registers with Output Latches
KS54/74HCTLS597	8-Bit Shift Registers with Input Latches
KS54/74HCTLS640	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS643	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS645	Octal Bus Transceivers with 3-State Outputs
KS54/74HCTLS646	Octal 3-State Bus Transceivers with Registers
KS54/74HCTLS648	Octal 3-State Bus Transceivers with Registers
KS54/74HCTLS651	Octal 3-State Bus Transceivers with Registers
KS54/74HCTLS652	Octal 3-State Bus Transceivers with Registers
KS54/74HCTLS658	Octal Bus Transceivers with Parity
KS54/74HCTLS659	Octal Bus Transceivers with Parity
KS54/74HCTLS664	Octal Bus Transceivers with Parity
KS54/74HCTLS665	Octal Bus Transceivers with Parity
KS54/74HCTLS670	4-By-4 Register Files with 3-State Outputs
KS54/74HCTLS679	12-Bit Address Comparators
KS54/74HCTLS680	12-Bit Address Comparators
KS54/74HCTLS682	8-Bit Magnitude Comparators
KS54/74HCTLS684	8-Bit Magnitude Comparators
KS54/74HCTLS686	8-Bit Magnitude Comparators
KS54/74HCTLS688	8-Bit Identity Comparators
KS54/74HCTLS689	8-Bit Identity Comparators with Open-Drain Outputs
KS54/74HCTLS793	Octal Latches with Readback
KS54/74HCTLS794	Octal Registers with Readback
KS54/74HCTLS821	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS822	10-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS823	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS824	9-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS825	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS826	8-Bit Bus Interface Registers with 3-State Outputs
KS54/74HCTLS841	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS842	10-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS843	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS844	9-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS845	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS846	8-Bit Bus Interface D-Type Latches with 3-State Outputs
KS54/74HCTLS4049	Hex Inverting Logic Level Down Converters
KS54/74HCTLS4050	Hex Logic Level Down Converters

## 2. Functional Selection Guide

Function	Part Number KS54/74AHCT KS54/74HCTLs	Description	Package
Gates and Inverters	00	Quad 2-Input NAND Gates	14 DIP/SOP
	01	Quad 2-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	02	Quad 2-Input NOR Gates	14 DIP/SOP
	03	Quad 2-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	04	Hex Inverters	14 DIP/SOP
	05	Hex Inverters with Open-Drain Outputs	14 DIP/SOP
	08	Quad 2-Input AND Gates	14 DIP/SOP
	09	Quad 2-Input AND Gates with Open-Drain Outputs	14 DIP/SOP
	10	Triple 3-Input NAND Gates	14 DIP/SOP
	11	Triple 3-Input AND Gates	14 DIP/SOP
	12	Triple 3-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	14	Hex Schmitt-Trigger Inverters	14 DIP/SOP
	20	Dual 4-Input NAND Gates	14 DIP/SOP
	21	Dual 4-Input AND Gates	14 DIP/SOP
	22	Dual 4-Input NAND Gates with Open-Drain Outputs	14 DIP/SOP
	27	Triple 3-Input NOR Gates	14 DIP/SOP
	30	8-Input NAND Gate	14 DIP/SOP
	32	Quad 2-Input OR Gates	14 DIP/SOP
	51	Dual AND-OR-Invert Gates	14 DIP/SOP
	58	Dual AND-OR Gates	14 DIP/SOP
86	Quad 2-Input Exclusive-OR Gates	14 DIP/SOP	
132	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs	14 DIP/SOP	
133	13-Input NAND Gate	16 DIP/SOP	
266	Quad Exclusive-NOR Gates with Open-Drain Outputs	16 DIP/SOP	
Buffers and Line Drivers	125	Quad Buffers with 3-State Outputs	14 DIP/SOP
	126	Quad Buffers with 3-State Outputs	14 DIP/SOP
	210	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	240	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	241	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	244	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	365	Hex Bus-Drivers with 3-State Outputs	16 DIP/SOP
	366	Hex Bus-Drivers with 3-State Outputs	16 DIP/SOP
	367	Hex Bus-Drivers with 3-State Outputs	16 DIP/SOP
	368	Hex Bus-Drivers with 3-State Outputs	16 DIP/SOP
	465	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	466	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	467	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
	468	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP
540	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP	
541	Octal Buffers and Line Drivers with 3-State Outputs	20 DIP/SOP	
Level Shifters	4049	Hex Inverting Logic Level Down Converters	16 DIP/SOP
	4050	Hex Logic Level Down Converters	16 DIP/SOP
Flip-Flops	73	Dual J-K Negative-Edge-Triggered Flip-Flops with Clear	14 DIP/SOP
	74	Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear	14 DIP/SOP
	76	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear	16 DIP/SOP
	78	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset, Common Clear and Common Clock	14 DIP/SOP
	107	Dual J-K Negative-Edge-Triggered Flip-Flops with Clear	14 DIP/SOP
	109	Dual J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear	16 DIP/SOP
	112	Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear	16 DIP/SOP
	173	4-Bit D-Type Registers with 3-State Outputs	16 DIP/SOP
	174	Hex D-Type Flip-Flops with Clear	16 DIP/SOP
	175	Quad D-Type Flip-Flops with Clear	16 DIP/SOP
	273	Octal D-Type Flip-Flops	20 DIP/SOP
	374	Octal D-Type Flip-Flops with 3-State Outputs	20 DIP/SOP

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## Functional Selection Guide (continued)

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
	377	Octal D-Type Flip-Flops with Clock Enable	20 DIP/SOP
	399	Quad 2-Port Registers	16 DIP/SOP
	534	Octal D-Type Flip-Flops with 3-State Outputs	20 DIP/SOP
	564	Octal D-Type Flip-Flops with 3-State Outputs	20 DIP/SOP
	574	Octal D-Type Flip-Flops with 3-State Outputs	20 DIP/SOP
	670	4-By-4 Register Files with 3-State Outputs	16 DIP/SOP
	794	Octal Registers with Readback	20 DIP/SOP
	821	10-Bit Bus Interface Registers with 3-State Outputs	24 DIP/SOP
	822	10-Bit Bus Interface Registers with 3-State Outputs	24 DIP/SOP
	823	9-Bit Bus Interface Registers with 3-State Outputs	24 DIP/SOP
	824	9-Bit Bus Interface Registers with 3-State Outputs	24 DIP/SOP
	825	8-Bit Bus Interface Registers with 3-State Outputs	24 DIP/SOP
	826	8-Bit Bus Interface Registers with 3-State Outputs	24 DIP/SOP
Latches	75	Quad Bistable Transparent Latches	16 DIP/SOP
	77	Quad D-Type Latches	14 DIP/SOP
	259	8-Bit Addressable Latches	16 DIP/SOP
	373	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP/SOP
	533	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP/SOP
	563	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP/SOP
	573	Octal D-Type Transparent Latches with 3-State Outputs	20 DIP/SOP
	793	Octal Latches with Readback	20 DIP/SOP
	841	10-Bit Bus Interface D-Type Latches with 3-State Outputs	24 DIP/SOP
	842	10-Bit Bus Interface D-Type Latches with 3-State Outputs	24 DIP/SOP
	843	9-Bit Bus Interface D-Type Latches with 3-State Outputs	24 DIP/SOP
	844	9-Bit Bus Interface D-Type Latches with 3-State Outputs	24 DIP/SOP
	845	8-Bit Bus Interface D-Type Latches with 3-State Outputs	24 DIP/SOP
	846	8-Bit Bus Interface D-Type Latches with 3-State Outputs	24 DIP/SOP
Multiplexers	151	1 of 8 Data Selectors/Multiplexers	16 DIP/SOP
	153	Dual 1 of 4 Data Selectors/Multiplexers	16 DIP/SOP
	157	Quad 2-Line to 1-Line Data Selectors/Multiplexers	16 DIP/SOP
	158	Quad 2-Line to 1-Line Data Selectors/Multiplexers	16 DIP/SOP
	251	1 of 8 Data Selectors/Multiplexers with 3-State Outputs	16 DIP/SOP
	253	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs	16 DIP/SOP
	257	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs	16 DIP/SOP
	258	Quad 2-Line to 1-Line Data Selectors/Multiplexers with 3-State Outputs	16 DIP/SOP
	352	Dual 4-Line to 1-Line Data Selectors/Multiplexers	16 DIP/SOP
	353	Dual 1 of 4 Data Selectors/Multiplexers with 3-State Outputs	16 DIP/SOP
Shift Registers	164	8-Bit Serial-In/Parallel-Out Shift Registers	14 DIP/SOP
	165	8-Bit Parallel-In/Serial-Out Shift Registers	16 DIP/SOP
	166	8-Bit Parallel-In/Serial-Out Shift Registers with Clear	16 DIP/SOP
	194	4-Bit Bidirectional Universal Shift Registers	16 DIP/SOP
	195	4-Bit Bidirectional Universal Shift Registers	16 DIP/SOP
	299	8-Bit Universal Shift/Storage Registers with 3-State Outputs	20 DIP/SOP
	322	8-Bit Shift Registers with Sign Extend	20 DIP/SOP
	595	8-Bit Shift Registers with Output Latches	16 DIP/SOP
	596	8-Bit Shift Registers with Output Latches	16 DIP/SOP
	597	8-Bit Shift Registers with Input Latches	16 DIP/SOP
Transceivers	242	Quad Bus Transceivers with 3-State Outputs	14 DIP/SOP
	243	Quad Bus Transceivers with 3-State Outputs	14 DIP/SOP
	245	Octal Bus Transceivers with 3-State Outputs	20 DIP/SOP
	640	Octal Bus Transceivers with 3-State Outputs	20 DIP/SOP
	643	Octal Bus Transceivers with 3-State Outputs	20 DIP/SOP
	645	Octal Bus Transceivers with 3-State Outputs	20 DIP/SOP
	646	Octal 3-State Bus Transceivers with Registers	24 DIP/SOP
	648	Octal 3-State Bus Transceivers with Registers	24 DIP/SOP

## Functional Selection Guide (continued)

Function	Part Number KS54/74AHCT KS54/74HCTLS	Description	Package
	651	Octal 3-State Bus Transceivers with Registers	24 DIP/SOP
	652	Octal 3-State Bus Transceivers with Registers	24 DIP/SOP
	658	Octal Bus Transceivers with Parity	24 DIP/SOP
	659	Octal Bus Transceivers with Parity	24 DIP/SOP
	664	Octal Bus Transceivers with Parity	24 DIP/SOP
	665	Octal Bus Transceivers with Parity	24 DIP/SOP
Counters	90	Decade Counters	14 DIP/SOP
	92	Divide-by-Twelve Counter	14 DIP/SOP
	93	4 Bit Binary Counter Divide by Two and Divide by Eight	14 DIP/SOP
	160	Synchronous 4-Bit Decade Counters	16 DIP/SOP
	161	Synchronous 4-Bit Binary Counters	16 DIP/SOP
	162	Synchronous 4-Bit Decade Counters	16 DIP/SOP
	163	Synchronous 4-Bit Binary Counters	16 DIP/SOP
	168	Synchronous 4-Bit Up/Down Decade Counters	16 DIP/SOP
	169	Synchronous 4-Bit Up/Down Binary Counters	16 DIP/SOP
	190	Presettable Synchronous BCD Decade Up/Down Counter	16 DIP/SOP
	191	Synchronous 4-Bit Up/Down Binary Counters	16 DIP/SOP
	192	Presettable Synchronous BCD Decade Up/Down Counter	16 DIP/SOP
	193	Synchronous 4-Bit Up/Down Binary Counters with Dual Clock	16 DIP/SOP
	390	Dual 4-Bit Decade Counters	16 DIP/SOP
	393	Dual 4-Bit Binary Counters	16 DIP/SOP
	590	8-Bit Binary Counters with 3-State Output Register	16 DIP/SOP
	591	8-Bit Binary Counters with 3-State Output Register	16 DIP/SOP
	592	8-Bit Binary Counters with Input Register	16 DIP/SOP
	593	8-Bit Binary Counters with Bidirectional Input Register Counter Output	20 DIP/SOP
Decoders Encoders	42	BCD-to-Decimal Decoder	16 DIP/SOP
	138	3-Line to 8-Line Decoders/Demultiplexers	16 DIP/SOP
	139	Dual 1 of 4 Decoders/Demultiplexers	16 DIP/SOP
	148	8-Line to 3-Line Priority Encoders	16 DIP/SOP
	154	4-Line to 16-Line Decoders/Demultiplexers	24 DIP/SOP
	155	Dual 2 to 4 Line Decoders/Demultiplexers	16 DIP/SOP
	238	3-Line to 8-Line Decoders/Demultiplexers	16 DIP/SOP
	239	Dual 1-of-4 Decoders/Demultiplexers	16 DIP/SOP
Multivibrators	123	Dual Retriggerable Monostable Multivibrators	16 DIP/SOP
	423	Dual Retriggerable Monostable Multivibrators	16 DIP/SOP
Arithmetic Circuits	181	4-Bit Arithmetic Logic Unit	24 DIP/SOP
	182	Look-Ahead Carry Generator	16 DIP/SOP
	183	Dual High Speed Adder	14 DIP/SOP
	280	9-Bit Parity Generators/Checkers with Clear	14 DIP/SOP
	518	8-Bit Identity Comparators	20 DIP/SOP
	519	8-Bit Identity Comparators	20 DIP/SOP
	520	8-Bit Identity Comparators	20 DIP/SOP
	521	8-Bit Identity Comparators	20 DIP/SOP
	522	8-Bit Identity Comparators	20 DIP/SOP
	679	12-Bit Address Comparators	20 DIP/SOP
	680	12-Bit Address Comparators	20 DIP/SOP
	682	8-Bit Magnitude Comparators	20 DIP/SOP
	684	8-Bit Magnitude Comparators	20 DIP/SOP
	686	8-Bit Magnitude Comparators	20 DIP/SOP
	688	8-Bit Identity Comparators	20 DIP/SOP
	689	8-Bit Identity Comparators with Open-Drain Outputs	20 DIP/SOP

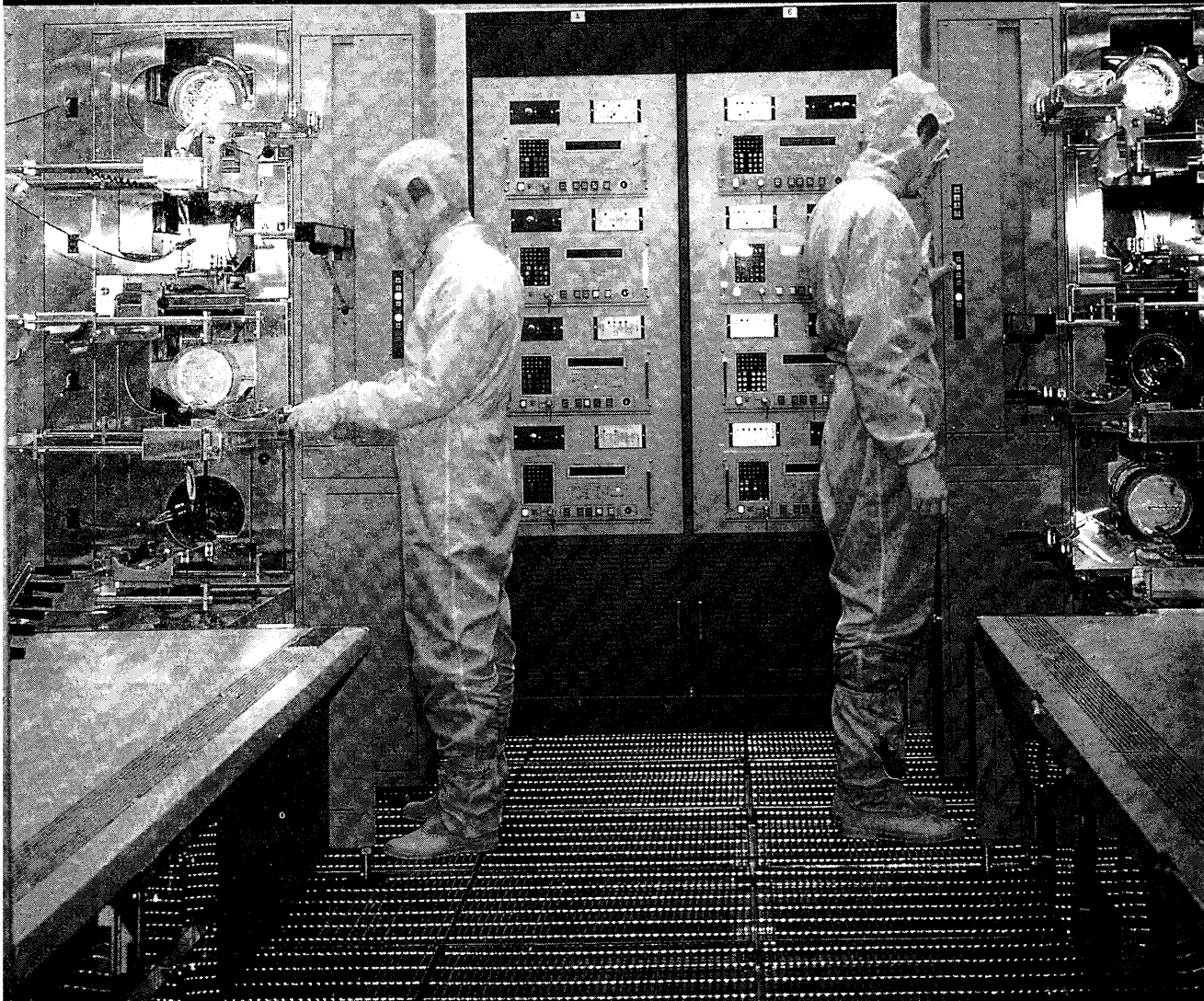
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# NOTES

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# ***PARAMETER MEASUREMENT INFORMATION***

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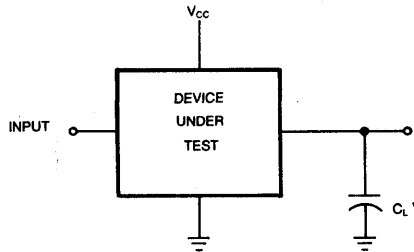




# PARAMETER MEASUREMENT INFORMATION

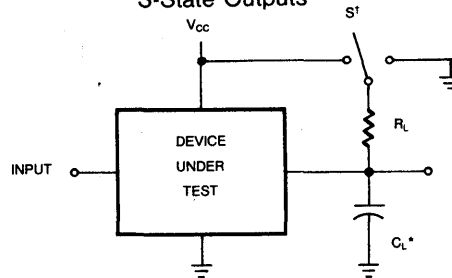
## AC SWITCHING TEST CIRCUITS

### Totem-Pole Outputs



\* $C_L$  includes load and test jig capacitance

### 3-State Outputs

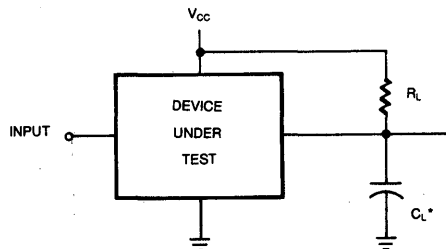


\* $C_L$  includes load and test jig capacitance

$S^\dagger = V_{CC}$  for  $t_{pZL}$  and  $t_{pLZ}$  measurements

$S = GND$  for  $t_{pZH}$  and  $t_{pHZ}$  measurements.

### Open-Drain Outputs

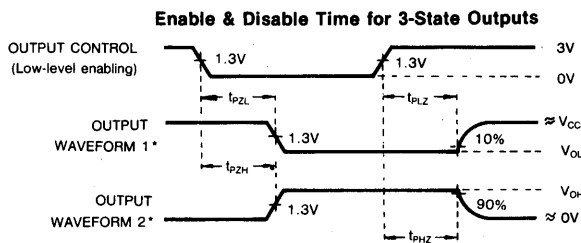
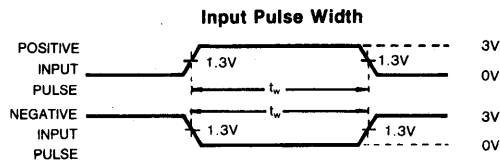
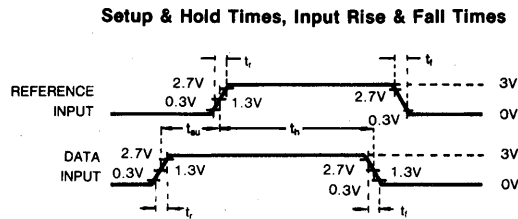
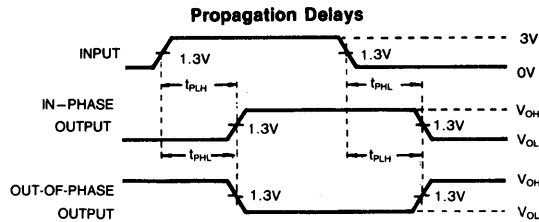


\* $C_L$  includes load and test jig capacitance



# PARAMETER MEASUREMENT INFORMATION

## TIMING WAVEFORMS





- \* Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. This waveform is applicable to both 3-state and open-drain outputs.
- \* Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.



# PARAMETER MEASUREMENT INFORMATION

## DEFINITIONS OF TERMS & SYMBOLS

### FUNCTION TABLE SYMBOLS

- H = Steady state high level
- L = Steady state low level
- ↑ = Transition from low to high level
- ↓ = Transition from high to low level
- X = Don't care (high, low states or transitions)
- Z = High-impedance state of a 3-state output
- a..h = The level of steady-state inputs at inputs A thru H, respectively
- $Q_0$  = Level of Q before the indicated steady-state input conditions were established
- $\bar{Q}_0$  = Complement of  $Q_0$  or level of  $\bar{Q}$  before the indicated steady-state conditions were established
- $Q_n$  = Level of Q before the most recent active transition indicated by ↑ or ↓
-  = One high-level pulse
-  = One low-level pulse

TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓  
If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as level (H, L,  $Q_0$ , or  $\bar{Q}_0$ ), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit)

## DC Characteristics Terms

### $V_{IH}$ High-Level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

### $V_{IL}$ Low-Level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

### $V_{OH}$ High-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

### $V_{OL}$ Low-Level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

### $V_{T+}$ Positive-Going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage,  $V_{T-}$ .

# PARAMETER MEASUREMENT INFORMATION

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## **V<sub>T-</sub> Negative-Going threshold level**

The voltage at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V<sub>T+</sub>.

## **I<sub>O</sub> Output Current**

The current into\* an output with input conditions applied that, according to the product specification, will establish a high or a low level at the output.

## **I<sub>IN</sub> Input Current**

The current into\* an input when a high or a low level voltage is applied to that input.

## **I<sub>OZ</sub> Off-State (high-impedance-state) output current (of a three-state output)**

The current flowing into\* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a low-voltage level (if it were enabled) when the externally applied voltage is high; or high-voltage level when the externally applied voltage is low.

## **I<sub>CC</sub> Supply current**

The current into\* the V<sub>CC</sub> supply terminal of an integrated circuit.

\*Current out of a terminal is given as negative value.

## AC CHARACTERISTICS TERMS

### **t<sub>r</sub> Rise time**

The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the high level.

### **t<sub>f</sub> Fall time**

The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

### **f<sub>max</sub> Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of a logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

### **t<sub>PLH</sub> Propagation delay time, low-to-high-level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

### **t<sub>PHL</sub> Propagation delay time, high-to-low-level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

### **t<sub>PZH</sub> Enable time (of a three-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from a high-impedance (off) state to the defined high level.

### **t<sub>PZL</sub> Enable time (of a three-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from a high-impedance (off) state to the defined low level.

# PARAMETER MEASUREMENT INFORMATION

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**t<sub>PHZ</sub> Disable time (of a three-state output) from high level**

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from the defined high level to high-impedance (off) state.

**t<sub>PLZ</sub> Disable time (of a three-state output) from low level**

The time interval between the specified reference points on the input and output voltage waveforms with the three-state outputs changing from the defined high level to high-impedance (off) state.

**t<sub>w</sub> Pulse width**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

**t<sub>su</sub> Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

**t<sub>h</sub> Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

**C<sub>PD</sub> Power dissipation capacitance**

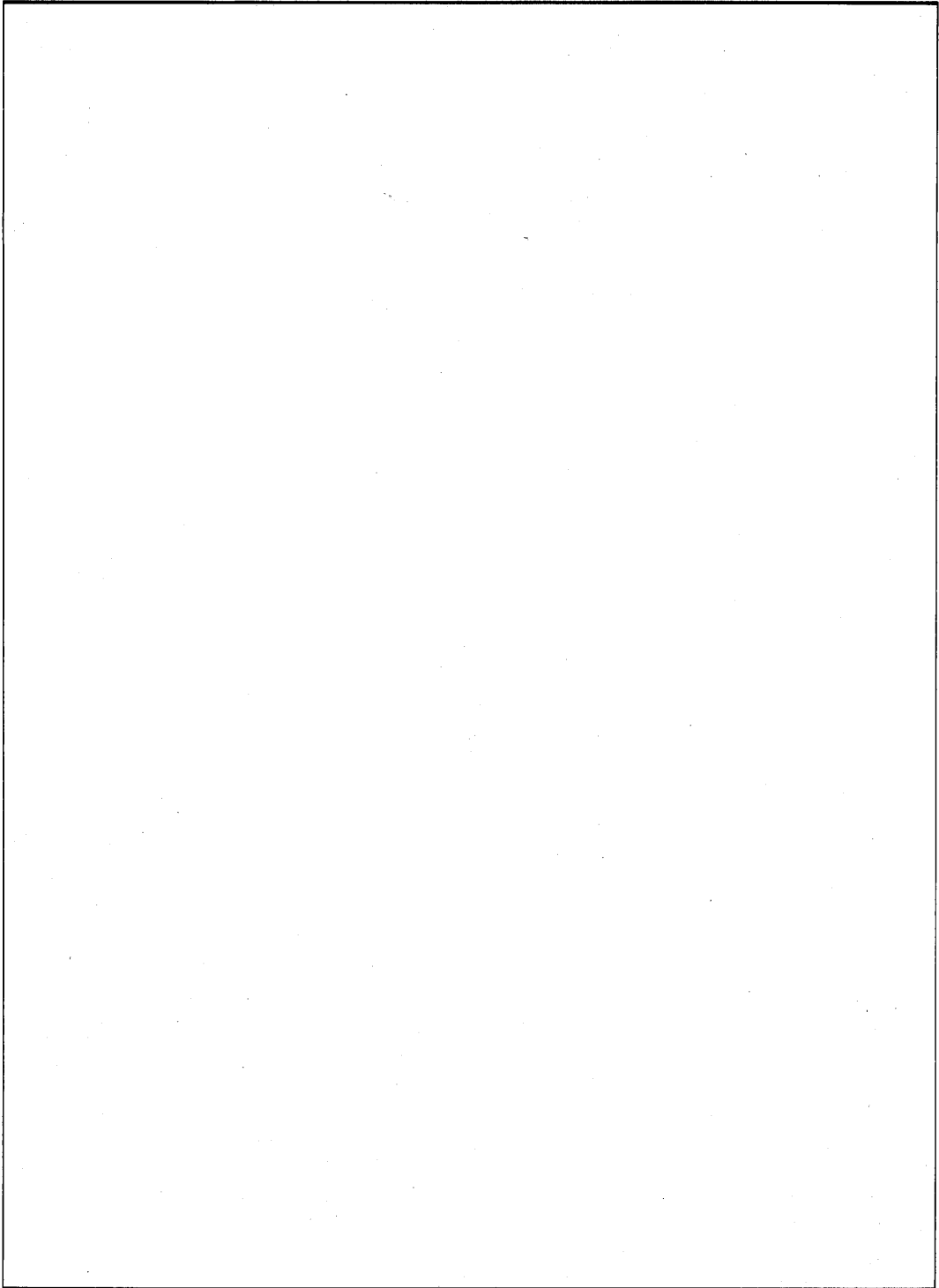
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):

$$P_D = C_{PD} V_{CC}^2 f$$



# NOTES

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**TECHNICAL OVERVIEW** 3



# TECHNICAL OVERVIEW

## INTRODUCTION

The 54/74AHCT Advanced High-Speed CMOS and the 54/74HCTLS High-Speed CMOS logic families were designed to offer the most desirable features of their CMOS and bipolar predecessors. They have the low power dissipation, superior noise immunity, wide voltage and temperature ranges and the very low input currents of the other high-speed CMOS logic families, in addition to the high speed and drive capability of LS and ALS bipolar logic.

The AHCT family is an equivalent of the bipolar ALS and can readily replace ALS in most existing applications to reduce power dissipation. In many applications, AHCT parts can also be used as replacements for FAST™ and S (Schottky). The HCTLS parts, on the other hand, meet and exceed all of industry-standard LS and HCT specifications, and can be used as replacements to these to lower the power dissipation and improve performance. The design tips section on page 53 gives specific details for direct replacement. Figure 1 shows how AHCT and HCTLS families rank with the other bipolar technologies in terms of speed and power dissipation.

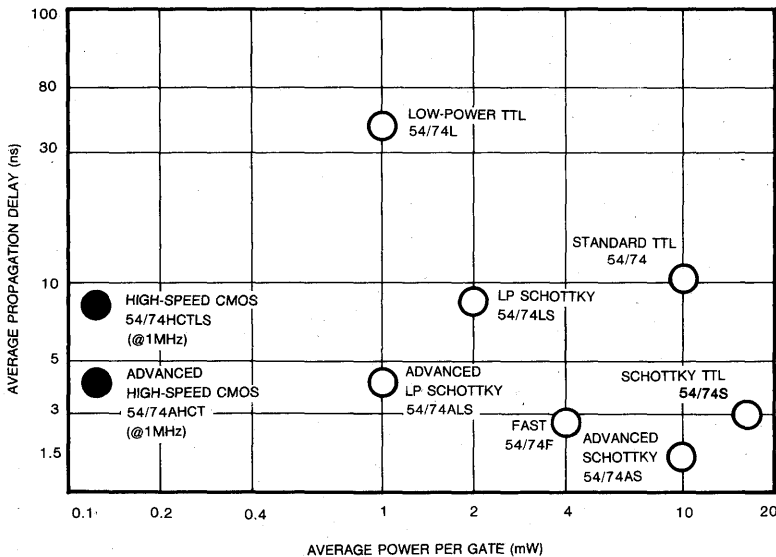


FIGURE 1. Power dissipation vs gate delay characteristics for a two-input NAND gate (74XX00) implemented in various bipolar and CMOS technologies

Both families feature TTL input voltage levels which enable them to interface with all TTL, NMOS or CMOS outputs without any external components. All AHCT and HCTLS parts are fully characterized and specified over the 4.5 to 5.5V voltage range, and the industrial (-40 to 85°C) and military (-55 to 125°C) temperature ranges. This is a significant improvement over the older bipolar logic families, where, for example LS would specify DC specs over 4.75V to 5.25V and AC specs only at 5V and room temperature. (ALS is specified over 4.5 to 5.5V and 0 to 70°C). A comparison of the key characteristics for an octal buffer illustrates these improvements clearly in Figure 2. The DC characteristics common to all AHCT and HCTLS parts are listed in Figure 3.



	TTL			SAMSUNG CMOS		OTHER CMOS		
	74LS244	74ALS244	74F244	74HCTLS244	74AHCT244	74HC244	74HCT244	
Operating Voltage Range (Commercial)	4.75V to 5.25V	4.5V to 5.5V	4.75V to 5.25V	4.5V to 5.5V	4.5V to 5.5V	2V to 6V	4.5V to 5.5V	
Operating Temperature Range (Commercial)	0°C to 70°C	0°C to 70°C	0°C to 70°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	
Maximum Propagation Delay ( $C_L = 50$ pF)	18 ns ( $V_{CC} = 5V$ , $T_a = 25^\circ C$ )	10 ns (Over Operating Conditions)	6.5 ns (Over Operating Conditions)	18 ns ( $V_{CC} = 5V$ , $T_a = 25^\circ C$ )	10 ns (Over Operating Conditions)	20 ns ( $V_{CC} = 5V$ , $T_a = 25^\circ C$ )	18 ns ( $V_{CC} = 5V$ , $T_a = 25^\circ C$ )	
Maximum Quiescent Current	54 mA	27 mA	90 mA	0.08 mA	0.08 mA	0.08 mA	0.08 mA	
Typical Power Dissipation	Static	120 mW	70 mW	260 mW	0.004 mW	0.004 mW	0.004 mW	0.004 mW
	At 100 kHz (All inputs toggling)	120 mW	70 mW	260 mW	0.6 mW	0.6 mW	1.0 mW	1.8 mW
Output Drive Currents	$I_{OH}$	-3 mA ( $V_{OH} = 2.4V$ ) -15 mA ( $V_{OH} = 2.0V$ )	-3 mA ( $V_{OH} = 2.4V$ ) -15 mA ( $V_{OH} = 2.0V$ )	-15 mA ( $V_{OH} = 2.0V$ )	-6 mA ( $V_{OH} = 3.84V$ )	-6 mA ( $V_{OH} = 3.84V$ )	-6 mA ( $V_{OH} = 3.84V$ )	-6 mA ( $V_{OH} = 3.84V$ )
	$I_{OL}$	12 mA ( $V_{OL} = 0.4V$ ) 24 mA ( $V_{OL} = 0.5V$ )	12 mA ( $V_{OL} = 0.4V$ ) 24 mA ( $V_{OL} = 0.5V$ )	64 mA ( $V_{OL} = 0.55V$ )	12 mA ( $V_{OL} = 0.4V$ ) 24 mA ( $V_{OL} = 0.5V$ )	12 mA ( $V_{OL} = 0.4V$ ) 24 mA ( $V_{OL} = 0.5V$ )	6 mA ( $V_{OL} = 0.33V$ )	6 mA ( $V_{OL} = 0.33V$ )
Input Threshold Voltages	$V_{IL}$	0.8V	0.8V	0.8V	0.8V	0.8V	0.9V ( $V_{CC} = 4.5V$ )	0.8V
	$V_{IH}$	2.0V	2.0V	2.0V	2.0V	2.0V	3.15V ( $V_{CC} = 4.5V$ )	2.0V
Input Currents	$I_{IL}$	-0.2 mA ( $V_i = 0.4V$ )	-0.1 mA ( $V_i = 0.4V$ )	-1.6 mA ( $V_i = 0.5V$ )	-1.0 $\mu A$	-1.0 $\mu A$	-1.0 $\mu A$	-1.0 $\mu A$
	$I_{IH}$	20 $\mu A$ ( $V_i = 2.7V$ )	20 $\mu A$ ( $V_i = 2.7V$ )	20 $\mu A$ ( $V_i = 2.7V$ )	1.0 $\mu A$	1.0 $\mu A$	1.0 $\mu A$	1.0 $\mu A$

FIGURE 2. Key performance characteristics for 74XXX244 octal buffer

# TECHNICAL OVERVIEW

The Samsung CMOS logic families include a comprehensive set of buffers, registers, latches and transceivers that are offered in 8, 9 and 10-bit versions. A wide variety of gates, flip-flops, multiplexers, shift registers, encoder/decoders, schmitt triggers and multivibrators complete the family of 157 part types. Each function is available in both AHCT and HCTLS version.

Characteristic	Symbol	Conditions	T <sub>a</sub> = 25°C		Commercial T <sub>a</sub> = -40°C to +85°C		Military T <sub>a</sub> = -55°C to +125°C		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0			V
Minimum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads I <sub>OH</sub> =-20μA	V <sub>CC</sub>	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1	V <sub>CC</sub> -0.1		V
			Standard Outputs I <sub>OH</sub> =-4 mA	4.2	3.98	3.84	3.7		
			Bus-Driver Outputs I <sub>OH</sub> =-6 mA	4.2	3.98	3.84	3.7		
Minimum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads I <sub>OL</sub> =20 μA	0.1	0.1	0.1	0.1		V
			Standard Outputs I <sub>OL</sub> =4 mA I <sub>OL</sub> =8 mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4		
			Bus-Driver Outputs I <sub>OL</sub> =12 mA I <sub>OL</sub> =24 mA	0.2 0.3	0.26 0.39	0.33 0.5	0.4		
Maximum Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> =Max, V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	1.0		μA	
Maximum 3-State Leakage Current	I <sub>OZ</sub>	V <sub>CC</sub> =Max, Enable=V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0		μA	
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>CC</sub> =Max V <sub>IN</sub> =V <sub>CC</sub> or GND All Outputs Open	SSI Circuits		2.0	20.0	40.0	μA	
			Dual and Quad Flip-Flops & Latches		4.0	40.0	80.0		
			MSI Circuits & Circuits with High-Current Outputs		8.0	80.0	160.0		

FIGURE 3. DC characteristics of the 54/74AHCT and 54/74 HCTLS Families (V<sub>CC</sub>=5.0V ±10%)

# TECHNICAL OVERVIEW

## PROCESS TECHNOLOGY

The high performance of the AHCT and HCTLS is a result of a unique self-aligned metal-gate CMOS process technology that features  $1.2\mu\text{m}$  effective gate lengths and double metallization. The following table compares the general characteristics of this process with other existing CMOS and bipolar technologies used for logic circuits:

	SAMSUNG CMOS	INDUSTRY CMOS (HC & HCT)	INDUSTRY ALS
Number of Masking Steps	8	12-14	13
Number of Metal Layers	2	1	2
Minimum Feature Size (drawn)	$2\mu\text{m}$	$3\text{-}4\mu\text{m}$	$4\mu\text{m}$
Interconnections	All Metal	Poly & Metal	All Metal
Relative Die Size	1X	2.5-5X	1.5-2X
Manufacturing Equipment	Standard	Standard	Standard

Samsung's CMOS process was designed from the ground up to be a scaled two-layer metal CMOS process (see Figure 4 for a cross section). The goal was to make the process as simple as possible, and be able to readily control gate length and gate dielectric thickness. The process uses 8 masking steps. Other semiconductor manufacturers, in trying to go to two-layer metal short-channel processes have generally embellished pre-existing silicon-gate processes and have wound up with 12-14 masking steps. More masking steps, of course, make wafers more costly, but most importantly, reduce yield because of more chances for random defects.

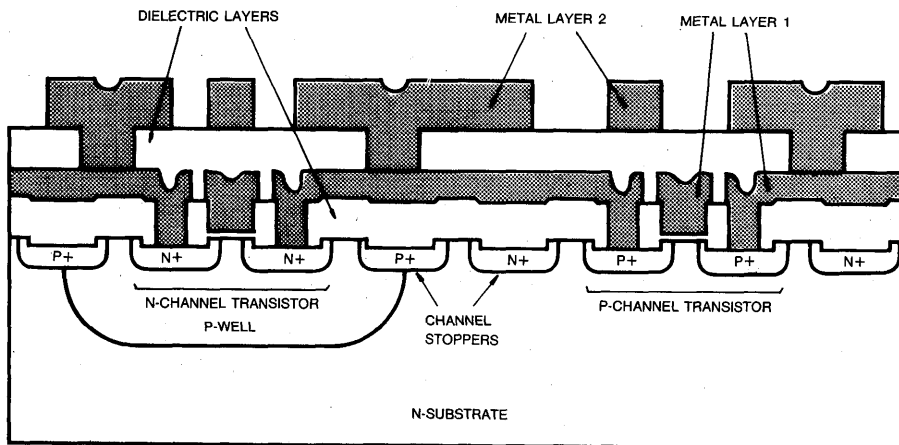
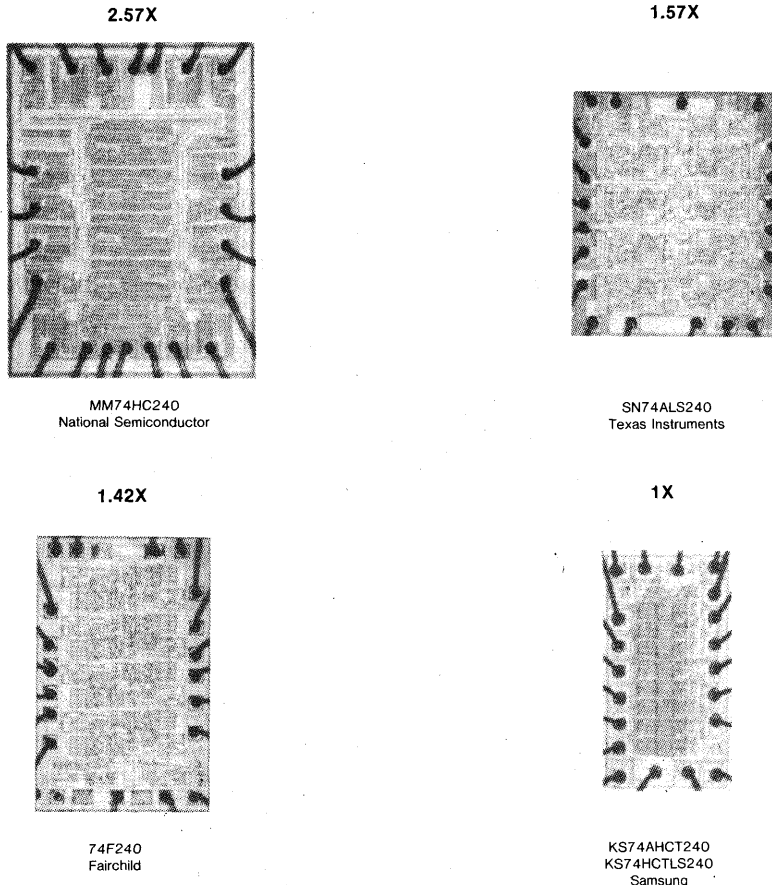


FIGURE 4. Samsung CMOS process cross section for an inverter stage

The Samsung process, with the short  $2\mu\text{m}$  channel lengths ( $1.2\mu\text{m}$  effective), yields gate delays as fast as those of the bipolar LS and ALS processes, and the same short channel lengths allow high-current output drivers to occupy a modest silicon area. Generally, the AHCT and HCTLS logic chips are much smaller than their CMOS and bipolar equivalents (see Figure 5). In achieving this small size, two-layer metal is as important as having short channels. For example, in the on-chip bussing of ground and  $V_{CC}$  to the output drivers, very wide metal lines have to be used that take considerable area. In this case, if these lines are in Metal 2, no extra area is wasted since the circuitry can be placed underneath.

# TECHNICAL OVERVIEW



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FIGURE 5. Die size comparison for a 74XXX244 from various technologies.

## INPUT CHARACTERISTICS

The input stage of an AHCT or HCTLS circuit is illustrated in *Figure 6*. It consists of a diode protection network and a CMOS inverter stage that has very high input impedance. The ultra-low input current specified in the data sheets ( $1\mu\text{A}$  maximum) is due to the reverse leakage currents of the diodes and is not used for "driving" the CMOS transistors i.e. the inputs are voltage-driven. This makes AHCT and HCTLS inputs very easy to drive and results in a very high fan-in capability.

TTL-compatible input threshold voltages of  $0.8\text{V } V_{IL}$  and  $2.0\text{V } V_{IH}$  are accomplished by properly sizing the p- and n-channel transistors of the CMOS inverter stage. The actual logic transition takes place mid-way between these values, at  $1.4\text{V}$ , and is very sharp compared to TTL logic due to the very high gain of the first inverter stage. This is illustrated in *Figure 7* for a two-input NAND gate. Note that the input threshold for CMOS is much more stable with temperature than that for LS.

While the AHCT and HCTLS parts are recommended as direct replacements for ALS and LS, one needs to pay attention to not leaving any inputs floating, i.e. unconnected. Since the inputs have very high impedance, they can easily pick up external noise which can result in random switching of the device and high power consumption. Therefore, all unused inputs must be terminated to either  $V_{CC}$  or ground.

# TECHNICAL OVERVIEW

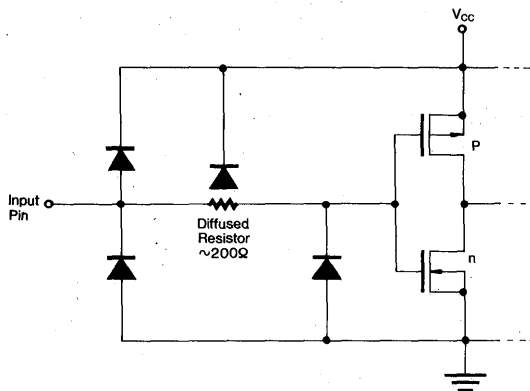


FIGURE 6. The input circuit of AHCT and HCTLS parts.

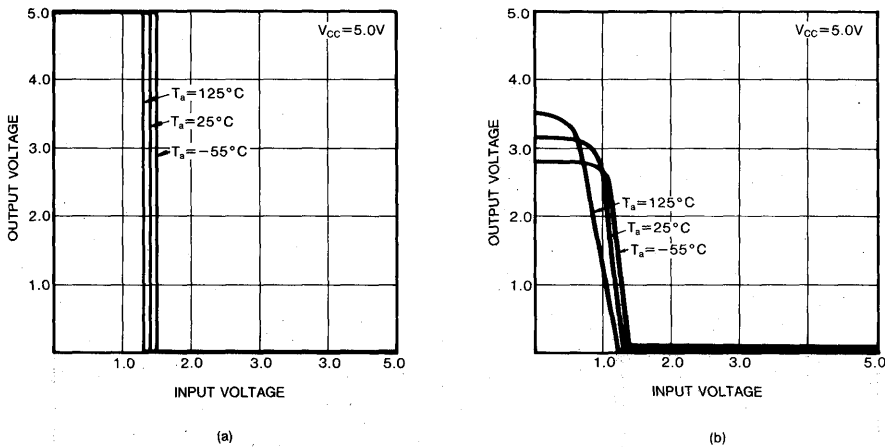


FIGURE 7. Input-Output transfer characteristics for (a) AHCT/HCTLS00, (b) LS00.

# TECHNICAL OVERVIEW

## OUTPUT CHARACTERISTICS

A typical output stage of an AHCT or HCTLS part consists of a complementary pair of transistors and a diode protection network (see Figure 8). Unlike the bipolar outputs, the voltage swing is rail-to-rail, which is responsible for the improved noise margin of AHCT/HCTLS systems. The drive capability of these outputs is similar to the bipolar parts, i.e. 24mA or 8mA  $I_{OL}$  (at 0.5V  $V_{OL}$ ) for bus-driver and standard outputs, respectively. This means that AHCT and HCTLS parts can drive as many loads or as large bus capacitances as their ALS and LS counterparts. Figure 9 shows a comparison of the output drive capabilities of AHCT/HCTLS and LS/ALS outputs. Figure 10 illustrates the variations of  $I_{OL}$  and  $I_{OH}$  with supply voltage and temperature for a standard output ('00) and a bus driver ('244).

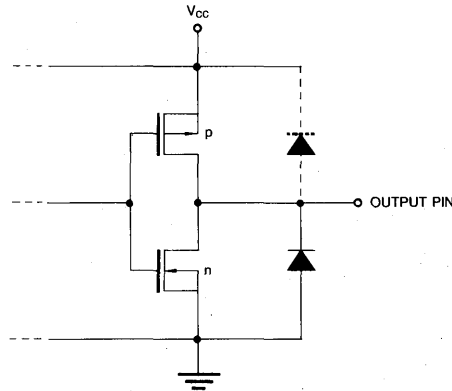


FIGURE 8. A typical output circuit of an AHCT or HCTLS part.  
The upper diode is parasitic and embedded in the p-channel transistor.

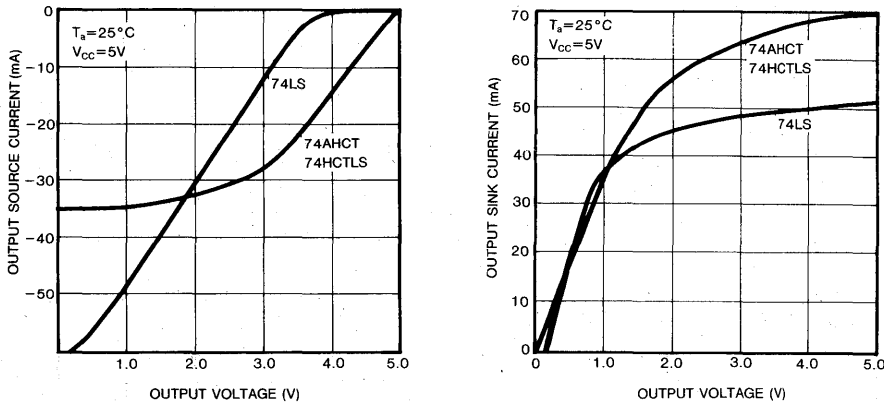
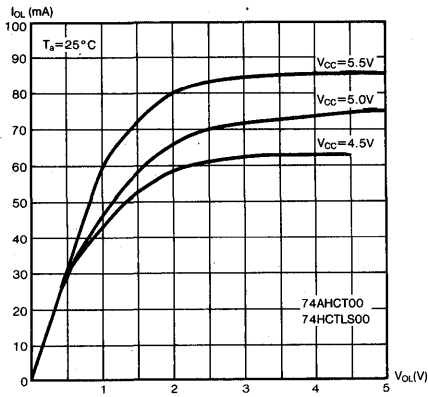
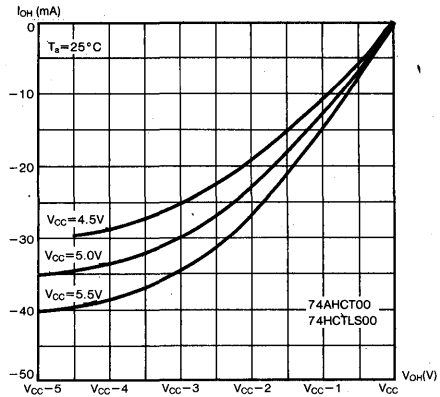


FIGURE 9. Comparison of standard AHCT/HCTLS and standard LS output (a) Source, and (b) sink currents.

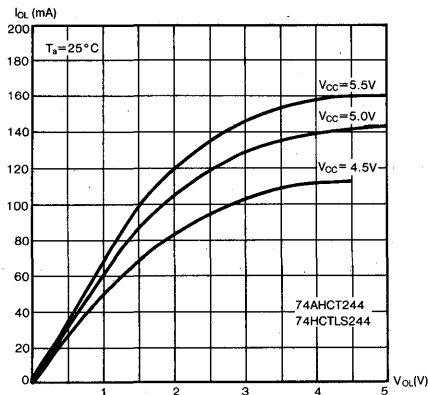
# TECHNICAL OVERVIEW



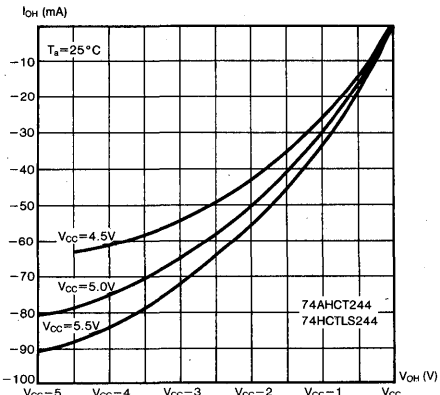
(a)



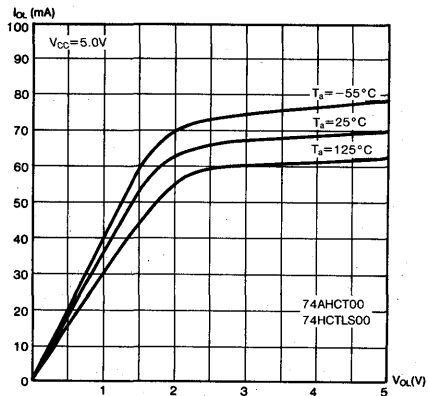
(b)



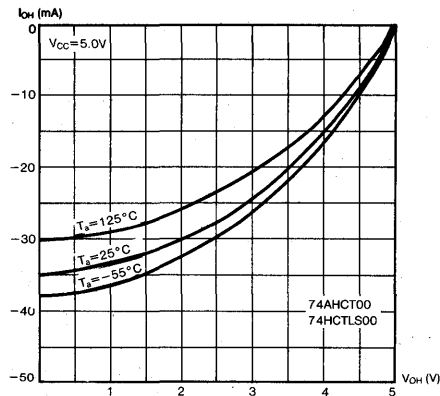
(c)



(d)



(e)



(f)

# TECHNICAL OVERVIEW

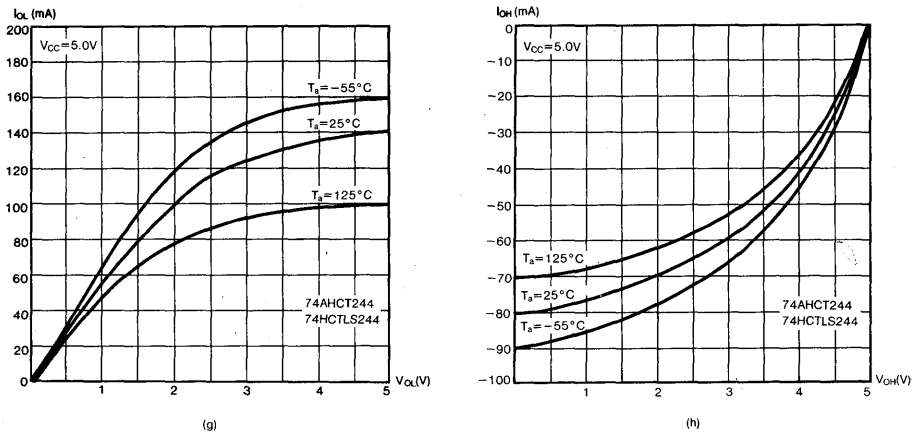


FIGURE 10. Output current variations with supply voltage and temperature for standard [(a), (b), (e) (f)] and bus driver [(c), (d), (g), (h)] outputs.

3

## NOISE IMMUNITY & NOISE MARGINS

The term "noise" in the context of digital circuits and systems means unwanted transient variations of voltages and currents at logic nodes. Typically noise is transferred to logic nodes or interconnecting lines by unwanted capacitive or inductive coupling, as illustrated in Figure 11.

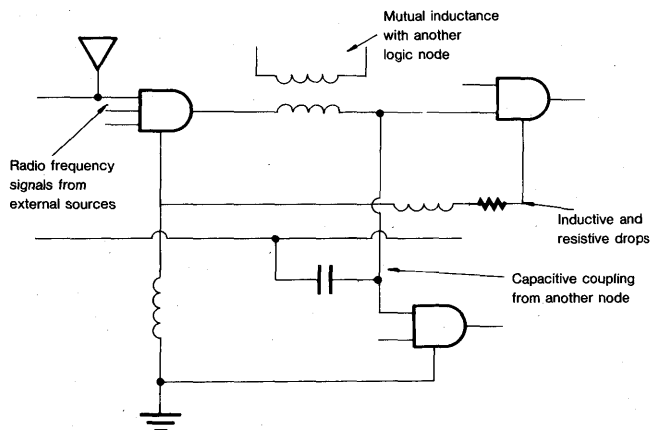


FIGURE 11. Sources of noise in digital systems.

Noise becomes a particularly critical issue in high-speed systems where fast voltage transitions accentuate these parasitic capacitances and inductances. Also, higher speeds allow the device to respond more quickly to noise transients. Therefore, special board layout and decoupling techniques have to be employed to confine noise to an "acceptable range". Obviously, the wider this range, the easier it is to design a clean system. This range is dictated by the input and output characteristics of the ICs in the system, as illustrated in Figure 12, and is measured in terms of "noise margins".



# TECHNICAL OVERVIEW

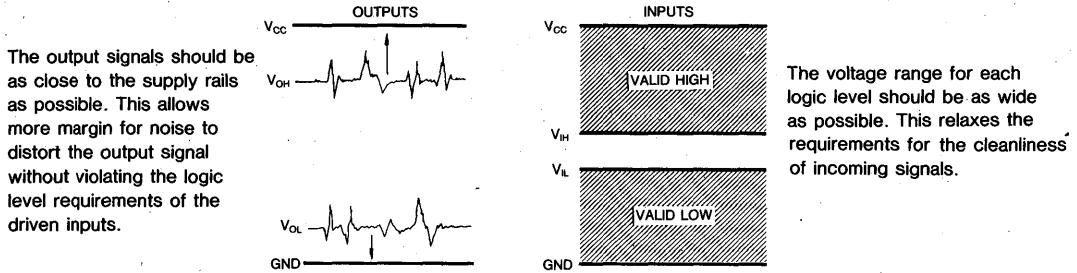


FIGURE 12. Requirements for good noise immunity.

Noise margins specify the maximum amplitude noise pulse that will not change the state of a driven stage, assuming the driving stage presents a worst-case logic level to the driven stage. Specifically, the high-level and the low-level noise margins ( $NM_H$  and  $NM_L$ ) are defined as:

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

where the voltage values are the guaranteed worst-case extremes for each case. Figure 13 shows the noise margins for several different interfaces.

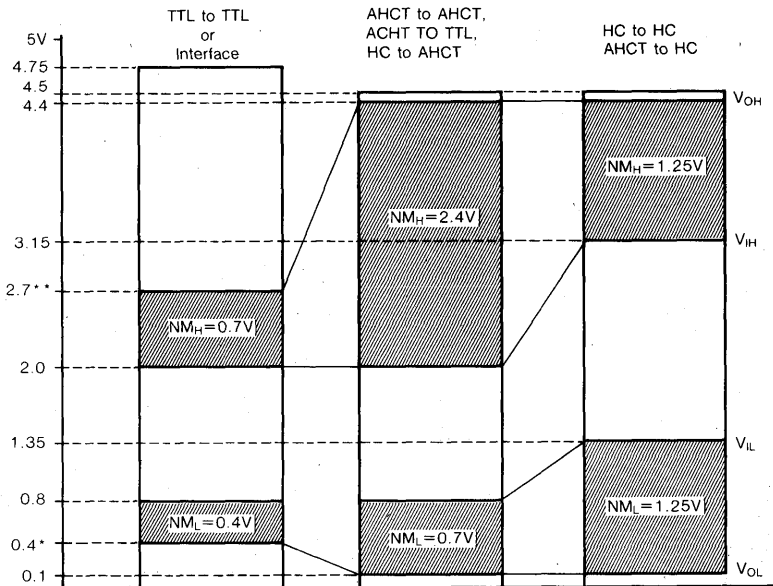


FIGURE 13. Noise margins for various interfaces. Noise margins for HCTLS are the same as those for AHCT.

\* When an AHCT output drives TTL loads the  $V_{OH}$  level will be dependent on how many loads are driven. For example if an AHCT244 drives 60LS loads, the  $V_{OH}$  will rise to 0.4V

\*\* For some, TTL parts,  $V_{OH}$  is 2.4V, instead of 2.7V

## TECHNICAL OVERVIEW

It is immediately obvious that the TTL-to-TTL interfaces have the poorest noise immunity and those driven by CMOS have the best. This is due to the rail-to-rail voltage swings of CMOS outputs.

Note the HC logic has almost symmetrical noise margins while AHCT (or HCTLS) has a very large noise margin for high level and a smaller low-level one. This is due to the fact that AHCT (or HCTLS) inputs are designed for direct interface with TTL and NMOS outputs as well as other CMOS. Notice, however, that the low-level noise margin ( $NM_L$ ) for AHCT is only 0.1V less than that for HC, which means that it provides nearly as much immunity to ground noise. In addition, since AHCT drive capability is two to four times better than HC, it is less susceptible to noise currents coupled to its outputs. That is, lower stray voltages are induced for a given amount of current coupling than for HC.

## ESD PROTECTION

Historically, MOS devices have always been considered to be more susceptible to damages due to electrostatic discharges (ESD), which can occur during handling and assembly procedures. However, the new protection circuitry, design, and special processing used for AHCT and HCTLS have improved the ESD immunity for these devices where it is now much better than that of bipolar logic.

Figure 6 and 8 show the input and output ESD protection circuitry employed. All AHCT and HCTLS pins are protected to ESD levels typically greater than  $\pm 2kV$ , the tests are conducted using the "human-body" model that is shown in Figure 14.

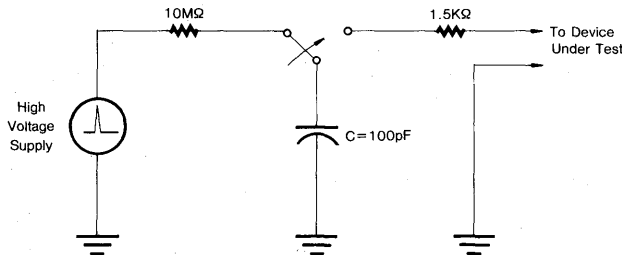


FIGURE 14. Test circuit used to measure ESD damage in AHCT and HCTLS circuits.

3

## LATCHUP CHARACTERISTICS

SCR latchup is an undesirable parasitic phenomenon which is inherent in circuits fabricated using bulk CMOS technology. A parasitic four-layer (P-N-P-N) SCR structure that appears between  $V_{CC}$  and ground can be triggered when voltages greater than  $V_{CC}$  or less than ground are applied to inputs or outputs. When this happens,  $V_{CC}$  gets effectively shorted to ground, and the only way to get the device off the latchup mode is to shut off the power supply. If large currents are allowed to flow through the chip, it may be destroyed. Samsung CMOS logic parts have been designed and processed to virtually eliminate this possibility in real-life situations where voltages out of the supply range many appear at the input or output pins (overshoots, undershoots, power-up & power-down situations).

# TECHNICAL OVERVIEW

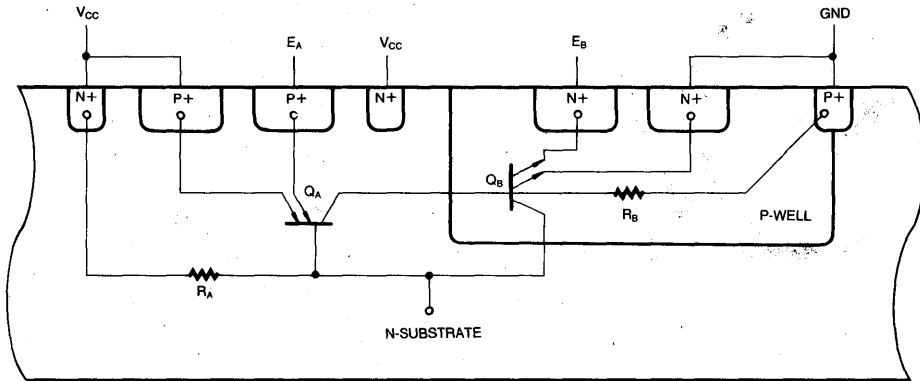


FIGURE 15. Simplified cross section of a CMOS inverter

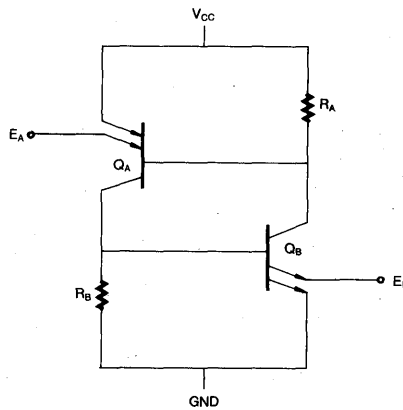


FIGURE 16. CMOS SCR structure

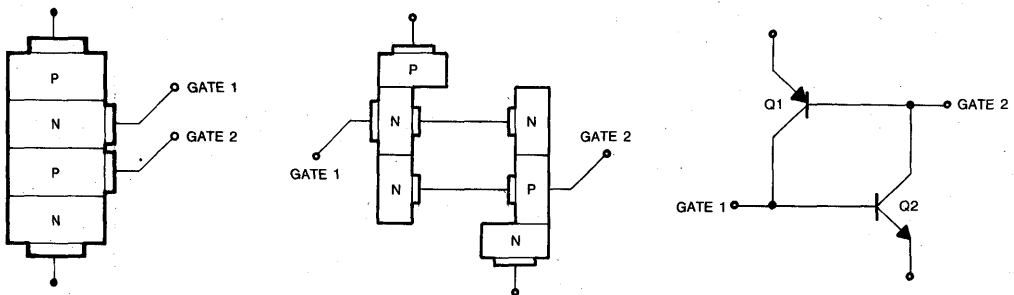


FIGURE 17. Simplified four layer SCR structure

## TECHNICAL OVERVIEW

The parasitic SCR structure in a CMOS inverter cross section is illustrated in *Figure 15*, where vertical and lateral NPN and PNP transistors are formed back-to-back by the N and P diffusions.  $R_A$  and  $R_B$  are the P-well and the N-substrate power supply connections. *Figure 16* is a schematic representation of this parasitic structure that looks like a cross-coupled transistor model of an SCR (*Figure 17*). The exceptions are the  $R_A$  and  $R_B$  resistors and the fact that the real SCR is triggered at the gates, while the CMOS parasitic SCR is triggered at its emitters. This happens when either the  $E_A$  is raised above  $V_{CC}$  enough to turn on  $Q_A$ , or  $E_B$  is lowered below ground enough to turn on  $Q_B$ . When  $E_A$  is brought above  $V_{CC}$ , current is injected from the emitter of  $Q_A$  and is swept to its collector. This current, in turn, will increase the voltage at the  $Q_B$  gate and once it is above 0.7V,  $Q_B$  will turn on and feed current from its collector back into  $R_A$  and into  $Q_A$ . When 0.7V drop appears across  $R_A$ ,  $Q_A$  will turn on even more.

If the two transistors have enough gain and enough current is provided by the supply to sustain the SCR, it will turn on and remain on even after  $E_A$  and  $E_B$  are returned to the rail voltages. Notice that low resistor values effectively reduce the gain of the transistors by stealing current away from their bases. Therefore, transistors should actually have much higher gains in order to have an overall SCR loop gain greater than one and enable SCR to trigger.

Samsung CMOS logic parts are designed and processed to have very low  $R_A$ ,  $R_B$  values and low gains for the parasitic transistors. In addition, large diodes exist between each signal pin and the supply rails to shunt out voltages above  $V_{CC}$  and below ground. In fact, traditionally, one refers to the current that flows through these diodes as the element that triggers latchup, i.e. we talk of "latchup trigger currents", not voltages.

Measured on a static basis, i.e. by applying DC voltages above  $V_{CC}$  and below ground, Samsung parts can withstand currents typically well above 200mA-even under the worst-case conditions of 7V  $V_{CC}$  and +125°C operation. *Figure 18* illustrates the test set-up used for static latchup tests.

A common occurrence of voltages above  $V_{CC}$  and below ground in systems is overshoots and undershoots that are caused by signal line ringing and power supply transients. In this case, unlike the static operation, only short pulses cause forward-bias diode currents and hence possible latch-up. It turns out, fortunately, that the parasitic SCR has extremely slow response time to transients, i.e. very poor frequency characteristics. *Figure 19* shows the increased peak currents required to latch an AHCT or HCTLS device up when the pulse width is decreased. For pulse widths in the range of several tens of nanoseconds, it is virtually impossible to latch the device up.

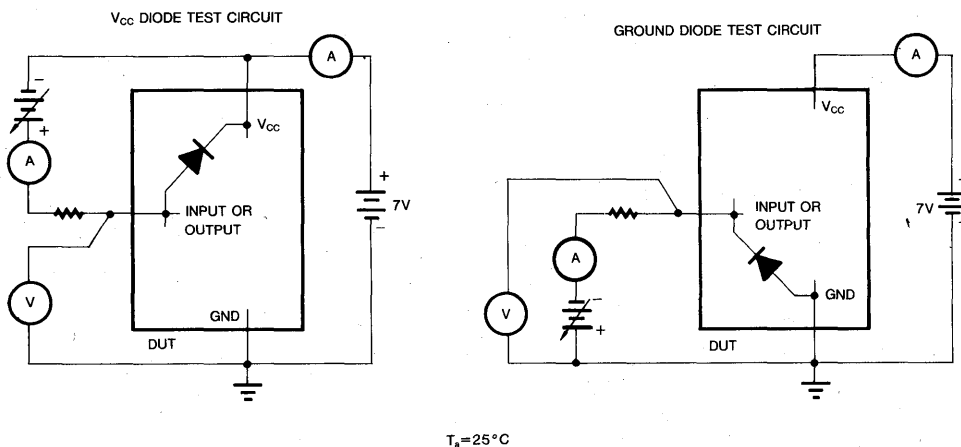


FIGURE 18. Test setup for measuring DC latch-up

# TECHNICAL OVERVIEW

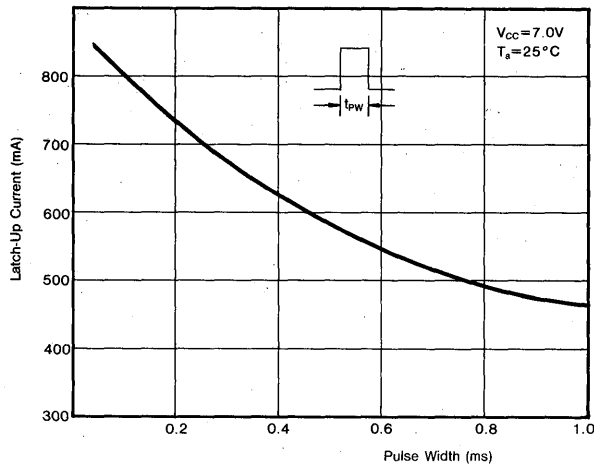


FIGURE 19. Pulsed latch-up characteristics

## POWER DISSIPATION

Low power dissipation is by far the most important advantage of CMOS over any other technology. Particularly in the quiescent state, the AHCT and HCTLS circuits consume up to seven orders of magnitude less power than the equivalent TTL functions. This makes them ideal for battery-operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

The dynamic power dissipation, however, depends on:

1. Cross-over currents of the internal CMOS transistors,
2. Internal load capacitances,
3. External load capacitances, and
4. Input voltage levels.

All of the above add up every time there is a logic transition and dynamic power dissipation is the sum of these contributions averaged at a given operating frequency. A practical formula is developed to calculate the dynamic power dissipation ( $P_D$ ) resulting from the first three items: (input voltage transitions are rail-to-rail)

$$P_D = (C_L + C_{PD}) V_{CC}^2 f,$$

where  $C_L$  is the load capacitance;  $C_{PD}$  is the "internal power dissipation capacitance",  $V_{CC}$  is the supply voltage and  $f$  is the operating frequency. The  $C_{PD}$  value, as specified in each data sheet, sums up the contributions of the first two factors (crossover currents and internal load capacitances) as a capacitance value for purposes of this calculation. The equation indicates that the dynamic power dissipation is directly proportional to frequency.

The contribution of the fourth factor listed above, the input voltage levels, can also be significant when AHCT or HCTLS inputs are driven by TTL outputs. Figure 20 shows the typical crossover currents generated at the input inverter stage as the input voltage swings from 0 to  $V_{CC}$ . This is because both the n-channel and the p-channel transistors turn on partially and provide a low-resistance current path between  $V_{CC}$  and ground when the input voltage is near the threshold voltage of the complementary pair. At 2.7V, which is the worst case  $V_{OH}$  for TTL parts, the  $I_{CC}$  can be as high as 0.5mA per input. This has to be taken into account when calculating the worst-case power dissipation of an AHCT or HCTLS part operating in a TTL environment.

# TECHNICAL OVERVIEW

Figure 21 shows the internal power dissipation for an AHCT244 (same for HCTLS244) and compares it with the dynamic power dissipation for LS, ALS and F244. It can be seen that the curves for the bipolar parts are essentially flat for frequencies up to 1 MHz where the quiescent currents mask out the dynamic effects. However, as the frequency goes up, the currents that charge the internal capacitances start adding to the quiescent currents and increase the overall power dissipation. The AHCT244 driven by worst-case TTL voltage levels (all inputs, 50% duty cycle) displays a similar trend but still dissipates an order of magnitude less power than the lowest-power TTL. When CMOS input voltage levels are used, however, the power dissipation is directly proportional to frequency as predicted by the above mentioned formula, and is less than those for the TTL parts, Although the power dissipation becomes comparable to ALS levels at around 10MHz, a crossover does not happen below 50MHz, which is already beyond the maximum clock frequencies of most systems. This behaviour is pretty much the same for all parts in the AHCT and HCTLS families.

In calculating the power dissipation of a system, however, note that only a small percentage of the devices operate at the maximum clock frequency while others operate at a fraction of that. Therefore the average operating frequency tends to be much lower where CMOS has a clear advantage.

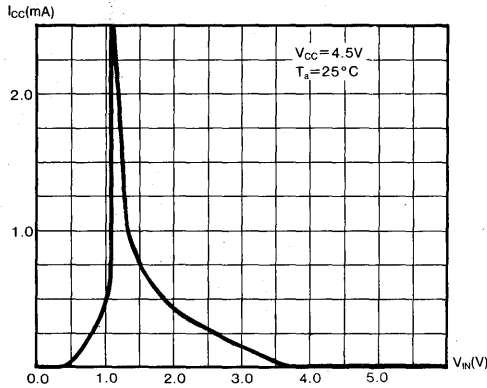


FIGURE 20. Typical crossover current of an AHCT or HCTLS input.

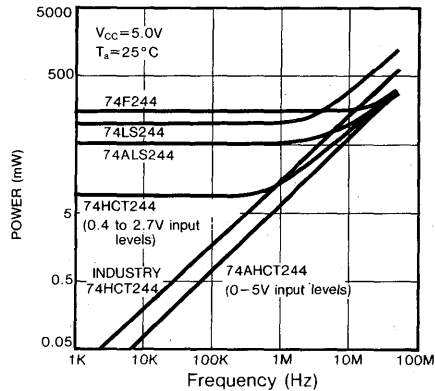


FIGURE 21. Typical dynamic power consumption (no-load) of the 74XXX240 octal buffer with all inputs toggling.

3

# TECHNICAL OVERVIEW

## AC CHARACTERISTICS

All AHCT and HCTLS parts are designed to meet or exceed the ALS and LS propagation delay specifications, respectively. Coupled with the equivalent drive capability, this makes them ideal replacements for the ALS and LS in existing designs. In addition the AC specifications for AHCT and HCTLS parts are improved to reflect more realistic design situations. First of all, unlike LS, the AHCT & HCTLS propagation delays are specified with a 50pF load for all part types and guaranteed over the entire voltage and temperature ranges ( $5V \pm 10\%$ ,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ). Standard LS propagation delays are specified with a 15pF load and guaranteed only at room temperature and 5V  $V_{CC}$ . In addition, all bus drivers specify the propagation delays with a 150pF load capacitance to enable the designer to predict a worst-case maximum speed degradation due to capacitive loading.

The effect of the supply voltage variations on propagation delay is illustrated in Figure 22 for a bus-driver (AHCT244). It can be seen that the parts are functional over a very wide range of voltages and that they slow down as  $V_{CC}$  goes down. However, propagation delays are specified and guaranteed only over the 4.5 to 5.5V range.

Figure 23 shows the effect of temperature on the propagation delays for the same part. As for all CMOS circuits, AHCT and HCTLS parts slow down as temperature goes up. Typically speeds derate linearly from  $25^\circ\text{C}$  at about  $0.02 \text{ ns}/^\circ\text{C}$ . The propagation delay at any temperature (between  $-55^\circ\text{C}$  and  $+125^\circ\text{C}$ ) can therefore be calculated using the following formula:

$$t_{PD}(T) = t_{PD}(25^\circ\text{C}) + k_T(T - 25^\circ\text{C})$$

where:

$t_{PD}(T)$  = Propagation delay at the desired T temperature,

$t_{PD}(25^\circ\text{C})$  = Propagation delay at  $25^\circ\text{C}$ ,

$k_T$  = Temperature derating factor =  $0.02 \text{ ns}/^\circ\text{C}$

The effect of capacitive loading of the outputs on the propagation delay is illustrated in Figure 24: the higher the load capacitance, the slower the propagation delay gets. To determine the maximum limit for propagation delay at any value of capacitive loading up to 500pF, the following equation is used:

$$t_{PD}(C_L) = t_{PD}(50\text{pF}) + k_C(C_L - 50\text{pF})$$

where:

$t_{PD}(C_L)$  = Maximum propagation delay at the desired  $C_L$ ,

$t_{PD}(50\text{pF})$  = Maximum propagation delay from device data sheet,

$k_C$  = Maximum multiplicative factor (ns/pF):

- 0.04 for standard outputs, and
- 0.02 for bus-drivers.

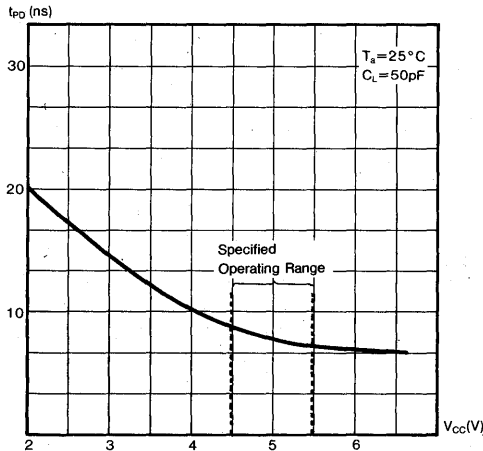


FIGURE 22. Propagation delay versus supply voltage for an AHCT244.

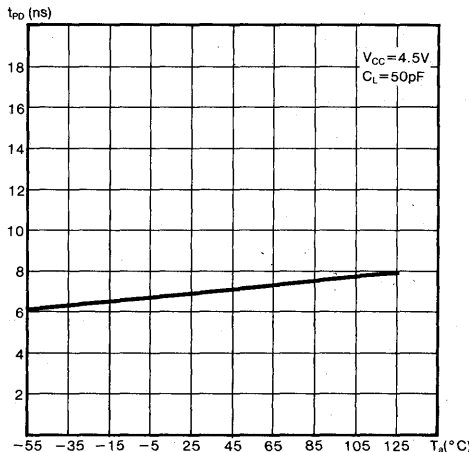


FIGURE 23. Propagation delay versus ambient temperature for an AHCT244.

# TECHNICAL OVERVIEW

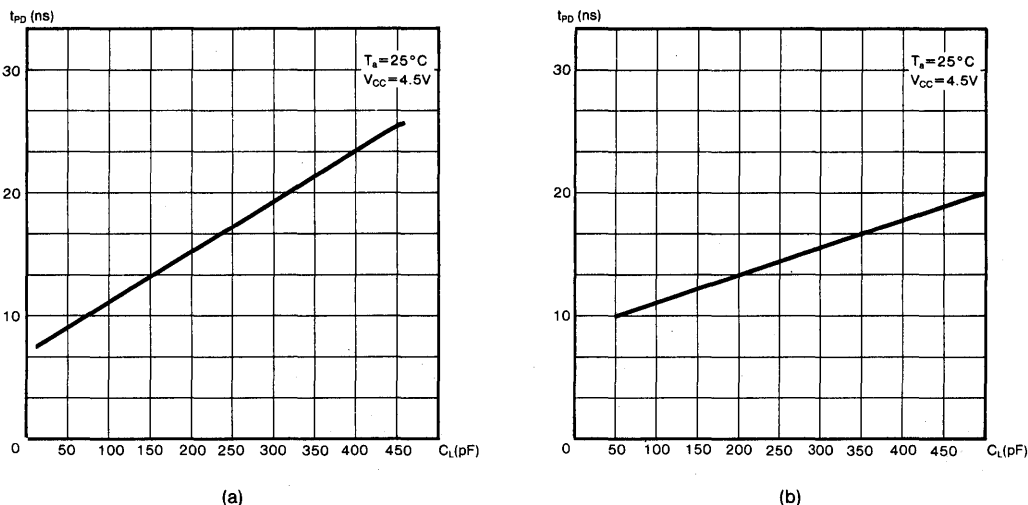


FIGURE 24. Propagation delay versus capacitive load for a (a) standard output (HCTLS00), (b) bus-driver output (HCTLS374)

3

## INTERFACING 54/74AHCT AND 54/74HCTLS WITH OTHER LOGIC FAMILIES AND LOADS

Speed and power, while paramount in the initial choice of a logic family, are not the only basis of decision. Another very important factor is the interface flexibility: the inherent capacity of a family to interface with other types of logic and to drive various loads. The Samsung CMOS logic families have this very attractive feature that they can easily be interfaced to all other kinds of digital logic with minimal or no external components.

AHCT and HCTLS parts can be coupled directly with all other TTL, NMOS and CMOS parts if they operate from the same supply voltage. The list includes Standard TTL, Schottky(S), Low-Power Schottky(LS), Advanced Low-Power Schottky(ALS), Advanced Schottky (AS and FAST); all industry-standard CMOS logic families (HC, HCT, CD4000, 14000); all bipolar, NMOS and CMOS microprocessors, microcontrollers, peripherals and memory circuits (see figure 25). This is due to the TTL-compatible input voltage levels coupled with CMOS (rail-to-rail) output voltage swings.

Interface with ECL logic, however, requires external components as shown in Figure 26.

Methods of interfacing with standard CMOS logic families (4000 and 14000), when supply voltages are different, are illustrated in Figure 27 and 28.

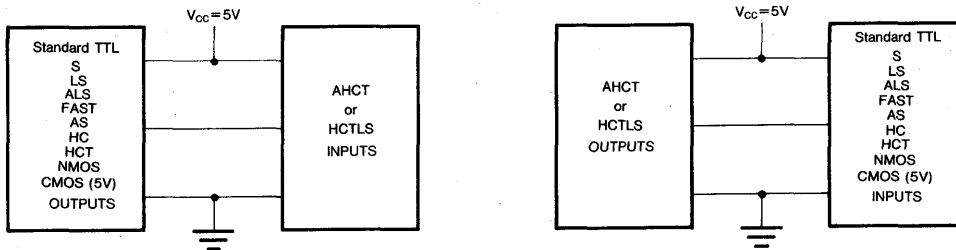


FIGURE 25. Interfacing with TTL, NMOS and other CMOS logic. No extra components are needed.



# TECHNICAL OVERVIEW

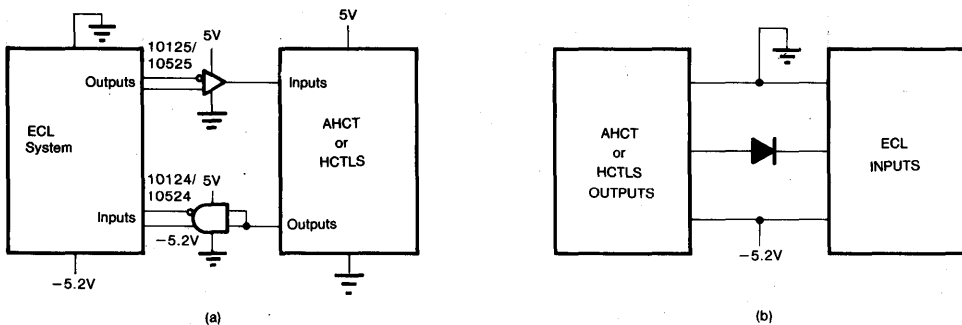


FIGURE 26. (a) General ECL interface

(b) Driving ECL from same power supply.

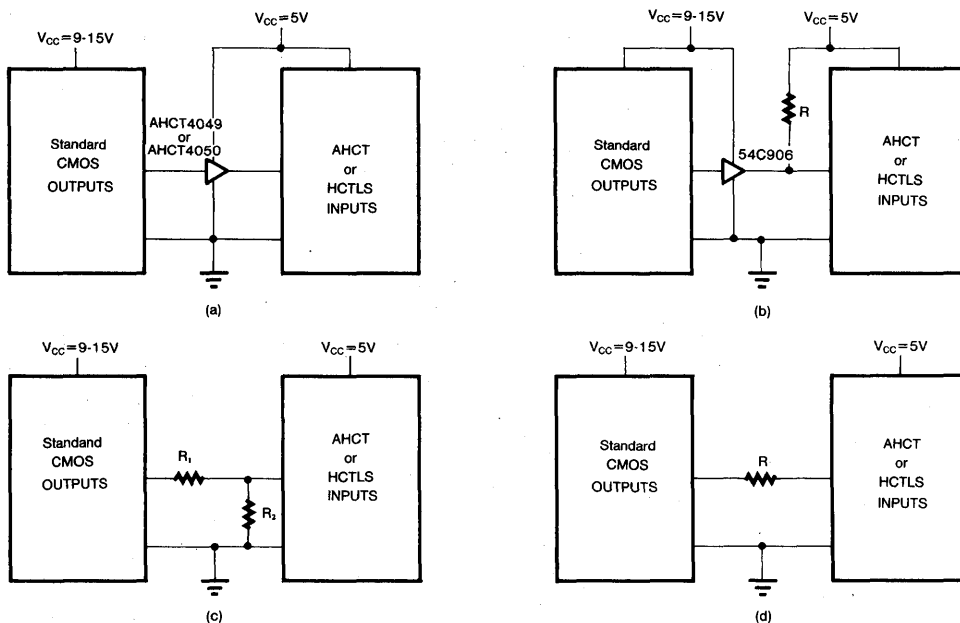


FIGURE 27. Methods of interfacing standard CMOS (4000 and 14000 series) outputs with AHCT and HCTLS inputs when supply voltages are different.

- (a) Using logic down converters,
- (b) Using Open-drain CMOS
- (b) Using resistor divider ( $V_{OH} \cdot R_2 / (R_1 + R_2) \leq 5V$ )
- (d) Using series resistor

# TECHNICAL OVERVIEW

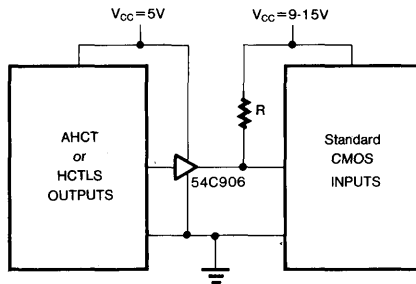


FIGURE 28. Interfacing AHCT and HCTLS outputs with standard CMOS (4000 and 14000) using an open-drain CMOS circuit.

## High Voltage and Industrial Control Interfaces

Interfacing with high voltage industrial control circuitry where 4000 or 14000-type of CMOS logic is used has been described in Figure 27 and 28. In rugged industrial and automotive environments, more care may be required to prevent large transients from harming AHCT and HCTLS logic. Figure 29 shows a typical connection that utilizes external diode clamps for input and output protection. The values of  $R_1$  and  $R_2$  depend on the output voltage of the driving circuit and  $C$  depends on the noise level and speed. The values of  $R_3$  and  $R_4$  depend on supply voltage and transistor type.

## Driving Relays

The high-drive of AHCT and HCTLS outputs enable direct interface with relays, but additional isolation is recommended. Clamp diodes can be used to prevent spikes generated by the relay from harming the circuit. For higher current drive, an external transistor may be employed (Figures 30 (a) and (b)). Alternatively, multiple gates may be connected in parallel to increase the current sinking and sourcing capability.

## Driving LED's

Any AHCT or HCTLS output can be used to drive light-emitting diodes (LED's) directly. Figure 31 shows two methods of doing this. The resistor performs the function of current limiter. The luminous intensity of the LED depends on the amount of forward current.

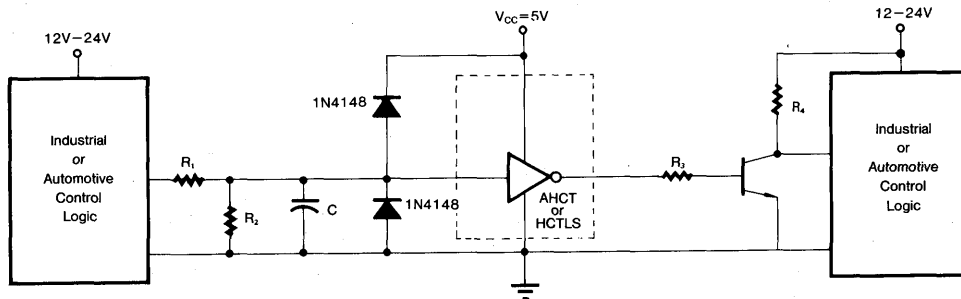


FIGURE 29. Interfacing between AHCT/HCTLS logic and high-voltage industrial and automotive circuitry in rugged environments.

# TECHNICAL OVERVIEW

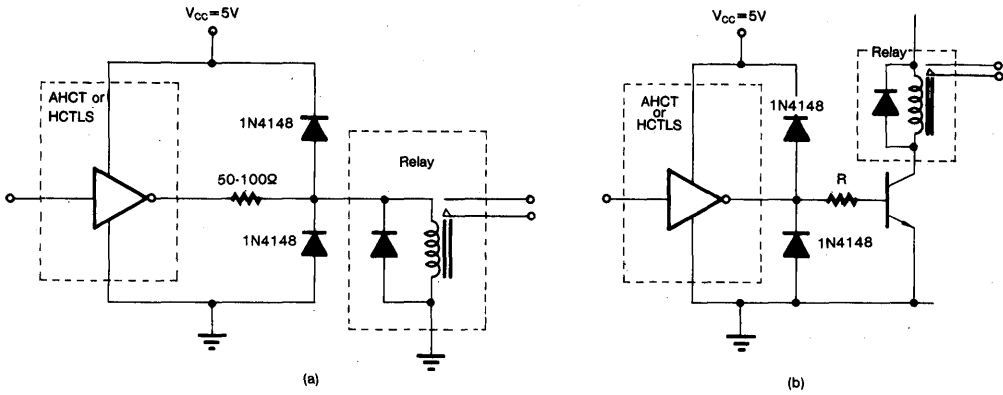


FIGURE 30. Methods of driving relays. (a) Direct and (b) Through a transistor for higher drive ( $R = (V_{CC} - 0.7) / (I_C / \beta)$ ).

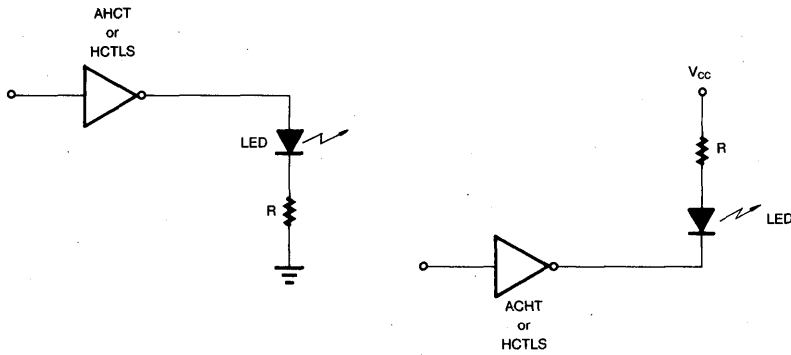


FIGURE 31. Methods of driving LED's

# TECHNICAL OVERVIEW

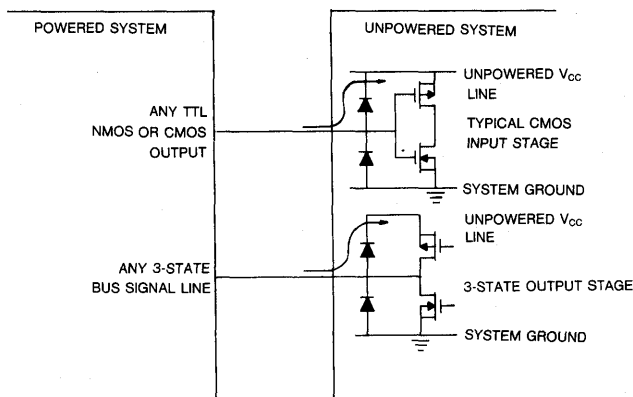
## Design Tips

Although the AHCT and HCTLS families are functionally equivalent to the ALS and LS families, some conditions have to be satisfied in order to be able to simply replace them in existing designs. The AHCT and HCTLS families essentially integrate TTL and CMOS characteristics into one family. Therefore, in general, the do's and don'ts of both families apply to the AHCT and HCTLS.

- Don't leave any AHCT or HCTLS input floating. This is frequency overlooked problem with bipolar devices although it is discouraged by every bipolar manufacturer. CMOS inputs have extremely high input impedance and if left unterminated, can pick up noise that causes excursions through the threshold. The result is random switching of the device and high power consumption which can be excessive, especially if the inputs stay very close to the device threshold. Prolonged exposure to these conditions can damage the device. The thing to do is to simply tie the unused inputs to  $V_{CC}$  or ground (or they can be tied to nearest operational pin although this may cause more power consumption).

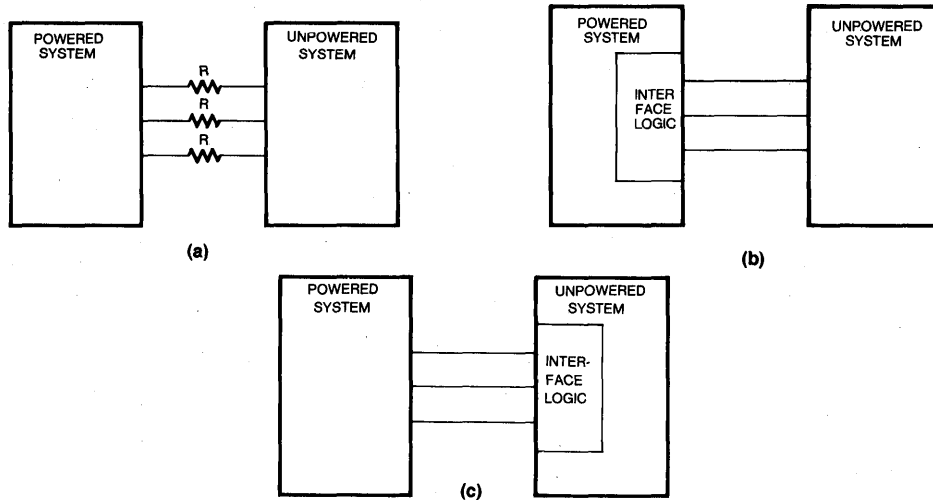
- Don't power up inputs before both  $V_{CC}$  and ground are connected, and don't plug boards into or out of powered connectors unless input currents are limited to the absolute maximum ratings specified for the device, and are short-lived. Both conditions can forward bias the input and output ESD protection diodes, resulting in excessive diode currents (see *Figure 32*). If these conditions cannot be avoided, one of the following methods should be used to prevent damage to the AHCT/HCTLS circuits:

- Use connectors that apply power before signals.
- Add series resistors at each input to limit currents to the absolute maximum ratings (*Figure 33a*).
- Add logic to board interfaces that forces all outputs to either ground or high-impedance state when they are connected to unpowered devices (*Figure 33b*).
- Add logic to board inputs to prevent direct interface with unpowered HCTLS inputs (*Figure 33c*). Circuits designed for this purpose are 74AHCT4049 (Hex Inverting Logic Level Down Converter) and 74AHCT4050 (Hex Logic Level Down Converter). These parts have a modified input protection structure that enables them to be used as logic level translators which convert high-level logic to low-level logic while operating from the low logic supply. In this case, since the low logic supply is zero (unpowered), the outputs of the 4049 and 4050 will always be zero regardless of the inputs.



**FIGURE 32. Direct interface to unpowered CMOS ICs presents a dangerous situation where high-level signals forward-bias input and output protection diodes and try to “power-up” the  $V_{CC}$  line. Excessive currents at such an interface can cause damage to the circuitry.**

## TECHNICAL OVERVIEW



**FIGURE 33. Methods of protection in power-down situations: (a) Use of series resistors to limit input currents to absolute maximum ratings, (b) Interface logic circuitry that forces all outputs to either ground or high-impedance state, (c) Interface circuitry at board inputs that acts as buffer between powered and unpowered devices; ideal components for this purpose are the 74AHCT4049 and 74AHCT 4050 Hex Logic Level Down Converters that lack the  $V_{CC}$  diode in their protection circuitry.**

- In bus-oriented systems, don't allow the bus to stay in high-impedance state for extended periods of time if it is not terminated, because this will have the same effect as leaving inputs open. Two simple ways of terminating the bus are illustrated in Figure 34. Most microprocessor-based systems, however, do not keep the bus in 3-state for long periods, in which case, the bus capacitance can maintain valid logic levels. In these cases, pull-up or pull-down circuitry may not be necessary.

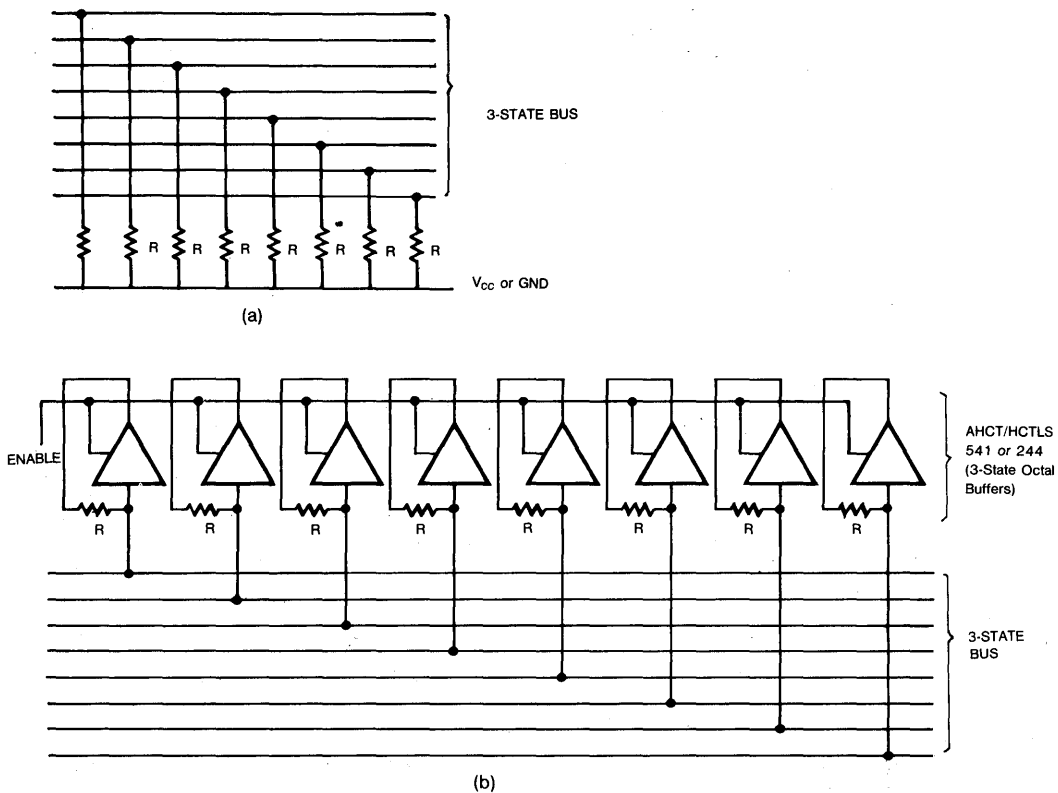
- The edge-rates of the AHCT and HCTLS part are similar to the very high-speed TTL parts. Therefore, system grounding and supply-decoupling techniques normally employed in high-speed TTL designs should be duplicated in AHCT/HCTLS designs to ensure proper operation. A good rule of thumb to reduce the affects of PC board trace inductance is to place 0.01 to 0.1  $\mu\text{F}$  RF-grade capacitors every two-to-five ICs (octal flip-flops and buffers may require more decoupling). This, of course, has to be accompanied by careful pc board layout to minimize these inductances.

- The testing problems encountered in ALS, LS and FAST apply also to AHCT and HCTLS. Most of these problems result from the noise produced by the interactions of the device being tested and the test system. Typical test fixtures have lead inductances several times that of a PC board socket. This inductance, especially in the device ground path is the source of these problems.

The outputs, for example, can cause transient currents in the 50 to 200 mA range within a couple of nanoseconds while changing state. These appear as changes in the voltage drop across the device ground lead. The test system's input and output reference voltages are set with respect to tester ground and are not affected by these transients. Consequently the effective input voltages to the device will vary. If the ground pin goes up 1 volt, all the inputs effectively go down 1 volt. This must be considered in selecting input and output voltage levels. In functional tests, for example, solid input logic levels should be applied, instead of 0.8 and 2.0 volts.

Furthermore, if TTL test programs are to be used, one must be particularly careful not to apply voltages to inputs and outputs that are below ground or above  $V_{CC}$  in excess of the absolute maximum limits specified in the data sheets.

# TECHNICAL OVERVIEW



**FIGURE 34. Methods of terminating 3-state buses; (a) Pullup or pulldown resistors (b) Use of 3-state buffers. The latter approach terminates the bus to the last active logic level and dissipates no static power.**

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## NOTES

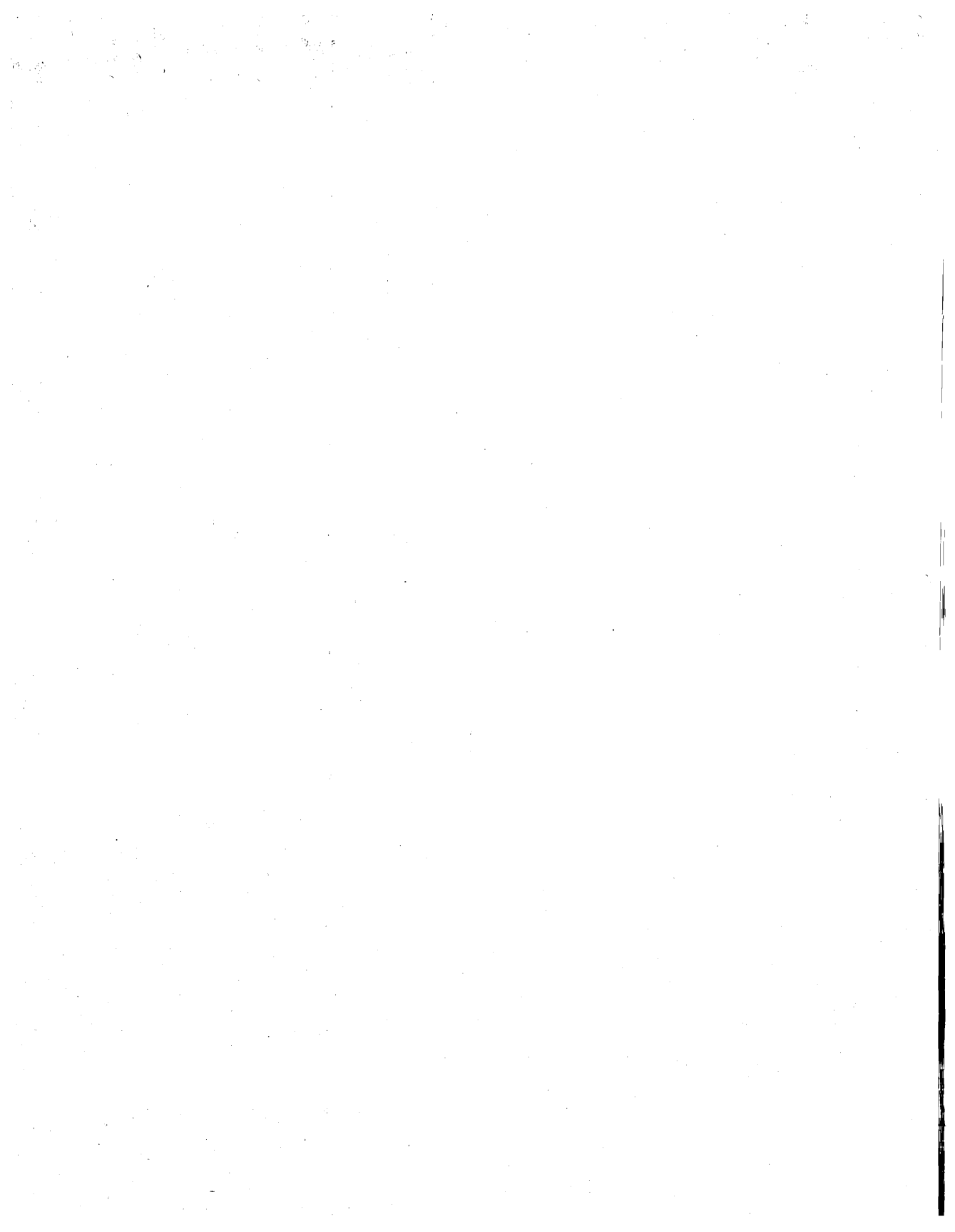
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# ***KS54/74AHCT DATA SHEETS 4***







**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

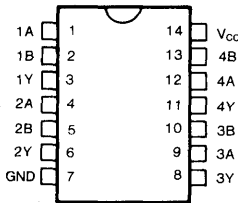
**DESCRIPTION**

These devices contain four independent 2-input NAND gates that perform the Boolean functions  $Y = \overline{A \cdot B}$  or  $Y = \overline{A + B}$

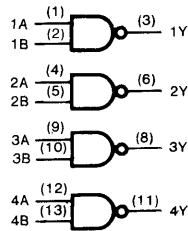
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84		$V_{CC}-0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0		40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT00

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0V$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	7		11		14	ns	
	$t_{PHL}$		8		11		14		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f$

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include 'small outline' packages (Available Tape & Reel), standard DIPs.

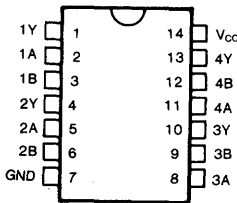
### DESCRIPTION

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

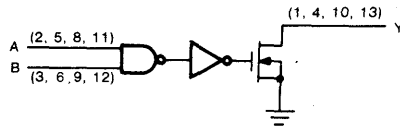
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAM



4

### FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0 0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT01

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$ $R_L=1k\Omega$	17		25		29	ns	
	$t_{PHL}$		10		16		19		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

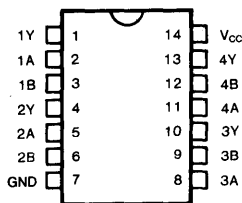
**DESCRIPTION**

These devices contain four independent 2-input NOR gates that perform the Boolean functions  $Y = \overline{A+B}$  or  $Y = \overline{A} \cdot \overline{B}$ .

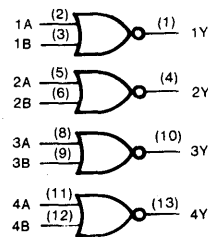
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	X	L
X	H	L
L	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$  .....  
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$  .....  
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$  .....  
 (-0.5V  $< V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0		$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0		mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT02

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	7		12		14	ns	
	$t_{PHL}$		7		12		14		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$

† For AC switching test circuits and timing waveforms see section 2

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

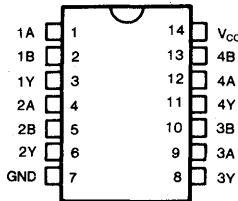
**DESCRIPTION**

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

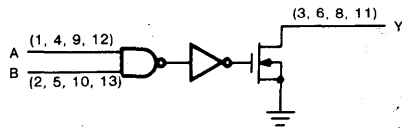
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**4**

**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_D$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0 0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns), AHCT03

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0V$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$ $R_L=1\text{k}\Omega$	17		25			29	ns
	$t_{PHL}$		10		16		19		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

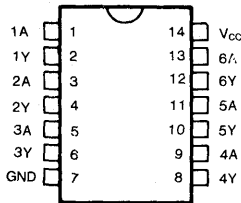
**DESCRIPTION**

These devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$ .

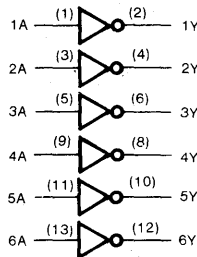
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**4**

**FUNCTION TABLE**

(Each Inverter)

Input	Output
A	Y
H	L
L	H

#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0		40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

#### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns, AHCT04)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	7		11		14	ns	
	$t_{PHL}$		7		11		14		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in} I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

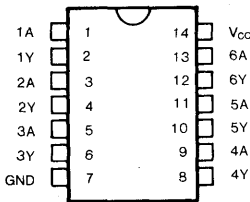
**DESCRIPTION**

These devices contain six independent inverters with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

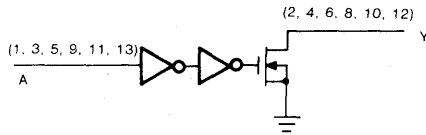
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**4**

**FUNCTION TABLE**

(Each Inverter)

Input	Output
A	Y
H	L
L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-1\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ..... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT		KS54AHCT		Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$ per input pin		2.0	20.0	40.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	$V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT05

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74AHCT		KS54AHCT		Unit
			$V_{CC}=5.0V$		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	17		25		29		ns
	$t_{PHL}$	$R_L=1k\Omega$	8		14		33		
Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$	(per inverter)	15						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$  cc  $V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

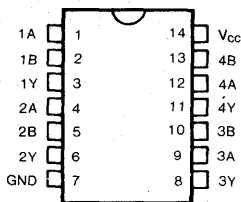
**DESCRIPTION**

These devices contain four independent 2-input AND gates. They perform the Boolean functions  $Y = A \cdot B$  or  $Y = \overline{A+B}$ .

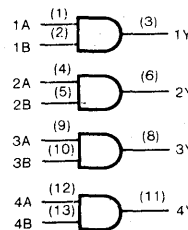
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	20.0	40.0	40.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	2.9	3.0	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT08

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
			Propagation Delay	$t_{PLH}$ $t_{PHL}$	$C_L = 50pF$	8		14	
Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

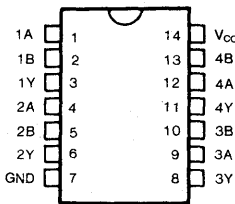
**DESCRIPTION**

These devices contain four independent 2-input AND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

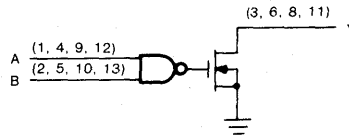
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**4**

**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $85^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0 0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT09

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			$V_{CC}=5.0V$	$V_{CC}=5.0V \pm 10\%$		$V_{CC}=5.0V \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	18		27		31	ns
	$t_{PHL}$	$R_L=1k\Omega$	9		15		18	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

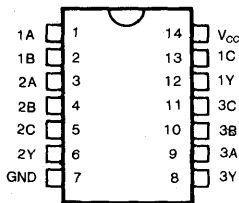
### DESCRIPTION

These devices contain three independent 3-input NAND gates. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{A + B + C}$ .

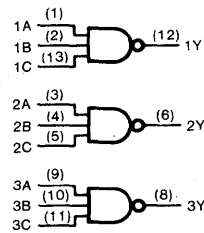
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$	2.0	20.0	40.0	$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$	2.7	2.9	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT10

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$	KS74AHCT		KS54AHCT		Unit
			$V_{CC}=5.0V$	$T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC}=5.0V \pm 10\%$		$T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC}=5.0V \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay	$t_{PLH}$	$C_L = 50pF$	9		15		18	ns
	$t_{PHL}$		9		15		18	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

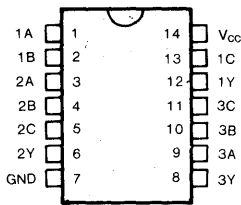
**DESCRIPTION**

These devices contain three independent 3-input AND gates. They perform the Boolean functions  $Y = A \cdot B \cdot C$  or  $Y = \overline{A+B+C}$ .

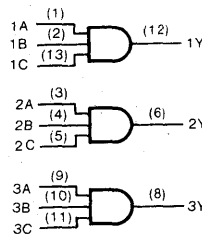
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ		Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT11

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ		Min	Max	Min	Max	
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$		9		15		18	ns
	$t_{PHL}$			9		15		18	
Input Capacitance	$C_{IN}$			5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)		15					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

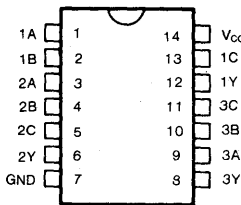
# KS54AHCT 12 KS74AHCT

## Triple 3-Input NAND Gates with Open-Drain Outputs

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### DESCRIPTION

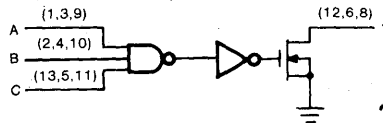
These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{A + B + C}$ .

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT12

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC}=5.0V$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L=50pF$	19		27		31	ns	
	$t_{PHL}$		11		18		22		
Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF		

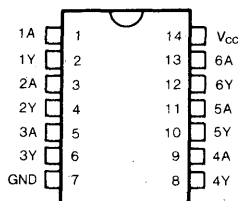
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

#### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

#### PIN CONFIGURATION



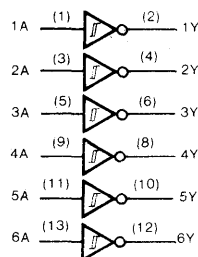
#### DESCRIPTION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$ .

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAM



#### FUNCTION TABLE

(Each Inverter)

Input	Output
A	Y
H	L
L	H



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$				Unit
			KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
			Typ	Guaranteed Limits			
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.11$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**DC ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Min	Max	Min	Max	Min	Max	
			Positive-Going Threshold Voltage	$V_{T+}$	$V_{CC}=4.5V$ $V_{CC}=5.5V$	1.2 1.4	1.9 2.1	1.2 1.4	
Negative-Going Threshold Voltage	$V_{T-}$	$V_{CC}=4.5V$ $V_{CC}=5.5V$	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V
Hysteresis ( $V_{T+}-V_{T-}$ )	$V_H$	$V_{CC}=4.5V$ $V_{CC}=5.5V$	0.4 0.4	1.4 1.5	0.4 0.4	1.4 1.5	0.4 0.4	1.4 1.5	V

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT14)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	8		14		17	ns
	$t_{PHL}$		8		15		19	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF

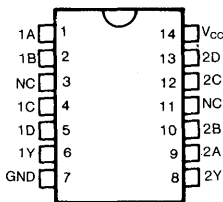
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



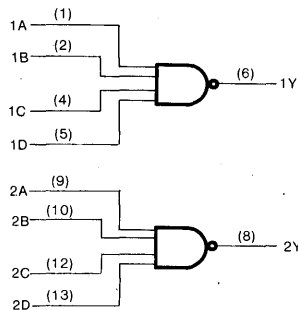
**DESCRIPTION**

These devices contain two independent 4-input NAND gates. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$  in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

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### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns, AHCT20)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			$V_{CC}=5.0V$	$V_{CC}=5.0V \pm 10\%$		$V_{CC}=5.0V \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	$t_{PLH}$	$C_L=50\text{pF}$	7		11		13	ns
	$t_{PHL}$		7		11		13	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF

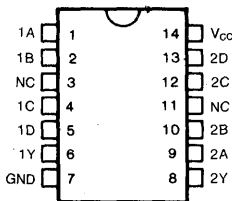
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

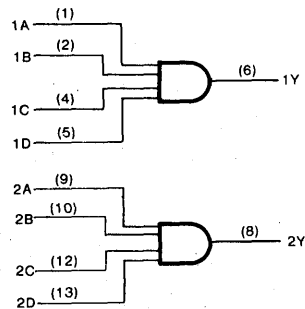
### DESCRIPTION

These devices contain two independent 4-input AND gates. They perform the Boolean functions  $Y = A \cdot B \cdot C \cdot D$  or  $Y = \overline{A + B + C + D}$  in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns), AHCT21

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			$V_{CC}=5.0V$	$V_{CC}=5.0V \pm 10\%$		$V_{CC}=5.0V \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	$t_{PLH}$	$C_L=50\text{pF}$	8		14		17	ns
	$t_{PHL}$		8		14		17	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

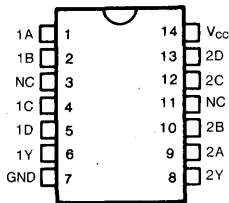
**DESCRIPTION**

These devices contain two independent 4-input NAND gates. These gates perform the Boolean functions  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{A + B + C + D}$  in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

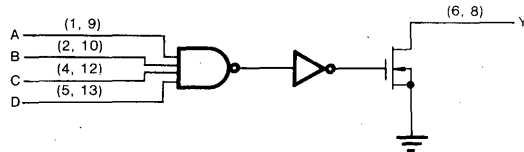
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0 0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA

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### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns, AHCT22)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay, Any input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	19		29			34	ns
	$t_{PHL}$	$R_L = 1k\Omega$	11		18			22	
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

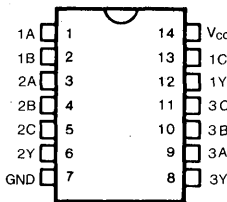
† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**PIN CONFIGURATION**



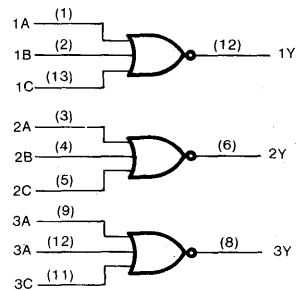
**DESCRIPTION**

These devices contain two independent 3-input NOR gates. They perform the Boolean functions  $Y = A + B + C$  or  $Y = \overline{A \cdot B \cdot C}$  in positive logic.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA	

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns), AHCT27

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			$V_{CC}=5.0V$		$V_{CC}=5.0V \pm 10\%$		$V_{CC}=5.0V \pm 10\%$		
			Typ	Min	Max	Min	Max		
Propagation Delay, Any input to Y	$t_{PLH}$	$C_L=50\text{pF}$	8		14		17		ns
	$t_{PHL}$		10		16		20		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**DESCRIPTION**

The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

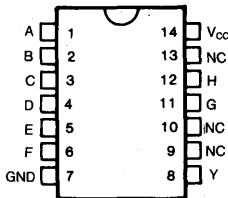
$$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$$

$$Y = \overline{A + B + C + D + E + F + G + H}$$

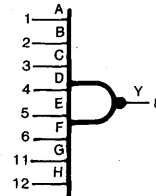
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs A Through H		Output Y
All Inputs	H	L
One or more inputs	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT30

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$				Unit		
			$V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$			KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	
			Typ	Min	Max	Min		Max	
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	6		11		ns		
	$t_{PHL}$		6		11				
Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$		15				pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

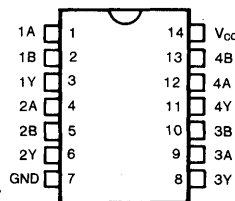
### DESCRIPTION

These devices contain four independent 2-input OR gates. They perform the Boolean functions  $Y=A+B$  or  $Y=\overline{A}\cdot\overline{B}$ .

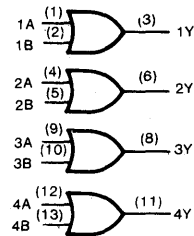
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Gate)

Inputs		Outputs
A	B	Y
H	X	H
X	H	H
L	L	L

### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 35$ mA
Continuous Current Through	
$V_{CC}$ or GND pins	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$	-65°C to +150°C
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	0V to $V_{CC}$
Operating Temperature	
Range	KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0		40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT32

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	8		14		17	ns	
	$t_{PHL}$		9		14		17		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

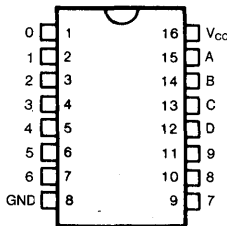
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Full decoding of Input Logic
- All outputs are High for Invalid BCD Conditions
- Also for application as 3-Line to 8-Line Decoders
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

No.	Inputs				Outputs										
	D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H

**DESCRIPTION**

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active low input enables.

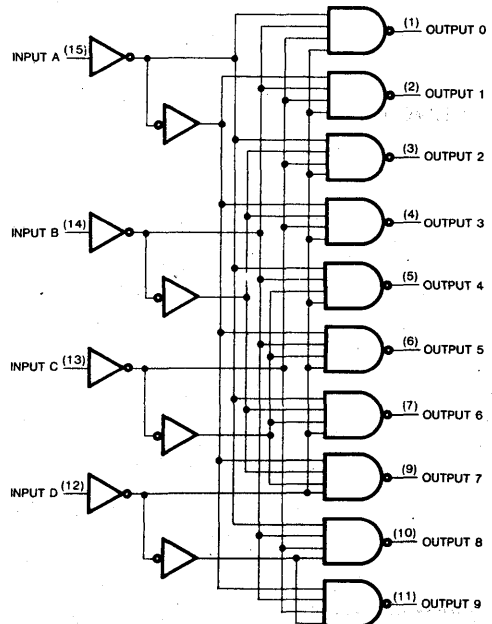
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0		160.0		$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9		3.0		mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns), AHCT42

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			$V_{CC}=5.0V$	$V_{CC}=5.0V \pm 10\%$		$V_{CC}=5.0V \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	$t_{PLH}$	$C_L = 50pF$	11		18		22	ns
	$t_{PHL}$		11		18		22	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

The '51 performs the following Boolean functions:

$$1Y = (\overline{1A} \cdot \overline{1B} \cdot 1C) + (1D \cdot 1E \cdot 1F)$$

$$2Y = (2A \cdot 2B) + (2C \cdot 2D)$$

The '58 performs:

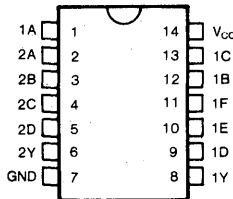
$$1Y = (\overline{1A} \cdot \overline{1B} \cdot 1C) + (1D \cdot 1E \cdot 1F)$$

$$2Y = (2A \cdot 2B) + (2C \cdot 2D)$$

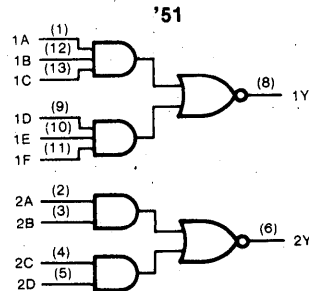
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



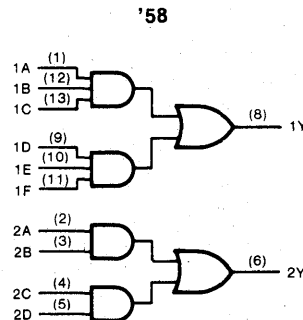
### LOGIC DIAGRAMS



### FUNCTION TABLES

Inputs						Output 1Y	
1A	1B	1C	1D	1E	1F	'51	'58
H	H	H	X	X	X	L	H
X	X	X	H	H	H	L	H
Any other combination						H	L

Inputs				Output 2Y	
2A	2B	2C	2D	'51	'58
H	H	X	X	L	H
X	X	H	H	L	H
Any other combination				H	L



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$	-65°C to +150°C
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	0V to $V_{CC}$
Operating Temperature Range	
KS74AHCT:	-40°C to +85°C
KS54AHCT:	-55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits	Min	Max	Min	Max	
Minimum High-Level Input Voltage	$V_{IH}$		2.0		2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8		0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0		40.0		$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9		3.0		mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT51, AHCT58

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L = 50pF$	9		15		18	ns	
	$t_{PHL}$		9		15		18		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

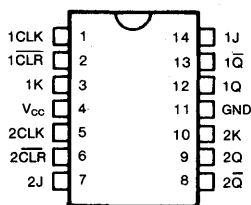
**DESCRIPTION**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

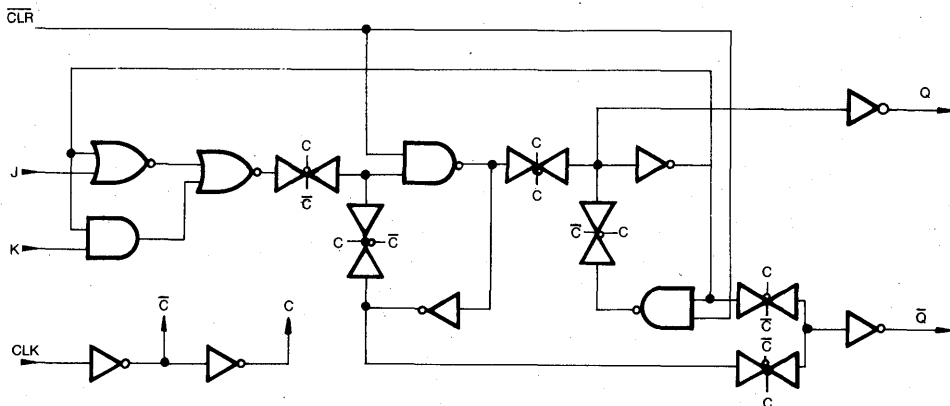
**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs				Outputs	
$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	X	X	X	L	H
H	↓	L	L	$Q_0$	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	$Q_0$	$\overline{Q}_0$

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND).

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
			Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT73

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min		Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	45	30		25	MHz		
Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns	
	$t_{PHL}$		10		17		20		
Propagation Delay, $\bar{CLR}$ to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns	
	$t_{PHL}$		10		17		20		
Setup Time before CLK↓	J or K		$t_{su}$	8	13		15	ns	
	$\bar{CLR}$ Inactive	8		13		15			
Hold Time, J or K after CLK↓	$t_h$		-3	0		0	ns		
Pulse Width	CLK High or Low	$t_w$	8	13		15	ns		
	$\bar{CLR}$ Low		8	13		15			
Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$	(per flip-flop)	40				pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

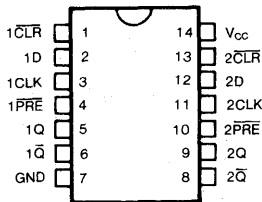
**DESCRIPTION**

These devices contain two independent positive-edge-triggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and  $\bar{Q}$  outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

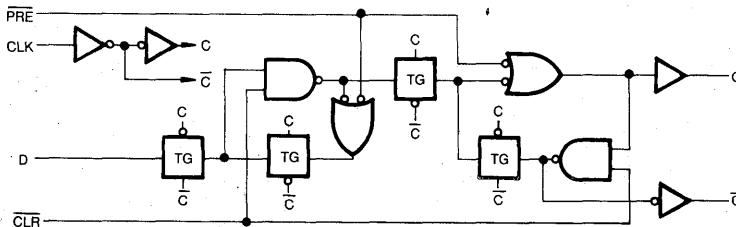


**FUNCTION TABLE**

Inputs				Outputs	
PRE	CLR	CLK	D	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	↓	X	No Change	No Change

\*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT74

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C	KS74AHCT		KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	V <sub>CC</sub> = 5.0V ± 10%		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	55	34		30		MHz
Propagation Delay, CLK to Q or $\bar{Q}$	t <sub>PLH</sub>		13		18		19	ns
	t <sub>PHL</sub>		13		18		19	ns
Propagation Delay, PRE or CLR to Q or $\bar{Q}$	t <sub>PLH</sub>		9		17		18	ns
	t <sub>PHL</sub>		9		17		18	ns
Setup Time before CLK†	Data		t <sub>su</sub>	7	12		15	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive			5	8		10	ns
Hold Time, Data after CLK†	t <sub>h</sub>			0	0		0	ns
Pulse Width	CLK High or Low	t <sub>w</sub>	9	14		17	ns	
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		9	15		17	ns	
Input Capacitance	C <sub>IN</sub>		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>		40				pF	

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.



### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

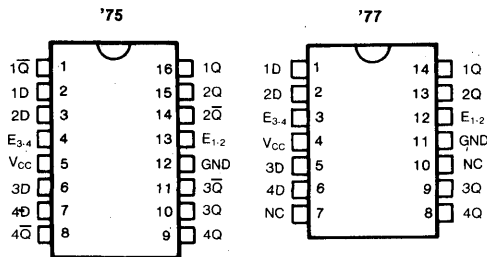
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and  $\bar{Q}$  output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

### PIN CONFIGURATION

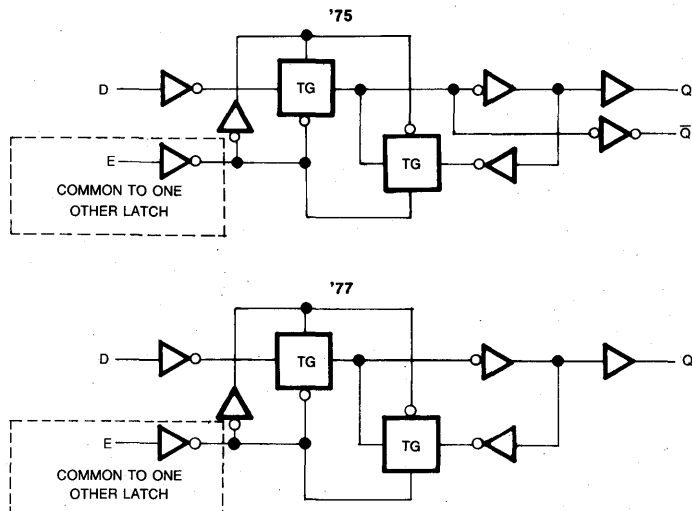


### FUNCTION TABLE

Inputs		Outputs	
D	E	Q	$\bar{Q}^*$
L	H	L	H
H	H	H	L
X	L	Q <sub>0</sub>	$\bar{Q}_0$

\* $\bar{Q}$ : '75 only

### LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_{d1}$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT75

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay E to Q or $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	10		16		20	ns
	$t_{PHL}$		10		16		20	
Propagation Delay D to Q or $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	10.5		15		18	ns
	$t_{PHL}$		9		15		18	
Data Set up Time D to Enable	$t_{SU}$		6	10		12		ns
Data Hold Time Enable to D	$t_h$		10	0		10		ns
Input Capacitance	$C_{IN}$		5					pF
Power dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT77

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay E to Q	$t_{PLH}$	$C_L = 50\text{pF}$	8		14		17	ns
	$t_{PHL}$		8		14		17	
Propagation Delay D to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	8		13		15	ns
	$t_{PHL}$		8		13		15	
Data Set up Time D to Enable	$t_{SU}$		6	10		12		ns
Data Hold Time Enable to D	$t_h$		0	0	5	0	6	ns
Input Capacitance	$C_{IN}$		5					pF
Power dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

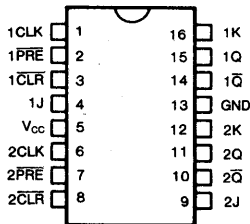
### DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

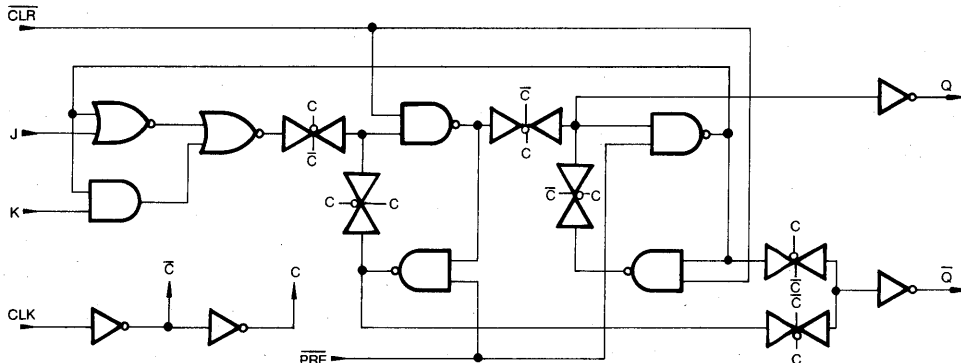


### FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

\*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

### LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT76

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min		Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	45	30		25	MHz		
Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns	
	$t_{PHL}$		10		17		20	ns	
Propagation Delay, PRE or CLR to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns	
	$t_{PHL}$	10		17		20	ns		
Setup Time before CLK↓	J or K	$t_{su}$	10	17		20	ns		
	$\bar{PRE}$ or CLR Inactive		10	17		20	ns		
Hold Time, Data after CLK↓	$t_h$		-3	0		0	ns		
Pulse Width	CLK High or Low	$t_w$	8	13		15	ns		
	$\bar{PRE}$ or CLR Low		8	13		15	ns		
Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$	(per flip-flop)	40				pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

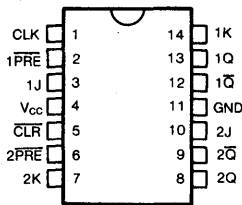
**DESCRIPTION**

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

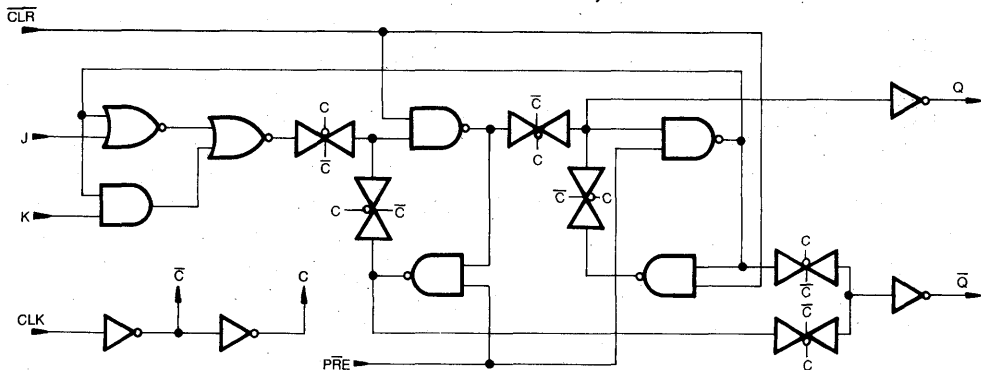


**FUNCTION TABLE**

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

\*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0		$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0		mA	

4



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT78

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$		45	30		25		MHz
Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	10		17		20	ns
	$t_{PHL}$		10		17		20	
Propagation Delay, PRE or CLR to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	
Setup Time before CLK↓	J or K	$t_{su}$	10	17		20		ns
	PRE or CLR Inactive		10	17		20		
Hold Time, J or K after CLK↓	$t_h$		-3	0		0		ns
Pulse Width	CLK High or Low	$t_w$	8	13		15		ns
	PRE or CLR Low		8	13		15		
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per flip-flop)	40					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

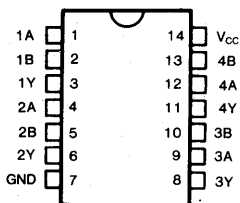
**DESCRIPTION**

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions  $Y=A\oplus B$  or  $Y=\bar{A}B+A\bar{B}$ .

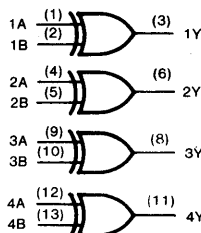
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT86

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C	KS74AHCT		KS54AHCT		Unit	
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C		T <sub>a</sub> = -55°C to +125°C			
			Typ	Min	Max	Min	Max		
Propagation Delay, A or B to Y (Other Input Low)	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	10		16		19	ns	
	t <sub>PHL</sub>		10		16		19		
Propagation Delay, A or B to Y (Other Input High)	t <sub>PLH</sub>		10		16		20	ns	
	t <sub>PHL</sub>		10		16		20		
Input Capacitance	C <sub>IN</sub>		5					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>	(per flip-flop)	15						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

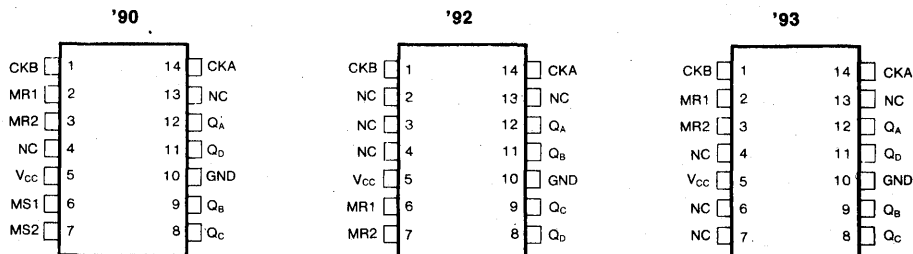
- Various counting mode.
- Function, Pin-out, speed and drive compatibility with 54/74 ALS logic family.
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Input and output interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**DESCRIPTION**

These devices contain four master-slave flip-flops and addition gating to provide a divide by a counter and a three-stage binary counter for which the count cycle length is divide by five for the AHCT90, divide by six for the AHCT92, and divide by eight for the AHCT93. All of these counters have a gated zero reset and the AHCT90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four bit binary), the CKB input is connected to the  $Q_A$  output. The input count pulses are applied to CKA and the outputs are as described in the appropriate truth table. A symmetrical divide-by-the count can be obtained from the AHCT90 counters by connecting the  $Q_D$  output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output  $Q_A$ .

**PIN CONFIGURATION**



FUNCTION TABLE

'90  
BCD COUNT SEQUENCE  
(See Note A)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90  
BI-QUINARY (5-2)  
(See Note B)

Count	Output			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92  
COUNT SEQUENCE  
(See Note C)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93  
COUNT SEQUENCE  
(See Note C)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'90  
RESET/COUNT TRUTH TABLE

Reset Inputs				Output			
MR1	MR2	MS1	MS2	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L				COUNT
L	X	L	X				COUNT
L	X	X	L				COUNT
X	L	L	X				COUNT

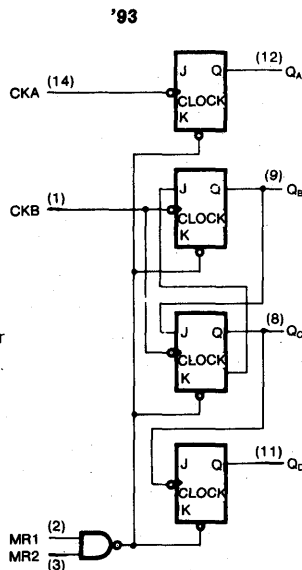
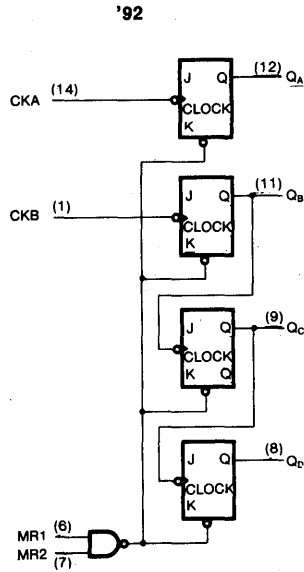
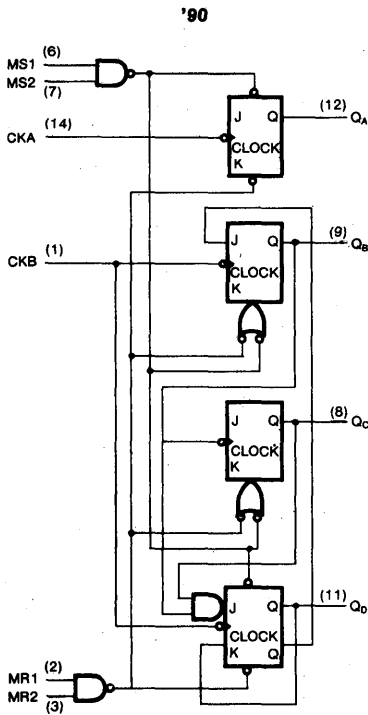
'92, '93  
RESET/COUNT TRUTH TABLE

Reset Inputs		Output			
MR1	MR2	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X				COUNT
X	L				COUNT

**Note A:** Output Q<sub>A</sub> is connected to input CKB for BCD count.  
**Note B:** Output Q<sub>D</sub> is connected to input CKA for bi-quinary count.  
**Note C:** Output Q<sub>A</sub> is connected to input CKB.  
**Note D:** H=High Level, L=Low Level, X=Don't Care.



**LOGIC DIAGRAMS**



Note: The J,K inputs shown without connection are for reference only and are functionally at a high state.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ..... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT90

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			
			Typ	Min	Max	Min	Max		
Maximum clock Frequency	CKA to Q <sub>A</sub>	$f_{max}$	50	40		35		MHz	
	CKB to Q <sub>B</sub>		25	20		18			
Maximum Propagation Delay, CKA to Q <sub>A</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	8		14		17	ns	
	t <sub>PHL</sub>		8		14		17	ns	
Maximum Propagation Delay CKA to Q <sub>D</sub>	t <sub>PLH</sub>		21		42		50	ns	
	t <sub>PHL</sub>		21		42		50	ns	
Maximum Propagation Delay CKB to Q <sub>B</sub>	t <sub>PLH</sub>		8		14		17	ns	
	t <sub>PHL</sub>		9		15		18	ns	
Maximum Propagation Delay CKB to Q <sub>C</sub>	t <sub>PLH</sub>		14		28		33	ns	
	t <sub>PHL</sub>		14		28		33	ns	
Maximum Propagation Delay CKB to Q <sub>D</sub>	t <sub>PLH</sub>		14		28		33	ns	
	t <sub>PHL</sub>		14		28		33	ns	
Maximum Propagation Delay MS to Q <sub>A</sub> , Q <sub>D</sub>	t <sub>PLH</sub>		13		25		30	ns	
Maximum Propagation Delay MS to Q <sub>B</sub> , Q <sub>C</sub>	t <sub>PHL</sub>		18		35		42	ns	
Maximum Propagation Delay MR to any Q	t <sub>PHL</sub>		18		35		42	ns	
Pulse Width	CKA		t <sub>w</sub>	10	15		20		ns
	CKB			20	30		40		
	MS			10	15		20		
	MR	10		15		20			
Recovery Time MR to CKA, CKB	t <sub>rec</sub>		17	24		29	ns		
Maximum Input Capacitance	C <sub>IN</sub>		5				pF		
Power Dissipation Capacitance	C <sub>PD</sub>						pF		

\* C<sub>PD</sub> determines the no-load dynamic dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

† For AC Switching test circuits and timing waveforms see sections

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT92

Characteristic	Symbol	Conditions†	T <sub>A</sub> = 25°C	KS74AHCT		KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		
			Typ	Min	Max	Min	Max	
Maximum clock Frequency	CKA to Q <sub>A</sub>	f <sub>max</sub>	50	40		35		MHz
	CKB to Q <sub>B</sub>		25	20		18		
Maximum Propagation Delay, CKA to Q <sub>A</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	8		13		15	ns
	t <sub>PHL</sub>		8		14		17	
Maximum Propagation Delay CKA to Q <sub>D</sub>	t <sub>PLH</sub>		21		42		48	ns
	t <sub>PHL</sub>		21		42		48	
Maximum Propagation Delay CKB to Q <sub>B</sub>	t <sub>PLH</sub>		8		14		16	ns
	t <sub>PHL</sub>		10		15		17	
Maximum Propagation Delay CKB to Q <sub>C</sub>	t <sub>PLH</sub>		10		14		16	ns
	t <sub>PHL</sub>		11		16		21	
Maximum Propagation Delay CKB to Q <sub>D</sub>	t <sub>PLH</sub>		14		28		33	ns
	t <sub>PHL</sub>		14		20		24	
Maximum Propagation Delay MR to any Q	t <sub>PHL</sub>		18		35		42	ns
Pulse Width	CKA		t <sub>w</sub>	10	15		20	
	CKB	20		30		40		
	MR	10		15		20		
Recovery Time MR to CKA, CKB	t <sub>rec</sub>	17	24		29		ns	
Maximum Input Capacitance	C <sub>IN</sub>		5					pF
Power Dissipation Capacitance	C <sub>PD</sub>							pF

\*C<sub>PD</sub> determines the no-load dynamic dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>

† For AC Switching test circuits and timing waveforms see sections

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT93

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Maximum clock Frequency	CKA to Q <sub>A</sub>	$f_{max}$	50	40		35		MHz
	CKB to Q <sub>B</sub>		25	20		18		
Maximum Propagation Delay, CKA to Q <sub>A</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	8		13		15	ns
	t <sub>PHL</sub>		8		14		17	
Maximum Propagation Delay CKA to Q <sub>D</sub>	t <sub>PLH</sub>		30		56		70	ns
	t <sub>PHL</sub>		30		56		70	
Maximum Propagation Delay CKB to Q <sub>B</sub>	t <sub>PLH</sub>		8		14		17	ns
	t <sub>PHL</sub>		9		15		18	
Maximum Propagation Delay CKB: to Q <sub>C</sub>	t <sub>PLH</sub>		16		29		34	ns
	t <sub>PHL</sub>		17		29		34	
Maximum Propagation Delay CKB to Q <sub>D</sub>	t <sub>PLH</sub>		24		42		50	ns
	t <sub>PHL</sub>		24		42		50	
Maximum Propagation Delay MR to any Q	t <sub>PHL</sub>		17		35		42	ns
Pulse Width	CKA		t <sub>w</sub>	10	15		20	
	CKB	20		30		40		
	MR	10		15		20		
Recovery Time MR to CKA, CKB	t <sub>rec</sub>		17	24		29	ns	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF	
Power Dissipation Capacitance	C <sub>PD</sub>						pF	

\* C<sub>PD</sub> determines the no-load dynamic dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

† For AC Switching test circuits and timing waveforms see sections

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

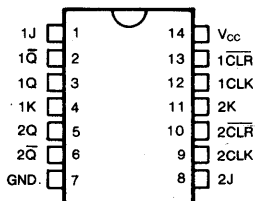
**DESCRIPTION**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

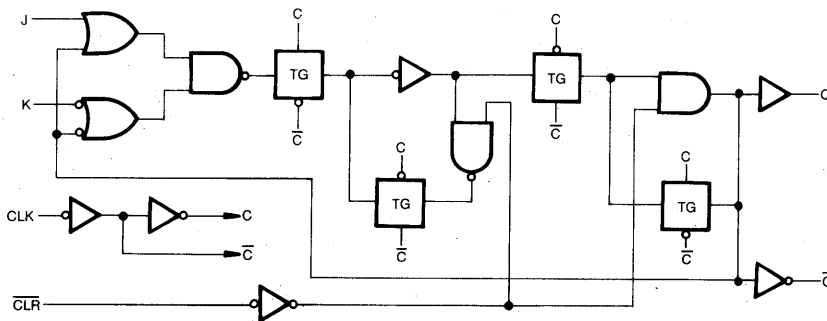
**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs				Outputs	
$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	X	X	X	L	H
H	↓	L	L	$Q_0$	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	$Q_0$	$\overline{Q}_0$

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT107

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$	KS74AHCT			KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	45	30		25		MHz	
Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns	
	$t_{PHL}$		10		17		20	ns	
Propagation Delay, $\bar{CLR}$ to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns	
	$t_{PHL}$		10		17		20	ns	
Setup Time before CLK $\downarrow$	J or K		$t_{su}$	10	17		20		ns
	CLR Inactive			10	17		20		ns
Hold Time, J or K after CLK $\downarrow$	$t_h$			-3	0		0		ns
Pulse Width	CLK High or Low	$t_w$	8	13		15		ns	
	CLR Low		8	13		15		ns	
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per flip-flop)	40					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

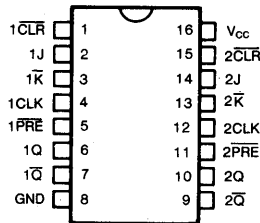
**DESCRIPTION**

These devices contain two positive-edge-triggered J-K̄ flip-flops with independent preset and clear inputs and complementary Q and Q̄ outputs. The present and clear inputs are active-low and operate independently of the clock. Data at the J and K̄ inputs are transferred to the outputs on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggle flip-flops by grounding K and tying J high. They can also perform as D-type flops if J and K̄ are tied together.

These devices provide speeds and drive capability equivalent to their ALST, L counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**PIN CONFIGURATION**

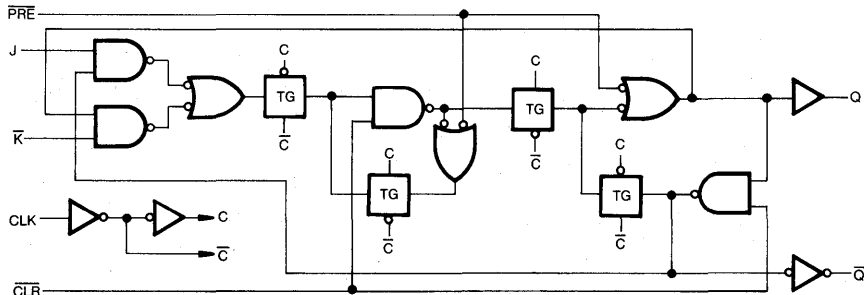


**FUNCTION TABLE**

Inputs					Outputs	
PRE	CLR	CLK	J	K̄	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

\*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

**LOGIC DIAGRAM**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT		KS54AHCT		Unit
			Typ		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Guaranteed Limits									
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

4



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT109

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	55	34		30		MHz
Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	ns
Propagation Delay, PRE or CLR to Q or $\bar{Q}$	$t_{PLH}$		10		14		20	ns
	$t_{PHL}$		10		14		20	ns
Setup Time before CLK†	Data		$t_{su}$	7	12		15	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive		5	8		10	ns	
Hold Time, Data after CLK†	$t_h$		0	0		0	ns	
Pulse Width	CLK High or Low	$t_w$	9	14		17	ns	
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		9	15		17	ns	
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$		40				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

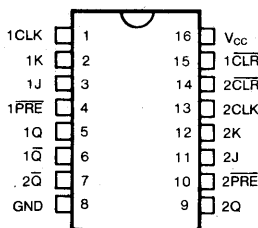
**DESCRIPTION**

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

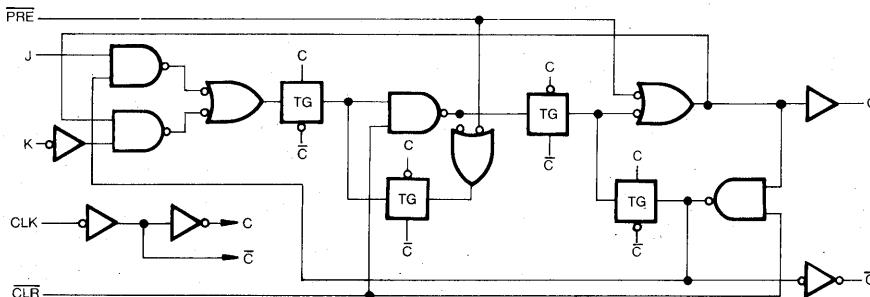


**FUNCTION TABLE**

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	Q <sub>0</sub> -bar
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q <sub>0</sub>	Q <sub>0</sub> -bar

\*Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

**LOGIC DIAGRAM**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	.0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT112

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	30		25		MHz
Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	
Propagation Delay, PRE or CLR to Q or $\bar{Q}$	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	
Setup Time before CLK↓	J or K		$t_{su}$	10	17		20	ns
	PRE or CLR Inactive	10		17		20		
Hold Time, Data after CLK↓	$t_h$		0	0		0	ns	
Pulse Width	CLK High or Low	$t_w$	10	17		20	ns	
	PRE or CLR Low		6	10		15		
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$ (per flip-flop)		40				pF	

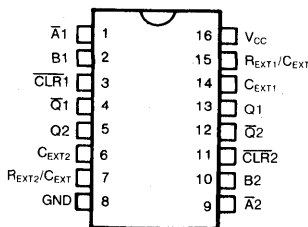
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Simple pulse width formula  $t_w = 0.45RC$
- DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor (Rext) and capacitor (Cext). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input (Ai) or the active HIGH going edge input (Bi). By repeating this process, the output pulse period (nQ=HIGH, nQ=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Low-going edge on input CLR, which also inhibits the triggering. An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when  $C_{EXT} > 10nF$ , the typical output pulse width is defined as;  $t_w = 0.45 \times R_{EXT} \times C_{EXT}(typ)$ .

Where  $t_w$  is in seconds. R is in ohm. and C is in farads. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

Inputs			Outputs	
CLR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

- H= HIGH voltage level
- L= LOW voltage level
- X= don't care
- ↑= LOW to HIGH transition
- ↓= HIGH to LOW transition
- = one HIGH level output pulse
- = one LOW level output pulse

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package(N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ..... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT} = 0\mu A$		2.7	2.9	3.0	mA



AC ELECTRICAL CHARACTERISTICS (Input  $t_r, t_f \leq 2$  ns), AHCT123

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$ $C_{ext} = 0,$ $R_{ext} = 5\text{k}\Omega$	18		33		39	ns
$\bar{A}, B$ to $Q, \bar{Q}$	$t_{PHL}$		18		33		39	
Propagation Delay	$t_{PLH}$		16		27		32	
$\bar{CLR}$ to $Q, \bar{Q}$	$t_{PHL}$		16		27		32	
Output Pulse Width 1	$t_{WQ1}$		116		207		209	ns
Output Pulse Width 2	$t_{WQ2}$	$C_L = 50\text{pF}$ $C_{ext} = 10\text{nF}$ $R_{ext} = 10\text{k}\Omega$	45	38	52	38	52	$\mu\text{s}$
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $A_i = \text{LOW}$	5		16		20	ns
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $B_i = \text{High}$	5		16		20	ns
Clear Pulse Width	$t_w$	$C_L = 50\text{pF}$ $CLR_i = \text{LOW}$	6		16		20	ns
External Timing Resistance	$R_{ext}$			2	100	2	100	$\text{k}\Omega$
External Timing Capacitance	$C_{ext}$		no restriction					$\text{pF}$
Input Capacitance	$C_{in}$		5					$\text{pF}$
Power Dissipation Capacitance	$C_{PD}$							$\text{pF}$

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance.

For output pulse widths greater than  $100\mu\text{s}$  or external capacitance greater than  $10\text{nF}$  the following equation should be used.

$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

$t_w$  is in  $\mu\text{s}$

K is the multiplying factor

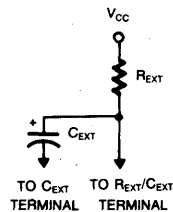
and is approximately 0.45 for

$C_{ext}$  is in  $\text{nF}$

$R_{ext}$  is in  $\text{k}\Omega$

For best results, system ground should be applied to the  $C_{ext}$  terminal. These devices do not require a switching diode in series with the  $R_{ext}/C_{ext}$  terminal (as required by some other monostable multivibrators)

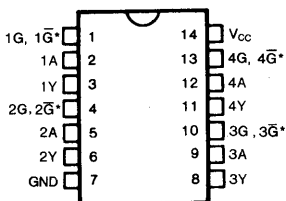
TIMING COMPONENT



#### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

#### PIN CONFIGURATION



\* $\bar{G}$  for '125; G for '126

#### FUNCTION TABLES

'125

Inputs		Output
A	$\bar{G}$	Y
H	L	H
L	L	L
X	H	Z

'126

Inputs		Output
A	G	Y
H	H	H
L	H	L
X	L	Z

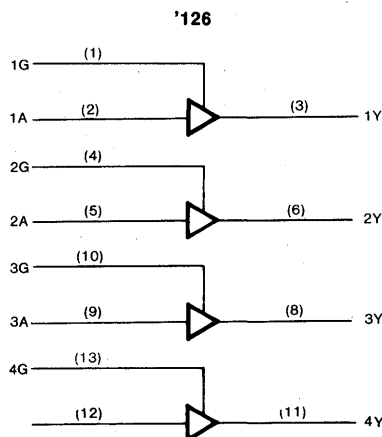
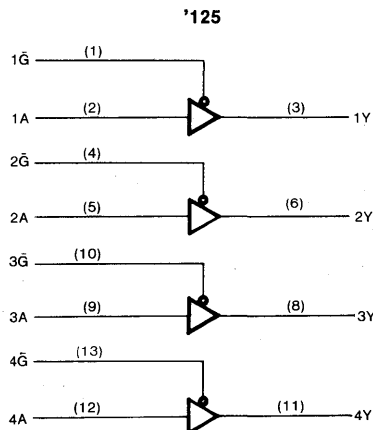
#### DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### LOGIC DIAGRAMS





#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_D^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT125, AHCT126

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$			
			Typ	Min	Max	Min	Max		
Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	6		10		12	ns	
		$C_L = 150\text{pF}$	9		15		18		
	$t_{PHL}$	$C_L = 50\text{pF}$	7		13		15		
		$C_L = 150\text{pF}$	10		17		19		
Output Enable Time Enable to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	ns
			$C_L = 150\text{pF}$	14		23		28	
	$t_{PZL}$		$C_L = 50\text{pF}$	11		18		22	
			$C_L = 150\text{pF}$	14		23		28	
Output Disable Time, Enable to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22		
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output disabled	10					pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$G$ or $\bar{G} = V_{CC}$	5					pF	
		$G$ or $\bar{G} = \text{GND}$	30						

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

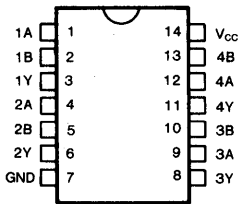
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function  $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$  in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

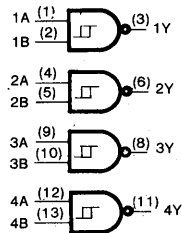
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  .. 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84		$V_{CC}-0.11$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0		40.0		$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9		3.0		mA

**DC ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Min	Max	Min	Max	Min	Max	
			Positive-Going Threshold Voltage	$V_{T+}$	$V_{CC}=4.5V$ $V_{CC}=5.5V$	1.2 1.4	1.9 2.1	1.2 1.4	
Negative-Going Threshold Voltage	$V_{T-}$	$V_{CC}=4.5V$ $V_{CC}=5.5V$	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V
Hysteresis ( $V_{T+}-V_{T-}$ )	$V_H$	$V_{CC}=4.5V$ $V_{CC}=5.5V$	0.4 0.4	1.4 1.5	0.4 0.4	1.4 1.5	0.4 0.4	1.4 1.5	V



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT132

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	8		14		17	ns
	$t_{PHL}$		8		14		17	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF

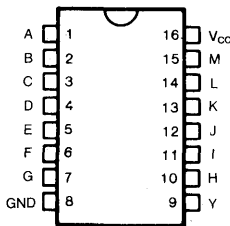
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

INPUTS A THRU M		OUTPUT Y
All inputs	H	L
One or more inputs	L	H

**DESCRIPTION**

The 133 contains a single 13-input NAND gate. It performs the boolean functions (in positive logic):

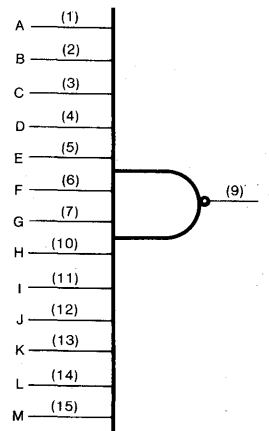
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

$$Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}}$$

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_D$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits						
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0			$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT133

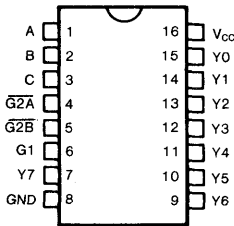
Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay, Any input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	11		18		22	ns	
	$t_{PHL}$		11		18		22		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$		15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .  
 † For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

Enable Inputs		Select Inputs			Outputs							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

\*G2 = G2A + G2B

**DESCRIPTION**

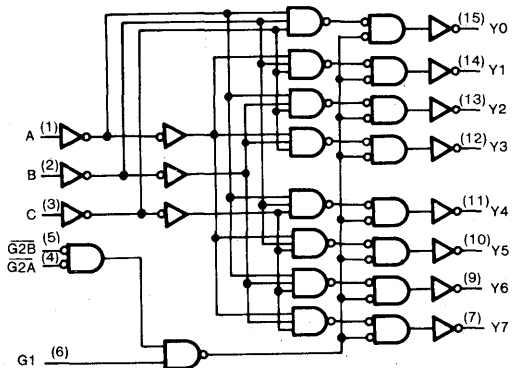
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

**LOGIC DIAGRAM**





**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$				Unit
			Typ	Guaranteed Limits			
			KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT138

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, A, B, C or any Y	$t_{PLH}$	$C_L = 50\text{pF}$	12		20		24	ns
	$t_{PHL}$		12		20		24	
Propagation Delay, G1 to any Y	$t_{PLH}$		12		18		20	ns
	$t_{PHL}$		12		18		20	
Propagation Delay, $\bar{G}2A$ or $\bar{G}2B$ to any Y	$t_{PLH}$		12		18		20	ns
	$t_{PHL}$		12		18		20	
Input Capacitance	$C_{IN}$						pF	
Power Dissipation Capacitance*	$C_{PD}$		50				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

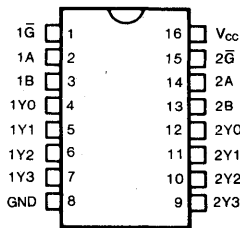
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory, this means that the effective system delay introduced by the decoder is negligible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

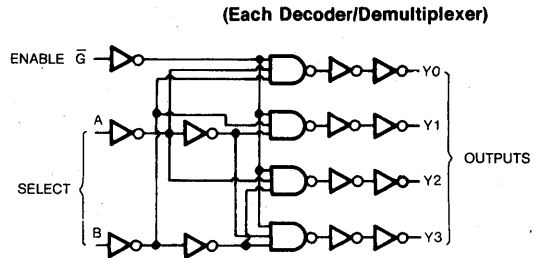
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs			Outputs			
Enable $\bar{G}$	Select B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
					$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT139

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to Y	$t_{PLH}$	$C_L = 50\text{pF}$	11		17		20	ns
	$t_{PHL}$		11		17		20	
Propagation Delay, $\bar{G}$ to any Y	$t_{PLH}$		11		18		21	ns
	$t_{PHL}$		11		18		21	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$		50					pF

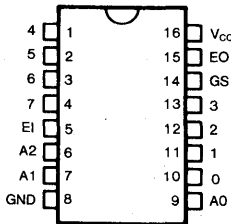
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Encodes eight data lines in priority
- Provides 3-bit binary priority code
- Input enable capability
- Easily cascadable
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The 148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

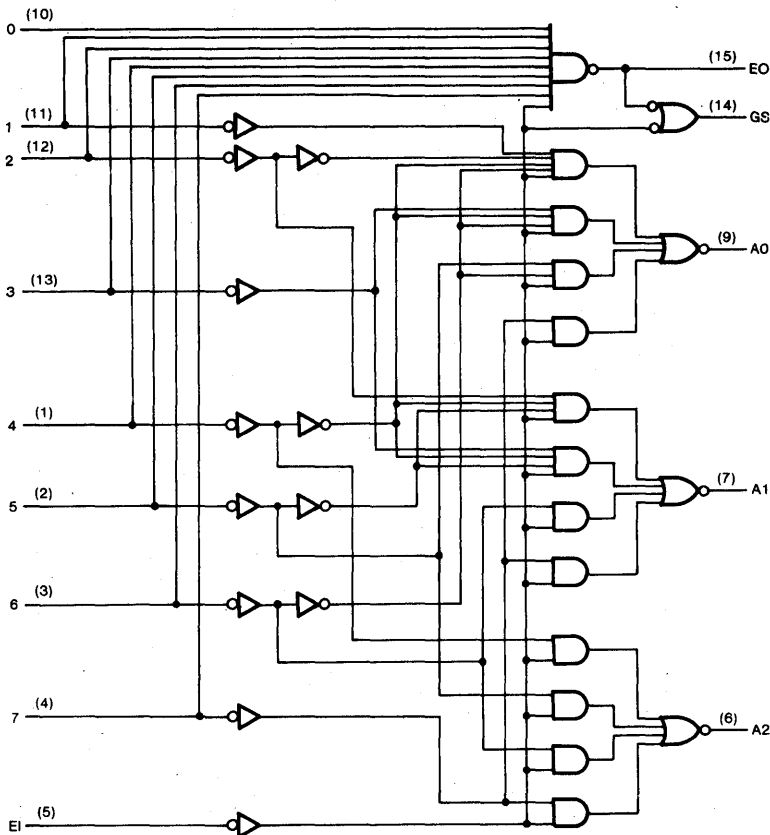
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

**4**

		Inputs						Outputs					
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	L	H	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits						
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	0.1 0.4	V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	160.0	160.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	3.0	3.0	mA	

**4**

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT148)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			$V_{CC} = 5.0\text{V}$	$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, 1-7 to A0, A1 or A2	$t_{PLH}$	$C_L = 50\text{pF}$	10		17		20	ns
	$t_{PHL}$		10		17		20	
Propagation Delay, 0-7 to EO	$t_{PLH}$		11		18		22	ns
	$t_{PHL}$		11		18		22	
Propagation Delay, 0-7 to GS	$t_{PLH}$		14		24		29	ns
	$t_{PHL}$		14		24		29	
Propagation Delay, E1 to A0, A1 or A2	$t_{PLH}$		10		16		19	ns
	$t_{PHL}$		10		16		19	
Propagation Delay, E1 to GS	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	
Propagation Delay, E1 to EO	$t_{PLH}$		11		18		22	ns
	$t_{PHL}$		11		18		22	
Input Capacitance	$C_{IN}$			5				pF
Power Dissipation Capacitance*	$C_{PD}$			50				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

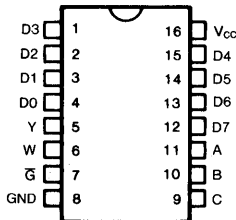
† For AC switching test circuits and timing waveforms see section 2.



### FEATURES

- Can perform as:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive currents outputs  
( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  - KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
  - KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ( $\bar{G}$ ) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLE

INPUTS			OUTPUTS	
SELECT		STROBE $\bar{G}$	Y	W
C	B			
X	X	X	H	L
L	L	L	L	H
L	L	L	D0	$\bar{D0}$
L	L	H	D1	$\bar{D1}$
L	H	L	D2	$\bar{D2}$
L	H	H	D3	$\bar{D3}$
H	L	L	D4	$\bar{D4}$
H	L	H	D5	$\bar{D5}$
H	H	L	D6	$\bar{D6}$
H	H	H	D7	$\bar{D7}$

H = high level, L = low level, X = irrelevant  
D0, D1 ... D7 = the level of the D respective input

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , .....  $-0.5\text{V}$  to  $+7\text{V}$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5\text{V}$  or  $V_I > V_{CC} + 0.5\text{V}$ ) .....  $\pm 20 \text{ mA}$   
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5\text{V}$  or  $V_O > V_{CC} + 0.5\text{V}$ ) .....  $\pm 20 \text{ mA}$   
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5\text{V} < V_O < V_{CC} + 0.5\text{V}$ ) .....  $\pm 70 \text{ mA}$   
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250 \text{ mA}$   
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † .....  $500 \text{ mW}$

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

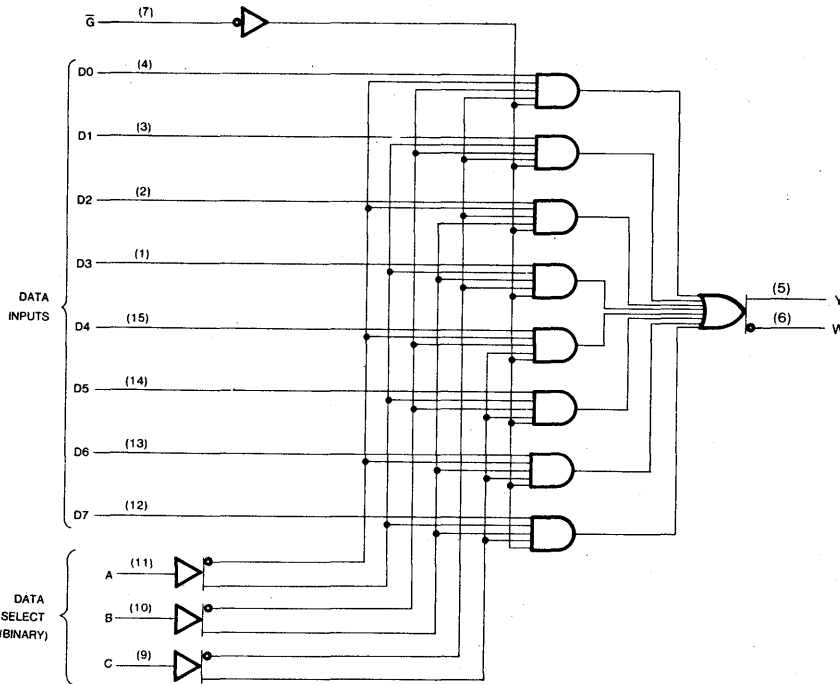
Plastic Package (N):  $-12 \text{ mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  .....  $4.5\text{V}$  to  $5.5\text{V}$   
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ...  $0\text{V}$  to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max  $500 \text{ ns}$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

LOGIC DIAGRAM



4

DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-6 mA	V <sub>CC</sub> 4.2	V <sub>CC</sub> - 0.1 3.98	V <sub>CC</sub> - 0.1 3.84	V <sub>CC</sub> - 0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI <sub>CC</sub>	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT151

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$		
			Min	Max	Min	Max		
Propagation Delay, A, B or C to Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31	
Propagation Delay, A, B or C to W	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		24 29		27 33	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		24 29		27 33	
Propagation Delay, Any D to Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	9 12		15 20		18 24	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	9 12		15 20		18 24	
Propagation Delay Any D to W	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		15 20		18 24	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		15 20		18 24	
Propagation Delay, $\bar{G}$ to Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		19 24		23 29	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		19 24		23 29	
Propagation Delay, $\bar{G}$ to W	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

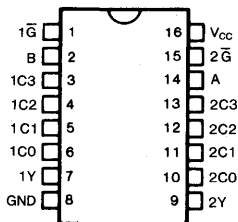
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Allows Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- '253 is the 3-State Version of this part
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive currents Outputs (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

Each of these data selectors/multiplexers contains inverters and drives to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

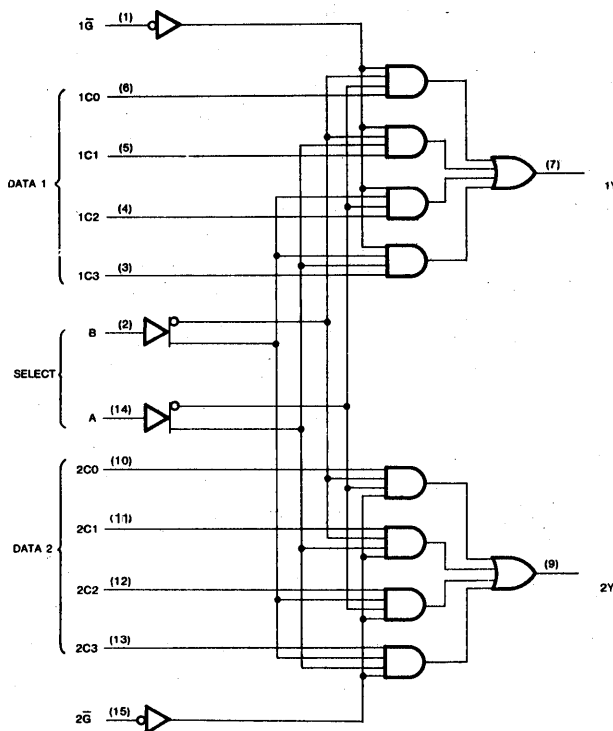
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**FUNCTION TABLE**

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	Ḡ	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT153

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0\text{V}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		Unit
			Typ		Min	Max	Min	Max	
Propagation Delay, A or B to Y	$t_{PLH}$	$C_L=50\text{pF}$	13		21		25	ns	
		$C_L=150\text{pF}$	16		26		31		
	$t_{PHL}$	$C_L=50\text{pF}$	13		21		25	ns	
		$C_L=150\text{pF}$	16		26		31		
Propagation Delay, Data (Any C) to Y	$t_{PLH}$	$C_L=50\text{pF}$	9		15		18	ns	
		$C_L=150\text{pF}$	12		20		24		
	$t_{PHL}$	$C_L=50\text{pF}$	9		15		18	ns	
		$C_L=150\text{pF}$	12		20		24		
Propagation Delay, G to Y	$t_{PLH}$	$C_L=50\text{pF}$	11		18		22	ns	
		$C_L=150\text{pF}$	14		23		28		
	$t_{PHL}$	$C_L=50\text{pF}$	11		18		22	ns	
		$C_L=150\text{pF}$	14		23		28		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

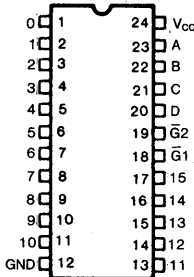
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



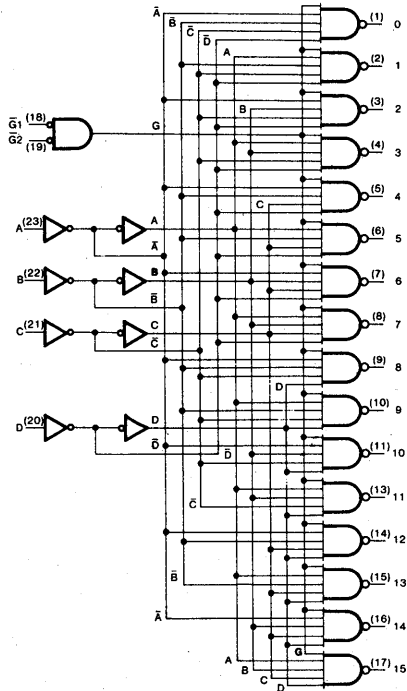
**DESCRIPTION**

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs,  $\bar{G}1$  and  $\bar{G}2$ , are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



FUNCTION TABLE

Inputs					Outputs																	
$\bar{G}1$	$\bar{G}2$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
L	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

4

**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA
- Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C
- Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$
- Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -8\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0		160.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		$\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT154

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay, A, B, C, D to Any Output	$t_{PLH}$	$C_L = 50\text{pF}$	12		20		24	ns	
	$t_{PHL}$		12		20		24		
Propagation Delay, $\bar{G}1$ or $\bar{G}2$ to Any Output	$t_{PLH}$		12		20		24	ns	
	$t_{PHL}$		12		20		24		
Input Capacitance	$C_{IN}$		5					$\text{pF}$	
Power Dissipation Capacitance*	$C_{PD}$		50					$\text{pF}$	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Typical applications:**  
 Dual 2-to-4 line decoder  
 Dual 1-to-4 line demultiplexer  
 3-to-8 line decoder  
 1-to-8 line demultiplexer
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

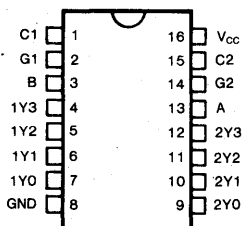
**DESCRIPTION**

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

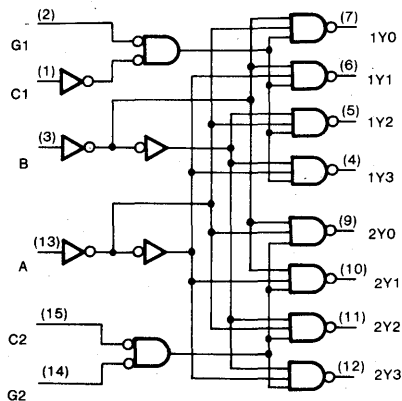
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLES**

**2-to-4 Line Decoder or 1-to-4 Line Demultiplexer**

Inputs				Outputs			
Select	Strobe	Data	B				
X	X	H		X	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select	Strobe	Data	B				
X	X	H		X	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

**3-to-8 Line Decoder or 1-to-8 Line Demultiplexer**

Select			Strobe or Data	(0) (1) (2) (3) (4) (5) (6) (7)								
C†	B	A		G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H
H	H	L	L	H	H	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	H	H	L

†=Inputs C1 and C2 Connected together

‡=Inputs G1 and G2 Connected together

**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA
- Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C
- Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$
- Operating Temperature  
Range  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V\pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				KS74AHCT		KS54AHCT		Unit
			Typ		Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0		2.0		2.0		V		
Maximum Low-Level Input Voltage	$V_{IL}$		0.8		0.8		0.8		V		
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V		
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V		
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$		$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$		
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	8.0		80.0		160.0		$\mu\text{A}$		
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7		2.9		3.0		mA		

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT155)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC}=5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Propagation Delay, A, B, C2, G1 or G2 to any Output (2 levels of logic)	$t_{PLH}$	$C_L = 50\text{pF}$	12		20		24	ns
	$t_{PHL}$		12		20		24	
Maximum Propagation Delay, A or B to any Y (3 levels of logic)	$t_{PLH}$		14		23		28	ns
	$t_{PHL}$		14		23		28	
Maximum Propagation Delay, C1 to any Y	$t_{PLH}$		13		22		26	ns
	$t_{PHL}$		13		22		26	
Maximum Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$						pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

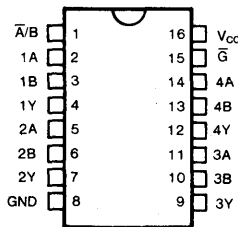
**DESCRIPTION**

These are data selectors multiplexers which select a 4-bit word from one of two sources via the control of a common select input ( $\bar{A}/B$ ). A separate strobe input ( $\bar{G}$ ) is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

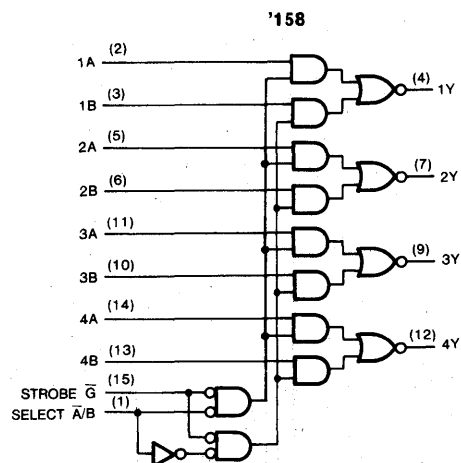
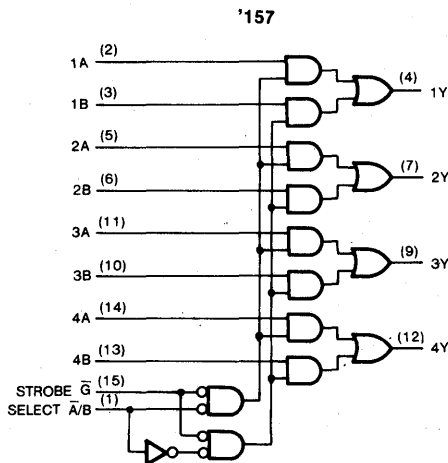
**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs				Output Y	
Strobe $\bar{G}$	Select $\bar{A}/B$	Data		'157	'158
		A	B		
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT157, AHCT158

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to Y	tPLH	$C_L = 50\text{pF}$	11		15		18	ns
	tPHL		11		15.5		18	
Propagation Delay, A/B to Y	tPLH		13		22		26	ns
	tPHL		13		22		26	
Propagation Delay, G to Y	tPLH		12		19		23	ns
	tPHL		12		19		23	
Input Capacitance	C <sub>IN</sub>		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>						pF	

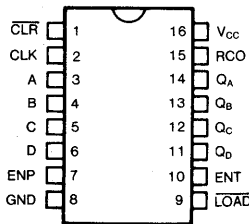
\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Internal Look Ahead for Fast Counting
- Carry Output for n-bit cascading
- Synchronous Counting
- Synchronously Programmable
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLES**

'160, '161

CLK	CLR	ENP	ENT	LOAD	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

'162, '163

CLK	CLR	ENP	ENT	LOAD	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment counter

**DESCRIPTION**

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and 163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with QA high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or LOAD) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

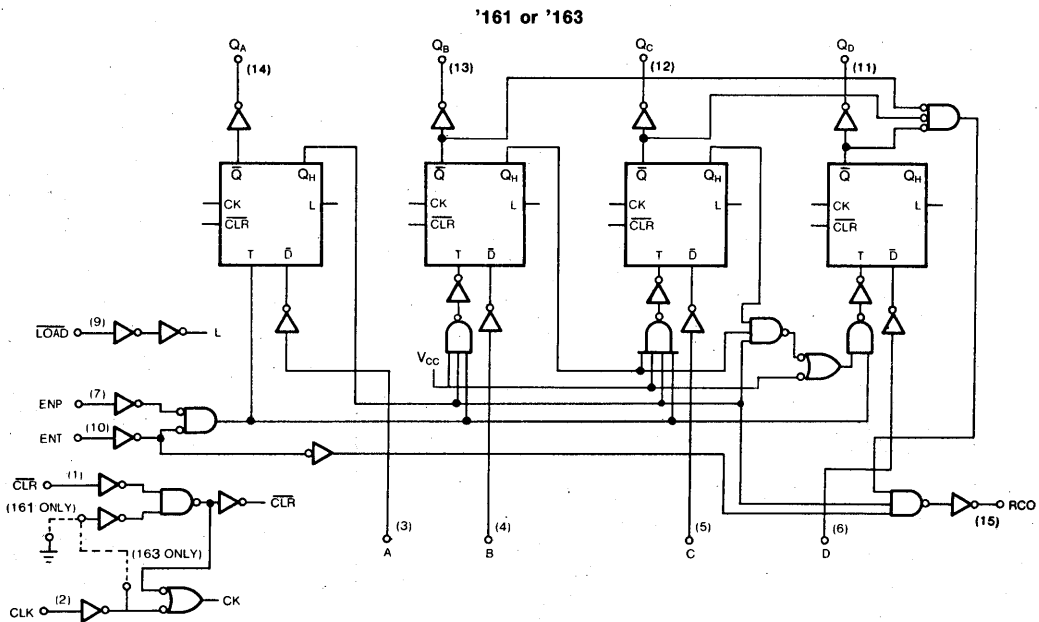
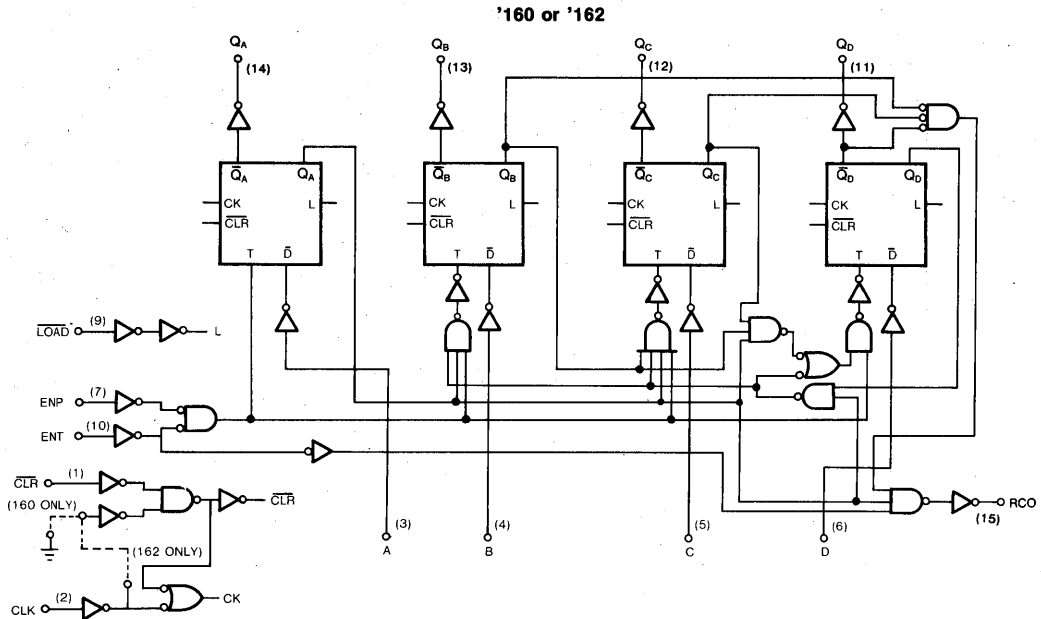
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

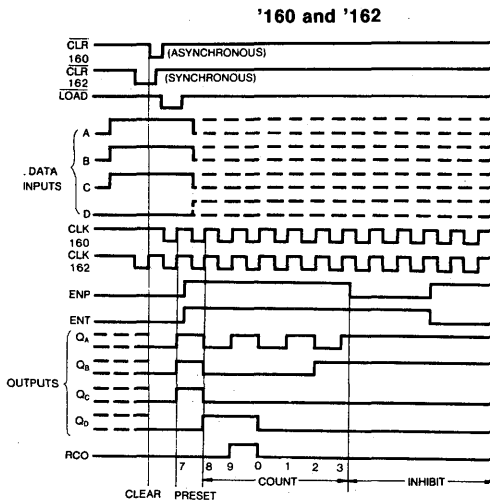




**LOGIC DIAGRAMS**

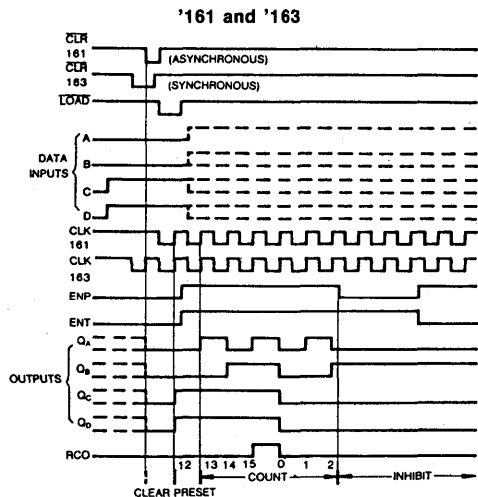


**Typical Clear, Preset, Count and Inhibit Sequences**



**Sequence:**

- (1) Clear outputs to zero
- (2) Preset to BCD seven
- (3) Count to eight, nine, zero, one, two, and three
- (4) Inhibit



**Sequence:**

- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one and two
- (4) Inhibit

**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$
- DC Input Diode Current,  $I_{IK}$   
 $(V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
 $(V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
 $(-0.5V < V_O < V_{CC} + 0.5V)$  . . . . .  $\pm 35$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA
- Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$
- Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$
- Operating Temperature  
 Range  
 KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = -20\mu\text{A}$ $I_o = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = 20\mu\text{A}$ $I_o = 4\text{mA}$ $I_o = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	80.0	160.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_1 = 2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	2.9	3.0	3.0	$\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT160, AHCT161)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0\text{V}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	40		35		MHz	
Propagation Delay, CLK to RCO	$t_{PLH}$		15		20		24	ns	
	$t_{PHL}$		15		20		24	ns	
Propagation Delay, CLK to any Q	$t_{PLH}$		10		16		19	ns	
	$t_{PHL}$		10		16		19	ns	
Propagation Delay, ENT to RCO	$t_{PLH}$		9		13		16	ns	
	$t_{PHL}$		9		13		16	ns	
Propagation Delay, CLR to any Q	$t_{PHL}$		15		24		29	ns	
Propagation Delay, CLR to RCO	$t_{PHL}$	17		23		33	ns		
Pulse Width	CLK High or Low	$t_w$	8	12		16		ns	
	CLR Low		10	15		20		ns	
Setup Time before CLK†	A, B, C, D	$t_{su}$	10	15		20		ns	
	LOAD		10	15		20			
	ENP, ENT		10	15		20			
	CLR inactive		6	10		10			
Hold time, All Synchronous Inputs after CLK†	$t_h$		0	0		0		ns	
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$		80					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT162, AHCT163

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$		50	40		35		MHz
Propagation Delay, CLK to RCO	$t_{PLH}$	$C_L = 50\text{pF}$	15		20		24	ns
	$t_{PHL}$		15		20		24	
Propagation Delay, CLK to any Q	$t_{PLH}$		10		16		20	ns
	$t_{PHL}$		10		16		20	
Propagation Delay, ENT to RCO	$t_{PLH}$		9		15		18	ns
	$t_{PHL}$		9		15		18	
Pulse Width, CLK High or Low	$t_w$		8	12.5		20		ns
Setup Time before CLK†	A, B, C, D	$t_{su}$	10	15		20		ns
	LOAD		10	15		20		
	ENP, ENT		15	15		20		
	CLR inactive		6	10		10		
	CLR Low		6	15		20		
Hold time, All Synchronous Inputs after CLK†	$t_h$		0	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$		80					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **AND—Gated (enable/disable) serial inputs**
- **Fully buffered clock and serial inputs**
- **Direct clear**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**DESCRIPTION**

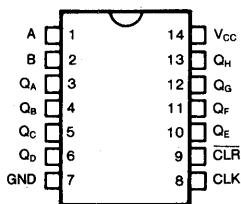
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of their clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

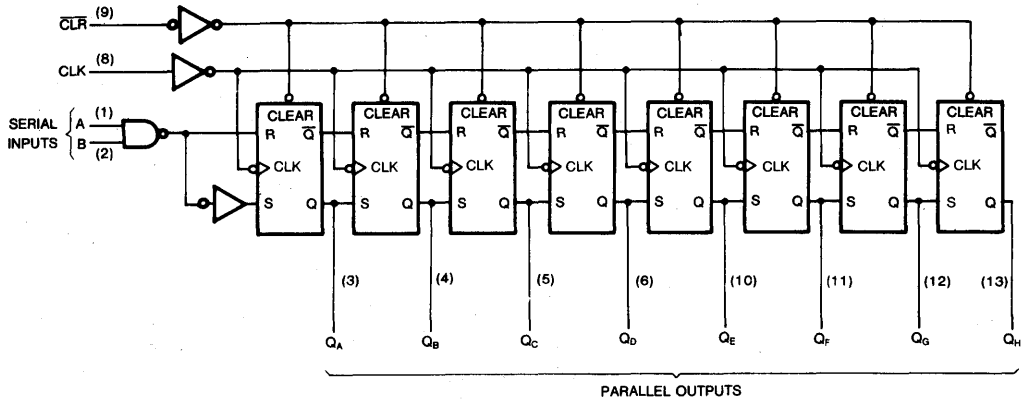


**FUNCTION TABLE**

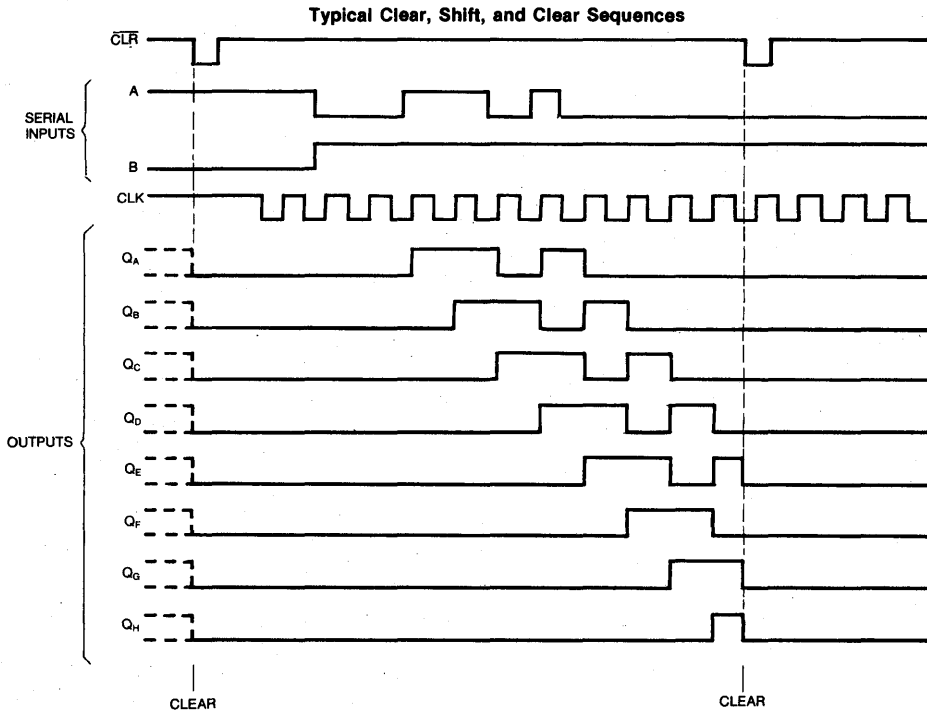
Inputs				Outputs		
CLR	CLK	A	B	QA	QB ... QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

H = high level (steady state), L = low level (steady state)  
 X = irrelevant (any input, including transitions)  
 ↑ = transition from low to high level.  
 QA0, QB0, QH0 = the level of QA, QB or QH, respectively, before the indicate steady-state input conditions were established.  
 QAn, QGn = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

LOGIC DIAGRAMS



4



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
			Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT164

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	60	36		30		MHz
Propagation Delay, CLR to any Q	$t_{PHL}$		12		20		24	ns
Propagation Delay, CLK to any Q	$t_{PLH}$		11		18		21	ns
	$t_{PHL}$		11		18		21	
Pulse Width	CLR Low		$t_w$	8	12		15	ns
	CLK High or Low	8		12		15		
Setup Time before CLK†	Data	$t_{su}$	8	12		15	ns	
	CLR Inactive		8	12		15		
Hold Time Data after CLK†	$t_h$		0	4		5	ns	
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$	(per package)	120				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-Serial data conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

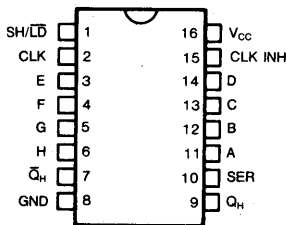
These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/LD input low. When SH/LD is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the SH/LD input is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

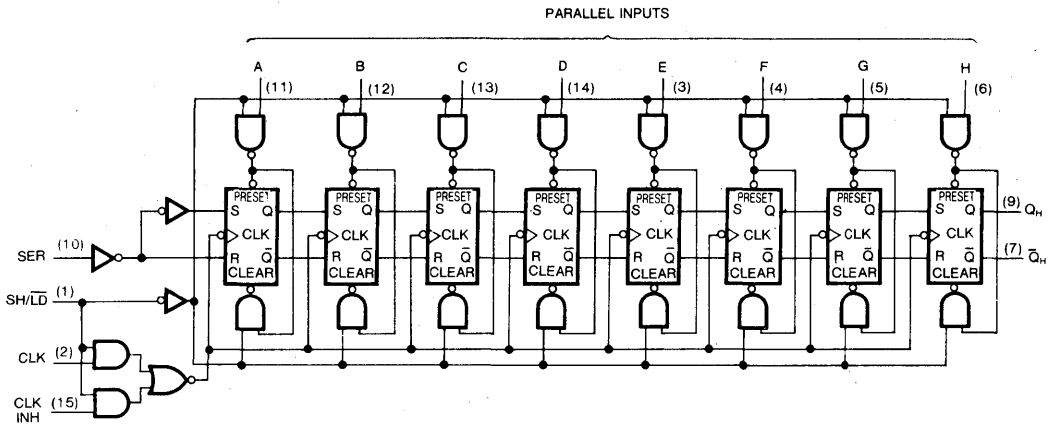


**FUNCTION TABLE**

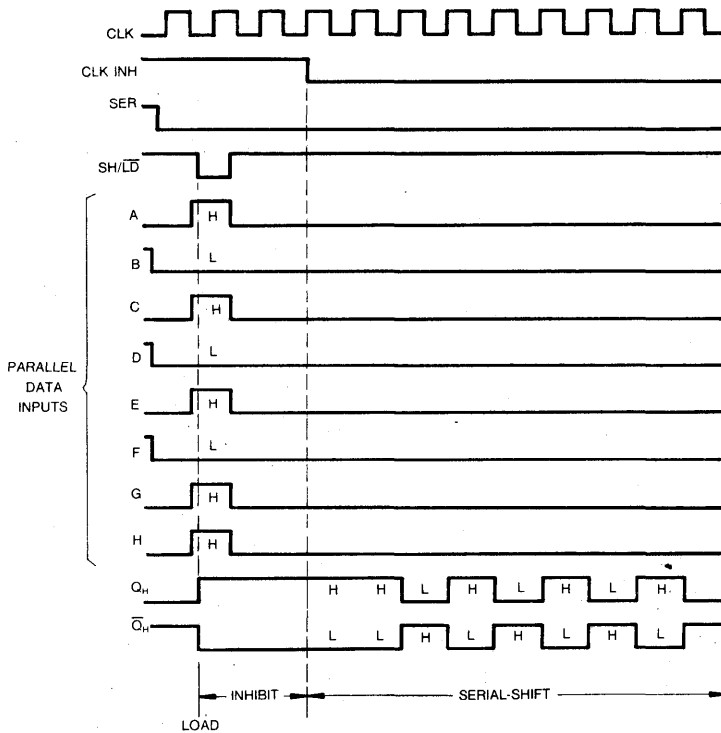
SH/LD	Inputs		Function
	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT*
H	↑	L	SHIFT*

\*Content of each internal register shifts toward output  $Q_h$ . Data at serial input is shifted into first register.

LOGIC DIAGRAMS



Typical Shift, Load and Inhibit Sequences



4

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT165

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$		50	30		25		MHz
Propagation Delay, SH/LD to $Q_H$ or $\bar{Q}_H$	$t_{PLH}$	$C_L = 50\text{pF}$	15		25		30	ns
	$t_{PHL}$		15		25		30	
Propagation Delay, CLK to $Q_H$ or $\bar{Q}_H$	$t_{PLH}$		19		31		37	ns
	$t_{PHL}$		19		31		37	
Propagation Delay, H to $Q_H$ or $\bar{Q}_H$	$t_{PLH}$		12		20		24	ns
	$t_{PHL}$		12		20		24	
Pulse Width	SH/ $\bar{LD}$ Low	$t_w$	8	12		15		ns
	CLK High or Low		8	12		15		
Setup Time	SH/ $\bar{LD}$ High before CLK↑	$t_{su}$	7	15		20		
	SER before CLK↑		8	12		15		
	CLK INH Low before CLK↑		7	15		20	ns	
	CLK INH High before CLK↓		7	15		20		
Hold Time	Data before SH/ $\bar{LD}$ ↑		5	8		10		
	SER Data after CLK↑	$t_h$	0	0		0		ns
PAR Data after SH/ $\bar{LD}$ ↑	0		0		0			
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$		100					pF

4

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Synchronous load
- Direct overriding clear
- Parallel to serial conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

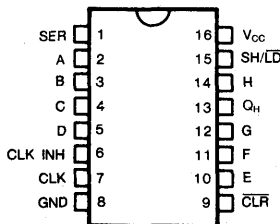
**DESCRIPTION**

These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

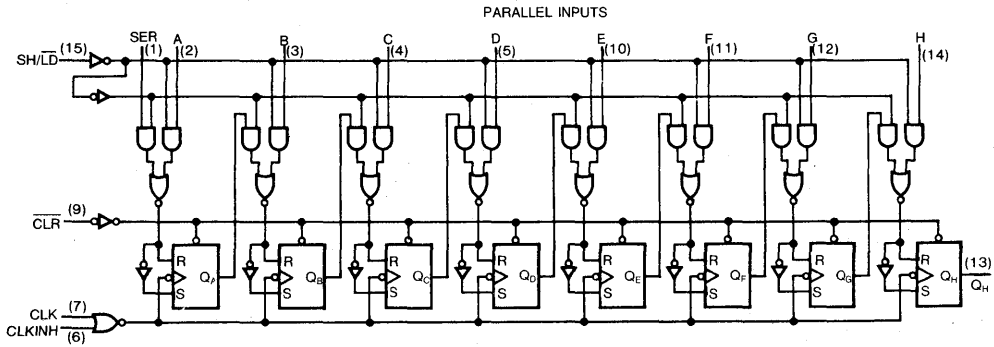
**PIN CONFIGURATION**



**FUNCTION TABLE**

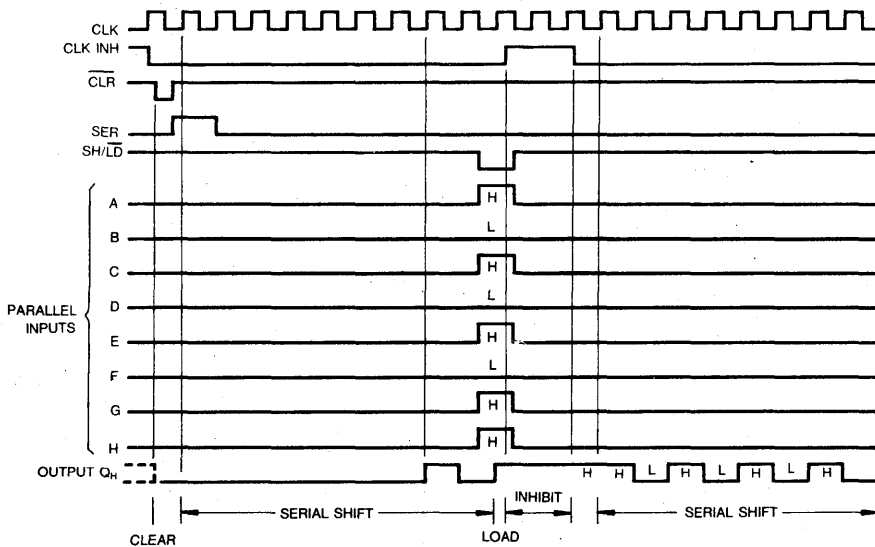
Inputs						Internal Outputs		Output
$\overline{\text{CLR}}$	$\overline{\text{SH/LD}}$	CLK INH	CLK	SER	Parallel A ... H	$Q_A$	$Q_B$	$Q_H$
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	L	↑	X	a ... h	a	b	h
H	H	L	↑	H	X	H	$Q_{An}$	$Q_{Gn}$
H	H	L	↑	L	X	L	$Q_{An}$	$Q_{Gn}$
H	X	H	↑	X	X	$G_{A0}$	$Q_{B0}$	$Q_{H0}$

**LOGIC DIAGRAM**



**4**

**Typical Clear, Shift, Load, Inhibit, and Shift Sequences**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT166

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	60	36		30		MHz	
Propagation Delay, CLR to $Q_H$	$t_{PHL}$		10		17		20	ns	
Propagation Delay, CLK to $Q_H$	$t_{PLH}$		13		21		25	ns	
	$t_{PHL}$		13		21		25		
Pulse Width	CLR Low		$t_w$	8	12		15		ns
	CLK High or Low			8	12		15		
Setup Time	SH/LD High before CLK↑	$t_{su}$	8	12		15		ns	
	SER before CLK↑		8	12		15			
	CLK INH before before CLK↑		8	12		15			
	Data before SH/LD↑		8	12		15			
	CLR Inactive before CLK		8	12		15			
Hold Time	SH/LD High after CLK↑	$t_h$	5	8		10		ns	
	SER after CLK↑		5	8		10			
	CLK INH after CLK↑		5	8		10			
	Data after SH/LD↑		5	8		10			
	CLR Active after CLK↑		5	8		10			
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

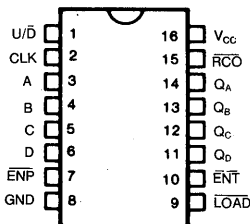
† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Fully Synchronous Operation for Counting and Programming
- Internal Look Ahead for Fast Counting
- Carry Output for N-bit Cascading
- Fully Independent Clock Circuit
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

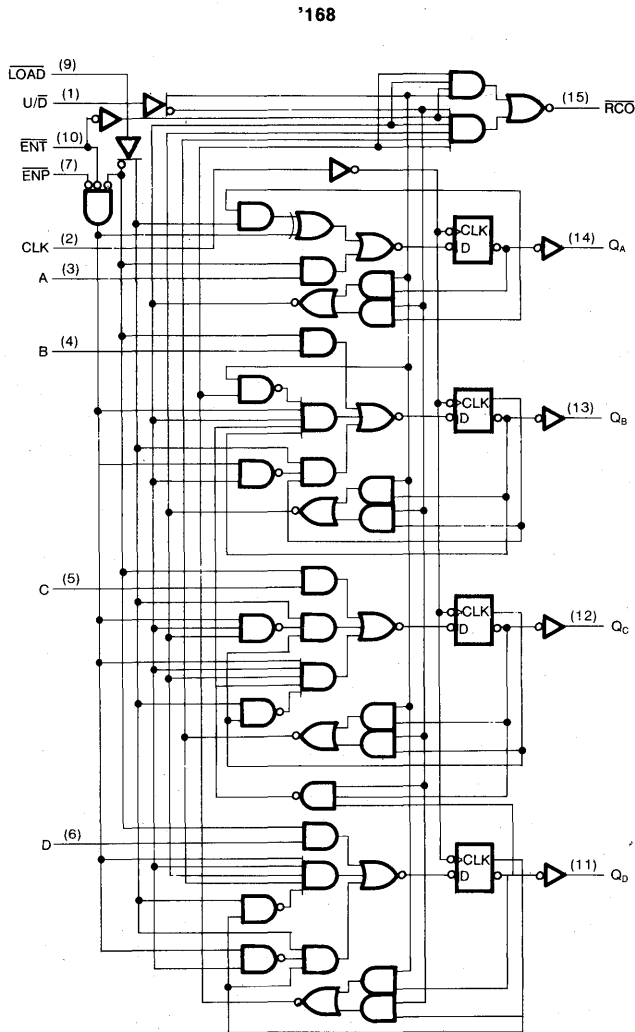
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs ( $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$ ) must be low to count. The direction of the count is determined by the level of the  $U/\overline{D}$  input. When  $U/\overline{D}$  is high, the counter counts up; when low, it counts down. Input  $\overline{\text{ENT}}$  is fed forward to enable the carry output. The ripple carry output ( $\overline{\text{RCO}}$ ) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at  $\overline{\text{ENP}}$  or  $\overline{\text{ENT}}$  are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs ( $\overline{\text{ENP}}$ ,  $\overline{\text{ENT}}$ ,  $\overline{\text{LOAD}}$ ,  $U/\overline{D}$ ) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

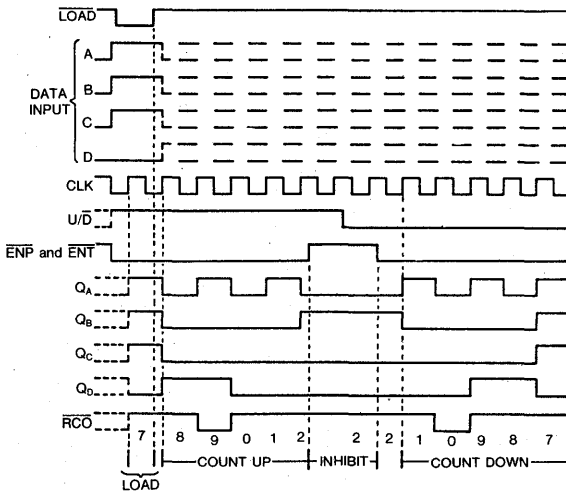
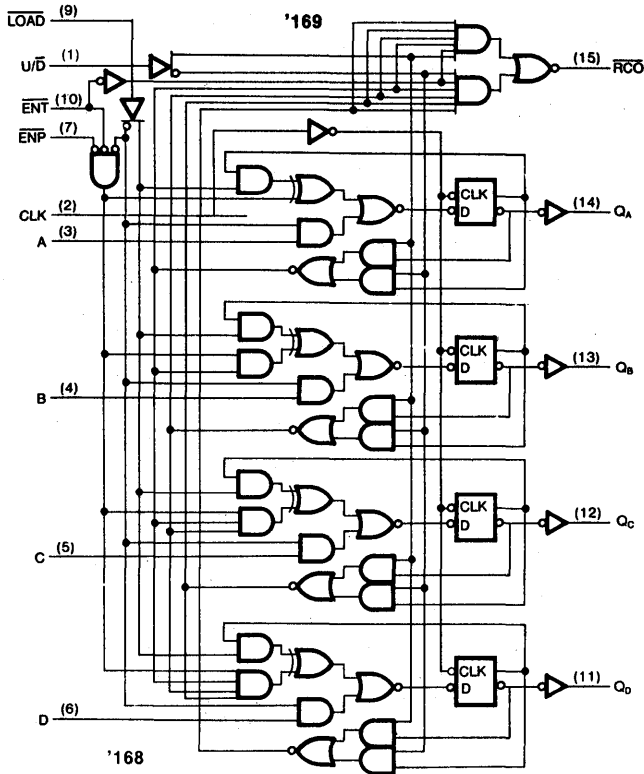
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

LOGIC DIAGRAMS

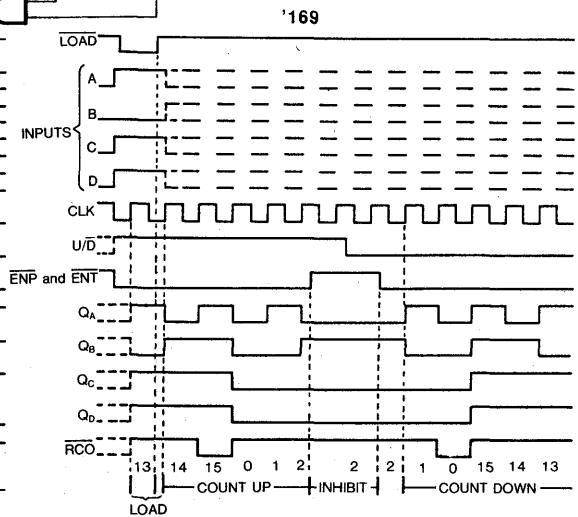


**LOGIC DIAGRAMS** (continued)



Illustrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



Illustrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

**FUNCTION TABLE**

OPERATING MODE	INPUTS						OUTPUTS	
	CLK	U/D	ENP	ENT	LOAD	D <sub>n</sub>	Q <sub>n</sub>	RCO
Parallel Load	↑	X	X	X	l	i	L	(1)
	↑	X	X	X	i	h	H	(1)
Count Up	↑	h	l	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold	↑	X	h	X	h	X	q <sub>n</sub>	(1)
	↑	X	X	h	h	X	q <sub>n</sub>	H

H=HIGH voltage level steady state

h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L=LOW voltage level steady state

l=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X=Don't care

q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑=LOW-to-HIGH clock transition

**NOTE:**

1. The RCO is LOW when ENT is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.

The RCO is LOW when ENT is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

**4**

**Absolute Maximum Ratings\***

Supply Voltage Range V<sub>CC</sub> . . . . . -0.5V to +7V

DC Input Diode Current, I<sub>IK</sub>  
 (V<sub>I</sub> < -0.5V or V<sub>I</sub> > V<sub>CC</sub> +0.5V) . . . . . ±20 mA

DC Output Diode Current, I<sub>OK</sub>  
 (V<sub>O</sub> < -0.5V or V<sub>O</sub> > V<sub>CC</sub> +0.5V) . . . . . ±20 mA

Continuous Output Current Per Pin, I<sub>O</sub>  
 (-0.5V < V<sub>O</sub> < V<sub>CC</sub> +0.5V) . . . . . ±35 mA

Continuous Current Through  
 V<sub>CC</sub> or GND pins . . . . . ±125 mA

Storage Temperature Range, T<sub>stg</sub> . . . . . -65°C to +150°C

Power Dissipation Per Package, P<sub>d</sub>† . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . 4.5V to 5.5V

DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . . . 0V to V<sub>CC</sub>

Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT168, AHCT169)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	$f_{max}$		50	40		35		MHz
Propagation Delay, CLK to $\overline{RCO}$	$t_{PLH}$	$C_L = 50\text{pF}$	14		20		27	ns
	$t_{PHL}$		14		20		27	
Propagation Delay, CLK to Any Q	$t_{PLH}$		12		18		22	ns
	$t_{PHL}$		12		18		22	
Propagation Delay, $\overline{ENT}$ to $\overline{RCO}$	$t_{PLH}$		10		16		19	ns
	$t_{PHL}$		10		16		19	
Propagation Delay, $U/\overline{D}$ to $\overline{RCO}$	$t_{PLH}$		13		19		24	ns
	$t_{PHL}$		13		19		24	
Pulse Duration, CLK high or low	$t_w$			8	12		15	ns
Setup Time, Before CLK†	A, B, C or D			9	15		20	ns
	$\overline{ENP}$ or $\overline{ENT}$		9	15		15		
	LOAD		9	15		20		
	$U/\overline{D}$		9	15		20		
Hold Time, Data after CLK†	$t_h$		0	0		0	ns	
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$						pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT 173 KS74AHCT 4-Bit D-Type Registers with 3-State Outputs

## FEATURES

- Gated output control lines for enabling or disabling the outputs
- Fully independent clock for operation in parallel-load or hold modes
- For application as bus buffer registers
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components.

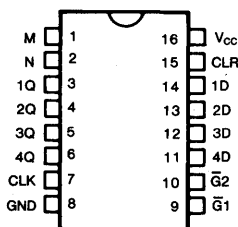
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION



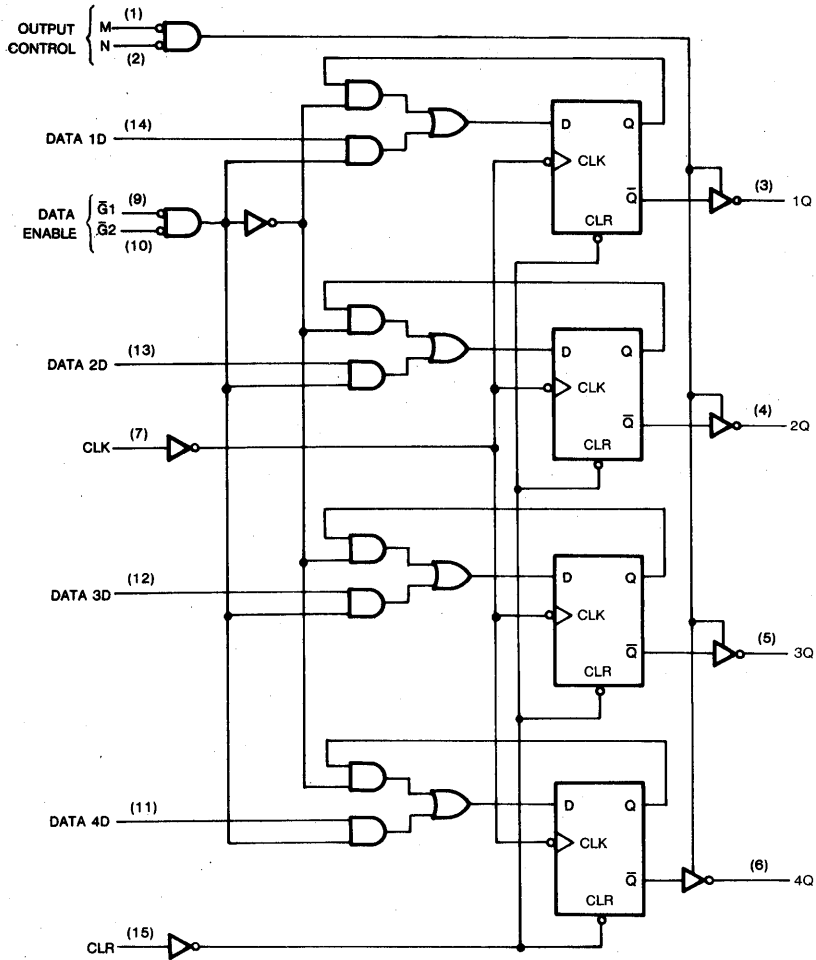
## FUNCTION TABLE

CLR	CLK	Input			Output Q
		Data Enable		Data	
		$\bar{G}1$	$\bar{G}2$	D	
H	X	X	X	X	L
L	L	X	X	X	$Q_0$
L	$\uparrow$	H	X	X	$Q_0$
L	$\uparrow$	X	H	X	$Q_0$
L	$\uparrow$	L	L	L	L
L	$\uparrow$	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

**KS54AHCT 173** 4-Bit D-Type Registers with 3-State Outputs  
**KS74AHCT**

**LOGIC DIAGRAM**



# KS54AHCT 173 4-Bit D-Type Registers with 3-State Outputs

## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature

Range  
 KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Min	Min	Max	Min	Max	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

4



# KS54AHCT 173 4-Bit D-Type Registers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT173

Characteristic	Symbol	Conditions†	KS74AHCT			KS54AHCT		Unit
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$		50	30		25		MHz
Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31	
Propagation Delay, CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		25 30		30 36	ns
Output Enable Time, M or N to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15	20 25		24 30	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15	20 25		24 30	
Output Disable Time, M or N to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega, C_L = 50\text{pF}$		10	17		20	ns
	$t_{PLZ}$			10	17		20	
Pulse Width	CLK High or Low	$t_w$		7	12		15	ns
	CLR High			7	12		15	
Setup Time, before CLK†	$\bar{G}1$ and $\bar{G}2$	$t_{su}$		8	15		20	ns
	Data			7	12		15	
	CLR Inactive			7	12		15	
Hold Time After CLK†	$\bar{G}1$ and $\bar{G}2$	$t_h$		-3	0		0	ns
	Data			-3	0		0	
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

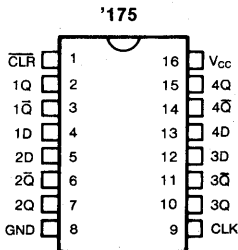
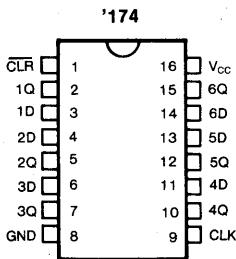
The '174 contains six, and the '175 contains four D-type flip-flops all sharing a common clock and a common clear. The '174 features single nail outputs for every flip-flop whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATIONS**



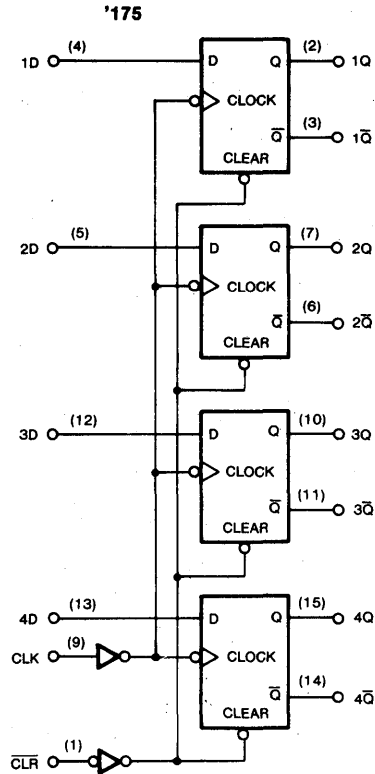
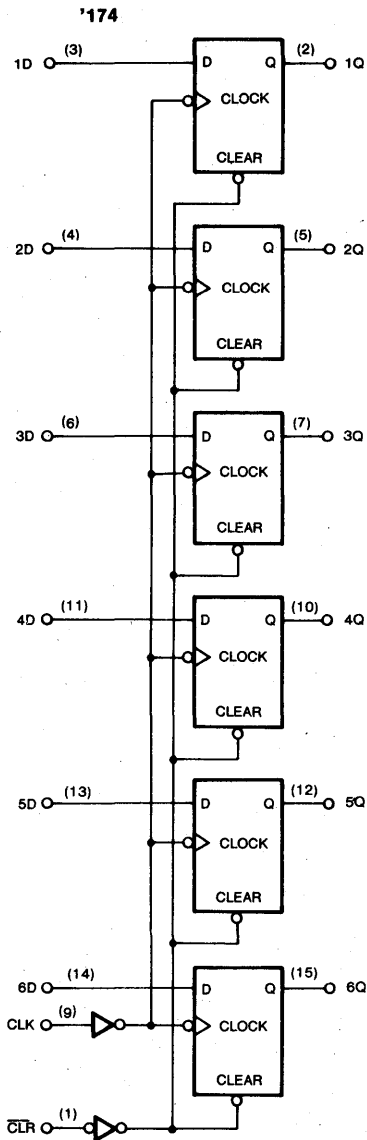
**FUNCTION TABLE**

(Each Flip-Flop)

Inputs			Outputs	
CLR	CLK	D	Q	Q <sup>†</sup>
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q <sub>0</sub>	Q <sub>0</sub>

† '175 only

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C  
Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT174, AHCT175

Characteristic	Symbol	Conditions†	T <sub>A</sub> = 25°C	KS74AHCT		KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	70	50		40		MHz
Propagation Delay, CLK to Q or $\bar{Q}$	t <sub>PLH</sub>		11		17		20	ns
	t <sub>PHL</sub>		11		17		20	
Propagation Delay, CLR to Q or $\bar{Q}$	t <sub>PLH</sub>		12		21		25	ns
	t <sub>PHL</sub>	12		21		25		
Setup Time before CLK†	Data	t <sub>su</sub>	6	10		15		ns
	CLR Inactive		4	6		8		
Hold Time, Data after CLK†	t <sub>h</sub>		0	0		0		ns
Pulse Width	CLK High or Low	t <sub>w</sub>	6	10		15		ns
	CLR Low		6	10		15		
Input Capacitance	C <sub>IN</sub>		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

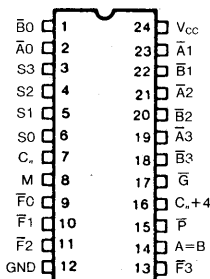
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Arithmetic operating modes:**
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus 12 other arithmetic operations
- **Logic function modes:**
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus 10 other logic operations
- **Full look-ahead for high-speed operations on long words**
- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:**  
I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

**PIN CONFIGURATION**



**DESCRIPTION**

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input(M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascade-outputs ( $\bar{P}$  and  $\bar{G}$ ) for the 4-bits in the package. When used in conjunction with AHCT182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input (C<sub>n</sub>) and a ripple-carry output (C<sub>n+4</sub>) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires and end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C<sub>n</sub>=H when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C<sub>n+4</sub>) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table 1)	$\bar{A}_0$	$\bar{B}_0$	$\bar{A}_1$	$\bar{B}_1$	$\bar{A}_2$	$\bar{B}_2$	$\bar{A}_3$	$\bar{B}_3$	$\bar{F}_0$	$\bar{F}_1$	$\bar{F}_2$	$\bar{F}_3$	C <sub>n</sub>	C <sub>n+4</sub>	$\bar{P}$	$\bar{G}$
Active-High Data (Table 2)	A <sub>0</sub>	B <sub>0</sub>	A <sub>1</sub>	B <sub>1</sub>	A <sub>2</sub>	B <sub>2</sub>	A <sub>3</sub>	B <sub>3</sub>	F <sub>0</sub>	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	$\bar{C}_n$	$\bar{C}_n+4$	X	Y



**ALU SIGNAL DESIGNATION**

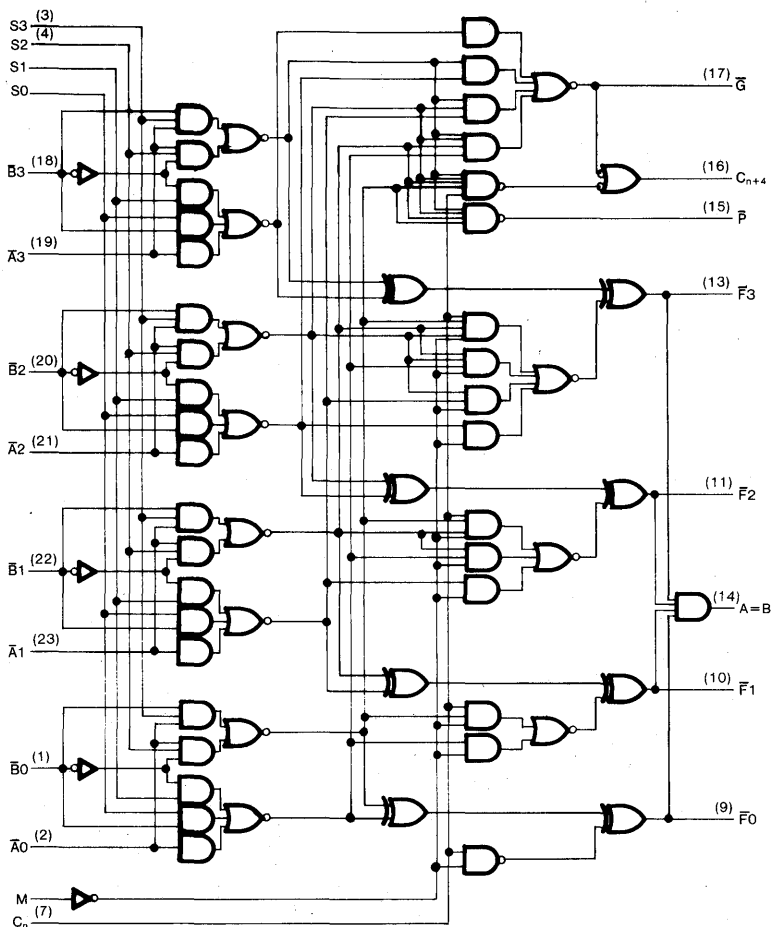
The '181 can be used with the signal designations. The logic functions and arithmetic operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels

allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



○ Table 1

Selection				Active-Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C <sub>n</sub> =L (no carry)	C <sub>n</sub> =H (with carry)
L	L	L	L	$F=\bar{A}$	F=A Minus 1	F=A
L	L	L	H	$F=\bar{A}\bar{B}$	F=AB Minus 1	F=AB
L	L	H	L	$F=\bar{A} + B$	F= $\bar{A}\bar{B}$ Minus 1	F= $\bar{A}\bar{B}$
L	L	H	H	F=1	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	$F=\bar{A} + \bar{B}$	F=A Plus (A + $\bar{B}$ )	F=A Plus (A + $\bar{B}$ ) Plus 1
L	H	L	H	$F=\bar{B}$	F=AB Plus (A + $\bar{B}$ )	F=AB Plus (A + $\bar{B}$ ) Plus 1
L	H	H	L	$F=\bar{A} \oplus \bar{B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	$F=A + \bar{B}$	F=A + B	F=(A + $\bar{B}$ ) Plus 1
H	L	L	L	$F=\bar{A}B$	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
H	L	L	H	$F=A \oplus B$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F= $\bar{A}\bar{B}$ Plus (A + B)	F= $\bar{A}\bar{B}$ Plus (A + B) Plus 1
H	L	H	H	$F=A + B$	F=(A + B)	F=(A + B) Plus 1*
H	H	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	$F=\bar{A}\bar{B}$	F=AB Plus A	F=AB Plus A Plus 1
H	H	H	L	$F=AB$	F= $\bar{A}\bar{B}$ Plus A	F= $\bar{A}\bar{B}$ Plus A Plus 1
H	H	H	H	F=A	F=A	F=A Plus 1

○ Table 2

Selection				Active-High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C <sub>n</sub> =L (no carry)	C <sub>n</sub> =H (with carry)
L	L	L	L	$F=\bar{A}$	F=A	F=A Plus 1
L	L	L	H	$F=\bar{A} + \bar{B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	$F=\bar{A}B$	F=A + $\bar{B}$	F=(A + $\bar{B}$ ) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	$F=\bar{A}\bar{B}$	F=A Plus $\bar{A}\bar{B}$	F=A Plus $\bar{A}\bar{B}$ Plus 1
L	H	L	H	$F=\bar{B}$	F=(A + B) Plus $\bar{A}\bar{B}$	F=(A + B) Plus $\bar{A}\bar{B}$ Plus 1
L	H	H	L	$F=\bar{A} \oplus \bar{B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	$F=\bar{A}\bar{B}$	F= $\bar{A}\bar{B}$ Minus 1	F= $\bar{A}\bar{B}$
H	L	L	L	$F=\bar{A} + B$	F=A Plus $\bar{A}B$	F=A Plus $\bar{A}B$ Plus 1
H	L	L	H	$F=\bar{A} \oplus B$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\bar{B}$ ) Plus $\bar{A}B$	F=(A + $\bar{B}$ ) Plus $\bar{A}B$ Plus 1
H	L	H	H	$F=AB$	F= $\bar{A}B$ Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	$F=A + \bar{B}$	F=(A + B) Plus A	F=(A + B) Plus A Plus 1
H	H	H	L	$F=A + B$	F=(A + $\bar{B}$ ) Plus A	F=(A + $\bar{B}$ ) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

\* Each bit is shifted to the next more significant position



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

INPUT PAIRS HIGH/NOT HIGH TEST TABLE  
FUNCTION INPUTS:  $S_2 = M = 4.5 \text{ V}$ ,  $S_0 = S_1 = S_3 = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ , $C_n$	Remaining $\bar{B}$	$\bar{P}$	In-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{B}$ , $C_n$	Remaining $\bar{A}$	$\bar{P}$	In-Phase
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ , $C_n$	Remaining $\bar{B}$	$C_n+4$	Out-of-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{B}$ , $C_n$	Remaining $\bar{A}$	$C_n+4$	Out-of-Phase

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE  
FUNCTION INPUTS:  $S_0 = S_3 = 4.5 \text{ V}$ ,  $S_1 = S_2 = M = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	$C_n$	$\bar{F}_i$	In-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	$C_n$	$\bar{F}_i$	In-Phase
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , $C_n$	$\bar{P}$	In-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , $C_n$	$\bar{P}$	In-Phase
$t_{PLH}$	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$\bar{G}$	In-Phase
$t_{PHL}$	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$\bar{G}$	In-Phase
$t_{PLH}$	$C_n$	None	None	All $\bar{A}$	All $\bar{B}$	Any $\bar{F}$ or $C_n+4$	In-Phase
$t_{PHL}$	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$C_n+4$	Out-of-Phase
$t_{PHL}$	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$C_n+4$	Out-of-Phase

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT181

Characteristic	Symbol	Conditions†  $C_L = 50\text{pF}$	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Propagation Delay, $C_n$ to $C_{n+4}$	$t_{PLH}$	M=0V,	8		14		17	ns	
	$t_{PHL}$	Sum or Diff Mode	8		14		17		
Propagation Delay, $\bar{A}$ or $\bar{B}$ to $C_{n+4}$	$t_{PLH}$	M=S1=S2=0V	16		24		29	ns	
	$t_{PHL}$	S0=S3=4.5V	16		24		29		
Propagation Delay, $\bar{A}$ or $\bar{B}$ to $C_{n+4}$	$t_{PLH}$	M=S0=S3=0V	17		25		30	ns	
	$t_{PHL}$	S1=S2=4.5V	17		25		30		
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{G}$	$t_{PLH}$	M=S1=S2=0V	17		25		30	ns	
	$t_{PHL}$	S0=S3=4.5V	17		25		30		
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{G}$	$t_{PLH}$	M=S0=S3=0V	17		25		30	ns	
	$t_{PHL}$	S1=S2=4.5V	17		25		30		
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{F}$	$t_{PLH}$	M=S0=S3=0V	15		23		27	ns	
	$t_{PHL}$	S1=S2=4.5V	15		23		27		
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{F}$	$t_{PLH}$	M=S1=S2=0V	16		24		29	ns	
	$t_{PHL}$	S0=S3=4.5V	16		24		29		
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{F}_i$	$t_{PLH}$	M=S1=S2=0V	20		29		35	ns	
	$t_{PHL}$	S0=S3=4.5V	20		29		35		
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{F}_i$	$t_{PLH}$	M=S0=S3=0V	19		27		32	ns	
	$t_{PHL}$	S1=S2=4.5V	19		27		32		
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{F}_i$	$t_{PLH}$	M=4.5V	16		24		29	ns	
	$t_{PHL}$		16		24		29		
Propagation Delay $\bar{A}$ or $\bar{B}$ to A=B	$t_{PLZ}$	M=S0=S3=0V	19		27		32	ns	
	$t_{PZL}$	S1=S2=4.5V	16		24		29		
Propagation Delay $C_n$ to any F	$t_{PLH}$		15		23		24	ns	
	$t_{PHL}$		15		23		27		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE  
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	$\bar{F}_i$	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	$\bar{F}_i$	Out-of-Phase
t <sub>PHL</sub>							

INPUT BITS EQUAL/NOT EQUAL TEST TABLE  
FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	Out-of-Phase
t <sub>PHL</sub>							

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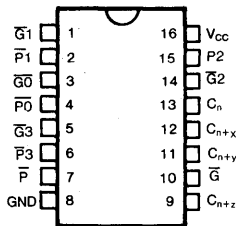
DIFF MODE TEST TABLE  
FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$	In-Phase
t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$	Out-of-Phase
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{P}$	In-Phase
t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{P}$	Out-of-Phase
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{G}$	In-Phase
t <sub>PHL</sub>	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{G}$	Out-of-Phase
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	A=B	In-Phase
t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	A=B	Out-of-Phase
t <sub>PLH</sub>	C <sub>n</sub>	None	None	All $\bar{A}$ and $\bar{B}$	None	C <sub>n</sub> +4 or any $\bar{F}$	In-Phase
t <sub>PHL</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	C <sub>n</sub> +4	Out-of-Phase
t <sub>PLH</sub>	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}, \bar{B}, C_n$	C <sub>n</sub> +4	In-Phase

**FEATURES**

- Compatible Carry Functions for direct ALU connection
- Cascadable to perform look-ahead across n-bit adders.
- High output current drive:  $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Low power consumption characteristic of CMOS
- Direct interface capability to TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**PIN DESIGNATIONS**

Designation	Pin No	Function
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3, 1, 14, 5	Active Low Carry Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4, 2, 15, 6	Active Low Carry Propagate Inputs
$C_n$	13	Carry Input, Active HIGH
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Carry Outputs
$\overline{G}$	10	Active Low Carry Generate Output
$\overline{P}$	7	Active Low Carry Propagate Output
$V_{cc}$	16	Supply Voltage
$GND$	8	Ground

**DESCRIPTION**

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 182 are:

$$C_{n+x} = G0 + P0 C_n$$

$$C_{n+y} = G1 + P1 G0 + P1 P0 C_n$$

$$C_{n+z} = G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 C_n$$

$$\overline{G} = \overline{G3} + P3 G2 + P3 P2 G1 + P3 P2 P1 G0$$

$$\overline{P} = P3 P2 P1 P0$$



FUNCTION TABLES

FOR  $\bar{G}$  OUTPUT

INPUTS							OUTPUT $\bar{G}$
$\bar{G}_3$	$\bar{G}_2$	$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_3$	$\bar{P}_2$	$\bar{P}_1$	
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR  $\bar{P}$  OUTPUT

INPUTS				OUTPUT $\bar{P}$
$\bar{P}_3$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	
L	L	L	L	L
All other combinations				H

FOR  $C_{n+x}$  OUTPUT

INPUTS			OUTPUT $C_{n+x}$
$\bar{G}_0$	$\bar{P}_0$	$C_n$	
L	X	X	H
X	L	H	H
All other combinations			L

$C_{n+y}$  OUTPUT

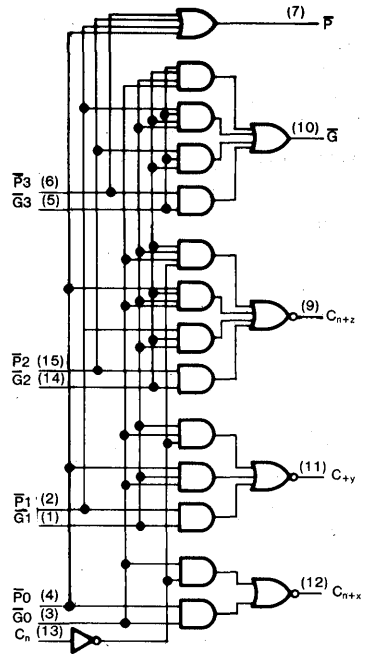
INPUTS					OUTPUT $C_{n+y}$
$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_1$	$\bar{P}_0$	$C_n$	
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

$C_{n+z}$  OUTPUT

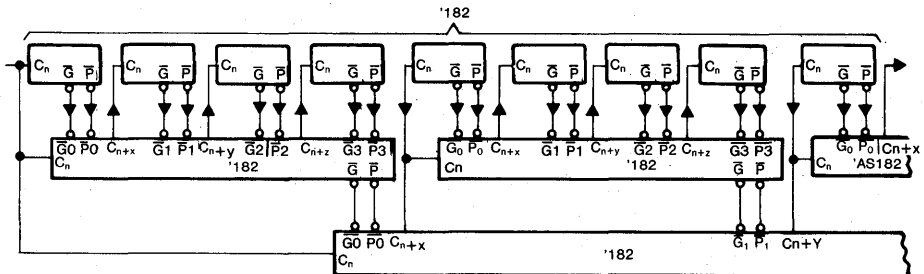
INPUTS							OUTPUT $C_{n+z}$
$\bar{G}_2$	$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	$C_n$	
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = don't care  
Any inputs not shown in a given table are don't care with respect to that output.

LOGIC DIAGRAM



Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 (-0.5V <  $V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT182

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay, $\bar{P}_i$ or $\bar{G}_i$ to $C_{n+x}C_{n+y}, C_{n+z}$	$t_{PLH}$	$C_L = 50\text{pF}$	12		20		24	ns
	$t_{PHL}$		12		20		24	
Propagation Delay, $\bar{P}_i$ or $\bar{G}_i$ to $\bar{G}$	$t_{PLH}$	$C_L = 50\text{pF}$	12		20		24	ns
	$t_{PHL}$		12		20		24	
Propagation Delay, $C_n$ to $C_{n+x}, C_{n+y}, C_{n+z}$	$t_{PLH}$	$C_L = 50\text{pF}$	15		21		26	ns
	$t_{PHL}$		15		21		26	
Propagation Delay $\bar{P}_i$ to $\bar{P}$	$t_{PLH}$	$C_L = 50\text{pF}$	11		18		21	ns
	$t_{PHL}$		11		18		21	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- For use in high-speed wallace-tree summing
- Fast addition operation
- Low power consumption characteristic of CMOS
- High output current drive:  $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

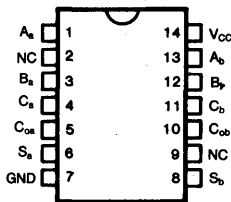
**DESCRIPTION**

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

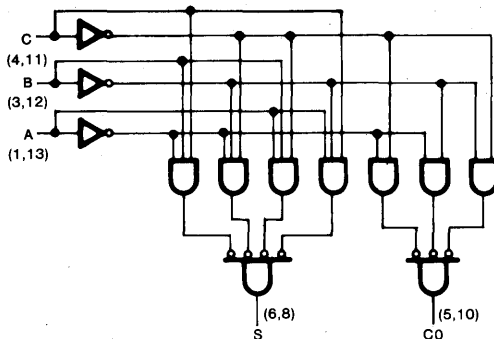
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**4**

**FUNCTION TABLE**

(Each Half)

Inputs			Output	
A	B	C	S	Co
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
L	L	H	H	L
H	H	L	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_D^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . .  $4.5V$  to  $5.5V$   
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . .  $0V$  to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), AHCT183

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC} = 5.0V$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L = 50pF$	10		15		18	ns	
	$t_{PHL}$		13		20		24		
Input Capacitance	$C_{IN}$		5					pF	
Power dissipation Capacitance*	$C_{PD}$							pF	

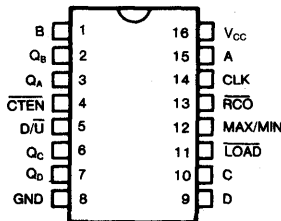
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Single down/up count control line
- Look-ahead circuit enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

OPERATING MODE	INPUTS				OUTPUTS	
	LOAD	D/U	CTEN	CLK	Input	$O_n$
parallel load	L	X	X	X	L	L
count up	H	L	↑	X	X	count up
count down	H	H	↓	X	X	count down
hold (do nothing)	H	X	H	X	X	no change

**RCO AND MAX/MIN FUNCTION TABLE**

INPUTS		TERMINAL COUNT STATE				OUTPUTS	
D/U	CTEN	QA	Qb	Qc	Qd	MAX/MIN	RCO
H	H	X	H	X	X	H	H
L	H	X	H	X	X	H	H
L	L	↓	H	X	X	H	↓
L	H	X	L	L	L	L	H
H	H	X	L	L	L	L	H
H	L	↓	L	L	L	L	↓

H = HIGH voltage level  
 L = LOW voltage level  
 ↓ = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition  
 X = Don't care  
 ↑ = LOW-to-HIGH CLK transition  
 ↓ = one LOW level pulse  
 ↓ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

**DESCRIPTION**

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (CTEN) is low. A high at CTEN inhibits counting. The direction of the count is determined by the level of the down/up (D/U) input. When D/U is low, the counter counts up and when D/U is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTEN and D/U) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

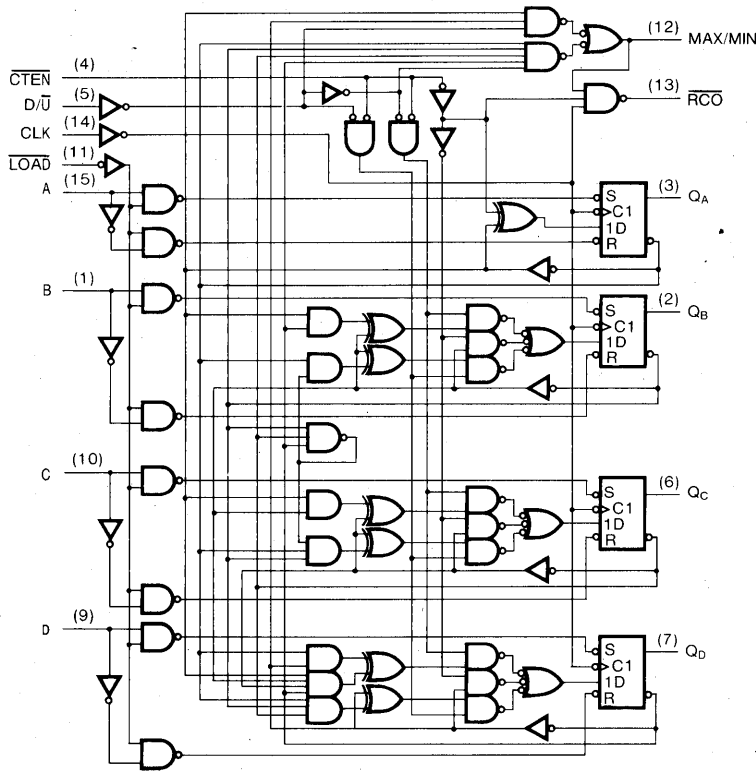
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

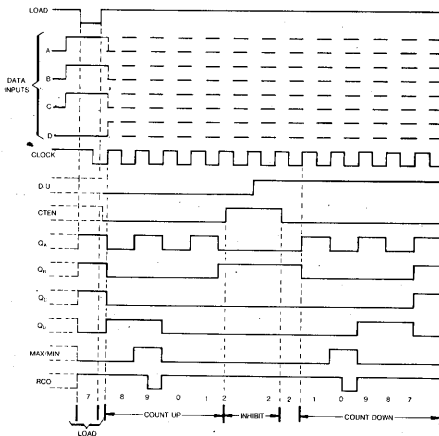
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.



**LOGIC DIAGRAM**



**Typical load, count, and inhibit sequences**



Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, nine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, eight, and seven

**NOTE A:** Clear overrides load data, and count inputs.

**NOTE B:** When count up, count-down input must be high; when counting down, countup input must be high.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
					$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT190

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	30		25		MHz
Propagation Delay, LOAD to any Q	$t_{PLH}$		18		30		36	ns
	$t_{PHL}$		18		30		36	
Propagation Delay, A,B,C, D to any Q	$t_{PLH}$		13		21		25	ns
	$t_{PHL}$		13		21		25	
Propagation Delay, CLK to $\overline{RCO}$	$t_{PLH}$		12		20		24	ns
	$t_{PHL}$		12		20		24	
Propagation Delay, CLK to any Q	$t_{PLH}$		11		18		22	ns
	$t_{PHL}$		11		18		22	
Propagation Delay, CLK to MAX/MIN	$t_{PLH}$		19		31		37	ns
	$t_{PHL}$		19		31		37	
Propagation Delay, D/ $\overline{U}$ to $\overline{RCO}$	$t_{PLH}$		19		32		38	ns
	$t_{PHL}$		19		32		38	
Propagation Delay, D/ $\overline{U}$ to MAX/MIN	$t_{PLH}$		15		25		30	
	$t_{PHL}$		15		25		30	
Propagation Delay, CTEN to $\overline{RCO}$	$t_{PLH}$	11		18		22	ns	
	$t_{PHL}$	11		18		22		
Pulse Width	CLK High or Low	$t_w$	10		17		20	ns
	LOAD Low		12		20		25	
Setup Time	Data before $\overline{LOAD}\uparrow$	$t_{su}$	10	17		20	ns	
	CTEN before $\text{CLK}\uparrow$		10	17		20		
	D/ $\overline{U}$ before $\text{CLK}\uparrow$		10	17		20		
	LOAD Inactive before $\text{CLK}\uparrow$		10	17		20		
Hold Time	Data after $\overline{LOAD}\uparrow$	$t_h$	2	4		5	ns	
	CTEN after $\text{CLK}\uparrow$		0	0		0		
	D/ $\overline{U}$ after $\text{CLK}\uparrow$		0	0		0		
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$		80				pF	

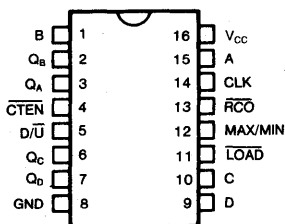
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	LOAD	D/U	CTEN	CLK	Input	$Q_n$
parallel load	L	X	X	X	L	L
count up	H	L	I	↑	X	count up
count down	H	H	I	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

RCO AND MAX/MIN FUNCTION TABLE

INPUTS		TERMINAL COUNT STATE					OUTPUTS	
D/U	CTEN	CLK	$Q_A$	$Q_B$	$Q_C$	$Q_D$	MAX/MIN	RCO
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	↑	H	X	X	H	↓	↑
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	L	H
H	L	↑	L	L	L	L	↓	↑

- H = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- ↑ = LOW-to-HIGH CLK transition
- ↓ = one LOW level pulse
- ↘ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

DESCRIPTION

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (CTEN) is low. A high at CTEN inhibits counting. The direction of the count is determined by the level of the down/up (D/U) input. When D/U is low, the counter counts up and when D/U is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTEN and D/U) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

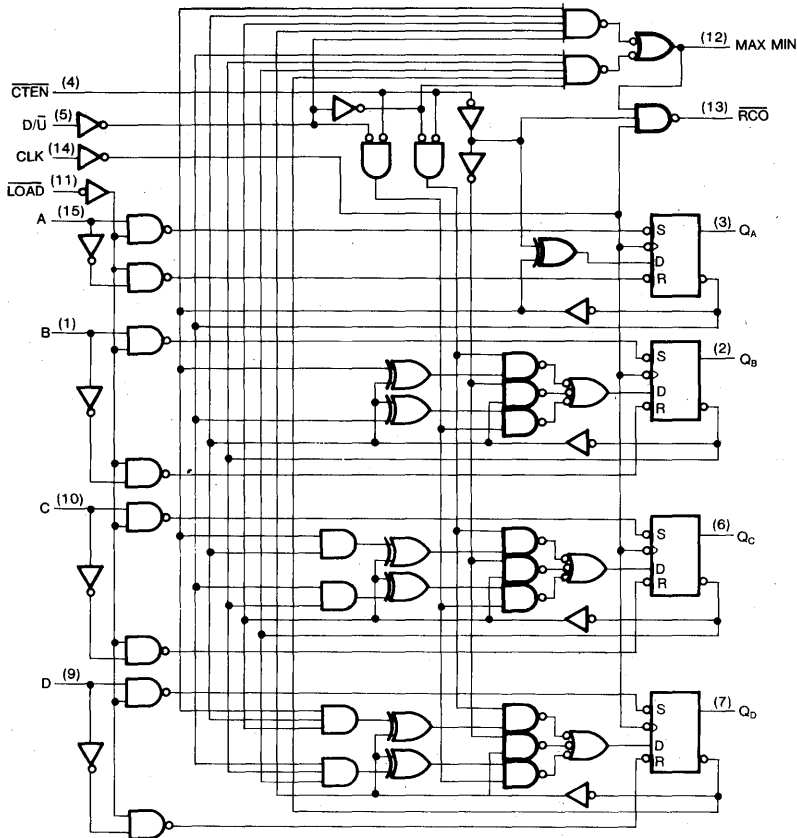
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

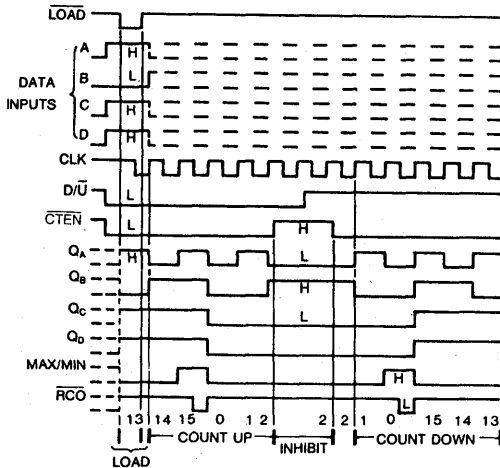
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.



**LOGIC DIAGRAM**



**Typical Load, Count, and Inhibit Sequence**



- Sequence:  
 (1) Load (preset) to binary thirteen.  
 (2) Count up to fourteen, fifteen, zero, one, and two.  
 (3) Inhibit.  
 (4) Count down to one, zero, fifteen, fourteen, and thirteen.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT191

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit	
			$V_{CC} = 5.0\text{V}$	$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	30		25		MHz	
Propagation Delay, LOAD to any Q	$t_{PLH}$		18		30		36		ns
	$t_{PHL}$		18		30		36		
Propagation Delay, A,B,C, D to any Q	$t_{PLH}$		13		21		25		ns
	$t_{PHL}$		13		21		25		
Propagation Delay, CLK to $\overline{RCO}$	$t_{PLH}$		12		20		24		ns
	$t_{PHL}$		12		20		24		
Propagation Delay, CLK to any Q	$t_{PLH}$		11		18		22		ns
	$t_{PHL}$		11		18		22		
Propagation Delay, CLK to MAX/MIN	$t_{PLH}$		19		31		37		ns
	$t_{PHL}$		19		31		37		
Propagation Delay, D/ $\overline{U}$ to $\overline{RCO}$	$t_{PLH}$		19		32		38		ns
	$t_{PHL}$		19		32		38		
Propagation Delay, D/ $\overline{U}$ to MAX/MIN	$t_{PLH}$		15		25		30		
	$t_{PHL}$		15		25		30		
Propagation Delay, CTEN to $\overline{RCO}$	$t_{PLH}$		11		18		22		ns
	$t_{PHL}$	11		18		22			
Pulse Width	CLK High or Low	$t_w$	10		17		20	ns	
	LOAD Low		12		20		25		
Setup Time	Data before $\overline{LOAD}\uparrow$	$t_{su}$	10	17		20		ns	
	$\overline{CTEN}$ before $\text{CLK}\uparrow$		10	17		20			
	D/ $\overline{U}$ before $\text{CLK}\uparrow$		10	17		20			
	LOAD Inactive before $\text{CLK}\uparrow$		10	17		20			
Hold Time	Data after $\overline{LOAD}\uparrow$	$t_h$	2	4		5		ns	
	$\overline{CTEN}$ after $\text{CLK}\uparrow$		0	0		0			
	D/ $\overline{U}$ after $\text{CLK}\uparrow$		0	0		0			
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$		80					pF	

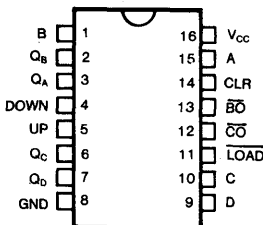
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Look-ahead circuit enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

OPERATING MODE	INPUTS								OUTPUTS					
	CLR	LOAD	UP	DOWN	A	B	C	D	QA	QB	QC	QD	CO	BO
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	A	B	C	D	L	H
	L	L	H	X	H	X	X	H	A	B	C	D	H	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X		count down				H	H**

\* CO=Up at terminal count up (HHHH)

\*\* BO=Down at terminal count down (LLLL)

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW to HIGH clock transition

**DESCRIPTION**

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

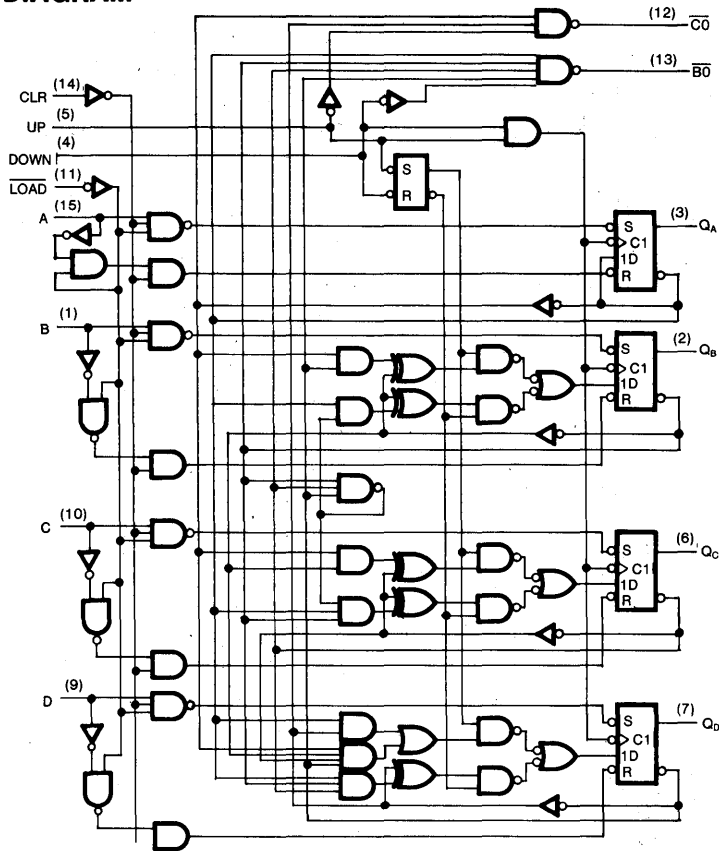
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (CO) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

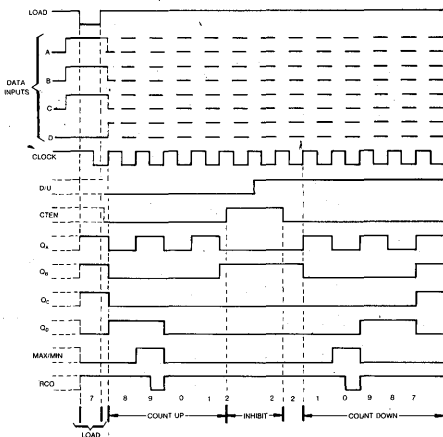
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.



LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, nine (maximum), zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, eight, and seven

**NOTE A:** Clear overrides load data, and count inputs.

**NOTE B:** When count up, count-down input must be high; when counting down, countup input must be high.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND).

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT		KS54AHCT		Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	160.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT 192

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C	KS74AHCT			KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%			T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	50	30		25		MHz	
Propagation Delay, UP to $\bar{C}O$	t <sub>PLH</sub>		11		18		22		ns
	t <sub>PHL</sub>		11		18		22		
Propagation Delay, DOWN to any Q	t <sub>PLH</sub>		11		18		22		ns
	t <sub>PHL</sub>		11		18		22		
Propagation Delay, UP or DOWN to any Q	t <sub>PLH</sub>		11		19		23		ns
	t <sub>PHL</sub>		11		19		23		
Propagation Delay, LOAD to any Q	t <sub>PLH</sub>		17		29		35		ns
	t <sub>PHL</sub>		17		29		35		
Propagation Delay, CLR to any Q	t <sub>PLH</sub>		10		17		20		ns
Pulse Width	CLR High	t <sub>w</sub>	6	10		15		ns	
	LOAD Low		10	17		20			
	UP or DOWN High or Low		10	17		20			
Setup Time	Data before $\overline{LOAD}\dagger$	t <sub>su</sub>	10	17		29		ns	
	CLR Inactive before UP† or DOWN†		10	17		20			
	LOAD Inactive before UP† or DOWN†		10	17		20			
	UP high before DOWN†		10	17		17			
	Down high before UP†		8	15		15			
Hold Time	Data after $\overline{LOAD}\dagger$	t <sub>h</sub>	0	0		0		ns	
	UP High after DOWN†		0	0		0			
	DOWN High after UP†		3	8		6			
Input Capacitance	C <sub>IN</sub>		5					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>		80						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

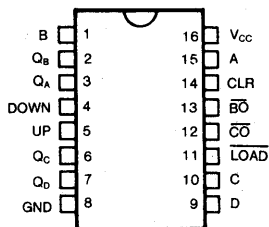
A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ( $\overline{BO}$ ) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ( $\overline{CO}$ ) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**FUNCTION TABLE**

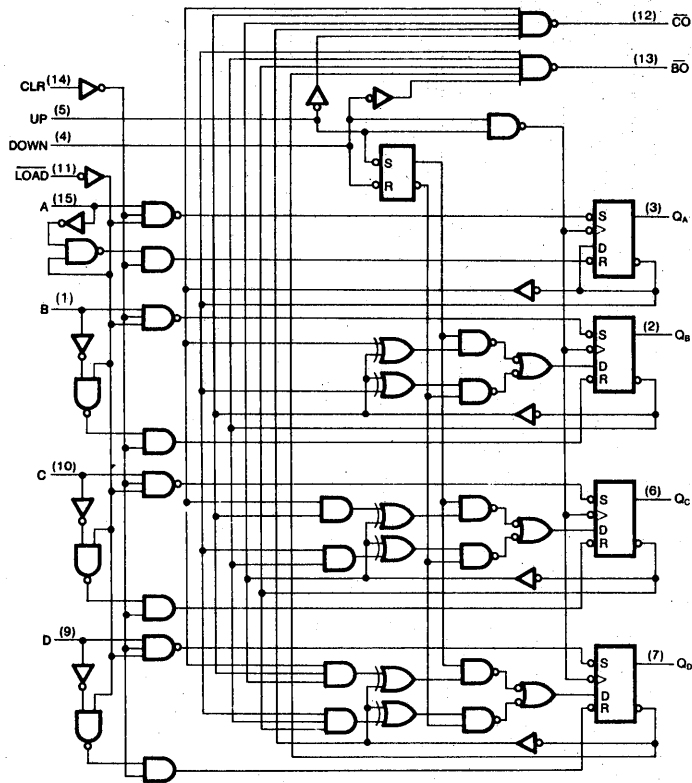
OPERATING MODE	INPUTS								OUTPUTS					
	CLR	LOAD	UP	DOWN	A	B	C	D	QA	QB	QC	QD	CO	BO
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X		count down				H	H**

H= HIGH voltage level      ↑ = LOW-to-HIGH clock transition  
 L= LOW voltage level      \*  $\overline{CO}$  = UP at terminal count up (HHHH)  
 X= don't care                \*\*  $\overline{BO}$  = DOWN at terminal count down (LLLL)

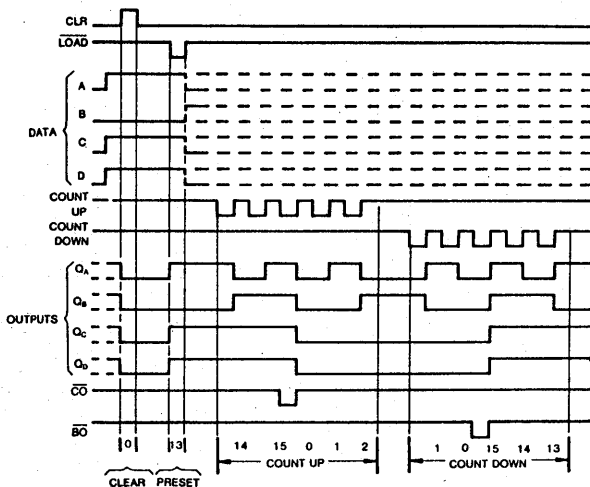




LOGIC DIAGRAM



Typical Clear, Load, and Count Sequences



Sequence:

- (1) Clear outputs to zero.
- (2) Load (preset) to binary thirteen.
- (3) Count up to fourteen, fifteen, carry, zero, one and two.
- (4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

**Note A:** Clear overrides load data, and count inputs.

**Note B:** When counting up, count-down input must be high; when counting down, count-up input must be high.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT193)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	30		25		MHz	
Propagation Delay, UP to $\overline{CO}$	$t_{PLH}$		11		18		22		ns
	$t_{PHL}$		11		18		22		ns
Propagation Delay, DOWN to any Q	$t_{PLH}$		11		18		22		ns
	$t_{PHL}$		11		18		22		ns
Propagation Delay, UP or DOWN to any Q	$t_{PLH}$		11		19		23		ns
	$t_{PHL}$		11		19		23		ns
Propagation Delay, LOAD to any Q	$t_{PLH}$		17		29		35		ns
	$t_{PHL}$		17		29		35		ns
Propagation Delay, CLR to any Q	$t_{PLH}$		10		17		20		ns
Pulse Width	CLR High	$t_w$	6	10		15		ns	
	$\overline{LOAD}$ Low		10	17		20			
	UP or DOWN High or Low		10	17		20			
Setup Time	Data before $\overline{LOAD}\dagger$	$t_{su}$	10	17		29		ns	
	CLR Inactive before $UP\dagger$ or $DOWN\dagger$		10	17		20			
	$\overline{LOAD}$ Inactive before $UP\dagger$ or $DOWN\dagger$		10	17		20			
	UP high before $DOWN\dagger$		10	17		17			
	Down high before $UP\dagger$		8	15		15			
Hold Time	Data after $\overline{LOAD}\dagger$	$t_h$	0	0		0		ns	
	UP High after $DOWN\dagger$		0	0		0			
	DOWN High after $UP\dagger$		3	8		6			
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$		80					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data Latching Capability
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

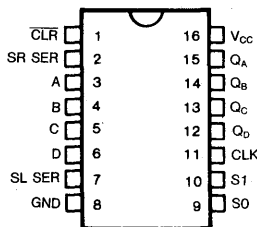
- Inhibit clock (temporary data latch/do nothing)
- Shift-right (in the direction  $Q_A$  toward  $Q_D$ )
- Shift-left (in the direction  $Q_D$  toward  $Q_A$ )
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.



**PIN CONFIGURATION**

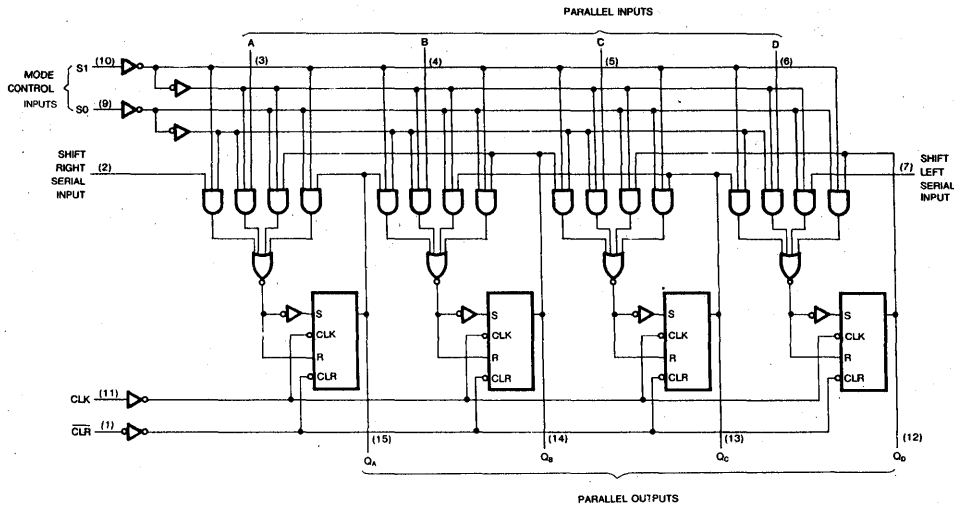


**FUNCTION TABLE**

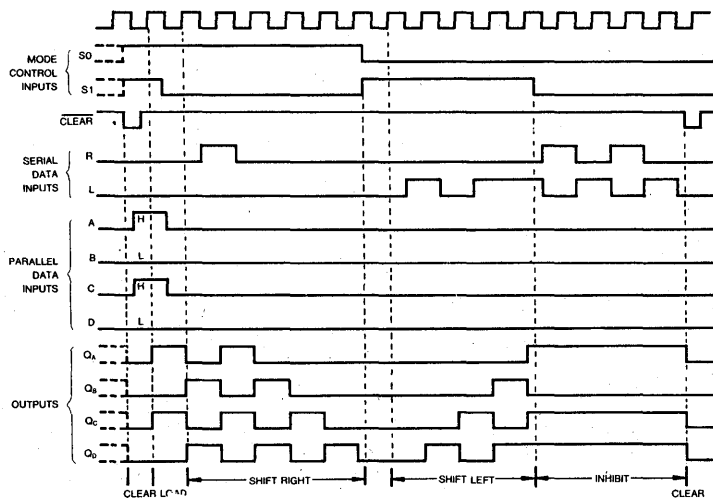
CLR	MODE		INPUTS				OUTPUTS						
	S1	S0	CLK	SERIAL		PARALLEL		QA	QB	QC	QD		
				LEFT	RIGHT	A	B					C	D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	H	L	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

H=high level (steady state)  
 L=low level (steady state)  
 X=irrelevant (any input, including transitions)  
 ↑=transition from low to high level  
 a,b,c,d=the level of steady-state input at inputs A,B,C, or D, respectively.  
 QA0, QB0, QC0, QD0=the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established.  
 QAn, QBn, QCn, QDn=the level of QA, QB, QC, respectively, before the most-recent ↑ transition of the clock.

**LOGIC DIAGRAM**



**typical clear, load, right-shift, inhibit, and clear sequences**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0		V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8		V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0		$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0		mA	

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT194

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT			KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	60	35		30		MHz	
Propagation Delay, CLK to $Q_H$	$t_{PLH}$		10		17		20	ns	
	$t_{PHL}$		10		17		20	ns	
Propagation Delay, CLR to $Q_H$	$t_{PHL}$		11		19		22	ns	
Pulse Width	CLR LOW	$t_w$	10	17		20		ns	
	CLK High or LOW		10	17		20			
Setup Time, Any Input before CLK†	$t_s$		10	17		20		ns	
Hold Time, Data after CLK†	$t_s$		-3	0		0		ns	
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$		80					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- J and K Inputs to First Stage
- Right-shift Only with Complementary Outputs on Last Stage
- Direct Overriding Clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

- Parallel (broadside) load
- Shift (in the direction  $A_A$  toward  $Q_D$ )

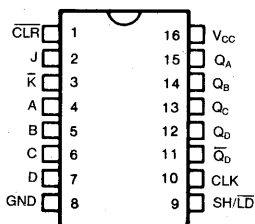
Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



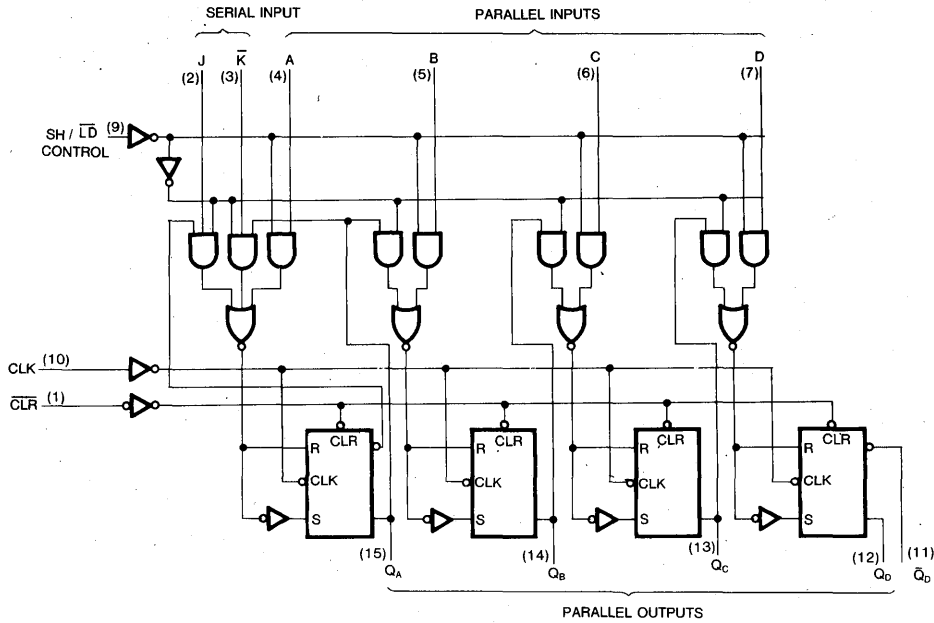
**FUNCTION TABLE**

INPUTS			OUTPUTS										
CLR	SH/LD	CLK	SERIAL		PARALLEL		QA	QB	QC	QD	QD-bar		
			J	K-bar	A	B						C	D
L	X	X	X	X	X	X	X	L	L	L	L	H	
H	L	↑	X	X	a	b	c	d	a	b	c	d	d-bar
H	H	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0	QD0-bar
H	H	↑	L	H	X	X	X	X	QA0	QA0	QBn	QCn	QCn-bar
H	H	↑	L	L	X	X	X	X	L	QA0	QBn	QCn	QCn-bar
H	H	↑	H	H	X	X	X	X	H	QA0	QBn	QCn	QCn-bar
H	H	↑	H	L	X	X	X	X	QA0	QA0	QBn	QCn	QCn-bar

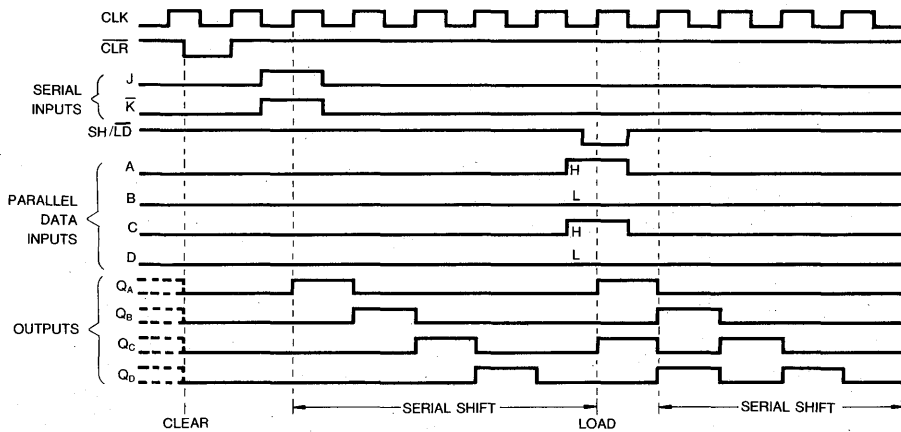
H=high level (steady state)  
 L=low level (steady state)  
 X=irrelevant (any input, including transitions)  
 ↑=transition from low to high level  
 a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.  
 QA0, QB0, QC0, QD0=the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established.  
 QA0, QBn, QCn=the level of QA, QB or QC, respectively, before the mostrecent transition of the clock.



**LOGIC DIAGRAMS**



**typical clear, shift, and load sequences**



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 35$ mA
Continuous Current Through	
$V_{CC}$ or GND pins	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	0V to $V_{CC}$
Operating Temperature	
Range	KS74AHCT: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54AHCT: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r, t_f$	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	Guaranteed Limits			
			$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	8.0	80.0	160.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT195

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	60	35		30		MHz
Propagation Delay, CLK to $Q_H$	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	
Propagation Delay, CLR to $Q_H$	$t_{PHL}$			11		19		22
Pulse Width	CLR Low	$t_w$	10	17		20		ns
	CLK High or Low		10	17		20		
Setup Time before CLK†	SH/LD High	$t_{su}$	10	17		20		ns
	Serial or Parallel Data		10	17		20		
	CLR inactive		10	17		20		
Hold Time after CLK†	SH/LD High		-3	0		0		ns
	Serial or Parallel Data		-3	0		0		
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

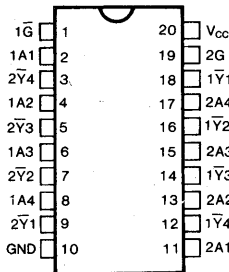
These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

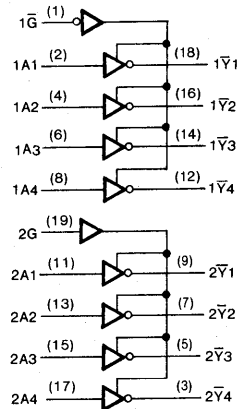
### PIN CONFIGURATION



### FUNCTION TABLE

Input		Output
$\bar{G}$	A	Y
L	L	H
L	H	L
H	X	Z

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT210

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	6		10		12	ns	
		$C_L = 150\text{pF}$	9		15		18		
	$t_{PHL}$	$C_L = 50\text{pF}$	7		10		12		
		$C_L = 150\text{pF}$	11		16		19		
Output Enable Time, Enable to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	12		20		24	ns
			$C_L = 150\text{pF}$	15		25		30	
	$t_{PZL}$		$C_L = 50\text{pF}$	12		20		24	
			$C_L = 150\text{pF}$	15		25		30	
Output Disable Time, Enable to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$		13		18		22	ns
			$C_L = 50\text{pF}$	13		18		22	
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}^*$	Output Disabled	5					pF	
		Output Enabled	30						

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems.
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

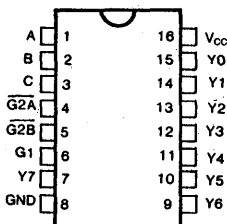
This conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**PIN CONFIGURATION**

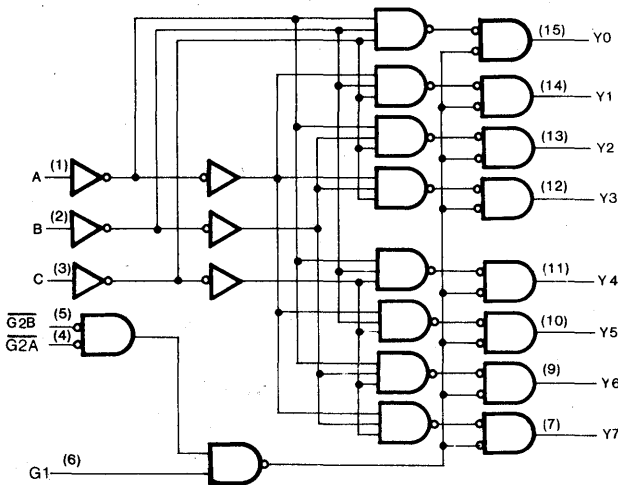


**FUNCTION TABLE**

Enable Inputs		Select Inputs			Outputs							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	H	L	L	L	L	L	H	L	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

\* G2 = G2A + G2B

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	-65°C to +150°C
Power Dissipation Per Package, $P_d$ <sup>†</sup> . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range . . . . .	KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$ . . . . .	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)





**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.33 0.5	0.1 0.4 0.5	0.1 0.4 0.5	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	80.0	160.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	2.9	3.0	3.0	$\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT238

Characteristic	Symbol	Conditions <sup>†</sup>	$T_A = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, A, B, C or Y	$t_{PLH}$	$C_L = 50\text{pF}$	12		20		24	ns
	$t_{PHL}$		12		20		24	
Propagation Delay, G1 to any Y	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	
Propagation Delay, G2A or G2B to any Y	$t_{PLH}$		10		17		20	ns
	$t_{PHL}$		10		17		20	
Input Capacitance	$C_{IN}$		5				$\text{pF}$	
Power Dissipation Capacitance*	$C_{PD}$		50				$\text{pF}$	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

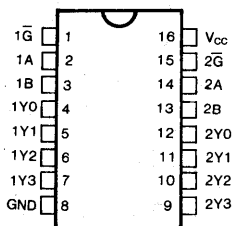
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times in high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

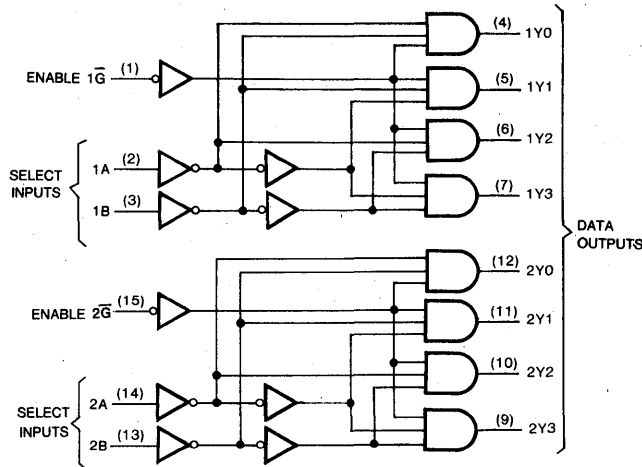
**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs			Outputs			
Enable	Select		Y0	Y1	Y2	Y3
$\bar{G}$	B	A				
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C			KS74AHCT T <sub>a</sub> = -40°C to +85°C		KS54AHCT T <sub>a</sub> = -55°C to +125°C		Unit
			Typ	Guaranteed Limits		Guaranteed Limits				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-4mA	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	V <sub>CC</sub> -0.1 3.7	V <sub>CC</sub> -0.1 3.7	V	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	0.1 0.4	V	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	±1.0	±1.0	μA	
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	80.0	160.0	160.0	μA	
Additional Worst Case Supply Current	ΔI <sub>CC</sub>	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	2.9	3.0	3.0	mA	

**4**

**AC ELECTRICAL CHARACTERISTICS** (Input t<sub>r</sub>, t<sub>r</sub> ≤ 2 ns), AHCT239

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C	KS74AHCT		KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	T <sub>a</sub> = -55°C to +125°C		
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	12		20		24	ns
	t <sub>PHL</sub>		12		20		24	
Propagation Delay, G̅ to any Y	t <sub>PLH</sub>		10		17		20	ns
	t <sub>PHL</sub>		10		17		20	
Input Capacitance	C <sub>IN</sub>		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>		50					pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT 240/241/244 Octal Buffers and Line Drivers with 3-State Outputs

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

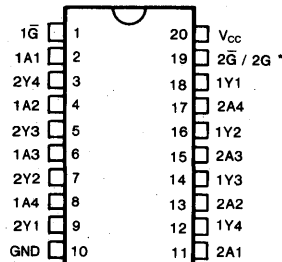
These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting/non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

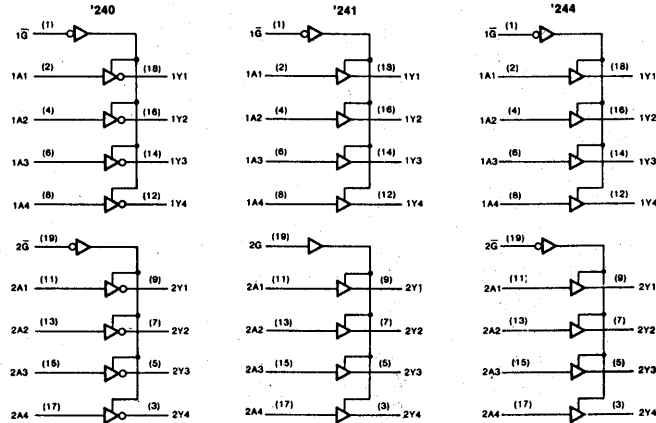
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION



\*2G for '240 and '244  
2G for '241

## LOGIC DIAGRAMS



## FUNCTION TABLE

Input			'241, '244	'240
			Output	Output
G	$\bar{G}$	A	Y	Y
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z

# KS54AHCT 240/241/244 Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$

# KS54AHCT 240/241/244 Octal Buffers and Line Drivers KS74AHCT with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns, AHCT240, AHCT241, AHCT244)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	6 9		10 15		12 18	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	6 9		10 15		12 18	
Output Enable Time, Enable to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		20 25	24 30	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		20 25	24 30	
Output Disable Time, Enable to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22	
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance*	$C_{PD}$	Output Disabled	5					pF
		Output Enabled	30					

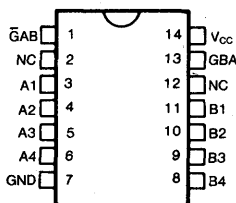
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- 2-Way Asynchronous Communication Between Data Buses
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

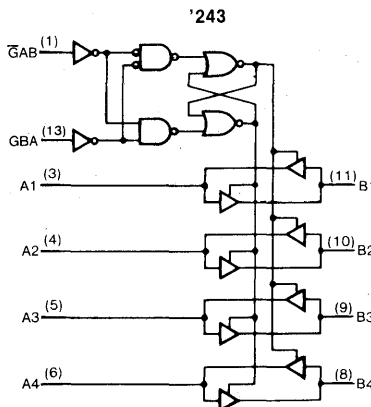
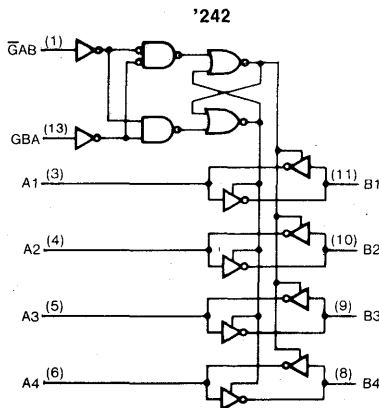
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

INPUTS		'242	'243
GAB	GBA		
L	L	$\bar{A}$ to B	A to B
H	H	B to A	B to A
H	L	Isolation	Isolation
L	H	Isolation	Isolation

**LOGIC DIAGRAMS**





### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 1.0\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT242, AHCT243

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay, A to B or B to A	t <sub>PLH</sub>	C <sub>L</sub> =50pF	7		11		15	ns
		C <sub>L</sub> =150pF	10		16		21	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF	7		11		15	
		C <sub>L</sub> =150pF	10		16		21	
Output Enable Time GAB to B, GBA to A	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF	12		20	25	ns
			C <sub>L</sub> =150pF	15		25	21	
	t <sub>PZL</sub>	C <sub>L</sub> =50pF	12		20		25	
		C <sub>L</sub> =150pF	15		25		21	
Output Disable Time, GAB to B, GBA to A	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ	12		20		25	ns
	t <sub>PLZ</sub>	C <sub>L</sub> =50pF	12		20		25	
Input Capacitance	C <sub>IN</sub>		5					pF
Output Capacitance	C <sub>OUT</sub>	Output Disabled	10					pF
Power Dissipation Capacitance*(per stage)	C <sub>PD</sub>	Output Enabled	30					pF
		Output Disabled	5					

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

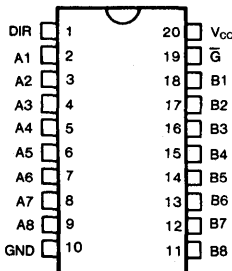
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ( $\bar{G}$ ) can be used to disable the device so that the buses are effectively isolated.

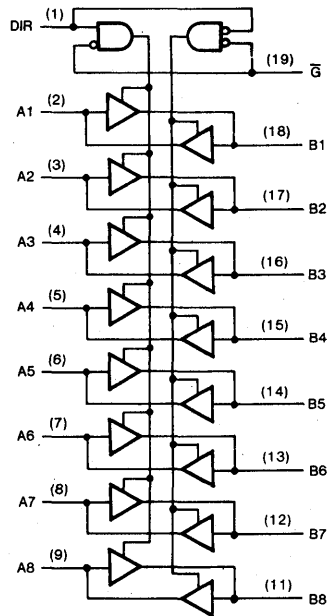
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs		Operation
$\bar{G}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_{d1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range  
 KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT		KS54AHCT		Unit
					$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$			
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V		
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V		
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$		
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$		
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$		
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA		

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT245

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to B or B to A	$t_{PLH}$	$C_L = 50\text{pF}$	7		11		14	ns
		$C_L = 150\text{pF}$	9		15		20	
	$t_{PHL}$	$C_L = 50\text{pF}$	7		10		14	ns
		$C_L = 150\text{pF}$	9		15		20	
Output Enable Time $\bar{G}$ to A or B	$t_{PZH}$	$C_L = 50\text{pF}$	12		20		25	ns
		$C_L = 150\text{pF}$	15		25		31	
	$t_{PZL}$	$R_L = 1\text{k}\Omega$						
		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 17		20 25		25 31	
Output Disable Time, $\bar{G}$ to A or B	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22	
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance*	$C_{PD}$	$\bar{G} = V_{CC}$ (per stage) $\bar{G} = \text{GND}$	5 30					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Three-State Version of '151
- Three-State Outputs Interface Directly with System Bus
- Performs Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

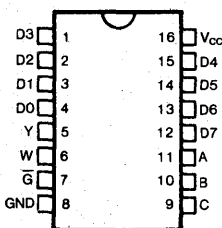
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ( $\bar{G}$ ). The outputs are disabled when  $\bar{G}$  is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

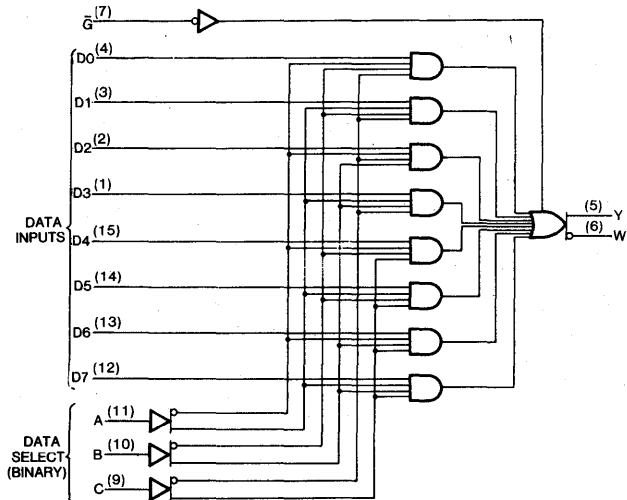
**PIN CONFIGURATION**



**FUNCTION TABLE**

INPUTS				OUTPUTS	
SELECT			STROBE $\bar{G}$	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\bar{D}0$
L	L	H	L	D1	$\bar{D}1$
L	H	L	L	D2	$\bar{D}2$
L	H	H	L	D3	$\bar{D}3$
H	L	L	L	D4	$\bar{D}4$
H	L	H	L	D5	$\bar{D}5$
H	H	L	L	D6	$\bar{D}6$
H	H	H	L	D7	$\bar{D}7$

**LOGIC DIAGRAM**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_i < -0.5V$  or  $V_i > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_o < -0.5V$  or  $V_o > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_o$   
 ( $-0.5V < V_o < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = -20\mu\text{A}$ $I_o = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = 20\mu\text{A}$ $I_o = 12\text{mA}$ $I_o = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$		$\pm 10.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0		160.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_i = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f < 2$  ns), AHCT251

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min		Max	
Propagation Delay, A, B or C to Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16		21 26		25 31		
Propagation Delay, A, B or C to W	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		24 29		27 33	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		24 29		27 33		
Propagation Delay, Any D to Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	9 12		15 20		18 24	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	9 12		15 20		18 24		
Propagation Delay, Any D to W	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		15 20		18 24	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		15 20		18 24		
Output Enable Time, $\bar{G}$ to Y or W	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	
Output Disable Time, $\bar{G}$ to Y or W	$t_{PHZ}$	$R_L = 1\text{k}\Omega$		13		18		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$		13		18		22	
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

4



**FEATURES**

- Three-State Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

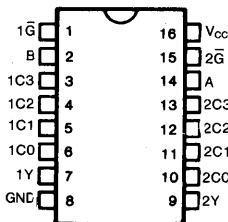
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ( $\bar{G}$ ). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



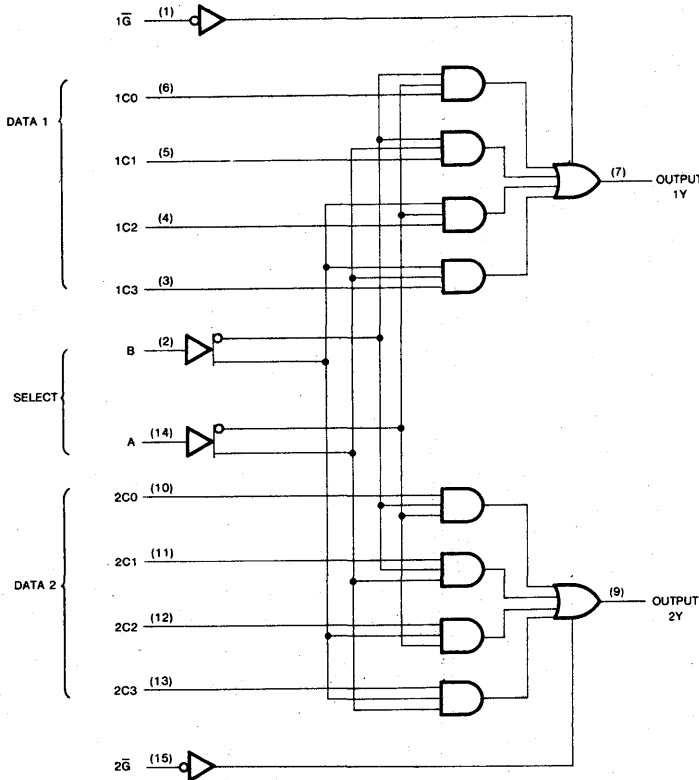
**FUNCTION TABLE**

SELECT		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

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 KS54AHCT, KS74AHCT  
 16-PIN DIP PACKAGE  
 16-PIN SOIC PACKAGE  
 16-PIN SSOP PACKAGE  
 16-PIN TSOP PACKAGE

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA
- Storage Temperature Range,  $T_{stg}$ , ..... -65°C to +150°C
- Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$
- Operating Temperature  
Range                      KS74AHCT: -40°C to +85°C  
                                  KS54AHCT: -55°C to +125°C
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits	Typ	Guaranteed Limits	Typ	Guaranteed Limits	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu\text{A}$	
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$		$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0		$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0		$\text{mA}$	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT253)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay, A or B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$	13		21		25	ns	
		$C_L = 150\text{pF}$	16		26		31		
Propagation Delay, Data (any C) to any Y	$t_{PHL}$	$C_L = 50\text{pF}$	13		21		25	ns	
		$C_L = 150\text{pF}$	16		26		31		
Output Enable Time G to Y	$t_{PZH}$	$C_L = 50\text{pF}$	10		16		19	ns	
		$C_L = 150\text{pF}$	13		21		35		
Output Disable Time, G to Y	$t_{PZL}$	$C_L = 50\text{pF}$	10		16		19	ns	
		$C_L = 150\text{pF}$	13		21		35		
Input Capacitance	$C_{IN}$	$R_L = 1\text{k}\Omega$	5					pF	
		$C_L = 50\text{pF}$							
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{IN}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54AHCT 257/258 Quad 2-Line to 1-Line Data Selector/ KS74AHCT Multiplexers with 3-State Outputs

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

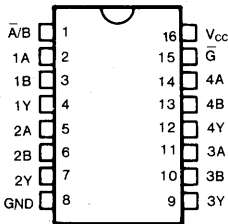
## DESCRIPTION

The '257 and '258 multiplex signals from four-bit data sources to four-output data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257, and inverted for the '258.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

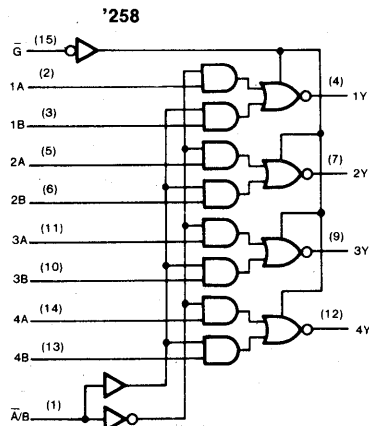
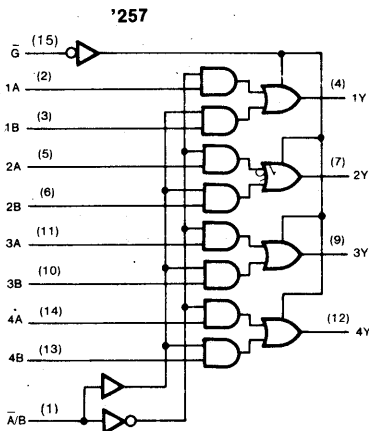


## FUNCTION TABLE

Inputs				Output Y	
Output Control	Select	Data		'257	'258
$\bar{G}$	$\bar{A/B}$	A	B		
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

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## LOGIC DIAGRAMS



# KS54AHCT 257/258 Quad 2-Line to 1-Line Data Selector/ KS74AHCT Multiplexers with 3-State Outputs

## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_{d\uparrow}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

# KS54AHCT 257/258 Quad 2-Line to 1-Line Data Selector/ KS74AHCT Multiplexers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT257

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	7 10		12 17		14 20	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	7 10		12 17		14 20	
Propagation Delay, A/B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		20 25		24 30	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		20 25		24 30	
Output Enable Time, G to any Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16	18 23		22 28	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	13 16	18 23		22 28	
Output Disable Time, G to any Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	12		15		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	12		15		22	
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT258

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	6 9		8 13		14 19	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	6 9		8 13		14 19	
Propagation Delay, A/B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17		23 28		28 34	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17		23 28		28 34	
Output Enable Time, G to any Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14	18 23		22 28	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14	18 23		22 28	
Output Disable Time, G to any Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22	
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

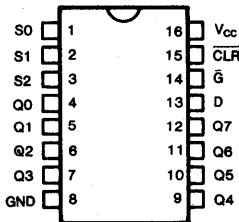
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/Disable input simplifies expansion
- Expandable for N-bit applications
- Four distinct functional modes
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### FUNCTION TABLE

Inputs		Output of Addressed Latch	Each Other Output	Function
CLR	$\bar{G}$			
H	L	D	$Q_{i0}$	Addressable Latch
H	H	$Q_{i0}$	$Q_{i0}$	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.

$Q_{i0}$  = the level of  $Q_i$  ( $i = Q, 1, \dots, 7$ , as appropriate) before the indicated steady-state input conditions were established.

### DESCRIPTION

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear (CLR) and enable ( $\bar{G}$ ) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

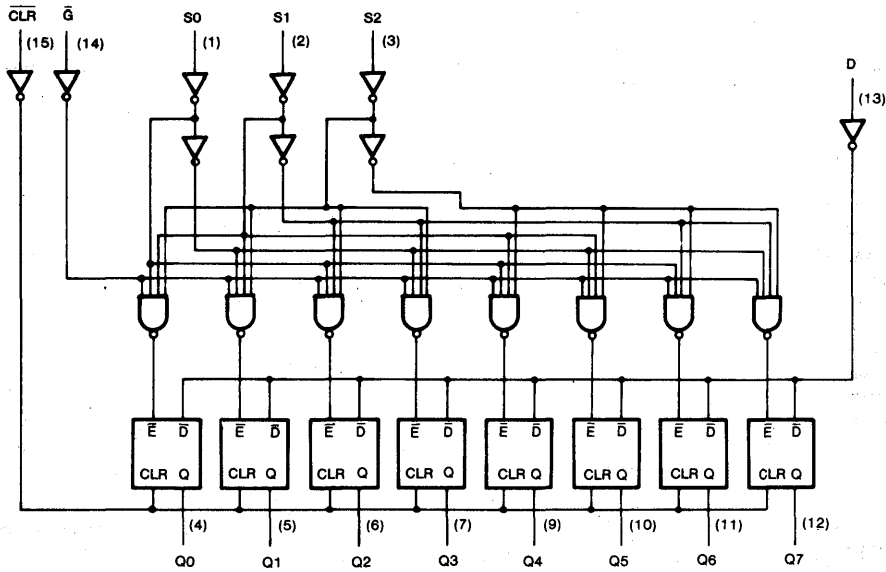
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LATCH SELECTION TABLE

Select Inputs			Latch Addressed
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

LOGIC DIAGRAM



4

**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA
- Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$
- Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$
- Operating Temperature  
Range  
KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				Unit
			KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2\text{ ns}$ , AHCT259)

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0\text{V}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
			Propagation Delay CLR to any Q	$t_{PHL}$	$C_L=50\text{pF}$	9		15	
Propagation Delay, Data to any Q	$t_{PLH}$	12		19			23	ns	
	$t_{PHL}$	12		19			23	ns	
Propagation Delay, Address to any Q	$t_{PLH}$	13		22			27	ns	
	$t_{PHL}$	13		22			27	ns	
Propagation Delay, $\bar{G}$ to any Q	$t_{PLH}$	12		20			24	ns	
	$t_{PHL}$	12		20			24	ns	
Pulse Width	$\bar{C}LR$ Low	$t_w$	6	10			10		ns
	$\bar{G}$ Low		9	15		20		ns	
Setup Time Data or Address before $\bar{G}\uparrow$	$t_{su}$		10	15		20	ns		
Hold Time, Data or Address before $\bar{G}\uparrow$	$t_h$		-3	0		0	ns		
Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$		80				pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

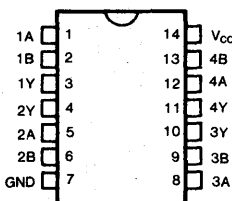
**DESCRIPTION**

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

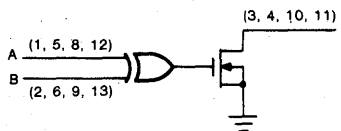
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 2$ ns), AHCT266

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$				Unit
			KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		
			Typ	Min	Max	Min	
Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	19		29	35	ns
	$t_{PHL}$	$R_L=1\text{k}\Omega$	11		18	22	
Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Eight positive-edge-triggered D-type flip-flops with single-rail outputs
- Buffered common clock and asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 24\text{mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

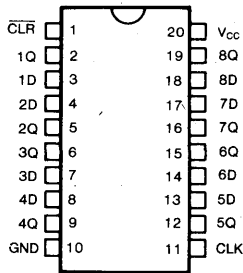
These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear (CLR) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

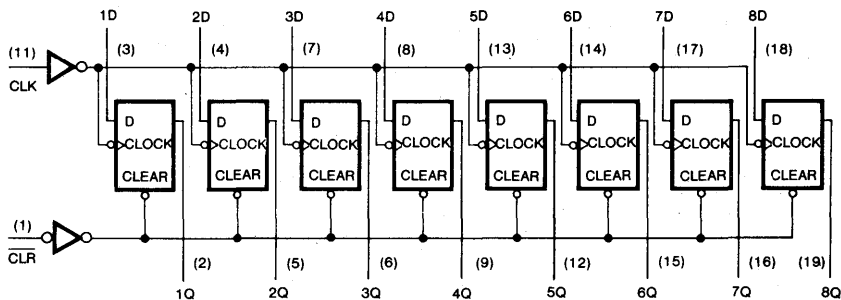


### FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , .....	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....	$\pm 70$ mA
Continuous Current Through $V_{CC}$ or GND pins .....	$\pm 250$ mA
Storage Temperature Range, $T_{stg}$ .....	-65°C to +150°C
Power Dissipation Per Package, $P_d$ † .....	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ .....	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}$ , $V_{OUT}$ ...	0V to $V_{CC}$
Operating Temperature Range	KS74AHCT: -40°C to +85°C KS54AHCT: -55°C to +125°C
Input Rise & Fall Times, $t_r$ , $t_f$ .....	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT273)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30		MHz
Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	13		18.5		19	ns
		$C_L = 150\text{pF}$	13		20		34	
Propagation Delay, CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$	13		17.5		19	ns
		$C_L = 150\text{pF}$	13		20		34	
Propagation Delay, CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$	13		18.5		22	ns
		$C_L = 150\text{pF}$	14		23		28	
Pulse Width	CLR Low	$t_w$	8	14		17		ns
	CLK High or Low		8	14		17		
Setup Time before CLK†	Data	$t_{su}$	6	10		10		ns
	Clear inactive State		9	15		15		
Hold time, Data after CLK†	$t_h$		-3	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$	(per package)	150					pF

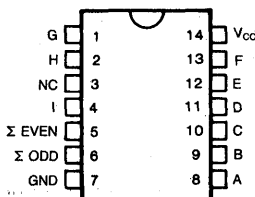
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Generates Odd or Even Parity for Nine Data Lines
- Cascadable for N-Bits Parity
- Can be used to Upgrade Existing Systems using MSI Parity Circuits
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## DESCRIPTION

These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

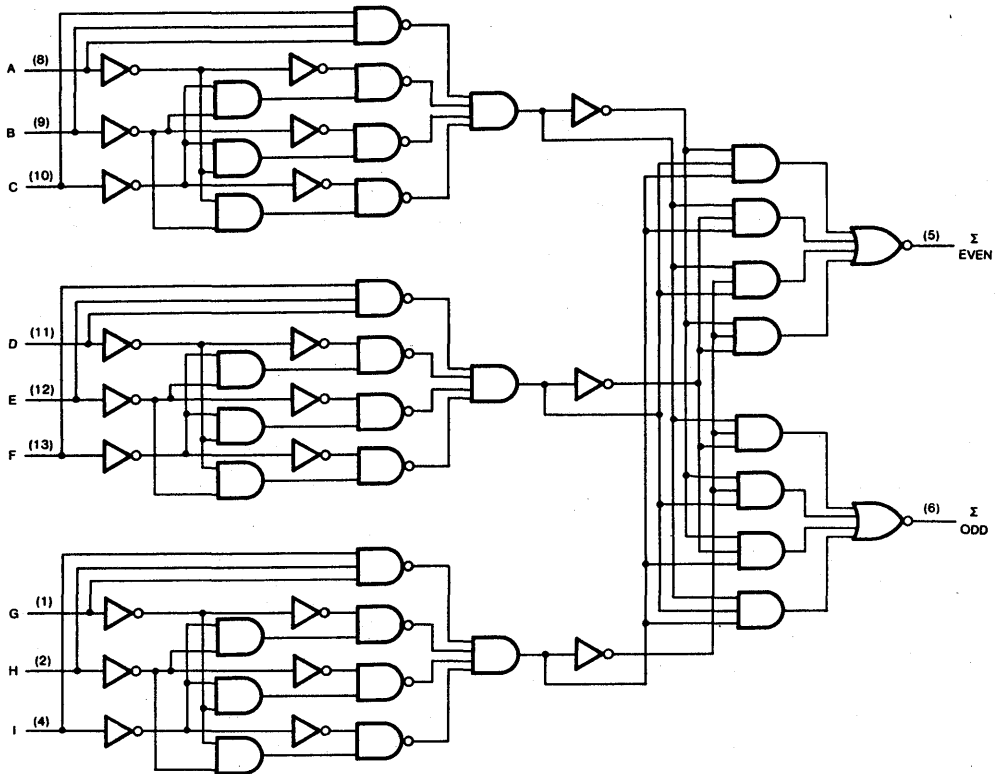
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

LOGIC DIAGRAM



4

**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA
- Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$
- Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$
- Operating Temperature  
Range  
KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84		$V_{CC}-0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0		160.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT280)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			$V_{CC}=5.0\text{V}$	$V_{CC}=5.0\text{V} \pm 10\%$		$V_{CC}=5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to $\Sigma$ Even	$t_{PLH}$	$C_L=50\text{pF}$	12		21		24	ns
		$C_L=150\text{pF}$	15		25		30	
Propagation Delay, Any input to $\Sigma$ Odd	$t_{PHL}$	$C_L=50\text{pF}$	12		21		24	ns
		$C_L=150\text{pF}$	15		25		30	
Propagation Delay, Any input to $\Sigma$ Odd	$t_{PLH}$	$C_L=50\text{pF}$	13		22		26	ns
		$C_L=150\text{pF}$	16		27		32	
Propagation Delay, Any input to $\Sigma$ Odd	$t_{PHL}$	$C_L=50\text{pF}$	13		22		26	ns
		$C_L=150\text{pF}$	16		27		32	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

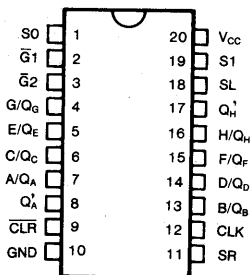
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift right, shift left, and load data
- Operates with outputs enabled or at high impedance
- Can be cascaded for N-bit word lengths
- Direct overriding clear
- Application:  
Stacked or push-down registers, buffer storage, and accumulator registers
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### DESCRIPTION

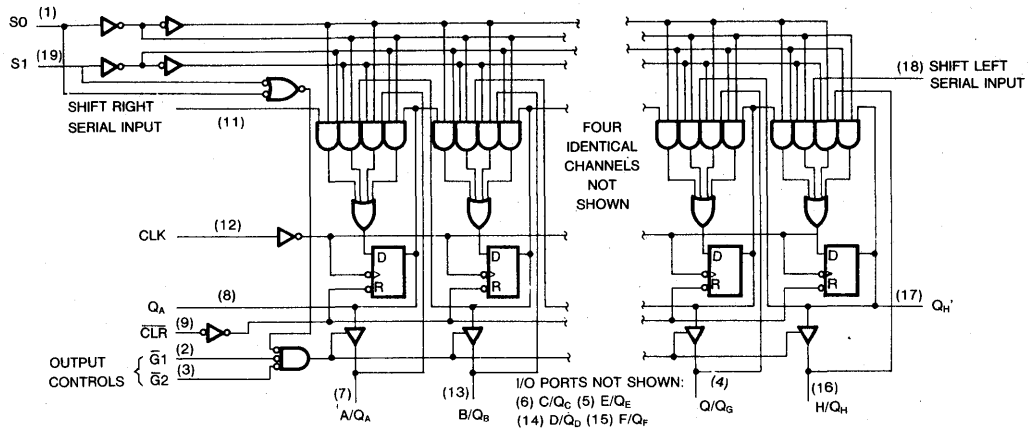
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when  $\overline{\text{CLR}}$  is low. Pulling either of the output controls,  $\overline{\text{G1}}$  or  $\overline{\text{G2}}$ , high disables the outputs but this has no effect on clearing, shifting, or storage of data.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**LOGIC DIAGRAM**



**FUNCTION TABLE**

Mode	Inputs						I/O Ports								Outputs			
	$\overline{CLR}$	$S_1$	$S_0$	Output Control		CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
				$\bar{G}_1$	$\bar{G}_2$													
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . . ( $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12mW/^\circ C$  from  $85^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $Q'_A$ and $Q'_H$ outputs: $I_O = -4mA$ $Q_A$ thru $Q_H$ outputs: $I_O = -6mA$	$V_{CC}$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
			4.2	3.98	3.84	3.7	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $Q'_A$ and $Q'_H$ outputs: $I_O = 4mA$ $I_O = 8mA$ $Q_A$ thru $Q_H$ outputs: $I_O = 12mA$ $I_O = 24mA$	0	0.1	0.1	0.1	V
				0.26 0.39	0.33 0.5	0.4	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IN}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT299

Characteristic	Symbol	Conditions†	KS74AHCT			KS54AHCT		Unit	
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$		50	30		25		MHz	
Propagation Delay, CLK to Q'A or Q'H	$t_{PLH}$	$C_L = 50\text{pF}$	10		17		20	ns	
	$t_{PHL}$		10		17		20		
Propagation Delay, CLR to Q'A or Q'H	$t_{PHL}$		13		22		26	ns	
Propagation Delay, CLK to Q_A thru Q_H	$t_{PLH}$	$C_L = 50\text{pF}$	10		16		19	ns	
	$t_{PHL}$	$C_L = 150\text{pF}$	13		21		25		
Propagation Delay, CLR to Q_A thru Q_H	$t_{PHL}$	$C_L = 50\text{pF}$	10		16		19	ns	
	$t_{PHL}$	$C_L = 150\text{pF}$	13		21		25		
Output Enable Time, $\bar{G}1, \bar{G}2$ , to Q_A thru Q_H	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		19		23	ns
	$t_{PZL}$		$C_L = 150\text{pF}$	14		24		29	
Output Disable Time, $\bar{G}1, \bar{G}2$ to Q_A thru Q_H	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		19		23	ns
	$t_{PLZ}$		$C_L = 150\text{pF}$	14		24		29	
Pulse Width	CLK High or Low	$t_w$		9	15		20	ns	
	$\overline{\text{CLR}}$ Low			5	8		10		
Setup time before CLK†	S0 and S1	$t_{su}$		12	20		10	ns	
	High-Level Inputs			8	13		15		
	Low-Level Inputs			8	13		15		
	CLR Inactive			8	13		15		
Hold Time after CLK†	S0 and S1	$t_h$		0	0		0	ns	
	All Inputs			0					
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

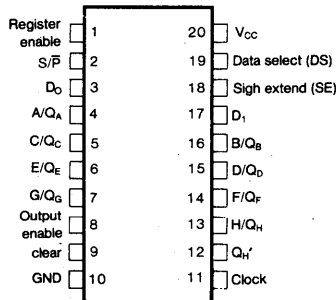
- Multiplexed inputs/outputs provide improved bit density
- Sign extend function
- Direct overriding clear
- 3 state outputs drive bus lines directly
- Function pin-out, speed and drive compatibility with 54/74 ALS logic family
- Low power consumption characteristic of CMOS
- High drive current output ( $I_{OL} = 24mA @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices.
- Wide Operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature range:  
KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}$   
KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**DESCRIPTION**

These 8 bit Shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either  $D_0$  or  $D_1$  input as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the  $S/\bar{P}$  inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high clock transition. The data extend function repeats the sign in the  $Q_A$  flip flop during shifting. An overriding clear input clears the internal register when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

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**PIN CONFIGURATION**



**FUNCTION TABLE**

OPERATION	INPUT							INPUT/OUTPUTS				Output Q <sub>H</sub>
	Clear	Register enable	S/P	Sign extend	Data select	Output enable	Clock	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub> ... H/Q <sub>H</sub>		
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q <sub>AO</sub>	Q <sub>BO</sub>	Q <sub>CO</sub>	Q <sub>HO</sub>	Q <sub>HO</sub>
Shift Right	H	L	H	H	L	L	↑	D <sub>O</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Gn</sub>	Q <sub>Gn</sub>
	H	L	H	H	H	L	↑	D <sub>I</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Gn</sub>	Q <sub>Gn</sub>
Sign Extend	H	L	H	L	X	L	↑	Q <sub>An</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Gn</sub>	Q <sub>Gn</sub>
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any inputs, including transitions)

↑ = transition from low to high level

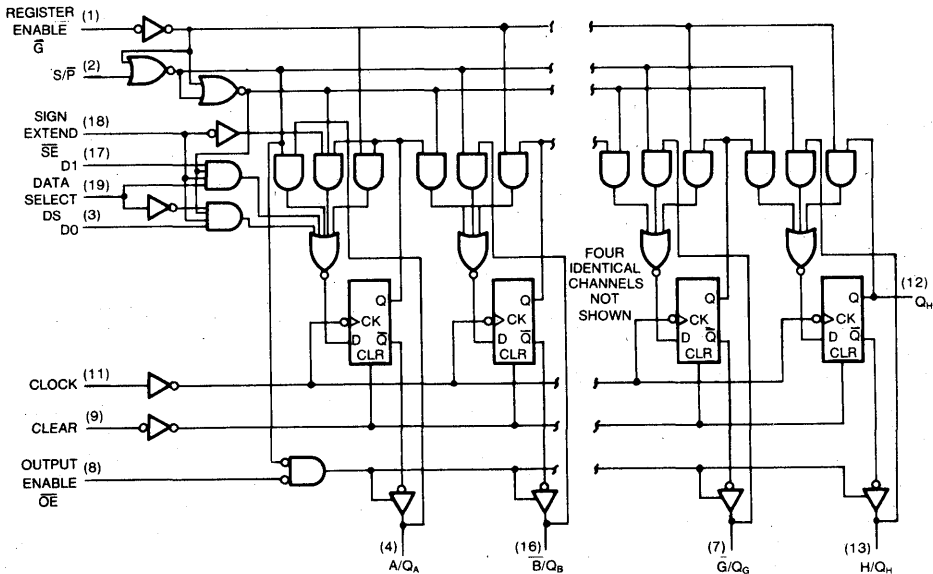
Q<sub>AO</sub>...Q<sub>HO</sub> = the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the indicated steady-state conditions were established.

Q<sub>An</sub>...Q<sub>Hn</sub> = the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the most recent ↑ transition of the clock.

D<sub>O</sub>, D<sub>I</sub> = the level of steady-state inputs at inputs D<sub>O</sub> and D<sub>I</sub> respectively

a...h = the level of steady-state inputs at input A through H respectively.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $85^\circ\text{C}$  to  $85^\circ\text{C}$   
 Ceramic Package (J):  $-12\text{mW}/^\circ\text{C}$  from  $100^\circ\text{C}$  to  $125^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT322

Characteristic	Symbol	Conditions†	TA = 25°C VCC = 5.0V		KS74AHCT TA = -40°C to +85°C VCC = 5.0V ± 10%		KS54AHCT TA = -55°C to +125°C VCC = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max		
			Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	50	30		
Maximum Propagation Delay, Clock to Q <sub>H</sub>	t <sub>PHL</sub>	12		20			24	ns	
	t <sub>PLH</sub>	12		20			24		
Maximum Propagation Delay, Clear to Q <sub>H</sub>	t <sub>PHL</sub>	13		21			25	ns	
Maximum Propagation Delay, Clock to Q <sub>A</sub> -Q <sub>H</sub>	t <sub>PHL</sub>	12		20			24	ns	
	t <sub>PLH</sub>	12		20			24		
Propagation Delay Clear to Q <sub>A</sub> -Q <sub>H</sub>	t <sub>PHL</sub>	13		21			25	ns	
Output Enable Time	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF	13			21		25	ns
	t <sub>PZL</sub>		13			21		25	
Output Disable Time	t <sub>PHZ</sub>		11			18		21	ns
	t <sub>PLZ</sub>		11		18		21		
Clock Pulse Width	High t <sub>w</sub>		7	12		15		ns	
	Low t <sub>w</sub>		7	12		15			
Clear Pulse Width Low	t <sub>w</sub>		7	12		15		ns	
Data Set up Time	t <sub>s</sub>		8	15		20		ns	
Select Set up Time	t <sub>s</sub>		8	15		20			
Data Hold Time	t <sub>h</sub>		-3	0		0	0	ns	
Select Hold Time	t <sub>h</sub>	5	8		10				
Recovery Time	t <sub>rec</sub>	10	17		20		ns		
Maximum Input Capacitance	C <sub>in</sub>	5					pF		
Power Dissipation Capacitance	C <sub>PD</sub>	100					pF		

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Inverting Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs  
 ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

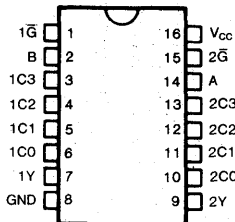
**DESCRIPTION**

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ( $\bar{G}$ ) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

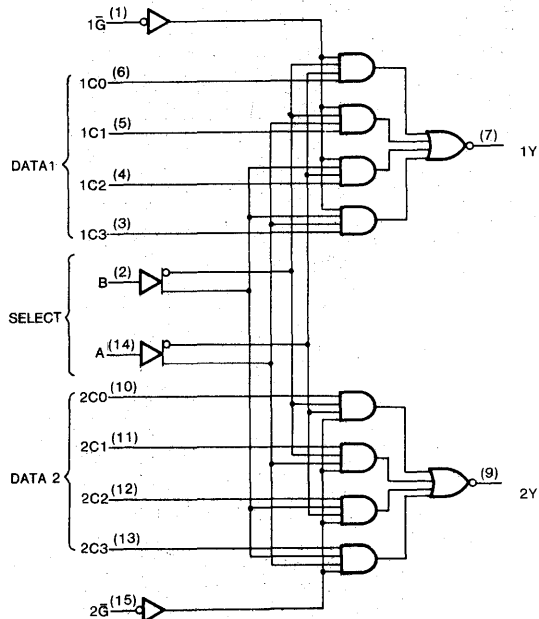


**FUNCTION TABLE**

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit			
					$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$				
			Typ				Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V			
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V			
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V			
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V			
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$			
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$			
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA			

AC ELECTRICAL CHARACTERISTICS (Input  $t_r, t_f \leq 2$  ns), AHCT352

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min		Max	
Propagation Delay, A or B to Y	$t_{PLH}$	$C_L = 50\text{pF}$	14		23		28	ns	
		$C_L = 150\text{pF}$	17		28		34		
	$t_{PHL}$	$C_L = 50\text{pF}$	14		23		28	ns	
		$C_L = 150\text{pF}$	17		28		34		
Propagation Delay, Data (Any C) to Y	$t_{PLH}$	$C_L = 50\text{pF}$	11		18		21	ns	
		$C_L = 150\text{pF}$	14		23		27		
	$t_{PHL}$	$C_L = 50\text{pF}$	11		18		21	ns	
		$C_L = 150\text{pF}$	14		23		27		
Propagation Delay, $\bar{G}$ to Y	$t_{PLH}$	$C_L = 50\text{pF}$	12		20		24	ns	
		$C_L = 150\text{pF}$	15		25		30		
	$t_{PHL}$	$C_L = 50\text{pF}$	12		20		24	ns	
		$C_L = 150\text{pF}$	15		25		30		
Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

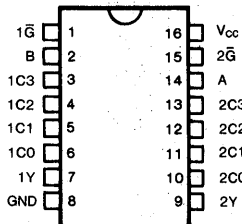
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Inverting Version of '253
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

**DESCRIPTION**

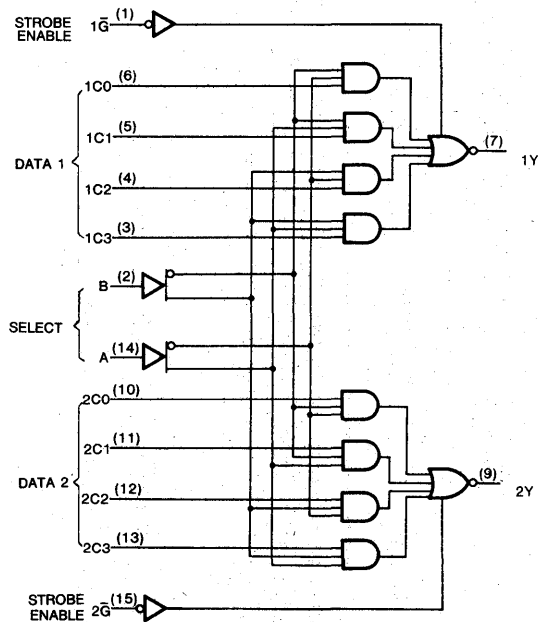
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ( $\bar{G}$ ) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ( $\bar{G}$ ). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT353

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ	Min	Max	Min	Max		
Propagation Delay, A or B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$	14		24		28	ns	
		$C_L = 150\text{pF}$	17		29		34		
	$t_{PHL}$	$C_L = 50\text{pF}$	14		24		28	ns	
		$C_L = 150\text{pF}$	17		29		34		
Propagation Delay, Data (Any C) to Any Y	$t_{PLH}$	$C_L = 50\text{pF}$	10		18		21	ns	
		$C_L = 150\text{pF}$	13		23		27		
	$t_{PHL}$	$C_L = 50\text{pF}$	10		18		21	ns	
		$C_L = 150\text{pF}$	13		23		27		
Output Enable Time, $\bar{G}$ to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	10		16		19	ns
			$C_L = 150\text{pF}$	13		21		25	
	$t_{PZL}$	$C_L = 50\text{pF}$	10		16		19		
			$C_L = 150\text{pF}$	13		21		25	
Output Disable Time, $\bar{G}$ to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	10		18		22	ns	
			$C_L = 50\text{pF}$	10		18			22
Input Capacitance	$C_{IN}$		5				pF		
Output Capacitance	$C_{OUT}$	Output Disabled	10				pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

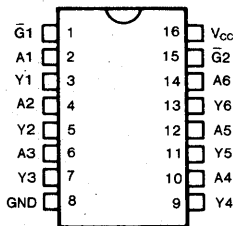
The '365 and '366 have two output enables ( $\bar{G}1$  and  $\bar{G}2$ ) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable ( $\bar{G}1$ ) controls four gates and the other ( $\bar{G}2$ ) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.



**PIN CONFIGURATION**



**FUNCTION TABLES**

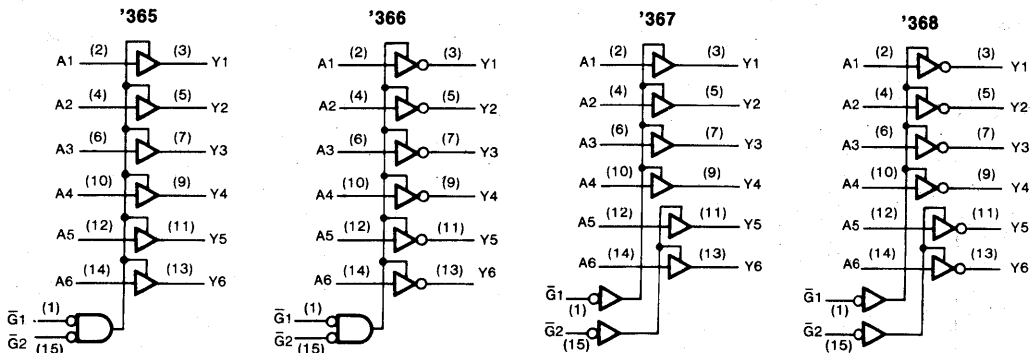
**'365 and '366**

Inputs		Y Outputs		
$\bar{G}1$	$\bar{G}2$	A	'365	'366
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

**'367 and '368**

Inputs		Y Outputs	
G1 & G2	A	'367	'368
L	L	L	H
L	H	H	L
H	X	Z	Z

**LOGIC DIAGRAMS**





**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT365, AHCT366, AHCT367, AHCT368

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	Min	Max		Min
			Typ	$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$			
Propagation Delay, A to Y,	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	8		14		17	ns	
		C <sub>L</sub> = 150pF	11		19		33		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	8		14		17		
		C <sub>L</sub> = 150pF	11		19		33		
Output Enable Time, $\bar{G}$ to Y	t <sub>PZH</sub>	R <sub>L</sub> = 1k $\Omega$	C <sub>L</sub> = 50pF	14		23		28	ns
			C <sub>L</sub> = 150pF	17		28		34	
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	14		23		28		
		C <sub>L</sub> = 150pF	17		28		34		
Output Disable Time, $\bar{G}$ to Y	t <sub>PHZ</sub>	R <sub>L</sub> = 1k $\Omega$	15		20		22	ns	
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	15		20		22		
Input Capacitance	C <sub>IN</sub>		5					pF	
Output Capacitance	C <sub>OUT</sub>	Output Disabled	10					pF	
Power Dissipation Capacitance* (per driver)	C <sub>PD</sub>	$\bar{G} = V_{CC}$ $\bar{G} = \text{GND}$	5					pF	

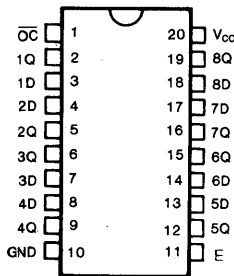
\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

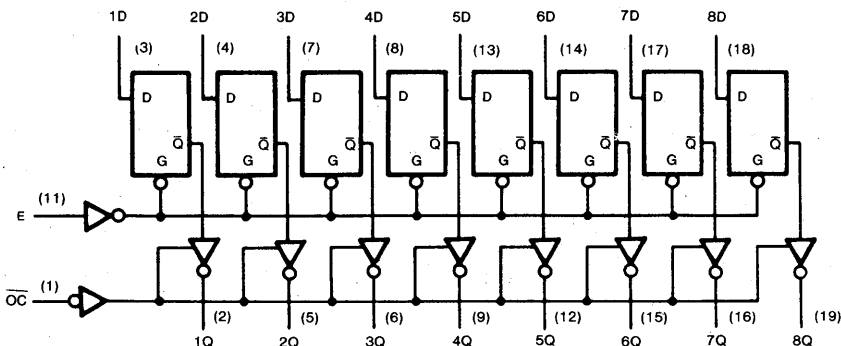
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

(Each Latch)

Inputs			Output
$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT373

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, D to Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11		16		19	ns
			14		19		23	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11		16		19	
			14		19		23	
Propagation Delay, E to Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14		23		27	ns
			17		28		33	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14		23		27	
			17		28		33	
Output Enable Time, OC to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12		20		24	ns
			15		25		30	
	$t_{PZL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12		20		24	
			15		25		30	
Output Disable Time, OC to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22	
Pulse Width, E High	$t_w$		9	15		18		ns
Setup Time, D before E↓	$t_{SU}$		6	10		10		ns
Hold Time, D after E↓	$t_H$		3	5		7		ns
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance* (per latch)	$C_{PD}$	$\overline{OC} = V_{CC}$	5					pF
		$\overline{OC} = \text{GND}$	30					

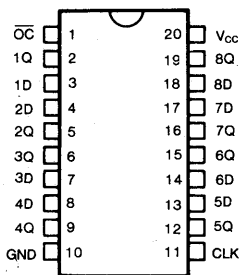
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

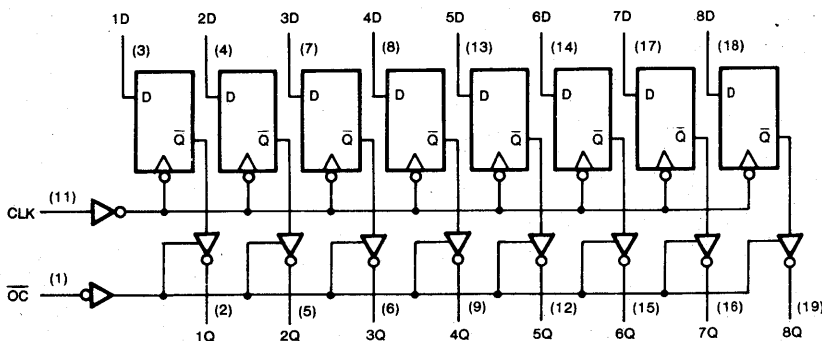
### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### LOGIC DIAGRAM



### DESCRIPTION

The '374 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	$Q_0$
H	X	X	Z

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_{d1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT374

Characteristic	Symbol	Conditions†	$T_s = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_s = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_s = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30		MHz
Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	10 13		15 19		17 23	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	10 13		15 19		17 23	
Output Enable Time, $\overline{OC}$ to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$		11 14		18 23	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$		11 14		18 23	
Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		13		18	22	ns
	$t_{PLZ}$			13		18	22	
Pulse Width, CLK High or Low	$t_w$		7	15		18		ns
Setup Time, D before CLK†	$t_{su}$		9	14		13		ns
Hold Time, D after CLK†	$t_h$		-3	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance*		$\overline{OC} = V_{CC}$ (per stage)	5					
		$\overline{OC} = \text{GND}$	30					

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

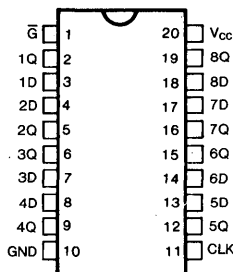
† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Can be used for implementing
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The '377 contains eight positive-edge-triggered D-type flip-flops with an enable input. This part is similar to '273 but features a latched clock enable ( $\bar{G}$ ) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if  $\bar{G}$  is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the  $\bar{G}$  input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

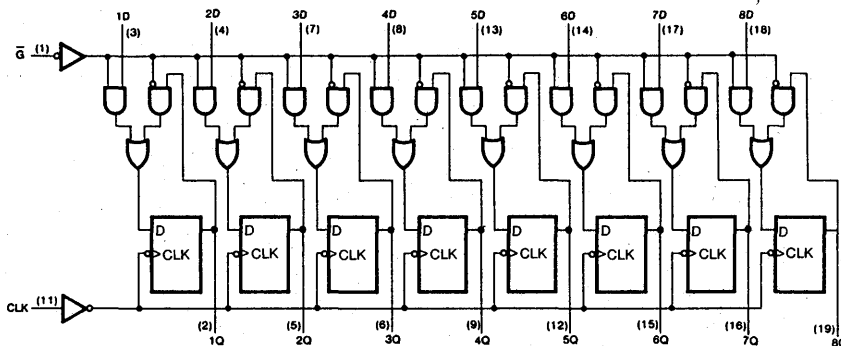
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\bar{G}$	CLK	DATA	Q
H	X	X	$Q_0$
L	↑	H	H
L	↑	L	L
X	L	X	$Q_0$

**LOGIC DIAGRAM**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT377

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C	KS74AHCT		KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C			
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	f <sub>max</sub>		50	35		30		MHz
Propagation Delay, CLK to any Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	10		16		19	ns
	t <sub>PHL</sub>		10		16		19	
Pulse Width	⎯ Low	t <sub>w</sub>	8	14		17		ns
	⎯ CLK High or Low		8	14		17		
Setup time before CLK†	Data	t <sub>su</sub>	6	10		10		ns
	⎯ High or Low		9	15		15		
Hold Time, Data after CLK†	t <sub>h</sub>		-3	0		0		ns
Input Capacitance	C <sub>IN</sub>		5					pF
Power Dissipation Capacitance*	C <sub>PD</sub>	per package	50					pF

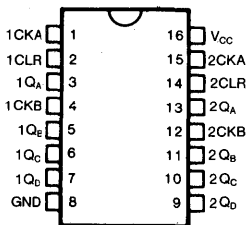
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Individual clock for A and B flip-flops provide dual +2 and +5 counters
- Direct clear for each 4-bit counter
- Significant improvement in system density through reduced counter package count.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
( $I_{OL} = 8 \text{ mA}$  @  $V_{OL} = 0.5V$ )
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### DESCRIPTION

These devices incorporate dual divide-by-two and divide-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiple of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

4

### FUNCTION TABLES

**BCD COUNT SEQUENCE  
(EACH COUNTER)  
(See Note A)**

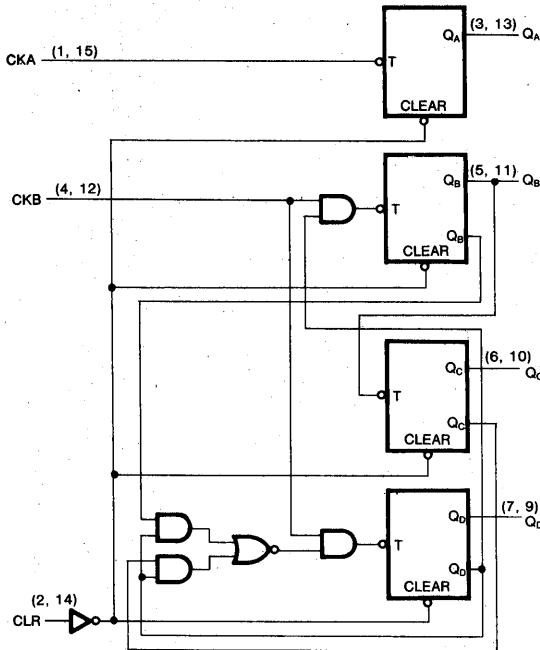
COUNT	OUTPUT			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**BIQUINARY (5-2)  
(EACH COUNTER)  
(See Note B)**

COUNT	OUTPUT			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

- NOTES A. Output  $Q_A$  is connected to input CKB for BCD count.  
B. Output  $Q_D$  is connected to input CKA for biquinary count.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , .....	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins .....	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ † .....	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage, $V_{CC}$ .....	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ ..	0V to $V_{CC}$
Operating Temperature Range	KS74AHCT: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54AHCT: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r, t_f$ .....	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C		KS54AHCT T <sub>a</sub> = -55°C to +125°C		Unit
			Typ		Guaranteed Limits				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-4mA	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	V <sub>CC</sub> -0.1 3.7	V	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	±1.0	μA	
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	160.0	μA	
Additional Worst Case Supply Current	ΔI <sub>CC</sub>	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	3.0	mA	

#### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub> ≤ 2 ns, AHCT390)

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C	KS74AHCT T <sub>a</sub> = -40°C to +85°C		KS54AHCT T <sub>a</sub> = -55°C to +125°C		Unit
			V <sub>CC</sub> = 5.0V	V <sub>CC</sub> = 5.0V ± 10%		V <sub>CC</sub> = 5.0V ± 10%		
			Typ	Min	Max	Min	Max	
Propagation Delay, CKA to Q <sub>A</sub> or CKB to Q <sub>B</sub>	t <sub>max</sub>	C <sub>L</sub> = 50pF	50	30		25		MHz
Propagation Delay, CKA to Q <sub>A</sub>	t <sub>PLH</sub>		9		15		18	ns
	t <sub>PHL</sub>		9		15		18	ns
Propagation Delay, CKA to Q <sub>C</sub>	t <sub>PLH</sub>		24		40		48	ns
	t <sub>PHL</sub>		24		40		48	ns
Propagation Delay, CKB to Q <sub>B</sub>	t <sub>PLH</sub>		10		17		21	ns
	t <sub>PHL</sub>		10		17		21	ns
Propagation Delay, CKB to Q <sub>C</sub>	t <sub>PLH</sub>		16		27		33	ns
	t <sub>PHL</sub>		16		27		33	ns
Propagation Delay, CKB to Q <sub>D</sub>	t <sub>PLH</sub>		10		17		21	ns
	t <sub>PHL</sub>	10		17		21	ns	
Propagation Delay, CLR to Any Q	t <sub>PHL</sub>		19		30		35	ns
Pulse Width	CKA or CKB High or Low CLR High	t <sub>w</sub>	7	12		15		ns
			7	12		15		ns
Minimum Setup Time, CLR inactive before CKA or CKB	t <sub>SU</sub>		5	8		10		ns
Input Capacitance	C <sub>IN</sub>		5					pF
Power Dissipation Capacitance	C <sub>PD</sub>							pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

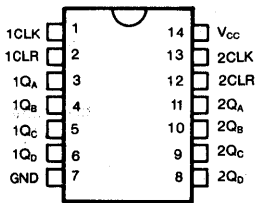
**DESCRIPTION**

The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. parallel outputs from each counter stage provided any submultiple of the input count frequency for system timing signals.

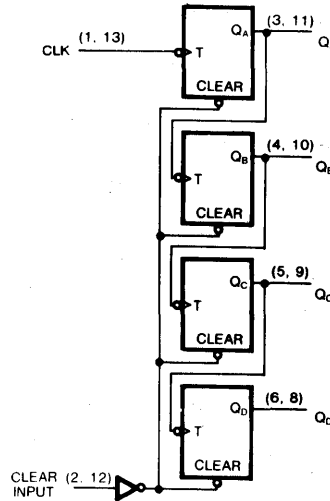
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

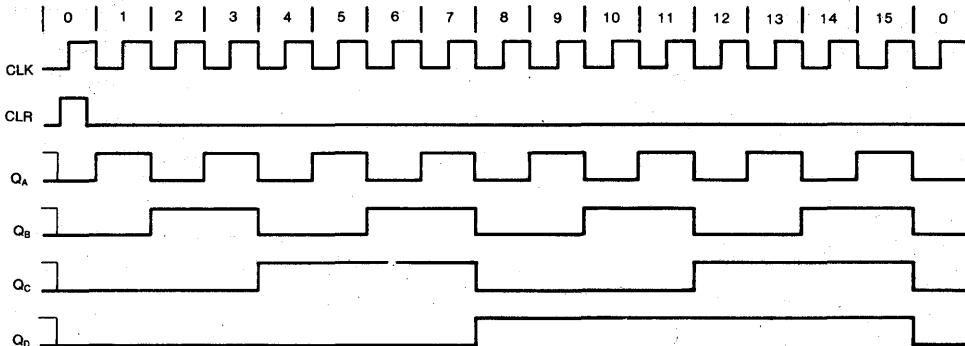
**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**LOGIC TIMING WAVEFORMS**



#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (input  $t_r, t_f \leq 2$  ns), AHCT393

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	30		25		MHz
Propagation Delay, A to $Q_A$	$t_{PLH}$		14		22		26	ns
	$t_{PHL}$		14		22		26	ns
Propagation Delay, A to $Q_B$	$t_{PLH}$		18		27		32	ns
	$t_{PHL}$		18		27		32	ns
Propagation Dealy, A to $Q_C$	$t_{PLH}$		20		33		40	ns
	$t_{PHL}$		20		33		40	ns
Propagation Delay, A to $Q_D$	$t_{PLH}$		26		40		48	ns
	$t_{PHL}$	26		40		48	ns	
Propagation Dealy, CLR to any Q	$t_{PHL}$		15	25		30	ns	
Pulse Width	A Input High or Low	$t_w$	7	12		15		ns
	CLR High		7	12		15		ns
Setup Time, CLR Inactive before A	$t_{su}$		5	8		10	ns	
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$	(per counter)	40				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74AHCT: -40°C to +85°C**  
**KS54AHCT: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

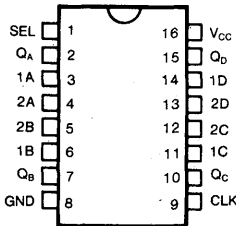
**DESCRIPTION**

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

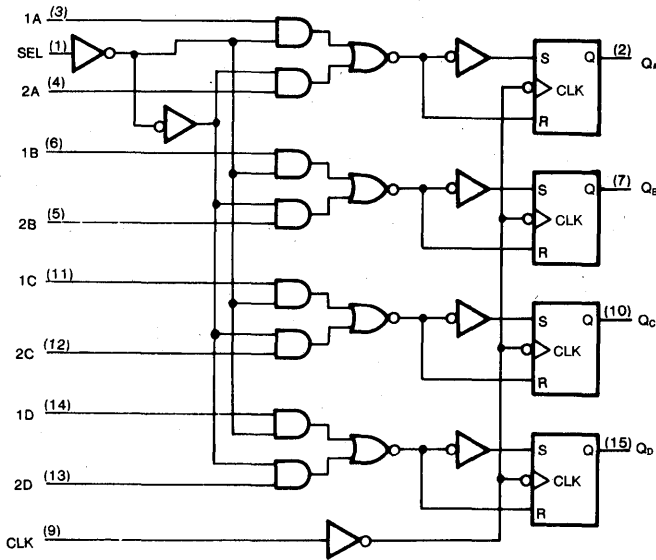


**FUNCTION TABLE**

SEL	Inputs		Output
	Port 1	Port 2	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

- l = Low Voltage Level one setup time prior to the low-to-high clock transition
- h = High Voltage Level one setup time prior to the low-to-high clock transition

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ		Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT399

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			$V_{CC} = 5.0\text{V}$	$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, CLK to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	12		19		23	ns
	$t_{PHL}$		12		19		23	
Pulse Width, CLK High or Low	$t_w$		6	10		15		ns
Time before CLK†	Data	$t_{su}$	6	10		15		ns
	Word Select		6	10		15		
Hold Time, Data after CLK†	$t_h$		-3	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

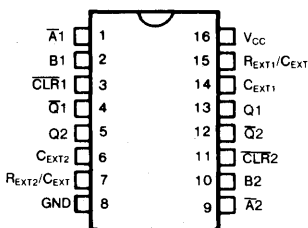
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Simple pulse width formula  $t_w = 0.45RC$
- DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}C$   
KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor ( $R_{EXT}$ ) and capacitor ( $C_{EXT}$ ). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input ( $A_i$ ) or the active High-going edge input ( $B_i$ ). By repeating this process, the output pulse period ( $nQ=HIGH, n\bar{Q}=LOW$ ) can be made as long as desired.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply;

$$t_w = 0.45 \times (R_{EXT}) (C_{EXT})$$

Where  $t_w$  is in seconds. R is in ohm. and C is in farads.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

Inputs			Outputs	
CLR	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌋	⌋
H	↓	H	⌋	⌋

H= HIGH voltage level

L= LOW voltage level

X= don't care

↑= LOW to HIGH transition

↓= HIGH to LOW transition

⌋= one HIGH level output pulse

⌋= one LOW level output pulse

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package(N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ..... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$				Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT} = 0\mu A$		2.7	2.9	3.0	mA

**4**

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT 423

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit	
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max	
Propagation Delay $\bar{A}, B$ to $Q, \bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_{ext} = 0,$ $R_{ext} = 5\text{k}\Omega$	18		33		40	ns
	$t_{PHL}$		18		33		40	
Propagation Delay $\bar{CLR}$ to $Q, \bar{Q}$	$t_{PLH}$		16		27		33	ns
	$t_{PHL}$		16		27		33	
Output Pulse Width 1	$t_{WQ1}$		116		207		209	ns
Output Pulse Width 2	$t_{WQ2}$	$C_L = 50\text{pF}$ $C_{ext} = 10\text{nF}$ $R_{ext} = 10\text{k}\Omega$	45	38	52	38	52	$\mu\text{s}$
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $A_i = \text{LOW}$	5		16		20	ns
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $B_i = \text{High}$	5		16		20	ns
Clear Pulse Width	$t_w$	$C_L = 50\text{pF}$ $CLR_i = \text{LOW}$	6		16		20	ns
External Timing Resistance	$R_{ext}$			2	100	2	100	$\text{k}\Omega$
External Timing Capacitance	$C_{ext}$		no restriction					
Input Capacitance	$C_{in}$		5					pF
Power Dissipation/Capacitance	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .  
 † For AC switching test circuits and timing waveforms see section 2.

**Application Information**

The basic output pulse width is determined by the value of external capacitance and timing resistance.  
 For output pulse widths greater than  $100\mu\text{s}$  or external capacitance greater than  $10\text{nF}$  the following equation should be used.

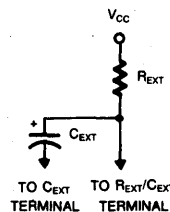
$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

- $t_w$  is in  $\mu\text{s}$
- $k$  is the multiplying factor and is approximately 0.45 for
- $C_{ext}$  is in  $\text{nF}$
- $R_{ext}$  is in  $\text{k}\Omega$

For best results, system ground should be applied to the  $C_{ext}$  terminal. These devices do not require a switching diode in series with the  $R_{ext}/C_{ext}$  terminal (as required by some other monostable multivibrators)

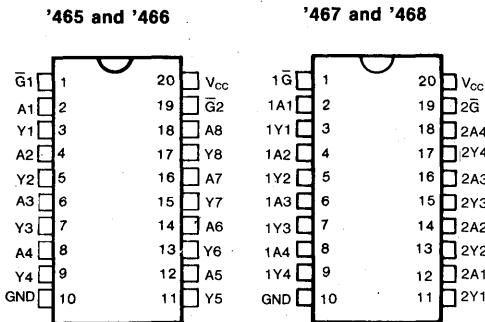
**TIMING COMPONENT**



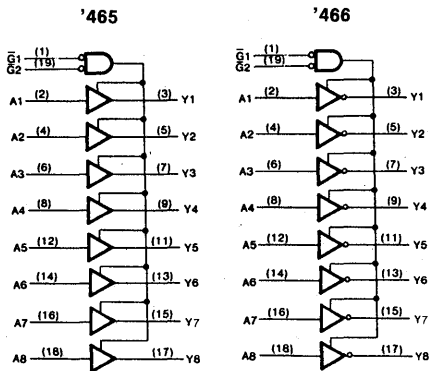
**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATIONS**



**LOGIC DIAGRAMS**



**DESCRIPTION**

These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has the choice of inverting/noninverting outputs and various types of output controls.

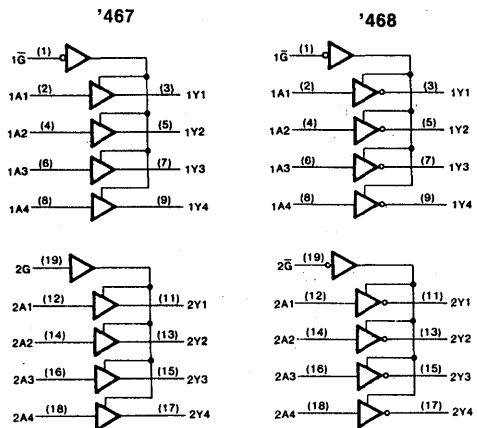
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

Input			Output	
$\bar{G}_1$	$\bar{G}_2$	A	'465	'466
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

Input			Output	
G	$\bar{G}$	A	'467	'468
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z





**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
(-0.5V <  $V_O$  <  $V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns). AHCT465, AHCT466, AHCT467, AHCT468

Parameter	Symbol	Conditions	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		54AHCT $T_a = +55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	7 10		12 17		14 20	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	7 10		12 17		14 20	
Output Enable Time, Enable to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		20 25		24 30	ns
	$t_{PZL}$		12 15		20 25		24 30	
Output Disable Time, Enable to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22	
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	$C_{PD}$	Output Disabled	5					pF
		Output Enabled	30					

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .  
 For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

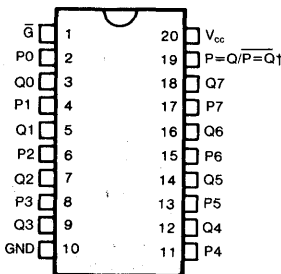
- Compares two 8-bit words
- '518, '520 and 522 have 20kΩ pull-up Resistors on Q Inputs

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q Open-Drain
'519	No	P=Q Open-Drain
'520	Yes	$\overline{P}=\overline{Q}$ Totem-Pole
'521	No	$\overline{P}=\overline{Q}$ Totem-Pole
'522	Yes	$\overline{P}=\overline{Q}$ Open-Drain

† '521 is identical to '688

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



† P=Q for '518 and '519;  
 $\overline{P}=\overline{Q}$  for '520, '521, '522.

**DESCRIPTION**

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide P=Q outputs, while the '520, '521, and '522 provide  $\overline{P}=\overline{Q}$  outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-kΩ inputs for analog or switch data.

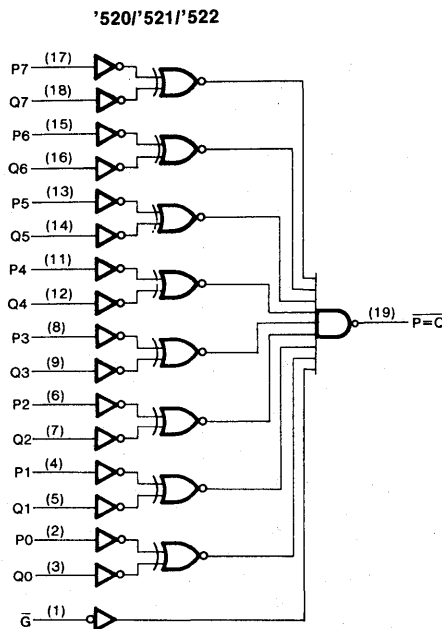
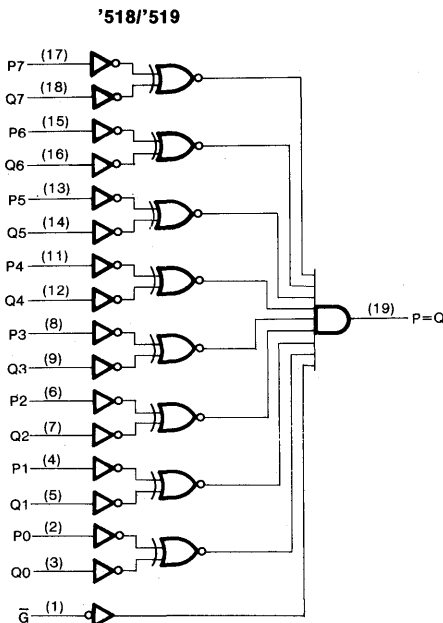
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

**FUNCTION TABLE**

INPUTS		OUTPUTS	
DATA P, Q	ENABLE G	P=Q	$\overline{P}=\overline{Q}$
P=Q	L	H	L
P>Q	L	L	H
P<Q	L	L	H
X	H	L	H

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$
- DC Input Diode Current,  $I_{IK}$   
 $(V_i < -0.5V$  or  $V_i > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
 $(V_o < -0.5V$  or  $V_o > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_o$   
 $(-0.5V < V_o < V_{CC} + 0.5V)$  . . . . .  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA
- Storage Temperature Range,  $T_{sig}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$
- Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . 0V to  $V_{CC}$
- Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$
- Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	54AHCT	Unit
			Typ	Guaranteed Limits			
					$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.93	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('518, '520 and '522 Q input)		$V_{CC} = \text{Max}$ $V_{IN} = 2.7\text{V}$ $V_{IN} = 0.4\text{V}$		-0.2 -0.6	-0.2 -0.6	-0.2 -0.6	mA
Maximum Input Current (All other Inputs)	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current (Open-Drain Outputs)	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	For '518, '520 and '522: $V_{IN} = \text{GND (Q0-Q7)}$ $V_{IN} = V_{CC}$ or GND (all other inputs)		3.5	3.5	3.5	mA
		For '519 and '521: $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT} = 0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT518, AHCT519)

Characteristic	Symbol	Conditions	54/74AHT	KS74AHT		54AHT		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			$V_{CC} = 5\text{V}$	$V_{CC} = 5\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	$t_{PLH}$	$C_L = 50\text{pF}$	20		30		35	ns
		$C_L = 150\text{pF}$	23		35		41	
	$t_{PHL}$	$C_L = 50\text{pF}$	15		25		30	ns
		$C_L = 150\text{pF}$	18		30		36	
Propagation Delay, $\bar{G}$ to P=Q	$t_{PLH}$	$C_L = 50\text{pF}$	16		23		27	ns
		$C_L = 150\text{pF}$	19		28		33	
	$t_{PHL}$	$C_L = 50\text{pF}$	11		18		22	ns
		$C_L = 150\text{pF}$	14		23		28	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT520, AHCT521)

Characteristic	Symbol	Conditions	54/74AHT	KS74AHT		54AHT		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			$V_{CC} = 5\text{V}$	$V_{CC} = 5\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	$t_{PLH}$	$C_L = 50\text{pF}$	12		19		23	ns
		$C_L = 150\text{pF}$	15		24		29	
	$t_{PHL}$	$C_L = 50\text{pF}$	12		19		23	ns
		$C_L = 150\text{pF}$	15		24		29	
Propagation Delay, $\bar{G}$ to P=Q	$t_{PLH}$	$C_L = 50\text{pF}$	11		17		20	ns
		$C_L = 150\text{pF}$	14		22		26	
	$t_{PHL}$	$C_L = 50\text{pF}$	11		17		20	ns
		$C_L = 150\text{pF}$	14		22		26	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHC522)

Characteristic	Symbol	Conditions	54/74AHT	KS74AHT		54AHT		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			$V_{CC} = 5\text{V}$	$V_{CC} = 5\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typical	Min	Max	Min	Max	
Propagation Delay, P or Q to P=Q	$t_{PLH}$	$C_L = 50\text{pF}$	19		28		33	ns
		$C_L = 150\text{pF}$	22		33		39	
	$t_{PHL}$	$C_L = 50\text{pF}$	14		23		28	ns
		$C_L = 150\text{pF}$	17		28		34	
Propagation Delay, $\bar{G}$ to P=Q	$t_{PLH}$	$C_L = 50\text{pF}$	16		23		27	ns
		$C_L = 150\text{pF}$	19		28		33	
	$t_{PHL}$	$C_L = 50\text{pF}$	11		18		22	ns
		$C_L = 150\text{pF}$	14		27		33	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

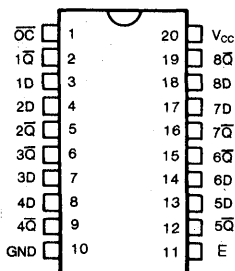
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

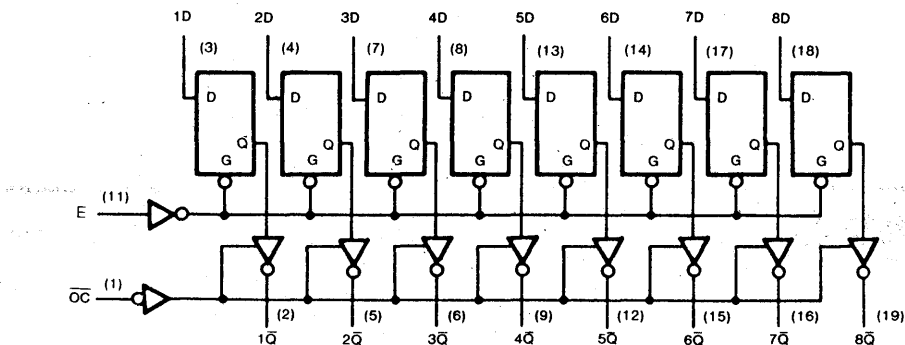
## FEATURES

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## LOGIC DIAGRAM



## DESCRIPTION

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the  $\bar{Q}$  outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	E	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**4**



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f < 2$  ns), AHCT533

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max		
			Propagation Delay, D to $\bar{Q}$	t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	10 13		16 21	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	10 13		16 21		19 25		
Propagation Delay, E to $\bar{Q}$	t <sub>PLH</sub>	C = 50pF C <sub>L</sub> = 150pF	13 16		21 26		25 31	ns	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	13 16		21 26		25 31		
Output Enable Time, OC to any $\bar{Q}$	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	11	18		22	ns	
			C <sub>L</sub> = 150pF	14	23		28		
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	C <sub>L</sub> = 150pF	11	18		22		
			C <sub>L</sub> = 150pF	14	23		28		
Output Disable Time, OC to any $\bar{Q}$	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	13		18		22	ns	
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	13		18		22		
Pulse Width, E High	t <sub>w</sub>		9	15		18		ns	
Setup Time, D before E ↓	t <sub>su</sub>		9	15		18		ns	
Hold Time, D after E ↓	t <sub>h</sub>		3	5		7		ns	
Input Capacitance	C <sub>IN</sub>		5					pF	
Output Capacitance	C <sub>out</sub>	Output Disabled	10					pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	$\bar{OC} = V_{CC}$ $\bar{OC} = GND$	5 30					pF	

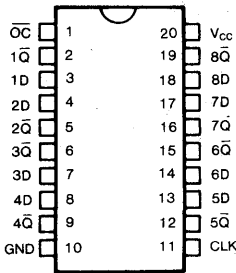
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

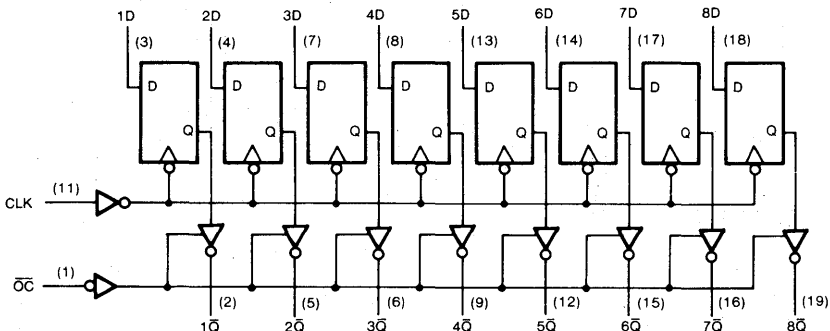
**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**DESCRIPTION**

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock: the  $\bar{Q}$  outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\bar{OC}$ ) which places the outputs in high-impedance state when it is taken high, the OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

(Each Latch)

Inputs			Output
$\bar{OC}$	CLK	D	$\bar{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_i < -0.5V$  or  $V_i > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_o < -0.5V$  or  $V_o > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_o$   
 ( $-0.5V < V_o < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = -20\mu A$ $I_o = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = 20\mu A$ $I_o = 12mA$ $I_o = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{oz}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_i = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f < 2$  ns), AHCT534

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ	Min	Max	Min	Max		
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30		MHz	
Propagation Delay, CLK to any $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23		
Output Enable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	
Output Disable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22		
Pulse Width, CLK High or Low	$t_w$		9	15		18		ns	
Setup Time, D before CLK†	$t_{su}$		9	14		17		ns	
Hold Time, D after CLK†	$t_h$		0	0		0		ns	
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{OC} = V_{CC}$	5					pF	
		$\bar{OC} = \text{GND}$	30						

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

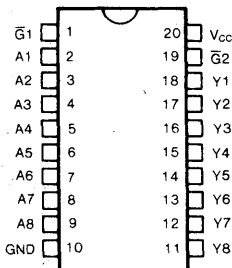
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either  $\bar{G}_1$  or  $\bar{G}_2$  is high, all eight outputs are in the high impedance state.

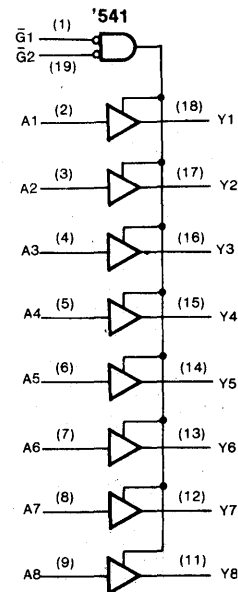
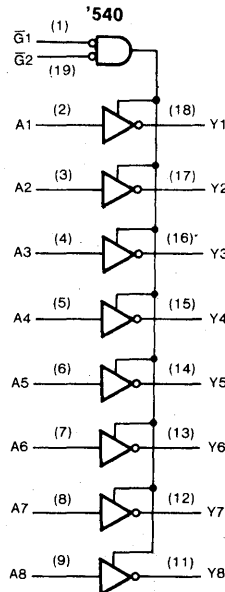
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAMS



### FUNCTION TABLE

Input			Output	
$\bar{G}_1$	$\bar{G}_2$	A	'540	'541
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT540, AHCT541

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ	Min	Max	Min	Max		
Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	7		12		14	ns	
		$C_L = 150\text{pF}$	10		17		20		
	$t_{PHL}$	$C_L = 50\text{pF}$	7		12		14		
		$C_L = 150\text{pF}$	10		17		20		
Output Enable Time, $\bar{G}$ to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	12		20		24	ns
			$C_L = 150\text{pF}$	15		25		30	
	$t_{PZL}$	$C_L = 50\text{pF}$		12		20		24	
			$C_L = 50\text{pF}$	15		25		30	
Output Disable Time $\bar{G}$ to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	14		19		23	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	14		19		23		
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{G} = V_{CC}$	5					pF	
		$\bar{G} = \text{GND}$	30						

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24mA @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}C$  to  $+85^{\circ}C$   
KS54AHCT:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

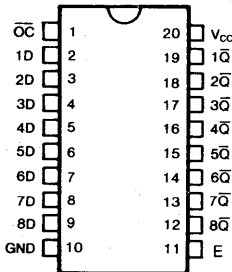
The latches are transparent: when the enable (E) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

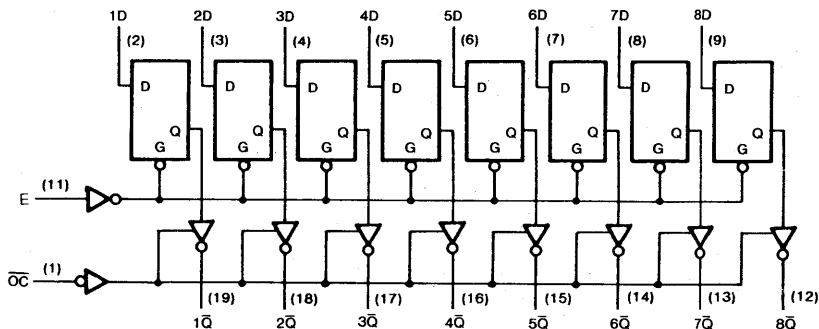


**FUNCTION TABLE**

(Each Latch)

Inputs			Output
$\overline{OC}$	E	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

**LOGIC DIAGRAM**





**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_i < -0.5V$  or  $V_i > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_o < -0.5V$  or  $V_o > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
(-0.5V <  $V_o$  <  $V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_i=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT563

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min	Max		
Propagation Delay, D to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	12		18		22	ns	
		$C_L = 150\text{pF}$	15		23		28		
	$t_{PHL}$	$C_L = 50\text{pF}$	12		18		22	ns	
		$C_L = 150\text{pF}$	15		23		28		
Propagation Delay, E to $\bar{Q}$	$t_{PLH}$	$C = 50\text{pF}$	14		22		27	ns	
		$C_L = 150\text{pF}$	17		27		33		
	$t_{PHL}$	$C_L = 50\text{pF}$	14		22		27	ns	
		$C_L = 150\text{pF}$	17		27		33		
Output Enable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	ns
			$C_L = 150\text{pF}$	14		23		28	
	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	ns
			$C_L = 150\text{pF}$	14		23		28	
Output Disable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PHZ}$	$R_L = 1\text{k}\Omega$		13		19		22	ns
			$t_{PLZ}$		13		19		
Pulse Width, E High	$t_w$		9	15		18		ns	
Setup Time, D before E $\downarrow$	$t_{su}$		6	10		10		ns	
Hold Time, D after E $\downarrow$	$t_h$		3	5		7		ns	
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{OC} = V_{CC}$	5					pF	
		$\bar{OC} = \text{GND}$	30						

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24\text{mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C} + 85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C} + 125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

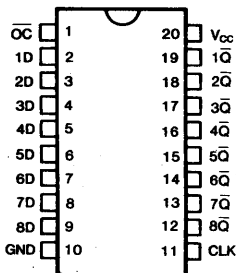
The flip-flops are edge-triggered: on the positive transition of the clock, the  $\bar{Q}$  outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at high impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

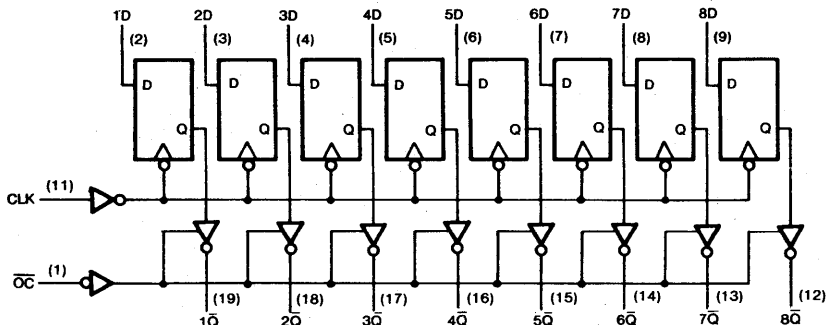


### FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	$\bar{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT564

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30		MHz
Propagation Delay, CLK to any $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23	
Output Enable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23	22 28	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23	22 28	
Output Disable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		19		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		19		28	
Pulse Width, CLK High or Low	$t_w$		9	15		18		ns
Setup Time, D before CLK†	$t_{su}$		9	14		17		ns
Hold Time, D after CLK†	$t_h$		0	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{OC} = V_{CC}$ $\bar{OC} = \text{GND}$	5 30					pF

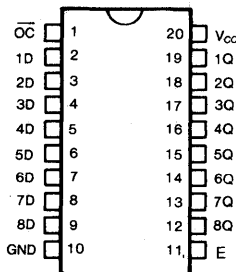
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

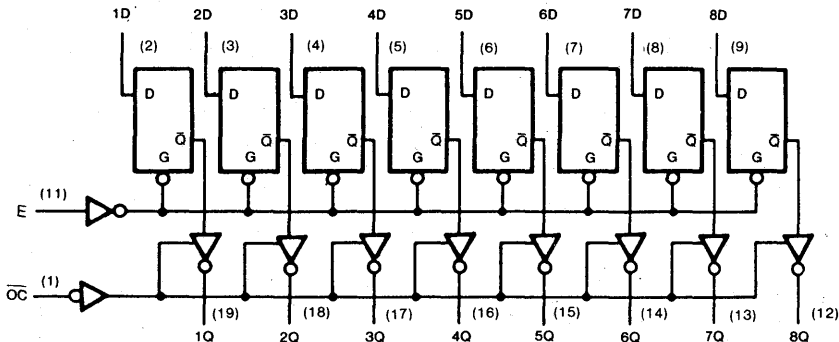
**FEATURES**

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compability with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C to } +85^{\circ}\text{C}$   
 KS54AHCT:  $-40^{\circ}\text{C to } +125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**DESCRIPTION**

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing bufer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable  $E$  is high, the  $Q$  outputs follow the data ( $D$ ) inputs. When the enable is low, the outputs latch at the levels that were set up at the  $D$  inputs.

The output buffers are controlled by a common signal ( $OC$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent of their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

(Each Latch)

Inputs			Output
$\overline{OC}$	$E$	$D$	$Q$
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature

Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT573

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, D to Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	9 12		16 19		20 23	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	9 12		16 19		20 23	
Propagation Delay, E to Q	$t_{PLH}$	$C = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		20 25		24 30	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15		20 25		24 30	
Output Enable Time OC to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23	22 28	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23	22 28	
Output Disable Time OC to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		19		22	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		19		22	
Pulse Width, E High	$t_w$		9	15		18		ns
Setup Time, D before E↓	$t_{su}$		6	10		12		ns
Hold Time, D after E↓	$t_h$		4	7		9		ns
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	$C_{PD}$	OC = $V_{CC}$	5					pF
		OC = GND	30					

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

4



**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current  
 (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

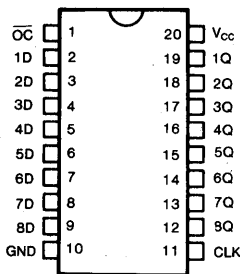
The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**PIN CONFIGURATION**

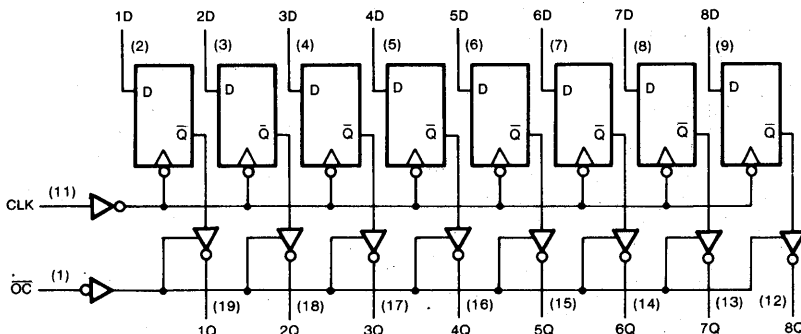


**FUNCTION TABLE**

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{STG}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
Power Dissipation Per Package,  $P_{D1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-1.2\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				Unit
			Typ	Guaranteed Limits			
			KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	$\text{mA}$

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT574)

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min		Max	
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30	MHz		
Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23		
Output Enable Time, $\overline{OC}$ to any Q	$t_{pZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	ns
	$t_{pZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	
Output Disable Time, $\overline{OC}$ to any Q	$t_{pHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns	
	$t_{pLZ}$	$C_L = 50\text{pF}$	13		18		22		
Pulse Width, CLK High or Low	$t_w$		9	15		18	ns		
Setup Time, D before CLK†	$t_{su}$		9	14		17	ns		
Hold Time, D after CLK†	$t_h$		-3	0		0	ns		
Input Capacitance	$C_{IN}$		5				pF		
Output Capacitance	$C_{OUT}$	Output Disabled	10				pF		
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5					pF	
		$\overline{OC} = \text{GND}$	30						

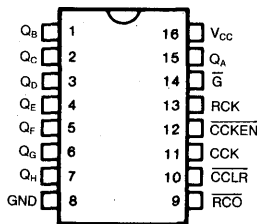
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Choice of 3-State ('590) and Open-Drain ('591) Outputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## FUNCTION TABLE

INPUTS					FUNCTION
$\bar{G}$	RCK	CCLR	CCKEN	CCK	
H	X	X	X	X	Q Outputs disable
L	X	X	X	X	Q Outputs enable
L		X	X	X	Counter data is stored into register
L		X	X	X	Register state is not changed
L	X	L	X	X	Counter clear
L	X	H	L		Advance one count
L	X	H	L		No count
L	X	H	H	X	No count

X: Don't care

$$RCO = Q_A' \cdot Q_B' \cdot Q_C' \cdot Q_D' \cdot Q_E' \cdot Q_F' \cdot Q_G' \cdot Q_H'$$

( $Q_A' \sim Q_H'$ : Internal outputs of the counter)

## DESCRIPTION

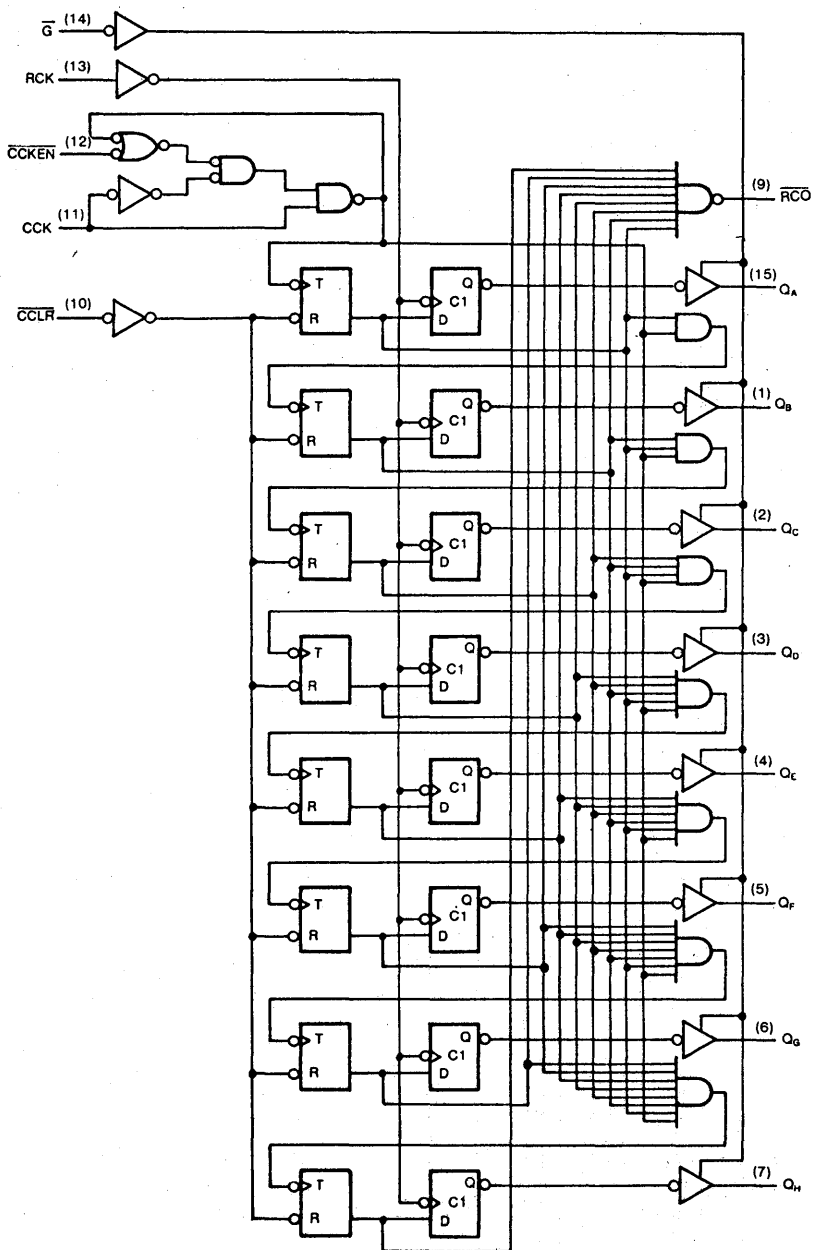
These devices each consist of an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out, RCO, will go low. This enables either synchronous cascading of the counters by connecting the RCO of the first stage to the CCKEN of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input,  $\bar{G}$ , is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage (All '590 Outputs and '591 RCO Output)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V		
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V		
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$		
Maximum Output Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$		
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$		
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA		

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT590

Characteristic	Symbol	Conditions†	54/74AHT	KS74AHT		54AHT		Unit	
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$ Typical	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
				Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$		50	30		25		ns	
Propagation Delay, CCK† to RCO	$t_{PLH}$	$C_L = 50\text{pF}$	15		25		29	ns	
	$t_{PHL}$		15		25		29		
Propagation Delay, CCLR† to RCO	$t_{PHL}$		17		28		33	ns	
Propagation Delay, RCK† to Q	$t_{PLH}$		10		16		19	ns	
	$t_{PHL}$		10		16		19		
Output Enable Time, $\bar{G}$ † to Q	$t_{PZH}$		$C_L = 50\text{pF}$ $R_L = 1\text{K}\Omega$	13		18		22	ns
	$t_{PZL}$	13			18		22		
Output Disable Time, $\bar{G}$ † to Q	$t_{PHZ}$	13			18		22	ns	
	$t_{PLZ}$	13			18		22		
Pulse Duration	CCK or RCK High or Low	$t_w$		10	15		20		ns
	$\bar{\text{CCLR}}$ Low			10	15		20		
Setup Time	$\bar{\text{CCKEN}}$ ‡ before CCK†	$t_{su}$	10	15		20		ns	
	$\bar{\text{CCLR}}$ † before CCK†		6	10		10			
	CCK† to RCK††		15	20		25			
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance (Q Outputs)	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT591

Characteristic	Symbol	Conditions†	54/74AHT	KS74AHT		54AHT		Unit
			$T_a = 25^\circ\text{C}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			$V_{CC} = 5\text{V}$	$V_{CC} = 5\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typical	Min	Max	Min	Max	
Maximum Clock Frequency	$f_{\text{max}}$	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$	50	30		25		MHz
Propagation Delay, CCK↑ to RCO	$t_{\text{PLH}}$		15		25		29	ns
	$t_{\text{PHL}}$		15		25		29	
Propagation Delay, CCLR↓ to RCO	$t_{\text{PHL}}$		17		28		33	ns
Propagation Delay, RCK↑ to Q	$t_{\text{PLH}}$		18		31		37	ns
	$t_{\text{PHL}}$		10		16		19	
Propagation Delay, $\bar{G}$ ↑ to Q	$t_{\text{PHL}}$		14		20		24	ns
Propagation Delay, $\bar{G}$ ↑ to $\bar{Q}$	$t_{\text{PLH}}$	14		20		24	ns	
Pulse Duration	CCK or RCK High or Low	$t_w$	10	15		20		ns
	CCLR Low		10	15		20		
Setup Time	CCKEN↓ Low to CCK↑	$t_{\text{su}}$	10	15		20		ns
	CCLR↑ High to CCK↑		6	10		10		
	CCK↑ to RCK↑††		15	20		25		
Input Capacitance	$C_{\text{IN}}$		5				pF	
Power Dissipation Capacitance*	$C_{\text{PD}}$						pF	

\*  $C_{\text{PD}}$  determines the no-load dynamic power dissipation:  $P_D = C_{\text{PD}} V_{CC}^2 f_{\text{in}}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

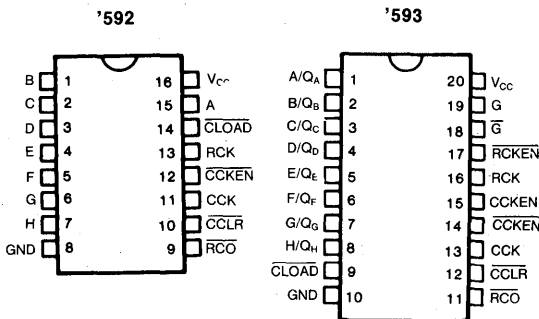
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## FEATURES

- Parallel Register Inputs ('592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)
- Counter Has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATIONS



## DESCRIPTION

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out,  $\overline{\text{RCO}}$ , will go low. This enables either synchronous cascading of the counters by connecting the  $\overline{\text{RCO}}$  or the first stage to the  $\overline{\text{CCKEN}}$  of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, CLOAD, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional I input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input,  $\bar{G}$ , is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin, CCKEN, which is active high and it also has an active low register clock enable, RCKEN.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

## FUNCTION TABLE

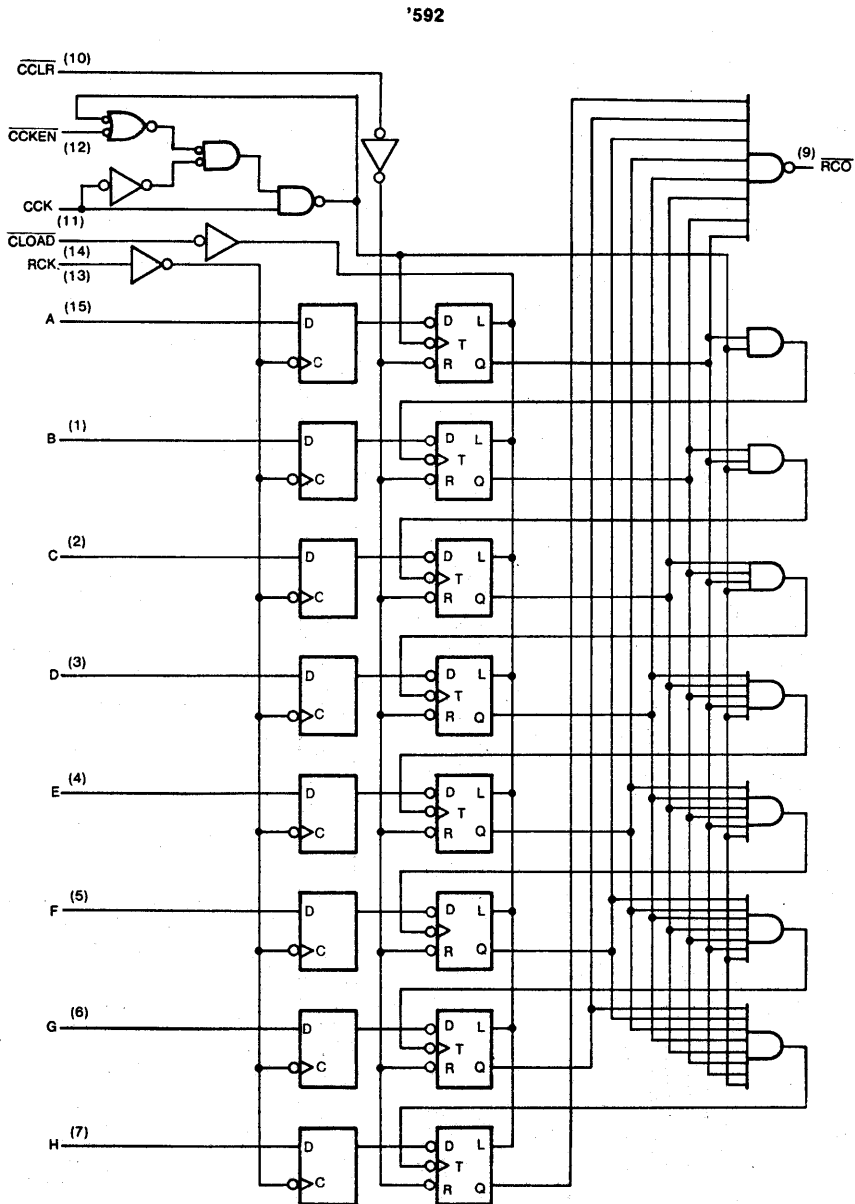
INPUTS ('592)					FUNCTION
RCK	CLOAD	CCLR	CCKEN	CCK	
X	L	H	X	X	Register data is loaded into counter
X	H	L	X	X	Counter clear
	H	H	X	X	The data of a thru H inputs is stored into register
	H	H	X	X	Register state is not changed
X	H	H	L		Counter advances the count
X	H	H	L		No count
X	H	H	H	X	No count

X: Don't care

$$\text{RCO} = Q_A' \cdot Q_B' \cdot Q_C' \cdot Q_D' \cdot Q_E' \cdot Q_F' \cdot Q_G' \cdot Q_H'$$

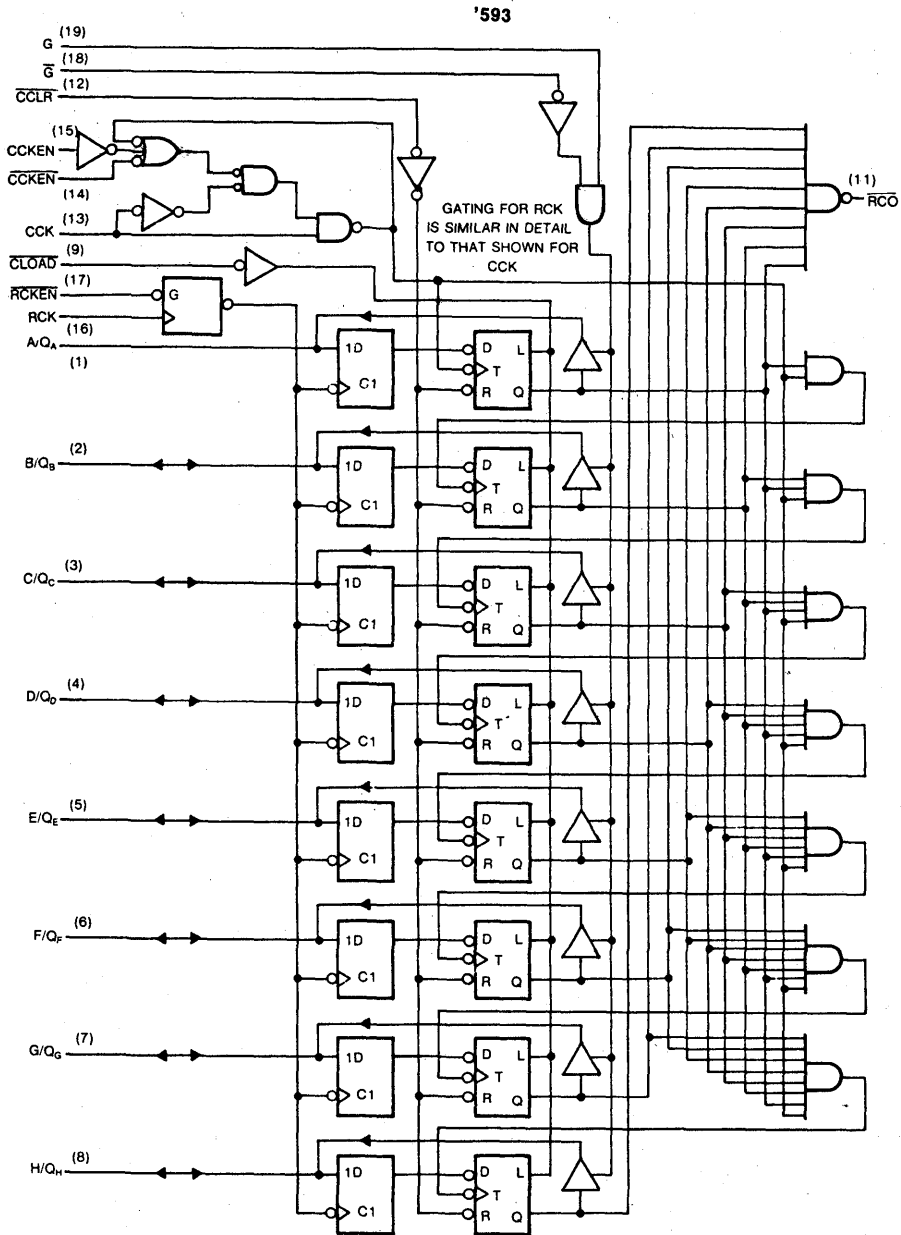
( $Q_A' \sim Q_H'$ : Internal outputs of the counter)

**LOGIC DIAGRAMS**



4

**LOGIC DIAGRAMS** (Continued)



## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$		$\pm 10.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0		160.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT592

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$			
			Typ	$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$			
			Min	Max	Min	Max			
Maximum Clock Frequency	$f_{max}$		50	30		25		MHz	
Propagation Delay, CCK↑ to $\overline{\text{RCO}}$	$t_{PLH}$	$C_L = 50\text{pF}$	15		25		29	ns	
	$t_{PHL}$		15		25		29		
Propagation Delay, $\overline{\text{CLOAD}}\downarrow$ to $\overline{\text{RCO}}$	$t_{PLH}$		15		25		29	ns	
	$t_{PHL}$		15		25		29		
Propagation Delay, CCLR↓ to $\overline{\text{RCO}}$	$t_{PHL}$			15		25		29	ns
Propagation Delay, RCK↑ to $\overline{\text{RCO}}$	$t_{PLH}$		$C_L = 50\text{pF}$	18		30		36	ns
	$t_{PHL}$	$\overline{\text{CLOAD}} = \text{GND}$	18		30		36		
Pulse Width	CCK or RCK High or Low	$t_w$	10	15		20		ns	
	$\overline{\text{CCLR}}$ Low		10	15		20			
	$\overline{\text{CLOAD}}$ Low		10	15		20			
Setup Time	$\overline{\text{CCKEN}}\downarrow$ before CCK↑	$t_{su}$	10	15		20		ns	
	$\overline{\text{CCLR}}\uparrow$ before CCK↑		6	10		10			
	RCK↑ before $\overline{\text{CLOAD}}\uparrow\uparrow$		10	15		20			
	Data A-H↑ before RCK↑		10	15		20			
Hold Time	$t_h$		-3	0		0		ns	
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$		.					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to  $\overline{\text{CLOAD}}$  setup time ensures that the counter will see stable data from the register output.

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns, AHCT593)

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min		Max	
Maximum Clock Frequency	$f_{max}$		50	30		25	MHz		
Propagation Delay, CCK† to Q	$t_{PLH}$	$C_L = 50\text{pF}$	15		25		29	ns	
		$C_L = 150\text{pF}$	18		30		35		
Propagation Delay, CCK† to $\overline{RCO}$	$t_{PHL}$	$C_L = 50\text{pF}$	15		25		29	ns	
		$C_L = 150\text{pF}$	18		30		35		
Propagation Delay, $\overline{CLOAD}\dagger$ to Q	$t_{PLH}$	$C_L = 50\text{pF}$	15		25		29	ns	
		$C_L = 150\text{pF}$	18		30		35		
Propagation Delay, $\overline{CLOAD}\dagger$ to $\overline{RCO}$	$t_{PHL}$	$C_L = 50\text{pF}$	15		25		29	ns	
		$C_L = 150\text{pF}$	18		30		35		
Propagation Delay, RCK† to $\overline{RCO}$	$t_{PLH}$	$C_L = 50\text{pF}$	18		30		36	ns	
		$\overline{CLOAD} = \text{GND}$	18		30				
Propagation Delay, $\overline{CCLR}\dagger$ to Q	$t_{PHL}$	$C_L = 50\text{pF}$	15		25		29	ns	
		$C_L = 150\text{pF}$	18		30		35		
Propagation Delay, $\overline{CCLR}\dagger$ to $\overline{RCO}$	$t_{PLH}$	$C_L = 50\text{pF}$	15		25		29	ns	
		$C_L = 150\text{pF}$	18		30		35		
Enable Time, $\overline{G}\dagger$ or $\overline{G}\dagger$ to Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	13		20		24	ns
			$C_L = 150\text{pF}$	16		25		30	
	$t_{PZL}$	$C_L = 50\text{pF}$	$C_L = 50\text{pF}$	13		20		24	
			$C_L = 150\text{pF}$	16		25		30	
Disable Time, $\overline{G}\dagger$ or $\overline{G}\dagger$ to Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		20		24	ns	
		$C_L = 50\text{pF}$	13		20		24		
Pulse Width	CCK or RCK High or Low	$t_w$		10	15		20	ns	
			$\overline{CCLR}$ Low	10	15		20		
			$\overline{CLOAD}$ Low	10	15		20		
Setup Time	CCKEN† before CCK†	$t_{su}$		10	15		20	ns	
			RCKEN† to RCK†	10	15		20		
			$\overline{CCLR}\dagger$ before CCK†	6	10		10		
			RCK† before $\overline{CLOAD}\dagger$	10	15		20		
			Data A-H before RCK†	10	15		20		
Hold Time	$t_h$		-3	0		0	ns		
Input Capacitance	$C_{IN}$		5				pF		
Output Capacitance	$C_{OUT}$	Output Disabled	10				pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK† to  $\overline{CLOAD}$  setup time ensures that the counter will see stable data from the register output.

## FEATURES

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage.
- Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs.
- Shift Register Has Direct Clear.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

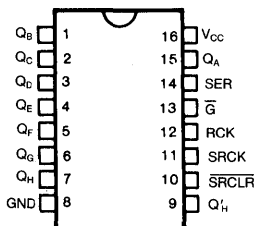
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or open-drain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

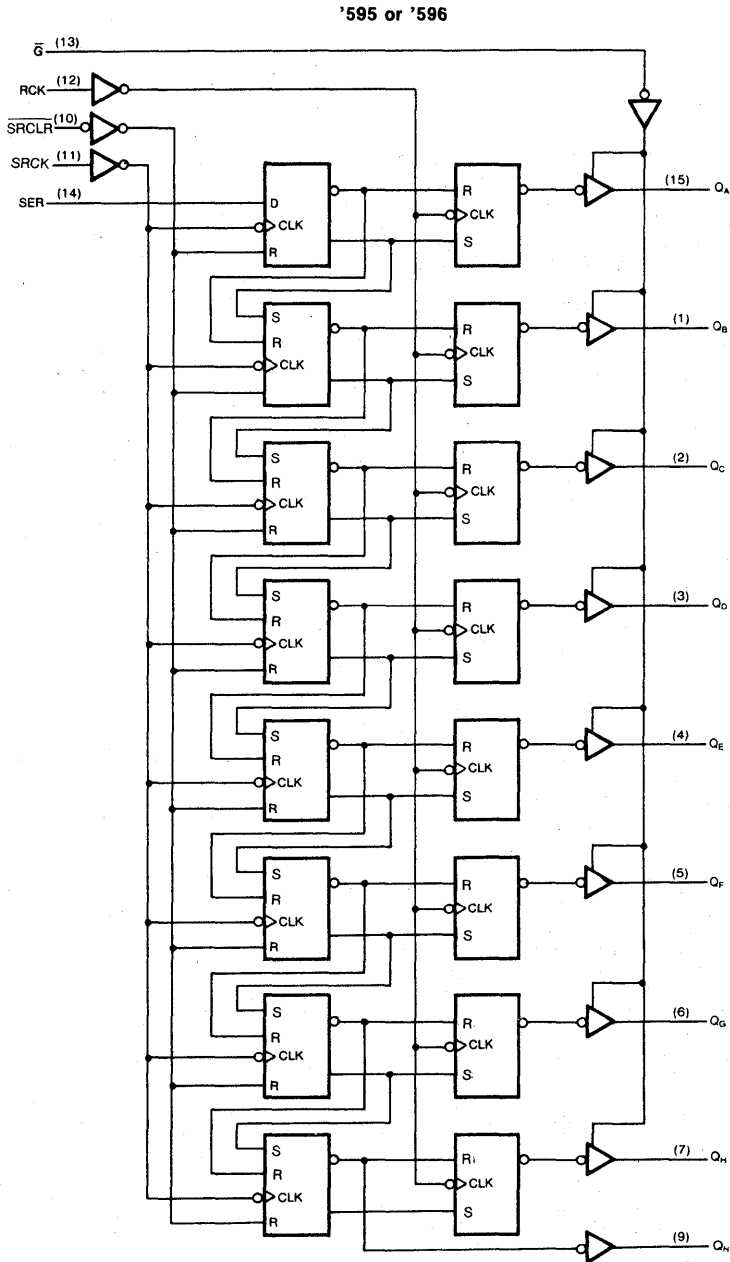


## FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCK	SRCLR	RCK	G-bar	
X	X	X	X	H	$Q_A$ thru $Q_H$ outputs disable
X	X	X	X	L	$Q_A$ thru $Q_H$ outputs enable
X	X	L	X	X	Shift register is cleared.
L		H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H		H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X		H	X	X	State of S.R. is not changed.
X	X	X		X	S.R. data is stored into storage register.
X	X	X		X	Storage register state is not changed.

X: DON'T CARE

**LOGIC DIAGRAM**



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**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
(-0.5V <  $V_O$  <  $V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '595 Outputs and '596 QH' Output)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_C=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_C=12mA$ $I_C=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT595, AHCT596

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$ Typ	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
				Min	Max	Min	Max	
				Propagation Delay, SRCK† to Q <sub>H</sub>	t <sub>PLH</sub> t <sub>PHL</sub>	C <sub>L</sub> = 50pF	15	
Propagation Delay, RCK† to Q <sub>A</sub> thru Q <sub>H</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	11	22		27	ns	
		C <sub>L</sub> = 150pF	14	21		25		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	11	17		20		
		C <sub>L</sub> = 150pF	14	22		26		
Output Enable Time, Ḡ† to Q <sub>A</sub> thru Q <sub>H</sub> (*595 only)	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	14	20		24	ns
			C <sub>L</sub> = 150pF	17	25		30	
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	14	20		24		
		C <sub>L</sub> = 150pF	17	25		30		
Output Disable Time, Ḡ† to Q <sub>A</sub> thru Q <sub>H</sub> (*595 only)	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	14	20		24	ns	
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	14	20		24		
Propagation Delay, Ḡ† to Q <sub>A</sub> thru Q <sub>H</sub> (*596 only)	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	14	20		24	ns	
		C <sub>L</sub> = 150pF	17	25		30		
Propagation Delay, Ḡ† to Q <sub>A</sub> thru Q <sub>H</sub> (*596 only)	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	14	20		24	ns	
		C <sub>L</sub> = 150pF	17	25		30		
Pulse Width	SRCK or RCK	t <sub>w</sub>	10	15		20	ns	
	SRCLR Low		10	15		20		
Setup Time	SRCLR† to SRCK†	t <sub>su</sub>	6	10		12	ns	
	SER to SRCK†		10	15		20		
	SRCK† to RCK††		15	20		25		
Hold Time,	t <sub>h</sub>		-3	0		0	ns	
Input Capacitance	C <sub>IN</sub>		5				pF	
Output Capacitance	C <sub>OUT</sub>	Output Disabled	10				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>						pF	

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

Note: The RCK† to CCK† setup time ensures that the counter will see stable data from the register output.

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## FEATURES

- 8-Bit Parallel Storage Register Inputs
- shift Register has Direct Overriding Load and Clear.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

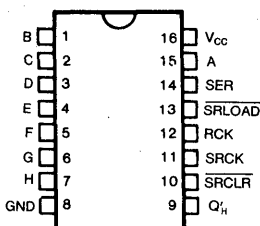
## DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

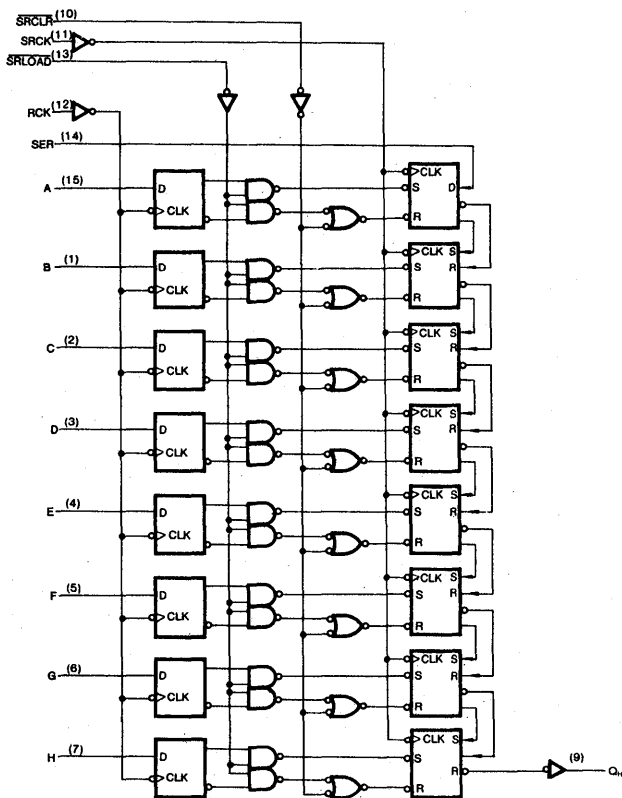
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION



## LOGIC DIAGRAM



**FUNCTION TABLE**

INPUTS					FUNCTION
SER	SRCK	SRCLR	SRLOAD	RCK	
X	X	L	H	X	S.R. is cleared to "L"
X	X	H	J	X	Input register data is stored into S.R.
L		H	H	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H		H	H	X	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
X	X	X	X		State of S.R. is not changed.
X	X	X	X		Input data on A~H line is stored into input register
X	X	X	X		Storage register state is not changed.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4 mA$ $I_O = 8 mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$	8.0	80.0	160.0	$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$	2.7	2.9	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT597

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$			
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	$f_{max}$		50	30		25		MHz	
Propagation Delay, SRCK↑ to Q'H	$t_{PLH}$	$C_L = 50\text{pF}$	15		17		20	ns	
	$t_{PHL}$		15		17		20		
Propagation Delay, SRLOAD↓ to Q'H	$t_{PLH}$		14		20		24	ns	
	$t_{PHL}$		14		20		24		
Propagation Delay, SRCLR↓ to Q'H	$t_{PHL}$			11		18		21	ns
Propagation Delay, RCK↑ to Q'H	$t_{PLH}$		$C_L = 50\text{pF}$ SLOAD=Low	15		25		29	ns
	$t_{PHL}$	15			25		29		
Pulse Width	RCK or SRCK High or Low	$t_w$	10	15			20	ns	
	SRCLR or SRLOAD Low		10	15		20			
Setup Time	SRCLR↑ before SRCK↑	$t_{su}$	6	10		12		ns	
	RCK↑ before SRCK↑††		15	20		25			
	SER before SRCK↑		10	15		20			
	A thru H before RCK↑		10	15		20			
Hold Time	$t_h$		-3	0		0		ns	
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

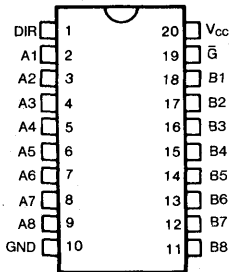
**DESCRIPTION**

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

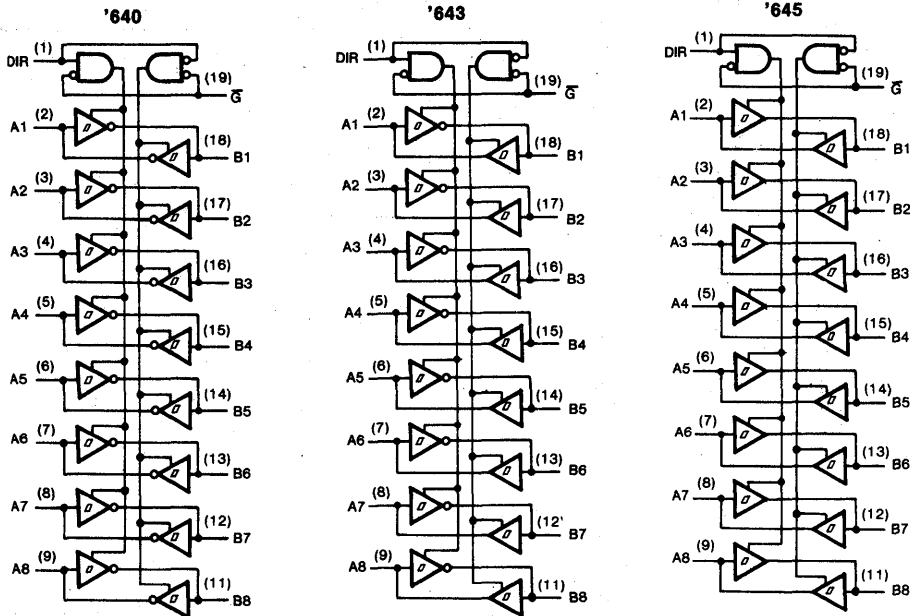


**FUNCTION TABLE**

Control Inputs		Operation		
$\bar{G}$	DIR	'640	'643	'645
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A
L	H	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B
H	X	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)



LOGIC DIAGRAMS



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long-exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 5.0$	$\pm 10.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	80.0	160.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	2.9	3.0	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns, AHCT640, AHCT643)

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit	
			$V_{CC} = 5.0\text{V}$	$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Propagation Delay, A to B, or B to A	$t_{PLH}$	$C_L = 50\text{pF}$	7		12		14	ns	
		$C_L = 150\text{pF}$	10		17		20		
	$t_{PHL}$	$C_L = 50\text{pF}$	7		12		14	ns	
		$C_L = 150\text{pF}$	10		17		20		
Output Enable Time, G to A or B	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	12		20		25	ns
			$C_L = 150\text{pF}$	15		25		31	
			$C_L = 50\text{pF}$	12		20		25	
	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 150\text{pF}$	15		25		31	ns
			$C_L = 50\text{pF}$	12		20		25	
Output Disable Time, G to A or B	$t_{PHZ}$	$R_L = 1\text{k}\Omega$		13		18		22	ns
			$C_L = 50\text{pF}$	13		18		22	
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}^*$	$\bar{G} = V_{CC}$ (per stage) $\bar{G} = \text{GND}$		5					pF
				30					

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT645

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, A to B, or B to A	$t_{PLH}$	$C_L = 50\text{pF}$	6		10		14	ns
		$C_L = 150\text{pF}$	9		19		25	
	$t_{PHL}$	$C_L = 50\text{pF}$	6		10		14	ns
		$C_L = 150\text{pF}$	9		19		25	
Output Enable Time G to A or B	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	12		20	25	ns
			$C_L = 150\text{pF}$	18		29	36	
	$t_{PZL}$	$C_L = 50\text{pF}$	12		20	25		
			$C_L = 150\text{pF}$	18		29	36	
Output Disable Time, G to A or B	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18	22	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18	22		
Input Capacitance	$C_{IN}$		5				pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10				pF	
Power Dissipation Capacitance*	$C_{PD}^*$	$\bar{G} = V_{CC}$ (per stage)	5				pF	
		$\bar{G} = \text{GND}$	30					

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

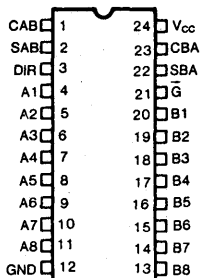
# KS54AHCT 646/648 KS74AHCT

# Octal 3-State Bus Transceivers with Registers

## FEATURES

- 8 bi-directional data paths
- Transmits direct or stored data in either direction
- 24-pin slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## DESCRIPTION

The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

$\bar{G}$  (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.

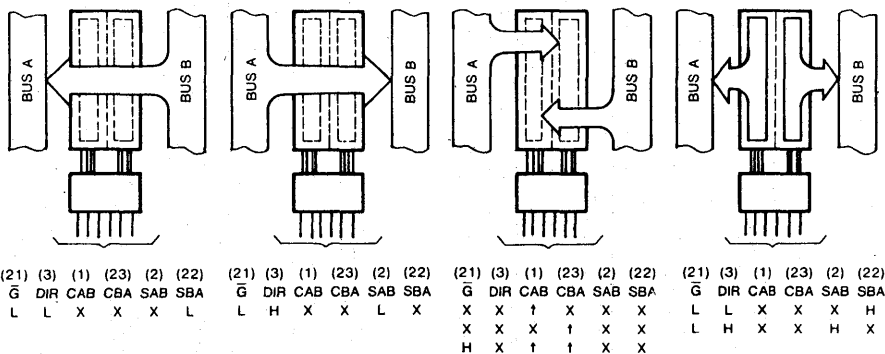
DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.

SAB, SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.

CAB, CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the  $\bar{G}$  and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.



Real-Time transfer  
bus B to bus A

Real-Time transfer  
bus A to bus B

Storage from  
A AND/OR B

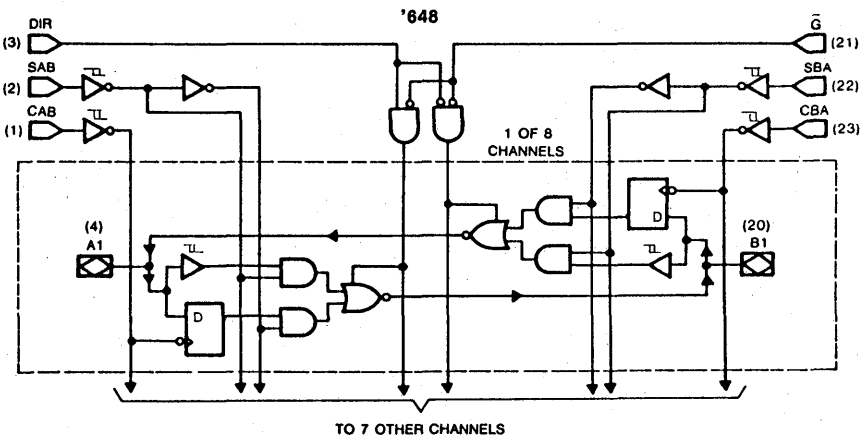
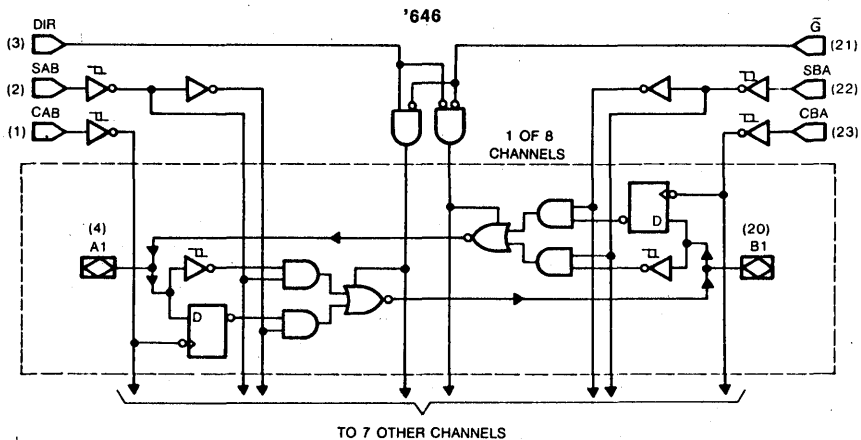
Transfer stored data  
to A AND/OR B

**FUNCTION TABLE**

Inputs						Data I/O*		Operation or Function	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648
X	X	↑	X	X	X	input	input <sup>†</sup>	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Not specified	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B data to A bus Stored B data to A bus	Real-Time $\bar{B}$ data to A bus Stored $\bar{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Real-Time B data to A bus Stored B data to A bus	Real-Time $\bar{B}$ data to A bus Stored $\bar{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-Time A data to B bus Stored A data to B bus	Real-Time $\bar{A}$ data to B bus Stored $\bar{A}$ data to B bus
L	H	H or L	X	H	X	Input	Output	Real-Time A data to B bus Stored A data to B bus	Real-Time $\bar{A}$ data to B bus Stored $\bar{A}$ data to B bus

\*The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f < 2$  ns), AHCT646, AHCT648

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Frequency	$f_{max}$	$C_L = 50\text{pF}$	45		30		25	MHz
Propagation Delay, A or B Input to B or A Output	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	
Propagation Delay, CBA or CAB Input to A or B Output	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		25 30		30 36	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		25 30		30 36	
Propagation Delay,†† SBA or SAB Input to A or B Output (with A or High)	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	16 19		27 33		32 38	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	16 19		27 33		32 38	
Propagation Delay,†† SBA or SAB Input to A or B Output (with A or Low)	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		25 30		30 36	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18		25 30		30 36	
Out Enable Time, $\bar{G}$ or DIR Input to A or B Output	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17	22 27		26 32	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17	22 27		26 32	
Output Disable Time, $\bar{G}$ or DIR Input to A or B Output	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		22		26	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		22		26	
Pulse Duration, Clocks High or low	$t_w$		8	12		15		ns
Set up Time, A before CAB† or B before CBA†	$t_{su}$		8	12		15		ns
Hold Time, A after CAB† or B after CBA†	$t_h$		0	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

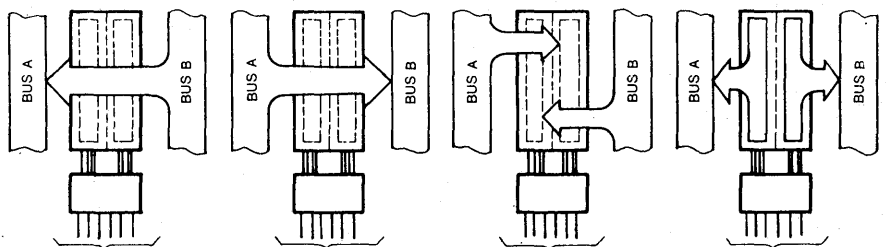
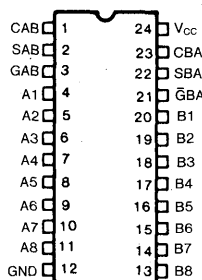
† For AC switching test circuits and timing waveforms see section 2.

†† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

**FEATURES**

- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored-Data
- Choice of Time and Inverting Data Paths
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



(3)	(21)	(1)	(23)	(2)	(22)	(3)	(21)	(1)	(23)	(2)	(22)	(3)	(21)	(1)	(23)	(2)	(22)
GAB	GBA	CAB	CBA	SAB	SBA	GAB	GBA	CAB	CBA	SAB	SBA	GAB	GBA	CAB	CBA	SAB	SBA
L	L	X	X	X	L	H	H	X	X	L	X	X	X	↑	X	X	X
X	X	X	X	↑	X	X	X	↑	X	X	X	L	H	X	X	H	X
H	X	↑	↑	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Real-Time transfer bus B to bus A

Real-Time transfer bus A to bus B

Storage from A AND/OR B

Transfer stored data TO A AND/OR B

**DESCRIPTION**

These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and  $\bar{G}BA$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and  $\bar{G}BA$ . In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

FUNCTION TABLE

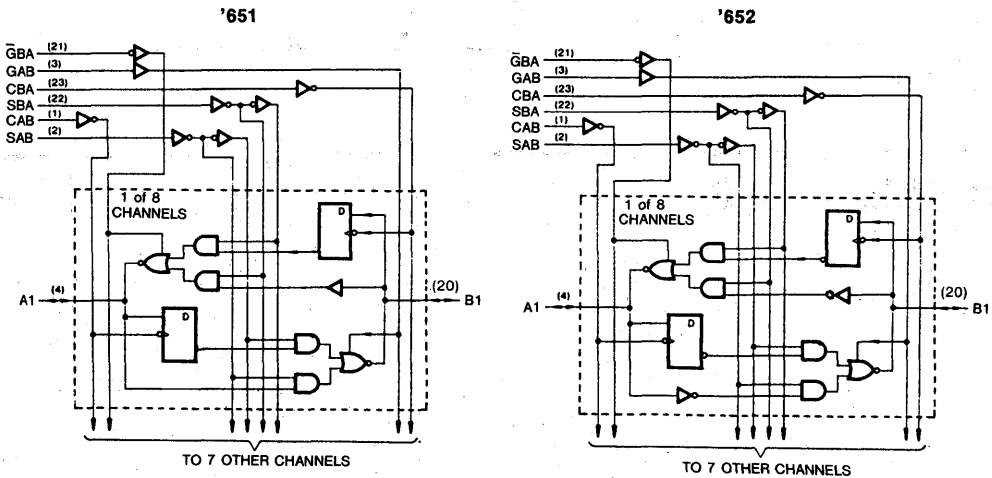
INPUTS				DATA I/O*				OPERATION OR FUNCTION	
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'651	'652
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L	H	$\uparrow$	$\uparrow$	X	X	Input	Not specified	Store A, Hold B Store A in both registers	Store A Hold B Store A in both registers
X	H	$\uparrow$	H or L	X	X	Input	Output*	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers
H	H	$\uparrow$	$\uparrow$	X**	X	Not specified	Input	Real-Time $\bar{B}$ Data to A Bus Stored $\bar{B}$ Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus
L	X	H or L	$\uparrow$	X	X	Not specified	Input	Real-Time $\bar{A}$ Data to B Bus Stored $\bar{A}$ Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus
L	L	$\uparrow$	$\uparrow$	X	X**	Output	Input	Stored $\bar{A}$ Data to B Bus and Stored $\bar{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

\* The data output functions may be enabled or disabled by various signals at the GAB and  $\bar{G}BA$  inputs. Data input functions are always enabled, ie., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

\*\* Select control=L: clocks can occur simultaneously

Select control=H: clocks must be staggered in order to load both registers

LOGIC DIAGRAMS



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  .....  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ...  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

4



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT651, AHCT652

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%			T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Min	Max	Min		Max	
Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	45	30		25		MHz	
Propagation Delay, A or B Input to B or A Output	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	11		18		22	ns	
		C <sub>L</sub> = 150pF	14		23		28		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	11		18		22		
		C <sub>L</sub> = 150pF	14		23		28		
Propagation Delay, CBA or CAB Input to A or B Output	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15		25		30	ns	
		C <sub>L</sub> = 150pF	18		30		36		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	15		25		30		
		C <sub>L</sub> = 150pF	18		30		36		
Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	16		27		32	ns	
		C <sub>L</sub> = 150pF	19		32		38		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	16		27		32		
		C <sub>L</sub> = 150pF	19		32		38		
Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15		25		30	ns	
		C <sub>L</sub> = 150pF	18		30		36		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	15		25		30		
		C <sub>L</sub> = 150pF	18		30		36		
Output Enable Time, G <sub>BA</sub> to A or G <sub>AB</sub> to B	t <sub>PZL</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	19		32		38	ns
			C <sub>L</sub> = 150pF	22		37		44	
	t <sub>PZH</sub>	C <sub>L</sub> = 50pF	19		32		38		
		C <sub>L</sub> = 150pF	22		37		44		
Output Disable Time, G <sub>BA</sub> to A or G <sub>AB</sub> to B	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	13		22		26	ns	
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	13		22		26		
Pulse Width Clocks High or Low	t <sub>w</sub>		8	12		15		ns	
Setup Time, A before CAB† or B before CBA†	t <sub>su</sub>		8	12		15		ns	
Hold Time, A after CAB† or B after CBA†	t <sub>h</sub>		0	0		0		ns	
Maximum Input Capacitance	C <sub>IN</sub>		5					pF	
maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>							pF	

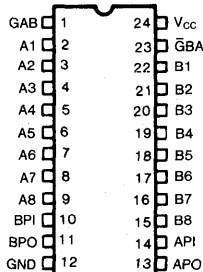
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Bus Transceivers with Inverting Outputs ('658) or True Outputs ('659)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and  $\bar{G}BA$ . These devices also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

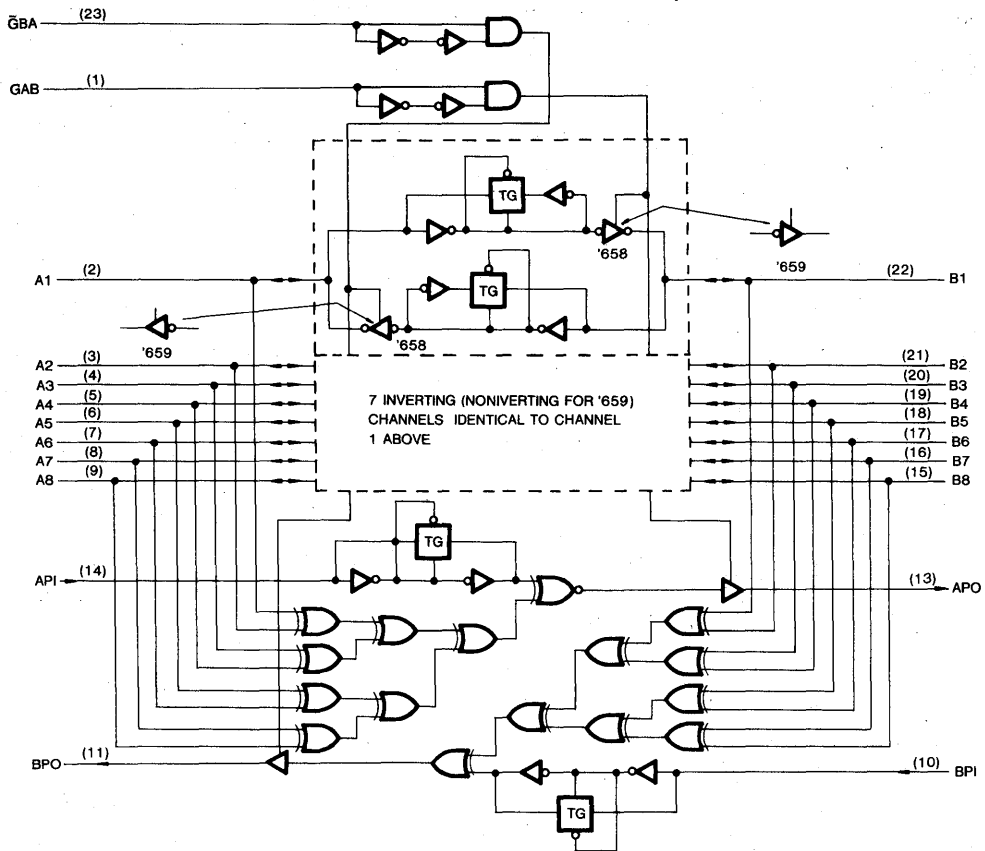
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.



**FUNCTION TABLE**

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\bar{G}BA$	GAB			APO	BPO	'658	'659
L	L	X	0, 2, 4, 6, 8	Z	H	$\bar{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
H	H	0, 2, 4, 6, 8	X	H	Z	$\bar{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	L	X	X	Z	Z	Isolation	Isolation
		X	0, 2, 4, 6, 8		H		
L	H	X	1, 3, 5, 7, 9		L	$\bar{B}$ Data to A Bus, $\bar{A}$ Data to B Bus	B Data to A Bus, A Data to B Bus
		0, 2, 4, 6, 8	X	H			
		1, 3, 5, 7, 9	X	L			

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74AHCT T <sub>a</sub> = -40°C to +85°C		KS54AHCT T <sub>a</sub> = -55°C to +125°C		Unit
			Typ		Guaranteed Limits				
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20μA I <sub>O</sub> = -6mA	V <sub>CC</sub> 4.2	V <sub>CC</sub> - 0.1 3.98	V <sub>CC</sub> - 0.1 3.84	V <sub>CC</sub> - 0.1 3.7			V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20μA I <sub>O</sub> = 12mA I <sub>O</sub> = 24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0			μA
Maximum 3-State Leakage Current	I <sub>OZ</sub>	Output Enable = V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0			μA
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0			μA
Additional Worst Case Supply Current	ΔI <sub>CC</sub>	per input pin V <sub>I</sub> = 2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0			mA

4

### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub> ≤ 2 ns, AHCT658, AHCT659)

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74AHCT T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54AHCT T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Typ		Min	Max	Min	Max	
			Propagation Delay, A or B to B or A		t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11 14	18 23	
		t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11 14	18 23	22 28	22 28		
Propagation Delay, A or B to APO or BPO		t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	16 19	27 32	32 38	32 38	ns	
		t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	16 19	27 32	32 38	32 38		
Propagation Delay, API or BPI to APO or BPO		t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11 14	18 23	22 28	22 28	ns	
		t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11 14	18 23	22 28	22 28		
Enable Time, GAB or GBA to APO or BPO		t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	16 19	27 32	32 38	ns	
		t <sub>PZL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	16 19	27 32	32 38		
Disable Time, GAB or GBA to APO or BPO		t <sub>PLZ</sub>	R <sub>L</sub> = 1kΩ	16	27	32	ns		
		t <sub>PHZ</sub>	C <sub>L</sub> = 50pF	16	27	32			
Input Capacitance	C <sub>IN</sub>			5				pF	
Output Capacitance	C <sub>OUT</sub>							pF	
Power Dissipation Capacitance*	C <sub>PD</sub>							pF	

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

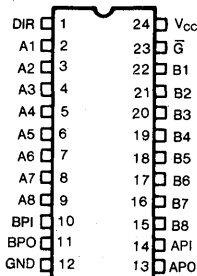
These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input,  $\bar{G}$ , can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

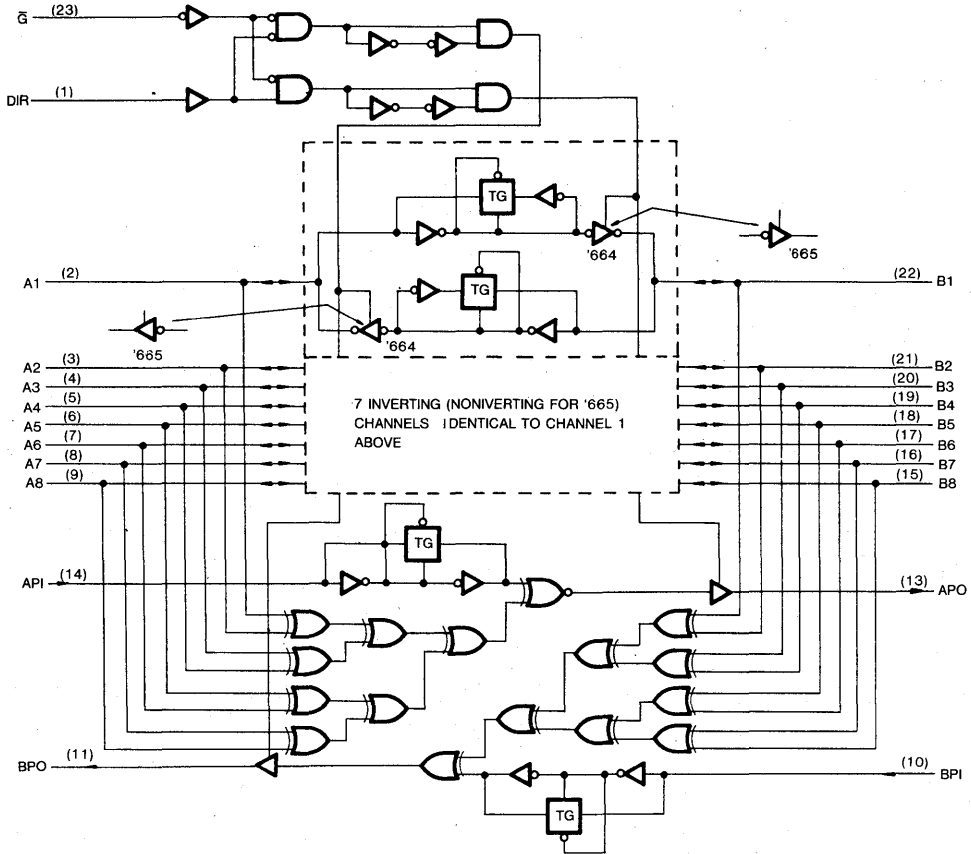
**PIN CONFIGURATION**



**FUNCTION TABLE**

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\bar{G}$	DIR			APO	BPO	'664	'665
L	L	X	0, 2, 4, 6, 8	Z	H	$\bar{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\bar{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA
- Storage Temperature Range,  $T_{STG}$  . . . . . -65°C to +150°C
- Power Dissipation Per Package,  $P_d$ ! . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

! Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$
- Operating Temperature  
Range KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT664, AHCT665

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay, A or B to B or A	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	11		18		22	ns
		C <sub>L</sub> = 150pF	14		23		28	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	11		18		22	ns
		C <sub>L</sub> = 150pF	14		23		28	
Propagation Delay, A or B to APO or BPO	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	16		27		32	ns
		C <sub>L</sub> = 150pF	19		32		38	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	16		27		32	ns
		C <sub>L</sub> = 150pF	19		32		38	
Propagation Delay, API or BPI to APO or BPO	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	11		18		22	ns
		C <sub>L</sub> = 150pF	14		23		28	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	11		18		22	ns
		C <sub>L</sub> = 150pF	14		23		28	
Output Enable Time, G to A or B	t <sub>PZH</sub>	C <sub>L</sub> = 50pF	16		27		32	ns
		C <sub>L</sub> = 150pF	19		32		38	
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	16		27		32	ns
		C <sub>L</sub> = 150pF	19		32		38	
Output Disable Time, G to A or B	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	16		27		32	ns
		C <sub>L</sub> = 50pF	16		27		32	
	t <sub>PLZ</sub>	R <sub>L</sub> = 1kΩ	16		27		32	ns
		C <sub>L</sub> = 50pF	16		27		32	
Output Enable Time, DIR to A or B	t <sub>PZH</sub>	C <sub>L</sub> = 50pF	16		27		32	ns
		C <sub>L</sub> = 150pF	19		32		38	
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	16		27		32	ns
		C <sub>L</sub> = 150pF	19		32		38	
Output Disable Time, DIR to A or B	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	16		27		32	ns
		C <sub>L</sub> = 50pF	16		27		32	
	t <sub>PLZ</sub>	R <sub>L</sub> = 1kΩ	16		27		32	ns
		C <sub>L</sub> = 50pF	16		27		32	
Input Capacitance	C <sub>IN</sub>		5				pF	
Output Capacitance	C <sub>OUT</sub>	Output Disabled					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>						pF	

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

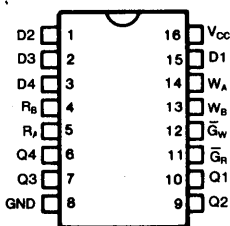
† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Separate Read Write Addressing Permits Simultaneous Reading and Writing
- Expandable to 512 Words of 7-bits
- For use as:
  - Scratch pad memory
  - Buffer Storage between processors
  - Bit storage in fast multiplication designs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLES**

**WRITE MODE SELECT TABLE**

OPERATING MODE	INPUTS		INTERNAL LATCHES <sup>(a)</sup>
	$\bar{G}_W$	$D_n$	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE:

a. The Write Address ( $W_A$  and  $\bar{W}_B$ ) to the "internal latches" must be stable while  $\bar{G}_W$  is LOW for conventional operation.

**DESCRIPTION**

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs ( $W_A$  and  $W_B$ ) determine the location of the stored word. When the Write Enable ( $\bar{G}_W$ ) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the  $\bar{G}_W$  is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when  $\bar{G}_W$  is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs ( $R_A$  and  $R_B$ ). The addressed word appears at the four outputs when the Read Enable ( $\bar{G}_R$ ) is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the  $I_{OH}$  current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

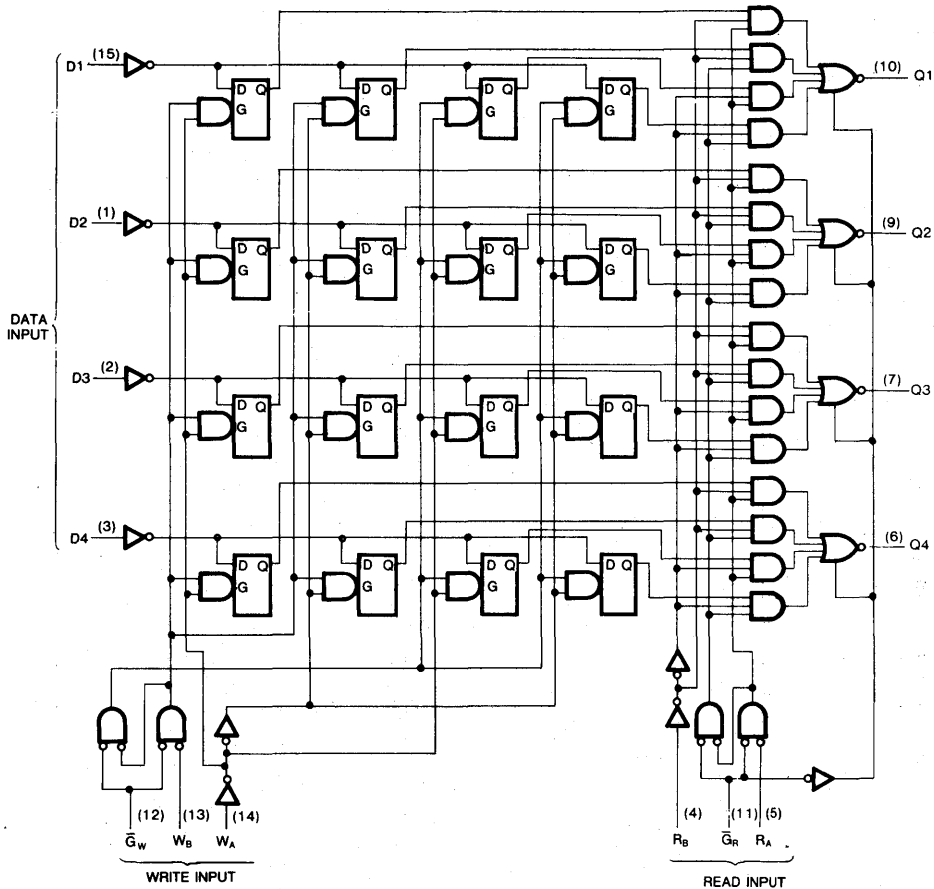
**READ MODE SELECT TABLE**

OPERATING MODE	INPUTS		OUTPUT $Q_n$
	$\bar{G}_R$	INTERNAL LATCHES <sup>(b)</sup>	
Read	L	L	L
	L	H	H
Disabled	H	H	(Z)

NOTE:

b. The selection of the "internal latches" by Read Address ( $\bar{R}_A$  and  $R_B$ ) are not constrained by  $\bar{G}_W$  or  $\bar{G}_R$  operation.

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA
- Storage Temperature Range,  $T_{STG}$  . . . . . -65°C to +150°C
- Power Dissipation Per Package,  $P_{D\uparrow}$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$
- Operating Temperature  
Range . . . . . KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits			
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT670

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C	KS74AHCT		KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		
			Typ	Min	Max	Min	Max	
Maximum Propagation Delay, R <sub>A</sub> or R <sub>B</sub> to Output	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	14		23		23	ns
		C <sub>L</sub> = 150pF	17		28		34	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	14		23		28	ns
		C <sub>L</sub> = 150pF	17		28		34	
Propagation Delay, G <sub>W</sub> to Output	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15		25		30	ns
		C <sub>L</sub> = 150pF	18		30		36	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	15		25		30	ns
		C <sub>L</sub> = 150pF	18		30		36	
Propagation Delay, Data to Output	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	14		23		28	ns
		C <sub>L</sub> = 150pF	17		28		34	
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	14		23		28	ns
		C <sub>L</sub> = 150pF	17		28		34	
Output Enable Time G <sub>R</sub> to Output	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	13		21	25	ns
			C <sub>L</sub> = 150pF	16		26	31	
	t <sub>PZL</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	13		21	25	ns
			C <sub>L</sub> = 150pF	16		26	31	
Output Disable Time G <sub>R</sub> to Output	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	17		28		34	ns
	t <sub>PLZ</sub>	C <sub>L</sub> = 150pF	17		28		39	
Set up Time	t <sub>SU</sub>	D <sub>n</sub> to G <sub>W</sub>	6	10		12		ns
		W <sub>A</sub> , W <sub>B</sub> to G <sub>W</sub>	10	14		16		
Hold Time	t <sub>H</sub>	D <sub>n</sub> to G <sub>W</sub>	0	0		0		ns
		W <sub>A</sub> , W <sub>B</sub> to G <sub>W</sub>	0	0		0		
Input Capacitance	C <sub>IN</sub>		5					pF
Output Capacitance	C <sub>OUT</sub>	Output disabled	10					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>

† For AC switching test circuits and timing waveforms see section 2.

4

**FEATURES**

- '679: 12-bit to 4-bit comparator with enable
- '680: 12-bit to 4-bit comparator with latch
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

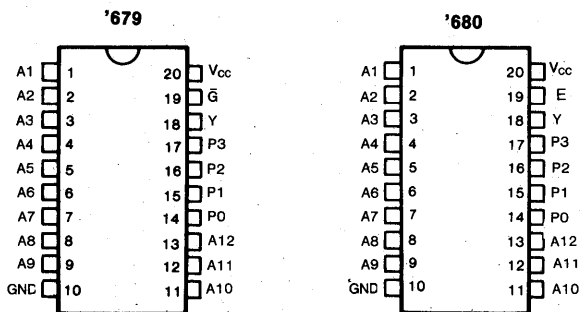
The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The '679 features an enable input ( $\bar{G}$ ). When  $\bar{G}$  is low, the device is enabled. When  $\bar{G}$  is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (E). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

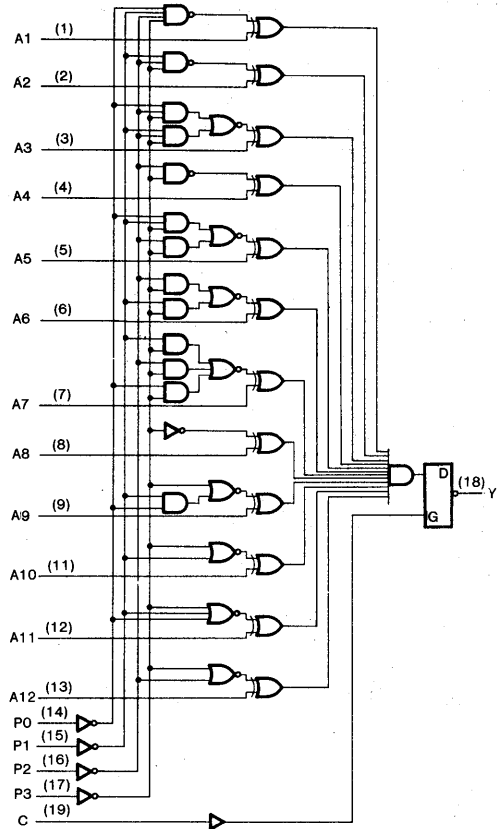
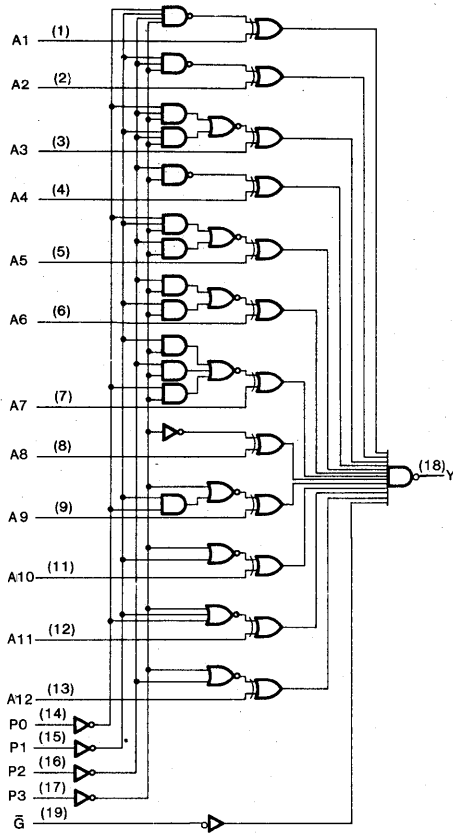
**PIN CONFIGURATIONS**



LOGIC DIAGRAMS

'679

'680



4

**FUNCTION TABLE**

'679 G	'680 E	INPUTS COMMON TO '679 AND '680												OUTPUT Y				
		P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8		A9	A10	A11	A12
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L*
L	H	L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L*
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L*
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations															H	
H		'679: Any combination															H	
	L	'680: Any combination															Latched	

Note: These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
 $(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$  ..... ±20 mA
- DC Output Diode Current,  $I_{OK}$   
 $(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$  ..... ±20 mA
- Continuous Output Current Per Pin,  $I_O$   
 $(-0.5V < V_O < V_{CC} + 0.5V)$  ..... ±70 mA
- Continuous Current Through  
 $V_{CC}$  or GND pins ..... ±250 mA
- Storage Temperature Range,  $T_{STG}$  ..... -65°C to +150°C
- Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V
  - DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$
  - Operating Temperature  
 Range  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C
  - Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ		Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84		$V_{CC}-0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$		$\pm 10.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0		160.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT679

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			$V_{CC}=5.0\text{V}$	$V_{CC}=5.0\text{V} \pm 10\%$		$V_{CC}=5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Any P to Y	$t_{PLH}$	$C_L=50\text{pF}$	18		30		36	ns
		$C_L=150\text{pF}$	21		35		42	
	$t_{PHL}$	$C_L=50\text{pF}$	18		30		36	ns
		$C_L=150\text{pF}$	27		35		42	
Propagation Delay, Any A to Y	$t_{PLH}$	$C_L=50\text{pF}$	16		26		31	ns
		$C_L=150\text{pF}$	19		31		37	
	$t_{PHL}$	$C_L=50\text{pF}$	16		26		31	ns
		$C_L=150\text{pF}$	19		31		37	
Propagation Delay, G to Y	$t_{PLH}$	$C_L=50\text{pF}$	12		19		23	ns
		$C_L=150\text{pF}$	15		24		29	
	$t_{PHL}$	$C_L=50\text{pF}$	12		19		23	ns
		$C_L=150\text{pF}$	15		24		29	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r \leq 2$  ns), AHCT680

Characteristic	Symbol	Conditions <sup>†</sup>	$T_A = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Any P to Y	$t_{PLH}$	$C_L = 50\text{pF}$	21		35		42	ns
		$C_L = 150\text{pF}$	24		40		48	
	$t_{PHL}$	$C_L = 50\text{pF}$	21		35		42	
		$C_L = 150\text{pF}$	24		40		48	
Propagation Delay, Any A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	18		30		36	ns
		$C_L = 150\text{pF}$	21		35		42	
	$t_{PHL}$	$C_L = 50\text{pF}$	18		30		36	
		$C_L = 150\text{pF}$	21		35		42	
Propagation Delay, E to Y	$t_{PLH}$	$C_L = 50\text{pF}$	13		21		25	ns
		$C_L = 150\text{pF}$	16		26		31	
	$t_{PHL}$	$C_L = 50\text{pF}$	13		21		25	
		$C_L = 150\text{pF}$	16		26		31	
Set up Time An before E	$t_{SU}$		6	10		12	ns	
Hold Time An after E	$t_H$		0	0		0	ns	
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$						pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Compares Two 8-Bit Words
- '682 has 20kΩ pullup Resistors on the Q Inputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

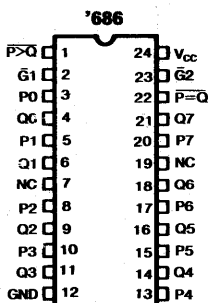
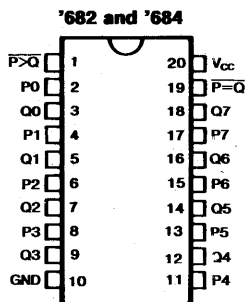
### DESCRIPTION

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide  $P=Q$  and  $P>Q$  outputs. The '682 features 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATIONS



NC—No internal connection

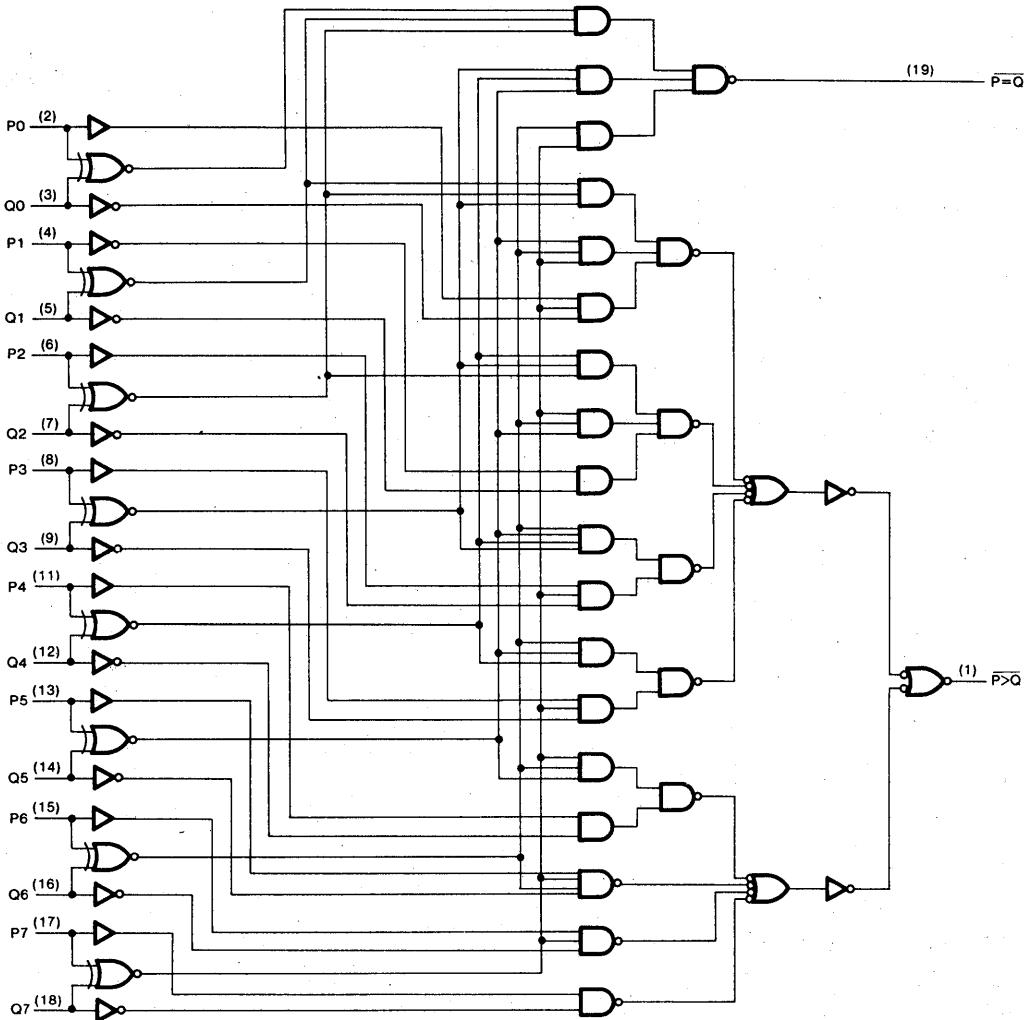
### FUNCTION TABLE

INPUTS		OUTPUTS	
DATA	ENABLES	$P=Q$	$P>Q$
P, Q	$\bar{G}1 \quad \bar{G}2$	$P=Q$	$P>Q$
$P=Q$	L X	L	H
$P>Q$	X L	H	L
$P<Q$	X X	H	H
$P=Q$	H X	H	H
$P>Q$	X H	H	H
X	H H	H	H

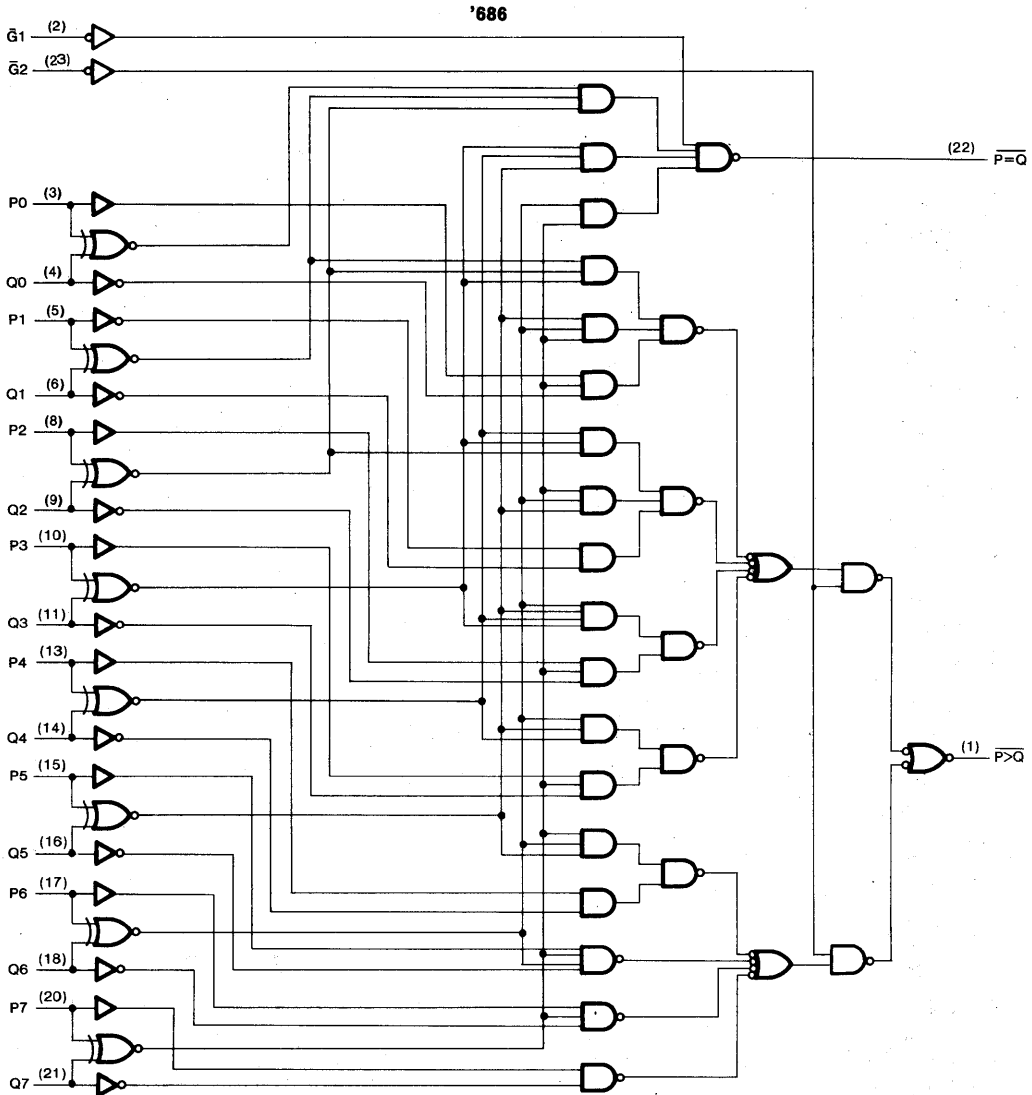
- NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.  
2. The  $P<Q$  function can be generated by applying the  $P=Q$  and  $P>Q$  outputs to a 2-input NAND gate.

**LOGIC DIAGRAMS**

'682 or '684



**LOGIC DIAGRAMS** (continued)



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**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	54AHCT	Unit
			Typ		$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
					Guaranteed Limits		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.93	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current, ('682 Q Inputs)		$V_{CC}=\text{Max}$ $V_{IN}=2.7V$ $V_{IN}=0.4V$		-0.2 -0.4	-0.2 -0.4	-0.2 -0.4	mA
Maximum Input Current (All other Inputs)	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	For '682: $V_{IN}=\text{GND}$ (Q0-Q7) $V_{IN}=V_{CC}$ or GND (all other inputs)		3.5	3.5	3.5	mA
		For '684 and '688 $V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT682, AHCT684, AHCT686

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Propagation Delay, P or Q to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17 16		22 27		27 33	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17 16		22 27		27 33	
Propagation Delay, P or Q to $\overline{P>Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	16 19		27 32		32 38	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	16 19		27 32		32 38	
Propagation Delay, G1 to $\overline{P=Q}$ ('686 Only)	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	10 13		16 21		19 25	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	10 13		16 21		19 25	
Propagation Delay, G2 to $\overline{P<Q}$ ('686 Only)	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		19 24		23 29	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		19 24		23 29	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

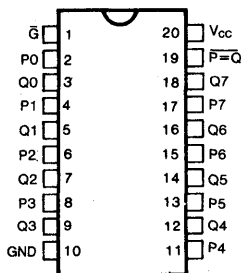
† For AC switching test circuits and timing waveforms see section 2.

4

**FEATURES**

- Compares Two 8-Bit Words
- Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High output drive  
( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

INPUTS		OUTPUT
DATA ENABLE P, Q	G-bar	P=Q
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

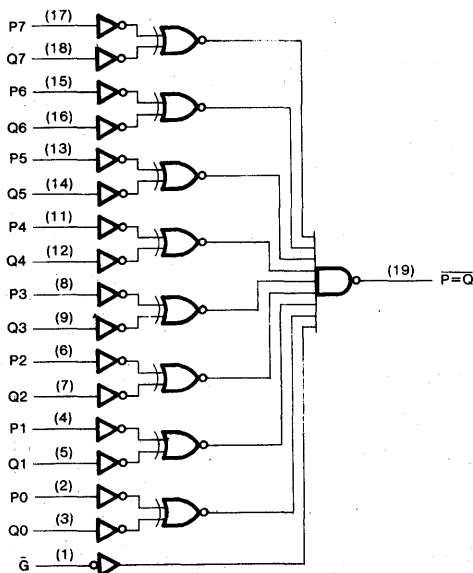
**DESCRIPTION**

These identity comparators perform comparisons of two 8-bit binary or BCD words. The outputs of the '688 are totempole, while '688's are open-drain.

These devices provide speed<sup>o</sup> and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through:  
      $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
     Range           KS74AHCT: -40°C to +85°C  
                     KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit
			Typ	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
Guaranteed Limits						
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V
Minimum High-Level Output Voltage ('688 only)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2 $V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0 0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current ('689 only)	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT688

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, P to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	12		19		23	ns
		$C_L = 150\text{pF}$	15		24		29	
	$t_{PHL}$	$C_L = 50\text{pF}$	12		19		23	ns
		$C_L = 150\text{pF}$	15		24		29	
Propagation Delay, Q to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	12		19		23	ns
		$C_L = 150\text{pF}$	15		24		29	
	$t_{PHL}$	$C_L = 50\text{pF}$	12		19		23	ns
		$C_L = 150\text{pF}$	15		28		29	
Propagation Delay, $\overline{G}$ to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	11		17		20	ns
		$C_L = 150\text{pF}$	14		22		26	
	$t_{PHL}$	$C_L = 50\text{pF}$	11		17		20	ns
		$C_L = 150\text{pF}$	14		22		26	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT689

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, P to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	19		28		33	ns
		$C_L = 150\text{pF}$	22		33		39	
	$t_{PHL}$	$C_L = 50\text{pF}$	14		23		28	ns
		$C_L = 150\text{pF}$	17		28		34	
Propagation Delay, Q to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	19		28		33	ns
		$C_L = 150\text{pF}$	22		33		39	
	$t_{PHL}$	$C_L = 50\text{pF}$	14		23		28	ns
		$C_L = 150\text{pF}$	17		28		34	
Propagation Delay, $\overline{G}$ to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	16		23		27	ns
		$C_L = 150\text{pF}$	19		28		33	
	$t_{PHL}$	$C_L = 50\text{pF}$	11		18		22	ns
		$C_L = 150\text{pF}$	16		23		28	
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

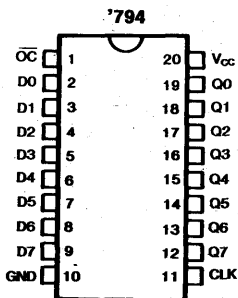
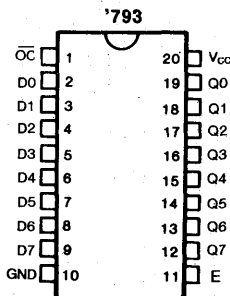
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- I/O port configuration enables output data back onto input bus
- Latch ('793) and Register ('794) options
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATIONS**



**DESCRIPTION**

These are 8-bit latches/registers that allow temporary storage and retrieval of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The Data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when E is high, and it is latched when E goes low. The output control ( $\overline{OC}$ ) is used to enable data on the D0-D7 pins. when  $\overline{OC}$  is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When  $\overline{OC}$  is high, D0-D7 are inputs to the latches/registers configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**FUNCTION TABLES**

**'793**

E	$\overline{OC}$	Q	D
L	L	Q <sub>0</sub> **	Output, Q
L	H	Q <sub>0</sub> **	Input
H†	L	D*	Output, Q*
H	H	D	Input

\* In this case the output of the latch feeds the input, and a "race" condition results.

\*\* Q<sub>0</sub> represents the previous "latched" state.

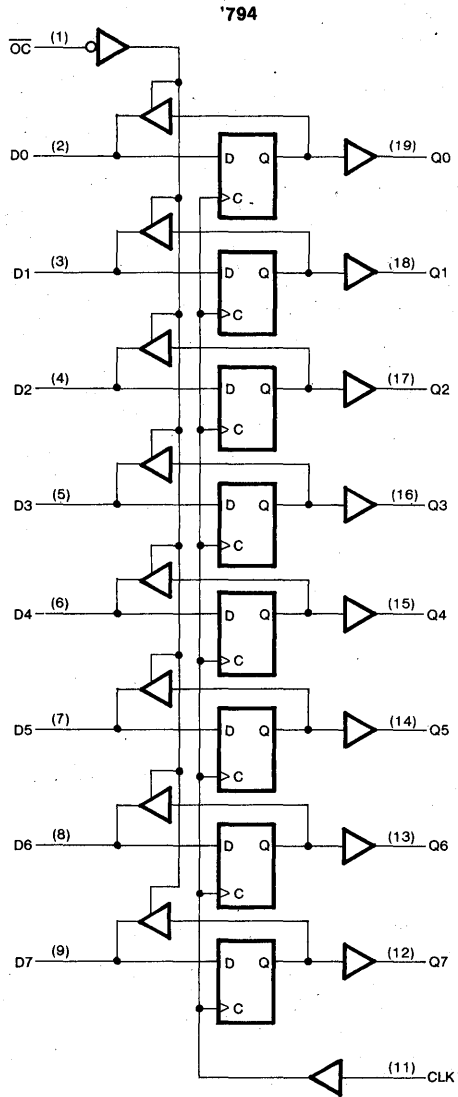
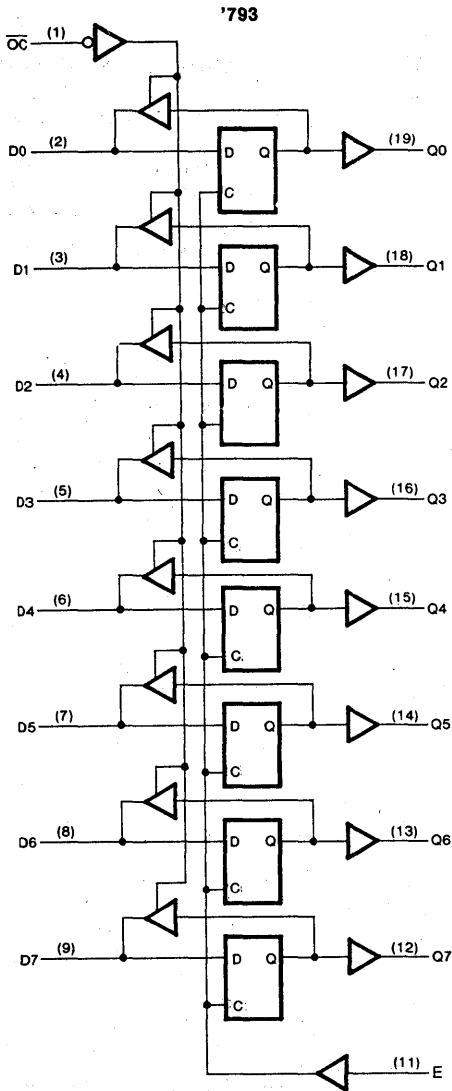
† This transition is not a normal mode of operation and may produce hazards.

**'794**

CLK	$\overline{OC}$	Q	D
L or H or ↓	L	Q <sub>0</sub>	Output, Q
L or H or ↓	H	Q <sub>0</sub>	Input
↑	L	Q <sub>0</sub>	Output, Q*
↑	H	D	Input

\* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q<sub>0</sub>.

**LOGIC DIAGRAMS**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{Stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (t<sub>out</sub> t<sub>r</sub> < 2 ns), AHCT793, AHCT794

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C	KS74AHCT		KS54AHCT		Unit
			V <sub>CC</sub> = 5.0V	T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	V <sub>CC</sub> = 5.0V ± 10%	V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency ('794 only)	t <sub>max</sub>	C <sub>L</sub> = 50pF	60	40		35		MHz
Propagation Delay D to Any Q ('793 only)	t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	10 13		16 21		19 25	ns
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	10 13		16 21		19 25	
Propagation Delay CLK/E to Any Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	12 15		20 25		24 30	ns
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	12 15		20 25		24 30	
Enable Time, OC to D	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ (C = Low for '793)	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11 14		18 23	22 28	ns
	t <sub>PZL</sub>		C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11 13		18 23	22 28	
Disable Time OC to D	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF (C = Low for '793)		11		18	22	ns
	t <sub>PLZ</sub>			11		18	22	
Pulse Width, CLK/C High or low	t <sub>w</sub>		9	14		19		ns
Setup time	D before E↓ ('793)		6	10		12		ns
	D before CLK↑ ('794)		10	15		20		
Hold Time	D after E↓ ('793)		9	10		12		ns
	D after CLK↑ ('794)		0	0		0		
Input Capacitance	C <sub>IN</sub>		5					pF
Output Capacitance	C <sub>OUT</sub>	OC = GND	10					pF
Power Dissipation Capacitance*	C <sub>PD</sub>							ns

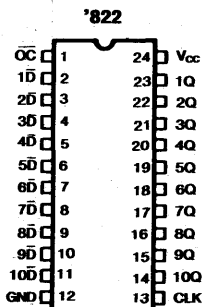
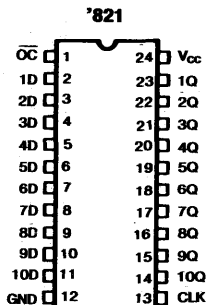
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Functionally Equivalent to AMD's Am29821 and Am29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATIONS



### DESCRIPTION

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speed and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLES

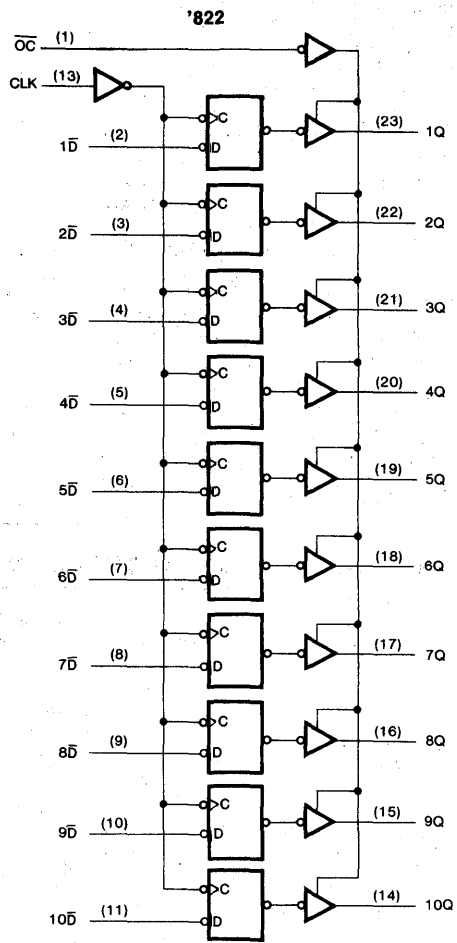
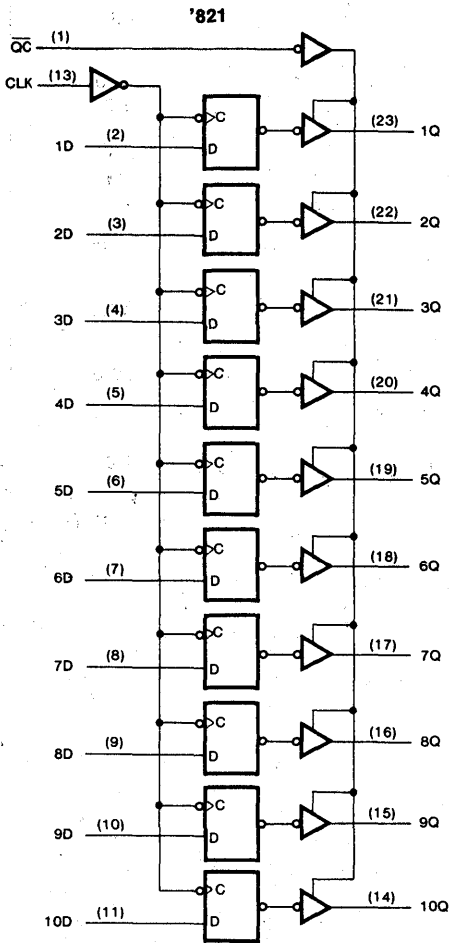
(Each Flip-Flop)  
**'821**

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
L	H	X	$Q_0$
H	X	X	Z

**'822**

Inputs			Output
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	$Q_0$
L	H	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
Power Dissipation Per Package,  $P_d$ <sup>†</sup> ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

<sup>†</sup> Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature

Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

4



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f < 2$  ns), AHCT821, AHCT822

Characteristic	Symbol	Conditions†	KS74AHCT		KS54AHCT		Unit		
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Min	Max	Min		Max	
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30	MHz		
Propagation Delay CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	13		15		18	ns	
		$C_L = 150\text{pF}$	16		20		23		
	$t_{PHL}$	$C_L = 50\text{pF}$	13		15		18		
		$C_L = 150\text{pF}$	16		20		23		
Output Enable Time, $\overline{OC}$ to any Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	ns
			$C_L = 150\text{pF}$	14		23		28	
	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	
			$C_L = 150\text{pF}$	14		23		28	
Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22		
Pulse Width, CLK High or Low	$t_w$		9	15		18	ns		
Setup Time, Data before CLK†	$t_{su}$		9	14		17	ns		
Hold Time, Data after CLK†	$t_h$		0	0		0	ns		
Input Capacitance	$C_{IN}$		5				pF		
Output Capacitance	$C_{OUT}$	Output Disabled	10				pF		
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5				pF		
		$\overline{OC} = \text{GND}$	30				pF		

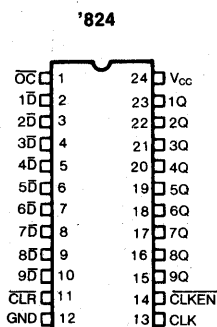
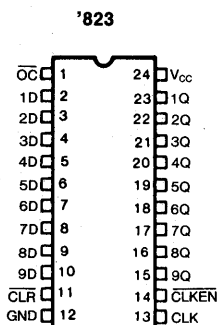
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Functionally Equivalent to AMD's Am29823 and Am29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATIONS



## DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ( $\overline{\text{CLKEN}}$ ) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting  $\overline{\text{D}}$  inputs. Taking the  $\overline{\text{CLR}}$  input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ( $\overline{\text{OC}}$ ) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

## FUNCTION TABLES

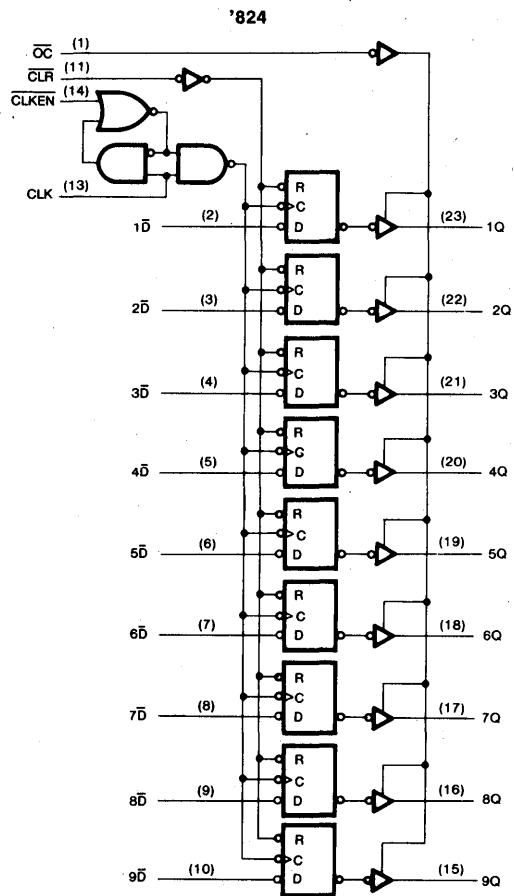
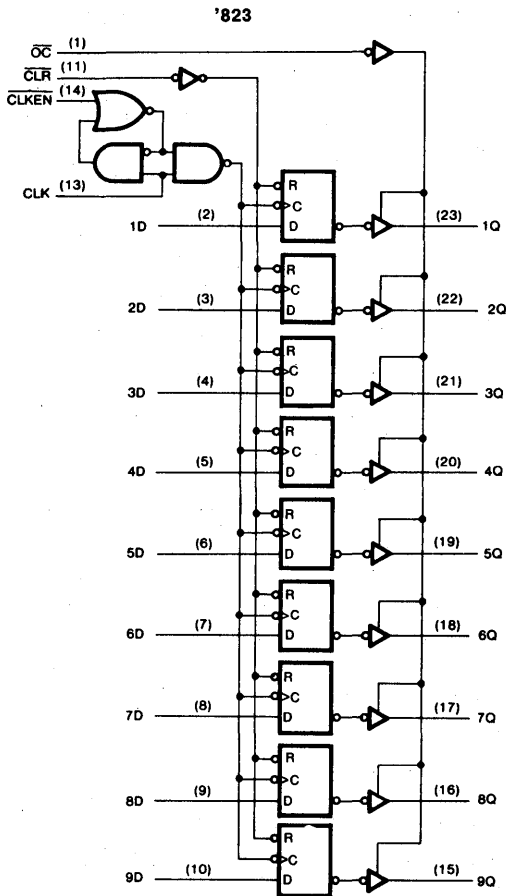
**'823**

INPUT					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q <sub>0</sub>
H	X	X	X	X	Z

**'824**

INPUTS					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	$\overline{\text{D}}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q <sub>0</sub>
H	X	X	X	X	Z

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT823, AHCT824

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30		MHz
Propagation Delay CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17 20		19 24		23 28	ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17 20		19 24		23 28	
Propagation Delay, CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17 20		20 25		25 31	ns
Output Enable Time, $\overline{OC}$ to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23	22 28	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23	22 28	
Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	17		20		25	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	17		20		25	
Pulse Width	CLR low	$t_w$		9	15		18	ns
	CLK high or low			9	15		18	
Setup Time before CLK†	CLR inactive	$t_{su}$		9	14		17	ns
	Data			9	14		17	
	CLKEN high or low			9	14		17	
Hold Time, CLKEN or data after CLK†	$t_h$		0	0		0	ns	
Input Capacitance	$C_{IN}$		5				pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10				pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5				pF	
		$\overline{OC} = \text{GND}$	30				pF	

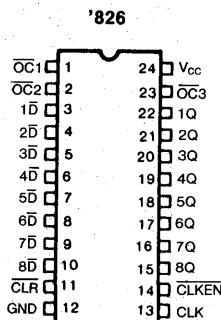
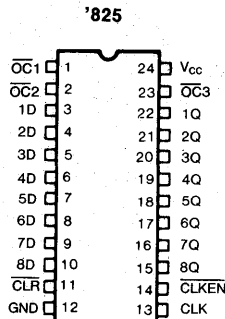
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Functionally Equivalent to AMD's Am29825 and Am29826
- Improved  $I_{OH}$  Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24\text{ mA @ }V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATIONS**



**DESCRIPTION**

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing multi-user buffer registers, I/O ports, bus drivers and working registers.

With the clock enable ( $\overline{\text{CLKEN}}$ ) low, all D-type edge-triggered flip-flops enter data on the low-to-high transition of the clock. Taking  $\overline{\text{CLKEN}}$  high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting  $\overline{\text{D}}$  inputs. Taking the  $\overline{\text{CLR}}$  inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ( $\overline{\text{OC1}}$ ,  $\overline{\text{OC2}}$ , and  $\overline{\text{OC3}}$ ) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.



# KS54AHCT 825/826 KS74AHCT

# 8-Bit Bus Interface Flip-Flops with 3-State Outputs

## FUNCTION TABLES

'825

Inputs					Output Q
$\overline{OC}^*$	CLR	CLKEN	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

\*  $\overline{OC} = H$  if any of  $\overline{OC}1$ ,  $\overline{OC}2$ , or  $\overline{OC}3$  are high.  
 $\overline{OC} = L$  if all of  $\overline{OC}1$ ,  $\overline{OC}2$ , and  $\overline{OC}3$  are low.

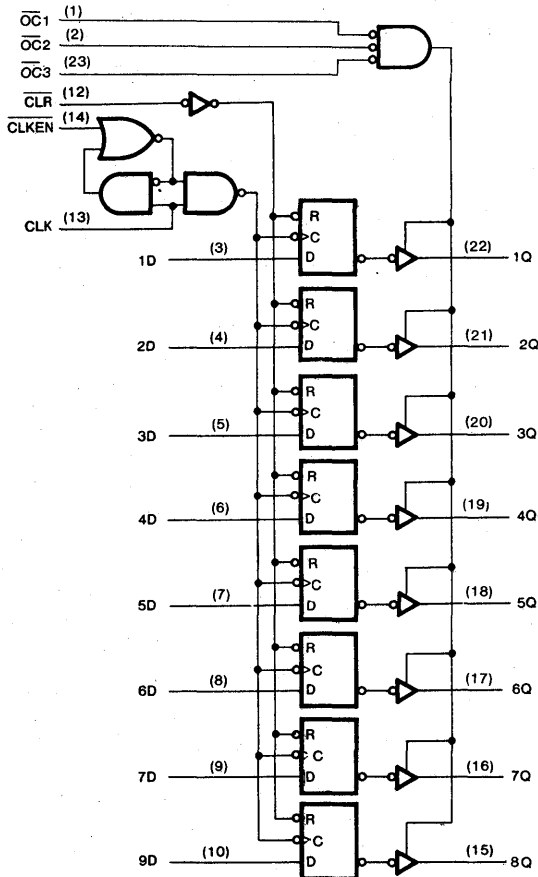
'826

Inputs					Output Q
$\overline{OC}^*$	CLR	CLKEN	CLK	$\overline{D}$	
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

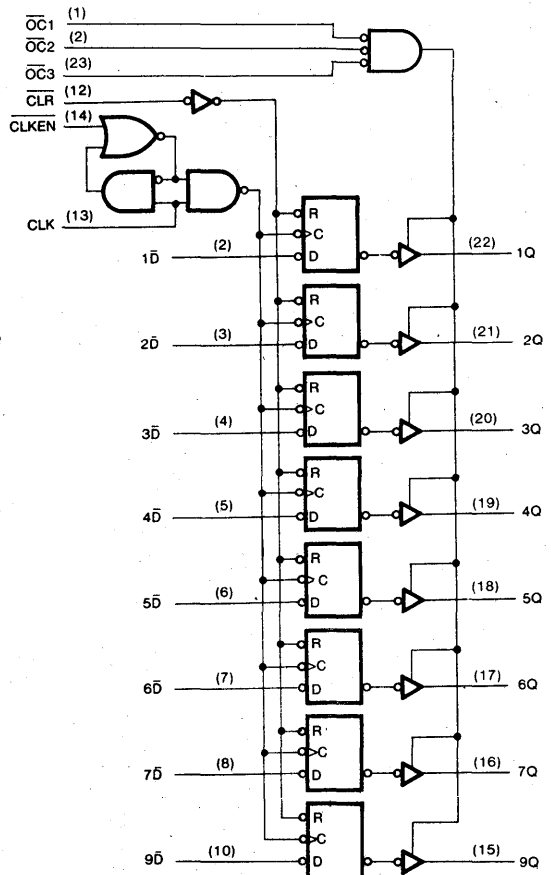
\*  $\overline{OC} = H$  if any of  $\overline{OC}1$ ,  $\overline{OC}2$ , or  $\overline{OC}3$  are high.  
 $\overline{OC} = L$  if all of  $\overline{OC}1$ ,  $\overline{OC}2$ , and  $\overline{OC}3$  are low.

## LOGIC DIAGRAMS

'825



'826



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT:  $-40^\circ C$  to  $+85^\circ C$   
 KS54AHCT:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT825, AHCT826

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35		30		MHz	
Propagation Delay CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	17		19		23	ns	
		$C_L = 150\text{pF}$	20		24		28		
Propagation Delay, CLR to Any Q	$t_{PHL}$	$C_L = 50\text{pF}$	17		19		23	ns	
		$C_L = 150\text{pF}$	20		24		28		
Propagation Delay, CLR to Any Q	$t_{PHL}$	$C_L = 50\text{pF}$	12		19		23	ns	
		$C_L = 150\text{pF}$	15		22		27		
Output Enable Time, OC to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	ns
			$C_L = 150\text{pF}$	14		23		28	
Output Disable Time, OC to any Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	ns
			$C_L = 150\text{pF}$	14		23		28	
Output Disable Time, OC to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$		13		18		22	ns
	$t_{PLZ}$		$C_L = 50\text{pF}$		13		18		
Pulse Width	CLR low	$t_w$		9	15		18	ns	
	CLK high or low			9	15		18		
Setup Time before CLK†	CLR inactive	$t_{su}$		9	14		17	ns	
	Data			9	14		17		
	CLKEN high or low			9	14		17		
Hold Time, CLKEN or data after CLK†	$t_h$		0	0		0		ns	
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	OC = $V_{CC}$ OC = GND	5					pF	
			30					pF	

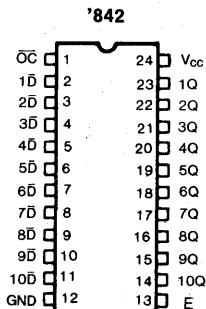
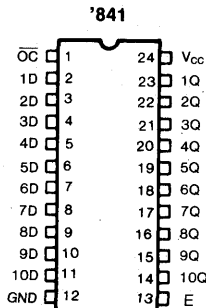
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Bus-Structured Pinout
- Provides Extra Bus Driving Latches
- Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24\text{ mA @ }V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATIONS**



**DESCRIPTION**

These 10-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting (D) inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLES**

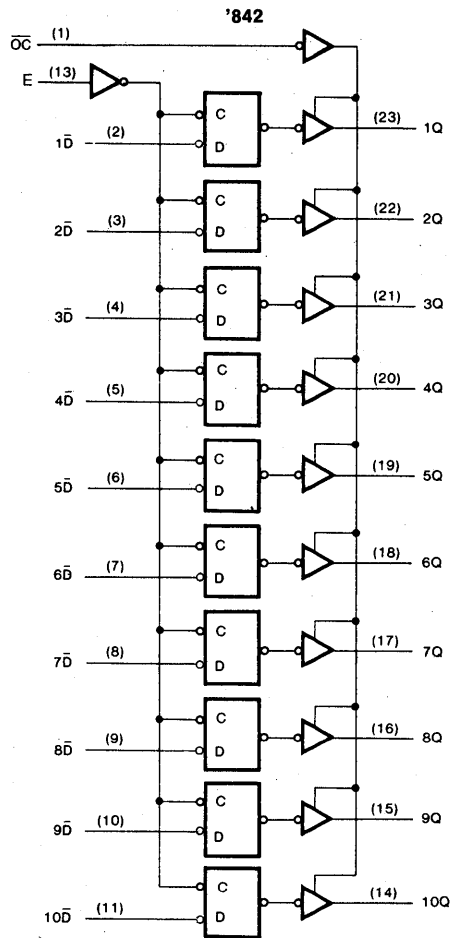
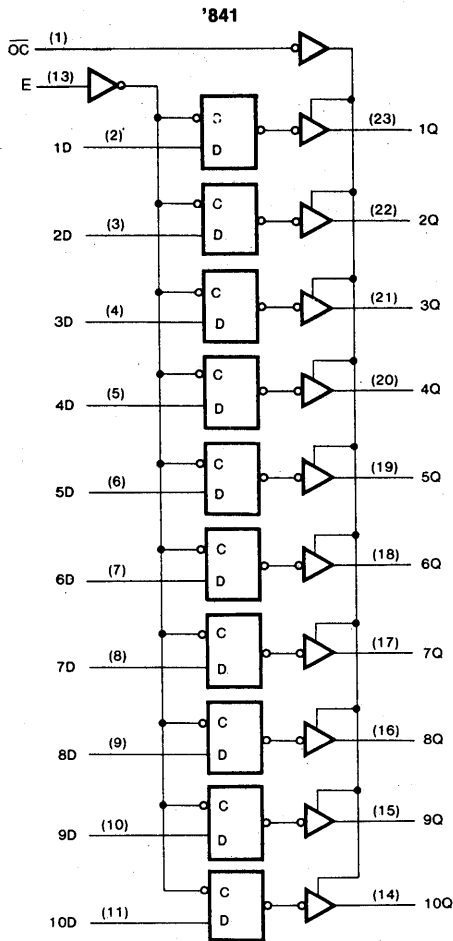
**'841**

Inputs			Output
$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**'842**

Inputs			Output
$\overline{OC}$	E	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAM S**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT841, AHCT842

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Propagation Delay, Data to Q	$t_{PLH}$	$C_L = 50\text{pF}$	10		13		19	ns
		$C_L = 150\text{pF}$	13		21		25	
	$t_{PHL}$	$C_L = 50\text{pF}$	10		13		19	ns
		$C_L = 150\text{pF}$	13		21		25	
Propagation Delay, E to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	15		24		29	ns
		$C_L = 150\text{pF}$	18		29		35	
	$t_{PHL}$	$C_L = 50\text{pF}$	15		24		29	ns
		$C_L = 150\text{pF}$	18		29		35	
Output Enable Time, $\overline{OC}$ to any Q	$t_{PZH}$	$C_L = 50\text{pF}$	13		18		22	ns
		$C_L = 150\text{pF}$	16		23		28	
	$t_{PZL}$	$C_L = 50\text{pF}$	13		18		22	ns
		$C_L = 150\text{pF}$	16		23		28	
Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns
		$C_L = 50\text{pF}$	13		18		22	
	$t_{PLZ}$		13		18		22	
Pulse Width, E High	$t_w$		12	20		25		ns
Setup Time, Data before E $\downarrow$	$t_{su}$		6	10		12		ns
Hold Time, Data after E $\downarrow$	$t_h$		3	5		7		ns
Input Capacitance	$C_{IN}$		5					pF
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5					pF
		$\overline{OC} = \text{GND}$	30					pF

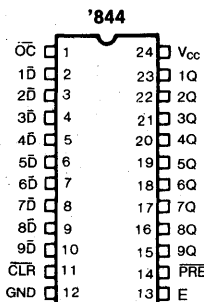
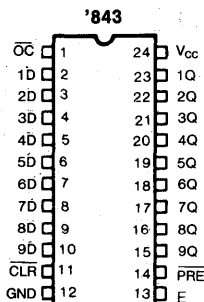
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Bus-Structured Pinout
- Provide Extra Bus Driving Latches  
Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High Impedance
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATIONS**



**DESCRIPTION**

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting  $\bar{D}$  inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLES**

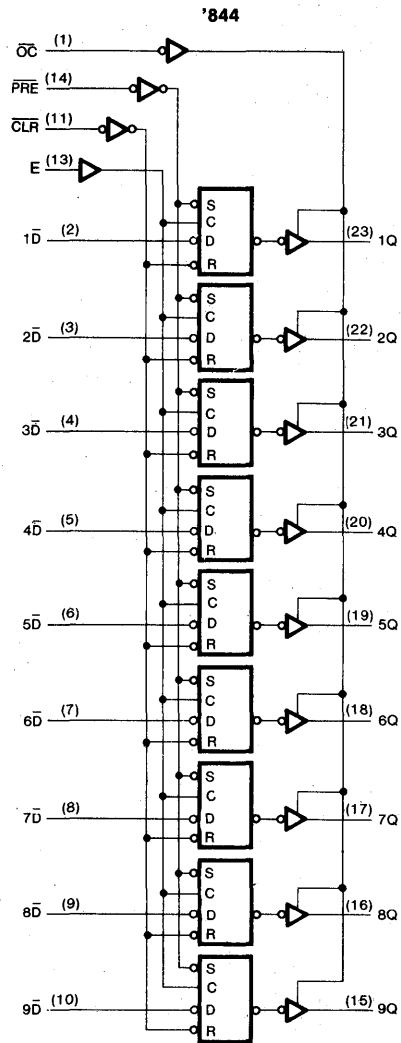
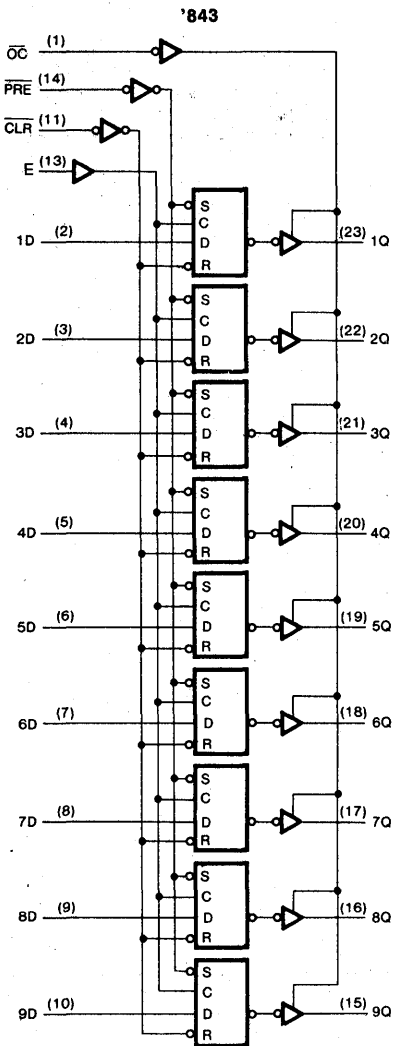
'843

INPUTS					OUTPUT
PRE	CLR	$\overline{OC}$	E	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	$Q_0$
X	X	H	X	X	Z

'844

INPUTS					OUTPUT
PRE	CLR	$\overline{OC}$	E	$\bar{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	$Q_0$
X	X	H	X	X	Z

**LOGIC DIAGRAMS**



# KS54AHCT 843/844

## KS74AHCT

### 9-Bit Bus Interface D-Type Latches with 3-State Outputs

#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT843, AHCT844

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit	
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
			Typ	Min	Max	Min	Max		
Propagation Delay, Data to Q	$t_{PLH}$	$C_L = 50\text{pF}$	13		18		22	ns	
		$C_L = 150\text{pF}$	16		23		28		
	$t_{PHL}$	$C_L = 50\text{pF}$	13		18		22	ns	
		$C_L = 150\text{pF}$	16		23		28		
Propagation Delay, E to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	16		26		31	ns	
		$C_L = 150\text{pF}$	19		31		37		
	$t_{PHL}$	$C_L = 50\text{pF}$	16		26		31	ns	
		$C_L = 150\text{pF}$	19		31		37		
Propagation Delay, PRE to Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17 20		27 32		32 38	ns	
Propagation Delay, CLR to Q	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17 20		27 32		32 38	ns	
Output Enable Time, OC to any Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	11		18		22	ns
			$C_L = 150\text{pF}$	14		23		28	
	$t_{PZL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28		
Output Disable Time, OC to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13		18		22	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	13		18		22		
Pulse Width, E High	$t_w$		12	20		25		ns	
Setup Time, Data before E $\downarrow$	$t_{SU}$		8	10		12		ns	
Hold Time, Data after $\downarrow$	$t_h$		3	5		7		ns	
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	OC = $V_{CC}$	5					pF	
		OC = GND	30						

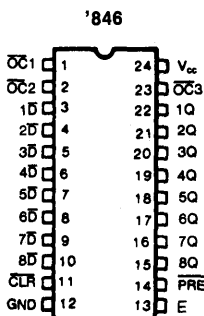
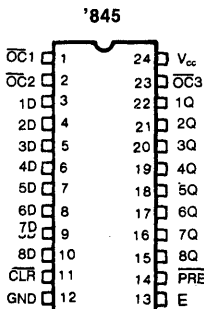
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

**FEATURE**

- 3-state buffer-type outputs drive bus-lines directly
- Bus-structured pinout
- Provides extra bus driving latches necessary for wider address/data paths or buses with parity
- Low power consumption characteristic of CMOS devices
- 3-state outputs with high drive current ( $I_{OL} = 24\text{mA}$  @  $V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATIONS**



**DESCRIPTION**

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since CLR and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

The buffered output control inputs (OC1, OC2, and OC3) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.



# KS54AHCT 845/846 KS74AHCT

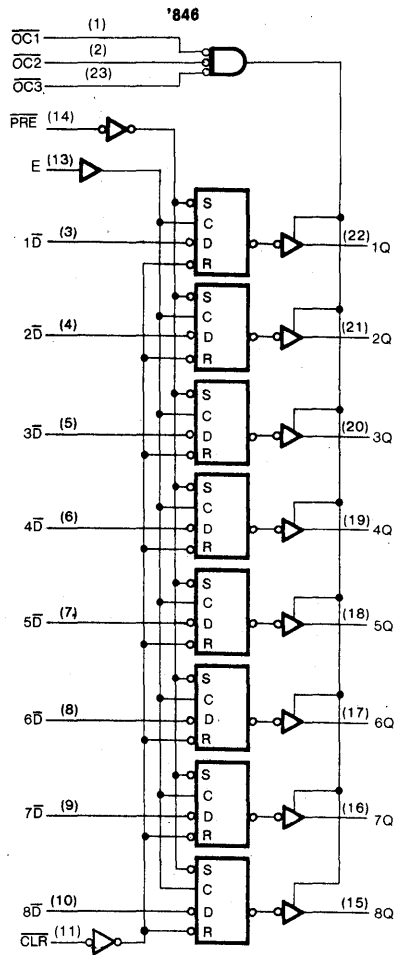
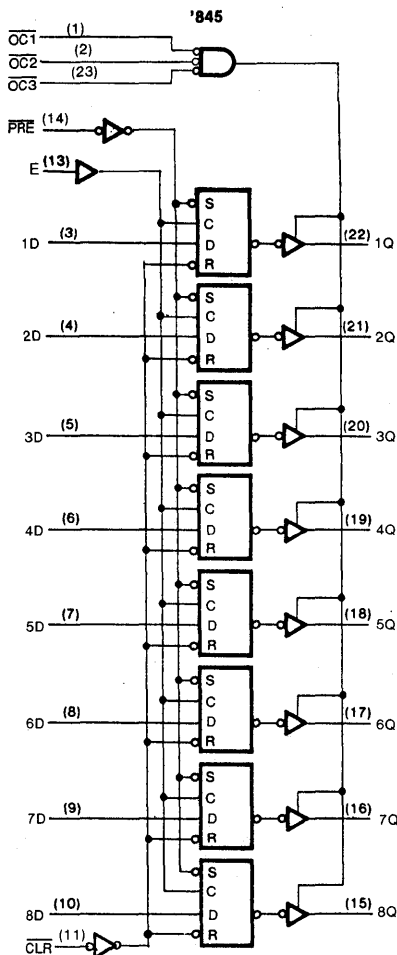
# 8-Bit Bus Interface D-Type Latches with 3-State Outputs

## FUNCTION TABLE

'845							
INPUTS							OUTPUT
PRE	CLR	OC1	OC2	OC3	E	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q <sub>0</sub>
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'846							
INPUTS							OUTPUT
PRE	CLR	OC1	OC2	OC3	E	$\bar{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	L	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q <sub>0</sub>
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

## LOGIC DIAGRAMS



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				Unit
			Typ	Guaranteed Limits			
			KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$			KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT845

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay E to Q	$t_{PLH}$		13		22		26	ns
	$t_{PHL}$		13		22		26	
Propagation Delay D to Q	$t_{PLH}$		8		15		20	ns
	$t_{PHL}$		8		15		20	
Propagation Delay CLR to Q	$t_{PLH}$		16		26		31	ns
	$t_{PHL}$		16		26		31	
Propagation Delay PRE to Q	$t_{PLH}$		16		26		31	ns
	$t_{PHL}$		16		26		31	
Output Enable Time OC to Q	$t_{PZH}$		12		20		24	ns
	$t_{PZL}$		12		20		24	
Output Disable Time OC to Q	$t_{PHZ}$		12		20		24	ns
	$t_{PLZ}$		12		20		24	
Set up Time Dn before E	$t_{SU}$		8	10		12		ns
Hold Time Dn after E	$t_H$		0	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT846

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Min	Max	Min	Max	
Propagation Delay E to Q	$t_{PLH}$		14		24		32	ns
	$t_{PHL}$		14		24		32	
Propagation Delay D to Q	$t_{PLH}$		10		17		22	ns
	$t_{PHL}$		10		17		22	
Propagation Delay CLR to Q	$t_{PLH}$		13		22		26	ns
	$t_{PHL}$		13		22		26	
Propagation Delay PRE to Q	$t_{PLH}$		13		22		26	ns
	$t_{PHL}$		13		22		26	
Output Enable Time OC to Q	$t_{PZH}$		12		20		24	ns
	$t_{PZL}$		12		20		24	
Output Disable Time OC to Q	$t_{PHZ}$		12		20		24	ns
	$t_{PLZ}$		12		20		24	
Set up Time Dn before E	$t_{SU}$		8	10		12		ns
Hold Time Dn after E	$t_H$		0	0		0		ns
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- **Modified input structure allows voltages up to 15V**
- **High-Drive-current Outputs:**  
 $I_{OL} = 8\text{mA} @ V_{OL} = 0.5\text{V}$
- **Low power consumption characteristic of CMOS**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

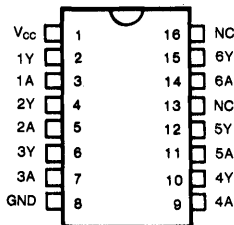
### DESCRIPTION

The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be converted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to  $V_{CC}$ , thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

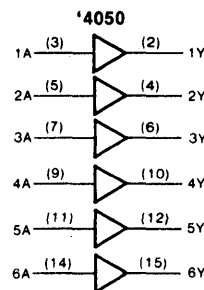
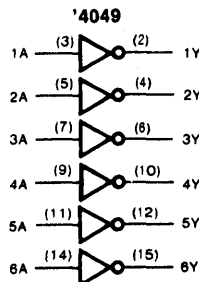
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAMS



### FUNCTION TABLE

Input A	Output Y	
	'4049	'4050
H	L	H
L	H	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > +15.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits	Typ	Guaranteed Limits	Typ	Guaranteed Limits	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND $V_{IN}=15V$		$\pm 0.1$	$\pm 1.0$ $\pm 10.0$		$\pm 1.0$ $\pm 10.0$		$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0		40.0		$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9		3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT4049, AHCT4050

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC}=5.0V$		KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC}=5.0V \pm 10\%$		KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max		
Propagation Delay	$t_{PLH}$	$C_L=50pF$	7		12		14	ns	
	$t_{PHL}$		7		12		14		
Input Capacitance	$C_{IN}$		5					pF	
Power-Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

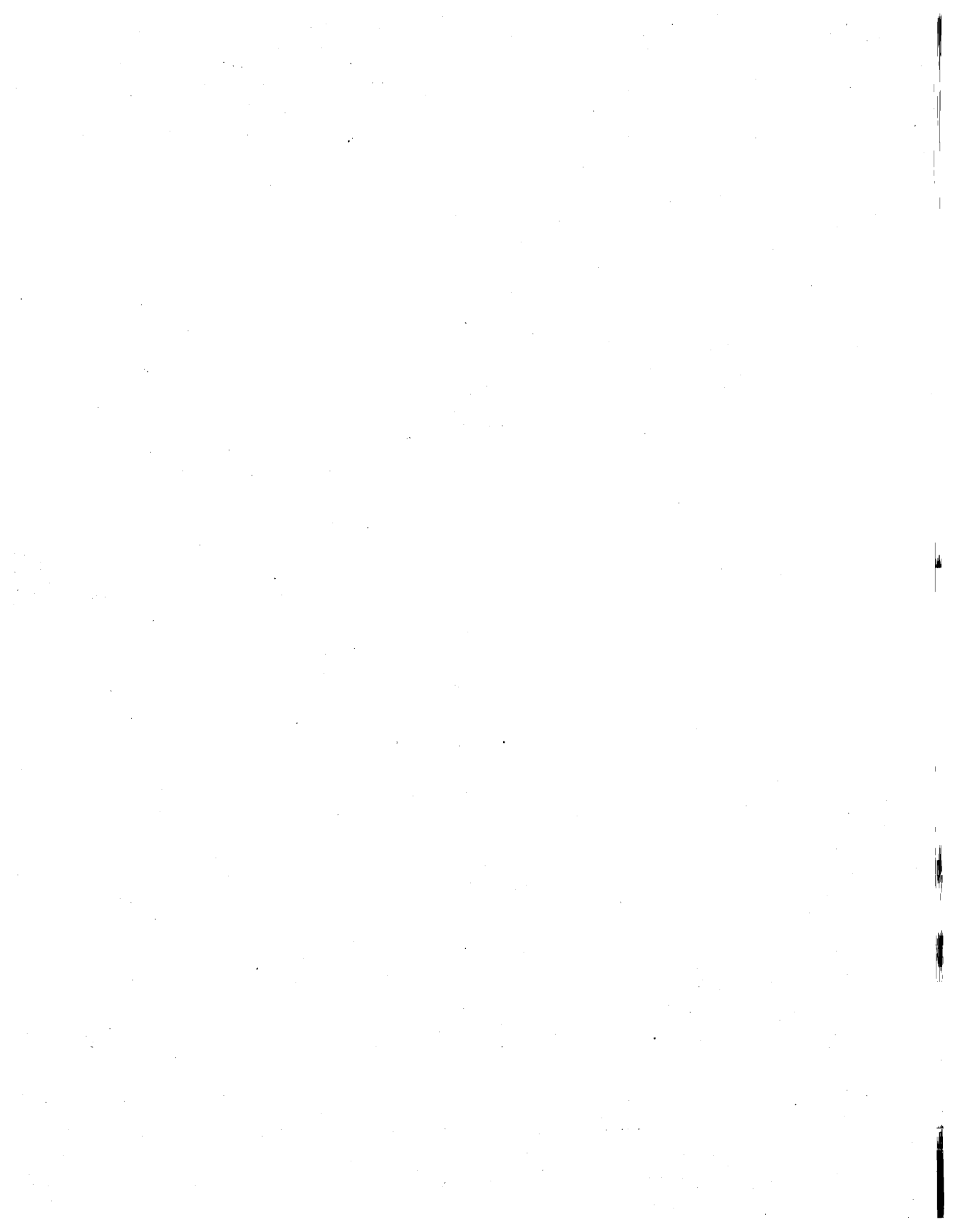
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



***KS54/74HCTLS DATA SHEETS 5***

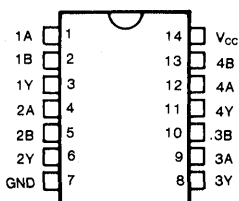




### FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8\text{mA} @ V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

### PIN CONFIGURATION



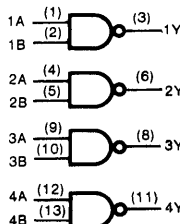
### DESCRIPTION

These devices contain four independent 2-input NAND gates that perform the Boolean functions  $Y = \overline{A \cdot B}$  or  $Y = \overline{A + B}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

5

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns, HCTLS00)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	10	15	18	22	ns
	$t_{PHL}$		10	15	18	22	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

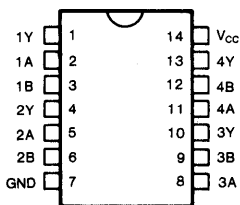
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**PIN CONFIGURATION**



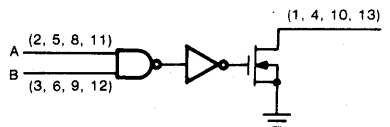
**DESCRIPTION**

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V

DC Input Diode Current,  $I_{IK}$

( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA

DC Output Diode Current,  $I_{OK}$

( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA

Continuous Output Current Per Pin,  $I_O$

( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA

Continuous Current Through

$V_{CC}$  or GND pins . . . . .  $\pm 125$  mA

Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C

Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V

DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$

Operating Temperature

Range KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Typ	$T_a = 25^\circ\text{C}$	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$	Unit
				Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS01

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0V$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$	Unit
			Guaranteed Limits				
Maximum Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	24	30	36	43	ns
	$t_{PHL}$	$R_L=1\text{k}\Omega$	15	20	25	30	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74HCTLS: -40°C to +85°C**  
**KS54HCTLS: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

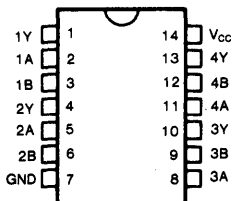
**DESCRIPTION**

These devices contain four independent 2-input NOR gates that perform the Boolean functions  $Y = \overline{A+B}$  or  $Y = \overline{A \cdot B}$ .

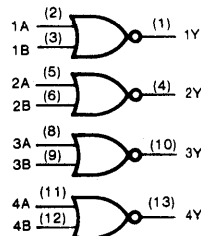
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	X	L
X	H	L
L	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_{df}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$	Guaranteed Limits		
			Typ				
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$	2.0	20.0	40.0	$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$	2.7	2.9	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS02

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Guaranteed Limits				
			Typ				
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50pF$	9	15	18	22	ns
	$t_{PHL}$		10	15	18	22	
Maximum Input Capacitance	$C_{IN}$		5			pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15			pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current Outputs:**  
 $I_{OL} = 8\text{mA} @ V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

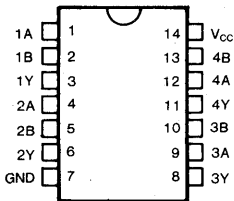
**DESCRIPTION**

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

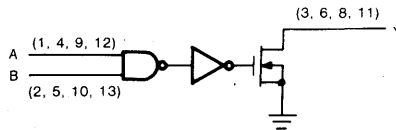
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0 0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$	2.0	20.0	40.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$	2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS03

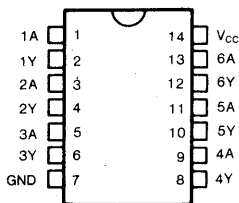
Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$	Unit	
			$V_{CC}=5.0V$	$V_{CC}=5.0V \pm 10\%$	$V_{CC}=5.0V \pm 10\%$		
			Typ	Guaranteed Limits			
Maximum Propagation Delay	$t_{PLH}$	$C_L=50pF$ $R_L=1k\Omega$	24	28	30	38	ns
	$t_{PHL}$		15	28	30	38	
Maximum Input Capacitance	$C_{IN}$		5			pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15			pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .  
 † For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{ V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

### PIN CONFIGURATION



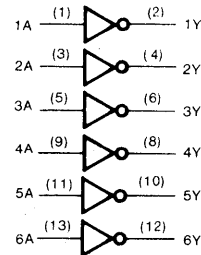
### DESCRIPTION

These devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Inverter)

Input	Output
A	Y
H	L
L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_{Df}$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns, HCTLS04)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC} = 5.0V$		$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
			Typ	Guaranteed Limits			
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50pF$	9	15	18	22	ns
	$t_{PHL}$		10	15	18	22	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

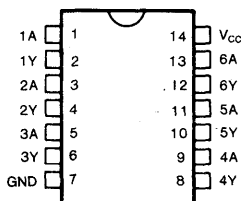
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



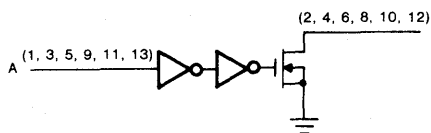
**DESCRIPTION**

These devices contain six independent inverters with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Inverter)

Input	Output
A	Y
H	L
L	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$ , ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$	KS74HCTLS		KS54HCTLS		Unit
				$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8		0.8		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$		$\pm 10.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0		40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9		3.0		mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS05

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0V$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		KS54 HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	24	30	36		43		ns
	$t_{PHL}$	$R_L=1\text{k}\Omega$	16	22	28		33		
Maximum Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

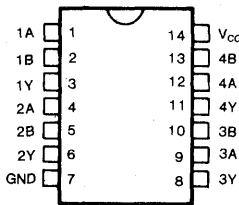
**DESCRIPTION**

These devices contain four independent 2-input AND gates. They perform the Boolean functions  $Y = A \cdot B$  or  $Y = \overline{A + B}$ .

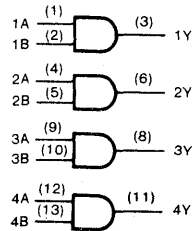
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			KS74HCTLS	KS54HCTLS	Unit
			Typ			$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$		2.0			2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8			0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$			$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0			20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7			2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS08

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$			KS74HCTLS	KS54HCTLS	Unit
			$V_{CC}=5.0V$			$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
			Typ			Guaranteed Limits		
Maximum Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	10	15	18	22	ns	
	$t_{PHL}$		10	20	25	30		
Maximum Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

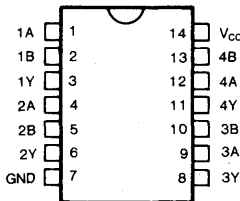
**DESCRIPTION**

These devices contain four independent 2-input AND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

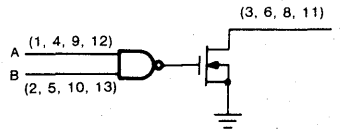
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	H
L	X	L
X	L	L



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS09

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	26	32	38	45	ns
	$t_{PHL}$	$R_L = 1\text{k}\Omega$	16	22	28	33	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

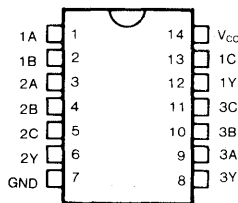
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



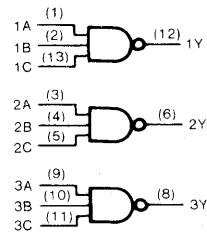
### DESCRIPTION

These devices contain three independent 3-input NAND gates. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 35$ mA
Continuous Current Through	
$V_{CC}$ or GND pins	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$	-65°C to +150°C
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	0V to $V_{CC}$
Operating Temperature	
Range	KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0		40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS10

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	11	15	19		23		ns
	$t_{PHL}$		11	15	19		23		
Maximum Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15						pF

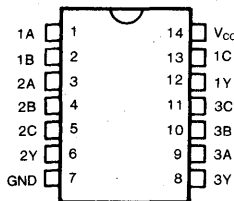
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



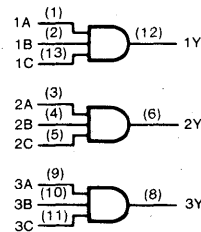
### DESCRIPTION

These devices contain three independent 3-input AND gates. They perform the Boolean functions  $Y = A \cdot B \cdot C$  or  $Y = \overline{A+B+C}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS11

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC} = 5.0V$		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
					$V_{CC} = 5.0V \pm 10\%$		
			Typ	Guaranteed Limits			
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	13	18	22	26	ns
	$t_{PHL}$		13	18	22	26	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTL5:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTL5:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**DESCRIPTION**

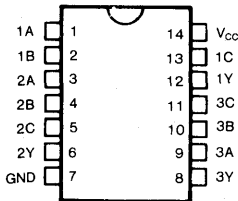
These devices contain three independent 3-input NAND gates with open-drain outputs. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{A + B + C}$ .

Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

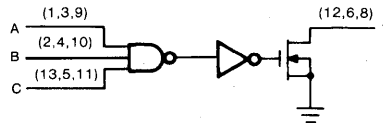
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ † . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-1.2\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r, t_f$ . . . . .	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0		2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8		0.8		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$		$\pm 10.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0		40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS12

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	26	32	38		45		ns
	$t_{PHL}$	$R_L = 1k\Omega$	16	22	28		33		
Maximum Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15						pF

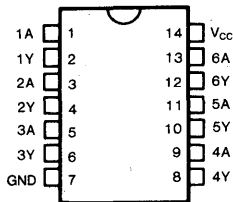
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$   
KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



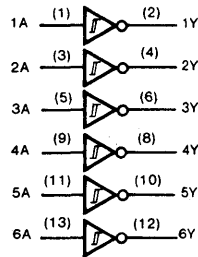
**DESCRIPTION**

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Inverter)

Input	Output
A	Y
H	L
L	H

5



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 (-0.5V <  $V_O$  <  $V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_{d1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84		$V_{CC} - 0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$		$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0		20.0		40.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7		2.9		3.0		mA

**DC ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Min	Max	Min	Max	Min	Max	
Positive-Going Threshold Voltage	$V_{T+}$	$V_{CC}=4.5V$	1.2	1.9	1.2	1.9	1.2	1.9	V
		$V_{CC}=5.5V$	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going Threshold Voltage	$V_{T-}$	$V_{CC}=4.5V$	0.5	1.2	0.5	1.2	0.5	1.2	V
		$V_{CC}=5.5V$	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis ( $V_{T+}-V_{T-}$ )	$V_H$	$V_{CC}=4.5V$	0.4	1.4	0.4	1.4	0.4	1.4	V
		$V_{CC}=5.5V$	0.4	1.5	0.4	1.5	0.4	1.5	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS14

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS	KS54 HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Propagation Delay	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15	20	25	30	ns
	t <sub>PHL</sub>		16	22	28	33	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

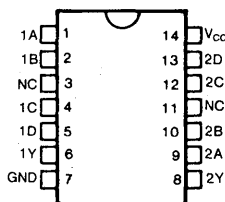
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages. (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



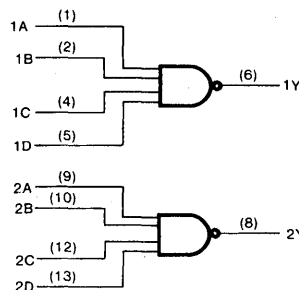
### DESCRIPTION

These devices contain two independent 4-input NAND gates. They perform the Boolean functions  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{A+B+C+D}$  in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns, HCTLS20)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC} = 5.0V$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ		Guaranteed Limits		
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	11	15	19	23	ns
	$t_{PHL}$		11	15	19	23	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

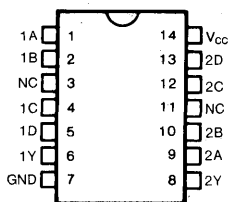
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

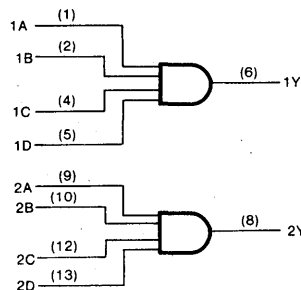
### DESCRIPTION

These devices contain two independent 4-input AND gates. They perform the Boolean functions  $Y = A \cdot B \cdot C \cdot D$  or  $Y = \overline{A + B + C + D}$  in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS21

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC}=5.0V$		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L=50\text{pF}$	12	18	22	27	ns
	$t_{PHL}$		12	18			
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD}V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

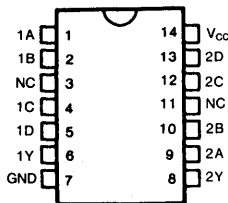
**DESCRIPTION**

These devices contain two independent 3-input NOR gates. These gates perform the Boolean functions  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{A + B + C + D}$  in positive logic. The open-drain outputs require pull-up resistors to perform correctly. They may be connected to other open-drain outputs to implement active low wired-OR or active high wired-AND functions.

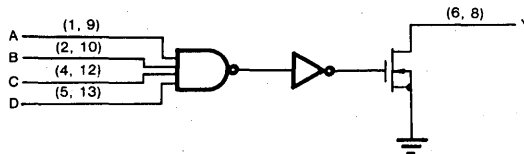
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

## AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS22

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC}=5.0V$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L=50\text{pF}$	26	33	40	47	ns
	$t_{PHL}$		15	20			
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

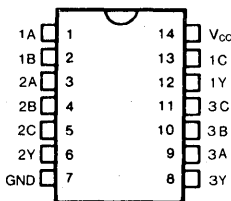
† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**PIN CONFIGURATION**



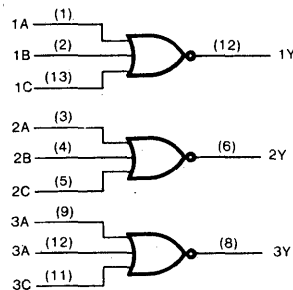
**DESCRIPTION**

These devices contain two independent 3-input NOR gates. They perform the Boolean functions  $\overline{Y} = A + B + C$  or  $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$  in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0		V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8		V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0		$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0		$\mu A$	

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS27

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L = 50pF$	11	15	19	23		ns	
	$t_{PHL}$		13	15	19	26			
Maximum Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**DESCRIPTION**

The '30 contains a single 8-input NAND gate. It performs the boolean functions (in positive logic):

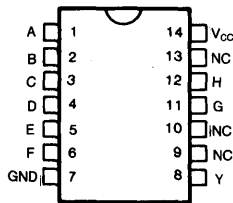
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

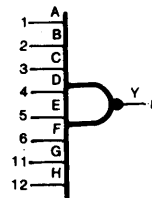
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs A Through H		Output Y
All Inputs	H	L
One or more inputs	L	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$		0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS30

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	11	15	19	22	ns
	$t_{PHL}$		11	15	19	22	
Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$		15				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

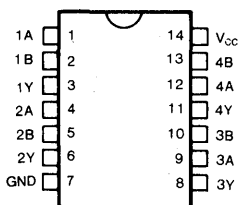
**DESCRIPTION**

These devices contain four independent 2-input OR gates. They perform the Boolean functions  $Y = A + B$  or  $Y = \overline{A \cdot B}$ .

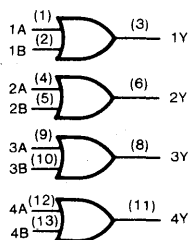
These devices provide speed and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damaged due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	X	H
X	H	H
L	L	L

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 (-0.5V <  $V_O$  <  $V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA	

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS32

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC}=5.0V$	Guaranteed Limits			
Maximum Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	13	22	25	28	ns
	$t_{PHL}$		13	22	25	28	
Maximum Input Capacitance	$C_{IN}$		5			pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15			pF	

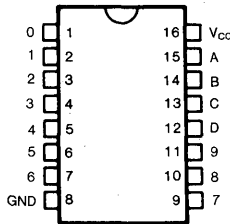
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Full decoding of Input Logic
- All outputs are High for Invalid BCD Conditions
- Also for application as 3-Line to 8-Line Decoders
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

No.	Inputs				Outputs										
	D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H
7	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	L	H	H	H
9	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

**DESCRIPTION**

The '42 decoder accepts for active-high BCD inputs and provides 10 mutually exclusive active-low outputs, as shown by logic symbol or diagram. The active-low outputs facilitate addressing other MSI units with active-low input enables.

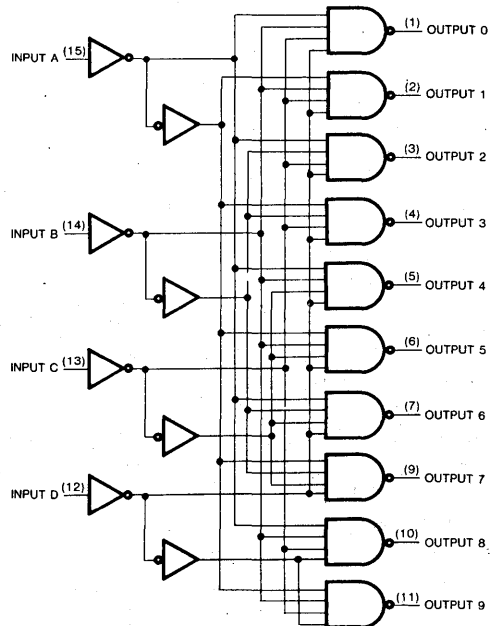
The logic design of the '42 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant input, D, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns, HCTLS42)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74 HCTLS	KS54 HCTLS	Unit
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	19	25	32	38	ns
	$t_{PHL}$		19	25	32	38	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

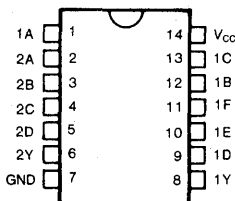
† For AC switching test circuits and timing waveforms see section 2.



## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## DESCRIPTION

The '51 performs the following Boolean functions:

$$1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$$

$$2Y = (2A \cdot 2B) + (2C \cdot 2D)$$

The '58 performs:

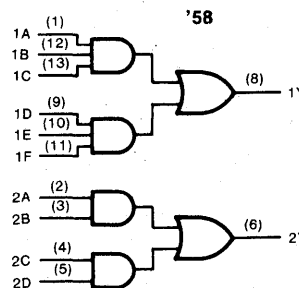
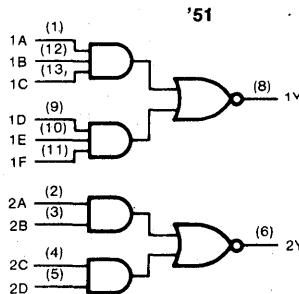
$$1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$$

$$2Y = (2A \cdot 2B) + (2C \cdot 2D)$$

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## LOGIC DIAGRAMS



## FUNCTION TABLES

Inputs						Output 1Y	
1A	1B	1C	1D	1E	1F	'51	'58
H	H	H	X	X	X	L	H
X	X	X	H	H	H	L	H
Any other combination						H	L

Inputs				Output 2Y	
2A	2B	2C	2D	'51	'58
H	H	X	X	L	H
X	X	H	H	L	H
Any other combination				H	L

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns, HCTLS51, HCTLS58)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Maximum Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$	13	18	23	27	ns
	$t_{PHL}$		13	18	23	27	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

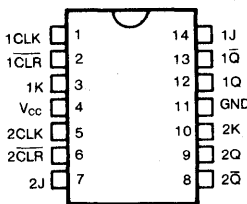
**DESCRIPTION**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

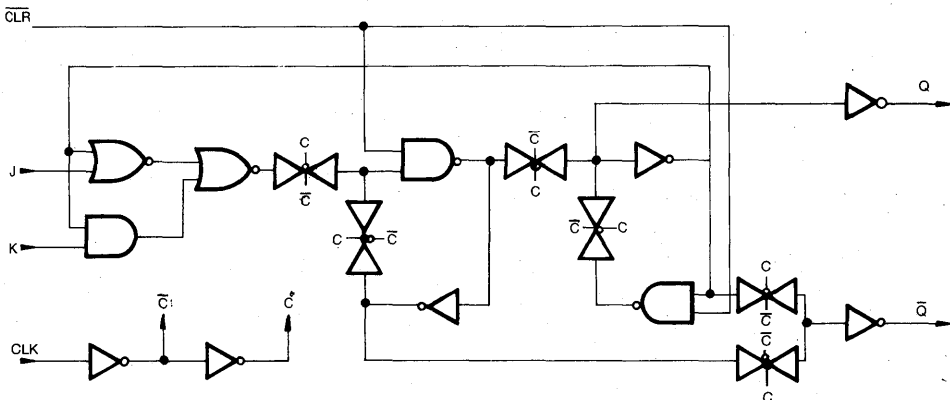
**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs				Outputs	
$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	X	X	X	L	H
H	↓	L	L	$Q_0$	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	$Q_0$	$\overline{Q}_0$

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS73A

Characteristic	Symbol	Conditions <sup>†</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit	
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		
			Typ				Guaranteed Limits	
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	40	30	25	21	MHz	
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	t <sub>PLH</sub>		15	20	25	30	ns	
	t <sub>PHL</sub>		15	20	25	30		
Maximum Propagation Delay, CLR to Q or $\bar{Q}$	t <sub>PLH</sub>		15	20	25	30	ns	
	t <sub>PHL</sub>	15	20	25	30			
Minimum Setup Time before CLK↓	J or K	t <sub>su</sub>	10	13	17	20	ns	
	CLR Inactive		10	13	17	20		
Minimum Hold Time, J or K after CLK↓	t <sub>h</sub>		0	0	0	0	ns	
Minimum Pulse Width	CLK High or Low	t <sub>w</sub>	10	13	17	20	ns	
	CLR Low		10	13	17	20		
Maximum Input Capacitance	C <sub>IN</sub>		5				pF	
Power Dissipation Capacitance*	C <sub>PD</sub>	(per flip-flop)	40				pF	

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

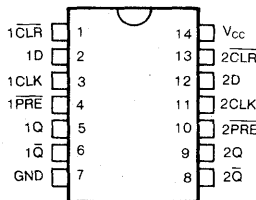
**DESCRIPTION**

These devices contain two independent positive-edge-triggered D-type flip-flops. Each flip-flop has its own data, clock, preset and clear inputs and complementary Q and  $\bar{Q}$  outputs. The preset and clear inputs are active-low and operate independently of the clock. Data at the D input is transferred to the Q outputs on the positive transition of the clock, provided setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**PIN CONFIGURATION**

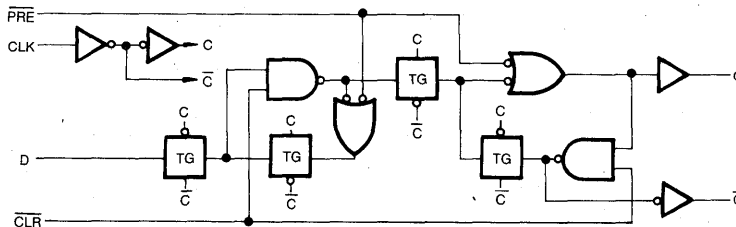


**FUNCTION TABLE**

Inputs				Outputs	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	↓	X	No Change	No Change

\* Both outputs will remain high as long as PRE and CLR are low, but the output states are unpredictable if PRE and CLR go high simultaneously.

**LOGIC DIAGRAM**



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ † . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r, t_f$ . . . . .	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS74A

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25	20			MHz
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		18	25	31	37			ns
	$t_{PHL}$		18	25	31	37			
Maximum Propagation Delay, PRE or CLR to Q or $\bar{Q}$	$t_{PLH}$		18	25	31	37			ns
	$t_{PHL}$		18	25	31	37			
Minimum Setup Time before CLK↑	Data		$t_{su}$	10	13	17	20		ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	10		13	17	20			
Minimum Hold Time, J or K after CLK↓	$t_h$		0	0	0	0		ns	
Minimum Pulse Width	CLK High or Low	$t_w$	8	15	20	25		ns	
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		8	15	20	25			
Maximum Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$ (per flip-flop)		40					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



#### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

#### DESCRIPTION

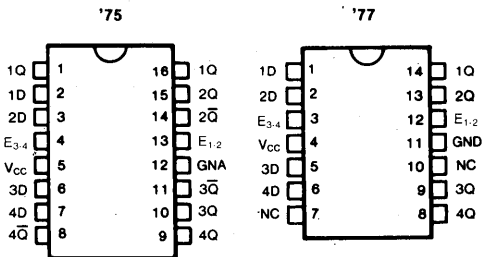
The '75 and '77 consist of 4 high-speed D-type latches that can be used as temporary storage for binary information between processing units. The '75 features complementary Q and  $\bar{Q}$  output while the '77 features single nail output. These devices are ideal for high component density application.

The latches are transparent: when the enable (E) is high, the Q output will follow the data input. When the enable goes low, the output latches at the level that was set up at the D-input.

These device provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

#### PIN CONFIGURATION

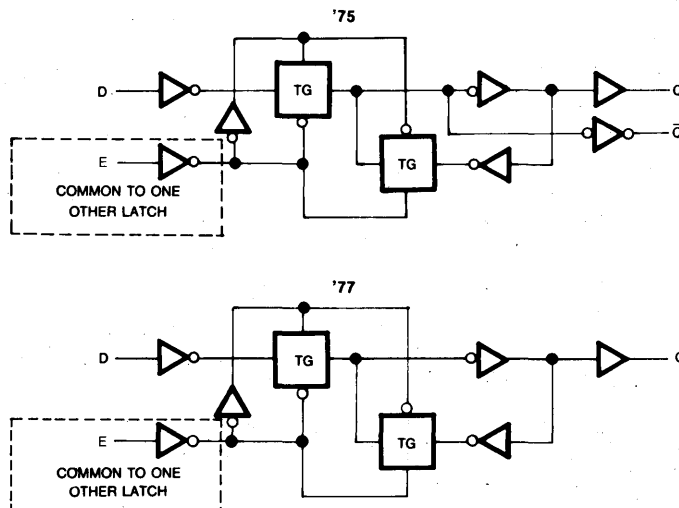


#### FUNCTION TABLE

Inputs		Outputs	
D	E	Q	$\bar{Q}^*$
L	H	L	H
H	H	H	L
X	L	Q <sub>0</sub>	$\bar{Q}_0$

\* $\bar{Q}$ : '75 only

#### LOGIC DIAGRAM



#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS75

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Propagation Delay, E to Q or $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	19	25	31	38	ns
	$t_{PHL}$		19	25	31	38	
Propagation Delay, D to Q or $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	13	21	26	32	ns
	$t_{PHL}$		13	21	26	32	
Data Set up Time D to E	$t_{SU}$		12	15	18	22	ns
Data Hold Time E to D	$t_h$		0	0	0	0	ns
Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS77

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Propagation Delay, E to Q	$t_{PLH}$	$C_L = 50\text{pF}$	13	18	23	27	ns
	$t_{PHL}$		13	18	23	27	
Propagation Delay, D to Q or $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	13	18	23	27	ns
	$t_{PHL}$		13	18	25	27	
Data Set up Time D to E	$t_{SU}$		12	15	18	22	ns
Data Hold Time E to D	$t_h$		0	0	0	0	ns
Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTL5 76A Dual J-K Flip-Flops with Preset and Clear

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTL5:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTL5:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

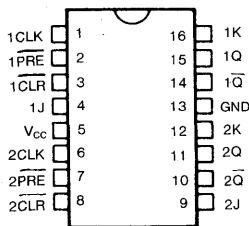
## DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

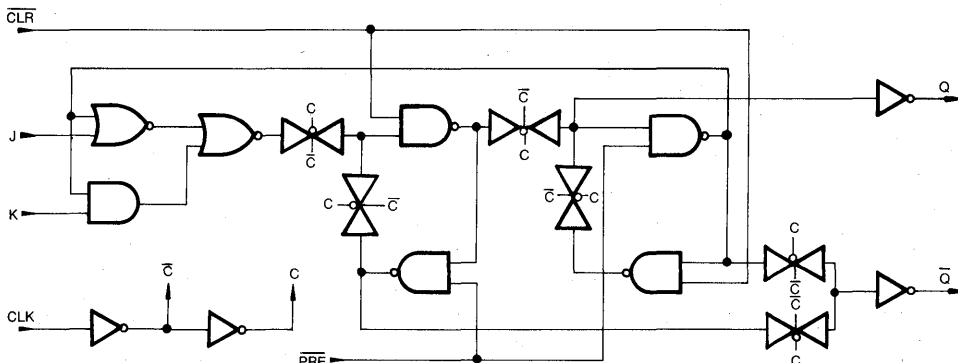


## FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

\* Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

## LOGIC DIAGRAM



# KS54HCTLS 76A Dual J-K Flip-Flops with Preset and Clear

## KS74HCTLS

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS76A

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25	21	MHz
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		15	20	25	30	ns
	$t_{PHL}$		15	20	25	30	
Maximum Propagation Delay, PRE or CLR to Q or $\bar{Q}$	$t_{PLH}$		15	20	25	30	ns
	$t_{PHL}$		15	20	25	30	
Minimum Setup Time before CLK↓	Data		$t_{su}$	10	13	17	20
	$\overline{\text{PRE}}$ or CLR Inactive	10		13	17	20	
Minimum Hold Time, J or K after CLK↓	$t_h$		0	0	0	0	ns
Minimum Pulse Width	CLK High or Low	$t_w$	10	13	17	20	ns
	$\overline{\text{PRE}}$ or CLR Low		10	13	17	20	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per flip-flop)	40				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

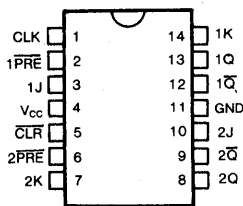
### DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K and preset inputs and complementary outputs. The clear and clock inputs are common to both flip-flops. The J-K inputs are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

### PIN CONFIGURATION

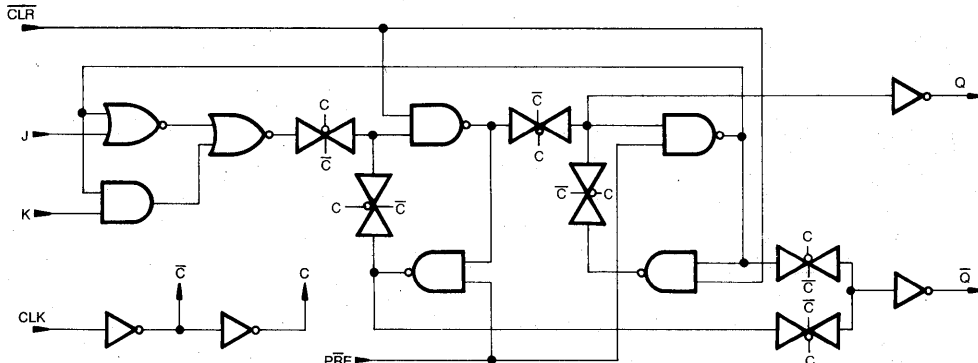


### FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↓	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

\*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per. Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	80.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	3.0	mA	

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS78A

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25	21			MHz
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		15	20	25	30			ns
	$t_{PHL}$		15	20	25	30			ns
Maximum Propagation Delay, PRE or CLR to Q or $\bar{Q}$	$t_{PLH}$		15	20	25	30			ns
	$t_{PHL}$	15	20	25	30			ns	
Minimum Setup Time before CLK↓	J or K	$t_{su}$	10	13	17	20			ns
	PRE or CLR Inactive		10	13	17	20			ns
Minimum Hold Time, J or K after CLK↓	$t_h$		0	0	0	0			ns
Minimum Pulse Width	CLK High or Low	$t_w$	10	13	17	20			ns
	PRE or CLR Low		10	13	17	20			ns
Maximum Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$ (per flip-flop)		40						pF

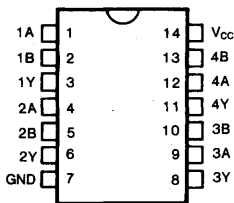
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .  $f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



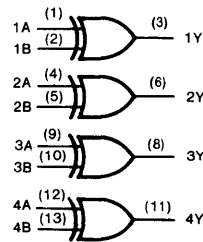
### DESCRIPTION

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions  $Y = A \oplus B$  or  $Y = \bar{A}B + A\bar{B}$ .

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### FUNCTION TABLE

(Each Gate)

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS86

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74 HCTLS	KS54 HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y (Other Input Low)	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15	20	25	30	ns
	t <sub>PHL</sub>		15	20	25	30	
Maximum Propagation Delay, A or B to Y (Other Input High)	t <sub>PLH</sub>		18	25	31	37	ns
	t <sub>PHL</sub>		18	25	31	37	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per gate)	15				pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

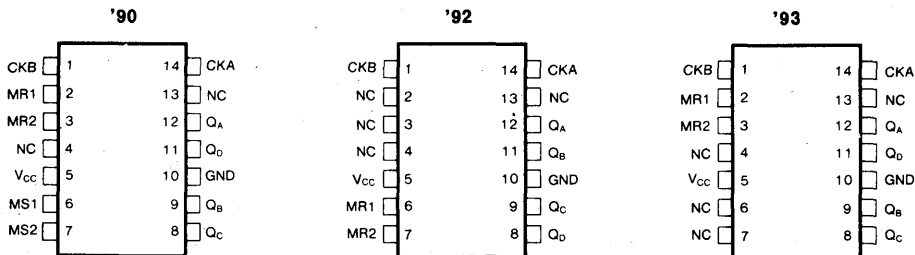
- Various counting mode.
- Function, Pin-out, speed and drive compatibility with 54/74 ALS logic family.
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8\text{mA} @ V_{OL} = 0.5\text{V}$
- Input and output interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**DESCRIPTION**

These devices contain four master-slave flip-flops and addition gating to provide a divide by a counter and a three-stage binary counter for which the count cycle length is divide by five for the HCTLS90, divide by six for the HCTLS92, and divide by eight for the HCTLS93. All of these counters have a gated zero reset and the HCTLS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four bit binary), the CKB input is connected to the  $Q_A$  output. The input count pulses are applied to CKA and the outputs are as described in the appropriate truth table. A symmetrical divide-by-the count can be obtained from the HCTLS90 counters by connecting the  $Q_D$  output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output  $Q_A$ .

**PIN CONFIGURATION**



**FUNCTION TABLE**

'90  
BCD COUNT SEQUENCE  
(See Note A)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90  
BI-QUINARY (5-2)  
(See Note B)

Count	Output			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92  
COUNT SEQUENCE  
(See Note C)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93  
COUNT SEQUENCE  
(See Note C)

Count	Output			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'90  
RESET/COUNT TRUTH TABLE

Reset Inputs				Output			
MR1	MR2	MS1	MS2	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92, '93  
RESET/COUNT TRUTH TABLE

Reset Inputs		Output			
MR1	MR2	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

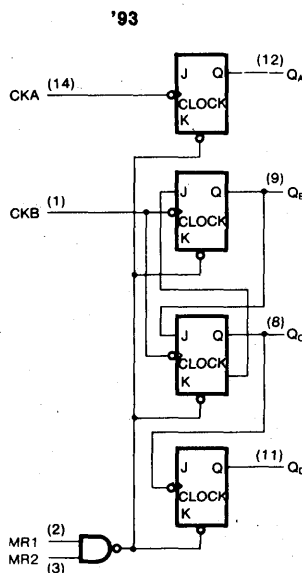
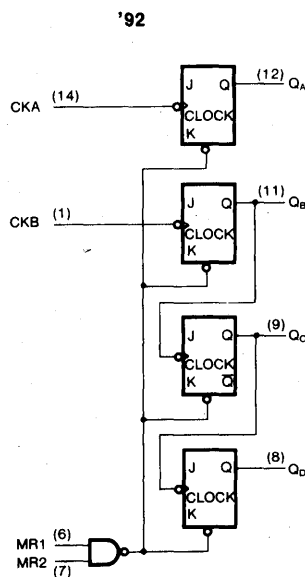
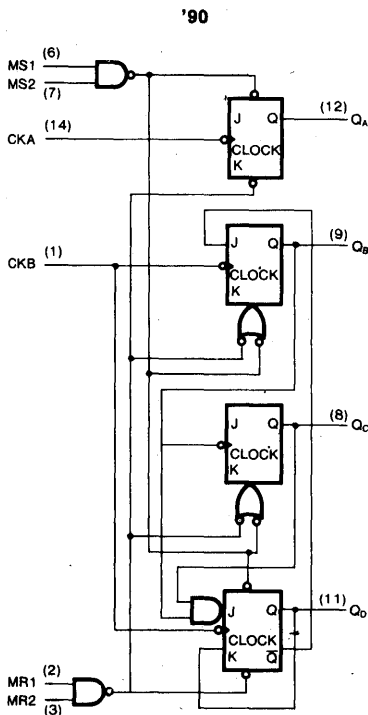
**Note A:** Output Q<sub>A</sub> is connected to input CKB for BCD count.

**Note B:** Output Q<sub>D</sub> is connected to input CKA for bi-quinary count.

**Note C:** Output Q<sub>A</sub> is connected to input CKB.

**Note D:** H=High Level, L=Low Level, X=Don't Care.

**LOGIC DIAGRAMS**



Note: The J.K inputs shown without connection are for reference only and are functionally at a high state.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$   
 Ceramic Package (J):  $-12\text{mW}/^\circ\text{C}$  from  $100^\circ\text{C}$  to  $125^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS90

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
			Maximum Clock Frequency	CKA to $Q_A$ CKB to $Q_B$	$f_{max}$	42	32	26	
Maximum Propagation Delay, CKA to $Q_A$		$t_{PLH}$	20	16	13	11		ns	
			10	16	20	24			
Maximum Propagation Delay CKA to $Q_D$		$t_{PLH}$	12	18	23	27		ns	
			32	48	60	72			
Maximum Propagation Delay CKB to $Q_B$		$t_{PHL}$	34	48	60	72		ns	
			10	16	20	24			
Maximum Propagation Delay, CKB to $Q_C$		$t_{PHL}$	14	21	26	32		ns	
			21	32	40	48			
Maximum Propagation Delay MS to $Q_A, Q_D$		$t_{PLH}$	23	35	43	52		ns	
			20	30	37	45			
Maximum Propagation Delay MS to $Q_B, Q_C$		$t_{PHL}$	26	40	50	60		ns	
			26	40	50	60			
Pulse Width	CKA	$t_w$	12	15	18	22		ns	
	CKB		24	30	36	44			
	MS		12	15	18	22			
	MR		12	15	18	22			
Recovery Time MR to CKA, CKB		$t_{rec}$	20	25	31	37		ns	
Maximum Input Capacitance		$C_{IN}$	5					pF	
Power Dissipation Capacitance		$C_{PD}$						pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS92

Characteristic		Symbol	Conditions†	TA = 25°C VCC = 5.0V		KS74HCTLS TA = -40°C to +85°C VCC = 5.0V ± 10%		KS54HCTLS TA = -55°C to +125°C VCC = 5.0V ± 10%		Unit
				Typ	Guaranteed Limits					
Maximum Clock Frequency	CKA to QA	f <sub>max</sub>	CL = 50pF	42	32	26		21		MHz
	CKB to QB			20	16	13		11		
Maximum Propagation Delay, CKA to QA		t <sub>PLH</sub>		10	16	20		24		ns
		t <sub>PHL</sub>		12	18	23		27		
Maximum Propagation Delay CKA to QD		t <sub>PLH</sub>		32	48	60		72		ns
		t <sub>PHL</sub>		34	48	60		72		
Maximum Propagation Delay CKB to QB		t <sub>PLH</sub>		10	16	20		24		ns
		t <sub>PHL</sub>		14	21	26		32		
Maximum Propagation Delay, CKB to QC		t <sub>PLH</sub>		10	16	20		24		ns
		t <sub>PHL</sub>		14	21	26		32		
Maximum Propagation Delay CKB to QD		t <sub>PLH</sub>		21	30	40		48		ns
		t <sub>PHL</sub>		23	35	43		52		
Maximum Propagation Delay: MR to Any Q		t <sub>PHL</sub>	26	40	50		60		ns	
Pulse Width	CKA			12	15	18		22		ns
	CKB			24	30	36		44		
	MR			12	15	18		22		
Recovery Time MR to CKA, CKB		t <sub>rec</sub>	20	25	31		37		ns	
Maximum Input Capacitance		C <sub>IN</sub>	5						pF	
Power Dissipation Capacitance		C <sub>PD</sub>							pF	

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>.

† For AC switching test circuits and timing waveforms see section 2.

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS93

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits	Typ	Guaranteed Limits	Typ	Guaranteed Limits	
Maximum Clock Frequency	CKA to Q <sub>A</sub>	$C_L = 50\text{pF}$	42	32	26	21	21	MHz	
	CKB to Q <sub>B</sub>		20	16	13	11			
Maximum Propagation Delay, CKA to Q <sub>A</sub>	t <sub>PLH</sub>		10	16	20	24	ns		
	t <sub>PHL</sub>		12	18	23	27			
Maximum Propagation Delay CKA to Q <sub>D</sub>	t <sub>PLH</sub>		46	70	87	105	ns		
	t <sub>PHL</sub>		46	70	87	105			
Maximum Propagation Delay CKB to Q <sub>B</sub>	t <sub>PLH</sub>		10	16	20	24	ns		
	t <sub>PHL</sub>		14	21	26	32			
Maximum Propagation Delay, CKB to Q <sub>C</sub>	t <sub>PLH</sub>		21	32	40	48	ns		
	t <sub>PHL</sub>		23	35	44	53			
Maximum Propagation Delay CKB to Q <sub>D</sub>	t <sub>PLH</sub>	34	50	60	70	ns			
	t <sub>PHL</sub>	34	50	60	70				
Maximum Propagation Delay: MR to Any Q	t <sub>PHL</sub>	26	40	50	60	ns			
Pulse Width	CKA	tw	12	15	18	22	ns		
	CKB		24	30	36	44			
	MR		12	15	18	22			
Recovery Time MR to CKA, CKB	t <sub>rec</sub>	20	25	31	37	ns			
Maximum Input Capacitance	C <sub>IN</sub>	5				pF			
Power Dissipation Capacitance	C <sub>PD</sub>					pF			

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:  
 $I_{OL} = 8\text{mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

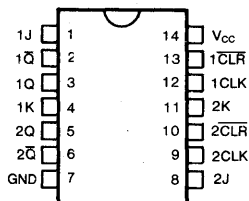
**DESCRIPTION**

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the  $\overline{\text{CLR}}$  input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

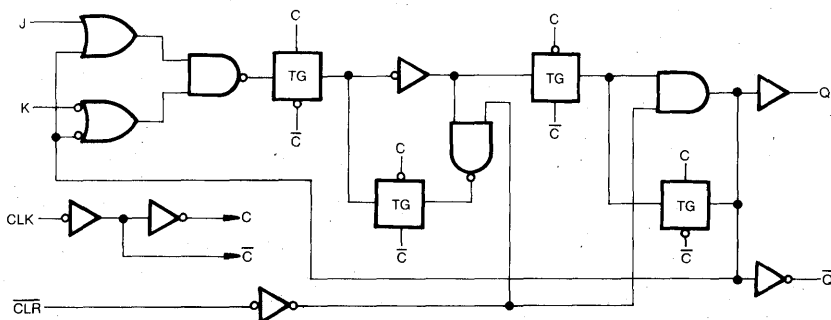
**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	$Q_0$	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	$Q_0$	$\overline{Q}_0$

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS107A

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	40	30	25	21	MHz
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	t <sub>PLH</sub>		15	20	25	30	ns
	t <sub>PHL</sub>		15	20	25	30	ns
Maximum Propagation Delay, CLR to Q or $\bar{Q}$	t <sub>PLH</sub>		15	20	25	30	ns
	t <sub>PHL</sub>	15	20	25	30	ns	
Minimum Setup Time before CLK↓	J or K	t <sub>su</sub>	10	13	17	20	ns
	$\bar{CLR}$ Inactive		10	13	17	20	ns
Minimum Hold Time, J or K after CLK↓	t <sub>h</sub>		0	0	0	0	ns
Minimum Pulse Width	CLK High or Low	t <sub>w</sub>	10	13	17	20	ns
	$\bar{CLR}$ Low		10	13	17	20	ns
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per flip-flop)	40				pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:  
I<sub>OL</sub> = 8mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

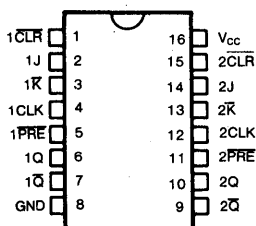
### DESCRIPTION

These devices contain two positive-edge-triggered J-K flip-flops with independent preset and clear inputs and complementary Q and  $\bar{Q}$  outputs. The preset and clear inputs are active-low and operate independently of the clock Data at the J and  $\bar{K}$  inputs are transferred to the outputs on the positive transition of the clock provided setup requirements have been met. These versatile flip-flops can perform as toggle flip-flops by grounding  $\bar{K}$  and tying J high. They can also perform as D-type flops if J and K are tied together.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

### PIN CONFIGURATION

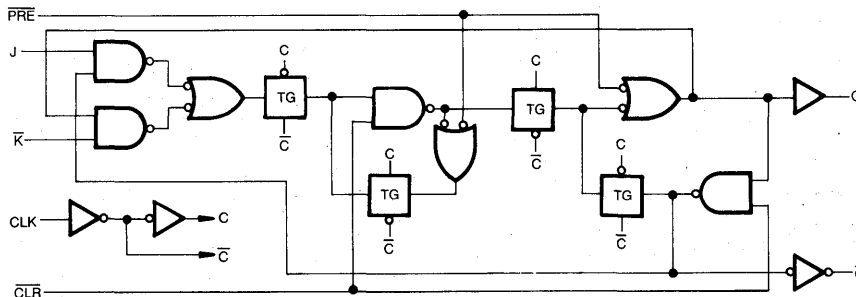


### FUNCTION TABLE

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	$\bar{L}$	H	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>

\*Both outputs will remain high as long as  $\overline{PRE}$  and  $\overline{CLR}$  are low, but the output states are unpredictable if  $\overline{PRE}$  and  $\overline{CLR}$  go high simultaneously.

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_{dF}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTL5: -40°C to +85°C  
 KS54HCTL5: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTL5	KS54HCTL5	Unit
			Typ	Guaranteed Limits			
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		4.0	40.0	80.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS109A

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ		Guaranteed Limits		
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	40	30	25	20	MHz
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	t <sub>PLH</sub>		18	25	31	37	ns
	t <sub>PHL</sub>		18	25	31	37	
Maximum Propagation Delay, PRE or CLR to Q or $\bar{Q}$	t <sub>PLH</sub>		18	25	31	37	ns
	t <sub>PHL</sub>		18	25	31	37	
Minimum Setup Time before CLK↑	Data		t <sub>su</sub>	10	13	17	20
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Inactive	10		13	17	20	
Minimum Hold Time, Data after CLK↓	t <sub>h</sub>		0	0	0	0	ns
Minimum Pulse Width	CLK High or Low	t <sub>w</sub>	8	15	20	25	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ Low		8	15	20	25	
Maximum Input Capacitance	*C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub> (per flip-flop)		40				pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:  
 $I_{OL} = 8\text{mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

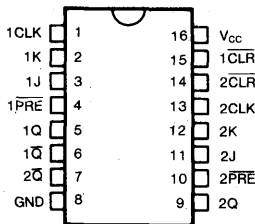
## DESCRIPTION

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

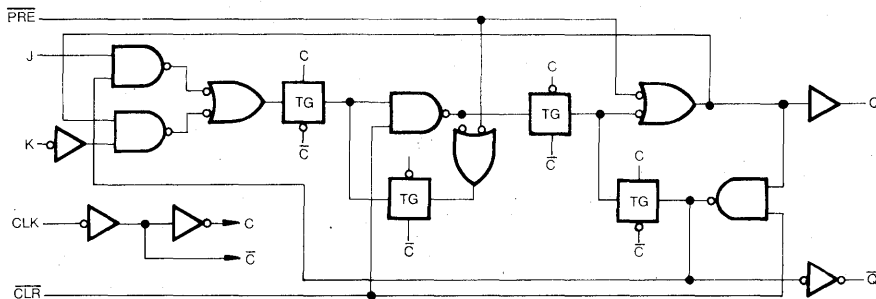


## FUNCTION TABLE

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

\*Both outputs will remain high as long as  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are low, but the output states are unpredictable if  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  go high simultaneously.

## LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_D$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		4.0	40.0	80.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS112A

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ		Guaranteed Limits		
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	40	30	25	21	MHz
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	t <sub>PLH</sub>		15	20	25	30	ns
	t <sub>PHL</sub>		15	20	25	30	
Maximum Propagation Delay, CLR to Q or $\bar{Q}$	t <sub>PLH</sub>		15	20	25	30	ns
	t <sub>PHL</sub>		15	20	25	30	
Minimum Setup Time before CLK↓	J or K		t <sub>su</sub>	10	13	17	20
	CLR Inactive	10		13	17	20	
Minimum Hold Time, Data after CLK↓	t <sub>h</sub>		0	0	0	0	ns
Minimum Pulse Width	CLK High or Low	t <sub>w</sub>	10	13	17	20	ns
	PRE or CLR Low		10	13	17	20	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per flip-flop)	40				pF

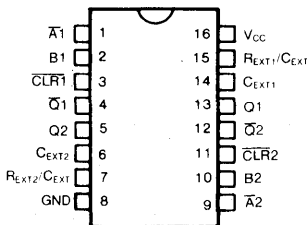
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Simple pulse width formula  $t_w = 0.45RC$
- DC triggered from active HIGH or active Low inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The '123 contains dual retriggerable monostable multivibrators with output pulse width control by three methods.

The basic pulse time is programmed by selection of an external resistor ( $R_{ext}$ ) and capacitor ( $C_{ext}$ ). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low going edge input ( $A_i$ ) or the active HIGH going edge input ( $B_i$ ). By repeating this process, the output pulse period ( $nQ=HIGH$ ,  $n\bar{Q}=LOW$ ) can be made as long as desired. Alternatively an output delay can be terminated at any time by a Low-going edge on input CLR, which also inhibits the triggering. An internal connection from CLR to the input gates makes it possible to trigger the circuit by a positive-going signal at input CLR as shown in the function table when  $C_{EXT} > 10nF$ , the typical output pulse width is defined as;  $t_w = 0.45 \times R_{EXT} \times C_{EXT}(typ)$ .

Where  $t_w$  is in seconds. R is in ohm. and C is in farads. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

Inputs			Outputs	
CLR	$\bar{A}$	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

- H= HIGH voltage level
- L= LOW voltage level
- X= don't care
- ↑= LOW to HIGH transition
- ↓= HIGH to LOW transition
- = one HIGH level output pulse
- = one LOW level output pulse

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  -65°C to +150°C  
 Power Dissipation Per Package,  $P_d \dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package(N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ..... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT} = 0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS123

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Propagation Delay $\bar{A}, B$ to $Q, \bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_{ext} = 0$	23	33	41	50	ns
	$t_{PHL}$		23	33	41	50	
Propagation Delay $\bar{CLR}$ to $Q, \bar{Q}$	$t_{PLH}$	$R_{ext} = 5\text{k}\Omega$	20	27	34	41	ns
	$t_{PHL}$		20	27	34	41	
Output Pulse Width 1	$tw_{Q1}$		116	200	207	209	ns
Output Pulse Width 2	$tw_{Q2}$	$C_L = 50\text{pF}$ $C_{ext} = 10\text{nF}$ $R_{ext} = 10\text{k}\Omega$	45	40 50	38(min) 52(max)	38(min) 52(max)	$\mu\text{s}$
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $A_i = \text{LOW}$	7	20	25	30	ns
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $B_i = \text{High}$	7	20	25	30	ns
Clear Pulse Width	$t_w$	$C_L = 50\text{pF}$ $CLR_i = \text{LOW}$	8	20	25	30	ns
External Timing Resistance	$R_{ext}$			2 100	2(min) 100 (max)	2(min) 100 (max)	$\text{k}\Omega$
External Timing Capacitance	$C_{ext}$			no restriction			pF
Input Capacitance	$C_{in}$		5				pF
Power Dissipation Capacitance	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance.

For output pulse widths greater than  $100\mu\text{s}$  or external capacitance greater than  $10\text{nF}$  the following equation should be used.

$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

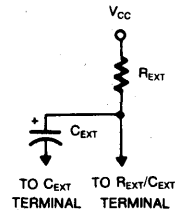
Where

$t_w$  is in  $\mu\text{s}$

K is the multiplying factor  
and is approximately 0.45 for  
 $C_{ext}$  is in nF  
 $R_{ext}$  is in  $\text{k}\Omega$

For best results, system ground should be applied to the  $C_{ext}$  terminal. These devices do not require a switching diode in series with the  $R_{ext}/C_{ext}$  terminal (as required by some other monostable multivibrators)

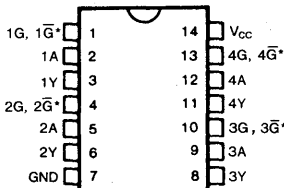
### TIMING COMPONENT



### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



\*  $\bar{G}$  for '125; G for '126

### FUNCTION TABLES

'125

Inputs		Output Y
A	$\bar{G}$	
H	L	H
L	L	L
X	H	Z

'126

Inputs		Output Y
A	G	
H	H	H
L	H	L
X	L	Z

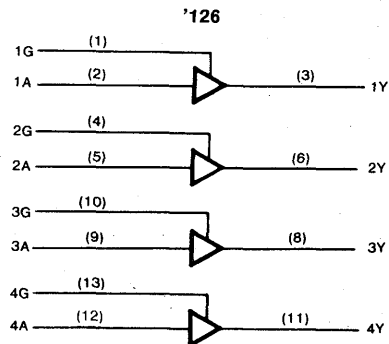
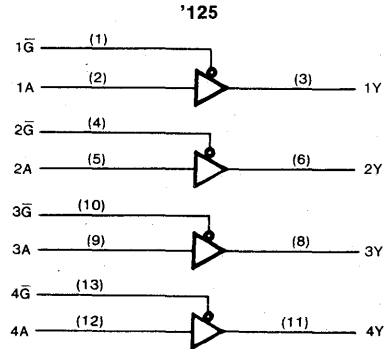
### DESCRIPTION

These bus buffers feature four independent line drivers with 3-state outputs. The output enable functions for the '125 buffers are active-low, while those for '126 are active high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAMS





#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS125, HCTLS126

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit	
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ		Guaranteed Limits			
Maximum Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	13	18	22	27	ns	
		$C_L = 150\text{pF}$	16	21	27	33		
	$t_{PHL}$	$C_L = 50\text{pF}$	13	18	22	27		
		$C_L = 150\text{pF}$	16	21	27	33		
Maximum Output Enable Time, Enable to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	17	23	29	34	ns
			$C_L = 150\text{pF}$	20	26	34	40	
	$t_{PZL}$	$C_L = 50\text{pF}$	17	23	29	34		
		$C_L = 150\text{pF}$	20	26	34	40		
Maximum Output Disable Time, Enable to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	16		26	32	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	16		26	32		
Maximum Input Capacitance	$C_{IN}$		5				pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10				pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	Output Disabled	5				pF	
		Output Enabled	30					

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**DESCRIPTION**

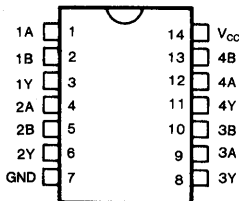
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function  $Y = \overline{A \cdot B} = \overline{A} + \overline{B}$  in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

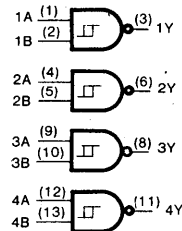
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

INPUTS		OUTPUTS Y
A	B	
L	L	H
L	H	H
H	L	H
H	H	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.11$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0			$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0			mA

**DC ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Min	Max	Min	Max	Min	Max	
Positive-Going Threshold Voltage	$V_{T+}$	$V_{CC}=4.5V$	1.2	1.9	1.2	1.9	1.2	1.9	V
		$V_{CC}=5.5V$	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going Threshold Voltage	$V_{T-}$	$V_{CC}=4.5V$	0.5	1.2	0.5	1.2	0.5	1.2	V
		$V_{CC}=5.5V$	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis ( $V_{T+} - V_{T-}$ )	$V_H$	$V_{CC}=4.5V$	0.4	1.4	0.4	1.4	0.4	1.4	V
		$V_{CC}=5.5V$	0.4	1.5	0.4	1.5	0.4	1.5	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS132

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74 HCTLS	KS54 HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	17	22	28	33	ns
	$t_{PHL}$		17	22	28	33	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)					pF

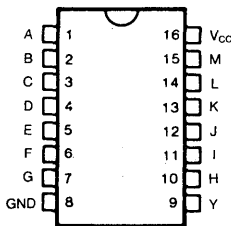
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

INPUTS A THRU M		OUTPUT Y
All inputs	H	L
One or more inputs	L	H

**DESCRIPTION**

The 133 contains a single 13-input NAND gate. It performs the Boolean functions (in positive logic):

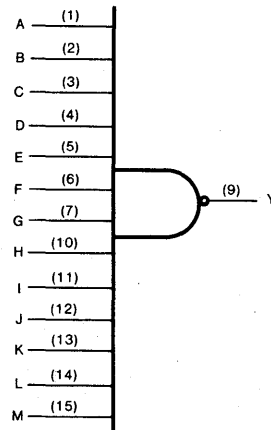
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

$$Y = \overline{A + B + C + D + E + F + G + H + I + J + K + L + M}$$

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**LOGIC DIAGRAM**



5

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS133

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits	Guaranteed Limits		
Maximum Propagation Delay Any Input to Y	$t_{PLH}$	$C_L = 50\text{pF}$	18	24	30	36	ns
	$t_{PHL}$		18	25	30	36	
Maximum Input Capacitance	$C_{IN}$		5			pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15			pF	

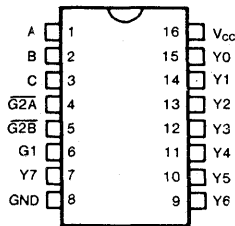
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

Enable Inputs		Select Inputs			Outputs							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H
H	L	H	H	L	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	L	H

\* G2 = G2A + G2B

**DESCRIPTION**

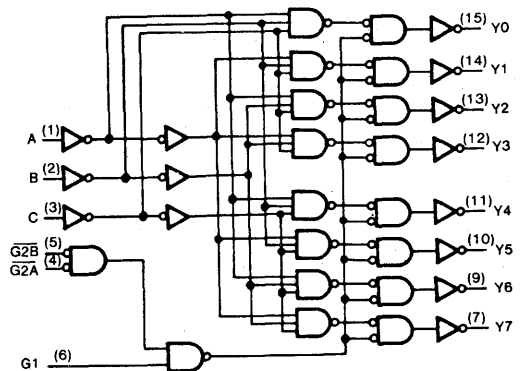
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

**LOGIC DIAGRAM**





**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ		Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	160.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	3.0	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS138

Characteristic	Symbol	Conditions <sup>1</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74 HCTLS	KS54 HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y	$t_{PLH}$	$C_L = 50\text{pF}$	22	30	37	45	ns
	$t_{PHL}$		22	30	37	45	
Maximum Propagation Delay, G1 to any Y	$t_{PLH}$		24	32	40	48	ns
	$t_{PHL}$		24	32	40	48	
Maximum Propagation Delay, G2A or G2B to any Y	$t_{PLH}$		18	25	31	37	ns
	$t_{PHL}$		18	25	31	37	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	)	50				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

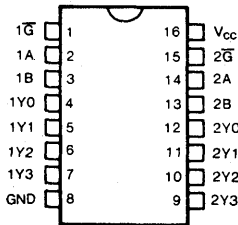
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The '139 consists of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

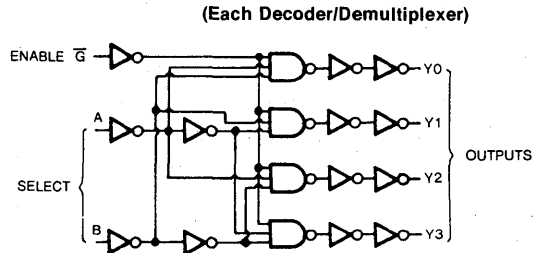
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs			Outputs			
Enable G	Select B A		Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**5**

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS139

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A or B to Y	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	22	30	37	45	ns
	t <sub>PHL</sub>		22	30	37	45	
Maximum Propagation Delay, G to any Y	t <sub>PLH</sub>		21	28	35	42	ns
	t <sub>PHL</sub>		21	28	35	42	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>		50				pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Encodes eight data lines in priority
- Provides 3-bit binary priority code
- Input enable capability
- Easily cascadable
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

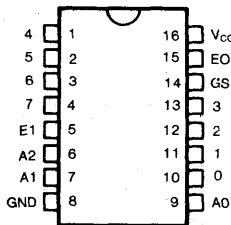
**DESCRIPTION**

The '148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

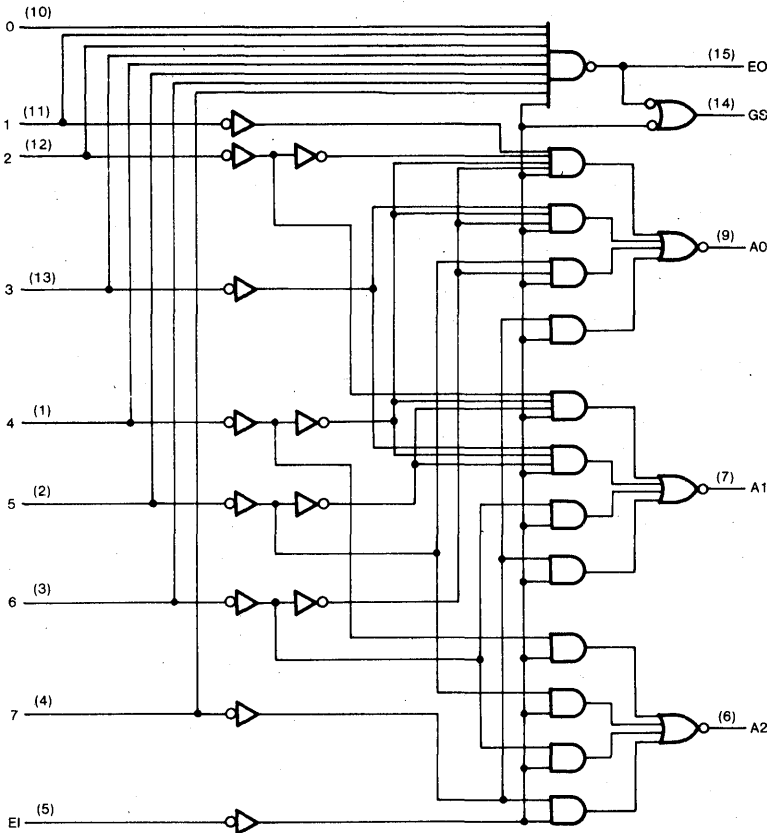
**PIN CONFIGURATION**



**FUNCTION TABLE**

EI	Inputs							Outputs					
	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{STG}$  . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ		Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84		$V_{CC}-0.1$ 3.7		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$		$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0		160.0		$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9		3.0		mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS148

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, 1-7 to A0, A1 or A2	$t_{PLH}$	$C_L=50\text{pF}$	20	27	34	41			ns
	$t_{PHL}$		20	27	34	41			
Maximum Propagation Delay, 0-7 to EO	$t_{PLH}$		22	29	36	44			ns
	$t_{PHL}$		22	29	36	44			
Maximum Propagation Delay, 0-7 to GS	$t_{PLH}$		28	38	47	57			ns
	$t_{PHL}$		28	38	47	57			
Maximum Propagation Delay, EI to A0, A1 or A2	$t_{PLH}$		19	25	31	38			ns
	$t_{PHL}$		19	25	31	38			
Maximum Propagation Delay, EI to GS	$t_{PLH}$		20	26	33	39			ns
	$t_{PHL}$		20	26	33	39			
Maximum Propagation Delay, EI to EO	$t_{PLH}$		21	28	35	42			ns
	$t_{PHL}$		21	28	35	42			
Maximum Input Capacitance	$C_{IN}$			5					pF
Power Dissipation Capacitance*	$C_{PD}$		(per gate)	50					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

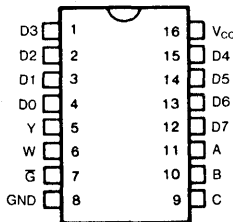
† For AC switching test circuits and timing waveforms see section 2.



#### FEATURES

- Can perform as:
  - Boolean Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  - KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
  - KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

#### PIN CONFIGURATION



#### DESCRIPTION

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ( $\bar{G}$ ) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\bar{G}$		
X	X	X	H	L	H
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

H = high level, L = low level, X = irrelevant  
D0, D1 ... D7 = the level of the D respective input

#### Absolute Maximum Ratings\*

- Supply Voltage Range  $V_{CC}$  .....  $-0.5V$  to  $+7V$
- DC Input Diode Current,  $I_{IK}$  ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20 \text{ mA}$
- DC Output Diode Current,  $I_{OK}$  ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20 \text{ mA}$
- Continuous Output Current Per Pin,  $I_O$  ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70 \text{ mA}$
- Continuous Current Through  $V_{CC}$  or GND pins .....  $\pm 250 \text{ mA}$
- Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$
- Power Dissipation Per Package,  $P_d$  .....  $500 \text{ mW}$

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

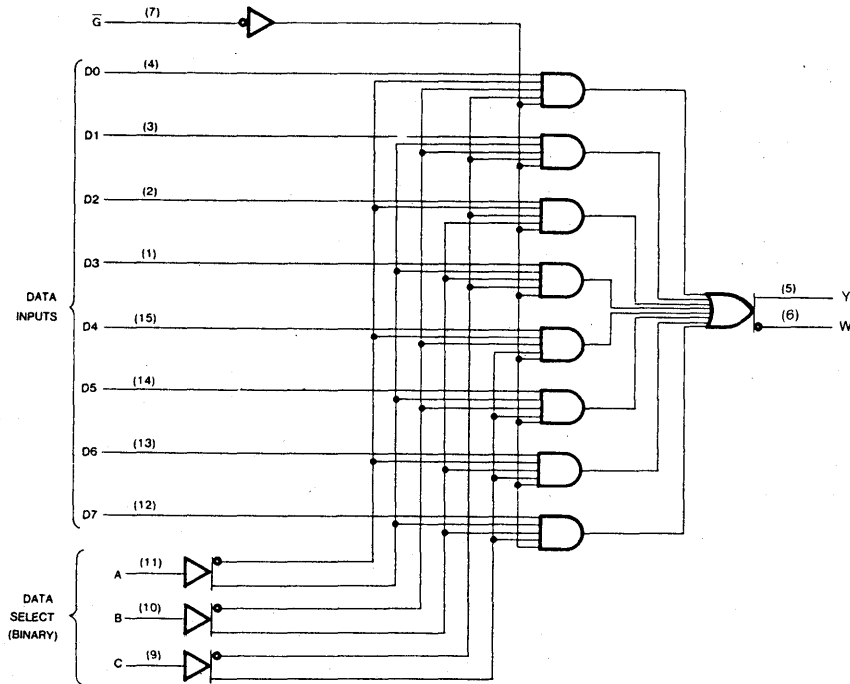
† Power Dissipation temperature derating:

Plastic Package (N):  $-12 \text{ mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

#### Recommended Operating Conditions

- Supply Voltage,  $V_{CC}$  .....  $4.5V$  to  $5.5V$
  - DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ...  $0V$  to  $V_{CC}$
  - Operating Temperature
    - Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
    - KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
  - Input Rise & Fall Times,  $t_r, t_f$  ..... Max  $500 \text{ ns}$
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**LOGIC DIAGRAM**



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0		V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8		V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0		$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0		mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS151

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A, B or C to Y	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40	48	ns
		$C_L = 150\text{pF}$	27	35	45	54	
	$t_{PHL}$	$C_L = 50\text{pF}$	24	32	40	48	
		$C_L = 150\text{pF}$	27	35	45	54	
Maximum Propagation Delay, A, B or C to W	$t_{PLH}$	$C_L = 50\text{pF}$	27	36	45	54	ns
		$C_L = 150\text{pF}$	30	39	50	60	
	$t_{PHL}$	$C_L = 50\text{pF}$	27	36	45	54	
		$C_L = 150\text{pF}$	30	39	50	60	
Maximum Propagation Delay, Any D to Y	$t_{PLH}$	$C_L = 50\text{pF}$	20	26	33	39	ns
		$C_L = 150\text{pF}$	23	29	38	45	
	$t_{PHL}$	$C_L = 50\text{pF}$	20	26	33	39	
		$C_L = 150\text{pF}$	23	29	38	45	
Maximum Propagation Delay, Any D to W	$t_{PLH}$	$C_L = 50\text{pF}$	16	21	26	32	ns
		$C_L = 150\text{pF}$	19	24	31	38	
	$t_{PHL}$	$C_L = 50\text{pF}$	16	21	26	32	
		$C_L = 150\text{pF}$	19	24	31	38	
Maximum Propagation Delay, $\bar{G}$ to Y	$t_{PLH}$	$C_L = 50\text{pF}$	20	26	33	39	ns
		$C_L = 150\text{pF}$	23	29	38	45	
	$t_{PHL}$	$C_L = 50\text{pF}$	20	26	33	39	
		$C_L = 150\text{pF}$	23	29	38	45	
Maximum Propagation Delay, $\bar{G}$ to W	$t_{PLH}$	$C_L = 50\text{pF}$	20	26	33	39	ns
		$C_L = 150\text{pF}$	23	29	38	45	
	$t_{PHL}$	$C_L = 50\text{pF}$	20	26	33	39	
		$C_L = 150\text{pF}$	23	29	38	45	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

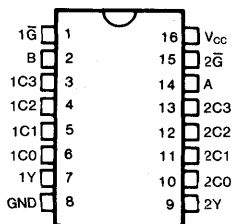
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Allows Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- '153 is the 3-State Version of this port
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### DESCRIPTION

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ( $\bar{G}$ ) are provided for each of the two four-line sections.

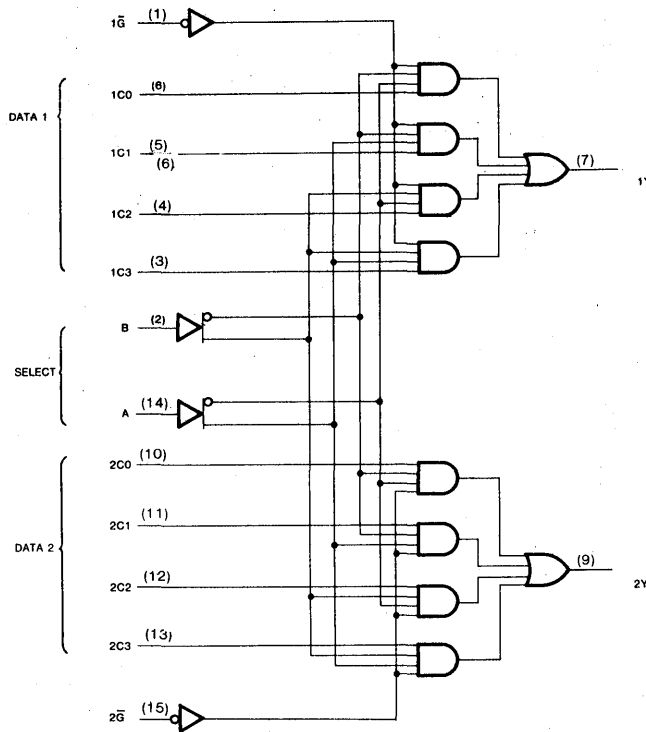
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , .....	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....	$\pm 70$ mA
Continuous Current Through $V_{CC}$ or GND pins .....	$\pm 250$ mA
Storage Temperature Range, $T_{stg}$ .....	-65°C to +150°C
Power Dissipation Per Package, $P_d$ † .....	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage, $V_{CC}$ .....	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ ..	0V to $V_{CC}$
Operating Temperature Range	KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$ .....	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS153

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC}=5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y	$t_{PLH}$	$C_L=50\text{pF}$	23	30	38	45	ns
		$C_L=150\text{pF}$	26	33	43	51	
	$t_{PHL}$	$C_L=50\text{pF}$	23	30	38	45	ns
		$C_L=150\text{pF}$	26	33	43	51	
Maximum Propagation Delay, Data (Any C) to Y	$t_{PLH}$	$C_L=50\text{pF}$	15	20	25	30	ns
		$C_L=150\text{pF}$	18	23	30	36	
	$t_{PHL}$	$C_L=50\text{pF}$	15	20	25	30	ns
		$C_L=150\text{pF}$	18	23	30	36	
Maximum Propagation Delay, G to Y	$t_{PLH}$	$C_L=50\text{pF}$	21	28	35	42	ns
		$C_L=150\text{pF}$	24	31	40	48	
	$t_{PHL}$	$C_L=50\text{pF}$	21	28	35	42	ns
		$C_L=150\text{pF}$	24	31	40	48	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

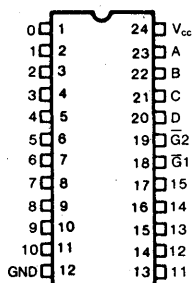
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input to Any One of 16 Outputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



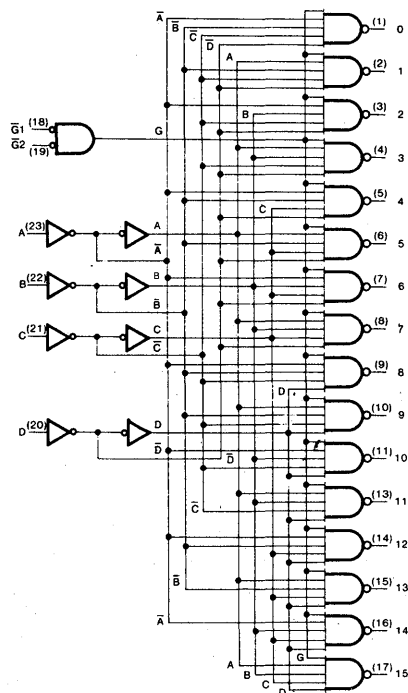
### DESCRIPTION

These monolithic, 4-line to 16-line decoders decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs,  $\bar{G}_1$  and  $\bar{G}_2$ , are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



# KS54HCTLS 154 4-Line to 16-Line Decoders/Demultiplexers

## KS74HCTLS

### FUNCTION TABLE

Inputs					Outputs																	
$\bar{G}1$	$\bar{G}2$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{STG}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		<b>KS74HCTLS</b> $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		<b>KS54HCTLS</b> $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	$V_{CC}-0.1$ 3.7	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	80.0	160.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	2.9	3.0	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS154

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		<b>KS74 HCTLS</b> $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		<b>KS54HCTLS</b> $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay, A, B, C or D to Any Output	$t_{PLH}$	$C_L = 50\text{pF}$	21	28	35	35	42	42	ns
	$t_{PHL}$		21	28	35	35	42	42	
Maximum Propagation Delay, G1 or G2 to Any Output	$t_{PLH}$		21	28	35	35	42	42	ns
	$t_{PHL}$		21	28	35	35	42	42	
Maximum Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$								pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Typical applications:**  
Dual 2-to-4 line decoder  
Dual 1-to-4 line demultiplexer  
3-to-8 line decoder  
1-to-8 line demultiplexer
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

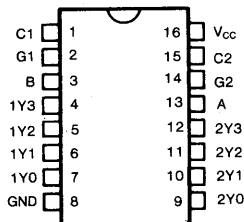
**DESCRIPTION**

The '155 consists of two 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

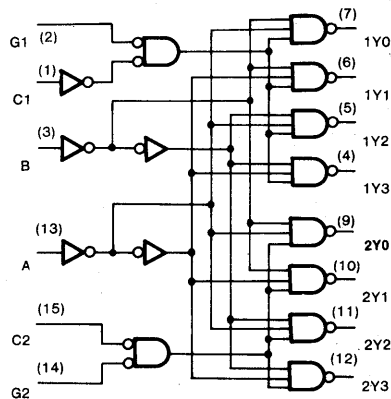
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLES**

**2-to-4 Line Decoder or 1-to-4 Line Demultiplexer**

Inputs			Outputs				
Select	Strobe	Data					
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs			Outputs				
Select	Strobe	Data					
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

**3-to-8 Line Decoder or 1-to-8 Line Demultiplexer**

Select		Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	L	H	H
H	L	H	L	H	H	H	H	H	L	H
H	H	L	L	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	L	L

†=Inputs C1 and C2 Connected together

‡=Inputs G1 and G2 Connected together

**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA
- Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C
- Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$
- Operating Temperature  
Range  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS155)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay, A, B, C2, G1 or G2 to any Output (2 levels of logic)	$t_{PLH}$	$C_L=50\text{pF}$	17	23	29	35			ns
	$t_{PHL}$		17	23	29	35			
Maximum Propagation Delay, A or B to any Y (3 levels of logic)	$t_{PLH}$		21	28	35	42			ns
	$t_{PHL}$		21	28	35	42			
Maximum Propagation Delay, C1 to any Y	$t_{PHL}$		20	27	34	41			ns
	$t_{PHL}$		20	27	34	41			
Maximum Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

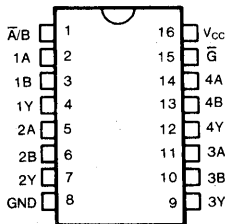
### DESCRIPTION

These are data selectors/multiplexers which select a 4-bit word from one of two sources via the control of a common select input ( $\bar{A}/B$ ). A separate strobe input ( $\bar{G}$ ) is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

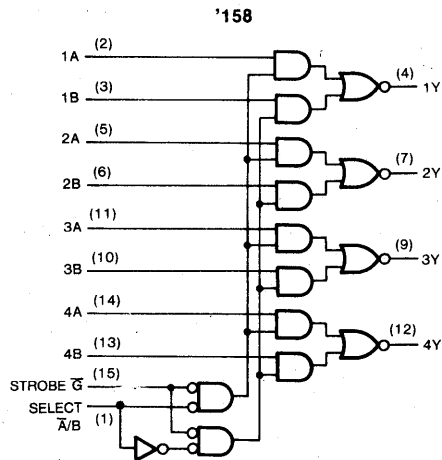
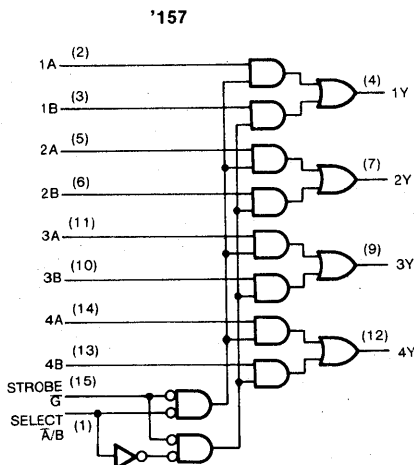
### PIN CONFIGURATION



### FUNCTION TABLE

Inputs				Output Y	
Strobe $\bar{G}$	Select $\bar{A}/B$	Data		'157	'158
		A	B		
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

### LOGIC DIAGRAMS



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d \dagger$  . . . . . 500 mW

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

5

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS157, HCTLS158

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54 HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Propagation Delay, A or B to Y	$t_{PLH}$		11	15	19	22	ns
	$t_{PHL}$		11	15	19	22	
Maximum Propagation Delay, $\bar{A}/\bar{B}$ to Y	$t_{PLH}$		17	23	29	34	ns
	$t_{PHL}$		17	23	29	34	
Maximum Propagation Delay, $\bar{G}$ to Y	$t_{PLH}$		15	20	25	30	ns
	$t_{PHL}$		15	20	25	30	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

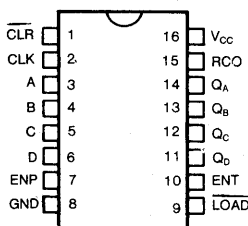
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Internal Look Ahead for Fast Counting
- Carry Output for n-bit cascading
- Synchronous Counting
- Synchronously Programmable
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLES**

'160, '161

CLK	CLR	ENP	ENT	LOAD	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

'162, '163

CLK	CLR	ENP	ENT	LOAD	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

**DESCRIPTION**

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The '160 and '162 are decade counters, and the '161 and '163 are 4-bit binary counters. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '162 and '163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with QA high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or LOAD) that will modify the operating model have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

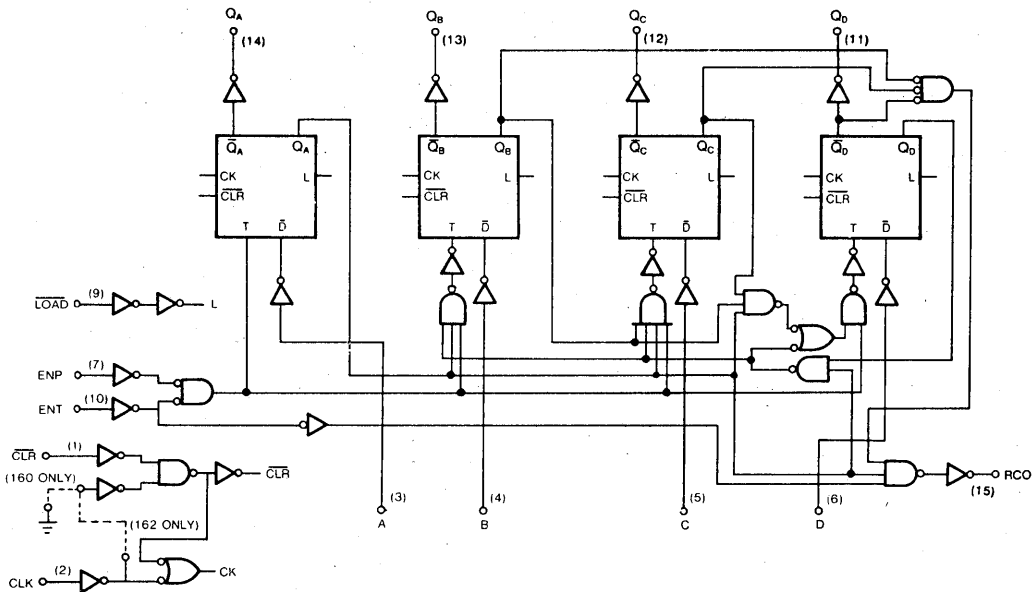
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to Vcc and ground.

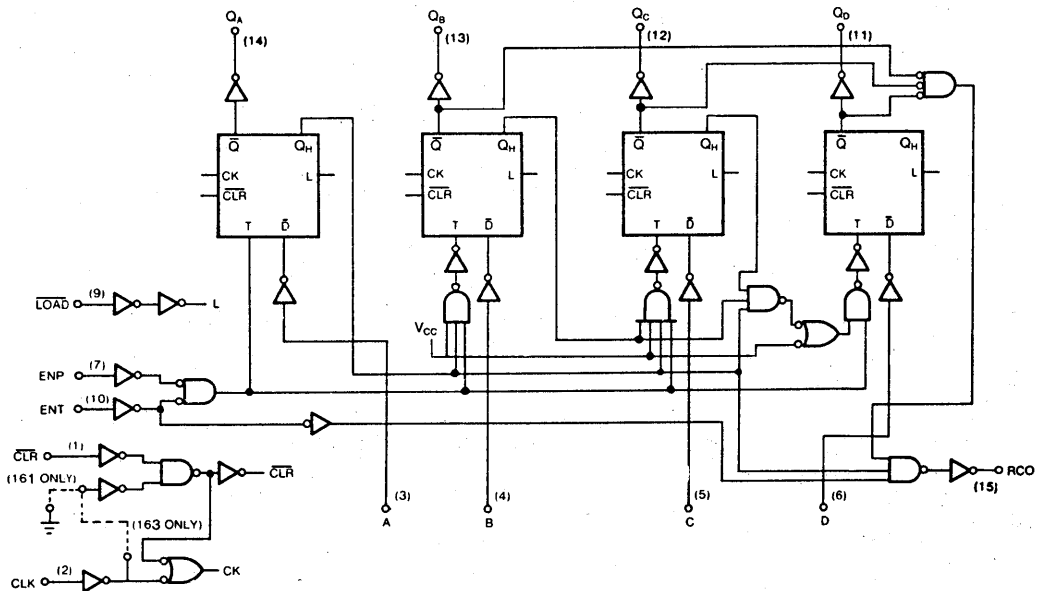


**LOGIC DIAGRAMS**

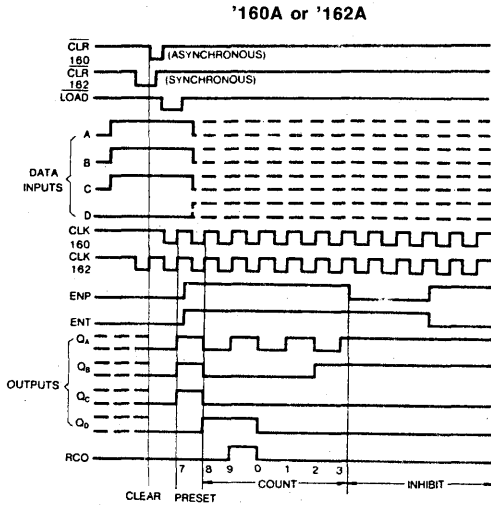
**'160A or '162A**



**'161A or '163A**

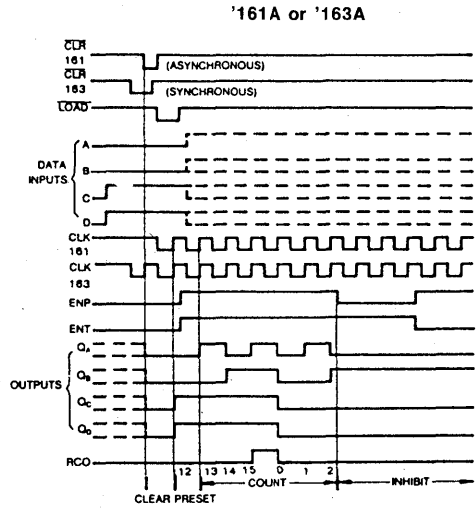


### Typical Clear, Preset, Count and Inhibit Sequences



**Sequence:**

- (1) Clear outputs to zero
- (2) Preset to BCD seven
- (3) Count to eight, nine, zero, one, two, and three
- (4) Inhibit



**Sequence:**

- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one and two
- (4) Inhibit

### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 35$ mA
Continuous Current Through	
$V_{CC}$ or GND pins	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	0V to $V_{CC}$
Operating Temperature	
Range	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r, t_f$	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

# KS54HCTLS 160A/161A KS74HCTLS 162A/163A

## Synchronous 4-Bit Decade and Binary Counters

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS160A, HCTLS161A

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit	
			Typ	Guaranteed Limits				
Maximum Clock Frequency	$f_{max}$		40	30	25	20	MHz	
Maximum Propagation Delay, CLK to RCO	$t_{PLH}$	$C_L=50\text{pF}$	26	35	44	53	ns	
	$t_{PHL}$		26	35	44	53		
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$		20	26	33	39	ns	
	$t_{PHL}$		20	26	33	39		
Maximum Propagation Delay, ENT to RCO	$t_{PLH}$		11	14	18	21	ns	
	$t_{PHL}$		11	14	18	21		
Maximum Propagation Delay, CLR to any Q	$t_{PHL}$		21	28	35	42	ns	
Maximum Propagation Delay, CLR to RCO	$t_{PHL}$		21	28	35	42	ns	
Minimum Pulse Width	CLK High or Low		$t_w$	10	13	17	20	ns
	CLR Low			10	13	17	20	
Minimum Setup Time before CLK†	A, B, C, D	$t_{su}$	10	13	17	20	ns	
	LOAD		10	13	17	20		
	ENP, ENT		10	13	17	20		
	CLR inactive		10	13	17	20		
Minimum Hold Time, All Synchronous Inputs after CLK†	$t_h$		0	0	0	0	ns	
Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$		80				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS **160A/161A** KS74HCTLS **162A/163A**

## Synchronous 4-Bit Decade and Binary Counters

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS162A, HCTLS163A

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25		20		MHz
Maximum Propagation Delay, CLK to RCO	$t_{PLH}$		26	35	44		53		ns
	$t_{PHL}$		26	35	44		53		
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$		20	26	33		39		ns
	$t_{PHL}$		20	26	33		39		
Maximum Propagation Delay, ENT to RCO	$t_{PLH}$		11	14	18		21		ns
	$t_{PHL}$		11	14	18		21		
Maximum Propagation Delay, $\overline{\text{CLR}}$ to any Q	$t_{PHL}$		21	28	35		42		ns
Maximum Propagation Delay, $\overline{\text{CLR}}$ to RCO	$t_{PHL}$	21	28	35		42		ns	
Minimum Pulse Width	CLK High or Low	$t_w$	10	13	17		20		ns
	$\overline{\text{CLR}}$ Low		10	13	17		20		
Minimum Setup Time before CLK†	A, B, C, D	$t_{su}$	10	13	17		20		ns
	LOAD		10	13	17		20		
	ENP, ENT		10	13	17		20		
	$\overline{\text{CLR}}$ inactive		10	13	17		20		
	$\overline{\text{CLR}}$ Low		10	13	17		20		
Minimum Hold Time, All Synchronous Inputs after CLK†	$t_h$		0	0	0		0		ns
Input Capacitance	$C_{iN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$		80						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **AND—Gated (enable/disable) serial inputs**
- **Fully buffered clock and serial inputs**
- **Direct clear**
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

**DESCRIPTION**

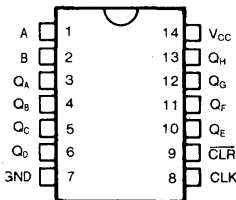
These are high-speed 8-bit registers with AND-gated serial inputs and an asynchronous clear. Data is entered serially through either one of the two inputs, A and B. A high on one input enables the other one, which will then determine the state of the first flip-flop. A low at either or both inputs inhibits data entry and resets the first flip-flop to a low level at the next positive clock transition.

Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of their clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

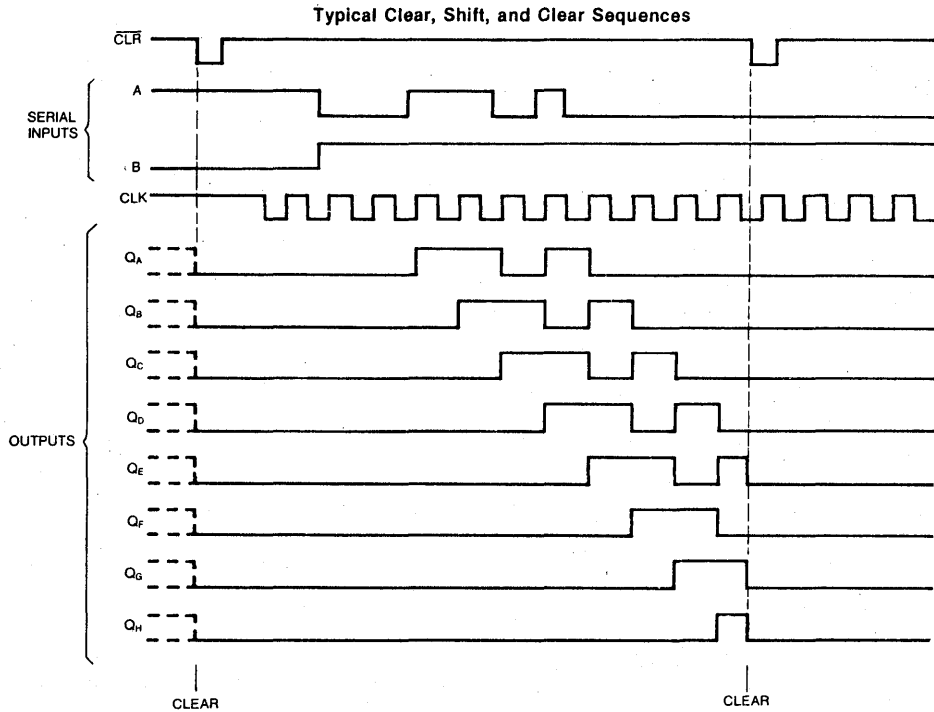
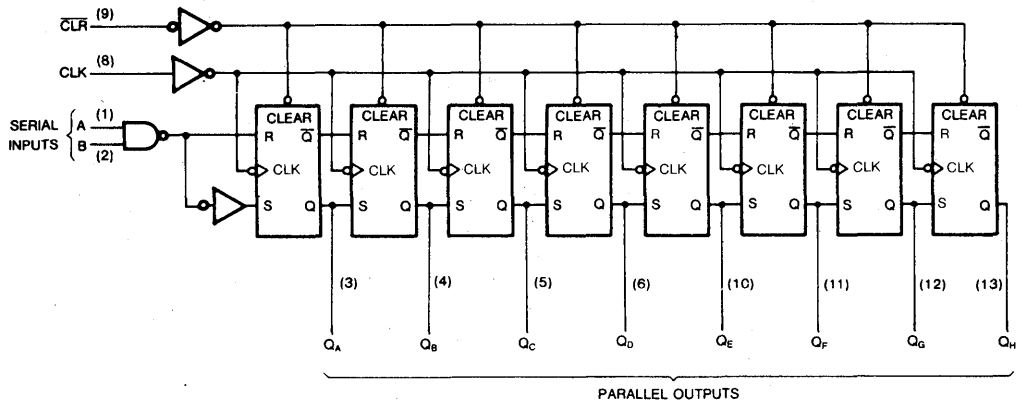


**FUNCTION TABLE**

Inputs				Outputs		
Clear	Clock	A	B	QA	QB . . . QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

H = high level (steady state), L = low level (steady state)  
 X = irrelevant (any input, including transitions)  
 ↑ = transition from low to high level.  
 QA0, QB0, QH0 = the level of QA, QB or QH, respectively, before the indicate steady-state input conditions were established.  
 QAn, QGn = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_D$ † . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}$ , $V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r$ , $t_f$ . . . . .	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS164

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	40	30	25	20	MHz
Maximum Propagation Delay, CLR to any Q	t <sub>PLH</sub>		27	36	45	54	ns
Maximum Propagation Delay, CLK to any Q	t <sub>PLH</sub>		22	30	37	45	ns
	t <sub>PHL</sub>		22	30	37	45	
Minimum Pulse Width	CLR Low	t <sub>w</sub>	10	13	17	20	ns
	CLK High or Low		10	13	17	20	
Minimum Setup Time before CLK†	Data	t <sub>su</sub>	8	10	13	15	ns
	CLR Inactive		8	10	13	15	
Minimum Hold Time Data after CLK†	t <sub>h</sub>		0	5	5	5	ns
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per package)	120				pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-Serial data conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

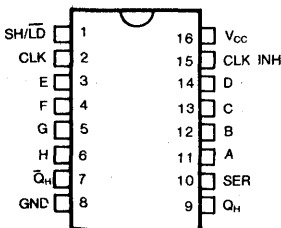
These are high-speed 8-bit parallel-load or serial-in shift registers with complementary serial outputs available from the last stage. Parallel-in access is asynchronous and is enabled by pulling the SH/LD input low. When SH/LD is high, data is entered serially at the SER input and shifted one place to the right with each positive clock transition.

Clocking is accomplished through a 2-input NOR gate which permits one of the clocks to be used as a clock inhibit function. Holding either clock input high inhibits clocking. Either clock input is enabled by holding the other clock input low while the SH/LD input is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**PIN CONFIGURATION**

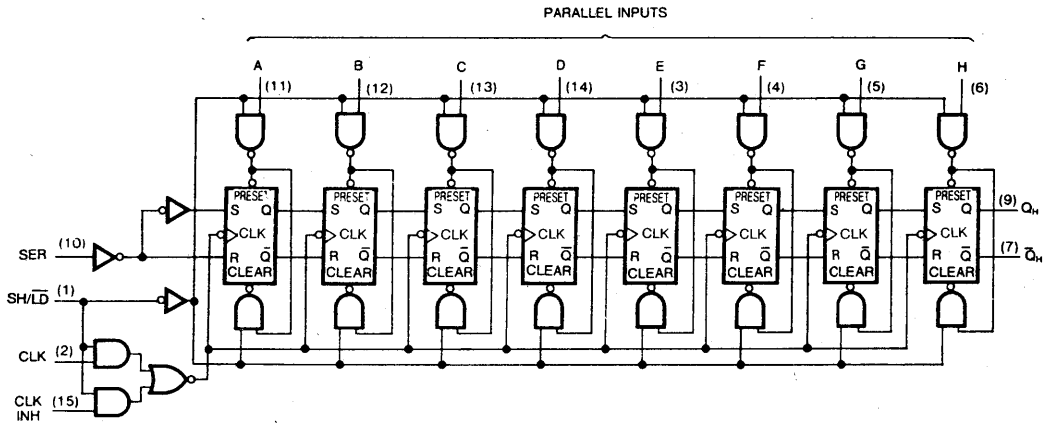


**FUNCTION TABLE**

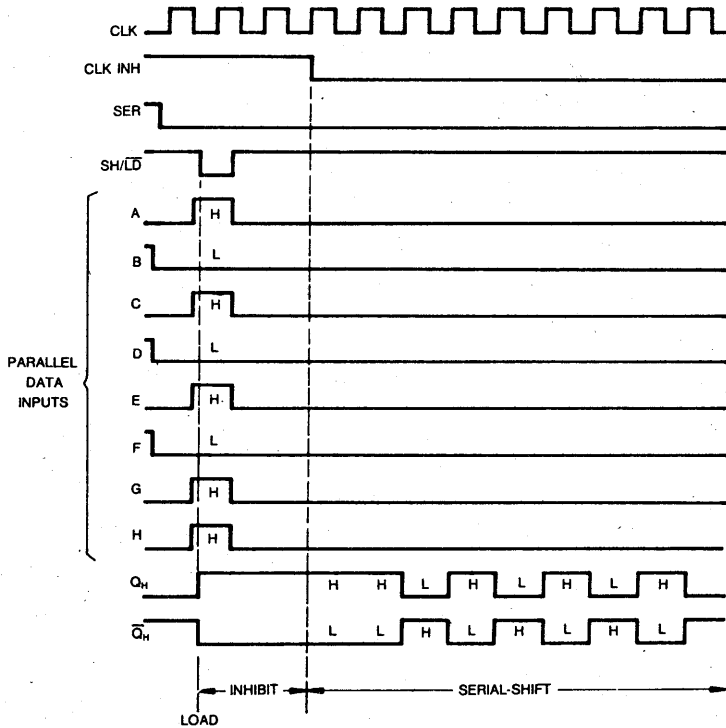
Inputs			Function
SH/LD	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT*
H	↑	L	SHIFT*

\* Content of each internal register shifts toward output Q<sub>H</sub>. Data at serial input is shifted into first register.

LOGIC DIAGRAM



Typical Shift, Load and Inhibit Sequences



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS165

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74HCTLS		KS54HCTLS		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\%$	$V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits				
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25	20		MHz
Maximum Propagation Delay, SH/LD to $Q_H$ or $\bar{Q}_H$	$t_{PLH}$		26	35	44	53		ns
	$t_{PHL}$		26	35	44	53		ns
Maximum Propagation Delay, CLK to $Q_H$ or $\bar{Q}_H$	$t_{PHL}$		30	40	50	60		ns
	$t_{PLH}$		30	40	50	60		ns
Maximum Propagation Delay, H to $Q_H$ or $\bar{Q}_H$	$t_{PLH}$		20	27	34	41		ns
	$t_{PHL}$		20	27	34	41		ns
Minimum Pulse Width	SH/LD Low		$t_w$	7	10	13	15	
	CLK High or Low	13		16	20	25		ns
Minimum Setup Time	SH/LD High before CLK†	$t_{su}$	13	16	20	25		ns
	SER before CLK†		10	13	17	20		
	CLK INH Low before CLK†		13	16	20	25		
	CLK INH High before CLK†		13	16	20	25		
	Data before SH/LD†		5	7	8	10		
Minimum Hold Time	SER Data after CLK†	$t_h$	-3	0	0	0		ns
	PAR Data after SH/LD†		-3	0	0	0		
Maximum Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$		100					pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Synchronous load
- Direct overriding clear
- Parallel to serial conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

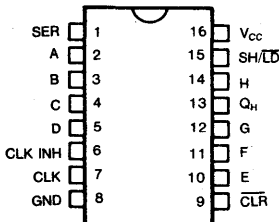
**DESCRIPTION**

These devices feature parallel-in or serial-in, serial-out registers, gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, the input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

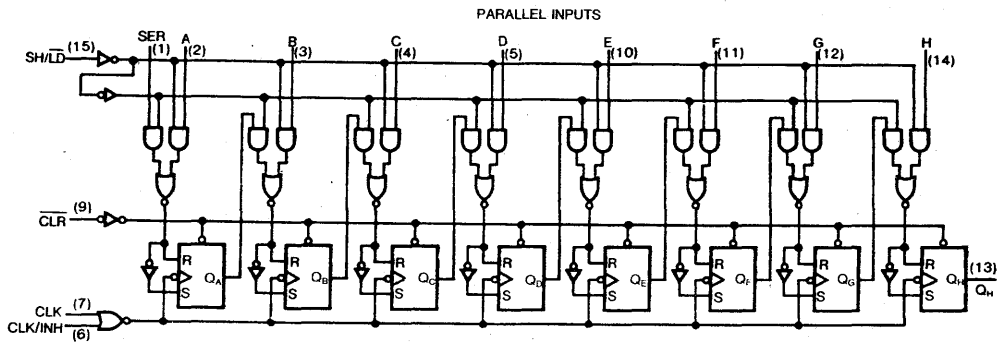
**PIN CONFIGURATION**



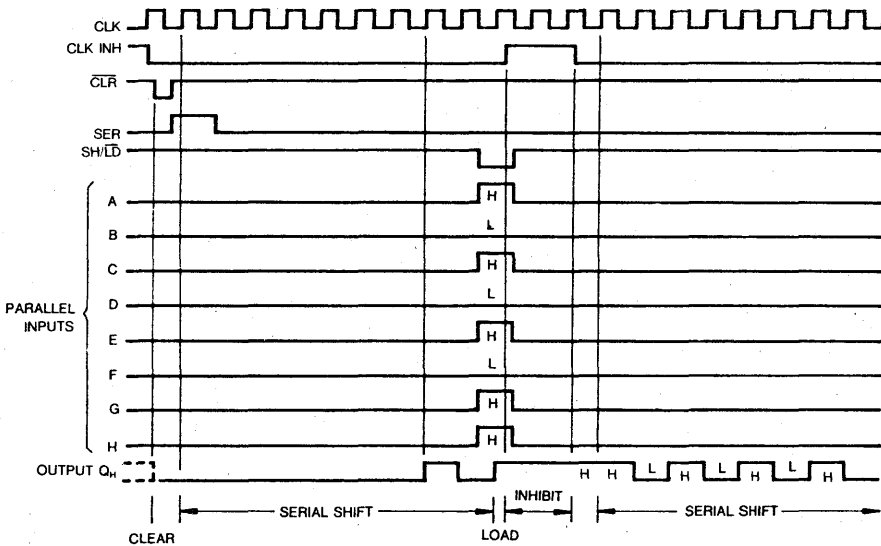
**FUNCTION TABLE**

Inputs					SER	Internal		Output $Q_H$
$\overline{\text{CLR}}$	SH/LD	CLK INH	CLK	Parallel A ... H		$Q_A$	$Q_B$	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	L	↑	X	a ... h	a	b	h
H	H	L	↑	H	X	H	$Q_{An}$	$Q_{Gn}$
H	H	L	↑	L	X	L	$Q_{An}$	$Q_{Gn}$
H	X	H	↑	X	X	$G_{A0}$	$Q_{B0}$	$Q_{H0}$

LOGIC DIAGRAM



Typical Clear, Shift, Load, Inhibit, and Shift Sequences



5

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS166

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	40	30	25	20	MHz
Maximum Propagation Delay, CLR to Q <sub>H</sub>	t <sub>PHL</sub>		22	30	37	45	ns
Maximum Propagation Delay, CLK to Q <sub>H</sub>	t <sub>PLH</sub>		26	36	44	53	ns
	t <sub>PHL</sub>		26	35	44	53	
Minimum Pulse Width	CLR Low	t <sub>w</sub>	10	13	17	20	ns
	CLK High or Low		10	13	17	20	
Minimum Setup Time	SH/LD High before CLK↑	t <sub>su</sub>	10	13	17	20	ns
	SER before CLK↑		10	13	17	20	
	CLK INH before CLK↑		10	13	17	20	
	Data before SH/LD↑		10	13	17	20	
	CLR Inactive before CLK ↑		10	13	17	20	
Minimum Hold Time	SH/LD High after CLK↑	t <sub>h</sub>	7	10	12	15	ns
	SER after CLK↑		7	10	12	15	
	CLK INH after CLK↑		7	10	12	15	
	Data after SH/LD↑		7	10	12	15	
	CLR Active after CLK↑		7	10	12	15	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

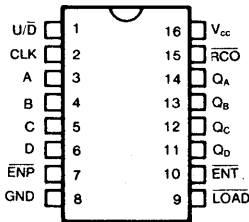
† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Fully Synchronous Operation for Counting and Programming
- Internal Look Ahead for Fast Counting
- Carry Output for N-bit Cascading
- Fully Independent Clock Circuit
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The '168 is a decade counter and the '169 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

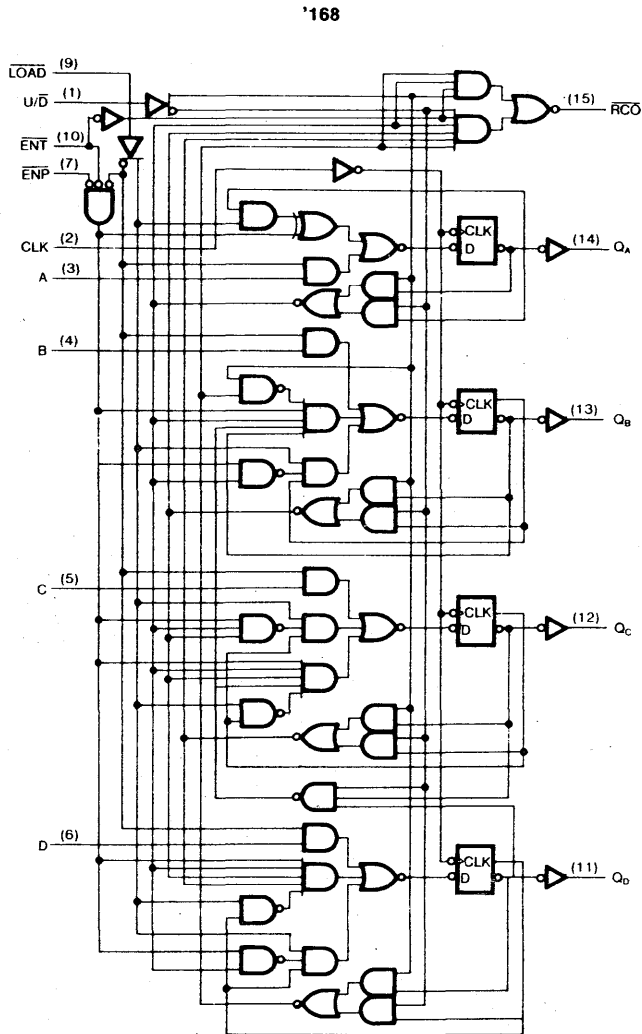
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ( $\overline{\text{ENP}}$  and  $\overline{\text{ENT}}$ ) must be low to count. The direction of the count is determined by the level of the U/D input. When U/D is high, the counter counts up; when low, it counts down. Input  $\overline{\text{ENT}}$  is fed forward to enable the carry output. The ripple carry output ( $\overline{\text{RCO}}$ ) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transition at  $\overline{\text{ENP}}$  or  $\overline{\text{ENT}}$  are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs ( $\overline{\text{ENP}}$ ,  $\overline{\text{ENT}}$ , LOAD, U/D) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

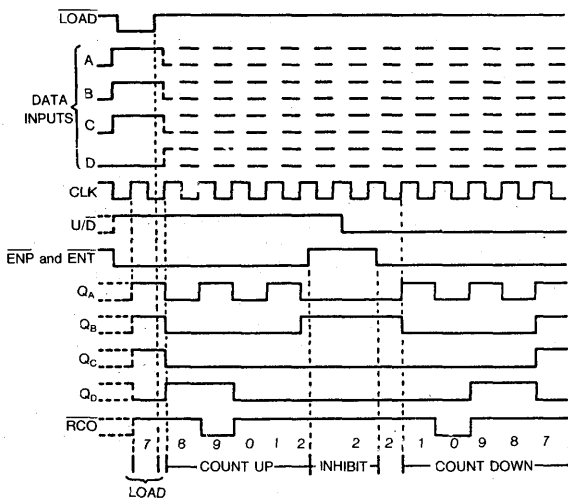
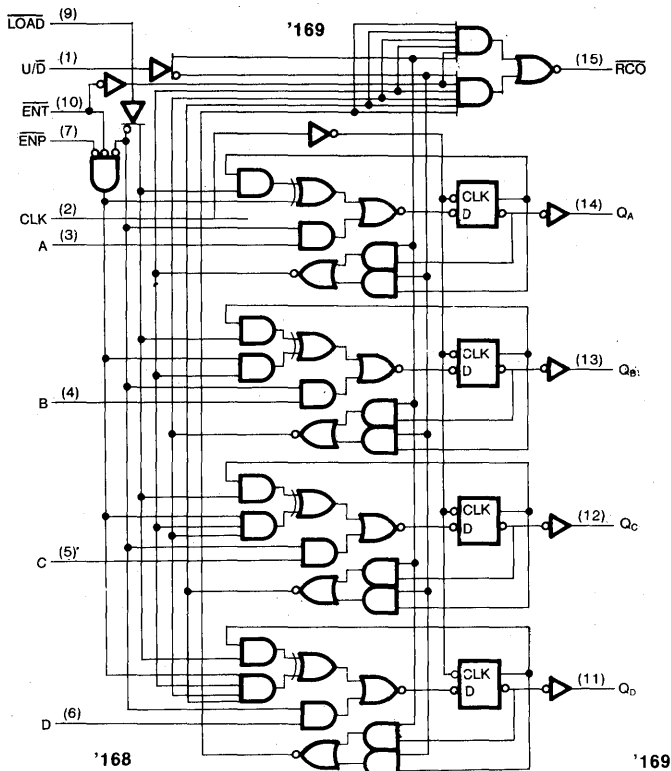
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>cc</sub> and ground.

LOGIC DIAGRAMS

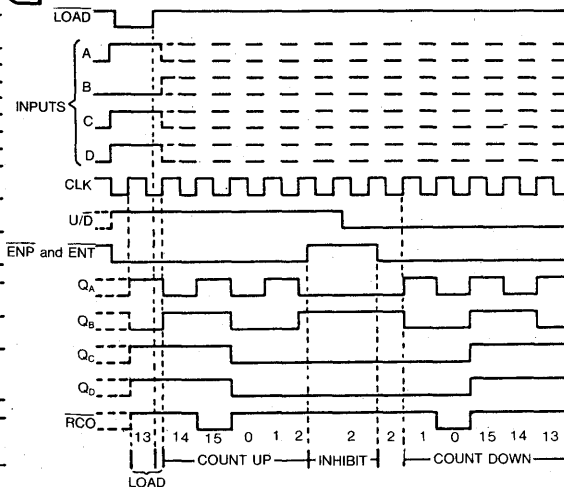


**LOGIC DIAGRAMS (Continued)**



Illustrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



Illustrated above is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

**FUNCTION TABLE**

OPERATING MODE	INPUTS						OUTPUTS	
	CLK	U/D	ENP	ENT	LOAD	D <sub>n</sub>	Q <sub>n</sub>	RCO
Parallel Load	↑	X	X	X	l	i	L	(1)
	↑	X	X	X	i	h	H	(1)
Count Up	↑	h	l	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold	↑	X	h	X	h	X	q <sub>n</sub>	(1)
	↑	X	X	h	h	X	q <sub>n</sub>	H

H=HIGH voltage level steady state

h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L=LOW voltage level steady state

l=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X=Don't care

q=Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑=LOW-to-HIGH clock transition

**NOTE:**

1. The  $\overline{RCO}$  is LOW when  $\overline{ENT}$  is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.

The  $\overline{RCO}$  is LOW when  $\overline{ENT}$  is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

**Absolute Maximum Ratings\***

Supply Voltage Range V<sub>CC</sub>, . . . . . -0.5V to +7V

DC Input Diode Current, I<sub>IK</sub>

(V<sub>I</sub> < -0.5V or V<sub>I</sub> > V<sub>CC</sub> + 0.5V) . . . . . ±20 mA

DC Output Diode Current, I<sub>OK</sub>

(V<sub>O</sub> < -0.5V or V<sub>O</sub> > V<sub>CC</sub> + 0.5V) . . . . . ±20 mA

Continuous Output Current Per Pin, I<sub>O</sub>

(-0.5V < V<sub>O</sub> < V<sub>CC</sub> + 0.5V) . . . . . ±35 mA

Continuous Current Through

V<sub>CC</sub> or GND pins . . . . . ±125 mA

Storage Temperature Range, T<sub>stg</sub>, . . . . . -65°C to +150°C

Power Dissipation Per Package, P<sub>d</sub>† . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): - 12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage, V<sub>CC</sub> . . . . . 4.5V to 5.5V

DC Input & Output Voltages\*, V<sub>IN</sub>, V<sub>OUT</sub> . . . 0V to V<sub>CC</sub>

Operating Temperature

Range KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t<sub>r</sub>, t<sub>f</sub> . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>CC</sub> or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	160.0	$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS168, HCTLS169)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ C$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Operating Frequency	$f_{max}$	$C_L = 50pF$	35	30	25	20	MHz		
Maximum Propagation Delay, CLK to $\overline{RCO}$	$t_{PLH}$		26	35	44	52	ns		
	$t_{PHL}$		26	35	44	52			
Maximum Propagation Delay, CLK to Ary Q	$t_{PLH}$		17	22	28	33	ns		
	$t_{PHL}$		17	22	28	33			
Maximum Propagation Delay, ENT to $\overline{RCO}$	$t_{PLH}$		15	20	25	30	ns		
	$t_{PHL}$		15	20	25	30			
Maximum Propagation Delay, U/D to $\overline{RCO}$	$t_{PLH}$		20	27	34	40	ns		
	$t_{PHL}$		20	27	34	40			
Minimum Pulse Duration, CLK high or low	$t_w$			12	16	20	24	ns	
Minimum Setup Time Before CLK†	A, B, C or D			12	16	20	24	ns	
	ENP or ENT		$t_{su}$	12	16	20	24	ns	
	LOAD		12	16	20	24	ns		
	U/D		12	16	20	24	ns		
Minimum Hold Time, Data after CLK†	$t_h$		0	0	0	0	ns		
Maximum Input Capacitance	$C_{IN}$		5				pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 173 KS74HCTLS 4-Bit D-Type Registers with 3-State Outputs

## FEATURES

- Gated output control lines for enabling or disabling the outputs
- Fully independent clock for operation in parallel-load or hold modes
- For application as bus buffer registers
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5 \text{ V}$  for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

These 4-bit registers contain D-type flip-flops with 3-state outputs, capable of driving highly-capacitive or low-impedance loads. This provides the device with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components.

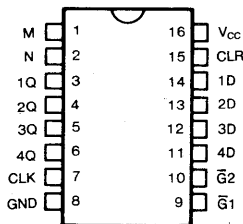
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gated output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION



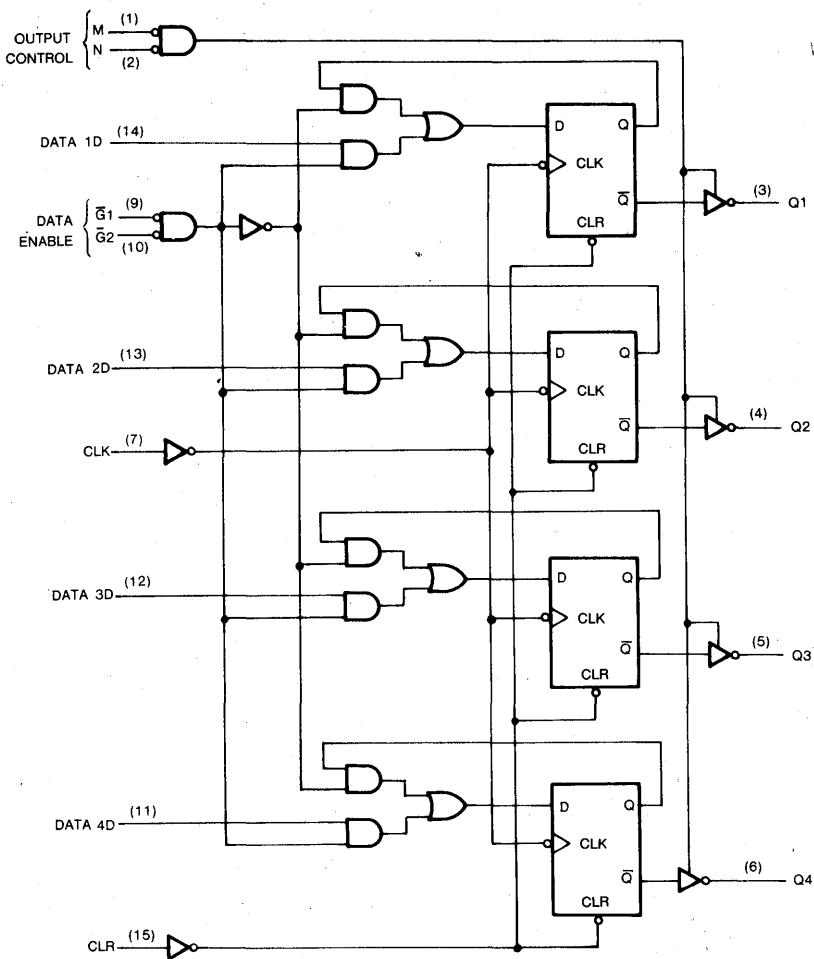
## FUNCTION TABLE

Clear	Clock	Input		Data D	Output Q
		Data Enable			
		$\bar{G}1$	$\bar{G}2$		
H	X	X	X	X	L
L	L	X	X	X	$Q_0$
L	↑	H	X	X	$Q_0$
L	↑	X	H	X	$Q_0$
L	↑	L	L	L	L
L	↑	L	L	H	H

When either  $\bar{M}$  or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

# KS54HCTLS 173 KS74HCTLS 4-Bit D-Type Registers with 3-State Outputs

## LOGIC DIAGRAM



# KS54HCTLS 173 4-Bit D-Type Registers with 3-State Outputs

## KS74HCTLS

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



# KS54HCTLS 173 4-Bit D-Type Registers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns, HCTLS173)

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ		Guaranteed Limits					
Maximum Clock Frequency	$f_{max}$		45	30	25		20		MHz	
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	20	27	34		41		ns	
		$C_L = 150\text{pF}$	23	30	39		47			
Maximum Propagation Delay, CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$	20	27	34		41		ns	
		$C_L = 150\text{pF}$	23	30	39		47			
Maximum Propagation Delay, CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$	22	30	37		45		ns	
		$C_L = 150\text{pF}$	25	33	42		51			
Maximum Output Enable Time, M or N to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	25	31		37		ns
			$C_L = 150\text{pF}$	21	28	36		43		
Maximum Output Disable Time, M or N to any Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	25	31		37		ns
			$C_L = 150\text{pF}$	21	28	36		43		
Maximum Output Disable Time, M or N to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega, C_L = 50\text{pF}$	15	20	25		30		ns	
	$t_{PLZ}$		15	20	25		30			
Minimum Pulse Width	CLK High or Low	$t_w$	10	13	17		20		ns	
	CLR High		10	13	17		20			
Minimum before CLK <sup>†</sup>	$\bar{G}1$ and $\bar{G}2$	$t_{su}$	15	20	25		30		ns	
	Data		8	11	14		17			
	CLR Inactive		5	7	8		10			
Minimum Hold Time After CLK <sup>†</sup>	$\bar{G}1$ and $\bar{G}2$	$t_h$	0	0	0		0		ns	
	Data		0	0	0		0			
Maximum Input Capacitance	$C_{IN}$		5						pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF	
Power Dissipation Capacitance*	$C_{PD}$								pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

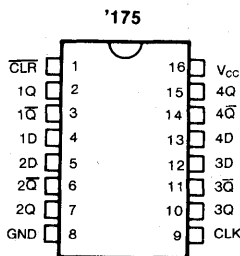
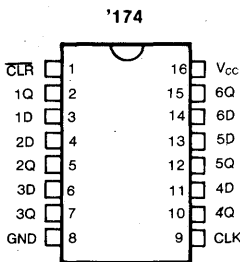
The '174 contains six, and the '175 contains four D-type flip-flops all sharing a common clock and a common clear. The '174 features single rail outputs for every flip-flops whereas the '175 has complementary outputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATIONS**



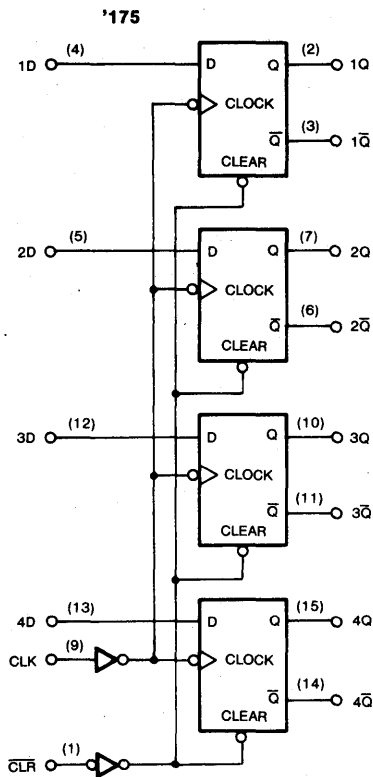
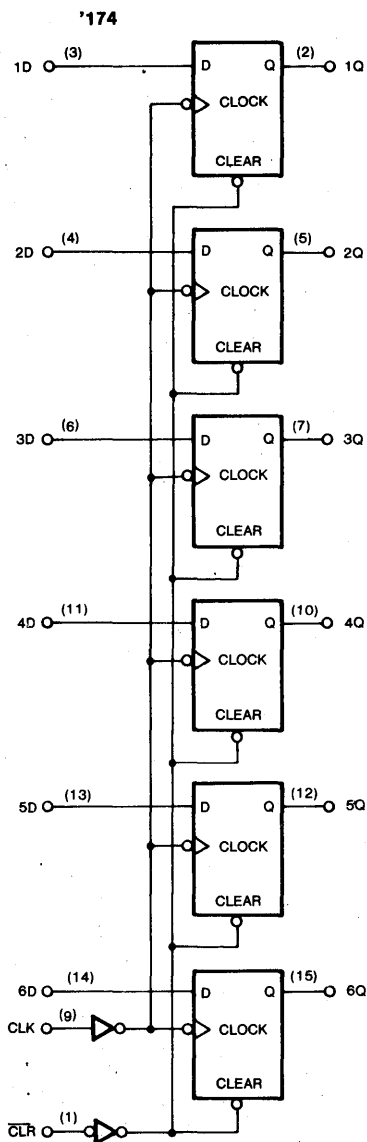
**FUNCTION TABLE**

(Each Flip-Flop)

Inputs			Outputs	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}^\dagger$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	$\text{Q}_0$	$\overline{\text{Q}}_0$

† '175 only

LOGIC DIAGRAMS



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
(-0.5V <  $V_O$  <  $V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS174, HCTLS175

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25		20		MHz
Maximum Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$		22	30	37		45		ns
	$t_{PHL}$		22	30	37		35		
Maximum Propagation Delay, CLR to Q or $\bar{Q}$	$t_{PLH}$		26	35	43		52		
	$t_{PHL}$	26	35	43		52			
Minimum Setup Time before CLK†	Data	$t_{su}$	10	13	17		20		ns
	$\bar{CLR}$ Inactive		12	16	20		25		
Minimum Hold Time, Data after CLK†		$t_h$	0	0	0		0		ns
Minimum Pulse Width	CLK High or Low	$t_w$	10	13	17		20		ns
	$\bar{CLR}$ Low		10	13	17		20		
Maximum Input Capacitance		$C_{IN}$	5						pF
Power Dissipation Capacitance*		$C_{PD}$							pF

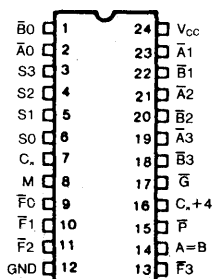
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus 12 other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus 10 other logic operations
- Full look-ahead for high-speed operations on long words
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current Outputs:
  - $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  - KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$
  - KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The '181 is an Arithmetic Logic Unit (ALU)/Function Generator that performs 16 binary arithmetic operations on two 4-bit words as shown in table 1 and 2. These operations are selected by the four functions select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of 2 cascade-outputs ( $\bar{P}$  and  $\bar{G}$ ) for the 4-bits in the package. When used in conjunction with HCTLS182, high-speed arithmetic operation can be performed. The typical addition times shown in table below illustrates how little is required for addition of longer words when full carry look-ahead is employed.

If high speed is not important, a ripple-carry input ( $C_n$ ) and a ripple-carry output ( $C_n+4$ ) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small lengths can be performed without external circuitry.

The '181 will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The '181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of the equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with  $C_n=H$  when performing the comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ( $C_n+4$ ) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L,H,H,L respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two boolean variables without the use of external circuitry. These logical functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, OR and NOR functions.

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table 1)	$\bar{A}_0$	$\bar{B}_0$	$\bar{A}_1$	$\bar{B}_1$	$\bar{A}_2$	$\bar{B}_2$	$\bar{A}_3$	$\bar{B}_3$	$\bar{F}_0$	$\bar{F}_1$	$\bar{F}_2$	$\bar{F}_3$	$C_n$	$C_n+4$	$\bar{P}$	$\bar{G}$
Active-High Data (Table 2)	A <sub>0</sub>	B <sub>0</sub>	A <sub>1</sub>	B <sub>1</sub>	A <sub>2</sub>	B <sub>2</sub>	A <sub>3</sub>	B <sub>3</sub>	F <sub>0</sub>	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	$\bar{C}_n$	$\bar{C}_n+4$	X	Y

**ALU SIGNAL DESIGNATION**

The '181 can be used with the signal designations.

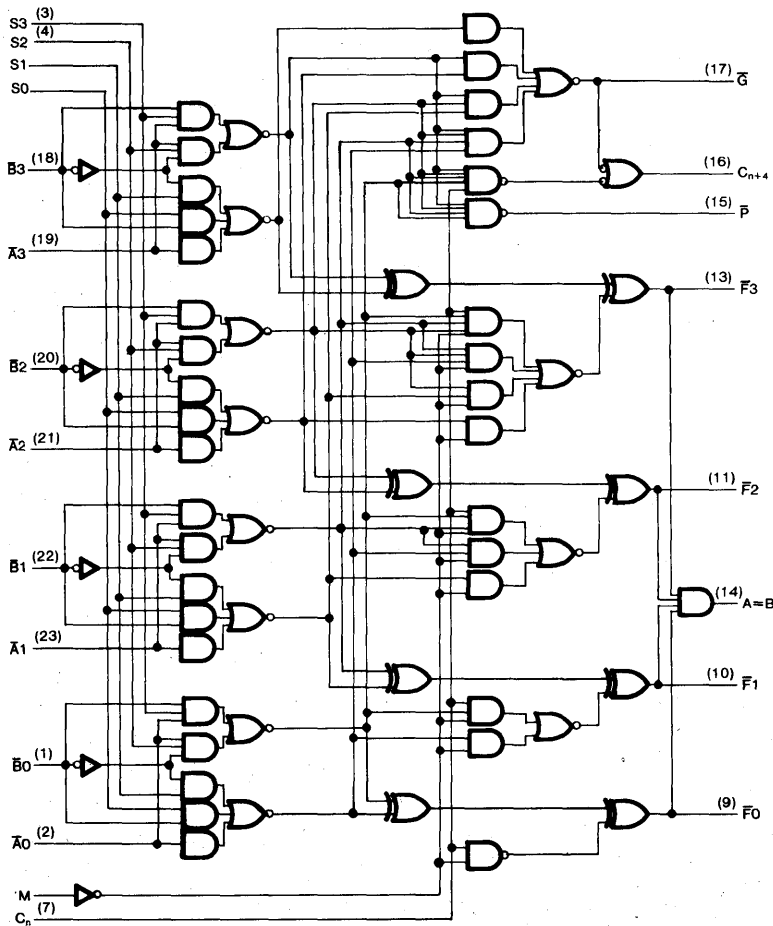
The logic functions and arithmetic operations obtained with signal designations as in Table 1.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels

allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**LOGIC DIAGRAM**



○ Table 1

Selection				Active-Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C <sub>n</sub> =L (no carry)	C <sub>n</sub> =H (with carry)
L	L	L	L	$F=\bar{A}$	F=A Minus 1	F=A
L	L	L	H	$F=\bar{A}\bar{B}$	F=AB Minus 1	F=AB
L	L	H	L	$F=\bar{A} + B$	F= $\bar{A}\bar{B}$ Minus 1	F= $\bar{A}\bar{B}$
L	L	H	H	F=1	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	$F=\bar{A} + \bar{B}$	F=A Plus (A + $\bar{B}$ )	F=A Plus (A + $\bar{B}$ ) Plus 1
L	H	L	H	$F=\bar{B}$	F=AB Plus (A + $\bar{B}$ )	F=AB Plus (A + $\bar{B}$ ) Plus 1
L	H	H	L	$F=\bar{A} \oplus \bar{B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	$F=A + \bar{B}$	F=A + $\bar{B}$	F=(A + $\bar{B}$ ) Plus 1
H	L	L	L	$F=\bar{A}B$	F=A Plus (A + B)	F=A Plus (A + B) Plus 1
H	L	L	H	$F=A \oplus B$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F= $\bar{A}\bar{B}$ Plus (A + B)	F= $\bar{A}\bar{B}$ Plus (A + B) Plus 1
H	L	H	H	F=A + B	F=(A + B)	F=(A + B) Plus 1
H	H	L	L	F=0	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	$F=A\bar{B}$	F=AB Plus A	F=AB Plus A Plus 1
H	H	H	L	F=AB	F= $\bar{A}\bar{B}$ Plus A	F= $\bar{A}\bar{B}$ Plus A Plus 1
H	H	H	H	F=A	F=A	F=A Plus 1

○ Table 2

Selection				Active-High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C <sub>n</sub> =L (no carry)	C <sub>n</sub> =H (with carry)
L	L	L	L	$F=\bar{A}$	F=A	F=A Plus 1
L	L	L	H	$F=\bar{A} + \bar{B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	$F=\bar{A}B$	F=A + $\bar{B}$	F=(A + $\bar{B}$ ) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Comp)	F=Zero
L	H	L	L	$F=\bar{A}\bar{B}$	F=A Plus AB	F=A Plus $\bar{A}\bar{B}$ Plus 1
L	H	L	H	$F=\bar{B}$	F=(A + B) Plus $\bar{A}\bar{B}$	F=(A + B) Plus $\bar{A}\bar{B}$ Plus 1
L	H	H	L	$F=\bar{A} \oplus \bar{B}$	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	$F=A\bar{B}$	F= $\bar{A}\bar{B}$ Minus 1	F= $\bar{A}\bar{B}$
H	L	L	L	$F=\bar{A} + B$	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	$F=\bar{A} \oplus B$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\bar{B}$ ) Plus AB	F=(A + $\bar{B}$ ) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	$F=A + \bar{B}$	F=(A + B) Plus A	A=(A + B) Plus A Plus 1
H	H	H	L	F=A + B	F=(A + B) Plus A	F=(A + B) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

\* Each bit is shifted to the next more significant position



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**INPUT PAIRS HIGH/NOT HIGH TEST TABLE**  
 FUNCTION INPUTS:  $S_2 = M = 4.5 \text{ V}$ ,  $S_0 = S_1 = S_3 = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ , $C_n$	Remaining $\bar{B}$	$\bar{P}$	In-Phase
$t_{PHL}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ , $C_n$	Remaining $\bar{B}$	$\bar{P}$	In-Phase
$t_{PLH}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{B}$ , $C_n$	Remaining $\bar{A}$	$\bar{P}$	In-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{B}$ , $C_n$	Remaining $\bar{A}$	$\bar{P}$	In-Phase
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ , $C_n$	Remaining $\bar{B}$	$C_n + 4$	Out-of-Phase
$t_{PHL}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ , $C_n$	Remaining $\bar{B}$	$C_n + 4$	Out-of-Phase
$t_{PLH}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{B}$ , $C_n$	Remaining $\bar{A}$	$C_n + 4$	Out-of-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{B}$ , $C_n$	Remaining $\bar{A}$	$C_n + 4$	Out-of-Phase

**PARAMETER MEASUREMENT INFORMATION**

**$\bar{SUM}$  MODE TEST TABLE**  
 FUNCTION INPUTS:  $S_0 = S_3 = 4.5 \text{ V}$ ,  $S_1 = S_2 = M = 0 \text{ V}$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	$C_n$	$\bar{F}_i$	In-Phase
$t_{PHL}$	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	$C_n$	$\bar{F}_i$	In-Phase
$t_{PLH}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	$C_n$	$\bar{F}_i$	In-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	$C_n$	$\bar{F}_i$	In-Phase
$t_{PLH}$	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , $C_n$	$\bar{P}$	In-Phase
$t_{PHL}$	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , $C_n$	$\bar{P}$	In-Phase
$t_{PLH}$	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , $C_n$	$\bar{P}$	In-Phase
$t_{PHL}$	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , $C_n$	$\bar{P}$	In-Phase
$t_{PLH}$	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$\bar{G}$	In-Phase
$t_{PHL}$	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$\bar{G}$	In-Phase
$t_{PLH}$	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$\bar{G}$	In-Phase
$t_{PHL}$	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$\bar{G}$	In-Phase
$t_{PLH}$	$C_n$	None	None	All $\bar{A}$	All $\bar{B}$	Any $\bar{F}$ or $C_n + 4$	In-Phase
$t_{PHL}$	$C_n$	None	None	All $\bar{A}$	All $\bar{B}$	Any $\bar{F}$ or $C_n + 4$	In-Phase
$t_{PLH}$	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$C_n + 4$	Out-of-Phase
$t_{PHL}$	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$C_n + 4$	Out-of-Phase
$t_{PLH}$	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$C_n + 4$	Out-of-Phase
$t_{PHL}$	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}$ , $C_n$	$C_n + 4$	Out-of-Phase

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS181

Characteristic	Symbol	Conditions†  $C_L = 50\text{pF}$	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Propagation Delay, $C_n$ to $C_n+4$	$t_{PLH}$	$M=0\text{V}$	14	18	23	27	ns
	$t_{PHL}$	Sum or Diff Mode	14	18	23	27	
Propagation Delay, $\bar{A}$ or $\bar{B}$ to $C_n+4$	$t_{PLH}$	$M=S1=S2=0\text{V}$	20	28	35	42	ns
	$t_{PHL}$	$S0=S3=4.5\text{V}$	20	28	35	42	
Propagation Delay, $\bar{A}$ or $\bar{B}$ to $C_n+4$	$t_{PLH}$	$M=S0=S3=0\text{V}$	25	34	42	50	ns
	$t_{PHL}$	$S1=S2=4.5\text{V}$	25	34	42	50	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{G}$	$t_{PLH}$	$M=S1=S2=0\text{V}$	22	31	39	47	ns
	$t_{PHL}$	$S0=S3=4.5\text{V}$	22	31	39	47	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{G}$	$t_{PLH}$	$M=S0=S3=0\text{V}$	23	32	40	48	ns
	$t_{PHL}$	$S1=S2=4.5\text{V}$	23	32	40	48	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{P}$	$t_{PLH}$	$M=S0=S3=0\text{V}$	25	34	43	51	ns
	$t_{PHL}$	$S1=S2=4.5\text{V}$	25	34	43	51	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $\bar{P}$	$t_{PLH}$	$M=S1=S2=0\text{V}$	25	34	42	50	ns
	$t_{PHL}$	$S0=S3=4.5\text{V}$	25	34	42	50	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $F_i$	$t_{PLH}$	$M=S1=S2=0\text{V}$	25	34	42	50	ns
	$t_{PHL}$	$S0=S3=4.5\text{V}$	25	34	42	50	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $F_i$	$t_{PLH}$	$M=S0=S3=0\text{V}$	25	34	42	50	ns
	$t_{PHL}$	$S1=S2=4.5\text{V}$	25	34	42	50	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $A=B$	$t_{PLH}$	$M=4.5\text{V}$	20	29	35	42	ns
	$t_{PHL}$		20	28	35	42	
Propagation Delay $\bar{A}$ or $\bar{B}$ to $A=B$	$t_{PLH}$	$M=S0=S3=0\text{V}$	25	34	42	50	ns
	$t_{PHL}$	$S1=S2=4.5\text{V}$	25	34	42	50	
Propagation Delay $C_n$ to any $\bar{F}$	$t_{PLH}$		20	28	35	42	ns
	$t_{PHL}$		20	28	35	42	
Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**PARAMETER MEASUREMENT INFORMATION**

**LOGIC MODE TEST TABLE**  
**FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V**

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	$\bar{F}_i$	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	$\bar{F}_i$	Out-of-Phase
t <sub>PHL</sub>							

**INPUT BITS EQUAL/NOT EQUAL TEST TABLE**  
**FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V**

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	$\bar{P}$	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	In-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	Out-of-Phase
t <sub>PHL</sub>							
t <sub>PLH</sub>	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{A}$ and $\bar{B}$ , C <sub>n</sub>	None	C <sub>n</sub> +4	Out-of-Phase
t <sub>PHL</sub>							

**DIFF MODE TEST TABLE**  
FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$	In-Phase
t <sub>PHL</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$	In-Phase
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$	Out-of-Phase
t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$	Out-of-Phase
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{P}$	In-Phase
t <sub>PHL</sub>	$\bar{A}_i$	None	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{P}$	In-Phase
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{P}$	Out-of-Phase
t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{P}$	Out-of-Phase
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{G}$	In-Phase
t <sub>PHL</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{G}$	In-Phase
t <sub>PLH</sub>	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{G}$	Out-of-Phase
t <sub>PHL</sub>	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}, C_n$	$\bar{G}$	Out-of-Phase
t <sub>PLH</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	A=B	In-Phase
t <sub>PHL</sub>	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	A=B	In-Phase
t <sub>PLH</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	A=B	Out-of-Phase
t <sub>PHL</sub>	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	A=B	Out-of-Phase
t <sub>PLH</sub>	C <sub>n</sub>	None	None	All $\bar{A}$ and $\bar{B}$	None	C <sub>n</sub> +4 or any F	In-Phase
t <sub>PHL</sub>	C <sub>n</sub>	None	None	All $\bar{A}$ and $\bar{B}$	None	C <sub>n</sub> +4 or any F	In-Phase
t <sub>PLH</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	C <sub>n</sub> +4	Out-of-Phase
t <sub>PHL</sub>	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	C <sub>n</sub> +4	Out-of-Phase
t <sub>PLH</sub>	$\bar{B}_i$	None	$\bar{a}_i$	None	Remaining $\bar{A}, \bar{B}, C_n$	C <sub>n</sub> +4	In-Phase
t <sub>PHL</sub>	$\bar{B}_i$	None	$\bar{a}_i$	None	Remaining $\bar{A}, \bar{B}, C_n$	C <sub>n</sub> +4	In-Phase

**FEATURES**

- Compatible Carry Functions for direct ALU connection
- Cascadable to perform look-ahead across n-bit adders.
- High output current drive:  $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Low power consumption characteristic of CMOS
- Direct interface capability to TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 182 are:

$$C_{n+x} = G_0 + P_0 C_n$$

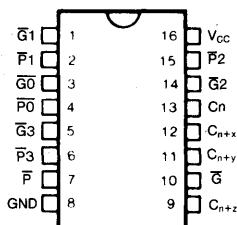
$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$\bar{G} = \bar{G}_3 + P_3 \bar{G}_2 + P_2 \bar{G}_1 + P_3 P_2 \bar{P}_1 \bar{G}_0$$

$$\bar{P} = P_3 P_2 P_1 P_0$$

**PIN CONFIGURATION**



**PIN DESIGNATIONS**

Designation	Pin No	Function
$\bar{G}_0, \bar{G}_1, \bar{G}_2, \bar{G}_3$	3, 1, 14, 5	Active Low Carry Generate Inputs
$\bar{P}_0, \bar{P}_1, \bar{P}_2, \bar{P}_3$	4, 2, 15, 6	Active Low Carry Propagate Inputs
$C_n$	13	Carry Input, Active High
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Carry Outputs
$\bar{G}$	10	Active Low Carry Generate Output
$\bar{P}$	7	Active Low Carry Propagate Output
$V_{cc}$	16	Supply Voltage
GND	8	Ground

FUNCTION TABLES

FOR  $\bar{G}$  OUTPUT

INPUTS							OUTPUT $\bar{G}$
$\bar{G}_3$	$\bar{G}_2$	$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_3$	$\bar{P}_2$	$\bar{P}_1$	
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR  $\bar{P}$  OUTPUT

INPUTS				OUTPUT $\bar{P}$
$\bar{P}_3$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	
L	L	L	L	L
All other combinations				H

FOR  $C_{n+x}$  OUTPUT

INPUTS			OUTPUT $C_{n+x}$
$\bar{G}_0$	$\bar{P}_0$	$C_n$	
L	X	X	H
X	L	H	H
All other combinations			L

$C_{n+y}$  OUTPUT

INPUTS					OUTPUT $C_{n+y}$
$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_1$	$\bar{P}_0$	$C_n$	
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

$C_{n+z}$  OUTPUT

INPUTS							OUTPUT $C_{n+z}$
$\bar{G}_2$	$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	$C_n$	
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = don't care  
Any inputs not shown in a given table are don't care with respect to that output.

LOGIC DIAGRAM

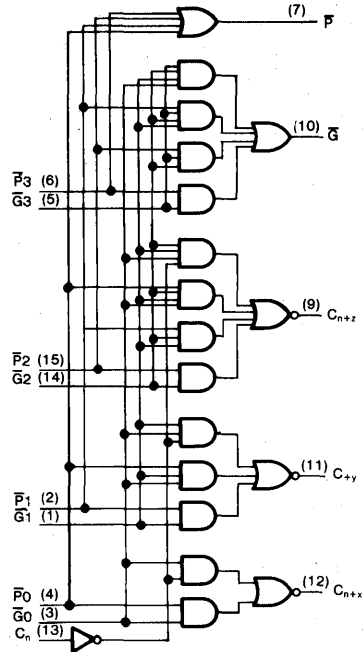
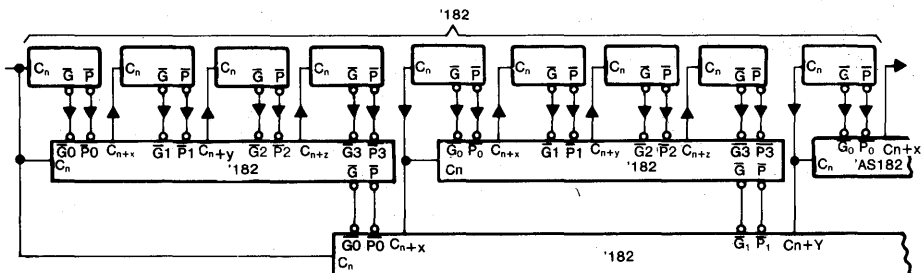


Figure: THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



#### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

#### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS182

Characteristic	Symbol	Conditions <sup>1</sup>	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Propagation Delay $\overline{P_i}$ or $\overline{G_i}$ to C <sub>n+x</sub> , C <sub>n+y</sub> , C <sub>n+z</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	19	26	32	39	ns
	t <sub>PHL</sub>		19	26	32	39	
Propagation Delay $P_i$ or $G_i$ to $\overline{G}$	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	19	26	32	39	ns
	t <sub>PHL</sub>		19	26	32	39	
Propagation Delay C <sub>n</sub> to C <sub>n+x</sub> , C <sub>n+y</sub> , C <sub>n+z</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	25	27	34	41	ns
	t <sub>PHL</sub>		25	27	34	41	
Propagation Delay $\overline{P_i}$ to $\overline{P}$	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15	20	25	30	ns
	t <sub>PHL</sub>		15	20	25	30	
Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: PD = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

<sup>1</sup>For Acc switching test circuits and timing waveforms see section 2.

**FEATURES**

- For use in high-speed wallace-tree summing
- Fast addition operation
- Low power consumption characteristic of CMOS
- High output current drive:  $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

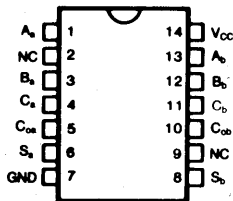
**DESCRIPTION**

The '183 is a dual full adder features an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than 2 gate delays.

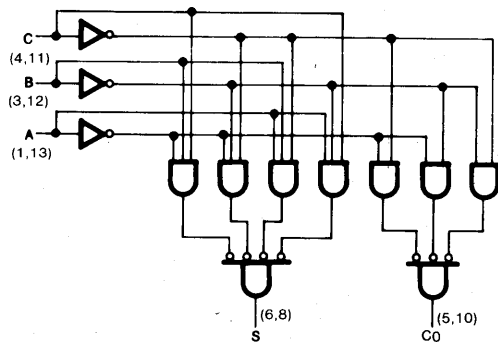
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**5**

**FUNCTION TABLE**

(Each Half)

Inputs			Output	
A	B	C	S	Co
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
L	L	H	H	L
H	H	L	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation

of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.  
 † Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS 183

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$			Unit
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	
Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	15	22	27	ns
	$t_{PHL}$		17	23	29	
Input Capacitance	$C_{IN}$				pF	
Power dissipation Capacitance*	$C_{PD}$				pF	

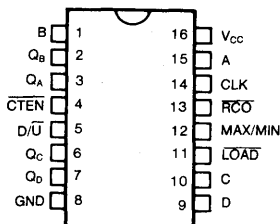
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	LOAD	D/ $\bar{U}$	$\bar{C}TEN$	CLK	Input	$R\bar{C}O$	$O_n$
parallel load	L	X	X	X	L	L	L
	L	X	X	X	X	H	H
count up	H	L	I	↑	X		count up
count down	H	H	I	↑	X		count down
hold (do nothing)	H	X	H	X	X		no change

$R\bar{C}O$  AND MAX/MIN FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
D/ $\bar{U}$	$\bar{C}TEN$	CLK	$Q_A$	$Q_b$	$Q_c$	$Q_d$	MAX/MIN	$R\bar{C}O$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⌊	H	X	X	H	⌊	⌊
L	L	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌊	L	L	L	L	⌊	⌊

- H = HIGH voltage level  
 L = LOW voltage level  
 I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition  
 X = Don't care  
 ↑ = LOW-to-HIGH CLK transition  
 ⌊ = one LOW level pulse  
 ⌋ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

## DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ( $\bar{C}TEN$ ) is low. A high at  $\bar{C}TEN$  inhibits counting. The direction of the count is determined by the level of the down/up (D/ $\bar{U}$ ) input. When D/ $\bar{U}$  is low, the counter counts up and when D/ $\bar{U}$  is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ( $\bar{C}TEN$  and D/ $\bar{U}$ ) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

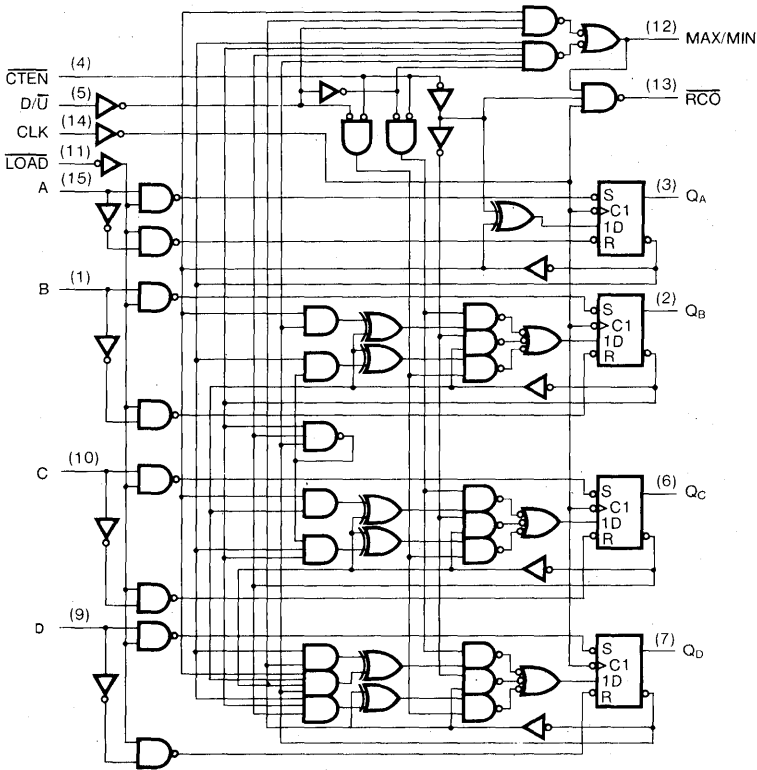
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

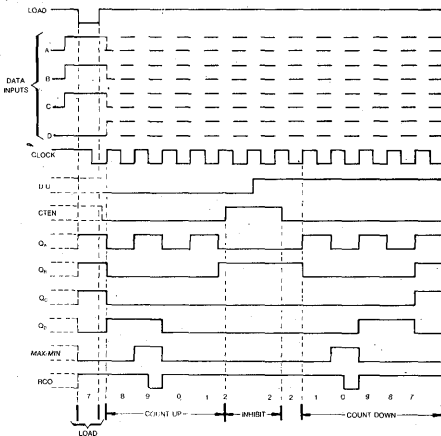
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence:

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, nine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, eight, and seven

**NOTE A:** Clear overrides load data, and count inputs.

**Note B:** When count up, count-down input must be high; when counting down, countup input must be high.

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS190

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ		Guaranteed Limits		
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	30	20	16	14	MHz
Maximum Propagation Delay, LOAD to any Q	t <sub>PLH</sub>		30	40	50	60	ns
	t <sub>PHL</sub>		30	40	50	60	
Maximum Propagation Delay, A,B,C, D to any Q	t <sub>PLH</sub>		27	36	45	64	ns
	t <sub>PHL</sub>		27	36	45	54	
Maximum Propagation Delay, CLK to $\overline{RCO}$	t <sub>PLH</sub>		17	22	28	33	ns
	t <sub>PHL</sub>		17	22	28	33	
Maximum Propagation Delay, CLK to any Q	t <sub>PLH</sub>		23	30	37	45	ns
	t <sub>PHL</sub>		23	30	37	45	
Maximum Propagation Delay, CLK to MAX/MIN	t <sub>PLH</sub>		35	47	59	70	ns
	t <sub>PHL</sub>		35	47	59	70	
Maximum Propagation Delay, D/ $\overline{U}$ to $\overline{RCO}$	t <sub>PLH</sub>		33	45	56	67	ns
	t <sub>PHL</sub>		33	45	56	67	
Maximum Propagation Delay, D/ $\overline{U}$ to MAX/MIN	t <sub>PLH</sub>		25	33	41	50	
	t <sub>PHL</sub>		25	33	41	50	
Maximum Propagation Delay, $\overline{CTEN}$ to $\overline{RCO}$	t <sub>PLH</sub>		25	33	41	50	ns
	t <sub>PHL</sub>		25	33	41	50	
Minimum Pulse Width	CLK High or Low		t <sub>w</sub>	13	17	21	25
	LOAD Low	13		17	21	25	
Minimum Setup Time	Data before $\overline{LOAD}\dagger$	t <sub>su</sub>	10	13	17	20	ns
	$\overline{CTEN}$ before CLK†		20	26	34	40	
	D/ $\overline{U}$ before CLK†		10	13	17	20	
	LOAD Inactive before CLK†		15	20	25	30	
Minimum Hold Time	Data after $\overline{LOAD}\dagger$	t <sub>h</sub>	1	3	5	5	ns
	$\overline{CTEN}$ after CLK†		0	0	0	0	
	D/ $\overline{U}$ after CLK†		0	0	0	0	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>		80				pF

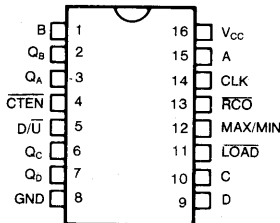
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
I<sub>OL</sub> = 8 mA @ V<sub>OL</sub> = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	LOAD	D/U	CTEN	CLK	Input	O <sub>n</sub>	
parallel load	L	X	X	X	L	L	H
count up	H	L	I	↑	X		count up
count down	H	H	I	↑	X		count down
hold (do nothing)	H	X	H	X	X		no change

RCO AND MAX/MIN FUNCTION TABLE

INPUTS		TERMINAL COUNT STATE					OUTPUTS	
D/U	CTEN	CLK	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	MAX/MIN	RCO
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	↓	H	X	X	H	L	↓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	↓	L	L	L	L	L	↓

- H = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one setup time prior to the LOW-to-HIGH CLK transition
- X = Don't care
- ↑ = LOW-to-HIGH CLK transition
- ↓ = one LOW level pulse
- ⌊ = MAX/MIN goes LOW ON A LOW-to-HIGH CLK transition

## DESCRIPTION

These are high-speed synchronous, reversible 4-bit binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with a synchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input (CTEN) is low. A high at CTEN inhibits counting. The direction of the count is determined by the level of the down/up (D/U) input. When D/U is low, the counter counts up and when D/U is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (CTEN and D/U) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

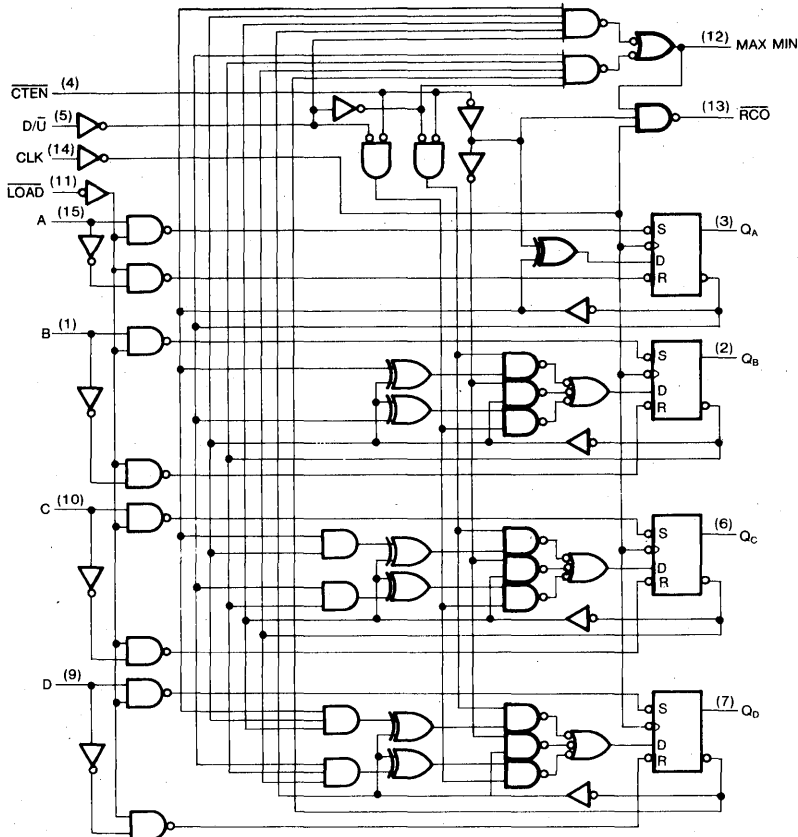
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

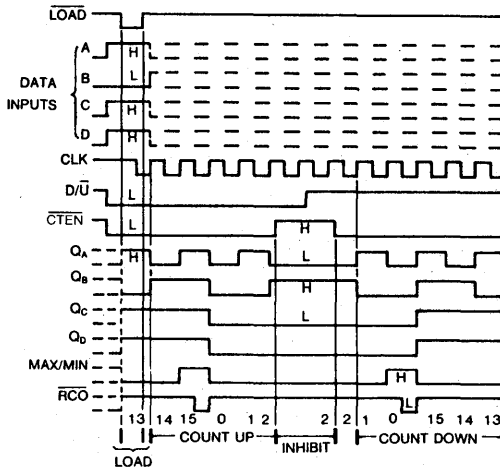
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>cc</sub> and ground.



LOGIC DIAGRAM



Typical Load, Count, and Inhibit Sequence



- Sequence:
- (1) Load (preset) to binary thirteen
  - (2) Count up to fourteen, fifteen, zero, one, and two
  - (3) Inhibit
  - (4) Count down to one, zero, fifteen, fourteen, and thirteen

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-4mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS191

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Typ		Guaranteed Limits				
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	30	20	16		14		MHz
Maximum Propagation Delay, LOAD to any Q	t <sub>PLH</sub>		30	40	50		60		ns
	t <sub>PHL</sub>		30	40	50		60		
Maximum Propagation Delay, A,B,C, D to any Q	t <sub>PLH</sub>		27	36	45		64		ns
	t <sub>PHL</sub>		27	36	45		54		
Maximum Propagation Delay, CLK to $\overline{RCO}$	T <sub>PLH</sub>		17	22	28		33		ns
	t <sub>PHL</sub>		17	22	28		33		
Maximum Propagation Delay, CLK to any Q	t <sub>PLH</sub>		23	30	37		45		ns
	t <sub>PHL</sub>		23	30	37		45		
Maximum Propagation Delay, CLK to MAX/MIN	t <sub>PLH</sub>		35	47	59		70		ns
	t <sub>PHL</sub>		35	47	59		70		
Maximum Propagation Delay, D/ $\overline{U}$ to $\overline{RCO}$	t <sub>PLH</sub>		33	45	56		67		ns
	t <sub>PHL</sub>		33	45	56		67		
Maximum Propagation Delay, D/ $\overline{U}$ to MAX/MIN	t <sub>PLH</sub>		25	33	41		50		
	t <sub>PHL</sub>	25	33	41		50			
Maximum Propagation Delay, $\overline{CTEN}$ to $\overline{RCO}$	t <sub>PLH</sub>	25	33	41		50		ns	
	t <sub>PHL</sub>	25	33	41		50			
Minimum Pulse Width	CLK High or Low	t <sub>w</sub>	13	17	21		25		ns
	$\overline{LOAD}$ Low		13	17	21		25		
Minimum Setup Time	Data before $\overline{LOAD}\uparrow$	t <sub>su</sub>	10	13	17		20		ns
	$\overline{CTEN}$ before CLK $\uparrow$		20	26	34		40		
	D/ $\overline{U}$ before CLK $\uparrow$		10	13	17		20		
	$\overline{LOAD}$ Inactive before CLK $\uparrow$		15	20	25		30		
Minimum Hold Time	Data after $\overline{LOAD}\uparrow$	t <sub>h</sub>	1	3	5		5		ns
	$\overline{CTEN}$ after CLK $\uparrow$		0	0	0		0		
	D/ $\overline{U}$ after CLK $\uparrow$		0	0	0		0		
Maximum Input Capacitance	C <sub>IN</sub>		5					pF	
Power Dissipation Capacitance*	C <sub>PD</sub>		80					pF	

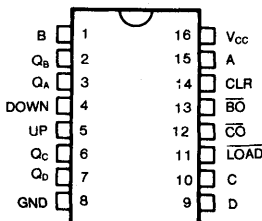
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Look-ahead circuit enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

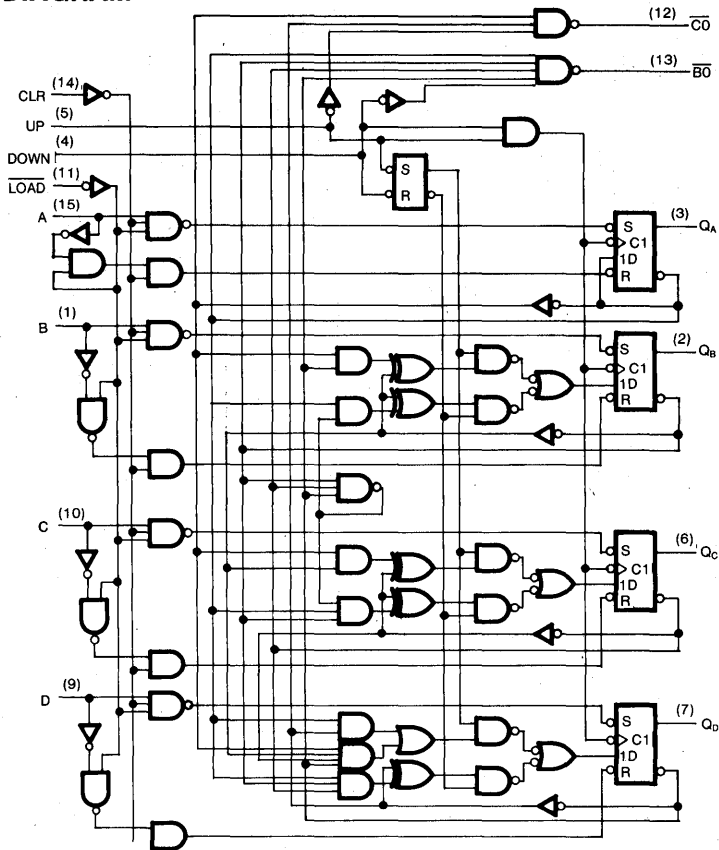
A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ( $\overline{BO}$ ) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ( $\overline{CO}$ ) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

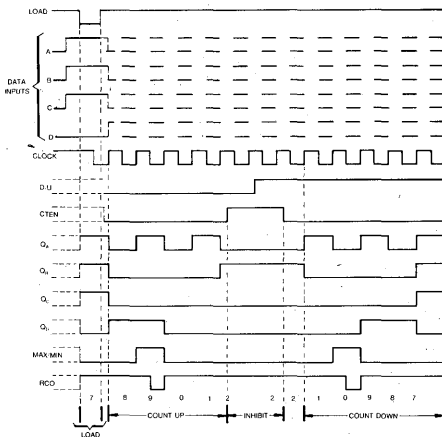
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence:

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, nine(maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, eight, and seven

NOTE A: Clear overrides load data, and count inputs.

Note B: When count up, count-down input must be high; when counting down, countup input must be high.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS192

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	35	25	20	18	MHz
Maximum Propagation Delay, UP to CO	$t_{PLH}$		18	25	31	37	ns
	$t_{PHL}$		18	25	31	37	
Maximum Propagation Delay, DOWN to BO	$t_{PLH}$		18	24	30	36	ns
	$t_{PHL}$		18	24	30	36	
Maximum Propagation Delay, UP or DOWN to any Q	$t_{PLH}$		32	42	52	63	ns
	$t_{PHL}$		32	42	52	63	
Maximum Propagation Delay, LOAD to any Q	$t_{PLH}$		30	40	50	60	ns
	$t_{PHL}$		30	40	50	60	
Maximum Propagation Delay, CLR to any Q	$t_{PHL}$		18	24	30	36	ns
Minimum Pulse Width	CLR High	$t_w$	10	13	17	20	ns
	LOAD Low		10	13	17	20	
	UP or DOWN High or Low		10	13	17	20	
Minimum Setup Width	Data before LOAD†	$t_{su}$	10	13	17	20	ns
	CLR Inactive before UP† or DOWN†		10	13	17	20	
	LOAD Inactive before UP† or DOWN†		10	13	17	20	
	UP high before DOWN†		10	13	17	20	
	DOWNhigh before UP†		10	13	17	20	
Minimum Hold Time	Data after LOAD†	$t_h$	1	3	5	5	ns
	UP High after DOWN†		0	0	0	0	
	DOWN High after UP†		0	0	0	0	
Maximum Input Capacitance	$C_{IN}$		5			pF	
Power Dissipation Capacitance*	$C_{PD}$		80			pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

These are high-speed synchronous reversible 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

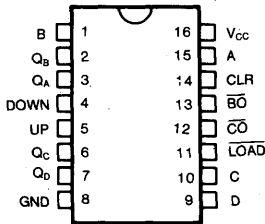
A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ( $\overline{BO}$ ) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ( $\overline{CO}$ ) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



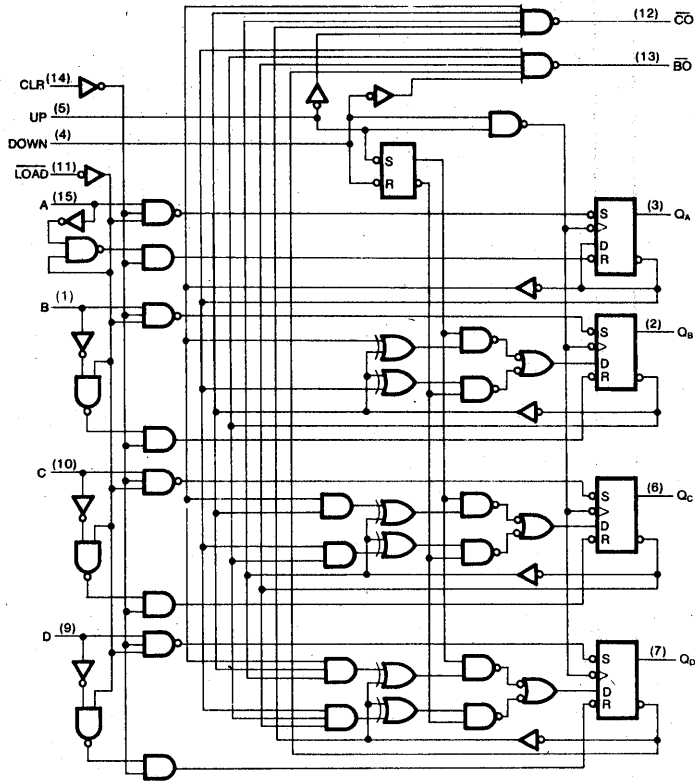
**FUNCTION TABLE**

OPERATING MODE	INPUTS								OUTPUTS					
	CLR	$\overline{LOAD}$	UP	DOWN	A	B	C	D	QA	QB	QC	QD	$\overline{CO}$	$\overline{BO}$
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X		count down				H	H**

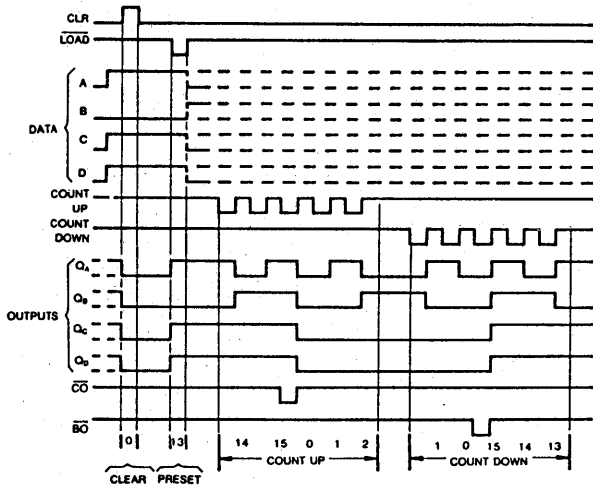
H= HIGH voltage level      ↑ = LOW-to-HIGH clock transition  
 L= LOW voltage level      \*  $\overline{CO}$  = UP at terminal count up (HHHH)  
 X= don't care                \*\*  $\overline{BO}$  = DOWN at terminal count down (LLLL)



LOGIC DIAGRAM



Typical Clear, Load, and Count Sequences



Sequences:  
 (1) Clear outputs to zero.  
 (2) Load (preset) to binary thirteen.  
 (3) Count up to fourteen, fifteen, carry, zero, one, and two.  
 (4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.  
 Note A: Clear overrides load data, and count inputs.  
 Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS193)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit	
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ				Guaranteed Limits	
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	35	25	20	18	MHz	
Maximum Propagation Delay, UP to CO	$t_{PLH}$		18	25	31	37	ns	
	$t_{PHL}$		18	25	31	37		
Maximum Propagation Delay, DOWN to BO	$t_{PLH}$		18	24	30	36	ns	
	$t_{PHL}$		18	24	30	36		
Maximum Propagation Delay, UP or DOWN to any Q	$T_{PLH}$		32	42	52	63	ns	
	$t_{PHL}$		32	42	52	63		
Maximum Propagation Delay, LOAD to any Q	$t_{PLH}$		30	40	50	60	ns	
	$t_{PHL}$		30	40	50	60		
Maximum Propagation Delay, CLR to any Q	$t_{PHL}$		18	24	30	36	ns	
Minimum Pulse Width	CLR High	$t_w$	10	13	17	20	ns	
	LOAD Low		10	13	17	20		
	UP or DOWN High or Low		10	13	17	20		
Minimum Setup Width	Data before LOAD†	$t_{su}$	10	13	17	20	ns	
	CLR Inactive before UP† or DOWN†		10	13	17	20		
	LOAD Inactive before UP† or DOWN†		10	13	17	20	ns	
	UP high before DOWN†		10	13	17	20		
	DOWN high before UP†		10	13	17	20		
Minimum Hold Time	Data after LOAD†	$t_h$	1	3	5	5	ns	
	UP High after DOWN†		0	0	0	0		
	DOWN High after UP†		0	0	0	0		
Maximum Input Capacitance	$C_{IN}$		5			pF		
Power Dissipation Capacitance*	$C_{PD}$		80			pF		

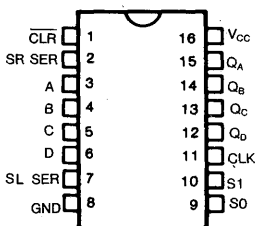
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data Latching Capability
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

CLR	MODE		INPUTS				OUTPUTS						
			CLK	SERIAL		PARALLEL		QA	QB	QC	QD		
	S1	S0		LEFT	RIGHT	A	B					C	D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

H=high level (steady state)  
 L=low level (steady state)  
 X=irrelevant (any input, including transitions)  
 ↑=transition from low to high level  
 a,b,c,d=the level of steady-state input at inputs, A,B,C, or D, respectively.  
 QA0, QB0, QC0, QD0=the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established.  
 QAn, QBn, QCn, QDn=the level of QA, QB, QC, respectively, before the most-recent ↑ transition of the clock.

**DESCRIPTION**

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Inhibit clock (temporary data latch/do nothing)
- Shift-right (in the direction QA toward QD)
- Shift-left (in the direction QD toward QA)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

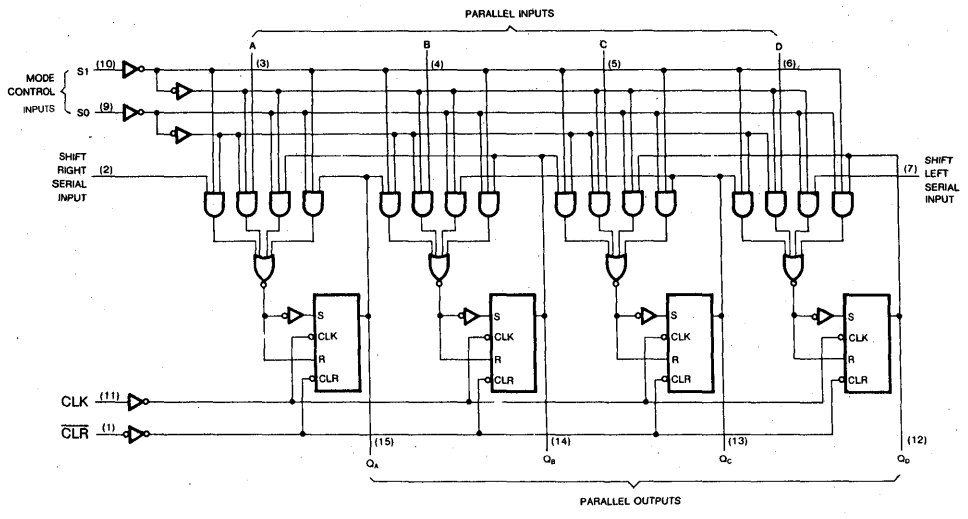
Shift-right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

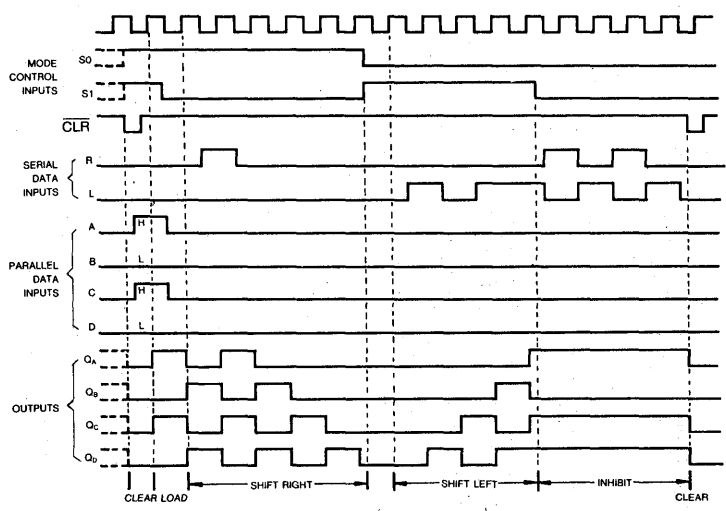
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to VCC and ground.

LOGIC DIAGRAM

(positive logic)



typical clear, load, right-shift, inhibit, and clear sequences



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS194

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ				
			Guaranteed Limits				
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25	20	MHz
Maximum Propagation Delay, CLK to $Q_H$	$t_{PLH}$		18	24	30	36	ns
	$t_{PHL}$		18	24	30	36	
Maximum Propagation Delay, CLR to $Q_H$	$t_{PHL}$		21	28	35	42	ns
Minimum Pulse Width	CLR to Low	$t_w$	12	16	20	24	ns
	CLK High or Low		12	16	20	24	
Minimum Setup Time, Any Input before CLK↑	$t_s$		10	17	20	20	ns
Minimum Hold Time, Data after CLK↑	$t_s$		0	0	0	0	ns
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

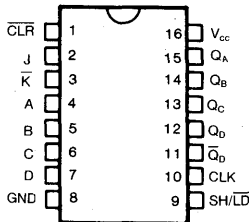
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- J and K Inputs to First Stage
- Right-shift Only with Complementary Outputs on Last Stage
- Direct Overriding Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

- Parallel (broadside) load
- Shift (in the direction  $A_A$  toward  $Q_D$ )

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associate flip-flops and appears at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

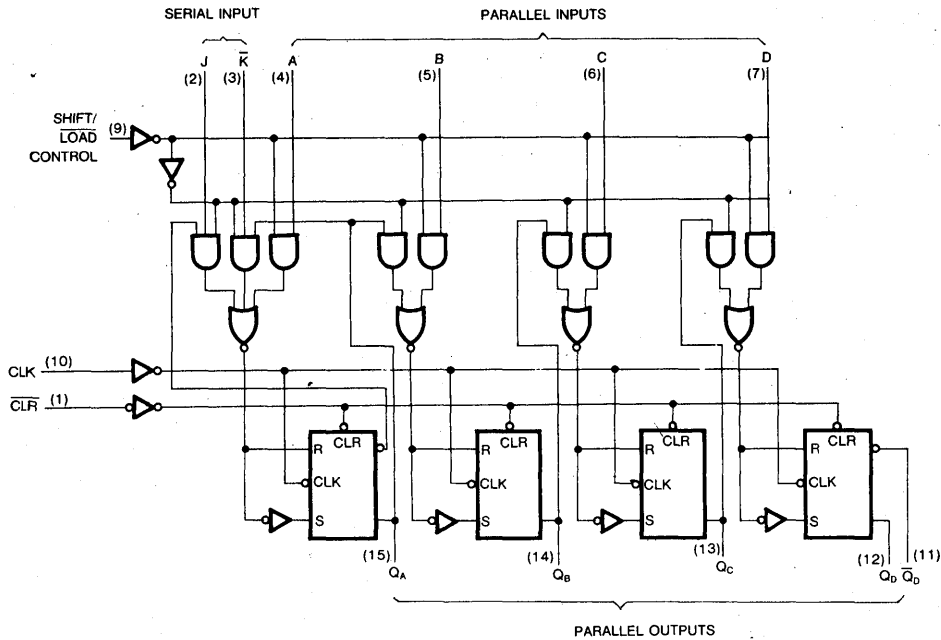
**FUNCTION TABLE**

INPUTS			OUTPUTS											
CLR	SHIFT/LOAD	CLK	SERIAL		PARALLEL		Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>D</sub> <sup>-</sup>			
			J	K	A	B						C	D	
L	X	X	X	X	X	X	X	L	L	L	L	H		
H	L	↑	X	X	a	b	c	d	a	b	c	d		
H	H	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>D0</sub> <sup>-</sup>	
H	H	↑	L	H	X	X	X	X	Q <sub>A0</sub>	Q <sub>A0</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Cn</sub> <sup>-</sup>	
H	H	↑	L	L	X	X	X	X	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Cn</sub> <sup>-</sup>	
H	H	↑	H	H	X	X	X	X	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Cn</sub> <sup>-</sup>	
H	H	↑	H	L	X	X	X	X	H	Q <sub>An</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Cn</sub> <sup>-</sup>

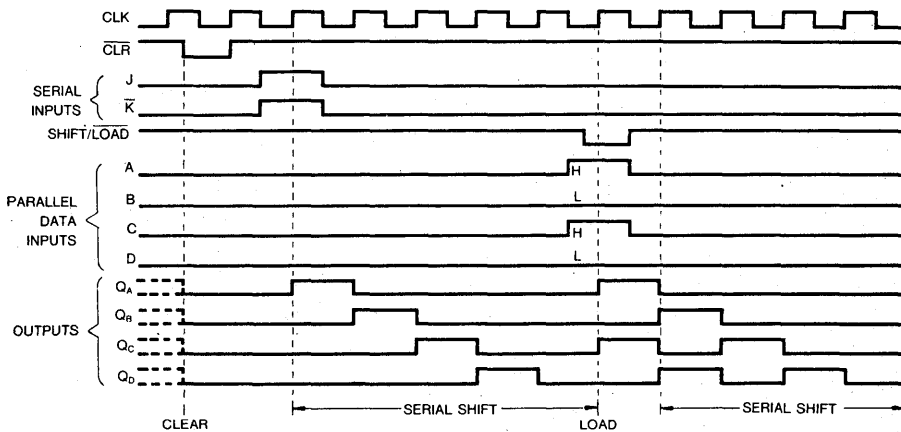
H=high level (steady state)  
 L=low level (steady state)  
 X=irrelevant (any input, including transitions)  
 ↑=transition from low to high level  
 a,b,c,d=the level of steady-state input at A,B,C, or D, respectively.  
 Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>C0</sub>, Q<sub>D0</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the indicated steady-state input conditions were established.  
 Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>=the level of Q<sub>A</sub>, Q<sub>B</sub> or Q<sub>C</sub>, respectively, before the mostrecent transition of the clock.



LOGIC DIAGRAM



typical clear, shift, and load sequences



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS195

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	50	30	25	20	MHz
Maximum Propagation Delay, CLK to Q <sub>H</sub>	t <sub>PLH</sub>		18	24	30	36	ns
	t <sub>PHL</sub>		18	24	30	36	ns
Maximum Propagation Delay, CLR to Q <sub>H</sub>	t <sub>PHL</sub>		21	28	35	42	ns
Maximum Pulse Width	CLR Low	t <sub>w</sub>	10	12	15	20	ns
	CLK High or Low		12	16	20	24	
Minimum Setup Time before CLK†	SH/LD High	t <sub>su</sub>	15	20	25	25	ns
	Serial or Parallel		12	15	20	24	
	CLR inactive		15	20	25	25	
Minimum Hold Time after CLK†	SH/LD High	t <sub>h</sub>	0	0		0	ns
	Serial or Parallel Data		0	0		0	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

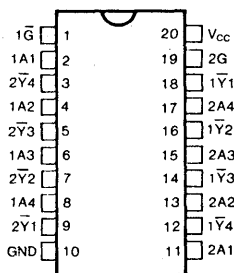
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 24\text{mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### FUNCTION TABLE

Input	Output
$\bar{G}$ A	Y
L L	H
L H	L
H X	Z

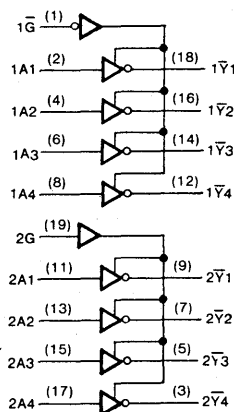
### DESCRIPTION

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS210

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit	
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		
			Typ	Guaranteed Limits				
Maximum Propagation Delay, A to Y	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	13	18	22	27	ns	
		C <sub>L</sub> = 150pF	16	21	27	33		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	13	18	22	27		
		C <sub>L</sub> = 150pF	16	21	27	33		
Maximum Output Enable Time, Enable to Y	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	17	23	29	34	ns
			C <sub>L</sub> = 150pF	20	26	34	40	
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	17	23	29	34		
Maximum Output Disable Time, Enable to Y̅	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	16	21	26	32	ns	
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	16	21	26	32		
Maximum Input Capacitance	C <sub>IN</sub>		5				pF	
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10				pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Output Disabled	5				pF	
		Output Enabled	30					

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used with high-speed memories utilizing a fast enable circuit. The delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

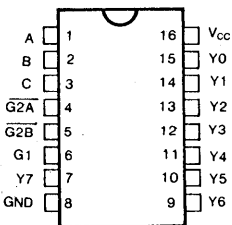
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding.

A 24-line decoder can be implemented without external inverters and a 31-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

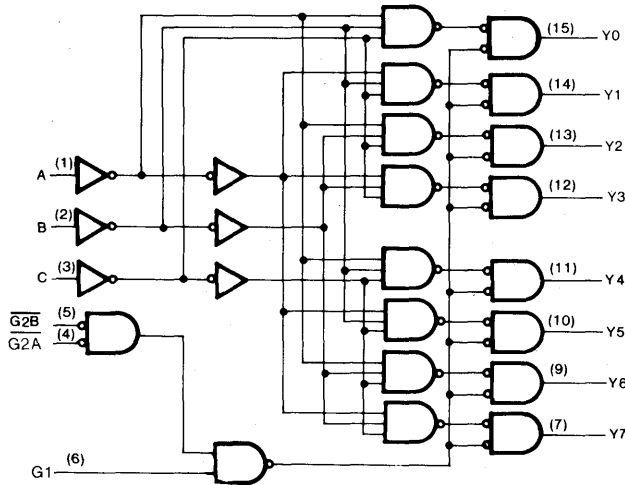


**FUNCTION TABLE**

Enable Inputs		Select Inputs			Outputs							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

\*G2 = G2A + G2B

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
					T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	
Minimum High-Level Input Voltage	V <sub>IH</sub>		2.0		2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>		0.8		0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-4mA	V <sub>CC</sub> 4.2	V <sub>CC</sub> - 0.1 3.98	V <sub>CC</sub> - 0.1 3.84	V <sub>CC</sub> - 0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND	±0.1		±1.0	±1.0	μA
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	8.0		80.0	160.0	μA
Additional Worst Case Supply Current	ΔI <sub>CC</sub>	per input pin V <sub>Z</sub> =2.4V Other Inputs: At V <sub>CC</sub> or GND I <sub>O</sub> =0	2.7		2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub> ≤ 6 ns, HCTLS238)

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C		KS74HCTLS	KS54HCTLS	Unit
			V <sub>CC</sub> = 5.0V		T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	
					V <sub>CC</sub> = 5.0V ± 10%		
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A, B, C or any Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF	22	30	37	45	ns
	t <sub>PHL</sub>		22	30	37	45	
Maximum Propagation Delay, G1 to any Y	t <sub>PLH</sub>		24	32	40	48	ns
	t <sub>PHL</sub>		24	32	40	48	
Maximum Propagation Delay, G2A or G2B to any Y	t <sub>PLH</sub>		18	25	31	37	ns
	t <sub>PHL</sub>		18	25	31	37	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>		50				pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 2 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

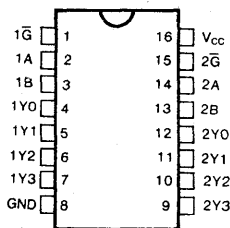
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory.

This means that the effective system delay introduced by the decoder is negligible.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

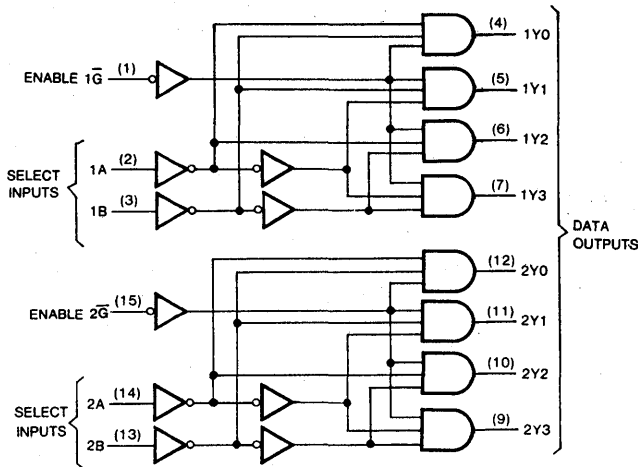
**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs			Outputs			
Enable	Select		Y0	Y1	Y2	Y3
$\bar{G}$	B	A				
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V\pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$	KS74HCTLS		KS54HCTLS		Unit
			Typ	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	Guaranteed Limits		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0		V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8		V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS239

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74HCTLS		KS54HCTLS		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Guaranteed Limits				
Maximum Propagation Delay, A or B any Y	$t_{PLH}$	$C_L = 50\text{pF}$	22	30	37	45	ns	
	$t_{PHL}$		22	30	37	45		
Maximum Propagation Delay, $\bar{G}$ to any Y	$t_{PLH}$		21	8	35	42	ns	
	$t_{PHL}$		22	8	35	42		
Maximum Input Capacitance	$C_{IN}$		5				pF	
Power Dissipation Capacitance*	$C_{PD}$		50				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 240/241/244 Octal Buffers and Line Drivers with 3-State Outputs

## KS74HCTLS

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

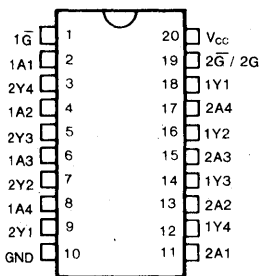
These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The designer has the choice of combinations of inverting/non-inverting outputs and symmetrical complementary input control (both active-low, or one active-low, the other active-high).

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

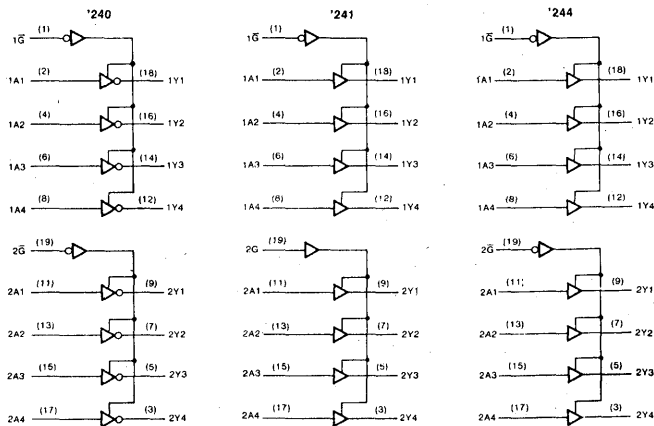
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



\*2G for '240 and '244  
2G for '241

### LOGIC DIAGRAMS



### FUNCTION TABLE

Input			'241, '244	'240
			Output	Output
G	$\bar{G}$	A	Y	Y
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z

# KS54HCTLS 240/241/244 Octal Buffers and Line Drivers with 3-State Outputs

## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$

# KS54HCTLS 240/241/244 Octal Buffers and Line Drivers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS240, HCTLS241, HCTLS244

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit		
			Typ		Guaranteed Limits						
Maximum Propagation Delay, A to Y	t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	13	18	22		27		ns		
			16	21	27		33				
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	13	18	22		27				
			16	21	27		33				
Maximum Output Enable Time, Enable to Y	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	17	23	29		34		ns		
			20	26	34		40				
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	17	23	29		34				
			20	26	34		40				
Maximum Output Disable Time, Enable to Y	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	16	21	26		32		ns		
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	16	21	26		32				
Maximum Input Capacitance	C <sub>IN</sub>		5						pF		
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10						pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Output Disabled	5						pF		
		Output Enabled	30								

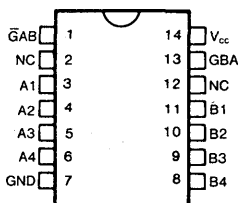
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f.

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- 2-Way Asynchronous Communication Between Data Buses
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## DESCRIPTION

These four-data line transceivers are designed for asynchronous two-way communications between data buses.

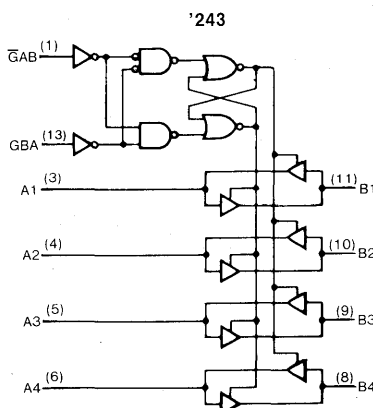
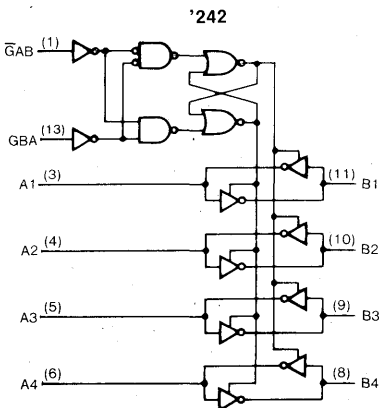
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## FUNCTION TABLE

INPUTS		'242	'243
$\bar{G}AB$	GBA		
L	L	$\bar{A}$ to B	A to B
H	H	B to A	B to A
H	L	Isolation	Isolation
L	H	Isolation	Isolation

## LOGIC DIAGRAMS





### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS242, HCTLS243

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit		
			Typ		Guaranteed Limits						
Maximum Propagation Delay, A to B or B to A	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	14	18	22		27		ns		
		C <sub>L</sub> = 150pF	17	21	27		33				
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	14	18	22		27				
		C <sub>L</sub> = 150pF	17	21	27		33				
Maximum Output Enable Time  GAB to B, GBA to A	t <sub>PZH</sub>	R <sub>L</sub> = 1 kΩ	C <sub>L</sub> = 50pF	23	30	38		45		ns	
			C <sub>L</sub> = 150pF	26	33	43		51			
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	23	30	38		45				
		C <sub>L</sub> = 150pF	26	33	43		51				
Maximum Output Disable Time, GAB to B, GBA to A	t <sub>PHZ</sub>	R <sub>L</sub> = 1 kΩ	18	25	31		37		ns		
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	18	25	31		37				
Maximum Input Capacitance	C <sub>IN</sub>		5					pF			
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10					pF			
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Output Disabled	5					pF			
		Output Enabled	30								

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-state outputs with high drive current ( $I_{OL} = 24mA @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$   
KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

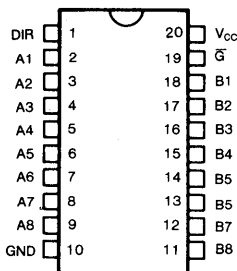
These high-speed octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ( $\bar{G}$ ) can be used to disable the device so that the buses are effectively isolated.

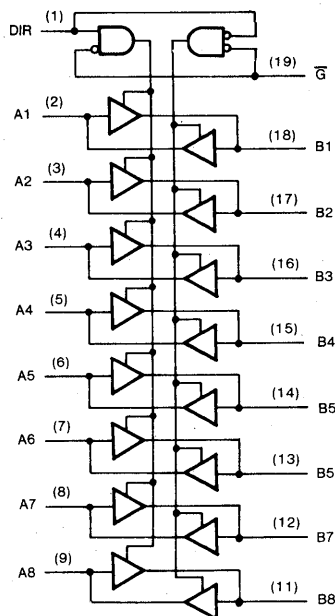
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION



## LOGIC DIAGRAM



## FUNCTION TABLE

Inputs		Operation
$\bar{G}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 70$ mA
Continuous Current Through	
$V_{CC}$ or GND pins	$\pm 250$ mA
Storage Temperature Range, $T_{stg}$	-65°C to +150°C
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	0V to $V_{CC}$
Operating Temperature	
Range	KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS245

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, A to B or B to A	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	9	12	15	18			ns
		C <sub>L</sub> = 150pF	12	15	20	34			
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	9	12	15	18			ns
		C <sub>L</sub> = 150pF	12	15	20	34			
Maximum Output Enable Time, $\bar{G}$ to A or B	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	30	40	50	60		ns
			C <sub>L</sub> = 150pF	33	43	55	66		
	t <sub>PZL</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	30	40	50	60		ns
			C <sub>L</sub> = 150pF	33	43	55	66		
Maximum Output Disable Time, $\bar{G}$ to A or B	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ		18	25	31	37		ns
			t <sub>PLZ</sub>		18	25	31	37	
Maximum Input Capacitance	C <sub>IN</sub>		5					pF	
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10					pF	
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	$\bar{G} = V_{CC}$ $\bar{G} = GND$	5					pF	

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Three-State Version of '151
- Three-State Outputs Interface Directly with System Bus
- Performs Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

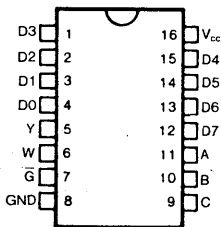
These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ( $\bar{G}$ ). The outputs are disabled when  $\bar{G}$  is high.

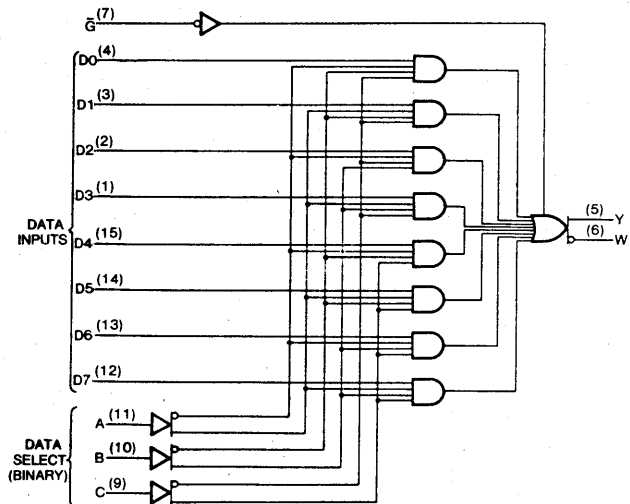
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### LOGIC DIAGRAM



### FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE $\bar{G}$	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\bar{D}0$
L	L	H	L	D1	$\bar{D}1$
L	H	L	L	D2	$\bar{D}2$
L	H	H	L	D3	$\bar{D}3$
H	L	L	L	D4	$\bar{D}4$
H	L	H	L	D5	$\bar{D}5$
H	H	L	L	D6	$\bar{D}6$
H	H	H	L	D7	$\bar{D}7$

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
Operating Temperature  
Range KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS251

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ		Guaranteed Limits					
Maximum Propagation Delay, A, B or C to Y	$t_{PLH}$	$C_L = 50\text{pF}$	20	26	33		40		ns	
		$C_L = 150\text{pF}$	23	29	38		46			
	$t_{PHL}$	$C_L = 50\text{pF}$	20	26	33		40			
		$C_L = 150\text{pF}$	23	29	38		46			
Maximum Propagation Delay, A, B or C to W	$t_{PLH}$	$C_L = 50\text{pF}$	25	34	42		50		ns	
		$C_L = 150\text{pF}$	28	37	47		56			
	$t_{PHL}$	$C_L = 50\text{pF}$	25	34	42		50			
		$C_L = 150\text{pF}$	28	37	47		56			
Maximum Propagation Delay, Any D to Y	$t_{PLH}$	$C_L = 50\text{pF}$	11	15	19		22		ns	
		$C_L = 150\text{pF}$	14	18	24		28			
	$t_{PHL}$	$C_L = 50\text{pF}$	11	15	19		22			
		$C_L = 150\text{pF}$	14	18	24		28			
Maximum Propagation Delay, Any D to W	$t_{PLH}$	$C_L = 50\text{pF}$	17	22	28		33		ns	
		$C_L = 150\text{pF}$	20	25	33		39			
	$t_{PHL}$	$C_L = 50\text{pF}$	17	22	28		33			
		$C_L = 150\text{pF}$	20	25	33		39			
Maximum Output Enable Time, G to Y or W	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40		48		ns
			$C_L = 150\text{pF}$	27	35	45		54		
	$t_{PZL}$	$C_L = 50\text{pF}$	24	32	40		48			
		$C_L = 150\text{pF}$	27	35	45		54			
Maximum Output Disable Time, G to Y or W	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40		48		ns
			$C_L = 150\text{pF}$	27	35	45		54		
	$t_{PLZ}$	$C_L = 50\text{pF}$	24	32	40		48			
		$C_L = 150\text{pF}$	27	35	45		54			
Maximum Input Capacitance	$C_{IN}$		5					pF		
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10					pF		
Power Dissipation Capacitance*	$C_{PD}$		0					pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



### FEATURES

- Three-State Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to—Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

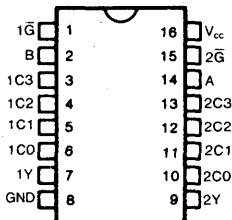
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ( $\bar{G}$ ). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

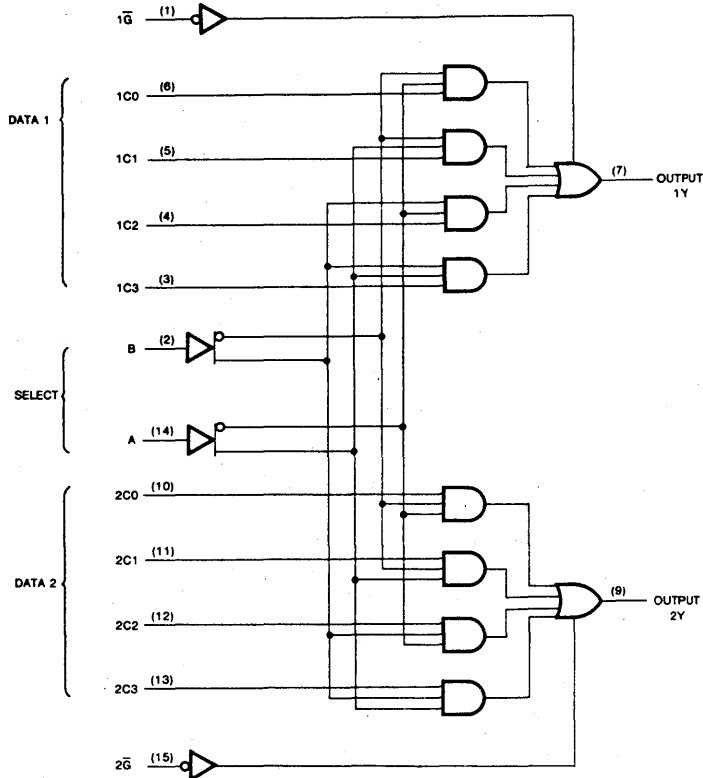


### FUNCTION TABLE

SELECT		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , .....	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
Continuous Output Current* Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....	$\pm 35$ mA
Continuous Current Through	
$V_{CC}$ or GND pins .....	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ .....	-65°C to +150°C
Power Dissipation Per Package, $P_d$ † .....	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage, $V_{CC}$ .....	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ ..	0V to $V_{CC}$
Operating Temperature	
Range	KS74HCTLS: -40°C to +85°C
	KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$ .....	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-6mA	V <sub>CC</sub> 4.2	V <sub>CC</sub> - 0.1 3.98	V <sub>CC</sub> - 0.1 3.84	V <sub>CC</sub> - 0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =12mA I <sub>O</sub> =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I <sub>oz</sub>	Output Enable = V <sub>IH</sub> V <sub>OUT</sub> =V <sub>CC</sub> or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI <sub>CC</sub>	per input pin V <sub>I</sub> =2.4V other inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub>, t<sub>f</sub>≤6 ns, HCTLS253)

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C		KS74HCTLS	KS54HCTLS	Unit
			V <sub>CC</sub> = 5.0V		T <sub>a</sub> = -40°C to +85°C	T <sub>a</sub> = -55°C to +125°C	
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A or B to Any Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24	32	40	48	ns
			27	35	45	54	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24	32	40	48	ns
			27	35	45	54	
Maximum Propagation Delay, Data (any C) to any Y	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15	20	25	30	ns
			18	23	30	36	
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15	20	25	30	ns
			18	23	30	36	
Maximum Output Enable Time, $\bar{G}$ to Y	t <sub>PZH</sub>	R <sub>L</sub> =1kΩ	C <sub>L</sub> =50pF	17	22	28	ns
			C <sub>L</sub> =150pF	20	25	33	
	t <sub>PZL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	17	22	28	33	ns
			20	25	33	39	
Maximum Output Disable Time, $\bar{G}$ to Y	t <sub>PHZ</sub>	R <sub>L</sub> =1kΩ	17	22	28	33	ns
			17	22	28	33	
	t <sub>PLZ</sub>	C <sub>L</sub> =50pF	17	22	28	33	ns
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

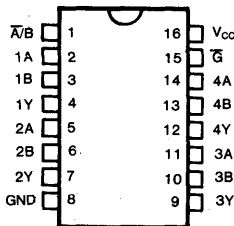
† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 257/258 Quad 2-Line to 1-Line Data Selectors/ KS74HCTLS Multiplexers with 3-State Outputs

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## DESCRIPTION

The '257 and '258 multiplex signals from four-bit data sources to four-output data lines in bus organized systems. The data presented at the outputs is non-inverted for the '257 and inverted for the '258.

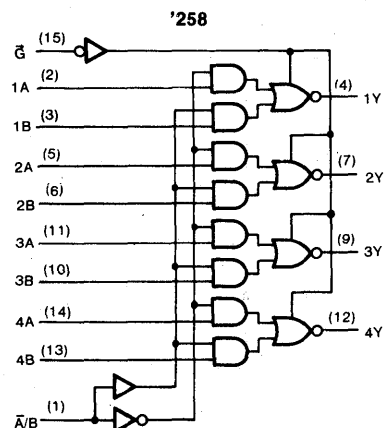
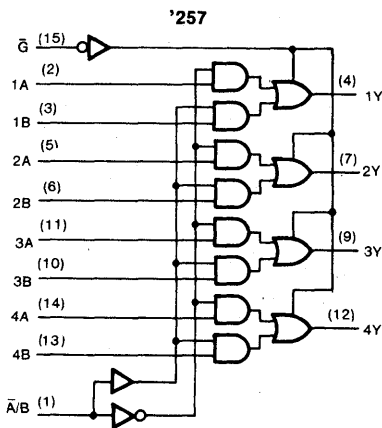
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## FUNCTION TABLE

Output Control	Inputs		Output Y	
	select	Data	'257	'258
$\bar{G}$	$\bar{A}/B$	A B		
H	X	X X	Z	Z
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

## LOGIC DIAGRAMS



# KS54HCTLS 257/258 Quad 2-Line to 1-Line Data Selectors/ KS74HCTLS Multiplexers with 3-State Outputs

## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ		$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
					Guaranteed Limits		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

# KS54HCTLS 257/258 Quad 2-Line to 1-Line Data Selectors/ KS74HCTLS Multiplexers with 3-State Outputs

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS257, HCTLS258

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, A to B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17	18 21	23 28	27 33			ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17	18 21	23 28	27 33			
Maximum Propagation Delay, A/B to any Y	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	16 19	21 24	26 31	31 37			ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	16 19	21 24	26 31	31 37			
Maximum Output Enable Time, G to any Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	22 25	30 33	37 42	45 51		ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	22 25	30 33	37 42	45 51		
Maximum Output Disable Time, G to any Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	20	27	34	41		ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	20	27	34	41			
Maximum Input Capacitance	$C_{IN}$		5					pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

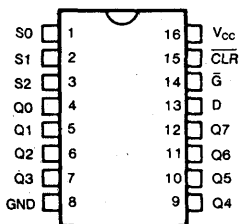
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/Disable input simplifies expansion
- Expandable for N-bit applications
- Four distinct functional modes
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs		Output of Addressed Latch	Each Other Output	Function
CLR	G			
H	L	D	$Q_{i0}$	Addressable Latch
H	H	$Q_{i0}$	$Q_{i0}$	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.  
 $Q_{i0}$  = the level of  $Q_{i0}$  ( $i = 0, 1, \dots, 7$ , as appropriate) before the indicated steady-state input conditions were established.

**DESCRIPTION**

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear ( $\overline{\text{CLR}}$ ) and enable ( $\overline{\text{G}}$ ) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

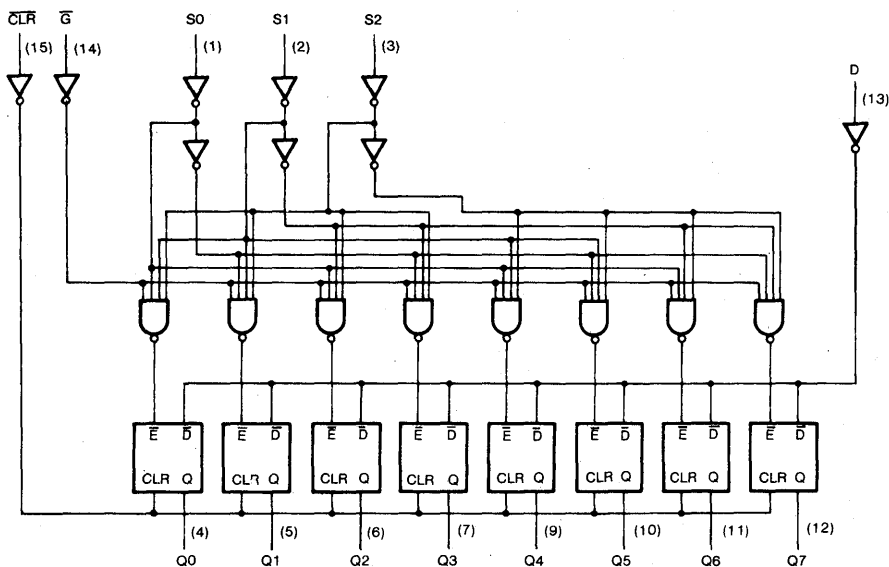
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LATCH SELECTION TABLE**

Select Inputs			Latch Addressed
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$ , . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ † . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}$ , $V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range . . . . .	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r$ , $t_f$ . . . . .	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS259)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Maximum Propagation Delay CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$	22	30	37	45	ns
Maximum Propagation Delay, Data to Any Q	$t_{PLH}$		20	27	34	41	ns
	$t_{PHL}$		20	27	34	41	
Maximum Propagation Delay, Address to any Q	$t_{PLH}$		26	34	43	51	ns
	$t_{PHL}$		26	34	43	51	
Maximum Propagation Delay, $\bar{G}$ to any Q	$t_{PLH}$		22	30	37	45	ns
	$t_{PHL}$		22	30	37	45	
Minimum Pulse Width	CLR LOW		$t_w$	8	10	13	15
	$\bar{G}$ Low	8		10	13	15	
Minimum Setup Time, Data or Address before $\bar{G}\uparrow$	$t_{su}$		8	10	13	15	ns
Minimum Hold Time, Data or Address before $\bar{G}\uparrow$	$t_h$		-3	0	0	0	ns
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$		80				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

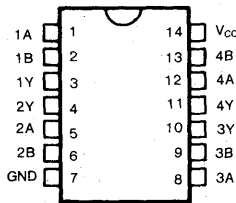
**DESCRIPTION**

These devices contain four independent exclusive-NOR gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

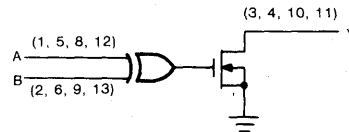
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS266

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0V$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Maximum Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$ $R_L=1\text{k}\Omega$	18	25	31	37		ns	
	$t_{PHL}$		16	22	28	33			
Maximum Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Eight positive-edge-triggered D-type flip-flops with single-rail outputs
- Buffered common clock and asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
( $I_{OL} = 24\text{mA}$  @  $V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

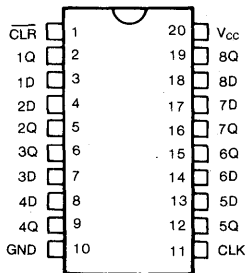
These devices are high-speed octal registers. They consist of eight positive-edge-triggered D-type flip-flops with individual D inputs and Q outputs. All flip flops are loaded and cleared simultaneously by the common buffered clock (CLK) and clear (CLR) inputs.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

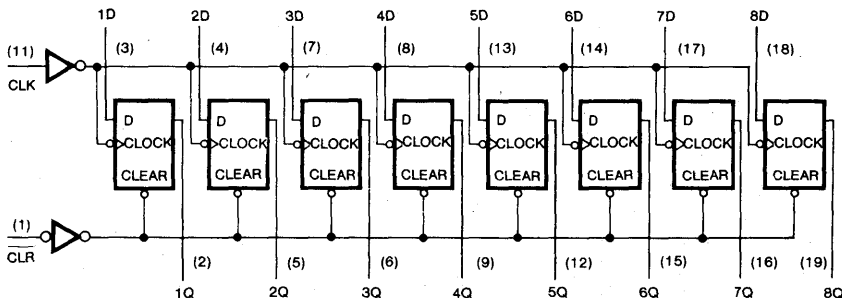


### FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$

### LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS273

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25	20	MHz
Maximum Propagation Delay, CLK to any	$t_{PLH}$	$C_L = 50\text{pF}$	20	27	33	40	ns
		$C_L = 150\text{pF}$	23	30	38	46	
Maximum Propagation Delay, CLR to any Q	$t_{PHL}$	$C_L = 50\text{pF}$	20	27	33	40	ns
		$C_L = 150\text{pF}$	23	30	38	46	
Minimum Pulse Width	CLR Low CLK High or Low	$t_w$	10	13	17	20	ns
			10	13	17	20	
Minimum Setup Time before CLK†	Data	$t_{su}$	10	13	17	20	ns
	Clear inactive State		13	17	21	25	
Minimum Hold Time, Data after CLK†	$t_h$		-3	0	0	0	ns
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$	(per package)	150				pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Generates Odd or Even Parity for Nine Data Lines
- Cascadable for N-Bits Parity
- Can be used to Upgrade Existing Systems using MSI Parity Circuits
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

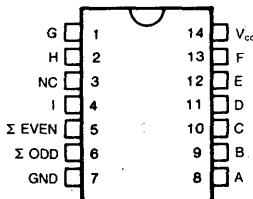
These universal, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the '280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the '280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

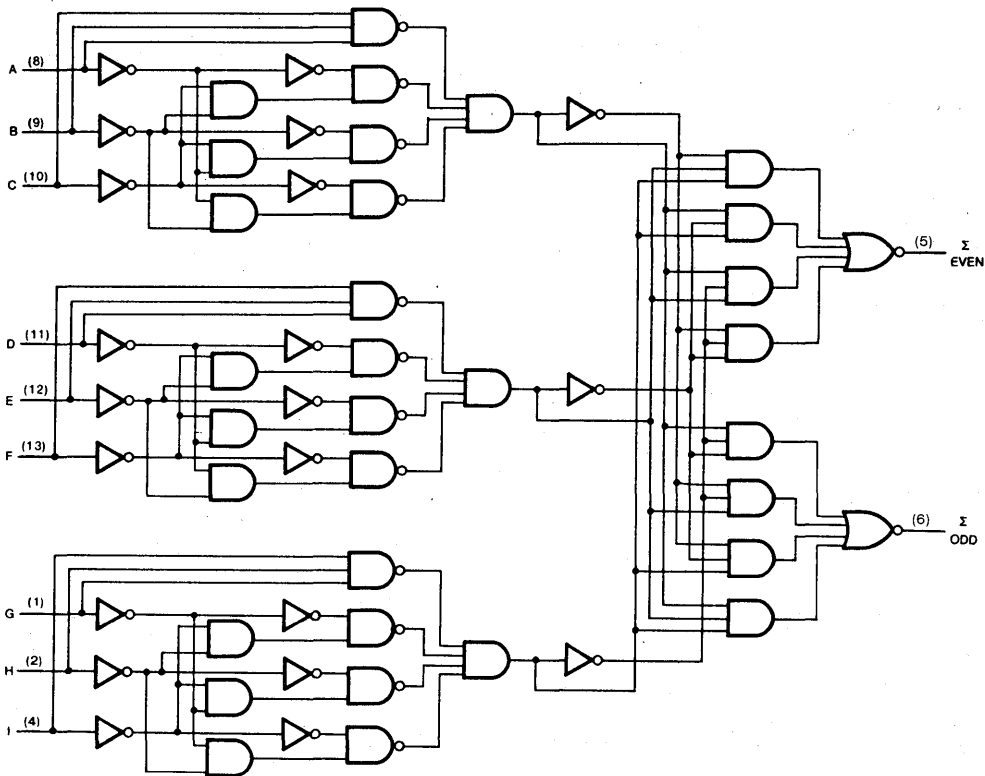
**PIN CONFIGURATION**



**FUNCTION TABLE**

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,4,5,9	L	H

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)



**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V\pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = -20\mu\text{A}$ $I_o = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o = 20\mu\text{A}$ $I_o = 12\text{mA}$ $I_o = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	160.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_i = 2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS280

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay, Any input to $\Sigma$ Even	PLH	$C_L = 50\text{pF}$	30	40	50	60	60	60	ns
		$C_L = 150\text{pF}$	33	43	55	66	66	66	
Maximum Propagation Delay, Any input to $\Sigma$ Odd	tPHL	$C_L = 50\text{pF}$	30	40	50	60	60	60	ns
		$C_L = 150\text{pF}$	33	43	55	66	66	66	
Minimum Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift, shift left, and load data
- Operates with outputs enabled or at high impedance
- Can be cascaded for N-bit word lengths
- Direct overriding clear
- Application:
  - Stacked or push-down registers, buffer storage, and accumulator registers
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  - KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
  - KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

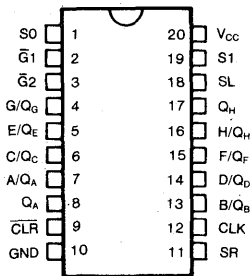
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when  $\overline{\text{CLR}}$  is low. Pulling either of the output controls,  $\overline{\text{G}}1$  or  $\overline{\text{G}}2$ , high disables the outputs but this has no effect on clearing, shifting, or storage of data.

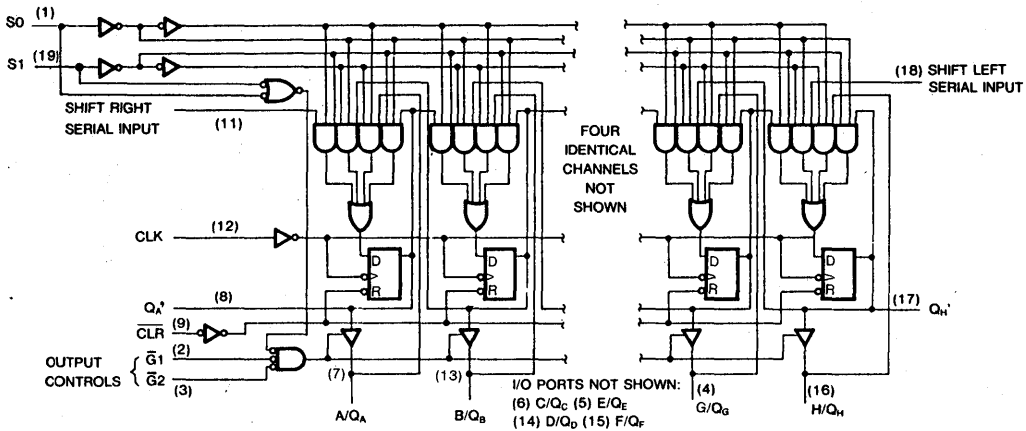
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



LOGIC DIAGRAM



FUNCTION TABLE

Mode	Inputs						I/O Ports								Outputs	
	CLR	S1	S0	Output Control G1 G2	CLK	SL SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
Clear	L	X	L	L L	X	X X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L L	X	X X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X X	X	X X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L L	X	X X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L L	L	X X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L L	↑	X H	H	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	H	QH <sub>n</sub>
	H	L	H	L L	↑	X L	L	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	L	QH <sub>n</sub>
Shift Left	H	H	L	L L	↑	H X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	H	QB <sub>n</sub>	H
	H	H	L	L L	↑	L X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	L	QB <sub>n</sub>	L
Load	H	H	H	X X	↑	X X	a	b	c	d	e	f	g	h	a	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , . . . . . -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
(-0.5V <  $V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
Operating Temperature  
Range KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $Q'_A$ and $Q'_H$ outputs: $I_O = -4mA$ $Q_A$ thru $Q_H$ outputs: $I_O = -6mA$	$V_{CC}$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
			4.2	3.98	3.84	3.7	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $Q'_A$ and $Q'_H$ outputs: $I_O = 4mA$ $I_O = 8mA$ $Q_A$ thru $Q_H$ outputs: $I_O = 12mA$ $I_O = 24mA$	0	0.1	0.1	0.1	V
					0.26 0.39	0.33 0.5	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IN}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS299

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit	
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$
Maximum Clock Frequency	$f_{max}$		35	25	20	18	MHz	
Maximum Propagation Delay, CLK to Q'A or Q'H	$t_{PLH}$	$C_L = 50\text{pF}$	26	35	4	53	ns	
	$t_{PHL}$		26	35	44	53		
Maximum Propagation Delay, CLR to Q'A or Q'H	$t_{PHL}$		30	40	50	60	ns	
Maximum Propagation Delay, CLK to Q <sub>A</sub> thru Q <sub>H</sub>	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40	48	ns	
		$C_L = 150\text{pF}$	27	35	45	54		
	$t_{PHL}$	$C_L = 50\text{pF}$	24	32	40	48		
		$C_L = 150\text{pF}$	27	35	45	54		
Maximum Propagation Delay, CLR to Q <sub>A</sub> thru Q <sub>H</sub>	$t_{PHL}$	$C_L = 50\text{pF}$	30	40	50	60	ns	
		$C_L = 150\text{pF}$	33	43	55	66		
Maximum Output Enable Time, G1, G2, to Q <sub>A</sub> thru Q <sub>H</sub>	$t_{pZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	20	26	33	39	ns
			$C_L = 150\text{pF}$	23	29	38	45	
	$t_{pZL}$		$C_L = 50\text{pF}$	20	26	33	39	
			$C_L = 150\text{pF}$	23	29	38	45	
Maximum Output Disable Time, G1, G2 to Q <sub>A</sub> thru Q <sub>H</sub>	$t_{pHZ}$	$R_L = 1\text{k}\Omega$	13	17	21	26	ns	
	$t_{pLZ}$	$C_L = 50\text{pF}$	13	17	21	26		
Minimum Pulse Width	CLK High or Low	$t_w$	10	13	17	20	ns	
	CLR Low		10	13	17	20		
Minimum Setup time before CLK <sup>†</sup>	S0 and S1	$t_{su}$	13	17	21	25	ns	
	High-Level Inputs		10	13	17	20		
	High-Level Inputs		10	13	17	20		
	CLR Inactive		10	13	17	20		
Minimum Hold Time after CLK <sup>†</sup>	S0 and S1	$t_h$	5	7	8	10	ns	
	All Inputs		0	0	0	0		
Maximum Input Capacitance	$C_{IN}$			5			pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled		10			pF	
Power Dissipation Capacitance*	$C_{PD}$						pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

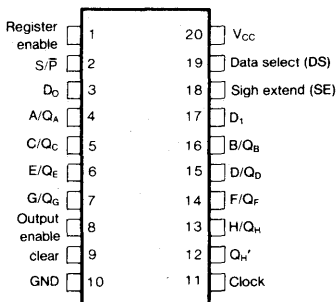
**FEATURES**

- Multiplexed inputs/outputs provide improved bit density
- Sign extend function
- Direct overriding clear
- 3 state outputs drive bus lines directly
- Function pin-out, speed and drive compatibility with 54/74 LS logic family
- Low power consumption characteristic of CMOS
- High drive current output ( $I_{OL} = 24mA @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices.
- Wide Operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature range:  
KS74HCTLS :  $-40^{\circ}C$  to  $+85^{\circ}$   
KS54HCTLS :  $-55^{\circ}C$  to  $+125^{\circ}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**DESCRIPTION**

These 8 bit Shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either  $D_0$  or  $D_1$  input as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/P inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high clock transition. The data extend function repeats the sign in the  $Q_A$  flip flop during shifting. An overriding clear input clears the internal register when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

**PIN CONFIGURATION**



**FUNCTION TABLE**

OPERATION	INPUT							INPUT/OUTPUTS				Output Q <sub>H</sub> '
	Clear	Register enable	S/P	Sign extend	Data select	Output enable	Clock	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub> ...	H/Q <sub>H</sub>	
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q <sub>AO</sub>	Q <sub>BO</sub>	Q <sub>CO</sub>	Q <sub>HO</sub>	Q <sub>HO</sub>
Shift Right	H	L	H	H	L	L	↑	D <sub>0</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Gn</sub>	Q <sub>Gn</sub>
	H	L	H	H	H	L	↑	D <sub>1</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Gn</sub>	Q <sub>Gn</sub>
Sign Extend	H	L	H	L	X	L	↑	Q <sub>An</sub>	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Gn</sub>	Q <sub>Gn</sub>
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H= high level (steady state)

L= low level (steady state)

X= irrelevant (any inputs, including transitions)

↑ = transition from low to high level

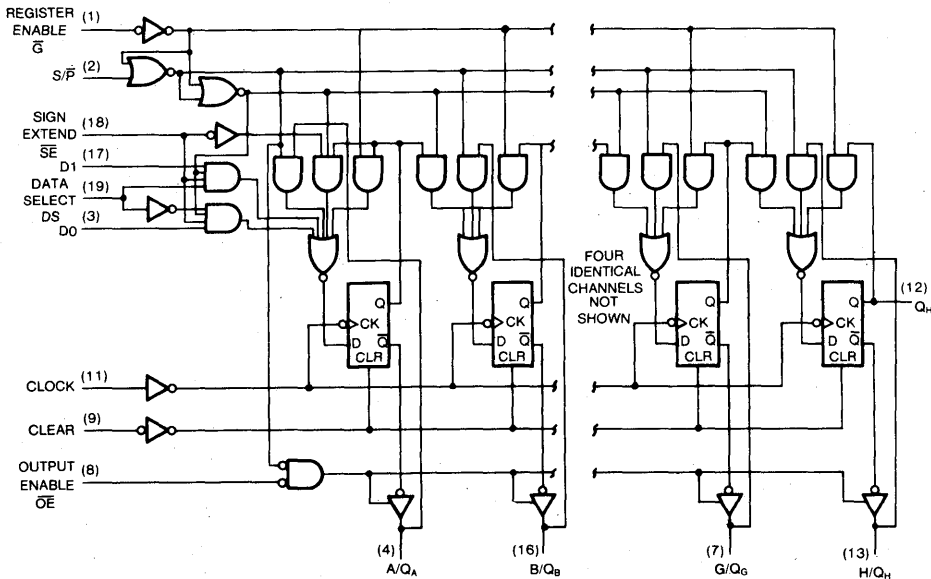
Q<sub>AO</sub>...Q<sub>HO</sub>= the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the indicated steady-state conditions were established.

Q<sub>An</sub>...Q<sub>Hn</sub>= the level of Q<sub>A</sub> through Q<sub>H</sub>, respectively, before the most recent ↑ transition of the clock.

D<sub>0</sub>, D<sub>1</sub>= the level of steady-state inputs at inputs D<sub>0</sub> and D<sub>1</sub> respectively

a...h= the level of steady-state inputs at input A through H respectively.

**LOGIC DIAGRAM**



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ r
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N):	$-12\text{mW}/^\circ\text{C}$ from $65^\circ\text{C}$ to $85^\circ\text{C}$
Ceramic Package (J):	$-12\text{mW}/^\circ\text{C}$ from $100^\circ\text{C}$ to $125^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}$ , $V_{OUT}$	0V to $V_{CC}$
Operating Temperature	
Range	KS74AHCT: $-40^\circ\text{C}$ to $+85^\circ\text{C}$
	KS54AHCT: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r$ , $t_f$	Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT	KS54AHCT	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTL5322A)

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTL5	KS54HCTL5	Unit	
					$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ		Guaranteed Limits			
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25	20	MHz	
Maximum Propagation Delay, Clock to $Q_H$ †	$t_{PHL}$		22	33	41	50	ns	
	$t_{PLH}$		22	33	41	50		
Maximum Propagation Delay, Clear to $Q_H$ †	$t_{PHL}$		27	35	44	53	ns	
Maximum Propagation Delay, Clock to $Q_A$ - $Q_H$	$t_{PHL}$		22	33	41	50	ns	
	$t_{PLH}$		16	25	31	38		
Propagation Delay Clear to $Q_A$ - $Q_H$	$t_{PHL}$	22	35	44	53	ns		
Output Enable Time	$t_{PZH}$	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$	15	35	44	53	ns	
	$t_{PZL}$		15	35	44	53		
Output Disable Time	$t_{PHZ}$		15	25	31	38	ns	
	$t_{PLZ}$		15	25	31	38		
Clock Pulse Width	High		$t_w$	12	16	20	24	ns
	Low		$t_w$	12	16	20	24	
Clear Pulse Width Low		$t_w$	12	16	20	24	ns	
Minimum Data Set up Time		$t_s$	13	16	20	25	ns	
Minimum Select Set up Time		$t_s$	13	16	20	25		
Minimum Data Hold Time		$t_h$	-3	0	0	0	ns	
Minimum Select Hold Time		$t_h$	7	10	12	15		
Minimum Recovery Time		$t_{rec}$	15	20	25	30	ns	
Maximum Input Capacitance		$C_{in}$	5				pF	
Power Dissipation Capacitance		$C_{PD}$	100				pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Inverting Version of '153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

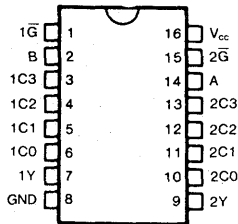
**DESCRIPTION**

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ( $\bar{G}$ ) are provided for each of the two four-line sections.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**PIN CONFIGURATION**

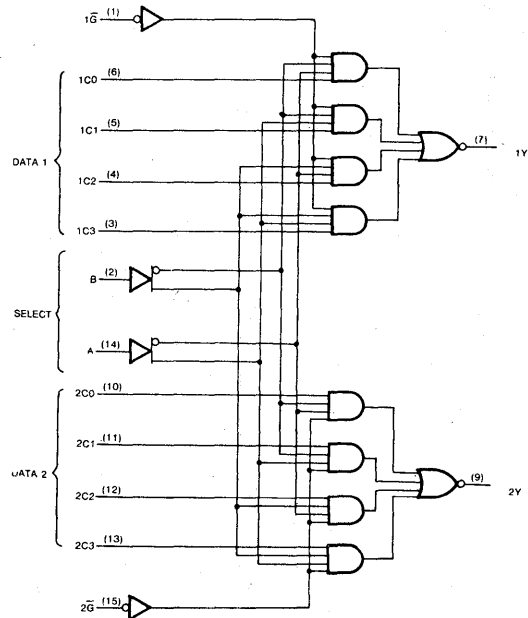


**FUNCTION TABLE**

SELECT		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA
- Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C
- Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$
- Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTL5352

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTL5	KS54HCTL5	Unit
			Guaranteed Limits				
			Typ				
Maximum Propagation Delay, A or B to Y	$t_{PLH}$	$C_L = 50\text{pF}$	23	30	38	45	ns
		$C_L = 150\text{pF}$	26	33	43	51	
	$t_{PHL}$	$C_L = 50\text{pF}$	23	30	38	45	
		$C_L = 150\text{pF}$	26	33	43	51	
Maximum Propagation Delay, Data (Any C) to Y	$t_{PLH}$	$C_L = 50\text{pF}$	19	26	32	39	ns
		$C_L = 150\text{pF}$	21	29	37	45	
	$t_{PHL}$	$C_L = 50\text{pF}$	19	26	32	39	
		$C_L = 150\text{pF}$	21	29	37	45	
Maximum Propagation Delay, $\bar{G}$ to Y	$t_{PLH}$	$C_L = 50\text{pF}$	19	26	32	39	ns
		$C_L = 150\text{pF}$	21	29	37	45	
	$t_{PHL}$	$C_L = 50\text{pF}$	19	26	32	39	
		$C_L = 150\text{pF}$	21	29	37	45	
Maximum Input Capacitance	$C_{IN}$			5			pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Inverting Version of '253
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

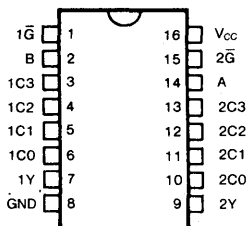
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ( $\bar{G}$ ) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ( $\bar{G}$ ). The output is disabled when its strobe is high.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

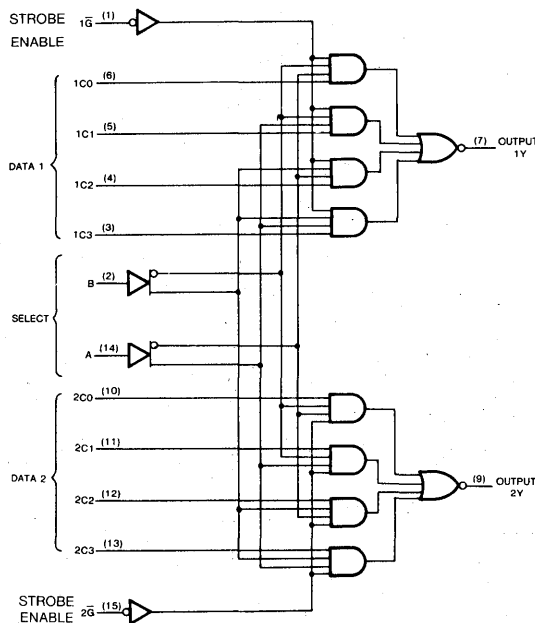


## FUNCTION TABLE

SELECT		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

## LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS353

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		<b>KS74HCTLS</b> $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		<b>KS54HCTLS</b> $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay, A or B to Any Y	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40	48	ns		
		$C_L = 150\text{pF}$	27	35	45	54			
	$t_{PHL}$	$C_L = 50\text{pF}$	24	32	40	48	ns		
		$C_L = 150\text{pF}$	27	35	45	54			
Maximum Propagation Delay, Data (any C) to any Y	$t_{PLH}$	$C_L = 50\text{pF}$	15	20	25	30	ns		
		$C_L = 150\text{pF}$	18	23	30	36			
	$t_{PHL}$	$C_L = 50\text{pF}$	15	20	26	31	ns		
		$C_L = 150\text{pF}$	18	23	31	37			
Maximum Output Enable Time, $\bar{G}$ to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	17	23	29	35	ns	
			$C_L = 150\text{pF}$	20	26	34	41		
	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	17	23	29	35	ns	
			$C_L = 150\text{pF}$	20	26	34	41		
Maximum Output Disable Time, $\bar{G}$ to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	20	27	34	41	ns		
			$C_L = 50\text{pF}$	20	27	34		41	
Maximum Input Capacitance	$C_{IN}$		5				pF		
Maximum Output Capacitance	$C_{OUT}$		10				pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 365A/366A KS74HCTLS 367A/368A

## Hex Bus-Drivers with 3-State Outputs

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

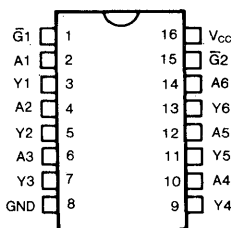
These high-speed Hex bus drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The '365 and '366 have two output enables ( $\bar{G}1$  and  $\bar{G}2$ ) NOR'ed together to control all six gates. The '367 and '368 have two output enables which are configured so that one enable ( $\bar{G}1$ ) controls four gates and the other ( $\bar{G}2$ ) controls the remaining two gates. The '366 and '368 have inverting data paths. The '365 and '367 have noninverting data paths.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION



### FUNCTION TABLES

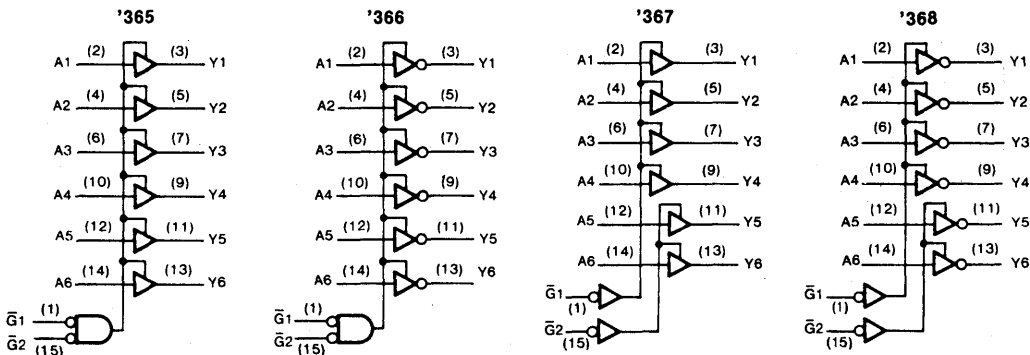
'365 and '366

Inputs		Y Outputs		
$\bar{G}1$	$\bar{G}2$	A	'365	'366
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

'367 and '368

Inputs		Y Outputs	
$\bar{G}1$ & $\bar{G}2$	A	'367	'368
L	L	L	H
L	H	H	L
H	X	Z	Z

### LOGIC DIAGRAMS





# KS54HCTLS **365A/366A** KS74HCTLS **367A/368A**

## Hex Bus-Drivers with 3-State Outputs

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

# KS54HCTLS 365A/366A KS74HCTLS 367A/368A

## Hex Bus-Drivers with 3-State Outputs

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS365A, HCTLS367A

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	14	19	24	28	ns
		$C_L = 150\text{pF}$	17	22	29	34	
	$t_{PHL}$	$C_L = 50\text{pF}$	14	19	24	28	
		$C_L = 150\text{pF}$	17	22	29	34	
Maximum Output Enable Time, $\bar{G}$ to Y	$t_{PZH}$	$C_L = 50\text{pF}$	26	35	44	52	ns
		$C_L = 150\text{pF}$	29	38	49	58	
	$t_{PZL}$	$C_L = 50\text{pF}$	26	35	44	52	
		$C_L = 150\text{pF}$	29	38	49	58	
Maximum Output Disable Time, $\bar{G}$ to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	26	35	44	52	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	26	35	44	52	
Maximum Input Capacitance	$C_{IN}$		5				pF
Maximum Output Capacitance	$C_{OUT}$	Output disabled	10				pF
Power Dissipation Capacitance* (per driver)	$C_{PD}$	$\bar{G} = V_{CC}$	5				pF
		$\bar{G} = \text{GND}$	30				

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS366A, HCTLS368A

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Maximum Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	13	17	21	25	ns
		$C_L = 150\text{pF}$	16	20	26	31	
	$t_{PHL}$	$C_L = 50\text{pF}$	13	17	21	25	
		$C_L = 150\text{pF}$	16	20	26	31	
Maximum Output Enable Time, $\bar{G}$ to Y	$t_{PZH}$	$C_L = 50\text{pF}$	26	35	44	52	ns
		$C_L = 150\text{pF}$	29	38	49	58	
	$t_{PZL}$	$C_L = 50\text{pF}$	26	35	44	52	
		$C_L = 150\text{pF}$	29	38	49	58	
Maximum Output Disable Time, $\bar{G}$ to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	26	35	44	52	ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	26	35	44	52	
Maximum Input Capacitance	$C_{IN}$		5				pF
Maximum Output Capacitance	$C_{OUT}$	Output disabled	10				pF
Power Dissipation Capacitance* (per driver)	$C_{PD}$	$\bar{G} = V_{CC}$	5				pF
		$\bar{G} = \text{GND}$	30				

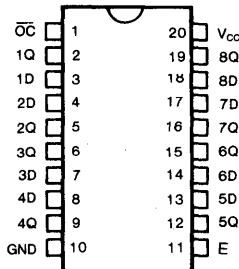
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

The '373 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent: when the enable (E) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

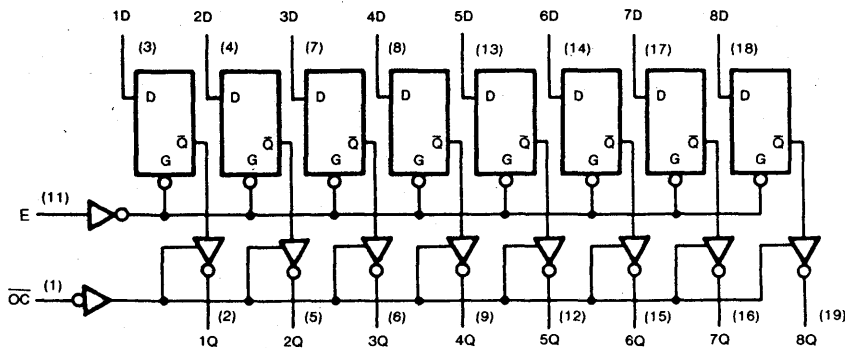
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLE**

(Each Latch)

Inputs			Output
$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_{O1}$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_{d1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_A = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_Z=2.4V$ Other Inputs: At $V_{CC}$ or GND $I_O=0$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS373)

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit	
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		
			Typ		Guaranteed Limits			
Maximum Propagation Delay, D to Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	14	18	23	27	ns	
		C <sub>L</sub> = 150pF	17	21	28	33		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	14	18	23	27	ns	
		C <sub>L</sub> = 150pF	17	21	28	33		
Maximum Propagation Delay, E to any Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	22	30	37	45	ns	
		C <sub>L</sub> = 150pF	25	33	42	51		
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	22	30	37	45	ns	
		C <sub>L</sub> = 150pF	25	33	42	51		
Maximum Output Enable Time, OC to any Q	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	24	32	40	48	ns
			C <sub>L</sub> = 150pF	27	35	45	54	
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	C <sub>L</sub> = 50pF	24	32	40	48	
			C <sub>L</sub> = 150pF	27	35	45	54	
Maximum Output Disable Time, OC to any Q	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	19	25	31	37	ns	
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	19	25	31	37		
Minimum Pulse Width, E High	t <sub>w</sub>		6	10	12	15	ns	
Minimum Setup Time, D before E↑	t <sub>su</sub>		2	3	4	5	ns	
Minimum Hold Time, D after E↓	t <sub>h</sub>		6	10	12	15	ns	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF	
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10				pF	
Power Dissipation Capacitance* (per latch)	C <sub>PD</sub>	OC = V <sub>CC</sub> OC = GND	5				pF	
			30					

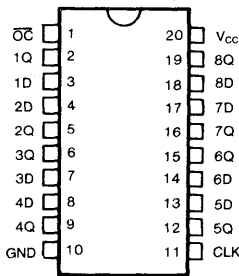
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
**KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$**   
**KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$**
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## DESCRIPTION

The '374 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

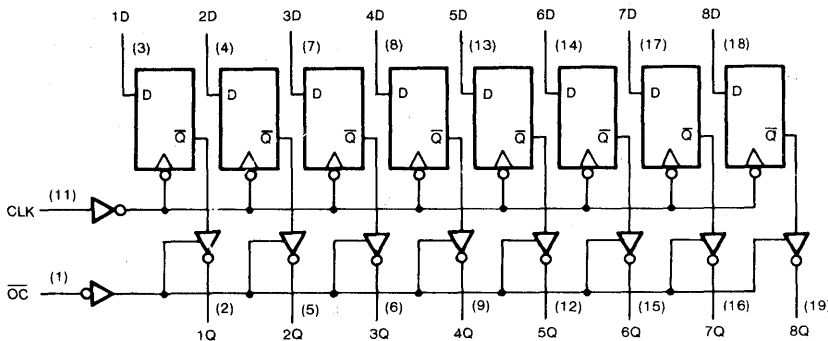
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

## LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_{d1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature

Range KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
				$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu A$ $I_O=-6mA$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS374

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit		
			Typ		Guaranteed Limits						
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	45	35	30		25		MHz		
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48		ns		
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48				
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{pZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48		ns	
	$t_{pZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48			
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{pHZ}$	$R_L = 1\text{k}\Omega$	19 25		31		37		ns		
	$t_{pLZ}$	$C_L = 50\text{pF}$	19 25		31		37				
Minimum Pulse Width, CLK High or Low	$t_w$		7	10	12		15		ns		
Minimum Setup Time, D before CLK†	$t_{su}$		10	13	17		20		ns		
Minimum Hold Time, D after CLK†	$t_h$		-3	0	0		0		ns		
Maximum Input Capacitance	$C_{IN}$		5						pF		
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF		
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5						pF		
		$\overline{OC} = \text{GND}$	30								

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Can be used for implementing
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5 \text{ V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

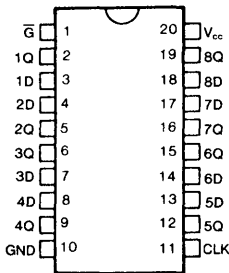
The '377 contains eight positive-edge-triggered D-type flip-flops with an enable input. This part is similar to '273 but features a latched clock enable ( $\bar{G}$ ) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if  $\bar{G}$  is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the  $\bar{G}$  input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

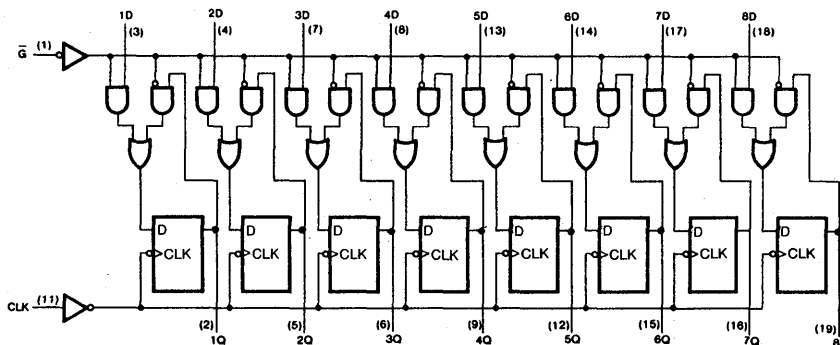


**FUNCTION TABLE**

(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\bar{G}$	CLK	DATA	Q
H	X	X	$Q_0$
L	↑	H	H
L	↑	L	L
X	L	X	$Q_0$

**LOGIC DIAGRAM**



#### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ † . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

#### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range . . . . .	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r, t_f$ . . . . .	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

#### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS377

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%		KS54HCTLS T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%		Unit
			Typ	Guaranteed Limits					
Maximum Clock Frequency	f <sub>max</sub>		45	35	30		25		MHz
Maximum Propagation Delay, CLK to Any Q	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	18	27	32		38		ns
	t <sub>PHL</sub>		18	27	32		38		
Minimum Pulse Width	$\bar{G}$ Low	t <sub>w</sub>	12	16	20		25		ns
	CLK high or Low		12	16	20		25		
Minimum Setup Time before CLK†	Data	t <sub>su</sub>	6	10	15		20		ns
	$\bar{G}$ high or LOW		15	20	25		25		
Minimum Hold Time, Data after CLK†	t <sub>h</sub>		-3	0	0		0		ns
Maximum Input Capacitance	C <sub>IN</sub>		5						pF
Power Dissipation Capacitance*	C <sub>PD</sub>								pF

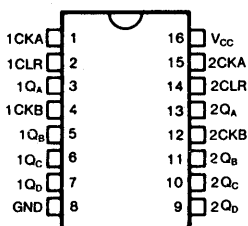
\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Individual clock for A and B flip-flops provide dual +2 and +5 counters
- Direct clear for each 4-bit counter
- Significant improvement in system density through reduced counter package count.
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### FUNCTION TABLES

**BCD COUNT SEQUENCE**  
( Each Counter )  
(See Note A)

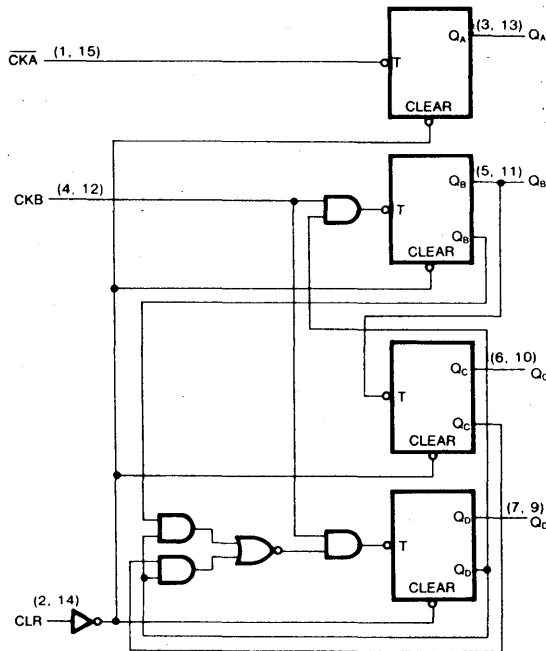
COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**BIQUINARY (5-2)**  
( Each Counter )  
(See Note B)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES A. Output Q<sub>A</sub> is connected to input CKB for BCD count.  
B. Output Q<sub>D</sub> is connected to input CKA for biquinary count.

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , .....  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d^\dagger$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTL5:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTL5:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

#### DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T <sub>a</sub> = 25°C		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	V <sub>IH</sub>			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =-20μA I <sub>O</sub> =-4mA	V <sub>CC</sub> 4.2	V <sub>CC</sub> -0.1 3.98	V <sub>CC</sub> -0.1 3.84	V <sub>CC</sub> -0.1 3.7	V
Maximum Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> =20μA I <sub>O</sub> =4mA I <sub>O</sub> =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI <sub>CC</sub>	per input pin V <sub>I</sub> =2.4V other Inputs: at V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA		2.7	2.9	3.0	mA

#### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> ≤ 6 ns, HCTLS390)

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C		KS74HCTLS	KS54HCTLS	Unit
			V <sub>CC</sub> = 5.0V	Guaranteed Limits			
Maximum Clock Frequency CKA to Q <sub>A</sub> or CKB to Q <sub>B</sub>	f <sub>max</sub>		35	25	20	20	MHz
Maximum Propagation Delay, CKA to Q <sub>A</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15	20	25	30	ns
	t <sub>PHL</sub>		15	20	25	30	
Maximum Propagation Delay, CKA to Q <sub>C</sub>	t <sub>PLH</sub>		36	48	60	72	ns
	t <sub>PHL</sub>		36	48	60	72	
Maximum Propagation Delay, CKB to Q <sub>B</sub>	t <sub>PLH</sub>		16	21	26	31	ns
	t <sub>PHL</sub>		16	21	26	31	
Maximum Propagation Delay, CKB to Q <sub>C</sub>	t <sub>PLH</sub>		24	32	40	48	ns
	t <sub>PHL</sub>		24	32	40	48	
Maximum Propagation Delay, CKB to Q <sub>D</sub>	t <sub>PLH</sub>		16	21	26	31	ns
	t <sub>PHL</sub>		16	21	26	31	
Maximum Propagation Delay, CLR to Any Q	t <sub>PHL</sub>		24	32	40	48	ns
Minimum Pulse Width CKA or CKB high or low CLR high	t <sub>su</sub>		12	16	20	24	ns
			12	16	20	24	
Minimum Setup Time, CLR inactive before CKA or CKB	t <sub>su</sub>		15	20	25	30	ns
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance	C <sub>PD</sub>						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub>=C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>IN</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74HCTLS: -40°C to +85°C**  
**KS54HCTLS: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

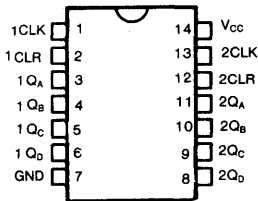
**DESCRIPTION**

The '393 consists of two independent 4-bit binary counters each with its own clear and clock inputs. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. Parallel outputs from each counter stage provide any submultiple of the input count frequency for system timing signals.

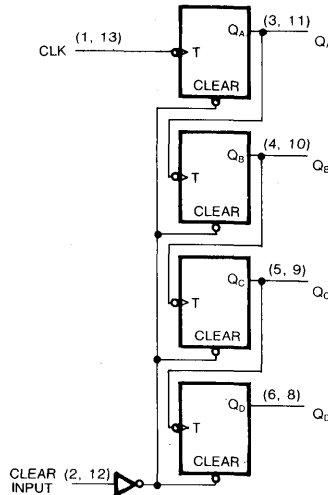
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

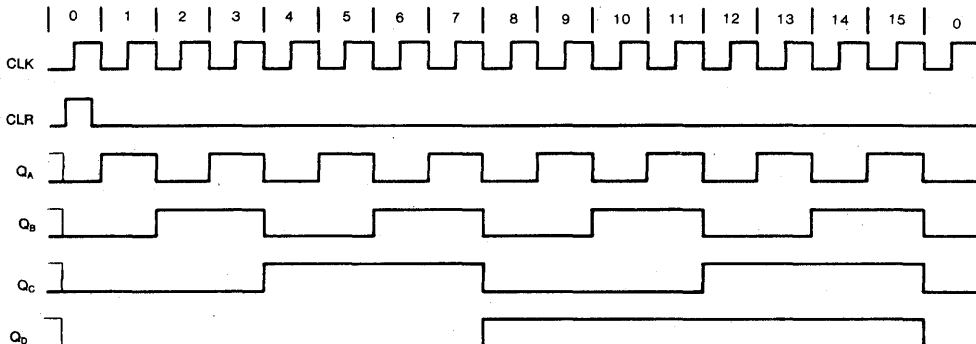
**PIN CONFIGURATION**



**LOGIC DIAGRAMS**



**LOGIC TIMING WAVEFORMS**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_{d1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-1\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS		KS54HCTLS		Unit
					$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$			
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS393

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	f <sub>max</sub>	C <sub>L</sub> = 50pF	40	30	25	20	MHz
Maximum Propagation Delay, A to Q <sub>A</sub>	t <sub>PLH</sub>		15	20	25	30	ns
	t <sub>PHL</sub>		15	20	25	30	
Maximum Propagation Delay, A to Q <sub>B</sub>	t <sub>PLH</sub>		26	35	44	53	ns
	t <sub>PHL</sub>		26	35	44	53	
Maximum Propagation Delay, A to Q <sub>C</sub>	t <sub>PLH</sub>		34	45	56	67	ns
	t <sub>PHL</sub>		34	45	56	67	
Maximum Propagation Delay, A to Q <sub>D</sub>	t <sub>PLH</sub>		45	60	75	90	ns
	t <sub>PHL</sub>		45	60	75	90	
Maximum Propagation Delay, CLR to any Q	t <sub>PHL</sub>		29	39	49	58	ns
Minimum Pulse Width	A Input High or Low	t <sub>w</sub>	10	13	17	20	ns
	CLR High		10	13	17	20	
Minimum Hold Time, CLR Inactive before A	t <sub>su</sub>		10	13	17	20	ns
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>	(per counter)	40				pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74HCTLS: -40°C to +85°C**  
**KS54HCTLS: -55°C to +125°C**
- **Package options include "small outline" packages (Available Tape & Reel), standard DIPs.**

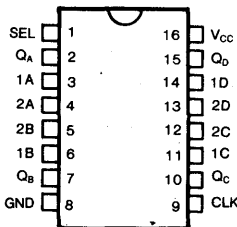
**DESCRIPTION**

These are high-speed quad 2-port registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A common select input (SEL) selects between two 4-bit input ports. The selected data is transferred to the output register on the low-to-high transition of the clock input.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

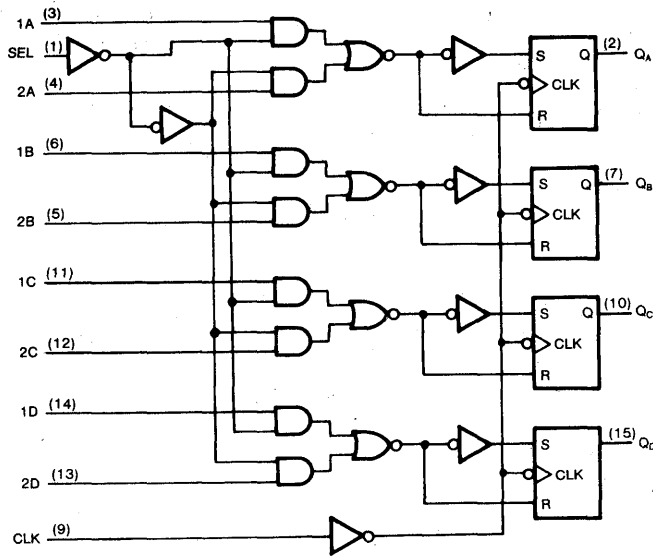


**FUNCTION TABLE**

SEL	Inputs		Output
	Port 1	Port 2	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = Low Voltage Level one setup time prior to the low-to-high clock transition  
h = High Voltage Level one setup time prior to the low-to-high clock transition

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range $V_{CC}$	..... -0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	..... $\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	..... $\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	..... $\pm 35$ mA
Continuous Current Through	
$V_{CC}$ or GND pins	..... $\pm 125$ mA
Storage Temperature Range, $T_{stg}$	..... $-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ †	..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage, $V_{CC}$	..... 4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	... 0V to $V_{CC}$
Operating Temperature	
Range	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r, t_f$	..... Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o=-20\mu\text{A}$ $I_o=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_o=20\mu\text{A}$ $I_o=4\text{mA}$ $I_o=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_i=2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**5**

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS399

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			$V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Propagation Delay, CLK to Q or $\bar{Q}$	$t_{PLH}$	$C_L=50\text{pF}$	22	30	37	45	ns
	$t_{PHL}$		22	30	37	45	
Minimum Pulse Width, CLK High or Low	$t_w$		10	13	17	20	ns
Minimum Setup Time before CLK†	Data	$t_{su}$	10	13	17	20	ns
	Word Select		10	13	17	20	
Minimum Hold Time after CLK†	Data	$t_h$	-3	0	0	0	ns
	Word Select		-3	0	0	0	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Simple pulse width formula  $t_w = 0.45RC$
- DC triggered from active HIGH or active Low Inputs
- Retriggerable for very long output pulses up to 100% duty cycle
- Overriding clear terminates output pulse
- Schmitt trigger A & B inputs allow infinite rise and fall times on these inputs
- Functions, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:  
 $I_{OL} = 8mA @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range; 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}C$  to  $+85^{\circ}C$   
 KS54HCTLS:  $-55^{\circ}C$  to  $+125^{\circ}C$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

The '423 contains dual retriggerable monostable multivibrators with output pulsewidth control by two methods. The basic pulse time is programmed by selection of an external resistor ( $R_{EXT}$ ) and capacitor ( $C_{EXT}$ ). The external resistor and capacitor are normally connected as shown timing component.

Once triggered, the basic output pulse width may be extended by retriggering the gated active Low-going edge input ( $A_i$ ) or the active High-going edge input ( $B_i$ ). By repeating this process, the output pulse period ( $nQ=HIGH, n\bar{Q}=LOW$ ) can be made as long as desired.

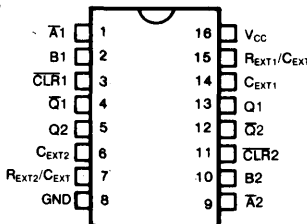
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques.

The output pulse equation is simply;

$$t_w = 0.45 \times R_{EXT} \times C_{EXT}(typ).$$

Where  $t_w$  is in seconds. R is in ohm. and C is in farads. All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**FUNCTION TABLE**

Inputs			Outputs	
CLR	$\bar{A}$	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		

- H= HIGH voltage level
- L= LOW voltage level
- X= don't care
- ↑= LOW to HIGH transition
- ↓= HIGH to LOW transition
- = one HIGH level output pulse
- = one LOW level output pulse

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  -65°C to +150°C  
 Power Dissipation Per Package,  $P_d \uparrow$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package(N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ..... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input in $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT} = 0\mu\text{A}$		2.7	2.9	3.0	mA

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns, HCTLS423)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74AHCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ		Guaranteed Limits					
Propagation Delay $\bar{A}, B$ to $Q, \bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_{ext} = 0,$ $R_{ext} = 5\text{k}\Omega$	23	33	41		50		ns	
	$t_{PHL}$		23	33	41		50			
Propagation Delay $\text{CLR}$ to $Q, \bar{Q}$	$t_{PLH}$		20	27	34		41		ns	
	$t_{PHL}$		20	27	34		41			
Output Pulse Width 1	$t_{WQ1}$		116	200	207		209		ns	
Output Pulse Width 2	$t_{WQ2}$	$C_L = 50\text{pF}$ $C_{ext} = 10\text{nF}$ $R_{ext} = 10\text{k}\Omega$	45	40 50	38(min) 52(max)		27(min) 75(max)		$\mu\text{s}$	
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $A_i = \text{LOW}$	7	20	25		30		ns	
Trigger Pulse Width	$t_w$	$C_L = 50\text{pF}$ $B_i = \text{High}$	7	20	25		30		ns	
Clear Pulse Width	$t_w$	$C_L = 50\text{pF}$ $\text{CLR}_i = \text{LOW}$	8	20	25		30		ns	
External Timing Resistance	$R_{ext}$			2 100	2(min) 100 (max)		2(min) 100 (max)		$\text{k}\Omega$	
External Timing Capacitance	$C_{ext}$		no restriction							
Input Capacitance	$C_{in}$		5							pF
Power Dissipation Capacitance	$C_{PD}$									pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## Application Information

The basic output pulse width is determined by the value of external capacitance and timing resistance.

For output pulse widths greater than  $100\mu\text{s}$  or external capacitance greater than  $10\text{nF}$  the following equation should be used.

$$t_w = k \cdot R_{ext} \cdot C_{ext}$$

Where

$t_w$  is in  $\mu\text{s}$

$k$  is the multiplying factor

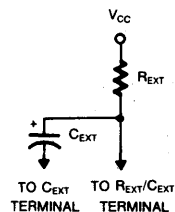
and is approximately 0.45 for

$C_{ext}$  is in nF

$R_{ext}$  is in  $\text{k}\Omega$

For best results, system ground should be applied to the  $C_{ext}$  terminal. These devices do not require a switching diode in series with the  $R_{ext}/C_{ext}$  terminal (as required by some other monostable multivibrators)

## TIMING COMPONENT



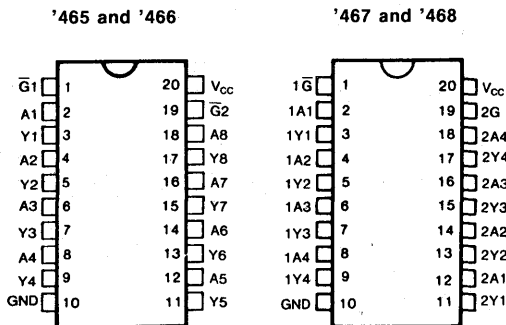
# KS54HCTLS **465/466** KS74HCTLS **467/468**

## Octal Buffers and Line Drivers with 3-State Outputs

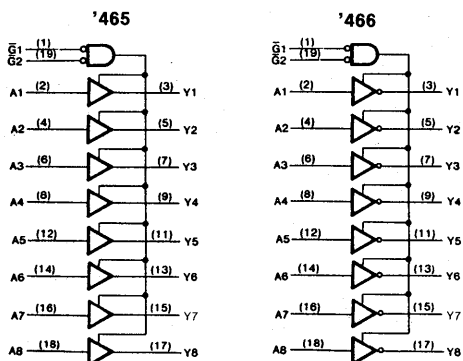
### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATIONS



### LOGIC DIAGRAMS



### DESCRIPTION

These high-speed octal buffers and drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has the choice of inverting/noninverting outputs and various types of output controls.

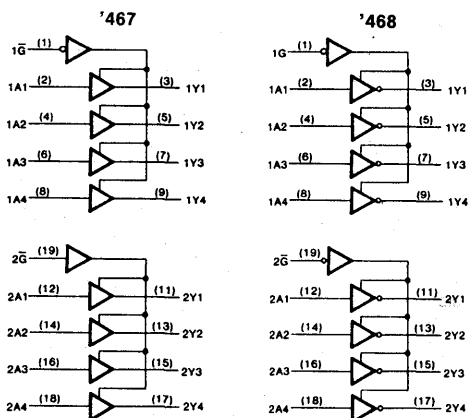
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLE

Input			Output	
$\bar{G}_1$	$\bar{G}_2$	A	'465	'466
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

Input			Output	
G	$\bar{G}$	A	'467	'468
H	L	L	L	H
H	L	H	H	L
L	H	X	Z	Z





**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
Continuous Current-Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
Operating Temperature  
Range KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

KS54HCTLS **465/466**  
 KS74HCTLS **467/468**

**Octal Buffers and Line Drivers  
 with 3-State Outputs**

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS465, HCTLS466,  
 HCTLS467, HCTLS468

Characteristic	Symbol	Conditions	54/74A8CT		KS74HCTLS		54HCTLS		Unit
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ		Guaranteed Limits				
Maximum Propagation Delay, A to Y	t <sub>PLH</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11	15	19	22	ns		
			14	18	24	28			
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	11	15	19	22			
			14	18	24	28			
Maximum Output Enable Time, Enable to Y	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF	24	32	40	48	ns		
			27	35	45	54			
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF C <sub>L</sub> = 150pF	24	32	40	48			
			27	35	45	54			
Maximum Output disable Time, Enable to Y	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	24	32	40	48	ns		
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	24	32	40	48			
Maximum Input Capacitance	C <sub>IN</sub>		4				pF		
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10				pF		
Power Dissipation Capacitance* (per stage)	C <sub>PD</sub>	Output Disabled	5				pF		
		Output Enabled	30						

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.  
 † For AC switching test circuits and timing waveforms see section 2.

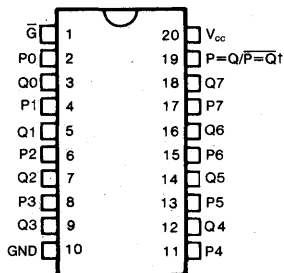
### FEATURES

- Compares two 8-bit words
- '518, '520 and '522 have 20KΩ Pull-up resistors on Q inputs

TYPE	INPUT PULL-UP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
'518	Yes	P=Q open-drain
'519	No	P=Q open-drain
'520	Yes	$\overline{P}=\overline{Q}$ totem-pole
'521	No	$\overline{P}=\overline{Q}$ totem-pole
'522	Yes	$\overline{P}=\overline{Q}$ open-drain

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



† P=Q for '518 and '519;  $\overline{P}=\overline{Q}$  for '520, '521, '522.

### DESCRIPTION

These identity comparators perform comparisons on two eight-bit binary or BCD words. The '518 and '519 provide P=Q outputs, while the '520, '521, and '522 provide  $\overline{P}=\overline{Q}$  outputs. The '518, '519, and '522 have open-drain outputs. The '518, '520, and '522 feature 20-kΩ inputs for analog or switch data.

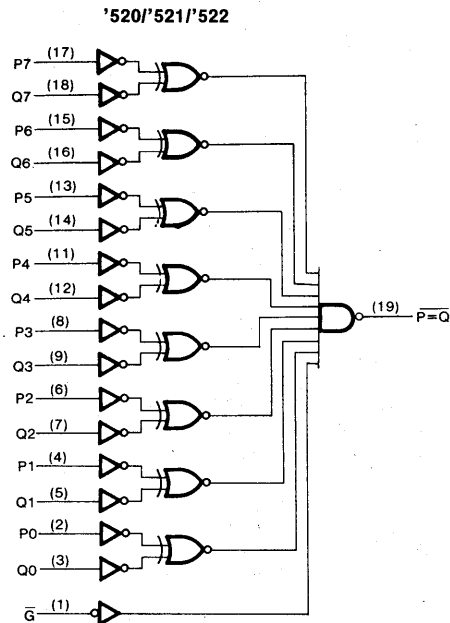
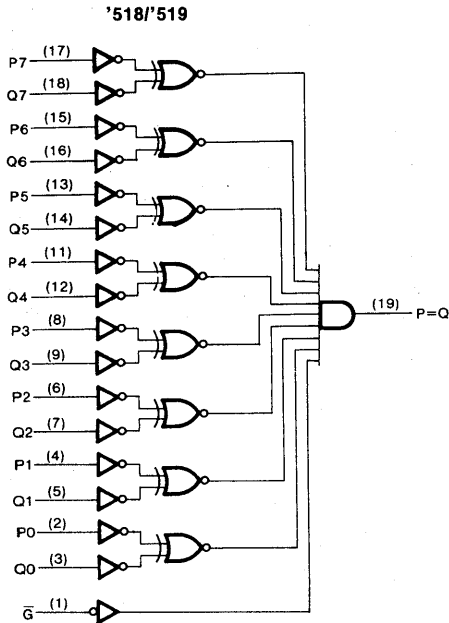
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLE

INPUTS		OUTPUTS	
DATA P, Q	ENABLE $\overline{G}$	P = Q	$\overline{P} = \overline{Q}$
P=Q	L	H	L
P>Q	L	L	H
P<Q	L	L	H
X	H	L	H

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V=10\%$  Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS		KS54HCTLS		Unit
					$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage (Totem-pole Outputs)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.93	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage (All Outputs)	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	C	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current ('518, '520 and '522 Q input)		$V_{CC}=\text{Max}$ $V_{IN}=2.7\text{V}$ $V_{IN}=0.4\text{V}$		-0.2 -0.6	-0.2 -0.6	-0.2 -0.6	-0.2 -0.6	mA	
Maximum Input Current (All other Inputs)	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum Output Leakage Current (Open-Drain Outputs)	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\pm 10.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	For '518, '520 and '522: $V_{IN}=\text{GND}$ (Q0-Q7) $V_{IN}=V_{CC}$ or GND (all other inputs)		3.5	3.5	3.5	3.5	mA	
		For '519 and '521: $V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	160.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_i=2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS518, HCTLS519

Characteristic	Symbol	Conditions	54174AIGHT $T_a = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$		54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, from P or Q to $P=Q$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	26 29	33 36	40 45		47 53		ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48		
Maximum Propagation Delay, from $\bar{G}$ to $P=Q$	$t_{PLH}$	$C = 50\text{pF}$ $C_L = 150\text{pF}$	23 26	29 32	35 40		41 47		ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	18 21	24 27	30 35		36 42		
Maximum Input Capacitance	$C_{IN}$		5						pF
Maximum Output Capacitance	$C_{OUT}$								pF
Power Dissipation Capacitance*	$C_{PD}$								pF

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS520, HCTLS521

Characteristic	Symbol	Conditions	54174AIGHT $T_a = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$		54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, from P or Q to $\bar{P}=\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	12 15	22 25	28 33		33 39		ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	16 19	22 25	28 33		33 39		
Maximum Propagation Delay, from $\bar{G}$ to $\bar{P}=\bar{Q}$	$t_{PLH}$	$C = 50\text{pF}$ $C_L = 150\text{pF}$	15 18	20 23	25 30		30 36		ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18	20 23	25 30		30 36		
Maximum Input Capacitance	$C_{IN}$		5						pF
Maximum Output Capacitance	$C_{OUT}$								pF
Power Dissipation Capacitance*	$C_{PD}$								pF

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS522

Characteristic	Symbol	Conditions	54174AIGHT $T_a = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$		54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, from P or Q to $\bar{P}=\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	24 27	31 34	37 42		43 49		ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	19 22	26 29	32 37		38 44		
Maximum Propagation Delay, from $\bar{G}$ to $\bar{P}=\bar{Q}$	$t_{PLH}$	$C = 50\text{pF}$ $C_L = 150\text{pF}$	23 27	29 32	35 40		41 47		ns
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	18 21	24 27	30 35		36 42		
Maximum Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$								pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTL5: -40°C to +85°C  
 KS54HCTL5: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

The '533 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

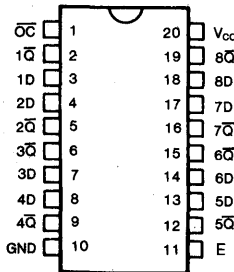
The latches are transparent: when the enable (E) is high, the  $\bar{Q}$  outputs follow the complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\bar{OC}$ ) which places the outputs at high-impedance state when it is taken high. The  $\bar{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**PIN CONFIGURATION**

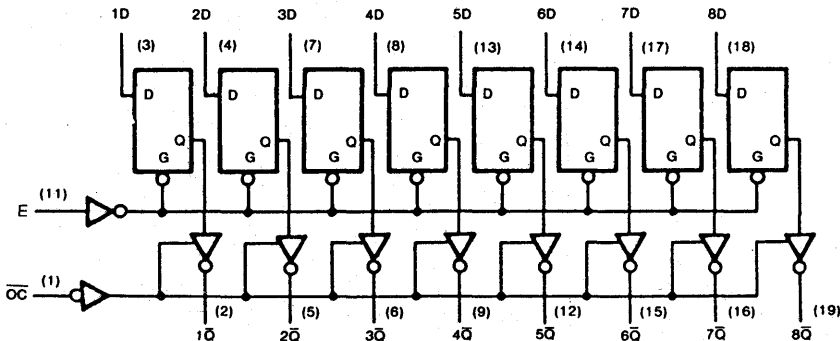


**FUNCTION TABLE**

(Each Latch)

Inputs			Output
$\bar{OC}$	E	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS533

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, D to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	14	18	23	27	ns		
		$C_L = 150\text{pF}$	17	21	28	33			
	$t_{PHL}$	$C_L = 50\text{pF}$	14	18	23	27			
		$C_L = 150\text{pF}$	17	21	28	33			
Maximum Propagation Delay E to $\bar{Q}$	$t_{PLH}$	$C = 50\text{pF}$	22	30	37	45	ns		
		$C_L = 150\text{pF}$	25	33	43	41			
	$t_{PHL}$	$C_L = 50\text{pF}$	22	30	37	48			
		$C_L = 150\text{pF}$	25	33	43	54			
Maximum Output Enable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{pZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40	48	ns	
			$C_L = 150\text{pF}$	27	35	45	54		
	$t_{pZL}$	$C_L = 50\text{pF}$	24	32	40	48			
		$C_L = 150\text{pF}$	27	35	45	54			
Maximum Output Disable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{pHZ}$	$R_L = 1\text{k}\Omega$	19	25	31	37	ns		
	$t_{pLZ}$	$C_L = 50\text{pF}$	19	25	31	37			
Minimum Pulse Width, E High	$t_w$		6	10	12	15	ns		
Minimum Setup Time, D before E↓	$t_{su}$		2	3	4	5	ns		
Minimum Hold Time, D after E↓	$t_h$		6	10	12	15	ns		
Maximum Input Capacitance	$C_{IN}$		5				pF		
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10				pF		
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{OC} = V_{CC}$	5				pF		
		$\bar{OC} = \text{GND}$	30						

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**DESCRIPTION**

The '534 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

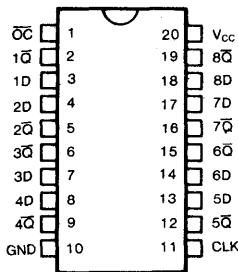
The flip-flops are edge-triggered on the positive transition of the clock; the  $\bar{Q}$  outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs in high-impedance state when it is taken high. The OC signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**

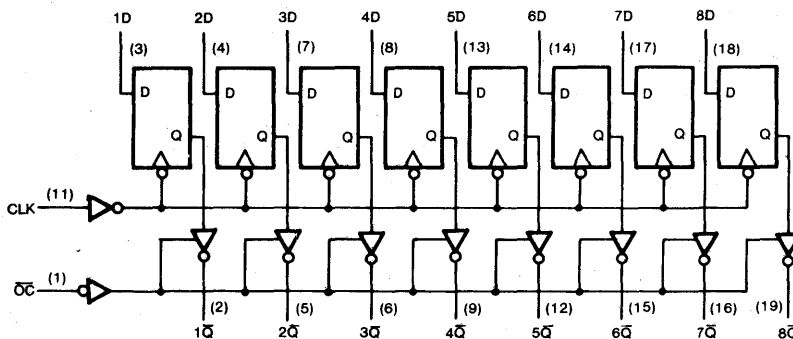


**FUNCTION TABLE**

(Each Latch)

Inputs			Output
$\overline{OC}$	CLK	D	$\bar{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74HCTL5: -40°C to +85°C  
KS54HCTL5: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTL5 $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTL5 $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0			$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS534

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ	Guaranteed Limits						
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	50	35	30		25		MHz	
Maximum Propagation Delay, CLK to any $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	21	28	35		42		ns	
		$C_L = 150\text{pF}$	24	31	40		48			
	$t_{PHL}$	$C_L = 50\text{pF}$	21	28	35		42		ns	
		$C_L = 150\text{pF}$	24	31	40		48			
Maximum Output Enable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	21	28	35		42		ns
			$C_L = 150\text{pF}$	24	31	40		48		
	$t_{PZL}$	$C_L = 50\text{pF}$	21	28	35		42			
		$C_L = 150\text{pF}$	24	31	40		48			
Maximum Output Disable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	19	25	31		37		ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	19	25	31		37			
Minimum Pulse Width, CLK High or Low	$t_w$		9	13	15		18		ns	
Minimum Setup Time, D before CLK†	$t_{su}$		10	13	17		20		ns	
Minimum Hold Time, D after CLK†	$t_h$		-3	0	0		0		ns	
Maximum Input Capacitance	$C_{IN}$		5						pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{OC} = V_{CC}$	5						pF	
		$\bar{OC} = \text{GND}$	30							

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 540/541 KS74HCTLS

## Octal Buffers and Line Drivers with 3-State Outputs

### FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA}$  @  $V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

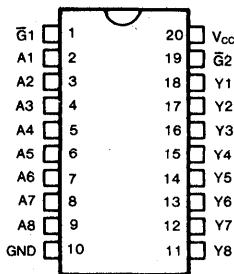
The '540 and '541 are general purpose high-speed octal line drivers/buffers with 3-state outputs. The inputs and outputs are located on opposite sides of the 20-pin package, thus improving circuit board density. The '540 provides inverted data and the '541 provides true data at the outputs.

The three-state control gate is a 2-input NOR such that if either  $\overline{G}_1$  or  $\overline{G}_2$  is high, all eight outputs are in the high impedance state.

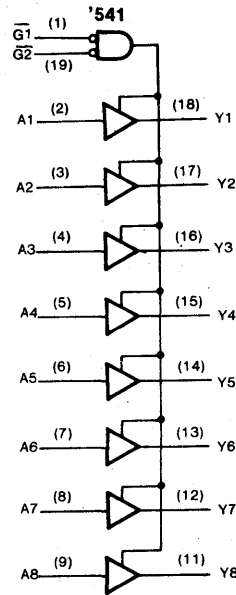
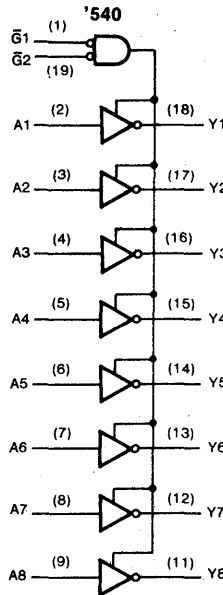
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground

### PIN CONFIGURATION



### LOGIC DIAGRAMS



### FUNCTION TABLE

Input			Output	
$\overline{G}_1$	$\overline{G}_2$	A	'540	'541
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		
			Guaranteed Limits				
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$	8.0	80.0	160.0	$\mu A$	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS540, HCTLS541

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay, A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	11	15	19	23	ns		
		$C_L = 150\text{pF}$	14	18	24	29			
	$t_{PHL}$	$C_L = 50\text{pF}$	11	15	19	23	ns		
		$C_L = 150\text{pF}$	14	18	24	29			
Maximum Output Enable Time, $\bar{G}$ to Y	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	25	25	37	ns	
			$C_L = 150\text{pF}$	21	28	30	43		
	$t_{PZL}$	$C_L = 50\text{pF}$	18	25	31	37			
		$C_L = 50\text{pF}$	21	28	36	43			
Maximum Output Disable Time, $\bar{G}$ to Y	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	13	18	23	27	ns		
	$t_{PLZ}$	$C_L = 50\text{pF}$	13	18	23	27			
Maximum Input Capacitance	$C_{IN}$		5				pF		
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10				pF		
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{G} = V_{CC}$	5				pF		
		$\bar{G} = \text{GND}$	30						

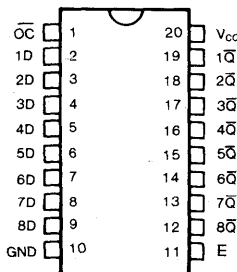
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24\text{mA}$  @  $V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### DESCRIPTION

The '563 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer register, I/O ports, bidirectional bus drivers and working registers.

The latches are transparent; when the enable (E) is high, the Q outputs follow complements of the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal (OC) which places the outputs at a high-impedance stage when it is taken high. The OC signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

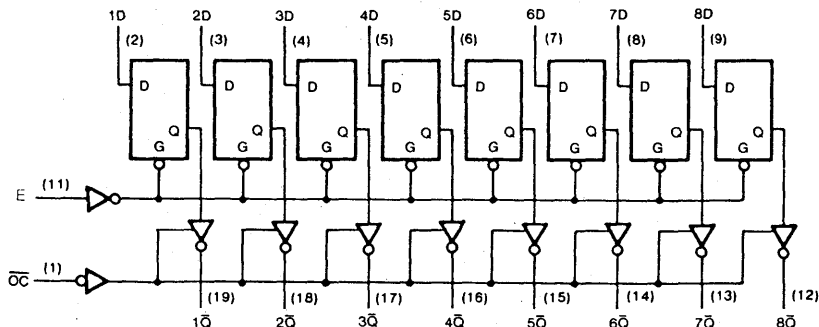
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	E	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

### LOGIC DIAGRAM





### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 70$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 250$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	-65°C to +150°C
Power Dissipation Per Package, $P_d$ † . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range . . . . .	KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$ . . . . .	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS563

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ		Guaranteed Limits					
Maximum Propagation Delay, D to $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	14	18	23	27	23	27	ns	
		$C_L = 150\text{pF}$	17	21	28	33	28	33		
	$t_{PHL}$	$C_L = 50\text{pF}$	14	18	23	27	23	27	ns	
		$C_L = 150\text{pF}$	17	21	28	33	28	33		
Maximum Propagation Delay E to $\bar{Q}$	$t_{PLH}$	$C = 50\text{pF}$	22	30	37	45	37	45	ns	
		$C_L = 150\text{pF}$	25	33	42	51	42	51		
	$t_{PHL}$	$C_L = 50\text{pF}$	22	30	37	45	37	45	ns	
		$C_L = 150\text{pF}$	25	33	42	51	42	51		
Maximum Output Enable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40	48	40	48	ns
			$C_L = 150\text{pF}$	27	35	45	54	45	54	
	$t_{PZL}$	$C_L = 50\text{pF}$	24	32	40	48	40	48		
		$C_L = 150\text{pF}$	27	35	45	54	45	54		
Maximum Output Disable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	19	25	31	37	31	37	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	19	25	31	37	31	37		
Minimum Pulse Width, E High	$t_w$		9	13	15	18	15	18	ns	
Minimum Setup Time, D before E†	$t_{su}$		6	8	10	10	10	10	ns	
Minimum Hold Time, D after E†	$t_h$		6	10	12	15	12	15	ns	
Maximum Input Capacitance	$C_{IN}$		5						pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{OC} = V_{CC}$	5						pF	
		$\bar{OC} = \text{GND}$	30							

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

The '564 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus driver and working registers.

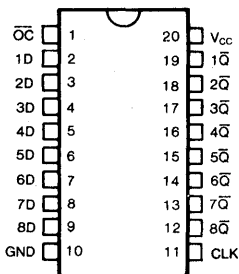
The flip-flops are edge-triggered: on the positive transition of the clock, the  $\bar{Q}$  outputs are set to the complement of the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at high impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

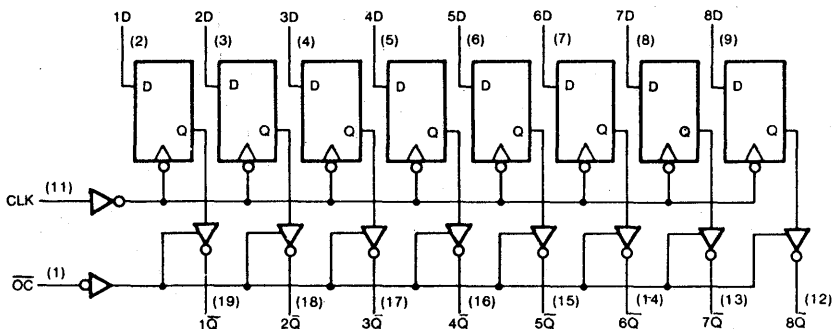


## FUNCTION TABLE

(Each Flip-Flop)

Inputs			Output
$\overline{OC}$	CLK	D	$\bar{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$Q_0$
H	X	X	Z

## LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
Operating Temperature  
Range . . . . . KS74HCTLS: -40°C to +85°C  
. . . . . KS54HCTLS: -55°C to +125°C  
Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS564

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit	
			Typ		Guaranteed Limits					
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	45	35	30		25		MHz	
Maximum Propagation Delay, CLK to any $\bar{Q}$	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48		ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48			
Maximum Output Enable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48		ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40		42 48		
Maximum Output Disable Time, $\bar{OC}$ to any $\bar{Q}$	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	19	25	31		37		ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	19	25	31		37			
Minimum Pulse Width, CLK High or Low	$t_w$		9	12	15		18		ns	
Minimum Setup Time, D before CLK <sup>†</sup>	$t_{su}$		10	13	17		20		ns	
Minimum Hold Time, D after CLK <sup>†</sup>	$t_h$		-3	0	0		0		ns	
Maximum Input Capacitance	$C_{IN}$		5						pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{OC} = V_{CC}$	5						pF	
		$\bar{OC} = \text{GND}$	30							

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- 8 latches in a single package
- Full parallel access for loading
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54HACT:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

The '573 consists of 8 high-speed D-type latches coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

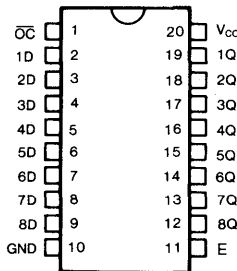
The latches are transparent: when the enable (E) is high, the Q outputs follow the data (D) inputs. When the enable is low, the outputs latch at the levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the latches. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATION

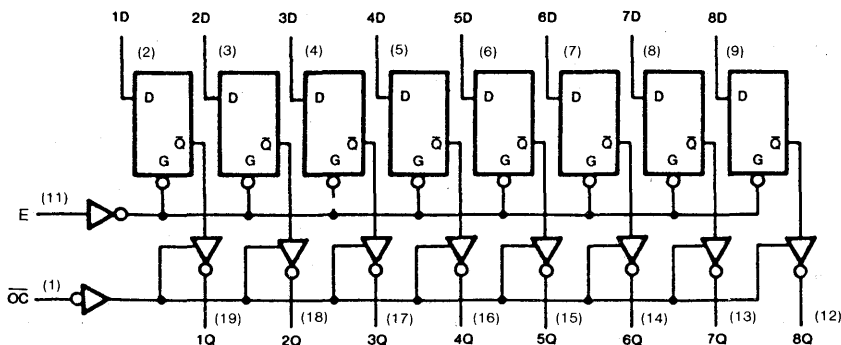


### FUNCTION TABLE

(Each Latch)

Inputs			Output
$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

### LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ <sup>†</sup> . . . . . 500 mW

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ C$ to $+85^\circ C$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS573

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit		
			Typ		Guaranteed Limits						
Maximum Propagation Delay, D to Q	$t_{PLH}$	$C_L = 50\text{pF}$	14	18	23		27		ns		
		$C_L = 150\text{pF}$	17	21	28		33				
	$t_{PHL}$	$C_L = 50\text{pF}$	14	18	23		27		ns		
		$C_L = 150\text{pF}$	17	21	28		33				
Maximum Propagation Delay E to Q	$t_{PLH}$	$C = 50\text{pF}$	22	30	37		45		ns		
		$C_L = 150\text{pF}$	25	33	42		51				
	$t_{PHL}$	$C_L = 50\text{pF}$	22	30	37		45		ns		
		$C_L = 150\text{pF}$	25	33	42		51				
Maximum Output Enable Time, $\overline{OC}$ to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40		48		ns	
			$C_L = 150\text{pF}$	27	35	45		54			
	$t_{PZL}$	$C_L = 50\text{pF}$	24	32	40		48				
		$C_L = 150\text{pF}$	27	35	45		54				
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	19	25	31		37		ns		
	$t_{PLZ}$	$C_L = 50\text{pF}$	19	25	31		37				
Minimum Pulse Width, E High	$t_w$		9	12	15		18		ns		
Minimum Setup Time, D before E↓	$t_{su}$		6	8	10		12		ns		
Minimum Hold Time, D after E↓	$t_h$		6	10	12		15		ns		
Maximum Input Capacitance	$C_{IN}$		5						pF		
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF		
Power Dissipation Capacitance*	$C_{PD}$	$\overline{OC} = V_{CC}$ (per stage)	5						pF		
		$\overline{OC} = \text{GND}$	30								

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



## FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

The '574 consists of 8 high-speed D-type edge-triggered flip-flops coupled to 3-state output buffers with high drive current capability. It can be used in implementing buffer registers, I/O ports, bidirectional bus drivers and working registers.

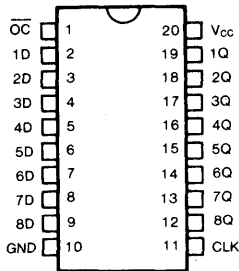
The flip-flops are edge-triggered on the positive transition of the clock. The Q outputs are set to the logic levels that were set up at the D inputs.

The output buffers are controlled by a common signal ( $\overline{OC}$ ) which places the outputs at a high-impedance state when it is taken high. The  $\overline{OC}$  signal does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

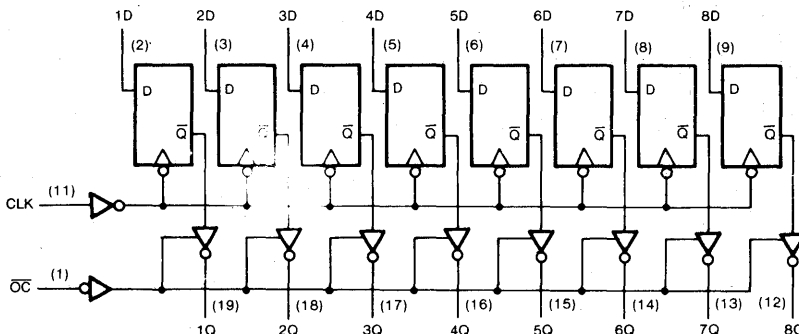


## FUNCTION TABLE

(Each Flip-Flop)

Inputs		Output	
$\overline{OC}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	$Q_0$
H	X	X	Z

## LOGIC DIAGRAM



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$	
( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$	
( $-0.5V < V_O < V_{CC} + 0.5V$ )	$\pm 70$ mA
Continuous Current Through $V_{CC}$ or GND pins	$\pm 250$ mA
Storage Temperature Range, $T_{stg}$	-65°C to +150°C
Power Dissipation Per Package, $P_d$ †	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$	0V to $V_{CC}$
Operating Temperature Range	
KS74HCTLS:	-40°C to +85°C
KS54HCTLS:	-55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS574

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit		
			Typ		Guaranteed Limits						
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	45	35	30		25		MHz		
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	21	28	35		42		ns		
		$C_L = 150\text{pF}$	24	31	40		48				
	$t_{PHL}$	$C_L = 50\text{pF}$	21	28	35		42		ns		
		$C_L = 150\text{pF}$	24	31	40		48				
Maximum Output Enable Time, $\overline{OC}$ to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	21	28	35		42		ns	
			$C_L = 150\text{pF}$	24	31	40		48			
	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	21	28	35		42		ns	
			$C_L = 150\text{pF}$	24	31	40		48			
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	19	25	31		37		ns		
			$t_{PLZ}$	19	25	31		37			
Minimum Pulse Width, CLK High or Low	$t_w$		9	12	15		18		ns		
Minimum Setup Time, D before CLK†	$t_{su}$		10	13	17		20		ns		
Minimum Hold Time, D after CLK†	$t_h$		-3	0	0		0		ns		
Maximum Input Capacitance	$C_{IN}$		5						pF		
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF		
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5						pF		
		$\overline{OC} = \text{GND}$	30								

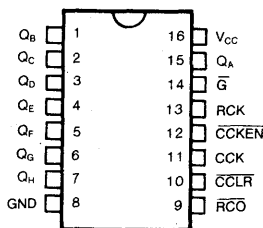
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Choice of 3-State ('590) and Open-Drain ('591) Outputs
- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs**  
( $I_{OL} = 24\text{mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
KS74HCTL5:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTL5:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATION



### DESCRIPTION

These devices each consist of an 8-bit counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out,  $\overline{\text{RCO}}$ , will go low. This enables either synchronous cascading of the counters by connecting the  $\overline{\text{RCO}}$  of the first stage to the  $\overline{\text{CCKEN}}$  of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the  $\overline{\text{RCO}}$  of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, G, is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLE

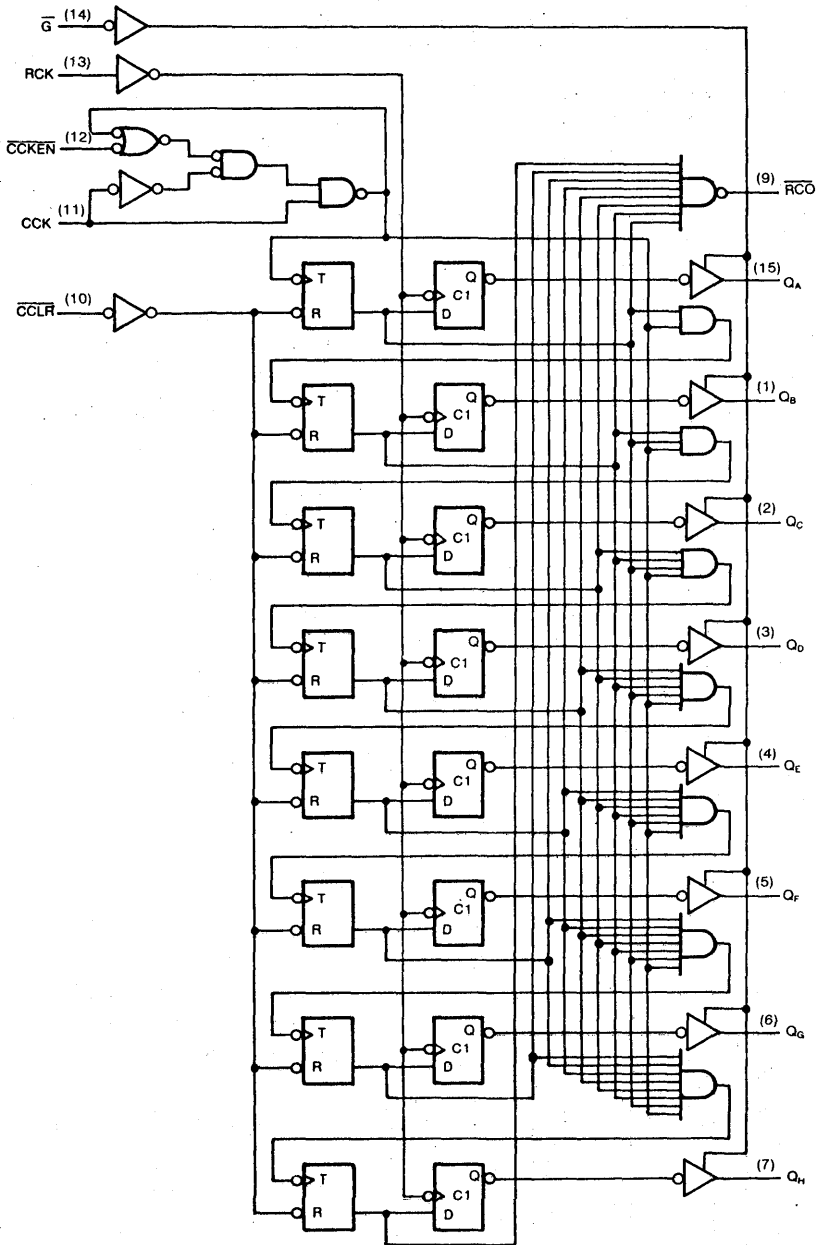
INPUTS					FUNCTION
$\overline{\text{G}}$	RCK	CCLR	CCKEN	CCK	
H	X	X	X	X	Q Outputs disable
L	X	X	X	X	Q Outputs enable
L		X	X	X	Counter data is stored into register
L		X	X	X	Register state is not changed
L	X	L	X	X	Counter clear
L	X	H	L		Advance one count
L	X	H	L		No count
L	X	H	H	X	No count

X: Don't care

$$\text{RCO} = \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D} \cdot \overline{Q_E} \cdot \overline{Q_F} \cdot \overline{Q_G} \cdot \overline{Q_H}$$

( $Q_A \sim Q_H$ : Internal outputs of the counter)

**LOGIC DIAGRAM**



## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ..... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '590 Outputs and '591 RCO Outputs)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS590

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	$f_{max}$		35	25	20	20	ns
Maximum Propagation Delay, CCK↑ to $\overline{RCO}$	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40	48	ns
	$t_{PHL}$		24	32	40	48	
Maximum Propagation Delay, $\overline{CCLR}\downarrow$ to $\overline{RCO}$	$t_{PLH}$		26	35	44	52	ns
Maximum Propagation Delay, RCK↑ to Q	$t_{PLH}$		16	21	26	31	ns
	$t_{PHL}$	16	21	26	31		
Maximum Output Enable Time, $\overline{G}\downarrow$ to Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$	18	24	30	36	ns
	$t_{PZL}$		18	24	30	36	
Maximum Output Disable Time, $\overline{G}\uparrow$ to Q	$t_{PHZ}$		18	24	30	36	ns
	$t_{PLZ}$		18	24	30	36	
Minimum Pulse Width	CCK or RCK High or Low	$t_w$	12	16	20	24	ns
			$\overline{CCLR}$ Low	12	16	20	
Minimum Setup Time	$\overline{CCKEN}\downarrow$ before CCK↑	$t_{su}$	12	16	20	24	ns
	$\overline{CCLR}\uparrow$ before CCK↑		12	16	20	24	
	CCK↑ to RCK↑↑↑		24	32	40	48	
Maximum Input Capacitance	$C_{IN}$		5				pF
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f < 6$ ns, HCTLS591)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	$f_{max}$		35	25	20	20	ns
Maximum Propagation Delay, CCK↑ to RCO	$t_{PLH}$	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$	24	32	40	48	ns
	$t_{PHL}$		24	32	40	48	
Maximum Propagation Delay, CCLR↓ to RCO	$t_{PLH}$		26	35	44	52	ns
Maximum Propagation Delay, RCK↑ to Q	$t_{PLH}$		27	37	46	55	ns
	$t_{PHL}$		16	21	26	31	
Maximum Output Enable Time, $\bar{G}$ ↓ to Q	$t_{pZL}$			18	24	30	36
Maximum Output Disable Time, $\bar{G}$ ↑ to Q	$t_{pLZ}$		18	24	30	36	ns
Minimum Pulse Duration	CCK or RCK High or Low	$t_w$	12	16	20	24	ns
	CCLR Low		12	16	20	24	
Minimum Setup Time	CCKEN↓ before CCK↑	$t_{su}$	12	16	20	24	ns
	CCLR↑ before CCK↑		12	16	20	24	
	CCK↑ to RCK↑††		24	32	40	48	
Maximum Input Capacitance	$C_{IN}$		5				pF
Maximum Output Capacitance	$C_{OUT}$	Output Disabled					pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

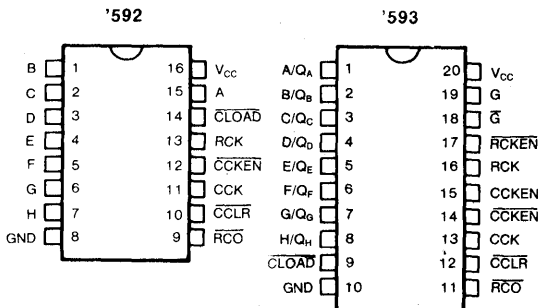
†† The clocks may be tied together, in which case the register state will be one clock pulse behind the counter.



## FEATURES

- Parallel Register Inputs ('592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('593)
- Counter Has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTL5: -40°C to +85°C  
KS54HCTL5: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATIONS



## DESCRIPTION

The '592 and '593 both contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out, RCO, will go low. This enables either synchronous cascading of the counters by connecting the RCO of the first stage to the CCKEN of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, CLOAD, input is taken low.

The '592 differs from the '593 in that the latter device has bidirectional input/output pins. The 3-state outputs of the counter can be enabled and are active when enable input,  $\bar{G}$ , is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The '593 also has a second clock enable pin, CCKEN, which is active high and it also has an active low register clock enable, RCKEN.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

## FUNCTION TABLE

INPUTS ('592)					FUNCTION
RCK	CLOAD	CCLR	CCKEN	CCK	
X	L	H	X	X	Register data is loaded into counter
X	H	L	X	X	Counter clear
	H	H	X	X	The data of a thru H inputs is stored into register
	H	H	X	X	Register state is not changed
X	H	H	L		Counter advances the count
X	H	H	L		No count
X	H	H	H	X	No count

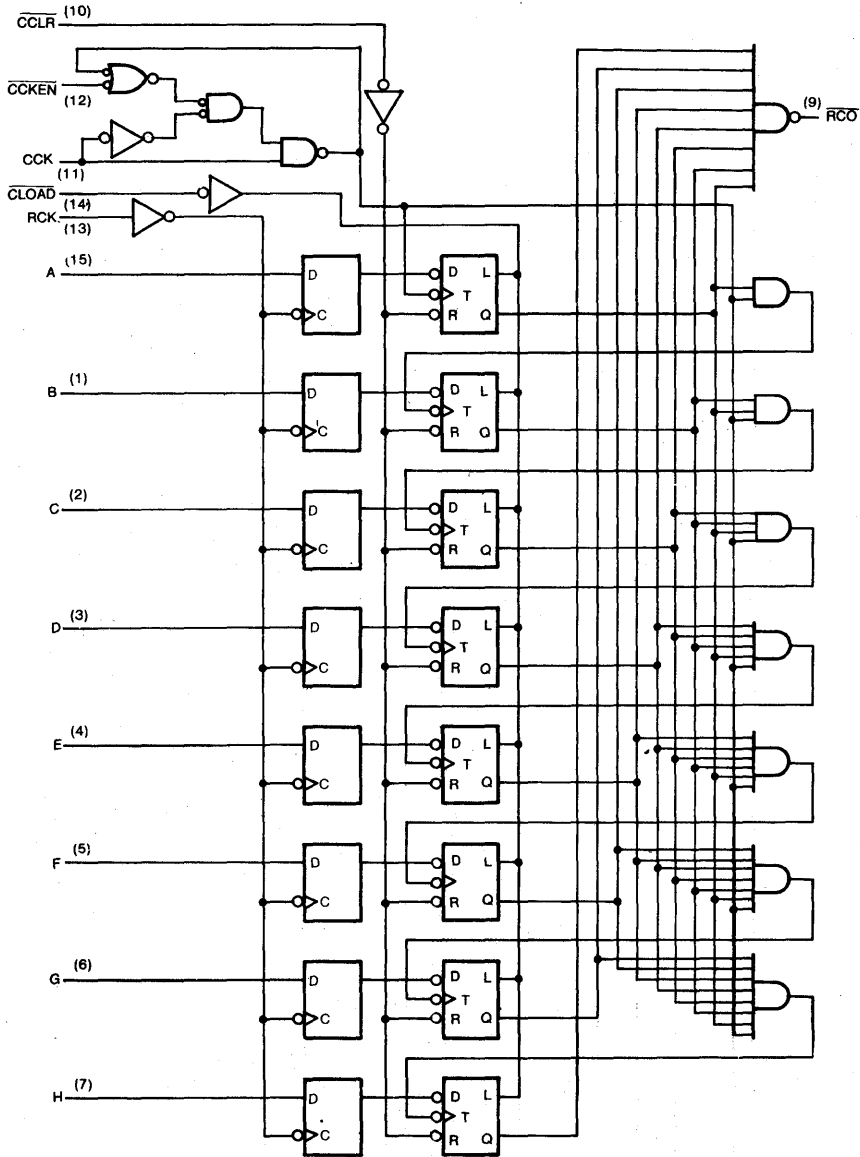
X: Don't care

$$RCO = Q_A' \cdot Q_B' \cdot Q_C' \cdot Q_D' \cdot Q_E' \cdot Q_F' \cdot Q_G' \cdot Q_H'$$

(Q<sub>A</sub>' ~ Q<sub>H</sub>': Internal outputs of the counter)

LOGIC DIAGRAMS

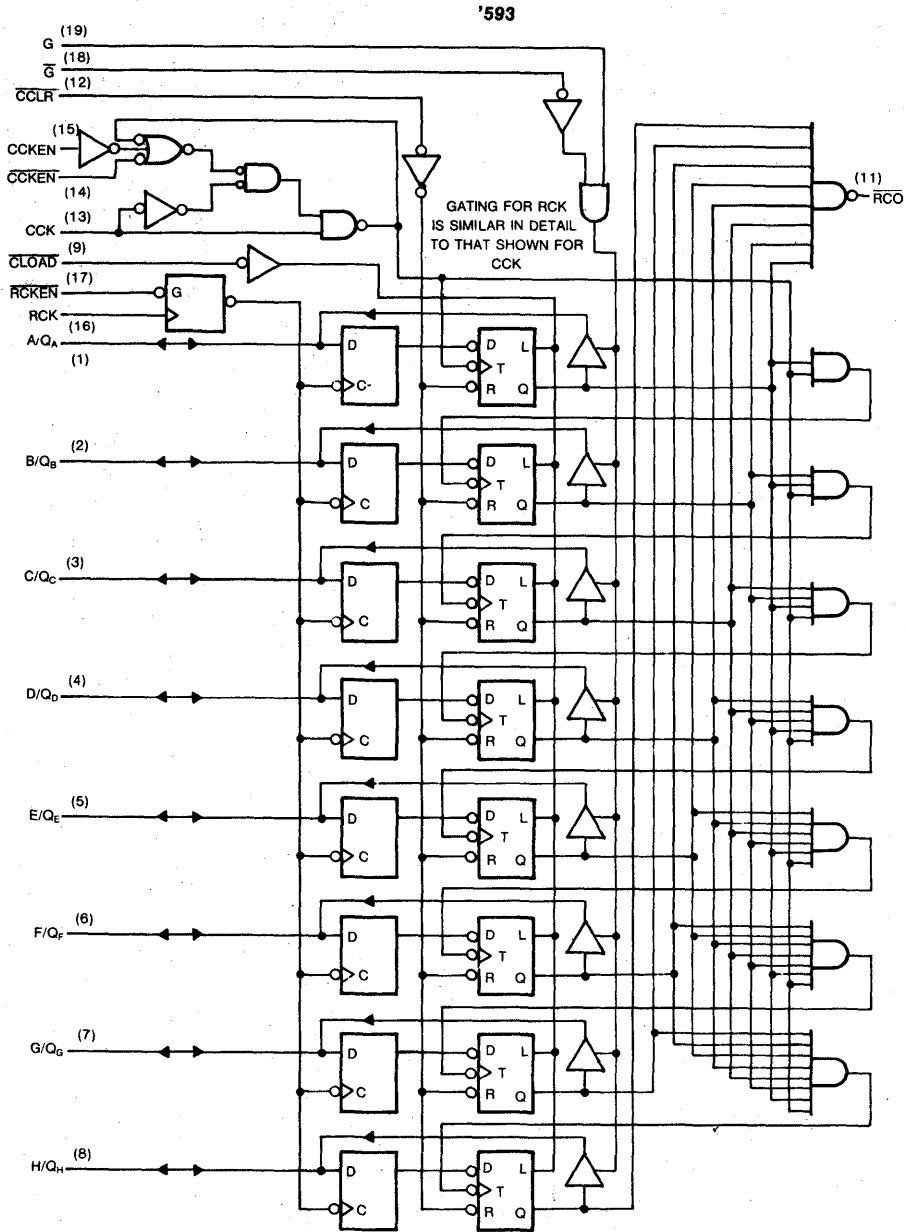
'592



# KS54HCTLS 592/593

# 8-Bit Binary Counters with Input Registers

## LOGIC DIAGRAMS (Continued)



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , .....	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....	$\pm 70$ mA
Continuous Current Through $V_{CC}$ or GND pins .....	$\pm 250$ mA
Storage Temperature Range, $T_{stg}$ .....	-65°C to +150°C
Power Dissipation Per Package, $P_d$ † .....	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ .....	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}, V_{OUT}$ ..	0V to $V_{CC}$
Operating Temperature Range	KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r, t_f$ .....	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input  $t_r, t_f \leq 2$  ns), HCTLS592

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	$f_{max}$		35	25	20	20	MHz
Maximum Propagation Delay, CCK↑ to RCO	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40	48	ns
	$t_{PHL}$		24	32	40	48	
Maximum Propagation Delay, CLOAD↓ to RCO	$t_{PLH}$		24	32	40	48	ns
	$t_{PHL}$		24	32	40	48	
Maximum Propagation Delay, CCLR↑ to RCO	$t_{PHL}$	$C_L = 50\text{pF}$ CLOAD=GND	24	32	40	48	ns
	$t_{PLH}$		26	35	44	52	
Maximum Propagation Delay, RCK↑ to RCO	$t_{PHL}$		26	35	44	52	ns
	$t_{PLH}$		26	35	44	52	
Minimum Pulse Width	CCK or RCK High or Low	$t_w$	12	16	20	24	ns
	CCLR Low		12	16	20	24	
	CLOAD Low		12	16	20	24	
Minimum Setup Time	CCKEN↓ before CCK↑	$t_{su}$	12	16	20	24	ns
	CCLR↑ before CCK↑		12	16	20	24	
	RCK↑ before CLOAD↑↑		24	32	40	48	
	Data A-H↑ before RCK↑		12	16	20	24	
Minimum Hold Time	$t_h$		0	0	0	0	ns
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to CLOAD setup time ensures that the counter will see stable data from the register output.

## AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS593

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Clock Frequency	$f_{max}$		35	25	20		20		MHz
Maximum Propagation Delay, CCK $\uparrow$ to Q	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40		48		ns
		$C_L = 150\text{pF}$	27	35	45		54		
Maximum Propagation Delay, CCK $\uparrow$ to $\overline{RCO}$	$t_{PHL}$	$C_L = 50\text{pF}$	24	32	40		48		ns
		$C_L = 150\text{pF}$	27	35	45		54		
Maximum Propagation Delay, CLOAD $\downarrow$ to Q	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40		48		ns
		$C_L = 150\text{pF}$	27	35	45		54		
Maximum Propagation Delay, CLOAD $\downarrow$ to $\overline{RCO}$	$t_{PHL}$	$C_L = 50\text{pF}$	24	32	40		48		ns
		$C_L = 150\text{pF}$	27	35	45		54		
Maximum Propagation Delay, RCK $\uparrow$ to $\overline{RCO}$	$t_{PLH}$	$C_L = 50\text{pF}$	26	35	44		52		ns
		CLOAD=GND	26	35	44		52		
Maximum Propagation Delay, $\overline{CCLR}$ $\uparrow$ to Q	$t_{PHL}$	$C_L = 50\text{pF}$	24	32	40		48		ns
		$C_L = 150\text{pF}$	27	35	45		54		
Maximum Propagation Delay, CCLR $\uparrow$ to $\overline{RCO}$	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40		48		ns
		$C_L = 150\text{pF}$	27	35	45		54		
Maximum Enable Time, G $\uparrow$ or $\overline{G}$ $\downarrow$ to Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	21	28	39		42	ns
			$C_L = 150\text{pF}$	24	31	44		48	
	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	21	28	35		42	ns
			$C_L = 150\text{pF}$	24	31	44		48	
Maximum Disable Time G $\uparrow$ or G $\downarrow$ to Q	$t_{PLH}$	$R_L = 1\text{k}\Omega$	24	28	35		42	ns	
	$t_{PZL}$	$C_L = 50\text{pF}$	21	28	35		42		
Minimum Pulse Width	$t_w$	CCK or RCK High or Low		12	16	20		24	ns
		$\overline{CCLR}$ Low		12	16	20		24	
		CLOAD Low		12	16	20		24	
Minimum Setup Time	$t_{su}$	CCKEN $\downarrow$ before CCK $\uparrow$		12	16	20		24	ns
		RCKEN $\downarrow$ to RCK $\uparrow$			12	16		24	
		$\overline{CCLR}$ $\uparrow$ before CCK $\uparrow$		12	16	20		24	
		RCK $\uparrow$ before CLOAD $\uparrow$		24	32	40		48	
		Data A-H before RCK $\uparrow$		12	16	20		24	
Hold Time	$t_h$		0	0	0		0	ns	
Maximum Input Capacitance	$C_{IN}$		5					pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10	10				pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> The RCK $\uparrow$  to  $\overline{CLOAD}$  setup time ensures that the counter will see stable data from the register output.

## FEATURES

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs
- Shift Register Has Direct Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## DESCRIPTION

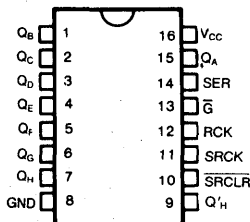
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or open-drain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION

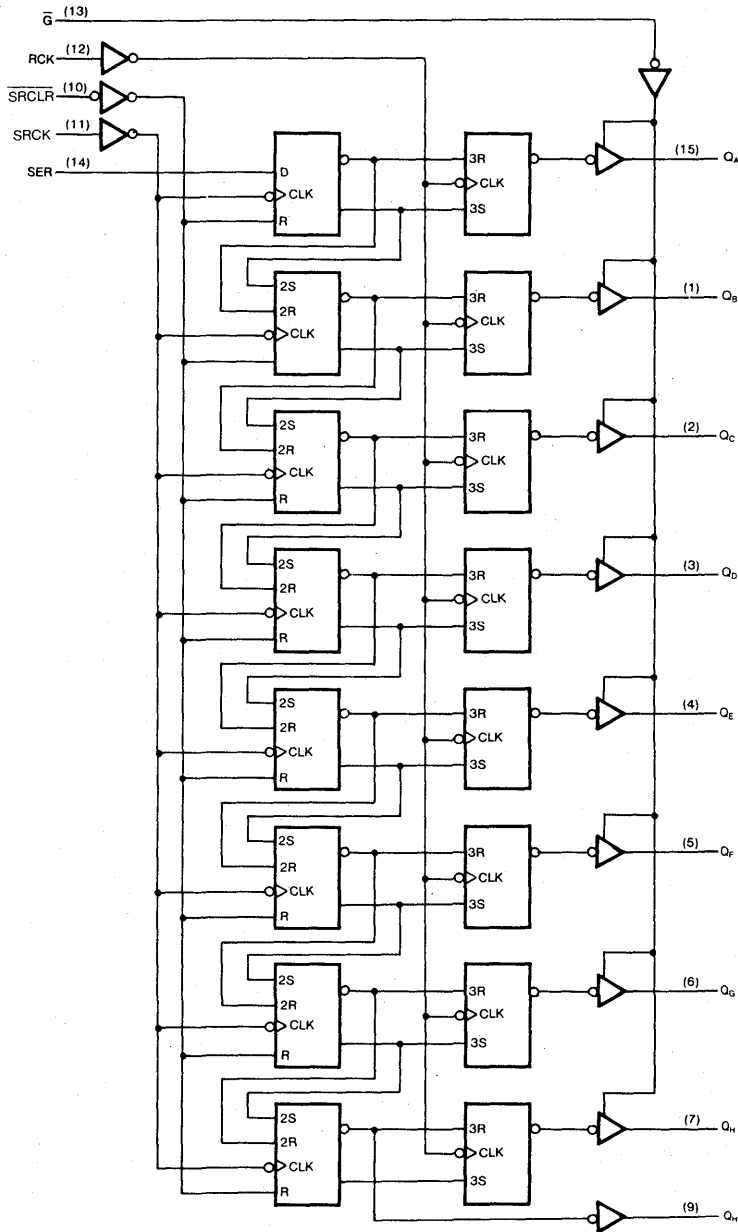


## FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCK	SRCLR	RCK	$\bar{G}$	
X	X	X	X	H	$Q_A$ thru $Q_H$ outputs disable
X	X	X	X	L	$Q_A$ thru $Q_H$ outputs enable
X	X	L	X	X	Shift register is cleared.
L		H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H		H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X		H	X	X	State of S.R. is not changed.
X	X	X		X	S.R. data is stored into storage register.
X	X	X		X	Storage register state is not changed.

X: DON'T CARE

**LOGIC DIAGRAM**





## Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  .....  $-0.5V$  to  $+7V$   
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ C$  to  $+150^\circ C$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

## Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '595 Outputs and '596 Q <sub>H</sub> Output)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu A$
Maximum Output Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0			$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS595, HCTLS596

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit		
			Typ		Guaranteed Limits						
Maximum Propagation Delay, SRCK† to Q <sub>H</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15	18	25	30			ns		
	t <sub>PHL</sub>		15	18	25	30					
Maximum Propagation Delay, RCK† to Q <sub>A</sub> thru Q <sub>H</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	17	22	28	33			ns		
		C <sub>L</sub> = 150pF	20	25	33	39					
	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	17	22	28	33					
		C <sub>L</sub> = 150pF	20	25	33	39					
Maximum Output Enable Time, $\bar{G}$ † to Q <sub>A</sub> thru Q <sub>H</sub> ('595 only)	t <sub>PZH</sub>	R <sub>L</sub> = 1kΩ	C <sub>L</sub> = 50pF	18	24	30	36			ns	
			C <sub>L</sub> = 150pF	21	27	35	42				
	t <sub>PZL</sub>	C <sub>L</sub> = 50pF	18	24	30	36					
		C <sub>L</sub> = 150pF	21	27	35	42					
Maximum Output Disable Time, $\bar{G}$ † to Q <sub>A</sub> thru Q <sub>H</sub> ('595 only)	t <sub>PHZ</sub>	R <sub>L</sub> = 1kΩ	18	24	30	36			ns		
			21	27	35	42					
	t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	18	24	30	36					
Maximum Propagation Delay, $\bar{G}$ † to Q <sub>A</sub> thru Q <sub>H</sub> ('596 only)	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	18	24	30	36			ns		
		C <sub>L</sub> = 150pF	21	27	35	42					
Maximum Propagation Delay, $\bar{G}$ † to Q <sub>A</sub> thru Q <sub>H</sub> ('596 only)	t <sub>PHL</sub>	C <sub>L</sub> = 50pF	18	24	30	36			ns		
		C <sub>L</sub> = 150pF	21	27	35	42					
Minimum Pulse Width	SRCK or RCK	t <sub>w</sub>	12	16	20	24			ns		
	SRCLR Low		12	16	20	24					
Minimum Setup Time	SRCLR† to SRCK†	t <sub>su</sub>	12	16	20	24			ns		
	SER to SRCK†		12	16	20	24					
	SRCK† to RCK††		24	32	40	48					
Minimum Hold Time	t <sub>h</sub>		-3	0	0	0			ns		
Maximum Input Capacitance	C <sub>IN</sub>		5						pF		
Maximum Output Capacitance	C <sub>OUT</sub>	Output Disabled	10						pF		
Power Dissipation Capacitance *	C <sub>PD</sub>								pF		

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the register output.

## FEATURES

- 8-Bit Parallel Storage Register Inputs
- shift Register has Direct Overriding Load and Clear
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTL5:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTL5:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

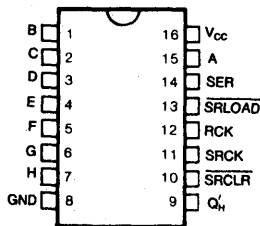
## DESCRIPTION

The '597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

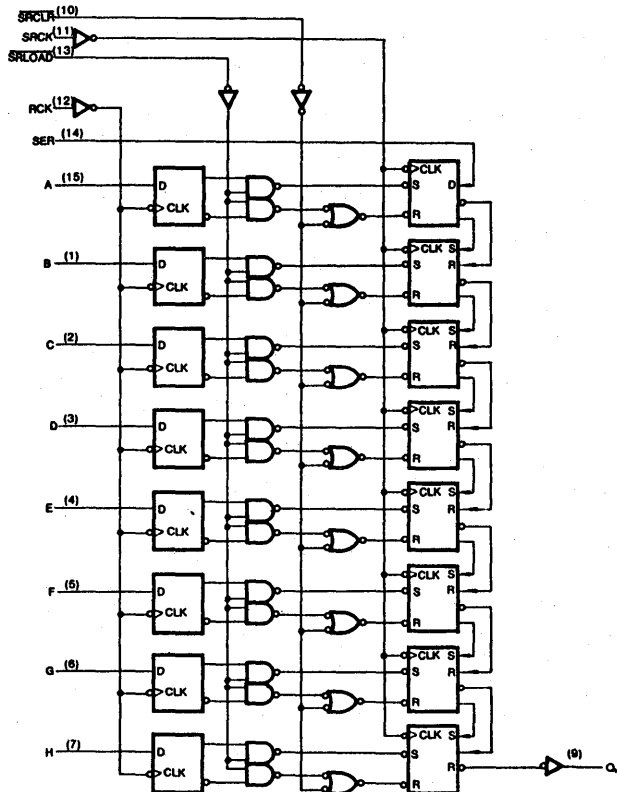
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

## PIN CONFIGURATION



## LOGIC DIAGRAM



**FUNCTION TABLE**

INPUTS					FUNCTION
SER	SRCK	SRCLR	SRLOAD	RCK	
X	X	L	H	X	S.R. is cleared to "L"
X	X	H	J	X	Input register data is stored into S.R.
L		H	H	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H		H	H	X	First stage of S.R. becomes "H". Other stages stores the data of previous stage, respectively.
X	X	X	X		State of S.R. is not changed.
X	X	X	X		Input data on A~H line is stored into input register
X	X	X	X		Storage register state is not changed.

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$		KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0		V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8		V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -4mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0		$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0		mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS597

Characteristic	Symbol	Conditions†	T <sub>a</sub> = 25°C V <sub>CC</sub> = 5.0V		KS74HCTLS	KS54HCTLS	Unit
					T <sub>a</sub> = -40°C to +85°C V <sub>CC</sub> = 5.0V ± 10%	T <sub>a</sub> = -55°C to +125°C V <sub>CC</sub> = 5.0V ± 10%	
			Typ	Guaranteed Limits			
Maximum Clock Frequency	f <sub>max</sub>		35	25	20	20	MHz
Maximum Propagation Delay, SRCK↑ to Q <sub>H</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF	15	18	25	30	ns
	t <sub>PHL</sub>		15	18	25	30	
Maximum Propagation Delay, SRLOAD↓ to Q <sub>H</sub>	t <sub>PLH</sub>		18	24	30	36	ns
	t <sub>PHL</sub>		18	24	30	36	
Maximum Propagation Delay, SRCLR↓ to Q <sub>H</sub>	t <sub>PHL</sub>		17	22	28	33	ns
Maximum Propagation Delay, RCK↑ to Q <sub>H</sub>	t <sub>PLH</sub>	C <sub>L</sub> = 50pF SLOAD = Low	21	29	35	42	ns
	t <sub>PHL</sub>		21	29	35	42	
Minimum Pulse Width	RCK or SRCK High or Low	t <sub>w</sub>	12	16	20	24	ns
	SRCLR or SRLOAD Low		12	16	20	24	
Minimum Setup Time	SRCLR↑ before SRCK↑	t <sub>su</sub>	12	16	20	24	ns
	RCK↑ before SRCK↑↑↑		24	32	40	48	
	SER before SRCK↑		12	16	20	24	
	A thru H before RCK↑		12	16	20	24	
Minimum Hold Time	t <sub>h</sub>		0	0	0	0	ns
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>in</sub>.

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ before SRCK↑ setup time ensures that shift register will see stable data coming from the register output.

**FEATURES**

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current**  
 (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**  
**KS74HCTLS: -40°C to +85°C**  
**KS54HCTLS: -55°C to +125°C**
- **Package options include "small outline" packages**  
 (Available Tape & Reel), standard DIPs.

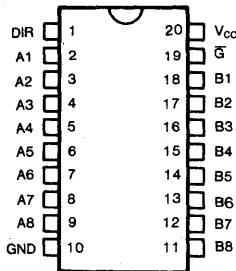
**DESCRIPTION**

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

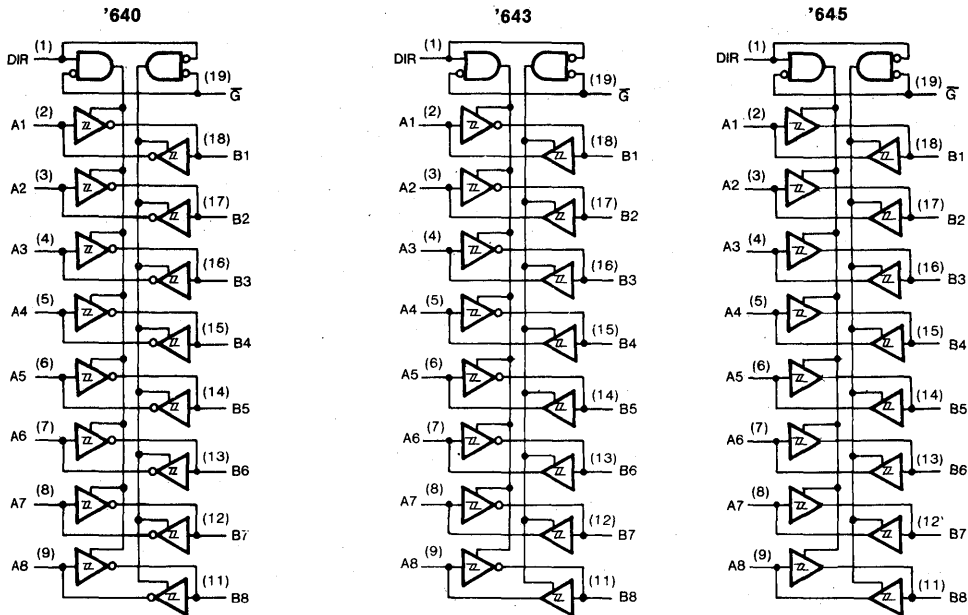
**PIN CONFIGURATION**



**FUNCTION TABLE**

Control Inputs		Operation		
$\bar{G}$	DIR	'640	'643	'645
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A
L	H	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B
H	X	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)

LOGIC DIAGRAMS



**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  . . . . .  $-0.5V$  to  $+7V$
- DC Input Diode Current,  $I_{IK}$   
 $(V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
 $(V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
 $(-0.5V < V_O < V_{CC} + 0.5V)$  . . . . .  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA
- Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ C$  to  $+150^\circ C$
- Power Dissipation Per Package,  $P_d^\dagger$  . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12mW/^\circ C$  from  $65^\circ C$  to  $85^\circ C$

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
- DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . 0V to  $V_{CC}$
- Operating Temperature  
 Range KS74HCTLS:  $-40^\circ C$  to  $+85^\circ C$   
 KS54HCTLS:  $-55^\circ C$  to  $+125^\circ C$
- Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	$V_{CC}-0.1$ 3.7	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 5.0$	$\pm 10.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	80.0	160.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	2.9	3.0	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS640, HCTLS643, HCTLS645)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay, A to B, or B to A	$t_{PLH}$	$C_L=50\text{pF}$ $C_L=150\text{pF}$	9	12	16	16	19	19	ns
	$t_{PHL}$	$C_L=50\text{pF}$ $C_L=150\text{pF}$	12	15	21	21	25	25	
Maximum Output Enable Time, $\bar{G}$ or DIR to A or B	$t_{PZH}$	$R_L=1\text{k}\Omega$ $C_L=50\text{pF}$ $C_L=150\text{pF}$	30	40	50	50	60	60	ns
	$t_{PZL}$		33	43	55	55	65	65	
Maximum Output Disable Time, $\bar{G}$ or DIR to A or B	$t_{PHZ}$	$R_L=1\text{k}\Omega$ $C_L=50\text{pF}$	20	27	34	34	40	40	ns
	$t_{PLZ}$		20	27	34	34	40	40	
Maximum Input Capacitance	$C_{IN}$		5						pF
Maximum Output Capacitance	$C_{OUT}$	Output disabled	10						pF
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\bar{G}=V_{CC}$ $\bar{G}=GND$	5						pF
			30						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f_{in}$ .

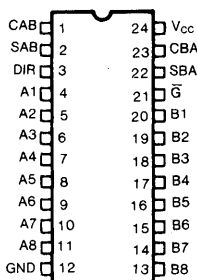
† For AC switching test circuits and timing waveforms see section 2.



## FEATURES

- 8 bi-directional data paths
- Transmits direct or stored data in either direction
- 24-pin 0.3" slim DIP package
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HACT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



## DESCRIPTION

The '646 and '648 are bi-directional bus transceivers with D-type flip-flops and control circuitry to facilitate high speed multiplexed data transmission. The '646 transmits true data and the '648 transmits inverted data.

Data can be transmitted directly from one port to the other in either direction. It also can be stored in the flip-flops from either or both ports for subsequent transmission to the opposite port. Six control inputs govern the data flow:

$\bar{G}$  (output enable) when high, all outputs are disabled, isolating the A and B ports. When low, one port is enabled at a time as determined by the DIR pin.

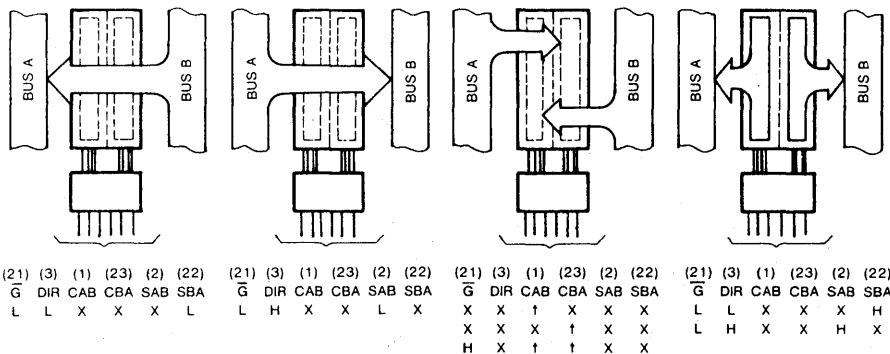
DIR (direction control) disables A or B outputs permitting the pins to be used as inputs thus determining the direction of a data flow. When DIR=high, data flows from A to B.

SAB, SBA (data source AB and BA) determines whether data transmitted is from the data inputs or the registers associated with those inputs.

CAB, CBA (Clock AB and BA) clocks data from the A inputs and the B inputs, respectively, into their associated registers. Since the clocks are not gated with the  $\bar{G}$  and DIR pins, data at the A and B pins can be clocked into the flip-flops at any time.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.



Real-Time transfer  
bus B to bus A

Real-Time transfer  
bus A to bus B

Storage from  
A AND/OR B

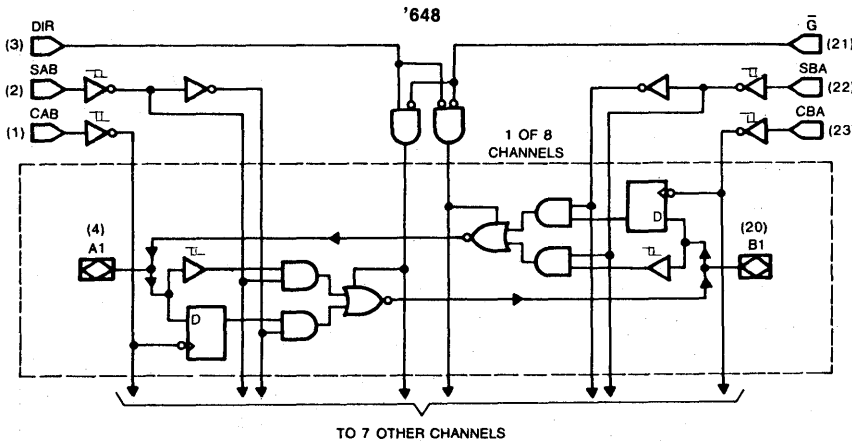
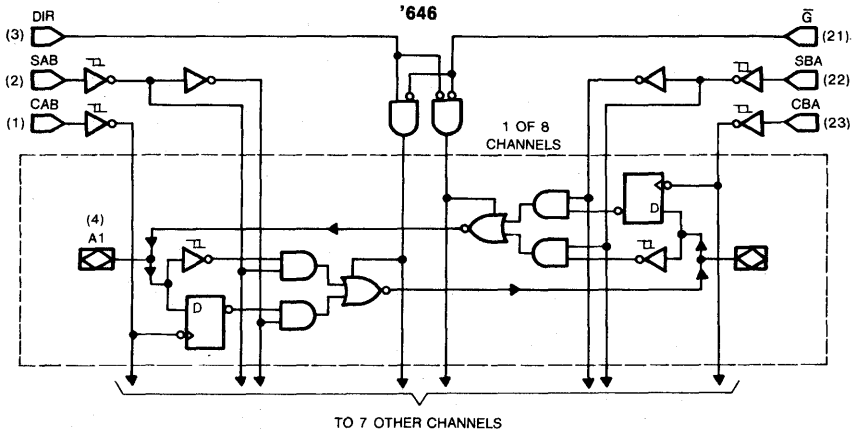
Transfer stored  
data to A AND/OR B

**FUNCTION TABLE**

Inputs						Data I/O*		Operation or Function	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'646	'648
X	X	↑	X	X	X	input	input	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Not specified	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B data isolation, hold storage	Store A and B data isolation, hold storage
H	X	H or L	H or L	X	X				
L	L	X	X	X	L	Output	Input	Real-Time B data to A bus	Real-Time $\bar{B}$ data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored $\bar{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-Time A data to B bus	Real-Time $\bar{A}$ data to B bus
L	H	H or L	X	H	X			Stored A data to B bus	Stored $\bar{A}$ data to B bus

\*The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

**LOGIC DIAGRAMS**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $= V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS646, HCTLS648

Characteristic	Symbol	Conditions <sup>1</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit		
			Typ		Guaranteed Limits						
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	30	25		20		MHz		
Maximum Propagation Delay, A or B Input to B or A Output	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14	19	24		29		ns		
			17	22	29		35				
Maximum Propagation Delay, CBA or CAB Input to A or B Output	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14	19	24		29		ns		
			17	22	29		35				
Maximum Propagation Delay, SBA or SAB Input to A or B Output	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	22	30	37		45		ns		
			25	33	42		51				
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	22	30	37		45		ns		
			25	33	42		51				
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	26	35	44		53		ns		
			29	38	49		59				
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	26	35	44		53		ns		
			29	38	49		59				
Maximum Output Enable Time, $\bar{G}$ or DIR Input to A or B Output	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	33	45	56		67	ns		
			$C_L = 150\text{pF}$	36	48	61		73			
Maximum Output Disable Time, $\bar{G}$ or DIR Input to A or B Output	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	33	45	56		67	ns		
			$C_L = 150\text{pF}$	36	48	61		73			
Maximum Output Disable Time, $\bar{G}$ or DIR Input to A or B Output	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	26	35	44		53	ns			
			$C_L = 50\text{pF}$	26	35	44			53		
Pulse Duration, Clocks High or Low	$t_w$		10	13	17		20	ns			
Setup Time, A before CAB <sup>†</sup> or B before CBA <sup>†</sup>	$t_{su}$		10	13	17		20	ns			
Hold Time, A after CAB <sup>†</sup> or B after CBA <sup>†</sup>	$t_h$		0	0			0	ns			
Maximum Input Capacitance	$C_{IN}$		5					pF			
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10					pF			
Power Dissipation Capacitance*	$C_{PD}$							pF			

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

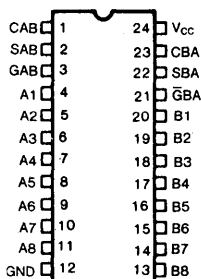
<sup>†</sup> For AC switching test circuits and timing waveforms see section 2.

<sup>††</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

## FEATURES

- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of Time and Inverting Data Paths
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATION



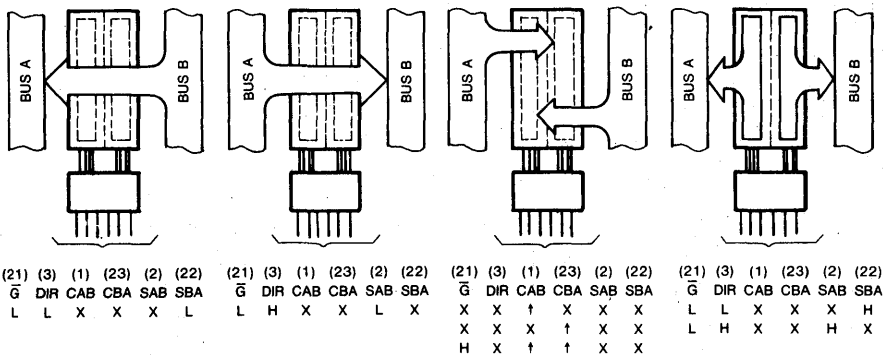
## DESCRIPTION

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and  $\bar{G}BA$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and  $\bar{G}BA$ . In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.



Real-Time transfer  
bus B to bus A

Real-Time transfer  
bus A to bus B

Storage from  
A AND/OR B

Transfer stored data  
to A and/or B

**FUNCTION TABLE**

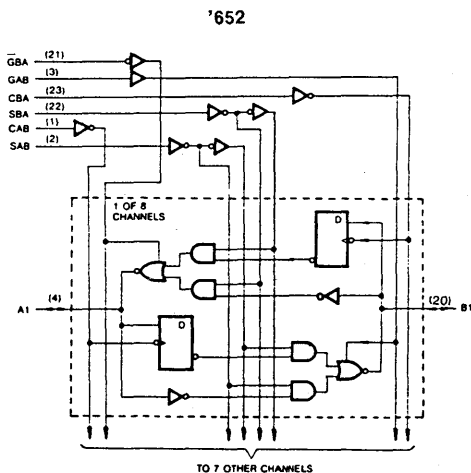
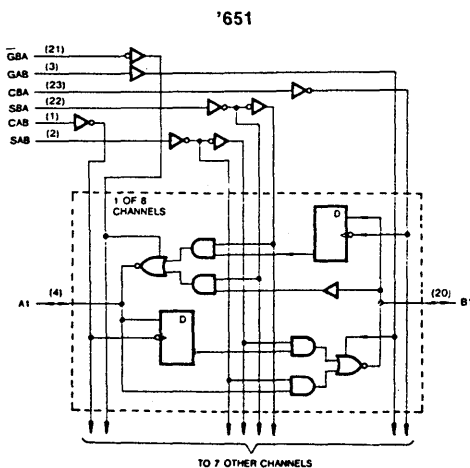
INPUTS				DATA I/O*		OPERATION OR FUNCTION		
GAB	GBA	CAB	CBA	SAB SBA	A1 THRU A8	B1 THRU B8	'651	'652
L	H	H or L	H or L	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L	H	↑	↑	X X	Input	Input	Store A, Hold B Store A in both registers	Store A Hold B Store A in both registers
X	H	↑	H or L	X X	Input	Not specified	Store A, Hold B Store A in both registers	Store A Hold B Store A in both registers
H	H	↑	↑	X** X	Input	Output*	Store A, Hold B Store A in both registers	Store A Hold B Store A in both registers
L	X	H or L	↑	X X	Not specified	Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers
L	L	↑	↑	X X**	Output*	Input	Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers
L	L	X	X	X L	Output	Input	Real-Time $\bar{B}$ Data to A Bus Stored $\bar{B}$ Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus
L	L	X	H or L	X H	Output	Input	Real-Time $\bar{B}$ Data to A Bus Stored $\bar{B}$ Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus
H	H	X	X	L X	Input	Output	Real-Time $\bar{A}$ Data to B Bus Stored $\bar{A}$ Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H	H	H or L	X	H X	Input	Output	Real-Time $\bar{A}$ Data to B Bus Stored $\bar{A}$ Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H H	Output	Output	Stored $\bar{A}$ Data to B Bus and Stored $\bar{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

\* The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

\*\* Select control=L: clocks can occur simultaneously

Select control=H: clocks must be staggered in order to load both registers

**LOGIC DIAGRAMS**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS651, HCTLS652

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Clock Frequency	$f_{\max}$	$C_L = 50\text{pF}$	40	30	25	20	20		MHz
Maximum Propagation Delay, A or B Input to B or A Output	$t_{PLH}$	$C_L = 50\text{pF}$	14	19	24	29	29		ns
		$C_L = 150\text{pF}$	17	22	29	35	35		
	$t_{PHL}$	$C_L = 50\text{pF}$	14	19	21	26	20		ns
		$C_L = 150\text{pF}$	17	22	26	32	26		
Maximum Propagation Delay, CBA or CAB Input to A or B Output	$t_{PLH}$	$C_L = 50\text{pF}$	22	30	37	42	45		ns
		$C_L = 150\text{pF}$	25	33	42	49	51		
	$t_{PHL}$	$C_L = 50\text{pF}$	22	30	37	42	45		ns
		$C_L = 150\text{pF}$	25	33	42	49	51		
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	$t_{PLH}$	$C_L = 50\text{pF}$	26	35	44	49	53		ns
		$C_L = 150\text{pF}$	29	38	49	56	59		
	$t_{PHL}$	$C_L = 50\text{pF}$	26	35	44	49	53		ns
		$C_L = 150\text{pF}$	29	38	49	56	59		
Maximum Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	$t_{PLH}$	$C_L = 50\text{pF}$	26	35	44	49	53		ns
		$C_L = 150\text{pF}$	29	38	49	56	59		
	$t_{PHL}$	$C_L = 50\text{pF}$	26	35	44	49	53		ns
		$C_L = 150\text{pF}$	29	38	49	56	59		
Maximum Output Enable Time, $\bar{G}BA$ to A or $\bar{G}AB$ to B	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	33	45	56	67		ns
			$C_L = 150\text{pF}$	39	48	61	73		
	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	33	45	56	67		ns
			$C_L = 150\text{pF}$	39	48	61	73		
Maximum Output Disable Time, $\bar{G}BA$ to A or $\bar{G}AB$ to B	$t_{PHZ}$	$R_L = 1\text{k}\Omega$		26	35	44	53		ns
			$C_L = 50\text{pF}$						
Minimum Pulse Width Clocks High or Low	$t_w$		10	13	17	20		ns	
Minimum Setup Time, A before $\bar{C}AB\uparrow$ or B before $\bar{C}BA\uparrow$	$t_{su}$		10	13	17	20		ns	
Minimum Hold Time, A after $\bar{C}AB\uparrow$ or B after $\bar{C}BA\uparrow$	$t_h$		0	0	0	0		ns	
Maximum Input Capacitance	$C_{IN}$		5					pF	
Maximum Output Capacitance	$C_{OUT}$	Output Disabled		10				pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

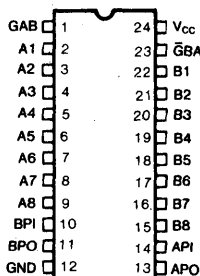
† For AC switching test circuits and timing waveforms see section 2.



**FEATURES**

- Bus Transceivers with Inverting Outputs ('658) or True Outputs ('659)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTL5: -40°C to +85°C  
KS54HCTL5: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus, or from the B Bus to the A Bus, depending on the levels at the direction control inputs, GAB and GBA. These devices also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuits on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuits.

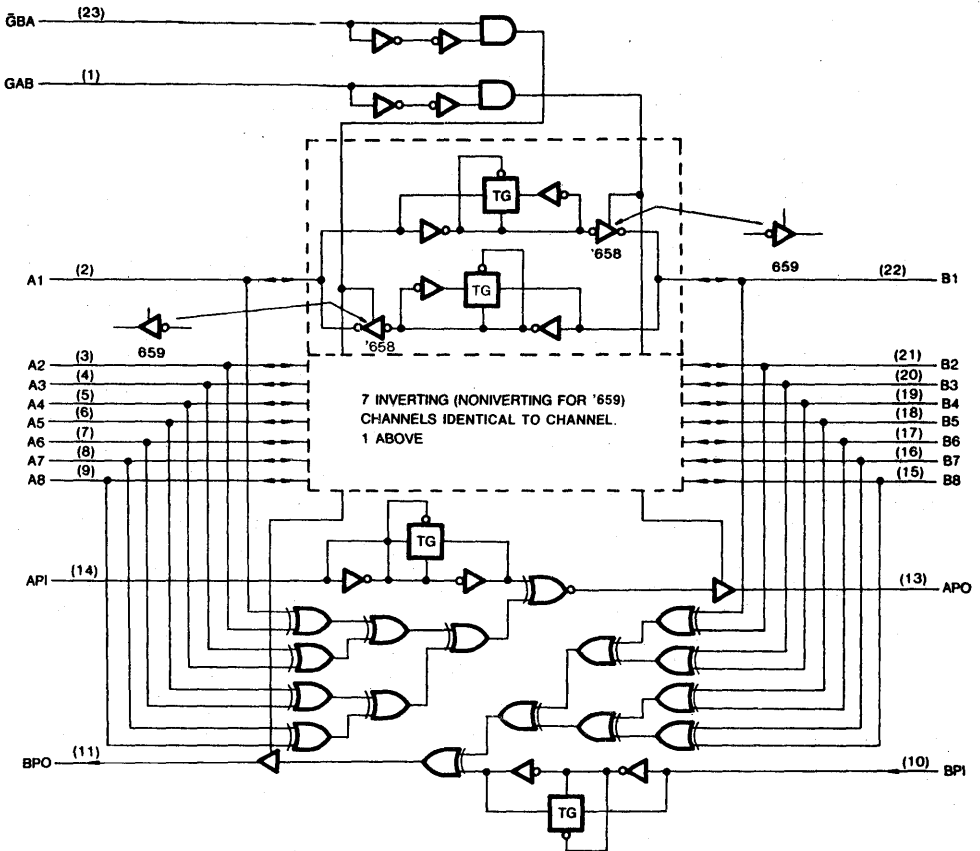
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**FUNCTION TABLE**

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
GBA	GAB			APO	BPO	HCTL5658	HCTL5659
L	L	X	0, 2, 4, 6, 8	Z	H	B Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
H	H	0, 2, 4, 6, 8	X	H	Z	A Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	L	X	X	Z	Z	Isolation	Isolation
L	H	X	0, 2, 4, 6, 8		H	B̄ Data to A Bus, Ā Data to B Bus	B Data to A Bus, A Data to B Bus
		X	1, 3, 5, 7, 9		L		
		0, 2, 4, 6, 8	X		H		
		1, 3, 5, 7, 9	X		L		

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$				Unit
			KS74HCTLS		KS54HCTLS		
			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$		
			Guaranteed Limits				
			Typ				
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f < 6$  ns), HCTLS658, HCTLS659

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, A or B to B or A	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39	ns		
			23	28	35	45			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39	ns		
			23	28	35	45			
Maximum Propagation Delay, A or B to B or A	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	24	32	40	48	ns		
			27	35	45	54			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	24	32	40	48	ns		
			27	35	45	54			
Maximum Propagation Delay A or B to APO or BPO	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39	ns		
			23	28	35	45			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39	ns		
			23	28	35	45			
Maximum Enable Time, GAB or $\bar{G}BA$ to APO or BPO	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	20	25	30	39	ns	
			$C_L = 150\text{pF}$	23	28	35	45		
	$t_{PZL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39			
			23	28	35	45			
Maximum Disable Time, GAB or $\bar{G}BA$ to APO or BPO	$t_{PLZ}$	$R_L = 1\text{k}\Omega$	20	25	30	39	ns		
			$t_{PHZ}$	$C_L = 50\text{pF}$	20	25		30	39
Maximum Input Capacitance	$C_{IN}$		5				pF		
Maximum Output Capacitance	$C_{OUT}$						pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

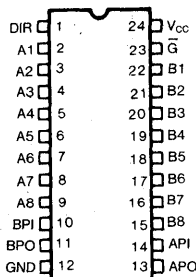
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Bus Transceivers with Inverting Outputs ('664) or True Outputs ('665)
- Generates a Parity Bit for A Bus and B Bus
- Easily Cascadable
- Internal Active Pull-Ups and Pull-Downs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**DESCRIPTION**

These octal bus transceivers are designed for asynchronous, bidirectional communication between data buses. The devices transmit data from the A Bus to the B Bus or from the B Bus to the A Bus, depending on the level at the direction control input, DIR. The enable input,  $\bar{G}$  can be used to disable the device so that the buses are isolated. These devices will also generate parity outputs, APO and BPO, which reflect the number of high levels at the A Bus and B Bus, respectively, taking into account the parity inputs API and BPI.

The bidirectional I/O ports feature active circuitry on the input stage that, when the output shared by that pin is disabled, will maintain the input in the last state taken by the output. This state will be maintained until changed by the activity on the bus. The advantage of this arrangement is that when all outputs on the bus are disabled, the inputs will be prevented from floating, resulting in minimum power dissipation and minimum susceptibility to noise. This eliminates any need for external pull-up or pull-down resistors. The parity inputs API and BPI have similar circuitry.

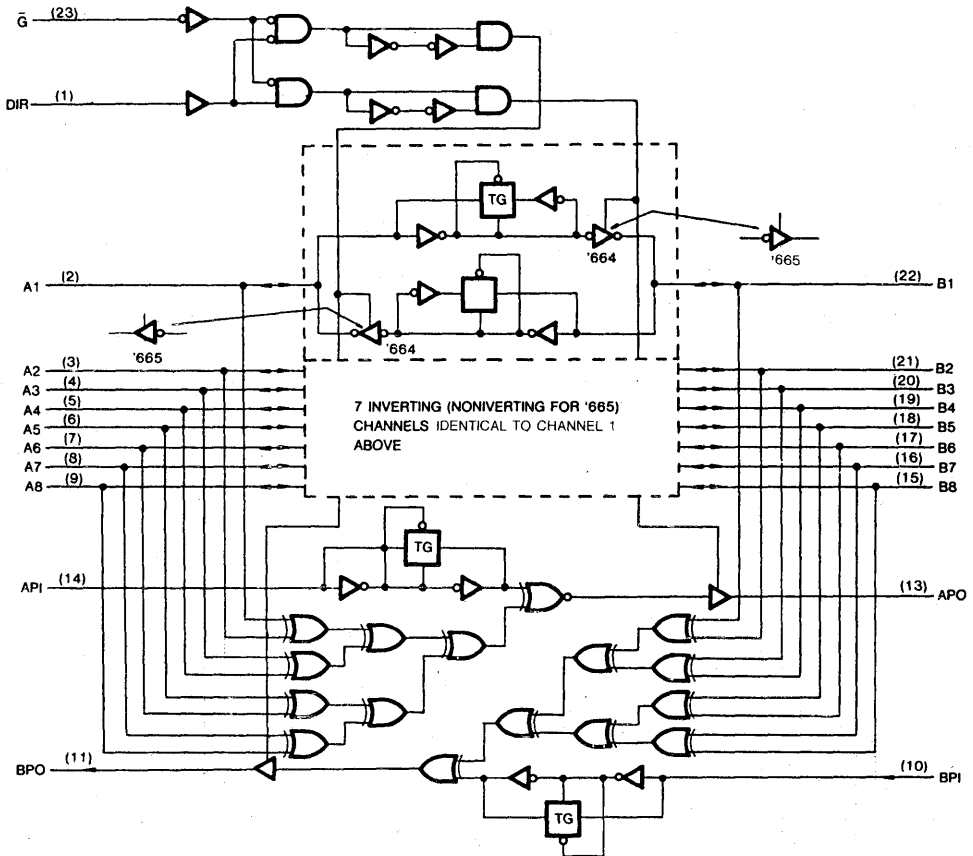
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

**FUNCTION TABLE**

CONTROL INPUTS		NUMBER OF HIGH INPUTS ON A BUS AND API	NUMBER OF HIGH INPUTS ON B BUS AND BPI	OUTPUTS		OPERATION	
$\bar{G}$	DIR			APO	BPO	'664	'665
L	L	X	0, 2, 4, 6, 8	Z	H	$\bar{B}$ Data to A Bus	B Data to A Bus
		X	1, 3, 5, 7, 9	Z	L		
L	H	0, 2, 4, 6, 8	X	H	Z	$\bar{A}$ Data to B Bus	A Data to B Bus
		1, 3, 5, 7, 9	X	L	Z		
H	X	X	X	Z	Z	Isolation	Isolation

**LOGIC DIAGRAM**



**Absolute Maximum Ratings\***

- Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V
- DC Input Diode Current,  $I_{IK}$   
 $(V_I < -0.5V \text{ or } V_I > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- DC Output Diode Current,  $I_{OK}$   
 $(V_O < -0.5V \text{ or } V_O > V_{CC} + 0.5V)$  . . . . .  $\pm 20$  mA
- Continuous Output Current Per Pin,  $I_O$   
 $(-0.5V < V_O < V_{CC} + 0.5V)$  . . . . .  $\pm 70$  mA
- Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA
- Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C
- Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

- Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V
  - DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  . . . . . 0V to  $V_{CC}$
  - Operating Temperature  
Range KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C
  - Input Rise & Fall Times,  $t_r, t_f$  . . . . . Max 500 ns
- Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V\pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	$\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 6$  ns), HCTLS664/655

Characteristic	Symbol	Conditions†	$T_s = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_s = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_s = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Guaranteed Limits					
Maximum Propagation Delay, A or B to B or A	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39	ns		
			23	28	35	45			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	38	ns		
			23	28	35	36			
Maximum Propagation Delay, A or B to APO or BPO	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	24	32	40	48	ns		
			27	35	45	54			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	24	32	40	48	ns		
			27	35	45	54			
Maximum Propagation Delay, API or BPI to APO or BPO	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39	ns		
			23	28	35	45			
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	20	25	30	39	ns		
			23	28	35	45			
Maximum Output Enable Time, $\bar{G}$ to A or B	$t_{pZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40	48	ns	
			$C_L = 150\text{pF}$	27	35	45	54		
	$t_{pZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40	48	ns	
			$C_L = 150\text{pF}$	27	35	45	54		
Maximum Output Delay Time, $\bar{G}$ to A or B	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	24	32	40	48	ns		
			$C_L = 50\text{pF}$	24	22	40		50	
	$t_{PLZ}$	$R_L = 1\text{k}\Omega$	24	32	40	48	ns		
			$C_L = 50\text{pF}$	24	22	40		50	
Maximum Output Enable Time DIR to A or B	$t_{pZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40	48	ns	
			$C_L = 150\text{pF}$	27	35	45	54		
	$t_{pZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	24	32	40	48	ns	
			$C_L = 150\text{pF}$	27	35	45	54		
Maximum Output Disable Time, DIR to A or B	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	20	32	40	48	ns		
			$C_L = 50\text{pF}$	24	32	40		48	
	$t_{HLZ}$	$R_L = 1\text{k}\Omega$	20	32	40	48	ns		
			$C_L = 50\text{pF}$	24	32	40		48	
Maximum Input Capacitance	$C_{IN}$		5				pF		
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10				pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

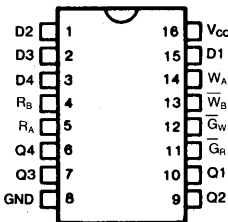
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**FEATURES**

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Expandable to 512 Words of N-bits
- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTL5:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54HCTL5:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLES**

**WRITE MODE SELECT TABLE**

OPERATING MODE	INPUTS		INTERNAL LATCHES <sup>(a)</sup>
	$\bar{G}_W$	$D_n$	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE:

a. The Write Address ( $W_A$  and  $W_B$ ) to the "Internal latches" must be stable while  $\bar{G}_W$  is LOW for conventional operation.

**DESCRIPTION**

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable Inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs ( $W_A$  and  $W_B$ ) determine the location of the stored word. When the write enable ( $\bar{G}_W$ ) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the  $\bar{G}_W$  is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when  $\bar{G}_W$  is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs ( $R_A$  and  $R_B$ ). The addressed word appears at the four outputs when the read enable ( $\bar{G}_R$ ) is LOW. Data outputs are in the HIGH impedance "off" state when the read enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the  $I_{OH}$  current available. Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

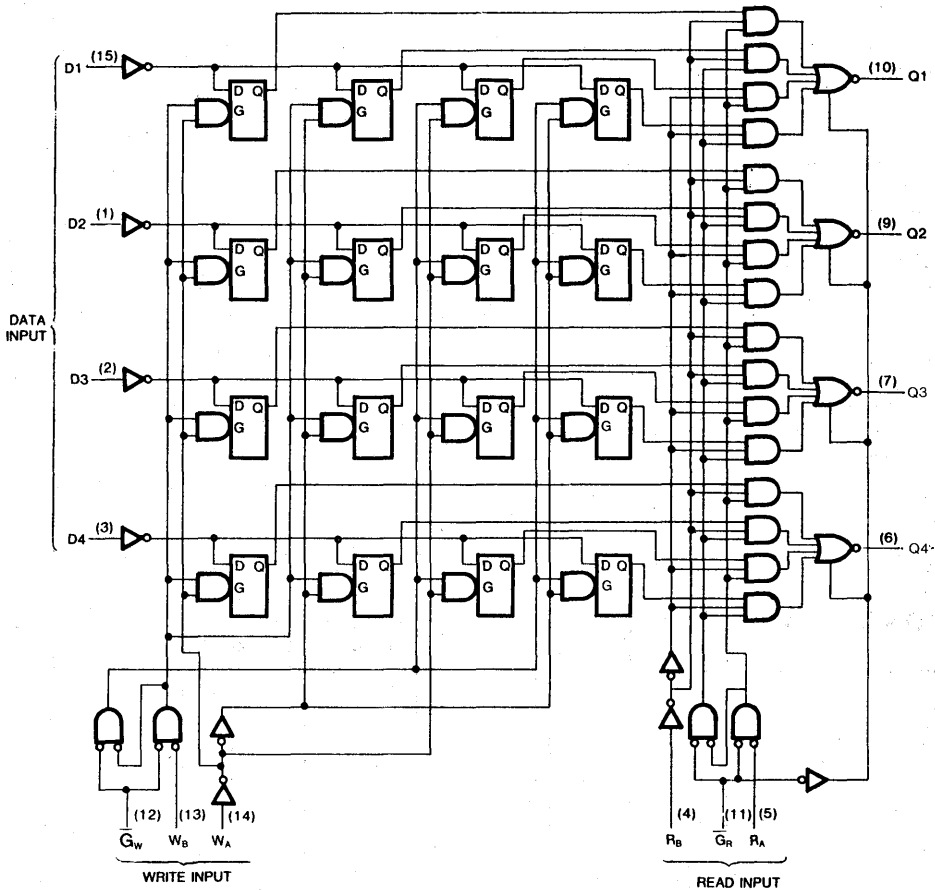
**READ MODE SELECT TABLE**

OPERATING MODE	INPUTS		OUTPUT $Q_n$
	$\bar{G}_R$	INTERNAL LATCHES <sup>(b)</sup>	
Read	L	L	L
	L	H	H
Disabled	H	H	(Z)

NOTE:

b. The selection of the "internal latches" by Read Address ( $R_A$  and  $R_B$ ) are not constrained by  $\bar{G}_W$  or  $\bar{G}_R$  operation.

LOGIC DIAGRAM



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTL5:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTL5:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	$V_{CC}-0.1$ 3.7	V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\pm 10.0$	$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	160.0	$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	3.0	mA	

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS670)

Characteristic	Symbol	Conditions <sup>†</sup>	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, $R_A$ or $R_B$ to Output	$t_{PLH}$	$C_L = 50\text{pF}$	20	32	40	48	ns		
		$C_L = 150\text{pF}$	23	35	45	54			
	$t_{PHL}$	$C_L = 50\text{pF}$	20	32	40	48			
		$C_L = 150\text{pF}$	23	35	45	54			
Maximum Propagation Delay, $G_W$ to Output	$t_{PLH}$	$C_L = 50\text{pF}$	27	36	45	59	ns		
		$C_L = 150\text{pF}$	30	39	50	65			
	$t_{PHL}$	$C_L = 50\text{pF}$	27	36	45	59			
		$C_L = 150\text{pF}$	30	39	50	65			
Maximum Propagation Delay, Data to Output	$t_{PLH}$	$C_L = 50\text{pF}$	27	38	45	59	ns		
		$C_L = 150\text{pF}$	30	39	50	65			
	$t_{PHL}$	$C_L = 50\text{pF}$	27	36	45	54			
		$C_L = 150\text{pF}$	30	39	50	60			
Maximum Output Enable Time $G_R$ to Output	$t_{PZH}$	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$	24	32	40	48	ns		
		$C_L = 150\text{pF}$	27	35	45	54			
	$t_{PZL}$	$C_L = 50\text{pF}$	24	32	40	48			
		$C_L = 150\text{pF}$	27	35	45	54			
Maximum Output Disable Time $G_R$ to Output	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	24	32	40	48	ns		
	$t_{PLZ}$	$C_L = 150\text{pF}$	24	32	40	48			
Set up Time	$D_n$ to $G_W$	$t_{SU}$	9	12	15	18	ns		
	$W_A, W_B$ to $G_W$		15	18	23	27			
Hold Time	$D_n$ to $G_W$	$t_h$	0	0	0	0	ns		
	$W_A, W_B$ to $G_W$		0	0	0	0			
Maximum Input Capacitance	$C_{IN}$		5				pF		
Maximum Output Capacitance	$C_{OUT}$	Output disabled	10				pF		
Power Dissipation Capacitance*	$C_{PD}$						pF		

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- '679: 12-bit to 4-bit comparator with enable
- '680: 12-bit to 4-bit comparator with latch
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### DESCRIPTION

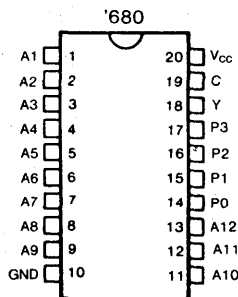
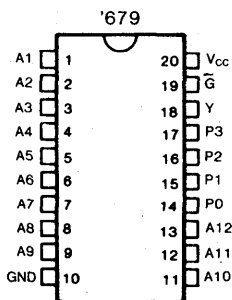
The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The '679 features an enable input ( $\bar{G}$ ). When  $\bar{G}$  is low, the device is enabled. When  $\bar{G}$  is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

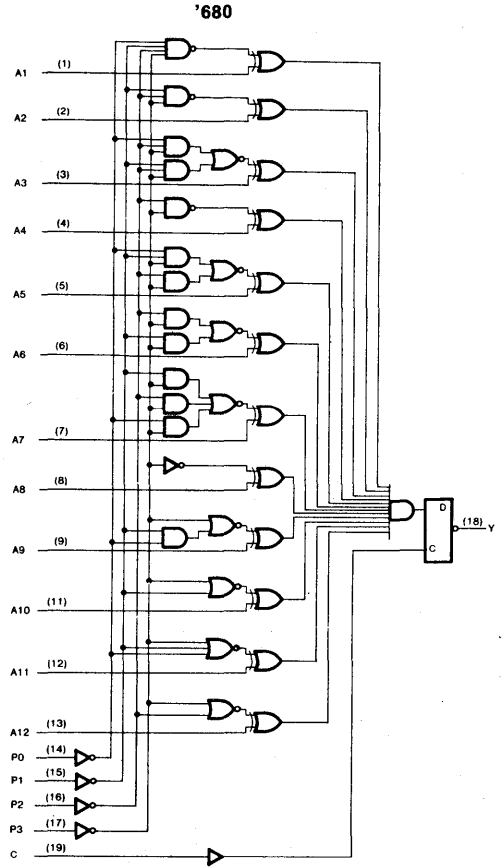
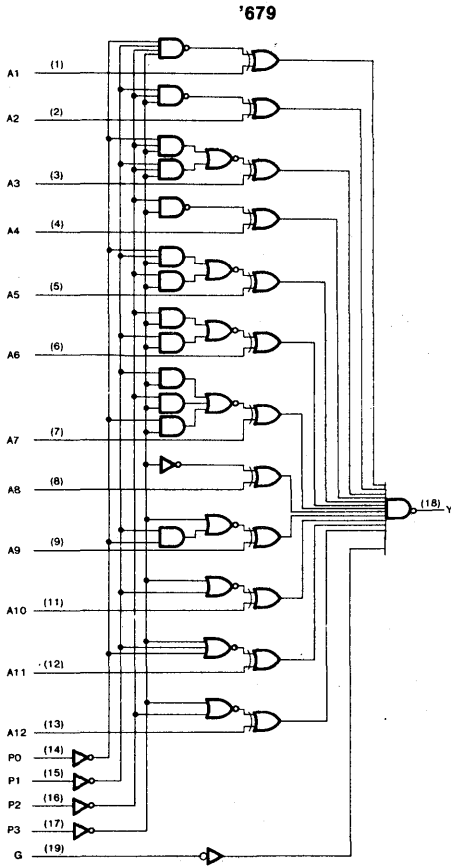
These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### PIN CONFIGURATIONS



LOGIC DIAGRAMS



### FUNCTION TABLE

'679	'680	INPUTS COMMON TO '679 AND '680												OUTPUT Y				
		P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8		A9	A10	A11	A12
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
H		'679: Any combination															H	
	L	'680: Any combination															Latched	

Note: These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which  $P=12, 13$  and  $14$ . If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change  $P\geq 9$  to  $P=9 \dots 11/13 \dots 15, P\geq 10$  to  $P=10/11/14/15$ , and  $P\geq 11$  to  $P=11/15$ .

### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V

DC Input Diode Current,  $I_{IK}$

( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA

DC Output Diode Current,  $I_{OK}$

( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA

Continuous Output Current Per Pin,  $I_O$

( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA

Continuous Current Through

$V_{CC}$  or GND pins .....  $\pm 250$  mA

Storage Temperature Range,  $T_{stg}$ , ..... -65°C to +150°C

Power Dissipation Per Package,  $P_d$ , ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur.

These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V

DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$

Operating Temperature

Range

KS74HCTLS: -40°C to +85°C

KS54HCTLS: -55°C to +125°C

Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTL5	KS54HCTL5	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4\text{V}$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	$\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTL5679)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74HCTL5	KS54HCTL5	Unit
			$V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	
			Typ	Guaranteed Limits			
Maximum Propagation Delay, Any P to Y	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40	48	ns
		$C_L = 150\text{pF}$	27	35	45	54	
	$t_{PHL}$	$C_L = 50\text{pF}$	27	32	40	48	ns
		$C_L = 150\text{pF}$	30	35	45	54	
Maximum Propagation Delay, Any A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	21	28	35	42	ns
		$C_L = 150\text{pF}$	24	31	40	48	
	$t_{PHL}$	$C_L = 50\text{pF}$	21	28	35	42	ns
		$C_L = 150\text{pF}$	24	31	40	48	
Maximum Propagation Delay, G to Y	$t_{PLH}$	$C_L = 50\text{pF}$	18	24	30	36	ns
		$C_L = 150\text{pF}$	21	27	35	42	
	$t_{PHL}$	$C_L = 50\text{pF}$	18	24	30	36	ns
		$C_L = 150\text{pF}$	21	27	35	42	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS680)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Propagation Delay, Any P to Y	$t_{PLH}$	$C_L = 50\text{pF}$	27	36	45		54		ns
		$C_L = 150\text{pF}$	30	39	50		60		
	$t_{PHL}$	$C_L = 50\text{pF}$	27	32	40		48		
		$C_L = 150\text{pF}$	30	35	45		64		
Maximum Propagation Delay, Any A to Y	$t_{PLH}$	$C_L = 50\text{pF}$	24	32	40		48		ns
		$C_L = 150\text{pF}$	27	35	45		64		
	$t_{PHL}$	$C_L = 50\text{pF}$	24	32	40		48		
		$C_L = 150\text{pF}$	27	35	45		64		
Maximum Propagation Delay, C to Y	$t_{PLH}$	$C_L = 50\text{pF}$	19	26	32		38		ns
		$C_L = 150\text{pF}$	22	29	37		44		
	$t_{PHL}$	$C_L = 50\text{pF}$	19	26	32		38		
		$C_L = 150\text{pF}$	22	29	37		44		
Set up Time An before E	$t_{SU}$		9	12	15		18		ns
Hold Time An after E	$t_H$		0	0	0		0		ns
Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$								pF

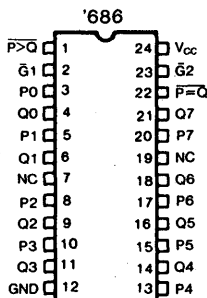
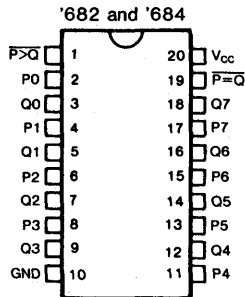
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

## FEATURES

- Compares Two 8-Bit Words
- '682 has 20kΩ pull-up Resistors on the Q Inputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:  
( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

## PIN CONFIGURATIONS



NC—No internal connection

## DESCRIPTION

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide  $\overline{P=Q}$  and  $P>Q$  outputs. The '682 features 20-kΩ pull-up termination resistors on the Q inputs for analog or switch data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

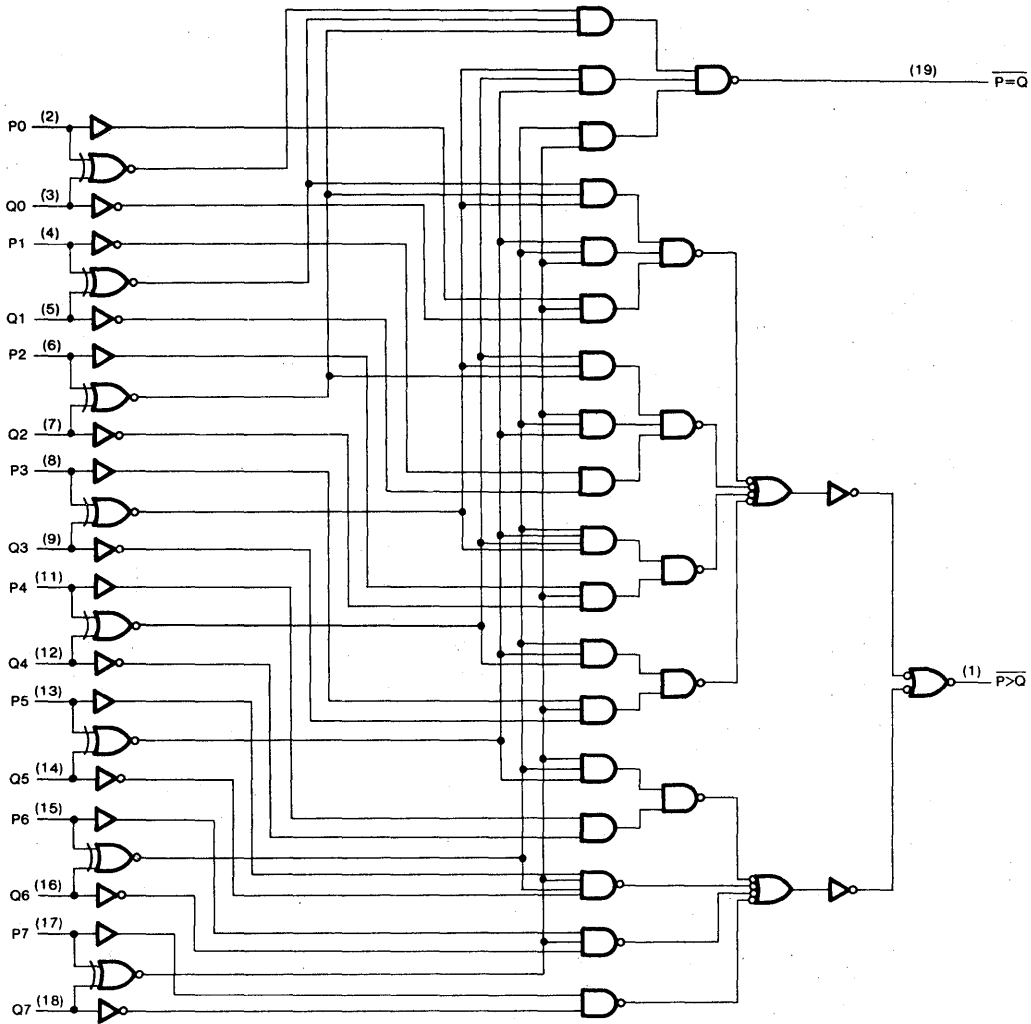
## FUNCTION TABLE

DATA	INPUTS		OUTPUTS	
	$\overline{G1}$	$\overline{G2}$	$\overline{P=Q}$	$P>Q$
P, Q	L	X	L	H
P=Q	X	L	H	L
P>Q	X	X	H	H
P=Q	H	X	H	H
P>Q	X	H	H	H
X	H	H	H	H

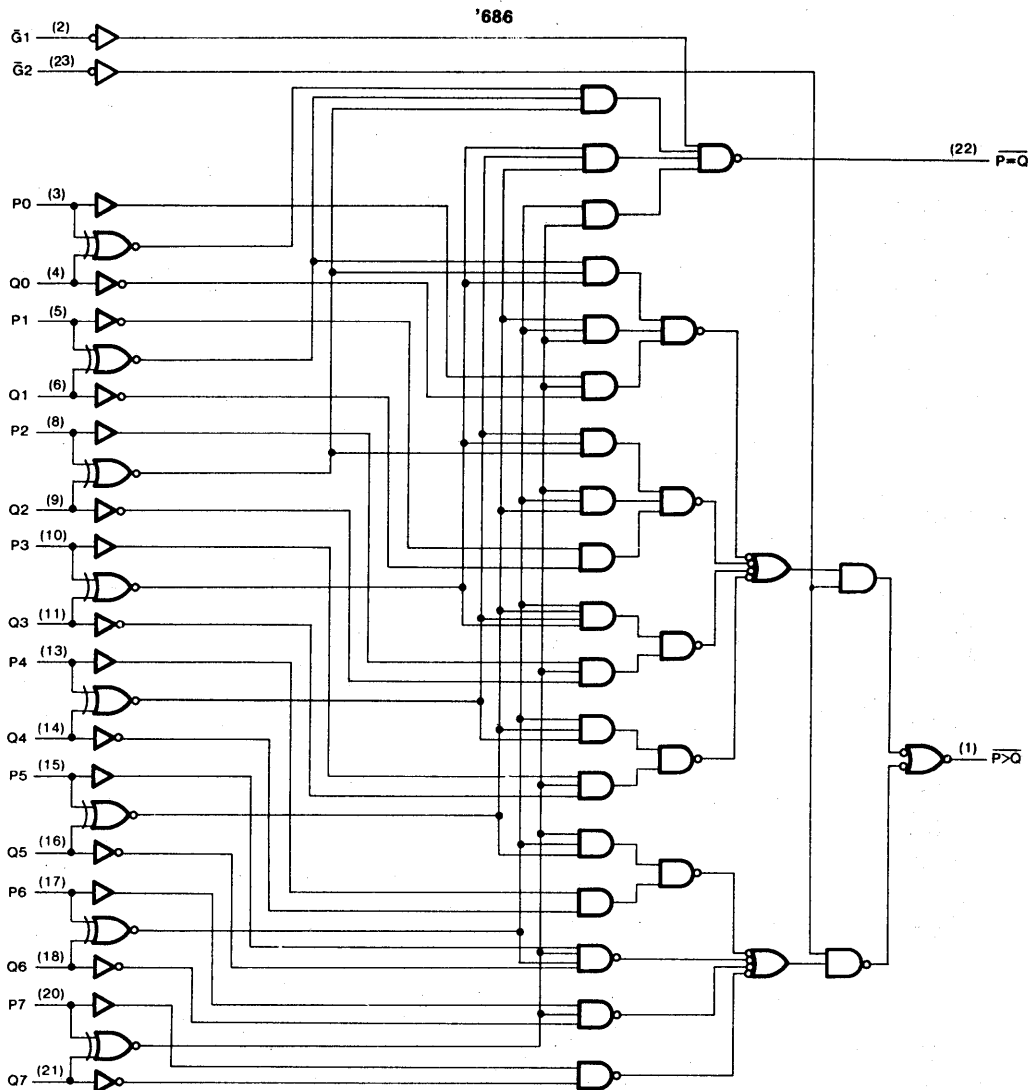
- NOTES: 1. The last 3 lines of the function table apply only to the device having enable inputs, i.e., '686.  
2. The  $\overline{P=Q}$  function can be generated by applying the  $\overline{P=Q}$  and  $P>Q$  outputs to a 2-input NAND gate.

**LOGIC DIAGRAMS**

'682 or '684



LOGIC DIAGRAMS (continued)



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$ , ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTL5: -40°C to +85°C  
 KS54HCTL5: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Parameter	Symbol	Test Conditions	$T_A = 25^\circ C$		KS74AHCT	54AHCT	Unit
			Typ		$T_A = -40^\circ C$ to $+85^\circ C$	$T_A = -55^\circ C$ to $+125^\circ C$	
Guaranteed Limits							
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (Totem-pole Outputs)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.93	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage (All Outputs)	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current ('682 Q Inputs)		$V_{CC} = Max$ $V_{IN} = 2.7V$ $V_{IN} = 0.4V$		-0.2 -0.4	-0.2 -0.4	-0.2 -0.4	mA
Maximum Input Current (All other Inputs)	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT} = V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	For '682: $V_{IN} = GND$ (Q0-Q7) $V_{IN} = V_{CC}$ or GND (all other inputs)		3.5	3.5	3.5	mA
		For '684 and '688 $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT} = 0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS682, HCTLS684, HCTLS686

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Maximum Propagation Delay, P or Q to $\overline{P=Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	18	25	31	38	ns
		$C_L = 150\text{pF}$	21	28	36	44	
	$t_{PHL}$	$C_L = 50\text{pF}$	18	25	31	38	ns
		$C_L = 150\text{pF}$	21	28	36	44	
Maximum Propagation Delay, P or Q to $\overline{P>Q}$	$t_{PLH}$	$C_L = 50\text{pF}$	22	32	38	45	ns
		$C_L = 150\text{pF}$	25	35	43	51	
	$t_{PHL}$	$C_L = 50\text{pF}$	22	30	38	45	ns
		$C_L = 150\text{pF}$	25	33	43	51	
Maximum Propagation Delay, $\overline{G1}$ to $\overline{P=Q}$ ('686 Only)	$t_{PLH}$	$C_L = 50\text{pF}$	15	20	25	30	ns
		$C_L = 150\text{pF}$	18	23	30	36	
	$t_{PHL}$	$C_L = 50\text{pF}$	15	20	25	30	ns
		$C_L = 150\text{pF}$	18	23	30	36	
Maximum Propagation Delay, $\overline{G2}$ to $\overline{P<Q}$ ('686 Only)	$t_{PLH}$	$C_L = 50\text{pF}$	18	25	31	38	ns
		$C_L = 150\text{pF}$	21	28	36	44	
	$t_{PHL}$	$C_L = 50\text{pF}$	18	25	31	38	ns
		$C_L = 150\text{pF}$	21	28	36	44	
Maximum Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

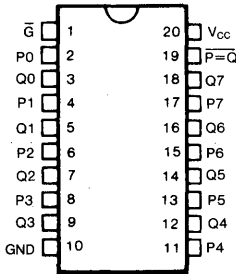
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Compares Two 8-Bit Words
- Choice of Totem-pole ('688) and open-drain ('689) outputs ('688 is identical to '521)
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:  
( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages  
(Available Tape & Reel), standard DIPs.

**PIN CONFIGURATION**



**FUNCTION TABLE**

INPUTS		OUTPUT $\overline{P=Q}$
DATA P,Q	ENABLE $\overline{G}$	
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

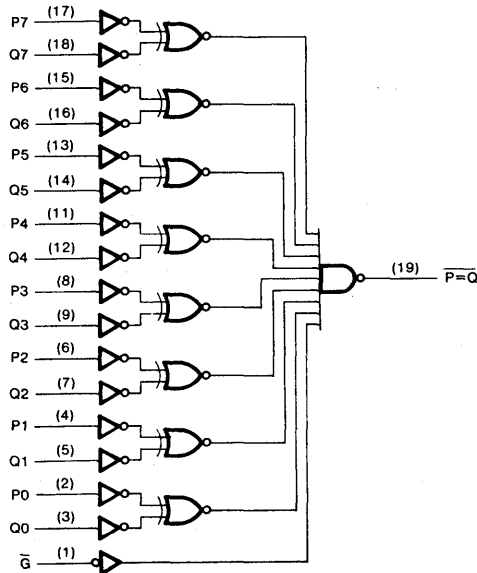
**DESCRIPTION**

These identity comparators perform comparisons of two 8-bit binary or BCD words. The output of '688 is totem-pole while '689's are open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**LOGIC DIAGRAM (Positive Logic)**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . . -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . . . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74HCTLS		KS54HCTLS		Unit
			Typ	Guaranteed Limits	$T_a = -40^\circ C$ to $+85^\circ C$	$T_a = -55^\circ C$ to $+125^\circ C$			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage ('688 only)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu A$	
Maximum 3-State Leakage Current ('689 only)	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$		$\mu A$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0		$\mu A$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0		mA	



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS688

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$				
			Typ		Guaranteed Limits		
Maximum Propagation Delay, P to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39	
Maximum Propagation Delay, Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	16 19	22 25	28 33	33 39	
Maximum Propagation Delay, G to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	15 18	20 23	25 30	30 36	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS689

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$				
			Typ		Guaranteed Limits		
Maximum Propagation Delay, P to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	31 34	37 42	43 49	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22	26 29	32 37	38 44	
Maximum Propagation Delay, Q to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	24 27	31 34	37 42	43 49	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	19 22	26 29	32 37	38 44	
Maximum Propagation Delay, G to P=Q	t <sub>PLH</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	23 27	29 32	35 40	41 47	ns
	t <sub>PHL</sub>	C <sub>L</sub> =50pF C <sub>L</sub> =150pF	18 21	24 27	30 35	36 42	
Maximum Input Capacitance	C <sub>IN</sub>		5				pF
Power Dissipation Capacitance*	C <sub>PD</sub>						pF

\* C<sub>PD</sub> determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

FEATURES

- I/O port configuration enables output data back onto input bus
- Latch ('793) and Register ('794) options
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

DESCRIPTION

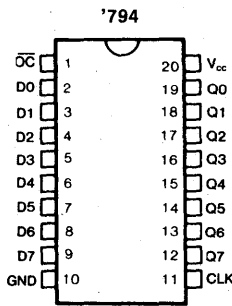
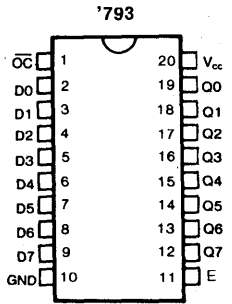
These are 8-bit latches/registers that allow temporary storage and retrieval of data on a bus. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in a '793 or '794, for verification and/or updating.

The data is loaded in the registers on the positive-edge of the clock (CLK) for the '794. The data is passed through the '793 when E is high, and it is latched when E goes low. The output control ( $\overline{OC}$ ) is used to enable data on the D0-D7 pins. when  $\overline{OC}$  is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When  $\overline{OC}$  is high, D0-D7 are inputs to the latches/registers configuring D as an input bus.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

PIN CONFIGURATIONS



FUNCTION TABLES

'793

E	$\overline{OC}$	Q	D
L	L	$Q_0^{**}$	Output, Q
L	H	$Q_0^{**}$	Input
H†	L	$D^*$	Output, Q*
H	H	D	Input

\* In this case the output of the latch feeds the input, and a "race" condition results.

\*\*  $Q_0$  represents the previous "latched" state.

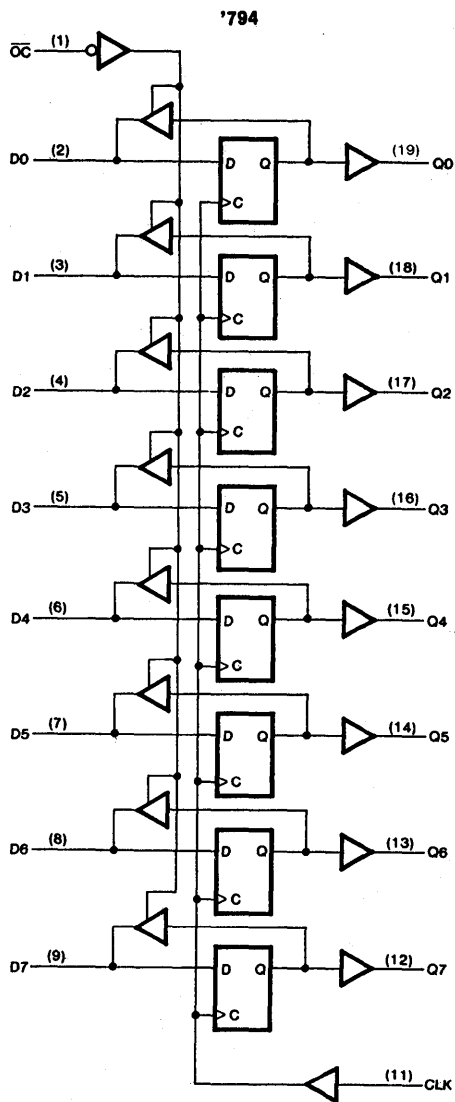
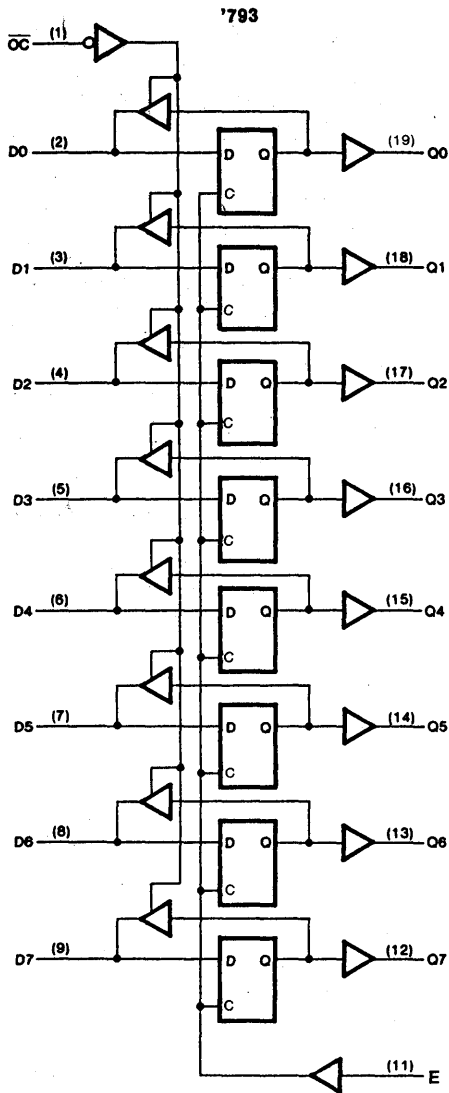
† This transition is not a normal mode of operation and may produce hazards.

'794

CLK	$\overline{OC}$	Q	D
L or H or ↓	L	$Q_0$	Output, Q
L or H or ↓	H	$Q_0$	Input
↑	L	$Q_0$	Output, Q*
↑	H	D	Input

\* In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at  $Q_0$ .

**LOGIC DIAGRAMS**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  . . . . . -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) . . . . .  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins . . . . .  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † . . . . . 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  . . . . . 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  . . 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  . . . . . Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS793, 794

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit	
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Guaranteed Limits				
Maximum Clock Frequency ('794 only)	$t_{max}$	$C_L = 50\text{pF}$	50	40	35	30	MHz	
Maximum Propagation Delay, D to Any Q ('793 only)	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17	18 21	23 28	27 33	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	14 17	18 21	23 28	27 33		
Maximum Propagation Delay, CLK/E to Any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18	20 23	25 30	30 36	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18	20 23	25 30	30 36		
Maximum Enable Time, OC to D	$t_{PZH}$	$R_L = 1\text{k}\Omega$ (C=Low for '793)	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18	20 23	25 30	30 36	ns
	$t_{PZL}$		$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18	20 23	25 30	30 36	
Maximum Disable Time, OC to D	$t_{PHZ}$	$R_L = 1\text{k}\Omega, C_L = 50\text{pF}$ (C=Low for '793)		15	20	25	30	ns
	$t_{PLZ}$			15	20	25	30	
Minimum Pulse Width, CLK/E High or low	$t_w$		10	15	18	20	ns	
Minimum Setup Time	D before $E\downarrow$ ('793)	$t_{su}$		8	10	13	15	ns
	D before $CLK\uparrow$ ('794)			10	15	18	20	
Minimum Hold Time	D after $E\downarrow$ ('793)	$t_h$		8	10	13	15	ns
	D after $CLK\uparrow$ ('794)			0	0	0	0	
Maximum Input Capacitance	$C_{IN}$		5				pF	
Maximum Output Capacitance	$C_{OUT}$		10				pF	
Power Dissipation Capacitance*	$C_{PD}$						ns	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

# KS54HCTLS 821/822 KS74HCTLS

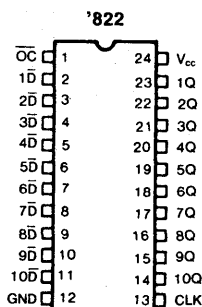
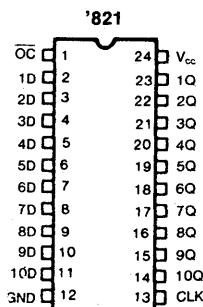
## 10-Bit Bus Interface Flip-Flops with 3-State Outputs

### Preliminary Specifications

### FEATURES

- Functionally Equivalent to AMD's Am29821 and Am29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATIONS



### DESCRIPTION

These 10-bit bus-interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

All of the flip-flops are edge-triggered and D-type. On the positive transition of the clock the Q outputs on the '821 will be true, and on the '822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLES

(Each Flip-Flop)

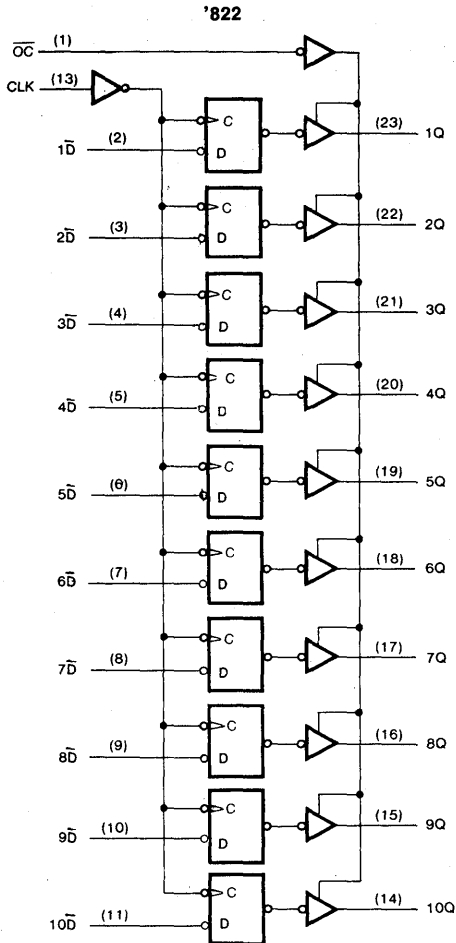
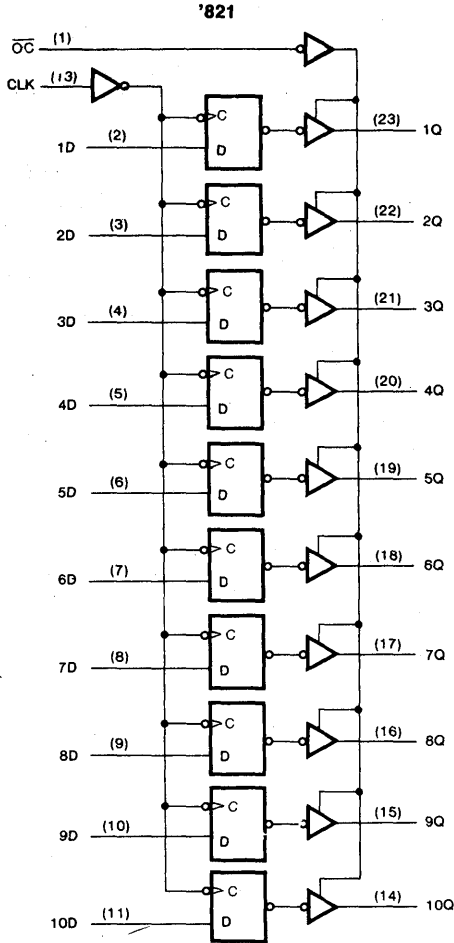
**'821**

Inputs			Output Q
$\overline{OC}$	CLK	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	$Q_0$
L	H	X	$Q_0$
H	X	X	Z

**'822**

Inputs			Output Q
$\overline{OC}$	CLK	$\overline{D}$	
L	$\uparrow$	H	L
L	$\uparrow$	L	H
L	L	X	$Q_0$
L	H	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAMS**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns, HCTLS821, HCTLS822)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit	
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Guaranteed Limits				
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	35	30	25	MHz	
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	15	20	25	30	ns	
		$C_L = 150\text{pF}$	18	23	30	36		
Maximum Output Enable Time, $\overline{OC}$ to any Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	24	30	36	ns
			$C_L = 150\text{pF}$	21	27	35	42	
	$t_{PZL}$		$C_L = 50\text{pF}$	18	24	30	36	
			$C_L = 150\text{pF}$	21	27	35	42	
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	18	24	30	36	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	18	24	30	36		
Minimum Pulse Width, CLK High or Low	$t_w$		12	16	20	24	ns	
Minimum Setup Time, Data before CLK†	$t_{su}$		12	16	20	24	ns	
Minimum Hold Time, Data after CLK†	$t_h$		0	0	0	0	ns	
Maximum Input Capacitance	$C_{IN}$		5				pF	
Maximum Output Capacitance	$C_{OUT}$	$\overline{OC} = V_{CC}$	10				pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$ $\overline{OC} = \text{GND}$	5				pF	

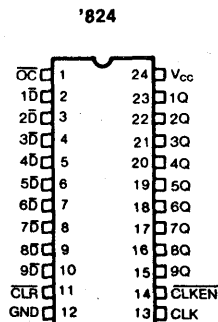
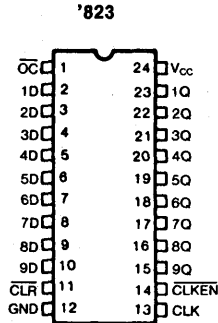
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**FEATURES**

- Functionally Equivalent to AMD's Am29823 and Am29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

**PIN CONFIGURATIONS**



**DESCRIPTION**

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ( $\overline{\text{CLKEN}}$ ) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting D inputs. Taking the  $\overline{\text{CLR}}$  input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ( $\overline{\text{OC}}$ ) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLES**

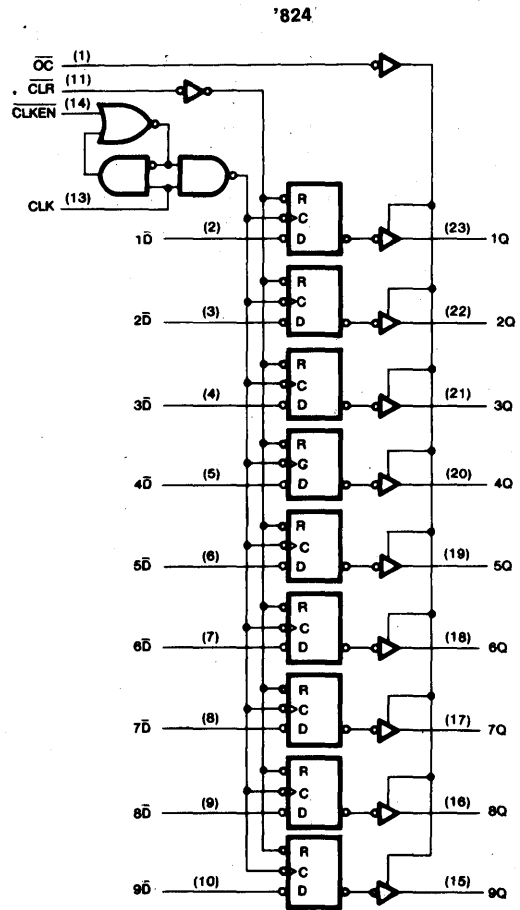
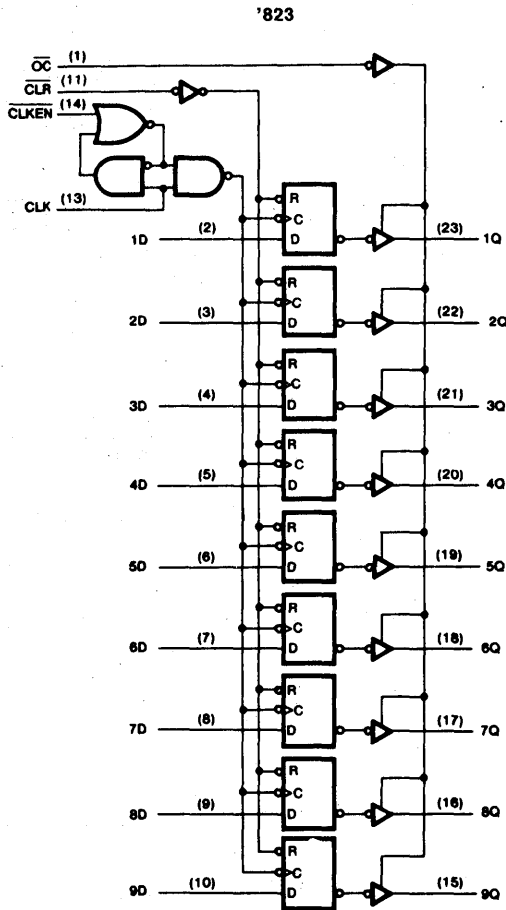
**'823**

INPUT					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

**'824**

INPUTS					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	$\overline{\text{D}}$	Q
L	L	X	X	X	L
L	H	L	$\uparrow$	H	L
L	H	L	$\uparrow$	L	H
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5 to +7V  
DC Input Diode Current,  $I_{IK}$   
( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
DC Output Diode Current,  $I_{OK}$   
( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
Continuous Output Current Per Pin,  $I_O$   
( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
Power Dissipation Per Package,  $P_{d1}$  ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
DC Input & Output Voltages\*,  $V_{IN}, V_{OUT}$  ... 0V to  $V_{CC}$   
Operating Temperature  
Range KS74HCTLS: -40°C to +85°C  
KS54HCTLS: -55°C to +125°C  
Input Rise & Fall Times,  $t_r, t_f$  ..... Max 500 ns  
Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ C$ to $+85^\circ C$	KS54HCTLS $T_a = -55^\circ C$ to $+125^\circ C$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS823, HCTLS824

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54HCTLS $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	35	30		25		MHz
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15	20	25		30		ns
			18	23	30		36		
Maximum Propagation Delay, CLR to Any Q	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15	20	25		30		ns
			18	23	30		36		
Maximum Propagation Delay, CLR to Any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	17	22	28		34		ns
			20	25	33		40		
Maximum Output Enable Time, $\overline{OC}$ to any Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$		18		24		ns
			$C_L = 150\text{pF}$		21		27		
	$C_L = 50\text{pF}$		18		24				
	$C_L = 150\text{pF}$		21		27				
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	18	24	30		36		ns
	$t_{PLZ}$	$C_L = 50\text{pF}$	18	24	30		36		
Minimum Pulse Width CLR high or Low	$t_w$	$\overline{CLR}$ Low			12		16		ns
					12		16		
Minimum Setup Time Before CLK†	$t_{su}$	$\overline{CLR}$ Inactive			12		16		ns
		Bata			12		16		
		CLKEN high or Low			12		16		
Minimum Hold Time, CLKEN or data after CLK†	$t_h$		0	0	0		0		ns
Maximum Input Capacitance	$C_{IN}$		5						pF
Maximum Output Capacitance	$C_{OUT}$	Output Disabled	10						pF
Power Dissipation Capacitance* (per stage)	$C_{PD}$	OC = $V_{CC}$ OC = GND	5		30				pF

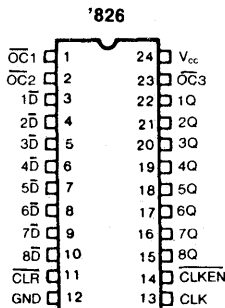
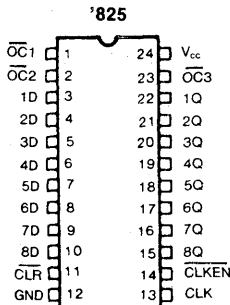
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Functionally Equivalent to AMD's Am29825 and Am29826
- Improved  $I_{OH}$  Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATIONS



### DESCRIPTION

These 8-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing multiuser buffer registers, I/O ports, bidirectional bus drivers and working registers.

With the clock enable ( $\overline{\text{CLKEN}}$ ) low, all D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high will disable the clock buffer, thus latching the outputs. The '825 has non-inverting D inputs and the '826 has inverting  $\overline{\text{D}}$  inputs. Taking the  $\overline{\text{CLR}}$  inputs low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ( $\overline{\text{OC1}}$ ,  $\overline{\text{OC2}}$ , and  $\overline{\text{OC3}}$ ) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**FUNCTION TABLES**

**'825**

Inputs					Output Q
$\overline{OC}^*$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

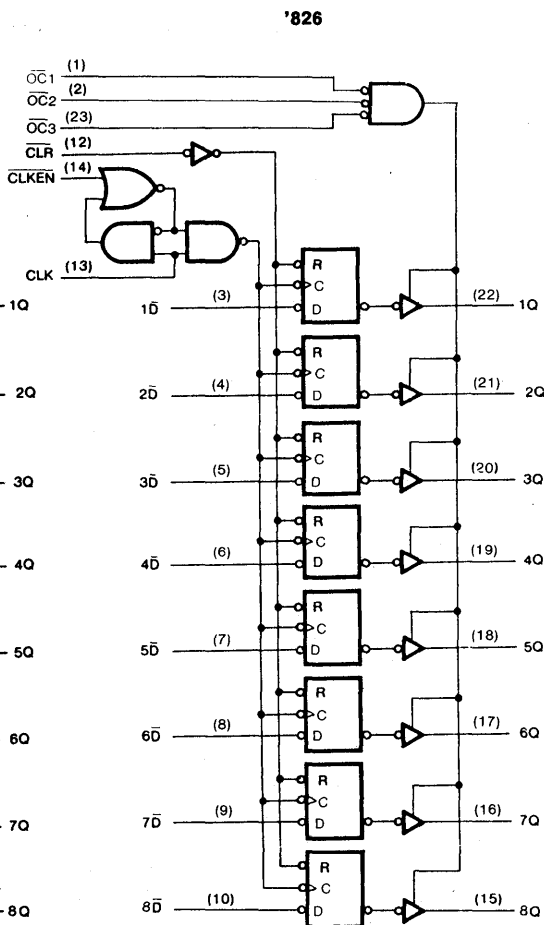
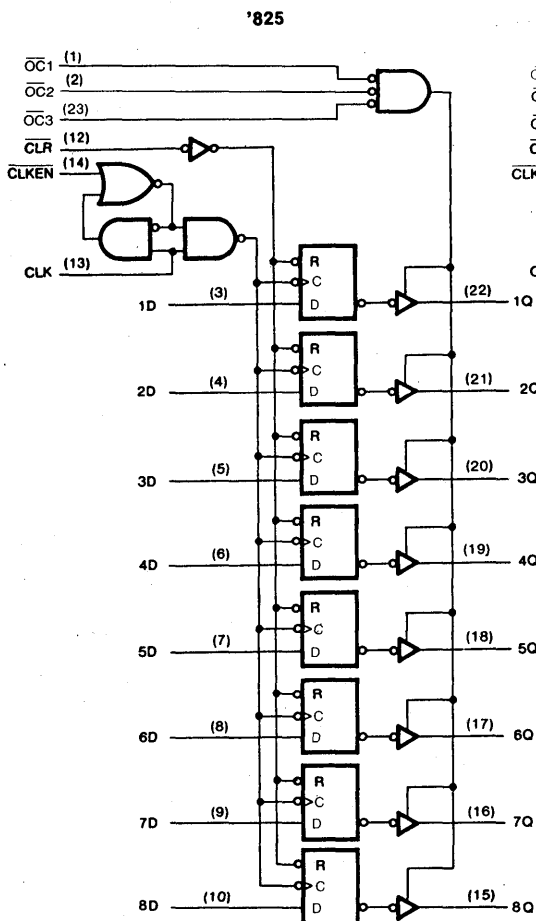
\*  $OC = H$  if any of  $OC1$ ,  $OC2$ , or  $OC3$  are high.  
 $OC = L$  of  $OC1$ ,  $OC2$ , and  $OC3$  are low.

**'826**

Inputs					Output Q
$\overline{OC}^*$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

\*  $OC = H$  if any of  $OC1$ ,  $OC2$ , or  $OC3$  are high.  
 $OC = L$  of  $OC1$ ,  $OC2$ , and  $OC3$  are low.

**LOGIC DIAGRAMS**



### Absolute Maximum Ratings\*

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74HCTLS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCTLS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS	KS54HCTLS	Unit
			Typ	Guaranteed Limits			
					$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS825, HCTLS826

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ		Guaranteed Limits				
Maximum Operating Frequency	$f_{max}$	$C_L = 50\text{pF}$	40	35	30		25		MHz
Maximum Propagation Delay, CLK to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	15	20	25		30		ns
		$C_L = 150\text{pF}$	18	23	30		36		
Maximum Propagation Delay, $\overline{\text{CLR}}$ to Any Q	$t_{PHL}$	$C_L = 50\text{pF}$	15	20	25		30		ns
		$C_L = 150\text{pF}$	18	23	30		36		
Maximum Propagation Delay, $\overline{\text{CLR}}$ to Any Q	$t_{PLH}$	$C_L = 50\text{pF}$	17	22	28		34		ns
		$C_L = 150\text{pF}$	20	25	33		40		
Maximum Output Enable Time, $\overline{\text{OC}}$ to any Q	$t_{PZL}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	24	30		36	ns
			$C_L = 150\text{pF}$	21	27	35		42	
	$t_{PZL}$	$C_L = 50\text{pF}$		18	24	30		36	
			$C_L = 150\text{pF}$	21	27	35		42	
Maximum Output Disable Time, $\overline{\text{OC}}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	18	24	30		36	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	18	24	30		36		
Minimum Pulse Width	$\overline{\text{CLR}}$ Low CLK high or Low	$t_w$		12	16	20		24	ns
				12	16	20		24	
Minimum Setup Time Before CLK†	$\overline{\text{CLR}}$ Inactive	$t_{su}$		12	16	20		24	ns
	Data			12	16	20		24	
	$\overline{\text{CLKEN}}$ high or Low			12	16	20		24	
Minimum Hold Time, CLKEN or data after CLK†	$t_h$		0	0	0		0	ns	
Maximum Input Capacitance	$C_{IN}$		5					pF	
Maximum Output Capacitance	$C_{OUT}$		10					pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$		5					pF	
			30						

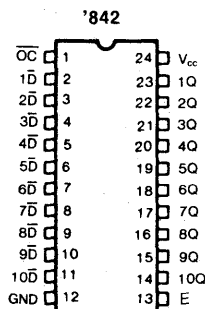
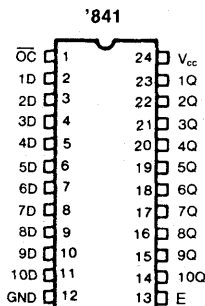
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Bus-Structured Pinout
- Provides Extra Bus Driving Latches
- Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ( $I_{OL} = 24 \text{ mA @ } V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATIONS



### DESCRIPTION

These 10-bit bus interface latches feature three state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The '841 has noninverting data (D) inputs and the '842 has inverting ( $\bar{D}$ ) inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLES

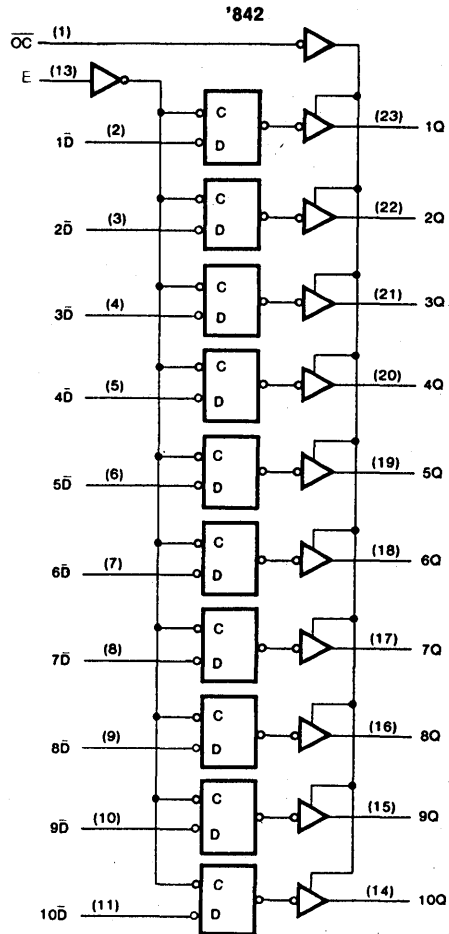
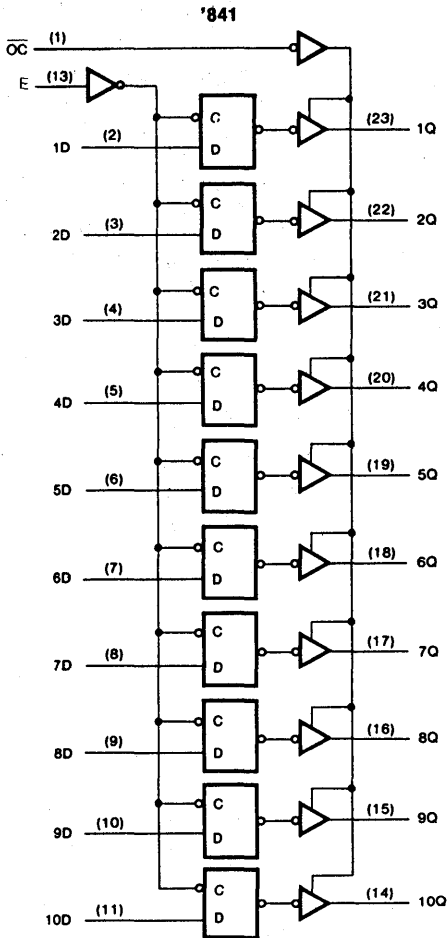
**'841**

INPUTS			OUTPUT
$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**'842**

INPUTS			OUTPUT
$\overline{OC}$	E	$\bar{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAMS**



### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , . . . . .	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) . . . . .	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) . . . . .	$\pm 70$ mA
Continuous Current Through $V_{CC}$ or GND pins . . . . .	$\pm 250$ mA
Storage Temperature Range, $T_{stg}$ . . . . .	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Power Dissipation Per Package, $P_d$ † . . . . .	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ . . . . .	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}$ , $V_{OUT}$ . . . . .	0V to $V_{CC}$
Operating Temperature Range . . . . .	KS74HCTLS: $-40^\circ\text{C}$ to $+85^\circ\text{C}$ KS54HCTLS: $-55^\circ\text{C}$ to $+125^\circ\text{C}$
Input Rise & Fall Times, $t_r$ , $t_f$ . . . . .	Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -6\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS841, HCTLS842

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit	
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ		Guaranteed Limits			
Maximum Propagation Delay, Data to Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	15 18	20 23	25 30	30 36	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}^\dagger$	15 18	20 23	25 30	30 36		
Maximum Propagation Delay, E to any Q	$t_{PLH}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40	42 48	ns	
	$t_{PHL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	21 24	28 31	35 40	42 48		
Maximum Output Enable Time, $\overline{OC}$ to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	24	30	36	ns
			$C_L = 150\text{pF}$	21	27	35	42	
	$t_{PZL}$	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	18	24	30	36		
			21	27	35	42		
Maximum Output Disable Time, $\overline{OC}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	18	24	30	36	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	18	24	30	36		
Minimum Pulse Width, E High	$t_w$		15	20	25	30	ns	
Minimum Setup Time, Data before E↓	$t_{su}$		12	16	20	24	ns	
Minimum Hold Time, Data after E↓	$t_h$		6	8	10	12	ns	
Maximum Input Capacitance	$C_{IN}$		5				pF	
Maximum Output Capacitance	$C_{OUT}$		10				pF	
Power Dissipation Capacitance* (per stage)	$C_{PD}$	$\overline{OC} = V_{CC}$	5				pF	
		$\overline{OC} = \text{GND}$	30					

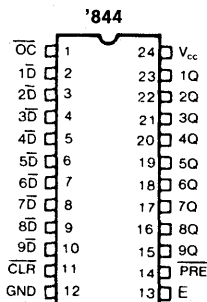
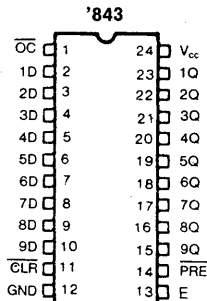
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURES

- Bus-Structured Pinout
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High Impedance
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current  
( $I_{OL} = 24 \text{ mA} @ V_{OL} = 0.5V$ ) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATIONS



### DESCRIPTION

These 9-bit bus interface latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

The nine latches are transparent D-type. The '843 has noninverting data (D) inputs and the '844 has inverting  $\bar{D}$  inputs.

A buffered output control ( $\overline{OC}$ ) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### FUNCTION TABLES

'843

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	E	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	$Q_0$
X	X	H	X	X	Z

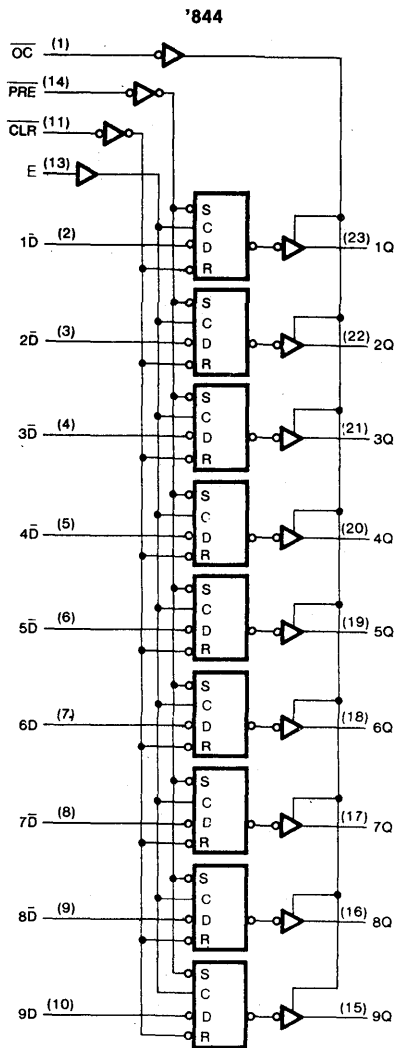
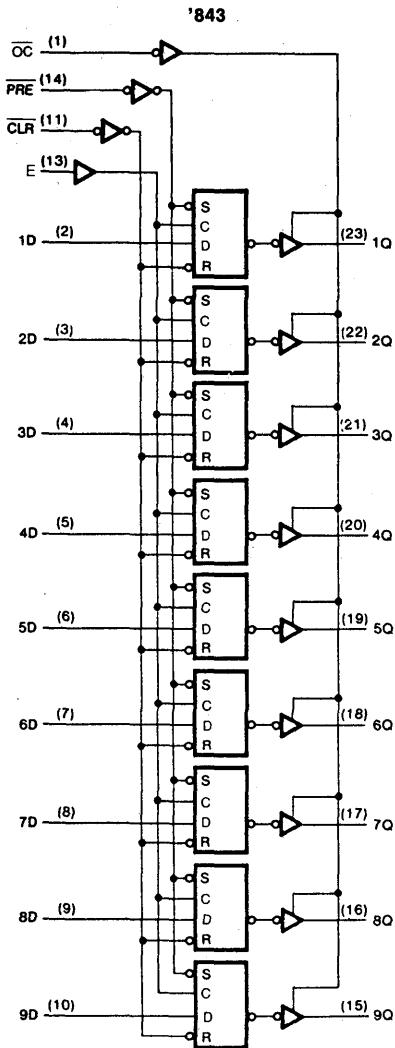
'844

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	E	$\bar{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	$Q_0$
X	X	H	X	X	Z

KS54HCTLS **843/844**  
KS74HCTLS

**9-Bit Bus Interface D-Type Latches with 3-State Outputs**

**LOGIC DIAGRAMS**



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous-Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCTLS: -40°C to +85°C  
 KS54HCTLS: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0		V	
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8		V	
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7		V	
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V	
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu\text{A}$	
Maximum 3-State Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$ or GND		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$		$\mu\text{A}$	
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0		$\mu\text{A}$	
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0		mA	



**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS843, HCTLS844

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit	
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ		Guaranteed Limits			
Maximum Propagation Delay, $t_o$	$t_{PLH}$	$C_L = 50\text{pF}$	18	24	30	36	ns	
		$C_L = 150\text{pF}$	21	27	35	42		
	$t_{PHL}$	$C_L = 50\text{pF}$	18	24	30	36	ns	
		$C_L = 150\text{pF}$	21	27	35	42		
Maximum Propagation Delay, E to any Q	$t_{PLH}$	$C_L = 50\text{pF}$	21	28	35	42	ns	
		$C_L = 150\text{pF}$	24	31	40	48		
	$t_{PHL}$	$C_L = 50\text{pF}$	21	28	35	42	ns	
		$C_L = 150\text{pF}$	24	31	40	48		
Maximum Propagation Delay, $\overline{\text{PRE}}$ to Q	$t_{PLH}$	$C_L = 50\text{pF}$	23	30	38	46	ns	
		$C_L = 150\text{pF}$	26	33	43	52		
Maximum Propagation Delay, $\overline{\text{CLR}}$ to Q	$t_{PHL}$	$C_L = 50\text{pF}$	23	30	38	46	ns	
		$C_L = 150\text{pF}$	26	33	43	52		
Maximum Output Enable Time, $\overline{\text{OC}}$ to any Q	$t_{PZH}$	$R_L = 1\text{k}\Omega$	$C_L = 50\text{pF}$	18	24	30	36	ns
			$C_L = 150\text{pF}$	21	27	35	42	
	$t_{PZL}$	$C_L = 50\text{pF}$		18	24	30	36	
			$C_L = 150\text{pF}$	21	27	35	42	
Maximum Output Disable Time, $\overline{\text{OC}}$ to any Q	$t_{PHZ}$	$R_L = 1\text{k}\Omega$	18	24	30	36	ns	
	$t_{PLZ}$	$C_L = 50\text{pF}$	18	24	30	36		
Minimum Pulse Width, E High	$t_w$		15	20	25	30	ns	
Minimum Setup Time, Data after E↓	$t_{su}$		12	16	20	24	ns	
Minimum Hold Time, Data before E↓	$t_h$		6	8	10	12	ns	
Maximum Input Capacitance	$C_{IN}$		5				pF	
Maximum Output Capacitance	$C_{OUT}$		10				pF	
Power Dissipation Capacitance (per stage)	$C_{PD}$	$\overline{\text{OC}} = V_{CC}$	5				pF	
		$\overline{\text{OC}} = \text{GND}$	30					

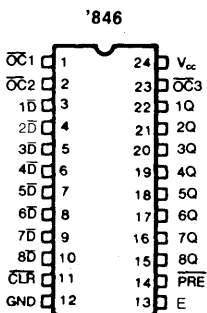
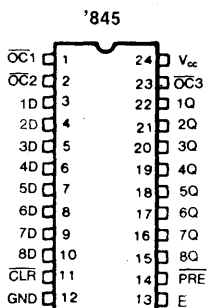
\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

### FEATURE

- 3-state buffer-type outputs drive bus-lines directly
- Bus-structured pinout
- Provides extra bus driving latches necessary for wider address/data paths or buses with parity
- Low power consumption characteristic of CMOS devices
- 3-state outputs with high drive current ( $I_{OL} = 24\text{mA}$  @  $V_{OL} = 0.5\text{V}$ ) for direct bus interface
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

### PIN CONFIGURATIONS



### DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since CLR and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

The buffered output control inputs (OC1, OC2, and OC3) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

# KS54HCTLS **845/846** KS74HCTLS

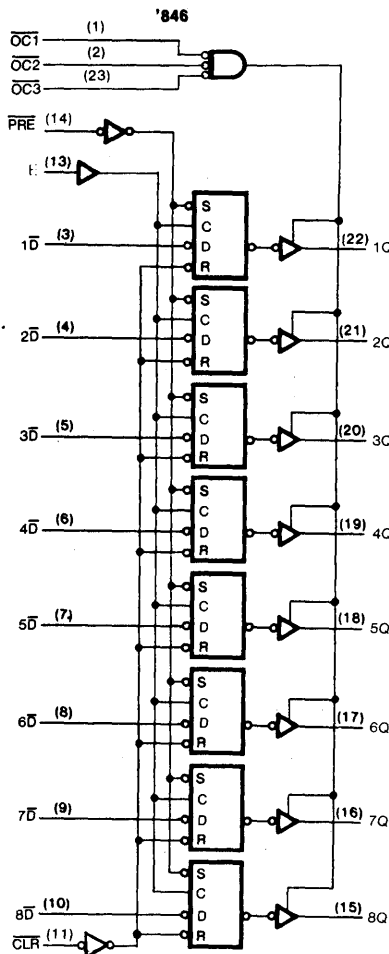
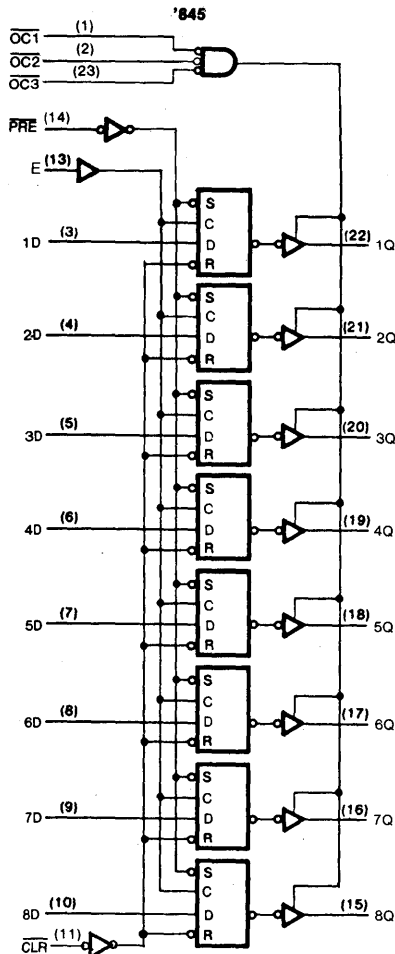
## 8-Bit Bus Interface D-Type Latches with 3-State Outputs

### FUNCTION TABLE

'845							OUTPUT
PRE	CLR	OC1	OC2	OC3	E	D	
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q <sub>0</sub>
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'846							OUTPUT
PRE	CLR	OC1	OC2	OC3	E	D	
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q <sub>0</sub>
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

### LOGIC DIAGRAMS



**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74HCLTS:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54HCLTS:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=-20\mu\text{A}$ $I_O=-4\text{mA}$	$V_{CC}$ 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other Inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS845

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Propagation Delay E to Q	$t_{PLH}$		23	30	38	46	ns
	$t_{PHL}$		23	30	38	46	
Propagation Delay $\bar{D}$ to Q	$t_{PLH}$		18	24	30	36	ns
	$t_{PHL}$		18	24	30	36	
Propagation Delay CLR to Q	$t_{PLH}$		27	36	45	54	ns
	$t_{PHL}$		27	36	45	54	
Propagation Delay PRE to Q	$t_{PLH}$		27	36	45	54	ns
	$t_{PHL}$		27	36	45	54	
Output Enable Time OC to Q	$t_{PZH}$		23	30	38	46	ns
	$t_{PZL}$		23	30	38	46	
Output Disable Time OC to Q	$t_{PHZ}$		16	21	26	31	ns
	$t_{PLZ}$		16	21	26	31	
Set up Time Dn before E	$t_{SU}$		12	16	20	24	ns
Hold Time Dn after E	$t_h$		0	0	0	0	ns
Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 6$  ns), HCTLS846

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		KS74HCTLS	KS54HCTLS	Unit
					$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ		Guaranteed Limits		
Propagation Delay E to Q	$t_{PLH}$		25	34	42	65	ns
	$t_{PHL}$		25	34	42	65	
Propagation Delay $\bar{D}$ to Q	$t_{PLH}$		20	27	34	40	ns
	$t_{PHL}$		20	27	34	40	
Propagation Delay CLR to Q	$t_{PLH}$		26	35	44	53	ns
	$t_{PHL}$		26	35	44	53	
Propagation Delay PRE to Q	$t_{PLH}$		26	35	44	52	ns
	$t_{PHL}$		26	35	44	52	
Output Enable Time OC to Q	$t_{PZH}$		19	26	32	38	ns
	$t_{PZL}$		19	26	32	38	
Output Disable Time OC to Q	$t_{PHZ}$		14	19	24	30	ns
	$t_{PLZ}$		14	19	24	30	
Set up Time Dn before E	$t_{SU}$		12	16	20	24	ns
Hold Time Dn after E	$t_h$		0	0	0	0	ns
Input Capacitance	$C_{IN}$		5				pF
Power Dissipation Capacitance*	$C_{PD}$						pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

† For AC switching test circuits and timing waveforms see section 2.

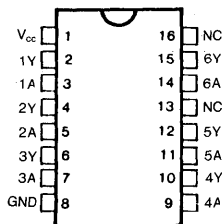
### FEATURES

- Modified input structure allows voltages up to 15V
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High drive current outputs:  
 $I_{OL} = 8\text{mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74HCTLS:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54HCTLS:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

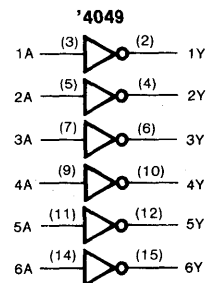
### DESCRIPTION

The '4049 and '4050 have a modified input protection structure that enable them to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0-15V logic can be converted to 0-5V logic when using a 5V supply. The modified input protection has no diode connected to  $V_{CC}$ , thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition the '4049 and '4050 can be used as simple buffers or inverters without level translation.

### PIN CONFIGURATION

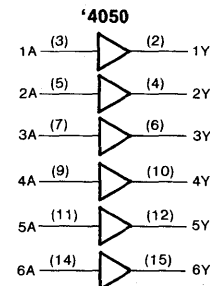


### LOGIC DIAGRAMS



### FUNCTION TABLE

INPUT A	OUTPUT Y	
	'4049	'4050
H	L	H
L	H	L



# KS54HCTLS 4049/4050 KS74HCTLS

## Hex Logic Level Down Converters

### Absolute Maximum Ratings\*

Supply Voltage Range $V_{CC}$ , .....	-0.5V to +7V
DC Input Diode Current, $I_{IK}$ ( $V_I < -0.5V$ or $V_I > +15.5V$ ) .....	$\pm 20$ mA
DC Output Diode Current, $I_{OK}$ ( $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ) .....	$\pm 20$ mA
Continuous Output Current Per Pin, $I_O$ ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....	$\pm 35$ mA
Continuous Current Through $V_{CC}$ or GND pins .....	$\pm 125$ mA
Storage Temperature Range, $T_{stg}$ .....	-65°C to +150°C
Power Dissipation Per Package, $P_d$ † .....	500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
Plastic Package (N): -12mW/°C from 65°C to 85°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ .....	4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}$ , $V_{OUT}$ ..	0V to $V_{CC}$
Operating Temperature Range	
Range	KS74HCTLS: -40°C to +85°C KS54HCTLS: -55°C to +125°C
Input Rise & Fall Times, $t_r$ , $t_f$ .....	Max 500 ns
Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)	

### DC ELECTRICAL CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Minimum High-Level Input Voltage	$V_{IH}$			2.0	2.0	2.0			V
Maximum Low-Level Input Voltage	$V_{IL}$			0.8	0.8	0.8			V
Minimum High-Level Output Voltage	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7			V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4			V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND $V_{IN}=15V$		$\pm 0.1$	$\pm 1.0$ $\pm 10.0$	$\pm 1.0$ $\pm 10.0$			$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0			$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0			mA

### AC ELECTRICAL CHARACTERISTICS (Input $t_r$ , $t_f \leq 6$ ns), HCTLS4049, HCTLS4050

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$		KS74HCTLS $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
Maximum Propagation Delay	$t_{PLH}$	$C_L = 50\text{pF}$	13	17	21	26			ns
	$t_{PHL}$		13	17	21	26			
Maximum Input Capacitance	$C_{IN}$		5						pF
Power Dissipation Capacitance*	$C_{PD}$	(per gate)							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f_{in}$ .

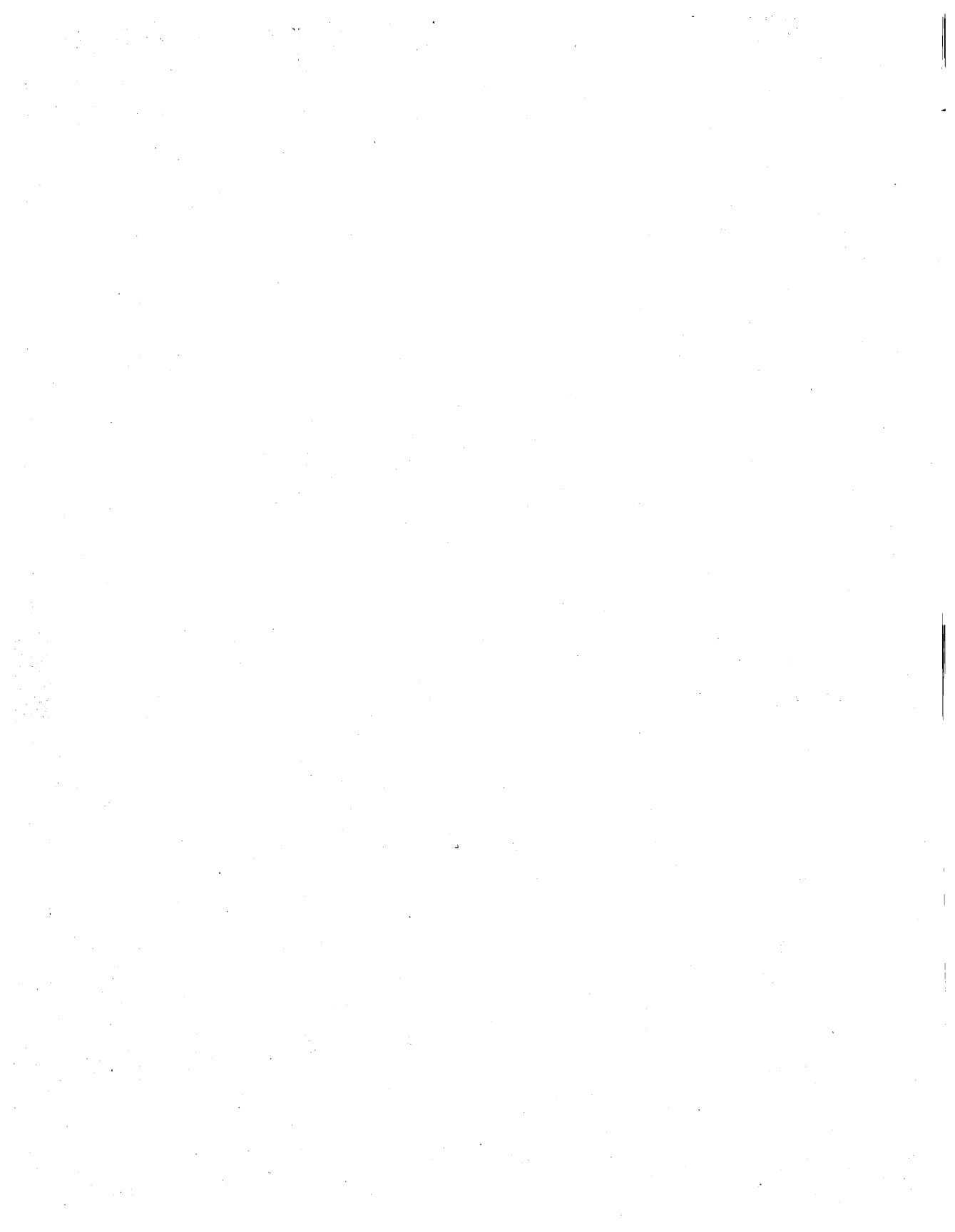
† For AC switching test circuits and timing waveforms see section 2.

A black and white photograph showing a person from behind, wearing a white protective suit with a circular patch on the back. They are seated at a desk, operating a vintage computer terminal. The terminal consists of a CRT monitor displaying a graphical interface with a grid and a keyboard. The person's hands are on the keyboard. The background is slightly out of focus, showing other equipment.

***PACKAGE DIMENSIONS &  
ORDERING INFORMATION***

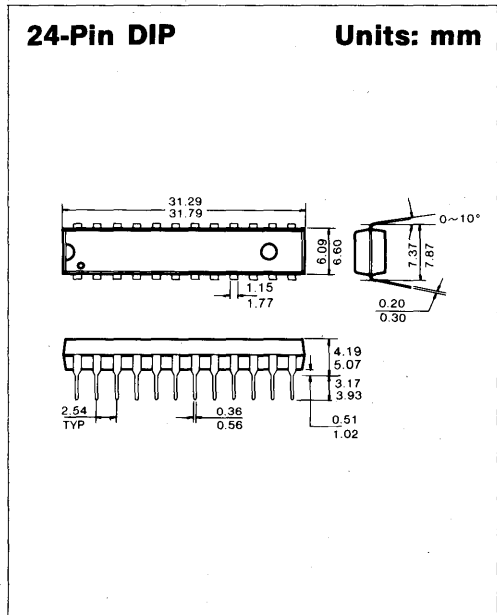
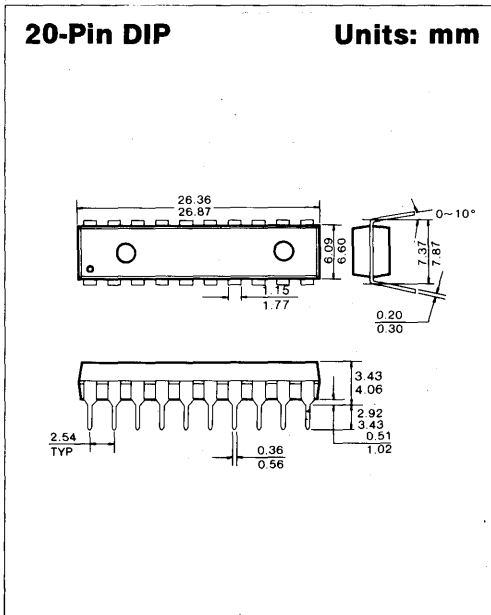
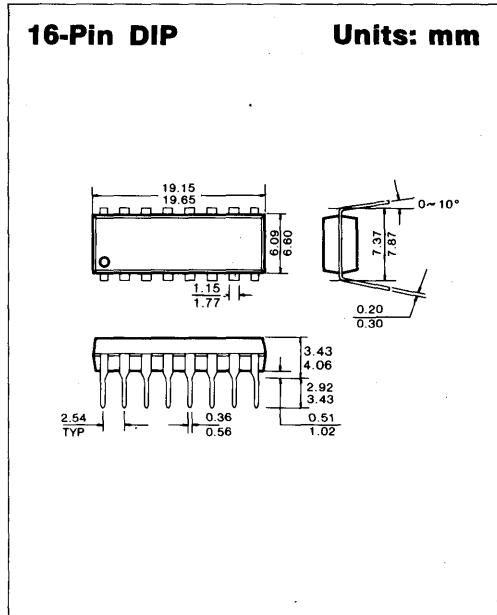
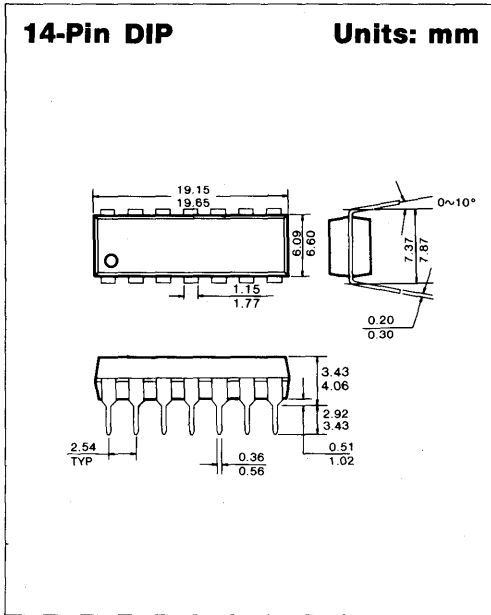
6





# PACKAGE DIMENSIONS

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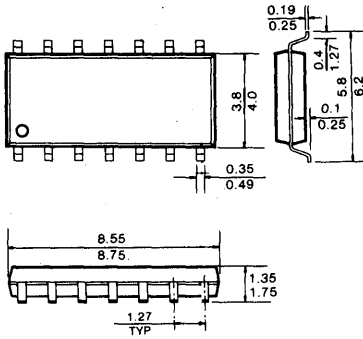


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# PACKAGE DIMENSIONS

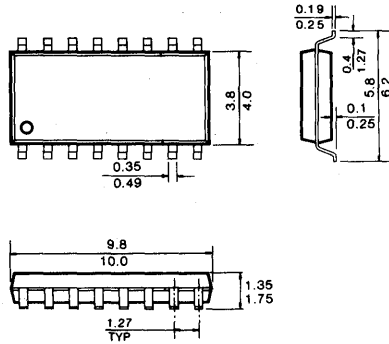
14-Pin SOP

Unit: mm



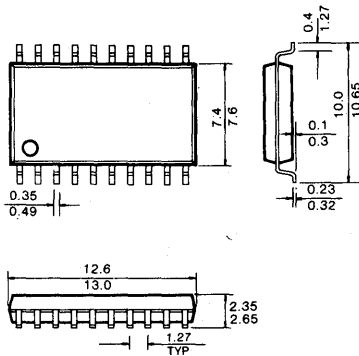
16-Pin SOP

Unit: mm



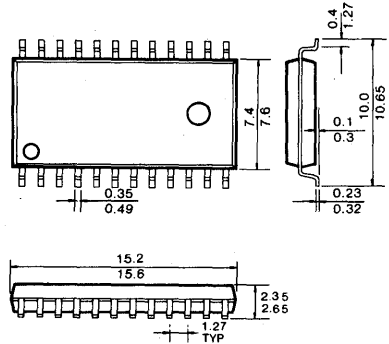
20-Pin SOP

Unit: mm



24-Pin SOP

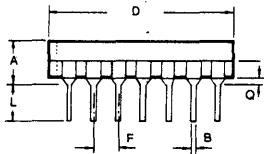
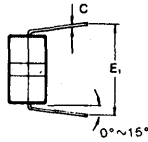
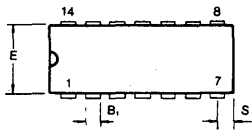
Unit: mm



# PACKAGE DIMENSIONS

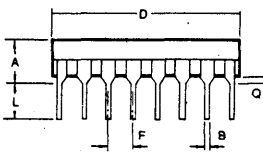
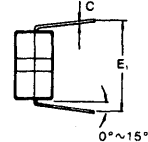
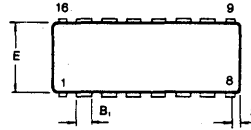
## 2. CERAMIC PACKAGES

### 14-Pin Ceramic DIP Units: mm



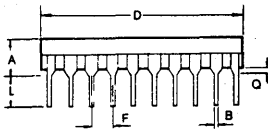
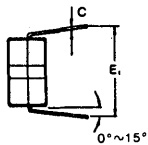
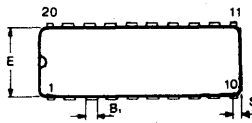
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B <sub>1</sub>	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E <sub>1</sub>	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

### 16-Pin Ceramic DIP Units: mm



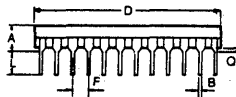
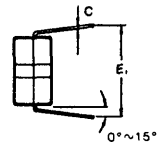
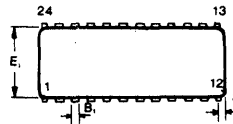
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B <sub>1</sub>	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E <sub>1</sub>	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

### 20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B <sub>1</sub>	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E <sub>1</sub>	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

### 24-Pin Ceramic DIP Units: mm

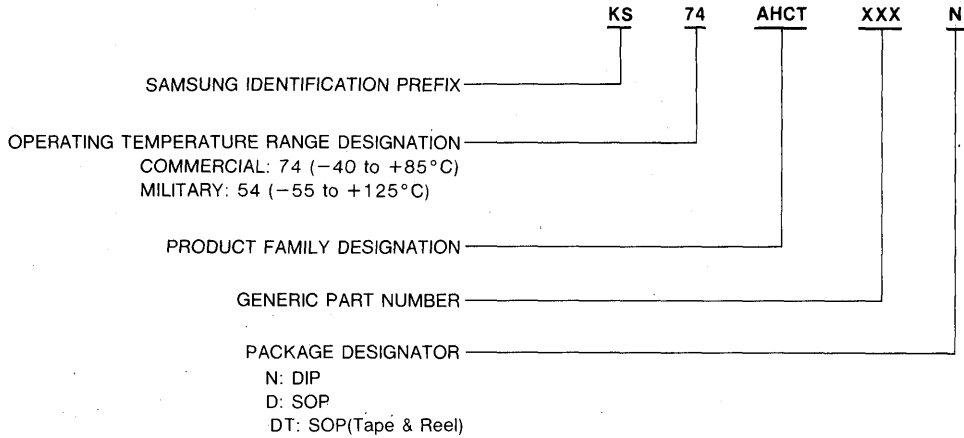


DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B <sub>1</sub>	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E <sub>1</sub>	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.776
S	1.85	1.93

# ORDERING INFORMATION

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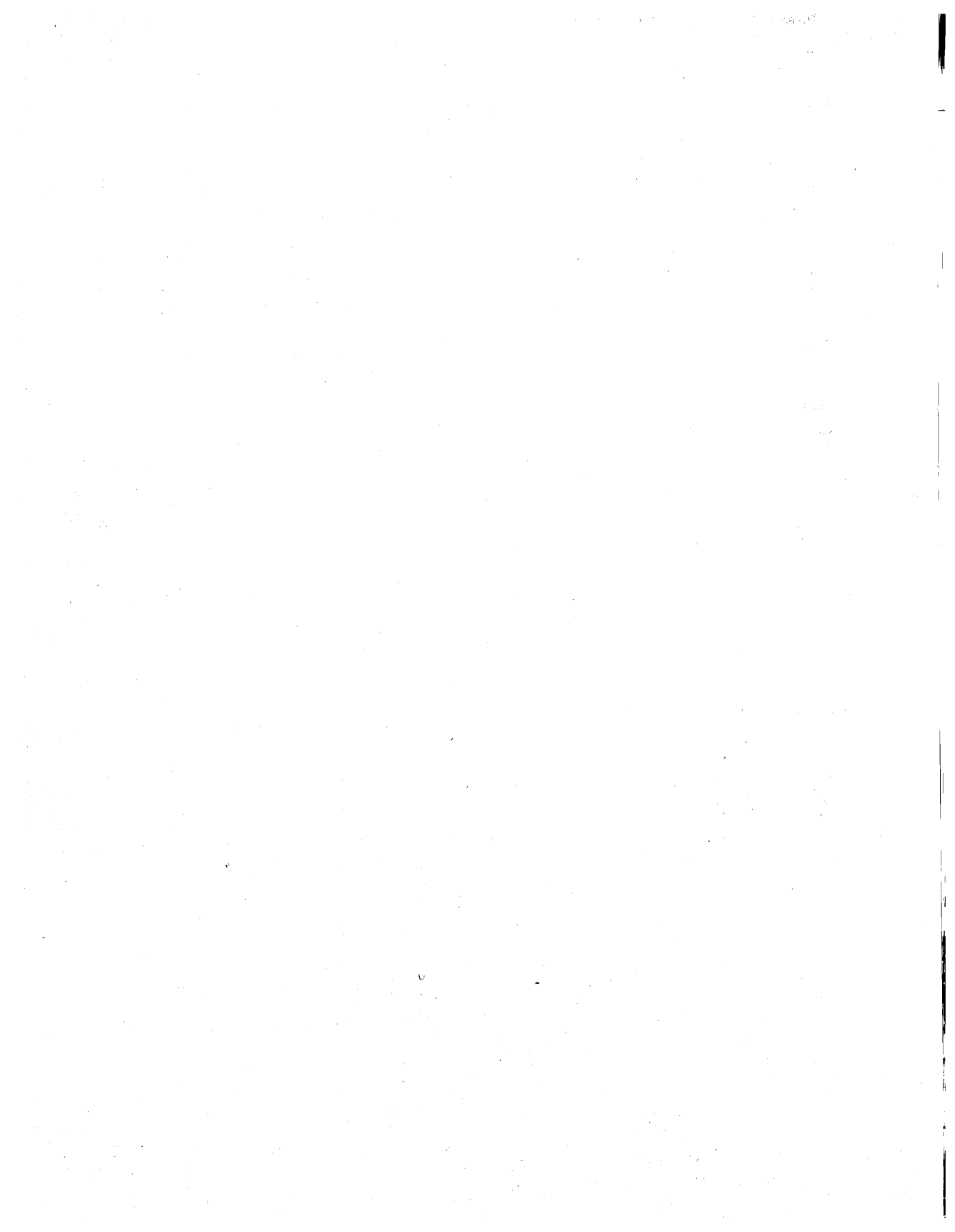
To ensure prompt and accurate processing of your order, please use the product code system as described in the following example.



Pin	Quantity/Reel
SO-14	3000
SO-16	3000
SO-20	1000
SO-24	1000



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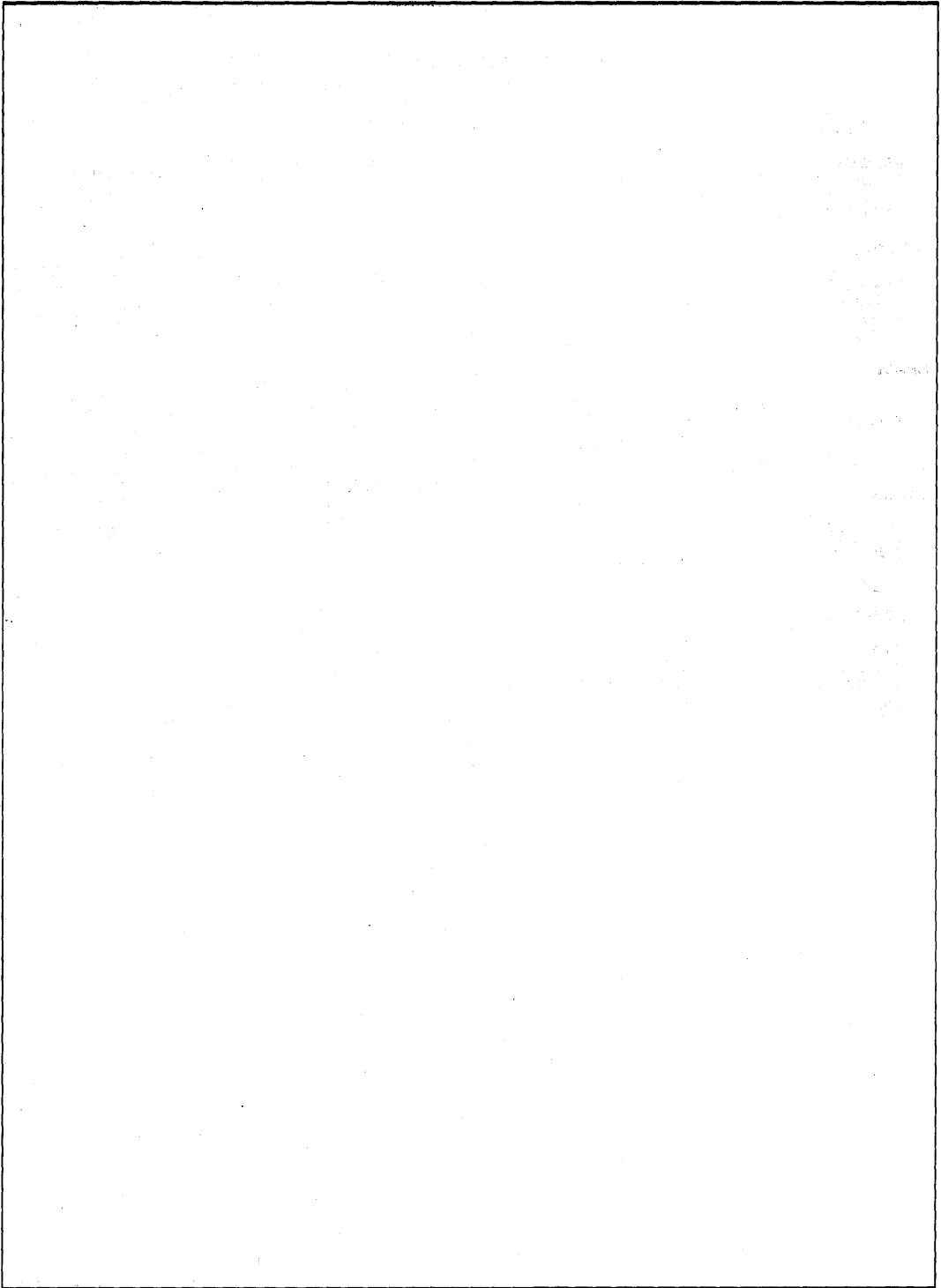
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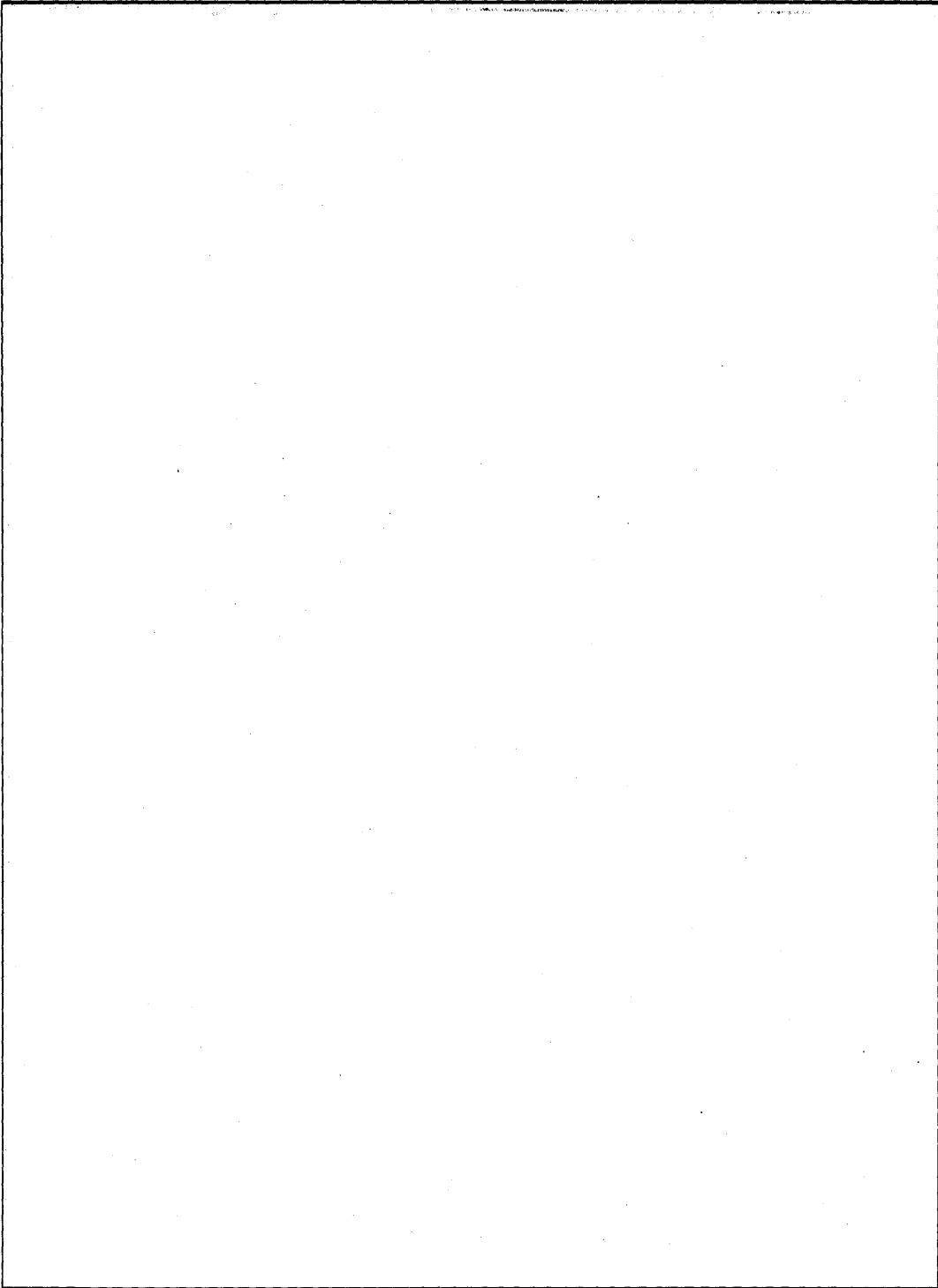
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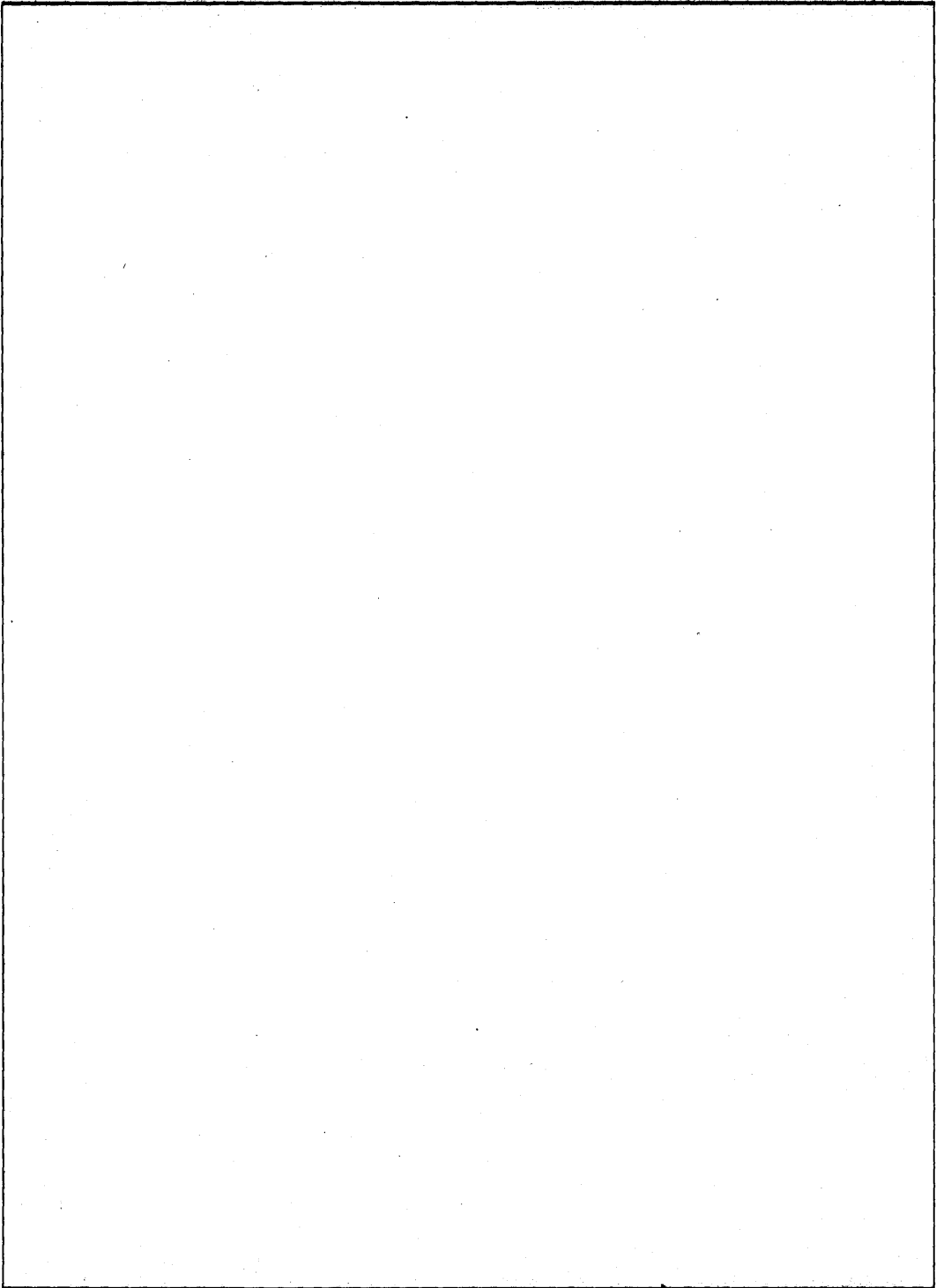
# NOTES



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