NEC ELECTRONICS (EUROPE) GMBH

SYSTEM SPECIFICATION

µPD 7762
µPD 7761
MC 4760

1/83 V1.0
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SYSTEM SPECIFICATIONS µPD7762, µPD7761, MC4760

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1. System Configuration

NEC's voice recognition LSI has been developed with the goal of simplifying the normally highly complicated voice recognition process.

Voice recognition consists of an analysis process, which analyzes input voice data, and a recognition process, which performs matching calculation of registered voice data against input voice data that has been analyzed by the first process. These processes are performed by two voice recognition LSIs and an RIC. The RIC (MC-4760) integrates amplifier, equalizer and A/D converter functions and serves as an analog interface.

As for the two voice recognition LSIs, one is the control LSI (µPD7762) which controls operation of the system and the other is the calculation LSI (µPD7761) which performs analysis and matching calculations using an 8-channel band-pass filter.

By employing the compression DP matching algorithm, the voice recognition system consisting of the abovementioned three chips recognizes a maximum of 128 words of single-word input by a specific speaker with an average recognition response time of 0.7 sec. and a minimum recognition rate of 98% when using a 16K-byte memory.

A system configuration using a 64K-byte memory accordingly allows a maximum of 512 words to be registered in the system.

Fig. 1.1 shows a system configuration.
Fig. 1.1 System Block

EXTERNAL SYSTEM

[HOST]
SYSTEM

System Interface

serial
RS 232C
parallel

CONTROL PROCESSOR
(μPD 7762)

serial

ARITHMETIC PROCESSOR
(μDP 7761)

bus

PATTERN MEMORY

ANALOG INTERFACE
(MC 4760)

TAPE
MIC

1-3
Fig. 2.2 Functional Relation of Voice Recognition Chips

Host System

Command

Recognition result

02 Error Code

μPD 7762

Matching

Result

Analysis

μPD 7761

Speech data (serial)

MC 4760

Speech in

Memory

search
cataloging
2.1.3 Serial interface (7762)

Since the 7762 is provided with a built-in serial port, it can be controlled directly when connected to a host system equipped with a compatible serial port. The serial clock for this kind of I/O operation must be provided externally.

A configuration example and basic timing are shown in Figs. 2.9 and 2.10, respectively. I/O of control commands through the serial port of the 7762 have the following points that require special attention. (Refer to Fig. 2.4.)

Input operation (Host to 7762)
After the host system has sent the control commands and terminator to the 7762, it must also send dummy data (00H). If this dummy data is not sent, the wrong data may be output. (For descriptions of the commands and the terminator, refer to 2.2.)

Output operation
The 7762 outputs a response (recognition result or error code) to the host system. Unlike the input operation, dummy data will not be sent. (For details of the response of 7762, refer to 2.2.)

NOTE: Input of the dummy data causes the SAK to be low level.
(1) Read cycle

\[ \phi_{out} \]

\[ \overline{RD} (7762) \]

\[ IO/\overline{M} (7762) \]

\[ ACK (8255) \]

\[ OBF (8255) \]

\[ PA_7-\beta (8255) \]

\[ DB_{7-\beta} (7762) \]

\[ INTR (8255) \]

NOTE: T1 means 1 machine cycle

(2) Write cycle

\[ \phi_{out} \]

\[ \overline{WR} (7762) \]

\[ IO/\overline{M} (7762) \]

\[ STB (8255) \]

\[ IBF (8225) \]

\[ DB_{7-\beta} (7762) \]

\[ PA_7-\beta (8255) \]

\[ INTR (8255) \]

Fig. 2.6 Basic Timing of Parallel Interface (8255)
(1) Read cycle
8251-7762
\[ \phi_{\text{out}} \]
\[ \text{AB}_{15-0}, \text{C/D} \]
\[ \text{IO/M} \]
\[ \text{RD} \]
\[ \text{CS} \]
\[ D_{7-0} (8251) \]
\[ DB_{7-0} (7762) \]

(2) Write cycle
8251-7762
\[ \phi_{\text{out}} \]
\[ \text{AB}_{15-0}, \text{C/D} \]
\[ \text{IO/M} \]
\[ \text{WR} \]
\[ \text{CS} \]
\[ D_{7-0} \]
\[ DB_{7-0} \]
(1) Serial Input  Host system to 7762

NOTES: # indicates the data transfer inside of the 7762. 
will be the status of the last output. This 
* becomes 0 immediately after the reset operation.

Fig. 2.10 Basic Timing of 7762 Serial Interface.
## Table 2.1 μPD7762 Command Summary

<table>
<thead>
<tr>
<th>Command Name</th>
<th>Command Format</th>
<th>Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>INITIALIZE</td>
<td>00H, OFFH</td>
<td>2</td>
</tr>
<tr>
<td>LEVEL ADJUST</td>
<td>01H [Bank No.] [Bank No.] [Bank No.] [Bank No.] OFFH</td>
<td>6 max.</td>
</tr>
<tr>
<td>TRAINING</td>
<td>02H, Record No. [Syntax No. Word reject value] OFFH</td>
<td>5 max.</td>
</tr>
<tr>
<td>RECOGNITION</td>
<td>03H, [Syntax No. ] [ ] [Syntax No.] OFFH</td>
<td>33 max.</td>
</tr>
<tr>
<td>SECOND DECISION</td>
<td>04H, OFFH</td>
<td>2</td>
</tr>
<tr>
<td>ROT START</td>
<td>05H, OFFH</td>
<td>2</td>
</tr>
<tr>
<td>DOWN LOAD</td>
<td>06H, Registration No., OFFH, Parameter</td>
<td>No. of parameter + 3</td>
</tr>
<tr>
<td>UP LOAD</td>
<td>07H, OFFH (Used with DOWN LOAD in a pair.)</td>
<td>2</td>
</tr>
<tr>
<td>CHANGE REJECT LEVEL</td>
<td>08H, Word reject value, OFFH</td>
<td>3</td>
</tr>
<tr>
<td>MEMORY TEST</td>
<td>09H, OFFH</td>
<td>2</td>
</tr>
<tr>
<td>BANK SELECT</td>
<td>0AH, Bank No., OFFH</td>
<td>3</td>
</tr>
<tr>
<td>TIMER SET</td>
<td>0BH, Timer value, OFFH</td>
<td>4</td>
</tr>
<tr>
<td>WORD REJECT</td>
<td>0CH, Record No., Word reject value, OFFH</td>
<td>4</td>
</tr>
<tr>
<td>ARO SET</td>
<td>0DH, OFFH</td>
<td>2</td>
</tr>
<tr>
<td>LOAD DATA</td>
<td>0EH, Address, No. of data, OFFH, data, data</td>
<td>10 + No. of data</td>
</tr>
<tr>
<td>EXECUTE</td>
<td>0FH, Address, OFFH</td>
<td>6</td>
</tr>
</tbody>
</table>

**NOTES:**
1. OFFH: Terminator
2. The items enclosed in brackets ([ ]) can be omitted.
Function: Registering the voice pattern

* Voice data is input through the MC-4760 and analyzed by the µP/7761.
* In accordance with the record No., the registered voice pattern and the representative data are set in the table and the syntax No. and word reject value are entered in the dictionary.
* Syntax No. and word reject value are used during voice recognition.

Output code: 00H (acknowledge): Normal completion

All other outputs are error codes.

NOTE: See System Configuration Drawing Fig. 2.12.

(4) RECOGNITION
Command format: 03H [syntax No.] [syntax No.] [---]

0FFH
0 < syntax No. < 128
However, the maximum number of syntax Nos. that can be set is 31.
If syntax No. is omitted, 0 is assumed.

Function:
To input voice data, perform DP matching calculations against the registered voice patterns and output the result to the host system.
* Voice data is input through the MC-4760 and analysis is performed by the µPD7761.
* DP matching calculations are performed to compare the input voice pattern against each of the registered voice patterns with the specified syntax No(s).
(5) SECOND DECISION

Command format: 04H, OFFH

Function: To output the registered voice pattern found to have the second smallest distance from the input voice pattern. Valid only after execution of RECOGNITION command.

Output code: 00H (Acknowledge): Normal completion
After output of the acknowledge code, the record No. and the distance will be output.
Any output other than the acknowledge code will be an error code. However, in the case of error code 0AH, record No. and distance will also be output. In all other cases, only the error code will be output.

(6) HOT START

Command format: 05H, OFFH

Function: To initialize all elements of the chip set system except the memory.
- Initializes serial ports 8251 and 8255.
- Resets the 7761.
- Initializes the gain of the MC-4760.

Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(7) DOWNLOAD

Command format: 06H No. of registered patterns, OFFH, parameters

1 \leq \text{No. of registered patterns} \leq 128
Parameters are described below.

Function: To load the registered voice pattern data from the host system to the current memory bank.
- Erases the registered voice pattern data in the current bank memory.
Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(12) TIMER SET
Command format: OBH, timer value, OFFH
Timer value in 2 bytes is transmitted in the order of low- to high- order bits. 12 bits are effective.
Function: To set a value in the timer of the 7762 and to activate the timer.
  * The timer is a 12-bit down counter and counts at speeds of 4 µS to 16 ms, with a resolution of 4 µS. Causes the output of a time-out signal from the TO terminal of the 7762.
Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(13) WORD REJECT
Command format: OCH, record No., word reject value, OFFH
Function: To set the word reject value for the specified record No.
Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(14) ARO SET
Command format: ODH, OFFH
Function: A data setting command to be used for the record/reproduction board (PC-8012-04).
  * Outputs D, P, R and E.
Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(15) LOAD DATA
Command format: OEH, address, No. of data, OFFH, data address and No. of data are input in units of 4 bytes. The first 2 bytes input the low byte and the next 2 bytes, the high byte, respectively.
to set very strict conditions for recognition of a single word (a code word, for example,) so that it will only be recognized when it is carefully and accurately pronounced.

2.2.4 Parameters for UP LOAD and DOWN LOAD

Input of UP LOAD or DOWN LOAD command enables I/O of registered voice pattern data with the host system. The UP LOAD command, outputs the acknowledge code, and then causes output of the No. of registered voice patterns, reject value table, record No., dictionary table, registered voice pattern table, extraction table, and next record No., in the above order. This operation may be repeated as many times as the number of the registered data.

Input of the DOWN LOAD command, on the other hand, after outputting the acknowledge code, causes the reject value table, record No., dictionary table, registered voice table, representative data table, and the next record No. to be output in that order and this output may be repeated for each registered voice pattern.

* Reject value table ............... 2 bytes
  Record No. ........................ 1 byte
  Dictionary table .................. 6 bytes
  Registered voice pattern table ... 64 bytes (16 frames)
  Representative data table ........ 16 bytes (16 frames)

Output of items marked ** may be repeated for the number of registered voice patterns.
* Reject value table referred to here is for the bank reject value.
NOTE: The numbers indicate the phase

Fig. 2.11 Block Diagram of LEVEL ADJUST Command
Fig. 2.13 Block Diagram of RECOGNITION Command

NOTE: The status of each phase is shown in Figs. 2.14 to 2.16.
Phase 2
Reset input
(7761-7762)

Mode code input
(7761-7762)

Phase 3
Data transmission request
(7761-7762)

Analysis process

Data transmission

Voice data input from MC-4760

NOTE: Data transmitted, power and channel data: Total 10 bytes.
Phase No.s correspond to those in Fig. 2.13
3. System Configuration

This chapter describes the features, terminal connections and functions of the µPD7762, µPD7761 and MC-4760 chips which make up the voice recognition chip set system. Brief explanations of the memories and clock are also presented.

3.1 µPD7762

3.1.1 Introduction

The µPD7762 is the control LSI of the voice recognition chip set and performs interfacing with the host system, receives commands from the host system, performs memory management and controls the µPD7762 and MC-4760.

3.1.2 Features

- Control LSI for the voice recognition LSI set.
- Connectable to an external memory of 64K bytes max. (addresses 1000H to FF7FH)
- µPD8255 interface port (fixed I/O addresses)
- µPD8251 interface port (fixed I/O addresses)
- Built-in serial interface
- Built-in clock oscillator (external drive (1 to 4MHz) also possible.)
- N-channel MOS
- 5V single power supply
- 64-pin QUFP plastic package
3.1.4 Terminal functions

(1) DB0 to DB7 (Data bus) 3-state input/output
   8-bit bidirectional data bus.
   Output becomes high during input mode and reset operation.

(2) AB0 to AB15 (Address bus) output
   16-bit address bus for setting memory and specifying
   I/O addresses. Memory addresses are from 1000H to
   FF7FH.

(3) SAK (Serial acknowledged) output
   Outputs data transfer status when the serial port is
   used.

(4) SCS (Serial chip select) input
   This pin should be connected to the GND terminal when
   the serial port is used.

(5) IO/M (I/O or memory) output
   This pin outputs low level during memory access; at
   all other times, high level is output.

(6) ATC0 - ATC5 (Attenuator control) output
   Output signal for control of the MC-4760 attenuator.

(7) SEL0, SEL1 (I/F Select) input
   Input terminal for selection of the external interface.

<table>
<thead>
<tr>
<th>SEL0</th>
<th>SEL1</th>
<th>I/F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>µPD8255 parallel</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>µPD7762G serial</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>µPD8251 RS-232C</td>
</tr>
</tbody>
</table>

(8) MMO, MML (Memory mode) input
   Input terminal for specification of the memory area

<table>
<thead>
<tr>
<th>MMO</th>
<th>MML</th>
<th>Memory area</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>64K bytes</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>16K bytes</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>32K bytes</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>48K bytes</td>
</tr>
</tbody>
</table>

(9) OBF, IBF input
   When the µPD8255 is used, these terminals are used
   for input of control signals OBF and IBF from the
   µPD8255, and are left open when µPD8255 is not used.
(20) **RE (Refresh enable) output**
Output terminal for refresh enable when using the DRAM in the µPD7762G memory. While this signal is high level, the memory of µPD7762G will not be accessed.

(21) **WAIT input**
Input terminal for wait signal when using the slow RAM in the memory. The wait signal is checked at the end of the T2 cycle and if it is low, the wait cycle (Tw) will be repeated until it becomes high.

(22) **C.G. (Contact ground) input**
This pin is connected to the GND terminal.

(23) **DORQ (Data output request) input**
Input terminal for data transfer request signal from the µPD7761. When this signal is high, the 7762 receives data from the 7761 via the data bus.

(24) **HST (Hot start) input**
Input terminal for hot start request signal from the hardware. After detection of the rising edge, if high level on this signal is maintained for 4μS (4MHz clock), a request signal will be assumed.

(25) **Vcc**
+5V power supply.

(26) **GND**
0V

3.1.5 Reset operation of 7762
When a low level signal is applied to the RESET terminal for more than 4μS (4MHz clock), internal reset of the 7762 will be performed. After reset, the 7762 will perform the following operations.
- Outputs a high level signal to the RST terminal for at least 3 clock pulses to reset the 7761.
- Performs mode setting of the 8251.
- Reads the dummy data in the PA port of the 8255 and initializes the timing with the 8255. (Mode setting of the 8255 must be complete before timing can be initialized.)
- Sets the serial port of the 7762 in the input mode.
3.1.10 7762 clock signal generator

The clock signal for the µPD7762G is provided either by the internal crystal oscillator circuit or by an external clock signal generator.

The circuit examples for internal and external clocks are shown below.

(1) Internal clock circuit (reference)

![Internal Clock Circuit](image1)

(2) External clock circuit (reference)

![External Clock Circuit](image2)
(i) Memory read (From memory to 7762)

(ii) Memory write (From 7762 to memory)

NOTE: *Input the wait cycle when a slow memory is being used.

Fig. 3.2 Access Timing of Memory
3.2 μPD7761

3.2.1 Introduction
The μPD7761 performs calculation process such as analysis of voice data, matching calculation of input voice patterns against registered voice patterns, and so forth.

3.2.2 7761 features
- Analysis and matching calculation processor for the voice recognition LSI set.
- Data communications with the 7762 are performed through the data bus using a handshake signal.
- Voice analysis is performed by an 8-channel biquad digital filter.
- Control is by 16-bit mode code from the 7762.
- Built-in serial port for input of voice data from MC-4760
- Fixed I/O addresses (as viewed from the 7762)
- Clock signal frequency: 8MHz ~ 1MHz
- N-channel MOS
- +5V single power supply
- 28-pin DIP ceramic package
3.2.4 Terminal functions

(1) D0 ~ D7 (Data bus) 3-state I/O
   8-bit bidirectional data bus for I/O of data and
   mode codes with the 7762.

(2) A0 (Address select) input
   Input terminal used to select between access of the
   data register (DR) and the status register (SR)
   of the 7761.
   When A0 is 0, DR is selected and when A0 is 1, SR is
   selected.

(3) CS (Chip select) input
   When this signal is high, D0 ~ D7 are enabled for I/O.

(4) RD (Read) input
   Read control signal used when reading the contents of
   either DR or SR.

(5) WR (Write) input
   Write control signal used when writing to DR.

(6) DORQ (Data output request) output
   Output signal to request data transfer from the
   7762.

(7) DVI (Digitized voice input) input
   Input for voice data after it has been converted
   to 8-bit digital data by MC-4760.

(8) CG (Contact ground) input
   Connects to GND.

(9) SMPL0, SMPL1 (Sampling clock) input
   Inputs terminal for A/D strobe signal. Signal input
   is 10 KHz sampling clock; normally, this is the
   reverse phase of the signal input to the SMPL termi-
   nal of the MC-4760.

(10) SCLK (Serial clock) input
    The reverse phase of the signal input to the CLK
    terminal of the MC-4760 is input. This signal is
    synchronized with that clock and provides timing for
    the input of voice data from DVI.

(11) RST (Reset) input
    Input terminal for reset signal to initialize the
    internal system of the uPD7761D. To initialize the
The 7761 is first synchronized with the SCLK (serial clock) signal; 8-bit digitized voice data from the MC-4760 is then input to the 7761 through the DVI terminal.

The frequency of the voice data input is analyzed by an 8-channel digital filter and the power is calculated.

After all analysis processes have been completed, the 7761 sends a DORQ signal to the 7762, indicating the end of the process.

Through the data bus, the 7761 then sends a 2-byte code (00H) to the 7762 which indicates that the result to be output is that of the analysis process. (The code is sent starting from the lower-order byte.)

Then, power data and data for CH1 to CH8 is sent to the 7762 in units of 2 bytes in the order of the lower-order byte to the higher-order byte.

When the data transmission is completed, the 7761 will re-enter the WAIT state, and wait for input of the next reset signal from the 7762.

(4) Matching calculation mode (mode code = 8xxxH)

When the 7761 is set in matching calculation mode by input of a mode code from the 7762, the following operations will be performed.

- The number of frames of input voice pattern data is sent from the 7762 to the 7761 as 1 byte of data.
- Input voice pattern data (4 bytes) and representative data (1 byte) are input from the 7762 for the number of frames of voice data.
- Number of frames of registered voice pattern data is input from the 7762 as 1 byte of data
- Registered voice pattern (4 bytes), cutoff parameters and representative data (1 byte) are input for the above number of frames.
- Matching calculation will be performed for the two sets of data (input and registered voice patterns).
The voice data sent from the 4760 to the 7761 through the DVI terminal of the 7761 is synchronized with SCLK. Although the data from the 4760 normally flows to the DVI terminal of the 7761, the selection of whether or not to accept data is made internally at the 7762. For input timing for serial data, refer to the section on the MC-4760.

3.2.8 Serial clock and reset of 7761 and 4760
Serial voice data input to the 7761 from the 4760 is synchronized with the serial clock input to the SCLK terminal of the 7761 and the terminal CLK of the 4760. Therefore, when the 7761 is reset, it is also necessary to reset the serial clock at the same time. If this reset operation is not performed, normal data transmission may not be possible.

3.3 MC-4760
3.3.1 Introduction
The MC-4760 is an integrated voice input circuit designed to perform optimum analysis of voice band signals. Voice signals are input from a microphone or a tape, amplified and equalized. They are then converted from analog to digital signals by the A/D converter and output as serial data. Furthermore, the built-in digital attenuator enables the 7762 to perform gain adjustment.

3.3.2 Features
- IC performs analog interfacing for the voice recognition LSI set.
- Built-in variable amplifier with external resistor
- Built-in equalizer
- 8-bit TTL control digital attenuator incorporated
- 8-bit A/D serial output (MSB first)
- Built-in lowpass filter for elimination of foldover noise
3.3.3 MC-4760 Terminal connections

MC-4760 pin connection

Top view

N.C: Non connection

* DVO: Digital Voice Out
(13) LPF OUT (Lowpass filter output) output
Observation terminal for the analog signal immediately before A/D conversion. Do not connect the load to this terminal.

(14) LINE IN (Line input) input
For voice input from a tape. Input impedance: 10kΩ.
Maximum input level: ±0.6O-p
(when sin wave calculation: EQL AMP: 20dB, Attenuator valve: 7FH)
3.3.7 Others

(1) G ADJ

The G ADJ terminal is an external resistance terminal which determines the gain of the variable amplifier in the MC-4760. The relation of the external resistance to gain, and the mounting method of the resistor are shown in Table 3.1 and Fig. 3.4, respectively.

Table 3.1 Changes Effected in Gain by External Resistance

<table>
<thead>
<tr>
<th>Resistance (Ω)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>0.6</td>
</tr>
<tr>
<td>1100</td>
<td>10</td>
</tr>
<tr>
<td>505</td>
<td>15</td>
</tr>
<tr>
<td>258</td>
<td>20</td>
</tr>
<tr>
<td>138</td>
<td>25</td>
</tr>
<tr>
<td>75 *</td>
<td>30</td>
</tr>
</tbody>
</table>

Gain is obtained by the following formula.

\[
G = 20 \left\{ \log \frac{R}{10} \right\} + 1.9 + \frac{(4.3)^2 + 8.6}{10}
\]

where:

- G: gain (dB)
- R: resistance (kΩ)

* Do not use a resistance of less than 75Ω.

Fig. 3.4 Connecting External Resistor
Table 3.2 ATC Value and Output Voltage

<table>
<thead>
<tr>
<th>ATC value (HEX)</th>
<th>Output voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>$-V_{REF} \left(\frac{255}{256}\right)$</td>
</tr>
<tr>
<td>81</td>
<td>$-V_{REF} \left(\frac{129}{256}\right)$</td>
</tr>
<tr>
<td>80</td>
<td>$-V_{REF} \left(\frac{128}{256}\right) = -\frac{1}{2} V_{REF}$</td>
</tr>
<tr>
<td>7F</td>
<td>$-V_{REF} \left(\frac{127}{256}\right)$</td>
</tr>
<tr>
<td>01</td>
<td>$-V_{REF} \left(\frac{1}{256}\right)$</td>
</tr>
<tr>
<td>00</td>
<td>$-V_{REF} \left(\frac{0}{256}\right) = 0$</td>
</tr>
</tbody>
</table>

$V_{REF} = \text{Input voltage to internal attenuator}$

$1\text{LSB} = (2^{-8}) V_{REF}$

(3) MIC input amplifier and A/D converter

The abbreviation 'AMP' in the block diagram in 3.3.5 denotes the MIC input amplifier, which is used to amplify voice signals as they are input from a microphone. The specifications of this amplifier are as follows:

- **Gain**: 40dB
- **Input impedance**: 1kΩ
- **Band**: BPF of 100Hz to 10KHz

The A/D converter is used to convert voice signals input from a microphone or tape into digital signals. The ratings of the A/D converter conform to CODEC standards.
(6) Cautions in using memory
Although both SRAM and DRAM memories can be used, the memory capacity must be large enough to derive the bank configuration described on the preceding page. There are difficulties involved in the adoption of commercially available memories in that the read cycle of the 7762 is very fast and the minimum delay time until data read begins after the RD signal becomes high is only 350ns. Therefore, it is necessary to insert one "wait" in the read cycle (this will result in a delay time of 850ns.). In comparison, the write cycle does not require the insertion of any wait time. Timing calculations are based on CLK of 4MHz and $f_{out}$ of 2MHz.

Fig. 3.5 Circuit Example to Generate One "Wait" in Read Cycle
4. Specifications

4.1 Introduction

This voice recognition system comprises three LSI chips: \( \mu P D7762 \), \( \mu P D7761 \) and \( MC-4760 \). The detailed specifications for each chip are presented below.
**AC Characteristics** \( (T_a = -10 \to +70^\circ C, \ V_{CC} = \pm 5.0 \pm 10\% ) \)

**Clock timing:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1 - Input cycle time</td>
<td>CYX</td>
<td>227</td>
<td>1000</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>X1 - Input low pulse width</td>
<td>XXL</td>
<td>105</td>
<td>105</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>X1 - Input high pulse width</td>
<td>XXH</td>
<td>454</td>
<td>2000</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>pOUT - Cycle time</td>
<td>CYp</td>
<td>150</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>pOUT - Low pulse width</td>
<td>pL</td>
<td>150</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>pOUT - High pulse width</td>
<td>pH</td>
<td>150</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>pOUT - Raise/fall time</td>
<td>tr.tf</td>
<td>150</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Read/write operation:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD L.E. - pOUT L.E.</td>
<td>RE</td>
<td>100</td>
<td>550+500xN</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Address (AB0-15) - Data input</td>
<td>ADI</td>
<td>200</td>
<td>350+500xN</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RD T.E. - Address</td>
<td>RA</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD L.E. - Data input</td>
<td>RD</td>
<td>0</td>
<td>850+500xN</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RD T.E. - Data hold time</td>
<td>RDH</td>
<td>250</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD Low pulse width</td>
<td>RR</td>
<td>850</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD L.E. - WAIT L.E.</td>
<td>RWT</td>
<td>450</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address (AB0-15) - WAIT L.E.</td>
<td>AWT1</td>
<td>650</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WAIT Setup time (for pOUT L.E.)</td>
<td>WTS</td>
<td>290</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WAIT Hold time (for pOUT L.E.)</td>
<td>WTH</td>
<td>200</td>
<td>120</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RE - RD L.E.</td>
<td>MR</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD T.E. - RE</td>
<td>RM</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO/M - RD L.E.</td>
<td>IR</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD T.E. - IO/M</td>
<td>RI</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>pOUT L.E. - WR L.E.</td>
<td>pW</td>
<td>40</td>
<td>125</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Address (AB0-15) - pOUT T.E.</td>
<td>AØ</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address (AB0-15) - Data output</td>
<td>ADZ</td>
<td>450</td>
<td>600+500xN</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data output - WR T.E.</td>
<td>DW</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WR T.E. - Data stable time</td>
<td>WD</td>
<td>400</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address (AB0-15) - WR L.E.</td>
<td>AW</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WR T.E. - Address stable time</td>
<td>WA</td>
<td>600+500xN</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WR Low pulse width</td>
<td>WW</td>
<td>500</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO/M - WR L.E.</td>
<td>WI</td>
<td>250</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Timing of $^{1}CY^{0}$-dependent bus parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Formula</th>
<th>MIN./MAX.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{RC}$</td>
<td>$(1/5)\ T$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ADT}$</td>
<td>$(3/2+N)\ T-200$</td>
<td>MAX.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RA}$</td>
<td>$(1/2)\ T-50$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RD}$</td>
<td>$(1+N)\ T-150$</td>
<td>MAX.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RR}$</td>
<td>$(2+N)\ T-150$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RWT}$</td>
<td>$(3/2)\ T-300$</td>
<td>MAX.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AWT1}$</td>
<td>$(2)\ T-350$</td>
<td>MAX.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ER}$</td>
<td>$(1/2)\ T-50$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RE}$</td>
<td>$(1/2)\ T-50$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IR}$</td>
<td>$(1/2)\ T-50$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{RI}$</td>
<td>$(1/2)\ T-50$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{W}$</td>
<td>$(1/4)\ T$</td>
<td>MAX.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{A4}$</td>
<td>$(1/5)\ T$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ADZ}$</td>
<td>$T-50$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DW}$</td>
<td>$(3/2+N)\ T-150$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WD}$</td>
<td>$(1/2)\ T-100$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{AW}$</td>
<td>$T-100$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WA}$</td>
<td>$(1/2)\ T-50$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WW}$</td>
<td>$(3/2+N)\ T-150$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{IW}$</td>
<td>$T$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{WI}$</td>
<td>$(1/2)\ T$</td>
<td>MIN.</td>
<td>ns</td>
</tr>
</tbody>
</table>

NOTES: 1. No. of wait states
2. $T = ^{1}CY^{0}$
AC characteristics ($T_a = -10 \sim 70 \, ^\circ C, V_{cc} = +5.0 \, V \pm 5\%$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK cycle time</td>
<td>$\delta_{CY}$</td>
<td></td>
<td>122</td>
<td>1000</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK pulse width</td>
<td>$\delta_{D}$</td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK rise time</td>
<td>$\delta_r$</td>
<td>Voltage at timing measured point 1.0 V &amp; 3.0 V</td>
<td></td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK fall time</td>
<td>$\delta_f$</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$\overline{A_0}$, $\overline{CS}$ set time for RD</td>
<td>$t_{AR}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$\overline{A_0}$, $\overline{CS}$ hold time for RD</td>
<td>$t_{RA}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>RD pulse width</td>
<td>$t_{RR}$</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data access time for RD</td>
<td>$t_{RD}$</td>
<td>$C_L = 100 , \mu F$</td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data float time for RD</td>
<td>$t_{DR}$</td>
<td></td>
<td>10</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$\overline{A_0}$, $\overline{CS}$ set time for WR</td>
<td>$t_{AW}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$\overline{A_0}$, $\overline{CS}$ hold time for WR</td>
<td>$t_{WA}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>WR pulse width</td>
<td>$t_{WW}$</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data set time for WR</td>
<td>$t_{DW}$</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time for WR</td>
<td>$t_{WD}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>RD, WR reset time</td>
<td>$t_{RV}$</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(Continued next page.)
Timing diagram (7861)

Clock

CLK

\phi_{CY}
\delta_D
\delta_D
3.0V
1.0V

Read operation

A_R, CS

RD

D_{B-7}

Write operation

A_B, CS

WR

D_{B-7}
### MC-4760

**Absolute maximum ratings (Ta = 25°C)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>(V_{CC})</td>
<td></td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>(V^+)</td>
<td></td>
<td>(-18.0)</td>
<td>V</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>(V^-)</td>
<td></td>
<td>(-12.0)</td>
<td>V</td>
</tr>
<tr>
<td>Digital input terminal voltage</td>
<td>(V_{IT})</td>
<td></td>
<td>(-0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>(P_d)</td>
<td></td>
<td>1000</td>
<td>mW</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>(T_{opt})</td>
<td></td>
<td>(-20)</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>(T_{sig})</td>
<td></td>
<td>(-40)</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Recommend operating range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input high voltage</td>
<td>(V_{IH})</td>
<td>2.0</td>
<td>3.0</td>
<td>(V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td>Input low voltage</td>
<td>(V_{IL})</td>
<td>0.0</td>
<td>0.8</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>(f_{CLK})</td>
<td>1.9</td>
<td>2.0</td>
<td>2.1</td>
<td>MHz</td>
</tr>
<tr>
<td>Sampling signal frequency</td>
<td>(f_{SMPL})</td>
<td>9.5</td>
<td>10.0</td>
<td>11.0</td>
<td>kHz</td>
</tr>
<tr>
<td>Mic input impedance</td>
<td>(Z_{INM})</td>
<td>0</td>
<td>600</td>
<td>1000</td>
<td>Ω</td>
</tr>
<tr>
<td>Line input impedance</td>
<td>(Z_{INL})</td>
<td>0</td>
<td>1000</td>
<td>2000</td>
<td>Ω</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>(V_{CC})</td>
<td>4.75</td>
<td>5.00</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Power supply voltage (rating: 12V)</td>
<td>(1V \pm 1)</td>
<td>11.40</td>
<td>12.00</td>
<td>12.60</td>
<td>V</td>
</tr>
<tr>
<td>Power supply voltage (rating: 15V)</td>
<td>(1V + 1)</td>
<td>14.25</td>
<td>15.00</td>
<td>15.75</td>
<td>V</td>
</tr>
</tbody>
</table>

### Electrical characteristics (\(T_a = 25\pm3°C, 1V = 12V = 5\%\))

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC IN input impedance</td>
<td>(Z_{MIN})</td>
<td>(V_{IN} = 1mVrms, f = 1kHz)</td>
<td>850</td>
<td>1000</td>
<td>1150</td>
<td>Ω</td>
</tr>
<tr>
<td>LINE IN input impedance</td>
<td>(Z_{LIN})</td>
<td>(V_{IN} = 1mVrms, f = 1kHz)</td>
<td>8.5</td>
<td>10.0</td>
<td>11.5</td>
<td>kΩ</td>
</tr>
<tr>
<td>MIC IN non-distortion input voltage</td>
<td>(V_{MIN})</td>
<td>(R_{GAPJ} = 75\Omega, f = 1kHz)</td>
<td>120</td>
<td>12.0</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td>LINE IN non-distortion input voltage</td>
<td>(V_{LIN})</td>
<td>(R_{GAPJ} = 75\Omega, f = 1kHz)</td>
<td>2.0</td>
<td>200</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td>MIC IN min. effective input voltage</td>
<td>(V_{MIN})</td>
<td>(R_{GAPJ} = 75\Omega, f = 1kHz)</td>
<td>120</td>
<td>200</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td>LINE IN min. effective input voltage</td>
<td>(V_{LIN})</td>
<td>(R_{GAPJ} = 75\Omega, f = 1kHz)</td>
<td>2.0</td>
<td>200</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td>A_{out} max. output voltage</td>
<td>(V_{AOUT})</td>
<td>(R_{L} = 10k\Omega)</td>
<td>5.0</td>
<td>5.0</td>
<td></td>
<td>Vp-p</td>
</tr>
<tr>
<td>LPF out max. output voltage</td>
<td>(V_{LPFO})</td>
<td>(R_{L} = 10k\Omega)</td>
<td>5.0</td>
<td>5.0</td>
<td></td>
<td>Vp-p</td>
</tr>
<tr>
<td>LPF out noise voltage</td>
<td>(V_{NS})</td>
<td>(R_{L} = 100k\Omega, R_{GAPJ} = 75\Omega, V_{IN} = 0V, ATC = FFH)</td>
<td>3.0</td>
<td></td>
<td></td>
<td>mVp-p</td>
</tr>
</tbody>
</table>

4-13
APPENDIX

A. Registered Voice Pattern Data Format
B. Outline of DP Matching Method
C. Example of System Configuration (Circuit Drawings)
(1) Dictionary

- Registered voice pattern registration flag
  (1 ... Registered, 0 ... Non-registered)
- Syntax No. (008 to 00H)
- Length of registered voice pattern
  (No. of frames before compression)
- Matching window
- No. of registered voice pattern frames
  (after compression)
- Reject value

Record No. 1

128 entries per memory block

1st frame 2nd frame 16th frame

(2) Registered voice pattern

Record No. 1

 byte

CH 1 CH 2 CH 3 CH 4 CH 5 CH 6 CH 7 CH 8
4 bits

(3) Representative data

Record No. 1

 byte

1st frame 2nd frame 16th frame

Fig. A.1 Registered Voice Data Configuration
Fig. B.1 Distance between Two Pattern of Unequal Length
This can be expressed by the following formula.

\[
D(A, B) = \min_{j = J(i)} \left[ I_d(i, j) \right] \quad \text{..... (2)}
\]

In this formula \(d(i, j)\) represents the distance \(|a_i - b_j|\) of the vectors between \(a_i\) and \(b_j\). The symbol "\(\min.\)" denotes that a value enclosed in the brackets \([\ ]\) will be minimized by the function \(J(i)\).

The DP (dynamic programming) method is applied to resolve this kind of problem.

By performing graduated formula calculation with DP method on the \(i - j\) plane as shown in Fig. B.2 under the initial conditions \(g(1,1) = d(1,1)\), the distance between patterns \(A\) and \(B\), \(D(A, B)\) can be obtained as \(D(A,B) = G(I,J)\).

\[
G(i,j) = d(i,j) + \min \left\{ \begin{array}{l}
g(i-1,j) \\
g(i-1, j-1) \\
g(i-1,j-2) \\
\end{array} \right. \quad \text{..... (3)}
\]

The matching window in Fig. B.2 prevents unnecessarily flexible matching and reduces the calculation load.

The function of the DP matching method is, as can be seen, to model the fluctuation of the time axis by using mapping function \((ji)\) and to calculate the simplified problem.

In comparison with conventional linear matching methods, the DP matching method reduces the erroneous recognition rate to \(1/4\) to \(1/7\) and dramatically improves the operating precision.

However, since its calculation load is very large, a special processor is required to perform real-time processing.
## History of Modifications

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