Radio, RF and Video Applications
Radio, RF and Video Applications

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Abstracts of Applications Documents
Abstracts

AN433 TV On-Screen Display Using the MC68HC05T1
The T-series devices in the M68HC05 MCU Family provide a convenient and cost-effective means of adding On Screen Display capability (OSD) to TVs and VCRs. The MC68HC05T1 is at the centre of the T-series price/performance range, and is used in this example. Full software listings are provided for a ROM-efficient implementation of an 8-row by 16-character display, including Programme Change, Channel Mode, Automatic Search, Analogue and Channel Name.

AN438 300W, 88–108MHz Amplifier Using the TP1940 MOSFETs Push-Pull Transistor
Provides the design of an efficient 300W amplifier with high power gain, compact physical layout and operation on a 50V power supply. It uses the TP1940, a high power, high gain, broadband push-pull Power MOSFET with low Reverse Transfer Capacitance. Includes circuit, parts list, PCB artwork and component layout.

AN531 MC1596 Balanced Modulator
The MC1596 Monolithic Balanced Modulator is a versatile HF communications building block. It functions as a broadband, double-sideband suppressed-carrier balanced modulator without the need for transformers or tuned circuits. This article describes device operation and biasing, and gives circuit details for typical modulator/demodulator applications in AM, SSB and suppressed-carrier AM. Additional uses as an SSB Product Detector, AM Modulator/Detector, Mixer, Frequency Doubler, Phase Detector and others are also illustrated. An appendix gives detailed AC and DC analysis.

AN535 Phase-Locked Loop Design Fundamentals
The fundamental design concepts for phase-locked loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example.

AN545A Television Video IF Amplifier Using Integrated Circuits
This application note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been designed specially for consumer oriented products. The integrated circuits used are the MC1350 MC1352 and the MC1330.

AN556 Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic
The MECL 10,000 Series is designed to be the most usable very high speed logic available. It satisfies the growing need for high clock rate capability and short propagation delays with minimum layout constraints.

This comprehensive note describes some characteristics of high speed digital signal lines and the wiring rules for MECL 10,000. Discussions include PCB interconnects and wirewrapping techniques.

AN721 Impedance Matching Networks Applied to RF Power Transistors
This note covers the basics of interstage and output impedance matching of RF power transistors. Graphical and numerical methods of solution are clearly described along with sample problems. Photos, schematics and charts are generously provided throughout.

AN761 Video Amplifier Design: Know Your Picture Tube Requirements
This note describes video amplifier design considerations for unitized gun and conventional picture tubes. Some unique design techniques are discussed taking advantage of Motorola's MC1323 chroma demodulator. Design objectives of video amplifiers are discussed.

AN779 Low-Distortion 1.6 to 30MHz SSB Driver Designs
A general discussion for broadband drivers and their requirements for linear operation. Design examples are given using Motorola plastic transistors and high-gain hybrid modules designed for operation in the 1.0 to 250MHz range. The amplifiers range in power gain from 25 to 55dB and are capable of driving power amplifiers to levels up to several hundred watts.

AN791 A Simplified Approach to VHF Power Amplifier Design
The design of 35W and 75W VHF linear amplifiers. The construction technique features printed inductors, the design theory of which is fully described. Complete constructional details, including a printed circuit layout, facilitate easy reproduction of the amplifier.

AN827 The Technique of Direct Programming by Using a Two-Modulus Prescaler
The technique and system described here offer a new approach to the construction of a phase-locked loop divider.

AN847 Tuning Diode Design Techniques
Tuning diodes are voltage-variable capacitors employing the junction capacitance of a reverse-biased PN junction. A simplified theory of tuning diodes is presented,
Abstracts (continued)

and a number of considerations to be employed in designs using tuning diodes are also discussed.

AN860 Power MOSFETs versus Bipolar Transistors
This application note discusses the characteristics of FETs and bipolar devices. Both have the same basic geometry but with some mask changes. One is processed as a MOSFET and the other as a bipolar. It is doubtful that the power FET will ever replace the bipolar transistor in all areas of communications equipment. It will have its applications in low and medium power VHF and UHF amplifiers, eliminating the need for internal matching, and up to medium power low band and VHF SSB, where the high order IMD is beginning to be more significant due to the crowded frequency spectrums.

AN878 VHF MOS Power Applications
The construction characteristics and advantages of RF power FETs are described with emphasis on the VHF frequency range. Particular attention is given to the excellent gain control characteristics of these devices.

AN879 Monomax: Application of the MC13001 Monochrome Television Integrated Circuit
This application note presents a complete 12" black and white line-operated television receiver including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome and the significance of component selections and locations are discussed.

AN921 Horizontal APC/AFC Loops
The most popular method used in modern television receivers to synchronize the line frequency oscillator is the phase locked loop. The operating characteristics and parameters of the loops are discussed.

AN923 800MHz Test Fixture Design
Techniques for the general case of UHF-800MHz circuit design are presented. Emphasis is placed specifically on test fixture design for the 800MHz. Text fixtures, the most valuable tools available for measuring and maintaining device consistency, are also presented.

AN932 Application of the MC1377 Colour Encoder
The MC1377 is and economical, high quality, RGB encoder for NTSC or PAL applications. It accepts RGB and composite sync inputs, and delivers a 1V p-p composite NTSC or PAL video output into a 75Ω load. It can provide its own colour oscillator and burst gating, or it can easily be driven from external sources. Performance virtually equal to high-cost studio equipment is possible with common colour receiver components.

AN955 A Cost Effective VHF Amplifier for Land Mobile Radios
This application note describes a two-stage, 30 watt VHF amplifier featuring high gain, broad bandwidth and outstanding ruggedness to load mismatch, achieved by the use of the new MRF1946A power transistor.

AN969 Operation of the MC145159 PLL Frequency Synthesizer with Analog Phase Detector
The MC145159 is a phase-locked loop frequency synthesizer with an improved sample-and-hold phase detector. It incorporates a range of features making it of particular interest in 2-way radios, cellular radio-telephones and avionics equipment. This note discusses its open loop characteristics, and shows that it reduces VCO modulation sidebands while allowing wider loop bandwidths than are possible with digital phase detectors.

AN980 VHF Narrowband FM Receiver Design Using the MC3362 and the MC3363 Dual Conversion Receivers
The MC3362 and MC3363 narrow-band FM dual conversion receivers feature excellent VHF performance with low power drain, making them ideal for cordless telephones, narrowband voice and data receivers and RF security devices. This note provides a detailed description of the operation of the two devices, plus circuits and descriptions for four applications: A single Channel VHF FM Narrowband Receiver; A Ten Channel Frequency Synthesized Cordless Telephone Receiver; A 256 Channel Frequency Synthesized Two Metre Amateur Band Receiver; and A Single Chip Weather Band Receiver.

AN1019 Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation
The TDA3330 is a Composite Video to RGB Colour Decoder originally intended for PAL and NTSC colour TV receivers and monitors — so its data sheet concentrates on picture tube drive. This practical application note supplements the data sheet by providing circuits for video cable drive as used in video processing, frame store and other specialized applications, and expands on TDA3330 functional details. Includes PCB artwork and layout of an evaluation board.

AN1040 Mounting Considerations for Power Semiconductors
The operating environment is a vital factor in setting current and power ratings of a semiconductor device. Reliability is increased considerably for relatively small reductions in junction temperature. Faulty mounting not only increases the thermal gradient between the device and its heat sink, but can also cause mechanical damage. This comprehensive note shows correct and incorrect methods of mounting all types of discrete packages, and discusses methods of thermal system evaluation.
AN1041 Mounting Procedures for Very High Power RF Transistors
High power (200-600W) RF semiconductors such as the MRF153... and MRF141G... series dissipate an abnormally large amount of heat within a small physical area. Heat sink material, surface finish, mounting screws, washers and screw torque are extremely important factors in ensuring reliability. This note explains why.

AN1044 The MC1378 — A Monolithic Composite Video Synchronizer
The MC1378 provides an interface between a remote composite colour video source and local RGB. On-chip circuitry can lock a local computer to the remote source, switching between local and remote signals to generate composite video overlays. This detailed note describes the circuitry and switching between local and remote operation, picture-in-picture applications and the design of test fixtures to help system development. Printed circuit artwork for an evaluation board is provided. The NTSC/PAL colour encoder is similar to the MC1377, discussed in detail in AN932.

AN1051 Transmission Line Effects in PCB Applications
As rise and fall times become faster in order to achieve high operating speeds, transmission line effects on PCBs can be very significant, with the possibility of unpredictable behaviour. This note presents a guideline as to when to analyse, discusses the characteristics of different types of PCB trace, describes Lattice Diagram and Bergeron Plot analysis, and summarises termination methods. Includes 10 worked examples.

AN1076 Speeding up Horizontal Outputs
Motorola's SCANSWITCH transistors are designed specifically as fast drivers for horizontal outputs. Optimum performance is achieved when 5 base drive conditions are met. This successful base drive circuit starts with the output transistor's physics and works back to the horizontal oscillator.

AN1080 External-Sync Power Supply with Universal Input Voltage Range for Monitors
As the resolution of colour monitors increases, the performance and features of their power supplies becomes more critical. EMI/RFI generated by switching power supplies can adversely affect resolution if switching frequency is not synchronised to horizontal scanning frequency. This 90W flyback switching supply demonstrates the use of new high-performance devices in a low-cost design, and includes a new universal input voltage adapter.

AN1103 Using the CR3424 for High Resolution CRT Applications
The CR3424 hybrid video amplifier solves the problem of video amplifier speed that has hitherto limited the performance of ultra-high resolution CRT monitors. The amplifier achieves less than 2.9ns rise and fall time for a 40V output swing. This note discusses the effect of the video amplifier on CRT picture quality, input characteristics of the CR3424, and two example drive circuits.

AN1106 Considerations in Using the MHW801 and MHW851 Series RF Power Modules
The MHW801 and MHW851 series of power modules are designed for use in cellular portable radios. A considerable amount of applications information is included in the data sheet; this note provides additional information concerning general electrical considerations, noise characteristics, gain control, circuit considerations and mounting.

AN1107 Understanding RF Data Sheet Parameters
The data sheet is often the only source of information about the characteristics and capability of a product. This is especially true of RF devices, which have many unique specifications. It is therefore important that the manufacturer and designer speak a common language. This paper reviews the significance of the quoted values and highlights critical characteristics. Descriptions cover the procedures used to obtain impedance and thermal data, the importance of test circuits, low noise considerations and linearity requirements.

ANE416 MC68HC05B4 Radio Synthesizer
Synthesis of the local oscillator in a superheterodyne radio provides many advantages over mechanical tuning, including accuracy, stability and storing often-used frequencies. In this application, an MC145157 CMOS Synthesizer is controlled by an MC68HC05B4 MCU — the software is mask programmed in parts marked 'MC68HC05B4 DEMO', but could alternatively be programmed into an MC68HC805B6. A 6-digit LCD driver is controlled through the Serial Communications Interface, while the standby mode is used to eliminate interference with the radio.

ANHK02 Low Power FM Transmitter System MC2831A
This application note provides information concerning the MC2831A, a one-chip low-power FM transmitter system designed for AM/FM communication equipment such as FM transceivers, cordless telephones, remote control and RF data link.

ANHK07 A High Performance Manual-Tuned Receiver for Automotive Application Using Motorola ICs MC13021, MC13020 and MC13041
This design is intended to provide radio engineers with a good start in automotive manually-tuned AM/FM stereo receiver design. After discussing the most important principles of this type of receiver, a design is presented complete with circuit, PCB artwork and performance curves.
Abstracts (continued)

**EB104  Get 600 Watts RF from Four Power FETs**
This unique push-pull/parallel circuit produces the power output of four devices without the loss and cost of power splitters and combiners. Full circuit details and PCB masters are provided for this MRF50 RF power FET design, including transformer details and performance analysis.

**EB109  Low Cost UHF Device Gives Broadband Performance at 3.0 Watts Output**
The package is the major cost in low to medium power RF transistors. Motorola introduced the common emitter TO-39 some years ago to limit cost increases. Good design and construction techniques can extend its use to broadband UHF amplifiers, like this broadband application of the low-cost MRF630, a transistor capable of 3W output power with 10dB gain at 512MHz. Emphasis is placed on mounting techniques.
Applications
Documents
TV on-screen display using the MC68HC05T1

By Peter Topping
Motorola Ltd., East Kilbride, Scotland

INTRODUCTION

The "T" members of the MC68HC05 family of MCUs provide a convenient and cost-effective method of adding on-screen display (OSD) to TVs and VCRs. As well as the OSD capability, they include 8 Kbytes of ROM (adequate for Teletext, frequency-synthesis, stereo and OSD), 320 bytes of RAM, a 16-bit timer and 8 pulse-width-modulated D/A converters. The MC68HC17/05T7/8 also includes IIC hardware and, by using a 56/64-pin package, 4 ports of I/O independent of the OSD, serial and D/A outputs. It is thus suitable for large full-feature chassis. The MC68HC05T1 is in the middle of the price/performance range and includes most of the features of the MC68HC05T8 but in a 40-pin package. This is achieved by sharing I/O with the other pin functions (SPI, OSD, D/A). Even if all these features are used there is sufficient I/O for most applications. The low cost MC68HC05T4 has 5 Kbytes of ROM and 96 bytes of RAM making it suitable for simpler (mono, non-Teletext) applications.

68HC05T1 OSD FEATURES

- Programmable display of 10 rows of 18 characters
- 24 byte (18 data + 6 control) single row architecture
- Settable in software to any one of four standards
- Zero inter-row and inter-column spacing
- 64 user-defined mask-programmable 8 x 13 characters
- Programmable horizontal position
- Character colour selectable from 4 colours/row
- Software programmable (start, stop and colour) window
- 4 character sizes (normal, double height and/or width)
- Half-dot character rounding
- Selectable half-dot black outline

OSD CHARACTERISTICS

The HC05TX series have an OSD capability of 10 rows of 18 characters. Each row can contain characters of four colours selected from the eight available colours (black, blue, green, cyan, red, magenta, yellow and white). The rows can independently select double height and/or double width and the start and stop positions of a background window of any colour. The signals sent to the TV are Red, Green, Blue, fast-blanking and half-tone. Separate horizontal and vertical synchronisation inputs are required.

The OSD architecture employed includes only a single line of display RAM. This makes the software more complicated but reduces the silicon area required to implement the OSD function. The software is required to update the display RAM on a regular basis. When operating in the 625-line PAL standard the updates must occur at 1.66 ms (26 lines) intervals in order to display adjacent lines. The OSD hardware can generate an interrupt when an update is required. There are 18 data registers (one for each character) and 6 control registers arranged as shown below. The table is for the T1, some of the control bits are different in the T4/7/8.

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
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<tr>
<td>$20</td>
<td>OSD Data registers</td>
</tr>
<tr>
<td>$32</td>
<td>CAS Read status, Write colours 1 &amp; 2 and outline enable</td>
</tr>
<tr>
<td>$33</td>
<td>C34 Colours 3 &amp; 4</td>
</tr>
<tr>
<td>$34</td>
<td>RAD Row address, character size, int enable, RGB invert</td>
</tr>
<tr>
<td>$35</td>
<td>WCR OSD &amp; PLL enable, Window enable and start column</td>
</tr>
<tr>
<td>$36</td>
<td>CCP Window colour and end column</td>
</tr>
<tr>
<td>$37</td>
<td>HPD Horizontal position, standard selection</td>
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The OSD display is timed from an on-chip 14 MHz oscillator which is phase locked to the TV's line synchronisation pulses. The vertical synchronisation depends on the standard in use. Four standards are available (15.75 kHz/60 Hz, 31.5 kHz/120 Hz, 15.625 kHz/50 Hz and 31.25 kHz/100 Hz). The standard is selected by control bits in the T1/2 but is automatic in the T4 and the T7/8.

64 OSD characters are mask programmed along with the user ROM. The spacing and full size of the characters is the same as 8 x 13 (for 625-line standard). This allows continuous graphics. Half-dot interpolation hardware doubles the apparent resolution to produce smoother characters. A software selectable black outline (a half-dot wide) is also implemented in the hardware. Because the half-dot circuitry has to know the information for the next line of pixels, a 14th line is available in the character generator ROM to facilitate look ahead. The vertical height of a character is 26 lines (52 including interlace) and the horizontal width is 2 2.7 µs (1 7 µs per half pixel).

SOFTWARE

There are several approaches to writing OSD software to operate with the single line architecture. The choice will affect the amount of ROM and RAM used. One principle is to have a separate interrupt routine for each type of row to be displayed. This method will use little RAM but will be inefficient in its use of ROM. The other approach is to write a single interrupt routine which transfers display information from a block of normal RAM to the display RAM as it is required for each new line. This method will be more ROM efficient but requires a RAM location for every display character. The amount of RAM used depends on the maximum amount of data which has to be displayed at any one time. The choice between these two methods will depend on the type of data to be displayed. The first method may be better if much of the displayed data is fixed. This could be, for example, a series of menus. The second method will however be more appropriate if the data is mostly variable. This will usually be the case in conventional TV applications.

This application note describes an implementation of the second of the above approaches. A block of RAM is used to contain a copy of all the data to be displayed. The size of this block can be changed to reflect the number of rows and the number of characters per row. The choice made in the example described here is 8 rows of 16 characters. This is slightly less than the maximum available and was chosen because the total number of characters (128) corresponds to the available page 1 RAM in the MC68HC05T1. The choice of 16 characters per row also slightly simplifies the software. The software allows any eight of the ten available rows to be used but only the first 16 of the 18 available characters. This choice does not prevent access to the right-hand-side of the screen as the display can be moved to the right under software control. The use of page 1 RAM does not incur any significant compromise in execution time. It also leaves free the page 0 RAM for the rest of the TV control software, which would be made less efficient if it had to use page 1 RAM, where direct addressing and bit manipulation instructions cannot be used. This choice slightly increases the ROM used by the OSD code, as 3-byte extended store instructions sometimes need to be used to write data to the RAM used for OSD characters.

The 1-byte indexed addressing mode can however be used in page 1. This addressing mode can access up to address $1FE and is made use of in the example software. For example the OSDCLR routine used to initialise RAM locations used for OSD employs a CLR DRAM-1,X instruction. DRAM is the start of page 1 RAM at $100 so DRAM-1 evaluates as $FF a 1-byte offset.

The OSD update interrupt routine (INLINE) shown in the program listing transfers data from page 1 RAM to display RAM each time an interrupt occurs. The first operation is to increment the pointer which selects the next row number. This pointer (OSDL) is subsequently used to transfer the appropriate data from page 1 RAM to the OSD RAM. So that any row number can be used the pointer selects the number from a table unique to each type of display. The appropriate table is determined by the value of LIND. The pointer is incremented until the corresponding row number is zero when the pointer is reset to zero. This allows any sub-set of up to 8 of the 10 available rows to be used. The next row number (ORed with the character size information contained in RAM) is written into the appropriate register ($34). The row number in this register is compared by the OSD hardware with the current position of the raster. When they match, an interrupt is generated and the next interrupt routine is performed. The other control registers are then updated from the page 0 RAM locations, which are used for this purpose.

To save RAM only three (RAD, CAS & CCR) of the six control registers are loaded in this way. The pointer OSDL is multiplied by 3 using the table M3, as this is quicker than shifting and adding. In this example the other registers are loaded by the main program and therefore have fixed values for each display. The fixed registers are Colour 3/4 ($33), Window enable/start column ($35) and Horizontal position delay ($37). As this choice would not allow windows to be enabled on individual rows, window enable is controlled by the un-used bit (6) in the RAM byte used to update the Colour 1/2 register (CAS). This choice of fixed registers limits the flexibility of the display but clearly all registers can be updated on a line-by-line basis if more RAM is used. The limitations imposed by this choice are that colours 3 & 4, the window start column and the horizontal position apply to a whole display rather than to individual lines. In practice these constraints were not found to be significant restrictions for the displays required for TV use.
The interrupt routine then transfers the relevant OSD data from page 1 RAM into the OSD data registers. This is done using linear, repetitive code in order to minimise the time taken by the interrupt routine. The code used uses 8 cycles (4 µs) for each byte transferred. Less ROM space would be utilised if a loop was employed but this would use 28 cycles per byte. The best choice depends on whether time or ROM use is more critical. The example code includes a cycle count to calculate the length of the interrupt routine. The time taken is $121 \pm 4\mu s$. This includes the time taken by the interrupt itself. An alternative method of OSD data transfer (TOSD2) using a loop is included as comments in the listing. It would take an additional 165 µs.

The last task performed by the interrupt routine is to control any character or window flashing. The software allows one or two characters (on a selected row) and one window (on the same or a different row) to be flashed at a rate determined by the MCU’s timer. This function could be performed outwith the interrupt routine in the main program and the time taken to perform it is not included in the figure given above.

**MAIN OSD PROGRAM**

The remainder of the OSD control program does not write directly to most of the display registers. It simply puts the required display and control information into the blocks of RAM allocated for this purpose, together with supplying the coordinates of any required flashing characters or windows. It must, however, write to the display control registers not updated by the interrupt routine; in this example these are $33$, $35$ and $37$. The program has 4 main parts. These are the idle, channel name table, program/channel number and analogue displays. The idle display applies when no transient display (e.g. program number and channel number or name) is on. The OSD idle condition is selectable between blank and a small program number at the bottom right hand corner of the screen.

The OSD example program (assembler listing included) is just part of the code required to control a TV set. This program was incorporated in HCOST1 software along with four other modules. These were the base module (idle loop, transient control, local keyboard, IR, IIC and ‘reset), the tuning module (PLL, analogue and NVM control), the stereo module (stereoton and Nicam) and the Teletext module (FLOF level 1.5).

The microprocessor in a TV application will usually need to handle the reception of IR commands. Polled methods of IR reception are most effective if the time made unavailable to them by interrupts is minimised. It is for this reason that the illustrated OSD interrupt routine was written to execute as fast as possible. This is, however, not so much of a problem if the TCAP facility is used for IR reception. When a falling edge occurs, the timer value is saved and it does not matter if the interrupt which processes this information is not serviced until several hundred microseconds later. The allowable size of this delay will of course depend on the IR protocol in use. The bi-phase protocol used with the example OSD software (transmitter chip: MC144105) has a minimum spacing of 1 ms between consecutive edges.

The next section describes the OSD features of this software. Some of the data used in the OSD is passed from other modules (particularly the tuning module). The same RAM allocation file was used in all modules so this part of the listing shows the locations used to pass data between them.

**OSD FEATURES PROVIDED IN THE EXAMPLE PROGRAM**

**Program change**

When keys 0-9, PC- or PC+ are pressed, the new program number appears (in cyan) at the bottom-right-hand corner of the screen in double height/double width characters and stays for 5 seconds after the last change. Above this display either the channel name (if one has been defined) or the channel number is shown (normal size). After 5 seconds this display times out and there is either no display or a permanent normal size program number display. This is selectable using the Teletext MIX key.

For program numbers of 10 and over, three keys are required. They are selected by first pressing "—” Two flashing dashes are displayed, the first 0-9 key (only 0-4 valid) will be taken as the tens digit and the second as the units digit. If a new program number has not been selected within 30 seconds, the TV returns to the previous display (nothing or the old program number).

**Channel mode**

When the P/C key is pressed, the program number and channel name (or number) is displayed for 5 seconds as an indication of the current status. If it is pressed again during this period, the TV changes to channel mode. This will remain for 30 seconds after the last key-press. The display (in yellow) shows the program number as in program mode along with the channel number. The channel number flashes to show that it will be changed if a number or PC- or PC+ key is pressed. New channels can be selected. If the STORE key is pressed then the current channel is stored against the current program number. If no key is pressed for 30 seconds, the TV returns to program mode. If the channel has been changed but STORE not pressed then the TV will return back to the channel stored against the current program number.
**Automatic search**

When SEARCH is pressed the TV goes into the channel mode and the on screen display is as described above. The channel number is incremented at a rate of 2 per second until a signal is found. The search then stops. A press of STORE returns the TV to program mode, storing the new channel against the current program number.

**Analogues**

When any of the analogues are selected the appropriate logo is displayed along with a horizontal bar indicating the current value in the D/A converter (full-scale 63). Display returns to default (nothing or program number) 5 seconds after the last change. If no analogue is selected the volume is shown (and adjusted) when the ANALOGUE +/- keys are used.

**Channel name table**

Up to 24 channels can have a 4 character name and standard bit associated with them. If the channel number and standard of one of these entries in the table correspond to those selected by the current program number then the name is displayed along with the program number when the program is selected or when P/C is pressed. Entry of names is done using the Teletext INDEX key. When it is pressed a table of six lines is displayed. Each line (identified by a “station” number in the leftmost column) contains a channel number, standard and the associated name. All of this data is user definable.

One character on the screen flashes to indicate the current position of the cursor. The character at the cursor position can be changed through 0-9, A-Z and space by pressing PC+ or PC- (0-9 for channel number digits and PAL/SECAM for standard). When a character (or the standard) is changed, its colour changes from yellow to red. The cursor is moved to the left and right by the Teletext RED and GREEN keys and up and down by the BLUE and YELLOW keys. The current line appears in a light blue (cyan) window as opposed to the dark blue window used for the other lines. The whole table scrolls when the cursor is required to go beyond the bottom (or top) of the current display.

To save a name the STORE key is pressed. This will save the name and standard on the current line against its channel number. This is indicated by the colour of any changed characters returning to yellow. Any changes which have been made to lines other than the one being stored are lost. Channel 00 cannot have a name. The procedure for removing a name from the table is to set the channel number to zero and then to save the line. Any name left on the line will not be used. The table display is exited by pressing the Teletext INDEX key. The function of each key is shown at the bottom of the display.
EXAMPLE PROGRAM

******************************************************************************
* TV/Teletext/OSD/Stereo program (MC68HC65TL/8).                      *
* On-Screen-Display module                                              *
* This software was developed by Motorola Ltd. for demonstration purposes.*
* No liability can be accepted for its use in any specific application.*
* Original software copyright Motorola - all rights reserved.            *
*                                                                 *
* P. Topping 25th May '90                                              *
******************************************************************************

IMPORT CHEX,CBCD,READ,WRITE,CDISP2

EXPORT NLINE,PC0SD,DRAM,ANOSD,PRDP,CHST

EXPORT CUP,CDWN,CLFT,CRGT,PLUS,MINUS,SAVE,OSDLE,OSDEF

LIB RAMT1.505

SECTION .S .RAM,COMM

******************************************************************************
* Teletext RAM allocation.                                              *
******************************************************************************

SUB1 RMB 1
R1 RMB 1 mode register
R2 RMB 1 page request address register
R3 RMB 1 page req. data reg. col. 0 : mag.
C1 RMB 1
C2 RMB 1 " " " " 2 : ppu.
C3 RMB 1 " " " " 3 : pt.
C4 RMB 1 " " " " 4 : hu.
C5 RMB 1 " " " " 5 : mt.
C6 RMB 1 " " " " 6 : mu.

SUB2 RMB 1
R4 RMB 1 display chapter register
R5 RMB 1 display control register (normal)
R6 RMB 1 display control register (news/sub)
R7 RMB 1 display mode register

SUB3 RMB 1
R8 RMB 1 active chapter register
R9 RMB 1 active row register
R10 RMB 1 active column register
R11 RMB 1 active data register
PH RMB 1 2nd " "
PT RMB 1 3rd " "
PU RMB 1 4th " 

LIFO RMB 9 LINKED PAGE No. LIFO BUFFER

INDEX PAGE No. 7 PAGE No. INPUT BUFFER
PA00 RMB 3 ACO PAGE No.
PA01 RMB 3 AC1 PAGE No.
PA02 RMB 3 AC2 PAGE No.
PA03 RMB 3 AC3 PAGE No.
PACG RMB 3 CYAN PAGE No.
PAG1 RMB 3 INDEX PAGE No.

PDF RMB 1 PAGE DIGIT POINTER
ACC RMB 4 DISP, RED, GREEN, YELLOW AC. CIR.
WACC RMB 1 WORKING ACC No.
ADDR RMB 1 IIC ADDRESS
DPWT RMB 1 IIC DATA POINTER FOR WRITE
SUBADR RMB 1 IIC SUB-ADDRESS
DSBUF RMB 4 IIC BUFFER, +2 & +3 RSRVD FOR PLL

STAT2 RMB 1 0: ROM24 FETCH FLAG
  1: REMOTE REPEATING
  2: SEARCH/STANDBY IIC LOCK
  3: STANDBY STATUS
  4: UPDATE PENDING
  5: DIFFERENCE FOUND
  6: NO TELETXT TRANSMISSION
  7: MIXED

LINKC RMB 1 LINK OPTIONS
  0: CYAN LINK ON
  1: YELLOW LINK ON
  2: GREEN LINK ON
  3: LINKS/ROM24 ON
00000049
PLLHI RMB 1 PLL DIVIDE RATIO MSB
PLLLOW RMB 1 PLL DIVIDE RATIO LSB
W1 RMB 1 WORKING
W2 RMB 1 *
W3 RMB 1 *
COUNT RMB 1 LOOP COUNTER
KOUNT RMB 1 LOCAL KEYBOARD COUNTER
CNT RMB 1 12.8mS (inc, free running)
CNT1 RMB 1 12.8mS (inc, reset every 15 during transient)
CNT2 RMB 1 3.25 S (inc, store timeout)
CNT3 RMB 1 3.25 S (dec, automatic standby timeout)
CNT4 RMB 1 12.8mS (cleared for row24 delay when page arrives)
CNT5 RMB 1 12.8mS (inc, transient mute)
TMR RMB 1 TRANSIENT DISPLAY SECONDS COUNTER
00000056
STAT RMB 1 0: TV/TELETEXT
* 1: IIC R/W
* 2: HOLD
* 3: IR REPEAT INHIBIT
* 4: TRANSIENT DISPLAY ON
* 5: TIME HOLD
* 6: SUB-PAGE MODE
* 7: IR TASK PENDING
00000057
STAT4 RMB 1 0: KEY FUNCTION PERFORMED
* 1: LOCAL REPEATING
* 2: P/C PROG : 0, CHAN : 1
* 3: MUTE (TRANSIENT)
* 4: OSD STATUS TRANSIENT
* 5: MUTE (BUTTON)
* 6: COINCIDENCE MUTE
* 7: SEARCH
00000058
PWR RMB 1 $55 AT RESET, $AA NORMALLY
PROG RMB 1 CURRENT PROGRAM NUMBER
CHAN RMB 1 CURRENT CHANNEL NUMBER
DISP RMB 1 CURRENT DISPLAY NUMBER
FTUNE RMB 1 FINE TUNING REGISTER
AVOL RMB 1 VOLUME LEVEL
KEY RMB 1 CODE OF PRESSED KEY (LOCAL)
NUMO RMB 1 4 LED DISPLAY RAM
IRRA1 RMB 1 1 JR INTERRUPT TEMP.
IRRA2 RMB 1 *
IRRA3 RMB 1 *
IRRA4 RMB 1 *
IRRA6 RMB 1 *
IRRA7 RMB 1 *
DIFFH RMB 1 IR TIME DIFFERENCE
IRRH RMB 1 IR CODE BIT
IRL RMB 1 COLLECTION
IRCODE RMB 1
IRCNT RMB 1
IRCMCT RMB 1
OLDIR RMB 1
0000006f
POOLTM RMB 1 Poll timer
TONEA RMB 1 Tone (unadjusted for loudness)
LABL RMB 1 Loudspeaker balance variable
LVL RMB 1 Loudspeaker left volume
LVR RMB 1 Loudspeaker right volume
HVL RMB 1 Headphone volume left
HVR RMB 1 Headphone volume right
TONE RMB 1 Tone variable (Bass/Treble)
MATRIX RMB 1 Current matrix
MATNO RMB 1 Frequent mode (mono/stereo/lan 1/11.12/12.11)
00000079
WS1 RMB 1 Workspace 1 (no interrupt usage)
WS2 RMB 1 Workspace 2 (use for these please.)
0000007b
VAV RMB 1
0000007c
MCNCNT RMB 1 Mono ident count
SCNCNT RMB 1 Stereo ident count
DNCNT RMB 1 Dual lang ident count
ERCNT RMB 1 Error ident count
RCOUNT RMB 1 Ident countdown
RANG0 RMB 1 Total ident poll number
00000082
TEMP RMB 1
STATS RMB 1
0: LOUDNESS
1: VCR
2: OSD NAME TABLE
3: OSD DEFAULT P/C NUMBER
4: ANALOGUE OSD ON
5: NAME-TABLE STANDARD
6: STANDARD CHANGED
7: RE-INITIALISE TELETEXT

STAT6 RMB 1
0: 2-DIGIT PROGRAM ENTRY

TMPPR RMB 1
TEMPORARY PROGRAM NUMBER

* OSD RAM allocation.

********************************************

CAS1 RMB 1
ROW 1, colour 1/2 & outline enable
RAD1 RMB 1
Row address & character size
CCR1 RMB 1
Window colour & end column
CAS2 RMB 1
ROW 2, colour 1/2 & outline enable
RAD2 RMB 1
Row address & character size
CCR2 RMB 1
Window colour & end column
CAS3 RMB 1
ROW 3, colour 1/2 & outline enable
RAD3 RMB 1
Row address & character size
CCR3 RMB 1
Window colour & end column
CAS4 RMB 1
ROW 4, colour 1/2 & outline enable
RAD4 RMB 1
Row address & character size
CCR4 RMB 1
Window colour & end column
CAS5 RMB 1
ROW 5, colour 1/2 & outline enable
RAD5 RMB 1
Row address & character size
CCR5 RMB 1
Window colour & end column
CAS6 RMB 1
ROW 6, colour 1/2 & outline enable
RAD6 RMB 1
Row address & character size
CCR6 RMB 1
Window colour & end column
CAS7 RMB 1
ROW 7, colour 1/2 & outline enable
RAD7 RMB 1
Row address & character size
CCR7 RMB 1
Window colour & end column
CAS8 RMB 1
ROW 8, colour 1/2 & outline enable
RAD8 RMB 1
Row address & character size
CCR8 RMB 1
Window colour & end column

OSDL RMB 1
CURRENT OSD ROW POINTER
LIND RMB 1
ROW TABLE INDEX
BROW RMB 1
CHARACTER FLASH ROW
BCOL RMB 1
CHARACTER FLASH COLUMNS
WROW RMB 1
WINDOW FLASH ROW
*RROW RMB 1
FIRST ROW No. (NAME TABLE)

ANAL RMB 1

ANAF RMB 1

TEMP2 RMB 1

STACK RMB 22
23 BYTES USED FOR STACK

SP RMB 1
(1 INTERRUPT AND 9 NESTED SUBS)

KEYI EQU $00
KEYO EQU $00
KEYIO EQU $00
SERO EQU $03

VOLU EQU $0A
D/A 2
JP08 IN EVB

CONT EQU $0B
D/A 3
JP09 IN EVB

BRIL EQU $0C
D/A 4
JP10 IN EVB

SATU EQU $0D
D/A 5
JT11 IN EVB

LI EQU $05
Lang. 1 indicator bit

L2 EQU $06
Lang. 2 indicator bit

WIDE EQU $04
Wide matrix bit

PST EQU $05
Fake-synthetic matrix bit

VCR EQU $06
VCR active bit

LOUD EQU $05
LOUDness effect active bit

MUT EQU $03
Mute indicator bit

STADR EQU $80
Stereo ton address (IIC)

NORMVOL EQU $25
normal volume (mid balance)
**Equates.**

---

PORTA EQU $00  Port A address
PORTB EQU $01  Port B
PORTC EQU $02  Port C
PORTD EQU $03  Port D
DDRA EQU $04  Port A data direction reg.
DDRb EQU $05  Port B
DDRC EQU $06  Port C
DDRD EQU $07  Port D

TCR EQU $12  Timer control register.
TSR EQU $13  Timer status register.
ICRB EQU $14  Input capture register, high.
ICRL EQU $15  Input capture register, low.
OCRB EQU $16  Output compare register, high.
OCRl EQU $17  Output compare register, low.
TDRH EQU $18  Timer data register, high.
TDLR EQU $19  Timer data register, low.
MISC EQU $1C  Misc. register
OSD EQU $20  16 OSD data registers
CAS EQU $32  Color & status register
C34 EQU $33  Color 3/4 register
RAD EQU $34  Row address & character size
MCR EQU $35  Window/Column register
CCR EQU $36  Column/color register
HFD EQU $37  Horizontal position delay
MAD EQU $39  M-bus address register
MPD EQU $3A  M-bus frequency divider
MCR EQU $3B  M-bus control register
MSR EQU $3C  M-bus status register
MEX EQU $3D  M-bus data register
TR1 EQU $3E  Test 1, OSD/Timer/PLM
TR2 EQU $3F  Test 2, EPROM

---

`SECTION .RAM2`

- DRAM RMB 128

---

`SECTION .ROM2`

- OSD update routine - row number & data.

---

`DRAM update routine - row number & data.`

---

`SECTION .ROM2`

- OSD update routine - row number & data.
83 0000039 b723 STA<br>84 000003b >e6f4 LDA <DRAM-12,X<br>85 000003d b724 STA OSD+3<br>86 000003f >e6f5 LDA OSD+4<br>87 0000041 b725 STA <DRAM-11,X<br>88 0000043 >e6f6 LDA OSD+5<br>89 0000045 b726 STA <DRAM-10,X<br>90 0000047 >e6f7 LDA OSD+6<br>91 0000049 b727 STA <DRAM-9,X<br>92 000004b >e6f8 LDA OSD+7<br>93 000004d b728 STA <DRAM-8,X<br>94 000004f >e6f9 LDA OSD+8<br>95 0000051 b729 STA <DRAM-7,X<br>96 0000053 >e6fa LDA OSD+9<br>97 0000055 b72a STA <DRAM-6,X<br>98 0000057 >e6fb LDA OSD+10<br>99 0000059 b72b STA <DRAM-5,X<br>100 000005b >e6fc LDA OSD+11<br>101 000005d b72c STA <DRAM-4,X<br>102 000005f >e6fd LDA OSD+12<br>103 0000061 b72d STA <DRAM-3,X<br>104 0000063 >e6fe LDA OSD+13<br>105 0000065 b72e STA <DRAM-2,X<br>106 0000067 >e6ff LDA OSD+14<br>107 0000069 b72f STA <DRAM-1,X<br>108<br>109<br>110<br>111<br>112<br>113<br>114<br>115<br>116<br>117<br>118<br>119<br>120<br>121<br>122<br>123<br>124<br>125<br>126 000004b >09001f STA<br>127 000006e >b600 LDA<br>128 0000070 2719 STA<br>129 0000072 b634 STA<br>130 0000074 a40f STA<br>131 0000076 b100 STA<br>132 0000078 2611 STA<br>133 000007a >b600 STA<br>134 000007c a40f STA<br>135 000007e 97 STA<br>136 000007f a61b STA<br>137 0000081 b600 STA<br>138 0000083 54 STA<br>139 0000085 54 STA<br>140 0000087 54 STA<br>141 0000089 54 STA<br>142 000008b 2000 STA<br>143 000008d b100 STA<br>144 000008d >b600 STA<br>145 000008e 290a STA<br>146 0000091 b634 STA<br>147 0000093 a40f STA<br>148 0000097 b600 STA<br>149 0000099 b600 STA<br>150 000009e >e620 STA<br>151 00000a0 1f35 STA<br>152 00000a0 80 RTS<br>153<br>154 00000b5 640 RTS<br>155 00000b0 63f RTS<br>156 00000ba 620 RTS<br>157 00000ba 620 RTS<br>158 00000ba e20 RTS<br>159 00000ba e20 RTS<br>160 00000ba 620 RTS<br>161 00000ba 620 RTS<br>162 00000ba 620 RTS<br>163 00000ba 620 RTS<br>140 00000ba 620 RTS<br>81 00000ba 620 RTS<br>80 00000ba 620 RTS<br>79 00000ba 620 RTS<br>78 00000ba 620 RTS
165 166 167 168 169 170 171 000000a0 >060004
172 000000b1 >1600
173 000000b3 2002
174 175 000000b5 >1700
176 177 000000b7 9b
178 000000b8 >1900
179 000000ba >1500
180 181 000000bc ae1d
182 000000be >efff
183 000000ce 5a
184 000000c1 26fb
185 186 000000c3 >cd0000
187 000000c6 3f30
188 000000c8 3f31
189 000000ca >06000a
190 000000cc >c6000c
191 000000d0 b730
192 000000d2 >c6000a
193 000000d5 b731
194 000000d7 5f
195 000000d8 a67f
196 000000da ad1b
197 198 000000dc a620
199 000000de b737
200 000000e0 a6a3
201 000000e2 >050002
202 000000e5 a6f6
203 000000e7 >b700
204 000000e9 a610
205 000000eb >b700
206 207 000000ed a60c
208 000000ef >b700
209 000000f1 >a600
210 000000f3 >b700
211 000000f5 9a
212 000000f6 81
213 214 000000f7 4c
215 000000f8 >b700
216 000000fa 5c
217 000000fb >efff
218 000000fd >b300
219 000000ff 26f9
220 00000101 81

*******************************************************************************
* OSD idle condition. *
*******************************************************************************

OSED BSET 3, STAT5, DOFF
BSET 3, STAT5
BRA OSDLE

DOFF BCLR 3, STAT5

OSDLE SEI
BCLR 4, STAT5 NOT ANALOGS
BCLR 2, STAT5 NOT NAME TABLE

DOOP CLR CAS1-1, X OSD CONTROL
DECX
BNE DOOP

JSR CDISP2
CLR $30
CLR $31

BSR OSDECL

LDA #00010000 HORIZONTAL POSITION : ZERO
LDA #10100011 COLOR 1, 0 - RED, CYAN, EDGE ON
LDA #10100110 NO, COLOR 0 - YELLOW

LDA #00010000 SINGLE WIDTH/HIGHT
LDA #00
STA NVOL

LDA #50C DEFAULT TO VOLUME
STA ANAL
LDA #AVOL
STA ANAF

CLT

STA W1

DCLR INCX

STA W1

DCLR DRAM-1,X

BNE DCLR

R6

26
Program/Channel/Name display.

BNTAB FCB $33,$34,0,$23,$28,0,$33,$34
MTAB FCB $24,$0E,0,0,$3E,$21,$2D,$25,$Co

000000102 3334002328003334
00000010a 24000002e212d25
000000113 005e009e003c00fe
00000011b 008b008d006d00a9

000000124 3334002328003334
000000127 005E009E003C00FE
000000129 008B008D006D00A9

000000135 3F30
000000137 3F31
000000139 3F30
00000013b 3F31
00000013d 3F30
00000013f 3F31

000000141 3F30
000000143 3F31
000000145 3F30
000000147 3F31
000000149 3F30
00000014b 3F31
00000014d 3F30
000000150 3F31

000000152 3F30
000000154 3F31
000000156 3F30
000000158 3F31

000000160 3F30
000000162 3F31
000000164 3F30
000000166 3F31

000000168 3F30
00000016a 3F31
00000016c 3F30
00000016e 3F31

000000170 3F30
000000172 3F31
000000174 3F30
000000176 3F31

000000180 3F30
000000182 3F31
000000184 3F30
000000186 3F31

000000188 3F30
00000018a 3F31
00000018c 3F30
00000018e 3F31

000000190 3F30
000000192 3F31
000000194 3F30
000000196 3F31

000000198 3F30
00000019a 3F31
00000019c 3F30
00000019e 3F31

000000198 3F30
00000019a 3F31
00000019c 3F30
00000019e 3F31

0000001a0 3F30
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Look for channel name.
Cursor control (left & right).

CURTAB FCB 3, 4, 12, 13, 14, 15

Cursor control (up & down).

WIND LDA \#00110001 WINDOW BLUE, OFF AT 1/

WIND LDA \#00010001 WINDOW BLACK, OFF AT 17

CUP LDA BROW

CDWN LDA BROW

TOOBSM LDA COUNT

SEC31 BEQ SEC32

FIN30 BRA FIN30

INC COUNT

BRA WIND

BNE TOOBSM

BRA WIND

BNE TOOBSM

BRA WIND
*** Standard change.  ***

CHST BCLR 5, STAT5 DEFAULT TO SECAM

LDX BROW

DECX

LDX M16, X

LDA DRAM+6, X

AND #$3F

CMP #$30

BEQ SIER

BSET 5, STAT5 NO, MAKE IT PAL

JSR SEC30

0000032c >lb00 CHST BCLR

STATS DEFAULT TO SECAM

0000032e >be00

00000330 5a

00000331 5a

00000332 5a

00000333 >de0000

00000336 >d60006

00000339 >a3f

0000033b >a30

0000033c >2002

0000033d 2702

0000033f >a000

00000341 >1c00

00000343 >ed0000

00000346 >a630

00000349 >d70006

0000034c >a621

0000034f >d70007

00000350 >a62c

00000352 >d70008

00000355 >a600

00000357 >d70009

0000035a >a600

0000035c >d7000a

0000035d >a021c

00000360 >a0019

00000363 >a630

00000365 >d70006

00000368 >a625

0000036a >d70007

0000036d >a623

0000036f >d70008

00000372 >a621

00000374 >d70009

00000377 >a62d

00000379 >d7000a

0000037c >a0012

0000037f 9f

00000380 >a0b5

00000382 >b700

00000384 >d60006

00000387 >a400

00000389 >d70006

0000038c 5c

0000038d >b300

0000038f 26f3

00000391 #1

00000393 0d

00000395 a400

00000399 4c

0000039d a43f

0000039f 6d

000003a0 119

000003a3 >a10

000003a6 2410

000003aa a610

000003ad 200c

000003af a121

000003b0 >a202

000003b1 >a621

000003b3 a13a

000003b5 >a202

000003b7 >a600

000003b9 6a

000003ba a43f

000003bb 31

Character change.

*** Character change.  ***

PLUS BSR GETIT

INCA

AND #$3F

CMP #$219

BHI MT9

LTO

CMP #$110

BHS NLTO

LDA #$210

BRA NLTO

MT9

CMP #$212

BHI MTA

LTO

CMP #$33A

BLS NLTO

SPACE

LDA #$200

SPACE

NLTO ORA #$240

STA DRAM, X

JMP SEC30

MINUS BSR GETIT

DECA

AND #$3F

31
GETIT: LDA BROW
SUB $2
LSLA x2
LSLA x4
LSLA x8
ADD BCOL
ADD $bb00
TAX
LDA DRAM, X
RTS

***********************************************************************

* Name store.
* *
* ***********************************************************************

SAVE: LDA $5a0
LDA ADDR
ADD BROW
LSLA
LDA COUNT
ADD $bb00
STA SUBADR
LDA #3
STA W1
STA W2
LDX BROW
DECX
DECX
LSLX
LSLX
LSLX
LSLX
LSLX
LSLX
LSLX
LSLX
LSLX
LDA DRAM+12, X
STA IORUF
LDA DRAM+13, X
STA IORUF+1
LDA $SUBADR
JSR WRITE

INC SUBADR
INC SUBADR
LDA W3
STA #3
STA W1
STA W2
LDA DRAM+14, X
STA $63F
LDA DRAM+15, X
STA IORUF+1
LDA $SUBADR
JSR WRITE

32
** Name store (continued) **

***********************************************************

** Name store (continued) **

***********************************************************

718 0000433 >be00      LDX W3
719 0000435 >d6003      LDA DRAM+3, X
720 0000438 48          LSLA
721 0000439 48          LSLA
722 000043a 48          LSLA
723 000043b 48          LSLA
724 000043c >b700       STA W1
725 000043e >d6004      LDA DRAM+4, X
726 0000441 a40f        AND $0F
727 0000443 >bb00       ADD W1
728 0000445 >c80000     JSR CHEX
729 0000448 >b700       STA IOBUF
730
731 000044a >be00       LDX W3
732 000044c >d60006     LDA DRAM+6, X
733 000044f a43f        AND $3F
734 0000451 a133        CMP $33
735 0000453 2702        BEQ STSEC
736 0000455 >1e00       BSET 7, IOBUF
737
738 0000457 >b600       STSEC LDA COUNT
739 0000459 >bb00       ADD BROW
740 000045b abdc        ADD $3DC
741 000045d >b700       STA SUBADR
742 000045f a602        LDA $2
743 0000461 >b700       STA W1
744 0000463 >b700       STA W2
745 0000465 >ae00       LDX $SUBADR
746 0000467 >c80000     JSR WRITE
747
748 000046a >c80000     JSR SEC30
749 000046d >cc0000     JMP FINBH
750
751
752
753
754
755
756
757 00000470 0a00       LTAB0 FCB 10, 0          IDLE DISPLAY
758 00000472 090800     LTAB1 FCB 9, 8, 0        FR/CH DISPLAY
759 00000475 07080a00   LTAB2 FCB 7, 8, 10, 0  ANALOGUE DISPLAY
760 00000479 0203040506070809 LTAB3 FCB 2, 3, 4, 5, 6, 7, 8, 9, 0 PR/CH/STD/NAME TABLE
761
762 00000482 120304050607080  M16 FCB $10,$20,$30,$40,$50,$60,$70,$80 MUL x 16
763 0000048a 00306090c0f1215 M3 FCB 0, 3, 6, 9, 12, 15, 18, 21 MUL x 3

33
Bottom corner Program/Channel no. display.

00000492 a60c PCOSD LDA #$0C
00000494 >b700 STA ANAL
00000496 >a600 LDA #$AVOL
00000498 >b700 STA ANAF
0000049a >b735 BCLR 4, STAT5 NOT ANALOGS
0000049c #‰#0001010 LDA #$0010000 OD 4 PLL ON
0000049e >b700 STA C34 COLOR 2 = GREEN
000004a0 >a670 LDA #$01110000 HD 4 PLL ON
000004a2 >b735 STA WCR WINDOW OFF (COLUMN 16)
000004a4 >a622 LDA $00100000 HORIZONTAL POSITION : TWO
000004a6 >b737 STA HFD
000004a8 3f30 CLR $30 PUT A SPACE AT 17th AND 18th
000004aa 3f31 CLR $31 CHARACTERS
000004ac 5f CLRX
000004ad a609 LDA #9
000004ae >o0000 JSR OSDCLR CLEAR UNUSED CHARACTERS
000004af >b700 LDA #$16
000004b0 LDA #$31
000004b1 JSR OSDCLR CLEAR UNUSED CHARACTERS
000004b2 a610 PNAME LDA #$16
000004b3 LDA $3
000004b4 >b700 JSR FNAME BEQ SKPQN
000004b5 8f30 CLR $30 PUT A SPACE AT 17th AND 18th
000004b7 8f31 CLR $31 CHARACTERS
000004b9 8f32 CLRX
000004bc a601 SKPQN LDA #$1 START AT 1 TO PREVENT
000004bd a602 LDA OSDL DOUBLE-HIGHT-LINE-SHIFT FLASH
000004be a603 LDA #LTAB1-LTAB0 FIRST TABLE
000004bf 8f50 LDA #$10100011 COLOR 1,0 = RED, CYAN, EDGE ON
000004c0 >214 STA 2, STAT4, PMD2 PROGRAM MODE ?...
000004c1 PMD2 LDA #$101000110 NO, COLOR 0 = YELLOW
000004c2 >b700 STA CAS1
000004c4 a604 STA CAS2
000004c5 a6a3 LDA #$10110000 DOUBLE WIDTH/HIGHT
000004c6 >b700 STA RAD1
000004c8 a600 LDA #$00010000 SINGLE WIDTH/HIGHT
000004c9 a610 STA RAD2
000004ca >b700 LDA #$00010010 WINDOW CYAN
000004cc a612 STA CCR1
000004ce a646 STA CCR2
000004cf a620 SEC5 BSET 4, STAT CHANNEL MODE ?
000004d0 >a646 LDA #$30
000004d2 >b700 BRSET 2, STAT4, S30 NO, 2-DIGIT PROG NO. ENTRY ?
000004d4 >b700 LDA #6
000004d6 a600 S30 STA TMR
000004d7 >b700 RTS
000004d8 8f30
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LOGO

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890
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892
893
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899 00000573 >3900
900 00000575 >b700
901 00000577 ae10
902 00000579 5a
903 0000057a >b300
904 0000057c 270a
905 0000057e 2204
906 00000580 ae14
907 00000582 200d
908 00000584 a60e
909 00000586 2009
910 00000588 >bf00
911 0000058a >be00
912 0000058c >d60000
913 0000058f >be00
914 00000591 >d70020
915 00000594 5d
916 00000595 26e2
917
918 00000597 >cc0000
919
920
***************************************************
* Analogue bar.                                  *
* ***************************************************

LDA W3
CLR W2
LSRA
ROL W2
LSRA
ROL W2
STA W3
LDX #16

CPX W3
BEQ STAR
BHI DOT
LDA #614
BRA SKST
LDX #600
BRA SKST

STX W1
LDX W2
LDA CHAR, X
STX W1
SKST STA DRAM+32,X
BNE LRAN

JMP SEC5
END
300W, 88–108MHz Amplifier using the TP1940 MOSFETs Push-pull Transistor

By Georges Chambaudu
Motorola Semiconducteurs Bordeaux SA

INTRODUCTION

The TP1940 is a high power, high gain and broadband device with low Reverse Transfer Capacitance, C_{rss}. It makes possible fully solid-state transmitters of above 5 kW for FM broadcasts.

Like all MOS devices, it is susceptible to damage from electrostatic discharge. Observe reasonable precautions in handling and packaging it.

The 300 W amplifier described in this Application Note has these features:
- Operates from a 50 V supply
- High power gain
- Compact physical layout
- High efficiency

Typical data for the circuit in Figure 2 are given below.

FUNCTIONAL TESTS (V_{DD} = 50 V, P_{out} = 300 W, I_{dq} = 2 x 200 mA)

<table>
<thead>
<tr>
<th>f (MHz)</th>
<th>Option 1 (with C9p and without C9s)</th>
<th>Option 2 (with C9s and without C9p)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>G_{A} (dB)</td>
<td>η (%)</td>
</tr>
<tr>
<td>108</td>
<td>19.2</td>
<td>62</td>
</tr>
<tr>
<td>98</td>
<td>19.7</td>
<td>62.6</td>
</tr>
<tr>
<td>88</td>
<td>19.4</td>
<td>64</td>
</tr>
</tbody>
</table>

Note:
2. Bias shown is set for 200 mA at 50 V.
3. A copper heat spreader must be mounted on, or laid on top of, a heat sink with thermal grease interface.
4. Drain efficiency can be increased by:
   a. Lowering Drain Idle current (power gain will be reduced by 1–2 dB).
   b. Increasing the value of feedback resistors R8 and R9. This will change the Gain–Frequency slope and Input VSWR. The value of C1 must be raised.
5. In addition to the normal cooling of the units, some air flow is recommended over the top side of the amplifier boards.
Figure 1. Component layout of 300W amplifier (not full size)
C1 24pF Ceramic Chip
C2 1000pF Ceramic Chip
C3, C10, C11 0.1µF Ceramic Chip
C4, C5 1000pF Ceramic Chip
C7 5000pF Ceramic Chip
C8 0.47µF Ceramic Chip or lower values in parallel to reach the value indicated.
C9p ARCO 404, 8-60pF or equivalent
C9s ARCO 425, 40-200pF or equivalent

Note 1: All ceramic capacitors of 5000pF or less in value are ATC type 100 or equivalent.

Note 2: The Table on Page 1 shows the effect of operating with C9p only or C9s only.

R5 6.8 - 8.2kΩ 1/4W (depending on FET gds)
R6 Thermistor, 10kΩ at 25°C/2.5kΩ at 75°C
R7 2kΩ 1/2W
R8, R9 KDI Pyrofilm PPR515-20-3 or EMC Technologie model 5310 or equivalent 100Ω
L1 10 turns AWG #16 enamelled Wire, 0.2" I.D.
L2 Ferrite beads, 1.5 µH Total
L3, L4 Lead lengths of R8 and R9, 0.6" total.
FET TP1940
T1 9:1 impedance ratio (input transformer)
25Ω, 0.062" O.D. semi rigid co-ax, with L = 28 mm, I = 11 mm (see Figure 3)
T2 4:1 impedance ratio (output transformer)
25Ω, 0.090" O.D. semi rigid co-ax, with L = 19 mm, I = 9 mm (see Figure 3)

(T1 transformer must be loaded with ferrite toroids of suitable dimensions and µ of 35-40, or other type ferrite cores, such as Fair-Rite Products Corporation E and I types 9467012002 and 9367021002 respectively.)

Figure 2. 300 W, 88–108 MHz amplifier schematic and parts list
Figure 3. Constructional details of transformers

Epoxy glass 1/16"
The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators for AM, SSB, and suppressed carrier AM; demodulators for the previously mentioned modulation forms; frequency doublers and HF/VHF double balanced mixers.
INTRODUCTION

The Motorola MC1596 monolithic balanced modulator makes an excellent building block for high frequency communications equipment.

The device functions as a broadband, double-sideband suppressed carrier balanced modulator without a requirement for transformers or tuned circuits. In addition to its basic application as a balanced modulator/demodulator, the device offers excellent performance as an SSB product detector, AM modulator/detector, FM detector, mixer, frequency doubler, phase detector, and more.

The article consists of a general description of the MC1596, its gain equations, biasing information, and circuits illustrating typical applications. It is followed by an appendix containing a detailed mathematical ac and dc analysis of the device.

Many readers may find that one of the circuits described in the article will fill the needs of their application. However, it is impossible to show typical circuits for every possible requirement, and the detailed analysis given in the appendix will assist the designer in developing an optimum circuit for any application within the basic capabilities of the MC1596.

MC1596 GENERAL DESCRIPTION

Figure 1 shows a schematic diagram of the MC1596. For purposes of the analysis, the following conventional assumptions have been made for simplification: (1) Devices of similar geometry within a monolithic chip are assumed identical and matched where necessary, and (2) transistor base currents are ignored with respect to the magnitude of collector currents; therefore, collector and emitter currents are assumed equal.

Referring to Figures 1 and 2, the MC1596 consists of differential amplifier Q5 – Q6 driving a dual differential amplifier composed of transistors Q1, Q2, Q3 and Q4. Transistors Q7 and Q8 and associated bias circuitry form constant current sources for the lower differential amplifier Q5 – Q6.

The analysis of operation of the MC1596 is based on the ability of the device to deliver an output which is proportional to the product of the input voltages $V_x$ and $V_y$. This holds true when the magnitudes of $V_x$ and $V_y$ are maintained within the limits of linear operation of the three differential amplifiers in the device. Expressed mathematically, the output voltage (actually output current, which is converted to an output voltage by an external load resistance), $V_O$ is given by

$$V_O = K V_x V_y$$

where the constant $K$ may be adjusted by choice of external components. A detailed description of how the MC1596 circuit configuration performs the basic func-
An example of a four-quadrant multiplier utilizing these principles is the Motorola MC1595, which has been described in a previous article. The MC1595 multiplier contains the basic circuit configuration of the MC1596 plus additional circuitry which results in linear multiplier operation over a large input voltage range. However, the less complex MC1596 has higher frequency response, greater versatility and is less expensive than the MC1595. For these reasons the MC1596 is preferred in many communications applications such as those to be described later in this note.

**DEVICE OPERATION**

The most common mode of operation of the MC1596 consists of applying a high level input signal to the dual differential amplifiers, Q1, Q2, Q3, and Q4, (carrier input port) and a low level input signal to the lower differential amplifier, Q5 and Q6, (modulating signal input port). This results in saturated switching operation of carrier dual differential amplifiers, and linear operation of the modulating differential amplifier.

The resulting output signal contains only the sum and difference frequency components and amplitude information of the modulating signal. This is the desired condition for the majority of the applications of the MC1596.

Saturated operation of the carrier-input dual differential amplifiers also generates harmonics (which may be predicted by Fourier analysis, see Appendix). Reducing the carrier input amplitude to its linear range greatly reduces these harmonics in the output signal. However, it has the disadvantages of reducing device gain and causing the output signal to contain carrier signal amplitude variations.

The carrier input differential amplifiers have no emitter degeneration. Therefore, the carrier input levels for linear and saturated operation are readily calculated. The crossover point is in the vicinity of 15 – 20 mV rms, with linear operation below this level and saturated operation above it.

The modulating-signal differential amplifier has its emitters brought out to pins 2 and 3. This permits the designer to select his own value of emitter degeneration resistance and thereby tailor the linear dynamic range of the modulating-signal input port to a particular requirement. The resistor also determines device gain.

The approximate maximum level of modulating signal input for linear operation is given by the expression:

\[ V_m(\text{peak}) = I_1 R_E \]  

(2)
where $R_E$ = resistance between pins 2 and 3, and $I_1$ refers to the notation in the analysis model shown in Figure 2. Since base currents were assumed to be zero and transistors identical,

$$I_1 = I_5$$

where $I_5$ = current flowing into pin 5. Therefore, Equation (2) becomes

$$V_y(\text{peak}) = I_5 R_E$$

Device voltage gain (single ended output with respect to modulating signal input) is given by the expression (also see Appendix):

$$A_v = \frac{R_L}{R_E} f(m)$$

where

$$f(m) = \left( \frac{e^{m} \cdot e^{-m}}{1 + e^{m} \cdot e^{-m}} \right)$$

$$m = \frac{V_X}{kT}$$

$f(m)$ may be approximated for the two general cases of high and low level carrier operation, resulting in the following gain expressions: High level case ($V_X > 100$ mV peak):

$$f(m) \approx 1$$

therefore,

$$|A_v| \approx \frac{R_L}{R_E}$$

The low-level case ($V_X < 50$ mV peak) is given by:

$$f(m) \approx \frac{-m}{2}$$

therefore

$$|A_v| \approx \frac{R_{LM}}{2R_E}$$

The foregoing expressions assume the condition $R_E >> r_e$, where $r_e$ is the dynamic emitter resistance of transistors Q5 and Q6. When $I_1 = 1$ mA, $r_e$ is approximately 26 ohms at room temperature.

There are numerous applications where it is desirable to set $R_E$ equal to some low value or zero. For this condition, Equations (7) and (9) can be expanded to the more general form:

high-level $V_X$:

$$|A_v| \approx \frac{R_L}{R_E + 2r_e}$$

low-level $V_X$:

$$|A_v| \approx \frac{R_{LM}}{2(R_E + 2r_e)}$$

Equations (10) and (11) summarize the single ended conversion voltage gains of the MC1596 with a dc input voltage ($V_X$) at the carrier port. Operation with a differential output would increase the gains by 6 dB.

Equations (10) and (11) may be combined with Equations (26) and (29) in the Appendix to compute the conversion gain of the MC1596 operating as a double sideband suppressed carrier modulator (dc carrier input).

For a high level carrier input signal, the expressions for output voltage and voltage gain become

$$V_O = \frac{R_L V_y}{R_E + 2r_e} \sum_{n=1}^{\infty} A_n \left[ \cos(n\omega_X + \omega_y)t + \cos(n\omega_X - \omega_y)t \right]$$

where $A_n = \left( \frac{\sin \frac{n\pi}{2}}{\sin \frac{n\pi}{2}} \right)$

Solving Equation (12) for the sidebands around $f_X$ ($n = 1$) yields:

$$V_O = \frac{R_L V_y}{R_E + 2r_e} (0.637) \left[ \cos(\omega_X + \omega_y)t + \cos(\omega_X - \omega_y)t \right]$$

Equation (13) may be further simplified to give the voltage gain for the amplitude of each fundamental sideband:

$$\frac{V_O}{V_y} = A_v = \frac{0.637 R_L}{R_E + 2r_e}$$

For the low level $V_X$ case:

$$V_O = \frac{-R_L V_y \cos(\omega_Y)t}{2(R_E + 2r_e)} \left[ \frac{V_X(\cos \omega_X)t}{kT/q} \right]$$

$$V_O = \frac{-R_L V_y V_X(\cos \omega_X + \omega_Y)t + \cos(\omega_X - \omega_Y)t}{4(\frac{kT}{q})(R_E + 2r_e)}$$

And the voltage gain for each sideband becomes:

$$\left| \frac{V_O}{V_y} \right| = |A_v| = \frac{R_L V_X(\text{rms})}{2 \sqrt{2} \left( \frac{kT}{q} \right)(R_E + 2r_e)}$$

Equations (14) and (17) summarize the single ended conversion voltage gains of the MC1596 for low and high level ac carrier inputs. Note that these gain expressions are calculated for the output amplitude of each of the two desired sidebands. The composite output signal consists of the sum of these two sidebands in the low level case and
in the high level case it is the sum of the sidebands of the
carrier and all the odd numbered harmonics of the carrier.

Laboratory gain measurements have shown good corre­
lation with Equations (10), (11), (14) and (17).

DC BIAS

A significant portion of the DC bias circuitry for the
MC1596 must be supplied externally. While this has the
disadvantage of requiring several external components, it
has the advantage of versatility. The MC1596 may be
operated with either single or dual power supplies at practically
any supply voltage(s) a semiconductor system has avail­
able. Further, the external load and emitter resistors pro­
vide the designer with complete freedom in setting device
gain.

The DC bias design procedure consists of setting bias
currents and 4 bias voltage levels, while not exceeding ab­
solute maximum voltage, current, and dissipation ratings.

The current levels in the MC1596 are set by controlling
I5 (subscripts refer to pin numbers). For bias current de­
sign the following assumption may be made:

\[
I_5 = I_6 = I_9 = \frac{I_{10}}{3}
\]

Since base currents may be neglected, I5 flows through
a forward biased diode and a 500Ω resistor to pin 10.

When pin 10 is grounded, I5 is most conveniently ad­
justed by driving pin 5 from a current source.

When pin 10 is connected to a negative supply, I5 may
be set by connecting a resistor from pin 5 to ground (R5). The value of R5 may be computed from the following
expression:

\[
R_5 = \frac{V_{10}}{I_5} \cdot \frac{\phi}{500 \Omega}
\]  

where \( \phi \) is the diode forward voltage, or about 0.75Vdc at
\( T_A = 25^\circ C \).
The absolute maximum rating for I5 is 10mA.

For all applications described in this article, bias cur­
cent I5 has been set at 1 mA. The MC1596 has been char­
acterized at this bias current and it is the recommended
current unless there is a conflict with power dissipation
requirements.
The 4 bias voltage levels that must be set up exter­
nally are:

- pins 6 and 9 most positive.
- pins 7 and 8 next most positive.
- pins 1 and 4 next most positive.
- pin 10 most negative.

The intermediate voltage levels may be provided by a
voltage divider(s) or any other convenient source such as
ground in a dual power supply system.

It is recommended that the voltage divider be designed
for a minimum current of 1mA. Then I1, I4, I7, and I8
need not be considered in the divider design as they are transis­
tors base currents.

Guidelines for setting up the bias voltage levels include
maintaining at least 2 volts collector-base bias on all transis­
tors while not exceeding the voltages given in the abso­
lute maximum rating table:

- \( V_6; V_9 \geq (V_{7}, V_8) \geq 2 \) Vdc
- \( V_7; V_8 \geq (V_{1}, V_4) \geq 2.7 \) Vdc
- \( V_6; V_9 \geq (V_{1}, V_4) \geq 2.7 \) Vdc

The foregoing conditions are based on the following as­
sumptions:

\[
V_6 = V_9, \quad V_7 = V_8, \quad V_4 = V_1
\]

The other consideration in bias design is total device
dissipation, which must not exceed 680 mW and 575 mW
at \( T_A = 25^\circ C \), respectively, for the metal and ceramic dual
in-line packages.

From the assumptions made above total device dissi­
pation may be computed as follows:

\[
P_D = 2 I_5(V_6 - V_10) + I_5(V_5 - V_{10}) \tag{19}
\]

For examples of various bias circuit designs, refer to
Figures 3, 8 and 9.

BALANCED MODULATOR

Figure 3 shows the MC1596 in a balanced modulator
circuit operating with \(+12\) and \(-8\) volt supplies. Excellent
gain and carrier suppression can be obtained with this cir­
cuit by operating the upper (carrier) differential amplifiers
at a saturated level and the lower differential amplifier in
a linear mode. The recommended input signal levels are
60 mV rms for the carrier and 300 mV rms for the maxi­
mum modulating signal levels.

For these input levels, the suppression of carrier, car­
rrier harmonics, and sidebands of the carrier harmonics is
given in Figures 4 and 5.

The modulating signal must be kept at a level to insure
linear operation of lower differential amplifier Q5 – Q6. If the signal input level is too high, harmonics of the mod­
ulating signal are generated and appear in the output as
spurious sidebands of the suppressed carrier. For a maxi­
mum modulating signal input of 300 mV rms, the suppres­
sion of these spurious sidebands is typically 55 dB at a car­
rrier frequency of 500 kHz.

Sideband output levels are shown in Figure 6 for vari­
ous input levels of both carrier and modulating signal for
the circuit of Figure 3.

Operating with a high level carrier input has the ad­
vantages of maximizing device gain and insuring that any
amplitude variations present on the carrier do not appear
on the output sidebands. It has the disadvantage of in­
creasing some of the spurious signals.

Fourier analysis for a 50% duty cycle switching wave­
form at the carrier differential amplifiers predicts no even
harmonics of the carrier (Appendix). However, the second
harmonic of the carrier is suppressed only about 20 dB in
the LF and HF range with a 60 mV carrier injection level, apparently due to factors such as the waveform not being a perfect square wave and slight mismatch between transistors. If the sine wave carrier signal is replaced with a 300 mV peak-to-peak square wave, an additional 15 dB of carrier, second-harmonic suppression is achieved. Attempting to accomplish the same result by increasing carrier sine-wave amplitude degrades carrier suppression due to additional carrier feedthrough with, however, no increase in the desired sideband output levels.

Operation with the carrier differential amplifiers in a linear mode theoretically should produce only the desired sidebands with no spurious outputs. Such linear operation is achieved by reducing the carrier input level to 15 mV rms or less.

This mode of operation does reduce spurious output levels significantly. Table I lists a number of the spurious output levels for high (60 mV) and low (10 mV) level carrier operation. Reduction of carrier injection from 60 mV to 10 mV decreased desired sideband output by 12.4 dB. This is in excellent agreement with the analysis in the Appendix, which predicts 12.5 dB.

Spurious levels during low level operation are so low that they are affected significantly by the special purity of the carrier input signal. For example, initial readings for Table I were taken with a carrier signal generator which has second and third harmonics 42 and 45 dB below the fundamental, respectively. Additional filtering of the carrier input signal was required to measure the true second and third carrier-harmonic suppression of the MC1596.

The decision to operate with a low or high level carrier input would of course depend on the application. For a typical filter-type SSB generator, the filter would remove all spurious outputs except some spurious sidebands of the carrier. For this reason operation with a high level carrier would probably be selected to maximize gain and insure that the desired sideband does not contain any spurious amplitude variations present on the carrier input signal.

On the other hand, in a low frequency broadband balanced modulator spurious outputs at any frequency may be undesirable and low level carrier operation may be the best choice.

Good carrier suppression over a wide temperature range requires low dc resistances between the bases of the lower differential amplifier (pins 1 and 4) and ground. It is recommended that the values of these resistors not be increased significantly higher than the 51 ohms utilized in
FIGURE 7 – Amplitude Modulator

FIGURE 8 – Product Detector +12 Vdc Single Supply

FIGURE 9 – Double Balanced Mixer, Broadband Inputs, 9 MHz Tuned Output
the circuit shown in Figure 3 in applications where carrier suppression is important over full operating temperature range of -55°C to +125°C. Where operation is to be over a limited temperature range, resistance values of up to the low kilohm range may be used.

AMPLITUDE MODULATOR

The MC1596 balanced modulator circuit shown in Figure 3 will function as an amplitude modulator with just one minor modification. All that is necessary is to unbalance the carrier null to insert the proper amount of carrier into the output signal. However, the null circuitry used for balanced modulator operation does not provide sufficient adjustment range and must be modified. The resulting amplitude modulator is shown in Figure 7. This modulator will provide excellent modulation at any percentage from zero to greater than 100 percent.

PRODUCT DETECTOR

Figure 8 shows the MC1596 in an SSB product detector configuration. For this application, all frequencies except the desired demodulated audio are in the RF spectrum and can be easily filtered in the output. As a result, the carrier null adjustment need not be included.

Upper differential amplifiers Q1 – Q2 and Q3 – Q4 are again driven with a high level signal. Since carrier output level is not important in this application (carrier is filtered in the output) carrier input level is not critical. A high level carrier input is desirable to maximize gain of the detector and to remove any carrier amplitude variations from the output. The circuit of Figure 8 performs well with a carrier input level of 100 to 500 mV rms.

The modulated signal (single-sideband, suppressed carrier) input level to differential amplifier pair Q5 – Q6 is maintained within the limits of linear operation. Excellent linearity and undistorted audio output may be achieved with an SSB input signal level range 50 to 100 mV rms. Again, no transformers or tuned circuits are required for excellent product detector performance from very low frequencies up to 100 MHz.

Another advantage of the MC1596 product detector is its high sensitivity. The sensitivity of the product detector shown in Figure 8 for a 9 MHz SSB signal input and a 10 dB signal plus noise (S+N)/N ratio at the output is 3 microvolts. For a 20 dB (S+N)/N ratio audio output signal it is 9 microvolts.

For a 20 dB (S+N)/N ratio, demodulated audio output signal, a 9 MHz SSB input signal power of -101 dBm is required. As a result, when operated with an SSB receiver with a 50 ohm input impedance, a 0.5 microvolt RF input signal would require only 12 dB overall power gain from antenna input terminals to the MC1596 product detector.

Note also that dual outputs are available from the product detector, one from pin 6 and another from pin 9. One output can drive the receiver audio amplifiers while a separate output is available for the AGC system.

AM DETECTOR

The product detector circuit of Figure 8 may also be used as an AM detector. The modulated signal is applied to the upper differential amplifiers while the carrier signal is applied to the lower differential amplifier.

Ideally, a constant amplitude carrier signal would be obtained by passing the modulated signal through a limiter ahead of the MC1596 carrier input terminals. However, if the upper input signal is at a high enough level (>50 mV), its amplitude variations do not appear in the output signal. For this reason it is possible to use the product detector circuit shown in Figure 8 as an AM detector simply by applying the modulated signal to both inputs at a level of about 600 mV on modulation peaks without using a limiter ahead of the carrier input port. A small amount of distortion will be generated as the signal falls below 50 mV during modulation valleys, but it will probably not be significant in most applications. Advantages of the MC1596 AM detector include linear operation and the ability to have a detector stage with gain.

MIXER

Since the MC1596 generates an output signal consisting of the sum and difference frequencies of the two input signals only, it can also be used as a double balanced mixer.

Figure 9 shows the MC1596 used as a high frequency mixer with a broadband input and a tuned output at 9 MHz. The 3 dB bandwidth of the 9 MHz output tank is 450 kHz.

The local oscillator (LO) signal is injected at the upper input port with a level of 100 mV rms. The modulated signal is injected at the lower input port with a maximum level of about 15 mV rms. Note that for maximum conversion gain and sensitivity the external emitter resistance on the lower differential amplifier pair has been reduced to zero.

For a 30 MHz input signal and a 39 MHz LO, the mixer has a conversion gain of 13 dB and an input signal sensitivity of 7.5 microvolts for a 10 dB (S+N)/N ratio in the 9 MHz output signal. With a signal input level of 20 mV, the highest spurious output signal was at 78 MHz (2 fLO) and it was more than 30 dB below the desired 9 MHz output. All other spurious outputs were more than 50 dB down.

As the input is broadband, the mixer may be operated at any HF and VHF input frequencies. The same circuit was operated with a 200 MHz input signal and a 209 MHz LO. At this frequency the circuit had 9 dB conversion gain and a 14 microvolt sensitivity.

Greater conversion gains can be achieved by using tuned circuits with impedance matching on the signal input port. Since the input impedance of the lower input port is considerably higher than 50 ohms even with zero emitter resistance, most of the signal input power in the broadband configuration shown is being dissipated in the 50 ohm resistor at the input port.

The circuit shown has the advantage of a broadband input with simplicity and reasonable conversion gain. If
greater conversion gain is desired, impedance matching at
the signal input is recommended.

The input impedance at the signal input port is plotted
in Figures 10 and 11. The output impedance is also shown
in Figure 12. Both of these curves indicate the complex
impedance versus frequency for single ended operation.

The nulling circuit permits nulling of the LO signal and
results in a few dB additional LO suppression in the mixer
output. The nulling circuitry (the two 10 kΩ resistors and
50 kΩ potentiometer) may be eliminated when operating
with a tuned output in many applications where the com­
bination of inherent device balance and the output tank
provide sufficient LO suppression.

The tuned output tank may be replaced with a resis­
tive load to form a broadband input and output doubly­
balanced mixer. Magnitude of output load resistance be­
comes a simple matter of tradeoff between conversion gain
and output signal bandwidth. As shown in Figure 12, the
single ended output capacitance of the MC1596 at 9 MHz
is typically 5 pF.

With a 50 Ω output load, a 30 MHz input signal level
of 20 mV, and a 39 MHz LO signal level of 100 mV the
conversion gain was -8.4 dB (loss). Isolation was 30 dB
from input signal port to output port and 18 dB from LO
signal port to output port.

DOUBLER

The MC1596 functions as a frequency doubler when
the same signal is injected in both input ports. Since the
output signal contains only 2ω1 and 2ω2 frequency com­
ponents, there will be only a single output frequency at
2ω1 when ω1 = ω2.

For operation as a broadband low frequency doubler,
the balanced modulator circuit of Figure 3 need be modi­
fied only by adding ac coupling between the two input
ports and reducing the lower differential amplifier emitter
resistance between pins 2 and 3 to zero (ties in 2 to pin
3). The latter modification increases the circuit sensitiv­
ity and doubler gain.

A low frequency doubler with these modifications is
shown in Figure 13. This circuit will double in the audio
and low frequency range below 1 MHz with all spurious
outputs greater than 30 dB below the desired 2fIN output
signal.

For optimum output-signal spectral purity, both upper
and lower differential amplifiers should be operated within
their linear ranges. This corresponds to a maximum input
signal level of 15 mV rms for the circuit shown in Figure
13.

If greater signal handling capability is desired the cir­
cuit may be modified by using a 1000 Ω resistance be­
tween pins 2 and 3 and a 10:1 voltage divider to reduce the
input signal at the upper port to 1/10 the signal level at
the lower port.

The MC1596 will also function very well as an RF
doubler at frequencies up to and including UHF. Either a
broadband or a tuned output configuration may be used.

Suppression of spurious outputs is not as good at VHF
and UHF. However, in the broadband configuration, the desired doubled output is still the highest magnitude output signal when doubling from 200 to 400 MHz, where the spurious outputs are 7 dB or more below the 400 MHz output. Even at this frequency the MC1596 is still superior to a conventional transistor doubler before output filtering.

Figure 14 shows a 150 to 300 MHz doubler with output filtering. All spurious outputs are 20 dB or more below the desired 300 MHz output.

**FM DETECTOR AND PHASE DETECTOR**

The MC1596 provides a dc output which is a function of the phase difference between two input signals of the same frequency, and can therefore be used as a phase detector. This characteristic can also be utilized to design an
FM detector with the MC1596. All that is required is to provide a means by which the phase difference between the signals at the two input ports vary with the frequency of the FM signal.

Phase dependent FM detector operation can be explained by considering input and output currents for a high level signal at both input ports. These waveforms are shown in Figure 15 with inputs in phase at A and out of phase at B.

Since the output current is a constant times the product of the input currents, Figure 15 illustrates how a shift in phase between the two input signals causes a dc level shift in the output.

SUMMARY

A number of applications of the MC1596 monolithic balanced modulator integrated circuit have been explored. The basic device characteristics of providing an output signal at the sum and difference of the two input frequencies with options on gain and amplitude characteristics will undoubtedly lead to numerous other applications not discussed in this article.

REFERENCES


APPENDIX

AC AND DC ANALYSIS

With reference in Figure 2 of the text, the following equations apply:

\[ I_y = \frac{V_y}{R_E} \quad (\text{when } R_E \gg r_e, \text{ the transistor dynamic emitter resistance}) \]  

\[ I_2 = \frac{I_1 + I_y}{\frac{V_x}{a}} \quad I_3 = \frac{I_1 + I_y}{\frac{V_x}{a}} \quad I_4 = \frac{I_1 - I_y}{\frac{V_x}{a}} \quad I_5 = \frac{I_1 - I_y}{\frac{V_x}{a}} \]  

\[ I_A = I_2 + I_4 = \left(\frac{I_1 + I_y}{1 + e^m} + \frac{I_1 - I_y}{1 + e^m}\right) \]  

\[ I_B = I_3 + I_5 = \left(\frac{I_1 + I_y}{1 + e^m} + \frac{I_1 - I_y}{1 + e^m}\right) \]  

where

\[ a = \frac{kT}{q} \]  

\[ m = \frac{V_x}{a} \]  

\[ I_A \cdot I_B = (I_1 + I_y) \left(\frac{1}{1 + e^m} - \frac{1}{1 + e^m}\right) \]  

\[ + (I_1 \cdot I_y) \left[ \frac{1}{1 + e^m} \cdot \frac{1}{1 + e^m}\right] \]

\[ = (I_1 + I_y) \left[ \frac{1 + e^m \cdot 1 \cdot e^{-m}}{(1 + e^m)(1 + e^{-m})} \right] \]

\[ + (I_1 \cdot I_y) \left[ \frac{1 + e^m \cdot 1 \cdot e^{-m}}{(1 + e^m)(1 + e^{-m})} \right] \]

\[ \Delta V_0 = (I_A \cdot I_B) \frac{R_L}{R_E} \]

\[ = \frac{2I_y (e^m \cdot e^m)}{(1 + e^m)(1 + e^m)} \]

\[ \frac{\Delta V_0}{V_{in}} = \frac{2R_L}{V_{in}} \frac{e^m \cdot e^m}{(1 + e^m)(1 + e^m)} \]

But,

\[ I_y = \frac{V_{in}}{R_E} \]

Therefore,

\[ \frac{\Delta V_0}{V_{in}} = \frac{2R_L}{V_{in}} \left(\frac{e^m \cdot e^m}{(1 + e^m)(1 + e^m)}\right) \]
recalling that 

\[ m = \frac{V_x}{a} = \frac{kT}{q} \]

From this it can be seen that voltage gain is a function of the input level supplied to the upper four transistors:

\[ \frac{\Delta V_o}{V_{in}} = AV = \frac{2RL}{RE} [f(m)], \quad (9A) \]

and

\[ V_o = \frac{2RLV_y}{RE} [f(m)], \quad (10A) \]

A curve of \( f(m) \) versus input level supplied to the upper quad differential amplifier is shown in Figure 16 of the text.

![Figure 16 - Vx versus [fm]](image)

The MC1596 is therefore a linear multiplier over the range of \( V_x \) for which \( [f(m)] \) is a linear function of \( V_x \). This range of \( x \) can be obtained by inspection of Figure 16 and is approximately zero to 50 millivolts.

Examining the case of a small signal \( V_x \) input level mathematically yields:

Assume \( V_x \ll a \) \quad (11A)

Then:

\[ e^m \ll 0.1 \quad (12A) \]

\[ e^m \approx 1 + m \quad (13A) \]

\[ e^{-m} \approx 1 - m \]

\[ [f(m)] \approx \frac{(1 - m) \cdot (1 + m)}{(2 + m) \cdot (2 - m)} = \left( \frac{-2m}{4 - m^2} \right) \quad (14A) \]

\[ \left( \frac{-2m}{4 - m^2} \right) \approx \frac{-2m}{4} = \frac{-m}{2} \quad (15A) \]

Therefore

\[ AV = \frac{V_o}{V_y} = \frac{2RL}{RE} \frac{(m)}{2} = \frac{-RLm}{RE} \quad (16A) \]

Equation (17A) shows that the MC1596 is a linear multiplier when \( V_x \ll 2.6 \) mV. However, as was observed by inspection of Figure 16 earlier, the device is capable of approximate linear multiplier operation when \( V_x \ll 50 \) mV.

For the case of a large signal \( V_x \) input level:

\[ V_x \gg a \quad (18A) \]

\[ e^m \gg 1 \quad (19A) \]

\[ e^{-m} \ll 1 \]

\[ AV = \frac{2RL}{RE} \left[ \frac{e^m}{e^{-m}} \right] = \frac{-2RL}{RE} \quad (20A) \]

\[ V_o = \frac{-2RLV_y}{RE} \quad (21A) \]

Equation (20A) indicates that in this mode the output level is independent of the level of \( V_x \). This characteristic is useful in many communications applications of the MC1596.

![Figure 17 - Input and Output Waveforms for a High Level Upper Input and Low Level Lower Input Signals](image)

Mathematical analysis for ac input signals is given below for two modes of operation which cover most applications of the MC1596. These modes are (1) \( V_x \) and \( V_y \) both low level sine waves, and (2) low level sine wave for \( V_y \) and a large signal input for \( V_x \) (either a high level sine wave or a square wave input) giving rise to a symmetrical switching operation of the upper differential amplifier quad, Q1, Q2, Q3, and Q4.
For sine wave input signals,

\[ V_x = E_x \cos \omega_x t \]  \hspace{1cm} (22A)
\[ V_y = E_y \cos \omega_y t \]  \hspace{1cm} (23A)

where \( E_x \) and \( E_y \) are the peak values of the x and y input voltages, respectively. Therefore,

\[ V_0 = K E_x E_y (\cos \omega_x t) (\cos \omega_y t) \]  \hspace{1cm} (24A)

Performing this multiplication yields:

\[ V_0 = \frac{K E_x E_y}{2} \cos (\omega_x + \omega_y) t + \cos (\omega_x - \omega_y) t \]  \hspace{1cm} (25A)

The second mode of operation can be analyzed by assuming square wave switching function in the upper differential amplifiers and applying Fourier analysis.

The Fourier series form for the symmetrical square wave signal shown in Figure 17 is

\[ s(t) = 2 \sum_{n=1}^{\infty} A_n \cos n \omega_x t \]  \hspace{1cm} (26A)

where the Fourier coefficients are

\[ A_n = \left[ \frac{\sin \frac{\pi n}{2}}{\frac{\pi n}{2}} \right] \]  \hspace{1cm} (27A)

The output voltage is therefore:

\[ V_0 = KE_y \sum_{n=1}^{\infty} A_n \left[ \cos(n\omega_x + \omega_y)t + \cos(n\omega_x - \omega_y)t \right] \]  \hspace{1cm} (28A)

Note that Equation (25A) predicts that for low level input signals, the output signal consists of the sum and difference frequencies \((\omega_x \pm \omega_y)\) only, while Equation (28A) predicts that operation with a high level input for \( V_x \) input will yield outputs at frequencies \( 2\omega_x \pm \omega_y, 3\omega_x \pm \omega_y, 5\omega_x \pm \omega_y, \text{etc.} \)
The fundamental design concepts for phase locked loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example.
INTRODUCTION

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

PARAMETER DEFINITION

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). This response is twofold in nature in that it contains both the transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.

The parameters in Figure 1 are defined and will be used throughout the text.

Using servo theory, the following relationships can be obtained:

\[ \theta_e(s) = \frac{1}{1 + G(s)H(s)} \theta_i(s) \]  

\[ \theta_o(s) = \frac{G(s)}{1 + G(s)H(s)} \theta_i(s) \]

These parameters relate to the functions of a PLL as shown in Figure 2.
The phase detector produces a voltage proportional to the phase difference between the signals $\theta_i$ and $\theta_0/N$. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM - Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$ f_0 = N f_i $$

(3)
during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path ($N = 1$). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

**TYPE - ORDER**

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The type of a system refers to the number of poles of the loop transfer function $G(s) H(s)$ located at the origin. Example:

$$ G(s) H(s) = \frac{10}{s(s + 10)} $$

(4)

This is a type one system since there is only one pole at the origin.

The order of a system refers to the highest degree of the polynomial expression

$$ 1 + G(s) H(s) = 0 \Rightarrow C.E. $$

(5)
which is termed the Characteristic Equation (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function. Example:

$$ G(s) H(s) = \frac{10}{s(s + 10)} $$

then

$$ 1 + G(s) H(s) = 1 + \frac{10}{s(s + 10)} = 0 $$

(7)

therefore

$$ C.E. = s(s + 10) + 10 $$

(8)

$$ C.E. = s^2 + 10s + 10 $$

(9)

which is a second order polynomial. Thus, for the given $G(s) H(s)$, we obtain a type 1 second order system.

**ERROR CONSTANTS**

Various inputs can be applied to a system. Typically these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_0(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_0(s)/N$. In evaluating a system, $\theta_0(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_0(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.

Simply stated

$$ \lim_{t \to \infty} \theta(t) = \lim_{s \to 0} [s \theta_0(s)] $$

(10)

Where

$$ \theta_0(s) = \frac{1}{1 + G(s) H(s)} \theta_i(s) $$

(11)

The input signal $\theta_i(s)$ is characterized as follows:

Step position: $\theta_i(t) = C_p \ t \geq 0$

(12)

Or. in Laplace notation: $\theta_i(s) = \frac{C_p}{s}$

(13)

where $C_p$ is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by $C_p$ radians:

Step velocity: $\theta_i(t) = C_v \ t \geq 0$

(14)

Or. in Laplace notation: $\theta_i(s) = \frac{C_v}{s^2}$

(15)

where $C_v$ is the magnitude of the rate of change of phase in radians per second. This corresponds to inputting a frequency that is different than the feedback portion of the VCO frequency. Thus, $C_v$ is the frequency difference in radians per second seen at the phase detector:

Step acceleration: $\theta_i(t) = C_a \ t^2 \geq 0$

(16)

Or. in Laplace notation: $\theta_i(s) = \frac{C_a}{s^3}$

(17)

$C_a$ is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop $G(s) H(s)$ transfer functions for types 1, 2, and 3 are:

$$ G(s) H(s) = \frac{K}{s(s + \alpha)} $$

(18)
Type 2 \( G(s) H(s) = \frac{K(s + a)}{s^2} \) \( \text{(19)} \)

Type 3 \( G(s) H(s) = \frac{K(s + a)(s + b)}{s^3} \) \( \text{(20)} \)

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

\[
\theta_e(s) = \left( \frac{1}{K} \right) \left( \frac{C_p}{s} \right) \left( \frac{s + a}{s^2 + as + K} \right)
\]

\[
\theta_e(t=\infty) = \lim_{s \to 0} \left( \frac{s + a}{s^2 + as + K} \right) C_p = 0 \] \( \text{(21)} \)

Thus the final value of the phase error is zero when a step position (phase) is applied.

Similarly applying the three inputs into type 1, 2 and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

**TABLE 1 -- Steady State Phase Errors for Various System Types**

<table>
<thead>
<tr>
<th></th>
<th>Type 1</th>
<th>Type 2</th>
<th>Type 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step Position</td>
<td>Zero</td>
<td>Zero</td>
<td>Zero</td>
</tr>
<tr>
<td>Step Velocity</td>
<td>Constant</td>
<td>Zero</td>
<td>Zero</td>
</tr>
<tr>
<td>Step Acceleration</td>
<td>Continually Increasing</td>
<td>Constant</td>
<td>Zero</td>
</tr>
</tbody>
</table>

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table 1 the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

**STABILITY**

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.²

**Rule 1** - The root locus begins at the poles of \( G(s) H(s) \) \((K = 0)\) and ends at the zeroes of \( G(s) H(s) \) \((K = \infty)\). Where \( K \) is loop gain.

**Rule 2** - The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of \( G(s) H(s) \).

**Rule 3** - The root locus contour is bounded by asymptotes whose angular position is given by

\[
\frac{2n + 1}{\#P - \#Z} \pi \quad n = 0, 1, 2, \ldots
\]

Where \( \#P \) (\( \#Z \)) is the number of poles (zeroes).

**Rule 4** - The intersection of the asymptotes is positioned at the center of gravity \( C.G. \)

\[
C.G. = \frac{\Sigma P - \Sigma Z}{\#P - \#Z}
\]

Where \( \Sigma P \) (\( \Sigma Z \)) denotes the summation of the poles (zeroes).

**Rule 5** - On a given section of the real axis, root loci may be found in the section only if the \( \#P + \#Z \) to the right is odd.

**Rule 6** - Breakaway points from negative real axis is given by:

\[
\frac{dK}{ds} = 0
\]

Again where \( K \) is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

\[
G(s) H(s) = \frac{K}{s(s + 4)}
\]

The root locus has two branches (Rule 2) which begin at \( s = 0 \) and \( s = -4 \) and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes the equation becomes:

\[
\frac{2n + 1}{2} \pi = \begin{cases} 
\pi & \text{for } n = 0 \\
\frac{3\pi}{2} & \text{for } n = 1
\end{cases}
\]

58
The position of the intersection according to the Rule 4 is:

\[
 s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4 - 0) - (0)}{2 - 0}
\]

\[s = -2 \quad (28)\]

The breakaway point as defined by Rule 6 can be found by first writing the characteristic equation.

\[
\text{C.E.} - 1 + G(s) H(s) = 0
\]

\[= 1 + \frac{K}{s(s + 4)} = s^2 + 4s + K = 0 \quad (29)\]

Now solving for \(K\) yields

\[K = -s^2 - 4s \quad (30)\]

Taking the derivative with respect to \(s\) and setting it equal to zero then determines the breakaway point.

\[
\frac{dK}{ds} = \frac{d}{ds} (-s^2 - 4s) \quad (31)
\]

\[\frac{dK}{ds} = -2s - 4 = 0 \quad (32)\]

or

\[s = -2 \quad (33)\]

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

This second order characteristic equation given by Equation 29 has been normalized to a standard form

\[s^2 + 2 \xi \omega_n s + \omega_n^2 = 0 \quad (34)\]

where the damping ratio \(\xi = \cos \phi \ (0^\circ \leq \phi \leq 90^\circ)\) and \(\omega_n\) is the natural frequency as shown in Figure 3.

The response of this type 1, second order system to a step input is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

The overshoot and stability as a function of the damping ratio \(\xi\) is illustrated by the various plots. Each response is plotted as a function of the normalized time \(\omega_n t\). For a given \(\xi\) and a lock-up time \(t\), the \(\omega_n\) required to achieve the desired results can be determined. Example:

Assume \(\xi = 0.5\)

\[\text{error} < 10\% \quad \text{for} \ t > 1 \text{ ms} \]

From \(\xi = 0.5\) curve the error is less than 10% of final value for all time greater than \(\omega_n t = 4.5\). The required \(\omega_n\) can then be found by:

\[\omega_n t = 4.5 \quad (35)\]

Or

\[\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ rad/s} \quad (36)\]
\[ \zeta \text{ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.} \]

Example:

Another common loop transfer function takes the form

\[ G(s)H(s) = \frac{(s + a)K}{s^2} \quad (37) \]

This is a type 2 second order system. A zero is added to provide stability. (Without the zero the poles would move along the jw axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is \( s = a \); however, with only one asymptote there is no intersection at this point. The root locus lies on a circle centered at \( s = -a \) and continues on all portions of the negative real axis to left of the zero. The breakaway point is \( s = -2a \).

![Figure 5 - Type 2 Second Order Root Locus Contour](image)

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example the required \( \omega_n \) can be determined by the use of the graph when \( \xi \) and the lock up time are given.

**BANDWIDTH**

The -3 dB bandwidth of the PLL is given by

\[ \omega_{-3\,dB} = \omega_n \left( 1 + 2 \xi^2 + \sqrt{2 + 4 \xi^2 + 4 \xi^4} \right)^{1/2} \quad (38) \]

for a type 1 second order system, and by

\[ \omega_{-3\,dB} = \omega_n \left( 1 + 2 \xi^2 + \sqrt{2 + 4 \xi^2 + 4 \xi^4} \right)^{1/2} \quad (39) \]

for a type 2 second order system.

**PHASE-LOCKED LOOP DESIGN EXAMPLE**

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach to these design constraints is now illustrated. It is desired for the system to have the following specifications:

- Output frequency: 2.0 MHz to 3.0 MHz
- Frequency steps: 100 kHz
- Phase coherent frequency output
- Lock up time between channels: 1 ms
- Overshoot: < 20%

**NOTE:** These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer.

From the given specifications the circuit parameters shown in Figure 7 can now be determined.

The devices used to configure the PLL are:

- Frequency-Phase Detector: MC4044/4344
- Voltage Controlled Multivibrator (VCM): MC4024/4324
- Programmable Counter: MC4016/4316

The forward and feedback transfer functions are given by:

\[ G(s) = K_p K_f K_0 \quad H(s) = K_n \quad (40) \]

where \( K_n = 1/N \)

\[ \text{FIGURE 6 - Type 2 Second Order Step Response} \]
The programmable counter divide ratio $K_n$ can be found from Equation 3.

\[
N_{\text{min}} = \frac{f_0}{f_1} = \frac{f_0}{f_{\text{step}}} = \frac{2 \text{ MHz}}{100 \text{ kHz}} = 20 \quad (42)
\]

\[
N_{\text{max}} = \frac{f_0}{f_{\text{step}}} = \frac{3 \text{ MHz}}{100 \text{ kHz}} = 30 \quad (43)
\]

\[
K_n = \frac{1}{20} \quad \text{to} \quad \frac{1}{30} \quad (44)
\]

A type 2 system is required to produce a phase coherent output relative to the input (see Table I). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2 MHz to 3 MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields $C = 100 \text{ pF}$. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

The transfer function of the VCM is given by

\[
K_o = \frac{K_v}{s} \quad (45)
\]

Where $K_v$ is the sensitivity in radians per second per volt. From the curve in Figure 8, $K_v$ is found by taking the reciprocal of the slope.

\[
K_v = 4 \text{ MHz} - 1.5 \text{ MHz} \quad \frac{2\pi \text{ rad/s/V}}{5 \text{ V} - 3.6 \text{ V}} = 4.2 \times 10^6 \text{ rad/s/V} \quad (46)
\]

Thus

\[
K_o = \frac{11.2 \times 10^6 \text{ rad/s/V}}{s} \quad (47)
\]

The $s$ in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by 5

\[
K_p = \frac{2.3 \text{ V} - 0.9 \text{ V}}{-2(2\pi)} = \frac{2.3 \text{ V} - 0.9 \text{ V}}{-4\pi} = 0.111 \text{ V rad} \quad (48)
\]

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include $K_p$, $K_o$, $K_n$ leaving only $K_f$ as the variable for design. Writing the loop transfer function and relating it to Equation 19

\[
G(s)H(s) = \frac{K_p K_v K_n K_f}{s} = \frac{K(s + a)}{s^2} \quad (49)
\]

Thus $K_f$ must take the form

\[
K_f = \frac{s + a}{s} \quad (50)
\]

in order to provide all the necessary poles and zeroes for
the required $G(s) H(s)$. The circuit shown in Figure 9 yields
the desired results.

$K_f$ is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \text{ for large } A$$  \hspace{1cm} (51)

where $A$ is voltage gain of the amplifier.

$R_1$, $R_2$, and $C$ are then the variables used to establish
the overall loop characteristics.

The MC4044/4344 provides the active circuitry required
to configure the filter $K_f$. An additional low current high
$\beta$ buffering device or FET can be used to boost the input
impedance thus minimizing the leakage current from the
capacitor $C$ between sample updates. As a result longer
sample periods are achievable.

Since the gain of the active filter circuitry in the
MC4044/4344 is not infinite, a gain correction factor $K_c$
must be applied to $K_f$ in order to properly characterize the
function. $K_c$ is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5 \left( \frac{R_2Cs + 1}{R_1Cs} \right)$$  \hspace{1cm} (52)

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 10 and its
Laplace representation in Figure 11.

The loop transfer function is

$$G(s) H(s) = K_p K_{fc} K_o K_n$$  \hspace{1cm} (53)

$$G(s) H(s) = K_p (0.5) \left( \frac{R_2Cs + 1}{R_1Cs} \right) \left( \frac{K_v}{s} - \frac{1}{N} \right)$$  \hspace{1cm} (54)

The characteristic equation takes the form

$$CE = 1 + G(s) H(s) = 0$$

$$s^2 + 0.5 \frac{K_p K_v R_2}{R_1N} - s + 0.5 \frac{K_p K_v}{R_1CN} = 0$$  \hspace{1cm} (55)

Relating Equation 55 to the standard form given by
Equation 34

$$s^2 + 0.5 \frac{K_p K_v R_2}{R_1N} - s + 0.5 \frac{K_p K_v}{R_1CN} = s^2 + 2 \xi \omega_n s + \omega_n^2$$  \hspace{1cm} (56)

Equating like coefficients yields

$$0.5 \frac{K_p K_v}{R_1CN} = \omega_n^2$$  \hspace{1cm} (57)

and

$$0.5 \frac{K_p K_v R_2}{R_1N} = 2 \xi \omega_n$$  \hspace{1cm} (58)

With the use of an active filter whose open loop gain ($A$)
is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p K_v}{R_1CN} = \omega_n^2$$  \hspace{1cm} (59)

$$\frac{K_p K_v R_2}{R_1N} = 2 \xi \omega_n$$  \hspace{1cm} (60)

The percent overshoot and settling time are now used
to determine $\omega_n$. From Figure 6 it is seen that a damping
ratio $\xi = 0.8$ will produce a peak overshoot less than 20% and
will settle to within 5% at $\omega_n t = 4.5$. The required
lock-up time is 1 ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s}$$  \hspace{1cm} (61)

Rewriting Equation 57

$$\frac{R_1C}{\omega_n^2} = \frac{0.5 K_p K_v}{(0.111)(11.2 \times 10^6)}$$  \hspace{1cm} (62)

$$= \frac{(0.5)(0.00102)(11.2 \times 10^6)}{(4500)^2} \hspace{1cm} (30)$$

$$R_1C = 0.00102$$

(Maximum overshoot occurs at $N_{max}$ which is minimum
loop gain)

Let \hspace{1cm} $C = 0.5 \mu F$

Then \hspace{1cm} $R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04 \text{ k}\Omega$

Use \hspace{1cm} $R_1 = 2 \text{ k}\Omega$
FIGURE 10 – Circuit Diagram of Type 2 Phase Locked Loop

FIGURE 11 – Laplace Representation of Diagram in Figure 10
Rt is typically selected greater than 1 kΩ.

Solving for R2 in Equation 58

\[ R_2 = \frac{2\omega_n R_1 N}{K_p K_v (0.5)} = \frac{2\omega_n}{C \omega_n} \] (63)

\[ = \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5 \text{ k})} \]

\[ = 711 \Omega \]

use \( R_2 = 680 \Omega \)

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio \( K_n \), the closed loop poles will vary in position as \( K_n \) varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter \( N = 30 \). The system response for \( N = 20 \) exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

\[ N = 30 \]
\[ \omega_n = 4.61 \text{ k rad/s} \]
\[ f = 0.785 \]
\[ N = 20 \]
\[ \omega_n = 5.64 \text{ k rad/s} \]
\[ f = 0.961 \]

\[ \text{FIGURE 12 - Root Locus Variation} \]

NOTE: The type 2 second order loop was illustrated as a design example because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency a type 2 loop still offers an optimum design:

**EXPERIMENTAL RESULTS**

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve \( N = 30 \) illustrates the frequency response when the programmable counter is stepped from 29 to 30 thus producing a change in the output frequency from 2.9 MHz to 3.0 MHz. An overshoot of 18% is obtained and the output frequency is within 5 kHz of the final value one millisecond after the applied step. The curve \( N = 20 \) illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the output frequency is proportional to the VCM control voltage, the PLL frequency response can observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30 the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrates that the experimental results obtained from the configured system follow the predicted results shown in Figure 13. Linearity is maintained for phase errors less than 2π, i.e. there is no cycle slippage at the phase detector.

\[ \text{FIGURE 13 - Frequency-Time Response} \]

\[ \text{FIGURE 14 - VCM Control Voltage (Frequency) Transient} \]
The parameters listed below apply to the following plot:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Detector Gain Constant</td>
<td>$V_1 = 0.111$ Volts Per Radian</td>
</tr>
<tr>
<td>VCM Gain Constant</td>
<td>$V_2 = 1.12 \times 10^7$ Volts Per Volt</td>
</tr>
<tr>
<td>Filter Input Resistor</td>
<td>$R_1 = 3900$ Ohms $(R_{1_C} = 2 , k)$</td>
</tr>
<tr>
<td>Filter Feedback Resistor</td>
<td>$R_2 = 680$ Ohms</td>
</tr>
<tr>
<td>Filter Capacitor</td>
<td>$C_1 = 0.5$ Microfarads</td>
</tr>
<tr>
<td>Divider Value</td>
<td>$N_1-N_2 = 29 - 38$</td>
</tr>
<tr>
<td>Reference Frequency</td>
<td>$F_1 = 1000000$ CPS</td>
</tr>
<tr>
<td>Output Frequency Change</td>
<td>$F_5 = 10000$ CPS</td>
</tr>
</tbody>
</table>

$P_2 = 0.111$, $V_2 = 1.12 \times 10^7$, $R_3 = 3900$ $(R_{1_C} = 2 \, k)$, $R_4 = 680$

Plot of functions:

(Note: $Y(T)$ is plotted '•', $Z(T)$ is '○', and 'O' is common)

For $T$: Top = 0, Bottom = 0.0015, Increment = 0.00005
For FCTS: Left = 0, Right = 0.12, Increment = 0.002

![Plot of functions](image)

Figure 15 – VCM Control Signal Transient
Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\xi \leq 1.0$. The program prints or plots the control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between the experimental and analytical results.

SUMMARY

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

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TELEVISION VIDEO IF AMPLIFIER USING INTEGRATED CIRCUITS

Prepared by
Applications Engineering

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer-oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330.
TELEVISION VIDEO IF AMPLIFIER USING INTEGRATED CIRCUITS

INTRODUCTION

The very stringent requirements of the television video IF amplifier can now be met using integrated circuits while giving a substantial increase in performance and cost saving over conventional discrete components. Circuit techniques that would not have been technically or economically possible with discrete components, can now be utilized with integrated circuits.

Figure 1 indicates the signal levels and degree of automatic gain control (AGC) required if a television receiver is to function correctly throughout the range of input signal conditions commonly encountered. In some locations, all TV channels may provide high level signals, or conversely, all channels appear as low level signals. However, in most practical situations, each channel has its own amplitude. Some signals are nearly lost in noise, while others approach overload strength. This range of field intensity at the antenna requires AGC compensation in the television receiver over a dynamic range greater than 90 dB. Some of this control can be accomplished in the tuner, since a good solid-state TV tuner has an AGC reduction capability usually greater than 36 dB. The difference of at least 60 dB must be provided by the video IF amplifier.

The detected video output level will depend on the video amplifier and picture tube drive requirements. In the extreme case of a single stage, tube video amplifier, as used in inexpensive monochrome receivers, the level could be as high as 6 V. But in most hybrid and all solid-state receivers a one to two volt composite video and sync signal is sufficient. Figure 2 shows a block diagram using two integrated circuits, which gives the required IF gain, more than adequate AGC gain reduction, and a detected composite video output signal level of up to six volts, if required.
CIRCUIT DESCRIPTION – MC1350

Figure 3 is a schematic diagram of the MC1350 video IF amplifier. Q1, Q2, Q3, and Q6 form a differential cascade amplifier. When Q4 and Q5 are not conducting, the amplifier is at maximum gain. With a positive AGC bias voltage applied to the bases of Q4 and Q5, they will conduct and shunt away the signal current of Q3 and Q6. This will attenuate the gain of the amplifier, although the collector currents of Q1 and Q2 will remain constant preventing a large input impedance change. The output amplifiers, Q7, Q8, Q9, and Q10, are supplied from an active current source that maintains a constant quiescent bias keeping the output admittance nearly constant over the AGC range. The differential output is taken from the collectors of Q8 and Q9, however single-ended output may be taken from either collector, provided the unused collector is connected to the positive supply (V+). Operation in this latter mode reduces the circuit gain. Either differential or single-ended inputs may be applied to Q1 and Q2. For single-ended input, there will be no loss in gain provided the unused input is grounded through a capacitor.

Figure 4 is a graph of the AGC gain reduction characteristics versus the voltage applied to Pin 5, through a 5 kΩ resistor.

In later paragraphs a more complex, keyed or gated AGC system will be discussed.
THE FINAL VIDEO IF AMPLIFIER AND DETECTOR

The final video IF amplifier and video detector must be linear, if the video waveforms are to be undistorted. If the detector or final video IF amplifier limits the video carrier, either the sync pulses or the white region of the video may be clipped.

In present day TV receivers, a germanium diode is often used for the video detector. While the germanium diode functions exceedingly well, it is inherently non-linear. The non-linearity is the result of the forward impedance characteristics of germanium. When the collector current of the final video IF transistor reaches a certain level, $h_{FE}$ may begin to decrease resulting in non-linear amplification. Both of these effects are illustrated in Figure 5. These nonlinearities generate unwanted sum and difference frequencies ("tweets"). The high frequency tweets may radiate into either the receiver antenna input, or into the low level stages of the IF amplifier, causing instability. The low frequency products may mix with the video signal and produce unwanted patterns on the picture tube. Television manufacturers incorporate filters and shields to eliminate these effects, however, a low level detection system not utilizing a germanium diode would eliminate these problems.

The MC1330, low level detector (LLD), is a doubly balanced, full wave, synchronous detector featuring very linear detection and excellent frequency response. The linearity is displayed in Figure 6. Carrier rejection for this type of detector is typically 60 dB. The synchronous detector functions by multiplying the signal to be detected by the same signal which has been amplified and limited. (See Figure 7.) Further information on low level detectors may be obtained in Motorola Application Notes AN-489 and AN-490.
CIRCUIT DESCRIPTION – MC1330

Figure 8 is a simplified circuit diagram of the MC1330. Q7 is a constant current source, Q1 and Q2 form a differential amplifier, while Q3, Q4, Q5, and Q6 are carrier operated switches. When positive half cycles of the amplitude modulated carrier appear at the base of Q1, it begins to conduct. The in-phase, clipped carrier signal will turn on Q3 causing current flow through R1 to increase. No current will flow through Q4, because it is switched off.
When negative half cycles appear at the base of Q1, Q2 will conduct through differential action. The reverse phase carrier pulse will turn on Q4, causing the current through R1 to increase. No current will flow through Q3, since the in-phase carrier pulse is negative at this time. The current flow through R1 increases for either positive or negative half cycles of the carrier, producing a negative voltage change at the collectors of Q3 and Q4.

The reverse action takes place in R2 due to Q5 and Q6. Figure 8(a) is the amplitude modulated carrier appearing at the base of Q1. Q2 would see the same waveform inverted. The two clipped carrier waveforms required as switching pulses are shown in Figures 8(b) and 8(c). The detector is switched at twice carrier frequency, with Q3 conducting on the positive half cycles and Q4 conducting on the negative half cycles. Figure 8(d) is the voltage waveform across R1. Notice that the original carrier no longer exists and that the detected modulation is constructed of pulses of double the carrier frequency.

The stages which follow the basic detector in Figure 9 have limited frequency response, amplifying only lower frequency components. i.e., the modulation, and making the detector self filtering for the high frequency products. Therefore, shielding the detector to prevent spurious radiation of the IF and harmonics of the IF is not necessary. It is essential that the switching waveform contains only the carrier and not sideband information. To prevent spurious switching, an external tuned circuit is connected between the bases of the switching transistors. This is composed of L3 and C10 in Figure 10.

The Q of this tuned circuit directly affects two characteristics of the detector. First, the higher the Q, the more critical and difficult tuning becomes. Secondly, the magnitude of the sum and difference products of two modulating frequencies decreases as Q is increased. This is indicated in the data in Figure 11 along with the test circuit used to obtain the data. It is obvious that some compromise must be achieved. The inter-modulation product between the chroma subcarrier (3.58 MHz) and the sound subcarrier (4.5 MHz) must be kept to a minimum, to avoid the 920 kHz beat pattern, without making the tuning excessively critical. The compromise value of Q is usually between 15 and 25. Within these values of Q, tuning is not critical; in fact, mistuning by 1 MHz gives acceptable pictures, while the 920 kHz beat is 14 dB below the level of the sound subcarrier. If the sound subcarrier trap (41.25 MHz) cuts the subcarrier by 40 dB, the beat frequency will be 54 dB below the video signal level, or 200 mV, when the video drive is 100 V. At the same time, there will be 2 mV of 4.5 MHz information at the detector producing one volt of detected video output which is adequate to drive most sound IF integrated circuits. The conversion gain of the MC1330 is typically 34 dB.

The circuit requires about 33 mA from the 18 V supply. Some regulation of the supply is desirable as gain and the output dc reference level change with the supply voltage. The required regulation depends on the changes in these parameters which can be tolerated.

A PRACTICAL TELEVISION IF AMPLIFIER AND DETECTOR

Figure 10 shows a complete practical circuit for an integrated circuit, video IF amplifier. This circuit employs the two integrated circuits previously discussed. This circuit has a typical voltage gain of 84 dB and a typical AGC range of 80 dB. It gives very small changes in bandpass shape, usually less than 1 dB tilt for 60 dB compression. There are no shielded sections. The detector uses a single tuned circuit (L3 and C10).

Coupling between the two integrated circuits is achieved by a double tuned transformer (L1 and L2). No block filters or traps have been designed for the front end of this amplifier, as different television manufacturers may have their own preferences and rejection requirements. The sound intercarrier information may be taken from the detected video output.

ALIGNMENT PROCEDURE

The following equipment is required for alignment:

1. Signal generator—tuned to video carrier frequency
2. Sweep generator that will sweep IF band and supply markers
3. VHF attenuator
4. 5 MHz bandwidth, dual trace oscilloscope
5. Power supply to deliver 100 mA at 18 V
6. Power supply adjustable 0-12 V (AGC)
7. Resistive mixing pad

If the amplifier is swept in the conventional manner, the resultant display will be misleading due to the absence of a fixed frequency carrier. The detector tuned circuit will follow the sweep generator and indicate a high amplitude response at the resonant frequency of C10 and L3 as shown in Figure 12. A block diagram of the alignment operation is given in Figure 15. The signal generator tuned to the video carrier frequency of 45.75 MHz (no modulation) is connected to the input. The scope probe is attached to the output, Pin 4 of the MC1330, and L3 is tuned to give a maximum dc output. The only method of tuning the open core inductor L3 is stretching or compressing the windings. After L3 has been correctly tuned by distorting the windings, it should not be retuned in later stages of alignment.

TUNING L1 AND L2

In order to tune L1 and L2 connect the scope probe to Pin 4 of MC1330 and sweep generator input through an attenuator and a mixing pad. Apply 10 to 20 dB of AGC compression by adjusting the AGC power supply. Withdraw tuning cores of L1 and L2 as far as possible before beginning adjustment. Adjust L1 and L2 roughly to obtain response trace similar to Figure 12. Adjust the signal generator output level to give approximately 3 dB greater output than the sweep generator level and apply signal generator output to the mixing pad. This will give the detector the fixed carrier frequency it requires to operate. The AGC
FIGURE 10 – Typical MC1350 Video IF Amplifier and MC1330 Low-Level Video Detector Circuit

FIGURE 11 – Test Circuit for Intermodulation Products

<table>
<thead>
<tr>
<th>Component</th>
<th>36 MHz</th>
<th>45 MHz</th>
<th>58 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>C6</td>
<td>24 pF</td>
<td>15 pF</td>
<td>10 pF</td>
</tr>
<tr>
<td>C8</td>
<td>18 pF</td>
<td>12 pF</td>
<td>10 pF</td>
</tr>
<tr>
<td>C10</td>
<td>33 pF</td>
<td>33 pF</td>
<td>18 pF</td>
</tr>
<tr>
<td>L3</td>
<td>12 Turns</td>
<td>10 Turns</td>
<td>10 Turns</td>
</tr>
</tbody>
</table>

Table of Component Values

<table>
<thead>
<tr>
<th>Component</th>
<th>36 MHz</th>
<th>45 MHz</th>
<th>58 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>0.001 µF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>0.002 µF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>0.002 µF</td>
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<td>C4</td>
<td>0.002 µF</td>
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<tr>
<td>C5</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>C6</td>
<td>See Table</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C7</td>
<td>0.1 µF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C8</td>
<td>See Table</td>
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</tr>
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<td>C9</td>
<td>68 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C10</td>
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<td></td>
</tr>
<tr>
<td>R1</td>
<td>50 k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>5 k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>470 k</td>
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<td></td>
</tr>
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<td>R4</td>
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<td>R5</td>
<td>22 k</td>
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</tr>
<tr>
<td>R6</td>
<td>3.3 k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td>3.9 k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R8</td>
<td>3.9 k</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>16 Turns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2</td>
<td>6 Turns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L3</td>
<td>16 Turns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

All windings #30 AWG tinned nylon acetate wire tuned with high permeability slugs. Coil Craft #786 differential transformer.

All windings #26 AWG tinned nylon acetate wire tuned by distorting winding.

All Caps Marked µF Ceramic HiK
All Caps Marked pF Silver Mica 5%
may also be adjusted if required. The display on the scope should now be similar to Figure 13, with the zero beat between the sweep generator and the signal generator appearing within the modulation envelope. Adjust the second trace of the scope to display the marker frequencies, and adjust L1 and L2 to give bandpass shape as required. (See Figure 14.) L1 and L2 should be tuned to the first peak as the cores are turned into the windings to avoid over coupling.

A full-sized (1:1) printed circuit board layout is given in Figure 16. The components are identified as in the schematic diagram.
AUTOMATIC GAIN CONTROL – MC1352

The IF amplifier previously described will require AGC from an external source. However, there is another integrated circuit for IF amplifier applications which replaces the MC1350 and has built-in keyed AGC. The MC1352 has a positive-going AGC output. The schematic is given in Figure 17. A gating pulse, a reference level, and the composite video signal to be controlled are required for correct operation of this AGC system. If positive-going video (with negative sync) is available, apply it to Pin 6 and apply the reference voltage to Pin 10. However, if negative-going video (with positive sync) is used, apply it to Pin 10 and the reference voltage to Pin 6. The magnitude of the reference voltage determines the AGC threshold.

CIRCUIT DESCRIPTION – MC1352

A negative keying pulse of eight volts amplitude and timed to each sync pulse is taken from the horizontal time base. This pulse is applied to Pin 5. Q2, normally in
saturation, is turned off by this pulse, permitting the anode of diode D1 to rise toward the positive supply voltage. The level to which this point rises is determined by the difference between the reference and video input voltages applied to Pins 6 and 10. An external capacitor C2 is charged through D1. When Q2 returns to saturation, D1 will be back-biased preventing current flow from C2. The voltage on C2 is amplified by Q4 and Q5 and filtered by R1 and C1. The filtered voltage is supplied to the bases of Q12 and Q14 controlling the IF gain as described in the previous section on the MC1350. Q6 and Q7 form a differential amplifier. The amplified voltage from the capacitor is also applied to the base of Q6, while a delay voltage is applied to the base of Q7 through Pin 13. The delay voltage is used to determine the AGC threshold of the tuner. The output of the differential amplifier is taken from the collector of Q6 giving positive AGC action. Q8, Q9, and Q10 amplify the difference voltage (delayed AGC voltage) permitting gain control in the tuner. The full RF amplifier AGC compression is obtained with a much smaller change in video input voltage than required for full AGC compression in the IF amplifier. Figure 18 displays the AGC characteristics of the MC1352.
ADJUSTMENT OF RF AMPLIFIER BIAS

Figure 20 is a schematic diagram of a video IF amplifier for use at 45 MHz using an MC1330 low level detector and a MC1352. If the RF amplifier transistor in the tuner is an NPN device, a MC1352 is used. To set the maximum gain pre-bias on a forward AGC NPN transistor, a fixed resistor $R_{pb}$ must be selected. This forms a voltage divider with the 6.8 kΩ resistor ($R_3$). In the maximum gain condition, the voltage on Pin 12 would be zero volts without the voltage divider. To pre-bias a forward AGC PNP transistor, $R_{pb}$ is set at 6.8 kΩ and $R_3$ is selected for proper pre-bias. To obtain maximum gain without AGC control, for alignment purposes connect a 22 kΩ resistor between Pins 9 and 11 of the MC1352. Connecting a 200 kΩ variable resistor between Pin 14 and ground and also the 22 kΩ resistor between Pins 9 and 11 provides a method of obtaining any particular gain desired. The alignment procedure for Figure 20 is the same as described earlier for the MC1350. Additional information on the MC1352 can be obtained from the data sheet.
All windings #30 AWG tinned nylon acetate wire tuned with high permeability slugs, Coil Craft #4786 differential transformer.

TABLE I

<table>
<thead>
<tr>
<th>Video Polarity</th>
<th>Pin 6 Voltage</th>
<th>Pin 10 Voltage</th>
<th>R4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negative-Going Sync.</td>
<td>5.5 V</td>
<td>Adj. 1.0-4.0 Vdc</td>
<td>0</td>
</tr>
<tr>
<td>Positive-Going Sync.</td>
<td>4.5 V</td>
<td>Nom 4.5 V</td>
<td>3.9 kΩ</td>
</tr>
<tr>
<td>Positive-Going Sync.</td>
<td>4.5 V</td>
<td>Adj. 1.0-5.0 Vdc</td>
<td>0</td>
</tr>
</tbody>
</table>

TABLE II

<table>
<thead>
<tr>
<th>Component</th>
<th>36 MHz</th>
<th>45 MHz</th>
<th>58 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>C7</td>
<td>24 pF</td>
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<td>10 pF</td>
</tr>
<tr>
<td>C9</td>
<td>18 pF</td>
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<td>10 pF</td>
</tr>
<tr>
<td>C11</td>
<td>33 pF</td>
<td>18 pF</td>
<td></td>
</tr>
<tr>
<td>L3</td>
<td>12 Turns</td>
<td>10 Turns</td>
<td></td>
</tr>
</tbody>
</table>

FIGURE 19 — Television IF Amplifier and Detector Using an MC1330 and an MC1352
This application note describes some of the characteristics of high speed digital signal lines and gives wiring rules for MECL 10,000 emitter coupled logic. The note includes discussions of printed circuit board interconnects, board-to-board interconnects, and wirewrapping techniques.
INTRODUCTION

As the digital integrated circuit market has become more mature, the need for very high speed logic elements has grown. Future machine designs demand a logic family with high clock rate capability, short propagation delays, and a minimum of layout constraints. From this need, the MECL 10,000 family of emitter-coupled logic has evolved – designed to be the most usable very high speed logic family available.

The 2.0 nanosecond gate propagation delay of MECL 10,000 gives the family a speed range between the older 4.0 nanosecond MECL II and 1.0 nanosecond MECL III families. Additional characteristics, such as low power dissipation (25 mW per gate function), and slow rise and fall times have eased the difficulties encountered in trying to balance system speed versus ease of design.

A MECL 10,000 system has the capability for clock rates in excess of 100 MHz. To permit such high speed operation, gate propagation delays must necessarily be short. However, to simplify wiring techniques and to minimize the use of transmission lines, rise and fall times have been kept to slower values.

MECL III still remains the industry standard as the highest speed logic family available. However the 1 nanosecond rise time of MECL III demands a transmission line environment. On the other hand, MECL 10,000 has been designed to approach the higher speed rates of MECL III, but with simpler wiring requirements.

The operational behavior of a MECL III gate with a rise time of 1 nanosecond (10%/90%) is shown in figure 1 for comparison. Figure 1a shows the difference in rise times when either gate is driving only a pulldown resistor. Figure 1b shows the same outputs driving an 8 inch signal line to a gate input. The MECL III gate shows severe ringing. This necessitates the use of a transmission line. The effect of the slower rise time of the MECL 10,000 gate is obvious in that ringing is not as severe. Herein, lies an advantage for the system designer using MECL 10,000 that is, he may realize a very high speed system using only a minimum of transmission lines.

When driving long lines or large fanouts at maximum frequency, transmission lines are needed. MECL 10,000 has the capability to drive such lines. Also, the family is specified to be completely compatible with MECL III in the 16-pin dual-in-line packages. As a result, MECL 10,000 can be used to obtain maximum versatility with low power and ease of layout design.

The following discussion is intended to give the system designer insight into these problem areas: The use of non-transmission line interconnections; the characteristics of transmission lines which affect MECL interconnections; and the techniques used for transmission lines. Other considerations to be made for system interconnections are also discussed, such as noise margins, clock driving, wire wrapping, and party line techniques.

SIGNAL LINE CONSIDERATIONS

The purpose of an interconnection line in any digital system is to transmit information from one point of the system to another. When information on a signal line changes, a finite amount of time is necessary for the information to travel from the sending end to the receiving end of the line. As the circuit speed becomes faster and clock rates increase, the dynamic behavior of the interconnection line becomes increasingly important. The rise and fall times of the logic elements, loading effects, delay times of the signal paths, and the various other transient characteristics, all affect reliable operation of the system. The effects of these factors and the advantages of the dynamic characteristics of MECL 10,000 are perhaps best shown by briefly investigating the transmission line qualities of a signal path.

In figure 2a is shown a simple interconnection circuit. A MECL 10,000 gate is shown driving a line of length \( L \) to another gate with a pulldown resistor, \( R_L \). If the loading effect of the receiving gate is disregarded (input impedance is very large with respect to \( R_L \)), the same line could be modeled as shown in figure 2b.

The driving gate is modeled as a voltage source with output impedance, \( R_O \). The signal line will exhibit an impedance to a transient signal which is called its characteristic impedance, \( Z_0 \). If the line is not a regular transmission line, \( Z_0 \) will vary somewhat. However, for this example let us assume that \( Z_0 \) is constant.

When the output of the driving gate changes state, the voltage at point A is a function of the internal voltage swing, \( V_{INT} \), output impedance, and line impedance:

\[
V_{A(t)} = V_{INT}(t) \left( \frac{Z_0}{R_O + Z_0} \right)
\]

For MECL 10,000, \( R_O \) is small with respect to the line impedance, so the output swing is nearly the same as the input transition, typically 800 mV. The signal will prop-
FIGURE 1 – Comparison of MECL III and MECL 10,000 Waveforms

(a) Gate Driving 510 ohm Pulldown Resistor

(b) Gate Driving 510 ohm Pulldown Resistor and 8 Inch Line with Gate Load

FIGURE 2 – MECL 10,000 Interconnection Circuit
agate down the line and be seen at point B time $T_D$ later. The signal, when reaching the end of the line (point B), may be reflected and returned toward the sending end of the line. The reflected voltage is:

$$V_A' = \rho_L V_A,$$

where $\rho_L$ is the reflection coefficient,

$$\rho_L = \frac{R_L - Z_0}{R_L + Z_0}.$$

In the special case where $R_L = Z_0$, then $\rho_L = 0$ and the reflected voltage is zero. In this situation the load resistor exactly matches the characteristic impedance of the line, so no reflection occurs.

When reflection does occur, it returns to point A at time $2T_D$, where $T_D$ is the one-way line propagation delay. The sending end will again reflect this voltage with a reflection coefficient, $\rho_S$, given by:

$$\rho_S = \frac{R_o - Z_0}{R_o + Z_0}.$$

The reflected signal will continue to bounce back and forth between the ends of the signal line, gradually diminished in amplitude by reflection coefficients and the resistance in the line.

Now consider a second line in which the load resistor has been moved to the sending end of the line (figure 3a). This model is altered from the first only in that the load resistor is seen at the driver output. When the output of the driving gate changes state, the output swing, $V_{A'}$, will be typically 800 mV. The signal reaching point B will be reflected (as discussed). The coefficient, $\rho_L$, becomes worst case ($\approx 1$) because the input impedance of the receiving gate is high. In such a case the reflection will be large. As the reflection returns to point A at time $2T_D$, the reflection coefficient, $\rho_S$, comes into play. Its value will be very close to the previous case:

$$\rho_S = \frac{R_o - Z_0}{R_o + Z_0} \approx \frac{R_o - Z_0}{R_o + Z_0}.$$

since $R_o$ is small compared to $R_L$.

The reflections, as before, continue to bounce back and forth on the line getting successively smaller in amplitude. The result is that ringing appears on the signal line (figure 3c).

Rise time effects may be understood by considering the delay time of the line. If the line length $\ell$ is sufficiently short, the first reflections are seen at the sending end of the line while the driver is still changing state. The reflections are hidden by the rising edge of the pulse, and ringing is reduced. Therefore, the slow rise time of MECL 10,000 permits longer line lengths to be used before trouble with ringing is encountered.

This second signal line example is called an open line or an unterminated line. To limit undershoot to about 12 percent of the logic swing, the maximum open line length permitted would be:

$$L_{\text{max}} = \frac{t_f}{2 \tau_{\text{pd}}}$$

where: $t_f$ = Rise time of driving gate (ns) ($20\% - 80\%$)

$\tau_{\text{pd}}$ = Propagation delay per unit line length (ns/m).

The above expression may also be used to show the effect of loading on an interconnection. $\tau_{\text{pd}}$ is dependent on the rate of signal propagation on the line; the rate is controlled by the type of line and the loading on the line. MECL inputs are high impedance and capacitive in net reactance ($3$ to $5$ pF per input). Increased loading slows the rate of propagation of the line and decreases allowable open line length. That is, as fan-out increases, the maximum open line length decreases for acceptable undershoot.

To understand how ringing and undershoot affect system operation, it is helpful to define guaranteed noise mar-
gins. Noise margin is defined as the difference between a worst case input logic level (\(V_{OH\text{min}}\) or \(V_{OL\text{max}}\)) and the worst case threshold (\(V_{IH\text{min}}\) or \(V_{IL\text{max}}\)) for the corresponding logic level. Guaranteed noise margins (N.M.) for MECL 10,000 at 25°C are:

\[
\text{Logic 1 N.M.} = V_{OH\text{min}} - V_{IH\text{min}} \\
= -0.980 - (-1.105) = 125 \text{ mV};
\]
\[
\text{Logic 0 N.M.} = V_{IL\text{max}} - V_{OL\text{max}} \\
= -1.475 - (-1.630) = 155 \text{ mV}.
\]

However, using typical logic levels of –0.900 volts and –1.700 volts, the nominal voltage margins are greater than 200 mV for both logic levels.

For system design, worst case conditions should be considered. If so, a 125 mV noise margin becomes the design limit. This voltage margin protects against signal undershoot, power supply variations, and system noise. Good circuit interconnections should limit maximum undershoot to less than 100 to 110 mV to provide a design safety margin.

Other factors – such as line impedance and placement of loads on the line – also affect ringing of signals. A long and elaborate discussion would be necessary to describe all of the varying effects, and the description here is only intended to give a brief idea of the many factors involved. When line lengths and fanout go beyond limits (which will be defined), techniques such as twisted pair lines and terminated lines may be used.

PRINTED CIRCUIT BOARD INTERCONNECTS

Layout rules needed for designing with MECL 10,000 depend mainly on the design goals of the system user. MECL 10,000 may be used in layouts ranging from single layer printed circuit (PC) board with wired interconnects, to the most elaborate multilayer board with a complete transmission line environment. Optimization of system layout will include considerations of the system size, desired performance, and cost.

Use of a ground plane is a suggested procedure whenever possible. A ground plane is beneficial for maintaining a noise free voltage plane for the VCC supply, and for maintaining constant characteristic impedance whenever transmission lines become necessary. A ground plane may be established by using single sided board with wired interconnects, or by using double or multilayer PC board.

WITHOUT GROUND PLANE

In small systems where the number of interconnects and the package density are high, it is difficult to reserve a large ground plane area without the use of multilayer board, a costly approach. However, MECL 10,000 may still be used with good system performance if certain guidelines are followed:

1. VCC should be bussed to the VCC pins of each package. Bus lines should be as wide as possible with a width of 0.1 inch minimum per row of packages. If an edge connector is used, VCC should be pinned out to several connector pins.

2. VEE should also be bussed, if possible, to pin 8 of each package (pin 12 of the 24 pin package). When VEE is brought onto the board via an edge connector, the VEE line should be in close proximity to a VCC pin for easy bypassing.

3. Each device should be bypassed between the VCC and the VEE pins with a low inductance 0.01 µF capacitor.

4. Logic interconnecting lines should be kept to minimum length. A maximum line length of 6 inches is suggested; ringing will begin to get too severe with longer line lengths. For line lengths greater than 6 inches, signal lines with series damping resistors are necessary (similar to those shown in figure 13).

5. For high fanout (8 or greater) and high speed clock distribution, twisted pair lines or coaxial cable should be used. Both of these techniques are described in detail later.

Figure 4 shows a double-sided PC board in which the above rules are illustrated. Several MECL 10,000 devices are
used with MTTL in a high speed counter, in which the MECL and MTTL are operated by a common voltage supply. Notice that VEE and VCC are both bussed to the package and that bus lines are as wide as conveniently possible. Two 0.1 \( \mu F \) capacitors are used for low frequency bypassing on the board. Each MECL 10.000 device is bypassed with a 0.01 \( \mu F \) capacitor, and additional bypassing is scattered through the MTTL circuitry. Note that signal lines are short and no transmission lines are used.

WITH GROUND PLANE

A ground plane allows best performance for a MECL 10.000 system. The ground plane serves two purposes. First, it provides a constant characteristic impedance \( Z_0 \) to signal interconnections; secondly, it provides a low inductance path for ground currents on the VCC supply. As with systems which have no ground plane, certain design guidelines are recommended as follows:

1. The ground plane (VCC) need not cover 100\% of the board surface. Approximately 30 to 40\% of the ground area may be removed for signal interconnections, as illustrated in figure 5. When using edge connectors, the ground plane should be pinned out to about every seventh connector pin.
2. The VEE supply should be bussed if possible, to pin 8 of each package. Bus line width at any point should be a minimum of 0.1 inch. Where possible, the VEE supply should be extended to a plane under the signal lines etched on the ground plane side of a two-sided circuit board. If VEE is a plane under these lines, they will exhibit a constant characteristic impedance. This technique is also shown in figure 5.
3. Bypassing need not be as extensive as on a board without a ground plane. Provide a low inductance 0.01 \( \mu F \) capacitor every two to six packages, depending upon how extensive the ground plane is. As a rule if the ground plane covers less than 50\% of the board area, then bypass every two packages. On two-sided systems or multilayer systems where 100\% ground plane is present, only one capacitor for every four to six packages is needed.
4. In practice, the majority of board interconnects are shorter than six inches, with fanouts four or less. As discussed, the rise and fall times of MECL 10.000 allow these lines to be treated as unterminated transmission lines requiring only a pull-down resistor. Normally, a 510-ohm resistor to VEE is used. (Detailed limits for interconnections are provided as a function of line impedance and fanout in the following section).
5. For high fanout and high speed clock distribution, terminated transmission lines or twisted pair lines should be used. These techniques are discussed in the following sections.

TRANSMISSION LINE GEOMETRIES

With a ground plane present, three types of transmission line geometries are feasible: wire over ground; microstrip line; and strip line. The following sections summarize the characteristics of each type of line.

(1) Wire over ground The cross section of a wire over a ground is shown in figure 6a. The characteristic impedance of the wire is:

\[
Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{4h}{d} \right)
\]

where \( \varepsilon_r \) is the effective dielectric constant surrounding the wire. The wire over ground plane is useful for breadboard layouts (as with single-sided board) and for backplane wiring. The characteristic impedance of a wire over ground plane will be about 120 ohms with variance depending on the wire size, type of insulation, and distance from the ground plane.

(2) Microstrip lines A microstrip line (figure 6b) is a strip conductor separated from a ground plane by a dielectric medium. Two-sided and most multilayer boards use this type of transmission line. If the thickness, width, and height of the line above the ground plane are controlled, the line will exhibit a characteristic impedance of:

\[
Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left( \frac{5.98h}{0.8w + t} \right)
\]

(3) Strip line

FIGURE 6 – Transmission Line Geometries
Here $\varepsilon_r$ is the dielectric constant of the board. For standard G-10 fiberglass epoxy boards the dielectric constant is about 5.0.

The signal line is obtained by etching unwanted copper from the board using photo resist techniques. A characteristic impedance can easily be controlled to within 10 percent.

As mentioned above, board thickness and dielectric constant affect line impedance. Figure 7 gives a table of values for characteristic impedance versus line width for 0.031" and 0.062" G-10 board with one ounce copper (widths for two ounce copper are nominally 1 to 2 mils narrower).

The propagation delay of microstrip line may be calculated by:

$$t_d = 1.017 \sqrt{0.475 \varepsilon_r + 0.67} \text{ ns/ft}.$$  

Note that the propagation delay of the line depends only on the dielectric constant and is not a function of line width or spacing. For G-10 fiberglass epoxy boards ($\varepsilon_r = 5.0$) the propagation delay of the microstrip line is calculated to be 1.77 ns/ft.

**FIGURE 7 – Microstrip Characteristic Impedance versus Line Width for One Ounce G-10 Fiberglass Epoxy Board**

<table>
<thead>
<tr>
<th>$Z_0$ (OHMS)</th>
<th>LINE WIDTH (MILS)</th>
<th>0.062'' BOARD</th>
<th>0.031'' BOARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>103</td>
<td>47</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>89</td>
<td>41</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>77</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>66</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>57</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>49</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>42</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>36</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>90</td>
<td>31</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>95</td>
<td>27</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>23</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

---

(3) Strip Line - A strip line (figure 6c) is a copper ribbon centered in a dielectric medium between two conducting planes. This type of line is used in multilayer boards and is not seen in most systems. Multilayer boards are justified when operating MECL 10,000 at top circuit speed, and when high density packaging is a system requirement. Since most designers need not concern themselves with strip lines, little is presented here about them. A detailed discussion of strip lines is presented in the “MECL System Design Handbook,” reference 1.

**UNTERMINATED LINE LIMITS**

As previously mentioned, a MECL signal line may be considered as an unterminated transmission line. Rise time, characteristic impedance of the line, and loading affect the maximum interconnection length for unterminated lines. Figure 8 shows a tabulation of suggested maximum open line lengths for various fanouts and line impedances.

The tabulated values were calculated for limiting overshoot to 35% of the logic swing, or undershoot to 12% (whichever was the limiting factor under specified conditions). Severe overshoot can slow down clock rates, and severe undershoot can result in reduced noise immunity. The transmission line model of figure 3 was used in calculations.

As an example of how the table of line limits may be used, consider a system layout using 0.062" board (G-10 fiberglass epoxy). Assume that signal interconnection widths may be from 25 to 40 mils wide. If a ground plane is used on one side of the system PC board, all system interconnects would show a corresponding characteristic impedance. The wide line (40 mils) is preferable since $Z_0$ would be 82 ohms which is lower than that for a 25 mil line ($Z_0 \approx 97$ ohms) and the lower impedance allows a longer maximum length line. The lower impedance line with a fanout of 4 would then have a suggested maximum length of about 4.2 inches. On normal system-sized PC boards (5"x7"), the majority of signal line interconnections will be less than 4 inches in length if the system layout is well planned.

**FIGURE 8 – Maximum Unterminated Line Length for MECL 10,000 to Maintain Less Than 12% Undershoot**

<table>
<thead>
<tr>
<th>$Z_0$ (OHMS)</th>
<th>FANOUT 1 (29 pF)</th>
<th>FANOUT 2 (58 pF)</th>
<th>FANOUT 4 (116 pF)</th>
<th>FANOUT 8 (232 pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\xi$ MAX (IN)</td>
<td>$\xi$ MAX (IN)</td>
<td>$\xi$ MAX (IN)</td>
<td>$\xi$ MAX (IN)</td>
<td>$\xi$ MAX (IN)</td>
</tr>
<tr>
<td>MICROSTRIP (Propagation Delay 0.148 ns/in)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>83</td>
<td>75</td>
<td>67</td>
<td>57</td>
</tr>
<tr>
<td>68</td>
<td>70</td>
<td>62</td>
<td>50</td>
<td>40</td>
</tr>
<tr>
<td>75</td>
<td>69</td>
<td>59</td>
<td>46</td>
<td>36</td>
</tr>
<tr>
<td>82</td>
<td>66</td>
<td>57</td>
<td>42</td>
<td>33</td>
</tr>
<tr>
<td>90</td>
<td>65</td>
<td>54</td>
<td>39</td>
<td>30</td>
</tr>
<tr>
<td>100</td>
<td>63</td>
<td>51</td>
<td>36</td>
<td>26</td>
</tr>
<tr>
<td>BACKPLANE (Propagation Delay 0.140 ns/in)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>66</td>
<td>54</td>
<td>38</td>
<td>28</td>
</tr>
<tr>
<td>140</td>
<td>59</td>
<td>43</td>
<td>28</td>
<td>19</td>
</tr>
<tr>
<td>180</td>
<td>52</td>
<td>36</td>
<td>21</td>
<td>13</td>
</tr>
</tbody>
</table>

86
An interconnection with the pulldown resistor at the sending end of the line is the worst case situation for an unterminated line. If unterminated interconnection lengths are extended beyond the suggested limits, overshoot and undershoot are increased. The lengths given are calculated so that undershoot never exceeds the guaranteed noise margins, although typically noise margins are much greater than specified.

(a) 510-ohm Resistor at Sending End

(b) 510-ohm Resistor at Receiving End

(c) 330-ohm Resistor at Receiving End

FIGURE 9 – Gate Driving 8-Inch 50-ohm Line with Fanout of 4
Overshoot and undershoot may also be reduced by locating the pulldown resistor at the receiving end of the line. If the pulldown resistor is moved to the receiving end, the reflection coefficient ($\rho_L$) is reduced. This reduces ringing.

Figure 9 shows the signal at the receiving end of an 8-inch 50-ohm line with a fanout of 4. In figure 9a, a 510-ohm pulldown is at the sending end of the line. Figure 9b has a 510-ohm pulldown at the receiving end, while figure 9c has a 330-ohm pulldown at the receiving end. The overshoot and undershoot are successively reduced in the latter two cases.

For worst case, the reflection coefficient is approximately equal to one ($\rho_L \approx 1$). For the best case shown, using a 330-ohm pulldown, $\rho_L = (330 - 50)/(330 + 50) = 0.74$, which represents an improvement of about 25%. In comparing the waveforms, notice that overshoot is reduced by roughly the same percentage (9c versus 9a).

The tabulated values of figure 8 are not necessarily absolute limits for unterminated lines. Longer unterminated lines may be used if the pulldown resistor is moved to the receiving end of the line, or if increased overshoot and undershoot are acceptable.

TRANSMISSION LINE TERMINATION TECHNIQUES

Proper transmission line termination prevents reflections on the line, so ringing does not occur. As a result, interconnection lengths are only limited by attenuation, bandwidth, etc. MECL transmission line interconnections utilize several techniques:

1. Parallel Termination: A transmission line will have a reflection coefficient ($\rho_L$) of zero when driving a load impedance equal to its characteristic impedance. MECL 10,000 can source current for driving a 50-ohm characteristic impedance line with the line terminated by 50 ohms to ±2 volts. The termination voltage ($V_{TT} = ±2$ volts) is necessary since 50 ohms loaded to $V_{EE}$ would use excessive current. Figure 10 illustrates parallel termination.

Gate inputs may be distributed along the transmission line (10b), and do not have to be lumped at the end of the line (10a). The gate inputs appear as high impedance stubs to the transmission line and should be as short as possible. While inputs may appear anywhere along the line, the terminating resistor should be at the end of the line. As fanout with this configuration increases, the edge of the waveform slows down, since the signal drives an increasing amount of capacitance. The waveform is undistorted along the full length of the line.

For large systems where total power is a consideration, all lines should be parallel terminated to a ±2 volt supply. This is the most power-efficient manner for terminating MECL circuits. The drawback is of course, the requirement for an additional power supply.

An alternate approach is to use two resistors as shown in figure 11. The Thevenin equivalent of the resistor network is a resistor equal to the characteristic impedance of the line, terminated to ±2Vdc. $R_1$ and $R_2$ may be calculated as:

$$ R_1 = \frac{Z_0}{2} $$
$$ R_2 = \frac{Z_0}{2} $$

where $Z_0$ is the characteristic impedance of the line. The Thevenin equivalent resistors are:

<table>
<thead>
<tr>
<th>$Z_0$ (OHMS)</th>
<th>$R_1$ (OHMS)</th>
<th>$R_2$ (OHMS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>81</td>
<td>130</td>
</tr>
<tr>
<td>70</td>
<td>113</td>
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<tr>
<td>50</td>
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</tr>
<tr>
<td>100</td>
<td>162</td>
<td>260</td>
</tr>
<tr>
<td>120</td>
<td>194</td>
<td>312</td>
</tr>
<tr>
<td>150</td>
<td>243</td>
<td>390</td>
</tr>
</tbody>
</table>

FIGURE 10 - Parallel Termination

FIGURE 11 - Parallel Termination Using a Thevenin Equivalent Resistor Network
lated as follows:

\[ R_2 = 2.6 \, Z_0; \]
\[ R_1 = \frac{R_2}{1.6}. \]

(2) Series damping and series termination: A series terminated line eliminates reflections at the sending end of the line. Series termination is accomplished by inserting a resistor in series with the output of the gate as shown in figure 12. The resistor value plus the circuit output impedance is made equal to the impedance of the transmission line.

\[ \Delta V_B = \Delta V_{\text{INT}} \cdot \frac{Z_0}{R_S + R_0 + Z_0} \]

where \( R_0 \) is the output impedance of the gate.

Since \( R_S + R_0 \) is made equal to \( Z_0 \), the voltage change at \( B \) is \( 1/2 \) the voltage, \( \Delta V_{\text{INT}} \). It takes the propagation delay time of the transmission line, \( T_D \), for the waveform to reach point \( C \), where the voltage doubles due to the unity reflection coefficient at the end of the line. The reflected voltage, which is equal to the sending voltage, arrives back at point \( B \) at time \( 2 \, T_D \). No more reflections occur if \( R_S + R_0 \) is equal to \( Z_0 \). Similar waveforms occur when the driving gate switches to the high state.

An advantage of using series terminated lines is that only one power supply is required. The Thevenin equivalent parallel termination technique uses only one supply, but requires more overall power. A disadvantage of series termination is that distributed loading along the line cannot be used because of the half-voltage waveform traveling down this line (see figure 12, waveform B). A number of lumped loads may be placed at the end of the terminated line as far as reflection at the receiving end is concerned, since a full initial signal transition is observed at this point and all subsequent reflections will be absorbed at the source.

The disadvantage of using only lumped loading at the end of a series terminated line can be eliminated at the expense of more lines (figure 13). As shown, there are \( n \) transmission lines for parallel fanout. The value of \( R_S \) should be the same as discussed previously for the emitter pulldown resistor, in which case \( n \) was equal to one.

The value of \( R_E \), will be determined by the number of lines in the following way. \( R_E \) must be small enough to supply each transmission line with the proper voltage level. If \( R_E \) is too large, the output transistor will turn off when switching from the high to the low voltage state. The maximum value of \( R_E \) is given by:

\[ R_{E\text{(max)}} = \frac{10 \, Z_0 - R_S}{n}. \]
Figure 14a shows the gate output fall time (voltage A) and the fall time at the end of the line (voltage C) when \( N = 1 \), \( Z_0 = 50 \) ohms, \( R_E = 1 \) k ohms, \( R_S = 43 \) ohms, and fanout = 3. The "steps" in the fall time waveform are due to the output device turning off because \( R_E \) is too large. Figure 14b shows the fall time when \( R_E = 290 \) ohms (\( R_E < R_E(\text{max}) \)).

The fanout at the end of a series terminated line is limited by the value of the series resistor, \( R_S \). In the high state a voltage drop occurs across the series resistor:

\[
V_S = (\text{fanout}) \times (\text{input current}) \times R_S
\]

The input current to a MECL 10,000 gate is typically about 160 \( \mu \)A. If the fanout were 4 and \( R_S \) were 43 ohms for a 50 ohm line, \( V_S \) would equal about 28 mV. Noise margin would typically be cut by that amount. As fanout or the value of \( R_S \) increases, \( V_S \) increases and results in lower noise margins.

Series damping may also be used to reduce overshoot and ringing. Series damping is similar to series termination in that a small series resistor is used to reduce ringing rather than to completely terminate ringing. The resistor is smaller than the characteristic impedance of the line and it may be used to increase line length for the worst case open line (that is, \( R_S = 0 \)) as shown in figure 8.

Series damping may also be used for greatly extended line lengths while remaining within calculated limits of overshoot and undershoot. Figure 15 gives minimum values of \( R_S \) needed for various line impedances to limit overshoot to 35\% of signal swing, or undershoot to 12\%. Using these values of minimum \( R_S \), very long lines may be used.

<table>
<thead>
<tr>
<th>( Z_0 ) (OHMS)</th>
<th>MIN ( R_S ) (OHMS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>9</td>
</tr>
<tr>
<td>68</td>
<td>18</td>
</tr>
<tr>
<td>75</td>
<td>21</td>
</tr>
<tr>
<td>82</td>
<td>25</td>
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<tr>
<td>90</td>
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<td>100</td>
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<tr>
<td>120</td>
<td>43</td>
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<tr>
<td>140</td>
<td>53</td>
</tr>
<tr>
<td>160</td>
<td>63</td>
</tr>
</tbody>
</table>

Figure 15 — Minimum Values of \( R_S \) for Any Length Line, for Less Than 35\% Overshoot or 12\% Undershoot

Figure 16 — Rise and Fall Times (10 to 90\%) versus Fanout

(b) \( R_E < R_E(\text{max}) \)
OTHER CONSIDERATIONS

Additional factors other than line length and transmission line terminations must be considered in system design. Some of these are discussed here:

(1) Fanout – The dc fanout capability of MECL 10,000 is very high since its high impedance inputs require little current (typically 160 µA). System speed requirements will ordinarily be the limiting factor for ac fanout. Capacitance increases with fanout and can cause rise and fall times to slow down.

Figure 16 shows the rise and fall times of an MC 10,000 gate as a function of fanout, both for 50 Ω and 510 Ω terminations. As fanout increases, load capacitance (both device and interconnection capacitance) increases, resulting in longer rise and fall times.

Larger fanout will normally result in longer interconnecting lines with their longer line delays, so ringing can become excessive. Under these conditions, use of properly terminated lines will result in best performance. A low impedance (50 Ω) parallel terminated line has a shorter propagation delay than a series damped or series terminated line with equivalent fanout. However, multiple series terminated lines driven from a single gate output (figure 13), with lower fanout per line, will show shorter delay times than a single parallel terminated line with an equivalent total fanout. Multiple series terminated or damped lines also show greater flexibility in line routing than a single parallel terminated line. The choice between the two schemes will depend on the fanout number and physical layout of the system.

(2) Wired-OR – The outputs of several gates may be tied together to perform the Wired-OR or emitter dot function. One resistor is normally used to pulldown the outputs.

Figure 17 graphs typical rise and fall times and propagation delays versus the number of emitter dots for both 50 Ω to -2 volts termination and 510 Ω to VEE termination. Rise and fall times are not greatly affected by emitter dotting, with the exception of fall times with the 510 Ω loading. The reason for this is that the discharge path for load capacitance has a longer time constant with the 510 Ω resistor. The most significant effect of Wired-ORing is increased propagation delays. As for ac fanout, desired system speed is the basic limiting factor for the emitter dot.
A second limiting factor in the case of the emitter dot is a dc level shift as the number of dots increase. The wired emitter-followers share current through the pulldown resistor and each additional wired output causes the current in every output to decrease. The logic levels shift upward as device current decreases. As the 0 level shifts upward, noise margin may be lost. Figure 18 shows loading curves for a typical MECL 10,000 output and illustrates the shift in logic levels with output current. The 0 level shift and resulting reduction of noise margin may be a greater limiting factor than ac considerations, depending on system requirements.

When using Wire-OR, interconnections should be held to minimum lengths for unterminated lines and parallel terminated lines. For larger numbers of distributed emitter-dots and longer interconnections, a doubly terminated line called a “data bus” may be used. Figure 19 shows an example of a 100-ohm data bus system. The dc loading
on the line is 50 Ω as the 100 Ω terminating resistors are in parallel. However, for a transient waveform driven from any point on the line, the waveform travels to either end of the line and is properly terminated, so reflections are eliminated.

A lower impedance system is better for driving the high capacitive loading of a bus system. A 50 Ω system similar to the 100 Ω system is shown in figure 20. Notice that the drivers for the 50 Ω line must have two outputs in parallel to drive the 25 Ω dc load of the paralleled 50 Ω terminating resistors. The MC10110 or MC10111 multiple output gates may be used conveniently in this application.

When considering system timing, it must be noted that a long bus will add delay time to a data path. The worst case length on the bus, plus the effects of capacitive loading, should be considered for delay time. More will be said on bussing in the following section on board-to-board interconnections.

(3) Clock distribution Clock lines usually handle the highest frequency in a system. For large fanout, a distribution tree should be used for maximum frequencies (figure 21). A good rule of thumb is to limit fanout to 4 per line and use as low an impedance line as possible. Parallel terminated lines or series damped lines (as in figure 13) may be used. A parallel terminated 50 Ω line with a fanout of 4 will drive a clock line to a frequency of about 110 to 120 MHz.

For higher clock frequencies, series terminated lines with fanout limited to 1 or 2 may be used. Line lengths should be kept short and of equal length. A MECL III gate with faster edges will provide highest clock frequency capability.
BOARD-TO-BOARD INTERCONNECTS

Signal connections among logic cards, card panels, and cabinets are important for maintaining the best possible system performance. Ringing and crosstalk can appear when line lengths are long, or when characteristic impedance varies due to lack of a good ground. Ringing and crosstalk, along with power supply variations and system noise, can seriously affect system operation. To be within system noise margins (as previously mentioned, 125 mV worst case), maximum undershoot should be less than 100 to 110 mV.

The most practical means for limiting undershoot to less than 100 mV is either to limit line lengths, or else to use matched terminated transmission lines. Line lengths in board-to-board applications are necessarily long; therefore, some kind of terminated line should be used. The edge speeds of MECL 10,000 permit a choice among several methods for producing nominally constant impedance interconnections. Coaxial cable, mother-daughter boards, striplines, and wire over ground may be used.

When designing system interconnections, four parameters must be taken into consideration:

1. propagation delay per unit length of line;
2. attenuation of the line;
3. crosstalk between lines;
4. reflections due to mismatched impedance between the line and the line termination.

Propagation delay of the line is significant because unequal delays in parallel lines cause timing errors. Moreover, on long lines the total delay time will seriously affect system speed. Since the propagation delay of one foot of wire is approximately equal to the propagation delay of a MECL 10,000 Series gate, line lengths must be minimized when total system propagation time is of concern.

Attenuation is a characteristic of the line which increases for high frequency signals, due to higher impedance in the line. Attenuation first appears as a degradation in edge speed, then as a loss of signal amplitude for high frequencies on long lines. Within a backplane attenuation seldom is a problem, but is must be allowed for when interconnecting panels or cabinets.

Crosstalk is the coupling of a signal from one cable to a nearby cable. A coupled pulse in the direction of undershoot gives a reduction of noise immunity and should be avoided. A good ground system together with shielding is the best method for limiting crosstalk. Differential twisted pair line connections avoid problems of crosstalk by virtue of the common mode rejection of line receivers.

Reflections due to mismatched lines also cause loss of noise immunity. Successful termination of a line depends on how constant the impedance is maintained along the line. Coaxial cable is easier to terminate than open wire because of its constant impedance. In many cases twisted pair cable and ribbon cable may be purchased with specifications on the impedance of the line.

Conventional edge connectors may be utilized to get on and off PC boards with little mismatch in line impedances. Coaxial cable connectors which have excellent characteristics across the bandwidth exhibited by MECL 10,000 exist in a variety of types. The most popular types are BNC, and subminiature types such as SMA, SMB, or SMC.

SINGLE-ENDED LINES

Single ended lines are interconnections such as coaxial cable or other single path transmission line as opposed to a twisted pair of lines over which a differential signal is sent. To maintain some kind of constant impedance, a ground must be present. A ground plane may not be present for board-to-board interconnects, and so a ground must be run together with the signal line.

Types of single ended lines are discussed in the following paragraphs.

1. Coaxial Cable The well defined characteristic impedance of coaxial cable permits easy matching of the line, and the ground shield internal to the cable minimizes crosstalk between lines. In addition, low attenuation at high frequencies allows the cable to transmit the rise times associated with MECL signals.

Bandwidth and attenuation are the limiting factors in using coaxial cable. The bandwidth required for MECL 10,000 is:

\[
\text{f} \approx \frac{0.37}{\text{rise time}} ;
\]

\[
\approx \frac{3 \times 10^{-9}}{0.37} ;
\]

\[
\approx 125 \text{ MHz bandwidth for } 50 \text{ } \Omega \text{ load}. \]

Attenuation is due mainly to skin effect in the cable. The loss in signal amplitude due to attenuation will limit the maximum usable length of line. For a maximum signal reduction of 100 mV from the logic 1 and 0 levels (800 mV p/p to 600 mV p/p) the permissible attenuation is 2.5 dB:

\[
\text{dB} = 20 \log \left( \frac{V_{\text{in}}}{V_{\text{out}}} \right) = 20 \log \left( \frac{0.8}{0.6} \right) = 2.5 \text{ dB}.
\]

The maximum line length which will produce no more than 2.5 dB attenuation will be:

\[
\text{max length} = 100 \text{ ft.} \left( \frac{2.5 \text{ dB}}{\text{Atten}} \right)
\]

where Atten. is the cable attenuation in dB/100 ft. at the operating frequency.
Figure 22 shows curves for maximum line lengths versus operating frequencies for a 2.5 dB loss. Data for three cable types are plotted. A high bandwidth line is necessary to preserve fast signal edges regardless of the bit rate of a system.

In figure 22 it is assumed that the coaxial line is properly terminated with a resistive load equal to the characteristic impedance of the line. Standard carbon 28 or 14 watt resistors work well for all line terminations. However when using precision wire-wound or film resistors, care should be taken to determine the high frequency properties of these devices since they may become highly inductive at high frequencies, and thus be unusable.

Coaxial cable should be used for sending single-ended signals over long lines. The constant impedance and low attenuation of such cable allows transmission of signals with minimum distortion.

(2) Parallel Wire Cable Multiple conductor cable as purchased, or as constructed by lacing interconnecting wires together, is not normally used with MECL or other high speed logic types because of crosstalk. Such crosstalk is due to the capacitive and inductive coupling of signals between parallel lines. Such cable is also susceptible to external signals coupling to the entire cable. Multiple conductor, single-ended cable is not recommended for use with MECL unless individual shields on each wire are employed.

(3) Ribbon Cable Systems requiring large numbers of board-to-board interconnections may take advantage of multiconductor ribbon cable (figure 23). Ribbon cable is easily wired to connectors because of its in-line wire arrangement. Its flexibility permits easy routing and board removal. The side-by-side arrangement of signal lines produces a defined characteristic impedance because of the presence of alternate ground wires.

Commercial ribbon cable is available with a wide variety of characteristic impedances, and the manufacturer should be consulted for information on such cable parameters as attenuation, characteristic impedance, and number of conductors.

With ribbon as with coaxial cable, the maximum permissible attenuation is 2.5 dB. Attenuation per foot is generally higher for ribbon cable than for coaxial cable. Consequently maximum line lengths for ribbon are limited by operating frequency.

(4) Point-to-point Wiring A system made up of several logic cards may be assembled using edge connectors to form a card file. Point-to-point wiring via the board connectors may then be used for system interconnections.

A ground plane is often formed by a large printed circuit board to which the card connectors are mounted. The ground plane may be connected to the frame holding the card connectors. Metal is left on one side of the PC board to form the backplane system ground, or metal may be left on both sides of the board to supply power to the system logic cards. These card file systems are commercially available from a number of manufacturers.

When a solid ground plane is not practical, a ground screen should be constructed on the backplane. A ground screen may be made by connecting bus wires (wire size compatible with connector) to the edge connectors in a grid pattern, prior to signal wiring (figure 24). About every sixth pin on the card edge connectors is used as a ground, providing connection points for the ground grid. This interconnection of ground points forms a grid network of approximately 1 inch squares over which the signal lines are wired. A characteristic impedance of about 140 ohms can be expected for a wire over ground screen, depending upon the exact routing and distance from the screen.
To provide maximum signal purity, a motherboard composed of multilayer or two layer board may be used to mount the card connectors. Striplines or microstrip lines are designed on the circuit board, along with ground and voltage planes. Connectors are available to interface between cards and the motherboard with little line discontinuity. The motherboard technique is normally used when the system design is sufficiently determined that changes in the backplane wiring will be few.

When using point-to-point wiring with a ground plane or screen, soldered connections or wire wrap techniques may be used. In general one good terminating technique is to parallel terminate with approximately 100 to 120 Ω to -2 volts. The resistor will be near the characteristic impedance of the line and so minimize ringing. Series damping or termination may be used, following the rules presented previously. An unterminated line with a fanout of 4 may be up to 15 inches long when a ferrite bead is placed at the sending end of the line.

For high speed lines, such those for clock distribution, coaxial cable and twisted pair lines should be used between cards. Maximum signal integrity of clock signals should be maintained for best system performance.

DIFFERENTIAL TWISTED PAIR LINES

Twisted pair lines, differentially driven into a line receiver (figure 25), provide maximum noise immunity. Any noise coupled into a twisted pair line appears equally on both wires (common mode). Because the receiver senses only the differential voltage between the lines, crosstalk noise has no detrimental effect on the signal up to the common mode rejection limit of the receiver. The line receivers MC10115 and MC10116 have a common mode rejection limit of 1 volt to a positive-going common mode signal, and 2.5 volts to a negative-going common mode signal.

The partial schematic of an MC10115 line receiver is shown in figure 26. Each receiver is a differential amplifier whose output level is dependent on the input voltage differential. If the inputs, IN1 and IN2, are at the same voltage, the output will be at the mid point of a MECL 10,000 logic swing; that is, at -1.3 V = VBB (note that a pulldown resistor on the output is necessary). The output voltage will go more positive as input IN2 goes more positive than input IN1; that is, when the differential voltage from IN2 to IN1 is plus to minus. The inverse is also true. The output goes more negative than VBB when the polarity of the differential voltage from IN2 to IN1 is minus to plus (cf figure 26b).

The output voltage change of the receiver is equal to the input voltage differential times the voltage gain of the amplifier. To have a full MECL swing, the output must swing ±400 mV about VBB. Therefore, with the voltage gain of the differential amplifier typically 6 V/V, the minimum input differential must be approximately: 0.4 V/6 = 67 mV (either plus to minus or minus to plus.)

For system design, other factors affect the minimum differential input voltage. Decreasing voltage gain with increasing frequency (figure 27), offset voltage of the amplifier, and
plifier, noise, and other system parameters demand a larger input differential voltage. A minimum differential input voltage of 150 mV at maximum frequency is recommended for system design.

Except at slow bit rates, attenuation will be the limiting factor for twisted-pair line length. The dc equivalent of the twisted pair line of figure 25 is shown in figure 28. Ignoring the dc resistance in the line, the voltage across the terminating resistor is:

\[ V_{RT} = \frac{(5.2 \text{ V} - 0.9 \text{ V}) (100 \Omega)}{510 \Omega + 100 \Omega} \]

\[ = 0.705 \text{ V}. \]

Note that if \( V_R \) becomes as large as 800 mV and begins to go below a logic 0 level of -1.7 V, the NOR output will clamp the voltage at node B.

The voltage across the terminating resistor decreases as frequency increases due to attenuation in the line. Figure 29 tabulates the maximum differential voltage appearing across the termination resistor, versus frequency for a 50 ft. line as shown in figure 25. Maximum line length will be determined by operating frequency.

A different termination method for a twisted pair line is shown in figure 30. The pulldown resistors terminate the line. As a result, full output levels are presented to the receiver. Attenuation data for this line is shown in figure 31. Waveforms for input and output signals for both termination methods are pictured in figure 32.
A variety of cable types can be used with differential twisted pair lines:

1. Bundled twisted pair cable: Cable with several bundled twisted pairs is commercially available. When running MECL signals in parallel with higher voltage analog or logic signals, shielded twisted pair lines should be used. Shielded twisted pair lines have foil shield on each twisted pair that may be tied to the system ground.

2. Ribbon cable: Ribbon composed of several twisted pairs is one type of ribbon cable available. Conventional side-by-side cable (figure 23) may also be used with differentially driven signal lines (figure 33). With every other wire grounded, the signal lines will have a constant characteristic impedance.

Differential twisted pair lines offer several advantages under adverse conditions compared to single ended lines. For example, power supply and temperature variations might occur between panels or between cabinets of a system. Corresponding shifts in logic levels within the system will subtract from noise margins when driving single ended lines between these points in the system. However, differential lines are unaffected by variation in logic levels, since the receiver detects only the differential voltage between the driver outputs, rather than detecting absolute logic levels.

With single ended lines, noise generated on the signal line by crosstalk and inductive coupling directly reduces noise immunity. Noise is coupled equally onto both wires of a twisted pair line, so the differential voltage is unaffected. As a result, the receiver will not detect noise as long as it is within the common mode range of the receivers.

DATA BUSSING AND PARTY LINE TECHNIQUES

Data bussing usually requires large fanout, long lines, and several driving points. A MECL 10,000 bus or “party line” may be made by emitter-dotting gates together, with the restriction that only one driver is allowed to go high at one time.

Figures 19 and 20 illustrate data bus lines which may be extended for board-to-board use. The characteristic impedance of board-to-board interconnections will generally be from 100 to 150 ohms so the termination resistors must be adjusted accordingly.

Another scheme for bussing is the twisted-pair party line of figure 34. The driving gates are emitter-dotted. It is required that all their outputs be held low when not sending data. (VBB is available from the MC10115 and MC10116, and may be buffered as shown in figure 35 to handle the necessary termination current.)

In both bussing schemes the driving lines are operating single ended. However, the twisted pair bus retains the advantage of the common mode rejection of the line receivers. As previously mentioned, the limiting factors for emitter-dotting also apply to the party lines shown.

WIREWRAPPING TECHNIQUES

The versatility of MECL 10,000 allows the use of this logic family with wirewrapping techniques. Wirewrapping is popular for breadboarding large system prototypes and for interconnecting system logic boards. The ability to change system interconnections easily has made wirewrap extremely usable for breadboarding new system designs.
MECL 10,000 systems may be wirewrapped using high density dual-in-line packaging boards. In addition, wirewrapping may be used for board-to-board interconnections when the logic boards are mounted in a card file in edge connectors. Some general guidelines for use of MECL 10,000 with wirewrap follow:

SYSTEM PROTOTYPING Several types of wirewrap boards for dual-in-line packages are commercially available. For MECL 10,000 systems, a board should be used that has voltage planes on both sides of the board and low-profile device mounting. Device mounting via pins set in the boards is the most satisfactory method.

The VCC pins of the device mounting should be soldered to the VCC voltage plane (the voltage plane on the device side of the board is the best choice.) When the VCC pins are wirewrapped to the VCC voltage source, a ferrite bead on a wire between the VCC1 and the VCC2 pins of the same package will help avoid high frequency noise and will prevent possible oscillation. Long leads from the ground plane to the VCC pins help induce oscillation and noise, due to their added inductance. VEE pins may be wirewrapped to the VEE voltage plane with no detrimental effects. Bypassing on the board should be provided in a manner similar to that mentioned for a two-sided PC board with a ground plane.

Wiring rules for wirewrapped interconnections are similar to those for a wire over ground. If a voltage plane is present, the characteristic impedance of a wirewrap interconnection is 100 to 150 ohms. Parallel termination, series damping, and unterminated lines may all be used, and the unterminated line lengths of figure 8 (backplane) also apply to wirewrap. However, in prototyping and breadboarding these lengths may be extended if low bit rates are present or if greater ringing is acceptable. When doing prototype breadboarding, the designer is often concerned with the "workability" of the design, as opposed to operation with best noise margins and signal waveforms.

With wirewrap, the pulldown resistors may be provided by commercial resistor networks in a variety of values suitable for MECL 10,000 terminations. Resistor networks with good high frequency characteristics should be used. Networks composed of discrete resistor chips mounted in a package, or thick-film cermet resistors with a minimum of interconnect metal within the package, provide the best high frequency characteristics. Wirewrap equipment manufacturers have made dual-in-line adaptor plugs available, to allow discrete components to be mounted for use on the wirewrap board (cf figure 36).

An example of a wirewrap system is shown in figure 37. A 4 x 4 bit multiplier (figure 38) was constructed using MECL 10,000. The delay line oscillator has a frequency of 30 MHz and the total multiplication cycle time is about 175 ns. The multiplier uses an add-shift algorithm.

The clock distribution for this system used a parallel terminated wirewrap line (Thevenin equivalent). Twisted pair lines may also be used for clock distribution, and are helpful for higher clock rates. With wirewrap, maximum clock rates are in the neighborhood of 100 MHz, when using twisted pairs.

To get signals on and off the board, commercially available multiconductor ribbon cable was utilized. Commercial cable adaptors, which plug into the wirewrap board, are available. Alternate lines are grounded to minimize crosstalk and generate a characteristic impedance for the signal lines.

BACKPLANE WIREWRAP A card file composed of several logic cards may use wirewrap for board-to-board interconnection. The same rules as discussed in the section, SINGLE-ENDED LINES #4 for board-to-board interconnects, apply to wirewrap. A ground plane or ground screen is recommended; termination techniques and line lengths should follow the rules previously presented.
FIGURE 37 - 4 x 4 Bit Multiplier Prototype Showing Wirewrap with MECL 10,000 Logic
CONCLUSION

This application note has been written to present information which a designer may use to construct a reliable, high performance MECL 10,000 system. Much of the transmission line theory that explains the effects of high speed signals on interconnects has not been presented here because the application note is directed toward usage rules rather than a detailed theoretical discussion. For more detailed information on transmission line theory and other MECL system considerations such as power supply variations and thermal considerations, the designer is directed to the MECL System Design Handbook, published by Motorola Semiconductor Products Inc.

References:
IMPEDEANCE MATCHING NETWORKS
APPLIED TO R-F POWER TRANSISTORS

Prepared by:
B. Becciolini
Applications Engineering
Geneva, Switzerland
1. INTRODUCTION

Some graphic and numerical methods of impedance matching will be reviewed here. The examples given will refer to high frequency power amplifiers. Although matching networks normally take the form of filters and therefore are also useful to provide frequency discrimination, this aspect will only be considered as a corollary of the matching circuit.

Matching is necessary for the best possible energy transfer from stage to stage. In RF-power transistors the input impedance is of low value, decreasing as the power increases, or as the chip size becomes larger. This impedance must be matched either to a generator — of generally 50 ohms internal impedance — or to a preceding stage. Impedance transformation ratios of 10 or even 20 are not rare. Interstage matching has to be made between two complex impedances, which makes the design still more difficult, especially if matching must be accomplished over a wide frequency band.

2. DEVICE PARAMETERS

2.1 INPUT IMPEDANCE

The general shape of the input impedance of RF-power transistors is as shown in Figure 1. It is a large signal parameter, expressed here by the parallel combination of a resistance $R_P$ and a reactance $X_P$ (Ref. (1)).

The equivalent circuit shown in Figure 2 accounts for the behaviour illustrated in Figure 1.

With the presently used stripline or flange packaging, most of the power devices for VHF low band will have their $R_P$ and $X_P$ values below the series resonant point $f_S$. The input impedance will be essentially capacitive.

Most of the VHF high band transistors will have the series resonant frequency within their operating range, i.e. be purely resistive at one single frequency $f_S$, while the parallel resonant frequency $f_P$ will be outside.

Parameters for one or two gigahertz transistors will be beyond $f_S$ and approach $f_P$. They show a high value of $R_P$ and $X_P$ with inductive character.

A parameter that is very often used to judge on the broadband capabilities of a device is the input Q or $Q_{IN}$, defined simply as the ratio $R_P/X_P$. Practically $Q_{IN}$ ranges around 1 or less for VHF devices and around 5 or more for microwave transistors.

$Q_{IN}$ is an important parameter to consider for broadband matching. Matching networks normally are low-pass or pseudo low-pass filters. If $Q_{IN}$ is high, it can be necessary to use band-pass filter type matching networks and to allow insertion losses. But broadband matching is still possible. This will be discussed later.

2.2. OUTPUT IMPEDANCE

The output impedance of the RF-power transistors, as given by all manufacturers' data sheets, generally consists of only a capacitance $C_{OUT}$. The internal resistance of the transistor is supposed to be much higher than the load and is normally neglected. In the case of a relatively low internal resistance, the efficiency of the device would decrease by the factor:

$$1 + \frac{R_L}{R_T}$$
where $R_L$ is the load resistance, seen at the collector-emitter terminals, and $R_T$ the internal transistor resistance equal to:

$$\frac{1}{\omega_T \left( C_{TC} + C_{DC} \right)}$$

defined as a small signal parameter, where:

$$\omega_T = \text{transit angular frequency}$$

$$C_{TC} + C_{DC} = \text{transition and diffusion capacitances at the collector junction}$$

The output capacitance $C_{OUT}$, which is a large signal parameter, is related to the small signal parameter $C_{CB}$, the collector-base transition capacitance.

Since a junction capacitance varies with the applied voltage, $C_{OUT}$ differs from $C_{CB}$ in that it has to be averaged over the total voltage swing. For an abrupt junction and assuming certain simplifications, $C_{OUT} = 2 C_{CB}$.

Figure 3 shows the variation of $C_{OUT}$ with frequency. $C_{OUT}$ decreases partly due to the presence of the collector lead inductance, but mainly because of the fact that the base-emitter diode does not shut off anymore when the operating frequency approaches the transit frequency $f_T$.

3. OUTPUT LOAD

In the absence of a more precise indication, the output load $R_L$ is taken equal to:

$$R_L = \frac{V_{CC} - V_{CE \text{ (sat)}}}{2 P_{OUT}}$$

with $V_{CE \text{ (sat)}}$ equal to 2 or 3 volts, increasing with frequency.

The above equation just expresses a well-known relation, but also shows that the load, in first approximation, is not related to the device, except for $V_{CE \text{ (sat)}}$. The load value is primarily dictated by the required output power and the peak voltage; it is not matched to the output impedance of the device.

At higher frequencies this approximation becomes less exact and for microwave devices the load that must be presented to the device is indicated on the data sheet. This parameter will be measured on all Motorola RF-power devices in the future.

Strictly speaking, impedance matching is accomplished only at the input. Interstage and load matching are more impedance transformations of the device input impedance and of the load into a value $R_L$ (sometimes with additional reactive component) that depends essentially on the power demanded and the supply voltage.

4. MATCHING NETWORKS

In the following, matching networks will be described by order of complexity. These are ladder type reactance networks.

The different reactance values will be calculated and determined graphically. Increasing the number of reactances broadens the bandwidth. However, networks consisting of more than four reactances are rare. Above four reactances, the improvement is small.

4.1 NUMERICAL DESIGN

4.1.1 Two-Resistance Networks

Resistance terminations will first be considered. Figure 4 shows the reactive L-section and the terminations to be matched.

Matching or exact transformation from $R_2$ into $R_1$ occurs at a single frequency $f_0$.

At $f_0$, $X_1$ and $X_2$ are equal to:

$$X_1 = \pm R_1 \frac{R_2}{\sqrt{R_1 - R_2}} = R_1 \frac{1}{\sqrt{n - 1}}$$

$$X_2 = \frac{R_1 - R_2}{\sqrt{R_1 - R_2}} = R_1 \frac{\sqrt{n - 1}}{n}$$

At $f_0$: $X_1 \cdot X_2 = R_1 \cdot R_2$

$X_1$ and $X_2$ must be of opposite sign. The shunt reactance is in parallel with the larger resistance.

The frequency response of the L-section is shown in Figure 5, where the normalized current is plotted as a function of the normalized frequency.

If $X_1$ is capacitive and consequently $X_2$ inductive, then:

$$X_1 = -\frac{f_0}{f} R_1 \sqrt{\frac{R_2}{R_1 - R_2}} = -\frac{f_0}{f} R_1 \frac{1}{\sqrt{n - 1}}$$

and

$$X_2 = \frac{f_0}{f} \sqrt{\frac{R_2}{R_1 - R_2}} = \frac{f_0}{f} R_1 \frac{\sqrt{n - 1}}{n}$$
The normalized current absolute value is equal to:

\[ I_2 \left| \frac{I_0}{I_0} \right| = \frac{2\sqrt{n}}{\sqrt{(n-1)^2 - (f_0/f_1)^2 - (n+1)^2}} \]

where

\[ I_0 = \sqrt{\frac{V}{2R_1}} \]

and is plotted in Figure 5 (Ref. (2)).

If \( X_1 \) is inductive and consequently \( X_2 \) capacitive, the only change required is a replacement of \( f \) by \( f_0 \) and vice-versa. The L-section has low pass form in the first case and high-pass form in the second case.

The \( Q \) of the circuit at \( f_0 \) is equal to:

\[ Q = \frac{X_2}{R_1} = \frac{1}{\sqrt{(n-1)^2 - (f_0/f_1)^2 - (n+1)^2}} \]

For a given transformation ratio \( n \), there is only one possible value of \( Q \). On the other hand, there are two symmetrical solutions for the network, that can be either a low-pass filter or a high-pass filter.

The frequency \( f_0 \) does not need to be the center frequency, \( f_1 + f_2 \), of the desired band limited by \( f_1 \) and \( f_2 \).

In fact, as can be seen from the low-pass configuration of Figure 5, it may be interesting to shift \( f_0 \) toward the high band edge frequency \( f_2 \) to obtain a larger bandwidth \( w \), where

\[ w = \frac{2(f_1 + f_2)}{f_2 - f_1} \]

This will, however, be at the expense of poorer harmonic rejection.

Example:
For a transformation ratio \( n = 4 \), it can be determined from the above relations:

| Bandwidth \( w \) | 0.1 | 0.3 |
| Max insertion losses | 0.025 | 0.2 |
| \( X_1/R_1 \) | 1.730 | 1.712 |

If the terminations \( R_1 \) and \( R_2 \) have a reactive component \( X \), the latter may be taken as part of the external reactance as shown in Figure 6.

This compensation is applicable as long as

\[ Q_{INT} = \frac{X_{INT}}{R_2} \quad \text{or} \quad \frac{R_1}{X_{INT}} < n-1 \]

Tables giving reactance values can be found in Ref. (3) and (4).

4.1.1 Use of transmission lines and inductors
In the preceding section, the inductance was expected to be realized by a lumped element. A transmission line can be used instead (Fig 7).

As can be seen from the computed selectivity curves (Fig. 8) for the two configurations, transmission lines result in a larger bandwidth. The gain is important for a transmission line having a length \( L = \lambda/4 \) (\( \Theta = 90^\circ \)) and a characteristic impedance \( Z_0 = \sqrt{R_1 \cdot R_2} \). It is not significant for lines short with respect to \( \lambda/4 \). One will notice that there is an infinity of solutions, one for each value of \( C \), when using transmission lines.

4.1.2 Three-reactance matching networks
The networks which will be investigated are shown in Figure 9. They are made of three reactances alternatively connected in series and shunt.
A three-reactances configuration allows to make the quality factor $Q$ of the circuit and the transformation ratio $n = \frac{R_2}{R_1}$ independent of each other and consequently to choose the selectivity between certain limits.

For narrow band designs, one can use the following formulas (Ref. (5) AN-267, where tables are given):

Network (a):

$$X_{C1} = \frac{R_1}{Q} \quad Q \text{ must be first selected}$$

$$X_{C2} = R_2 \sqrt{\frac{R_1 R_2}{Q^2 + 1} - \frac{R_1}{R_2}}$$

$$X_L = \frac{Q R_1 + (R_1 R_2/X_{C2})}{Q^2 + 1}$$

---

**Fig. 8** - Bandwidth of the L-section for $n = 10$

(a) with lumped constants

(b) with a transmission line ($\lambda/4$)
Fig. 9 - Three-reactance matching networks

Network (b):

\[ X_{L1} = R_1 \Omega \]
\[ X_{L2} = R_2 \Omega \]
\[ X_{C1} = \frac{A}{Q + B} \]

Q must first be selected

A = \( R_1 \left( 1 + Q^2 \right) \)
B = \( \sqrt{\frac{A}{Q + B}} \)

Network (c):

\[ X_{L1} = Q R_1 \]
\[ X_{C2} = A R_2 \]
\[ X_{C1} = \frac{B}{Q - A} \]

Q must first be selected

A = \( \sqrt{\frac{R_2 \left( 1 + Q^2 \right)}{R_2}} \)
B = \( R_1 \left( 1 + Q^2 \right) \)

The network which yields the most practical component values, should be selected for a given application.

The three-reactance networks can be thought of as being formed of a L-section (two reactances) and of a compensation reactance. The L-section essentially performs the impedance transformation, while the additional reactance compensates for the reactive part of the transformed impedance over a certain frequency band.

Figure 10 shows a representation in the Z-plane of the circuit of Figure 9 (a) split into two parts \( R_1 \cdot C_1 \cdot L_1 \) and \( C_2 \cdot R_2 \).

Exact transformation from \( R_1 \) into \( R_2 \) occurs at the points of intersection \( M \) and \( N \). Impedances are then conjugate or \( Z^* = R' + jX' \) and \( Z'' = R'' + jX'' \) with \( R' = R'' \) and \( X' = -X'' \).

The only possible solution is obtained when \( X' \) and \( -X'' \) are tangential to each other. For the dashed curve, representing another value of \( L_1 \) or \( C_1 \), a wider frequency band could be expected at the expense of some ripple inside the band. However, this can only be reached with four reactances as will be shown in section 4.1.3.

With a three-reactance configuration, there are not enough degrees of freedom to permit \( X' = -X'' \) and simultaneously obtain the same variation of frequency on both curves from \( M' \) to point \( N' \).

The values of the three reactances can be calculated by making \( X' = -X'' \), \( R' = R'' \), and \( dX' = dX'' \), \( dR' = dR'' \).

The general solution of these equations leads to complicated calculations. Therefore, computed tables should be used.

One will note on Figure 10 that the compensation reactance contributes somewhat to impedance transformation, i.e. \( R' \) varies when going from \( M \) to \( R_2 \).

The circuit of Figure 9 (b) is dual with respect to the first one and gives exactly the same results in a Y-plane representation.

Circuit of Figure 9 (c) is somewhat different since only one intersection \( M \) exists as shown in Figure 11. Narrower frequency bands must be expected from this configuration. The widest band is obtained for \( C_1 = \infty \).

Again, if one of the terminations has a reactive component, the latter can be taken as a part of the matching network, provided it is not too large (see Fig. 6).
4.1.3 Four-reactance networks

Four-reactance networks are used essentially for broadband matching. The networks which will be considered in the following consist of two two-reactance sections in cascade. Some networks have pseudo low-pass filter character, others band-pass filter character. In principle, the former show narrower bandwidth since they extend the impedance transformation to very low frequencies unnecessarily, while the latter insure good matching over a wide frequency band around the center frequency only (see Fig. 14).

The two-reactance sections used in above networks have either transformation properties or compensation properties. Impedance transformation is obtained with one series reactance and one shunt reactance. Compensation is made with both reactances in series or in shunt.

If two cascaded transformation networks are used, transformation is accomplished partly by each one. With four-reactance networks there are two frequencies, \( f_1 \) and \( f_2 \), at which the transformation from \( R_1 \) into \( R_2 \) is exact. These frequencies may also coincide.

For network (b) for instance, at point M, \( R_1 \) or \( R_2 \) is transformed into \( \sqrt{R_1 R_2} \) when both frequencies fall together. At all points (M), \( Z_1 \) and \( Z_2 \) are conjugate if the transformation is exact.

In the case of Figure 12 (b) the reactances are easily calculated for equal frequencies:

\[
X_1 = \frac{R_1}{\sqrt{n-1}}, \quad X_2 = R_1 \sqrt{\frac{\sqrt{n-1}}{n}}, \quad X_3 = \frac{R_1}{\sqrt{n (\sqrt{n-1})}}, \quad X_4 = \frac{R_1}{n} \sqrt{\frac{\sqrt{n-1}}{n}}
\]

For network (a) normally, at point (M), \( Z_1 \) and \( Z_2 \) are complex. This pseudo low-pass filter has been computed elsewhere (Ref. (3)). Many tables can be found in the literature for networks of four and more reactances having Tchebyscheff character or maximally-flat response (Ref. (3), (4) and (6)).

Figure 13 shows the transformation path from \( R_1 \) to \( R_2 \) for networks (a) and (b) on a Smith-Chart (refer also to section 4.2, Graphic Design).

Case (a) has been calculated using tables mentioned in Ref. (4).

Case (b) has been obtained from the relationship given above for \( X_1 \ldots X_4 \). Both apply to a transformation ratio equal to 10 and for \( R_1 = 1 \).

![Fig. 13 - Transformation paths for networks (a) and (b)](image-url)
There is no simple relationship for $X'1 \ldots X'4$ of network (b) if $f_1$ is made different from $f_2$ for larger bandwidth.

Figure 14 shows the respective bandwidths of network (a) and (b) for the circuits shown in Figure 13.

\[ Q' = \sqrt{n - 1} \]

The maximum value of reactance that the terminations may have for use in this configuration can be determined from the above values of $Q'$.

As mentioned earlier, the four-reactance network can also be thought of as two cascaded two-reactance sections; one used for transformation, the other for compensation. Figure 16 shows commonly used compensation networks, together with the associated L-section.

From Figure 15 it can be seen that network (a) is more sensitive to $R_1$ changes than network (b).

The circuit of Figure 16 (a) can be compared to the three-reactance network shown in Figure 9 (c). The difference is that capacitor $C_2$ of that circuit has been replaced by a L-C circuit. The resulting improvement may be seen by comparing Figure 17 with Figure 11.
By adding one reactance, exact impedance transformation is achieved at two frequencies. It is now possible to choose component values such that the point of intersection $M'$ occurs at the same frequency $f_1$ on both curves and simultaneously that $N'$ occurs at the same frequency $f_2$ on both curves. Among the infinite number of possible intersections, only one allows to achieve this.

When $M'$ and $N'$ coincide in $M$, the new condition \[ \frac{dX'}{df} = \frac{dX''}{df} \]
can be added to the condition \[ X' = -X'' \] (for three-networks) and similarly $R' = R''$ and \[ \frac{dR'}{df} = \frac{dR''}{df} \].

If $f_1$ is made different from $f_2$, a larger bandwidth can be achieved at the expense of some ripple inside the band.

Again, a general solution of the above equations leads to still more complicated calculations than in the case of three-reactance networks. Therefore, tables are preferable (Ref. (3), (4) and (6)).

The circuit of Figure 16 (b) is dual of the circuit of Figure 14 (a) and does not need to be treated separately. It gives exactly the same results in the $Z$-plane. Figure 16 (c) shows a higher order compensation requiring six reactive elements.

The above discussed matching networks employing compensation circuits result in narrower bandwidths than the former solutions (see paragraph 4.1.3) using two transformation sections. A matching with higher order compensation such as in Figure 16 (c) is not recommended. Better use can be made of the large number of reactive elements using them all for transformation.

When the above configurations are realized using short portions of transmission lines, the equations or the usual tables no longer apply. The calculations must be carried out on a computer, due to the complexity. However, a graphic method can be used (see next section) which will consist essentially in tracing a transformation path on the $Z-Y$-chart using the computed lumped element values and replacing it by the closest path obtained with distributed constants. The bandwidth change is not significant as long as short portions of lines are used (Ref. (13)).

4.1.4 Matching networks using quarter-wave transformers

At sufficiently high frequencies, where $\lambda/4$-long lines of practical size can be realized, broadband transformation can easily be accomplished by the use of one or more $\lambda/4$-sections.

Figure 18 summarizes the main relations for (a) one-section and (b) two-section transformation.

A compensation network can be realized using a $\lambda/2$-long transmission line.

Figures 19 and 20 show the selectivity curves for different transformation ratios and section numbers.

Exponential lines

Exponential lines have largely frequency independent transformation properties.

The characteristic impedance of such lines varies exponentially with their length $l$:

\[ Z = Z_0 e^{k l} \]

where $k$ is a constant, but these properties are preserved only if $k$ is small.
4.1.5 Broadband matching using band-pass filter type networks. High Q case.

The above circuits are applicable to devices having low input or output Q, if broadband matching is required. Generally, if the impedances to be matched can be represented for instance by a resistor R in series with an inductor L (sometimes a capacitor C) within the band of interest and if L is sufficiently low, the latter can be incorporated into the first inductor of the matching network. This is also valid if the representation consists of a shunt combination of a resistor and a reactance.

Practically this is feasible for Q’s around one or two. For higher Q’s or for input impedances consisting of a series or parallel resonant circuit (see Fig. 2), it appears to be for large bandwidths, a different treatment must be followed.

Let us first recall that, as shown by Bode and Fano (Ref. (7) and (8)), limitations exist on the impedance matching of a complex load. In the example of Figure 21, the load to be matched consists of a capacitor C and a resistor R in shunt.

![Diagram of General matching conditions](image)

The reflection coefficient between transformed load and generator is equal to:

\[ \Gamma = \frac{Z_{IN} - R}{Z_{IN} + R} \]

\[ \Gamma = 0, \text{ perfect matching,} \]

\[ \Gamma = 1, \text{ total reflection.} \]

The ratio of reflected to incident power is:

\[ \frac{P_r}{P_i} = |\Gamma|^2 \]

The fundamental limitation on the matching takes the form:

\[ \int_{0}^{\infty} \ln \left( \frac{1}{|\Gamma|^2} \right) d\omega \leq \frac{\pi}{RC} \]

Bode equation

and is represented in Figure 22.

For a given complex load, an extension of the bandwidth from \( \omega_1 \) to \( \omega_2 \) is possible only with a simultaneous increase of the attenuation a. This is especially noticeable for Q’s exceeding one or two (see Figure 24).

Thus, devices having relatively high input Q’s are useable for broadband operation, provided the consequent higher attenuation or reflection introduced is acceptable.

The general shape of the average insertion losses or attenuation a (neglecting the ripple) of a low-pass impedance matching network is represented in Figure 24 as a function of 1/Q for different numbers of network elements n (Ref. (31)).

![Diagram of Insertion losses as a function of 1/Q](image)
For a given \( Q \) and given ripple, the attenuation decreases if the number \( n \) of the network elements increases. But above \( n = 4 \), the improvement is small.

For a given attenuation \( a \) and bandwidth, the larger \( n \) the smaller the ripple.

For a given attenuation and ripple, the larger \( n \) the larger the bandwidth.

Computations show that for \( Q < 1 \) and \( n \leq 3 \) the attenuation is below 0.1 dB approximately. The impedance transformation ratio is not free here. The network is a true low-pass filter. For a given load, the optimum generator impedance will result from the computation.

Before impedance transformation is introduced, a conversion of the low-pass prototype into a band-pass filter type network must be made. Figure 25 summarizes the main relations for this conversion.

\[
\begin{align*}
Q_{\text{IN max}} &= \frac{\omega_0 L_1}{R_0} \\
Q_{\text{IN max}} &= \frac{\omega_0 L_2}{R_0}
\end{align*}
\]

where \( \omega_0 = \frac{\omega}{\Delta \omega} \) and \( r = \frac{\omega_0}{\omega} \).

In practice the normal procedure for using a band-pass filter type matching network will be the following:

1. For a given bandwidth, center frequency and input impedance of a device to be matched, e.g. to 50 ohms, first determine \( Q_{\text{IN}} \) from the data sheet as \( \frac{\omega_0 L_1}{R_0} \) after having eventually added a series reactor for centering.
2. Convert the equivalent circuit \( R_0 L_1 C_1 \) into a low-pass prototype \( R_0 L_1 C_1 \) using the formulas of Figure 25.
3. Determine the other reactance values from tables (Ref. 13) for the desired bandwidth.
4. Convert the element values found by step (3) into series or parallel resonant circuit parameters.
5. Insert the impedance inverter in any convenient place.

In the above discussions, the gain roll-off has not been taken into account. This is of normal use for moderate bandwidths (30% for ex.). However, several methods can be employed to obtain a constant gain within the band despite the intrinsic gain decrease of a transistor with frequency.

Tables have been computed elsewhere (Ref. 10) for matching networks approximating 6 dB/octave attenuation versus frequency.

Another method consists in using the above mentioned network and then to add a compensation circuit as shown for example in Figure 27.
Resonance $\omega_b$ is placed at the high edge of the frequency band. Choosing $Q$ correctly, roll-off can be made 6 db/octave.

The response of the circuit shown in Figure 27 is expressed by:

$$1 + Q^2 \left( \frac{\omega}{\omega_b} - \frac{\omega_b}{\omega} \right)^2$$

where $\omega < \omega_b$

This must be equal to $\omega_c$ for 6db/octave compensation.

At the other band edge $\omega_a$, exact compensation can be obtained if:

$$Q = \frac{\omega_b}{\omega_a} - \frac{\omega_a}{\omega_b}$$

4.1.6 Line Transformers

The broadband properties of line transformers make them very useful in the design of broadband impedance matching networks (Ref. (11) and (12)).

A very common form is shown by Figure 28. This is a 4:1 impedance transformer. Other transformation ratios like 9:1 or 16:1 are also often used but will not be considered here.

The high frequency cut-off is determined by the length of line which is usually chosen smaller than $\lambda_{\text{min}}/8$. Short lines extend the high frequency performance.

The low frequency cut-off is determined first by the length of line, long lines extending the low frequency performance of the transformer. Low frequency cut-off is also improved by a high even mode impedance, which can be achieved by the use of ferrite material. With matched ends, no power is coupled through the ferrite which cannot saturate.

For matched impedances, the high frequency attenuation $a$ of the 4:1 transformer is given by:

$$a = \frac{1 + 3 \cos \frac{\pi}{\lambda} \frac{1}{\lambda} + 4 \sin^2 \frac{2\pi}{\lambda} \frac{1}{\lambda}^2}{4(1 + \cos \frac{2\pi}{\lambda} \frac{1}{\lambda}^2)}$$

For $l = \lambda/4$, $a = 1.25$ or 1 db; for $l = \lambda/2$, $a = \infty$

The characteristic impedance of the line transformer must be equal to:

$$Z_0 = \sqrt{R_L R}$$

Figures 29 and 30 show two different realizations of 4:1 transformers for a 50 to 12.5 ohm-transformation designed for the band 118-136 MHz.

The transformers are made of two printed circuit boards or two ribbons stuck together and connected as shown in Figures 29 and 30.
4.2 GRAPHIC DESIGN

The common method of graphic design makes use of the Impedance-Admittance Chart (Smith Chart). It is applicable to all ladder-type networks as encountered in matching circuits.

Matching is supposed to be realized by the successive algebraic addition of reactances (or susceptances) to a given start impedance (or admittance) until another end impedance (or admittance) is reached.

Impedance chart and admittance chart can be superimposed and used alternatively due to the fact that an immittance point, defined by its reflection coefficient $\Gamma$ with respect to a reference, is common to the Z-chart and the Y-chart, both being representations in the $\Gamma$-plane.

$$\Gamma = \frac{Z - R_s}{Z + R_s} = \gamma_r + j\gamma_i$$

$$\Gamma = \frac{G_s - Y}{G_s + Y} \quad R_s = \frac{1}{G_s} \quad \text{Characteristic impedance of the line}$$

More precisely, the Z-chart is a plot in the $\Gamma$-plane, while the Y-chart is a plot in the $-\Gamma$-plane. The change from the $\Gamma$ to $-\Gamma$-plane is accounted for in the construction rules given below.

Figure 31 and 32 show the representation of normalized $Z$ and $Y$ respectively, in the $\Gamma$-plane.

\[\begin{align*}
Z &= \frac{Z}{R_s} = \frac{z}{1 + \gamma_z} \\
\gamma_z &= \frac{1 - \gamma_z^2}{1 + \gamma_z^2} \\
x &= \frac{\gamma_z}{1 - \gamma_z^2} \\
\gamma_i &= \frac{2x^2 - 1}{(x + 1)^2 + x^2} \\
\gamma_i &= \frac{2x^2 - 1}{(x + 1)^2 + x^2}
\end{align*}\]
The Z-chart is used for the algebraic addition of series reactances. The Y-chart is used for the algebraic addition of shunt reactances.

For the practical use of the charts, it is convenient to make the design on transparent paper and then place it on a usual Smith-chart of impedance type (for example). For the addition of a series reactor, the chart will be placed with "short" to the left. For the addition of a shunt reactor, it will be rotated by 180° with "short" (always in terms of impedance) to the right.

The following design rules apply. They can very easily be found by thinking of the more familiar Z and Y representation in rectangular coordinates.

For joining two impedance points, there are a infinity of solutions. Therefore, one must first decide on the number of reactances that will constitute the matching network. This number is related essentially to the desired bandwidth and the transformation ratio.

<table>
<thead>
<tr>
<th>Addition of</th>
<th>Chart to be used</th>
<th>Direction</th>
<th>Using curve of constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>series R</td>
<td>Z</td>
<td>open</td>
<td>x</td>
</tr>
<tr>
<td>series G</td>
<td>Y</td>
<td>short</td>
<td>b</td>
</tr>
<tr>
<td>series C (+jωC)</td>
<td>Z</td>
<td>ccw</td>
<td>r</td>
</tr>
<tr>
<td>shunt C (+jωC)</td>
<td>Y</td>
<td>cw</td>
<td>g</td>
</tr>
<tr>
<td>series L (+jωL)</td>
<td>Z</td>
<td>cw</td>
<td>r</td>
</tr>
<tr>
<td>shunt L (+jωL)</td>
<td>Y</td>
<td>ccw</td>
<td>g</td>
</tr>
</tbody>
</table>

Secondly, one must choose the operating Q of the circuit, which is also related to the bandwidth. Q can be defined at each circuit node as the ratio of the reactive part to the real part of the impedance at that node. The Q of the circuit, which is normally referred to, is the highest value found along the path.

Constant Q curves can be superimposed to the charts and used in conjunction with them. In the Γ-plane, Q-curves are circles with a radius equal to\(\sqrt{1 + \frac{1}{Q^2}}\) and a center at the point \(+\frac{1}{Q}\) on the imaginary axis, which is expressed by:

\[
Q = \frac{x}{r} = \frac{2\gamma_i}{1 - \gamma_i^2 - \gamma_f^2} \quad \gamma_f^2 + \left(\frac{\gamma_i + \frac{1}{Q}}{Q}\right)^2 = 1 + \frac{1}{Q^2}.
\]

The use of the charts will be illustrated with the help of an example.

The following series shunt conversion rules also apply:

\[
R = \frac{R'}{1 + \frac{R'^2}{X'^2}} \quad G' = \frac{1}{R'} = \frac{R}{R^2 + X^2}
\]

\[
X = \frac{X'}{1 + \frac{X'^2}{R'^2}} \quad -B' = \frac{1}{X'} = \frac{X}{R^2 + X^2}
\]
Figure 33 shows the schematic of an amplifier using the 2N5642 RF power transistor. Matching has to be achieved at 175 MHz, on a narrow band basis. The rated output power for the device in question is 20 W at 175 MHz and 28 V collector supply. The input impedance at these conditions is equal to 2.6 ohms in parallel with -200 pF (see data Sheet). This converts to a resistance of 1.94 ohms in series with a reactance of 1.1 ohm.

The collector load must be equal to:

\[
\frac{[V_{cc} - V_{ce (sat)}]^2}{2 \times P_{out}} \quad \text{or} \quad \frac{(28 - 3)^2}{40} = 15.6 \text{ohms.}
\]

The collector capacitance given by the data sheet is 40 pF, corresponding to a capacitive reactance of 22.7 ohms.

The output impedance seen by the collector to insure the required output power and cancel out the collector capacitance must be equal to a resistance of 15.6 ohms in parallel with an inductance of 22.7 ohms. This is equivalent to a resistance of 10.6 ohms in series with an inductance of 7.3 ohms.

The input Q is equal to, \(Q_{in} = 1.1/1.94 \) or 0.57 while the output Q is 7.3/10.6 or 0.69.

It is seen that around this frequency, the device has good broadband capabilities. Nevertheless, the matching circuit will be designed here for a narrow band application and the effective Q will be determined by the circuit itself not by the device.

Figure 34 shows the normalized impedances (to 50 ohms).

Figure 35 shows the diagram used for the graphic design of the input matching circuit. The circuit Q must be larger than about 5 in this case and has been chosen equal to 10. At Q = 5, \(C_1\) would be infinite. The addition of a finite value of \(C_1\) increases the circuit Q and therefore the selectivity. The normalized values between brackets in the Figure are admittances \((g + jb)\).

At \(f = 175\text{MHz}\), the following results are obtained:

\[
\begin{align*}
\omega L_3 &= 50 \times 0.39 - 0.022 = 18.5 \text{ohms} \\
\omega C_2 &= 50 \times 0.420 = 20.04 \text{mhos} \\
\omega C_1 &= 50 \times 0.175 = 8.75 \text{ohms} \\
\omega C_5 &= 50 \times 0.038 = 1.9 \text{mhos}
\end{align*}
\]

The circuit Q at the output is equal to 1.9.
The selectivity of a matching circuit can also be determined graphically by changing the x or b values according to a chosen frequency change. The diagram will give the VSWR and the attenuation can be computed.

The graphic method is also useful for conversion from a lumped circuit design into a stripline design. The immittance circles will now have their centres on the 1 + jo point.

At low impedance levels (large circles), the difference between lumped and distributed elements is small.

5. PRACTICAL EXAMPLE

The example shown refers to a broadband amplifier stage using a 2N 6083 for operation in the VHF-band 118-136 MHz. The 2N 6083 is a 12.5 V-device and, since amplitude modulation is used at these transmission frequencies, that choice supposes low level modulation associated with a feedback system for distortion compensation.

Line transformers will be used at the input and output. Therefore the matching circuits will reduce to two-reactance networks, due to the relatively low impedance transformation ratio required.

5.1 DEVICE CHARACTERISTICS

Input impedance of the 2N 6083 at 125 MHz:
\[ R_p = 0.9 \text{ ohms} \]
\[ C_p = -390 \text{ pF} \]

Rated output power:
30W for 8W input at 175MHz. From the data sheet it appears that at 125MHz, 30W output will be achieved with about 4W input.

Output impedance:
\[ \frac{(V_{cc} - V_{ce \text{ (sat)}})^2}{2 \times P_{out}} = \frac{100}{60} = 1.67 \text{ ohms} \]

\[ C_{out} = 180 \text{ pF at 125 MHz} \]

5.2 CIRCUIT SCHEMATIC

5.3 TEST RESULTS
118-136 MHz amplifier (see Fig. 37) before coil adjustment.

Acknowledgements:
The author is indebted to Mr. T. O'Neal for the fruitful discussions held with him. Mr. O'Neal designed the circuit shown in Figure 37; Mr. J. Hennet constructed and tested the lab model.

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    München, Oldenburg 1951
VIDEO AMPLIFIER DESIGN:
KNOW YOUR PICTURE TUBE REQUIREMENTS

Prepared by:
Steve Tainsky,
Applications Engineering

This note describes video amplifier design considerations for unitized gun and conventional picture tubes. Some unique design techniques are discussed taking advantage of Motorola's MC1323 chroma demodulator. Finally, design objectives of video amplifiers are discussed.
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INTRODUCTION

The advent of the unitized gun picture tube brought with it many claims of superior performance over the conventional delta gun configurations. Among these advantages were: improved gray scale tracking, better spot size and improved highlight resolution. These advancements were made possible because of the better grid-to-cathode cutoff ratios between guns. Although the combined gun structure (common G1 and G2 for all three guns) improved the grid-cathode cutoff ratio between guns, it now required the video amplifier output stage to compensate for any remaining differences in individual gun cutoffs. Thus, a simplification of the picture tube has resulted in a complication of the video stages driving it.

The video systems described in this note were designed to alleviate the design compromises normally associated with driving a unitized gun picture tube. These include interaction between driver and cutoff control, high power dissipation needed to obtain bandwidth, setup adjustment, dc stability and supply ripple rejection. Some of the designs can also be employed in conjunction with a conventional picture tube as very high-quality, wide-bandwidth, video systems.

BIASING REQUIREMENTS OF UNITIZED GUN TUBE

Cutoff characteristics for a typical unitized gun picture tube are presented in Figure 1. The two solid lines represent the spread in electron gun spot cutoff for all tubes. This variation is shown to be a ratio of 1.8-to-1 in G1-to-cathode voltage for any given G2 voltage. This ratio is greatly reduced for electron guns within a given tube to 1.2-to-1, as depicted by Tube A or Tube B. The shaded area marked Tube A shows the range of cutoff voltage for the three guns, assuming the one gun is a worst-case for maximum spot cutoff. Similarly, the shaded area marked Tube B shows the range of cutoff voltages assuming it contains a gun which is a worst-case for a minimum spot cutoff gun. The important point to be obtained from these curves is that the range of adjustment required by the video output stages to adjust spot cutoff will be the 1.2-to-1 ratio for any tube. For example, if it is desired to use a 150 Volt G1-to-cathode voltage, then a 25 Volt adjustment range is required. Notice the same range is required for Tube A as for Tube B, the only difference being the required G2 voltage. Thus, the large variation expected in cutoff ratios between tubes can be compensated for by adjusting the G2s.

FIGURE 1

The cutoff ratio between guns in a given tube are compensated for by adjusting the cathode voltages. This method has the added advantage of using higher G2 voltages on tubes which do not have high cutoffs and thus obtain improved spot size. If, on the other hand, all tubes were biased at a fixed G2 of 420 Volts and the video amplifier used to compensate for cutoffs over the 1.8-to-1 ratio, the spot size on all tubes would be degraded to the worst-case condition. Also, in this case, the requirements on the video amplifier are more demanding.

Drive characteristic curves (Figure 2) show that with a cutoff of 150 Volts grid-to-cathode, a peak beam current of 6 mA per gun is possible. A gun with a 125 Volt EGK1 will still deliver 5 mA of peak current. Average current is limited between 1.0 and 3.0 mA, depending on the sys-
tern, by the Automatic Brightness Limiter (ABL) circuit to prevent damage to the picture tube. The high peak-to-average beam currents are necessary to reproduce peak whites and produce good highlight resolution.

To help design a video amplifier output stage consistent with the above requirements, it is useful to show the cathode and grid voltage on a diagram, as in Figure 3a. The G1 voltage should be selected as low as possible to keep the video output stage supply voltage low. This minimizes the power dissipation and voltage breakdown requirements of the video output devices. A lower limit on the G1 voltage is imposed by the saturation knee at high frequencies of the output stage. A common problem associated with setting the G1s too close to the saturation voltage of the output stage is color bleeding on luminance transients when accompanied by high color saturation levels. This problem manifests itself when the color sideband signals addition to the luminance in the output stage causes the luminance transients of one gun to be at a different level than the other gun, causing output stage saturation as shown in Figure 3b. Unitized gun tubes tend to exhibit this phenomenon, even without color drive, since the same effect is obtained when biasing the output stages at different black levels to compensate for the spot cutoffs of the guns. The effect of this can be avoided by: 1) picking the G1 voltage sufficiently above the saturation knee of the output devices, and 2) selection of a high
enough $E_{GK}$ such that each gun has the capability of supplying enough anode current before being driven into grid conduction. As can be seen by referring back to Figure 2, for a 150 Volt $E_{GK}$, a peak-anode current of 6 mA per gun can be obtained, even in the case of the 125 Volt $E_{GK}$ (other gun in same tube) a peak current of 5 mA is obtainable. Note also that the gun with the lower $E_{GK}$ will require less video drive to produce the same amount of peak-anode current. This tends to compensate for the effect of the color bleeding discussed above, provided the high $E_{GK}$ gun has the required peak current capability.

In Figure 3a, a GI voltage of 40 Volts and a corresponding black level voltage of 190 Volts for the design example was used. A video drive (Figure 2) of 120 Volts will guarantee a minimum of 3.5 mA peak-anode current per gun. The average video drive required for a 1.5 mA anode current (0.5 mA per gun) will be approximately 55 Volts. It is good design practice to allow enough dynamic range to be able to handle overshoots of 25%.

VIDEO AMPLIFIER REQUIREMENTS

The requirements for video output stages for unitized gun picture tube should include the following:

a) Bandwidth should be at least 3.5 MHz, either with or without peaking components. If peaking components are used, they should be common to all three outputs so that no differential peaking occurs due to tolerances on these components. Layout should be symmetrical so that stray capacitances do not cause differential peaking, and radiation between stages is minimized. The large signal rise time should be less than 150 ns and the differential rise time should be limited to 20 ns.

b) DC voltage stability of the cathodes should be maintained to < 6 Volts, and differential voltage drifts between cathodes caused by temperature and aging effects should be limited to < 2 Volts.

c) A low overall output stage gain is desirable to minimize bias drifts. Ideally, the gain should be sufficient to provide the required drive to the cathode with the signal available from the demodulator. The gain should be adjustable over a 30% range without affecting the black level voltage. Bandwidth and rise time changes caused by gain adjustment should be consistent with the above requirements.

d) Each output should have a black level adjustment sufficient to cover the range required by the variation in picture tube gun spot cutoffs (25 Volts). In addition, the dc coupled outputs from the chroma demodulator can vary over a 2–3 Volt range giving a 7.2 Volt variation in cathode voltage. If a demodulator device with a luminance/brightness input is used (MC1323 or MC1324), this cathode voltage variation can be reduced to 15 Volts (0.6 x 24). Thus, the black level adjustment control must accommodate at least a 40 Volt range and should not have any significant effects on gain or output stage bandwidth.

e) The transfer characteristics should be linear and independent of operating point and cutoff adjustment within the usable range (from black level to 0 Volts $E_{GK}$).

f) In order to maintain signal integrity, the rejection to power supply ripple should be maintained at > 40 dB down from output signal. To obtain this, it is sufficient to either: 1) filter and regulate the power supply, or 2) design video output stages which have the required rejection to power supply modulation, or 3) a combination of both, to obtain the desired objective. Also note that the sensitivity of the output stages to power supply voltage should not cause more variation than the limits set for dc stability.

BRUTE FORCE APPROACH TO OBTAIN DESIGN OBJECTIVES

To begin the discussion, it is convenient to analyze a circuit for driving a unitized gun picture tube as illustrated in Figure 4. The design chosen requires operation with a 220 Volt B+ and a voltage gain of 24 to supply a 120 Volt drive with 5 volts of signal from the demodulator. As noted earlier, black level voltage of 190 Volts with a 40 Volt range on black level adjustment is required. Equations for the design of this circuit are included.

As can be seen from the equations, any modulation on the 220 Volt supply will appear directly at the cathode. Also, modulation on the 24 Volt supply (or tolerance) is coupled to the cathode via the resistor connecting the cutoff adjustment potentiometer to the emitter of the output stage. Even with the low 6.8 kΩ collector load (high power dissipation), the 3 dB bandwidth of this stage, working into the 10 pF load is less than 2.5 MHz. Therefore, peaking components must be used in order to obtain the required 3.5 MHz bandwidth.

Select load resistor $R_L = 6.8 \text{k} \Omega$ (assuming maximum power dissipation of Q1 is 1.6 Watts).

Maximum Gain $= R_L/R_E \geq 6.8 \text{k} \Omega/270$ Select $R_E$ and $= 25.2 \ast I_B << I_E$

Minimum Gain $= R_L(R_E + R_{drive})$ desired max $= 6.8 \text{k} \Omega/(270 + 81) = 19.4$ and min gain

requirements.

For a black level voltage of 190 Volts

$I_C = (V_{CC} - V_C)/R_L = (220 - 190)/6.8 \text{k} \Omega = 4.41 \text{mA}$

For 40 Volt black level adjustment range

$\Delta I_C = \Delta V_C/R_L = 40/6.8 \text{k} \Omega = 5.88 \text{mA}$

assuming $\Delta I_C \approx \Delta I_E$ and $\Delta I_E$ is to be obtained via cutoff control from 24 Volts.

$R_{EI} = 24/\Delta I_C \approx 24/\Delta I_E \approx 24/5.88 \approx 4 \text{k} \Omega$

Quiescent dc voltage at demodulator output adjusted to 15

* Closest gain resulting from standard component values.
Volts on R-Y output via set-up adjustment.

\[ V_{B1} = 15 \text{ Vdc (for small) and } V_{E1} = 14.3 \text{ Vdc} \]

For Q1 on and \( V_{BE} = .7 \text{ Vdc} \)

\[ I_{E1} = \frac{(24 - V_{E})}{R_E} = 2.43 \text{ mA} \]

(Note: if wiper is grounded \( I_{E1} = (0 - V_{E})/R_E = -3.58 \).

\[ \Delta I_{E1} = 2.43 - (-3.58) = 5.98 \text{ mA (as predicted).} \]

\[ I_{E1} \approx I_{E1} + I_c \approx 4.41 + 2.43 \approx 6.84 \text{ mA assuming } I_c \ll I_E \]

Maximum Gain (drive control arm connected to emitter of video driver)

\[ V_{E1} - V_{E2} = I_E R_E = (6.84 \text{ mA}) (270) = 1.85 \]

\[ V_{E2} = V_{E1} - I_E R_E = 14.3 - 1.85 = 12.5 \]

\[ V_{E2} = V_{E2} - V_{BE2} = 12.5 - 0.7 = 11.8 \]

Bias network on base of video driver \( V_{B2} \) should be adjusted for 11.8 Vdc.

Minimum Gain (drive control arm connected to top of bridge resistor, R)

To prevent dc shift at cathode with drive control, maintain \( I_E \approx 6.84 \text{ mA} \). Select \( R \) such that 6.84 mA will result in 12.5 Volts at "V".

\[ R = \frac{12.5/6.84 \text{ mA}}{} \approx 1.8 \text{ k} \Omega \]

\[ I_E' = \frac{(V - V_{E2})}{R_{drive\ control}} = \frac{(12.5 - 12.5)}{81} = 0 \]

& \[ I_E = I + I_E' = 6.84 + 0 = 6.84 \text{ mA} \]

It should be emphasized that a demodulator with ability to set dc output must be used. A very serious drawback of this circuit is the inability to handle the variations in dc output voltage from one demodulator to the next. Typically, absolute output levels on demodulators vary 3 Volts from unit-to-unit, which would result in a 72 Volt tolerance at the cathode (3 Volts x gain of output stage). To correct this problem, a demodulator with a luminance input is employed and a potentiometer is used to adjust the quiescent output voltage to the required 15 Volts. An additional output variation between any two outputs to 0.6 Vdc can exist on a given demodulator. This variation, as previously discussed, can be compensated for at the cathode by the cutoff control, and at the expense of range on those controls. The 0.6 Volt offset also has the adverse effect of unbalancing the drive control bridge, thereby producing interaction between drive and cutoff controls. Motorola now has an MC1323 triple chroma demodulator with individually adjustable dc outputs, thus eliminating the need to compensate for the 0.6 Volt delta between outputs with the output stage. The range on control of the MC1323 dc outputs is also sufficient to compensate for picture tube cutoff variations.

25 Volts

gain of output stage = 1 Volt, thus eliminating the need for cutoff controls on the output stages. Refer to Application Note AN-763 for complete details on MC1323.

A quick computer analysis (using the Motorola Spice Circuit analysis program) of this basic circuit will aid in determining how well it meets design objectives. The model used and input documentation for this analysis is...
shown in Figure 5a. The computed node voltages, supply currents, transistor operating point, and element sensitivity chart are included in Figure 5b. The sensitivities are expressed in volts per unit (change in output voltage for a one unit change in element value) and volts per percent (change in output voltage for a one percent change in element value). This table will help in selecting tolerances on components as well as setting requirements for our 220 Volt power supply. For example, if our minimum (low contrast) output signal is 60 V(p-p), and we desire a power supply ripple rejection of > 40 dB in our output signal, the output ripple must be < 0.6 V(p-p). The $V_s$ supply sensitivity results in a 1 Volt change in output voltage for a 1 Volt change in supply, thus the $V_s$ supply...
ripple must be < 0.6 Volts. The sensitivity of the V24 supply is 1.63 Volts per Volt, requiring a ripple of < 0.6/1.63 or 0.37 V(p-p) to maintain signal integrity. The absolute value of the supplies must be regulated against line and load, due to the high sensitivity.

The computed dc transfer characteristics are shown in Figure 5c for minimum and maximum cutoff settings. Notice that in each case the solid and dotted lines are parallel, illustrating that the cutoff adjustment does not change the gain. Also, the solid and dotted lines cross at black level, indicating the gain adjustment does not affect the cutoff. The range of cutoff adjustment from the curves is 192 Volts minus 153 Volts, or 39 Volts. The gain control range varies from a maximum of 23.4 (slope of solid lines) to a minimum of 17.9 (slope of dotted lines). It is always reassuring to compare these computed results with those of the initial design.

The computed response curves for both the luminance and chroma sideband signals are shown in Figure 5d. The discrepancy in dc gain is caused by the voltage divider formed by RE1 and RE when driving from the luminance input, but which does not attenuate the chroma sideband signal. This effect is minimal as long as RE1 >> RE. In both cases, the effective emitter resistance is the parallel
summing input capability and performance characteristics generally independent of the amplifier parameters. Unfortunately, operational amplifiers are not suited for 250 Volt operation with 150 Volt swing capability. The objective here is to use components normally used in video output stages, arrange them in a high gain configuration (pseudo operational amplifier) and apply operational amplifier theory to take advantage of the above mentioned characteristics.

In its simplest form, the pseudo operational amplifier of the improved video system is shown in Figure 6a. The voltage gain of this section is very high and can be shown to be $A_V = \frac{R_L}{R_E + r_E}$ where $r_E = 26 \text{ mV/\mu}A$ at room temperatures. With the values shown $A_V = 435$.

If the above figure is redrawn in operational amplifier configuration, it can be utilized as a summing amplifier. By selecting the ratio of $R_F$ to $R_{in}$ the gain to each input can be individually selected.
Replacing V1 with the luminance signal Y1 and V2 with the demodulated R-Y chroma sideband signals will result in the required matrix for red, required to drive the red cathode.

Two other similar stages are used to obtain the blue and green outputs respectively. The third input V3 is used to establish the black level voltage at V0, which is connected to the picture tube cathodes. As can be seen from Equation 2 in Figure 6b, the dc voltage at V0 can be changed by varying Rin(3) with a dc reference voltage substituted for V3. Also the gain to V1 and V2 can be ganged together by the use of a common variable resistor in their signal path. Figure 6c illustrates these modifications.

Substituting some typical values in Figure 6c, gain, dc output voltage and output impedance can be calculated. Refer to Figure 6d for values.

**FIGURE 6c**

**FIGURE 6d**
Assuming sources V1 and V2 are ac ground and therefore do not contribute a dc current in RV, the output voltage is established by current II, flowing in RF. Therefore, II is equal to Vref/Rin(3) = 10.2/5.1 kΩ = 2.0 mA. This current results in a 182 Volts developed across RF (2.0 mA x 91 kΩ) and is the output voltage Vo1. Note that this voltage is independent of both the amplifier gain and the supply voltage. The luminance and chroma gain is defined by RF/Rin or (RF/Rin) x Rin/(Rin + 2 Ry) and is 25.3 and 17.5 respectively for maximum and minimum setting of gain adjustment RV. Output impedance may be calculated, using the Equation R0 = l + IA where R0 is the output resistance without feedback. Substituting into this equation yields R0 of 1.36 kΩ where R0 = 10 kΩ, A = 435 and B = REQ/RF. Where REQ is effective input resistance with RV = 0.

The effect of this low output resistance working into a 10 pF capacitive load (output capacity of transistor plus picture tube cathode capacity plus stray of wire from output stage to picture tube) gives a bandwidth well in excess of the 4 MHz required. This gives the advantage of not needing to peak the low level video amplifiers to compensate for frequency roll-off in the video output stage. It is also easier to produce high-frequency peaking which will give narrower overshoots and a crisper picture. This circuit can also be used in monitors where as much as 10 MHz of bandwidth may be required.

![Figure 6e](image)

Figure 6e reverts from the "fictional world" of the operational amplifier to reality. The reference input voltage to the output amplifier is elevated from zero to 10.2 Volts via the zener diode the voltage drop across the 10 Ohm resistor, and the two VBE drops of the darlington output. The reference voltage connected to Rin(3) becomes ground and the same current will flow as in Figure 6d. The output voltage is the 182 Volt drop across RF plus the 10.2 Volts at the input or 192.2 Volts. The output voltage can be varied by inserting a variable resistor in series with Rin(3). This will have the effect of decreasing II with increasing resistance and therefore decreasing the voltage across RF yielding decreasing Vo1 from the predetermined value of 192.2 Volts. Note that this has no effect on the gain of the stage nor will the gain have any effect on the dc output voltage if V1 and V2 are referenced to 10.2 Volts so no dc current can flow in RV.

The MC1323 triple chroma demodulator incorporates a unique power supply which enables the setting of V1 dc, or no signal output voltage, to precisely 10.2 Volts without the use of a "setup" potentiometer. Basically, as shown in Figure 6f, the dc output of the MC1323 is set 1.6 Volts above the voltage applied to Terminal 14 by referencing the three demodulator loads back to Pin 15. (See MC1323 data sheet for complete description of power supply operation.) Using the 8.8 Volt zener diode as a reference to the MC1323 power supply (Pin 14), the demodulated R-Y, B-Y and G-Y signals will be referenced 1.6 Volts above the zener. In practice, the two VBE voltage drops plus the drop across the 10-Ohm resistor will be approximately 1.6 Volts so the bridge voltage will be 10.4 Volts. (This ensures that no dc current will flow through the 3.6 kΩ and RV resistors.)

An alternative scheme for providing the 10.2 Volts at the output of the MC1323 is to connect the demodulator load resistor back to Pin 16. In this case, the dc voltage at the demodulator outputs will be precisely the same as that applied to Pin 14 (dc applied must be low impedance). Pin 14 voltage can be obtained via a voltage divider between the zener and the regulated supply. This method has the added advantage of allowing the designer to establish external to the MC1323, the voltage required for the VBE drops of the transistors being used. It also eliminates the tolerance introduced by the demodulator for this offset. An even more effective scheme would be to utilize a PNP small-signal driver in the output stage instead of the NPN driver. This would eliminate the need to provide an offset voltage across the MC1323 and give temperature compensation as an added benefit.

Two other features of the MC1323 enabling it to operate in conjunction with this "operational amplifier output stage" are low output impedance and the ability to filter the outputs at relatively high impedance levels prior to the emitter-follower output. This reduces the amount of subcarrier (due to switching pair unbalance in the demodulator) present at the input to the wideband amplifier.

A computer analysis of the operational amplifier output stage is a good vehicle for appreciation of its operation. Figure 7a shows the circuit, with the documentation required by the analysis program. In this model only one input, the luminance, is considered because the response to the chroma sidebands will be identical due to the cir-
FIGURE 6f

FIGURE 7a

VIDEO
V24 0 5 24
V220 0 10 DC 520
V1 0 9 AC 1 DC 10.1192
V0 0 3 DC 10.1192
V2 0 0 DC 3.6
PH1 9 7 3.6H
PH2 8 7 3.6H
PHV 7 6 1
PH3 6 0 5.1H
PF 1 6 91k
PE1 4 0 7.5H
PE 2 3 10
PL 10 1 10k
O1 1 4 2 PNP
O2 5 6 4 IC
.DEV PNP NPN BF=40 CJE=30P CJC=10P
.DEV IC NPN
.OUTPUT V1 V(1.0)V PRI MA PH DC
circuit symmetry. Figure 7b shows the dc operating point, power supply currents, transistor operating points and small-signal transfer function. The dc component of VL and VC were obtained by first running the analysis program with RY = 1 MΩ, and then using the computed node 6 voltage for VL and VC. This insures that at the operating point, no current will flow in Rin(1) and Rin(2). The value of RY was then adjusted back to one Ohm and the analysis of Figure 7b resulted. Note that some of the calculation presented earlier will yield slightly different results than those of the computer analysis. These differences result from the assumption that the output stage was a perfect operational amplifier. The computer analysis does show, however, that only small errors resulted from the approximations and that this is a very useful video output stage. (The major cause of the discrepancies is the change in input voltage at Pin 6 due to VBE changes with IC in the output transistor. Note that the effect of this becomes small as the output stage current increases.)

The sensitivity of the output dc voltage to element values is tabulated in Figure 7c. Comparison of these values with those computed for the previous circuit show a significant decrease in power supply sensitivity. Stable resistors with similar temperature coefficient should be used to minimize output drift. The absolute value is not critical as Rin(3) will have a variable resistor in series with it for black level adjustment. Sensitivity to the zener is somewhat compensated for by the black level adjustment.
The analysis was repeated for $R_{\text{in}}(3)$ equal to 6.6 kΩ and the node voltages, transistor operating points, etc., are tabulated in the computer printout in Figure 7d. Comparison of the data for the two different values of $R_{\text{in}}(3)$ shows a change in gain $V_{1}/V_{L}$ at the operating point. This is a result of the low current in the output transistor in the case of $R_{\text{in}}(3) = 5.1$ kΩ. As the signal $V_{L}$ is applied and current increases in the output stage, the gain will increase to the same value as that shown for $R_{\text{in}}(3) = 6.6$ kΩ. This effect is indicated in Figure 7e, which represents the transfer characteristic of the amplifier for the two values of $R_{\text{in}}(3)$. The data used to plot these curves along with the small-signal gain and impedance levels are presented in Figure 7f. The lower gain at low-current levels, again represent the departure of the configuration used from a true operational amplifier. The voltage gain is decreasing and the gain is no longer a function of the ratio of the resistors. This effect and the decrease in sensitivity to supply voltage is explained as follows: $g_{m} = I_{E}/26\, mV$ at room temperature increases with increasing $I_{E}$. Both lower output voltage and/or higher supply voltage will cause an increase in $I_{E}$. The increase in $I_{E}$ causes the voltage sensitivity at the base of Q1 to decrease $(g_{m} = \Delta I_{E}/\Delta V_{BE}$ or $\Delta V_{BE} = \Delta I_{E}/g_{m})$ consequently, reflecting a decrease in sensitivity at the base of Q2 and finally at the output after being multiplied by the ratio of the feedback resistors. The supply voltage can be raised above 220 Volts to improve gain linearity and decrease supply sensitivity. $R_{\text{in}}(1)$ and $R_{\text{in}}(2)$ have current flowing in them due to the increased voltage at the base of Q2 causing their sensitivities to increase from the previous computer run in which $R_{\text{in}}(3) = 5.1$ kΩ. Not, however, that the sensitivities are still quite small.

A computer analysis of the frequency response of this stage substantiates the claims previously made for it. Figure 7g shows the effects of gain and bias point variation on the frequency response. The capacitor C is included to show that the feedback resistor cannot be chosen arbitrarily high, in order to minimize current through the load resistor required for the feedback. The end-to-end capacity of a 1/2-Watt resistor is 0.4 pF worst-case. The 91 kΩ resistor used will cause a transmission zero to occur at $f = 1/2\pi RC)$ 4.4 MHz. Higher values of $R_{F}$ will bring the zero into the video passband. Smaller values of C will yield response curves somewhere between the limits shown. The computer data is tabulated in Figure 7h.

It is important to note that the $C_{CB}$ of the small-signal driver transistor is not in parallel with $R_{F}$ but is reflected as a capacity to ground because of the common collector configuration. Appendix A indicates the small-signal current gain transfer characteristics for the model used for the output transistor. The purpose for including this material is twofold: a) to justify that the model used accurately predicts the response characteristics of a typical high-voltage transistor used for output stages in TV receivers and, b) to compare with the results of the response shown in Figure 7g.

A sweep response of this amplifier was performed in the laboratory and the results are shown in Figure 7i, with a 10 kHz and 1 MHz square wave response. Notice that...
both the rise and fall times of the square wave are < 100 ns without peaking components used. Some of the values
used in the actual circuit are slightly different from the
previously calculated in order to satisfy the requirements of a
particular chassis. The variations will not cause any signif-
ificant differences in results. As a comparison, Figure 7d is
included to show the response of a "standard" output
stage. As can be seen, the response even with peaking does
not have sufficient bandwidth for a high-grade system and
peaking in the low-level video amplifier is normally em-
ployed to compensate for the output stage roll-off.
**FIGURE 7e**

**VIDEO 2**

**DC TRANSFER CURVES**

| Luminance Input | $R_{in(1)} = 5.1\ k\ 
| $R_V = 1\ \Omega$ | $R_{in(3)} = 5.1\ k\ 
| $R_V = 800$ | $R_{in(3)} = 6.6\ k\ 
| $R_V = 800$ | $R_{in(3)} = 6.6\ k\ 
| $R_V = 1\ \Omega$ |
|---|---|---|---|
| VL | V1 | V1 | V1 |
| 8.00E 00 | 1.992E 02 | 1.992E 02 | 1.386E 02 | 1.386E 02 |
| 9.00E 00 | 1.992E 02 | 1.992E 02 | 1.732E 02 | 1.732E 02 |
| 1.00E 01 | 1.940E 02 | 1.935E 02 | 1.573E 02 | 1.573E 02 |
| 1.10E 01 | 1.734E 02 | 1.787E 02 | 1.412E 02 | 1.412E 02 |
| 1.20E 01 | 1.512E 02 | 1.631E 02 | 1.250E 02 | 1.250E 02 |
| 1.30E 01 | 1.285E 02 | 1.471E 02 | 1.038E 02 | 1.038E 02 |
| 1.40E 01 | 1.052E 02 | 1.311E 02 | 9.248E 01 | 9.248E 01 |
| 1.50E 01 | 8.277E 01 | 1.149E 02 | 7.617E 01 | 7.617E 01 |
| 1.60E 01 | 6.975E 01 | 9.877E 01 | 5.993E 01 | 5.993E 01 |
| 1.70E 01 | 5.774E 01 | 8.256E 01 | 4.348E 01 | 4.348E 01 |
| 1.80E 01 | 4.666E 01 | 6.632E 01 | 2.712E 01 | 2.712E 01 |
| 1.90E 01 | 3.615E 00 | 5.006E 01 | 1.074E 01 | 1.074E 01 |
| 2.00E 01 | 2.817E 00 | 3.378E 01 | 9.146E 00 | 9.146E 00 |
| 2.10E 01 | 2.135E 00 | 1.749E 01 | 7.251E 00 | 7.251E 00 |
| 2.20E 01 | 9.535E 00 | 9.105E 00 | 3.366E 00 | 3.366E 00 |

**SMALL SIGNAL CHARACTERISTICS**

| V1 / VL | -1.923E 01 | -1.402E 01 | -1.603E 01 | -2.255E 01 |

**OUTPUT IMPEDANCE**

| AT V1 | 2.151E 03 | 1.757E 03 | 2.541E 03 | 9.668E 03 |

**INPUT IMPEDANCE**

| AT VL | 3.940E 03 | 4.484E 03 | 4.356E 03 | 3.753E 03 |

**FIGURE 7f**

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Hybrid P1 Small Signal Parameters of Q1 (From Computer Readout)

<table>
<thead>
<tr>
<th>Condition</th>
<th>IE</th>
<th>GM</th>
<th>RPI</th>
<th>CPI</th>
<th>CMU</th>
<th>$h_{fe}$</th>
<th>$f_T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{in(3)} = 5.1 \text{ k}$</td>
<td>0.89 mA</td>
<td>31.8 mmho</td>
<td>1.26 k</td>
<td>39.7 pF</td>
<td>0.738 pF</td>
<td>40</td>
<td>125 MHz</td>
</tr>
<tr>
<td>$R_{in(3)} = 6.6 \text{ k}$</td>
<td>4.85 mA</td>
<td>183 mmho</td>
<td>219 Ω</td>
<td>40.4 pF</td>
<td>0.872 pF</td>
<td>40</td>
<td>70.6 MHz</td>
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FIGURE 7g

136
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FIGURE 7a

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</table>

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Figure 7i

100 kHz Squarewave Response
A. 5 µs/Div  B. 0.1 µs/Div  10 V/Div

1 MHz Squarewave Response
Output 10 V/Div, Input 0.5 V/Div, 0.1 µs/Div

FIGURE 7i
Standard Circuit Used For Comparison With Other Circuits

Low Level Video Amplifier

Output (No Peaking Components)
Uncompensated Response

Input (Injected Sweep @ PNP Base)

Output (With Peaking Components)
Fully Compensated Response

100 kHz Square Wave Response

1 MHz Square Wave Response
ANOTHER NOVEL APPROACH

Motorola's European Division has developed an output stage for the European market which has all the properties of our preceding discussion plus some added advantage and trade-offs. The basic configuration again uses a pseudo operational amplifier configuration as shown in Figure 8a. Here, an emitter-follower output is used (instead of the darlington), thus allowing a large load resistor on Q1, providing both high-voltage gain and low-output impedance. One very interesting property of this design is that it can be made to draw a constant current from the power supply if $R_L$ and $R_F$ are the same value. This becomes apparent if one assumes the input is approximately at ground and the output is at supply. Q2 (ignore base current) collector current is determined by $R_F$ ($V_{supply}/R_F$) and a Q1 is cut-off. However, if the output is at ground, Q1 must be saturated and current is determined by $R_L$ ($V_{supply}/R_L$) and Q2 is cut-off. This feature, plus the fact that the output voltage is independent of supply voltage (apparent from previous discussions) makes the power supply requirement virtually nil.

Another advantage is the low power dissipation of each device due to the large load resistors. Of course, both devices must be capable of $V_{CEO}$ breakdowns in excess of the maximum supply voltage. This circuit was built using the Motorola BF393 (MPS-A42) transistor without heatsinking. This is a high-voltage, low-capacitance, TO-92, 650-mW device.

A practical circuit using this configuration is shown in Figure 8b. The equation for output voltage and gain are included in Figure 8b. The diode D1 provides a pulldown capability using Q1 as a current sink while driving capacitive loads at high slew rates. This is necessary since Q1 turning on tends to cut Q2 off when Q2 is driving a capacitive load. (Remember, output impedance of this configuration is low only while the amplifier is active.) Slowing in the opposite direction is no problem because the capacitive load tends to turn Q2 on harder as its base voltage increases during Q1 turnoff. During small-signal operation, the voltage across D1 is zero, due to the drop across D2 and the base-emitter drop of Q2, and therefore, no current will flow in it. The non-linearity introduced by the diodes in transition from small-signal to large-signal operation is greatly reduced by the large amount of feedback. With the values shown, the worst-case power dissipation per transistor is 312 mW.

The analysis of this stage will not be analyzed here because of its similarity to the preceding stage. The measured response and rise times are shown in Figure 8c for comparison with the other configurations. Note, the rolloff in the response which is caused by Q1 collector capacity, Q2 base capacity and stray working against the 47 kΩ load resistor of Q1. A 3 pF total effective capacity at that point will give a break frequency of 1.12 MHz. Lower value resistors may be used at the expense of transistor dissipation and power supply current required to extend bandwidth. The lack of voltage feedback at this internal point makes it susceptible to the transistor parameters and strays. This circuit offers excellent performance with minimal demand on supply and transistors and should prove to be a very advantageous circuit. Peaking in either the low-level video or splitting $R_{in}$ (Figure 8b) and introducing a pole in the response at 1.12 MHz will yield 3 dB bandwidth in excess of 5 MHz. Total supply current per stage is 5.3 mA at a supply of 250 Volts. Variation of dc output voltage with a supply range of 200-250 Volts is 1.5 Volts, or less than 3%.
2 V/Div

Sweep 0-6 MHz
Markers 3, 3.6, 4, 4.5 MHz

10 V/Div

Motorola
BF393
650 mW Device

100 kHz Square Wave Response
A. 5 μA/Div  B. 0.1 μA/Div  10 V/Div

1 MHz Square Wave Response
Output 10 V/Div, Input 0.5 V/Div, Y/Div 0.1 μV/Div

FIGURE 8c
The use of this output stage and the stages previously discussed will be covered in the next section. Although the previous configuration will be shown, everything described will apply to this output stage as well. As has already been perceived, this stage is also able to sum the chrominance signal by adding another input resistor.

THE SYSTEM

The circuit shown in Figure 6f is reproduced in Figure 9a for convenience. This circuit will be used as a vehicle for describing some system considerations because it is already familiar to the reader.

The luminance signal voltage source V1 is opened during black level adjustment, or picture tube gun cutoff, via service switch S1. This guarantees that no current flows in R_Y during setup, assuming the voltage between Pin 14 and Pin 6 compensates for two V BE drops plus the drop across the 10 Ω resistor. Under this condition, the 5.1 kΩ resistor and cutoff adjustment R determines the current in the feedback resistor R_F and therefore the output voltage. For a conventional picture tube, R would not be needed as the screen grids could be used to adjust spot cutoff of each gun. The procedure for setting up a unitized gun tube would be as follows: 1) Set R equal to zero Ohms in all three output amplifiers. 2) Adjust screen control bias (all three screens common) until all guns are turned off. (Last color just extinguished.) 3) Increase value of R in each output stage independently until each gun turns on. As value of R is increased, current I is decreasing, causing a corresponding decrease in voltage across R_F and thereby reducing V_0.

As a final step in completing the setup procedure, service switch S1 is closed, applying the luminance signal to the output stage. To ensure not having R_Y (gain control for adjusting color temperature) change gun cutoffs, it is only necessary to ensure the black reference level of the video signal (V1) be shifted through 10.2 Volts, via the brightness control in the low-level video amplifier. This guarantees that no current will flow in R_Y at black level. A low-impedance drive source for V1 also eliminates drive control interaction and chroma matrixing.

Figure 9b is a schematic of the entire system as described with the addition of an MC1396 video amplifier. The features of this amplifier include dc contrast and brightness, dc restorer for black level clamping, ganged contrast and color gain controls and ABL. Use of the 8.8 Volt zener as a reference for the MC1396 ensures (as mentioned earlier) that the brightness control has enough dynamic range to vary black level through 10.2 Volts. Note also the zener reference is filtered before it is used as a reference voltage for the MC1323. This is necessitated due to the dynamic impedance of the zener diode during the blanking interval causing a pulse to appear on the reference line.
FIGURE 9b - Video System

NOTE:
Pin 4, 9, 12 Reference inputs on MC1323 Not Shown.
Pin 3 Chroma Input Not Shown

Used to Match Vcc Drops on Output Transistors
It is beyond the scope of this paper to go into any detail on the TBA396. More information may be obtained by contacting the Consumer Applications Department.

Another important consideration in the design of video systems is to maintain enough dynamic range in the output stages to prevent black "wash-out." This phenomenon occurs when either the output stage or the low-level video amplifier cuts off, at or below the required cathode voltage required for picture tube gun cutoff. In Figure 9b, the 11 k\(\Omega\) emitter resistor (connected to service switch) serves to prevent this problem. Assume that the service switch was just closed, and a particular dc voltage had been established on each cathode prior to closing. Also assume that the brightness control is turned down such that the video driver transistor base-emitter junction is reversed biased. The input voltage to the three video output amplifiers always remains at 10.2 Volts, therefore the common 11 k\(\Omega\) resistor to ground in series with each 3.6 k\(\Omega\) resistor causes an additional 0.27 mA to flow in each output stage feedback resistor \(R_f\). This causes a 24.5 Volt increase in \(V_0\) from the black level voltage, guaranteeing cutoff. The resulting voltage on top of the 11 k\(\Omega\) resistor due to the 0.27 mA from each output stage is 8.9 Volts. As the brightness control is now turned up, the drive transistor starts to conduct at 8.9 Volts at the emitter, well below the black level voltage of 10.2 Volts, thus ensuring that both the output and low-level video amplifiers are active and linear at black level.

**SUMMARY**

This note has discussed the unitized gun picture tube and has made comparisons with conventional tubes. The drive requirements for the unitized gun tube were established and several approaches to handle these requirements were suggested. The particular video output design chosen will be a function of many factors which must be considered during the design cycle such as quality, cost effectiveness, hot/cold chassis, regulated chassis and many others. The information presented in this note should aid the designer in selecting the appropriate video system to satisfy his design objectives.
APPENDIX
SMALL-SIGNAL CURRENT GAIN TRANSFER CHARACTERISTICS

TRANSISTOR RESPONSE
PART LIST

** RESISTORS **

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<tr>
<th>NAME</th>
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<th>TO</th>
<th>MINIMUM</th>
<th>NOMINAL</th>
<th>MAXIMUM</th>
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** INDEPENDENT CURRENT SOURCES **

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<th>PHASE</th>
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** INDEPENDENT VOLTAGE SOURCES **

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** BIPOLAR JUNCTION TRANSISTORS **

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DEVICE NAME = PWR
TYPE = NPN

PARAMETER VALUE

| BF   | 4.000E+01 |
| BR   | 1.000E+00 |
| RB   | 0.000E+00 |
| RC   | 0.000E+00 |
| RE   | 0.000E+00 |
| CCS  | 2.000E-12 |
| TF   | 0.000E+00 |
| TR   | 0.000E+00 |
| CJE  | 3.000E-11 |
| CJC  | 1.000E-11 |
| IS   | 1.000E-14 |
| PE   | 1.000E+00 |
| PC   | 1.000E+00 |
| VA   | 0.000E+00 |
| EG   | 1.110E+00 |
$V_S = 20$ Volts

TRANSISTOR RESPONSE
SMALL SIGNAL BIAS SOLUTION

TEMPERATURE 27,000 DEG C

ITERATIONS = 6

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE
(1) 0.6548 (2) 20.0000 (3) 19.9990

VOLTAGE SOURCE CURRENTS

NAME CURRENT

$V_S$ 1.000E-03 AMPS

TOTAL POWER DISSIPATION 2.00E-02 WATTS

TRANSISTOR OPERATING POINTS

NAME MODEL IB IC VBE VBC VCE BETADC
01 PWR 2.51E-05 1.00E-03 0.655 -19.344 19.999 40.0

$V_S = 190$ Volts

TRANSISTOR RESPONSE
SMALL SIGNAL PARAMETERS

TEMPERATURE 27,000 DEG C

TRANSISTORS

NAME GM RPI PD CPI CMU BETADC FT
01 3.87E-02 1.03E 03 2.59E 12 3.93E-11 2.22E-12 40.0 1.46E 08
A general discussion for broadband drivers and their requirements for linear operation. Design examples are given using Motorola plastic transistors and high-gain hybrid modules designed for operation in the 1.0 to 250 MHz range. The amplifiers range in power gain from 25 to 55 dB and are capable of driving power amplifiers to levels up to several hundred watts.
GENERAL CONSIDERATION

Two of the most important factors to be considered in broadband linear amplifier design are the distortion and the output harmonic rejection.

The major cause for intermodulation distortion is amplitude nonlinearity in the active element. The nonlinearity generates harmonics, and the fundamental odd-order products are defined as $2f_1-f_2$, $2f_2-f_1$, $3f_2-2f_2$, $3f_2-2f_1$, etc., when a two-tone test signal is used. These harmonics may not always appear in the amplifier output due to filtering and cancellation effects, but are generated within the active device. The amplitude and harmonic distortion cannot really be distinguished, except in a case of a cascaded system, where even-order products in each stage can produce odd-order products through mixing processes that fall in the fundamental region. This, combined with phase distortion—which in practical circuits is more apparent at higher frequencies—can make the distortion analysis extremely difficult; whereas, if only amplitude distortion was present, the effect of IMD in each stage could easily be calculated.

In order to expect a low harmonic output of the power amplifier, it is also important for the driving source to be harmonic-free. This is difficult in a four-octave bandwidth system, even at 10–20 watt power levels. Class A biasing helps the situation, and Class A push-pull yields even better results due to the automatic rejection of even harmonics.

Depending on the application, a full Class A system is not always feasible because of its low efficiency. The theoretical maximum is 50%, but practical figures are not higher than 25% to 35%. It is sometimes advantageous to select a bias point somewhere between Class AB and A which would give sufficiently good results, since filtering is required in the power amplifier output in most instances anyway.

In order to withstand the high level of steady dc bias current, Class A requires a much larger transistor die than Class B or AB for a specific power output. There are sophisticated methods such as generating the bias voltage from rectified RF input power, making the dc bias proportional to the drive level. This also yields to a better efficiency.

20 W, 25 dB AMPLIFIER
WITH LOW-COST PLASTIC DEVICES

The amplifier described here provides a total power gain of about 25 dB, and the construction technique allows the use of inexpensive components throughout. The plastic RF power transistors, MRF475 and MRF476, featured in this amplifier, were initially developed for the CB market. The high manufacturing volume of these TO-220 packaged parts makes them ideal for applications up to 50 MHz, where low cost is an important factor.

The MRF476 is specified as a 3-watt device and the MRF475 has an output power of 12 watts. Both are extremely tolerant to overdrive and load mismatches, even under CW conditions. Typical IMD numbers are better than -35 dB, and power gains are 18 dB and 12 dB, respectively, at 30 MHz.

The collectors of the transistors are electrically connected to the TO-220 package mounting tab which must be isolated from the ground with proper mounting hardware (TO-220 AB) or by floating heat dissipators. The latter method, employing Thermalloy 6107 and 6106 heat dissipators, was adapted for this design. Without an airflow, the 6106 and 6107 provide sufficient heat sinking for about 30% duty cycle in the CW mode. Collector idle currents of 20 mA are recommended for both devices, but they were increased to 100 mA for the MRF475 and to 40 mA for the MRF476 to reduce the higher order IMD products and to achieve better harmonic suppression.

Biasing and Feedback

The biasing is achieved with the well-known clamping diode arrangement (Figure 2). Each stage has its own diode, resistor, and bypass network, and the diodes are mounted between the heat dissipators, being in physical contact with them for temperature-tracking purposes. A better thermal contact is achieved through the use of silicone grease in these junctions.
The bias currents of each stage are individually adjustable with R5 and R6. Capacitors C4 and C10 function as audio-frequency bypasses to further reduce the source impedance at the frequencies of modulation.

This biasing arrangement is only practical in low and medium power amplifiers, since the minimum current required through the diode must exceed $I_c/h_{fe}$.

Gain leveling across the band is achieved with simple RC networks in series with the bases, in conjunction with negative feedback. The amplitude of the out-of-phase voltages at the bases is inversely proportional to the frequency as a result of the series inductance in the feedback loop and the increasing input impedance of the transistors at low frequencies. Conversely, the negative feedback lowers the effective input impedance presented to the source (not the input impedance of the device itself) and with proper voltage slope would equalize it. With this technique, it is possible to maintain an input VSWR of 1:5:1 or less from 1.6 to 30 MHz.

**Impedance Matching and Transformers**

Matching of the input and output impedances to 50 ohms, as well as the interstage matching, is accomplished with broadband transformers (Figures 3 and 4).

**FIGURE 2**

Normally only impedance ratios such as 1:1, 4:1, 9:1, etc., are possible with this technique, where the low-impedance winding consists of metal tubes, through which an appropriate number of turns of wire is threaded to form the high-impedance winding. To improve the broadband characteristics, the winding inductance is increased with magnetic material. An advantage of this design is its suitability for large-quantity manufacturing, but it is difficult to find low-loss ferrites with sufficiently high permeabilities for applications where the physical size must be kept small and impedance levels are relatively high. Problems were encountered especially with the output transformer design, where an inductance of 4 µH minimum is required in the one-turn winding across the collectors, when the load impedance is

$$\frac{2(V_{CE} - V_{CE_{sat}})^2}{P_{out}} = \frac{2(13.6 - 2.5)^2}{20} = 12.3 \text{ ohms.}$$

Ferrites having sufficiently low-loss factors at 30 MHz range only up to 800—1000 in permeability and the inductance is limited to 2.5—3.0 µH in the physical size required. This would also limit the operation to approximately 4 MHz, below which excessive harmonics are
Examples of broadband transformers. Variations of these are used in all designs of this article (see text). All ferrites in transformers are Fair-A lite Products Corp.:±2643006301 ferrite beads.* The turns ratios shown in Figure 4 are imaginary and do not necessarily lead to correct design practices.

generated and the efficiency will degrade. One possible solution is to increase the number of turns, either by using the metal tubes for only part of the windings as in Figure 4B, or simply by winding the two sets of
windings randomly through ferrite sleeves or a series of beads (Figures 3C and 4C). In the latter, the metal tubes
can be disregarded or can be used only for mounting purposes. T3 was eventually replaced with a transformer of this type, although not shown in Figure 1.

Below approximately 100 MHz, the input impedances of devices of the size of MRF475 and smaller are usually capacitive in reactance, and the \( R_s \) is much smaller than the \( R_s \) (Low Q). For practical purposes, we can then use the formula \( \sqrt{R_s^2 + X_s^2} \) to find the actual input impedance of the device. The data-sheet numbers for 30 MHz are 4.5, -j2.4 ohms, and we get \( \sqrt{4.5^2 + 2.4^2} = 5.1 \) ohms. The base-to-base impedance in a push-pull circuit would be four times the base-to-emitter impedance of one transistor. However, in Class AB, where the base-emitter junction is forward biased and the conduction angle is increased, the impedance becomes closer to twice that of one device. The rounded number of 11 ohms must then be matched to the driver output. The drive power required with the 10 dB specified minimum gain is

\[
P_{\text{OUT}}/\log^{-1}(G_{\text{PE}}/10) = 2.0 \text{ W}
\]

and the driver output impedance using the previous formula is \( 2(11.1^2)/2 = 123 \) ohms. The 11 ohms in series with the gain-leveling networks (C8, R8 and C9, R11) is 17 ohms. The closest practical transformer for this interface would be one with 9:1 impedance ratio. This would present a higher-than-calculated load impedance to the driver collectors, and for the best linearity the output load

should be lower than required for the optimum gain and efficiency. Considering that the device input impedance increases at lower frequencies, a better overall match is possible with a 4:1, especially since the negative feedback is limited to only 4 dB at 2 MHz due to its effect on the efficiency and linearity.

The maximum amount of feedback a circuit can tolerate depends much on the physical layout, the parasitic inductances, and impedance levels, since they determine the phase errors in the loop. Thus, in general, the high-level stages should operate with lower feedback than the low-level stages.

The maximum amount of feedback the low-level driver can tolerate without noticeable deterioration in IMD is about 12 dB. This makes the total 16 dB, but from the data sheets we find that the combined gain variation for both devices from 2 to 30 MHz is around 29 dB. The difference, or 13 dB, should be handled by the gain-leveling networks.

The input impedance of the MRF476 is 7.55, -j0.65 ohms at 30 MHz resulting in the base-to-base impedance of 2 \( \times \sqrt{(7.55^2 + 0.65^2)} = 15.2 \) ohms. This, in series with networks R1, C1 and R4, C3 (2 \( \times \) 4.4 ohms), gives 24 ohms, and would require a 2:1 impedance ratio transformer for a 50-ohm interface. However, due to the influence of strong negative feedback in this stage, a better overall matching is possible with 4:1 ratio. The input networks were designed in a manner similar to that described in Reference 8.

* Wallkill, N.Y. 12589
Measurements and Performance Data

At a power output of 20 W CW, all output harmonics were measured about 30 dB or more below the fundamental, except for the third harmonic which was only attenuated 17 dB to 18 dB at frequencies below 5 MHz. Typical numbers for the higher order distortion products (d9 and d11) are in the order of -60 dB above 7 MHz and -50 dB to -55 dB at the lower frequencies. These both can be substantially reduced by increasing the idle currents, but larger heat sinks would be necessary to accommodate the increased dissipation.

The efficiency shown in Figure 6 represents the overall figure for both stages. Currents through the bias networks, which are $82/(13.6 - 0.7) = 0.16$ A each, are excluded. Modified values for R5 and R6 may have to be selected, depending on the forward voltage characteristics of D1 and D2.

Although this amplifier was designed to serve as a 1.6 to 30 MHz broadband driver, it is suitable for the citizens band use as well. With some modifications and design shortcuts, the optimization can be concentrated to one frequency.

**FIGURE 5**
Component Layout Diagram of Low-Cost 20 W Amplifier
The leads of R7 and R12 form the one-turn feedback windings in T2 and T3. Ferrite beads in dc line can be seen located under T1 and T2.

**FIGURE 6**
Intermodulation distortion and power gain versus frequency (upper curves).
Input VSWR and combined collector efficiency of both stages (lower curves).
20 W, 55 dB HIGH PERFORMANCE DRIVER
12-Volt Version

The second amplifier employs the MHW591 hybrid module to drive a pair of larger devices which can be operated Class A or AB, depending on the requirements. Transistors such as MRF449 and MRF455 are recommended for Class A and MRF433 for Class AB operation. A 24–28 volt version with MHW592 and a pair of MRF401s was also designed, and some of the test data will be presented. For Class A, the power parts should be replaced with MRF426s.*

These amplifiers are a good example of how a good gain flatness can be achieved across the four-octave band, with simple RC input networks and negative feedback, while maintaining a reasonable input VSWR.

The MHW591 is employed as a predriver in this unit. The MHW591 and its counterpart, MHW592, were developed for low-level SSB driver applications from 1.0 MHz to 250 MHz. The Class A operation results in a steady-state current drain of approximately 0.32 A, which does not vary with the signal level. At an output level of 600 mW PEP, the IMD is typically better than -40 dB, which can be considered sufficiently good for most purposes. Since the power gain is specified as 36.5 dB, the maximum drive level for the 600 mW output is 0.13 mW, or -9 dB. For the final power output of 20 W, a power gain of 15.2 dB minimum is required at the highest operating frequency for the power transistors. A good, inexpensive device for this is the MRF433, which has a 20 dB minimum gain and -30 dB IMD specification at an output level of 12.5 W PEP. The push-pull configuration, due to inconsistent ground planes and broadbanding due to matching compromises usually results in 2 dB to 3 dB gain losses from figures measured in a test fixture. Assuming a transistor power gain of 18 dB, the total will be 54.5 dB, representing an input power of -11 dB. Later measurements, however, indicated a gain of 56 dB (+0.5 dB) at the specified power output, making the input level around -13 dB.

![FIGURE 7](image)

**Biassing and Feedback**

The bias circuit employed with this amplifier is basically similar to the one described earlier, with the exception of having an emitter follower output. A second diode in series with the one normally seen with the clamping diode method compensates for the voltage drop in the base-emitter junction of the emitter follower, Q1 (Figure 8). The minimum current through D1 and D2 is (\(I_c/\overline{h_{fe}}\)\) (Q2 + Q3)/\(\overline{h_{fe}}\)(Q1), and in this case (2.5/40)/40 = 1.5 mA. Typical \(h_{fe}\) for the MRF433 is 40, and with the devices biased to 200 mA each, the standby base current is 10 mA. In operation the load current of Q1 then varies between 10 and 62 mA. A Case 77 transistor exhibiting low variations in base-emitter saturation voltage over this current range is MJE240. Base-emitter saturation voltage determines the bias source impedance, which should not exceed approximately 0.3 ohm, representing a 20 mV variation in voltage from idle to full drive conditions. If source impedance exceeds 0.3 ohms, a capacitor of 500 - 1000 µF should be connected from the emitter of Q1 to ground.

The peak dissipation of Q2 is under one watt, making it possible to mount the transistor directly to the circuit board without requiring any additional heat sinking. Diodes D1 and D2 are located on the lower side of the board, near Q2 and Q3 (Figure 9). The leads are formed to allow the diodes to come into contact with the transistor flanges. The thermal contact achieved in this manner is not the best possible, even when the gaps are filled with silicone compound, but the thermal time constant is lower than with most other methods. Both diodes are used for temperature tracking, although the voltage drop of only one is required to compensate for the \(V_{FE}\) forward drop of Q1. The advantages of this circuit are simplicity, low standby current drain, and ease of adjustment with a small trimpot.

The voltages for the negative feedback are derived separately from the collectors of Q2 and Q3 through L6, R6 and L7, R7. Capacitors C5 and C6 are used for decoupling. Because of the high RF voltage levels on the collectors, this method is only feasible in low- and medium-power amplifiers. At higher power levels, the power-handling requirements for the series resistors (Figure 8), which must be noninductive, become impractical. A feedback voltage source with lower impedance must be provided in such cases.

The MRF433 has a higher figure of merit (emitter periphery/base area) than the MRF475, for example. This results in smaller differences in power gain per given bandwidth, since the device is operating farther away from the 6 dB/octave slope. Disregarding the package inductances, which affect the \(Q\), the higher figure of merit makes such devices more suitable for broadband operation. The 2 MHz to 30 MHz \(\Delta G_{PE}\) of the MRF433 is 8 dB, which is divided equally between the negative feedback and the leveling networks C3, R4 and C4, R5. The 2 MHz and 30 MHz impedance values are 9.1, -j3.5 and 2.5, -j2.2 ohms, respectively, although the 2 MHz values are not given in the data sheet.

At 30 MHz we can first determine what type of transformer is needed for the 50-ohm input interface. The effective transformer load impedance is \(2\sqrt{(2.5^2 + 2.2^2) + (2.4^2)}\) ohms (leveling networks) = 11.5 ohms, which indicates that a 4:1 impedance ratio is the closest possible (see Figures 3B, 4A, and 8). These values are accurate for practical purposes, but they are not exact, since part of the capacitive reactance in C3 and C4 will be cancelled, depending on the transformer characteristics.

*To be introduced.
The output matching is done with a transformer similar to that described in the first part of this paper (Figures 4B, 4C). This transformer employs a multi-turn primary, which can be provided with a center tap for the collector dc feed. In addition to a higher primary inductance, more effective coupling between the two transformer halves is obtained, which is important regarding the even-order harmonic suppression.

28-Volt Version

A 28-V version of this unit has also been designed with the MHW592 and a pair of MRF401s. The only major change required is the output transformer, which should have a 1:1 impedance ratio in this case. The transformer consists of six turns of RG-196 coaxial cable wound on an Indiana General F-627-8-Q1 toroid. Each end of the braid is connected to the collector, and the inner conductor forms the secondary. A connection is made in the center of the braid (three turns from each end) to form the center tap and dc feed.

The MRF433 and MRF401 have almost similar input characteristics, and no changes are necessary in the input circuit, except for the series feedback resistors, which should be 68—82 ohms and 1 W.

In designing the gain-leveling networks, another approach can be taken, which does not involve the computer program described in Reference 8. Although the input VSWR is not optimized, it has proved to give satisfactory results.

The amount of negative feedback is difficult to determine, as it depends on the device type and size and the physical circuit layout. The operating voltage has a minimal effect on the transistor input characteristics, which are more determined by the electrical size of the die. High-power transistors have lower input impedances and higher capacitances, and phase errors are more likely to occur due to circuit inductances.

Since the input capacitance is an indication of electrical size of the device, we can take the paralleled value \( X_p \) at 2 MHz, which is \( X_2 + (R_3^2/X_2) \) and for MRF433 \( 3.5 + (9.1^2/3.5) = 27 \) ohms. The \( X_p \) of the largest devices available today is around 10 ohms at 30 MHz, and experience has shown that the maximum feedback should be limited to about 5 dB in such case. Using these figures...
as constants, and assuming the GPE is at least 10 dB, we can estimate the amount of feedback as: \[ \frac{5}{10^2/27} + 5 = 6.35 \text{ dB} \], although only 4 dB was necessary in this design due to the low \( \Delta \text{GPE} \) of the devices.

The series base resistors (R4 and R5) can be calculated for 4 dB loss as follows:

\[
\left[ \frac{(V_{\text{in}} \times 4\text{dB}) - V_{\text{in}}}{I_{\text{in}}} \right] = \left[ \frac{(0.79 \times 1.58) - 0.79}{0.04} \right] = 11.45 \text{ ohms, or} \\
11.45/2 = 5.72 \text{ ohms each.}
\]

\[ Z_{\text{in}}(2 \text{ MHz}) = \sqrt{9.1^2 + 3.5^2} = 9.75 \text{ ohms, in Class AB push-pull 19.5 ohms.} \]

\[ P_{\text{in}} = 20 \text{ W} - 28 \text{ dB} = 20/630 = 0.032 \text{ W} \]

\[ V_{\text{RMS}} \text{ (base to base)} = \sqrt{0.032 \times 19.5} = 0.79 \text{ V} \]

\[ I_{\text{in}} = V_{\text{in}}/R_{\text{in}} = 0.79/19.5 = 0.04 \text{ A} \]

\[ \Delta V_{4 \text{ dB}} = \sqrt{\log_{10}(4/10)} = 1.58 \text{ V} \]

The parallel capacitors (C3 and C4) should be selected to resonate with R (5.7 ohms) somewhere in the mid-band. At 15 MHz, out of the standard values, 1800 pF appears to be the closest, having a negligible reactance at 2 MHz, and 2.8 ohms at 30 MHz, where most of the capacitive reactance is cancelled by the transformer winding inductance.

**Measurements and Performance Data**

The output harmonic contents of this amplifier are substantially lower than normally seen in a Class AB system operating at this power level and having a 4.5-octave bandwidth. All harmonics except the third are attenuated more than 30 dB across the band. Between 20 and 30 MHz, -40 to -55 dB is typical. The third harmonic

![Graph](image-url)

**FIGURE 10**

Intermodulation Distortion and Power Gain versus Frequency (Upper Curves). Input VSWR and Collector Efficiency (excluding MHN591) (Lower Curves).

![Component Layout Diagram](image-url)

**FIGURE 9**

Component Layout Diagram of 20 W, 85 dB High-Performance Driver

The leads of D1 and D2 are bent to allow the diodes to contact the transistor mounting flanges.

Note that the mounting pad of Q1 must be connected to the lower side of the board through an eyelet or a plated through-hole.
has its highest amplitude (-20 to -22 dB), as can be expected, below 20 MHz. The measurements were done at an output level of 20 W CW and with 200 mA collector idle current per device. Increasing it to 400 mA improves these numbers by 3–4 dB, and also reduces the amplitudes of \( d_5 \), \( d_7 \), \( d_9 \), and \( d_{11} \) by an average of 10 dB, but at the cost of 2–3 dB higher \( d_3 \).

![FIGURE 11 – IMD versus Power Output](image)

**CONCLUSION**

The stability of both designs (excluding the 28 V unit) was tested into reactive loads using a setup described in Reference 8. Both were found to be stable into 5:1 load mismatch up to 7 MHz, 10:1 up to 30 MHz, except the latter design did not exhibit breakups even at 30:1 in the 20–30 MHz range. If the test is performed under two-tone conditions, where the power output varies from zero to maximum at the rate of the frequency difference, it is easy to see at once if instabilities occur at any power level.

The two-tone source employed in all tests consists of a pair of crystal oscillators, separated by 1 kHz, at each test frequency. The IMD \( (d_3) \) is typically -60 dB and the harmonics -70 dB when one oscillator is disconnected for CW measurements.

HP435 power meters were used with Anzac CH-130-4 and CD-920-4 directional couplers and appropriate attenuators. Other instruments included HP141T analyzer system and Tektronix 7704A oscilloscope-spectrum analyzer combination.

**REFERENCES**


7. Data Sheets, Motorola MRF475, MRF476, MRF433, and MHW591.

8. H. Grandberg, "Two-Stage 1 KW Solid-State Linear Amplifier," AN-758, Motorola Semiconductor Products Inc.

The PCB layouts below are a supplement to Figures 5 and 9 and may be used for generating printed circuit artwork.

FIGURE 12 – PCB Layout of Low-Cost 20W Amplifier (not full size)
FIGURE 13 – PCB Layout of Low-Cost 20W, 55dB High-Performance Driver (not full size)
A SIMPLIFIED APPROACH TO VHF POWER AMPLIFIER DESIGN

Prepared by
Helge O. Granberg
RF Circuits Engineering

This note discusses the design of 35-W and 75-W VHF linear amplifiers. The construction technique features printed inductors, the design theory of which is fully described. Complete constructional details, including a printed circuit layout, facilitate easy reproduction of the amplifiers.

Solid-state VHF amplifier design can be simplified by employing printed or etched lines for impedance matching. The lines, having a distant ground-plane reference and high $Z_0$, can be treated as lumped constant inductors, and make design and duplication easier than with wire-wound inductors.

An example is an optimized 35-W amplifier which yields over 10 dB of power gain across the 2-meter amateur band. It employs an inexpensive, non-internally matched transistor, the MRF240, which has good linear characteristics for SSB operation.

A higher power version with the same board layout is concentrated around the MRF247, although this results in some compromise in the impedance matching.

A carrier operated T/R switch (COR) is incorporated, allowing applications such as a booster amplifier for hand-held and mobile radios.

Both designs are biased class AB for linear operation, but are suitable for FM operation as well. Figure 1 shows the two amplifiers.

FIGURE 1 – 35-watt and 75-watt Engineering Models
GENERAL

VHF solid state amplifier design is almost exclusively done with lumped constant LC matching networks. Broadband transformer matching is feasible when extremely wide bandwidths are required. Transmission lines for impedance transformation usually require quarter-wave electrical lengths and make designs bulky at VHF unless materials with high dielectric constant are used. Transmission lines can be realized with coaxial cable or printed lines (strip-lines) on a circuit board with a continuous ground plane, separated by a suitable dielectric material. The printed lines discussed here are, in fact, high characteristic impedance transmission lines which, for the purposes of design calculation, are treated as inductors; therefore the quality of the board material is less critical. The printed lines also have the advantage of repeatability and easy access for designing multi-element networks. The network calculations can be done in the same manner as if lumped-constant, round-wire inductors were used.

Input and output impedance matching in transistor amplifiers is required to transform the source impedance (usually 50 ohms) to the low complex input impedance of the device. The output load impedance, which is a function of the supply voltage and power level, must also be matched to a 50-ohm load except in multistage designs.

At VHF, the input and output impedances of a power transistor are both usually inductive in reactance (designated as +JX in data sheets), becoming capacitive (−JX) at lower frequencies. For transistors such as MRF240, 2N6084 and 2N5591, the crossover point is around 100 MHz. This is determined by the transistor die size, geometry and package type, and smaller devices can be capacitive up to UHF frequencies.

Since the bandwidth required here is only a fraction of an octave, (140-150 MHz) the impedance matching can be adequately done with two section networks. In Figure 2, X1, which represents the +J input of the MRF240 transistor is not part of the external input matching network. C1 and C6 are dc blocking capacitors with measured parasitic inductances of close to 12 nH at the center frequency when the lead lengths are 0.1 inch.

These inductances, as well as the relay inductance, are added to the values of L1 and L5.

If the relay were used in a 50-ohm system, it would result in 0.3 dB power loss due to impedance mismatch and losses. This can be minimized if the relay inductance is used as part of a resonant circuit, but the series inductance (37 nH per contact pair) obviously places an upper frequency limit.

The simplest approach to matching network design is with a purely resistive source and load. This can be accomplished by compensating the +J with an equal amount of capacitance (−J). C3 and C4 are used to accomplish the compensation in Figure 2. This is not always practical, however, especially when maximum bandwidths are required. In this case, only part of the inductive component may be cancelled, leaving the base and collector still inductively reactive. In either case, it may be considered that part of the impedance-matching occurs within the device package itself; this is more obvious with internally matched devices, which are discussed later.

35-W LINEAR AMPLIFIER

The MRF240 was chosen for this application due to its ruggedness against load mismatch and inherently high power gain for a non-externally matched device. The transistor is rated for an output power of 40 W and a power gain of 8 dB at 175 MHz. A typical power gain at 145 MHz is 10 to 11 dB. At this frequency the input and output impedances of the MRF240 are 0.6 +J 0.8 ohms and 2.0 +J 0.1 ohms respectively (Pout = 35 W).

Before designing the matching networks, the values of C3 and C4 must be established to cancel the inductive reactance components at the base and the collector. For the input, the series numbers 0.6 +J 0.8 must be converted to parallel equivalent values, either by using a Smith chart or equations in references 3 and 4. The resulting equivalent values are: Rp = 1.67 ohms, Xp = 1.25 ohms or 880 pF. All capacitors have a series inductive reactance component, normally called parasitic inductance. It could be only a fraction of a microhenry, but at VHF its effect is large enough to be taken into consideration. The para-
sistic inductance results in an increased effective value of capacitance, and is frequency and impedance-level dependent.

The unencapsulated mica capacitors, widely used in VHF power applications, range from 1 to 2 nH in parasitic inductance for a single plate type, (up to 360 to 390 pF nominal values) depending on the mounting technique. Assuming a parasitic inductance of 1.5 nH, the equivalent low-frequency value can be calculated with Equation 1 as:

$$C_{\text{equiv}} = \frac{C}{1 + \left(\frac{2\pi f}{LC}\right)^2} \times 10^{-9}$$

where $C$ = effective capacitance required in pF
$L$ = parasitic inductance in nH
$f$ = frequency in MHz

Thus, for the required 880 pF, a capacitor of this type with equivalent low-frequency value of 420 pF, or the closest standard (390 pF), should be used.

Similarly, converting the output impedance ($2.0 + j0.1$ ohms) to parallel form, $R_p = 2.01$ ohms and $X_p = +j26.8$ ohms. The $X_C$ represents a capacitance value of 47 pF for $C_4$ (from Equation 2), or a 43 pF nominal value.

$$C = \left(\frac{1}{X_C}ight) \times 10^6$$

where $X_C$ = capacitive reactance in ohms
$C$ = capacitance in pF
$f$ = frequency in MHz

This high reactance in parallel with the low collector impedance had no noticeable effect and was completely omitted in later functional tests of the unit. It would be easy to see from a Smith chart that the resistive components of 1.67 ohms and 2.01 ohms remain unchanged, and can be treated as a purely resistive load and source for the matching network calculations.

At high frequencies the base-emitter impedance of the transistor die itself is always lower than the collector output impedance. With power devices, both can be only a fraction of an ohm. The input impedance is increased by the base and emitter bonding wire and package lead frame inductances, which are effectively in series with the transistor base (Figure 2, $X_1$ and $X_2$). The collector has normally much less series inductance since it is attached directly to the package bonding pad.

From this it can be seen that part of the matching network is actually built into the transistor package, and it is obvious that the amplifier bandwidth cannot be accurately determined by calculating the $Q$ values of the external matching networks. (See the discussion of a 75-W linear amplifier.)

As an approximation, the 3 dB bandwidth can be used to obtain a starting point. Assuming a 15 MHz bandwidth at ±1.5 dB is desired at 145 MHz center frequency, a loaded $Q$ of approximately 9 is required. For simplicity this number is applied to both input and output network design.

In Figure 2, $X_1$ and $X_2$ represent the inductive impedance component of the transistor and are shown only to give an idea of the transistor internal structure. The values of $L_1$, $L_2$ and $C_2$ can be obtained from the Appendix, or calculated by using Equation 3:

$$X_L = RLQ$$
$$X_C = Q + JB$$

where $R_S = $ source impedance
$R_L = $ load impedance

For $Q = 9$:

$$X_{L1} = R_S B = 50 \times 1.32 = 66 \text{ ohms}$$
$$X_{L2} = R_L Q = 1.67 \times 9 = 15 \text{ ohms}$$
$$X_{C2} = \frac{A}{Q + B} = \frac{137}{9 + 1.32} = 13.3 \text{ ohms}$$

$$A = 1.67 (1 + 9^2) = 137$$

$$B = \frac{\sqrt{A}}{R_S} = \frac{1.32}{50} = 1.32$$

Since

$$L = \left(\frac{X_L}{2\pi f}\right) \times 10^3$$

where

$$XL = \text{inductive reactance in ohms}$$
$$L = \text{inductance in nH}$$
$$f = \text{frequency in MHz}$$

we have from Equations 3 and 4:

$$L_1 = 73 \text{ nH}$$
$$L_2 = 16 \text{ nH}$$
$$C_2 = 82 \text{ pF}$$
Subtracting the relay inductance (37 nH) and the parasitic inductance of the blocking capacitor C3 (12 nH) from the total value of L1, L1' = 24 nH. This means the total printed line inductance must be L1' + L2 = 24 + 16 = 40 nH.

Calculating the values of the output network in a similar manner, the values for L4, L5 and C5 are obtained as 20 nH, 83 nH and 70 pF, respectively, and L5' becomes 34 nH.

The capacitors employed for C2 and C5 are of the same unencapsulated mica type as C3, but smaller in size, and their parasitic inductance is only about 1 nH. The equivalent values for C2 and C5 would then be 77 pF and 66 pF according to Equation 1. These are nonstandard values, and considering a 5% tolerance, a 68 pF marked value can be used for both.

Inductors L1, L2, L4 and L5 are comprised of etched lines on the circuit board. To determine their widths and lengths, the inductance of each line per unit length must be established. From the tables in the Reference section, it can be extrapolated that the inductance of #25 round wire is 24 nH per inch and #26 wire nearly 26 nH per inch. When a ground plane is 0.15 inch below, which in this case is the heat sink, and the side grounds are off an equal distance, the inductance is about one-half of this, which has been verified by measurement.

If the circuit board is made of 1-ounce, copper-clad material, (one ounce of copper per one square foot) the copper thickness is 1.4 mils. With a one mil solder plating, the total thickness is 2.4 mils, and a 100-mil-wide strip would be equivalent to a #26 round wire having a 240 square mil cross sectional area. Similarly, a 130-mil-wide strip would be equivalent to a #25 round wire with 312 square mil area. A wider line would have lower losses but would also be physically longer for a given inductance. As a compromise, a narrow line was used for the input in this design, and a wider line for the output, where the losses due to the high RF currents are more evident. Bends in the line have a minimal effect to the inductance compared to the presence of the ground plane.

From the above, the resulting inductances for the 100 mil and 130 mil lines are 13 nH per inch and 12 nH per inch, respectively. This means that for L1 + L2 a total length of 3.1 inches is required, and 4.4 inches for L4 + L5'. Then, for L2 = 16 nH, C2 should be located 1.3 inches from the transistor base along the input line. For L4 = 20 nH, C5 should be 1.6 inches from the collector along the output line. The Power Output and Efficiency vs. Power Input of the 35-W amplifier is shown in Figure 3.

**75-W LINEAR AMPLIFIER**

The MRF247 employed in this design is a version of the well-known MRF245, which has been reprocessed to improve the linear characteristics. It is a much larger device than the MRF240, resulting in lower input and output impedances. However, it employs internal base matching with a built-in MOS capacitor to bring the base impedance up to a level where external low loss matching networks can be realized.

In Figure 4 the dashed line encircles the specially designed T matching network, including the metal oxide capacitor X4. X1, X2, and X3 represent the bonding wires whose inductances can be varied by controlling the loop heights. This network will be part of the total matching network designed to match the transistor to function in a practical circuit.
The internal matching still leaves the input impedance inductively reactive.

The MRF247 input impedance under forward biased conditions (100 mA) is 0.45 +J 0.85 ohms at 145 MHz, which translates to 2.06 +J 1.08 ohms in parallel form. A capacitive reactance of -J 1.08 ohms is required for C₃. The nominal value equivalent value, using Equation 1, is obtained as 450 pF.

Since the remaining resistive component of the base impedance (2.06 ohms) is only slightly higher than that of the MRF240, only minor changes in the input matching network are necessary. When L₁ + L₂ is fixed, and only their ratio can be varied, the resulting Q will be lower for the increased R_L. If only L₁ + L₂ is known, the Q can be calculated with Equation 5 as:

\[ Q = \frac{4X_T^2 + (R_S/R_L + X_T^2/R_L - R_S)(R_S - R_L)^3/2X_T}{2(R_S - R_L)} \]  

(5)

where

- \( X_T = X_{L1} + X_{L2} \) or \( X_{L4} + X_{L5} \)
- \( R_S \) = source impedance
- \( R_L \) = load impedance

Therefore,

\[ Q = \sqrt{\frac{26244 + (1214 + 3185 - 50)(192)}{95.88}} - 162 \]

\[ Q = \frac{928 - 162}{95.88} = 7.99 \]

\[ Q = 8 \]

where

- \( X_T = X_{L1} + X_{L2} = 81 \) ohms
- \( R_S = 50 \) ohms
- \( R_L = 2.06 \) ohms

Then, with Equations 1, 2, 3 and 4, the values for L₁, L₂ and C₂ can be calculated as: L₁ = 71 nH, L₂ = 18 nH, C₂ = 63 pF (56 pF nearest standard). The position of C₂ will be approximately 1.6 inches from the transistor base. (See line inductance calculations in the discussion for the 35-watt amplifier.)

The measured output impedance of MRF247 is 0.65 +J 0.45 ohms, which is much lower and more reactive than the values shown for MRF240. The output matching must also be done with the existing total line inductance, (L₄ + L₅) and it can be expected that a higher factor of compromise in the output matching is evident regarding the network bandwidth.

The above impedance numbers convert to 0.96 ohms resistive and -J 1.39 ohms reactive in parallel form. Since -J 1.39 ohms = 790 pF, a nominal value of 400 pF (C₄) is required at the collector. To find the Q:

\[ X_T = 94 \text{ ohms (} X_{L4} + X_{L5} \) \]

\[ R_S = 0.96 \text{ ohms} \]

\[ R_L = 50 \text{ ohms} \]

Then:

\[ Q = 13.7 \text{ (Eq. 5), and:} \]

\[ L_4 = 13 \text{ ohms = 14 nH} \]

\[ L_5 = 81 \text{ ohms = 89 nH} \]

\[ C_5 = 11.8 \text{ ohms = 93 pF} \]

A practical value of 82-91 pF can be used for C₅, and it should be located 1.1 inches along the output line from the collector, to give the above inductance values for L₄ and L₅.

Although the output Q is higher than the value calculated earlier for the 40 W unit, the total bandwidth of this version is increased as shown in Figure 7. The input matching network is usually dominant in determining the total bandwidth since the impedance transformation required is greater than the output requires, although the output circuit also has secondary effect. The internal matching elements of the device further make the total
effective Q even lower than the calculated value, which in this case was 8. The higher output Q usually results in higher collector efficiency and better harmonic suppression, but at the same time the circulating RF currents will increase, resulting in higher overall circuit losses which is especially noticeable at increased power levels. These factors are difficult to determine without knowing all the internal transistor parameters.

**FIGURE 5 — Power Input vs. Power Output and Collector Efficiency of 75-W Amplifier**

CLASS AB BIASING AND OTHER CONSIDERATIONS

The biasing system, as seen in Figure 6, uses a forward biased transistor, $Q_2$, to provide a voltage source of 0.6 to 0.7 volts. When the collector is connected to the base, a second current path is formed, decreasing the base current according to the $h_{FE}$, and thus lowering the voltage drop across the base-emitter junction. In this manner the voltage drop can be adjusted by selecting the appropriate $h_{FE}$ for $Q_2$. For the 2N5190 series $h_{FE}$ is typically in the range of 80-100, although the minimum spec is 20-25.

Typical $h_{FE}$'s for the MRF240 and MRF247 are 50-60, and the worst case collector currents are around 4A and 9A respectively. The minimum base currents required, $I_{B}(Q_2)$ are 80 mA and 180 mA ($I_{C}/h_{FE}$).

$$R_2 = \frac{V_{CC} - V_{BE}(Q_2)}{I_{E}(Q_2)} = 160 \text{ ohms and 75 ohms.}$$

The bias, which should not exceed 50 mA for MRF240 and 150 mA for MRF247, can be further adjusted by varying the value of $R_2$, but the minimum $I_{B}(Q_2)$ should be maintained.

It should be noted that since $Q_2$ is attached to the heat sink for temperature tracking purposes, its collector must be electrically isolated from the ground. The anodized surface of the heat sink is normally sufficient, or a separate insulating washer can be employed.

The 0.3 dB relay insertion loss mentioned earlier amounts to a VSWR of 1.7:1. However, the reflected power is only 0.2% (VSWR = 1.1:1) in a straight-through mode (receive), indicating that most of the relay losses are due to contact resistance and the dielectric insula-

**FIGURE 6**

**PARTS LIST**

- $C_1, C_6, C_{13}$ - 1000 pF, 300 V dipped mica
- $C_2$ - 56 pF or 68 pF, see text
- $C_3, C_4$ - 390 pF or 470 pF, see text
- $C_5$ - 68 pF or 91 pF, see text
- $C_7$ - 1000 pF ceramic chip or small disc
- $C_9$ - .01 µF ceramic disc
- $C_{10}$ - 220 µF/6 V tantalum
- $C_{11}$ - 3 pF dipped mica
- $C_{12}$ - 10 µF/25 V tantalum
- $R_1$ - 10 ohms/3 W carbon
- $R_2$ - 120 to 200 ohms/3 W
- $R_3$ - 3.3K/3 W carbon
- $Q_1$ - see text
- $Q_3$ - 2N5190
- $Q_2$ - 2N4401
- $D_1$ - 1N914 or 1N4148
- $D_2$ - 1N4001
- $L_1, L_2, L_4, L_5$ - see text
- $L_3$ - 12AWG #16 enamelled wire, .041 I.D.
- $L_6$ - 10 µH, molded choke
- $L_7$ - .33-1.0 µH, molded choke
- $RL$ - Arrow M, NF2-12 or equivalent—OMRON, LZN2-UA-DC12 or equivalent
tion resistance, rather than impedance mismatch.

Both amplifier designs may be employed in FM applications without modification. The bias networks may be omitted and L6 connected to ground, which modifies the operation to Class C. The increased input impedance of the device operating class C results in increased input VSWR, but it will still remain less than 1.5:1 for the 145-150 MHz band.

The two amplifiers may be connected in cascade to provide a total power gain of around 20 dB; however, an attenuator of 4 to 6 dB is required between the two units to prevent overdrive of the MRF247. Since 10 to 20 watts will be dissipated in the attenuator, it cannot be built from discrete resistors. Most convenient, size and costwise, are the thin film attenuators such as those manufactured by Pyrofilm.

The COR circuit requires 400 to 500 mW for the relay to switch. At this drive level, without the attenuator, the second amplifier would already produce full power output.

The COR (Figure 5) incorporates one of the standard circuits popular with mobile add-on amplifiers. Part of the RF input signal is being rectified by D1. The dc turns on Q3 which activates the relay. L7 and R3 provide the bias for D1 and Q3, and D2 suppresses inductive transients produced by the relay coil inductance. A time constant for SSB operation is provided by C12, whose value can be changed according to individual requirements. For FM this capacitor can also be omitted along with the bias network.

The repeatability of these amplifiers has been proven by constructing more than half a dozen units. Capacitors C2 and C5 were simply located within the marked areas on the circuit board (see Figure 9 and the photograph). On these capacitors, 20% tolerances can be allowed, but this may result in adjustments of each individual unit for optimum performance.

References
2. Donald Kochen, Practical VHF and UHF Coil Winding Data, Ham Radio, April 1971
FIGURE 9 - Component Layout Diagram of 35W and 75W Amplifiers

- X DENOTES FEED THROUGH EYELETS OR PLATED THROUGH HOLES
- © DENOTES TERMINAL PINS
- ® DENOTES BOARD STANDOFFS
APPENDIX

This information was originally published in Motorola Application Note AN-267, "Matching Network Designs with Computer Solutions."

NETWORK D

The following is a computer solution for an RF "Tee" matching network.
Tuning is accomplished by using a variable capacitor for C1. Variable matching may also be accomplished by increasing XL2 and adding an equal amount of XC in series in the form of a variable capacitor.

TO DESIGN A NETWORK USING THE TABLES
1. Define Q, in column one, as XL1/R1.
2. For an R1 to be matched and a desired Q, read the reactances of the network components from the charts.
3. XL1' is equal to the quantity XL1 obtained from the tables plus |XCout|.
4. This completes the network.
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XL1
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1200
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1600
1800
2000
2200
2400

XLz

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85.16
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117.26
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153.3
163.55
173.21
182.35
191.05
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207.36
215.06
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491.17
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523.21
538.52
553.4
567.89
635.41
696.42
752.5
804.67
853.67
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944.06
986.15

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158.46
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171.71
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190.83
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218.04
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246.53
260.2
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323.84
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493.49
539.57
583.29
625
664.96
703.38

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810
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1125
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1800
2025
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2700

XL2
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75.5
98.99
117.9
134.16
148.66
161.88
174.07
185.47
196.21
206.4
216.1
225.39
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242.9
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493.46
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588.22
605.39
622.09
638.36
714.14
782.62
845.58
904.16
959.17
1011.19
1060.66
1107.93

R1

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I 46.91
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I 73.86
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116.49
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125.23
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137.97
142.12
146.22
I 150.28
154.3
162.23
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177.63
185.14
II 192.52
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213.98
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THE TECHNIQUE OF DIRECT PROGRAMMING
BY USING A TWO-MODULUS PRESCALER

INTRODUCTION
The MC12009, MC12011, or MC12013 can be used as part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase-Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter-divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase-locked loop divider. In addition to using either the MC12009, MC12011, or the MC12013 variable modulus prescaler, this system requires an MC12014 Counter Control Logic Function, together with suitable programmable counters (e.g., MC4016s or SN74LS716s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

DESIGN CONSIDERATIONS
The disadvantage of using a fixed modulus \((\div P)\) for frequency division in high-frequency phase-locked loops (PLL) is that it requires dividing the desired reference frequency by \(P\) also (desired reference frequency equals channel spacing).

The MC12009/11/13 are especially designed for use with a technique called “variable modulus prescaling”. This technique allows a simple MECL two-modulus prescaler to be controlled by a relatively slow MTTL programmer counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high-frequency prescaler.
The theory of “variable modulus prescaling” may be explained by considering the system shown in Figure 1. For the loop shown:

\[ f_{\text{out}} = N \cdot P \cdot f_{\text{ref}} \]  

(1)

**FIGURE 1 – FREQUENCY SYNTHESIS BY PRESCALING**

where \( P \) is fixed and \( N \) is variable. For a change of 1 in \( N \), the output frequency changes by \( P \cdot f_{\text{ref}} \). If \( f_{\text{ref}} \) equals the desired channel spacing, then only every \( P \) channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 2.

**FIGURE 2 – FREQUENCY SYNTHESIS BY PRESCALING**

\[ f_{\text{out}} = N \cdot f_{\text{ref}} \]

(2)

A \( \div P \) is placed in series with the desired channel spacing (frequency) to give a new reference frequency: channel spacing/\( P \).

Another solution is found by considering the defining equation (1) for \( f_{\text{out}} \) of Figure 1. From the equation it may be seen that only every \( P \) channel can be programmed simply, because \( N \) is always an integer. To obtain intermediate channels, \( P \) must be multiplied by an integer plus a fraction. This fraction would be of the form: \( A/P \). If \( N \) is defined to be an integer number, \( N_p \), plus a fraction, \( A/P \), \( N \) may be expressed as:

\[ N = N_p + A/P. \]

Substituting this expression for \( N \) in equation 1 gives:

\[ f_{\text{out}} = (N_p + A/P) \cdot P \cdot f_{\text{ref}} \]  

(2)

or:

\[ f_{\text{out}} = (N_p P + A) \cdot f_{\text{ref}} \]  

(3)

\[ f_{\text{out}} = N_p \cdot P \cdot f_{\text{ref}} + A \cdot f_{\text{ref}} \]  

(4)

Equation 4 shows that all channels can be obtained directly if \( N \) can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding \( \pm A/P \) to the coefficient of \( f_{\text{ref}} \), the equation becomes:

\[ f_{\text{out}} = (N_p \cdot P + A + A \cdot P - A \cdot P) \cdot f_{\text{ref}} \]  

(5)

Collecting terms and factoring gives:

\[ f_{\text{out}} = [(N_p - A) \cdot P + A \cdot (P + 1)] \cdot f_{\text{ref}} \]  

(6)

From equation 6 it becomes apparent that the fractional part of \( N \) can be synthesized by using a two-modulus counter \((P \text{ and } P + 1)\) and dividing by the upper modulus, \( A \) times, and the lower modulus \((N_p - A)\) times.

This equation (6) suggests the circuit configuration in Figure 3. The \( A \) counter shown must be the type that counts from the programmed state \((A)\) to the enable state, and remains in this state until divide by \( N_p \) is completed in the programmable counter.

In operation, the prescaler divides by \( P + 1 \), \( A \) times. For every \( P + 1 \) pulse into the prescaler, both the \( A \) counter and \( N_p \) counter are decremented by 1. The prescaler divides by \( P + 1 \) until the \( A \) counter reaches the zero state. At the end of \((P + 1) \cdot A \) pulses, the state of the \( N_p \) counter equals \((N_p - A)\). The modulus of the prescaler then changes to \( P \). The variable modulus counter divides by \( P \) until the remaining count, \((N_p - A)\) in the \( N_p \) counter, is decremented to zero. Finally, when this is completed, the \( A \) and \( N_p \) counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with \( P = 10 \). Equation 6 becomes:

\[ f_{\text{out}} = (A + 10 N_p) \cdot f_{\text{ref}} \]  

(7)

If \( N_p \) consists of 2 decades of counters then:

\[ N_p = 10 N_{p1} + N_{p0} \]

\( (N_{p1} \text{ is the most significant digit}) \)

and equation 7 becomes:
FIGURE 4  DIRECT PROGRAMMING UTILIZING
TWO-MODULUS PRESCALER

FIGURE 5 - WAVEFORMS FOR DIVIDE BY 43

FIGURE 6 - WAVEFORMS FOR DIVIDE BY 42

FIGURE 7 - WAVEFORMS FOR DIVIDE BY 44

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\[ f_{out} = (100Np1 + 10Np0 + A)f_{ref}. \]

To do variable modulus prescaling using the variable modulus prescalers (MC12009/11/13) and programmable divide by N counters (MC4016, MC4018) one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12013; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 4 shows the method of interconnecting the MC12013, MC12014, and MC4016 (or MC4018) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 4, consider division by 43. Division by 43 is done by programming \( Np1 = 0, Np0 = 4 \), and \( A = 3 \).

Waveforms for various points in the circuit are shown in Figure 5 for this division. From the waveforms it may be seen that the two-modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the \( Np \) counter to 3, and counter A to 2.

After 11 pulses, point \( A \) again goes high; the \( Np \) counter decrements to 2 and the A counter to 1. The "2" contained in the \( Np \) counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point \( A \) goes high again.

With this position transition at \( A \), the output \( f_{out} \) of the MC12014 goes low, the \( Np \) counter goes to 1, and the A counter goes to 0. The zero state of the A counter is detected by the MC12014, causing point \( B \) to go to 1 and changing the modulus of the MC12013 to 10 at the start of the cycle.

When \( f_{out} \) goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point \( A \) makes another positive transition. This positive transition causes \( f_{out} \) to return high, release the preset on the counter, and generates a pulse to clear the latch (return point \( B \) to 0).

After 10 pulses the cycle begins again (point \( B \) was high prior to point \( A \) going high). The number of input pulses that have occurred during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 6 and 7 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the \( Np \) counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 4 if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since \( Np \) is greater than \( A \) in most applications).

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 8 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A counter should not exceed the number of stages for the

**Figure 8 - Method of Interconnecting Counters**

- A Counter: \( A = 100A2 + 10A1 + A0 \)
- \( Np \) Counter: \( Np = 100Np2 + 10Np1 + Np0 \)
Np counters. As many counters as desired may be cascaded, as long as fan-in and fan-out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two-modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than \( P/(P + 1) \).

It can be shown that for a general case in which the moduli of the two-modulus prescaler are \( P \) and \( P + M \), equation 6 becomes:

\[
f_{\text{out}} = [(Np - A) P + A (P + M)] \cdot f_{\text{ref}}
\]

or

\[
f_{\text{out}} = \{Np \cdot P + M \cdot A\} \cdot f_{\text{ref}}.
\]  \( \text{(8)} \)

From equation 8 it may be seen that the upper modulus of the two-modulus prescaler has no effect on the Np counter, and that the number programmed in the A counter is simply multiplied by \( M \).

There is no one procedure which will always yield the best counter configuration for all possible applications. Each designer will develop his own special design for the counter portion of his PLL system.

**FIGURE 9 - DIRECT PROGRAMMING 100-200 MHz SYNTHESIZER IN 50 kHz STEPS**

*Used as Modulus Two Programmable Counter. Also could use MC4017.
APPLICATION OF THE
MC1374 TV MODULATOR

INTRODUCTION
The MC1374 was designed for use in applications where separate audio and composite video signals are available, which need to be converted to a high quality VHF television signal. It is ideally suited as an output device for subscription T.V. decoders, video disk and video tape players.

The MC1374 contains both FM and AM modulator and oscillator functions. The AM system is a basic multiplier combined with an integral balanced oscillator capable of over 100 MHz operation. Both multiplier signal inputs are brought out without internal bias, permitting flexibility of video dc level and polarity, and separate sound insertion. An external resistor value can be chosen to select video gain.

The FM oscillator/modulator is actually one circuit. It is, more accurately, a voltage-controlled oscillator, which exhibits a nearly linear output frequency versus input voltage characteristic for a wide deviation. This provides a good FM source with few and inexpensive external parts (no varactors). It has a frequency range of 1.4 to 14 MHz, and can typically produce a ±25 kHz modulated 4.5 MHz signal with about 0.6% total harmonic distortion.

The MC1374 can deliver nearly constant output amplitude from a supply voltage of 5.0 V to 12 Vdc. Typical current drain is about 12 mA. With 75Ω as the optionally selected source impedance, the open circuit RF output voltage is 170 mV p-p, more than sufficient to drive a vestigial side-band output filter and still provide the 3.0 mV RMS permitted by the FCC.
VIDEO MODULATOR (AM MODULATOR)

The AM modulator incorporated in this design is exactly the MC1596 except that the “upper quad” is already connected to a balanced oscillator drive source, and is therefore, not brought out. (See Figure 1.) All other “handles” are available for use. Access to both inputs enables the designer to keep video and intercarrier sound sources apart. Either input can be used for either signal, as circuit layout demands, but the arrangement shown is preferred to minimize interference between input signals and oscillator circuits, and to assure flexibility of video polarity and amplitude.

The input-output characteristic is shown in Figure 2, expressing output peak-to-peak carrier as a function of the difference voltage between the inputs, pin 11 and pin 1. This transfer function is extremely linear and basically reflects two simple operating rules:

1. When the inputs are equal, both Q10 and Q11 conduct $I_1 = 1.15 \text{ mA}$ each, established by internal current sources, Q8 and Q9. The output voltage is (theoretically) dc, and is $I_1 R_L$ below VCC.

2. As one of the inputs is lowered with respect to the other, the current in that input leg is transferred to the other side, in the amount of

$$\frac{\pm(V_{11} - V_1)}{R_G}$$

until both current sources feed only one side. ($R_G$ is the gain adjustment resistor between the input transistor emitters). At this input, the output voltage swings from VCC to $(V_{CC} - 2I_1 R_L)$, for a peak-to-peak RF output of $2I_1 R_L$. The conversion gain of the system is, therefore,

$$V_{out \text{ p-p}} = 2I_1 R_L = \frac{2R_L}{11 - V_1 I_1 R_G}$$

For a detailed explanation of the balanced modulator, see AN532.¹

---

¹ For a detailed explanation of the balanced modulator, see AN532.
The load resistor $R_L$ is usually 75 Ω to match a constant impedance filter and typical T.V. cable system. Other values are useable but a large value for $R_L$ will impose some limitation. This will be covered a little later under "Biasing the AM Section".

The gain resistor $R_G$ should be chosen in accordance with the available video amplitude. This will be covered in greater detail in the section on 920 kHz beat generation, but a good guideline would be to allow twice the dynamic range which would be anticipated from just the peak (sync level) video:

$$R_G = \frac{2 \text{ (peak video)}}{1.15 \text{ mA}}$$

While the theoretical range of input voltage and corresponding $R_G$ is quite wide, there are other considerations. At the upper end, the on-chip FM sound system can only deliver a maximum of about 500 mV p-p of 4.5 MHz to the AM modulator. This would imply a peak video of about 1.0 V maximum if standard broadcast picture-to-sound ratio is to be observed. At the lower end, the primary limitation is one of noise. In keeping with good practice, to assure that background noise is more than 60dB below standard white, the minimum peak (sync tip) video should be at least 0.25 volt.

Although the MC1374 is a state-of-the-art device with $f_t = 600$ MHz transistors, the application at 60 MHz is not totally free of difficulty. Small phase errors within the device begin to introduce substantial amounts of 2nd harmonic in the RF output. At 61.25 MHz, the 2nd harmonic is only 6 to 8dB below the maximum fundamental. Though this poses no real impairment of performance and would be ignored by a T.V. receiver's selectivity, it is disturbing in the lab work when trying to observe a modulation pattern, and it certainly would not meet FCC approval. For this reason a double pi low pass filter is shown in the test circuit of Figure 3 and works well for channel 3 and 4 lab work. For a fully commercial application, a vestigial sideband filter will be required. (The general form and approximate values are shown in Appendix I.) Since it is used to carefully truncate the lower AM sidebands, it must be exactly aligned to the particular channel.

**FIGURE 3 — AM SYSTEM TEST CIRCUIT**
THE AM OSCILLATOR

The AM oscillator can be used dependably to about 105 MHz. This goes well beyond the usual U.S. system channels 3 and 4 requirements (61.25 and 67.25 MHz), and is high enough to cover channels 1, 2 and 3 in Japan (91.25, 97.25 and 103.25). Remote electronic bandswitching and crystal control can be readily accommodated. Higher frequency operation, up to U.S. channel 7 (176.25 MHz) has been achieved, but is not recommended, due to problems with oscillator startup and unpredictable oscillator mode shifts. The oscillator requires only a parallel LC from pin 6 to pin 7 with simple provisions for connecting supply voltage. Over a very broad range of Q, the oscillator will operate stably and start dependably, but an operating Q of 10 to 20 is recommended as a compromise between parasitic tendencies and poor starting. It is best to keep the coil small and capacitance large to minimize the variation due to the IC capacitance. The capacitance added by the IC is approximately 4.0 pF, but can approach 6.0 pF with socket and wiring.

Unbalanced operation; i.e., pin 6 or 7 bypassed to ground, is not recommended. Although the oscillator will still run, and the modulator will produce a useable signal, this mode causes substantial base-band video feedthrough. The only reason for using the unbalanced tank would be simplification of bandswitching, but as Figure 4 shows, this can be accomplished just as economically without using the unbalanced method.

The oscillator frequency with respect to IC chip temperature is extremely well compensated. Performance of the channel 3 standard test circuit shows less than ±20 kHz total shift from 0°C to 50°C as shown in Figure 5. At higher temperatures the slope approaches 2.0 kHz/°C. Improvement in this region would require a temperature compensating tuning capacitor of the N75 family (75PPM negative), but note that many commercial designs only require 8.0 kHz/°C.

Oscillator supply voltage stability is also good, particularly toward the 12 V end, as shown in Figure 6. Operation near the low voltage end may require some supply regulation in stringent applications.

Crystal control is feasible using the circuit shown in Figure 7. The crystal is a 3rd overtone series type, used in series resonance. The L1, C2 resonance is adjusted well below the crystal frequency and is sufficiently tolerant to permit fixed values. A frequency shift versus temperature of less than 1.0 Hz/°C can be expected from this approach. The resistors Ra and Rb are to suppress parasitic resonances.
The circuit designer should be aware of the possibility of introducing carrier frequency shift in the AM system. Inattention to wiring and components on pins 1 and 11 can cause as much as 300 kHz shift in carrier (at 67 MHz) over the video input range. This appears to be caused by output RF being transmitted to components and wiring on the input pins. A careful layout can be expected to keep this shift below 10 kHz. Short leads are important everywhere in the AM system. If the video source impedance is low, pin 11 may be shunted by a small bypass (< 100 pF), further reducing the possibility of oscillator feedback. Oscillator may also be inadvertently coupled to the RF output, with the undesired effect of preventing a good null, or carrier rejection, when $V_{11} = V_1$. Reasonable care will yield carrier rejection ratios of 36 to 40 dB below sync tip level carrier.

**THE “920 BEAT” PROBLEM**

Non-linear devices cause signal mixing and intermodulation products. In television, one of the most serious concerns is the prevention of the intermodulation of color (3.58 MHz) and sound (4.5 MHz) frequencies, which causes a 920 kHz signal to appear in the spectrum. The concern is very great because this is a relatively “coarse” video frequency, with very high visibility. In fact, a level of “920” which is 54 dB below the picture carrier is considered to be at the threshold of perceptibility. Very little (3rd order) non-linearity is needed to cause this problem, and even though the MC1374 appears extremely linear, it does produce “920”. This is one of the most important considerations in choosing gain and signal input levels.

The most common test method used in the industry today for measuring “920” is to establish a reference sync level of video, then add 30% chroma and -12 dB of sound. This is usually interpreted to mean, for example:

- **Video reference = 1.0 V**
- **Chroma (3.58 MHz) = 300 mV p-p**
- **Sound (4.5 MHz) = 250 mV p-p**

A spectrum analyzer viewing the modulator output is first set up to 0 dB on the video reference. Then chroma and sound are added. (These will appear at -22 dB and -24 dB, respectively, assuming the gain setting value of $R_G$ is high enough to prevent overload). Finally, the amount of “920” with respect to the video carrier is measured over the useful video carrier range.

While this signal ratio may be widely used for comparative tests, it does not represent very closely the picture, chroma, and sound levels normally transmitted. A normal picture contains considerably less 3.58 MHz energy, due to the suppressed carrier encoding. On the other hand, a standard T.V. station transmits a much stronger sound signal, typically at -12 to -20 dB on the spectrum analyzer. This appears as a single sideband, and is actually a separate transmitter, usually operated at half the power of the video transmitter. A sound level of 500 mV p-p in the previous example would produce a spectrum analyzer level of -18 dB. This is a more realistic test signal for “920” evaluation.

Figures 8, 9 and 10 summarize a series of “920” measurements taken with different relative sound levels, video reference levels and values of gain resistor $R_G$. The results in Figure 8 are unsatisfactory by either measurement standard, and demonstrate that too much of the available dynamic range of the MC1374 has been used. The other examples show that by either reducing standard signal level, or reducing gain ($R_G$), acceptable results may be obtained.
BIASING THE AM SECTION

In this section there is frequent use of the letter \( \phi \), which represents one diode forward drop and is approximately 0.75 volts. The assumption has been made, and in most cases borne out experimentally, that avoidance of saturation in any stage is desirable to minimize non-linearities and interaction on the IC chip. With this in mind, the following guidelines are helpful in establishing bias levels. (Refer to Figure 1.)

The oscillator produces a symmetrical waveform of \( 2\phi \) peak-to-peak at pins 6 and 7. The values of \( R_1, R_2 \) and \( R_3 \) should be chosen to assure that pins 6 and 7 are at least \( \phi \) below \( V_{CC} \). Note that current source \( I_2 = 1.5 \text{ mA} \). This is the total current in pins 6 and 7. The resistor values shown provide sufficient drop while giving the best compromise of decoupling and Q. The oscillator outputs, via \( Q_21 \) and \( Q_22 \), drive the bases of the "upper quad" \( Q_{12}, Q_{13}, Q_{14} \) and \( Q_{15} \). The collectors of \( Q_{13} \) and \( Q_{15} \) can be as low as \( 2I_1 R_L \) below \( V_{CC} \); not very important when \( R_1 = 75 \), but worthy of consideration at higher loads. The supply voltage which should be established at the oscillator tank:

Average \( V \) pin 6 or 7 = \( V_{CC} - \phi - 2I_1 R_L \)

And since the emitters of \( Q_{12} \) through \( Q_{15} \) are \( 2\phi \) below the voltage on pin 6 or 7, the maximum voltage which should be applied at pins 1 and 11 is given by:

\[
\text{max \( V \) pin 1 or 11 = } V_{CC} - 3\phi - 2I_1 R_L
\]

For the 75 \( \Omega \) case:

\[
\text{V pin 6 or 7 = } V_{CC} - 0.9 \\
\text{max V pin 1 or 11 = } V_{CC} - 2.4
\]

On the low end, the bases of the current source transistors \( Q_8 \) and \( Q_9 \) are at \( 2\phi \) above ground. Conservatively, the input pins 1 and 11 should never go below \( 3\phi \) above ground, but in fact the current sources can be saturated without apparent problems. No distortions are evident down to 1.6 V on either input. Operation in this region is necessary when using a 5.0 V power supply, but should not be used when higher power supply is available. In summary, the useful "window" for pin 1 and pin 11 input voltages is shown in Figure 11.

A biasing divider to pin 1 and another to pin 11 can be chosen to establish nominal conditions for a static picture, such that a test pattern signal can be ac coupled to the input. Figure 12 is an illustration of the signal voltages as used in the test circuit. Note that the dc voltages on pin 1 and pin 11 are arbitrary in the absolute sense (within the "window" of Figure 11) but the relative polarity and exact difference between these dc levels is critical to the establishment of standard levels. If \( V_{CC} \) changes, divided voltages will change proportionately, as will the difference between them. This is unacceptable, as it changes modulation depth. Similar difficulties occur if the video input signal changes in average value, such as a full black or full white scene.

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In many cases the video source itself is dc referenced, and can be made to provide both pin 1 and pin 11 reference levels. If not, then the two divider voltages must be regulated, moved a bit farther apart and the sync signal clamped to the pin 11 bias by means of a diode, as shown in Figure 13. The divider impedance should be kept low to minimize the time constant of clamping corrections as video content changes. This is the classical sync clamping design problem, and workable compromises are achievable.  

**FIGURE 13 — SIMPLE VIDEO CLAMP**

THE AM MODULATOR PERFORMANCE

A widely accepted measurement tool, which is very effective in evaluation of a video modulator, is the IRE test signal. The photographs in Figure 14 and 15 show this video signal and the resulting modulated RF output from the MC1374. This signal contains sync, color burst, standard black and white levels and four equally spaced gray steps. Also, each step contains a bar of color of equal phase and amplitude (20 IRE Units). This signal is supplied to the MC1374, and bias is adjusted so that the white step produces 12.5% carrier, compared to sync tips. The output of the modulator is fed to a linear RF amplifier and a known high quality detector. The maximum measured phase difference between detected color bars is defined as differential phase error. The MC1374 typically gives less than a 2° total spread.

The difference in amplitude between the largest and smallest color bar is called differential gain distortion. In the MC1374, the test results range from 5 to 7%. (Note that this is the relative amplitude between bars which are only 20 IRE units in amplitude.) It is equivalent to an overall linearity (from below white to above black) of a little over 1%. This is good performance for a video amplifier, exceptional for a modulator.

The video input frequency response is, for all practical purposes, flat. Driven from a 75 Ω source, there is no rolloff at 30 MHz.

**FIGURE 14 — IRE TEST SIGNAL**

**FIGURE 15 — MC1374 MODULATED OUTPUT**
THE FM SECTION

The FM system was designed specifically for the T.V. intercarrier function at 4.5 MHz for the U.S. and 5.5 MHz for CCIR countries. For circuit economy, one-phase shift circuit was built into the chip. This had the benefit of saving components and pin outs, and the drawback of limiting the frequency range of this section. Still, it will operate from 1.4 MHz to 14 MHz, enough to be used in a cordless telephone base station (1.76 MHz), and high enough to possibly be used as an FM IF test signal generator.

The ability of this oscillator/modulator to be linearly frequency modulated is quite impressive. While certainly not capable of the fidelity required in "HI-FI" FM, the performance of this system compares favorably to many laboratory generators, and exceeds the distortion performance of varactor modulators by several times. At 4.5 MHz, a deviation of ±25 kHz can be achieved with 0.6% distortion (typical).

In the circuit of Figure 16 all seven devices Q1 through Q7 are active in the oscillator/modulator function. Differential amplifier Q3, Q4, Q5, Q6 acts as a gain stage, sinking current from input section Q1, Q2 and the phase-shift network R17 and C1. Input amplifier Q1, Q2 can vary the amount of "in phase" Q4 current, to be combined with phase-shifter current in load resistor R16. The R16 voltage is applied to emitter follower Q7 which drives an external series L-C circuit. Feedback from the center of the L-C circuit back to the base of Q6 closes the loop. As audio input is applied which would offset the stable oscillatory phase, the frequency changes to counteract.

It would seem natural to take the FM system output from pin 2, the emitter-follower output, but this output is high in harmonic content. Taking the output from pin 3 sacrifices somewhat in source impedance but results in a clean output fundamental, with all harmonics more than 40dB down. This choice removes the need for additional filtering components. The source impedance of pin 3 is approximately 2 kΩ, and the open-circuit amplitude is about 900 mV p-p for the test circuit shown in Figure 17.
FM SECTION CIRCUIT VALUES
The oscillator center frequency is approximately the resonance of the inductor L2 from pin 2 to pin 3 and the effective capacitance C3 from pin 3 to ground. Include approximately 6 pF (internal) when making frequency calculations. For overall oscillator stability, it is best to keep $X_L$ in the range of 300 Ω to 1 kΩ.

The modulator transfer characteristic at 4.5 MHz is shown in Figure 18. The curve should be interpreted as a transfer function relating instantaneous pin 14 voltage to output frequency. Transfer curves at other frequencies have a very similar shape, but differ in maximum deviation per input volt, as shown in Figure 19.

![Figure 18 - Modulator Transfer Function 4.5 MHz](image)

![Figure 19 - Modulator Sensitivity](image)

Most applications will not require dc connection to the audio input, pin 14. However, some improvements can be achieved by the addition of biasing circuitry. The unaided device will establish its own pin 14 bias at 4ε, or about 3.0 V. A brief study of the transfer characteristic shows that this bias is a little too high for optimum modulation linearity. This can be verified by means of distortion measurements using a high quality FM detector and distortion analyzer. Figure 20 shows better than 2 to 1 improvement in distortion between the unaided device and pulling pin 14 down to 2.6 to 2.7 V. This can be accomplished by a simple divider, if the supply voltage is relatively constant.

![Figure 20 - Distortion versus Modulation Depth](image)

The impedance of the divider has a bearing on the frequency versus temperature stability of the FM system. Figure 21 was taken using an adjustable regulated bias source and varying the "pull down" resistor from pin 14 to the bias source to determine the most stable impedance. The resulting value of 27 kΩ can be replaced by a divider of 180 kΩ and 30 kΩ (for $V_{CC} = 12$ V) with equally good temperature stabilization results.
Another reason for dc input to pin 14 is the possibility of automatic frequency control. In some systems where high accuracy of intercarrier frequency is required, it may be desirable to feed back the dc output of an AFC or phase detector for nominal carrier frequency control. Obviously the filtering and response time of such a system will have to be slow enough so as not to follow the desired audio. Only limited control range could be used without adversely affecting the distortion performance, but as shown earlier, very little frequency compensation will be needed.

One added convenience in the FM section is the separate pin “oscillator B+” which permits disabling of the sound system during alignment of the AM section. Usually it can be hard wired to the VCC source without decoupling.

PRE-EMPHASIS

Standard practice in television is to provide pre-emphasis of higher audio frequencies at the transmitter and a matching de-emphasis in the T.V. receiver audio amplifier. The purpose of this is to counteract the fact that less energy is usually present in the higher frequencies, and also that fewer modulation sidebands are within the deviation window. Both factors degrade signal-to-noise ratio. Pre-emphasis of 75 μs is standard practice. Usually the audio source to the T.V. modulator already has pre-emphasis, but for cases where it has not been provided, or is not capable of supplying the 6 kΩ input impedance of the MC1374, a suitable pre-emphasis network is covered in Appendix II.

ASSEMBLING A COMPLETE MODULATOR

Using the information developed in the preceding sections, a complete T.V. modulator circuit is presented. The schematic is shown in Figure 23. It includes the simple and almost lossless second harmonic output filter, rather than the more elaborate vestigial sideband type. The gain resistor, R8 in this case, is 2.2 kΩ, for an intended video input of approximately 1.0 V peak at sync tip. This produces an output of 70 mV p-p un-terminated, for a max RMS output of about 12 mV. This is 12dB greater than FCC rules permit, so it must be padded down for commercial applications.
The modulator circuit includes channel 3 and channel 4 bandswitching, video sync tip clamping, and audio bias to reduce distortion. All 3 of these features can easily be deleted when minimum cost is needed.

One area which was touched upon earlier, but not fully developed, is the coupling of the intercarrier sound output from pin 3 to the sound side of AM modulator input, pin 1. The method shown in Figure 23 is the preferred approach, primarily because it permits easy adjustment of intercarrier amplitude with the minimum of “antenna” on pin 1. The input impedance at pin 1 is very high, so the intercarrier level is determined by the source impedance of pin 3 (about 2K), driving through C4 into the bias circuit impedance of R4 and R5, about 2.2K. This provides an intercarrier level of nearly 500 mV p-p, just right for the video level chosen here.

The artwork for a printed circuit version of this design is provided in Appendix III. Performance of the board is consistent with the data presented earlier and has been used successfully with both static (test pattern) and video disk sources. With a 12 V regulated supply there is less than ±10 kHz shift of RF carrier frequency from 0° to 50°C for any video input level.

REFERENCES:
3. MC1376 — FM Modulator, Advance Information Data Sheet.
Drill Holes
A(12) 0.055 ±0.003
All Others
0.040 ±0.003
TUNING DIODE DESIGN TECHNIQUES

Tuning diodes are voltage variable capacitors employing the junction capacitance of a reverse biased PN junction. This note presents a simplified theory of tuning diodes and discusses a number of considerations to be employed in designs using tuning diodes.

INTRODUCTION

Voltage variable capacitors or tuning diodes are best described as diode capacitors employing the junction capacitance of a reverse biased PN junction. The capacitance of these devices varies inversely with the applied reverse bias voltage.

Tuning diodes have several advantages over the mechanical variable capacitor. They are much smaller in size and lend themselves to circuit board mounting. They are available in most of the same capacitance values as fixed capacitors. Tuning diodes offer the designer the desirable feature of electronic tuning.

The capacitance of all tuning diodes inherently varies with temperature and may require compensation. A simple scheme is available for compensation of the temperature drift, resulting in stabilities as good as, or better than, that of air capacitors. Digital techniques effectively eliminate temperature as a problem.

SIMPLIFIED THEORY

A tuning diode is a silicon diode with very uniform and stable capacitance versus voltage characteristics when operated in its reverse biased condition. In accordance with semiconductor theory, a depletion region is set up around the PN junction. The depletion layer is devoid of mobile carriers. The width of this depletion region is dependent upon doping parameters and the applied voltage. Figure 1A shows a PN junction with reverse bias applied, while Figure 1B shows the analogy, a parallel plate capacitor. The equation for the capacitance of a parallel plate capacitor given below predicts the capacitance of a tuning diode.

\[
C = \frac{\varepsilon A}{d}
\]

where
- \(\varepsilon = \) dielectric constant of silicon equal to 11.8 \(\times\) \(\varepsilon_0\)
- \(\varepsilon_0 = 8.85 \times 10^{-12} \text{ F/m}\)
- \(A = \) Device cross sectional area
- \(d = \) Width of the depletion layer.

The depletion layer width \(d\) may be determined from semiconductor junction theory.
The more accepted method of determining tuning diode capacitance is to use the defining formula for capacitance.
\[ C = \frac{dQ}{dV} \quad (2) \]
The charge, \( Q \) per unit area, is defined as:
\[ Q = \varepsilon E \quad (3) \]
where \( E \) = Electric field
So we have capacitance per unit area:
\[ c = \frac{C}{A} = \frac{dE}{dV} \quad (4) \]
Norwood and Shatz\(^1\) use these ideas to develop a general formula:
\[ c = \left[ \frac{q B_m m+1}{(m+2)(V+\phi)} \right]^{1/m+2} \quad (5) \]
where \( m \) = Impurity exponent
\( c \) = Capacitance per unit area
Lumping all the constant terms together, including the area of the diode, into one constant, \( C_D \), we arrive at:
\[ C_J = \frac{C_D}{(V+\phi)^\gamma} \quad (6) \]
where \( \gamma \) = Capacitance Exponent, a function of impurity exponent
\( \phi \) = The junction contact potential
\( (= 0.7 \) Volts)\]
The capacitance constant, \( C_D \), can be shown to be a function of the capacitance at zero voltage and the contact potential. At room temperature we have:
\[ C_D = C_0(\phi)\gamma \quad (7) \]
The simple formula given in Eq. 6, very accurately predicts the voltage-capacitance relationship of modern tuning diodes. There are many detailed derivations\(1,2,3,4,5\) of junction capacitance, so further explanation is not necessary in this note.

The capacitance of commercial tuning diodes must be modified by the case capacitance.

The equation then becomes:
\[ C = C_C + C_J \quad (8) \]
where
\( C_C \) = Case capacitance typically 0.1 to 0.25 pF
\( C_J \) = Junction capacitance given by Equation 6.

**TUNING RATIOS**

The tuning or capacitance ratio, \( TR \), denotes the ratio of capacitance obtained with two values of applied bias voltage. This ratio is given by the following expression for the diode junction.
\[ TR = \frac{C_J(V_2)}{C_J(V_1)} = \left[ \frac{V_1 + \phi}{V_2 + \phi} \right]^\gamma \quad (9) \]

where \( C_J(V_1) \) = Junction capacitance at \( V_1 \)
\( C_J(V_2) \) = Junction capacitance at \( V_2 \)
where \( V_1 > V_2 \)

In specifying \( TR \), some tuning diode data sheets use four volts for \( V_2 \). However, in order to achieve larger tuning ratios, the devices may be operated at slightly lower bias levels with some degradation in the \( Q \) specified at four volts. (See the discussion of \( Q \) versus voltage in the circuit \( Q \) section, later in this note). Furthermore, care must be taken when operating tuning diodes at these low reverse bias levels to avoid swinging the diode into forward conduction upon application of large ac signals. These large signals may also produce distortion due to capacitance modulation effects.

Since the effects of \( \phi \) and case capacitance, \( C_C \), are usually small, Eq. 9 may be simplified to the following for most design work:
\[ TR = \frac{C(V_{\min})}{C(V_{\max})} = \left( \frac{V_{\max}}{V_{\min}} \right)^\gamma \quad (10) \]

The frequency ratio is equal to the square root of the tuning ratio. This tunable frequency ratio assumes no stray circuit capacitance.

Another parameter of importance is \( \gamma \), the capacitance exponent. Physically, \( \gamma \) depends on the doping geometry employed in the diode. Tuning diodes with \( \gamma \) values from 1/3 to 2 can be manufactured by various processing techniques. The types of junctions, their doping profiles, and resulting values of \( \gamma \) are shown in Figure 2. These graphs show the variation of the number of acceptors (\( N_A \)) and the number of donors (\( N_D \)) with distance from the junction.

Abrupt junctions are the easiest to manufacture and the majority of tuning diodes on the market are of this type. This type of junction gives a \( \gamma \) of approximately 1/2 and a tuning ratio on the order 3 with the specified voltage range. Therefore the corresponding frequency range which may be tuned is about 1.7 to 1.0. A typical example is the MV2101:
\[ C(V_2) = C(30 \text{ V}) = 2.5 \text{ pF} \]
\[ C(V_1) = C(4 \text{ V}) = 6.8 \text{ pF} \]
\[ TR = 2.7 \]
\[ \gamma = 0.47 \]

The subscripts on the capacitance refer to the bias voltage applied.

In many applications, such as tuning the television channels, or the AM broadcast band, a wider frequency range is required. In this event, the designer must use a hyper-abrupt junction tuning diode. The hyper-abrupt diode has a \( \gamma \) of 1 or 2, and tunes over much larger frequency ranges. Table I shows typical types of tuning diodes available, their tuning ratios, frequency ratios and junction types.

The hyper-abrupt devices are constructed with special epitaxial growth, diffusion, and ion implant techniques, which create a doping profile similar to that shown in Figures 2C and 2D. The \( Q \) of the MMBV105G and MMBV109 series hyper-abrupt diodes is as high as abrupt
junction devices. Their capacitance range is from a few picofarads to 10 or 20 pF, and their major application is in television tuners. The MV1401 series are high capacitance devices for applications below 10 MHz. They are suitable for tuning elements in AM broadcast band receivers and similar low frequency applications.

### TABLE I SAMPLE TUNING DIODE TYPES

<table>
<thead>
<tr>
<th>Device Series</th>
<th>Nominal Capacitance</th>
<th>Tuning Ratio</th>
<th>Frequency Ratio</th>
<th>Junction Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1N5139</td>
<td>47-68 pF</td>
<td>2.7-3.4</td>
<td>0.47</td>
<td>1.6-1.8</td>
</tr>
<tr>
<td>MV2101</td>
<td>100-68 pF</td>
<td>1.6-3.3</td>
<td>0.47</td>
<td>1.6-1.8</td>
</tr>
<tr>
<td>MMBV109</td>
<td>2.0 pF</td>
<td>4.0-6.0</td>
<td>1.0</td>
<td>2.0-2.4</td>
</tr>
<tr>
<td>MV1401</td>
<td>550-120 pF</td>
<td>10-14</td>
<td>2.0</td>
<td>3.2-3.7</td>
</tr>
<tr>
<td>MMBV109</td>
<td>30 pF</td>
<td>5.0-6.5</td>
<td>1.0</td>
<td>2.2-2.5</td>
</tr>
</tbody>
</table>

CIRCUIT Q

Popular types of mechanical tuning capacitors often have Q's on the order of a thousand or greater. The Q of tuned circuits using these capacitors is generally dependent only on the coil. When using a tuning diode, however, one must be conscious of the tuning diode Q as well. The Q of the tuning diode is not constant, being dependent on bias voltage and frequency. The Q of tuning diode capacitors falls off at high frequencies, because of the series bulk resistance of the silicon used in the diode. The Q also falls off at low frequencies because of the back resistance of the reverse-biased diode.

The equivalent circuit of a tuning diode is often described as shown:

![Equivalent Circuit of Tuning Diode](image)

where

- \( R_p \) = Parallel resistance or back resistance of the diode
- \( R_s \) = Bulk resistance of the silicon in the diode
- \( L_s' \) = External lead inductance
- \( L_s \) = Internal lead inductance
- \( C_c \) = Case capacitance

Normally we may neglect the lead inductance and case capacitance. This results in simplified circuit of Figure 4.

![Simplified Equivalent Circuit of Tuning Diodes](image)

The tuning diode Q may be calculated with Equation 11.

\[
Q = \frac{2\pi f C R_p^2}{R_s + R_p + (2\pi f C)^2 R_s R_p^2}
\]

This rather complicated equation is plotted in Figure 5 for \( R_s = 1.0 \) ohm, \( R_p = 30 \times 10^9 \) ohms, at \( V = 4 \) volts and \( C = 6.8 \) pF, typical for a 1N5139 diode at room temperature.

![Graph of Q versus Frequency](image)
At frequencies above several MHz, the Q decreases directly with increasing frequency by the simpler formula given below:

\[ Q = \frac{Q_s}{2\pi f CR_s} \]  

(High frequency Q)  (12)

The emphasis today is on decreasing \( R_s \) so better high frequency Q can be obtained. At low frequencies Q increases with frequency since only the component resulting from \( R_p \), the back resistance of the diode, is of consequence.

\[ Q = Q_p + 2\pi f CR_p \]  

(Low frequency Q)  (13)

Q is also dependent on voltage and temperature. Higher reverse bias voltage yields a lower value of capacitance, and also since \( R_s \) decreases with increasing bias voltage, the Q increases with increasing voltages. Similarly, low reverse bias voltages accompany larger capacitances, and lower Q's. Increasing temperature also lowers the Q of tuning diodes. As the junction temperature increases, the leakage current increases, lowering \( R_p \). There is also a slight decrease in \( R_s \) with increasing temperature, but the effects of the decreasing \( R_p \) are greater and this causes the Q to decrease. The effects of temperature and voltage on the Q of a 1N5139 at 50 MHz are plotted in Figure 6.

![Figure 6 - Q versus Reverse Bias and Temperature](image)

**TEMPERATURE**

The Q and tuning ratio of tuning diodes are parameters that every design engineer must be aware of in his circuits. Another equally important characteristic of tuning diodes is their temperature coefficient. A typical example of the capacitance versus temperature drift is shown in Figure 7.

The temperature coefficient, \( T_C \), is a function of applied bias. Figure 8 shows \( T_C \) for a typical tuning diode. Note that for low bias levels, on the order of a volt or two, the \( T_C \) is as high as +600 parts per million per degree centigrade (ppm/°C). This represents a frequency change of -300 ppm/°C which at 100 MHz means a frequency shift of 30 kHz per degree. It is obvious that a temperature compensation scheme is desirable for any frequency control not using feedback techniques.

![Figure 7 - Capacitance versus Temperature for a MV2101 Diode Biased at 4.0 Volts](image)

![Figure 8 - Capacitance Drift in ppm/°C versus Voltage MV2101 Diode](image)

In Figure 9, the actual capacitance drift of a MV2101 per degree centigrade is plotted. The graph illustrates that a simple negative temperature coefficient compensating capacitor will not compensate for the tuning diode \( T_C \) because the change in capacitance is not constant with voltage.

![Figure 9 - Capacitance Drift in Attofarads/°C versus Voltage for the MV2101 Tuning Diode](image)
THEORY OF TEMPERATURE CHANGE

Before proceeding further with schemes to correct the temperature drift, it is informative to investigate the physical mechanisms responsible for the changing capacitance. Equations 6 and 8 may be combined to give the basic expression for capacitance below:

\[ C = \frac{C_d}{V + \phi} + C_c \]  

We can pinpoint the terms in Eq. 14 that may account for capacitance changes. The contact potential, \( \phi \), is a strong function of temperature, varying on the order of \(-2.0 \text{ mV/}^\circ\text{C}\). \( C_d \) is a function of geometric dimensions which can change with temperature and \( \epsilon \) which changes with temperature. Case capacitance also changes with temperature. For this analysis we will assume the only terms not temperature dependent are the supply voltage \( V \), and the capacitance exponent, which is a function only of the slope of the doping profile.

The contact potential, \( \phi \), is readily calculated from semiconductor theory, and the equations predict a large change with temperature. This change in \( \phi \) will produce a much larger change in capacitance for lower voltages than for higher voltages, and therefore accounts for the majority of capacitance change in tuning diode temperature drift. See Table II.

### Table II

<table>
<thead>
<tr>
<th>Applied Bias Voltage (Volts)</th>
<th>Capacitance Drift In ( \text{ppm/}^\circ\text{C} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>587</td>
</tr>
<tr>
<td>2</td>
<td>261</td>
</tr>
<tr>
<td>4</td>
<td>204</td>
</tr>
<tr>
<td>10</td>
<td>88.7</td>
</tr>
<tr>
<td>20</td>
<td>45.6</td>
</tr>
<tr>
<td>30</td>
<td>30.7</td>
</tr>
</tbody>
</table>

Comparing Table II with Figure 8, we see that a \(+40\) to \(+50 \text{ ppm/}^\circ\text{C}\) temperature drift still remains. Therefore \( \phi \) is not the only mechanism responsible for temperature drift and others must be sought. There is a change with temperature in physical dimensions in any material which has an affect on the order of \(1 \text{ ppm/}^\circ\text{C}\) for a tuning diode. However, this change is too small to be of any significance. Another possibility is a change in dielectric constant. Silicon, depleted of its charge carriers, forms a dielectric layer with a relative dielectric constant of \(11.8\). The dielectric constant of silicon has a temperature coefficient of \(+35 \text{ ppm/}^\circ\text{C}\). These effects change the value of \( C_d \) with temperature. The case capacitance also varies slightly with temperature. See Table III.

<table>
<thead>
<tr>
<th>Bias Voltage (Volts)</th>
<th>Capacitance (pf)</th>
<th>Changes attributable to case capacitance (ppm/°C)</th>
<th>Capacitance (pf)</th>
<th>Changes attributable to case capacitance (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>8.9</td>
<td>3.4</td>
<td>6.1</td>
<td>0.5</td>
</tr>
<tr>
<td>4.0</td>
<td>6.4</td>
<td>4.7</td>
<td>4.7</td>
<td>0.6</td>
</tr>
<tr>
<td>10.0</td>
<td>4.8</td>
<td>6.3</td>
<td>3.2</td>
<td>1.0</td>
</tr>
<tr>
<td>30.0</td>
<td>3.0</td>
<td>10.0</td>
<td>19</td>
<td>1.6</td>
</tr>
<tr>
<td>60.0</td>
<td>2.2</td>
<td>14.0</td>
<td>13</td>
<td>2.3</td>
</tr>
</tbody>
</table>

In summary, the largest changes are caused by the change in contact potential. This effect is most noticeable at low voltage, high capacitance levels. The change in silicon dielectric is the next most important factor providing a change that is uniform for all devices and voltages. Case capacitance changes are most noticeable in the low capacitance, high voltage range, and may be neglected for all devices except those low capacitance devices.

TEMPERATURE COMPENSATION

A popular method of temperature compensating tuning diodes involves the use of a forward biased diode. The voltage drop of a forward biased diode decreases as the temperature rises, thus applying a changing voltage to the tuning diode. In the network shown in Figure 10, an increase in temperature will result in a decrease of the diode voltage \( V_{DIODE} \) to perhaps \(0.5 \text{ V}\).

![FIGURE 10 — Simple Temperature Compensating Network](image)

If \( V_{IN} \) is maintained constant, the available output voltage \( V_{OUT} \) will rise by \(0.1 \text{ V}\). This increase in output voltage will lower the capacitance of the tuning diode and partially offset the initial capacitance increase caused by the temperature change. Obviously, for the above circuit to be effective, the compensating diode must be thermally coupled to the varactor to be corrected.

Frequently, the varactor is part of a feedback loop which controls the frequency of oscillation by digital techniques. In this case, the temperature effects are generally accounted for in the digital feedback loops, so that diode compensation is not required.

THE POWER SUPPLY

We previously assumed that the supply voltage did not change with temperature. This is rarely the case, and special consideration must be given to this part of the design. All our efforts to temperature compensate the tuning diode may be in vain if the power supply has a large \( T_C \) or is otherwise unstable. Figure 11 shows the common method of supplying voltage to a tuning diode.
The regulator is the most critical part of the circuit in Figure 11. It must be extremely stable in order to achieve good varactor tuning stability. The full drift of the power supply as expressed in ppm/°C will appear at $V_d$ regardless of the setting of the potentiometer. For example, if $V_{Reg}$ is 40 V with a drift of 100 ppm/°C (4 mV/°C), $V_d$ may be 10 V, but will still have a drift of 100 ppm/°C (1 mV/°C). A 50 ppm/°C stability figure in $V_d$ translates into a 25 ppm/°C stability of capacitance, when the capacitance exponent is 0.5. For hyper-abrupt junctions we realize capacitance stabilities of 50 and 100 ppm/°C for exponents of 1 and 2 respectively.

There are many differing power supply regulators available to the designer. Zener diodes are relatively inexpensive, but have a poor temperature coefficient. Temperature compensated zeners are very expensive and have a limited voltage range. The LM117, a monolithic integrated circuit voltage regulator, has excellent temperature characteristics, 37 volt output capability, and wide temperature range.

The MC7800 fixed output voltage regulators are extremely simple to use in that they have only input, output and ground terminals and require no external components other than possibly a high frequency by-pass capacitor. (The latter item is generally required with all IC regulators to prevent high frequency oscillations).

The MVS460 is a two leaded IC regulator especially designed for use with tuning diodes. It represents a simple, inexpensive solution to the voltage regulator problem. Table IV contains a summary of available power supply regulators.

**TABLE IV Summary of Power Regulators**

<table>
<thead>
<tr>
<th>Device</th>
<th>Voltage Range</th>
<th>Temperature Range</th>
<th>Voltage ppm/°C</th>
<th>Capacitance ppm/°C</th>
<th>Relative Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>1N5260 Zener</td>
<td>33</td>
<td>±65 +200°C</td>
<td>975</td>
<td>475</td>
<td>Low</td>
</tr>
<tr>
<td>1N4752 Zener</td>
<td>33</td>
<td>±65 +200°C</td>
<td>850</td>
<td>425</td>
<td>Low</td>
</tr>
<tr>
<td>1N3157 Temperature Compensated Zener</td>
<td>8-4</td>
<td>-50 +125°C</td>
<td>10</td>
<td>5</td>
<td>High</td>
</tr>
<tr>
<td>LM117 Regulator</td>
<td>37</td>
<td>±55 +125°C</td>
<td>50</td>
<td>25</td>
<td>Low</td>
</tr>
<tr>
<td>MC7800 Fixed Voltage Regulators</td>
<td>28</td>
<td>0° +125°C</td>
<td>40-60</td>
<td>20-30</td>
<td>Low</td>
</tr>
<tr>
<td>MVS460 TO-92 Regulator</td>
<td>31 V</td>
<td>0° +70°C</td>
<td>-100</td>
<td>12</td>
<td>Low</td>
</tr>
</tbody>
</table>

Notes:
1) See Figure 12 for some typical circuit connections
2) To compute frequency change (ppm/°C), divide capacitance (ppm/°C) change by 2.

**VARIABLE RESISTOR**

The variable resistor is considerably less critical.

Since it is being used as a voltage divider, all that is required is that the resistive material be uniform so any change in resistance is uniform throughout the potentiometer. Wire wound, and special high quality cermet film variable resistors are suitable for these applications. Generally speaking, a linear potentiometer should have a $T_C$ of ±150 ppm/°C or better. Special taper potentiometers should have a $T_C$ of ±50 ppm/°C or better.

The variable resistance cannot be made too large or there will be appreciable voltage drop as the reverse current in the diode increases. The reverse current in a silicon diode generally doubles every 10°C so this becomes an important problem at temperatures above 50°C. If the temperature is expected to run as high as 70°C, one must limit the variable resistor to 50 kΩ or the effect will be a greater than 5 ppm/°C capacitance change. If 50°C is the upper temperature limit, the resistance may be upped to 150 kΩ. These values apply to all Motorola's tuning diode series. When the tuning diodes are used in applications where temperature will greatly exceed 70°C, the divide resistance should be kept below 10 kΩ. This low value requires large power supply currents and would be undesirable in some applications. However, since the Motorola LM117 is the recommended power source at these temperatures, voltage control may be accomplished using the regulator without relying on an external divider potentiometer, as shown in Figure 12. The LM117's low output impedance of 0.05 ohms will easily and reliably handle the change in current demanded by the tuning diode as it heats up.

**HYPER-ABRUPT TEMPERATURE DRIFT**

The hyper-abrupt tuning diode is more sensitive than other types to temperature variations resulting in a greater need for temperature compensation. Also their drift with temperature is not as uniform as abrupt junction tuning diodes. Their drift factors expressed in ppm/°C run as high as 800 to 1200 for the units with a $\gamma$ of 2. Units having a $\gamma$ of 1 typically show 300 to 400 ppm/°C capacitance changes. These higher drift rates are caused by the hyper-abrupt tuning diode's greater...
sensitivity to changes in voltage, and the fact that the majority of capacitance change is caused by the change in contact potential, \( \phi \). This greater sensitivity to voltage changes means that power supply and other instabilities will also have a larger effect than with regular abrupt junction tuning diodes.

**FIGURE 12 — High Stability Regulator -50 to +125°C**

SUMMARY

Voltage variable capacitors have replaced air variable capacitors in most applications. These devices offer many advantages over previous variable capacitors, such as the ability to employ remote tuning. By carefully considering the proper design conditions, such as temperature drift, and designing accordingly, tuning diodes can replace air capacitors in virtually all but high power applications. The designer must be aware of the tuning range and Q limitation in order to use these devices effectively. Temperature drift ceases to be an issue when proper compensation schemes, or digital feedback loops are used.
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*Voltage-Controlled Oscillator*, Issue E, Motorola Data Sheet MC1648, M.
POWER MOSFETs
versus
BIPOLAR TRANSISTORS

What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price?

Several manufacturers have recently introduced power FETs for RF amplifier applications. Devices with 100 W output capabilities are available for VHF frequencies and smaller units are made for UHF operation. All are enhancement mode devices, which means that the gate must be biased with positive voltage (N channel) in respect to the source to “turn it on.” Early designs were so called V-MOS FETs, where the channel is in a V-groove. The V-groove must be etched with a special process, and the silicon material must have a different crystal orientation from the material normally used for bipolar transistors. The difficulty of the etching process in production has led to the development of other types of channel structures such as HEX and T, which are still vertical channel structures, but V-groove is eliminated, and the gate is on a straight surface. Thus, for an equal gate periphery, more room

<table>
<thead>
<tr>
<th>TABLE A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bipolar</td>
</tr>
<tr>
<td>$Z_{in}$ RS/ XS(30 MHz):</td>
</tr>
<tr>
<td>$Z_{in}$ RS/ XS(150 MHz):</td>
</tr>
<tr>
<td>$Z_{OL}$ (Load Impedance):</td>
</tr>
<tr>
<td>Biasing:</td>
</tr>
<tr>
<td>Ruggedness:</td>
</tr>
<tr>
<td>Linearity:</td>
</tr>
<tr>
<td>Advantages:</td>
</tr>
<tr>
<td>Disadvantages:</td>
</tr>
</tbody>
</table>
on the surface is required. Japanese manufacturers seem to favor geometries with horizontal channels. They are similar to small signal MOSFETs with a number of them paralleled on one chip. This technique represents even more wasteful use of the die surface than HEX or TMOS. Typically a power FET requires 50 to 100 percent more die area than a bipolar transistor for equal power output performance. For TMOS the number is about 50 percent. This is mainly due to the higher saturation voltage, but the geometry also gives some 30 percent less gate periphery than available base area in bipolar. Since the price of a solid state device is a function of a die size, we get fewer watts per dollar. This is completely opposite from what the industry has been trying to do in the past years with bipolar transistors. So, one may ask: What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price? This is where we come to the purpose of this article, which is to discuss the characteristics of the FET and bipolar device. Both have the same basic geometry, but with some mask changes, one was processed as a MOSFET and the other as a bipolar.

CIRCUIT CONFIGURATIONS

Since the gate of a MOSFET device is essentially a capacitor, which consists of MOS capacitance distributed between the channel and the surface metalization, the input Q is normally extremely high. For this reason, the gate must be de-Q’ed with a shunt resistance or applying negative feedback or a combination of the two. Unless this is done properly, the affect of feedback capacitance (C_{RSS}) will result in conditions, where stable operation is impossible to achieve.

Figure 1 shows a Smith Chart plot of a 150 W MOSFET and a bipolar device using the same basic geometry for comparison purposes. The gate of the FET has been shunted by a resistance of 20 ohms. Without the shunt resistance the input impedance would be a pure capacitive reactance, if package inductances are disregarded.

The input Q is an inverse function of the broadband-ability of a device. With the techniques mentioned above, the Q can be controlled to a large degree, but some power gain will be sacrificed, unless only some type of selective negative feedback is employed for that purpose. Amplifiers in the 100 W power level, covering five octaves can be designed, and the limiting factor only seems to be the proper design of the broadband matching transformers.

Due to the lack of base diode junctions inherent to bipolar devices, where the diode forward conductance depends on the drive level, the MOSFET gate impedance varies only slightly with the input voltage amplitude. The gate MOS capacitance should be more or less independent of voltage, depending on the die processing. This is considered one of the advantages with FETs, especially regarding amplitude modulated applications, where a constant load for the driver stage is important. Negative feedback should be limited, since it tends to deteriorate this characteristic. Another advantage is the AGC capability by varying the gate voltage. In common source configuration, depending on the initial power gain, etc., an AGC range of 20 dB is achievable.
has more tendency for parasitic oscillations, since the input and output are in the same phase. The de-Q'ing of the input can be done in the same manner as in a common source circuit, but negative feedback is not as easy to implement. This circuit also exhibits greater power gain versus bias voltage variation characteristics. In applications, where 40 dB to 50 dB AGC range is required, the common gate configuration should be considered.

A common drain configuration represents the emitter follower in bipolar circuits. In both cases the input impedance is high and the load impedance is effectively in series with the input. The input capacitance, (drain-to-gate, or collector-to-base) is lower than in common source or common gate circuits, and several times lower for the FET than bipolar for equal die size. This is due to lack of the diode junction. A MOSFET source follower cannot be regarded as having current gain as the emitter follower. The amplification rather takes place through impedance transformation. Due to the fair amount of input de-Q'ing required, the available power gain is lower than in common source circuit for example. Having less than unity voltage gain, the circuit exhibits exceptional stability, and negative feedback is not necessary, nor can it be easily implemented. Push pull broadband circuits for a frequency range of 2 to 50 MHz have been designed for 200-300 watt power levels. Their inherent characteristics are good linearity and gain flatness without any leveling networks. High power SSB amplifiers are probably the most suitable application for common drain operation. The AGC range is comparable to that in common source, but higher voltage swing is required. It must be noted that the MOS devices used must have high gate rupture voltage, since during the negative half cycle of the input signal, the gate voltage approaches the level of VDS.

LINEARITY ASPECTS

Some literature claims that MOS power FETs are inherently more linear than the bipolar transistors. This is only true up to the point where envelope distortion, caused by saturation, instabilities or other reasons, is not present. It is also a function of the bias current (I_DQ). The FETs usually require higher idling currents than the bipolar to get full advantage of their linearity. Bipolars are usually biased only to get the base-emitter diode into forward conduction, whereafter increasing the bias helps little. Class A is an exception, but the device must then be operated at 20-25 percent of the rated Class AB level.

Probably the main advantage with the MOS power FETs is their greatly superior high order IM distortion performance. This is mainly due to the fact that ballasting resistors are not required with FETs. In bipolar RF power transistors, nonlinear feedback is distributed to each emitter site through the MOS capacitance from the collector. In devices using diffused silicon resistors, this effect is even worse, and caused by additional nonlinear diode capacitance between the collector and the emitters. The high order IMD (9th and up) is actually in direct relation to the ballasting resistor values, which must be optimized for an even power distribution along the die. Too low values would result in a fragile device, and the opposite would, in addition to the IMD problem, result in high collector-emitter saturation voltage and low power gain.

The feedback capacitance, drain-to-gate or collector-to-base for example, also has a secondary effect in IMD. In both cases it is a function of the die geometry, and is usually lower with devices with higher figure of merit, such as the ones made for UHF and microwave applications. A MOS power FET exhibits some five times lower feedback capacitance than a bipolar transistor with a similar geometry. In a bipolar transistor this capacitance partly consists of the collector-base junction, which is highly nonlinear with voltage. This, together with the varying input impedance, generates internal feedback, which is nonlinear and produce high order IMD to some degree. A more noticeable effect is that the low order IMD goes up with reduced drive levels as shown in Figure 6.

This can be related to different turn on characteristics between the two device types. When a bipolar device is biased to Class AB, the bias does not usually, completely overcome the V_EE knee. Thus, at lower signal levels, the remaining nonlinear portion covers a larger area of the total voltage swing. Increasing the bias from the normally recommended Class AB values will help and full Class A should eliminate the problem completely.
FIGURE 5 — Two Tone Spectrographs of 300 W PEP, 50 V Amplifier Outputs

a. using bipolar transistors and b. with TMOS power FETs. 500 mA of bias current per device was used in each case. Doubling the bias current has a minimal effect in a. but b. the 7th order products would be lowered by 10-12 dB.

CLASS D/E APPLICATIONS

Switching mode RF power amplifiers have only become feasible since the introduction of the power FET. Being a majority carrier device, the FET does not exhibit the storage time phenomena, that limits the switching speed of a bipolar. For a given device, the switching speed is mainly determined by the speed the gate capacitance can be charged and discharged. If the capacitance is in the order of several hundred pF, a smaller FET is required to provide the fast charge-discharge switch. For low power stages, bipolars can be used, since the storage time is mainly an inverse function of the ft and device size. The advantages of a Class D amplifier are high efficiency, linearity and ruggedness, since power is ideally dissipated only during the switching transitions.

These amplifiers are readily applicable for FM modulation, after harmonic filtering. The analog gain is obtained by pulse-width modulation of the input switching signal, and demodulation of the output with suitable filters. Linearity is required only from the modulator, which is easy to achieve at small signal levels. The high speed voltage controlled one shot MC10198 should be ideal for a linear pulse-width modulator. By properly adjusting its operating point, low level AM or suppressed carrier double sideband signals can be generated.

FIGURE 6 — IM Distortion as a Function of Power Output. Solid Curves MOSFET, Dashed Curves Bipolar Transistor

FIGURE 7 — A Typical Power MOSFET Class D RF Amplifier, Arranged in Push-Pull Configuration

GENERAL

All MOSFETs can in theory have a positive temperature coefficient on the gate threshold voltage. This means that the gate threshold voltage increases with temperature, trying to "turn the device off." In addition the $g_m$ will decrease, which also helps in preventing the thermal runaway, which is commonly a problem with bipolars. The coefficient of the gate threshold
voltage is also a function of the drain current. Normally the coefficient is negative at low current levels, and turns positive at higher currents. The turnaround point, which can be controlled by doping the other fabrication steps, must be at a current level not to exceed the maximum dissipation rating, taking the derating factor into account. Thus, the power MOS devices can be easily biased to Class A, without fear of a thermal runaway.

Two types of high frequency noise are generated by bipolar transistors. Shot noise is caused by the forward biased junctions, and thermal noise by moving carriers upon flow of electrons. Both have different noise spectrums, and only the latter is present in a FET. In a transmitter, where the devices are biased for linear operation, the shot noise becomes a problem, especially if a receiver is in close proximity, as in transceiver designs. Also, if several stations are operated near each other, the noise can be transmitted through the antenna, disturbing the reception at nearby stations. In most instances, the bias of the power devices must be switched on and off during the transmit and receive functions, which will prevent a full break-in operation. Measurements of 150 W devices, intended for SSB applications, were performed at 30 MHz, at the proper idling current levels. The difference in the total noise figure between a bipolar and a FET is about three to one, or 7 dB and 2.2 dB respectively. The amount of noise that can be tolerated varies with each situation, and whether the difference above is significant in practice depends on other factors in involving the design of the equipment.

CONCLUSION

From the above we must conclude that it is doubtful the power FET ever will replace the bipolar transistor in all areas of communications equipment. It will have its applications in low and medium power VHF and UHF amplifiers, eliminating the need for internal matching, and up to medium power low band and VHF SSB, where the high order IMD is beginning to be more and more in emphasis due to the crowded frequency spectrums. The author's personal opinion is that the power FET is the most feasible device for the amplitude compandored sideband (ACSB) applications, proposed for future use in land mobile communications. The system principle requires extreme linearity in the amplifying stages, which in the past has only been achieved with Class A operation. The power FET also opens new applications for high efficiency switching mode power amplifiers, which have not been possible in the past for reasons described earlier. The possible upper frequency limit would be dictated by the physical lay-out of the system.

FIGURE 8 — An Experimental Three Stage, One Kilowatt Class D Amplifier.
The unit operates up to 10 MHz yielding an efficiency of 85 percent. The power gain is 30 dB.
INTRODUCTION

The assumption is made that the reader is familiar with the types, construction, and electrical characteristics of FETS. References 1 and 2 contain information on this subject.

Silicon RF power FETs are generally N-Channel MOS enhancement mode devices. Most are vertical structures, meaning that current flow is primarily vertical through the chip with the bottom forming the drain contact. Vertical construction has the advantage of providing greater current density which translates to more watts per unit area of silicon.

The assembly of RF power FET wafers into finished devices is similar to the assembly of bipolar RF power transistors (BPTs). Identical packaging is utilized for both types of devices.

ADVANTAGES OF RF POWER FETS

The advantages of FETs have been described elsewhere,2,3 and will not be repeated in detail. Some observations on this subject are given below.

The inherently higher power gain is illustrated by a comparison of the MRF171 FET and MRF315 BPT. Both are VHF devices rated at 45 watts power output. Typical power gains at similar operating conditions (\(f = 150\) MHz, \(P_{out} = 45\) W, dc supply voltage = 28 V) are 15.0 dB for the FET and 11 dB for the BPT.

Any gain comparison should also include ruggedness data. Ruggedness is defined as the ability of a device to survive operation into mismatched loads. Obviously, UHF and microwave BPTs are available with gains exceeding that of the MRF171 FET at 150 MHz, but the higher frequency BPTs will not survive much abuse at VHF. The superior ruggedness of the FET is even more impressive when it is recognized that no source site ballasting is used.

Another gain comparison at VHF is provided by the MRF174 FET and MRF317 BPT. The MRF317 is rated at 100 watts output, and contains an internal input matching network which increases the device gain by typically 5.0 dB. The MRF174 is rated at 125 watts output and has no internal input matching, yet the typical gain of the MRF174 at 125 watts output is 12 dB while the typical gain of the MRF317 is 10 dB at 100 watts output (both devices operating at 150 MHz with a 28 Vdc supply).

Impedance differences are found mainly at the device input. FET input impedance at dc approaches infinity, dropping at VHF to a level approximately equal to, but slightly higher than the input impedances of comparable BPTs.

This point can be illustrated by considering again the aforementioned 45 watt VHF devices. When operating at 150 MHz with a 28 Vdc supply and 45 watts output, the large-signal input impedances are 1.89 + j4.81 ohms for the MRF171 FET and 1.2 + j1.0 ohms for the MRF315 BPT.

These devices illustrate another difference. The large-signal input impedance of FETs at VHF is capacitive. By contrast, most VHF BPTs with power outputs greater than 20 watts have an inductive input impedance at 150 MHz. The input impedance of the MRF315 passes through resonance at about 100 MHz.

The low-noise figure of the FETs facilitates the design of low-noise power amplifiers and high dynamic range receiver front ends. Noise figures of less than 3.0 dB at \(f = 150\) MHz, \(V_{DS} = 28\) V, \(I_{D} = 2.0\) A have been measured with the 125 watt MRF174. The MRF134 5.0 W VHF FET has a typical noise figure of 2.0 dB at 150 MHz, 28 V, 100 mA, and values as low as 1.5 dB have been measured. Transmitter noise floor determines the antenna front to back ratio required for duplex systems.

A most interesting FET characteristic is the inherent gain control mechanism. The power output of a FET amplifier can be varied from full rated output over a range of greater than 20 dB (with RF input power held constant) by varying the dc gate voltage. Further, the device gate does not draw dc current, so the dc source utilized for gain control does not have to deliver any power to the FET. This capability, which does not exist in the RF power BPT, facilitates the design of systems requiring gain control, either manual or automatic.
AMPLIFIER DESIGN

The design of TMOS FET RF power amplifiers has much in common with the design of BPT amplifiers. The amplifier must include dc circuitry to apply bias voltages and RF matching networks to perform the necessary impedance transformation over the frequency band of interest. Amplifier design consists of the synthesis of circuitry to perform the above tasks.

A positive dc supply voltage is required on the drain. To date most RF power FETs have been designed for the standard BPT operating collector voltages, i.e. 12.5 V, 28 V, and 50 V. Some higher voltage FETs are also available. The FETs described are designed for 28 V operation.

There is no FET parallel to the popular zero base bias BPT amplifier. The typical FET RF power amplifier requires forward gate bias for optimum power output and gain. That is the bad news; the good news is that the FET gate is a dc open circuit and the bias network may often be just a simple resistive divider.

A convenient gate bias source is the drain supply. When utilizing this technique care must be taken in filtering the bias circuitry. An inadequately filtered bias circuit connected to the drain supply can form an output-to-input feedback path for oscillations.

FET amplifier $I_{DQ}$ (quiescent drain current) is not critical and values in the 10-150 mA range are suggested. $I_{DQ}$ may be varied from less than 100 mA to values approaching Class A operation without large changes in gain and efficiency at full rated power. Linear applications are an exception to this where $I_{DQ}$ should be selected to optimize linearity.

The design of RF impedance matching networks for FET amplifiers is similar to the corresponding task for BPT amplifiers. These networks usually take the form of broadband transformers at HF, lumped reactive elements at VHF, and microstrip lines with RF chip capacitors at UHF.

Solid-state power amplifier drain or collector load impedances are set primarily by supply voltage and power level. Therefore, FET and BPT amplifiers with like performance parameters can utilize similar output networks.

The inductive input impedance of high power VHF BPTs usually dictates that the input network design include shunt capacitors placed as close to the transistor package as is physically possible. FETs, with their capacitive input impedances at VHF, do not require these critical capacitive circuit elements. Figure 1 shows a 125 watt 150 MHz amplifier which utilizes the MRF174 TMOS FET. Note the following items which have been discussed previously:

1. No shunt capacitors at the gate.
2. Resistive bias network operating from the drain supply voltage.
3. Impedance matching networks similar to those of a comparable BPT amplifier (except for item 1 above).

This amplifier operates from a 28 volt dc supply. It has a typical gain of 12 dB, and can survive operation into a 30:1 VSWR load at any phase angle with no damage. The amplifier has an AGC range in excess of 20 dB. This means that with input power held constant at the level that provides 125 watts output, the output power may be reduced to less than 1 watt continuously by driving the dc gate voltage negative from its $I_{DQ}$ value. Figure 2 illustrates this performance feature. Note that...
a negative voltage capability would have to be added to the bias system to take full advantage of this AGC performance.

Another useful feature of RF power FETs is that they have less variation of input and output impedances with power level than does a BPT. This characteristic permits the use of small-signal 2 port scattering parameters to develop useful design information for gain, stability, and impedances. S-parameters are often found on RF power FET data sheets. While s-parameters will not provide an exact design solution for high power operation, they do produce a useful first approximation.

Power FETs with outputs below the 40 watt range often have such high gain at HF and VHF that stability problems may be encountered. This problem can be addressed by the classic methods used to stabilize RF small-signal amplifiers — loading of input or output terminals, feedback, or both. Here is an area where s-parameters are useful in calculating the effects of circuit techniques for achieving stability. References 7 and 8 discuss amplifier stability.

Figure 3 shows a 5.0 watt 150 MHz amplifier utilizing the MRF134 TMOS power FET. The MRF134 is a very high gain FET which is potentially unstable at both VHF and UHF. Note that a 68 ohm input loading resistor has been utilized to enhance stability. This amplifier has a gain of 14 dB and a drain efficiency of 55%. Figure 4 shows a 5.0 watt 400 MHz amplifier with a nominal gain of 10.5 dB.

CAUTIONARY NOTES

Some precautions regarding FET RF power amplifiers should be mentioned.

One involves temperature coefficient. Literature abounds with statements that FETs are totally immune to thermal runaway because of their negative temperature coefficient. Actually, many RF power FETs have a positive temperature coefficient over a portion of their operating range. Increasing drain current usually shifts the coefficient from positive to negative. See Figure 5.

DC bias experiments have been conducted with several RF TMOS FETs. While they all had positive temperature coefficients over a portion of their operating ranges, none exhibited a tendency toward thermal runaway at drain currents ranging from less than 100 mA to full Class A bias. Thermal runaway does not appear to be a problem, but the positive temperature coefficients suggest that the designer should not completely ignore the thermal aspects of dc bias design.

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FIGURE 2 — Gain Control Performance of 125 Watt Amplifier

FIGURE 3 — 5.0 Watt, 150 MHz TMOS FET Amplifier

C1, C4 — Arco 406, 15-115 pF
C2 — Arco 403, 3-35 pF
C3 — Arco 402, 1.5-20 pF
C5, C6, C7, C8, C12 — 0.1 µF Erie Redcap
C9 — 10 µF, 50 V
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 3 Turns, 0.310" ID, #18 AWG Enamel, 0.2" Long
L2 — 3-1/2 Turns, 0.310" ID, #18 AWG Enamel, 0.25" Long
L3 — 20 Turns, #20 AWG Enamel Wound on R5
L4 — Ferroxcube VK-200 — 19/4B
R1 — 68 kΩ, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils

FIGURE 3 — 5.0 Watt, 150 MHz TMOS FET Amplifier

C1, C4 — Arco 406, 15-115 pF
C2 — Arco 403, 3-35 pF
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L1 — 3 Turns, 0.310" ID, #18 AWG Enamel, 0.2" Long
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R1 — 68 kΩ, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils
FIGURE 4 — 5.0 Watt, 400 MHz TMOS FET Amplifier

C1, C6 — 270 pF, ATC 100 mils
C2, C3, C4, C5 — 0-20 pF Johnson
C7, C9, C10, C14 — 0.1 µF Erie Redcap, 50 V
C8 — 0.001 µF
C11 — 10 µF, 50 V
C12, C13 — 880 pF Feedthrough
D1 — 1N53925A Motorola Zener
L1 — 6 Turns, 1/4” ID, #20 AWG Enamel
L2 — Ferroxcube VK-200 — 19/4B
R1 — 68 ft. 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
Z1 — 1.4” × 0.166” Microstrip
Z2 — 1.1” × 0.166” Microstrip
Z3 — 0.95” × 0.166” Microstrip
Z4 — 2.2” × 0.166” Microstrip
Z5 — 0.85” × 0.166” Microstrip
Board — Glass Teflon, 62 mils

the VHF frequency range. Particular attention was given to the excellent gain control characteristics of these devices.

REFERENCES
1. Field Effect Transistors in Theory and Practice, Motorola Semiconductor Sector Application Note AN-211A.
5. H. Granberg, Broadband Transformers and Power Combining Techniques for RF, Motorola Semiconductor Sector Application Note AN-749.
8. R. Hejhall, RF Small-Signal Design using Two-Port Parameters, Motorola Semiconductor Sector Application Note AN-215A.
MONOMAX — APPLICATION OF
THE MC13001 MONOCHROME
TELEVISION INTEGRATED CIRCUIT

Prepared by
Ben Scott
Technical Consultants:
C.I. Tsui, Hong Kong
Peter Bissmire, Geneva
Lowell Kongable, Phoenix
Mike McGinn, Tempe

This application note presents a complete 12” black and
white line-operated television receiver, including artwork for
the printed circuit board. It is intended to provide a good start­
ing point for the first-time user. Some of the most common
pitfalls are overcome, and the significance of component
selections and locations are discussed. The design has only 4
factory adjustments: H. Hold, Height, AGC Delay, and V.
Linearity, and there are no alignments.

Note that while this discusses MC13001 (525 line, positive
tuner AGC) there are also parts for 625 line and negative
tuner AGC, in all combinations.

INTRODUCTION
Monomax has been on the market since mid-1981. It
was originally developed in a joint effort between
Zenith and Motorola for the purpose of creating a high
performance B&W receiver. It was intended for all
types of monochrome receivers, including the demand­
ing portable and mobile applications, which require
immunity to noise, “airplane flutter” and multipath
signal conditions. Features suggested by these require­
ments included: noise filtering and cancelling, dual­
loop horizontal PLL, countdown vertical, and a flexible
AGC system.

It was also required that the resulting receivers be
low in component and manufacturing cost. To meet
this objective, effort was made to minimize external
components (especially precision components) and
adjustments.

Above all, the receiver was to be reliable, so the chip
was designed to operate at low voltage and low dissi­
pation. Special attention was given to ESD (electro­
static discharge) immunity on all pins. An extremely
stable horizontal oscillator was devised.

Additional features which resulted from this design
effort included: a completely integrated IF and detector
with no detector tuning or external filtering components,
an on-chip dc contrast control which permits remote lo­
cation of the control without shielded cable, and fully
black level clamped video with blanking and beam cur­
rent limiting. The combination of system functions in the
Monomax chip permitted some elegant solutions which
would not have been practical or economically feasible
in more conventional designs.

It is not the purpose of this AN to describe the overall
Monomax chip in any greater detail than is required
for understanding receiver design decisions. The reader
is urged to obtain a copy of the MC13001 data sheet
available from Motorola Literature Distribution or
Linear Applications. It contains some of the basic

MONOMAX is a trademark of Motorola Inc.
FIGURE 1 — Simplified Block Diagram

FIGURE 2 — Monomax Functional Block Diagram
application information which will not be repeated in this note. Also recommended is a paper entitled “Monomax — An Approach to the One-Chip TV” by Gerald Lunn and Mike McGinn of Motorola. This can be obtained from the proceedings of the IEEE Chicago Spring Conference on Consumer Electronics, June, 1981, or from Linear Applications, Motorola.

Monomax is not difficult to apply. A functional TV set is virtually assured on the first try. But as anyone closely associated with television design can attest, there are, in every new design, a number of small but objectional problems which stubbornly resist solution. The receiver described here does not represent the “last word”, but it is pretty close to production quality, and it includes solutions to some of the most common beginner’s problems. In the following text, an attempt will be made to explain component value choices and locations in terms of problems solved or behavior avoided, so that the future experimenter will be alerted.

THE BASIC DECISIONS/POWER SUPPLY

One of the first considerations in a new TV design is whether the set is to be ac/dc (12 Vdc operable) or ac line only. Monomax fits well into either, and has been used in production designs of both types.

Figure 3 shows the architecture of an ac/dc type with all systems operated from 12 Vdc. In this case, the horizontal output stage is of the “boost” type, to minimize horizontal deflection current and make the yoke easier to manufacture. The flyback transformer contains auxiliary windings which provide supply voltages for the video output, picture tube grids, and vertical deflection. Sometimes the boost voltage of 20 to 30 Vdc is used as a power supply for the vertical output. The audio output section is usually a Class B type, operated directly from 12 Vdc. An IC combining the sound IF, detector, and audio output is ideal in this architecture. TDA1190 is an example which fits well with Monomax.

Figure 4 shows the basic power supply structure for the ac line operated type of design. This is the most economical and the most common approach for B&W television in most of the world, and it is the subject of much of this AN. Special thought was given to this type of set in the design of the MC13001 itself. Note that the horizontal oscillator and driver are supplied through high value resistors directly from the rectified power line dc (120 V). Only 4.0 mA are needed into Pin 18 to power the horizontal oscillator system. The balance of the horizontal circuit is also line operated so it is fully operable from the line supply. The horizontal section then produces the 12-14 Vdc for the rest of Monomax (50 mA), and for the tuners, the sound IF, the vertical output, etc., about 150 mA in all. This method avoids the problem of developing 12 Vdc directly from the line; i.e., the waste of power in a linear approach, the extra components for a switch-mode dc-dc converter, or the cost of a line transformer. As in the previous example, the TDA1190 can be used for the entire sound system, but many designers prefer to use a Class A, line operated, discrete output stage, and one of the standard sound IF/detector ICs, such as MC1358, CA3065 or TBA120. This removes the 12 V supply ripple caused by loud low-frequency audio passages, but costs a small audio output transformer. This is the approach presented in the complete receiver in this AN, but it could be easily changed to the single-chip sound system.

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**FIGURE 3 — Basic AC/DC Architecture**
It is important to use good bypass techniques on all power supplies, not only for low frequencies, but also for RF. It is critical in prevention of faint but objectional vertical lines in the picture, caused by horizontal deflection system waveforms getting into the supplies. Good high-frequency bypasses on Pins 18 and 19, with respect to Pin 16, are essential.

THE IF

The four stage IF in the MC13001 has 80 µV sensitivity, sufficient for excellent overall performance when used with an ordinary tuner and a conventional L/C input bandpass network. It is recommended that the input always be used differentially to reduce the possibility of feedback problems. The differential input capacitance decreases from its normal 5.0 pF, to about 2.0 pF, in the top 10 dB of gain-range of the IF. This can be used to narrow the input L/C filter, at very weak signals, to reduce overall detected noise, and improve picture lock.

If a SAW (surface acoustic wave) filter is used, as in this AN, the above bandpass “walking” technique cannot be used. Furthermore, if a SAW filter is used, an additional fixed gain-preamplifier is needed to overcome the 20 to 25 dB loss thus imposed. Nevertheless, this approach has become increasingly popular with the introduction of low cost SAW filters, because it eliminates a crucial and time consuming production alignment.

There is a steadily increasing supply of SAW filters in the marketplace, so some criteria for choosing the best one for the design are in order. Bear in mind that all of the video selectivity is concentrated in the tuner and the IF input filter in this design. In a B&W receiver, it is important to obtain a good compromise of picture and sound quality with a single selectivity channel. This means keeping color and sound subcarriers low enough to avoid 920 kHz beat generation in the detector, and yet not attenuating the sound so deeply that good sound quieting is irretrievably lost. A well-proven characteristic for achieving this goal is as shown in Figure 5, taken from tuner-mixer input to detector. Of this, some selectivity comes from the mixer-tuned circuits, but most of it is provided by the SAW filter.

Table I shows some available types, data normalized to 0 dB picture carrier. The major difference is the depth of 41.25 MHz. In this regard, the Toshiba F1032U, Kyocera, and the muRata parts are best for B&W design. The mixer-tuned circuits will supply the

![FIGURE 4 — Line Operated Architecture](image)

![FIGURE 5 — IF Bandpass Characteristic](image)
TABLE 1 — Some Available SAW Filters

<table>
<thead>
<tr>
<th>Relative Response</th>
<th>Toshiba F1032B</th>
<th>Toshiba F1032U</th>
<th>Toshiba F1032V</th>
<th>Toshiba F1052</th>
<th>Kyocera KAF45MR-MA</th>
<th>muRata SAF45MC 027</th>
</tr>
</thead>
<tbody>
<tr>
<td>39.75 Adjacent Picture</td>
<td>-40</td>
<td>-48</td>
<td>-45</td>
<td>-40</td>
<td>-37</td>
<td>-37</td>
</tr>
<tr>
<td>41.25 Sound</td>
<td>-12</td>
<td>-16</td>
<td>-6.5</td>
<td>-25</td>
<td>-18</td>
<td>-19</td>
</tr>
<tr>
<td>42.17 Color</td>
<td>+1.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Peak</td>
<td>+4.0</td>
<td>+4.0</td>
<td>+4.0</td>
<td>4.0</td>
<td>4.0</td>
<td>4.0</td>
</tr>
<tr>
<td>45.75 Picture</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>47.25 Adjacent Sound</td>
<td>-45</td>
<td>-48</td>
<td>-47</td>
<td>-40</td>
<td>-42</td>
<td>-38</td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>-18</td>
<td>-19</td>
<td>-18</td>
<td>-21</td>
<td>-23</td>
<td>-20</td>
</tr>
</tbody>
</table>

additional slight amount of narrowing required. The F1032V part is too wide, and F1052 is too narrow. These are intended for color receiver architectures of different types. The SAW manufacturers loading recommendations should be adhered to closely to prevent ghosts (before and after the picture) caused by capacitive feed-through and/or "triple transit" reflections.

At the input of the MC13001, it is important to use good bypass capacitors on Pins 2, 4 and 6 with respect to Pin 1 of the MC13001. The best value was found to be a straight lead, low-inductance 0.02 µF disc ceramic for reducing the infamous channel 6 beat. Pickup in this area is also a possible source of vertical scan bars in the picture caused by horizontal sweep currents. It is desirable to keep the SAW filter close to Pins 1, 2, 4 and 6. See the PC board layout Figure 14. Also, the IF preamplifier must be kept compact and well grounded to prevent feedback and oscillation with the tuner.

AGC

The AGC system was implemented here essentially as described in the Data Sheet, including the AGC speed-up capacitor between Pins 9 and 10. This keeps the AGC airplane flutter response time fast, even when the signal is strong enough to move the AGC into the tuner control region. The IF AGC delay setting is one of only 4 factory adjustments. Ideally it should be made with a calibrated signal level, but acceptable results can be obtained with a strong off-the-air signal and a switch type attenuator. A discussion of this adjustment is contained in Appendix I.

Remember that AGC loops have a large amount of gain, and fast AGC loops, with good airplane flutter performance, are especially vulnerable to deflection currents. Only a few millivolts on the AGC lines from stray fields or ground loops can cause a significant "bar" in the picture. Keep the tuner AGC lead away from yoke leads. The small bypass capacitor on Pin 11 further reduces this problem, and should be placed as close to the MC13001 as possible.

Monomax was designed so that in the strong signal region, "above the delay", the IF gain is held constant while AGC acts upon the RF stage in the tuner. This means that a small amount of IF AGC range may not be accessible in the normal implementation. Optimum setting of the delay pot keeps the RF section at maximum gain for RF signal levels of from <10 µV to 1.0 mVrms, using 40 dB of the IF AGC range. The tuner is not likely to be able to provide more than 40-46 dB of additional AGC, which will accommodate signal levels up to approximately 200 mVrms. This is adequate for the Monopole antenna applications, but certainly doesn't offer a lot to spare. Above this level, the AGC system loses control, the receiver overloads and eventually falls out of sync. One way to improve this, and pick up the remaining 6.0 dB or so of IF AGC capability, is to put a resistor from Pin 11 to Pin 10. The value of the resistor will be about 33 k for delay resistor values shown, but will have to be tailored to the particular tuner used. This can also be accomplished by a resistor from Pin 9 to Pin 10. This, in fact, is the only solution in parts providing negative tuner AGC.
THE SYNC SEPARATORS

Composite sync is stripped from noise-cancelled video in a peak detecting sync separator, as shown in Figure 2. The time constants for setting the slice level of the detector are connected at Pin 7. As always, there is the compromise between optimum noise immunity and tilting of the slice level during vertical interval. For best horizontal separation, a short time constant is required. There is also an AGC anti-lockup system which responds to the voltage at Pin 7. It also requires a short time constant. A second, longer time constant can be diode connected to the same pin, to prevent too much charge-up during the vertical interval.

Composite sync is subsequently integrated internally and fed to another amplifier whose emitter is brought out at Pin 23. Satisfactory vertical sync can be obtained (internally) by simply connecting Pin 23 to a divider. Weak signal performance can be improved by using an RC network on Pin 23 to make the separation self compensating, as in the horizontal separator. Also AGC from Pin 9 can be fed to Pin 23 to improve airplane flutter vertical hold.

FLYBACK INPUT

The only flyback pulse input to the MC13001 is at Pin 15. It takes care of keying the AGC, blanking the video output stage, and phase locking the horizontal system. The Pin 15 input is a base-emitter junction, with a reverse polarity diode for protection. The input requirement is for a negative-going pulse of 0.6 mA, but it is best to choose a pulse voltage and series resistor to give about -2.0 mA peak. This will make the effective width be the pulse width near its base.

HORIZONTAL OSCILLATOR/AFC

Monomax contains a really unique group of features in this area: dual-loop; variable-loop-gain (bandwidth) on the first (sync) PLL; externally adjustable phasing in the second PLL; simple flyback pulse input, requiring no ramp generation. These are described in detail in the data sheet, and will not be repeated here.

Shown in Figure 8(a) are the first PLL components as presented in earlier publications, and in 8(b) a new variation which has been implemented in this receiver. This very simple change retains the dual time constant on the phase detector. The improvement is the 13 k/22 k divider which sets a 5.0 V point for the return of the longer time constant filter. Since 5.0 V is the reference level in the oscillator, it is also the operating voltage at Pin 12, and at Pin 13 when in lock. The benefit, then, is that the 0.47 µF doesn't have to charge up, so there's very little frequency pulling during power-up or power-down. This reduces audible chirps and momentary stresses due to long cycles on the horizontal output device. Also the picture locks-in quickly, which is highly desirable with fast warm-up picture tubes.

Note that the proper setting of the horizontal hold control occurs when no average current flows through the 390 k resistor, either to, or from, the oscillator. A simple alignment procedure is to set the average Pin 12 to Pin 13 voltage to zero by adjusting the hold control, when locked to a standard broadcast signal, using a high impedance voltmeter.

The second horizontal phase detector compares the flyback output phase with that of the oscillator, and develops a proportional dc voltage, which is filtered at Pin 14. This dc voltage then sets the slice level on the oscillator ramp to produce the output timing desired. See Figure 9(a). Picture phasing can be adjusted slightly by a high value resistor on Pin 14 to +8.0 V or ground. A 220 k to +8.0 V will move the picture about 2.0 µs to the left. A 220 k to ground will move it 2.0 µs to the right.

Another application of Pin 14 provides a method of changing the duty cycle of the horizontal output waveform from Pin 17. Normally, the desired waveform would be 50%. This has been assured in the MC13001 by operating the slicer at 31.5 kHz. This permits output phasing correction without changing duty cycle, as shown in Figure 9(a). In some receivers, when large amounts of dc power are drawn from the flyback, the “on” time of the horizontal output may have to be more than 50% of the cycle. This can be accommodated by feeding back some driver collector signal to the second phase detector filter, as shown in Figure 10. This imposes alternate slice levels and hence, the desired change of duty cycle. Some tentative values for a set configured like the one in this AN are given in Figure 10. This was not actually used in the final design, because it wasn’t needed. It is supplied here as a reference for future designs having more power drain from the horizontal output. Bear in mind that the driver collector voltage would be much lower in the 12 Vdc receiver architecture mentioned earlier, requiring much different values to implement this idea. A practical limit of control by this technique is about a 60/40 duty cycle. The 0.001 capacitors on Pin 17 and the driver base are to “soften” waveform edges, to reduce their radiation into signal circuits.
THE VERTICAL SYSTEM

Aside from all of the sophistication of the countdown vertical system within the Monomax chip, what remains to be accomplished outside of the device is fairly conventional. At Pin 20, there is an external capacitor, charged from a high voltage, to produce a good linear ramp. It is discharged within the chip, usually by vertical sync, but sometimes by the countdown circuit when sync is momentarily absent. It is important for the capacitor to be a good stable low ESR type and to be located close to Pin 20 and grounded as closely as possible to Pin 1 to avoid pickup of horizontal sweep which could hurt interlace.

The approximately 1.5 Vp-p waveform on Pin 20 is inverted and buffered to Pin 22 to drive the external output circuit. In the receiver design in this AN, a fairly conventional vertical output stage has been used. An optional linearity control has been added, because many customers like to have one, but also because it permits using a smaller coupling capacitor for the yoke. The smaller coupling capacitor saves money and reduces picture bounce, but introduces some curvature which must be compensated. Feedback to Pin 21 provides overall output stage linearization and prevention of deflection current change with temperature. It is also a handy place to feedback a variable parabolic waveshape for linearity control, as shown in Figure 11.

THE SOUND SECTION

The buffered video detector output at Pin 28 is a wideband signal used for sound take-off. A ceramic sound take-off filter and detector “tank” were chosen to eliminate alignment steps. The MC1358 is a popular, multi-sourced, FM IF, detector and dc volume control. It can be used with conventional L-C circuits or the ceramic devices shown here. The L-C application costs less in piece parts, but has a higher manufacturing cost in assembly and alignment.

Keep in mind that a limiting IF produces a wide spectrum of 4.5 MHz harmonics. The sound IF grounds should be kept together and returned to Pin 1 by a single path as shown in the copper layout of Figure 14. Also it is a good idea to keep the input of the sound IF IC close to Pin 28 to reduce radiation of video IF harmonics, generated in the video detector, from getting back to the tuner or IF input.

In the receiver described here, an ac volume control has been used. A potentiometer is placed between the MC1358 detector output, Pin 8, and the post amplifier input, Pin 14. The dc volume control, Pin 6, is grounded for maximum volume. If the volume control is to be mounted some distance away, and deflection pickup is likely, then the dc volume control could be a better choice. This can be done by ac coupling Pin 8 to Pin 10, and placing a variable 50 k pot from Pin 6 to ground. The disadvantage is that the control contour is less predictable in the dc control configuration. It is, nonetheless, a production proven method.
THE VIDEO OUTPUT

Pin 24 provides up to 1.4 V, black-to-white video drive, black level clamped, with a widened and amplified blanking pulse added. This is sufficient to drive a single stage common-emitter video output transistor. A dc voltage of 0 to 5.0 V applied to Pin 26, varies the black-to-white amplitude at Pin 24 from 1.4 V to 0.1 V without changing the absolute black level of the output voltage. Beam current limiting can also be used to control maximum brightness. This is accomplished by circuit shown in Figure 12. As beam current increases, the H.V. winding current flowing in the 39 k resistor, pulls the Pin 27 voltage down. When Pin 27 falls below about 1.0 V, the contrast begins to be reduced. This circuit was not used in the complete receiver in this AN, for reasons which will be explained shortly.

The black level clamp capacitor on Pin 25 is usually shown connected to ground. It can also be connected to +8.0 V to cause the screen to be blanked for about 1 second after turn-on. This permits the scan systems to stabilize before the picture becomes visible. Note: If the brightness control design window is set too high, the raster may still be visible during start-up.

The video output circuit can take many forms. Monomax was designed to accommodate full dc coupling, as described earlier. However, many TV designers, and users, don’t like full dc coupling, because it sometimes seems to go too black, creating the suspicion that some information is hidden. Also, a directly coupled video output to picture tube cathode usually requires a negative voltage for at least one of the grids for proper set-up at high contrast settings. Finally, fully dc coupled designs are harder to protect from power-off flash or spot burn.

For these reasons the receiver described in this AN was a partially dc coupled type. This puts the brightness control in the cathode circuit, removes the need for the brightness limiting configuration, and makes spot/flash prevention easier. (The diode and electrolytic in G1 are for this latter purpose).

In the video output stage emitter, some dc set-up from the +12 V supply has been used to adjust the output dc level, to minimize overall dissipation. Also some additional vertical blanking has been fed through a diode, from the top of the vertical yoke. This blanking will be accomplished in the IC internally in later Monomax devices.

FIGURE 12 — Beam Current Limiting
APPENDIX I — AGC DELAY ADJUSTMENT

Ideally, a known antenna signal level of 1.0 mV (300 n balanced) or 500 µV (75 n unbalanced) is supplied to the tuner input. This signal level corresponds to the threshold of “snow” in the picture, for most receivers. With this signal level, the AGC delay pot is turned until the RF AGC voltage just begins to rise, and then is backed off slightly. The picture should be snow-free. If the RF AGC is permitted to rise, the picture will start to show some snow, which therefore represents less than optimum overall performance. If the setting is backed-off too much, the delay may be too large and mixer overload may occur at stronger signals.

The correctness of this setting should be checked at weaker and stronger signals. At weaker signals, say 6.0 dB down, it should not be possible to improve the picture noise by resetting the RF Delay. At stronger signal, say 40 dB stronger, there should be neither snow or overload evident in the picture, although the distance between these two conditions, as a function of delay setting, may be very narrow. The AGC system should automatically avoid these troubles. It may be necessary to make a slight compromise to avoid overload, which may produce a slight amount of snow in the 1.0 mV picture.

The above compromises can be achieved successfully without calibrated signals, with just a switchable attenuator and a strong signal. Starting at strong signal, note the available AGC Delay setting range between picture overload and snow. Using the switched attenuator, reduce the signal strength and make sure that neither problem appears. If necessary tweak the Delay, but don’t move outside the original range. Eventually the picture will get snowy, but the control will only be able to make it snowier. Setting it to the optimum (just barely) should still be within the noted range.

APPENDIX II — COMPONENT & CONSTRUCTION DETAILS

In order to make the enclosed PC board pattern easy to use, the following components are recommended: Remember that these are pertinent to this design architecture and this specific design. Many variations are possible with a little redesign work.

Flyback — Gold Star Type 154-028A with self-contained H.V. rectifier. Certainly, substitution is possible, but very careful attention to pin-outs and taps is required. The primary is, of course, a 120 Vdc type, which corresponds to about 800 Vp-p positive pulse at Pin 2. Pin 3 is a negative going pulse of 35 Vp-p and Pin 7 is a negative-going pulse of about 120 Vp-p. The H.V. terminal, which is internal in the above model, would be a positive going pulse of about 12 kVp-p. Very little flexibility can be permitted on these values. Be careful to watch pin-outs and horizontal polarity.

Yoke — Gold Star Type 153-020A for 90° 12” — 20 mm neck picture tube. It requires approximately 1.0 Ap-p in both horizontal and vertical windings to give proper overscan in the 90° tube at 10-11 kV. This means a horizontal (saddle) winding of about 3.4 mH and a vertical (toroid) winding of approximately 3.0 Ω, 10 mH. Numerous substitutions are available, but the above values must be adhered to for this set architecture.

Horizontal Output Transistor — The board was designed for a TO-3 type, such as a BU205, BU204, or MJ12003. A plastic TO-220 type MJ12007 will do the job with some mechanical revision. The important parameters are \( V_{(BR)CEX} = 1300 \text{ V} \) and \( I_C = 2.0 \text{ A} \). A small amount of heat sinking, such as a U channel with 2 flags of 1 square inch each is recommended. A mica or Thermalloy isolator is suggested to reduce shock hazard to the experimenter. If an ac/dc design is contemplated, as referred to back in Figure 3, a lower voltage, higher current part like BU806 will be required for the horizontal output, along with a different yoke and flyback.

Vertical Output Transistors — It is possible to “get by” with a TO-92 complementary pair, such as MPS6560 and MPS6562, or the new, tall TO-92, MPSW01 and MPSW51. However, the author’s opinion is that these operate too hot, with dissipation approaching 1 watt, each, worst case. Recommended alternatives include D40E1 and D41E1 in the TO-202, or TIP29 and TIP30 in TO-220. No heat sink is required. The devices need only \( V_{(BR)CEO} = 30 \text{ V} \) and good hFE at 1.0 A.

Video Output Transistor — For the load value shown in this design, a case 152 uniwatt, such as MPSU10, is best. The 300 V \( V_{(BR)CEO} \) is not needed, but the device must be “small geometry”; i.e., high \( f_t \) and low \( C_{oh} \) to preserve picture resolution. A tall TO-92 or even an MPSA43, TO-92, can be used if the collector load is increased to 6.8 k, but some picture quality will be lost.

Audio Output Section — The transformer should be approximately 30:1 turns ratio, capable of handling 1 watt into 8.0 Ω. The output transformer should be set up at about \( I_Q = 12-14 \text{ mA} \), and should be capable of 1.5 W continuous dissipation. A TO-220 type MJ23607, mounted on at least 3 square inches of aluminum is suggested.

H. Driver Stage — In the prototype receiver, the available driver transistor had only about 12:1 turns ratio. This necessitated a large wattage dropping resistor to provide the rather low-voltage, high-current primary waveforms. It would be better to obtain a transformer of 30:1 or so, to permit a more efficient driver stage. The 4.3 k / 2.0 W resistor could then be reduced considerably. In either case a TO-92 driver type MPSA42, is a good choice.

SUMMARY:

Figures 13 and 14 provide the copper pattern for the PC board and the component locations. Note that signal input circuits are compact and grounded near Pin 1. Subsequently these and all other circuits are connected to the central ground at Pin 16, without being interconnected beforehand. The full receiver schematic is given in Figure 15.
The most popular method used in modern television receivers to synchronize the line frequency oscillator is the phase locked loop. Although in detail the circuits may vary considerably, the fundamental operation is the same. Any designer with a good understanding of phase locked loops in general and the required operating characteristics of television line frequency oscillators in particular, should be able to handle these circuits successfully.

For color television signal transmissions in the United States, the line frequency \( f_H \) is directly related to the color subcarrier frequency \( f_{sc} \) such that:

\[
f_H = \frac{2 \times f_{sc}}{455}
\]

Since \( f_{sc} = 3.579545 \text{ MHz} \pm 10 \text{ Hz} \), then the line period is given by:

\[
H = 63.5555 \pm 0.0002 \text{ µs}
\]

1. Dynamic Phase Accuracy:
   - Dynamic phase accuracy: If the phase of a scan line is shifted with respect to the preceding line, a loss of detail can occur. For a given video frequency, a half cycle error from line to line will cause a complete loss of information at that frequency. At the system limit of 4.5 MHz, this corresponds to a 0.111 µs timing error between adjacent lines or a repetitive phase accuracy of 0.62 degrees. Should thermal noise be present in the signal, the miss-timing will be masked and much larger phase errors are tolerable. (See later discussions on noise performance.)

2. Static Phasing:
   - Static phase error with the line oscillator at nominal frequency \( f_H \). For monochrome receivers, this is determined by the tolerable shift of the picture information with respect to the raster and may be as much as 1.5 µs. For color receivers, it is generally much less (< 0.5 µs) to permit gating the burst information on the back porch of the signal.

3. Static Phase Error (with detuning):
   - When the line oscillator is detuned from the nominal line frequency, the timing between the picture information and the receiver raster will change. For an inexpensive monochrome receiver, this error can be large (2 µs for \( \Delta f = 300 \text{ Hz} \)), particularly if the screen is overscanned and the picture escutcheon masks the sides of the raster. For a color receiver, the S.P.E is usually smaller. Figure 1 gives the tolerance of the burst envelope on the signal back-porch and shows that the burst can occupy a 3 µs 'window' with respect to the leading edge of the sync pulse. The gating pulse for the burst channel is as narrow as possible to keep the chroma system noise bandwidth low and to prevent gating adjacent picture information or sync widgets. A gate pulse of 4 µs accurately centered when the line oscillator is at \( f_H \) will permit an S.P.E. of ±0.5 µs and yet maintain proper gating. Thus, for optimum performance, the S.P.E. over the detuning range of the line oscillator should be no more than ±0.5 µs.
4. Hold-In Range:
This is the total frequency deviation from \( f_H \) over which an already synchronized oscillator will remain in synchronism, with no interruption of the synchronizing signal. This can typically be from 600 Hz to 800 Hz but is not usually designed for and occurs as the result of other design considerations.

5. Pull-In Range:
This is the total frequency deviation of the line oscillator from \( f_H \) over which the receiver will remain in synchronism, even following a momentary interruption of the synchronizing signal. Expressed another way, it is the limits of free-running oscillator frequency from which the oscillator will pull into synchronism on application of a synchronizing signal. The required pull-in range will depend on the frequency stability of the line oscillator and the permissible static phase error. It is usually \( \pm 180 \) Hz.

6. Pull-In Time:
The time taken to synchronize from the limits of the pull-in range. Anything less than 1 second is considered instantaneous.

Four parameters are of primary interest: the phase detector sensitivity, the oscillator sensitivity, the loop gain, and the filter transfer characteristic.

1. Phase Detector Sensitivity (\( \mu \)):
The phase detector compares the incoming synchronizing signal with the line frequency oscillator signal and develops a control voltage that is proportional to the magnitude and polarity of the phase difference between the signals. If for a given phase difference at the phase detector of \( \delta \phi \) a control voltage \( \delta E \) is generated, then the phase detector sensitivity is defined as:

\[
\mu = \frac{\delta E}{\delta \phi}
\]

and is usually measured in volts/radian.

Since we are dealing with rectangular sync pulses and the signal from the oscillator is usually integrated to form a linear ramp, the phase detector output

\[
E = \mu \phi
\]

This is true over the stable operating region of the phase detector. (For further discussion of the stable and unstable operating regions, see Pull-In Range calculation on page 6.)

2. Oscillator Sensitivity (\( \beta \)):
If a voltage \( \delta E \) at the control terminal of the oscillator produces a change of \( \delta f \) in the free-running frequency of the oscillator, then the oscillator sensitivity (\( \beta \)) is defined as:

\[
\beta = \frac{\delta f}{\delta E}
\]

and the usual units are hertz/volt.

3. D.C. Loop Gain (\( f_c \)):
When the oscillator has a tuning error of \( \Delta f \) Hz, then the required correction voltage at the control terminal of the oscillator is \( \Delta f / \beta \). If the system is capable of producing this correction voltage, the oscillator will remain in synchronism and the output voltage from the filter will be d.c. If the filter has a d.c. transmission of 100\%, the phase detector output is \( \Delta f / \beta \) and a static phase error of \( \phi \) will exist between the inputs of the phase detector to maintain this voltage.

\[
\therefore \mu \phi = \Delta f / \beta
\]

or

\[
\phi = \frac{\Delta f}{\mu \beta}
\]

The quantity \( \mu \beta \) is defined as the d.c. loop gain (\( f_c \)) although its units are Hz/rad.

It is clear that the S.P.E. is directly proportional to the error in oscillator free-running frequency and is inversely proportional to the d.c. loop gain. The S.P.E. can be made as small as desired for a given tuning error by increasing the d.c. loop gain. However, note that the phase error \( \phi \) thus far defined is the static or long term phase error. To determine the dynamic phase error, i.e., the effect of impulse or thermal noise of the loop performance, we must evaluate the loop filter characteristics.

4. Filter Transfer Characteristic \( F(p) \):
The low pass filter connected between the phase detector and the oscillator will have a significant effect on the loop performance. As this part of the system is the one most open to design adjustment, it should be fully understood. If single time-constant networks are used, it
becomes impractical to achieve both small S.P.E.'s and small dynamic phase errors (low noise bandwidths) since the former requires a large value for $f_c$ and the latter a small value for $f_c$. To avoid this compromise, more elaborate networks are used.

Both a) and b) are equivalent “proportional plus integral” networks. The output control voltage is proportional to the current through $R$ plus the integral of the current in $C$. At any frequency, the ratio of the output voltage to the input voltage is:

$$F(p) = \frac{1 + pT_1}{1 + pT_2} \text{ where } T_1 = \frac{xRC}{1 + x} \text{ and } T_2 = \frac{(1 + x)RC}{1 + xRC}$$

:: $F(p) = \frac{1 + pR}{1 + (1 + x)R}$

At d.c., the filter transmission $F(p) = 1$ and at high frequencies, the above expression reduces to $\frac{x}{x + 1}$.

**AC gain ratio** $m = \frac{x}{x + 1}$

The parameter $m$ becomes important in the design of satisfactory loops.

**FIGURE 4 – Filter Frequency Characteristics**

5. **Dynamic Phase Error or Noise Bandwidth:**

Noise can be specified by its energy content and for a flat energy spectrum impulse noise and thermal noise are quite distinct. The relative phases of the frequency components of impulse noise are related and not random, although occurrence is a random variable. For thermal noise, the relative phases of the frequency components are completely random and incoherent and this type of noise is the most difficult to reject. Therefore, most of the following treatment is concerned with the rejection of thermal noise. However, methods to minimize the effects of impulse noise are also covered below in the selection of the filter components.

The presence of thermal noise in the signal will cause random variations in the output phase of the voltage controlled oscillator. An excellent way of determining the ability of the APC loop to reject thermal noise is to measure the noise bandwidth. This can be done by assuming a noise free input phase which has sinusoidal variation with time and calculating the corresponding output phase. If this is repeated over a range of frequencies, the bandwidth for which the loop has significant variations in output phase can be determined, i.e., the noise bandwidth has been found.

For a loop that is initially phase locked, if the input phase changes to $\phi_1$ with a corresponding output phase change of $\phi_2$, the resulting phase error of the system

$$\phi = \phi_1 - \phi_2$$

and the phase detector output voltage is $\mu \phi$.

For a filter transfer function of $F(p)$, the oscillator control voltage becomes

$$F(p) \mu \phi$$

and the oscillator (with sensitivity $\beta$) will attempt to change frequency by

$$F(p) 2\pi \mu \beta \phi$$

If frequency lock is to be maintained, the frequency shift of the oscillator must match the rate of change of the filter output phase

$$\phi_1 = \phi_0 = F(p) 2\pi \mu \beta \phi$$

and the phase detector output voltage is $\mu \phi$.

For a filter transfer function of $F(p)$, the oscillator control voltage becomes

$$F(p) \mu \phi$$

and the oscillator (with sensitivity $\beta$) will attempt to change frequency by

$$F(p) 2\pi \mu \beta \phi$$

or

$$\phi_1 = \phi_0$$

The phase transfer ratio

$$\phi_0 = \frac{\phi_1}{\phi_1} = \frac{F(p)}{F(p) + P/\omega_c}$$

Now for either of the filters shown in Figure 3,

$$F(p) = \frac{1 + pR}{1 + p(1 + x)R}$$

putting $RC = T$

$$P = j\omega$$

and

$$Q(\omega) = \frac{1 + j\omega T}{1 - \omega^2(1 + x) T/\omega_c + j\omega (xT + 1/\omega_c)}$$

It is important to note the presence of $\omega_c$ in the above expression. While the filter can modify the control voltage applied to the oscillator, the final output phase will depend on the loop gain $f_c$. The S.P.E. can be modified for a given detuning by changing $f_c$ alone. The dynamic phase error can be modified by changing either $f_c$ or $F(p)$, or both.
The equivalent noise bandwidth is found by squaring the $Q(\omega)$ curve and finding the rectangular bandwidth of the same height enclosing the same area. (See also CER100, page 11.)

**FIGURE 5**

A plot of $Q(\omega)$ against input frequency (noise frequency) will show the ability of the loop to reject thermal noise in the synchronizing signal.

The integration is carried out from $-\infty$ to $\infty$ since the abscissa does not represent the absolute frequency of the noise but the difference frequency between the noise and the oscillator frequency as detected by the phase detector. The phase detector output does not distinguish between frequencies above or below the oscillator frequency. A term commonly used for APC loops is the noise semi-bandwidth $f_{nn}$:

$$f_{nn} = \frac{1}{2} \int_{-\infty}^{\infty} |Q(\omega)|^2 \, df$$

Thus $f_{nn}$ is found by integrating $|Q(\omega)|^2$.

6. Other Synchronized Loop Characteristics:

It should be clear from (5) above that if $x \neq 0$ (1) for a given value of d.c. loop gain to produce satisfactory static phase performance, two parameters are available to produce satisfactory dynamic phase performance ($x$ and $T$).

If the filters of Figure 3 are simplified by pulling $x = 0$,

then eq. (5) reduces to

$$\omega_n = \frac{\Delta \omega}{\phi}.$$ 

Thus with $x = 0$ and a given detuning error, the S.P.E. and $f_{nn}$ cannot be chosen independently.

To obtain an idea of the best way to vary these parameters, assume that $\phi_i$ and $\phi_0$ are the voltage input and output of a low pass filter (Figure 6).

**FIGURE 6 - Equivalent Voltage Transfer Filter**

Step inputs to this filter can easily cause ringing. The output, following a step change in input phase (from signal source switching or a temporary spike of impulse noise) will assume a steady state following a transient.

$$\frac{\phi_0}{\phi_i} = Q(p) = \frac{1}{1/C_1 + \frac{1}{R\omega_c} + \frac{1}{\phi_i} + \frac{x}{R\omega_c}}$$

The steady state (particular solution) is $\phi_i - \phi_0 = \phi$. The transient (complementary function) is given by:

$$Q(p) = \frac{\phi_0}{\phi_i}$$

Solving for $p$, we have:

$$p = -(1+xT\omega_c) \pm \sqrt{(1+xT\omega_c)^2 - 4(1+x)T\omega_c}$$

The real part of (6) will give the natural undamped resonant frequency of the loop.

$$\omega_n = \frac{\sqrt{4(1+x)T\omega_c}}{2(1+x)T}$$

The quantity under the root sign in equation (6) will determine the response of the loop to a step input. For critical damping, this quantity will be zero.

$$(1+xT\omega_c)^2 = 4(1+x)T\omega_c$$

If we define a damping coefficient $K = \frac{(1+xT\omega_c)^2}{4(1+x)T\omega_c}$

then, $K = 1$ and the loop is critically damped.

$K > 1$ and the loop is overdamped.

$K < 1$ and the loop is underdamped and a period of oscillatory ringing will occur.
The values of \( \omega_n \) and \( K \) will have a significant effect on the loop synchronous performance. If \( \omega_n \) is low \( K > 1 \), the system may take an appreciable time to reach a stable state following a change of input phase. Therefore, there will be little transient disturbance from impulse noise because of the sluggish reaction of the loop. However, if the input phase changes as a result of airplane flutter, the loop may respond too slowly to produce satisfactory tracking of the input signal. Also, the pull-in from an asynchronous condition may be sloppy and slow. Conversely, if \( \omega_n \) is increased and \( K < 1 \), the loop can respond very rapidly to incoming phase changes, but may be unstable with oscillatory ringing when impulse noise is encountered. Suitable design values will depend on the required characteristics and the interaction of the APC loop with other subsystems in the receiver and these will be discussed in detail later. In general, it can be assumed that \( x << 1 \) and \( xT\omega_c >> 1 \) so that the formulae derived above can be simplified.

\[
\phi = \frac{\Delta f}{f_c} \quad (1)
\]

\[
f_{nn} = \frac{1 + x^2T\omega_c}{4xT} \quad (5)
\]

\[
\omega_n = \frac{\omega_c}{(1+x)T} \quad (7)
\]

\[
K = \frac{x^2T\omega_c}{4} \quad (8)
\]

7. Asynchronous Performance of the Loop:

As the tuning difference (\( \Delta f \)) between the oscillator free-running frequency and the incoming synchronizing signal increases, a larger static phase error is required at the inputs to the phase detector to maintain synchronism. Eventually, the phase detector output will stop increasing as the S.P.E. increases and the limit of hold-in will be reached(2). Should a further increase in \( \Delta f \) occur, the system becomes unstable and falls out of lock.

When the loop is out of synchronism, the phase detector will have two regions of operation (see Figure 7). If the sync pulse coincides with the steep slope of the integrated pulse from the V.C.O., this is the normal or stable operating region. The loop gain \( f_c \) is large and positive. When the sync pulse coincides with the more shallow slope of the sawtooth, operation is in the unstable region and the loop gain is much lower and negative.

Notice, however, that the phase detector outputs always operate to reduce the period of the beat note produced by the frequency difference between the sync and sawtooth. Hence, the beat note is very asymmetrical and has an average d.c. output at the filter terminal. As \( \Delta f \) decreases, the average d.c. voltage will build up on the filter capacitor until pull-in is achieved.

\[
\text{If the maximum output from the phase detector is } +f \text{ (obtained at points a and b on the sawtooth), then for the stable regions}
\]

\[
f_c = \frac{2 \beta E}{\phi_s}
\]

and for the unstable region \( \phi_{\mu} \)

\[
-f'_{c} = \frac{2 \beta E}{\phi_{\mu}}
\]

\[
\therefore f_c\phi_s = f'_{c}\phi_{\mu}
\]

Two assumptions are implicit in the above: (1) the oscillator sensitivity (\( \beta \)) remains constant over the range of control voltages produced by the phase detector, and (2) the integrated fly-back pulse is a linear ramp. For a typical diode bridge phase detector, the width of the narrow slope of the sawtooth is the stable region. However, the above expressions will still hold even if this is not the case. Should the phase detector output limit at a' and b' on the slope, the areas under the loop gain curve are reduced.

(2) The Static Phase Error \( \phi = \frac{\Delta f}{f_c} \) and \( \phi_{\max} = \frac{\phi_s}{2} \)

\( \phi_s \) = width of stable operating region of the loop.)

\[
\therefore \text{Maximum hold-in range } \Delta f_{\max} = \frac{f_c\phi_s}{2} \quad (10)
\]
correspondingly with new stable and unstable regions $\phi'_s$ and $\phi'_w$ (this limitation could also be caused by the inability of the oscillator control to change the oscillator frequency close to the peak phase detector output voltages). For an integrated circuit phase detector, the MC1391, the phase detector output is limited to the sync-pulse width since it is a sync-gated system, i.e., $\phi_s = 4.75 \mu s$.

When the loop is out of lock, a steady beat note output results from the phase detector. For a simple resistive filter (with no capacitors), the beat frequency would be constant and no pull-in would occur, but for the filters of interest the d.c. component of the waveform tends to reduce the mean tuning error. Thus at any time, the free-running frequency of the oscillator in the absence of syncs will be greater than the off-set frequency obtained when the loop is closed. Notice, however, that as the detuning error increases, the waveform becomes more sinusoidal, reducing the d.c. component and the pull-in effect. Should the mean value of the d.c. component be found in terms of its frequency shifting capability, we can find the pull-in range and the pull-in time from any frequency within the pull-in range.

As shown in Appendix H, the maximum pull-in range $\Delta f_{\text{max}}$ is given by:

$$\Delta f_{\text{max}} = \frac{2 \phi_s f_c \sqrt{m}}{(3 + m)}$$

if $m \ll 1$

The above expression, together with the formulae presented in 9 will completely specify the important characteristics of the conventional horizontal APC/AFC loop. The next section will cover the practical design use of these formulae, and detail instances of departure from the ideal case.

It should be apparent by now that the design of a satisfactory APC/AFC loop is not as straightforward as the simple block diagram of Figure 2 might have suggested. Five formulae are needed to define the characteristics of the loop and these formulae are not mutually independent. The designer has only three parameters that he can vary to fit all these formulae and meet his circuit needs. Further, his needs may change depending on the type and performance of circuits internal to the loop and, to complicate matters more, of circuits external to the loop. An obvious example of the former is the oscillator stability which will be a prime factor in determining the pull-in range required, and an example of the latter is the Static Phase Error permitted for correct burst gating in the chroma channel. If the burst is sync gated, then the S.P.E. requirement may not be as stringent although large oscillator drifts could result in high d.c. loop gain being needed that will also produce small S.P.E.'s.

Other factors that must be entered into the design concern the expected environment of the loop, both within the receiver and in the type and quality of the signals that will be received. Should the receiver manufacturer have a reputation for high performance in fringe reception areas, then he will be very concerned with thermal noise performance and the APC/AFC loop will tend to have small noise bandwidths. Alternatively, if the manufacturer is more concerned with urban reception, particularly near large airports, the loop will probably need to be high speed to track phase variations. More likely, the manufacturer will want the receiver to perform well everywhere and compromises must be made.

Within the receiver the characteristics of the loop will depend on the sync source and, for gated a.g.c. systems, the performance of the a.g.c. loop, especially when the horizontal oscillator is temporarily out of synchronism. Many loops use a dual diode arrangement for the phase detector and the sensitivity of this type of detector (see

![Diagram of Phase Detector](image-url)

FIGURE 8 - Detector Beat Notes
Appendix) depends on the amplitude of the smaller of the two waveforms applied to it. The reference sawtooth waveform from the sweep circuit is usually chosen so that the phase detector sensitivity will not change with adverse signal conditions that affect the syncs. With a fixed oscillator sensitivity, the required d.c. loop gain can be obtained by changing the reference sawtooth waveform amplitude. For high loop gains and maximum flexibility, this means that the sync amplitude should be large—a requirement that can be difficult to meet in a 12 V. battery operated set. Alternatively, the effective amplitude of the sawtooth can be raised by using an active shaper network to increase the slope of the sawtooth.

A slow a.g.c. loop can seriously modify the apparent performance of the loop. If airplane flutter causes significant changes in the video detector output level and the sync separator is too slow to follow these changes, then the varying slice level will cause phase shifts at the input to the loop (see CER105). Also, when the line oscillator is out of lock, the gating pulse will activate the a.g.c. system during the video portion of the signal. This tends to make the a.g.c. loop increase the gain of the R.F. and I.F. amplifiers. Conversely, when the gating pulse and sync pulse coincide, the a.g.c. loop will attempt to reduce the R.F. and I.F. amplifier gains. The detector output that results from this process is modulated with a ripple corresponding to the frequency difference between the horizontal oscillator and the sync waveform. If the ripple amplitude is large then 'holes' will appear in the separated sync. The phase detector output beat note will be modified by these 'holes' and the mean d.c. voltage generated will be reduced causing a reduction in the oscillator pull-in range. This effect should be particularly noted when comparing a solid state receiver with an earlier tube or hybrid design. The introduction of I/C's into the receiver to perform the a.g.c. function (e.g., MC1345/44) has meant that coincidence of the sync and flyback pulse is necessary to gate the a.g.c. Since erroneous gating does not occur during the video portion of the signal, the detector level remains much more constant and wider pull-in ranges approximately the theoretical maximum (equation 11) are obtained.

A popular method of assessing the pull-in range is to offset the oscillator while syncs are applied to the loop. The 60 Hz component in the sync waveform is usually enough to cause a side-lock at multiples of the field frequency and the pull-in range is noted as the last side-lock on either side of 15.734 KHz from which the oscillator pulls into synchronism. Since the ripple at the detector increases as the oscillator approaches 15.734 KHz (the a.g.c. gate samples video for longer periods), the APC/AFC loop will get very little sync information and the beat note pull-in effect is correspondingly weak. Thus, for a tube design, the pull-in range obtained by the above method is close to the actual free-running frequency from which the oscillator can be locked. By measuring the picture offset on the CRT at the pull-in limits, the maximum stable phase error the system will tolerate is also found. However, with a solid state receiver using an improved a.g.c. system, a strong beat note (but no ripple at the detector) is generated when the APC/AFC loop is out of lock and the side-lock frequency limits at pull-in are significantly lower than the oscillator actual free-running frequencies at pull-in. Since the true pull-in range is not observed, the S.P.E. over the pull-in range obtained by the above method will be larger than a similar design with a poor a.g.c. system.

Another characteristic of the APC/AFC loop that will depend in a large measure on the external circuitry is the required noise bandwidth. The effect of random noise in the sync waveform is to cause the position of individual picture elements to vary from instant to instant. The larger dynamic phase error that can be tolerated will depend on many subjective factors. For example: At the same time noise appears in the sync waveform, it will also be present in the video masking the true position of the picture elements. A moving picture or smaller screen size will also change the appearance of thermal noise.

In fact, when the video becomes unusable at the picture tube because of the noise interference, then the signal to noise ratio at the detector can be considered the system limit. As far as the sync circuits are concerned, the received bandwidth can be reduced without seriously modifying the sync waveform. This will improve the signal to noise ratio for the sync signal with a corresponding reduction in the dynamic phase error under limiting conditions.

If we treat the syncs as a trapezoidal waveform, the contribution of each harmonic to the effective timing information can be calculated. This is shown in Figure 9 and it can be seen that 90% of the timing information is

![Figure 9](image-url)

(3) The reduction of the pull-in range vs. a.g.c. loop frequency response has been dealt with in the literature. However, the use of fast sync separators and the superior characteristics of I/C a.g.c. loops will probably make further investigation academic in nature.
The receiver can take several different paths. For example:

- The oscillator at 15.734 KHz is the solution (the dotted line).

Sometimes the loading of the oscillator circuit may have to be duplicated, or further filtering in the sync channel before sync separation may be necessary to provide comparable thermal noise performance.

The approach to an APC/AFC design for a television receiver can take several different paths. For example:

- The design problem may simply be modification of a circuit to remove an undesirable characteristic caused by a faulty design, production spreads or a new operating environment. Cost reduction may be the objective, or adaptation of an existing circuit to a new chassis design.

- Should any of the above conditions be encountered, the best starting point is to fully evaluate the fundamental characteristics of the present circuit. This naturally includes measurements of the oscillator and phase detector sensitivities. Those are usually quite simple to make and may require just disconnecting the phase detector output from the voltage (or current) controlled device in the oscillator circuit. Sometimes the loading of the oscillator circuit on the phase detector may have to be duplicated (particularly with solid state circuits) or the effect of loading allowed for. Since linear operation of practical circuits is rarely encountered, the characteristics should be measured over the expected operating range of each block.

Figure 10(a) and (b) shows the measured sensitivity curves of a solid state monochrome receiver. In this particular case, asymmetrical pull-in was the problem and the cause is the change in oscillator sensitivity producing a fall in d.c. loop gain as the oscillator free-running frequency is lowered. Relocation of the d.c. operating point of the oscillator at 15.734 KHz is the solution (the dotted line on Figure 10).

Notice that the product of the two slopes will give the circuit d.c. loop gain. This will define the Static Phase Error as the oscillator drifts. For this particular circuit, a drift of ±180 Hz would produce an S.P.E. of ±1 µs. Clearly, if this design were to be adapted to a color receiver, the loop gain would have to be raised. Obviously, the amount of loop gain increase required will depend on the drift characteristics of the loop. Before any efforts are made to change the loop gain, the oscillator frequency variation with temperature and supply voltage should be measured and the effects of aging estimated. The lower operating ambient temperature of a solid state set means that the temperature/frequency drift can be held to less than ±190 Hz, including the turn-on warm-up drift. Wherever possible, if increased loop gain is still needed, the most stable circuit block should be changed or increased drift will result.

When further cost reduction will seriously impair the circuit performance, or the circuit already cannot meet the full performance capability of the simple APC/AFC loop, other circuits or a complete new design may have to be investigated.

One excellent solution to the problem of low cost combined with full performance can be provided by an integrated circuit, either in combination with other circuit functions or simply as an APC/AFC block. Several I/C's performing this function are available and one circuit, the MC1391P, will be used to demonstrate the use and universality of the preceding theoretical analysis. The MC1391P is well suited for this purpose as its parameters are stable and well documented. Although it is an I/C, it is very flexible with an external filter and externally adjustable loop gain allowing any performance characteristic, within the limits of the simple APC/AFC loop, to be obtained.

(See Figure 11 and Appendix)

The operating characteristics of the MC1391 are easily calculated (Ref. 5), or they can be measured. The oscillator sensitivity is best expressed in amps per radian as this is a current controlled device, and can be measured by disconnecting the phase detector output (pin 5) and noting the current through the filter resistor R into the oscillator timing pin (pin 7). This current can be positive...
Since the available voltage swing at pin 5 before saturation occurs is 5.8 V, then:

\[ R = \frac{5.8}{0.053 \times 10^{-3}} \approx 110 \text{ K} \Omega \]

\[ \therefore \text{Put } R = 100 \text{ K} \Omega \]

\[ xR = 4.2 \text{ K} \approx 3.9 \text{ K} \Omega \]

With these practical values, \( x = 0.039 \) and \( m = 0.038 \)

\[ C = \frac{T}{R} = \frac{15 \mu F}{3.3 \text{ K} \Omega} \]

The maximum possible pull-in range is given by equation (14):

\[ \Delta f = \pm \frac{2 \times 0.46 \times 6000 \sqrt{0.038}}{3 + 0.038} \]

\[ = \pm 354 \text{ Hz} \]

From equation (5):

\[ f_{nn} = \frac{1 + (0.039)^2 \times 0.015 \times 37699}{4 \times 0.039 \times 0.015} \]

\[ = 795 \text{ Hz} \]

The response time to recover from a step input is given by:

\[ t = \frac{\log_{10} 0.1}{a} \quad \text{where} \quad a = \frac{1 + xT_{WC}}{2(1+x)T} \]

\[ i.e., \quad t = 3 \mu s \quad = 739.6 \]

This example effectively shows the compromises involved in the design of an APC loop. In aiming for a fast responsive loop with a quick recovery time to give optimum tracking of incoming phase variations (airplane flutter, etc.), we have obtained a loop with a noise bandwidth about twice what it should be. The stability of the sync when the incoming signal is heavily contaminated with thermal noise may be considered unsatisfactory; a continual jitter or “rubber banding” will be evident on the CRT. Also, because of the high a-c gain and very low damping of the loop, impulse noise will cause ‘tearing’ as the loop attempts to follow the transient changes produced by the impulse noise.

To improve the design with respect to the noise performance, several things can be done—the problem is to decide which changes will have the least effect on the other loop characteristics. If the AC/DC gain ratio is reduced by changing \( x \); the pull-in range will be reduced also. A safer course is to decrease the natural resonant frequency of the loop by modifying \( T \), and a suitable design is shown in Figure 15.

The d.c. loop gain has been increased slightly to:

\[ f_c = \frac{1.61 \times 10^{-4} \times 13.9 \times 10^3 \times 15734}{5} \]

\[ = 7040 \text{ Hz/rad.} \]

To limit the hold-in range to ±1 KHz,

\[ R = 150 \text{ K} \Omega \quad xR = 3.3 \text{ K} \Omega \]

\[ x = 0.022 \quad \therefore m = 0.0215 \]

\[ T = RC = 1 \times 10^{-6} \times 150 \times 10^3 = 0.15 \]

The lower loop time constant reduces the natural resonant frequency to 85 Hz and the damping coefficient \( K = 0.8 \).

\[ f_{nn} = \frac{1 + (0.022)^2 \times 0.15 \times 2 \pi \times 7040}{4 \times 0.022 \times 0.15} = 319 \text{ Hz} \]

The pull-in range is slightly lower at ±315 Hz, and the recovery time from a step transient is 4.8 \( \mu s \).

REFERENCE AND FURTHER READING:

3. HEROTA, NABEYAMA, MIYAZAKI “Design and Analysis of the Pull-In Range of Horizontal AFC in Television Systems”
5. WILCOX, M. “A TV Horizontal I/C”
manufacturer, it avoids the use of a large inductor that may be subject to pick-up from toroidal yokes, for example. However, unless an expensive multiturn pot is used, the entire operating range of the oscillator is covered in a 320° rotation of the hold control. If the control capability is ±750 KHz, then each degree of rotation will change the oscillator frequency by 4.7 Hz. When an L-C oscillator is used, the t.p.i. of the inductor core can be used to limit the frequency change for a single 360° rotation of the hold control, thus making a relatively insensitive setting.

To avoid the use of a large inductor that may be subject to pick-up from toroidal yokes, for example. However, unless an expensive multiturn pot is used, the entire operating range of the oscillator is covered in a 320° rotation of the hold control. If the control capability is ±750 KHz, then each degree of rotation will change the oscillator frequency by 4.7 Hz. When an L-C oscillator is used, the t.p.i. of the inductor core can be used to limit the frequency change for a single 360° rotation of the hold control, thus making a relatively insensitive setting.

<table>
<thead>
<tr>
<th>Worst Case Oscillator Deviation From fH</th>
<th>Internal Drift</th>
<th>External Drift</th>
<th>Transmitted Operator Tolerance Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>25 Hz</td>
<td>75 Hz</td>
<td>30 Hz + 60 Hz = 190 Hz</td>
</tr>
</tbody>
</table>

Notice that the warm-up drift is not included in the above figure. This is the drift that occurs during the first few minutes after turn on as the I/C package temperature stabilizes to the 25°C ambient. It is not included since the hold control is usually adjusted after this period and unless it exceeds the pull-in range of an ‘instant on’ receiver, it cancels out and is not noticed.

The minimum loop gain is now defined by the permissible phase error over this frequency duration. Use equation (1):

\[
\frac{0.5 \times 2 \pi}{63.5} = \frac{190}{f_c}
\]

\[f_c = 3840 \text{ Hz/rad}.
\]

The drift characteristic has also defined the minimum pull-in range that can be tolerated and usually, if other dynamic performance characteristics are to be satisfactory, the value of loop gain given above is insufficient to guarantee pull-in over ±190 Hz. Also, the oscillator sensitivity and the phase detector sensitivity are subject to component tolerance and manufacturing tolerance and the loop gain must be in excess of 3800 Hz/rad to ensure that the S.P.E. will be maintained below 0.5 µs. It is a safe assumption that at least 50% more loop gain than the minimum will be needed.

\[f_c = \mu \beta = 6000 \text{ Hz/rad}.
\]

Now the frequency deviation can be as much as ±300 Hz for acceptable phase performance.

The phase detector sensitivity of the MC1391 is nominally:

\[\mu = 1.6 \times 10^{-4} \text{ A/rad}.
\]

(assuming a sync pulse deviation of 4.7 µs, i.e., \(\phi_s = 4.7 \times 0.095 = 0.46 \text{ rads}\).)

Therefore, the required oscillator sensitivity \(\beta = 37.3 \times 10^6 \text{ Hz/A}\).

The next part of the design procedure, the filter network, can appear somewhat arbitrary in nature as this is the area in which the designer can emphasize one performance characteristic but only at the expense of others.

Before making a first-cut try at the design, it should be noted that the resistor R between pins 5 and 7 can have a significant effect on the loop other than its function as part of the filter.

Earlier it was stated that the stable operating region of the phase detector in the MC1391 is confined to the width of the sync pulse. With the value of loop gain chosen previously, this means that the hold-in range of the oscillator can be as much as:

\[\pm \frac{2.35 \times 2 \pi \times 6000}{63.5} = \pm 1400 \text{ Hz}.
\]

and obviously if higher loop gains are needed for the synchronous performance, it will become possible for the oscillator free-running frequency to deviate even more from 15.734 KHz at the hold-in limits. The full hold-in range can be realized, of course, only if the loop remains linear over the stable operating region. Should the value of R be large, then the available voltage swing at pin 5 will not permit the full phase detector current to be applied to pin 7, i.e., the phase detector will saturate. Reducing the hold-in frequency limit can be desirable and making the value of R fairly large to do this is a useful technique. (For a discrete circuit actively shaping the reference saw-tooth to increase its slope or using limiting diode clamps on the oscillator control pin will have the same effect.)

When a step input phase change is applied to the loop, the response should be as rapid as possible to reach the new equilibrium. Two characteristics of the loop will define how far it can respond, the natural resonant frequency
FIGURE 13 – Jitter Generator

and the amount of overshoot permitted when the correct phase has been reached. Both of these characteristics can be ideally demonstrated by using a Jitter Generator. This generator is inserted into the video channel of the r.f. modulator used to supply a signal to the receiver and it introduces (typically) a 3 µs delay during one field and then switches back to an undelayed signal on the next field.

This switching between delayed signal and undelayed signal will cause a vertical line in the video to trace the transient response of the loop on the CRT of the receiver. A typical response is shown in Figure 14.

An ideal response would be one that approached equilibrium as fast as possible without overshooting or 'hunting.' This indicates that the damping should be critical and the natural resonant frequency high, but this will result in a system with high a-c loop gain corresponding to large noise bandwidths. The effect of a fast recovery with lower natural resonant frequencies and acceptable noise bandwidths can be obtained by allowing some overshoot to occur. Usually the recovery from the transient should be complete within 1/3 to 1/2 of the field scan period. If a single overshoot is permitted, this will tend to limit the natural resonant frequency to a maximum of 363 Hz or 250 Hz, respectively (more than one overshoot during the recovery time indicates high natural resonant frequencies and large noise bandwidths with the chance of ringing to occur on impulse noise).

Choosing a high natural resonant frequency of 250 Hz means that x should be selected to minimize the noise bandwidth.

From equation 5
\[
\frac{df}{dx}(f_{NN}) = -\frac{1}{4x^2T} + \frac{W_c}{4} = 0 \text{ for a minimum.}
\]

i.e.,
\[
x = \sqrt{\frac{W_c}{4T}}
\]

From equation (8), this produces a value of 0.25 for K.

\[
W_c = 2\pi x 6000 = 37699 \text{ rads/sec volt}
\]

and \[
W_n = 2\pi x 250 = 1571 \text{ rads/sec}
\]

If \(x\) is small, then \(W_n \approx \sqrt{\frac{W_c}{T}}\)

\[
\therefore T = \frac{37699}{(1571)^2} = 0.0153
\]

\[
\therefore x = \sqrt{\frac{37699 x 0.0153}{1571}} = 0.0417
\]

\[
\therefore m = \frac{x}{x+1} = 0.04
\]

If we decide to limit the hold-in range to ±1 KHz then the linear operating region of the phase detector \(\phi\) must be limited to:

\[
\phi = \frac{2000}{f_c} = 0.33 \text{ radians}
\]

The phase detector average current change = \(\mu\phi = 1.61 \times 10^{-4} \times 0.33 = 0.053 \text{ mA}\)
or negative corresponding to the direction of the oscillator frequency offset. Note, however, that the oscillator sensitivity is dependent on the impedance at pin 7 and can be increased by raising the value of the timing resistor (with a concomitant reduction in the capacitor value to keep the same time constant). This is the method by which the circuit loop gain can be changed to suit the design aims.

Since the oscillator characteristic around the centre frequency of 15.734 KHz is very linear, the phase detector sensitivity can be determined simply by producing a known phase error between the sync and flyback pulses and noting the resulting oscillator free-running frequency to produce this error when the phase detector is disconnected. The measured oscillator characteristic will then indicate the phase detector offset current for this phase error. In a more general case, the oscillator characteristic may not be linear (see Figure 10a) and the above method would not give a direct evaluation of the phase detector characteristic and a more complicated method must be resorted to. A typical set-up is shown in Figure 11 where a generator is used to provide the flyback pulse and is also phase-locked to a second generator which provides the sync pulse. By using the advance/delay pulse output from the second generator, the inputs to the phase detector can be varied by known phase differences and the detector output current measured. This method has the additional advantage that any loading by the oscillator on the phase detector is retained for a true operating characteristic. The phase detector characteristic of the MC1391 is also very linear with the end points occurring at the edges of the sync pulse as this is a sync gated detector. Notice that the operating range of the diode detector in Figure 10 is nearly ±6 µs—or the flyback pulse width. For that loop, the stable operating region is determined partially by the oscillator characteristic rather than wholly by the phase detector as it is with the MC1391.

Once the phase detector characteristic is known, it is an easy matter to select the oscillator impedance for the oscillator sensitivity required to produce sufficient circuit d.c. loop gain. How much loop gain is sufficient will depend on several factors.

Primarily, there must be enough gain to maintain the Static Phase Error within defined limits, ideally ±0.5 µs for a flyback pulse gated chroma channel. Because the oscillator section of the MC1391 is designed for a nominal zero temperature coefficient, the free-running frequency can drift in either direction from 15.734 KHz. Over a 30°C operating temperature range, the drift can be as much as ±25 Hz. The external frequency determining elements will add another ±75 Hz drift if the hold control is typically 10% of the total timing resistance (polystyrene and polyster capacitor ±100 p.p.m/°C, Cermet Pot 150 ppm/°C and NC5 resistor). Apart from temperature drift of the oscillator an S.P.E. can be caused by the permissible transmitter tolerance for fH. and sometimes CCTV applications must be considered, adding another 20 to 30 Hz. Finally, operator error must be included, that is the possibility of an incorrectly set hold control either by the factory or by the serviceman/customer.

The advantage of an R-C oscillator, from the I/C designer’s viewpoint, is that both timing and oscillator control can be achieved with a single pin-out. For the set

![FIGURE 11 - Test Set-up for Measuring Oscillator and Phase Detector Characteristics]
APPENDIX A

1 radian = 57.296 degrees

f_H = 15.734 KHz

T = 63.5 µsec.

1 µs at f_H = 5.699 degrees = 0.0989 radians

APPENDIX B

Loop Recovery Time From a Step Transient.

The D.E. of the loop can be written:

\[ p^2 + \frac{(1+xT_wc)p}{(1+x)T} + \frac{W_c}{(1+x)T} = 0 \]

i.e.,

\[ p^2 + 2ap + c = 0 \]

The envelope decay = \( K e^{-at} \)

The envelope decay = \( K e^{-at} \)

where \( K \) is proportional to the initial step amplitude.

\[ \therefore a = \frac{1+xT_wc}{2(1+x)T} \]

Therefore, the time to decay to 10% of the initial offset is given by:

\[ e^{-at} = 0.1 \]

\[ \therefore t = \frac{\log_0 0.1}{-a} \]

\[ = \frac{2.303}{(1+xT_wc) / 2(1+x)T} \]

= 231
**APPENDIX C**

**Spectrum of the Horizontal Sync Waveform.**

For a trapezoidal waveform of amplitude $A$, period $T$ and duration $t_0$ with rise and fall times of $t_1$ then:

$$A_{\text{rms}} = A \sqrt{\frac{3t_0 + 2t_1}{3T}}$$  

$$A_{\text{avg}} = A \frac{t_0 + t_1}{T}$$

$$= A \times 0.278$$

Amplitude of the $n$th harmonic:

$$A_n = 2A_{\text{avg}} \left[ \frac{\sin \left( \frac{n \pi T}{t_0} \right)}{\pi \frac{n}{t_0}} \cdot \frac{\sin \left( \frac{t_1 + t_0}{T} \right)}{\frac{t_1 + t_0}{T}} \right]$$

$$= A \times 0.1575 \times \frac{\sin(0.0124n) \sin(0.247n)}{3.06 \times 10^{-3} \times n^2}$$

Calculating the contribution of each harmonic to the total effective value generates the curve shown in Figure 9.

---

**APPENDIX D**

**Circuit Diagram of the MC1391.**

The output pulse width is adjusted by the resistive divider at pin 8. For stable operation, the impedance at pin 8 should be close to 1 KΩ. To advance the static phasing, a small resistor (< 100 Ω) can be placed between the flyback pulse integrating capacitor and ground.

---

**CIRCUIT SCHEMATIC**

- **Pre Driver**
- **Oscillator Timing**
- **Oscillator**
- **VCC Regulator**
- **Phase Detector**

---

FIGURE D-1

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APPENDIX E

The MC1391 Oscillator Circuit.

If it is assumed that \( Q_7 \) is initially off, then the capacitor connected from pin 7 to ground will be charged by an external resistor (\( R_T \)) connected to pin 6. As soon as pin 7 voltage exceeds 5 V, the potential at \( Q_9 \) base, \( Q_7 \) will conduct allowing \( Q_6 \) to supply base current to \( Q_5 \) and \( Q_{10} \). Transistor \( Q_{10} \) sets the base of \( Q_8 \) at approximately 2 V. \( Q_5 \) then discharges \( C_T \) through \( R_4 \) until pin 7 reaches 2 V and \( Q_7 \) turns off again and the cycle repeats.

The frequency of oscillation is given by:

\[
f_0 = \frac{1}{t_c \ln \left( 1 + \frac{R_3}{R_1 R_2 + R_3 + R_4} \right) + t_d \ln \left( 1 + \frac{R_1 R_2}{R_1 R_3 + R_4} \right)}
\]

and for \( f_0 = 15.734 \text{ KHz} \)

\[
t_c \Omega 10^{-4} \quad \text{if } R >> R_4
\]

\[
t_c = \text{charge time constant } = R_T C_T
\]

\[
t_d = \text{discharge time constant } = R_4 C_T
\]

For small frequency deviations, the oscillator sensitivity:

\[
\beta = \frac{15.734 \times R_T}{5 \text{ V}} \quad \text{Hz/A}
\]

The sensitivity can be adjusted by changing the external resistor \( R_T \).

![Figure E-1](image-url)
Phase Detector Operation of the MC1391P.

The phase detector consists of the comparator Q15 and Q16 and the gated current source Q17. Negative going sync pulses (1 V to 5 V (p-p)) at pin 3 turn off Q12 allowing Q17 to conduct. The current division between Q15 and Q16 during the sync pulse period will be determined by the phase relationship between the syncs and the sawtooth at pin 4 which is derived from the horizontal flyback pulse. If the steep slope of the sawtooth is symmetrical about the sync pulse (Figure F2), then Q15 and Q16 will each conduct for half the sync pulse period. When the sawtooth is just less than 2 V, Q15 conducts all the Q17 current, and this current is turned around by Q18 to flow out of pin 5. When the sawtooth is above 2 V, Q16 conducts and current flows into pin 5; thus the net current at balance is zero. When a phase offset occurs, there will be an average current flow either in or out of pin 5 to speed up or slow down the oscillator. Note that if the sawtooth amplitude is greater than about 1 V (p-p), the change in voltage at pin 4 to completely switch the comparator is small compared to the amplitude of the saw. Switching can be considered instantaneous and the detector sensitivity is independent of either the sawtooth amplitude or the sync pulse amplitude.

The average phase detector current goes from zero to full output in half the sync pulse width:

\[
\mu = \frac{(I_{\text{peak}} \times \text{duty cycle})}{(\text{conduction period})}
\]

\[
0.5 \times 10^{-3} \times \frac{4.7}{63.5} = 0.5 \times 4.7 \times 0.098
\]

If the sawtooth is reasonably linear, then the phase detector output current

\[
\pm I = \mp \mu \phi
\]

where \(\phi\) is the phase difference between the oscillator and the sync pulse.

![FIGURE F-1](image1)

![FIGURE F-2](image2)
Dual Diode Bridge Phase Detectors.

In the simple dual diode bridge phase detector, the negative going sync pulse tips are clamped to ground by D2 and the waveform at B is shown in Figure G2(a). The output voltage from the bridge due to the sync waveform is very small because the diode D1 is back biased between the sync pulses (when B is very positive) and the impedance at A, determined largely by the integrating capacitor for the flyback pulse, is small compared to the diode load resistors. Therefore, when an a.c. coupled sawtooth is applied to A and the phase is such that the steep slope of the waveform is symmetrical about the sync pulse, the waveform at A is as shown in Figure G2(b). The bridge output is nominally zero. If the oscillator begins to lead the sync pulses, the sawtooth is clamped later on its steep portion as shown in G2(c) and a net +ve voltage is obtained. This voltage is filtered and applied to the control device to slow the oscillator down. Similarly for a lagging oscillator, a net -ve voltage is developed to speed the oscillator up (Figure G2(d)). Notice that the output voltage obtained is a maximum at each end of the sawtooth steep slope, i.e., the stable operating range is over the flyback pulse width. If the flyback pulse width is $\phi_s$ radians and the peak-to-peak sawtooth amplitude is E volts, then:

$$\mu = \frac{E}{\phi_s} \text{ volts/radian}$$

and the phase detector output voltage for a phase shift between oscillator and sync pulse of $\pm \phi$ is:

$$\pm E_{out} = \pm \mu \phi$$

Obviously, the phase detector sensitivity can be increased by increasing the reference sawtooth amplitudes (but not to the point where the sawtooth amplitude exceeds the sync pulse amplitude). Alternatively increasing the slope (reducing $\phi_s$) has the same effect. The simple diode detector is very dependent on the sawtooth shape and amplitude. If the sync amplitude is large, then the bridge is relatively independent of amplitude modulation of the syncs, but if these are heavily differentiated amplitude modulation will also cause phase modulation when the bridge is unbalanced.
APPENDIX H

Derivation of the Approximate Expression Given in Equation 10 for the Maximum Pull-In Range.

The general D.E. for the loop is:

\[ \ddot{\phi} + F(p)\omega_c \phi = p\phi_i \]

which can be rewritten:

\[ \frac{d\phi}{dt} + F(p)\omega_c \phi = \Delta \omega \quad (1) \]

Now \[ F(p) = \frac{1+pxT}{1+p(1+x)T} = \frac{1-m+pT}{1+m+pT} \]

since \( x = \frac{m}{m-1} \)

\[ : F(p) = m + \left\{ \frac{1 - 2m + m^2}{1 - m + pT} \right\} \]

Substituting this in equation (1) gives:

\[ \frac{d\phi}{dt} + m\omega_c \phi + \left\{ \frac{1 - 2m + m^2}{1 - m + pT} \right\} \omega_c \phi = \Delta \omega \]

If we write \( W_1 = \Delta \omega - \left\{ \frac{1 - 2m + m^2}{1 - m + pT} \right\} \omega_c \phi \)

then \( W_1 \) is the effective instantaneous impressed frequency difference, produced by the detuning error of the oscillator (\( \Delta \omega \)) and the frequency drift generated by the correction voltage across the filter capacitor. As pull-in progresses the right-hand term will cause \( \omega_1 \) to be reduced, and the mean value of \( W_1 \)

\[ \overline{W_1} = \Delta \omega - \left\{ \frac{1 - 2m + m^2}{1 - m + pT} \right\} \omega_c \phi \]

Since the capacitor bias is generated by applying the mean phase detector output \( m\omega_c \phi \) to the filter

\[ \overline{W_1} \approx \Delta \omega - \left\{ \frac{1 - 2m + m^2}{1 - m + pT} \right\} \omega_c \phi \]

Now \( \frac{d\phi}{dt} + m\omega_c \phi = \overline{W_1} \quad (12) \)

If it is assumed that the average bias across the filter capacitor will not change significantly during a cycle of the beat-note (i.e., the filter time constant is long compared to the beat-note frequency), we can find this average bias by integrating the loop D.E. over a cycle of the beat-note.

Integrating (12) over the beat note period \( T_{BN} \):

\[ \int_{t}^{t+T_{BN}} \frac{d\phi}{dt} + m\omega_c \phi = \int_{t}^{t+T_{BN}} \overline{W_1} \]

The integral in the above equation is the area under a cycle of phase detector output and this integral, divided by the beat note period will give the mean d.c. component of the output:

\[ \overline{m\omega_c \phi} = \frac{1}{T_{BN}} \overline{W_1} + \overline{W_{BN}} \]

\[ \therefore \text{The mean d.c. component } \overline{m\omega_c \phi} = \frac{1}{m} \left[ \overline{W_1} - \overline{W_{BN}} \right] \quad (13) \]

When the phase detector generates a cycle of the beat note in the time \( T_{BN} \), it will have operated in two regions—the stable region for a time \( t_s \) and the unstable region for a time \( t_u \) such that:

\[ \frac{1}{T_{BN}} = \frac{1}{t_s + t_u} \]

Solving equation (13) in the region \( \phi_s \):

\[ \int_{0}^{t_s} m\omega_c \phi \frac{d\phi}{m\omega_c} = \int_{-\phi_s/2}^{+\phi_s/2} \overline{W_1} \]

\[ \therefore m\omega_c t_s = \log_e \left( \frac{W_1}{m\omega_c} - \phi \right) + \phi_s/2 \]

\[ \therefore t_s = \frac{1}{m\omega_c} \log_e \left\{ 1 + \frac{2W_1}{m\omega_c \phi_s} - 1 \right\} \]

Similarly during \( \phi_u \):

\[ \frac{m\omega_c \phi_u}{\phi_u} = \log_e \left\{ 1 + \frac{2W_1}{m\omega_c \phi_s} - 1 \right\} \]

\[ \therefore W_{BN} = \frac{2\pi}{T_{BN}} = \frac{m\omega_c \phi_s}{\log_e \left\{ 1 + \frac{2W_1}{m\omega_c \phi_s} - 1 \right\} \phi_s + \phi_u = 2\pi} \]
Substituting this expression into $E_y$ gives

$$\omega_c \phi = \frac{1}{m} \left[ \frac{m \omega_c \phi_5}{\overline{W}_1} - \frac{2}{\log_e \left( 1 + \left( \frac{2 \overline{W}_1}{m \omega_c \phi_5} - 1 \right) \right)} \right]$$ \hspace{1cm} (12)

Now:

$$\overline{W}_1 = \Delta \omega = \left[ \frac{1-2m+2m^2}{1-m+2m^2} \right] \omega_c \phi$$

$$\therefore \omega_c \phi = \left[ \frac{1-m+2m^2}{1-2m+2m^2} \right] \Delta \omega - \overline{W}_1$$

$$= \frac{\Delta \omega}{(1-m)} \frac{\overline{W}_1}{(1-m)} - \frac{T}{(1-m)^2} \frac{d}{dt} \overline{W}_1$$

using partial fractions and noting $T = RC = \text{const}$.

Substituting equation (12) in the above:

$$\overline{W}_1 - \frac{m \omega_c \phi_5}{\log_e \left( 1 + \left( \frac{2 \overline{W}_1}{m \omega_c \phi_5} - 1 \right) \right)} = \frac{m \Delta \omega}{(1-m)}$$

Putting $K = \frac{2 \overline{W}_1}{\omega_c \phi_5}$ representing the average frequency difference

and $K_0 = \frac{2 \Delta \omega}{\omega_c \phi_5}$ representing the initial frequency difference

and multiplying the equation by $\frac{(1-m)^2}{m \omega_c \phi_5}$

$$(1-m)K - \frac{2(1-m)}{\log_e \left( \frac{K+1}{K-1} \right)} = K_0 - mK - \frac{m}{1-m} T \frac{dK}{dt}$$

or

$$\left( \frac{1-m}{mT} \right) dt = \frac{dK}{K_0 - K + 2(1-m)} \frac{1}{\log_e \left( \frac{K+1}{K-1} \right)}$$

If the mean average frequency ($K$) decreases with time then the initial frequency difference ($K_0$) is within the pull-in range. Putting $T_F$ for the limit time to pull-in from

$$\overline{W}_1 = \Delta \omega \text{ to } \overline{W}_1 = \frac{m \omega_c \phi_5}{2}$$

$$(1-m) \frac{1}{mT} \int_{K_0}^{K_0 + \frac{2(1-m)}{\log_e \left( \frac{K+1}{K-1} \right)}} K_0 - K + 2(1-m)$$

In the limit, if $T_F$ is real:

$$K_0 - K + \frac{2(1-m)}{\log_e \left( \frac{K+1}{K-1} \right)} > 0$$

or

$$K_0 = \left\{ K - \frac{2(1-m)}{\log_e \left( \frac{K+1}{K-1} \right)} \right\} \text{ limit}$$

For a maximum,

$$\frac{d}{dk} (K_0) = 0 = 4(1-m)(K+1)(K-1) \left( \frac{1}{K} + \frac{1}{3K^3} + \frac{1}{5K^5} + \cdots \right)$$

$$\therefore 4(1-m) = (K+1)(K-1) 4 \left( \frac{1}{K^2} \right) \text{ if } (K) > 1$$

i.e.,

$$K = \frac{1}{\sqrt{m}}$$

$$\therefore K_{0 \text{ (max)}}$$

$$= \frac{1}{\sqrt{m}} - \frac{2(1-m)}{\log_e \left( \frac{1}{\sqrt{m} + 1} \right) - \log_e \left( \frac{1}{\sqrt{m} - 1} \right)}$$

$$= \frac{1}{\sqrt{m}} - \frac{2(1-m)}{2 \sqrt{m(3+m)}} \text{ if } m << 1$$

$$= 4 \sqrt{\frac{m}{(3+m)}}$$

$$\therefore \Delta \omega_{\text{max}} = \frac{\phi_3 \omega_c}{2} \frac{4 \sqrt{m}}{(3+m)}$$

i.e., Maximum pull-in range $\Delta f_{\text{max}} = \frac{2\phi_c \sqrt{m}}{(3+m)}$ \hspace{1cm} (11)
Although this article presents techniques for the general case of UHF-800 MHz circuit design, the emphasis is placed specifically on test fixture design for 800 MHz. Test fixtures tend to be the last consideration for most RF power amplifier development programs, yet they are the most valuable tool available for measuring and maintaining device consistency. Minimum power gain, collector efficiency and broadband performance requirements, though they are always detailed in some form of written specification, are meaningless unless they are demonstrated and controlled by a test fixture. A good test fixture will assure correlation between the customer and vendor and function as a trouble shooting tool in the event of radio problems. When alternate sources are pursued for a stage, test fixtures can shorten qualification cycles. But the prevention of gradual shifts in RF performance over the lifetime of a product is the major purpose of a test fixture.

Motorola has recognized the importance for good test fixtures and has established general guidelines for their implementation.

Each hi-tech product is tied to a well defined test fixture, which has the following general specifications:

- Broadband performance, demonstrating typical characteristics throughout the band. (Ex.: UHF: 450–512 MHz, 800: 800–870 MHz)
- A 3" x 5" mechanical format, which is rugged for high volume test applications.
- Simple RF match construction to represent realistic radio performance.
- Devices must meet all minimum test requirements at the specified test frequency. UHF: 470 MHz, 800: 870 MHz.

The repeatability, mechanical ruggedness and broadband performance are all very important factors needing consideration in the design of test fixtures. The remainder of this article goes into detail, using the MRF846 as an example.

The schematic representation of the fixture outlined in this article is shown below (Figure 1).

C_I and C_O represent the shunt capacitors at the input and output (respectively) which cancel most of the inductive reactance associated with the transistor’s input and output impedance. Mini clamped-mica capacitors are used for these components and are physically located beneath the common lead wear blocks. Inductance "L" is introduced by the input (and output) wear blocks. Because of this parasitic inductance, L, trimmer capacitors (C'1 or C'0) are required to transform the now reactive impedance back to real before launching off into the 1/4 transmission lines.
The transistor’s input and output impedance can be represented as a combined series resistor and inductor as shown in Figure 2.

This series combination can be transformed into a parallel equivalent by using the equations shown in Figure 3. The capacitors $C_1$ and $C_0$ are selected by calculating the value necessary to form a parallel resonance with $X_p$. Since all capacitors have a finite, series lead inductance, the capacitor is actually considered as a simple series resonant circuit. The resulting effect is the capacitance is always higher than the marked value and goes through resonance at some frequency. Mini clamped-mica capacitors are recommended for test fixture design due to the very low parasitic inductance associated with them which increases the usable range of capacitances. (They are also extremely high "Q"). A typical measured series inductance for clamped-mica capacitors is about 0.5 nH. The equivalent capacitance is calculated by subtracting the series lead inductance from the capacitive reactance, or $X_C(equiv) = X_C - X_L(0.5 \text{nH})$.

Since two capacitors are used in parallel, the total capacitance is derived as shown in Figure 4.
A value of 2.0 \( X_c \) is used in the above example since each capacitor will contribute only \( \frac{1}{2} \) to the total capacitance. By setting \( X_c(\text{equiv.}) = \frac{X_p + X_L(0.5 \text{ nH})}{2} \) equal to the parallel equivalent reactance calculated in Figure 3, the exact capacitor values may be determined.

\[
X_p = \frac{2.0 \times X_c - X_L(0.5 \text{ nH})}{2} \\
X_c = \frac{2.0 \times X_p + X_L(0.5 \text{ nH})}{2} \quad (X_c = 1/2 \text{ fC}) \\
C = \frac{1}{\pi f (2.0 \times X_p + X_L(0.5 \text{ nH}))}
\]

Introducing an actual example at this time should help in explaining the remaining steps involved in a test fixture design. The MRF846 is a 40 W, 12.5 V, 800 MHz device whose input and output impedances are:

| TABLE 1 - \( Z_{in}, Z_{out} \) FOR MRF846 |
|-----------------|------------------|
| Frequency       | \( Z_{in} \)     | \( Z_{out} \)   |
| 800 MHz         | \( 1.1 + j4.8 \) | \( 1.20 + j2.4 \) |
| 836 MHz         | \( 1.0 + j4.9 \) | \( 1.15 + j2.5 \) |
| 870 MHz         | \( 1.0 + j5.0 \) | \( 1.10 + j2.7 \) |
| 900 MHz         | \( 0.9 + j5.1 \) | \( 1.10 + j2.8 \) |

Since \( X_p \) will vary as a function of frequency, \( C_1 \) and \( C_0 \) need only be calculated for one point within the frequency band. Typically, the input response of an RF power transistor is optimized about the center of the band. Hence, the input \( R_p \) and \( X_p \) are generally calculated at this frequency \( (f_h + f_l)/2 \).

The output response is different. If \( C_0 \) were selected for a resonance to occur with \( X_p \) at band-center, an unacceptable performance roll-off would be seen at the upper end of the frequency band. Overall performance is best when \( C_0 \) is calculated at a frequency within 20% of the upper end of the band. Since device gain increases as frequency decreases, the performance at lower frequencies is generally no problem.

Using the MRF846 as an example, input and output capacitor values may be determined as follows:

\[
\begin{align*}
\text{INPUT:} & \\
\text{Frequency} &= 836 \text{ MHz} \\
Z_{in} &= 1 + j4.9 \\
Q &= \frac{4.9}{1} = 4.9/1 \\
X_p &= 4.9 \left( \frac{1 + \frac{1}{(4.9)^2}}{2} \right) \\
&= 5.1 \Omega \\
X_L(0.5 \text{ nH}) &= \frac{2.0 \pi}{(836 \times 10^6)(0.5 \times 10^{-9})} = 2.63 \Omega \\
C &= \frac{1}{\pi f (836 \times 10^6)} \\
&= 2.97 \text{ pF} \\
2-15 \text{ pF Capacitors would be the best choice.}
\end{align*}
\]

\[
\begin{align*}
\text{OUTPUT:} & \\
\text{Frequency} &= 870 \text{ MHz} \\
Z_{0} &= 1.1 + j2.7; Q = 2.7/1.1 \\
X_p &= 2.7 \left( \frac{1 + \frac{1}{(2.45)^2}}{2} \right) \\
&= 3.15 \Omega \\
X_L(0.5 \text{ nH}) &= \frac{2.0 \pi}{(870 \times 10^6)(0.5 \times 10^{-9})} = 2.7 \Omega \\
C &= \frac{1}{\pi f (870 \times 10^6)} \\
&= 40.7 \text{ pF} \\
2-20 \text{ pF Capacitors would be the best choice.}
\end{align*}
\]

Though the MRF846 test fixture used at Motorola does use these capacitor values, the above calculations may act only as a good starting point. Empirical measurements and more precise impedance measurements for a given application may result in minor deviations from these values.

Assuming no additional circuit parasitics had to be accounted for, the quarter wave transmission line sections could now be determined. The input (and output) fixture wave blocks do, however, contribute additional series lead inductance to the impedances. These inductances are counteracted by the trim capacitors \( C_1 \) and \( C_0 \). The wear block inductance could be calculated and then used to determine the proper capacitance values. However, since there are other, less obvious frequency and grounding effects which may influence the impedance transformation, it is a more practical (and generally a more accurate) procedure to measure the impedance which will be transformed by the transmission line to 50 \( \Omega \).
The capacitors \( C_1 \) and \( C_0 \) should be mounted into the test fixture and a known characteristic impedance transmission line soldered into place as shown below in Figure 5.

Triple stub tuners are used on the input and output to tune for maximum output power and minimum reflected power at various frequencies throughout the band. Band edges and band center are generally adequate for a good circuit design. Due to higher impedance levels produced by adding \( C_y \) and \( C_0 \), \( (Z_{in}) \) and \( (Z_{out}) \) are measured instead of the real transistor impedances, \( Z_{in} \) and \( Z_{out} \). Also, by measuring impedances in the actual applications fixture, the design can be optimized for the particular fixture. Perhaps a maximum gain tuning point is not what is desired. Obtaining impedances for an efficiency/gain compromise may be more desirable. If this is the case, an impedance table for the appropriate conditions may be obtained. It is then for these impedances that \( C_1 \), \( C_0 \) and \( Z_0 \) will be calculated.

The procedure for obtaining the impedances is simple and requires a vector voltmeter (VVM) or a network analyzer. Both are used at Motorola, but a vector voltmeter is less expensive and if used with a high directivity directional coupler, (>40 dB), is very accurate. The set-up is constructed as shown in Figure 5. With frequency set, stub tuners are adjusted for the desired performance. Again, using the MRF846 as an example, numbers shown in Table 2 were measured for \( P_{in} = 12.0 \text{ W} \), \( V_{CC} = 12.5 \text{ V} \).

The output stub tuners were adjusted for maximum gain at each frequency and the input stub tuners were adjusted for zero watts reflected power. After each measurement, the impedance presented to the fixture by the triple stub tuner and load (or source) combination is measured by the vector voltmeter. The impedance is then translated by the transmission line used in the test fixture to obtain \( (Z_{in}) \) and \( (Z_{out}) \). In the above example a 26 \( \Omega \), 0.309 \( \lambda \) (@836 MHz) transmission line was arbitrarily chosen to be in the MRF846 measurements. By using the equation: \( Z \omega = R_0 [(1 + \Gamma \omega) / (1 - \Gamma \omega)] \) or various computer or calculator programs, the transformation is easily calculated. The most important part of the whole procedure is obtaining an accurate measurement from the stub tuners. Prior to making any measurements, the vector voltmeter must be referenced to a short (180° on a Smith Chart). As a means of accounting for the errors introduced by the connectors at the fixture’s input and output, that same connector is used for a referencing short as shown in Figure 6.

The measurement reference plane is now the edge of the connector used on the test fixture, which is also the beginning of the transmission line. Assuming the same reference plane is maintained during the measurements, an accurate impedance value will be produced. A good technique for maintaining the appropriate reference plane is accomplished by creating a new connector to measure the triple stub tuners. Two connectors are attached as shown in Figure 7.

**TABLE 2 — PERFORMANCE OF MRF846 versus FREQUENCY**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>( P_{out} )</th>
<th>( P_{out} )</th>
<th>( P_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>MHz</td>
<td>806</td>
<td>838</td>
<td>870</td>
</tr>
<tr>
<td></td>
<td>50.0 W</td>
<td>48.3 W</td>
<td>44.0 W</td>
</tr>
<tr>
<td>Eff.</td>
<td>53.3%</td>
<td>55.2%</td>
<td>58%</td>
</tr>
<tr>
<td>Prefl.</td>
<td>0 W</td>
<td>0 W</td>
<td>0 W</td>
</tr>
</tbody>
</table>

**FIGURE 6 — ESTABLISHING REFERENCE PLANE**

**FIGURE 7 — MAINTAINING REFERENCE PLANE**
The triple stub tuner, load combination may now be measured with an adequate degree of accuracy using the test setup shown in Figure 8.

![Test Setup Diagram]

Figure 8 — Test Setup to Measure Stub Tuner W/Load

Repeat the process for the input stub tuner combination. Two numbers are obtained for each frequency which \( (Z_{\text{in}}) \) and \( (Z_{\text{out}}) \) can be calculated from, as shown in the MRF846 example below:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>INPUT</th>
<th>Measured ( \Gamma \beta )</th>
<th>( \Gamma \beta ) converted to Impedance in Ohms</th>
<th>Impedance Transformed Over 26 ( \Omega ) Line in Ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>806 MHz</td>
<td>INPUT</td>
<td>0.35 ( \angle 15^\circ )</td>
<td>24.97 + j8.42</td>
<td>20.72 - j5.64 = ( [Z_{\text{in}}] )</td>
</tr>
<tr>
<td></td>
<td>OUTPUT</td>
<td>0.37 ( \angle 144^\circ )</td>
<td>24.86 + j12.53</td>
<td>17.72 - j6.66 = ( [Z_{\text{out}}] )</td>
</tr>
<tr>
<td>838 MHz</td>
<td>INPUT</td>
<td>0.26 ( \angle 165^\circ )</td>
<td>29.78 + j3.98</td>
<td>21.35 + j0 = ( [Z_{\text{in}}] )</td>
</tr>
<tr>
<td></td>
<td>OUTPUT</td>
<td>0.22 ( \angle 154^\circ )</td>
<td>33.30 + j6.58</td>
<td>18.69 + j7.4 = ( [Z_{\text{out}}] )</td>
</tr>
<tr>
<td>870 MHz</td>
<td>INPUT</td>
<td>0.14 ( \angle -169^\circ )</td>
<td>38.25 - j1.99</td>
<td>20.21 + j6.92 = ( [Z_{\text{in}}] )</td>
</tr>
<tr>
<td></td>
<td>OUTPUT</td>
<td>0.07 ( \angle -158^\circ )</td>
<td>44.10 - j2.24</td>
<td>17.90 + j8.3 = ( [Z_{\text{out}}] )</td>
</tr>
</tbody>
</table>

Note: \( [Z_{\text{out}}] \) is conjugate of \( [Z_{\text{out}}] \)
\[ Z_{\text{in}}^* \] is conjugate of \( Z_{\text{in}} \)

The new impedances can be obtained by using a Smith Chart or using the equation \( Z_{\text{in}} = R_0 \left( (1 + \Gamma \beta)/(1 - \Gamma \beta) \right) \). These impedances (shown in the last column of Table 3) are the impedances which the test fixture will be optimized around. Once again, it is convenient to convert these numbers into parallel equivalents. By doing so, the values of \( C_1 \) and \( C_0 \) become more obvious. Table 4 shows this process.

<table>
<thead>
<tr>
<th>Series Impedance [( [Z_{\text{in}}] ) &amp; ( [Z_{\text{out}}] )</th>
<th>( R_P )</th>
<th>( X_P )</th>
<th>Capacitance Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>20.72 + j5.64</td>
<td>22.26</td>
<td>j81.8</td>
<td>2.42 pF ( C_1 )</td>
</tr>
<tr>
<td>17.72 + j6.66</td>
<td>20.2</td>
<td>j53.8</td>
<td>3.67 pF ( C_0 )</td>
</tr>
<tr>
<td>21.35 + j0</td>
<td>21.35</td>
<td></td>
<td>0.0 pF ( C_1 )</td>
</tr>
<tr>
<td>21.68 + j17.4</td>
<td>18.7</td>
<td>j472</td>
<td>0.40 pF ( C_0 )</td>
</tr>
<tr>
<td>20.21 - j6.92</td>
<td>21.6</td>
<td>-j68.3</td>
<td>-2.68 pF ( C_1 )</td>
</tr>
<tr>
<td>17.90 - j8.3</td>
<td>21.75</td>
<td>-j46.9</td>
<td>-3.90 pF ( C_0 )</td>
</tr>
</tbody>
</table>

From Table 4, notice the calculated values of \( C_1 \) and \( C_0 \) come close to giving the desired frequency response. \( C_1 \) is zero at the band center, indicating the capacitors selected for the input are optimum. The values for \( C_0 \) produce a slight skew in performance toward the high end of the band. Capacitor values for the output could be reduced slightly, but they will remain the same until final fixture performance is determined.
Since $C'1$ and $C'O$ are very small capacitor values, little or no capacitance is actually needed for $C'1$ or $C'O$. However, to allow minor tuning adjustments, a small trimmer capacitor is included at the wear block/transmission line interface.

The final calculation which needs to be performed is that of finding the optimum characteristic impedance for the transmission line. The recommended approach for doing this is to use a computer optimization program which will iterate any number of variables for a desired frequency response. The variables available to be optimized at this point are $Z_0$, $C'1$ and $C'O$ and even $\pi \lambda$ (transmission line length). $Z_0$, $C'1$ and $C'O$ are the very minimum variables.

In the example of the MRF846, where input $R_p$ varies from 22.3 $\Omega$ to 21.6 $\Omega$ over the frequency band, a close approximation can be had by using a mean value of 21.9 $\Omega$. The output $R_p$ starts at 20.2 $\Omega$, dips to 18.7 $\Omega$ and goes back up to 21.75 $\Omega$. Using the same method as before, $Z_0$ is calculated as $50 \times 21.9 = 33 \Omega$. The output $R_p$ starts at 20.2 $\Omega$, dips to 18.7 $\Omega$ and goes back up to 21.75 $\Omega$.

The goal was to demonstrate 12/40 W across the band with less than 2.0:1 input VSWR and greater than 45% collector efficiency. Further optimization could be done by performing impedance measurements on additional transistors or characterizing the test fixture more accurately. However, the above performance is very satisfactory to the required performance. The best compromise for a second pass fixture would be to trade-off gain at 806 and 838 MHz for efficiency, and redesign input and output matching networks for the new impedance tables. This, of course, is only one of the many procedures which may be followed in developing an 800 MHz test fixture.
APPLICATION OF THE MC1377 COLOR ENCODER

by Ben Scott and Marty Bergan
Linear I.C. Applications, Tempe, AZ

The MC1377 is an economical, high quality, RGB encoder for NTSC or PAL applications. It accepts red, green, blue, and composite sync inputs and delivers 1Vpp composite NTSC or PAL video output into a 75 Ω load. It can provide its own color oscillator and burst gating, or it can be easily driven from external sources. Performance virtually equal to high cost studio equipment is possible with common color receiver components. The following note is intended to explain the operation of the device and guide the prospective user in selecting the optimum circuit for his needs.

PREFACE

Since this device has applications in color cameras, video games, video text and computer generated graphics, it may attract potential users who are skilled in computer architecture, but not familiar with the encoding of color television. Perhaps they have spent extensive hours viewing graphics on a full R, G, B wideband monitor. This preface is intended to caution that PAL or NTSC encoding, no matter how rigorously executed, will cause some degree of picture degradation. The process of encoding involves some bandwidth reduction, which means loss of high frequency detail, and it creates the possibility of spurious picture patterns, due to coding and decoding system limitations. The original standards were established about 25 years ago and will probably be in use for many years to come. It is not the objective here to detail these standards as many references1-4 are available. Appendix A shows pictorially why some loss of information and detail is incurred.

The MC1377 is capable of encoding NTSC and PAL to virtually studio standards. It also can be used for very low cost applications where appropriate, with some compromises to picture quality. It can readily drive the 75 Ω input of a composite video monitor, or be used to drive a UHF or VHF modulator so that color television receivers can be used.

CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the color encoder. The three color inputs at Pins 3, 4, and 5 are matrixed to produce chrominance envelopes, (R−Y) and (B−Y), and luminance (−Y) by the standard NTSC/PAL formulae:

\[
Y = .59G + .30R + .11B \\
R−Y = .70R − .59G − .11B \\
B−Y = .89B − .59G − .30R \\
\]

Texts on the NTSC system will show that studio modulation is done on a different set of orthogonal axes called I and Q. Also they will point out that I is a somewhat wider bandwidth than Q. The MC1377 does not permit the circuit designer this refinement, but it should be noted that very few monitors or receivers contain any circuitry to process the unequal bandwidths. (This is the only compromise of standards in the MC1377 which cannot be circumvented by application means.) Rotation of the coordinate system from I/Q to (R−Y)/(B−Y) does not constitute any further compromise whatsoever, and it makes the encoding formulae for PAL and NTSC the same. It also aligns (B−Y) with the axis of the NTSC color burst, for internal circuit simplicity and system accuracy.

REFERENCES

The (B-Y) and (R-Y) signals drive two double balanced (double sideband suppressed carrier) modulators whose carriers are set at 0° and 90°, respectively. In the NTSC mode, the outputs of these chroma modulators are added to produce composite chroma. Burst envelope or "burst flag" is applied to the (B-Y) modulator in the negative direction to produce a burst pulse at a reference angle of 180°. Composite chroma is amplified and buffered to Pin 13 (to permit external bandwidth control as desired) and is then fed back into the IC at Pin 10 to be combined with the luminance component. The luminance signal is also "looped out" from Pin 6 to Pin 8 to permit insertion of a delay line to match the delay incurred in the chroma channel due to bandwidth reduction. The passive components used in the chroma and luma channels are like those used in the most common implementation of color television receivers.

In PAL mode, burst flag is driven into both modulators equally to produce a 225°/135° burst phase. The output phase, or polarity, of the (R-Y) modulator output is alternately switched from 90° to 270° on successive horizontal lines, before being combined with (B-Y), which remains at 0°. The switching of the modulator polarities for PAL mode is driven by the latching ramp generator through the PAL/NTSC control. This control allows PAL switching when Pin 20 is open, and stops when Pin 20 is grounded. The PAL phase can be detected at Pin 20 and controlled by means of external logic. The PAL phase can be reversed by sensing when Pin 20 is high and Pin 1 is low, and momentarily pulling Pin 20 to ground with an external switch.

The color subcarrier source for the modulators can be implemented by free running the on-chip crystal oscillator, or by external drive into Pin 17, or by a combination of both methods. The common collector Colpitts oscillator is completed by connecting a standard TV receiver color crystal and capacitor divider as shown. The oscillator is followed by a 90° phase shifter to provide the quadrature signal to the (R-Y) modulator. The direct oscillator output is taken as reference 0° and is fed directly to the (B-Y) modulator.

The composite sync input at Pin 2 performs three important functions: it provides the timing (but not the amplitude) for the sync in the final output; it drives the black level clamps in the modulators and output amplifier; and it triggers the ramp generator at Pin 1, which produces burst envelope and PAL switching signal.

The ramp generator at Pin 1 is a simple R-C type in which the pin is held low until the arrival of the leading edge of sync. The rising ramp function passes through two level sensors — the first one starts the burst pulse and the second stops it. Since the "early" part of the exponential function is used, the timing provided is relatively accurate from chip-to-chip and assembly-to-assembly. Fixed components are usually adequate. The ramp continues to rise for more than ½ of the line in-
ternal, thereby inhibiting burst generation on "half interval" pulses on vertical front and back porches. Burst is also inhibited if sync is wider than the time required for the ramp to reach the sense levels, as is the case during vertical sync. The ramp method will produce burst on the vertical front and back "porches" at full line intervals. In most applications, this discrepancy from standards will not cause any problem. If it is objectionable, and if a proper burst envelope signal is available, then it can be injected into Pin 1 directly. Another method, suitable for either PAL or NTSC, will be described later.

STANDARD INPUT LEVELS

The signals into Pins 3, 4, and 5 should each be 1 Vpp for standard, fully saturated, color output levels as shown in Figure 2. The levels are important because the IC will generate a predetermined 0.6 Vpp sync and 0.6 Vpp burst at the output, and it will need 1.0 Vpp input signals to produce the corresponding full luminance and chrominance amplitudes. The inputs are internally biased and present a 10 k input impedance. The 15µF input coupling capacitors are sufficient to prevent tilt during the 50 or 60 Hz vertical period. Input signals can be dc coupled (to save the cost of the capacitors), provided that the signal levels are between 2.2 V and 4.4 V at all times. It is essential that the portion of each input which occurs during the sync interval represent black for that input, because it will be clamped to reference black in the color modulators and the output stage. A refinement such as a difference between black and blanking level must be incorporated in the RGB input signals if required.

THE SYNC INPUT

As shown in Figure 2, the sync input can be varied over a wide latitude, but will require bias pull-up from most sync sources. The important requirements are that during the period between sync pulses, the voltage must be above 1.7 V and below the 8.2 V internal regulator. During sync, the voltage (negative going) must extend below +0.9 V and should not exceed −0.5 V (to prevent substrate leakage in the IC). For PAL operation, correctly serrated vertical sync is necessary to properly trigger the PAL divider. In NTSC mode, simplified "block" vertical sync can be used but the loss of proper horizontal timing may cause "top hook" or flag waving in some monitors. An interesting note is that composite video can be used directly as a sync signal, provided that it meets the sync input criteria.

THE LATCHING RAMP (BURST FLAG) GENERATOR

The recommended application is to connect a close tolerance (5%) 0.001 µF capacitor from Pin 1 to ground and a resistor of 51 k or 56 k from Pin 1 to the 8.2 V internally regulated supply (Pin 16). This will produce a burst pulse of 2.5 to 3.5 µs in duration, as shown in Figure 3. As the ramp on Pin 1 rises toward the charging voltage of 8.2 V, it passes first through a burst "start threshold" at 1.0 V, then a "stop threshold" at 1.3 V, and finally a ramp reset threshold at 5.0 V. If the resistor is reduced to 43 k, the ramp will rise more quickly, producing a narrower and earlier burst pulse (starting about...
0.4 µs after sync and only about 0.6 µs wide. The burst will be wider and later if the resistor is raised to 62 k, but more importantly, the 5.0 V reset point may not be reached in one full line interval, resulting in loss of alternate burst pulses.

As mentioned earlier, the ramp method does produce burst at full line intervals on the vertical porches. This is not rigorously correct for studio applications. If external burst flag is available, a positive pulse of between 1.0 V and 1.3 V (absolute value) can be applied to Pin 1 in the NTSC mode. This approach must be handled carefully, because a square pulse smaller than 1.0 V will not trigger the burst generator, and a square pulse larger than 1.3 V will shut off the burst generator almost before it starts. This direct injection technique does not provide the ramp to operate the PAL flip-flop. Another method, suitable for either PAL nor NTSC, is shown in Figure 4. It requires a "vertical drive" pulse, starting at the leading edge of vertical blanking and as wide as the interval where burst is not wanted (usually 9 line intervals). The extra transistor and diodes in the circuit add an abrupt step at the beginning of each line ramp which inhibits burst generation.

THE COLOR REFERENCE OSCILLATOR/BUFFER

As stated earlier in the general description, there is an on-board common collector Colpitts color reference oscillator with the transistor base at Pin 17 and the emitter at Pin 18. When used with a common low-cost tv crystal and capacitive divider, about 0.65 Vpp will be developed at Pin 17. The adjustment of oscillator frequency can be done with a series 30 pF trimmer capacitor over a total range of about 1.0 kHz. Oscillator frequency should be adjusted for each unit, keeping in mind that most monitors and receivers can pull in 1200 Hz.

If an external color reference is to be used exclusively, it must be continuous. The components on Pins 17 and 18 can be removed, and the external source capacitively coupled into Pin 17. The amplitude at Pin 17 should be between 0.5 Vpp and 1.0 Vpp, either sine or square wave.

It is also possible to do both; i.e., let the oscillator "free run" on its own crystal, and also be capable of being overridden from an external source. An extra coupling capacitor of 50 pF from the external source to Pin 17, and a signal of 1.0 Vpp was adequate with the limited experimentation attempted.

VOLTAGE CONTROLLED 90°

The oscillator drives the (B-Y) modulator and a voltage controlled phase shifter which produces an oscillator phase of 90° ± 7° at the (R-Y) modulator. If it is necessary to adjust the angle to better accuracy, the circuit shown in Figure 6 can be used. Pulling Pin 19 up will increase the (R-Y) to (B-Y) angle by about 0.25°/µA. Pulling Pin 19 down reduces the angle by the same sensitivity. The nominal Pin 19 voltage is about 6.3 V, so the 12 V supply is best for good control, even though it is unregulated. In most situations, the result of an error of 7° is very subtle to all but the most expert eye. For effective adjustment, the simplest approach is to apply RGB color bar inputs and use a vectorscope. A simple bar generator giving R, G and B outputs is shown in Appendix D.

RESIDUAL FEEDTHROUGH COMPONENTS

As shown on the MC1377 data sheet (and in Figure 2 (d), the composite output at Pin 9 for fully saturated color bars is about 2.6 Vpp, output with full chroma on the largest bars (cyan and red) being 1.7 Vpp. The typical device, due to imperfections in gain, matrixing, and modulator balance, will exhibit about 20 mVpp residual color subcarrier in both white and black. Both residuals can be reduced to less than 10 mVpp for the more exacting applications. The black imbalance is primarily in the modulators and can be nulled by sourcing or sinking small currents into clamp Pins 11 and 12 as shown in Figure 7. The nominal voltage on these pins is about 4.0 Vdc, so 8.2 V is capable of supplying a pull up source. (Pulling Pin 11 down is in the 0° direction, up is 180°. Pulling Pin 12 down is in the 90° direction, up is 270°.)
FIGURE 4(a) — VERTICAL PERIOD BURST INHIBITOR

FIGURE 4(b) — VERTICAL INTERVAL WHEN MC1377 STANDARD RAMP CIRCUIT IS USED

FIGURE 4(c) — STANDARD RAMP CIRCUIT

FIGURE 4(d) — VERTICAL INTERVAL WITH BURST INHIBITOR CIRCUIT

FIGURE 4(e) — BURST INHIBITOR RAMP CIRCUIT (NOTE FAINT RAMP CAUSED BY VERTICAL DRIVE PULSE)
FIGURE 5 - INTERNAL SCHEMATIC
FIGURE 5 - INTERNAL SCHEMATIC
Any direction of correction may be required from part to part. (Note that pulling Pin 11 up can produce a residual carrier on the horizontal back porch which is the same phase as burst, and can result in an almost normal color display even with burst not present.)

![FIGURE 6 — ADJUSTING MODULATOR ANGLE](image)

![FIGURE 7 — NULLING RESIDUAL COLOR CARRIER IN BLACK](image)

![FIGURE 8](image)

White carrier imbalance at the output can only be corrected by juggling the relative levels of R, G and B inputs for perfect balance. Standard devices are tested to be within 5% of balance at full saturation. Black balance should be adjusted first, because it affects all levels of gray scale equally. There is also usually some residual baseband video at the chroma output (Pin 13), which is most easily observed by disabling the color oscillator. Typical devices show 0.4 V pp of residual luminance for saturated color bar inputs. This is not a major problem since Pin 13 is always coupled to Pin 10 through either a bandpass or a high pass filter, but it serves as a warning to pay proper attention to the coupling network.

THE CHROMA COUPLING CIRCUITS

Without going deeply into the subject, it is generally true that monitors and receivers have color IF 6.0 dB bandwidths of ±0.5 MHz. It is therefore recommended that the encoder should also limit the chroma bandwidth to approximately ±0.5 MHz through insertion of a band-pass circuit between Pins 13 and 10. For proper color level in the composite output, a mid-band insertion loss of 3.0 dB is desired. The bandpass circuit shown in Figure 1, using the TOKO fixed tuned transformer (see Appendix B) gives this result. One of many tv color IF bandpass circuits could also be used. When such a bandwidth reduction is inserted, the chroma is delayed by approximately 350 ns (as shown in Figure 8).

This 350 ns delay results in a visible displacement of the color and black and white information on the final display. The solution is to place a delay line in the luminance path from Pins 6 to 8 to realign the two components. Again, a normal tv receiver delay line can be used. These delay lines are usually of 1.0 k to 1.5 k characteristic impedance, and the resistors at Pins 6 and 8 should be selected accordingly. A very compact, lumped constant delay line is available from TDK (see Appendix C for specifications). Some types of delay lines have very low impedances (approximately 100 ohms) and should not be used, due to drive and power dissipation requirements.

In some applications, it may be possible to delete both the bandpass transformer and the delay line. For instance, when the RGB information itself is very low resolution, i.e., very narrow band (less than 1.5 MHz), no cross-talk would be generated in the encoder (see Figure 9). Keep in mind, however, that the standard monitor or receiver will still "see" an incorrect luminance sideband at X'. This points up the value of at least some chroma bandwidth reduction in the encoder. A simpler, lower cost bandpass circuit is shown in Figure 10(a). It provides the proper insertion loss, approximately ±1.0 MHz bandwidth, and about 100 ns delay. The circuit shown in Figure 10(b) is even less costly, but has about 6.0 dB greater loss, provides very little bandwidth reduction except to remove the baseband feedthrough, and produces essentially no delay.

![FIGURE 9](image)

It will be left to the designer to decide which, if any, compromises are acceptable. Color bars viewed on a good monitor can be used to judge acceptability of step luminance/chrominance alignment and step edge transients, but signals containing the finest detail to be encountered in the system must also be examined before settling on a compromise.
THE OUTPUT STAGE

The output amplifier normally produces about 2.0 Vpp and is intended to be loaded with 150 ohms as shown in Figure 11. This provides about 1.0 Vpp into 75 ohms, an industry standard level (RS-343). In some cases the input to the monitor may be through a large coupling capacitor. If so, it is necessary to connect a 150 ohm resistor from Pin 9 to ground to provide a low impedance path to discharge the capacitor. The nominal average voltage at Pin 9 is over 4.0 volts. The 150 ohm dc load causes the current supply to rise another 30 mA (to approximately 60 mA total into Pin 14). Under this (normal) condition the total device dissipation is about 600 mW. The calculated worst case die temperature rise is 60°C, but the typical device in a test socket is only slightly warm to the touch at room temperature. The solid copper 20-Pin lead frame in a printed circuit board will be even more effectively cooled.

The MC1377 is designed to operate from an unregulated 10.8 to 13.2 volt dc power supply. Device current into Pin 14 with open output is typically 30 to 32 mA. To provide a stable reference for the ramp generator and the video output, a high quality 8.2 V internal regulator is provided. The 8.2 V regulator can supply up to 10 mA for external uses, with an effective source impedance of less than 1.0 ohm. This regulator is convenient for a tracking dc reference for dc coupling the output to an RF modulator. Typical turn-on drift for the regulator is approximately +35 mV over 1–2 minutes in otherwise stable ambient conditions.

SUMMARY

The preceding Application Note was intended to detail the application and basis of circuit choices for this versatile tv signal encoder. A complete MC1377 application with the MC1374 VHF modulator is shown in Figure 12. The internal schematic diagram of the MC1377 is provided in Figure 5. If further assistance is needed, contact Motorola Linear and Military IC Division, Applications Engineering.
APPENDIX A

In full RGB systems, three information channels are wired from the signal source to the display to permit unimpaired image resolution. The detail reproduction of the system is limited only by the signal bandwidth and the capability of the color display device. Higher than normal sweep rates may be employed to add more lines within a vertical period. Three separate projection picture tubes can be used to eliminate the "shadow mask" limitations of a conventional color CRT.

Figure (b) below shows the "baseband" components of a studio NTSC signal. As in the previous example, energy is concentrated at multiples of the horizontal sweep frequency. The system is further refined by precisely locating the color subcarrier midway between luminance spectral components. This places all color spectra between luminance spectra and can be accomplished in the MC1377 only if "full interlaced" external color reference and sync are applied. The individual components of luminance and color can then be separated by use of a comb filter in the monitor or receiver. This technique has not been widely used in consumer products, due to cost, but it is rapidly becoming less expensive and more common.

The unequal bandwidths of I and Q cannot be implemented with the MC1377, first because I and Q axes are not used, and second, because outputs of the two color modulators are added before any bandwidth reduction is imposed. Most monitors and receivers compromise the "standard" quite a bit, by using responses as shown in Figure (c). Some crosstalk of luminance information into chroma, and vice versa, is always present. The acceptability of the situation is enhanced by the suppression of the color carrier and the generally limited ability of the CRT to display information above 2.5 MHz. If the signal from the MC1377 is to be used primarily to drive conventional non-comb filtered monitors or receivers, it would be best to reduce the bandwidth at the MC1377 to that of Figure (c) to lessen crosstalk.

Spectral Energy Is Always Concentrated At Horizontal Sweep Frequency Multiples

FIGURE 13(a) — SPECTRA OF A FULL RGB SYSTEM

FIGURE 13(b) — NTSC STANDARD SPECTRAL CONTENT

FIGURE 13(c) — TYPICAL MONITOR/TV

FIGURE 13(d) — COLOR VECTOR RELATIONSHIP, I/Q SYSTEM versus (R–Y)/(B–Y) SYSTEM SHOWING STANDARD COLORS
APPENDIX B
A PROTOTYPE CHROMA BANDPASS TRANSFORMER
TOKO SAMPLE NUMBER 166NNF-10264AG

Connection Diagram
Bottom View

Unloaded Q (Pin 1–3): 15 @ 2.5 MHz
Inductance: 30 µH ± 10% @ 2.5 MHz
Turns: 60 (each winding)
Wire: #38 AWG (0.1 m/m)

APPENDIX C
A PROTOTYPE DELAY LINE
TDK SAMPLE NUMBER DL122401D-1533

*MARKING: PART NUMBER, MANUFACTURER'S IDENTIFICATION,
DATE CODE AND LEAD NUMBER.

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Time Delay</td>
<td>400 ns ± 10%</td>
</tr>
<tr>
<td>2 Impedance</td>
<td>1200 Ohms ± 10%</td>
</tr>
<tr>
<td>3 Resistance</td>
<td>Less Than 15 Ohms</td>
</tr>
</tbody>
</table>
| 4 Transient Response with 20 ns Rise-Time Input Pulse | Pre-Shoot: 10% Max  
Over-Shoot: 10% Max  
Rise-Time: 120 ns Max |
| 5 Attenuation | 3 dB Max at 6.0 MHz |
APPENDIX D
AN RGB PULSE GENERATOR

RGB PULSE GENERATOR
TIMING DIAGRAM

Reset (From Composite Blanking)

154 kHz Clock
Blue Output

Black White Yellow Cyan Green Magenta Red Blue
Red Output

Green Output
A Cost Effective VHF Amplifier For Land Mobile Radios

By Ken Dufour
Motorola Power Products Division

INTRODUCTION

This application note describes a two stage, 30 watt VHF amplifier featuring high-gain, broad bandwidth and outstanding ruggedness to load mismatch, achieved by use of the new MRF1946A power transistor. It uses a die geometry intended for RF power devices operating in the UHF region. The emitter periphery (EP) to base area (BA) ratio of this die is 4.9, up from the normal EP/BA range of 1.5 to 3.5 for VHF devices. Power sharing and current sharing in the chip are controlled with diffused emitter resistors. The end result is a VHF transistor with very high power gain (10 + dB), sufficient so that processing steps can be taken to provide tolerance to load mismatch while still maintaining excellent performance. By mounting this die in the 0.380 flange or stud package and providing characterization data that spans 136 to 220 MHz, Motorola has provided a very versatile component for the RF designer.

CIRCUIT DESCRIPTION

Smith chart techniques were used to develop the two stage amplifier shown pictorially in Figure 1 and schematically in Figure 2. The end result is an amplifier that can produce 20 dB overall gain in the specified band (150 to 175 MHz), with a midband efficiency of 50 percent. The Motorola MRF237 was selected for the driver stage. This...
common emitter (TO-39) RF power transistor produces high-gain, is easy to mount and is cost effective. In this design, the MRF237 is inserted into a hole in the circuit board and soldered to the ground plane for heat sinking, as shown in Figures 1 and 3. This method of attachment also provides a very effective emitter ground connection. By introducing a small amount of forward bias (5–15 mA) to the MRF237, it will track low drive levels and help maintain stability in the input stage. The amplifier is constructed on 1/16", double sided G-10 board with 2 ounce copper cladding. A photomaster of the printed circuit board is shown in Figure 4. The top and bottom ground planes of the board are connected by wrapping the board edges with thin copper foil (0.002") and then soldering it in place. Figures 1 and 3 illustrate how and where the board edges are wrapped in the prototype amplifier. No eyelets or plated-through-holes are required to achieve the level of performance noted here. Printed lines are used to match the devices’ input and output impedance to 50 ohms, and an inductor and two capacitors form the interstage match. This allows some flexibility in shaping the overall frequency response and helps conserve board area. The MRF1946A stage is operated in Class C and is mounted to the heatsink using conventional methods, i.e.; an 8–32 stud inserted into an appropriately prepared heatsink. An alternate packaging arrangement, the 0.380 flange, allows one to attach the transistor to the topside of the heatsink with two screws. A Motorola Application Note on mounting techniques for various semiconductors is available and provides detailed information on installing either of these package styles (see reference 1). Additional information on thermal considerations can be found in reference 2. Performance of the amplifier is illustrated in Figures 5, 6 and 7. Figure 5 is a plot of $P_{out}$ versus $P_{in}$ at 160 MHz, 12.5 volts; Figure 6 shows output power, input VSWR and collector efficiency as functions of frequency; while Figure 7 demonstrates harmonic content for 30 watts output power.

![Figure 2. Schematic Diagram of MRF1946A Wideband Amplifier](image-url)

C1 = 56 pF Dura Mica  
C2 = 39 pF Mini-Unelco  
C3, C7 = 68 pF Mini-Unelco  
C4, C5, C6, C9, C10 = 91 pF Mini-Unelco  
C8 = 250 pF Unelco J101  
C11 = 36 pF Mini-Unelco  
C12 = 43 pF Mini-Unelco  
C13 = 1 µF, 25 V Tantalum  
C14, C15 = 0.1 µF Mono-Block  
C16 = 10 µF 25 V Electrolytic  

D1 = Diode, 1N4933 or Equivalent  
L1 = Base Lead Cut to 0.4", Formed into Loop  
L2 = Collector Lead Cut to 0.35", Formed into Loop  
L3 = 0.7" #18 AWG into Loop  
L4 = 7 Turns #18 AWG, 1/8" ID  
L5 = 3 Turns #16 Enam, 3/16" ID  
R1 = 10 Ω, 1/4 W Carbon  

RFC1 = 10 µH Molded Choke  
RFC2 = 0.15 µH Molded Choke  
RFC3 = VK200–4B Choke  
B = Printed Line  
Z1, Z2 = 50 Ohm Printed Line  
Z3 = 50-590-65-3B  

R2 = 1500 Ω, 1/2 W (Select For Most Appropriate ICQ)  

Figure 2. Schematic Diagram of MRF1946A Wideband Amplifier
Figure 3. Parts Placement.

Figure 4. PCB Photomaster (not full size)
CONCLUSIONS

The two-stage amplifier described produces greater than 20 dB gain with 30 watts of output power over the frequency range of 150 to 175 MHz. Ruggedness and stability are achieved by use of the new MRF1946/A power transistor. The amplifier illustrates that relatively unsophisticated construction techniques properly implemented with the appropriate high gain devices can provide a cost effective 30 watt VHF amplifier for land mobile applications.

REFERENCES

Introduction

The MC145159 is a phase-locked loop frequency synthesizer with an analog, or more specifically a sample-and-hold, phase detector. The output of this phase detector (APD<sub>out</sub>) is used as a fine error signal. The synthesizer also contains a digital frequency steering phase comparator for coarse adjustment of loop frequency, separate power supply pins for the analog phase detector, a lock detect output, and on-chip logic for control of a dual-modulus prescaler. (See Figure 1.)

Other features of the MC145159 are a 14-bit reference counter, as well as a 10-bit divide-by-<i>N</i> counter and a 7-bit divide-by-<i>A</i> counter. All three counters are programmed via a serial data stream which is compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs. The device also has on-chip circuitry to support an external crystal. OSC<sub>in</sub> may also serve as an input for an externally-generated reference signal. This signal is typically ac coupled to OSC<sub>in</sub>, but for larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

With the features listed above, the MC145159 finds general purpose applications in such areas as 2-way radios, cellular radiotelephones, and avionics equipment.

As stated earlier, the MC145159 has a sample-and-hold phase detector. As opposed to standard digital phase comparators with fixed gain, the gain of the sample-and-hold phase comparator is programmable. Four external components, two resistors and two capacitors, help set the gain and drive levels of the phase detector. Higher gain is achievable with the MC145159 phase detector versus digital phase detectors.

Because a high degree of filtering compromises overall loop performance, phase detectors which provide an error signal that is as clean as possible prior to filtering are extremely advantageous. One obvious benefit of the sample-and-hold phase comparator is that its output is analog, and therefore already resembles the required control voltage necessary to drive the loop’s voltage-controlled oscillator (VCO), thereby minimizing filtering requirements. Ideally, this control voltage is a perfectly clean signal with no undesired perturbations. Any of these disturbances cause unwanted modulation on the VCOs output signal. For high performance radio equipment, the sidebands resulting from this modulation must be very low. The analog output reduces VCO modulation sidebands and also allows for wider loop bandwidths than are normally possible with digital phase detector outputs.

Figure 1. Logic Diagram

*NOTE: Pin 6 is not and cannot be used as a digital phase detector output.
TRADITIONAL SAMPLE-AND-HOLD PHASE DETECTORS

Before examining the method by which the MC145159 performs a sample-and-hold function, the theory of operation of traditional sample-and-hold phase detectors will be reviewed.

The reference signal (divided-down OSCin signal) and current source are used to establish the sawtooth voltage on the ramp capacitor, $C_R$. (See Figures 2 and 3.) $C_R$ is charged by the current source and quickly discharged by a switch that is controlled by the reference signal. In this way, the period of the sawtooth voltage is equal to the period of the reference signal. The divided-down VCO signal is used to sample the sawtooth voltage by closing a sampling switch for a window of time and letting the hold capacitor, $C_H$, charge to the sampled voltage. Neglecting leakage current, the charge established on $C_H$ at the end of the sample time remains constant until the next sample. If for some reason the VCO frequency begins to rise above the desired value, the phase of the sampling pulse falls back and sampling is done at a lower sawtooth voltage. This action, in effect, lowers the control voltage to slow down the VCO and keep the divided-down VCO frequency locked to the reference frequency. Likewise, if the VCO frequency falls below the desired value, the phase of the sampling pulse advances and sampling is done at a higher sawtooth voltage. This action raises the control voltage which speeds up the VCO to keep the divided-down VCO frequency locked to the reference frequency.

One serious side effect of this scheme is that an undesired ripple voltage occurs on $C_H$. This rippling is caused by the ramp waveform charging from level $V_A$ to level $V_B$ during the sample window. Upon opening of the sampling switch, $C_H$ is charged to $V_B$ and remains at $V_B$ until the switch is closed again and voltage $V_A$ is applied to the hold capacitor. Therefore, the hold capacitor is charged to $V_B$ and discharged to $V_A$ while in a locked condition. In effect, a ripple-free lock voltage cannot be established on $C_H$. The magnitude of this ripple is a function of the ramp charging slope, sample window time, and hold capacitor charge/discharge times.

To mask out the rippling effect, one solution is to follow $C_H$ by a second sampling switch and hold capacitor combination along with the necessary control signals. However, this additional circuitry introduces more switching transients and consumes more chip and/or board space.

![Figure 2. Traditional Sample-And-Hold Phase Detector Block Diagram](image)

![Figure 3. Traditional Sample-And-Hold Phase Detector Timing Diagram](image)
OPERATION OF THE MC145159

THEORY

The MC145159 uses a new, patented design approach for sample-and-hold phase detectors called ramp clamping, which results in improved performance over the traditional approach. Ramp clamping minimizes the need for a second hold capacitor, and in most applications only one hold capacitor is needed. When the loop is in frequency lock, the rising edge of \( f_R \) (divided-down \( \text{OSC}_{\text{in}} \) signal) activates a constant current source to initiate charging of the ramp capacitor. (See Figures 4 and 5.) The slope of this ramp waveform is also known as the phase detector gain. The ramp voltage continues to build, at a rate determined by \( R_R \), \( C_R \), and \( V_{DD'} \), until the rising edge of \( f_V \) (divided-down VCO signal) terminates the charge signal, thereby establishing a constant voltage on \( C_H \). After a predetermined delay (equal to two clock cycles of \( f_{\text{in}} \)) this ramp voltage is sampled onto the hold capacitor during a sample window lasting four periods of \( f_{\text{in}} \). \( C_H \) is then isolated from \( C_R \) and, after a delay of two clock cycles of \( f_{\text{in}} \), \( C_R \) is discharged. This cycle repeats every \( f_R \) period. The \( f_V \) edge relative to the \( f_R \) edge in time therefore determines how long the ramp charges before being clamped and sampled onto \( C_H \). This establishes the hold voltage necessary to maintain loop lock. The voltage on \( C_H \) feeds an N-channel source follower, the output of which \( \text{APD}_{\text{out}} \) controls an external VCO.

When the loop is out of frequency lock, that is when \( f_R \) and \( f_V \) are not in a one-to-one relationship over a \( 2\pi \) window with respect to \( f_R \), the Frequency Steering Output \( \text{FSO} \) becomes active. As a general rule, \( f_R \) and \( f_V \) must differ by 2% for the FSO to become active. However, as the reference frequency decreases, the frequency steering sensitivity increases. If the divided-down VCO frequency, \( f_V \), is lower than the divided-down oscillator frequency, \( f_R \), \( f_V < f_R \) then FSO pulses high. If \( f_V > f_R \), then FSO pulses low. The FSO pulse width is approximately equal to the period of time between two \( f_V \) pulses if \( f_V > f_R \), or two \( f_R \) pulses if \( f_R > f_V \). FSOs repetition rate is equal to the difference frequency between \( f_R \) and \( f_V \). When \( f_V = f_R \) over a \( 2\pi \) window with respect to \( f_R \), then the FSO remains in a high-impedance state and phase lock is maintained by the analog phase detector output. (See Figure 6.) By combining \( \text{APD}_{\text{out}} \) and FSO, the required low-noise VCO control voltage is provided by \( \text{APD}_{\text{out}} \), while the FSO provides a coarse error signal to achieve fast frequency lock.

The ramp clamp approach to phase detector design, which is implemented on the MC145159, offers significant advantages over the traditional method of sample-and-hold phase comparators. In traditional sample-and-hold detectors, ramp slewing during the sample window causes rippling on the hold capacitor. Therefore, a second hold capacitor and sampling switch may be needed. The ramp clamp technique, however, alleviates the need for a second hold capacitor and all of its related circuitry. This becomes very significant in the production of monolithic integrated circuits due to the savings in chip area that result.

Another benefit of ramp clamping is that the ramp amplitude is not allowed to go beyond the value reached when sampling occurs. The traditional method permits the ramp capacitor to charge all the way up to the positive supply voltage value; in most cases well after sampling has occurred. This extends the ramp amplitude beyond that allowed with the ramp clamp approach. A lower ramp pulse results in less ripple in the output error signal caused by parasitic ramp feed-through. With ramp clamping, the ramp amplitude is limited to only that value necessary to keep the loop locked and, more importantly, it provides a constant voltage to the hold capacitor during the entire sample window.

![Figure 4. Analog Phase Detector Logic Detail](image-url)
A word of caution exists for the analog phase detector power supply pins, \( V_{DD}' \) and \( V_{SS}' \). These two pins are provided to help isolate the analog section from noise coming from the digital sections of this device and also noise from the surrounding circuitry. Ensure that \( V_{DD}' \) and \( V_{DD} \) are at the same voltage potential at all times. Likewise, \( V_{SS}' \) and \( V_{SS} \) must be at the same potential at all times. Otherwise, damage to the MC145159 may occur due to latch up.

![Analog Phase Detector Timing Diagram](image)

Figure 5. Analog Phase Detector Timing Diagram (N = 17)

![Frequency Steering Output Timing Diagram](image)

Figure 6. Frequency Steering Output Timing Diagram

NOTE: \( f_R = \frac{f_{OSC}}{R} \), \( f_V = \frac{f_{in}}{N} \). The R and N counter outputs are not externally available.

*The FSO sensitivity limits are not guarantees, but are design aids.
PHASE DETECTOR GAIN

As stated earlier, the gain of the analog phase detector on the MC145159 is programmable. The gain is set by \( V_{DD} \) and two external components; the ramp resistor, \( R_R \), and the ramp capacitor, \( C_R \). The user must therefore determine the optimal value of gain for his or her system.

To select the optimal gain for the phase detector, let us assume a PLL system with a reference frequency of 10 kHz. (See Figure 7a.) With this frequency going into the phase detector, consecutive \( f_R \) pulses occur 100 \( \mu s \) apart. Assuming that the Frequency Steering Out pin has already pulled the system into frequency lock and turned off, the Analog Phase Detector Output is in complete control. Therefore, the rising edges of \( f_R \) and \( f_V \) can be nearly 100 \( \mu s \) apart. Because \( f_R \) initiates the ramp waveform and \( f_V \) terminates the charging cycle, the ramp should be at most 100 \( \mu s \), or 2\( \pi \) radians wide.

Moreover, the ramp should be capable of charging from VSS' to \( V_{DD} \) during this time. The design equation for phase detector gain given in the data sheet is stated as:

\[
K_\phi = \frac{l_{charge}}{2\pi f_R C_R} \quad [V/\text{rad}]
\]

Substituting in for \( K_\phi \), and \( f_R \) and selecting a value for \( C_R \), one can solve for \( l_{charge} \). From \( l_{charge} \), the value of ramp resistance, \( R_R \), is taken from Figure 8.

In this example, the gain of the phase detector is \( V_{DD}/2\pi \) [V/\text{rad}]. Larger values of gain can certainly be used. In fact, higher gain results in faster lock times. (See Figure 7b.) There is, however, an upper limit to the amount of gain selected. Higher gain is achieved by increasing \( V_{DD} \) or reducing \( R_R \) or \( C_R \) (or some combination thereof). Increasing phase detector gain by reducing the size of the ramp capacitor leads to increased noise induced into the ramp, and consequently, hold capacitors.

On the other hand, too little gain results in the ramp capacitor taking slightly longer to reach the required error voltage level, thereby widening the ramp waveform. This increased area under the curve represents more energy being transferred to the hold capacitor. The result is an increased potential to modulate the control voltage, yielding higher sidebands on the VCO output. Therefore, each system must be carefully analyzed and optimized for the gain/noise tradeoff.

The analog phase detector of the MC145159 can track changes in its input over a 2\( \pi \) range with respect to \( f_R \). The digital frequency steering portion of the device produces error signals over a wide range of input frequency differences.

OUTPUT BIAS CURRENT RESISTOR

Included on the MC145159 is a pin dedicated for use with an external component, called the output bias current resistor. A resistor connected from this pin \( R_{O1} \) to VSS' biases the output N-channel transistor, thereby setting a current sink on the analog phase detector output. With larger values of output resistance, the analog output bias current decreases (See Figure 9.)
METHOD OF PROGRAMMING THE COUNTERS

The MC145159 contains three fully-programmable counters. The R, N, and A counters are programmed by a serial data bit stream. (See Figure 10.) Perusing the logic diagram of the device gives insight as to how the counters are loaded with data. (See Figure 1.)

First, the desired values for R, N, and A must be converted to binary form with the proper amount of bit positions. Note that the R counter is 14 bits long, the N counter 10 bits long, and the A counter 7 bits long. To load the data, the Enable pin must be taken low to isolate the counters from changes that occur in the shift registers. With Enable low, data is then loaded into the shift registers on the rising edge of the clock input. Care must be taken to ensure that Data, Clock, and Enable voltage levels and rise, fall, setup, hold, and recovery times are not violated. The divide-by-R word is loaded first with its most-significant bit as the first bit entered. The divide-by-N word follows immediately, again with its most-significant bit as the first bit entered. Next is word A, similarly with its most-significant bit entering first. The last bit of the string is the control bit. A logic one for the control bit allows all the counters to be loaded with shift register information when Enable is taken high. A logic zero entered as the control bit inhibits a reference counter latch load. Therefore, only the N and A counters are loaded when Enable is taken high.

Finally, after all the data is properly loaded into the shift registers and the control bit is at the desired logic state, Enable is taken high to program the counters. After satisfying the minimum input pulse width for Enable, that pin must then be taken low to isolate the counters from outside disturbances.

For example, suppose system requirements dictate that the R, N, and A counters be programmed with 40, 200, and 72, respectively. The steps to load the counters are outlined below.

<table>
<thead>
<tr>
<th>Action</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Take Enable low (&lt;0.3 Vdd)</td>
<td>Isolate the counters</td>
</tr>
<tr>
<td>2. Shift in eight 0s</td>
<td>Start loading R word</td>
</tr>
<tr>
<td>3. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>4. Shift in one 0</td>
<td></td>
</tr>
<tr>
<td>5. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>6. Shift in five 0s</td>
<td>R word entered; start loading N word</td>
</tr>
<tr>
<td>7. Shift in two 1s</td>
<td></td>
</tr>
<tr>
<td>8. Shift in two 0s</td>
<td>N word entered</td>
</tr>
<tr>
<td>9. Shift in one 1</td>
<td>Start loading A word</td>
</tr>
<tr>
<td>10. Shift in three 0s</td>
<td></td>
</tr>
<tr>
<td>11. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>12. Shift in two 0s</td>
<td></td>
</tr>
<tr>
<td>13. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>14. Shift in three 0s</td>
<td>A word entered</td>
</tr>
<tr>
<td>15. Shift in one 1</td>
<td>Control bit high</td>
</tr>
<tr>
<td>16. Take Enable high (&gt;0.7 Vdd)</td>
<td>Load the three counters</td>
</tr>
<tr>
<td>17. Take Enable low (&lt;0.3 Vdd)</td>
<td>Isolate the counters</td>
</tr>
</tbody>
</table>

Now that the counters are loaded with the correct information and the system is working properly, changing the output frequency is desired. New values of N and A are chosen while keeping R the same. (R is only used in this case to set up the system resolution.) The same method can be used to program the N and A counters while simply ignoring the R counter. Take Enable low, shift in the appropriate binary data for N and A, shift in a control bit of logic zero to isolate the R counter form the Enable line, and pulse high the Enable input.

For example, suppose the new values for N and A are 178 and 13, respectively. The steps to load the counters are outlined below.

<table>
<thead>
<tr>
<th>Action</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Take Enable low (&lt;0.3 Vdd)</td>
<td>Isolate the counters</td>
</tr>
<tr>
<td>2. Shift in eight 0s</td>
<td>Start loading R word</td>
</tr>
<tr>
<td>3. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>4. Shift in one 0</td>
<td></td>
</tr>
<tr>
<td>5. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>6. Shift in five 0s</td>
<td>R word entered; start loading N word</td>
</tr>
<tr>
<td>7. Shift in two 1s</td>
<td></td>
</tr>
<tr>
<td>8. Shift in two 0s</td>
<td>N word entered</td>
</tr>
<tr>
<td>9. Shift in one 1</td>
<td>Start loading A word</td>
</tr>
<tr>
<td>10. Shift in three 0s</td>
<td></td>
</tr>
<tr>
<td>11. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>12. Shift in two 0s</td>
<td></td>
</tr>
<tr>
<td>13. Shift in one 1</td>
<td></td>
</tr>
<tr>
<td>14. Shift in three 0s</td>
<td>A word entered</td>
</tr>
<tr>
<td>15. Shift in one 1</td>
<td>Control bit high</td>
</tr>
<tr>
<td>16. Take Enable high (&gt;0.7 Vdd)</td>
<td>Load the three counters</td>
</tr>
<tr>
<td>17. Take Enable low (&lt;0.3 Vdd)</td>
<td>Isolate the counters</td>
</tr>
</tbody>
</table>

Figure 10. Data Entry Format
**Action**

1. Take Enable low
2. Shift in two Os
3. Shift in one 1
4. Shift in one 0
5. Shift in two 1s
6. Shift in two Os
7. Shift in one 1
8. Shift in four Os
9. Shift in two 1s
10. Shift in one 0
11. Shift in one 1
12. Shift in one 0
13. Take Enable high
14. Take Enable low

**Comment**

Isolate the counters
Start loading N word

N word entered; start loading A word

A word entered

Control bit low
Load the two counters
Isolate the counters

As is evident, the two prior routines are serial in nature. A microprocessor is therefore best suited to program the counters. Also, note that the counter outputs are not available on the MC145159 for checking correct counter operation. However, a shift register output, SRout, is available. (See Figure 1.) Therefore, the same microprocessor that programs the counters can also be used to verify the contents of the shift registers to ensure that the correct data has been loaded. Enable must be held low while verifying shift register contents to avoid affecting the counters.

Although the MC145159 has on-chip logic for control of an external dual modulus prescaler, the device is capable of performing in a single modulus mode simply by leaving the modulus control output unconnected. In this case, the 10-bit divide-by-N counter performs the loop divide-by-N function. The A counter must still be loaded with data, but that data is a don’t care. However, loading the A counter with all Os is strongly recommended. In that way, the modulus control output is stuck high and cannot cause any possible interference by switching periodically.

**f\textsubscript{in}, OSC\textsubscript{in} LIMITS**

Although not stated on the data sheet, the f\textsubscript{in} and OSC\textsubscript{in} limits for the MC145159 are the same as for the rest of the silicon-gate MC1451XX family of frequency synthesizers. (See Figures 11 and 12.) One limit is 15 MHz for a supply voltage of 5 V and a divide value of six or greater for the N and R counters. For the time being, refer to these graphs for frequency limits.

The analog phase detector component values play a small role in determining the input frequency limits at the input to the phase detector. For high reference frequencies, a large value of I\textsubscript{charge} is most likely required. Make certain that component values are in specified ranges. For best results, the following limits are recommended. (Low-leakage polystyrene or Mylar capacitors are recommended for CR and CH.)

\[
1 \, \text{k\Omega} \leq R_R \leq 1 \, \text{M\Omega} \\
500 \, \text{pF} \leq C_R \leq 0.1 \, \mu\text{F} \\
10 \, \text{C}_H \leq C_R \\
10 \, \text{k\Omega} \leq R_O \leq 1 \, \text{M\Omega}
\]

*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.*

**Figure 11. OSC\textsubscript{in} and f\textsubscript{in} Maximum Frequency versus Total Divide Value**

--28
\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p

\[\text{T} = 25°C\]
SQUARE WAVE, V\textsubscript{DD} - V\textsubscript{SS}
SINE WAVE, 500 mVp-p
DUAL-MODULUS PRESCALING CONSTRAINTS

The MC145159 contains all the necessary logic for control of an external dual-modulus prescaler. Dual-modulus prescaling is a solution to some of the shortcomings associated with single-modulus prescaling. Inherent in the design of synthesizers using single-modulus prescaling is the fact that the value of the reference frequency into the phase detector is multiplied by the prescale value P, as well as by the counter value, N. (See Figure 13.) This results in a loss of system resolution because any unitary change of N results in the output frequency of the VCO changing by the reference frequency times P, which may be undesired.

Dual-modulus prescaling is a solution to this problem. It allows VCO step sizes equal to the value of the phase detector reference frequency to be obtained. This technique utilizes an additional A counter and a special prescaler which divides by any one of two values, depending upon the state of its control line. (See Figure 14.) In dual-modulus prescaling, the lower speed counters are uniquely configured. Special control logic is necessary to select the divide value, P or P + 1, in the prescaler for the required amount of time.

The modulus control signal is low at the beginning of a count cycle, enabling the prescaler to divide by P + 1, until the A counter has counted down to zero. At this time, modulus control goes high, enabling the prescaler to divide by P, until the N counter counts down the rest of the way to zero; N minus A additional counts.

\[ N_{tot} = (P + 1)A + P(N - A) \]

\[ N_{tot} = NP + A \]

Modulus Control is then set back low, the counters preset to their respective programmed values, and the sequence is repeated.

This provides for a total programmable divide value of (N times P) + A. To have a range of total divide values in sequence, the A counter is programmed from zero through P - 1 for a particular value N in the N counter. N is then incremented by 1 and the A counter is sequenced from zero to P - 1 again.

Certain constraints apply when using dual-modulus prescaling: 1) N is greater than or equal to A always applies; 2) the value of P must be large enough so that the maximum frequency of the VCO divided by P must not exceed the frequency capability of the N and A counters; also, 3) P times the period of the maximum VCO frequency must be greater than the sum of the prop delay through the dual-modulus prescaler plus the prescaler setup or release time relative to its control signal plus the propagation delay of frequency in (f_in) to Modulus Control.

![Figure 12. OSCin and f_in Maximum Frequency versus Temperature for Sine and Square Wave Inputs](image)

![Figure 13. Single-Modulus Prescaling](image)
FREQUENCY SYNTHESIZER EXAMPLE

Suppose the MC145159 is to be used in a system which operates from 118.000 to 135.975 MHz in 25 kHz steps, i.e., aircraft communication transceivers. (See Figure 15.) A pre­
scaler is needed to divide down the maximum VCO output frequency to a frequency that the MC145159 can handle (15 MHz maximum at VDD = 5 V). A minimum prescale value of 10 is required. However, if a divide-by-10 single-modulus pre­
scaler is used, the reference frequency would have to be ad­
justed to 2.5 kHz in order to maintain the 25 kHz step size. Therefore, dual-modulus prescaling is desired and the
MC12016 divide-by-40/41 prescaler is selected due to an input
frequency capability of 225 MHz and the ability to divide down
the VCO frequency to well under 15 MHz.

Figure 14. Dual-Modulus Prescaling

Figure 15. Typical System Application
With a reference frequency of 25 kHz, the N and A counters must be loaded with the proper values to achieve 118 to 135.975 MHz at the loop output. For example, at $f_{\text{max}}$:

$$N_{\text{tot}} = \frac{135.975 \text{ MHz}}{25 \text{ kHz}}$$

$$N_{\text{tot}} = 5,439$$

To arrive at programming values for N and A, use:

$$N_{\text{tot}} = N P + A$$

Substituting in, and for now, letting $A = 0$:

$$5,439 = N(40)$$

$$N = 135.975$$

Therefore, $N = 135$ is used. Now, $A$ must be determined.

$$A = N_{\text{tot}} - NP$$

$$A = 5,439 - (135)(40)$$

Similarly, at $f_{\text{min}}$:

$$N_{\text{tot}} = \frac{118 \text{ MHz}}{25 \text{ kHz}}$$

$$N_{\text{tot}} = 4,720$$

$$N_{\text{tot}} = NP + A$$

Substituting in, and for now, letting $A = 0$:

$$4,720 = N(40)$$

$$N = 118$$

Therefore $N = 118$ and $A = 0$.

A table can be built up showing the values of $N$ and $A$ and their corresponding loop output frequencies.

**Table 1. Output Frequencies and Their Corresponding N and A Counter Values ($f_{\text{ref}} = 25 \text{ kHz}, P = 40$)**

<table>
<thead>
<tr>
<th>Output Frequency (MHz)</th>
<th>$N_{\text{tot}}$</th>
<th>N</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>118.000</td>
<td>4,720</td>
<td>118</td>
<td>0</td>
</tr>
<tr>
<td>118.025</td>
<td>4,721</td>
<td>118</td>
<td>1</td>
</tr>
<tr>
<td>118.050</td>
<td>4,722</td>
<td>118</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>...</td>
<td></td>
</tr>
<tr>
<td>118.975</td>
<td>4,759</td>
<td>118</td>
<td>39*</td>
</tr>
<tr>
<td>119.000</td>
<td>4,760</td>
<td>119</td>
<td>0</td>
</tr>
<tr>
<td>119.025</td>
<td>4,761</td>
<td>119</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>...</td>
<td></td>
</tr>
<tr>
<td>135.950</td>
<td>5,438</td>
<td>135</td>
<td>38</td>
</tr>
<tr>
<td>135.975</td>
<td>5,439</td>
<td>135</td>
<td>39</td>
</tr>
</tbody>
</table>

*Note that because $P = 40$, the maximum value of $A = 39$.

In the example above, a 25 kHz reference frequency is used. This frequency is generally established at the reference input of the phase detector by an on-chip oscillator used with an external crystal. The R counter is programmed to divide down the crystal frequency to the required reference frequency, in this case 25 kHz. With the MC145159, the divide-by-R range is from 3 to 16,383. Therefore, the designer has many options in choosing the crystal frequency. One example is a 3.2 MHz crystal with a divide-by-R of 128 to yield a reference frequency of 25 kHz. Obviously, many other combinations are possible.

Now, a suitable gain must be chosen for the phase detector. With a 25 kHz reference frequency, successive $f_R$ pulses occur 40 $\mu s$ apart. For the first attempt, the ramp capacitor is chosen to charge up to $VDD^{'}$ in one-eighth the time, or 5 $\mu s$. (The slope with which the ramp capacitor charges is the phase detector gain.) Therefore, the selected gain is 6.4 V/rad with a 5 V supply. Larger values of gain can be selected to speed up lock times; however, induced noise in the loop may be increased.

Values of phase detector components can now be determined using the equation for phase detector gain.

$$K_\phi = \frac{I_{\text{charge}}}{2\pi f_R C_R} \quad \text{[V/\text{rad}]}$$

letting $C_R = 500 \mu F$ and solving for $I_{\text{charge}}$ yields

$$I_{\text{charge}} = 500 \mu A$$

Figure 8 shows that the graph for $VDD = 5 \text{ V}$ crosses the 500 $\mu A$ axis at $R_R = 20 \text{ k} \Omega$. With $C_R = 500 \mu F$, $C_H$ is chosen to be 50 pF. Slightly larger values for hold capacitance may be required for noise considerations. Finally, the output resistor ($R_O$) can be any value between 10 k$\Omega$ and 1 M$\Omega$, as long as the analog output bias current is compatible with the employed low-pass filter. (See Figure 9.)

A major concern in designs with the MC145159 is combining the analog phase detector output with the Frequency Steering Output properly. Three possible methods are shown in Figure 16. It should be noted that these three connection schemes are theoretical only and have not been tested in the lab. Methods of connecting these two outputs will be the subject of a forthcoming application note.

The low-pass filter and voltage-controlled oscillator must also be planned out carefully for optimal loop performance. For the MC145159, the loop filter can be combined with the connection scheme for the phase detector outputs. Further filtering may be necessary if dictated by the system requirements. In the previous example of aircraft communication transceivers, a VCO must be chosen for the loop. The Motorola MC1648 is a good choice due to an output frequency capability above the $f_{\text{max}}$ constraint of 135.975 MHz. Consult the MC1648 data sheet for VCO design considerations.

With the loop all in place and powered up, the counters must be programmed for the synthesizer to tune to the desired channel. From Table 1, suppose 135.975 MHz is the VCO output frequency desired. The $N$ counter should be programmed to 135 and the $A$ counter to 39. Also, with a 3.2 MHz crystal and 25 kHz channel spacing, the $R$ counter should be programmed to 128.
**CONCLUSION**

This application note discussed the open-loop characteristics of the MC145159 PLL frequency synthesizer with analog phase detector. The MC145159 uses an improved method over the traditional sample-and-hold technique while providing an alternative to digital phase detectors in frequency synthesis applications. The Frequency Steering Output together with the Analog Phase Detector Output combine to produce an error signal without the introduction of excessive noise. In fact, this phase detector scheme minimizes filtering requirements, reduces VCO modulation sidebands, and allows for wider loop bandwidths than are normally possible with digital phase detector outputs.

An additional application note is planned to cover the closed-loop application of the MC145159, especially the methods for combining the two phase detector outputs.

**REFERENCES AND ACKNOWLEDGMENTS**

1. *CMOS/NMOS Special Functions Data*, Motorola Inc.


Motorola has developed a series of low power narrowband FM dual conversion receivers in monolithic silicon integrated circuits. The MC3362 and the MC3363 are manufactured in Motorola's MOSAIC process technology. This process develops NPN transistors with $f_T = 4 + GHz$, which allows the MC3362 and the MC3363 to have excellent very high frequency (VHF) operation with low power drain. They are ideal for application in cordless phones, narrowband voice and data receivers, CB and amateur band radios, radio frequency (RF) security devices and other applications through 200 MHz.

Features of the MC3362/3 Receiver ICs:
- Broadband RF input frequency capability (to 200 MHz using internal oscillator, over 450 MHz using external oscillator)
- Single supply operation from $V_{CC} = 2$ to 7 Vdc
- Low power consumption ($I_{CC} = 3 mA$ typical at $V_{CC} = 2$ Vdc)
- Internally biased NPN RF transistor amplifier (MC3363)
- Complete dual conversion circuitry — first mixer and oscillator included
- First local oscillator (LO) includes buffered output and varactor diode to allow phase locked-loop (PLL) frequency synthesis for multichannel operation.
- Buffered second local oscillator output available for PLL reference input (MC3362)
- Multistage limiter and quadrature detection circuitry included
- RSSI (Received Signal Strength Indicator) with Carrier Detect logic included
- Built-in data slicing comparator detects zero crossings of FSK data transmission
- Inverting operational amplifier included for audio muting or active filtering (MC3363)

SCOPE

This application note contains functional descriptions and applications information pertaining to the various functional blocks of the MC3362/3 receiver circuits. Four receiver application circuits are shown. A single channel receiver and a 10 channel frequency synthesized receiver designed for the 49 MHz cordless telephone band are shown. A 256 channel "2 Meter" (144–148 MHz) amateur band receiver is also shown, including an appropriate PLL frequency synthesizer design to control the receiver’s local oscillator. Finally, a low cost application featuring the MC3362 as a single chip manually tunable 162 MHz weatherband receiver is shown. A directory of external component manufacturers is included as an appendix.

COMPARISON OF THE MC3362 AND THE MC3363

Figures 1A and 1B show the system block diagrams of MC3362 and MC3363, respectively. The MC3362 and the MC3363 are made from the same die, but a final metal mask difference allows different features to be made available on each. Data pertaining to the common functional blocks are identical on both circuits.

The MC3363 is a complete VHF dual conversion FM receiver including RF amplifier, two mixers and oscillators, limiting IF amplifier and quadrature detection circuitry, received signal strength indicator (RSSI) circuitry, squelch circuitry and a data shaping comparator for detecting FM frequency shift keyed (FSK) data transmissions. Receivers using the MC3363 alone can achieve better than 0.3 µV input sensitivity for 12 dB SINAD, from a 50 Ω source. The MC3363 comes in a 28-lead plastic wide SOIC package only.

The MC3362 is optimized for cordless telephone applications and as such does not contain the RF preamplifier or squelch circuitry. In addition, the second local oscillator contains a buffered output so that it can serve as the system frequency reference in applications where a 10.240 MHz or 10.245 MHz reference is needed. In general, the MC3362 can be substituted for the MC3363 where:
- A receiver with sensitivity of 0.7 µV at the input for 12 dB SINAD is adequate.
- An external RF preamplifier with AGC is desired (such as MOSFET's 3N211 and MPF211).
- Receiver squelch is not needed.
- Surface mount technology cannot be used. The MC3362 is available in two 24-lead plastic packages (DIP and wide SOIC surface mount).
Figure 1A. MC3362 Internal Block Diagram
Figure 1B. MC3363 Internal Block Diagram
FEDERAL REGULATIONS, RECOMMENDED STANDARDS

Radios built for certain VHF and UHF bands may qualify under the FCC Code of Federal Regulations Title 47, Part 15, for use by unlicensed operators. It is important to know the federal regulations concerning a particular frequency channel or band of channels before a receiver or transmitter circuit is designed. Contact the FCC/Government Printing Office to order a copy of the Code of Federal Regulations, Title 47, Parts 0–20 which contains Part 15, before designing a radio receiver or transmitter for unlicensed utility applications.

Professional (landmobile) radios come under another part (Part 90) of the Title 47 code. There are a set of regulations for two way communication equipment. These standards provide useful information about radio performance, terminology and measurement techniques and are useful even if professional radios are not a designer's primary goal. Contact the EIA at (202) 457-4900 to order the standards listed below. The FCC/GPO can be reached at (202) 275-2054 or (213) 894-5841. The pertinent documents are:

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
<th>Parts Referenced</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCC Title 47, Part 90 Code of Federal Regulations</td>
<td>Landmobile Radios</td>
<td></td>
</tr>
<tr>
<td>RS-204-C</td>
<td>EIA Recommended Standard</td>
<td>FM/PM Receiver Standards</td>
</tr>
<tr>
<td>EIA-152-B</td>
<td>EIA Recommended Standard</td>
<td>FM/PM Transmitter Standards</td>
</tr>
<tr>
<td>EIA-316-B</td>
<td>EIA Recommended Standard</td>
<td>Test Conditions, Radio Standards</td>
</tr>
</tbody>
</table>

REFERENCE LITERATURE

The following Motorola literature may be useful when designing with the MC3362/3 receivers:

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
<th>Parts Referenced</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL128, Rev. 2</td>
<td>Linear and Interface Device Data</td>
<td>MC3362, MC3363, MC34119, MC2831A, MC2833, MC13060, MC33171</td>
</tr>
<tr>
<td>DL130</td>
<td>CMOS/NMOS Special Functions Data</td>
<td>MC1451XX CMOS PILL's</td>
</tr>
<tr>
<td>DL122</td>
<td>MECL Device Data</td>
<td>MC12XXX ECL</td>
</tr>
<tr>
<td>DL126</td>
<td>Small Signal Transistor Data</td>
<td>3N211, MPF211</td>
</tr>
</tbody>
</table>

COMPANION DEVICES

- The MC2831A and the MC2833 low power FM transmitter ICs provide all essential functions for cordless telephone and general transmitter and oscillator applications through 60 MHz (MC2831A) and 200 MHz (MC2833, using internal very high frequency [VHF] transistors as frequency multipliers).
- The MC34119 low power audio amplifier with differential outputs provides efficient power transfer and eliminates the need for the typical large audio coupling capacitor.
- The MC13060 Mini-Watt audio amplifier (for higher powered audio output).
- The MC33171 low power single supply operational amplifier for use as an RSSI buffer or active integrator.
- The MC14516X series of dual PLL frequency synthesizers for development of 10 channel cordless telephone band transceivers.
- The MC12XXX series of ECL prescalers and MC1451XX series of CMOS Frequency Synthesizers for development of VHF “high band” radios to 200 MHz.
- The MC145442/3 single chip 300 baud modems which allow audio frequency shift keyed (AFSK) RF modem design for very reliable data transmission.
- The 3N211 and MPF211 dual gate MOSFET's for MC3362 RF preamplification with AGC capability.

BLOCK DESCRIPTION

RF Amplifier (MC3363 only)

The MC3363 contains an internal NPN bipolar RF amplifier transistor. The base of the transistor is biased internally to approximately 0.8 Vdc, which simplifies common-emitter amplifier design. Grounding the emitter yields an emitter current $I_E = 1.5$ mA and voltage gain $A_V = 20$ dB with a collector load $R_C = 1$ kΩ. Emitter degeneration resistors can be added to lower current drain, with $R_E$ decoupling used to preserve the gain. With the emitter grounded the input at Pin 2 looks like 180 Ω in parallel with 20 pF at 50 MHz. The noise figure at 50 MHz and unity gain frequency ($f_T$) of the NPN transistor are approximately 2 dB and 3 GHz, respectively, at $I_E = 1.5$ mA. The collector load can be resistive, as shown in Figure 10, or tuned as shown in Figure 14. When both input and output are tuned and/or impedance matched, care must be taken to prevent unwanted oscillations — this is why the 2 kΩ resistor is included in the collector load of Figure 14.

First Mixer

The first mixer is a doubly balanced multiplier, driven directly from the RF input and from the first local oscillator via a cascode amplifier. It is used to convert the RF input frequency down to the first IF of 10.7 MHz. The input admittance seen at either RF input pin is 670 ohms in parallel with 7 pF at 50 MHz; that is, $Y_{in} = 670$ Ω and $C_p = 7$ pF. The series equivalent impedance at 50 MHz is $R_s = 210$ Ω and $C_s = 10.2$ pF. The first mixer's input is differential, but can be driven single-ended with no loss in system gain. If a single-ended input is used, be sure to AC ground the unused pin. This can be done with a bypass capacitor to the negative rail (Vcc) or by connecting the pin directly to the VCC supply.

The isolation of the mixer is shown in Table 1, and of particular value in many applications will be the strong attenuation (41 dB) of the local oscillator at the mixer input. The isolation is due to the fully balanced mixer configuration used and helps to reduce LO radiation at the receiver's antenna.

<table>
<thead>
<tr>
<th>Signal</th>
<th>LO Tank</th>
<th>Mixer Out (IF)</th>
<th>Mixer In (RF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO</td>
<td>0</td>
<td>-17</td>
<td>-41</td>
</tr>
<tr>
<td>RF</td>
<td>-16</td>
<td>-9</td>
<td>0</td>
</tr>
<tr>
<td>IF</td>
<td>-29</td>
<td>0</td>
<td>&lt; -40</td>
</tr>
</tbody>
</table>

Table 1. First Mixer Isolation Level (in dB) at:
NOTES:

1. The varactor control pin controls the net capacitance across the local oscillator tank pins. The net capacitance will be approximately 20–25 pF when this pin is left open and 10–15 pF when connected to VCC, depending upon strays and the VCC value used. If the VCC supply is regulated, connect the varactor control pin to VCC; otherwise, bypass via a 0.01 µF capacitor to ground.

2. Connect the oscillator as shown in the left hand drawing (Initial Alignment) and adjust L1 so that the tank resonates approximately 2–3 MHz below the crystal frequency. The frequency should be checked by examining the buffered output using a high impedance probe or by some sort of inductive pickup which will not push the oscillator off frequency. The frequency should be:

\[ f_{\text{LO}} = \frac{1}{2\pi \sqrt{L_1 + L_2} C_{\text{varactor}}} \]

3. Break the L1–L2 connection and add X1 and R2. Verify that the LO operates at the desired frequency by applying an RF input of 10.7 MHz above or below the crystal frequency and checking for receiver quieting. Make sure that there is proper LO amplitude. Also there should be approximately 200 mVpp seen at either LO tank pin. The buffered LO output should yield 200–600 mVpp depending on the VCC value used.

4. The R2 resistor must be included or else the oscillator will latch.

5. This method has been proven effective up to 85 MHz using 3rd overtone crystals, but has proven unreliable at higher frequencies (usually using 5th and 7th overtone types). For higher frequency operation on a single channel, a signal can be injected into the local oscillator port. (See the “First Mixer and Oscillator” section.)

6. Component values: The R1 resistors should be 10 to 50 kΩ and are included in order to add some current and gain to the local oscillator. L1 should equal L2 in nominal value and a fixed value might be used but startup with different crystals might be degraded. R2 should be 300 to 1500 Ω. X1 should be 3rd overtone, series mode resonant (no load capacitance specified).

The open circuit conversion voltage gain of the first mixer is typically 24 dB, flat to 7 MHz. Internal rolloff is provided above 7 MHz to suppress RF and LO signals and spurious products sent on to the second mixer. The gain at 10.7 MHz is typically 18 dB. The output circuit is an emitter follower which is impedance-matched to 330 ohms to drive 10.7 MHz ceramic filters which typically have 330 ohm input and output impedances. For applications which require a high impedance crystal filters, impedance matching will likely need to be added at the first mixer's output to preserve the filter's response.

First Local Oscillator and Varactor Diodes

Associated with the first mixer is the first local oscillator (LO). It is a complete voltage controlled oscillator and only requires an external LC tank circuit (no external varactor diode). For multichannel applications, the oscillator includes varactor tuning and a buffered output suitable for interfacing to a PLL frequency synthesizer. This is the approach used in the receivers of Figures 10 and 11. The maximum oscillation frequency obtained has been approximately 190 MHz, achieved by injecting extra current into the oscillator. To inject current into the local oscillator, connect pull-up resistors of 10–50 kΩ from VCC to each LO tank pin. The LO buffered output varies from 400 mVpp to 1100 mVpp with supply voltage and the output waveform appears best with \( R_{pd} = 3 \) kΩ, as shown in Figure 3.

There are internal varactor diodes which have capacitance which appears across the local oscillator tank pins. The internal capacitance can range from 10 to 25 pF depending on the control voltage applied to the varactor control pin (MC3362 Pin 23, MC3363 Pin 27). The capacitance is maximum when the voltage applied is at the minimum (0.7 V) value. Applying voltages greater than VCC and lower than 0.7 V to the varactor control pin can cause the oscillator to stop.

The first local oscillator can be crystal controlled to run on a single channel. The procedure of Figure 2 shows how to do this for applications through 65 MHz. The receiver of Figure 10 uses this approach.

Figure 2. Running the MC3362/3 First Local Oscillator on a Single Channel Under Crystal Control

Figure 3. First Local Oscillator Buffered Output
A third application of the local oscillator is to drive it from an external source. This is recommended for applications from 75 MHz to 200 MHz and beyond which do not require PLL frequency synthesis. The inputs are differential and they must be driven using a wideband RF transformer or balun. The input voltage seen at either tank pin should be roughly 100 mVrms to ensure proper operation of the mixer and care should be taken so that any inductance present at the LO tank pins does not resonate with the internal varactor capacitance (a small valued resistor of 50–100 Ω should ensure this does not occur). Using this approach, no loss in mixer gain is seen until the RF and LO inputs are taken over 450 MHz. The RF and LO inputs should be run with a 10.7 MHz difference in frequency to accommodate the first IF bandwidth, so image frequency considerations (preselector filter quality) may limit the maximum RF input frequency to less than 450 MHz.

Second Mixer and Second Local Oscillator
After the 10.7 MHz IF signal is filtered using a ceramic filter, it is applied to the second mixer input. The second mixer is also doubly balanced to reduce spurious responses and typically is used to convert the 10.7 MHz IF down to 455 kHz for application to the limiting amplifier and detection circuitry. In the typical low cost application, the mixer is driven single-endedly from a ceramic filter, with one of the mixer inputs bypassed directly to the Vcc supply. The open circuit conversion voltage gain is typically 27 dB. For applications which require a high impedance crystal filter, impedance matching will likely need to be added at the second mixer input to preserve the filter response. The second mixer output is rolled off above 500 kHz, to reduce spurious response and idle noise.

The second local oscillator is a Colpitts type which is typically run under crystal control. The crystal used is specified for fundamental mode operation, calibrated for parallel resonance with a load capacitance of 30–40 pF. The typical waveform seen at the base is shown in Figure 4. The oscillator can be run at 10.240 MHz or 10.245 MHz, depending on the first local oscillator frequency desired.

The MC3362 second local oscillator has a buffered output available which can be used to drive the reference frequency input of a PLL synthesizer or a prescaler. An external local oscillator signal can be injected into the local oscillator's base, with the emitter pin left open. The signal should be sinusoidal and should be approximately 300 mVpp to 500 mVpp in level.

The output admittance of the second mixer at 500 kHz is 1500 Ω in parallel with 50 pF; that is, Rp = 1500 Ω and Cp = 50 pF. The series equivalent impedance is Rs = 1420 Ω and Cs = 1065 pF. This impedance matches the typical input impedance of standard 455 kHz ceramic filters, which have 1500–2000 Ω typical input and output impedances.

Limiting IF Amplifier and Quadrature Detector
The 455 kHz IF signal is applied to the limiting IF amplifier, where it is amplified and limited before application to the quadrature detection circuitry. The limiting IF amplifier input has an input impedance of approximately 1.5 kΩ, which provides good power transfer from 1.5 kΩ ceramic filters. The limiting IF circuitry has 10 µV input sensitivity for −3 dB limiting, flat to 1 MHz. In order to preserve overall power supply current drain, the limiting IF and the receiver in general are not designed for wideband applications.

The coupling capacitor from limiter output to quadrature tank and detector input is provided internally and its value is 5 pF. The 455 kHz oscillator circuit is typically built around an LC tank circuit, with Cp = 180 pF, Lp = 680 µH. Typical ceramic resonators can not be driven from the quadrature tank pin. A waveform like that of Figure 5 should appear at the quadrature tank pin during periods of full receiver quieting and no modulation.

Meter Drive (RSSI)
The amplitude of the RF input signal at the appropriate frequency is monitored by meter drive circuitry. This circuitry detects the amount of limiting in the limiting IF amplifier and produces a linear change in current (nominal 0.1 µA) at the meter drive pin for each decibel of change in the RF input. The meter drive circuitry is fairly...
linear for input signal levels over a 60 dB range. This output can be used as a meter drive or Received Signal Strength Indicator (RSSI) and needs to be buffered. In order to provide a linear, wide ranging RSSI output voltage, three things must be accomplished:

1. The Meter Drive pin (MC3362 Pin 10, MC3363 Pin 12) should be clamped to within VBE/2 (approximately 300 mV) of the MC3362/3 supply voltage, or loading of the Meter Drive's current source will occur. The carrier detect output is disabled (high output) when the Meter Drive pin is clamped in this manner. There are diodes present at the Meter Drive pin which can interfere with the Meter Drive. (See Figure 6 for a schematic representation.) With these diodes present the voltage swing possible at the Meter Drive pin is limited to a diode drop above and below the VCC supply.

2. Some type of current to voltage conversion must take place. The RSSI output is typically 4 to 12 µA.

3. Negative feedback must be provided in the output buffer to counteract buffer amplifier gain variations. Some method of output level adjustment may be desirable.

![Figure 6. Schematic Representation of Meter Drive “Parasitic Circuits”](image)

**Carrier Detect**

Another configuration for the meter drive and carrier detect circuitry, is to program the carrier detect output using a resistor from the meter drive pin to the VCC supply. The carrier detect pin is an open collector output so a pull-up resistor is required. The carrier detect is active low, meaning that an RF input above the programmed trip level will yield a low output (<0.1 V) at the carrier detect pin. When the RF input is below the trip level (or is detuned) the carrier detect pin will be at the supply voltage. The trip level is set by the resistor value used between the meter drive pin and supply. A resistor of 130 kΩ sets the trip level to approximately ~110 dBm at the first mixer's input, which is roughly the 12 dB SINAD point of the receivers with no external RF amplification. It should be noted that the meter drive current will not have the same linear 0.1 µA/dB current-input level relationship as when the meter drive is buffered as discussed above, so an analog RSSI output is not really achievable when Carrier Detect is used.

![Figure 7. Sample RSSI Buffer](image)

- Recommend MC33171 as the operational amplifier. The MC33171 is a low-power single supply single op amp with offset adjustment capability.
- \( V_{CC1} = \text{MC3363 supply (2 V to 7 V)} \)
- \( V_{OUT} = V_{CC1} + I_{\text{meter}}(R_f) \)
- \( V_{CC2} = \text{Op amp supply. Make this high enough to stay within the op amp's common mode input range — equal to } V_{CC1} + 2.2 \text{ V for the MC33171. This voltage also must be high enough to provide the maximum } V_{OUT} \text{ desired.} \)
- \( R_{IS} \) can be added to level shift the output, and is optional. The output voltage will be adjusted downward by a factor of \( (V_{CC1} - V_{CC2})(R_f/R_{IS}) \).
- Compensation capacitor \( C_C \) is added to ensure stability and will limit the circuit's response time.
- This circuit is not recommended for general purpose AM detection.

**Muting (MC3363 only)**

Audio muting can be provided in two ways. The carrier detect output can be DC coupled to the MC3363 muting op amp input (Pin 15) and the op amp output can serve to mute the audio. That is, the op amp output (Pin 19) serves as a switch to ground in the audio signal path. When the carrier level decreases below the carrier detect trip point, the carrier detect pin will go to VEE and the op amp output will go into saturation, muting the audio. This yields a simple squelch with minimum external components and is shown in Figures 10 and 14.

Another way to mute the audio on MC3363 is to use the op amp as an active filter for detecting noise above the audio passband. The recovered audio is fed through the active filter, rectified, integrated and compared to a reference level. When the level rises above the reference, a squelch gate is triggered. The data slicing comparator on the MC3363 might be used as a squelch gate. This type of squelch frees the Meter Drive circuit to provide a linear output as noted under "Meter Drive (RSSI)" above.
Data Recovery

Both receivers contain a data slicing comparator which provides data shaping and limiting of frequency-shift keyed (FSK) serial data transmissions. The data slicer is a non-inverting type, with the negative input terminal biased internally to VCC/2. Typically the data slicer is AC coupled to the recovered audio pin via a 0.01 µF to 0.1 µF capacitor. Larger coupling capacitors can cause distortion of the detected output and this is seen as negative slew rate limiting in Figures 8 and 9. A pull down resistor from the detector output pin to VEE will reduce this effect if objectionable. The comparator output is an open collector so a pull-up resistor is required.

Comparator hysteresis is available by connecting the comparator output and input using a high-valued resistor. This helps maintain data integrity as the recovered audio becomes noisy, or for long bit strings of one polarity. Resistor values below 120 kΩ are not recommended as the comparator input signal will not be able to overcome the large hysteresis induced. Figure 8A shows data jitter resulting from noisy demodulated data signal. The improvement seen when hysteresis was added is shown in Figure 8B.

The maximum usable FSK data rate for any narrowband FM system is typically 1200 baud subject to IF and quadrature bandwidth and adjacent channel spacing limitations. The approximate bandwidth required to generate or receive a frequency modulated signal is:

\[ BW = 2 \left( f_{\text{mod}} + f_{\text{dev}} \right) \text{ kHz}, \]

where \( f_{\text{mod}} \) is the modulating frequency and \( f_{\text{dev}} \) is the frequency deviation.

This is known as Carson's Rule and is fairly accurate. Any modulating signal which exceeds the available IF bandwidth will be attenuated and/or distorted. For proper recovery of square waves including the leading and trailing edges approximately the 7th harmonic should be present. For a 1200 baud (600 Hz) square wave with \( f_{\text{dev}} = 3 \text{ kHz}, f_{\text{mod}} = 4.2 \text{ kHz} \) (7th harmonic of 600 Hz square wave), the bandwidth needed is: \( BW \approx 2(4.2 + 3) \text{ kHz} = 14.4 \text{ kHz} = \pm 7.2 \text{ kHz} \), which is acceptable in narrowband FM channels. Figures 9A and 9B show the effect of trying to pass a 9600 baud modulated carrier through a narrowband channel, with resulting degradation of recovered data.

Figure 8A. Noisy Recovered Data Signal Causes Data Jitter

Figure 8B. Improvement in Data Jitter Through Addition of Hysteresis

Figure 9A. FSK Data Recovery at 1200 Baud

Figure 9B. Distortion of Recovered Audio with 9600 Baud Modulation
For narrowband RF modems where 300 baud is adequate, an audio frequency shift keyed (AFSK) approach is recommended. In this application two audio tones (for Logic "0" and Logic "1") are modulated onto an RF carrier and transmitted to the receiver, which reproduces the audio tone sequence. The audio tones can be generated at the transmitter and decoded after the receiver by the MC145442/3 single chip 300 baud modems.

**APPLICATIONS CIRCUITS**

**Single Channel VHF FM Narrowband Receiver**

The first application shown is of a complete single channel VHF receiver operating at 49.67 MHz. This application includes a suitable circuit for running the first local oscillator under crystal control on a single channel, which is particularly useful for dedicated remote control links and low cost two-way radios through 75 MHz. The circuit contains a simple carrier level based squelch circuit and audio amplification.

The 49.67 MHz receiver frequency is within the 49 MHz USA cordless telephone band. Radios built for this band may qualify under FCC Code of Federal Regulations Title 47, Part 15, for use by unlicensed operators. It is important to know the federal regulations concerning a particular frequency channel or band of channels before a receiver circuit is design (see the notes on FEDERAL REGULATIONS, RECOMMENDED STANDARDS above).

Figure 10 shows the complete receiver schematic. The LC network shown is used to match the input impedance.
of the RF amplifier to 50 Ω at this frequency. The amplifier collector load is a single resistor for simplicity and in order to enhance stability. The method of Figure 2 was used to develop the crystal controlled oscillator circuit at 38.97 MHz. The RC integrator rolls off the audio above 2 kHz in order to minimize unwanted noise output. This enhances receiver sensitivity and provides proper audio deemphasis. The receiver, without the audio amplifier, has 6.2 mA current drain at \( V_{CC} = 5 \) V for a total dissipation of 31 mW. Using a 455 kHz filter with a 6 dB bandwidth of \( \pm 10 \) kHz the receiver has a 12 dB SINAD point of 0.28 \( \mu \)V, modulation acceptance of 10.4 kHz and distortion below 1.2% with \( f_{mod} = 1 \) kHz and modulation deviation \( f_{dev} = 3 \) kHz. The maximum (S+N)/N ratio obtained is 60 dB.

The MC34119 audio amplifier adds 3 mA quiescent current drain at 5 V, can deliver 250 mW into an 8 Ω speaker and has differential outputs which eliminate the need for the typical large audio coupling capacitor. It also has a chip disable input which provides muting and power conservation.

**Ten Channel Frequency Synthesized Cordless Telephone Receiver**

A demonstration receiver circuit has been built featuring the MC3362 and the MC145160 dual phase locked loop (DPLL). This receiver features frequency synthesis to cover the ten channels allocated in the USA for cordless telephone (CT) receivers in the 46 MHz (handset) and 49 MHz (base station) frequency ranges. The MC14516X series DPLL’s feature two complete loops which control both the transmitter output and receiver first LO frequencies.

![Circuit Diagram](image)

*Figure 11. Ten Channel Frequency Synthesized Receiver*
audio distortion is less than 3 percent. The minimum noise floor is less than 80 µV and the maximum (S+N)/N ratio is 53 dB.

There is a simpler way to interface the MC3362/3 to the MC145160 DPLL as shown in Figure 13. The VCO signal (about 400 mVpp with VCC = 3 V using a pull-down resistor of 3 kΩ from the MC3362 Pin 20 to VEE) is fed directly into the Fin-R input (Pin 16) of the MC145160. With this configuration, the noise floor is raised to 245 µV, 10 dB higher than the circuit of Figure 11.

256 Channel Frequency Synthesized Two Meter Amateur Band Receiver

A more traditional PLL frequency synthesizer approach is needed to provide frequency flexibility and to allow the MC3362/3 receivers to operate in the VHF “high band” (130 MHz to 172 MHz). A receiver is shown which covers the entire Two Meter (referring to radio wavelength) amateur radio band from 144 MHz to 148 MHz in 256 channels spaced at 20 kHz. The complete receiver and PLL frequency synthesizer are shown in Figures 14 and 15. The receiver achieved the same specifications as the 49.67 MHz MC3363 receiver discussed above.

The MC3363 receiver was chosen because squelch and good sensitivity with minimum component count were desired. To obtain good operation of MC3363 VCO above 75 MHz, the first local oscillator must be running well. To ensure this, the VCC supply voltage is kept above 3 V which increases the current in the local oscillator circuitry. Extra current is also injected into the local oscillator via pull-up resistors of 10 kΩ from each of the local oscillator tank pins to the VCC supply. With the components of Figure 14, the receiver VCO had an average gain of 1.5 MHz/V.

The VCO output is amplified and fed into an MC12017 dual modulus prescaler which drives the input of the PLL frequency synthesizer. The MC145152-1 PLL frequency synthesizer was chosen for its ease of use and parallel input format. The MC33171 bipolar operational amplifier was chosen as the active integrator (loop filter) because of its low power drain, offset adjustment capability and ability to operate from a single supply voltage. The design equations and assumptions used to determine loop filter components are shown below. The MC145152-1 data sheet and other sources go into much more detail on PLL theory and performance.

Calculations of Loop Filter For VCO PLL Frequency Synthesis
Assumptions:
- f0 = 135.3 MHz (local oscillator center frequency)
- fS = 20 kHz (channel spacing)
- fB = 0.01 fS (loop bandwidth)
- fC = 20 fB (filter cutoff frequency)
- $\xi = 0.707$ (loop damping factor)
- VDD = 5 V (PLL supply voltage)
- KVCO = 9.4 x 10^6 rad/V (VCO gain, measured on MC3363 receiver)
- C1 = 0.1 µF (active integrator component)
Results:

\[ f_b = 0.01 \]  \[ f_s = 0.01 \text{ (20 kHz)} = 200 \text{ Hz} \]

\[ f_{rc} = 20 \]  \[ f_b = 20 \text{ (200) = 4 \text{ kHz} \]}

\[ K_\phi = V_{DD}/2\pi = 0.796 \text{ (phase detector gain)} \]

\[ w_n = 2\pi f_b \]

\[ 0.5(2) - 0.5 - 1257 = 610 \text{ rad/sec} \]

\[ \frac{25^2 + 1 + (1257 + 1)^2}{2} - 1 = 1257 \]

\[ N_t = \frac{f_b}{f_s} = 135.3 \text{ MHz to 20 kHz = 6765} \]

\[ R_1 = K_{VCO} N_t \frac{w_n}{2} N_t = 29.7 \text{ k} \Omega = 30 \text{ k} \Omega \]

\[ R_2 = 2 \frac{0.5(2)}{w_n C_l} = 23.2 \text{ k} \Omega = 24 \text{ k} \Omega \]

\[ C_C = 4 \left(2 R_{1 fc}ight) = 0.017 \mu F \]

With an 8 bit parallel input format several possible switch settings and resultant counter values and receiver frequencies are shown in Table 2 below (Note: \( N_t = N_0 + P \), where \( P = 64 \) for the MC12017).

Table 2. PLL Frequency Synthesizer Switch Settings and Frequencies

<table>
<thead>
<tr>
<th>Switches</th>
<th>N</th>
<th>P</th>
<th>A</th>
<th>N_t</th>
<th>f_{VCO} (MHz)</th>
<th>f_{RX} (MHz + 10.7 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000000</td>
<td>104</td>
<td>64</td>
<td>0</td>
<td>6656</td>
<td>133.12</td>
<td>143.82</td>
</tr>
<tr>
<td>00000001</td>
<td>104</td>
<td>64</td>
<td>1</td>
<td>6657</td>
<td>133.32</td>
<td>143.84</td>
</tr>
<tr>
<td>01000000</td>
<td>105</td>
<td>64</td>
<td>0</td>
<td>3720</td>
<td>134.40</td>
<td>145.10</td>
</tr>
<tr>
<td>01111111</td>
<td>105</td>
<td>64</td>
<td>63</td>
<td>6783</td>
<td>135.66</td>
<td>146.36</td>
</tr>
<tr>
<td>10000000</td>
<td>106</td>
<td>64</td>
<td>0</td>
<td>6784</td>
<td>135.68</td>
<td>146.38</td>
</tr>
<tr>
<td>10011101</td>
<td>106</td>
<td>64</td>
<td>13</td>
<td>6797</td>
<td>135.94</td>
<td>146.64</td>
</tr>
<tr>
<td>11011100</td>
<td>106</td>
<td>64</td>
<td>28</td>
<td>6812</td>
<td>136.24</td>
<td>146.94</td>
</tr>
<tr>
<td>11111111</td>
<td>107</td>
<td>64</td>
<td>17</td>
<td>6865</td>
<td>137.30</td>
<td>148.00</td>
</tr>
</tbody>
</table>

LEGEND:

- X1 = 10.245 MHz, fundamental mode, load capacity 32 pF.
- F1 = 455 kHz ceramic filter, \( R_{in} = R_{out} = 1.5 \text{ k} \Omega \) to 2 k\Omega.
- Part numbers are muRata CFU455X or CFW455X — suffix denotes bandwidth.
- LC1 = 455 kHz quadrature tank circuit. Part numbers are Toko RMC2A 6597HM or SSVLC-0637BGT (smaller). Ceramic discriminators cannot be used with the MC3363/3, as their input impedance is too low.

Figure 14. 2 Meter Frequency Synthesized FM Receiver

Single Chip Weatherband Receiver

An application of the MC3362 as a simple receiver tuned to the NOAA Weatherband (162.4 MHz to 162.55 MHz) is shown in Figure 16. The RF input is applied directly to the mixer input, using a simple "L network" to provide impedance matching of the mixer input to 50 \Omega. The system sensitivity for 12 dB SINAD is 0.67 \mu V at the input from a 50 \Omega source in this application, which is as good as most inexpensive weather cubes and the dual conversion design allows for excellent image protection to be provided.
NOTES:
1. The values of R1, R2, C1 and Cc are very important in determining the loop characteristics. Those values calculated in the text gave fairly "clean" VCO Control Voltage and VCO Buffered Output signals.
2. Switches S1–S8 can be mini-DIP or hexadecimally coded thumbwheel switches. S1 is the MSB, S8 is the LSB.
3. Vcc3 = 7.2 V minimum, to ensure that the MC33171's input common mode range is not exceeded. An acceptable way of configuring the entire receiver's power is:

Figure 15. 256 Channel VCO Control Using PLL Frequency Synthesizer

NOTES:
1. Make Vcc connections along a substantial portion of copper plane. Do NOT use point to point wiring for Vcc interconnections!
2. Vcc (MC3362) = 2 V to 7 V, regulated. First local oscillator will drift if this supply is not regulated!
3. Vcc2 (MC34119) = 2 V to 12 V, must be well decoupled from the Vcc source for the MC3362.
4. L1 = 3 turns #18 AWG, .2" dia., .05" spacing, air wound.
5. Pins 1 and 24 are differential RF input, and are unmatched and used single-ended in this circuit. If single-ended input is used, be sure to bypass the unused pin.
6. All capacitors in microfarads, inductors in Henries and resistors in Ohms, unless otherwise specified.

Figure 16. MC3362 Application as a Tunable Weather Band Receiver
The first local oscillator is free-running in this application and the receiver is manually tunable over a range of ±1 MHz. The oscillator’s frequency and tuning range are determined by the external tank circuit values chosen. Keep in mind that the internal varactor diodes add 10–25 pF of capacity across the tank pins, depending on the varactor control voltage applied.

This circuit is easily built to verify receiver characteristics on the lab bench, but as shown is not suited for mass production. The local oscillator temperature stability is not nearly adequate in this free-running configuration and microphonic pickup is difficult to avoid. Before a narrowband receiver is production-ready, the first local oscillator must be stable to within approximately ±100 Hz. The "First Mixer and Oscillator" section provides notes on driving the first mixer using an external oscillator signal above 50 MHz. The MC2833 FM transmitter IC might serve as the local oscillator source up to 200 MHz.

**SUMMARY**

The high degree of integration and MOSAIC process used in the MC3362/3 receivers give the radio designer new levels of space and power economy, while providing high performance and considerable design flexibility. The receivers shown and alternate configurations discussed should interest designers of cordless phones, VHF two-way radios, remote control receivers, wireless data links and home security systems.

---

**APPENDIX — DIRECTORY OF COMPONENT MANUFACTURERS**

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Contact Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>muRata-Erie</td>
<td>(404) 436-1300 ceramic filters, coils</td>
</tr>
<tr>
<td>Toko America Inc.</td>
<td>(312) 297-0070 quadrature coils, crystal filters, coils, transformers</td>
</tr>
<tr>
<td>Mount Prospect, IL 60056</td>
<td>(800) 344-4539</td>
</tr>
<tr>
<td>Distributor — Digikeey</td>
<td>(800) 854-1881</td>
</tr>
<tr>
<td>Distributor — Inductor Supply</td>
<td>(800) 472-8421 (California)</td>
</tr>
<tr>
<td>Coilcraft</td>
<td>(312) 639-6400 coils</td>
</tr>
<tr>
<td>California Crystal Laboratories</td>
<td>(800) 333-9825 crystals</td>
</tr>
<tr>
<td>Comtec</td>
<td>(602) 526-4123 crystals</td>
</tr>
<tr>
<td>Fox Electronics</td>
<td>(813) 693-0099 crystals</td>
</tr>
<tr>
<td>International Crystals</td>
<td>(405) 236-3741 crystals</td>
</tr>
<tr>
<td>Standard Crystal Corporation</td>
<td>(818) 443-2121 crystals</td>
</tr>
</tbody>
</table>

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AN1019

NTSC Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation

Prepared by
Ben Scott and Khalid Shah
Bipolar Analog IC Division

PREFACE

The TDA3330 is a composite video to RGB Color Decoder originally intended for PAL and NTSC color TV receivers and monitors. The data sheet is oriented toward picture tube drive, rather than cable level outputs. This application note is intended to supplement the data sheet by providing circuits for video cable drive, such as used in video processing circuits, frame store, and other specialized applications, and to expand upon the functional details of the TDA3330.

CIRCUIT CONSTRUCTION TECHNIQUES

The best solution is a single or double sided PC board, such as shown in Figure 11, with as much ground plane as possible. The oscillator components at Pins 8 and 9 must be close to the pins. A low profile socket is acceptable for prototyping. Wirewrap is definitely not recommended. In most respects the part is not sensitive to layout, except for the oscillator, however, unwanted picture artifacts, beats and noise are much easier to control with a good ground plane layout.

MEASURING THE OSCILLATOR

The oscillator amplitude at Pin 9 should be about 400 mVpp, measured with an ordinary 4.0 pF/10 MΩ scope probe. Keep in mind that the oscillator frequency is 3.58 MHz and is part of a phase-locked loop with only a few hundred Hz pull-in range. The scope probe loading is enough to push the oscillator into or out of lock. It is recommended that Pin 9 be observed initially to ascertain that it is running, and then leave Pins 8 and 9 alone. A procedure for adjustment will be covered later. Of course, an output buffer (emitter follower) can be connected to Pin 9, permanently, and the Pin 9 tuning capacitor reduced accordingly.

THE SANDCASTLE INPUT

“Sandcastle” is a familiar term to European TV engineers. It is basically a 0 V baseline with a 4.0 V blanking pulse and a 10 V burst-gating pulse on top of it, as shown in Figure 1. Sometimes the expression “super sandcastle” is used, which means that composite blanking is present, i.e. vertical and horizontal blanking, in addition to the burst-gating pulse. Sometimes the vertical blanking is 2.5 V and the horizontal is 4.0 V, sometimes both are at 4.0 V. In the TDA3330, the blanking portion is only used to provide a blanking waveform at the blanking output, Pin 11, which is used to supply “extra” blanking in the picture tube driver application. Pin 11 is not used in other applications, so the blanking portions of the “sandcastle” are not required. For the “cable to cable” decoder, all that the TDA3330 really needs at Pin 15 is the burst-gate pulse. Pin 16 should be grounded.

The burst-gate pulse has 3 functions:
1. Gating the color IF gain control (ACC) so that IF gain is adjusted to keep burst amplitude constant;
2. Setting the black level in the R, G, B outputs, and
3. Gating the color phase detector (APC) so that the VCO can be phase-locked to the burst. See the block diagram in Figure 2.
It is important that the burst-gate pulse into Pin 15 be at least 8.0 V and timed correctly with respect to incoming video, as shown in Figure 3. If the gate pulse is too late or too wide it will still be present after the blanking has ended, leading to serious errors in black level, color level and VCO lock. The burst-gate pulse can sometimes be obtained from the same equipment that supplies the video, or it can be generated by a couple of one-shots and a sync separator; see Figure 4. Another method is to separate sync. Use a one-shot pulse stretcher to make an 8–8.5 µs wide pulse for Pin 15, and then put the separated sync into Pin 16. (Pin 16 could be called the “burst-gate inhibit”). This will prevent the first part of the Pin 15 pulse from gating sync, which would upset the black level clamping function; see Figure 5.

THE LUMINANCE PATH

The outputs at Pins 12, 13 and 14 are positive-going video, with the sync pulse almost completely removed. The black level of the output remains constant as the contrast, saturation and hue are changed. The contrast control changes both luminance and chrominance together, so that, for example, output color bar waveforms maintain the same shape. The DC level of all outputs is moved by the brightness control, with no change in the peak to peak signal amplitude. The brightness control can change black level from 1.4 V to about 6.7 V as the control voltage on Pin 18 is raised from about 2.0 V to 5.0 Vdc. See Figure 6. The contrast control, Pin 19, is at maximum at 5.0 Vdc; the output is reduced 6.0 dB when the control is 3.5 Vdc, and is reduced about 40 dB when the control voltage is 1.0 Vdc.
The maximum output voltage, black to white, is about 7 times greater than the black to white level at Pin 17. For a composite input signal of 1.0 V_{pp}, there is 0.5 V_{pp} at Pin 17, due to the delay line matching resistors. This is about 0.35 V_{pp} white to black and gives about 2.5 V_{pp} max at the outputs. The input to the total circuit can be doubled to 2.0 V_{pp}, which then yields about 5.0 V_{pp} at Pins 12, 13, and 14. However, note that any change in input amplitude requires realignment of the saturation control for correct chroma/luma proportion. This is because the luminance component directly follows the input, while the color component is almost unchanged due to the ACC of the color IF. Therefore, it is important to note that the TDA3330 can be set up to work with different levels of input, but it is not automatically compensated for input changes. Also note that at 5.0 V_{pp} out and max 

**brightness** (black level out 6.7 V) there will be clipping of the positive peaks. The upper limit for the output is about 10 V.

Troubleshooting note: If a proper (positive) video signal is AC coupled into Pin 17, and a proper burst-gate is applied to Pin 15, there should be video out, regardless of any aspects of the color processing portions of the IC.

Figure 4. Method of Obtaining Burst-Gate from Composite Video

Figure 5. Alternate Method of Gating from Video
THE CHROMA PATH

The chroma input is derived from the composite input by a simple 3.58 MHz single-tuned bandpass circuit with about ±0.5 MHz (6 dB) bandwidth. The chroma portion of a color bar pattern should look like Figure 7. The circuit components recommended in our application circuit should yield about 100 mVpp of burst at Pin 22, but anything from 10–200 mVpp will work. The output of the chroma IF is at Pin 24, where the burst should be about 150 mVpp. There may or may not be chroma present, depending on the contrast and saturation control settings. (Both controls have exactly the same effect at Pin 24, changing the picture chroma amplitude between the burst pulses.)

Figure 7. Chroma IF Output, Pin 24

Troubleshooting note: If there is 1.5 Vpp of burst at Pin 24, the burst-gating pulse is either too small or incorrectly positioned in time.

The chroma IF output from Pin 24 is coupled to the chroma demodulators, Pins 4 and 5 by a small capacitor. (Note: 100 pF performs better than the 1.0 nF on the data sheet; it reduces luminance component feedthrough.) Tweaking of demodulator balance to reduce residual chroma subcarrier in the outputs can be done at Pins 4 and 5 by the trimmer technique shown in Figure 8. This is a fine tuning which is usually not needed, but is available for the demanding application.
COLOR LOCKUP

If the required chroma is present at Pins 4, 5 (same as Pin 24), and if the oscillator is known to be running, then lockup is just a matter of adjusting the trimmer on Pin 9. As noted earlier, the scope probe cannot be put on the oscillator for this adjustment. Instead, put the scope on the AFC filter, Pin 7. Waveforms as shown in Figure 9 will be observed as the trimmer is adjusted.

Lock-in range is about 18–22 pF with the typical socket and PC board and ordinary (Radio Shack) 3.58 MHz TV crystal.

BUFFERING THE OUTPUTS

In order to be able to drive a cable, it is necessary to provide an output amplifier. The design shown in Figure 10 has two additional benefits:

1. It provides an opportunity to reduce the residual 2nd harmonic of the color subcarrier (7.16 MHz) by means of a trap, and
2. It reduces the DC level another 0.7 Vdc at the emitter of the 2N4401, and an additional 2:1 reduction due to the 75 Ω series R into the 75 Ω cable. Therefore, the black level into the cable can be as low as 0.35 V, for the minimum brightness control setting.

MISCELLANEOUS GREMLINS

It has been reported from the field that the internally supplied NTSC mode switch current (I3 in Figure 12 of the data sheet) is occasionally insufficient. This is characterized by a decoder which intermittently decodes and then "color kills." In the killed mode, Pin 3 is above 1.5 V and Pin 2 is below 0.7 V, which holds the saturation control low (off). This can be fixed by putting 22 k from Pin 3 to VCC. This supplies additional current into Pin 3, causing an internal latch to pull Pin 3 low (have faith), and returns Pin 2 to an open state so it can be varied by the Saturation control.

SUMMARY

The TDA3330 has a wide range of functional capability with relatively simple application circuitry (once understood). It is hoped that this paper will assist users in becoming familiar and satisfied with it.

APPENDIX

Initial Setup Sequence for TDA3330 Evaluation Board

After connecting a Composite Video Signal In and connecting the Sync, Red, Green and Blue outputs to an appropriate RGB monitor, follow the subsequent steps, in order, to adjust the 11 variable components to optimize performance of the RGB decoder:

1. Look at the signal out of the collector of the 2N4402 transistor. Adjust POT #9 so that the Composite Video Signal at this point is 1.0 Vpp.
2. Set POTS #2 and 3 to approximately the middle of their values (i.e., 50 kΩ). This helps in making the subsequent adjustments.
3. POT #7 sets the Burst-Gate Width and POT #8 sets the Burst-Gate Delay relative to the Video Sync Signal. Use a dual input oscilloscope and look at the Video In signal and the Burst-Gate Signal at Pin 15 of the TDA3330. Adjust POT #8 so that the Burst-Gate Signal begins ~ 250 ns after the Sync Signal ends. Next adjust POT #7 so that the width of the Burst-Gate Signal is 3.5–4 µs. Note: See Figure 3.
4. Put the oscilloscope probe on Pin 7 of the TDA3330. Adjust the Variable Capacitor, connected to Pin 9, until the VCO is In Lock. This will happen when the trace signal drops from ~ 650 mVpp to less than 100 mVpp. Try to make the signal as small as possible, possibly down to dc. (Make tilt flat) Note: See Figure 9.
5. Put the oscilloscope probe on Pin 17 of the TDA3330. Adjust the 10 µH Variable Inductor to minimize Chroma Signal Feedthrough.
6. In order to fine tune chroma demodulator balance, remove the chroma signal from the Composite Video Signal In (or, alternatively, turn the saturation POT all the way down). Look at the Red output on the oscilloscope and adjust POT #2 to minimize subcarrier from the V Signal (i.e., R-Y) input. Next look at the Blue signal and adjust POT #3 to minimize subcarrier from the U signal (i.e., B-Y) input.
7. POTS #1, 4, 5 and 6 can next be adjusted to optimize picture color quality. Suggestion for doing this is to set Saturation (POT #1) and Brightness (POT #5) to middle and then adjust Contrast (POT #4 and Hue POT #6) till picture colors are approximately right. Next adjust POT's 1 and 5. Repeat the above sequence until satisfied with color quality of picture.
Figure 10. TDA3330 RGB NTSC Decoder Circuit

NOTE: 5.0 V Regulator is included for convenience and for the SN74LS221N. If the TDA3330P is to be operated from unregulated 12 V, the controls should be operated from unregulated (tracking) 5.0 V.
NOTES: 1. For the 390 pF and the 22 pF capacitors in the 3.58 MHz and in the 7.16 MHz traps, silver mica capacitors should be used for better trap performance.
2. The board layout is for Toko part #BTKANS-9439HM.
3. Board layout will accommodate a Toko or a TDK 400 ns delay line.
4. A 3.58 MHz crystal available through Radio Shack was used.

Figure 11a. TDA3330P RGB NTSC Decoder Evaluation Board, Component Layout
Figure 11b. TDA3330 RGB NTSC Decoder Evaluation Board, Component Side

Figure 11c. TDA3330P RGB NTSC Decoder Evaluation Board, Bottomside
Mounting Considerations for Power Semiconductors

Prepared by Bill Roehr
Staff Consultant, Motorola Semiconductor Sector

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INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.\(^1\) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.\(^2\)

Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger. Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

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\(^1\) MIL-HANDBOOK — 2178, SECTION 2.2.


Cho-Therm is a registered trademark of Chromerics, Inc.

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Kapton is a registered trademark of E.I. Dupont

Rubber-Duc is a trademark of AAWID Engineering

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Figure 1 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4" hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

---

Figure 1. Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)
In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:
1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:
- Stud Mount
- Flange Mount
- Pressfit
- Plastic Body Mount
- Tab Mount
- Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

**MOUNTING SURFACE PREPARATION**

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

**Surface Flatness**

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e., Δh/TIR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

**Surface Finish**

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64 μ-in caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound. (3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

**Mounting Holes**

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

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(3) Catalog #87-4S-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.
When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

**Surface Treatment**

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint’s high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

**INTERFACE DECISIONS**

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

**Thermal Compounds (Grease)**

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

**Conductive Pads**

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 3. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes
Table 1
Approximate Values for Interface Thermal Resistance Data from Measurements Performed in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

<table>
<thead>
<tr>
<th>Package Type and Data</th>
<th>Interface Thermal Resistance (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>JEDEC Outlines</strong></td>
<td><strong>Test Torque In-Lb</strong></td>
</tr>
<tr>
<td>DO-203AA, TO-210AA</td>
<td>10-32 Stud 7/16&quot; Hex</td>
</tr>
<tr>
<td>TO-208AB</td>
<td>1/4-28 Stud 11/16&quot; Hex</td>
</tr>
<tr>
<td>DO-208AA</td>
<td>Pressfit, 1/2&quot;</td>
</tr>
<tr>
<td>TO-204AA (TO-3)</td>
<td>Diamond Flange</td>
</tr>
<tr>
<td>TO-213AA (TO-66)</td>
<td>Diamond Flange</td>
</tr>
<tr>
<td>TO-126</td>
<td>Thermopad 1/4&quot; x 3/8&quot;</td>
</tr>
<tr>
<td>TO-220AB</td>
<td>Thermowatt</td>
</tr>
</tbody>
</table>

NOTES: 1. See Figures 3 and 4 for additional data on TO-3 and TO-220 packages.
2. Screw not insulated. See Figure 12.

formed to the surface roughness of both the heatsink and semiconductor. Manufacturer’s data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

**INSULATION CONSIDERATIONS**

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

**Insulator Thermal Resistance**

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraded, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease. Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By
Figure 3. Interface Thermal Resistance for TO-204, TO-3 and TO-220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

comparing Figures 3c and 3d, it can be noted that Thermo­sil, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO-220 package.

A number of manufacturers offer silicone rubber insu­lators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product</th>
<th>$R_{ECS} @ 3$ Mils*</th>
<th>$R_{ECS} @ 7.5$ Mils*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wakefield</td>
<td>Delta Pad 173-7</td>
<td>.790</td>
<td>1.175</td>
</tr>
<tr>
<td>Bergquist</td>
<td>Sil Pad K-4</td>
<td>.752</td>
<td>1.470</td>
</tr>
<tr>
<td>Stockwell Rubber</td>
<td>1867</td>
<td>.742</td>
<td>1.015</td>
</tr>
<tr>
<td>Bergquist</td>
<td>Sil Pad 400-9</td>
<td>.735</td>
<td>1.205</td>
</tr>
<tr>
<td>Thermalloy</td>
<td>Thermalsil II</td>
<td>.680</td>
<td>1.045</td>
</tr>
<tr>
<td>Shin-Etsu</td>
<td>TC-30AG</td>
<td>.664</td>
<td>1.260</td>
</tr>
<tr>
<td>Bergquist</td>
<td>Sil Pad 400-7</td>
<td>.633</td>
<td>1.060</td>
</tr>
<tr>
<td>Chomerics</td>
<td>1674</td>
<td>.592</td>
<td>1.190</td>
</tr>
<tr>
<td>Wakefield</td>
<td>Delta Pad 174-9</td>
<td>.574</td>
<td>.755</td>
</tr>
<tr>
<td>Bergquist</td>
<td>Sil Pad 1000</td>
<td>.529</td>
<td>935</td>
</tr>
<tr>
<td>Ablestik</td>
<td>Thermal Wafers</td>
<td>.500</td>
<td>.990</td>
</tr>
<tr>
<td>Thermalloy</td>
<td>Thermalsil III</td>
<td>.440</td>
<td>1.035</td>
</tr>
<tr>
<td>Chomerics</td>
<td>1671</td>
<td>.367</td>
<td>.655</td>
</tr>
</tbody>
</table>

*Test Fixture Deviation from flat from Thermalloy EIR86-1010.
Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from Aavid shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 4. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

**Insulation Resistance**

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

**Insulated Electrode Packages**

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950’s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, shown on Figure 8, Case 806 (IcePAK) and Case 388 (TO-258AA) (see Figure 11) are examples of parts in this category. The second category contains parts which have a plastic over-mold covering the metal mounting base. The Full Pak,

![Figure 4. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators](image)

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from 0.9°C/W to 0.7°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With non-conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

<table>
<thead>
<tr>
<th>Material</th>
<th>Measured Thermal Resistance (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Thermalloy Data(1)</td>
</tr>
<tr>
<td>Bare Joint, greased</td>
<td>0.033</td>
</tr>
<tr>
<td>BeO, greased</td>
<td>0.082</td>
</tr>
<tr>
<td>Cho-Therm, 1617</td>
<td>0.233</td>
</tr>
<tr>
<td>Q Pad (non-insulated)</td>
<td>—</td>
</tr>
<tr>
<td>Si-Pad, K-10</td>
<td>0.263</td>
</tr>
<tr>
<td>Thermasil III</td>
<td>0.267</td>
</tr>
<tr>
<td>Mica, greased</td>
<td>0.329</td>
</tr>
<tr>
<td>Si-Pad 1000</td>
<td>0.400</td>
</tr>
<tr>
<td>Cho-therm 1674</td>
<td>0.433</td>
</tr>
<tr>
<td>Thermasil II</td>
<td>0.500</td>
</tr>
<tr>
<td>Si-Pad 400</td>
<td>0.533</td>
</tr>
<tr>
<td>Si-Pad K-4</td>
<td>0.583</td>
</tr>
</tbody>
</table>

(1) From Thermalloy EIR 87-1030
(2) From Berquist Data Sheet
Case 221C, illustrated in Figure 13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw. (4)

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping-process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed-nut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt-
furnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

**Adhesives**

Adhesives are available which have coefficients of expansion compatible with copper and aluminum. Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-serviceable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

**Plastic Hardware**

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

**FASTENING TECHNIQUES**

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

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To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws, the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

**Stud Mount**

Parts which fall into the stud-mount classification are shown in Figure 6. Mounting errors with non-insulated stud-mounted parts are generally confined to application

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(5) Robert Batson, Elliot Fraunglass and James P. Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83 Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.
of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 7.

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non-insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a beryllium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

R.F. transistors in the stud-mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic — metal interface are discussed in the section entitled “Connecting and Handling Terminals.”

**Press Fit**

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 8. A special fixture meeting the necessary requirements must be used.

**Flange Mount**

A large variety of parts fit into the flange mount category as shown in Figure 9. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 10. Machine screws (preferred) self-tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section, “Fastener and Hardware Characteristics.”

The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No
special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 9b, final torque should be applied first to the center position.

The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in EB107 “Mounting Considerations for Motorola RF Power Modules.” Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368-1 (HOG PAC) will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4-40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid-section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center.
of the flange, deforming it. Deformations of 2–3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

**Tab Mount**

The tab mount class is composed of a wide array of packages as illustrated in Figure 11. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 12. The rectangular washer shown in Figure 12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab. In addition, it separates

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...Preferred Arrangement for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used. Choose from Parts Listed Below.

- 6-32 HEX HEAD SCREW
- FLAT WASHER
- INSULATING BUSHING
- SEMICONDUCTOR (CASE 221, 221A)
- 2) RECTANGULAR INSULATOR
- HEATSINK
- 2) BUSHING
- FLAT WASHER
- 4) CONICAL WASHER
- E37 6-32 HEX NUT

Choose from Parts Listed Below.

- 4-40 PAN OR HEX HEAD SCREW
- FLAT WASHER
- INSULATING BUSHING
- SEMICONDUCTOR (CASE 221, 221A)
- (1) Used with thin chassis and/or large hole.
- (2) Used when isolation is required.
- (3) Required when nylon bushing is used.

Figure 12. Mounting Arrangements for Tab Mount TO-220

the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 15c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806-02) is basically an elongated TO-220 package with isolated chips. The mounting precautions for the TO-220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

**Plastic Body Mount**

The Thermopad and Full Pak plastic power packages shown in Figure 13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The Full Pak (Case 221C-01) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages: machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5.

Figure 14 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The Full Pak, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 15c, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 15b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 15a.

Figure 13. Plastic Body-Mount Packages
14a. Machine Screw Mounting

14b. Eyelet Mounting

14c. Clips

Figure 14. Recommended Mounting Arrangements for TO-225AA (TO-126) Thermopad Packages

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 16, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resis-

15a. Screw-Mounted TO-220

15b. Screw-Mounted Full Pak

15c. Clip-Mounted Full Pak

Figure 15. Mounting Arrangements for the Full Pak as Compared to a Conventional TO-220
The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 17 shows, thermal resistance asymptotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type. The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

![Figure 16. Surface Mount D-PAK Parts](image1)

![Figure 17. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board](image2)

**FREE AIR AND SOCKET MOUNTING**

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO-225AA) (TO-127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 18. The arrangement of part (a) could be used with any plastic package, but the scheme of part (18b) is more practical.

![Figure 18. Methods of Using Small Heatsinks With Plastic Semiconductor Packages](image3)

with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

**CONNECTING AND HANDLING TERMINALS**

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

**Metal Packages**

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

**EMS Modules**

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

**Plastic Packages**

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A lead bend radius greater than 1/16 inch is advisable for TO-225AA (CASE 77) and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be

---

**Figure 19. Mounting Details for SOE Transistors**
exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

**Stripline Packages**

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 19. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 19b shows a cross-section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud — BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

Figure 19c shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

**CLEANING CIRCUIT BOARDS**

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

**THERMAL SYSTEM EVALUATION**

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

\[ T_J = T_C + R_{JJC} \times P_D \]

where

- \( T_J \) = junction temperature (°C)
- \( T_C \) = case temperature (°C)
- \( R_{JJC} \) = thermal resistance junction-to-case as specified on the data sheet (°C/W)
- \( P_D \) = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

**Graphical Integration**

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instanta-
neous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

**Substitution**

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

### APPENDIX A

**THERMAL RESISTANCE CONCEPTS**

The basic equation for heat transfer under steady-state conditions is generally written as:

\[ q = hA \Delta T \]

where

- \( q \) = rate of heat transfer or power dissipation (Pd)
- \( h \) = heat transfer coefficient,
- \( A \) = area involved in heat transfer,
- \( \Delta T \) = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, \( R_\theta \), is

\[ R_\theta = \frac{\Delta T}{q} = \frac{1}{hA} \]

The coefficient \( h \) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm’s Law is often made to form models of heat flow. Note that \( T \) could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchhoff’s Law and the following equation results:

\[ T_J = P_D(R_{AJC} + R_{\theta CS} + R_{\theta SA}) + T_A \]

where

- \( T_J \) = junction temperature,
- \( P_D \) = power dissipation
- \( R_{AJC} \) = semiconductor thermal resistance (junction to case),
- \( R_{\theta CS} \) = interface thermal resistance (case to heatsink),
- \( R_{\theta SA} \) = heatsink thermal resistance (heatsink to ambient),
- \( T_A \) = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, \( R_{\theta CS} \), may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize \( R_{\theta CS} \).

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

---

**Figure A1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor**
Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that’s apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is “application oriented.”

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path. As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO-220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semiconductor's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the “case” temperature thermocouple readings become warmer. Thus the choice of reference point for the “case” temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

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**Figure B1. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End**
The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 µ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

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<th>Adhesives</th>
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<th>Al2O3</th>
<th>Anodize</th>
<th>Mica</th>
<th>Plastic</th>
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Other sources for silicone rubber pads: Chomerics, Berquist

 Suppliers Addresses

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443
AHAM-TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151
Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935-4944
Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835-2322
Chomerics, Inc., 16 Flagstone Drive, Hudson, New Hampshire 03051 1-800-633-8800
Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 629-3900
International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481
The Staver Company, Inc., 41-51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000
Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321
Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748
Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900
When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non-related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re-registered to the new system as time permitted.

For example the venerable TO-3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO-204 family. The TO-204AA conforms to the original outline for the TO-3 having 40 mil pins while the TO-204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the 00-4, 00-5 and TO-3 still convey sufficient meaning for general verbal communication.
Mounting Procedures for Very High Power RF Transistors

Prepared by
Helge O. Granberg
RF Engineering
Advanced Products Group

RF power semiconductors such as MRF153, MRF154, MRF155, MRF156 and MRF430 are housed in Case 368-01, whereas MRF141G, MRF151G, MRF175G and MRF176G use Case 375-01 (both shown below). All of these are high power devices (200-600 W), which results in an abnormally large amount of heat dissipated within a small physical area. For such high power transistors, special attention must be paid to the heat sink material as well as the finish and flatness of the mounting surface. The material should have at least a thermal conductivity equal to or better than copper and for the mounting surface flatness ± 0.0005" can be considered sufficient. The heat sink can be made of material with lower thermal conductivity such as aluminum, but in that case a copper heat spreader should be used. The heat spreader should have a minimum thickness of 0.25" for case 375-01 and 0.375" for 368-01 and should extend at least 0.5" to 1.0" beyond the flange edges, depending on the device type and the amount of dissipation involved. For die temperature calculations of devices in case 368-01, the Δ temperature between the mounting screw areas and the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions and dissipations of 150 W and 300 W respectively.

Although the data sheets contain information on the subject above as well as the mounting procedures of these devices, very few designers actually follow them. The maximum recommended torque on the #4 size mounting screws is 4-5 in.-lbs. along with split lock- and flat-washers, of which the latter should be in immediate contact with the flange’s top surface. Experiments have shown that merely compressing the split lock washer to its full flatness produces enough torque for sufficient pressure against the heat sink. The split lock washers are available with various spring tensions. Bell type compression washers would be an even better choice if found with 5 in.-lbs. or lower torque specifications.

Calculations indicate that the length of the case 368-01 copper flange increases in excess of two thousands of an inch with a temperature change of 75°C. In such case, if the mounting screws are torqued too tight, the flange cannot expand in length but will bend upwards in the mid section, cracking the Beryllium Oxide insulators as well as the dice. It must also be noted that the thickness of the flange increases with temperature. For the excursion mentioned above, the amount is around 0.25 mils, which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. However the amount of increase is difficult to measure and depends on the exact type of mounting hardware used. The copper-tungsten flange of case 375-01 has a much lower expansion coefficient than copper, but if mounted on a copper or aluminum heat sink, it can be similarly bent during a cooling cycle as the heat sink material contracts.

Deformation can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied along with sufficient screw torque. The thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it in a similar manner. Depending on the amount of thermal compound and its type, deflections of 2–3 mils have been measured between the flange center and corners created by such conditions. The same can happen with all flange mounted RF devices, but with thicker Beryllium Oxide insulators and lower dissipation levels the problem is less severe.

The maximum operating junction temperature and the total dissipation are usually given in the data sheets. It should be able for the device to be operated within these limits if the case temperature can be kept at 25°C or the derating factor is taken into account. The 150°C storage temperature indicated implies that the device can be operated at that case temperature, which is true but at a much derated dissipation rating. However good engineering practices would limit the case temperature to 70–80°C and the die temperature to not higher than twice that.
The MC1378 — A Monolithic Composite Video Synchronizer

Prepared by Geoffrey Perkins

INTRODUCTION

The MC1378 was designed to enable an interface to be made between remote composite color video sources and a locally controlled RGB source of video. It contains the necessary synchronizing circuits, plus a complete color encoder.

The NTSC/PAL color encoding circuitry is very similar to the MC1377 and a detailed discussion of this subject can be found in AN932. The major differences between the MC1378 and MC1377 color encoding sections are that in the MC1378 the burst flag and color subcarrier quadrature accuracy are determined digitally and are not externally adjustable, and the MC1378 is designed to operate from a 5 V supply.

The MC1378 contains all the necessary circuitry to lock a computer to a remote color composite video source and to switch between the remote and the locally generated signals to create overlays in composite video. By using an additional device, the TDA3301/3, simultaneous overlays in RGB can be created. Because the MC1378, when operated in the remotely locked mode, passes the remote signal directly to its output without decoding and re-encoding, no loss in picture quality is experienced as can happen in less sophisticated systems.

SYSTEM DESCRIPTION: LOCAL MODE

(SEE FIGURE 1 AND BLOCK DIAGRAM)

Because the MC1378 operates in two basic modes, local and remote, it is logical to describe them separately.

No external video is required in the local mode and the main function of the MC1378 is to encode the 1 V RGB signals into NTSC or PAL and to drive the graphics system’s clock using the 4X subcarrier crystal oscillator as a reference.

A double balanced phase detector, PD5, is used to compare the now free running 4X subcarrier oscillator divided by four with the returning subcarrier signal at pin 8 and control the clock oscillator. The clock is divided down by the appropriate number within the graphics system to subcarrier frequency. This forms a PLL using the crystal oscillator at pins 10 and 11 as a reference. A separate clock could be used if it is not a multiple of subcarrier frequency — the disadvantage being that the encoded video signal’s subcarrier will not be related to the horizontal frequency, and unpleasant dot crawl or beating on the display may result.

PD1 is a digital phase detector that compares the horizontal TTL sync fed into pin 40 with the MC1378’s internal horizontal sync and controls the 4 MHz VCO to form a PLL. The 4 MHz VCO signal is internally divided by 256 to horizontal frequency. The eight stage divider is also used to develop the burst gate and burst flag signals by decoding the countdown. Burst gate is used extensively within the device for gating and clamping chroma and video signals. Burst gate is 4 μs wide and is centered about the 2.2 μs burst flag signal. Burst gate is also fed out of pin 5 to drive other devices that should be locked to horizontal frequency; e.g. TDA3301/3. Phase detectors PD2, 3 & 4 are not actively used in the LOCAL MODE but PD4 sets an arbitrary oscillator phase to the two electronic phase shifters.

In the PAL mode the R-Y modulator is phase inverted line by line and a burst flag is sent to both R-Y and B-Y modulators. The PAL flip-flop runs at an arbitrary phase in the local mode when the ident circuit is disabled by an external diode connected to pin 29. If a particular PAL phase is required, the PAL flip-flop can be reset at this pin.

The overlay enable (pin 25) should be set low in the LOCAL MODE to view the NTSC or PAL encoded RGB signals at pin 27.

REMOTE MODE

In the remote mode all phase detectors are active except PD5. An external valid video signal or remote signal must be fed into pin 24 to provide all the timing information to the host computer. Composite sync is separated from the remote signal and then fed to the vertical sync separator to detect vertical sync. The separated composite sync is used to lock the 4 MHz VCO using PD1, the vertical sync being fed out to the graphics system to lock its sync generator. The 4 MHz is divided by 256 to horizontal frequency and this is compared in PD2 with the TTL negative going H sync signal at pin 40. The output of PD2 is used to lock the system clock VCO, the frequency of which can range from 14 to 36 MHz depending upon the host computer’s requirement. The system clock is divided down to Horizontal sync frequency within the host system and fed into pin 40.

The color burst from the remote signal is used to lock the 4X color subcarrier oscillator using PD3 which is
**XTAL Specifications**

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<th>Frequency</th>
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<td>Mode</td>
<td>Fundamental</td>
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<tr>
<td>Frequency Tolerance at 25°C</td>
<td>40 PPM Max</td>
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<td>Frequency Temperature Tolerance</td>
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<td>δf₀</td>
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<td>Equivalent Series Resistance</td>
<td>50 Ω Max</td>
</tr>
<tr>
<td>C₁</td>
<td>15 mF</td>
</tr>
</tbody>
</table>

For noisy remote video signals (color lock takes longer), use these values for either NTSC or PAL.

Gated with burst gate. By using PD4 and comparing the burst of the locally generated composite video from the encoder section with the same subcarrier reference used to lock PD3, the subcarrier phases of both the local and the remote signals are made essentially equal. Similarly, the two burst amplitudes are compared in the ACC detector and made equal using a variable gain ACC amplifier in the locally generated chroma path.

The absolute burst amplitude of the remote signal only is detected by the kill detector, the chroma of the locally generated signal being turned off when the remote burst falls below a predetermined level. The kill level can be adjusted by changing the value of the resistor at pin 31. 470 kΩ kills at about 10–20 mVp-p remote burst (normal = 300 mVp-p).
In the PAL mode the phase of the ident of the remote burst is compared with the half line signal from the PAL flip-flop. If an error is detected, indicating that the local ident is not compatible with the remote ident, the flip-flop is reset using the ident processor. If a continuous ident error is detected, i.e. fixed or no burst on remote signal, the chroma in the local signal is killed.

Because the black levels, burst phases, burst amplitudes, and in the case of PAL, ident states are compatible between local and remote signals, the fast video switch operated by the overlay enable signal fed into pin 25 can be used to switch from one signal to the other to create overlays in composite video. Even portions of the timing waveforms (sync, burst, etc.) can be selected from either the local or remote sources for specific purposes, such as noise reduction due to weak signal remote, or VCR tape jitter reduction.

**PHASE DETECTOR OPERATION SUMMARY**

(SEE BLOCK DIAGRAM)

**LOCAL MODE**
- PD1 — compares the internal horizontal frequency derived from the 4 MHz VCO with the Horizontal sync derived from the master clock from the host computer. The PLL formed locks the internal horizontal signal to the host computer’s signal.
- PD2 — not used in LOCAL MODE.
- PD3 — not used in LOCAL MODE.
- PD4 — active, but providing an arbitrary phase-shift setting between the subcarrier reference and the output chroma phase of the locally generated composite video.
- PD5 — locks the master clock VCO (divided down to subcarrier frequency within the host computer) to the four times subcarrier crystal oscillator. The crystal oscillator becomes the system timing standard in the LOCAL MODE.

**REMOTE MODE**
- PD1 — compares and locks the internally counted down 4 MHz VCO to the incoming remote horizontal sync. It is fast acting to follow VCR source fluctuations, etc.
- PD2 — locks the master clock oscillator by comparing the internal horizontal signal with the H sync returning from the host computer.
- PD3 — a gated phase detector, which locks the crystal oscillator frequency divided by four to the incoming remote signal burst.
- PD4 — controls an internal phase shifter to assure that the outgoing local color burst has the same phase as the incoming remote burst at PD3.
- PD5 — not used in REMOTE MODE.

**TYPICAL MASTER CLOCK FREQUENCY CONFIGURATIONS**

Many applications require a Master Clock frequency different from the one shown in the standard schematic. The figure to the right shows the circuit and component values for typical clock frequencies. It is recommended that silver mica capacitors be used for accuracy and temperature stability except for the 0.001 µF coupling caps which can be standard ceramics.

**PICTURE IN PICTURE**

Another test fixture that can be used with the RGB color bar generator (see schematic, Appendix D, in AN932) to insert video into color bars or vice-versa is the “picture in picture” circuit shown in Figure 3. Six one-shot monostables create variable delays and blanking pulses to drive the overlay input on the MC1378. T1, T2, T3, and T4 are variable delays such that the inserted picture window’s size, position and aspect ratio may be adjusted.

**TEST FIXTURES TO SIMULATE A COMPUTER**

Sometimes major problems can be avoided if, before connecting the MC1378 to a computer system, the MC1378 application is tried using a test fixture. The major problems can be solved using the fixture leaving smaller details to be fixed in the total system. Two types of test fixture are shown in Figures 4 and 5. Both use a 36 MHz Master Clock, one for 525/60 Hz NTSC and the other for 625/50 Hz PAL. Other clock frequencies can be accommodated by changing the divide ratios.
The Master Clock output from the MC1378 can be delivered using a short length (<12") of 50 Ω coax. The clock is amplified using one section of the MC74LS04 hex buffer-inverter connected with shunt feedback, followed by another stage to drive the first dividers. The first dividers bring the frequency down to 3.58 MHz or 4.43 MHz accordingly, to drive PD5 in the LOCAL MODE. This TTL output is reduced and rounded off using an RC network. Additional dividers are used to reach horizontal sync frequency. A one-shot MC74LS221 produces the 5 µs wide negative going horizontal sync signal to feed the MC1378 at pin 40. Other variations are possible and the two schematics are shown only as a guide.

**MC1378 SET-UP PROCEDURE USING TEST FIXTURE**

1. Switch to LOCAL MODE (pin 1 = 0 V). Ground pin 25.
2. Using a source of accurate subcarrier frequency, as an oscilloscope trigger, adjust the variable capacitor at pin 10 so that the burst appearing at pin 20 is the correct frequency to within 10 Hz.
   - NTSC = 3.579545 MHz
   - PAL = 4.4333619 MHz
3. Disconnect the signal feeding into pin 8 (3.58/4.43 MHz). Measure this frequency and adjust the Clock Oscillator until the meter reads 3.58 MHz (NTSC) or 4.43 MHz (PAL) ±10 kHz. Reconnect the signal to pin 8. This signal should now be phase-locked to the burst frequency at pin 20.
4. If a coil is used in the 4 MHz oscillator, adjust it to give the correct horizontal frequency at pin 5 (use pin 40 as a scope trigger). When the oscillator has phase locked, adjust the coil to give the correct waveform at pin 2.
   - Pin 2 waveform
   - ![Waveform Image](image)
5. Switch to "REMOTE" MODE (pin 1 = +5 V).
6. Adjust the 100 k potentiometer at pin 9 to give the correct subcarrier frequency to within 50 Hz at pin 20 as in #2.
7. Feed 1 V p-p composite color video into pin 24. Color burst and composite sync should now appear at pin 27. The color burst will be absent if the 100 k pot was incorrectly adjusted.

**MC1378 APPLICATION UPDATE: CLOCK OSCILLATOR ALIGNMENT**

Two new circuits are shown in Figure 6 to improve the pull-in range and speed of the Clock Oscillator phase-locked loop. Figure 6b shows a circuit that has no compromise between the characteristics in both the local and remote modes. Both circuits allow a much wider tolerance on the alignment of the Clock Oscillator.
Figure 4. Test Fixture, NTSC 525/60 Hz

Figure 5. Test Fixture, PAL 625/50 Hz
RGBI TTL TO RGB, 1 V ANALOG CONVERSION

Figure 7 shows a circuit to interface a TTL RGBI output personal computer to the RGB analog inputs of the MC1378. If the circuit is used with the values shown, no coupling capacitors are required to the RGB inputs of the MC1378. The +5 volt supply to the 390 Ω resistors should be very clean to prevent interference on the encoded signal. IC4 is used to simulate 'brown' to be compatible with TTL display monitors.

USING THE MC1378 IN CONJUNCTION WITH THE TDA3301/3 FOR OVERLAYS IN BOTH RGB AND COMPOSITE VIDEO

In some video applications both RGB overlay and composite video overlay are required. In these situations the MC1378 can be used as a time base locked to the remote source, not only for the graphics computer, but also for the color decoder.

The burst gate output of the MC1378 appearing at pin 5 can be used to drive the sandcastle pulse input of the TDA3301/3 at pin 27. Because the output level of the MC1378 is too low to drive the TDA3301/3 directly, a small noninverting buffer is used, as shown in Figure 8, to enable the burst gate pulse to exceed the required slice level at the TDA3301/3. A vertical pulse for the TDA3301/3 clamping system can be obtained at pin 38 of the MC1378 operating in the REMOTE MODE only when a valid video signal is applied. The vertical output must be inverted as shown in Figure 9. If a continuous vertical pulse is required so that the output clamps of the TDA3301/3 are always operating, a locked 50/60 Hz oscillator will have to be used. This could consist of a MC1455 type timer circuit. If a vertical pulse is produced by the microcomputer graphics source, it should be used instead. When in LOCAL MODE, an alternative source of vertical sync must be found to drive the TDA3301/3.

The overlay fast video switches in the MC1378 and TDA3301/3 operate in the opposite sense to each other. Therefore an inverter must be used between pin 25 of the MC1378 and pin 23 of the TDA3301/3.

The delay produced by the use of a delay line in the luminance path of the MC1378 must be compensated by using a similar delay in the overlay enable line as shown in Figure 10. The RGB inputs are essentially compatible between the MC1378 and the TDA3301/3, and can be connected as shown in Figure 11.
A 3.58 MHz chroma trap for the luminance input is shown in Figure 12. For more general information, see the TDA3301/3 data sheet.

A circuit for blanking, filtering and driving a 75 Ω load with 1 Vp-p is shown in Figure 13. The 5 V composite blanking could be developed by using part of the circuit shown in Figure 4.

Figure 14 shows a method for balancing the 3.58 MHz or 4.43 MHz demodulator leakage appearing at the RGB outputs. Normally this is not necessary, but for more exacting applications it may be required.

**MC1378 SUBCARRIER NOTCH FILTER**

Cross color can cause annoying rainbow effects on fast luminance edges especially in noninterlaced pictures. Figure 15 shows a simple subcarrier notch filter in the luminance delay path of the MC1378 to remove some of the offending cross color artifacts at the expense of luminance bandwidth. The cross color problem can be especially bad when attempting to record on consumer type VCRs because on playback the chroma-horizontal interleaving becomes random. The notch method is equally effective on PAL or NTSC.

**IMPROVED REMOTE VIDEO INPUT ISOLATION CIRCUIT**

Because of certain limitations in the device and its packaging, the cross talk from remote composite video input to composite video output can be troublesome when operating in the LOCAL MODE with a video signal present at the composite video input. Typically, the cross talk is about -35 dB at 4.43 MHz and better at 3.58 MHz. Low frequencies are better than -60 dB. The circuit shown in Figure 16 will improve the isolation in the LOCAL MODE by an additional -20 dB.
MC1378 NTSC LUMINANCE COMB FILTER

To avoid loss of luminance bandwidth while removing color artifacts, a simple comb filter can be used in NTSC (see Figure 17). For 625 line PAL, a more complex arrangement has to be made which would be beyond the scope of this application note. The NTSC comb filter is only effective on interlaced color and horizontal signals. Noninterlaced signals could become worse with this arrangement. However, it may be possible to short the delay line input, pins 1 and 2, on noninterlaced signals.

The amplitude and phase adjustments are made when a small amount (550 mVp-p) of 3.58 MHz subcarrier is added at the output of the 400 ns delay line. The two adjustments are trimmed for minimum subcarrier at pin 22. By using this technique, virtually all the cross color artifacts are removed without loss of luminance bandwidth.

Figure 17. MC1378 NTSC Luminance Comb Filter
(For Interlaced Video Only)

NTSC DECODER COMB FILTER FOR THE TDA3301/3

Figure 18 shows a circuit similar to Figure 17 to improve the luminance bandwidth by removing the 3.58 MHz notch in the luminance channel of the TDA3301/3. Again, this filter, as shown, is only applicable to NTSC. Both luminance and chrominance are combed of chroma and luma respectively to remove colored artifacts in interlaced video. The setup is accomplished by adjusting the amplitude and phase for minimum subcarrier at the luminance output.

Figure 18. NTSC Decoder Comb Filter for the TDA3301/3
CARRIER BALANCE OF COLOR MODULATORS

Certain applications require perfect carrier balance of the color modulators. This is simply realized in Figure 19. The two 100 k potentiometers should be adjusted with a black signal for minimum subcarrier at the video output.
Figure 21. Printed Circuit Board Components Layout

Figure 22. Photo
MC1378 EXPECTED WAVEFORMS

Pin 1  Local-0 Volts, Remote-5 Volts
2  3 Vdc Approximate (See Application Note)
3  4 MHz, 200–300 mVp-p Sine Wave (Oscilloscope Probe will disturb the Horizontal PLL)
4  Distorted 4 MHz Signal
5  4 V, 4 μs Wide Pulse Locked to Horizontal
6  NTSC-0 V/PAL-Open
7  Ground
8  3.58 MHz/4.43 MHz 300–800 mVp-p Sine or Square Wave from RMI in Local Mode — Shows Beat Between Remote Signal and Local Subcarrier, but otherwise unimportant
9  14.32/17.73 MHz, 150–300 mVp-p Sinewave (Scope Probe will disturb PLL)
10  Distorted 14.32/17.73 MHz Signal
11/12  3.5 Vdc Approximate
13/14/15/16 1 Vp-p RGB Color Signals, Low for Black, High for Color. All Blanking at Black Level both for Horizontal and Vertical. These are Analog Inputs, so any Noise on RGB will appear at the Output.
17  Inverted Luma Signal 1 Vp-p for 100% Color Bars (1.8 V White/2.8 V Black)
18  Chroma Output 3.58/4.43 MHz with Harmonics, Burst 100 mVp-p, Chroma 300 mVp-p, 100% Color Bars (Approximate Amplitudes)
19  3.4 Vdc Approximate
20  Chroma Input 3.58/4.43 MHz, Burst 100 mVp-p, Chroma 300 mVp-p, 100% Color Bars (Approximate Amplitudes)
21  3.3 Vdc Approximate
22  Inverted Luma 0.5 Vp-p, 100% Color Bars (0.9 White/1.4 V Black)
23  3.5 Vdc Approximate
24  Remote Video Input 1 Vp-p, Negative SYNC
25  Overlay Enable Input; Low — Encoded RGB, High — Remote Signal Threshold = Approximately 1.4 V
26  Ground
27  Composite Video Output
28  VCC + 5 Vdc
29  PAL Identification Pin (Not Used in NTSC)
   In PAL Stepped Waveform at Vertical Rate
   In NTSC DC 0.5 V
30  2.7 Vdc Approximate
31  DC 0.6 V with 100 mV Vertical Ripple When Color Unkilled, 4.2 Vdc Approximate When Color Killed
32/33  36 MHz 200 mVp-p. Difficult to Observe with Conventional Oscilloscope Probe because of Grounding Problems
34  Ground
35  Clock Output 36 MHz, Sinewave 300 mVp-p, Open Circuit Approximate. When used at Lower Frequencies the Output may become Bigger and Clipped. Also same Scope Problem as with 32/33 at 36 MHz
36  VCC + 5 Vdc
37  2.2 Vdc Approximate (See Application Note)
38  Local Composite SYNC Input in LOCAL MODE TTL Negative
   Remote Vertical SYNC Output in REMOTE MODE TTL Negative
39  Composite SYNC TTL Output Negative
40  Horizontal SYNC TTL Input Negative

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APPENDIX
DIRECTORY OF COMPONENT MANUFACTURERS

<table>
<thead>
<tr>
<th>Manufacturer/Division</th>
<th>Contact Information</th>
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<tbody>
<tr>
<td>California Crystal Laboratories</td>
<td>(800) 333-9825 crystals</td>
</tr>
<tr>
<td>Coilcraft</td>
<td>(312) 639-6400 coils</td>
</tr>
<tr>
<td>1102 Silver Lake Road</td>
<td></td>
</tr>
<tr>
<td>Cary, IL 60013</td>
<td></td>
</tr>
<tr>
<td>Comtec</td>
<td>(602) 526-4123 crystals</td>
</tr>
<tr>
<td>Fox Electronics</td>
<td>(813) 693-0099 crystals</td>
</tr>
<tr>
<td>GTE Sylvania Electronic Components Division</td>
<td>(717) 326-6591 crystals, ultrasonic delay lines (for comb filter)</td>
</tr>
<tr>
<td>2401 Reach Road</td>
<td></td>
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<tr>
<td>Williamsport, PA 17701</td>
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<tr>
<td>International Crystals</td>
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<td>muRata-Erie</td>
<td>(404) 436-1300 coils</td>
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<td>2200 Lake Park Drive</td>
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<tr>
<td>Smyrna, GA 30080</td>
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<tr>
<td>Distributor — Time Electronics</td>
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<tr>
<td>Distributor — Sterling Electronics</td>
<td>contact muRata for nearest location</td>
</tr>
<tr>
<td>Phillips/Amperex Optoelectronics Division</td>
<td>(401) 232-0500 ultrasonic delay lines (for comb filter)</td>
</tr>
<tr>
<td>Standard Crystal Corporation</td>
<td>(818) 443-2121 crystals</td>
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<tr>
<td>TDK Corporation of America</td>
<td>(312) 803-6100 400 ns delay lines</td>
</tr>
<tr>
<td>1600 Feehanville Drive</td>
<td></td>
</tr>
<tr>
<td>Mount Prospect, IL 60056</td>
<td></td>
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<tr>
<td>Toko America Inc.</td>
<td>(312) 297-0070 coils, transformers, 400 ns delay lines</td>
</tr>
<tr>
<td>1250 Feehanville Drive</td>
<td></td>
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<tr>
<td>Mount Prospect, IL 60056</td>
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<tr>
<td>Distributor — Digikey</td>
<td>(800) 344-4539</td>
</tr>
<tr>
<td>Distributor — Inductor Supply</td>
<td>(800) 854-1881</td>
</tr>
<tr>
<td></td>
<td>(800) 472-8421 (from within California)</td>
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TRANSMISSION LINE EFFECTS IN PCB APPLICATIONS

A thorough digital design must transcend the "1" and "0" scope of strictly digital considerations and venture into the traditionally analog world of transmission lines. The effects of transmission lines are evident in all interconnections. However, with the advent of devices possessing extremely fast rise and fall times, these effects are more pronounced. The results of these effects, delays or ringing along an interconnection, can cause unpredictable behavior. To minimize these undesirable events, additional care is required during the design of interconnections and termination. Figure 1 illustrates stair-stepping delays and ringing.

The basic guideline used to determine if a printed circuit board (PCB) trace needs to be examined for transmission line effects is that, if the smaller of the driving device's rise or fall time is less than the twice the time required for a switching wave to propagate through a trace, the transmission line effects are not masked during the rise or fall time of the driving device. The factor of twice the propagation time through a trace is not as arbitrary as it might seem; this factor allows for the switching wave to be transmitted from the driving device, travel through the PCB trace to the receiving device, reflect off the receiving device, and return to the driving device. With this guideline established, the rise and fall times and propagation times of a trace become paramount in transmission line analysis.

1. QUAD DESIGN's Transmission Line Calculator (TLC) 1385 Del Norte Rd., Camarillo, California
2. PARASITIC PARAMETERS is a registered trademark of Pacific Numerix Corp., 1200 Prospect St., Suite 300, La Jolla, California.
3. Viewsim System Development (View/SD) is a subset of Workview Series II which are registered trademarks of Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlborough, MA.
4. Green field is a registered trademark of Quantic Laboratories Inc., Suite 200, 281 McDermot Ave., Winnipeg, Canada.
5. Saber is a trademark of Analogy, Inc., 9205 S. W. Gemini Drive, Beaverton, Oregon and CADAT is a trademark of Racal-Redac, Inc., 100 Wychoff Ave., Mahwah, New Jersey.
As devices have been designed to run at higher speeds, their rise and fall times have diminished. Propagation times through a PCB trace depend on the PCB materials and the routing and loading of the trace. Conventional PCB materials have not changed to sustain performance at the faster rise and fall times of driving devices. This situation, as well as the fact that routing and loading can vary greatly from trace to trace, has elevated the importance of investigating PCB traces for transmission line effects.

The lumped capacitive load model shown in many data books is not sufficient for a detailed examination of transmission line effects in PCBs.

Two key elements to consider in transmission line analysis are the PCB traces' characteristic impedance, $Z_0$, and propagation delay, $T_{PD}$. The characteristic impedance is the ratio of the voltage to the current in a circuit; thus it describes what current and voltage parameters the driving and receiving devices connected to a trace will experience. Mismatches in impedance between segments of the trace and devices connected to the trace cause reflections, which result in performance-limiting ringing and delays. The propagation delay is important
because it predicts if the effects of these reflections will be hidden during the rise and fall times of a circuit. To account for these elements, more detailed hand-analysis methods, such as the lattice diagram and the Bergeron plot methods presented in this document, are required. The lattice diagram requires the following information: the rise and fall times of the driving devices, the output impedances of the driving devices, the input impedances of the receiving devices, and the capacitive loading values of the receiving devices. The Bergeron plot method requires the output voltage versus current curves for the driving devices and the input voltage versus current curves and the capacitive loading values of the receiving devices. A complete study also requires information about the PCB, such as the dielectric constant for the insulating materials used, the cross-section trace geometry, and the trace length.

Transmission line effects need to be examined prior to final PCB layout. Not all scenarios can be improved by adding termination. Occasionally, a trace with several segments and loads will have too much delay associated with the reflections and the characteristics of the driving device. In some cases, termination may absorb the reflections, but in other cases, it may overload the driving device, preventing it from operating at its prescribed rate. Hand analysis helps to highlight potential problem areas and can provide general rules used in PCB layout once a system designer gains expertise with an output driver type, but, to account for complex routing patterns, computer programs with transmission line and layout emphasis provide more detailed solutions than hand analysis. More comprehensive solutions using computer programs that provide graphical analysis are available, such as QUAD DESIGN's TLC\textsuperscript{1}, Pacific Numerix's PARASITIC EXTRACTOR\textsuperscript{TM}\textsuperscript{2}, Viewlogic's Viewsim/SD\textsuperscript{TM}\textsuperscript{3}, Quantic Laboratories Greenfield\textsuperscript{®}\textsuperscript{4} and Racal-Redac's Saber/CADAT\textsuperscript{TM}\textsuperscript{5}. The Simulation Program with Integrated Circuit Emphasis (SPICE) also has provisions for transmission line analysis. It is important that the designer knows basic transmission line theory to evaluate these programs' limitations and features.

Motorola understands the importance and complexity of this issue and is developing a solution that includes a tutorial on basic transmission line theory, a set of enhanced input and output electrical characteristics, and the release of models of the M88000 Family output buffers for use in transmission line programs. Solutions, from hand-analysis methods to results of transmission line programs, are useful in predicting transmission line effects, which need to be correlated with the hardware to verify the basic observations from the paper calculations and simulations. This application note serves as the tutorial intended to emphasize the importance of understanding transmission line effects in the application of PCBs. It covers the following subjects: PCB traces as transmission lines, transmission line analysis methods, termination schemes, general notes concerning layout, and examples for loaded traces and
termination. Discussions of termination and examples are presented for exercise only and do not imply behavior of any Motorola devices.

Some techniques promoted in this document have been in practice over 20 years in ECL designs. The premier source for ECL designs is the MECL Design Handbook (see Reference 1). Since the techniques presented there are designed for ECL applications, they do not automatically work for all CMOS and TTL applications. CMOS and TTL outputs are different from ECL outputs in that ECL has similar output impedances for the low-to-high-driven and the high-to-low-driven cases; whereas, CMOS and TTL output impedances often vary by an order of magnitude from their low-to-high-driven and high-to-low-driven cases. Also, many CMOS and TTL outputs drive 5-V swings in less than 2 ns (some actually reach down into the 500-ps range for rise and fall times). ECL outputs drive a 1-V swing in roughly 1 ns. These differences require close examination of the basic, entrenched termination schemes for ECL before they are used with CMOS and TTL.

PCB TRACES

The following paragraphs discuss PCB traces as transmission lines, the four trace types, and device loading.

PCB Traces as Transmission Lines

The key factor in determining if a trace should be treated as a transmission line rather than a lumped load is the relationship between the driving device's rise or fall time and the propagation delay of the signal through the trace. Specifically, the trace should be analyzed as a transmission line if

\[ 2 \times T_{PD} \times \text{trace length} > T_R \text{ or } T_F \text{ (minimum of the two)} \]  

(1)

\( T_{PD} \) is the unit propagation delay of the signal, usually given in nanoseconds per unit length. \( T_R \) and \( T_F \) are the rise and fall times of the driving device. Note that the fastest of the rise and fall time values should be used. The high-level interpretation of Equation (1) is that, if the round-trip time for the switching waveform is greater than the rise or fall time of the driving device, the settling of the transmission line effects are not hidden during the rise and fall times of the driving device.

PCB traces have resistive, inductive, and capacitive effects distributed throughout them. These characteristics are used to develop transmission line models, and the basic means for approximating the distributed effects is a
lumped load model. Figure 2 shows a transmission line modeled in lumped, constant terms, using the intrinsic resistance, inductance, and capacitance of a trace. This representation is reduced to a transmission line circuit that uses the characteristic impedance ($Z_0$) and propagation delay ($T_{PD}$) values to describe the trace. Referring to Figure 2, the effects of the intrinsic resistance ($R_0$) on $Z_0$ are negligible, leaving only the effects of $L_0$ and $C_0$ to be considered in the calculation of the characteristic impedance and propagation delay per unit length:

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \ \Omega$$  \hspace{2cm} (2)

$$T_{PD} = \sqrt{L_0 \times C_0} \text{ ns/length}$$  \hspace{2cm} (3)

NOTE:

$V_{SOURCE}$ = SWITCHING VOLTAGE SUPPLY
$Z_{SOURCE}$ = OUTPUT IMPEDANCE OF VOLTAGE SUPPLY
$R_0$ = INTRINSIC RESISTANCE OF TRANSMISSION LINE
$L_0$ = INTRINSIC INDUCTANCE OF TRANSMISSION LINE
$C_0$ = INTRINSIC CAPACITANCE OF TRANSMISSION LINE
$Z_{LOAD}$ = LOAD IMPEDANCE

Figure 2. Lumped Transmission Line Approximation

If the intrinsic capacitance and inductance are known, they can be used in Equations (2) and (3). Usually, the propagation delay and the characteristic impedance are calculated from cross-section geometries and dielectric materials used in the PCB traces. The equations using the geometries and materials are based on Equations (2) and (3), but then require considerations that treat the traces as if they are operating in the transverse electromagnetic mode. If more information is desired for that derivation, see Reference 1. For this discussion, only multilayer board types (microstrip and stripline) are analyzed. For wire-wrapped applications, consult Reference 1.
PCB Trace Types

The two basic trace types are the microstrip and stripline. Each type can be modified to form derivatives such as the embedded microstrip and the dual stripline configurations. Cross-section diagrams of these trace types are shown in Figure 3.
WHERE:

\[ \begin{align*}
\text{ER} &= \text{DIELECTRIC CONSTANT} \\
H &= \text{DIELECTRIC THICKNESS} \\
T &= \text{TRACE THICKNESS} \\
W &= \text{TRACE WIDTH}
\end{align*} \]

\( Z_0 = \frac{87}{\sqrt{\text{ER}+1.41}} \ln \left\{ \frac{5.98 H}{0.8 W+T} \right\} \)  

\[ T_{po} = 1.017 \sqrt{0.475 \text{ER}+0.67} \]

(a) Surface Microstrip

\[ Z_0 = \frac{K}{\sqrt{0.805 \text{ER}+2}} \ln \left\{ \frac{5.98 H}{0.8 W+T} \right\} \]  

WHERE: \( 60 \leq K \leq 65 \) 

\( \text{ER} \) = DIELECTRIC CONSTANT 

\( H \) = DIELECTRIC THICKNESS BETWEEN TRACE AND POWERGROUND PLANE 

\( B \) = OVERALL DIELECTRIC THICKNESS 

\( T \) = TRACE THICKNESS 

\( W \) = TRACE WIDTH

\[ T_{po} = 1.017 \sqrt{0.475 \text{ER}+0.67} \]

OR:

\[ Z_0 = \frac{87}{\sqrt{\text{ER}+1.41}} \ln \left\{ \frac{5.98 H}{0.8 W+T} \right\} \]

WHERE: 

\( \text{ER} = \text{ER} \left\{ 1 - \text{e} \left( -\frac{1.55 B}{H} \right) \right\} \)

\[ T_{po} = 1.017 \sqrt{0.475 \text{ER}+0.67} \]

(b) Embedded Microstrip

Figure 3. PCB Trace Types (Sheet 1 of 3)
$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \left\{ \frac{4B}{0.67 \pi W (0.8 + \frac{T}{W})} \right\}$

$T_{po} = 1.017 \times \sqrt{\varepsilon_r}$

WHERE:

$\varepsilon_r$ = DIELECTRIC CONSTANT
$H$ = DIELECTRIC THICKNESS BETWEEN TRACE AND POWER/GROUND PLANE
$B$ = OVERALL DIELECTRIC THICKNESS
$T$ = TRACE THICKNESS
$W$ = TRACE WIDTH

VALID FOR $(B - T) < 0.35$ AND $\frac{T}{B} < 0.25$

(c) Stripline

Figure 3. PCB Trace Types (Sheet 2 of 3)
\( Z_0 = \frac{2 Y Z}{Y + Z} \)

WHERE \( Y = \frac{60}{\sqrt{\varepsilon_r}} \ln \left\{ \frac{8A}{0.67 \pi W \left(0.8 + \frac{T}{W}\right)} \right\} \)

WHERE \( Z = \frac{60}{\sqrt{\varepsilon_r}} \ln \left\{ \frac{8(A + D)}{0.67 \pi W \left(0.8 + \frac{T}{W}\right)} \right\} \)

\( T_{PD} = 1.017 \times \sqrt{E_r} \)

WHERE:
- \( E_r = \) DIELECTRIC CONSTANT
- \( H = \) DIELECTRIC THICKNESS BETWEEN TRACE AND POWER/GROUND PLANE
- \( B = \) OVERALL DIELECTRIC THICKNESS
- \( T = \) DIELECTRIC THICKNESS BETWEEN TRACES
- \( W = \) TRACE WIDTH

OR:
\( Z_0 = \frac{80}{\sqrt{\varepsilon_r}} \ln \left\{ \frac{1.9(2A + T)}{0.8W + T} \right\} \)

\( T_{PD} = 1.017 \times \sqrt{E_r} \)

WHERE:
- \( E_r = \) DIELECTRIC CONSTANT
- \( A = \) DIELECTRIC THICKNESS BETWEEN TRACE AND POWER/GROUND PLANE
- \( B = \) DIELECTRIC THICKNESS BETWEEN TRACES
- \( T = \) TRACE THICKNESS
- \( W = \) TRACE WIDTH

LEGEND:
- DIELECTRIC
- TRACE
- GROUND OR POWER PLANE

(d) Dual Stripline

Figure 3. PCB Trace Types (Sheet 3 of 3)
The most frequently used types of dielectrics are glass-epoxy (G-10) and one of its derivatives (FR-4). The dielectric constants (or more specifically in relation to its derivation, relative permittivity) for G-10 can be characterized generally as 4.5 to 5.0, and the dielectric constant for FR-4 can be characterized as 4.5 to 5.2, although PCB manufacturers have seen values as low as 4.0 for both constants. The dielectric constant varies with frequency; Reference 2 provides a discussion on this. Trace dimensions can vary greatly depending on their applications. For multilayer boards with overall board thicknesses of 0.062 in, dielectric thicknesses of layers range from 0.005–0.016 in. Controlled impedance boards, in which all traces on the board have characteristic impedances within a specified range of several ohms, usually have the controlled characteristic impedance in the range of 55–75 ohms due to constraints on manufacturing PCB traces, such as maximum dielectric thicknesses and minimum trace widths.

**Device Loading**

When a trace is loaded with devices, inductance and capacitance from the devices add to the trace's inductance and capacitance. Figure 4 illustrates the loading down the line. This loading alters propagation delay and characteristic impedance values as shown in Equations (4) and (5):

\[
T_{PD}' = T_{PD} \times \sqrt{1 + \left(\frac{C_D}{C_O}\right)} \text{ ns/length} \tag{4}
\]

\[
Z_{O}' = Z_O / \sqrt{1 + \left(\frac{C_D}{C_O}\right)} \Omega \tag{5}
\]

where \( C_D \) is the distributed capacitance of the receiving devices (i.e., total load capacitance/trace length) and \( C_O \) is intrinsic capacitance of the trace. Sockets and vias also add to the distributed capacitance (sockets \( \approx 2 \) pF and vias \( \approx 0.3–0.8 \) pF). Since \( T_{PD} = \sqrt{L_O \times C_O} \) and \( Z_O = \sqrt{L_O / C_O} \), \( C_O \) can be calculated as follows:

\[
C_O = 1000 \times \left(\frac{T_{PD}}{Z_O}\right) \text{ pF/length} \tag{6}
\]

This loaded propagation delay value must be used when deciding whether a trace should be considered a transmission line (2 \( \times T_{PD}' \times \text{trace length} > T_R \) or \( T_F \)).
\[ \Delta V_{\text{OUT}} = \text{VOLTAGE SOURCE, } V_{\text{CM}} \text{ AND } V_{\text{CL}} \]
\[ Z_0 = \text{OUTPUT IMPEDANCE OF DRIVING DEVICE} \]
\[ Z_L = \text{LOAD IMPEDANCE} \]
\[ \Delta V_0 = \text{INCIDENT VOLTAGE} \]
\[ \Delta I_0 = \text{INCIDENT CURRENT} \]
\[ A = \text{DRIVING END OF TRACE} \]
\[ B = \text{RECEIVING END OF TRACE} \]
\[ Z_0' = \text{LOADED CHARACTERISTIC IMPEDANCE} \]
\[ \Delta V_1 = \text{REFLECTED VOLTAGE AT LOAD} \]
\[ \Delta V_2 = \text{REFLECTED VOLTAGE AT DRIVING DEVICE} \]
\[ \Delta I_1 = \text{REFLECTED CURRENT AT LOAD} \]
\[ \Delta I_2 = \text{REFLECTED CURRENT AT DRIVING DEVICE} \]

(a) Transmission Line Representation with \( Z_0' \) and Load Resistance

\[ \Delta V_0 = \Delta V_{\text{OUT}} \]
\[ \Delta I_0 = \Delta I_{\text{OUT}} \]

(b) Voltage Divider and Incident Wave at Driving Device

(c) Incident Wave and Reflected Wave at Receiving Device

(d) Reflected Wave at Source

NOTE: These are simplified, intermediate representations of the transmission line model.

Figure 4. Simplified Transmission Line Representation
The results of these equations are not as straightforward as they seem. $C_D$, the distributed capacitance per length of the trace, depends on the capacitive load of the receiving devices, sockets, and vias. To mask transmission line effects, slower rise and fall times are recommended. A heavily loaded trace slows the rise and fall times of the devices due to the increased RC time constant associated with the increased distributed capacitance and the filtering of high-frequency components out of the switching signal. Heavily loaded traces seem advantageous until the loaded trace condition is examined. A high $C_D$ raises the loaded propagation delay and lowers the loaded characteristic impedance. The higher loaded propagation delay value increases the likelihood that transmission line effects will not be masked during the rise and fall times, and a lower loaded characteristic impedance often exaggerates impedance mismatches between the driving device and the PCB trace. Thus, the apparent benefits of a heavily loaded trace are not realized unless the driving device is designed to drive large capacitive loads.

A higher intrinsic capacitance ($C_O$) reduces the effects of the distributed capacitance ($C_D$). A higher $C_O$ correlates to a higher unloaded propagation delay. The higher $C_O$ counteracts the higher $C_D$ values, but often the unloaded propagation delay is too high for transmission line effects to be avoided. Examples 1 and 2 in **APPENDIX A TRANSMISSION LINE EXAMPLES** illustrate these considerations. Calculations are performed on microstrip and stripline PCB configurations to demonstrate how loading affects each configuration. The microstrip has lower unloaded propagation delay and intrinsic capacitance values than the stripline. These examples show that the microstrip may be faster than the stripline, but it is affected by loading more than the stripline, which is the consequence of having a lower intrinsic capacitance. In each of these configurations, the best way to limit transmission line effects is to keep PCB traces as short as possible, which lowers the round-trip time of the signal, increasing the likelihood that transmission line effects will be masked during the rise and fall times of the signal.

Loading also alters the characteristic impedance of the trace. As with the loaded propagation delay, a high ratio between the distributed capacitance and the intrinsic capacitance exaggerates the effects of loading on the characteristic impedance. Because $Z_O = \sqrt{L_O/C_O}$ and the load adds capacitance, the loading factor ($\sqrt{1 + C_D/C_O}$) divides in $Z_O$, and the characteristic impedance is lowered when the trace is loaded. Reflections on a loaded PCB trace, which cause ringing and stair-stepped switching delays are more extreme when the loaded characteristic impedance differs substantially from the driving device's output impedance and the receiving device's input impedance. A complete discussion of these reflections is presented in **LATTICE DIAGRAM**.
TRANSMISSION LINE ANALYSIS TECHNIQUES

After the loaded characteristic impedance and the loaded propagation delay values of the PCB traces are calculated, the interaction between the devices and the trace can be defined. The two basic occurrences are ringing and stair-stepping delays (see Figure 1). Ringing causes unwanted crossings of logic thresholds, which can be detected by receiving devices with inputs that recognize very fast switching events. In cases with severe ringing, undershoot is produced, which can cripple receiving devices by violating the minimum voltage level allowed at their inputs. Delays caused by stair-stepped voltages limit the overall switching speed of an interconnection. Transmission line analysis methods, from hand-analysis methods to sophisticated computer programs, must be able to predict this behavior.

Lattice diagram and Bergeron plot methods are recommended for hand analysis of transmission line effects. The lattice diagram method requires several calculations to derive reflection coefficients, which are then used to determine the amplitude of reflections at points of unequal impedance throughout a transmission line. This method applies well to computer programs. References 1 and 3 provide a complete derivation of this method. The Bergeron plot is a graphic approach requiring little calculation. It uses the current versus voltage curves of the devices tied to the trace as well as the loaded characteristic impedance of the trace to determine voltages at the driving and receiving devices. References 4, 5, and 6 give basic descriptions of this method. These methods provide information necessary to compile voltage versus time plots, which show the severity and occurrence of transmission line effects.

Lattice Diagram

The following explanation of the lattice diagram method is derived from the finite-length transmission line with a resistive load representation (see Figure 4(a)). The first event in this derivation is that a voltage wave ($\Delta V_{out}$) is sent down the line in the positive-X direction (toward the load). At the output of the driving device, the voltage is split in proportion to the ratio of the output impedance of the driving device and the loaded characteristic impedance ($\frac{V_{o}}{V_{L}} = \frac{Z_{o}}{Z_{L}}$). A new voltage ($\Delta V_{0}$), called the incident voltage, now travels down the transmission line.

Throughout the transmission line portion of this circuit, the voltage-to-current ratio equals the loaded characteristic impedance ($\Delta V_{0}/\Delta I_{0} = Z_{0}'$). At the load, the voltage-to-current ratio equals the load impedance ($V_{L}/I_{L} = Z_{L}$). At the junction of the transmission line and the load, to satisfy Kirchoff's circuit equations, a new reflected voltage wave traveling in the negative-X direction (toward the driving device) is introduced; the voltage-to-current ratio as it travels down the
transmission line equals the loaded characteristic impedance \((\Delta V_1/\Delta I_1 = Z_O')\). The incident voltages and currents add with the reflected voltages and currents to equal the voltage and current at the load \((V_L = \Delta V_1 + \Delta V_0 \text{ and } I_L = \Delta I_1 + \Delta I_0)\). This concept is depicted in Figure 4(c).

The identical situation of accounting for Kirchoff's circuit equations by adding new, reflected voltages and currents occurs at the driving device's output. The voltage and current equations at the driving device's output are derived identically as those at the load, which require that a new voltage and current \((\Delta V_2 \text{ and } \Delta I_2)\) be introduced, using the Kirchoff circuit equations to derive voltage and current at the driving device \((V_D/ID = Z_D, V_D = \Delta V_1 + \Delta V_2, \text{ and } I_D = \Delta I_1 + \Delta I_2)\). Figure 4(d) is a representation of this concept.

The ratio of the reflected voltage to that of the incident voltage at the load is defined as the load reflection coefficient, \(\rho_L\); the ratio of the reflected voltage and its subsequent reflected voltage at the source is defined as the source reflection coefficient, \(\rho_S\). They are described as follows:

\[
\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} \quad \text{(7)}
\]
\[
\rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} \quad \text{(8)}
\]

where \(Z_L\) is the impedance at the receiving device's input, \(Z_D\) is the impedance at the driving device's output, and \(Z_O'\) is the loaded characteristic impedance.

Once computed, the reflection coefficients are used to determine the voltage and current reflected at each discontinuity by multiplying the incoming voltage and current by the reflection coefficients. The voltages and currents traveling into and out of each discontinuity sum to equal the voltages and currents at the discontinuity. If \(Z_L \text{ or } Z_D > Z_O'\), then the reflected wave is positive; if \(Z_L \text{ or } Z_D < Z_O\), then the reflected wave is negative. See Figure 5(a) for this representation of the lattice diagram.

The two basic types of transmission line effects are ringing and stair-stepped switching events. When CMOS and TTL devices are the receiving devices because they have large input impedances \((\rho_L \approx 1)\), indicating that the full incident wave from the driving device is reflected back to the driving device. The ringing or stair-stepping events depend on \(\rho_S\) which is calculated from the driving device's output impedance and the trace's loaded characteristic impedance. Specifically, when \(\rho_L = 0\), ringing is caused when the loaded characteristic impedance is greater than the driving device's output impedance, resulting in a negative source reflection coefficient and a large initial voltage step; stair-
stepping is present when the loaded characteristic impedance is less than the driving device's output impedance, resulting in a positive source reflection coefficient and a small initial voltage step. Some CMOS or TTL devices have grossly different output impedances for the low-to-high-driven and high-to-low-driven states, which produce ringing in high-to-low switching and stair-stepping delays in low-to-high switching. Termination often reduces ringing while increasing the stair-stepping, requiring the designer to choose which effect is worse and to terminate appropriately. Examples 3–5 in APPENDIX A TRANSMISSION LINE EXAMPLES illustrate the effects of loading and termination for transmission line effects.

This derivation of the lattice diagram method illustrates several details concerning transmission line effects. If the load impedance matches the loaded characteristic impedance, there are no reflections after the incident wave arrives at the load, which is the goal of most termination schemes. Also, this derivation uses a single transmission line with discontinuities at the load and driving device only. Often, a loaded trace connected to several devices is approximated in this manner rather than using a separate discontinuity for each device input. This approximate transmission line representation is accurate if the stubs off the main trace are very short (< 1 in) or if the trace is laid out using a daisy-chain format. If the designer is not afraid of a lattice diagram that looks like random molecules bouncing off various surfaces, then the nonapproximate method is straightforward, because the derivation for reflection coefficients at each discontinuity is identical to the derivation of the reflection coefficients at the driving device and receiving device. An example of this multiple discontinuity situation is shown on page 222 of Reference 1. Reference 2 provides an explanation of different layout and loading configurations.

The detailed mathematical representation of the lattice diagram is described as follows:

\[
V(t) = \Delta V_0(t) \times \{ U(t - T_{PD}) + \rho_L \times U[t - T_{PD}(2l - X)] + \\
\rho_L \times \rho_S \times U[t - T_{PD}(2l + X)] + \rho_L^2 \times \rho_S \times U[t - T_{PD}(4l - X)] + \\
\rho_L^2 \times \rho_S^2 \times U[t - T_{PD}(4l + X)] + \ldots \} + V_{INITIAL}
\]

where:

\[
\Delta V_0(t) = \text{voltage at driving device from the voltage divider equation}
\]

\[
\Delta V_0(t) = \Delta V_{OUT} \times [Z_O' / (Z_O' + Z_D)]
\]
where $\Delta V_{\text{OUT}}$ is the voltage output swing of the driving device, $Z_D$ is the output impedance of the driving device, and $Z_0'$ is the loaded characteristic impedance of the PCB trace.

$$T_{PD} = \text{propagation delay of the line}$$
$$U(t) = \text{unit step function}$$
$$l = \text{length of trace}$$
$$X = \text{any point along the trace}$$
$$\rho_L = \text{load reflection coefficient}$$
$$\rho_S = \text{source reflection coefficient}$$
$$V_{\text{INITIAL}} = \text{quiescent voltage throughout the trace prior to switching}$$

The derivation of this representation is found on page 123 of Reference 1. The simplified representation, complete with equations, is given in Figure 5(a), which shows how to compute the voltages at the driving and receiving ends of a transmission line using reflection coefficients. The vertical line on the left represents the starting position ($X = 0$) of the incident wave (driving device); whereas, the vertical line on the right represents the end position ($X = L$) of the incident wave and the point of the first reflected wave (receiving device). The voltages and currents at each endpoint are equal to the voltages and currents flowing into and out of them. The time required to travel the length of the transmission line (PCB trace) is equal to $T_{PD}'$, which are the units of the vertical scale. Units of length are used for the horizontal scale.
NOTE: $\rho_L$ and $\rho_S$ are reflection coefficients and $V_{\text{INITIAL}}$ is the steady-state voltage prior to the switching of the gate. Each TD is a propagation delay ($T_{PD}$) in duration. A and B indicate the driving and receiving ends of the trace, respectively.

(a) Lattice Diagram

Figure 5. Lattice Diagram Representation (Sheet 1 of 2)
The lattice diagram method does make an important assumption in that unless the $Z_D$ and $Z_L$ are specifically given by a data sheet, they have to be calculated over the particular voltage of interest. Not all devices behave linearly over the range of interest. For instance, if a high-to-low transition is to be analyzed, $V_{OL}/I_{OL}$ is used to calculate $Z_D$ for the driving device; for a low-to-high transition, $V_{OH}/I_{OH}$ is used. Frequently, these voltage and current values are given as test conditions or worst-case numbers in a device's specification and do not represent the typical or best-case performance of the device. It is also difficult to find input voltage and current curves, but they are usually approximated by using Schottky diode clamps for CMOS and TTL devices. If the device does not respond linearly and the $V_{OUT}/I_{OUT}$ curves for the driving device and if the $V_{IN}/I_{IN}$ curves for the receiving device are available, then the Bergeron plot method is advised.

The lattice diagram is translated into a voltage versus time plot to show the response at each end of the transmission line (see Figure 5(b)). The time required for each voltage wave to travel through the trace is $T_{PD}$; therefore, each
voltage level is plotted versus $T_{PD'}$ directly from the lattice diagram. In general, the voltage changes at the driving device at time $2n \times T_{PD'}$; the voltage changes at the receiving device at time $(2n + 1) \times T_{PD'}$.

**Bergeron Plot**

The Bergeron plot provides the same basic information as the lattice diagram (voltage and current versus time) but with fewer calculations. It relies on a graphic means of describing the reflections on the trace.

The current versus voltage curves for the devices connected to the trace and the loaded characteristic impedance of the trace itself are required for this method. The axes are the voltage and current ranges for the driving device and receiving device. The curves plotted on the graph are the $V_{OH}/I_{OH}$ and $V_{OL}/I_{OL}$ of the driving device and the $V_{IN}/I_{IN}$ of the receiving device. See Figure 6 for a basic representation.
The starting point for a transition depends on the quiescent values of the circuit, which are determined by the intersections of the output curves of the driving device with the input curves of the receiving device. These points are the voltage and current values to which the circuit settles in a stable high or low state prior to the transition. In tracking either a high-to-low or a low-to-high transition, a line of slope $\pm Z_O'$ is drawn between the curves. The means for calculating $Z_O'$ is presented in Equation (5).

For the low-to-high transition, the first line is drawn starting at the logic low quiescent point (intersection of $V_{OL}/I_{OL}$ and $V_{IN}/I_{IN}$) and has a slope of $+Z_O'$ (see Figure 7). The line ends at the $V_{OH}/I_{OH}$ line, with the intersection indicating the
voltage and current values at the output of the driving device and the input of the transmission line.

The second line drawn has a $-Z_0'$ slope from this second intersection point to the $V_{IN}/I_{IN}$ line. This point indicates the current and voltage at the input of the receiving device and the end of the transmission line after one propagation delay since the signal has traveled one trace length.

The third line is drawn from this point to the $V_{OH}/I_{OH}$ line at a slope of $+Z_0'$. This point is the voltage and current at the driving device after two propagation delays since the signal is reflected back to the driving device from the receiving device.
The fourth line on the plot has a slope of \(-Z_0\)' and ends at the \(V_{IN}/I_{IN}\). This procedure continues until the logic-high quiescent point is reached.

The high-to-low transition is handled similarly. The starting point is at the logic-high quiescent point. The first line has a \(-Z_0\)' slope drawn to the \(V_{OL}/I_{OL}\) line. The second line has a \(+Z_0\)' slope drawn from the intersection to the \(V_{IN}/I_{IN}\) line. In either case, intersection points that lie on a \(V_{OH}/I_{OH}\) or \(V_{OL}/I_{OL}\) line are values at the driving device; those on the \(V_{IN}/I_{IN}\) line are values at the receiving device.

The Bergeron plot results are easily transferred to a voltage versus time plot. The first intersection in the plot gives voltage at time \(T_0\), which is the instant that the driving device switches. The second intersection marks the voltage and current at the receiving device, which occurs at time \(T_1\) \((T_{PD}\) after \(T_0\)). The next change at the driving device occurs at \(2T_{PD}\). In general, the voltage switches at the driving device at time \(2n \times T_{PD}\); whereas, the voltage switches at the receiving device at time \((2n + 1) \times T_{PD}\). The two graphs can be superimposed if desired. See Figure 5(b) from the lattice diagram illustration.

Basic Bergeron plot exercises are shown in Examples 6 and 7 (see APPENDIX A TRANSMISSION LINE EXAMPLES). Examples 8–10 (see APPENDIX A TRANSMISSION LINE EXAMPLES) step through series and parallel termination results for various values.

**TERMINATIONS**

To dissipate the undesired effects of unmatched traces and loads, termination of traces may be utilized. No standard termination works universally due to the complexities of layout geometries, power considerations, component count, and other factors that are discussed in the following paragraphs. In some cases, a combination of these schemes works best. In cases in which a driving device is overloaded, termination adds to the loading of the circuit, further degrading the performance. When the effects of transmission lines rather than overloaded driving devices are dominant, termination may improve performance.

Five of the most frequently used terminations are as follows:

1. Series Termination Resistor
2. Parallel Termination Resistor
3. Thevenin Network
4. RC Network
5. Diode Network
Figure 8 and Table 1 provide a synopsis of these implementations.

**Figure 8. Termination Types**

**SERIES**

**PARALLEL**

**THEVENIN**

**RC NETWORK**

**DIODE**

**NOTES:**
1. A - driving device; B - receiving device.
2. Termination near A should be at the driving device's output, and those near B should be the receiving device's input.


### Table 1. Termination Types and Their Properties

<table>
<thead>
<tr>
<th>Termination Type</th>
<th>Added Parts</th>
<th>Delay Added</th>
<th>Power Required</th>
<th>Parts Values</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series</td>
<td>1</td>
<td>Yes</td>
<td>Low</td>
<td>$R_S = Z_{O'} - R_D$</td>
<td>Good dc Noise Margin</td>
</tr>
<tr>
<td>Parallel</td>
<td>1</td>
<td>Small</td>
<td>High</td>
<td>$R = Z_{O'}$</td>
<td>Power Consumption is a Problem</td>
</tr>
<tr>
<td>Thevenin</td>
<td>2</td>
<td>Small</td>
<td>High</td>
<td>$R = 2 \times Z_{O'}$</td>
<td>High Power for CMOS</td>
</tr>
<tr>
<td>RC Network</td>
<td>2</td>
<td>Small</td>
<td>Medium</td>
<td>$R = Z_{O'}$ $C = 300 \text{ pF}$</td>
<td>Check Bandwidth and Added Capacitance</td>
</tr>
<tr>
<td>Diode</td>
<td>2</td>
<td>Small</td>
<td>Low</td>
<td>—</td>
<td>Limits Undershoot; Some Ringing at Diodes</td>
</tr>
</tbody>
</table>

The series termination resistor is preferred when the load is lumped at the end of the trace, when the driving device's output impedance ($Z_D$) is less than the loaded characteristic impedance of the trace ($Z_{O'}$), or when a minimum number of components is required. It is placed near the driving device, and its value is equal to ($Z_{O'} - Z_D$). When the series resistance and output impedance equal $Z_{O'}$, as prescribed, the voltage wave is split evenly, causing half of the voltage to be transmitted to the receiving device. A receiving device with a very high input impedance sees the full waveform immediately (due to the reflection at its end of the trace), but the driving device does not see the full waveform until $2 \times T_{PD'}$ (see Example 4). Because devices often have different output impedance values for their high and low cases, choosing a series resistance value is not always straightforward.

**Parallel Termination Resistor**

The parallel termination resistor utilizes a single resistor whose value equals $Z_{O'}$ tied to ground, $V_{CC}$, or +3 V. It adds some delay because the RC time-constant effects of the trace are increased when the termination resistance is included. Its major disadvantage is that it dissipates much dc power since its value is small (50–150 ohms). Examples 5 and 8 illustrate these considerations concerning parallel termination.
**Thevenin Network**

The Thevenin network connects one resistor to ground and a second resistor to \( V_{CC} \). To avoid settling of the voltage at a point between the high and low logic levels that causes reduced noise margins, careful consideration of the ratio of resistors is required. This technique works well with TTL families, but care is required when using CMOS devices because the switching voltage is at 50% of the waveform. A balanced level near the threshold causes greater power dissipation and potential crossings of the threshold, resulting in unreliable output states. Because this method serves as a pullup and a pulldown termination scheme, it works well for clock signals.

**RC Network**

The RC network performs well in CMOS and TTL systems. The resistor serves to match the impedance of the trace; the capacitor holds the dc signal component, allowing the ac current to flow to the ground during the switching of logic states. Some delay is presented, but the power dissipation is much less than the parallel scheme. The resistor equals \( Z_0' \), and the capacitor is very small (200–600 pF). Their RC time constant must be greater than twice the loaded line propagation delay. This scheme is highly recommended for buses that have similar layouts for all lines (and similar \( Z_0's) because RC termination networks are available in single-in-line packages (SIPs), which require much less space than a two-discrete-component solution.

**Diode Network**

The diode termination network is used frequently for termination on differential networks. It limits overshoot to approximately 1 V and has low power dissipation, but the diodes' response at the switching frequency needs to be verified. An important observation is that the energy is not absorbed in this method. Overshoot is limited at each receiver that has these diodes at their inputs, but the overall energy is not absorbed as it is in the resistive terminations; thus, reflections occur throughout the trace.

**MISCELLANEOUS FACTORS**

Supply voltage, temperature, processes, crosstalk, and layout are factors affecting PCBs. The following paragraphs describe the factors involved.
Supply Voltage

The supply voltage to the devices affects their rise and fall times. Specifically, a higher supply voltage creates faster rise and fall times because the output transistors are being driven by a higher-than-nominal voltage.

Temperature

Temperature alters the performance of the output devices. A higher temperature adds to CMOS devices' propagation delay times, slowing the rise and fall times.

Process

The best-case and worst-case processes can have a large effect on the devices. Generally, best-case factors speed up the switching, and worst-case factors delay the switching. Since devices with best-case processes have faster rise and fall times, they may cause more transmission line situations than typical devices and become the worst-case devices for system designers.

Crosstalk

To reduce transmission line effects, the most compact layout with short traces is advised. However, traces that run close to each other for several inches are suspect to crosstalk problems. To avoid this problem, increased spacing or shielding between traces must be implemented. Increasing space between traces is difficult in dense layouts, which causes crosstalk to be another complicated issue. References 1, 7, 8, and 9 discuss this subject in detail.

Layout

The following general comments relate to PCB layout and components:

1. Evenly distributed devices along a trace are preferred to lumped loads because there are fewer large discontinuities in impedances.

2. Avoid stubs and T's in layout for critical signals, which cause impedance discontinuities. A daisy-chain method is preferred.

3. Sockets and vias add small amounts of capacitance (less than 2 pF and 0.5 pF, respectively). This amount can be added into calculations for distributed capacitance, if desired.
4. One package type of the future is tape-automated bonding (TAB). The pin orientation and package size require less interconnect area, potentially reducing trace lengths and transmission line effects. Another method used for layout is the multichip module, which mounts several devices together on silicon substrates to reduce interconnect area.

5. Although exotic materials are available, they are not normally used in digital PCB construction. Generally, they have lower dielectric constants, meaning their traces have smaller propagation delays. Reference 10 provides a list of these materials.

6. Controlled-impedance PCBs give a predictable environment for transmission line behavior. They can be expensive, but they are recommended for high-performance or prototype applications.

7. Bidirectional signals often use parallel, RC, or Thevenin terminations at both ends of the PCB trace.

8. Multiwire configurations for PCBs have applications in this high-speed world of digital designs. They have lower dielectric constants, providing faster unloaded propagation delay times.

9. A detailed means of accounting for all types of signal integrity issues is described in Reference 11. It focuses on noise budgets that examine powerdrops and tolerances throughout a system.

TIME-DOMAIN REFLECTOMETER

Reference 1 promotes a means of lab verification using a time-domain reflectometer (TDR), which is basically a step generator that stimulates a PCB trace for an oscilloscope display to monitor. The TDR is recommended for designers who desire to observe transmission lines on a PCB. Because it has a 1-V swing and uses an unpopulated PCB, some expertise is necessary to translate the results to the CMOS and TTL world.

CONCLUSION

PCB layout is not trivial. A poor layout can prevent a well-simulated conventional design from working properly. With devices achieving faster rise and fall times and PCB materials not improving, the transmission line effects must be resolved, usually by using terminations. This solution involves more components and more power consumed by the printed circuit assembly, but it provides improved performance and greater reliability.
The discussions presented in this document are designed to give a background into transmission line effects. To fully understand these effects, predicted results, whether from hand analysis or computer-aided programs, need to be correlated with actual hardware. This complete investigation reduces the unpredictability associated with transmission line effects.

REFERENCES


ADDITIONAL READING


APPENDIX A
TRANSMISSION LINE EXAMPLES

EXAMPLE 1: LOADED MICROSTRIP

An MC68030 with 3-ns rise and fall times drives a unidirectional 4-in surface microstrip trace with six devices (e.g., FAST family) distributed along the trace. Is termination necessary for transmission line effects?

Microstrip Geometry

Given as W = 0.010 in, T = 0.002 in, H = 0.012 in, and $E_R = 4.7$.

Calculate Characteristic Impedance and Propagation Delay:

Using the surface microstrip equations in Figure 3(a):

$$Z_0 = \frac{87}{\sqrt{E_R + 1.41}} \times \ln \left( \frac{5.98 \times H}{0.8 \times W + T} \right) = \frac{87}{\sqrt{4.7 + 1.41}} \times \ln \left( \frac{5.98 \times 12}{0.8 \times 10 + 2} \right) = 69.4 \Omega$$

$$T_{PD} = 1.017 \times \sqrt{0.475 \times E_R + 0.67} = 1.73 \text{ ns/ft} = 0.144 \text{ ns/in.}$$

Consider Loading

$C_D$ is the distributed capacitance per length of the load, which is the total input capacitance of the receiving devices divided by the length of the trace. The loading of each device is given in its specifications. For this case, each $C_L = 7$ pF. Since there are six devices distributed along the 4-in trace, $C_D = 6 \times C_L / \text{Trace Length} = 42 \text{ pF/4 in} = 10.5 \text{ pF/in.}$

$C_O$ is the intrinsic capacitance of the trace. $C_O = T_{PD}/Z_O = 0.0250 \text{ nF/ft} = 25.0 \text{ pF/ft} = 2.08 \text{ pF/in.}$

$T_{PD}' = T_{PD} \times \sqrt{1 + 10.5/2.08} = 4.26 \text{ ns/ft.}$ This is the new one-way propagation time for the signal from the MC68030.
Transmission Line Effects

If $2 \times T_{PD}' \times \text{Trace Length} \leq T_R$ or $T_F$, then the ringing and other transmission line effects are masked during the rise and fall times, and no termination will be needed.

$$2 \times T_{PD}' \times \text{Trace Length} = 2 \times 4.25 \text{ ns/ft} \times 1/3 \text{ ft} = 2.83 \text{ ns}.$$ 

$T_R$ and $T_F = 3 \text{ ns}$; since $2.83 \leq 3$, no termination is required, but this is a marginal case. Note that, if the guideline promoted by some device manufacturers of $3 \times T_{PD}' \times \text{Trace Length}$ is used, then termination would be required.

For comparison, if a 69-$\Omega$ stripline was used instead of a 69-$\Omega$ microstrip, would termination be required?

$$T_{PD} = 1.017 \times \sqrt{\varepsilon_R} = 2.20 \text{ ns/ft}.$$ 

$$C_O = T_{PD}/Z_O = 35 \text{ pF/ft} = 2.91 \text{ pF/in}.$$ 

$C_D$ is same as above ($= 10.5 \text{ pF/in}$).

$$T_{PD}' = T_{PD} \times \sqrt{1 + C_D/C_O} = 4.72 \text{ ns/ft}.$$ 

$$2 \times T_{PD}' \times \text{Trace Length} = 2 \times 4.72 \text{ ns/ft} \times 1/3 \text{ ft} = 3.14 \text{ ns}.$$ 

The rise and fall times are 3 ns. Since $3.14 > 3 \text{ ns}$, termination is needed for the 69-$\Omega$ stripline case.

In comparison, note that $C_O$ is greater for the stripline, which tends to lessen the effect of loading in the $T_{PD}'$ equation. However, the unloaded $T_{PD}$ is substantially greater for the stripline than the microstrip, and this factor prevents the transmission line effects from being masked during the rise and fall times, according to these equations. Notice that the unloaded propagation delay calculations depend only on $\varepsilon_R$, the dielectric constant, and not on the trace geometries.
EXAMPLE 2: LOADED STRIPLINE

An MC88100 with rise and fall times of 2 ns drives four MC88200s distributed over an 8-in stripline trace.

Stripline Geometry

Assume a stripline with \( B = 0.020 \) in, \( W = 0.006 \) in, \( T = 0.0014 \) in, and \( E_r = 4.6 \).

From Figure 3(c), the equations for \( Z_o \) and \( T_{po} \) for a stripline are:

\[
Z_o = \frac{60}{\sqrt{E_r}} \ln \left( \frac{4 \times B}{0.67 \pi W \times (0.8 + T/W)} \right)
\]

\[
= \frac{60}{\sqrt{4.6}} \ln \left( \frac{4 \times 20}{0.67 \pi \times 6 \times (0.8 + 1.4/6)} \right) = 50.7 \ \Omega
\]

\[
T_{po} = 1.017 \times \sqrt{E_r} = 2.18 \ \text{ns/ft} = 0.182 \ \text{ns/in}.
\]

Calculate the intrinsic capacitance of the trace:

\[
C_o = \frac{T_{po}}{Z_o} = 0.043 \ \text{nF/ft} = 43.0 \ \text{pF/ft} = 3.58 \ \text{pF/in}.
\]

Consider Loading

Each MC88200 has a capacitive load of 15 pF. The total load is 60 pF for the four MC88200s. \( C_D \) is the distributed load per length for the trace: \( C_D = 60 \ \text{pF}/8 \ \text{in} = 7.5 \ \text{pF/in}.

\[
T_{po'} = T_{po} \times \sqrt{1 + C_D/C_o} = 2.18 \times \sqrt{1 + 7.50/3.58} = 3.84 \ \text{ns/ft}.
\]

Transmission Line Effects

\( 2 \times T_{po'} \times \text{Trace Length} < T_R \) or \( T_F \) is the condition of interest.

\( 2 \times 3.84 \ \text{ns/ft} \times 2/3 \ \text{ft} = 5.10 \ \text{ns} \). Since this is not less than \( T_R \) or \( T_F \) (2 ns), termination is recommended to absorb transmission lines effects.

Look at a 50.7-\( \Omega \) microstrip line loaded similarly.

\[
T_{pd} = 1.017 \times \sqrt{0.475E_r + 0.67} = 1.72 \ \text{ns/ft}.
\]
\[ C_O = \frac{T_{PD}}{Z_O} = 2.83 \text{ pF/in.} \]

\[ T_{PD}' = T_{PD} \times \sqrt{1 + \frac{C_D}{C_O}} = 3.29 \text{ ns/ft.} \]

Is this a transmission line? \( 2 \times T_{PD}' \times \text{Trace Length} = 2 \times 3.29 \text{ ns/ft} \times 2/3 \text{ ft} = 4.38 \text{ ns.} \) Since this is greater than \( T_R \) or \( T_F \), termination is recommended.

For a trace this long, the rise and fall times are too fast to handle without termination. Trace length does not directly figure into the calculations for \( T_{PD} \) or \( Z_O \), but it is an important factor in the relationship that determines if a trace is a transmission line.
EXAMPLE 3: LATTICE DIAGRAM

Chip A is driving an 8-in 90-Ω stripline trace on a glass-epoxy PCB (Er = 4.7) loaded with four devices (chip B) of 15-pF load capacitance each. Chip A has an output low impedance of 20 Ω and an output high impedance of 120 Ω. Chip B has a very large input impedance (100 kΩ). Examine voltages at each end of the trace by using a lattice diagram.

Calculate $Z_O'$ and $T_{PD}'$

$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_D}{C_O}}}$

$T_{PD} = T_{PD} \times \sqrt{1 + \frac{C_D}{C_O}}$

$C_D = (4 \text{ devices} \times (15 \text{ pF/device})) / 8 \text{ in of trace} = 7.5 \text{ pF/in}.$

To calculate $C_O$, first calculate $T_{PD}$ for a stripline of $E_R = 4.7$ using the equations in Figure 3(c). $T_{PD} = 2.20 \text{ ns/ft}.$

Calculate intrinsic capacitance: $C_O = T_{PD}/Z_O = 2.04 \text{ pF/in}.$

Inserting the $C_O$ and $C_D$ values yields: $Z_O' = 41.6 \Omega$ and $T_{PD}' = 4.76 \text{ ns/ft}.$

The following procedure is outlined in LATTICE DIAGRAM (see Figure 5(a)).

Switching Levels

$V_{OH} = 4.75 \text{ V}, V_{OL} = 0.25 \text{ V}.$

Output High to Output Low

$\Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OL} - V_{OH} = -4.50 \text{ V}.$

Use $Z_D = 20 \Omega$ because the final value is the driven low case.

The voltage divider at the driving end of the trace for $Z_D = 20 \Omega$ and $Z_O' = 41.6 \Omega$ gives: $\Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = -3.04 \text{ V}.$
Calculate Reflection Coefficients

\[ \rho_s = \frac{Z_D - Z_o'}{Z_D + Z_o'} = \frac{20 - 41.6}{20 + 41.6} = -0.351 \]

\[ \rho_L = \frac{Z_L - Z_o'}{Z_L + Z_o'} = \frac{100k - 41.6}{100k + 41.6} = 1 (=0.999) \]

The voltages and currents down the trace are modified proportionally with the reflection coefficients. \( V_{\text{INITIAL}} = V_{\text{OH}} = 4.75 \, \text{V} \).

\[ V_0 = \Delta V_0 + V_{\text{INITIAL}} = 1.71 \, \text{V}. \]

\[ V_1 = \Delta V_0 \times (1 + \rho_L) + V_{\text{INITIAL}} = -1.33 \, \text{V}. \]

\[ V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = -0.261 \, \text{V}. \]

\[ V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 0.803 \, \text{V}. \]

\[ V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_L) + V_2 = 0.430 \, \text{V}. \]

\[ V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 0.058 \, \text{V}. \]

\[ V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_L) + V_4 = 0.188 \, \text{V}. \]

\[ V_7 = \Delta V_0 \times \rho_L^3 \times \rho_S^3 \times (1 + \rho_L) + V_5 = 0.319 \, \text{V}. \]

From Figure 5(a), \( V_{\text{FINAL}} \) is calculated:

\[ V_{\text{FINAL}} = \Delta V_{\text{OUT}} \times \frac{Z_L}{Z_L + Z_D} + V_{\text{INITIAL}} = -4.5 \times \frac{100k}{100k + 20} + 4.75 = 0.251 \, \text{V}. \]

Notice that the voltages are settling towards 0.251 V, which is the final value in this transition.

The voltage versus time plots are shown in Figure A-1:
Output Low to Output High

\[ \Delta V_{\text{OUT}} = V_{\text{FINAL}} - V_{\text{INITIAL}} = V_{\text{OH}} - V_{\text{OL}} = 4.50 \text{ V.} \]

For this case, \( Z_D = 120 \Omega \), since the final state is the high-driving state.

The voltage divider at the driving end of the trace for \( Z_D = 120 \Omega \) and \( Z_O' = 41.6 \Omega \) gives:

\[ \Delta V_0 = \Delta V_{\text{OUT}} \times \frac{Z_O'}{Z_O' + Z_D} = 1.16 \text{ V.} \]

Calculate Reflection Coefficients

\[ \rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{120 - 41.6}{120 + 41.6} = 0.485 \]

\[ \rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{100k - 41.6}{100k + 41.6} = 1 (=0.999) \]

The voltages and currents down the trace are modified proportionally with the reflection coefficients. The initial voltage is the logic-low state = 0.25 V.
\[ V_0 = \Delta V_0 + V_{\text{INITIAL}} = 1.41 \text{ V.} \]

\[ V_1 = \Delta V_0 \times (1 + \rho_L) + V_{\text{INITIAL}} = 2.57 \text{ V.} \]

\[ V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 3.13 \text{ V.} \]

\[ V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 3.69 \text{ V.} \]

\[ V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_L) + V_2 = 3.96 \text{ V.} \]

\[ V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 4.23 \text{ V.} \]

\[ V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_L) + V_4 = 4.36 \text{ V.} \]

\[ V_7 = \Delta V_0 \times \rho_L^3 \times \rho_S^3 \times (1 + \rho_L) + V_5 = 4.50 \text{ V.} \]

\[ V_{\text{FINAL}} = \Delta V_{\text{OUT}} \times \frac{Z_L}{Z_L + Z_D} + V_{\text{INITIAL}} = 4.5 \times \frac{100k}{100k + 20} + 0.25 = 4.75 \text{ V.} \]

In this case, the voltage creeps up toward the final value of 4.75 V. The ringing effects are not as severe as the high-to-low case, but the high-voltage value is not reached until several propagation delays have transpired. The stair-stepping occurs because the loaded characteristic impedance is lower than the output impedance of the driving device. In the first case, ringing occurs because the output impedance of the driving device is lower than the loaded characteristic impedance of the trace.

The voltage versus time plots are shown in Figure A-2:
Figure A-2. Example 3 Unterminated Low-to-High Switching Results
EXAMPLE 4: LATTICE DIAGRAM WITH SERIES TERMINATION

The conditions are the same as Example 3. A series termination resistor of 25 Ω is inserted to reduce ringing in the high-to-low switching state. The lattice diagram analysis for both states is performed to show the series termination tradeoffs in this situation.

Series Termination

For series termination, a resistor is placed in series at the driving device's output, altering the output impedance value used in the calculations.

\[ Z_D' = Z_D + R_S \]

where \( R_S \) is the series resistor and \( Z_D' \) is the new output impedance value used in calculations.

Output-High to Output-Low Switching

Choose \( R_S = 25 \, \Omega \). Now \( Z_D' = Z_D + R_S = 25 + 20 = 45 \, \Omega \).

\( Z_O' \) remains the same (41.6 Ω).

Recalculate \( \rho_S \)

\[
\rho_S = \frac{Z_D - Z_D'}{Z_D + Z_O'} = \frac{45 - 41.6}{45 + 41.6} = 0.0393
\]

\[
\rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{100k - 41.6}{100k + 41.6} = 1 (=0.999)
\]

Calculate Voltages

Output voltage levels are \( V_{OH} = 4.75 \, V \), \( V_{OL} = 0.25 \, V \).

For the high-to-low case, \( \Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OL} - V_{OH} = -4.5 \, V \).

The voltage divider at the driving end of the trace yields:

\[ \Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = -2.16 \, V. \]

The voltages and currents down the trace are modified proportionally with the reflection coefficients. Use initial voltage of high case (= 4.75 V).
\[ V_0 = \Delta V_0 + V_{\text{INITIAL}} = 2.59 \text{ V}. \]
\[ V_1 = \Delta V_0 \times (1 + \rho_L) + V_{\text{INITIAL}} = 0.429 \text{ V}. \]
\[ V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 0.344 \text{ V}. \]
\[ V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 0.259 \text{ V}. \]
\[ V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 0.256 \text{ V}. \]
\[ V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 0.252 \text{ V}. \]
\[ V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_S) + V_4 = 0.252 \text{ V}. \]
\[ V_7 = \Delta V_0 \times \rho_L^3 \times \rho_S^3 \times (1 + \rho_L) + V_5 = 0.252 \text{ V}. \]

The termination reduces the ringing as the voltage settles to its final voltage level of 0.252 V. It is important to note that the first waveform (\( V_0 \)) is a half-voltage waveform. This places the output in the region between logic levels in which noise on the trace may cause receiving devices to switch unpredictably, but only for a short time (2 x \( T_{PD} \)). Also, the devices at the receiving end of trace see the full waveform after one propagation delay; whereas, the driving device (and devices near it) see it after two propagation delays.

The voltage versus time plots are shown in Figure A-3:
This is a good fix for the ringing in the high-to-low switching event. To get a complete idea of the impact of the series resistor, the low-to-high event must be examined.

**Output-Low to Output-High Switching**

\[ \Delta V_{\text{OUT}} = V_{\text{FINAL}} - V_{\text{INITIAL}} = V_{\text{OH}} - V_{\text{OL}} = 4.5 \, \text{V}. \]

For this case, \( Z_0' = Z_D + R_S = 120 \, \Omega + 25 \, \Omega = 145 \, \Omega \), since the final state is the high-driving state and \( Z_{\text{OH}} = 120 \, \Omega \).

The voltage divider at the driving end of the trace for \( Z_D' = 145 \, \Omega \) and \( Z_0' = 41.6 \, \Omega \) yields: \( \Delta V_0 = \Delta V_{\text{OUT}} \times \frac{Z_0'}{Z_0' + Z_D'} = 1.00 \, \text{V} \).

**Calculate Reflection Coefficients**

\[ \rho_S = \frac{Z_D - Z_0'}{Z_D + Z_0'} = \frac{145 - 41.6}{145 + 41.6} = 0.554 \]
\[ \rho_L = \frac{Z_L - Z_0'}{Z_L + Z_0'} = \frac{100k - 41.6}{100k + 41.6} = 1 (\approx 0.999) \]
The voltages and currents down the trace are modified proportionally with the reflection coefficients. The initial voltage is the logic-low state = 0.25 V.

\[ V_0 = \Delta V_0 + V_{\text{INITIAL}} = 1.25 \text{ V}. \]

\[ V_1 = \Delta V_0 \times (1 + \rho_L) + V_{\text{INITIAL}} = 2.25 \text{ V}. \]

\[ V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 2.81 \text{ V}. \]

\[ V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 3.37 \text{ V}. \]

\[ V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 3.67 \text{ V}. \]

\[ V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_L) + V_3 = 3.98 \text{ V}. \]

\[ V_6 = \Delta V_0 \times \rho_L^3 \times \rho_S^2 \times (1 + \rho_S) + V_4 = 4.15 \text{ V}. \]

\[ V_{\text{FINAL}} = \Delta V_{\text{OUT}} \times \frac{Z_L'}{Z_L' + Z_D} + V_{\text{INITIAL}} = 4.5 \times \frac{100k}{100k + 145} + 0.25 = 4.74 \text{ V}. \]

The series termination exaggerates the low-to-high stair-stepping from the unterminated state because the output impedance of the driving device is larger than the unterminated state \((Z_D' = 145 \Omega; Z_D = 120 \Omega)\), which is exaggerated when the termination is added. This illustrates one of the sequences involved in terminating lines—one undesirable effect is reduced while another is exaggerated.

The voltage versus time plots are shown in Figure A-4:
Figure A-4. Example 4 Series Terminated Low-to-High Switching Results
EXAMPLE 5: LATTICE DIAGRAM WITH PARALLEL TERMINATION

The trace characteristics are identical to the previous two examples. Now a parallel resistor is placed at the end of the trace to absorb the energy of the switching wave. This implementation also represents the ac switching events that occur when a RC network is not changed when the voltage initially switches.

In the parallel termination scheme, a resistor of value $Z_O'$ is placed at the receiving device's end of the trace. Since $Z_O' = 41.6 \, \Omega$, choose $Z_L' = 40 \, \Omega$.

Output High to Output Low

$Z_D = 20 \, \Omega$ in the low-driving case. $Z_O' = 41.6 \, \Omega$.

Recalculate Reflection Coefficients

\[ \rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{20 - 41.6}{20 + 41.6} = -0.351 \]

\[ \rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{40 - 41.6}{40 + 41.6} = 0.0196 \]

This is the same source reflection coefficient as the unterminated case. The change in reflection coefficients due to the parallel termination is seen in $\rho_L$.

Calculate Voltages

\[ \Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OL} - V_{OH} = -4.5 \, V. \]

The voltage divider at the driving end of the trace gives:

\[ \Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = -4.5 \times \frac{41.6}{41.6 + 20} = -3.04 \, V. \]

Using $V_{INITIAL} = 4.75 \, V$, the voltages are:

\[ V_0 = \Delta V_0 + V_{INITIAL} = 1.71 \, V. \]

\[ V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = 1.65 \, V. \]

\[ V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 1.67 \, V. \]
\[ V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 1.67 \text{ V}. \]

The effect of driving the line low is not achieved because of the relationship between \( Z_D \) and \( Z_L' \). The final value depends on the voltage divider at the load where \( Z_L' \) is the value of the parallel impedance of the termination resistor and the load impedance. Since the termination resistor \( (RT = 40 \text{ } \Omega, Z_L = 100 \text{ k}\Omega) \) is much smaller than the load impedance, it is effectively the parallel impedance value. (Recall calculations for parallel resistance from circuit theory: \( Z_{L'} = \frac{R_T \times Z_L}{R_T + Z_L} = 40\Omega \)).

\[ V_{FINAL} = \Delta V_{OUT} \times \frac{Z_{L'}}{Z_{L'} + Z_D} + V_{INITIAL} = -4.5 \times \frac{40}{40 + 20} + 4.75 = 1.75 \text{ V}. \]

Most driving devices can drive to the low-logic state because the output impedance of the driving device changes as additional current is pumped into the circuit. With the nondynamic impedances used in the lattice diagram method, the final output low value is not reached, which is a limitation of this hand-analysis method.

For illustration of the parallel method, choose a larger \( Z_{L'} \) that allows the final output low value to be reached. For this case, choose \( Z_{L'} = 300 \text{ } \Omega \). Check final voltage: \( V_{FINAL} = \Delta V_{OUT} \times \frac{Z_{L'}}{Z_{L'} + Z_D} + V_{INITIAL} = -4.5 \times \frac{300}{300 + 20} + 4.75 = 0.531 \text{ V} \). This is an acceptable final voltage because it is less than the maximum input logic-low level (0.8 V).

**Recalculate Reflection Coefficients**

\[ \rho_S = \frac{Z_D - Z_{O'}}{Z_D + Z_{O'}} = \frac{20 - 41.6}{20 + 41.6} = -0.351 \]
\[ \rho_L = \frac{Z_L - Z_{O'}}{Z_L + Z_{O'}} = \frac{300 - 41.6}{300 + 41.6} = 0.756. \]

The voltage divider at the driving end of the trace yields:

\[ \Delta V_0 = \Delta V_{OUT} \times \frac{Z_{O'}}{Z_{O'} + Z_D} = -3.04 \text{ V}. \]

Using \( V_{INITIAL} = 4.75 \text{ V} \), the voltages at each end are:

\[ V_0 = \Delta V_0 + V_{INITIAL} = 1.71 \text{ V}. \]

375
V₁ = ΔV₀ × (1 + ρ_L) + V_{INITIAL} = -0.588 V.

V₂ = ΔV₀ × ρ_L × (1 + ρ_S) + V₀ = 0.218 V.

V₃ = ΔV₀ × ρ_L × ρ_S × (1 + ρ_L) + V₁ = 0.828 V.

V₄ = ΔV₀ × ρ_L² × ρ_S × (1 + ρ_S) + V₂ = 0.614 V.

V₅ = ΔV₀ × ρ_L² × ρ_S² × (1 + ρ_L) + V₃ = 0.453 V.

V₆ = ΔV₀ × ρ_L³ × ρ_S² × (1 + ρ_S) + V₄ = 0.509 V.

V₇ = ΔV₀ × ρ_L³ × ρ_S³ × (1 + ρ_L) + V₅ = 0.552 V.

The voltage versus time plots are shown in Figure A-5:

![Voltage versus time plots](image)

Figure A-5. Example 5 Parallel Terminated High-to-Low Switching Results

As shown earlier, the final voltage is 0.531. In this case, notice that the first voltage (V₀ = 1.71 V) at the driving device falls in the intermediate zone between logic states because Z₀ and Z₀ are close in value (41.6 and 20.0 Ω's, respectively), similarly to the unterminated case. The ringing is reduced at the
load but still exists. As with the series termination, this reduces the ringing in the high-to-low-switching event. The low-to-high-switching event must be examined, too.

**Output-Low to Output-High Switching**

\[ \Delta V_{OUT} = V_{FINAL} - V_{INITIAL} = V_{OH} - V_{OL} = 4.5 \text{ V}. \]

For this case, \( Z_D = 120 \text{ } \Omega \), since the final state is the high-driving state. The voltage divider at the driving end of the trace for \( Z_D = 120 \text{ } \Omega \) and \( Z_O' = 41.6 \text{ } \Omega \):

\[ \Delta V_0 = \Delta V_{OUT} \times \frac{Z_O'}{Z_O' + Z_D} = 1.16 \text{ V}. \]

**Calculate Reflection Coefficients**

\[ \rho_S = \frac{Z_D - Z_O'}{Z_D + Z_O'} = \frac{120 - 41.6}{120 + 41.6} = 0.485 \]

\[ \rho_L = \frac{Z_L - Z_O'}{Z_L + Z_O'} = \frac{300 - 41.6}{300 + 41.6} = 0.756 \]

The initial voltage is the logic-low state = 0.25 V.

\[ V_0 = \Delta V_0 + V_{INITIAL} = 1.41 \text{ V}. \]

\[ V_1 = \Delta V_0 \times (1 + \rho_L) + V_{INITIAL} = 2.29 \text{ V}. \]

\[ V_2 = \Delta V_0 \times \rho_L \times (1 + \rho_S) + V_0 = 2.71 \text{ V}. \]

\[ V_3 = \Delta V_0 \times \rho_L \times \rho_S \times (1 + \rho_L) + V_1 = 3.04 \text{ V}. \]

\[ V_4 = \Delta V_0 \times \rho_L^2 \times \rho_S \times (1 + \rho_S) + V_2 = 3.19 \text{ V}. \]

\[ V_5 = \Delta V_0 \times \rho_L^2 \times \rho_S^2 \times (1 + \rho_S) + V_3 = 3.31 \text{ V}. \]

\[ V_{FINAL} = \Delta V_{OUT} \times \frac{Z_L'}{Z_L' + Z_D} + V_{INITIAL} = 4.5 \times \frac{300}{300 + 120} + 0.25 = 3.46 \text{ V}. \]

The voltage versus time plots are shown in Figure A-6:
The final voltage predicted (3.46 V) is not the final output high voltage desired (4.75 V), but it is the new quiescent value, assuming the driving device does not supply additional current. Since the output impedance of the driving device is greater than the loaded characteristic impedance, stair-stepping occurs during the switching. Any additional load exaggerates the stair-stepping, which is the case when either parallel or series termination is added.

The major drawback with the parallel method of termination is the current consumed. The dc current for the high state would be:

$$I_{FINAL} = \frac{\Delta V_{OUT}}{Z_L'} \times Z_D + I_{INITIAL} = \frac{4.5}{320} + 14.9 \text{ mA} = 28.9 \text{ mA}$$

This dc current requirement violates the drive capability of many devices.

To solve this dc current drive issue, the RC termination scheme is recommended. In the first switching events of the circuit, the capacitor is not charged thus it acts identically as the parallel resistor tied to ground. After the voltage settles, the capacitor charges to the final voltage level and no dc current flows. The capacitor’s value ranges between 200-600 pF, and the resistor’s value is near $Z_O'$. The RC time constant must be less than twice the loaded propagation delay; otherwise, the RC network adds to the ringing.
For this case, use $Z_L' = 300 \ \Omega$ and $C = 300 \ \text{pF}$. Since the time constant is 90 ns, this scheme should be satisfactory. The voltage and current levels during switching follow those given in the parallel termination resistor calculations for $R_T = 300 \ \Omega$.

For designers who would like to experiment with various trace configurations and termination schemes, a spreadsheet of the formulas provides quick comparisons of the trade-offs involved in transmission line effects. Sample spreadsheets for Examples 1–3 are as follows:

### Calculations of Surface Microstrip PCB Traits (Example 1 Configuration)

<table>
<thead>
<tr>
<th>Property</th>
<th>Example 1</th>
<th>28.214 Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>ER (Dielectric Constant)</td>
<td>4.700</td>
<td>4.700</td>
</tr>
<tr>
<td>H (Dielectric Thickness)</td>
<td>12,000 in/1000</td>
<td>12,000 in/1000</td>
</tr>
<tr>
<td>T (Trace Thickness)</td>
<td>2,000 in/1000</td>
<td>2,000 in/1000</td>
</tr>
<tr>
<td>W (Trace Width)</td>
<td>10,000 in/1000</td>
<td>10,000 in/1000</td>
</tr>
<tr>
<td>$Z_0$ (Characteristic Impedance)</td>
<td>69.363 Ω</td>
<td>69.363 Ω</td>
</tr>
<tr>
<td>$T_{PD}$ (Unit Propagation Delay)</td>
<td>1.733 ns/ft</td>
<td>1.733 ns/ft</td>
</tr>
<tr>
<td>$C_0$ (Intrinsic Capacitance)</td>
<td>2.082 pF/in</td>
<td>2.082 pF/in</td>
</tr>
<tr>
<td>L (Length of Trace)</td>
<td>4,000 in</td>
<td>6,000 in</td>
</tr>
<tr>
<td>n (Number of Devices on Trace)</td>
<td>6,000</td>
<td>4,000</td>
</tr>
<tr>
<td>$C_d$ (Load Capacitance of Each Device)</td>
<td>7,000 pF</td>
<td>7,000 pF</td>
</tr>
<tr>
<td>$C_d$ (Distributed Capacitance)</td>
<td>10,500 pF/in</td>
<td>4,667 pF/in</td>
</tr>
<tr>
<td>$Z_0'$ (Loaded Characteristic Impedance)</td>
<td>28.214 Ω</td>
<td>38.524 Ω</td>
</tr>
<tr>
<td>$T_{PD}'$ (Loaded Propagation Delay)</td>
<td>4.260 ns/ft</td>
<td>3.120 ns/ft</td>
</tr>
<tr>
<td>$T_{TR}$ or $T_{TF}$ (Lesser of Rise and Fall Times)</td>
<td>3.000 ns</td>
<td>3.000 ns</td>
</tr>
<tr>
<td>Round-Trip Time ($2*T_{PD}'$)</td>
<td>2.840 ns</td>
<td>3.120 ns</td>
</tr>
<tr>
<td>Need Termination? ($2*T_{PD}' \leq T_{TR}$ or $T_{TF}$)</td>
<td>0.160 ns</td>
<td>-0.120 ns</td>
</tr>
</tbody>
</table>

If results from previous line < 0, then further investigation is needed.
Calculations of Surface Microstrip PCB Traits (Example 2 Configuration)

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
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<tbody>
<tr>
<td><strong>$E_R$</strong> (Dielectric Constant)</td>
<td>4.600</td>
<td>4.600</td>
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<tr>
<td><strong>B</strong> (Overall Dielectric Thickness)</td>
<td>20.000 in/1000</td>
<td>20.000 in/1000</td>
</tr>
<tr>
<td><strong>T</strong> (Trace Thickness)</td>
<td>1.400 in/1000</td>
<td>1.400 in/1000</td>
</tr>
<tr>
<td><strong>W</strong> (Trace Width)</td>
<td>6.000 in/1000</td>
<td>6.000 in/1000</td>
</tr>
<tr>
<td><strong>$Z_0$</strong> (Characteristic Impedance)</td>
<td>50.725 Ω</td>
<td>50.725 Ω</td>
</tr>
<tr>
<td>$Z_0$ Formula Valid for $W/(B-T)&lt;0.35$ and $T/B&lt;0.25$</td>
<td>0.323</td>
<td>0.323</td>
</tr>
<tr>
<td>0.070</td>
<td>0.070</td>
<td></td>
</tr>
<tr>
<td><strong>$T_{PD}$</strong> (Unit Propagation Delay)</td>
<td>2.181 ns/ft</td>
<td>2.181 ns/ft</td>
</tr>
<tr>
<td><strong>$C_Q$</strong> (Intrinsic Capacitance)</td>
<td>3.583 pF/in</td>
<td>3.583 pF/in</td>
</tr>
<tr>
<td><strong>L</strong> (Length of Trace)</td>
<td>8.000 in</td>
<td>4.000 in</td>
</tr>
<tr>
<td><strong>n</strong> (Number of Devices on Trace)</td>
<td>4.000</td>
<td>2.000</td>
</tr>
<tr>
<td><strong>$C_I$</strong> (Load Capacitance of Each Device)</td>
<td>15.000 pF</td>
<td>15.000 pF</td>
</tr>
<tr>
<td><strong>$C_D$</strong> (Distributed Capacitance)</td>
<td>7.500 pF/in</td>
<td>7.500 pF/in</td>
</tr>
<tr>
<td><strong>$Z_{0}'$</strong> (Loaded Characteristic Impedance)</td>
<td>28.843 Ω</td>
<td>28.843 Ω</td>
</tr>
<tr>
<td><strong>$T_{PD}'$</strong> (Loaded Propagation Delay)</td>
<td>3.836 ns/ft</td>
<td>3.836 ns/ft</td>
</tr>
<tr>
<td><strong>$T_R$ or $T_F$</strong> (Lesser of Rise and Fall Times)</td>
<td>3.000 ns</td>
<td>3.000 ns</td>
</tr>
<tr>
<td>Round-Trip Time ($2*T_{PD}'*I$)</td>
<td>5.115 ns</td>
<td>2.557 ns</td>
</tr>
<tr>
<td>Need Termination? ($2*T_{PD}'*I \leq T_R or T_F$)</td>
<td>-2.115 ns</td>
<td>0.443 ns</td>
</tr>
</tbody>
</table>

*If results from previous line < 0, then further investigation is needed.*
### Lattice Diagram Worksheet  
*(Example 3: High-to-low Case)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z_0$ (Characteristic Impedance)</td>
<td>90.000 Ω</td>
</tr>
<tr>
<td>$T_{PD}$ (Propagation Delay)</td>
<td>2.200 ns/ft</td>
</tr>
<tr>
<td>$C_{i}$ (Intrinsic Capacitance)</td>
<td>2.037 pF/in</td>
</tr>
<tr>
<td>$L$ (Length of Trace)</td>
<td>8.000 in</td>
</tr>
<tr>
<td>$n$ (Number of Devices on Trace)</td>
<td>4.000</td>
</tr>
<tr>
<td>$C_{l}$ (Load Capacitance of Each Device)</td>
<td>15.000 pF</td>
</tr>
<tr>
<td>$C_{D}$ (Distributed Capacitance)</td>
<td>7.500 pF/in</td>
</tr>
<tr>
<td>$Z_0'$ (Loaded Characteristic Impedance)</td>
<td>41.594 Ω</td>
</tr>
<tr>
<td>$T_{PP}'$ (Loaded Propagation Delay)</td>
<td>4.760 ns/ft</td>
</tr>
<tr>
<td>$V_{OH}$ (Output High Voltage)</td>
<td>4.750 V</td>
</tr>
<tr>
<td>$V_{OL}$ (Output Low Voltage)</td>
<td>0.250 V</td>
</tr>
<tr>
<td>$Z_{D}$ (Output Impedance of Driving Device)</td>
<td>20.000 Ω</td>
</tr>
<tr>
<td>$Z_{I}$ (Input Impedance of Driving Device)</td>
<td>100000.000 Ω</td>
</tr>
</tbody>
</table>

- $V_{INITIAL} = V_{OH}$
- $ΔV_{OUT} = V_{OL} - V_{OH}$
- $ΔV_{0} = ΔV_{OUT} * (Z_{D}'/(Z_{D}' + Z_{D}))$
- $V_{FINAL} = ΔV_{OUT} * (Z_{I}'/(Z_{I}' + Z_{D})) + V_{INITIAL}$

| $P_{S} = (Z_{D} - Z_{0})/(Z_{D} + Z_{0})$ | -0.351 |
| $P_{L} = (Z_{I} - Z_{0})/(Z_{I} + Z_{0})$ | 0.999 |

<table>
<thead>
<tr>
<th>Voltages</th>
<th>Source Voltage</th>
<th>Receiver Voltage</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{INITIAL}$</td>
<td>4.750</td>
<td>4.750</td>
<td>$T_{1}$</td>
</tr>
<tr>
<td>$V_{0}$</td>
<td>1.711</td>
<td>4.750</td>
<td>$T_{0}$</td>
</tr>
<tr>
<td>$V_{1}$</td>
<td>1.711</td>
<td>-1.325</td>
<td>$T_{1}$</td>
</tr>
<tr>
<td>$V_{2}$</td>
<td>-0.261</td>
<td>-1.325</td>
<td>$T_{2}$</td>
</tr>
<tr>
<td>$V_{3}$</td>
<td>-0.261</td>
<td>0.803</td>
<td>$T_{3}$</td>
</tr>
<tr>
<td>$V_{4}$</td>
<td>0.430</td>
<td>0.803</td>
<td>$T_{4}$</td>
</tr>
<tr>
<td>$V_{5}$</td>
<td>0.430</td>
<td>0.803</td>
<td>$T_{5}$</td>
</tr>
<tr>
<td>$V_{6}$</td>
<td>0.188</td>
<td>0.058</td>
<td>$T_{6}$</td>
</tr>
<tr>
<td>$V_{7}$</td>
<td>0.188</td>
<td>0.319</td>
<td>$T_{7}$</td>
</tr>
</tbody>
</table>

**Final Voltages**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.251</td>
<td>0.251</td>
</tr>
</tbody>
</table>
### Lattice Diagram Worksheet
(Example 3: Low-to-High Case)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_0 ) (Characteristic Impedance)</td>
<td>90.000 Ω</td>
</tr>
<tr>
<td>( T_{PD} ) (Propagation Delay)</td>
<td>2.200 ns/ft</td>
</tr>
<tr>
<td>( C_0 ) (Intrinsic Capacitance)</td>
<td>2.037 pF/in</td>
</tr>
<tr>
<td>( l ) (Length of Trace)</td>
<td>8.000 in</td>
</tr>
<tr>
<td>( n ) (Number of Devices on Trace)</td>
<td>4.000</td>
</tr>
<tr>
<td>( C_I ) (Load Capacitance of Each Device)</td>
<td>15.000 pF</td>
</tr>
<tr>
<td>( C_D ) (Distributed Capacitance)</td>
<td>7.500 pF/in</td>
</tr>
<tr>
<td>( Z_0' ) (Loaded Characteristic Impedance)</td>
<td>41.594 Ω</td>
</tr>
<tr>
<td>( T_{PD}' ) (Loaded Propagation Delay)</td>
<td>4.760 ns/ft</td>
</tr>
<tr>
<td>( V_{OH} ) (Output High Voltage)</td>
<td>4.750 V</td>
</tr>
<tr>
<td>( V_{OL} ) (Output Low Voltage)</td>
<td>0.250 V</td>
</tr>
<tr>
<td>( Z_D ) (Output Impedance of Driving Device)</td>
<td>120.000 Ω</td>
</tr>
<tr>
<td>( Z_I ) (Input Impedance of Driving Device)</td>
<td>100000.000 Ω</td>
</tr>
</tbody>
</table>

\[
\begin{align*}
V_{INITIAL} & = V_{OH} & 0.250 V \\
\Delta V_{OUT} & = V_{OL} - V_{OH} & 4.500 V \\
\Delta V_0 & = \Delta V_{OUT} \times (Z_0'/(Z_0' + Z_D)) & 1.158 V \\
V_{FINAL} & = \Delta V_{OUT} \times (Z_I/(Z_I + Z_D)) + V_{INITIAL} & 4.745 V \\
\rho_S & = (Z_D - Z_0')/(Z_D + Z_0') & 0.485 \\
\rho_L & = (Z_I - Z_0')/(Z_I + Z_0') & 0.999 \\
\end{align*}
\]

<table>
<thead>
<tr>
<th>Volages</th>
<th>Source Voltage</th>
<th>Receiver Voltage</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{INITIAL} )</td>
<td>0.250</td>
<td>0.250</td>
<td>( T_1 )</td>
</tr>
<tr>
<td>( V_0 )</td>
<td>1.408</td>
<td>0.250</td>
<td>( T_0 )</td>
</tr>
<tr>
<td>( V_1 )</td>
<td>1.408</td>
<td>2.566</td>
<td>( T_1 )</td>
</tr>
<tr>
<td>( V_2 )</td>
<td>3.127</td>
<td>2.566</td>
<td>( T_2 )</td>
</tr>
<tr>
<td>( V_3 )</td>
<td>3.127</td>
<td>3.688</td>
<td>( T_3 )</td>
</tr>
<tr>
<td>( V_4 )</td>
<td>3.960</td>
<td>3.688</td>
<td>( T_4 )</td>
</tr>
<tr>
<td>( V_5 )</td>
<td>3.960</td>
<td>4.232</td>
<td>( T_5 )</td>
</tr>
<tr>
<td>( V_6 )</td>
<td>4.364</td>
<td>4.232</td>
<td>( T_6 )</td>
</tr>
<tr>
<td>( V_7 )</td>
<td>4.364</td>
<td>4.496</td>
<td>( T_7 )</td>
</tr>
</tbody>
</table>

**Final Voltages**: 4.745, 4.745
EXAMPLE 6: BERGERON PLOT

A Motorola FACT device drives two MC88200s over an unterminated 5-in surface microstrip laid out in a daisy-chain configuration with a characteristic impedance of 70 Ω and a dielectric constant of 4.7.

The Bergeron plot method will be used as outlined in Reference 6 (page 2-3). The $V_{IN}$ versus $I_{IN}$ curve for the MC88200s is given in this example. These are hand-drawn approximations, not simulated or measured values (i.e., these are for exercise only).

Calculate $Z_0'$

$$Z_0' = \frac{Z_0}{\sqrt{1 + C_D/C_O}}$$

Find the intrinsic and distributed capacitance values:

$$C_O = \frac{T_{PD}}{Z_0} = 1.017 \times \sqrt{0.475E_R + 0.67} / Z_0 = 1.73 \text{ ns/ft} / 70 \Omega = 2.06 \text{ pF/in.}$$

$$C_D = 2 \times 15 \text{ pF/in} = 6 \text{ pF/in.}$$

$$Z_0' = \frac{70}{\sqrt{1 + 6.00/2.06}} = 35.4 \Omega. \text{ For simplicity, use 35 } \Omega.$$  

This value of 35 Ω is used as a slope throughout the Bergeron plot analysis. To graph it, select voltages and currents whose differences provide an impedance of 35 Ω. For example, to get a 35-Ω slope, choose one voltage and current point at the 0-V and 0-mA point. The second point should be 3.5 V and 100 mA for a positive 35-Ω slope or 3.5 V and -100 mA for a negative 35-Ω slope ($Z_0' = V/I$). Lines drawn parallel to this are used throughout the plot.

Bergeron Plot Method

1. Start at a quiescent point (intersection of $V_{OL}/I_{OL}$ or $V_{OH}/I_{OH}$ and $V_{IN}/I_{IN}$). For the high-to-low transition, start at the high quiescent point; for the low-to-high transition, start at the low quiescent point.

2. Draw line with slope of $+Z_0'$ for a low-to-high transition or $-Z_0'$ for a high-to-low transition. This intersects with a $V_{OL}/I_{OL}$ or $V_{OH}/I_{OH}$ line, indicating the voltage and current seen at the discontinuity between the output driving device and the trace.
3. Draw a line of slope $\pm Z_0'$ whose sign is opposite to that of the first line drawn. This line intersects with the $V_{IN}/I_{IN}$ line, which provides the voltage and current seen at the receiving device's input from the trace.

4. Repeat steps 2 and 3 until the $Z_0'$ lines converge on the new quiescent point.

5. Take the voltage values at the intersections and plot these with respect to time. Intersection points on the $V_{OL}/I_{OL}$ or $V_{OH}/I_{OH}$ curves are voltages at the driving device; whereas, points on the $V_{IN}/I_{IN}$ curves are voltages at the receiving device.

Each voltage step from a $V_{OL}/I_{OL}$ or $V_{OH}/I_{OH}$ line to a $V_{IN}/I_{IN}$ line occurs in time $T_{PD'}$.

**Comments**

In the low-to-high case, the receiving devices experience voltages as high as 6.4 V; in the high-to-low case, they experience voltages as low as -1 V.

The Bergeron method (see Figure A-7) requires much less calculation than the lattice diagram method. It also does not assume a linear value for $Z_0$ of the driving device. One drawback for the Bergeron plot is the availability of V/I curves. If the devices used have these curves available, then this is the preferred method of hand analysis. Also, these V/I curves vary over temperature, process, and supply voltage. To account for these factors in a worst-case manner may not always be straightforward. It is important to note this as a limitation.
Figure A-7. Bergeron Plot
The voltage versus time plots are shown in Figures A-8 and A-9:

Figure A-8. Example 6 Unterminated Low-to-High Switching Results

Figure A-9. Example 6 Unterminated High-to-Low Switching Results
EXAMPLE 7: BERGERON PLOT FOR DEVICES WITH HIGH-DRIVE CAPABILITIES

Determine the transmission line effects when a device designed to drive a heavy load is connected to four devices with a load capacitance of 15 pF each over an 8-in stripline trace that is laid out in daisy-chain configuration.

Trace Characteristics

\[ B = 0.016 \text{ in}, \ W = 0.006 \text{ in}, \ T = 0.0014 \text{ in}, \text{ and } E_R = 4.5. \]

From stripline equations in Figure 3(c), \( Z_0 = 45 \Omega \) and \( T_{PD} = 2.16 \text{ ns/ft} = 0.180 \text{ ns/in} \).

Calculate Effects of Load

\[ C_D = 4 \text{ devices} \times 15 \text{ pF/device/8 in} = 7.5 \text{ pF/in}. \]

\[ C_O = \frac{T_{PD}}{Z_0} = \frac{2.16 \text{ ns/ft}}{45 \Omega} \times \frac{1000 \text{ pF/1 nF} \times 1 \text{ ft/12 in}}{4 \text{ pF/in}} = 4 \text{ pF/in}. \]

\[ Z_0' = \frac{Z_0}{\sqrt{1 + C_D/C_O}} = 26.5 \Omega \approx 25 \Omega. \]

The Bergeron plot for \( Z_0' = 25 \Omega \) is shown in Figure A-10.
Figure A-10. Bergeron Plot for $Z_0' = 25 \, \Omega$
The voltage versus time plots are shown in Figures A-11 and A-12:

(a) Driving Device  
(b) Receiving Device

NOTE: The load matches the drive capability of the driving device fairly well; there is some stairstepping in the low-to-high case but little undershoot in the high-to-low case.

Figure A-11. Unterminated Low-to-High Switching Results
NOTE: The load matches the drive capability of the driving device fairly well; there is some stairstepping in the low-to-high case but little undershoot in the high-to-low case.

Figure A-12. Unterminated High-to-Low Switching Results
EXAMPLE 8: BERGERON PLOT WITH PARALLEL TERMINATION

The device and trace configuration is identical to Example 7. The parallel form of termination is examined to demonstrate how the V/I curves are altered when it is used.

For parallel terminations, the $V_{IN}/I_{IN}$ curve is modified such that its slope matches the value of the termination. Several different values are shown in Figure A-13.

Notice that the clamping effect from the diodes is applied, but the linear region follows the value of the termination.
To terminate the trace used in Example 7, use a 66.7-Ω resistor tied to ground. The $V_{in}/I_{in}$ curve is altered by changing the linear region of the curve to follow the slope of the parallel resistor (66.7 Ω). This can be implemented as the RC, Thevenin, or parallel method.

Although the ringing is reduced, there is not much difference from the unterminated state because this particular driving device handles the heavily loaded trace well.
Figure A-14. Bergeron Plot for $Z_0' = 24 \, \Omega$ with 66.7-$\Omega$ Parallel or RC Termination
EXAMPLE 9: BERGERON PLOT FOR A HEFTY OUTPUT DRIVING DEVICE CONNECTED TO A LIGHTLY LOADED TRACE

The same driving and receiving curves are used as in Examples 7 and 8, but a different characteristic impedance is used to illustrate what happens when a driving device that handles the heavily loaded trace (see Figure A-15) well is loaded lightly. Notice that the undershoot is greater and the ringing is substantial in the high-to-low switching case. There is less stair-stepping than in the case with $Z_0' = 25 \, \Omega$. The characteristic of this output buffer shown in Examples 7–9 is, if the trace is heavily loaded to match the high-to-low drive capabilities, then stair-stepping occurs in the low-to-high drive case; if the trace is lightly loaded to match the low-to-high drive capabilities, then ringing occurs in the high-to-low drive case. The designer must understand which case is worse for the design and account for it accordingly.
To alleviate the ringing from the lightly loaded condition shown previously, terminate using a 100-Ω resistor implemented in parallel or RC fashion. The $V_{IN}/I_{IN}$ curve is modified by using the slope of the parallel termination (100 Ω) for the linear region (see Figure A-16). This absorbs the ringing and overshoot well.

Figure A-15. Bergeron Plot with $Z_0^* = 70$ Ω
Figure A-16. Bergeron Plot with $Z_0' = 70 \, \Omega$ and $100 \, \Omega$ Parallel or RC Termination
EXAMPLE 10: BERGERON PLOT FOR SERIES TERMINATION

For demonstration, use a trace with a loaded characteristic impedance of 50 Ω and devices with voltage versus current curves similar to the devices used in Examples 7, 8, and 9. The driving devices have similar output impedances for the high-to-low and low-to-high cases.

If a series resistor method is chosen for termination, the output curves of the driving device are modified. $Z_D$, the output impedance of the driving device, adds to $R_s$, the series resistor, to give the new output impedance, $Z_D' = 25 \, \Omega$. This is the slope of the output curves for the driving device at both the high and low quiescent points.

An example of a 25-Ω series termination is shown in Figure A-17. The total output impedance is shown in the high and low states as a line with slope of 25. In this case, overshoot and undershoot occur. The stair-stepping is no longer evident, and the ringing is minimal.
Figure A-17. Bergeron Plot for \( Z_0' = 50 \ \Omega \) with 25-\( \Omega \) Series Termination
Speeding Up Horizontal Outputs

There are at least two ways to speed up a horizontal output stage. One is to design the transistor specifically for the application. That has been done with the SCANSWITCH series of horizontal output transistors. Another is to optimize the base drive. A very effective technique is to design the base drive backwards, i.e., start with the output transistor's device physics and work back to the horizontal oscillator. The base drive circuit described here takes this approach, and produces some rather interesting results.

TRANSISTOR SELECTION

In horizontal outputs, it turns out that most of the dissipation occurs as collector-emitter voltage rises during storage time. In other words, there is a tendency for the voltage rise waveform to be soft and rounded as opposed to abrupt and square. The parameter that describes this behavior is called dynamic desaturation. SCANSWITCH transistors are specifically designed to minimize dynamic desaturation, and simultaneously avoid collector current tailing.

Minimizing dynamic-desaturation requires a relatively wide base width. Monitor specific transistors, therefore, have wider bases than is normal for high voltage bipolars, and a somewhat unique set of characteristics. A drive strategy that optimizes the performance of the SCANSWITCH structure is outlined as follows.

DRIVE STRATEGY

Optimum drive strategy is driven by transistor physics. The conditions are:
1. Provide adequate drive just prior to turn-off to minimize dynamic desaturation.
2. Avoid overdrive during any portion of the turn-on time to avoid tailing.
3. Provide reverse base current that is independent of forward base current so that transistor performance can be optimized.
4. Provide for a controlled rate of transition from forward to reverse drive to avoid tailing.
5. Avalanche the base-emitter junction during fall time. This is especially important for wide base SCANSWITCH transistors.

Typical techniques for driving horizontal outputs rely on a pulse transformer to supply forward base current, and a turn-off network that includes a series base inductor to limit the rate of transition from forward to reverse drive. The resulting base current waveform is shown in Figure 1A. If this waveform is compared to the representation of collector current that is shown in dashed lines, it can readily be seen that condition number 2 is violated. As is evident from Figure 1B, heavy overdrive is present at the beginning of the collector current ramp. In addition, condition number 1 is violated since heavy overdrive at the beginning is compensated by underdrive just prior to turn-off.

Figure 1. Typical Base Drive
Heavy overdrive at the beginning of the collector current ramp is particularly significant since, bipolar transistors have a memory effect. In other words, the transistor will remember that it has been previously overdriven, for some period of time. For the 1000 volt to 1500 volt transistors that are used in horizontal outputs, there is a first order memory effect for roughly 5 $\mu$s, a second order effect for approximately 10 $\mu$s, and virtually no memory after 25 $\mu$s. As horizontal scan frequencies go up the memory effect becomes more and more important, since the time from which the worst overdrive occurs until the time that turn-off occurs gets shorter. At 64 kHz the memory effect is a first order design constraint. To comply with this constraint and satisfy condition number 1, it is necessary to ramp the base current, such that forced gain is approximately held constant.

A circuit that produces the required ramp and also meets all of the other conditions is shown schematically in Figure 2. In this circuit, a ramped forward current is produced when high side switch $Q_2$ applies $B^+$ to the primary of $T_1$. While $Q_2$ is conducting, $D_1$ is reverse biased and no current flows in the secondary. Forward base current, therefore, is a ramp that is determined by $B^+$ and the primary inductance of $T_1$. When $Q_2$ is turned off, virtually all of the energy that was stored in $T_1$ is available to produce reverse base current through the secondary winding, forward biased diode $D_1$, and $L_9$. With this arrangement, the amount of reverse base current is determined by the turns ratio and can be optimized for the type of device that is being driven. In addition, at turn-off the secondary of $T_1$ is a true current source, with a compliance voltage high enough to avalanche the output transistor’s base-emitter junction. As is common in horizontal output circuits, $L_9$ controls the rate of transition from forward to reverse drive.

At the front end, high side drive for $T_1$ is produced when an open collector horizontal input switches to ground, thereby turning on $Q_1$. With this arrangement, $Q_1$ is configured as a current source. The values of $R_1$, $R_2$, & $R_3$ are specific to a 24 volt power supply and are designed to generate 20 milliamps at the collector of $Q_1$. When present, this 20 milliamps flows through a forward biased diode in the MPSG1000 to turn on the gate of $Q_2$. Gate voltage is limited by an 11 volt zener in the MPSG1000, which is the reason for current source drive. In the absence of an input current, the MPSG1000 switches $R_3$ to $Q_2$’s source, turning off the high side switch when the horizontal oscillator input goes high. A schematic of the MPSG1000 is included in the appendix.

In addition to meeting all of the conditions that are necessary for a high performance base drive, this approach has two important advantages. First, the configuration of $T_1$ allows $L_9$ to be placed outside the path of forward base current. Therefore, at turn-off it is not necessary to expend energy to reverse current flow in a series base inductor. For a given $L_9$ more negative drive is obtained, and with it faster switching. The second advantage is also an important design constraint. Note that there is no resistor to limit forward base current, and therefore no power loss associated with setting the value of forward base current. The process of generating a ramp stores rather than dissipates energy. If the stored energy is used rather than wasted, forward base drive can be essentially “lossless.” This will happen if the amount of energy stored in $T_1$ to produce the ramp is equal to the amount of energy ($E_B(\text{off})$) that is required to turn off the output transistor. In other words, if $B^+$ and the primary inductance of $T_1$ ($L_p$) are chosen such that $1/2L_pI_B^2 = E_B(\text{off})$, then the forward drive is essentially lossless. $E_B(\text{off})$ is a new specification that is
included in the SCANSWITCH data sheets. It assumes an $R_{BE}$ of 22 ohms and targets a base-emitter avalanche time of 500 ns. If $B^+$ and $L_p$ are not chosen in this way, either enough energy to adequately avalanche the output transistor’s base-emitter junction will not be provided, or excess energy will show up in the output transistor as dissipation due to excess base-emitter avalanche time.

DESIGN EXAMPLE
A few simple steps are all that is required to compute nominal design values. As an example, let’s assume a 64 kHz application with peak collector current of 6 amps and on-time ($t_{on}$) of 6.25 µs. To start, base current is computed from data sheet test conditions for switching time. For the MJH16206 switching times are measured at 6.5 amps with a base drive of 1.5 amps, which implies a forced gain of $6.5/1.5 = 4.33$. Applying the same forced gain to operation at 6 amps gives a base current of 1.4 amps. For this transistor $E_{B(\text{off})}$ is specified at 30 µjoules. Using this value, $L_p$ and $B^+$ are selected to give 1.4 amps of base current in a 6.25 µs on-time and produce $1/2L_pB^+ = E_{B(\text{off})} = 30$ µJ. These values are computed in two steps given by equations 1 & 2.

1. $L_p = 2E_{B(\text{off})}/B^+ = 2 \times 30 \times 10^{-6}/(1.4)^2 = 31$ µH
2. $B^+ = L_pB^+/t_{on} + 1 = 31\times10^{-6}/1.4/6.25\times10^{-6} + 1 = 8$ Volts

In this example the turns ratio for $T_1$ ($n$) is chosen as 13:4 and $L_g$ is specified as 0.5 µH. These values are found on the SCANSWITCH data sheet. When this information is not available, a good place to start for 1000 volt to 1500 volt horizontal output transistors is $E_{B(\text{off})} = 30$ µJ, $n = 12:4$, and $L_g = 1$ µH.

Data sheet values take into account the gain variation that is normally expected in a production environment. When using these values, performance of the distribution, as opposed to performance of individual units is optimized. The average part will look better with less forward base drive (lower $B^+$), and all parts will perform better with a lower value of $L_g$ if $B^+$ has been adjusted for gain. Therefore, at very high frequencies, it is possible to further optimize performance by adjusting $B^+$ to accommodate individual transistor characteristics.

RESULTS
The resulting base drive waveform is shown in Figure 3. It produces the output waveforms that are plotted in Figure 4, and a storage time of only 1 µs. Both crossover losses and storage time are roughly half of what more common base drive techniques produce. Base-emitter voltage is plotted versus time along with collector current in Figure 5. Note that the base-emitter junction is avalanche for somewhat less than 1 µs, which minimizes fall time. In very high frequency monitors, the avalanche time can also be used to provide immunity to $dV/dt$ produced by the flyback pulse.

CONCLUSION
In order to get optimum performance from SCANSWITCH horizontal output transistors, there are 5 conditions which the base drive circuit must meet. When these conditions are all met, it is possible to significantly speed up horizontal outputs.
APPENDIX

Davies' Driver
Simplified Schematic

(2) INPUT

(3) OUTPUT

R2 15K

Q2

Q1

D2 10.4 V

R1 5K

TO-92

(1) RETURN
External-Sync Power Supply with Universal Input Voltage Range for Monitors

By S.K. Tong and K.T. Cheng

ABSTRACT

This paper describes the design of a low-cost 90 W flyback switching power supply for a multi-sync color monitor. In order to minimize the screen interference from the switching noise, the power supply can be automatically synchronize at the fixed frequency of the horizontal scanning frequency (15 to 32 kHz) of the color monitor. The line and load regulations of the power supply are excellent. Also, a new universal input-voltage adaptor enables the power supply to operate at two input voltage ranges, 90–130 Vac or 180–260 Vac. It can minimize the ripple current requirement of the input bulk capacitors and the stresses on the power switch. The design demonstrates how to use recently introduced components in a low-cost power supply. The state-of-the-art perforated emitter epi-collector bipolar power transistor MJE18004 and opto-isolator MOC8102 are utilized.

1. INTRODUCTION

As the resolution of modern color display increases, the power supply for these high-definition monitors become critical in its features and performance. Nowadays, switching power supplies replace the linear regulators due to high efficiency and light weight. However, the EMI/RFI generated by switching power supplies has adverse effects on the resolution of high-definition color monitors (e.g. 800x600 or higher). Asynchronous switching noise beat with the horizontal scanning frequency of the color monitor, creating undesirable interferences and jitter on the screen. It affects the horizontal resolution of the high-definition color monitor because the random pulses generated by the asynchronous switching operation and also deflect the electron beams and blur their precisely controlled positions. Thus, the switching power supply for the high-definition monitors or TVs must be synchronous with the horizontal frequency.

Recently, multi-sync color monitors became popular because they can adapt to several modes of computer displays. For examples, CGA, EGA and VGA display modes are used in IBM PCs. The three display modes have different horizontal resolutions and scanning frequencies, ranging from 15.7 kHz to 31.5 kHz. Hence, the switching power supply developed in this note can be synchronize to the horizontal scanning frequencies of the multi-sync color monitor, as shown in Figure 1. It provides three d.c. outputs. The specifications are:

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![Block Diagram of Modern Multi-Sync Color Monitor](image.png)

Figure 1. Block Diagram of Modern Multi-Sync Color Monitor
Outputs
+110 V 0.7 A for HV, RGB drivers and deflection.
+12 V 0.3 A for auxiliary use.
+5 V 0.2 A for logic ICs.

Inputs
90–130 Vac or 180–260 Vac 50/60 Hz

Power
90 W with overload protection

Conversion Efficiency
Minimum 70% at full load

Others
External synchronization with d.c. isolation (15 kHz to 32 kHz) which are regarded power supply standards for modern color monitors. The two low-voltage outputs are obtained by post-regulators of the +15 V and +8 V inputs.

In Figure 2, the block diagram of the switching power supply, according to the specifications, is shown. Besides the input filter, it mainly consists of three parts — the rectification circuit, the universal input-voltage adaptor and the 90 W flyback converter.

The universal input-voltage adaptor can automatically select the input-voltage range and controls the triac in order to provide the rectified d.c. voltage Vcc in between 200 to 370 V. In 90–130 V range, the triac is continuously fired and the whole rectification circuit forms a voltage doubler. In 180–260 V range, the triac turns off and the rectification circuit works as normal. This design can significantly reduce the current ripples of the two smoothing capacitors, Cm, and the switching stresses on the power transistor(s) due to wide range of Vcc. Some previous designs without the universal adaptor handle the full input-voltage range only by simple bridge rectification. The current ripple of the smoothing capacitors are usually several amperes for 90 W power converters. Furthermore, the output voltage ripple (at Vcc) is generally higher for the same value of smoothing capacitors at low line.

In section 2, the design of the flyback converter is reviewed, whereas the design of the universal input-voltage adaptor is given in section 3. Then, in section 4, the performance and further improvements of the power supply are discussed. In the last section, the conclusions include a summary of the design of the power supply and the future developments of switching power converters suitable for multi-sync monitors.

2. DESIGN OF THE FLYBACK POWER SUPPLY

2.1 TOPOLOGY SELECTION

The single-ended discontinuous-mode flyback topology is selected to perform the major power transfer from the rectified output (Vcc) to the load. Advantages and disadvantages of this topology are:

Advantages
1. It has smaller transformer size and output choke. The power density and cost of the power supply are lowered.
2. Current mode operation is excellent because the current waveform fed to the current mode controller is strictly triangular. It can improve the noise immunity of the current sensing circuit.
3. Single-pole roll-off characteristic of the power converter simplifies the design of feedback circuits. [1]
4. Simplified in design if single-ended configuration is used.
5. Good cross regulation. [1]
6. The working duty cycle can be greater than 50%. This is particularly important for multi-sync monitor power supply.
7. Lower cost than other topologies.

Disadvantages
1. High RMS and peak transformer currents result in high losses in power switch, windings and voltage clamp.
2. The large air gap in the flyback transformer causes higher EMI/RFI and flux fringe.
3. Higher ripple current appearing in output capacitors produces greater output ripple voltage which may cause screen interference. The switching frequency of the power supply is designed in synchronization with the horizontal frequency. The adverse effect due to this point becomes less significant.

Figure 2. Block Diagram of Switched-Mode Power Supply for Multi-Sync Monitor

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4. Transformer and snubber capacitor ring after the magnetic energy stored in the magnetic core is completely released. This phenomenon can be often found in the previous designs. With the considerations of cost effectiveness, size, and cross regulations, flyback topology is selected. It is particularly suitable for 90 W switching power converter application. Disadvantages are minimized through careful design (see later).

Current-mode control is employed in this power supply because:
1. Inherent line ripple rejection ($\delta V_0/\delta V_{CC} = 0$)
2. Eliminate the possible double-pole characteristics in continuous mode. This would cause instability of the power supply under some critical conditions.
3. Discontinuous mode flyback topology has excellent current mode operation due to large current amplitude.
4. Synchronization is easier to implement without greatly affecting the converter performances and circuit configuration.
5. Simple and low cost as commercial current-mode controller IC is available. UC3842A/3843A, Motorola current mode control IC, is used in the power supply to perform the current mode operation. The feedback from secondary side to primary is through MOC8102, a new Motorola opto-isolator.

2.2 DESIGN OF FLYBACK TRANSFORMER

The lowest value of $V_{CC}$ is assumed to be 200 V, i.e. 50 V below the rectified low-line peak voltage ($180 \times 1.414 = 255$ V), and the highest value is about 370 V. Therefore, the flyback converter shown in Figure 3 should operate within 200–370 Vdc. The total power is 90 W, slightly higher than the sum of all three outputs. The switching frequency is from 15 kHz to 32 kHz with external synchronization.

If the efficiency is taken into account and it is assumed that the typical conversion efficiency is about 70%, the total input power $P_{in}$ is,

$$P_{in} = 90/0.7 = 128.6 \text{ W}$$

Then, the following problem is how to determine suitable primary inductance $L_p$ and maximum working duty cycle $D$ of the power transistor. Assuming that the primary inductance and input power are constant,

$$P_{in} = L_p I_{pk}^2 f_s/2 \quad \text{(Energy law)} \quad (1)$$

$$V_{CC} = L_p I_{pk} I_{c} \quad \text{(Faraday's law)} \quad (2)$$

where $I_c$ = conduction time of the switch = $D$T,

$$T = 1/f_s = \text{switching period}.$$  

Hence,

$$P_{in} = (V_{CC} I_{pk} I_{pk} f_s/2 = V_{CC} I_{pk} D/2 \quad (3)$$

If we set $D = 0.4$ at $V_{CC} = 200$ V, $f_s = 15$ kHz and $P_{in} = 128.6$ W, we have, from (3), $I_{pk} = 3.215$ A.

The current waveform is shown in Figure 4. Put $I_{pk}$ into (1) or (2), then the primary inductance is calculated to be,

$$L_p = 1.66 \text{ mH}$$

The duty cycle at $V_{CC} = 370$ V is 0.216 under full-load condition. It becomes smaller as the load decreases. Also from (1), at same power level,

$$I_{pk} \text{ at 32 kHz } = \sqrt{\frac{15}{32}} = 0.6847$$

$$I_{pk} \text{ at 15 kHz } = \frac{1.66}{0.6847} = 2.42 \text{ A}$$

and $D_{max}$ at 32 kHz = 0.4/0.6847 = 0.584

For the flyback converter operating in discontinuous mode at 32 kHz, the duty cycle with respect to secondary side of transformer $D' = t_d/T$ is set to 0.4, which is slightly less than (1–0.584) = 0.416, because the remaining switching time is used to compensate other non-idealities such as leakage inductances, stray capacitances, finite switching fall and rise times, etc. To calculate the secondary inductances, the power relation is used again. If the output power (90 W) was lumped to +110 V output, from (3), at $f_s = 32$ kHz and $V_{CC} = 200$ V,
\[ P_0 = 90 \, W = V_o \, I_{pk} \, D'/2 \]
where \( P_0 \) = net output power
\( V_o \) = output voltage of +110 V
\( I_{pk} \) = peak inductor current of +110 V windings
\( D' = \frac{t_d}{T} = 0.4 \) (referred to Figure 3).
Hence, \( I_{pk} = 4.1 \, A \) and \( t_d = 12.5 \, \mu s \).

Then, substitute \( I_{pk} \) into (1) or (2), we have,
\[ L_s(110) = \text{inductance of +110 V winding} = 0.334 \, mH \]
And, the inductances of other two windings are,
\[ L_s(15) = L_s(110) \left( \frac{16}{111} \right)^2 = 6.9 \, \mu H \]
\[ L_s(8) = L_s(110) \left( \frac{9}{111} \right)^2 = 2.2 \, \mu H \]
The diode drops of the output rectifiers are taken into consideration for the two low-voltage outputs. The turn ratio \( n \) is equal to,
\[ n = \frac{N_p}{N_s(110)} = \frac{L_p/L_s(110)}{1/2} = 2.22 \]  \hspace{1cm} \text{(4)}
where \( N_p \) = number of turns of \( L_p \) (primary inductance)
\( N_s(110) \) = number of turns of \( L_s(110) \).

Two magnetic cores are found to be suitable for the implementation of the flyback transformer. They are EE40 core and ETD39 core. The spacing factors are just around 0.4 for both. The maximum working flux density \( B_{max} \) is set to 0.25T. For EE40 core, the effective cross-sectional area \( A_e \) is 130.65 mm\(^2\).
\[ N_p = \frac{(V_{CC} \times I_p)(B_{max} \times A_e)}{0.25 \times 130.65} = 163 \]
\[ N_s(110) = 163 \times 2.22 = 73 \]
\[ N_s(15) = 11 \]
\[ N_s(8) = 6 \]
where \( N_s(15) \) = number of turns of \( L_s(15) \), and
\( N_s(8) \) = number of turns of \( L_s(8) \).

For ETD39 core, \( A_e \) is 124.15 mm\(^2\). The required wire gauges of each winding are also listed in the following. \( I_{rms} \) value is equal to \( (D/3)^{1/2} \, I_{pk} \). At \( f_s = 15 \, kHz \), \( I_{pk} = 6 \, A \) and \( t_d = 18.2 \, \mu s \), hence,
\[ D' = 18.2 / 66.67 = 0.273 \]
\[ N_p = \frac{(200 \times 0.4 \times 66.67) / (0.25 \times 124.15)}{172} \]
\[ I_{rms} = (0.4/3)^{1/2} \times 3.215 = 1.17 \, A \] (AWG #23)
\[ N_s(110) = 77 \]
\[ I_{rms} = (0.273 / 3)^{1/2} \times 2 \times 0.7 / 0.273 = 1.55 \, A \] (AWG #22)
\[ N_s(15) = 11 \]
\[ I_{rms} = 0.66 \, A \] (AWG #26)
\[ N_s(8) = 7 \]
\[ I_{rms} = 0.44 \, A \] (AWG #26)
\[ N_A = 18 \, \text{for MTP4N90 and } N_A = 13 \, \text{for MJE18004} \]
(see later).

The ETD39 core will be used in the power supply due to its round bobbin shape and efficient AP product [1]. The temperature rise of the transformer core is about 30°C. To obtain an approximate length of air gap \( l_g \), the calculation is based on:
1. the reluctances of the magnetic core are negligible.
2. the air gap are in the middles of the three limbs, all equal to \( l_g \).
3. the relative permeability \( \mu_r \) is constant and equals 2000 for TDK H7C4 material.
Hence, \[
L_p = \frac{\mu_0 N_p^2 A_e}{2l_g} \]
(5)
or \( l_g = 1.4 \, mm \)
But, a 4 mm air gap is used practically to obtain the required inductance due to flux fringe and other non-idealities. The transformer construction diagram is shown in Figure 10. To meet with the world safety regulations (e.g. VDE, UL, CSA, etc.) for the transformer, readers should refer to corresponding regulation books and (4).

![Figure 5a. Current-Mode Controller and Sync Circuit for MTP4N90 (MOSFET)](image-url)
2.3 DESIGN OF OUTPUT CIRCUITS

The following paragraphs describe how to determine the values of output capacitors and to select output rectifiers as shown in Figure 3. The ultrafast recovery rectifier MUR140 is chosen for D_{110} due to its fast recovery time (75 ns), reliability and low cost. The maximum reverse voltage of this diode is \( V_{BR} + 370/n = 277 \) V, so a 400 V device is selected. The average current of D_{110} is 0.7 A maximum. D_{15} and D_{8} are schottky diodes, MBR160 and 1N5819 respectively, because schottky rectifiers are more suitable for low voltage outputs.

During \( t_d \), the output voltage rises from its minimum value to its peak.

\[
V_o = \frac{1}{C_{o(110)}} \int_0^{t_d} \left[ I_{pk(110)} - \frac{I_{pk(110)} t}{t_d} \right] dt + V_o(min)
\]

It consists of a linearly increasing term and a convex parabolic curve. Thus,

\[
V_o(max) = \frac{1}{C_{o(110)}} \int_0^{t_d} \left[ I_{pk(110)} t - \frac{I_{pk(110)} t^2}{2 t_d} \right] dt = V_o(min)
\]

and output ripple voltage is,

\[
\delta V_o = V_o(max) - V_o(min) = \frac{1}{2} \frac{I_{pk(110)} t_d}{C_{o(110)}}
\]

Since the maximum inductor current \( I_{pk(110)} \) at 110 V rail is 5.13 A, and the output ripple voltage is maximum at \( f_s = 15 \) kHz,

\[
t_d = 0.273 \times 66.67 \, \mu s = 18.2 \, \mu s
\]

\[
t_i = T - t_c - t_d = 21.8 \, \mu s
\]

If the output ripple voltage is set to 1% of \( V_o \), i.e. 1 V,

\[
\delta V_o = 1 = 0.5 \times 5.13 \times 18.2/C_{o(110)}
\]

\[
C_{o(110)} = 46.68 \, \mu F
\]

However, the output ripple current (1.55 A) is so large that two or more capacitors are needed to be connected in parallel in order to lower their individual ripple currents and the additional output ripple caused by ESR and ESL of the output capacitors. As a result, two of 22 \( \mu F \) to 33 \( \mu F \) capacitors each with maximum ripple current of 0.8 A are used in the power supply. Their maximum working voltage is 160 Vdc.

The dummy resistors R_{110}, R_{15} and R_{8} are used to maintain minimum load currents of the three outputs. R_{110} is set to 5.6 k\( \Omega \) and dissipates 2 W.

LC filter is cascaded with each output to lower the output ripple voltage. They are shown in Figure 8. The corner frequency for that at +110 V output is about 6.2 kHz and the approximate output ripple voltage is,

\[
\frac{1}{(1 + (15/6.2)^4)^{1/2}} = 0.1684 \, V \text{ (peak-to-peak)}.
\]

2.4 SELECTION OF SWITCHING TRANSISTOR, SNUBBERS AND VOLTAGE CLAMP

Two types of power switches are considered for the flyback power supply. They are TMOS power FETs, and the state-of-the-art perforated emitter bipolar transistors introduced in 1988. The new series of Motorola TMOS FETs simplifies the design of driving circuits and provides extremely fast switching transitions. These MOSFETs can operate in the MHz range. In this power supply, although the switching frequency is relatively low, it still provides several advantages such as simple drive circuit, less supply current for the MOS driver, fast switching times which result in less energy loss at switching transitions, and hence a smaller value of snubber capacitor \( C_1 \) (1000 \( \mu F \)) is required. Since the maximum drain voltage of M1 is near 850 V (see later), and the peak drain current is 3.2 A, MTP4N90 is selected for M1, with 4 \( \Omega \) rds(on) [5]. Thus, the approximate conduction loss in M1 is \([0.4/3]1/2 \times 3.2)^2 \times 4 = 5.5 \, W\) at \( f_s = 15 \) kHz, \( V_{CC} = 200 \, V\) and full load. The power dissipation is well below the maximum power that can be dissipated by the device.

To demonstrate the switching improvement of the newly introduced perforated-emitter BJT family, the design of the flyback power supply also provides an alternative for a new device. MJE18004 is chosen for M1 because its breakdown voltage \( V_{BR(ICEF)} \) is above 1000 V, the continuous collector current is 5 A and its switching times are excellent for switchers below 70 kHz (\( t_{fs} = 70 \) ns and \( t_{cs} = 0.6 \, \mu s \) at \( I_C = 2 \, A, I_{b1} = 250 \, mA \) and \( V_{BE} = -5 \, V \) [6]). Another two important features are its lower cost and power loss than the MOSFET. Its performance is quite different from the previous bipolar transistors. For the triple diffused power transistors, which are still widely used in Japan (e.g. BU508), these devices face three major problems: long switching times, dispersion of device characteristics, and \( h_{fe} \) degradations after several thousand operating hours. The epi-collector technologies which MJE18004 uses, improve the switching speed and control of device characteristics. Since the emitter of BJT affects the device performance very much, various emitter structures have evolved. With
Motorola SWITCHMODE III, with hollow emitter structure, the speed and RBcOA improvements are accompanied by the increased die size (about 125% of standard technology). For the perforated emitter structure, the emitter is interleaved by the base, thus, this increases the emitter perimeter to area ratio. That means higher speed switching transistor can be fabricated in a smaller die size. It improves the operating frequencies and lowers the cost.

In Figure 3, a dissipated RC turn-off snubber is shown. Its function is to reduce the power loss of the transistor $M_1$ at turn-off by limiting the rising slope of $V_{DS}$. It is also called the dV/dt limiter. When $M_1$ turns off, the inductor current begins to commutate from the power switch to the snubber capacitor $C_1$ through the diode $D_1$ within $t_f$. The snubber capacitor slows down the increasing rate of $V_{DS}$, so the $V_{DS}$ $I_f$ product area (during cross-over time) can be limited to certain acceptable value. This snubber is particularly important for the old and slow bipolar transistors. With the advents of TMOS FETs and perforated emitter bipolar power transistors, the snubber capacitance can be chosen to be as low as 1000 pF. As the current fall-time of power transistor given in data sheets includes the effect of transistor output capacitance ($C_{oss}$), it is difficult to calculate an optimum value of $C_1$ which requires the fall-time information without the effect of $C_{oss}$ [2,3].

Theoretically, the charge stored in $C_1$ at turn-off should be completely dissipated in $R_1$ when the switch $M_1$ turns on. However, in the discontinuous-mode flyback power supply, it cannot always have that because severe stray oscillation which is caused by $L_p$ and $C_1$ occurs when the energy stored in the magnetic core is completely discharged to the loads. This phenomenon is often seen in previous designs. Therefore, the resistor $R_1$ has another function that it acts as a damper for the $L_p$-$C_1$ resonant circuit. Then, a compromise between the two opposing operations should be considered. For a series LCR resonant circuit, the damping ratio can be used to control the envelope of the damped sinusoidal oscillation. From any standard text on linear control systems, the damping ratio is given by

$$Damping \; ratio = \frac{R_1}{2 \sqrt{L_p}}$$  \hspace{1cm}(7)

If the damping ratio is set to 1, no undershoot below $V_{CC}$ will result.

Thus,

$$1 = 0.5 \times R_1 \times (1000\mu \text{H}/1.66\mu \text{m})^{1/2} \text{ or } R_1 = 2.58 \text{ k}\Omega$$

In practice, a smaller value of $R_1$ will increase the discharge rate of $C_1$ at turn-on. So, a standard value of 2.4 k$\Omega$ is used. The maximum power dissipation of $R_1$ is equal to $C_1 V_{CC(max)}^2 f_s(max)^2 = 2.2$ W, for complete discharge of $C_1$ during the conduction time of $M_1$. But, due to the stray oscillation caused by $C_1$, $L_p$ and $R_1$, the resistor $R_1$ should have a power dissipation of 3 W.

Another RC snubber of 180 $\Omega$ and 470 pF used in the power supply is to damp the stray oscillation caused by the junction capacitance of $D_{110}$ and the leakage inductance [2].

In Figure 4, a high-voltage spike (point A) in $V_{DS}$ is caused by the discharge of leakage magnetic energy in the transformer. The time between A and B represents this period. Since the discontinuous-mode flyback converter has greater peak inductor current, the effect of leakage inductance can be the dominant source of power loss. As shown in Figure 3, a voltage clamp for the leakage inductance limits the spike voltage to a designated value, $V_{spk}$. In [3], it points out that voltage clamp is more effective than shunt snubber in limiting the spike voltage. It is actually a boost converter with an input voltage of approximately $nV_O$ and the leakage inductance as switching inductor. From power relation, neglecting the minor effect of the shunt RC snubber,

$$L_3 I_{pk}^2 f_s/2 + nV_O t_{spk} f_s I_{pk} = (V_{spk} - V_{CC})^2/R_2$$

for $C_2 R_2 = 1/f_s$

and from Faraday's law,

$$I_{pk} L_3/(V_{spk} - V_{CC} - nV_O) = t_{spk}$$

where $L_3$ = leakage inductance in primary side. On substitution,

$$\frac{1}{2} L_3 I_{pk}^2 f_s \left[ 1 + \frac{nV_O}{V_{spk} - V_{CC} - nV_O} \right] = (V_{spk} - V_{CC})^2 R_2$$  \hspace{1cm}(8)

Note that although the above result is similar to that shown in [3], the leakage inductance which stores energy to be dissipated is merely $L_3$, and the leakage inductances in the secondary side only come into effect between point A and B in Figure 4. The power loss due to $L_3$ is essentially same for all switching frequencies because $I_{pk}^2 f_s$ is constant for same power level and $V_{CC}$. At 15 kHz, the primary inductance was measured to be 0.15 mH with major secondary winding (110 V output) short-circuited at zero bias current. It is about one-tenth of $L_p$. So, $L_3$ is equal to 0.15 mH/2 = 75 $\mu$H. If the peak voltage of $M_1$ is limited to 850 V for MTP4N90, then,

$$0.5 \times 75 \times 3.2^2 \times 15 \times k x [1 + 244/(850-370-244)] = (850 - 370)^2/R_2$$

$$R_2 = 19.67 \text{ k}\Omega \quad (11.7 \text{ W})$$

For MJE18004, $V_{spk}$ is limited to 950 V and $R_2 = 33.8 \text{ k}\Omega \quad (9.95 \text{ W})$. Practical values of 20 k$\Omega$ (10 W) and 33 k$\Omega$ (10 W) are used for MTP4N90 and MJE18004, respectively.

2.5 CONTROL, BASE DRIVE AND EXTERNAL SYNC CIRCUITS

The current-mode control IC selected is the UC3842A or UC3843A. For MOSFET, MTP4N90, UC3842A is used to provide sufficient gate voltage because it is operated at 20 V. The circuit configuration is shown in Figure 5(a). The maximum current-sense (CS) voltage on pin 3 of UC3842A is 0.9 V (minimum) [9]. Hence, the current sensing resistor $R_5$ is 0.9/3.2 = 0.28 $\Omega$ with power dissipation less than 0.5 W. Three 1 $\Omega$ (1/4 W) and one 2.2 $\Omega$ (1/4 W) are connected in parallel to obtain the required resistance. A RC filter (1 $\text{k}\Omega$ and 470 pF) is added to “kill” the voltage spikes. The corner frequency of the filter is 339 kHz.

To be able to synchronize externally, the power supply must have a free-running frequency below 15 kHz. For the simplification of the design and operation of the oscillation in UC3842A, a constant current source $I_1$ is used instead of a resistor $R_T$. Since the internal current source $I_2$ in UC3842A provides a discharging current of 8.4 mA,
the dead time $t_2$ and switching frequency can be determined as follows.

$$I_1 = \frac{1.6}{T_1} \text{ and } I_2 - I_1 = \frac{1.6}{T_2} \quad (l_2 > l_1)$$

$$T = t_1 + t_2 = 1/f_s$$

The hysteresis voltage of the oscillator is $1.6 \text{ V}$. The time periods $t_1$ and $t_2$ are the rise and fall times of the triangular waveforms ($V_{CT}$). Due to the effect of leakage inductance, other parasitic and snubber circuits at $f_s = 32 \text{ kHz}$, the dead time $t_2$ is set to $6-8 \mu \text{s}$. Then, if the free-running frequency is assumed to be $12.5 \text{ kHz}$, $t_1/T = 0.91$,

$$\frac{l_2 - l_1}{l_1} = \frac{0.91}{1 - 0.91}$$

or $l_1 = 0.756 \text{ mA}$ and $C_T = 0.036 \mu \text{F}$

The constant current source $I_1$ is implemented using a single PNP transistor $Q_3$. The current gain of $2N3906$ is about $200$. The current through $RB_1$ and $RB_2$ is assumed to be $20 \times IB_3$, and the emitter voltage is set to $4 \text{ V}$ since the peak voltage of $V_{CT}$ is $3 \text{ V}$. Then, we have,

$$RE = 1/I_1 = 1.32 \text{ k} \Omega$$

and $IB_3 = 0.756 \text{ mA} / 200 \approx 4 \mu \text{A}$. Since $V_{B3} = 5 - 1 - 0.7 = 3.3 \text{ V},$

$$5 \times RB_2(RB_1 + RB_2) = 3.3$$

$$RB_1/RB_2 = 0.515$$

$$RB_1 = 20 \text{ k} \Omega \text{ and } RB_2 = 39 \text{ k} \Omega$$

The practical values for $RE$ and $C_T$ are $1.2 \text{ k} \Omega$ and $39 \text{ nF}$, and the free-running switching frequency is around $13 \text{ kHz}$. The constant current source $I_1$ can be directly replaced by Motorola current regulating diode (1N5294), which is a JFET with gate-source short-circuited. The regulated output current is actually its saturation current $I_{DSS}$ at pinch-off.

The external synchronization is achieved by the one-shot triggering circuit built around $Q_2$. It is active once when the falling edge of sync pulse appears. Then, a single high pulse of $2$ to $3 \mu \text{s}$ charges the timing capacitor $C_T$ through the charging resistor $RC$, at a very fast rate (about $50$–$100$ times the normal rate). The value of $RC$ can be calculated by,

$$(5 - 2.8 - 0.5) / (100 \times 0.756) = 47 \Omega$$

The minimum voltage drop on $RC$ is approximately $5 - 2.8 - 0.5 = 1.7 \text{ V}$ because $V_{CT}$ swings between $1.2$ to $2.8 \text{ V}$, with respect to ground [9], and the saturation voltage of $Q_2$ is about $0.5 \text{ V}$. The choices of the input capacitance and BE resistance can vary the pulse period. The anti-parallel BE diode, $1N4148$ is to prevent the BE junction from possible avalanche breakdown if the amplitude of $V_{SYNC}$ is above $5 \text{ V}$.

It is also possible to combine the sync circuit into the constant current source by injecting the sync signal into the base of the current source transistor.

The feedback scheme is selected as follows. A voltage reference with comparator (linear error amplifier) TL431 detects and amplifies the error signal, and drives the LED of the opt-coupler MOC8102. The gain of the error amplifier (EA) in UC3842A is set to unity for better noise immunity and stability. Since the output voltage of the error amplifier is from $1.4$ (two diode drops) to $4.1 \text{ V}$ ($1.4 + 0.3 \times 3$) typically [9], and $V_E$ is equal to $(5 - output \ voltage \ of \ EA)$, the voltage $V_E$ across $R_{OP}E$ is from $0.9$ to $3.6 \text{ V}$.

In the past opto-couplers have suffered from current transfer ratio (CTR) degradation. The main cause for CTR degradation is the reduction in efficiency of the LED within the opto-coupler due to the increase in space-charge recombination within the diode. Past industry LED burn-in data under accelerated conditions indicated that a $15\%$ to $20\%$ degradation after 1000 hours was unusual. Of even more concern was the fact that the population also contained “fliers” units through infant mortality mechanisms eventually exhibited degradations approximately $50\%$. A typical percentage degradation is $40\%$ after $10^5$ hours normal operation at $I_F = 25 \text{ mA}$. In 1987, Motorola’s Optoelectronics Operation decided to resolve the industry-wide problem of LED light output degradation. They concentrated their efforts to improve and control certain critical LED wafer processing steps and eventually, $5000$ hours of accelerated stress burn-in testing shows zero degradation. This means that low degradation characteristics are now achievable not only on an average (mean) basis, but also that “fliers” can be eliminated. Therefore, the opto-isolator can be regarded as a low-cost, reliable, simple but high performance component to be used in future power supplies. Besides the zero degradation of CTR, the new MOC810X series opto-coupler that are specifically designed for switching power supplies provides two additional features. Their specifications include tightly controlled window values of CTR. Also, each device’s internal base connection has been eliminated, effectively minimizing the noise susceptibility problem. Noise is further minimized by coplanar die placement, which puts the LED and phototransistor end-to-end, rather than one above the other. The result is a mere $0.2 \text{ pF}$ coupled capacitance, which minimizes the amount of capacitively coupled noise that is injected by the optoisolator.

MOC8102 is selected due to its moderate CTR (from $0.73$ to $1.17$ at $I_F = 10 \text{ mA}$) [11]. Then, two extreme cases are considered. For the lowest $I_F$ delivered by TL431, it should provide sufficient coupled current to develop a minimum voltage of $0.9 \text{ V}$ on $R_{OP}E$. The operating current range of $I_F$ is chosen to be $0.5$ to $20 \text{ mA}$. For the highest limit of the selected $I_F$ range, i.e. $20 \text{ mA}$, the value of $R_{OP}E$ is $3.6 \text{ V} / 0.5 \times 20 \text{ mA} = 360 \Omega$, if CTR is at the lowest value, i.e. $0.5$ approximately. Then, nearly whole ranges of CTR and $I_F$ are covered by the design with $R_{OP}E$ equal to $360 \Omega$. The practical value for $R_{OP}E$ is selected to be $390 \Omega$. For the determination of $R_{OP}D$, the maximum LED current is considered. Thus, the value of $R_{OP}D$ is $(8 - 1) \text{ V} / 20 \text{ mA} = 350 \Omega$. A $330 \Omega$ resistor is used in practice.

The feedback point is directly taken from the positive terminal of the output capacitors $C_{O1-10}$. This point must be placed before the output LC filter because the filter forms an additional double-pole in the feedback loop. Since the internal reference voltage of TL431 is $2.5 \text{ V}$, the values of $R_X$ and $R_Y$ (the voltage divider) are chosen to be $R_X = 142 \text{ k} \Omega$ and $R_Y = 3.3 \text{ k} \Omega$ because, $110 R_Y/(R_X + R_Y) = 2.5$ or $R_Y/R_X = 43$.
The gate drive circuit consists of a series 10 Ω resistor to minimize the "gate ring" problem. But for MJE18004, the base drive circuit is not as simple as that for MOSFET. It is shown in Figure 5(b). The supply voltage of the current-mode controller is lowered to 10 V in order to minimize the power loss in base drive circuit, and meanwhile, UC3843A is used instead of UC3842A, which has a lower ON threshold of supply voltage. Other functions are identical to UC3842A. The typical hFE value for MJE18004 is 14 [6], and thus, it is assumed that the minimum hFE value is 10 partly because of the tight control in manufacture. Then, the minimum base current Ib is 3.2/10 = 0.32 A to maintain transistor saturation at full load. A slightly larger base current of 0.35 A is used practically. From [9], the voltage drop on the source output transistor of UC3843A is about 2 V at an output current of 0.35 A. And the value of VBE(sat) of MJE18004 is 0.95 V [6]. Therefore, the value of base resistor RB is,

\[ R_B = \frac{10 - 0.95 - 2}{0.35} = 20 \Omega \]  

The base drive capacitor CB can be determined by 1/(2\(\pi f_C R_B)\) ≈ \(f_C\)min)/2, i.e. CB ≈ 1 μF. Note that the BE junction of MJE18004 will not have avalanche breakdown because the breakdown voltage of BE junction is about 9 V. Other optimum base drive circuits can be found in [7] (e.g., how to use base inductor to improve the turn-off operation of power transistor).

As shown in Figures 3 and 5, the primary control circuitry is self-supplied. The required power is delivered from the transformer winding NA through DA and RA. A zener diode of appropriate voltage rating is used to regulate the supply voltage for IC1. For UC3842A and MTP4N90, the supply voltage is 20 V and the total supply current is about 20 to 50 mA. Thus, NA is chosen to be 18 turns to provide an extra 5 V for regulation. RA is set to 47 Ω.

2.6 CLOSING THE FEEDBACK LOOP

After determination of almost all the component values and configurations for the flyback power supply, the last but not the least piece to design is the feedback loop. Figure 6(a) shows the gain-block diagram of the flyback power supply. The input of the system is the internal reference voltage in the TL431, which is 2.5 V ± 1%, and is compared to the feedback signal. The H-block is purely

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**Figure 6a. Approximate d.c. and Low-Frequency a.c. Model of the Flyback Power Supply**

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a voltage divider formed by \( R_X \) and \( R_Y \), thus the gain value in this block is \( \frac{3.3}{142 + 3.3} = 0.0227 = H_0 \). The difference or error signal is then amplified by the error amplifier in TL431, which is compensated externally. The compensation network is chosen to consist of an integrating capacitor \( C_f \) and a resistor \( R_f \). Thus, we have,

\[
A = \frac{-1}{sC_fR_f}
\]

where \( s \) = Laplace transform operator (jw for sinusoidal analysis),

\[
R_f = \frac{R_XR_Y}{(R_X + R_Y)} = 3.23 \, k\Omega
\]

The capacitance value of \( C_f \) can be determined for overall stability of the power supply once when the forward gain \( G \) is known under the worst condition.

The low-frequency a.c. model for the discontinuous-mode current-injected flyback converter consists of a d.c. gain block cascaded with a single-pole roll-off network which has a pole frequency at \( 1/(\pi C_0 R_L) \), where \( C_0 \) is the total output capacitance and \( R_L \) is the total load resistance at \( V_0 \) \([1]\). The equivalent maximum load resistance \( R_L(\text{max}) \) is approximated by experimental measurements at no load, \( f_s = 32 \, \text{kHz} \) and \( V_{CC} = 200 \, \text{V} \) (for MTP4N90). The input current was measured to be 0.06 A and thus,

\[
R_L(\text{max}) = 110^2/(200 \times 0.06) = 1 \, \text{k}\Omega
\]

For the equivalent total output capacitance (for MTP4N90), the capacitances at three output circuits are lumped to +110 V output, and by charge relation,

\[
C_0 = [(110 \, \text{V}) \times (66 \, \mu\text{F}) + (15 \, \text{V})(330 \, \mu\text{F}) + (8 \, \text{V})(470 \, \mu\text{F})]/110 \, \text{V} = 145 \, \mu\text{F}
\]

Hence, the lowest corner frequency \( f_p \) of the flyback power supply is approximately 2.2 Hz. If the ESR and ESL of the output capacitors are neglected, the G-block has a transfer function \([1]\) as,

\[
G = G_0/(1 + s/W_p)
\]

where \( W_p = 2\pi f_p = 13.8 \, \text{rad/s} \).

The forward gain block \( G \) is subdivided into its individual elemental blocks in Figure 6(a). They are the resistor \( R_{opD} \) which converts the output voltage of TL431 into the diode current for the LED of MOC8102, the non-linear CTR (0.65 to 4.5 from data sheet), the resistor \( R_{opE} \) which generates a voltage \( V_e \) from the coupled current \( I_C \), the internal one-third divider of UC3842A/3843A (the minus sign is due to the inverting configuration of the op amp), the current sensing resistor \( R_s \) which relates \( V_C \) to \( I_{pk} \), and finally, the gain of the power stage which includes the signal pole. The d.c. gain of the power stage can be directly derived from the power relation,

\[
\frac{V_{o2}}{R_L} = \frac{1}{2} \frac{Lp I_{pk}^2 f_s}{1}
\]

or

\[
V_{o pk} = \sqrt{\frac{Lp R_L f_s}{2}}
\]

Thus,

\[
G_o = \frac{-R_{opE} R_{opD} (CTR)}{3 R_s} \sqrt{\frac{R_L Lp f_s}{2}}
\]

The value of d.c. gain \( G_o \) can be determined analytically by substituting parameters under worst case, i.e. \( f_s = 32 \, \text{kHz} \) and \( R_L = 1 \, \text{k}\Omega \) (including +9 V and +15 V rails), when the value of \( G_o \) is highest. On substituting the known parameters,

\[
R_{opE} = 390 \, \Omega \quad R_{opD} = 330 \, \Omega \quad CTR = 1 \quad \text{(for MOC8102)}
\]

\[
R_s = 0.28 \, \Omega \quad Lp = 1.66 \, \text{mH}
\]

we have,

\[
|G_o| = 229 \text{ or } 47.2 \, \text{dB}
\]

It is observed that a local feedback occurs in the TL431 output circuit and the LED of the opto-coupler. Its end effects are:

1. loop-gain enhancement by the additional block connected in parallel with A-block, i.e. \( 9/(111 H_0) = 3.57 \);
2. a proportional-integral (PI) controller resulted, instead of a pure integrator.

The overall gain (transconductance) of the feedback error amplifier can be derived as follows.

\[
|f| = \frac{V_o}{(9/111) - V_o H_0 A} = \frac{9/(111 H_0) - A}{H_0 V_o}
\]

or

\[
|f| = \text{a.c. component of } f \text{ (LED current)}
\]

To simulate the equation (13), an additional block consisting of \( 9/(111 H_0) \) only is placed in Figure 6(a). The zero frequency of the error amplifier is,

\[
w_f = 1/(3.57 C_f R_f)
\]

when \( |A| = 9/(111 H_0) \).

After knowing all equivalent a.c. gains of the converter circuit, we can determine the value of \( C_f \) for optimum circuit dynamic performance. Since there is merely one

![Figure 6b. Bode Plot of the Flyback Converter at \( f_s = 32 \, \text{kHz} \) and No Load](image-url)
parameter that can be varied, i.e., $C_f$, and only one optimum condition (either gain or phase) can be satisfied, we set the minimum phase of the loop gain to $-120^\circ$ to guarantee the relative stability. That means $W_f$ should be placed $30/45 = 0.667$ decade beyond $W_p$ or,

$$W_f = 100.667 \text{ Wp}$$

$$= 4.64 \text{ Wp} = 64 \text{ \mu} \text{rad/s}$$

because the down slope phase of the phase of the flyback converter gain is $-45^{\circ}/\text{decade}$ and the PI controller has an initial phase shift of $-90^\circ$. Then,

$$C_f = 1/[(3.23 \text{ k}) (3.57) (64)] = 1.355 \mu\text{F}$$

A practical value of $1.5 \mu\text{F}$ is used. Plots for the overall loop gain of the power supply at $f_s = 32 \text{ kHz}$ and minimum load is shown in Figure 6(b), with the following equations.

$$A(f) = \frac{1}{sC_f R_f} + \frac{9}{111 H_0} = \frac{206.4}{14} + 3.57$$

$$G = \frac{G_0}{1 + s/W_p}$$

$$W_p = 13.8$$

$H_0 = 0.0227$

Gain $(f) = 0.2 \log_{10} |A'(f)| \times G \times H_0|$

Phase $(f) = \text{Arg}[A'(f)] \times G \times H_0|$

The unity gain bandwidth is about 40 Hz (at $f_\text{T}$) and the phase margin is about $82^\circ$. But, the dominant value in the phase plot is its lowest value of $-128^\circ$ at $W_f$, where the gain is greater than 0 dB. It determines nearly all transient load responses.

2.7 OTHER OPTIONS

Under normal circumstances, the output voltage should not exceed 150 V. But, as protection for the monitor circuits (it would generate X-ray if extremely high anode voltage appears), an optional high-voltage zener diode 1N5953A (1 W) is connected across the 110 V output rail. If abnormally high voltage (>150 V) continuously appears on this rail, the zener diode will be zapped to form a permanent short-circuit. Other better OVP circuits such as SCR crowbar circuit and 0 V shutdown circuit can be used with higher unit cost.

Another option which may be required in the power supply is short-circuit (not just overload) protection. Since the flyback power converter is operated with current-mode control, it is inherently over-power protected. But, if the outputs are short-circuited, maximum power will be delivered to the low voltages with high output currents. Then, the output rectifiers and windings are likely to be damaged. Short circuit protection is generally best installed in secondary output(s). Shutdown or foldback signal(s) can be fed to the UC3842A/3843A by a Motorola optocoupler.

To improve and control the start-up transients, a soft-start circuit may be added to the current-mode controller. Typical example can be found in [9].

3. UNIVERSAL INPUT-VOLTAGE ADAPTOR

The universal input-voltage adaptor is used with bridge rectification circuit to provide a rather narrower range of rectified d.c. output voltage at either low or high range of input voltage, i.e., 90–130 Vac or 180–260 Vac. A simplified circuit block diagram has been shown in Figure 2, and the detailed circuits are shown in Figure 7(a) and (b). The voltage range selection is performed by an over-voltage detector and the adaptor is supplied from a charge pump circuit. At low range, the triac is fired continuously by the adaptor, and a voltage doubler is formed, while simple bridge rectification is retained at high range. The rectified output voltage $(V_{CC})$ range is from 200 to 370 Vdc.

**Figure 7a. Negative Gate (Triac) Current — Preferred**

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3.1 ADVANTAGES OF USING UNIVERSAL INPUT-VOLTAGE ADAPTOR

Three advantages are gained by using the universal input-voltage adaptor. They are:
1. smaller ripple current in the smoothing bulk capacitors for fixed output power;
2. less output ripple voltage at the rectified d.c. output (VCC) at constant output power;
3. greatly reducing the stresses (voltage and current) on the power switch of the flyback converter for constant output voltage (V0).

3.2 DETAILS OF CIRCUIT DESIGN

To select a suitable capacitance for the input bulk capacitors Cin, the ripple voltage at VCC is considered. Sketches of voltage and current ripples are shown in Figure 7(c) and (d) for the following analysis. Figure 7(c) is for normal bridge rectification, while Figure 7(d) is for voltage doubler.

For simple bridge rectification, the ripple voltage δVCC is related to the capacitance of Cin as follows, from the power relation. It applies provided that ta is much less than T/2,

\[ P_{in} = \frac{1}{2} (C_{in}/2) \left[ V_{CC(pk)}^2 - V_{CC(min)}^2 \right] \left(2f_{in}\right) \]

or

\[ C_{in} = \frac{P_{in} \cdot \left(2f_{in}\right)}{V_{CC(pk)}^2 - V_{CC(min)}^2} \] (16)

and \( \delta V_{CC} = V_{CC(pk)} - V_{CC(min)} \)

where \( V_{CC(pk)} \) = peak voltage at VCC = 1.414 x input voltage (rms),
\( V_{CC(min)} \) = lowest voltage at VCC,
\( f_{in} \) = frequency of input voltage.

For the worst case, \( V_{CC(pk)} = 180 \times 1.414 = 255 \text{ V}, \)
\( V_{CC(min)} = 200 \text{ V}, P_{in} = 128.6 \text{ W} \) and \( f_{in} = 50 \text{ Hz} \) since the lowest working voltage of the flyback power supply is 200 V, and the frequency of input voltage is from 50 Hz to 60 Hz. Therefore,

\[ C_{in} = 205.6 \mu F \]

The time period \( t_{a} \), the conduction time of the bridge rectifiers, is given by,
In order to evaluate the rms ripple current \( I_{\text{cap(rms)}} \) of the smoothing capacitors \( C_{\text{in}} \), a triangular approximation is used to simplify the derivation. The a.c. peak current \( I_{\text{cap(pk)}} \) of \( C_{\text{in}} \) is,

\[
I_{\text{cap(pk)}} = C_{\text{in}} \frac{dV_{\text{CC}}}{dt} = \pi f_{\text{in}} C_{\text{in}} \sqrt{V_{\text{CC(pk)}}^2 - V_{\text{CC(min)}}^2} \\
= 5.5 \text{ A for the practical value of } C_{\text{in}} \text{ equal to } 220 \mu \text{F.}
\]

Thus,

\[
I_{\text{cap(rms)}} = I_{\text{cap(pk)}} \sqrt{\frac{2}{3}} = I_{\text{cap(pk)}} \sqrt{\frac{t_a}{3T/2}} \tag{19}
\]

assuming that the a.c. component contributed by the switching operation of the flyback converter is negligible. This assumption holds because the high-frequency (switching frequency) ripple current is filtered by the additional small-valued capacitor (0.1 \( \mu \text{F} \)) connected across \( V_{\text{CC}} \).

With reference to Figure 7(d), the voltage doubler, the two capacitors are alternatively charged to peak line voltage. Note that whenever the rectified voltage \( V_{\text{CC}} \) is at instantaneous minimum \( V_{\text{CC(min)}} \), the voltage of one capacitance is at its minimum, but the voltage on the other capacitor is at half way between peak and minimum voltages, \( V_{\text{C(pk)}} \) and \( V_{\text{C(min)}} \) respectively. The value of \( V_{\text{C(min)}} \) can be determined as follows.

\[
V_{\text{CC(min)}} = V_{\text{C(min)}} + \frac{1}{2} [V_{\text{C(pk)}} + V_{\text{C(min)}}] \\
\text{or } V_{\text{C(min)}} = \frac{1}{2} [2V_{\text{C(min)}} - V_{\text{C(pk)}}]^3 \\
= 91 \text{ V for } V_{\text{C(pk)}} = 90 \times 1.414 = 127 \text{ V and } V_{\text{CC(min)}} = 200 \text{ V.}
\]

From energy law,

\[
\frac{P_{\text{in}}}{2} = \frac{1}{2} C_{\text{in}} \frac{1}{2} V_{\text{C(pk)}}^2 - V_{\text{C(min)}}^2 f_{\text{in}} \\
C_{\text{in}} = \frac{P_{\text{in}}}{\frac{1}{2} V_{\text{C(pk)}}^2 - V_{\text{C(min)}}^2 f_{\text{in}}} \tag{21}
\]

\[
= 327.5 \mu \text{F at } f_{\text{in}} = 50 \text{ Hz and full load.}
\]

The time \( t_a \), ripple currents \( I_{\text{cap(pk)}} \) and \( I_{\text{cap(rms)}} \) are given by,

\[
t_a = \frac{2\pi f_{\text{in}}}{\cos^{-1} \left( \frac{V_{\text{C(max)}}}{V_{\text{C(pk)}}} \right)} = 2.46 \text{ ms} \tag{22}
\]

\[
I_{\text{cap(pk)}} = \frac{2\pi f_{\text{in}} C_{\text{in}} \sqrt{V_{\text{C(pk)}}^2 - V_{\text{C(min)}}^2}}{3} \\
= 9.18 \text{ A for } C_{\text{in}} = 330 \mu \text{F (practical value).}
\]

\[
I_{\text{cap(rms)}} = I_{\text{cap(pk)}} \sqrt{\frac{t_a}{3T/2}} \tag{24}
\]

\[
= 1.86 \text{ A}
\]

As the power supply is designed to operate at both input ranges, the latter case defines the relevant maximum ripple current. In order to demonstrate the effectiveness of the universal input-voltage adaptor, the ripple current and voltage assuming no doubler are calculated to be, with \( C_{\text{in}} = 330 \mu \text{F}, V_{\text{in}} = 90 \text{ Vac and } P_{\text{in}} = 128.6 \text{ W at } 50 \text{ Hz,}
\]

\[
V_{\text{CC(min)}} = \left[ (127^2 - 128.6/(60x165\mu\text{F}))^{1/2} = 23.3 \text{ V}
\]

\[
\delta V_{\text{CC}} = 23.3 - 23.3 = 103.7 \text{ V (compared with } 55 \text{ V for high range)}
\]

\[
t_a = 4.4 \text{ ms}
\]

\[
I_{\text{cap(pk)}} = 6.5 \text{ A}
\]

\[
I_{\text{cap(rms)}} = 3 \text{ A (nearly double of the value with voltage doubler).}
\]

Such a large ripple voltage at \( V_{\text{CC}} \) will greatly stress the switching transistor and will degrade the overall performance, especially the conversion efficiency and regulation.

The bridge rectifiers are selected to be 1N5398, a 1.5 A device because the highest average line input current is 0.9 x 128.6/90 = 1.3 A. The two 1 W resistors, in parallel with \( C_{\text{in}} \), are used to discharge the input capacitor after powered off. Note that one of them is connected to "start-up" at one end instead of the ground (the inverted triangular sign). It provides the starting current for the current-mode controller and drive circuit at initial power-on, when the control circuitry is still not self-supplied. The start-up current is limited to approximately 2 to 4.6 mA.

The inrush input current is limited to an acceptable level by the thermistor which has a resistance of 5 \( \Omega \) at room temperature and 1 \( \Omega \) after heated up.
MAC229A8 has been found suitable for the triac in the universal input-voltage adaptor because of the following points:

1. It is a sensitive gate device with IGT of 10 mA maximum for operation quadrants I, II and III [13]. The small gate current requirement will minimize the power dissipation in the adaptor and will lower the capacitance of the charge-pump capacitor C.

2. Its breakdown voltage is 600 V, which exceeds all input voltage limits.

3. Guaranteed 25 V/µs, rate of rise of off-state voltage ensures the accurate operation of MAC229A8 [13].

4. Low power loss in the device due to its low voltage drop across MT1 and MT2 at operation.

MC3423 is originally designed for overvolt “crowbar” sensing circuit, but it is also applicable in the universal input-voltage adaptor because of the similar working condition [14]. It has a temperature-compensated internal reference voltage of 2.6 V which is connected to one terminal of the input comparator. Thus, if the trip point at which the triac is turned off is set to 135 Vac or 191 Vdc, the divider ratio in Figure 7(a) is,

\[ \frac{2.6}{191} = \frac{A_2}{A_1 + A_2} \]

or \[ A_1/A_2 = 72.5 \]

\[ A_1 = 2.2 \text{ MΩ} \] and \[ A_2 = 30 \text{ kΩ} \].

The internal constant current source (pin 4) can provide a time delay before tripping the “crowbar” SCR. It results in better noise immunity and controlled start-up transients of the adaptor. The practical values of the capacitor and resistor connected at pin 4 to ground are 50 nF and 560 kΩ, respectively, which has a time delay of approximately 650 µs. The output is connected, through a resistive divider, to a small-power SCR (MCR102 with IK(max) = 0.8 A). When the input voltage is detected to be above the trip point, the SCR is fired to shunt all the incoming current from the charge pump, and the triac will remain off.

The MC3423 can operate from 4.5 V to 40 V of supply voltage [15]. Hence, a 6.2 V zener diode is used to clamp the supply voltage of the crowbar sensor to 6.2 + 0.7 = 7 V for stable operation. A 100 pF filtering capacitor for the sensing divider and a small-signal diode 1N4148 for clamping the input of MC3423 are also added in the circuit.

To calculate a suitable value for the charge-pump capacitor C, the working principle of the charge pump is first considered. It consists of two diodes (1N4001), a coupling capacitor C, and a smoothing capacitor (100 µF). C is charged during the rise time of input voltage and is discharged during fall time. Assuming that the voltage drop on the charge pump circuit is much less than the peak of input voltage (Vp), from charge balance principle,

\[ Q = \left( \frac{V_{p}}{2} \right) C = IT \]

or \[ C = \left( \frac{IT}{2V_{p}} \right) \]

where \( I = \) average d.c. current supplied to the line adaptor.

The boundary case is at low line, low range, where \( V_{p} = 127 \) V and \( I = 10 \) mA for gate current plus 6 mA for bias current. Thus,

\[ C = \left( \frac{10 + 6}{127} \right) \times 100 \mu F = 1.2 \mu F \]

At high line, high range, \( V_{p} \approx 370 \) V and the maximum value of \( I \) is 53 mA at 60 Hz. The maximum power consumption of the line adaptor is 7 x 0.053 = 0.37 W. The 10 Ω resistor in series with C is used to limit the inrush current when starting.

So far in the design of the universal input-voltage adaptor, an important point which has not yet been considered is the hazard of severe overvoltage at VCC during startup. If the power supply is started at high line, high range, \( V_{in} = 260 \) Vac, during the falling edge of input voltage, and the supply voltage of MC3423 is charged to about 7 V, the triac will be turned on for the doubler operation in the remaining negative cycle of input voltage, without the gate capacitor \( C_G \), since MC3423 had not yet and would not be tripped until the next positive cycle. Then, the lower bulk capacitor will be stressed to nearly double of its normal voltage rating. This harmful effect not only damages the bulk capacitor, but also produces abnormally high input voltage (VCC) for the flyback converter, in a small instant. Therefore, \( C_G \) is connected to the gate and MT1 terminal of the triac to serve two purposes:

1. to delay the turn-on of triac for nearly a quarter of one cycle.

2. to increase the dV/dt blocking capability of the triac (> 200 V/µs) and hence, the overall system reliability [13].

![Figure 7e. Worst Case Consideration for the Universal Input-Voltage Adaptor (Negative Gate Current)](image-url)
Figure 8. Complete Circuit Schematics of 90 W Off-the-Line Power Supply
The determination of the capacitance of \( C_G \) is determined as follows, with reference to Figure 7(e). At high line, high range, and 60 Hz, the average current \( I \) is maximum (53 mA). All discussions below are referred to a falling edge and the consequent rising edge of less than 1/4 cycle of input voltage, because the charge-pump capacitor \( C \) is discharging to the adaptor circuit during fall time and the crowbar sensor cannot be tripped if \( V_{in} \) falls beyond +200 V. If the supply voltage for MC3423 is just about 4.5 V, the crowbar sensing IC functions, and meanwhile, the instantaneous input voltage is at the trip point (200 V) and is going to the negative cycle, the gate capacitor \( C_G \) must be large enough to delay the conduction of the triac before the input voltage rises again, i.e. at the negative peak. Assume that, for simplicity, the supply voltage of MC3423 rises to about 6.2 V (zener voltage) when the input voltage falls to -200 V. Then,

\[
I_x = \text{charging time of the capacitor across the supply voltage of MC3423} = \frac{2 \times \sin^{-1} \left( \frac{200}{367} \right)}{(2 \pi \times 60)} = 3 \text{ ms}
\]

or capacitance value \( \approx 100 \mu F \) (connected across supply voltage of MC3423)

But this capacitance is necessary to meet the ripple voltage requirement of the adaptor circuit. Afterwards, the zener diode (1N4735A) conducts, and the two capacitors connected in parallel are needed to delay the remaining time \( t_y \) before the input voltage rises from its negative peak again, within the same negative cycle. Therefore,

\[
t_y = \left( \frac{16.67}{4} - \frac{3}{2} \right) \text{ ms} = 0.7 \text{ V} \times (C_G + 100) \mu F/47 \text{ mA}
\]

since the threshold gate voltage of MAC229A8 is 0.7 V typically.

\( C_G = 79 \mu F \)

A practical value of 100 \( \mu F \) is used in Figure 8. Note that the discharging current of \( C \) at zero-crossing of input voltage is greater than the average value \( I \). The time constant of the gate capacitance and gate resistor (1 k\( \Omega \)) is 0.1 s, which is sufficient for resetting the triac between consecutive power-off and on. The 10 k\( \Omega \) resistor is for discharge of the 100 \( \mu F \) capacitor, and the corresponding time constant is 1 second. Time constants too long in the above design may result in failure of the universal input-voltage adaptor if the power supply which was previously socketed in 110 V line is quickly plugged in 220 V line.

It should be noted that two optional power zener diodes (1N5956A) are connected across each bulk capacitor \( C_{in} \) because:

1. they can absorb short transient voltages (\( >200 \text{ V} \)) on \( C_{in} \);
2. they can prevent any failure of the universal input-voltage adaptor from damaging the flyback converter and the two bulk capacitors.

Although such failures are rare, the consequences are to be avoided since failure of the line adaptor poses a safety hazard to the human beings (especially the eyes radiated by X-ray).

Common-mode and differential-mode EMI/RFI filters are generally required for all switching power supplies. They are included in Figure 8, but are excluded in the DEMO board.

### 4. PERFORMANCE OF THE FLYBACK POWER SUPPLY

#### 4.1 COMPLETE CIRCUITRY

Figure 8 shows the complete circuit schematic of the 90 W flyback power supply. The triac in the universal adaptor is negatively driven by the charge pump, since

![Figure 8](image_url)

**Figure 8. Universal Input-Voltage Adaptor**

**Figure 9. P.C.B. and Component Layouts**

![Figure 9a](image_url)

**Figure 9a. Universal Input-Voltage Adaptor (+IG)**

![Figure 9b](image_url)

**Figure 9b. Universal Input-Voltage Adaptor (-IG)**

![Figure 9c](image_url)

**Figure 9c. Main Board (for MTP4N90 & MJE18004)**

![Figure 9d](image_url)

**Figure 9d. P.C.B. and Component Layouts**

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it is least sensitive to noise in this mode. Drive circuits for MTP4N90 and MJE18004 are also shown.

Sometimes, it is unnecessary to have the universal input-voltage adaptor because the power supply may be used only at one range. Then, a modular approach for the adaptor can lower the system cost and can increase the flexibility of manufacture. The universal input-voltage adaptor board can be simply removed or unplugged from the power supply board without affecting the normal operation of the power supply, if the adaptor is not needed. Therefore, using this approach, the adaptor becomes optional. The printed circuit board and component layouts of the universal input-voltage adaptor(s) and the main board of power supply are shown in Figure 9. The construction diagram of the power transformer is shown in Figure 10. Table 1 lists all Motorola semiconductor components used in this power supply.

### Table 1. List of Motorola Semiconductor Components

<table>
<thead>
<tr>
<th>Part Numbers</th>
<th>Qty.</th>
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</thead>
<tbody>
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<td>IC</td>
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<tr>
<td>UC3842A (for MTP4N90)</td>
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</tr>
<tr>
<td>UC3843A (for MJE18004)</td>
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<tr>
<td>MC3423P</td>
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</tr>
<tr>
<td>TL431CLP</td>
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<td>Opto</td>
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<tr>
<td>MOC8102</td>
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</tr>
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<td>MCR102</td>
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<td>TRIAC</td>
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<tr>
<td>MAC229A8</td>
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<tr>
<td>BJT</td>
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</tr>
<tr>
<td>MJE18004</td>
<td></td>
</tr>
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<td>2N3906</td>
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<td>Rectifier</td>
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<td>MUR180</td>
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<td>1N4747A 20 V (for MTP4N90)</td>
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<tr>
<td>1N5953A 150 V (optional)</td>
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<tr>
<td>1N5956A 200 V</td>
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</table>

4.2 EXPERIMENTAL MEASUREMENTS AND RESULTS

D.C. measurements are summarized in Table 2. Line and load regulation are excellent (better than 0.5%) for the +110 V output. Regulation for other two rails is within 10%, if the transformer is properly manufactured. Conversion efficiency, is close to the expected figure (70%), and the best one is 73.7% at I<sub>0</sub>(110) = 0.7 A, f<sub>s</sub> = 15.7 kHz and V<sub>CC</sub> = 360 V for MTP4N90; whereas for the bipolar power transistor MJE18004, the best efficiency is 74.2% at I<sub>0</sub>(110) = 0.7 A, f<sub>s</sub> = 15.7 kHz and V<sub>CC</sub> = 360 V. Although MJE18004 has lower conduction loss than MTP4N90, it has higher power losses in the base drive circuit and in the switching transitions. This is why MOSFETs can compete with advanced BJT even with higher conduction loss at relatively low switching frequency.

The maximum ripple voltage at 110 V output is approximately 150 mV (peak-to-peak) which is less than 0.2% of the output voltage, as predicted in section 2.3. The power supply is observed to be stable over the entire range of load currents. The dynamic response is also satisfactory, with an overshoot of less than 8 V at f<sub>s</sub> = 15.7 kHz and V<sub>CC</sub> = 200 V, from half-load to full-load (see Figure 1). Also in Figure 12, the transient responses of the power supply are introduced for very large-signal disturbances — from no load to full-load. The overshoot is about 20 V and the undershoot is over 30 V, which is quite satisfactory. The overshoot can be further reduced by increasing the integrating capacitance C<sub>f</sub> in the feedback loop. But, this will result in slower transient responses.

Typical experimental switching waveforms are shown in Figure 11, at different load currents, input voltages and switching frequencies. Also, Figure 13 shows the photo of the 90 W off-the-line power supply.

5. CONCLUSION

A low-cost 90 W flyback power supply with external synchronization and universal input-voltage adaptor for multi-sync color monitor has been discussed in detail. The power supply has excellent line and load regulation and is found to be suitable in the application of low-cost multi-sync color monitors or TVs. Also, it can operate at both a.c. mains, i.e. 90—130 V or 180—260 V, without greatly affecting the system cost and performance.
Table 2. Performance of 90 W Off-the-Line Flyback Power Supply

### MTP4N90 (MOSFET)

<table>
<thead>
<tr>
<th>I(_0) (110 V)</th>
<th>(V_O) (110 V)</th>
<th>(15 V)</th>
<th>(8.0 V)</th>
<th>(f_s)</th>
<th>(I_in)</th>
<th>(V_{CC})</th>
<th>Efficiency</th>
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<tr>
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<td>16.01</td>
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### MJE18004 (Bipolar)

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<th>(f_s)</th>
<th>(I_in)</th>
<th>(V_{CC})</th>
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*Ripple voltage at 110 V output is about 150 mVpp at \(V_{CC} = 300\) V, \(f_s = 15.7\) kHz & \(I_0 = 0.7\) A.

Figure 11. Experimental Oscillograms

**Figure 11a.** Key Waveforms at \(f_s = 25\) kHz and \(V_{CC} = 300\) V (for MTP4N90)

**Figure 11b.** \(V_{CE}\) and \(V_{BE}\) at \(f_s = 25\) kHz and \(V_{CC} = 300\) V (for MJE18004)
Figure 11. Experimental Oscillograms

Figure 11c. $V_{DS}$ and $V_{GS}$ at $f_5 = 15.7$ kHz and $V_{CC} = 360$ V (for MTP4N90)

Figure 11d. $V_{DS}$ and $V_{GS}$ at $f_5 = 15.7$ kHz and $V_{CC} = 200$ V (for MTP4N90)

Figure 11e. $V_{DS}$ and $V_{GS}$ at $f_5 = 25$ kHz and $V_{CC} = 360$ V (for MTP4N90)

Figure 11f. $V_{DS}$ and $V_{GS}$ at $f_5 = 25$ kHz and $V_{CC} = 200$ V (for MTP4N90)

Figure 11g. $V_{DS}$ and $V_{GS}$ at $f_5 = 32$ kHz and $V_{CC} = 360$ V (for MTP4N90)

Figure 11h. $V_{DS}$ and $V_{GS}$ at $f_5 = 32$ kHz and $V_{CC} = 200$ V (for MTP4N90)
Figure 12. Large-Signal Transient Load Responses

Figure 12a. For MTP4N90, From No Load to Full-Load at $f_s = 15.7$ kHz.

Figure 12b. For MTP4N90, From Half-Load to Full-Load at $f_s = 15.7$ kHz.

Figure 12c. For MJE18004, From No Load to Full-Load at $f_s = 15.7$ kHz.

Figure 12d. For MJE18004, From Half-Load to Full-Load at $f_s = 15.7$ kHz.

Figure 12e. For MTP4N90, From No Load to Full-Load at $f_s = 32$ kHz.

Figure 12f. For MTP4N90, From Half-Load to Full-Load at $f_s = 32$ kHz.
ACKNOWLEDGEMENTS

In the course of preparing of the manuscript, several persons gave their contributions to aid the completion of this application note. Mr. T.S. Au, a summer student from H.K. Polytechnic helped to draft all P.C.B. and component layouts and to prepare demo boards. Mr. Cedric Lai, a cooperative student from H.K. University, reviewed the script with great care. Also, continual supports from Power Group of Discrete Business, Motorola Semiconductors H.K. Ltd. was proved to be essential to the success of our works. We, Cheng and Tong, must express our thanks to these helpful people at the end of our article.

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Figure 13. Photo of 90 W Off-the-Line Power Supply
Using the CR3424 for High Resolution CRT Applications

by Curtis Gong
RF Products Division

Motorola RF Devices have used their unique high frequency RF semiconductor capabilities and thin film hybrid expertise to produce a hybrid video amplifier with less than 2.9 ns rise and fall time for a 40 V output swing. This device is the CR3424. This video amplifier provides a low power dissipation solution to a problem that has been limiting the performance of ultra-high resolution CRT monitors: video amplifier speed. This paper will discuss several points including effect of video amplifiers on CRT picture quality, basic drive requirements of the CR3424 and drive circuits for the CR3434 (example circuits and their performance will be provided).

THE VIDEO AMPLIFIER AND ITS EFFECT ON CRT PICTURE QUALITY

As stated previously, the problem that has been limiting the performance of ultra-high resolution CRT monitors is video amplifier speed. Many of the 1024 x 1024 and 1280 x 1024 pixel, 64 kHz horizontal sweep rate displays that are used in CAD/CAM and other high resolution graphics applications, have not realized their potential performance because of the speed of their video amplifiers. For these high resolution displays, the pixel width is approximately 10 ns. A video amplifier must be able to charge and discharge its load capacitance during a one pixel time period of 10 ns. A rule-of-thumb for minimum picture quality is that the pixel charge and discharge time (the rise and fall time of the video amplifier) should be no larger than 1/3 the pixel width; in this case 3.3 ns. Using this rule, the typical 3.4–4 ns rise time video amplifiers that are used in high resolution CRTs will not provide optimum picture quality. As a result, the slow video amplifier will produce dimmer vertical lines than horizontal lines. To solve this problem, monitor designers have been forced to a lower vertical refresh rate, which produces a dimmer overall picture. The CR3424 with its less than 2.9 ns (typically 2.6 ns) rise times for a 40 V output swing, and maximum output swing of 70 V, will easily provide the speed and output swing necessary for optimum picture quality (maximum flicker-free brightness).

CR3424 INPUT CHARACTERISTICS

Current Requirements

The CR3424 is a trans-impedance amplifier. To drive the CR3424 to its maximum rise time performance \( V_{\text{OUT}} = 40 \, \text{V}_{\text{P-P}} \) pulse, the input current profile must look like Figure 1. The current profile is shaped by the peaking network of

\[
\begin{align*}
20 \log (74 \, \text{mA}_{\text{P-P}}) &= 20 \log (11.4 \, \text{mA}_{\text{P-P}}) \\
\text{FREQUENCY (MHz)} &= 9.7 \\
20 \log (11.4 \, \text{mA}_{\text{P-P}}) &= 62.7 
\end{align*}
\]

Figure 3. Bode Plot
R, C and RG shown in Figure 2, the standard test set-up.

The characteristic equation for the input current is as follows:

\[ I_{in}(S) = \frac{V}{Rg} + \frac{1}{R} \left( \frac{1}{S + \frac{1}{RC}} + \frac{1}{S + \frac{1}{RgC}} \right) \]  

\[ (1) \]

The DC level of \( V_{in} \) is constant at 1.4 V for the CR3424, so the input current \( I_{in} \) can be set by adjusting \( V_1 \) such that

\[ I_{in} = \frac{V_1 - V_{in}}{R} \]  

\[ (2) \]

Often \( V_1 \) cannot be adjusted, so a different method must be used to control \( I_{in} \). Method 2 refers to Figure 5b. In this method \( I_{in} \) can be set by adjusting \( R_1 \). In this case

\[ I_{in} = \frac{V_1 - V_{in}}{R} - \frac{V_{in} - (-V)}{R_1 + R_{min}} \]  

\[ (3) \]

Note: \( R_{min} \) should be 400 Ω or greater to avoid changing the CR3424's internal thermal compensation network.

**CR3424 DRIVER CIRCUITS**

**A. Drive Circuit Design Approaches**

Any driver circuit being used to drive the CR3424 must be able to match the input current profile previously described. There are two major points that must be considered when designing a driver circuit.

1. The frequency response of the current profile must be matched.
2. The driver circuit must be able to provide the peak currents (up to ±40 mA)

There are two approaches to building a driver circuit:

1. **Voltage mode**

A circuit is designed that has an equivalent circuit similar to that of the generator in the test circuit (50 Ω output impedance). This circuit must be able to provide the peak currents. The frequency response would be obtained by using the same peaking network used in the test circuit. This network would also make the necessary voltage to current conversion.

---

**Biassing the CR3424 for a Specific DC Output Level**

The \( I_{in} \) versus \( V_{out} \) characteristics of the CR3424 is shown in Figure 4. To set the DC output level, the input current \( I_{in} \) must be set according to Figure 4. The input current can be set by one of two methods. Method 1 refers to Figure 5a.

---

**Figure 4. \( I_{in} \) versus \( V_{out} \) for the CR3424**

When deriving the equation, it is assumed that the input node to the CR3424 is a virtual ground. Bode plots of the equation are shown in Figure 3. The peak-to-peak current values listed on the plots are for a 40 Vp-p output pulse.

**Figure 5a. Input Current Adjustment, Method 1**

**Figure 5b. Input Current Adjustment, Method 2**
2. Current mode

A current source with the same frequency response as previously described would be designed. This current source would then be amplified to provide the necessary peak currents. This circuit could then be used to drive the CR3424 directly, without a peaking network. The equivalent circuits for both drivers are shown in Figure 6.

B. Example Circuits

1. Emitter Follower:

The most widely used driver circuit is the emitter follower in Figure 7. This circuit is capable of providing the peak currents without any degradation in the CR3424's performance. Rise times of 2.2 ns have been seen for a 40 Vp-p output driving an 8.5 pF load. It is important that this circuit is biased at iC = 50 mA because this circuit must work in a Class "A" mode.

There are two ways the DC offset adjustment can be made on this circuit. The previously mentioned method 1 can be implemented by replacing R1 with a potentiometer. This potentiometer could be used to vary the voltage on the emitter of the transistor which would change iin going to the CR3424. Method 2 can also be implemented for this circuit.

2. Common Emitter Driver

Another useful driver circuit is the common emitter driver shown in Figure 8. This circuit provides a voltage gain of 2. For a 40 Vp-p output and an 8.5 pF load, the rise time is 2.2 ns. If some gain is needed to compensate a gain-bandwidth problem of a pre-amp, then this circuit would be a good choice. The best method to use to adjust the DC offset is method 2.
FIGURES 9, and 10 show the performance of the CR3424 when driven by one of the previously mentioned drivers. Figure 9 shows the frequency response of the two driver circuits. Figure 10 shows the transfer characteristics of the driver circuits. $V_{\text{in}}$ is the input voltage to the base of the transistor and $V_{\text{out}}$ is the output of the CR3424.

**SUMMARY**

The performance of a video amplifier can seriously affect CRT picture quality. Fast rise times and large output swing capabilities are essential. The CR3424 has more than enough speed and output swing to satisfy the needs of today's high resolution CRTs. To drive the CR3424 to its optimum performance, an input current profile must have the frequency response and peak currents as previously described. Two circuits, the emitter follower and the common emitter, are examples of circuits with the capability to drive the CR3424.
Considerations in Using The MHW801 and MHW851 Series RF Power Modules

by Norm Dye and Mike Shields
RF Products Division

INTRODUCTION
The MHW801/851 Series of power modules are designed primarily for applications in cellular portable radios. The -1 module is frequency compatible with the American system called AMPS; the -2 module is frequency compatible with the European TACS system; the -3 module is frequency compatible with the Scandanavian system called NMT; and the -4 module is frequency compatible with the NTACS system in Japan. Other than frequency of operation, all models of the MHW801 and MHW851 are identical and meet the general electrical specifications set forth on the data sheet. The only difference in the MHW801 and MHW851 Series of modules is the flange design. In the case of the MHW801, the flange does not extend any appreciable distance beyond the PCB substrate/cap and it is intended that mounting to a heatsink will be accomplished by attaching the flange to the heatsink with solder. The MHW801 modules are considered to be surface mount modules. The MHW851 modules were introduced to offer similar modules with the more conventional method of mounting. The flange extends beyond the substrate/cap and attachment to a heatsink is intended to be by means of mounting screws.

A significant amount of applications information is contained in the MHW801/MHW851 Series data sheet. Also included are a block diagram of the module and decoupling networks used in the test fixture; typical performance curves showing parameters such as $V_{\text{Cont}}$, efficiency, input VSWR and output power as functions of frequency; and output power and $V_{\text{Cont}}$ as functions of temperature.

GENERAL ELECTRICAL CONSIDERATIONS
Modules are matched to an impedance of 50 ohms for both input and output. Thus their application in a sub-system such as the transmitter portion of a portable radio is relatively straightforward. However, there are certain precautions that should be observed. First, it is important that DC inputs to the module be de-coupled by means of by-pass capacitors and/or chokes to prevent bias and power supply circuitry contributing to circuit instabilities (spurious oscillations). It is recommended that the module user pay careful attention to the decoupling information presented in the data sheet. Second, grounding of the module should be adequate to prevent low-level impedances that result in signal feedback with consequent module instabilities. Remember that the back of the circuit substrate is ground and this is soldered to the module flange which then becomes the ground connection to external circuitry. Third, the board layout should be such that isolation of input lines from output lines is at least 50 dB.

Normal use of the module is to amplify CW signals that are frequency modulated. The first two stages of the module are biased Class A; however, the last two stages are biased Class C. Significant distortion will result if the signal contains amplitude information, such as amplitude modulation. However, it is possible to operate the module in less than a CW condition. In a pulse mode of operation, any duty cycle up to 100% should create no problems provided the peak power does not exceed the rated CW output power of the module. Note, however, that case temperature can no longer be tied to die temperature by the same constant difference used for CW operation. The thermal time constant of the die is approximately 10 micro-seconds which says that for moderately long pulse trains with low duty cycles, die temperature could be much higher than that predicted from CW measurements.

The modules have not been characterized for pulse power operation. It is to be assumed that greater than rated CW output power can be obtained from the module in a pulse mode of operation; however, this is not recommended without first consulting the factory because of concern for maximum voltage swings as well as maximum die temperature.

NOISE CHARACTERISTICS
One parameter of power modules frequently not specified is noise. Most applications of power modules have been in radios where transmitting and receiving did not occur simultaneously. Today, cellular radios are duplexed, i.e., they are capable of transmitting and receiving at the same time. Thus radio manufacturers are concerned about the noise characteristics of the transmitter in the receive frequency band, which is normally 45 MHz above the transmit frequency. For this reason, Motorola has begun to characterize and guarantee noise performance of modules designed primarily for use in duplexed cellular radios.
Noise power for the MHW801/851 Series modules is guaranteed in a 30 kHz bandwidth, 45 MHz above $f_0$. This is shown visually in Figure 1. Note that the noise is specified for two widely different temperatures and for rated output power only. A characteristic of the MHW801/851 Series modules is that the small signal (noise) gain of the amplifier is approximately 35 dB at rated output power but increases by as much as 3 dB as the control voltage ($V_{\text{Cont}}$) is decreased.

The block diagram for noise measurements is shown in Figure 2. Several comments about the block diagram are in order. First, the signal source must be extremely low noise, as close to $kT\beta$ noise as possible. The HP8614A signal generator uses a cavity oscillator and satisfies the requirement of low noise. On the other hand, a frequency synthesized source such as the HP8656 (or Wavetek 2520A) signal generator does not. If this type of signal generator is used to make noise measurements, it is necessary to add a bandpass filter which will reject any signals 45 MHz above the output frequency.

![Figure 1. Noise Power In Receive Band](image1)

![Figure 2. Block Diagram For Sideband Noise Measurement](image2)
Remember that any noise at the input of the MHW801/851 Series module is amplified by approximately 35 dB. This noise amplification should not be confused with internally generated noise which could be caused by a high stage noise figure or by regeneration in one of the module stages, neither of which is a factor in the MHW801/851 Series module design.

Second, it is essential that the module be terminated in a circulator which will prevent out-of-band impedances of the subsequent RF network from affecting the stability (and, thus noise) of the module. Third, care must be taken to prevent the carrier frequency from saturating the input stages of the spectrum analyzer used to measure the noise level. Again, it is critical in accurate noise measurements to be certain that the sensitivity of the spectrum analyzer be at least 10 dB better than the noise level being measured.

Normally to accomplish this it is necessary to reduce the resolution bandwidth (RBW) of the spectrum analyzer to 30 kHz and set the video filter to 100 Hz bandwidth. The manufacturer (Hewlett Packard) of the spectrum analyzer recommends a video bandwidth 100 times less than the RBW for best noise averaging.

The filters, "H" and "G" (in Figure 2) are stagger tuned to obtain adequate selectivity for rejecting the carrier frequency at the input to the spectrum analyzer. Obviously a single filter can be used if it has a rejection level of approximately 60 dB, 45 MHz away from the bandpass of the filter. The actual rejection needed depends on whatever is required to prevent saturation of the spectrum analyzer by the carrier signal.

GAIN CONTROL

The data sheet recommends gain control by keeping input power at 0 dBm and varying the control voltage. Output power versus control voltage is shown in the typical characteristics of the data sheet. Gain control in the MHW801/851 Series module is obtained by controlling the bias to the Class A input stage as opposed to other modules that controls the voltage to Class C driver stages. The benefit of this method of control is significantly less control current and a lower slope of the output power versus control voltage curve.

It is possible to control output power from the module by controlling input power with the control voltage maintained at a fixed level (generally maximum). This is somewhat intuitive; however, a major benefit of this method for power output control may not be obvious. This benefit is the best noise performance of the module because the small signal gain is approximately 3 dB less at high control voltage as compared to low control voltage. Other important factors such as stability, input VSWR, harmonics, efficiency and load mismatch are essentially unaffected by the method of output power control.

OTHER CIRCUIT CONSIDERATIONS

Performance of the module at less than rated output power is sometimes of significance in typical module applications. Regardless of output power control, the noise characteristics, efficiency and harmonics will degrade at reduced output power. As output power is reduced, the Class C stages of the module operate further and further from their optimum load line resulting in significantly poorer efficiency. As their operation approaches the more non-linear region of the transistor transfer function, noise will likely increase and harmonics will increase with respect to carrier power. Generally these degradations in performance are not serious because they are relative to carrier power level. For example, efficiency becomes much less at output power levels of 100 mW, but current drain is much lower than for the case of 2 watts of output power, so this is generally not considered a problem in radio applications.

Other circuit considerations external to the module that are sometimes overlooked are source and load impedances. Note that the stability of the module is guaranteed only for source VSWR's of 3:1 and load VSWR's of 6:1. Frequently the load for the module is the transmit portion of a duplex filter. The out-of-band impedance presented by the filter can affect the stability of the module. The impedance reflected to the module depends on the length of transmission line between the module and the filter thereby causing line length to be an additional circuit consideration. It should be remembered that the MHW801/851 Series of modules are not unconditionally stable for all load and source impedances.

Out-of-band impedances of filters result in significantly high VSWR's at out-of-band frequencies. If these impedances are reflected to the module such that the module is terminated in impedances that lead to regions of instability, the module will oscillate.

Input power to the module can vary from a low value of 0 mW to a recommended maximum of 3 mW. Input powers greater than 3 mW are not recommended because of the potential damage that might result from overdriving the two final class C stages in the module. Overdrive results in excessive power dissipation particularly for the simultaneous condition of maximum supply voltage of 7.5 volts. Overdriving the final Class C stages can also lead to circuit instabilities because of changing impedances. Likewise, supply voltages greater than 7.5 volts should not be applied to the module for the same reasons of overdissipation and potential instabilities.

MOUNTING CONSIDERATIONS

GENERAL

In mounting power modules, consideration must be given to heat dissipation and grounding. Motorola specifies the range of case temperatures over which the module will perform safely. The upper temperature is determined by thermal resistances between each die and the case with the guideline that die temperature will be maintained below 200°C, which is considered a safe temperature for silicon transistors. All the user has to do is provide sufficient heat sinking for the module to be certain that the flange of the module does not exceed the maximum operating temperature rating. The maximum power dissipated by the module can be determined by determining the maximum DC power...
input less the RF power output. Another way to determine the maximum power to be dissipated is to divide the rated output power by the minimum efficiency and then subtract the rated output power.

Maximum power dissipation for either the MHW801 or MHW851 Series modules is 2.44 watts (2 Watts divided by .45 minus 2 Watts). This relatively small amount of power can normally be dissipated by minimal thermal contact between the flange of the module and the heatsink provided in the application. Calculations using the MHW851 module attached to a heatsink only at the mounting screws indicate that the rise in flange temperature (at center of flange) above the temperature at the ends of the flange should not exceed 10°C.

Grounding the module to external circuitry through mounting screws only should be adequate to prevent spurious oscillations provided the ground contact does not become excessively resistive as a result of nickel oxide forming on the nickel plated flange. Nickel oxide (unlike copper and silver oxide) is resistive and its formation can lead to intermittent ground paths between the module and external circuits.

MHW801 Series

MHW801 modules are designed without "ears" on the flange. They should be attached to a heatsink with solder. When soldering, the primary consideration should be to prevent any part of the module flange from achieving a temperature greater than 165°C. A low temperature solder such as 52% In and 48% Sn (along with "R" type flux) is recommended because this solder liquifies below 150°C. Keep in mind that the internal construction of the module has been achieved using 36% Sn, 62% Pb and 2% Ag solder which liquifies at 179–180°C. If the module flange is allowed to achieve a temperature greater than 165°C, serious mechanical damage could occur with consequent failure to function electrically being the end result. Also, as stated on the data sheet, do not permit the module to be immersed in a flux removal system. The part is not hermetically sealed, and liquids could penetrate into the circuitry with potentially disastrous results.

MHW851 Series

MHW851 type modules have flanges with "ears" for attachment to a heatsink by means of screws. The cutouts at each end of the flange will accommodate 4–40 screws and these should be torqued to an amount no greater than 2 to 3 inch-pounds. The use of thermal grease is not recommended for the MHW851 Series module because the relatively low output power does not require intimate (thermal) contact of the flange surface to the heatsink. Use of thermal grease is permissible but care must be taken to prevent using an excessive amount. Since it is not needed, it is Motorola's recommendation that it not be used.

Flatness of the heatsink when using MHW851's is much less critical than that required for higher power modules. Motorola recommends that the heatsink surface be flat to within + or − 0.003 inches, a dimension that should be relatively easy to attain. The MHW801/851 Series module is constructed with a printed circuit board substrate which negates the stringent requirements for bending that are placed on ceramic substrate modules. Motorola believes that the MHW801/851 Series module can be distorted as much as 0.020 inches either concave or convex without damage to the module.

Because bending requirements are relaxed, it is also unnecessary to worry about tightening sequence as described in EB107 — "Mounting Considerations for Motorola RF Power Modules." This EB was written primarily for ceramic substrate modules and does not apply in total to printed circuit board substrate modules such as the MHW801/851 Series.
Understanding RF Data Sheet Parameters
by Norman E. Dye
RF Products Division

INTRODUCTION

Data sheets are often the sole source of information about the capability and characteristics of a product. This is particularly true of unique RF semiconductor devices that are used by equipment designers all over the world. Because the circuit designer often cannot talk directly with the factory, he relies on the data sheet for his device information. And for RF devices, many of the specifications are unique in themselves. Thus it is important that the user and the manufacturer of RF products speak a common language, i.e., what the semiconductor manufacturer says about his RF device is understood fully by the circuit designer.

This paper reviews RF transistor and amplifier module parameters from maximum ratings to functional characteristics. It is divided into 5 basic sections: 1) DC Specifications, 2) Power Transistors, 3) Low Power Transistors, 4) Power Modules and 5) Linear Modules. Comments are made about critical specifications, about how values are determined and what are their significance. A brief description of the procedures used to obtain impedance data and thermal data is set forth; the importance of test circuits is elaborated; and background information is given to help understand low noise considerations and linearity requirements.

DC SPECIFICATIONS

Basically RF transistors are characterized by two types of parameters: DC and functional. The "DC" specs consist (by definition) of breakdown voltages, leakage currents, hFE (DC beta) and capacitances, while the functional specs cover gain, ruggedness, noise figure, Zin and Zout, S-parameters, distortion, etc. Thermal characteristics do not fall cleanly into either category since thermal resistance and power dissipation can be either DC or AC. Thus, we will treat the spec of thermal resistance as a special specification and give it its own heading called "thermal characteristics." Figure 1 is one page of a typical RF power data sheet showing DC and functional specs.

A critical part of selecting a transistor is choosing one that has breakdown voltages compatible with the supply voltage available in an intended application. It is important that the design engineer select a transistor on the one hand that has breakdown voltages which will NOT be exceeded by the DC and RF voltages that appear across the various junctions of the transistor and on the other hand has breakdown voltages that permit the "gain at frequency" objectives to be met by the transistor. Mobile radios normally operate from a 12 volt source; portable radios use a lower voltage, typically 6 to 9 volts; avionics applications are commonly 28 volt supplies while base station and other ground applications such as medical electronics generally take advantage of the superior performance characteristics of high voltage devices and operate with 24 to 50 volt supplies. In making a transistor, breakdown voltages are largely determined by material resistivity and junction depths (Figure 2). It is for these reasons that breakdown voltages are intimately entwined with functional performance characteristics. Most product portfolios in the RF power transistor industry have families of transistors designed for use at specified supply voltages such as 7.5 volts, 12.5 volts, 28 volts and 50 volts.

Leakage currents (defined as reverse biased junction currents that occur prior to avalanche breakdown) are likely to be more varied in their specification and also more informative. Many transistors do not have leakage currents specified because they can result in excessive (and frequently unnecessary) wafer/die yield losses. Leakage currents arise as a result of material defects, mask imperfections and/or undesired impurities that enter during wafer processing. Some sources of leakage currents are potential reliability problems; most are not. Leakage currents can be material related such as stacking faults and dislocations or they can be "pipes" created by mask defects and/or processing inadequacies. These sources result in leakage currents that are constant with time and if initially acceptable for a particular application will remain so. They do not pose long term reliability problems.

On the other hand, leakage currents created by channels induced by mobile ionic contaminants in the oxide (primarily sodium) tend to change with time and can lead to increases in leakage current that render the device useless for a specific application. Distinguishing between sources of leakage current can be difficult, which is one reason devices for application in military environments require HTRB (high temperature reverse bias) and burn-in testing. However, even for commercial applications particularly where battery drain is critical or where bias considerations dictate limitations, it is essential that a leakage current limit be included in any complete device specification.
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)</td>
<td>V(BR)CEO</td>
<td>16</td>
<td></td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_BE = 0)</td>
<td>V(BR)CES</td>
<td>36</td>
<td></td>
<td></td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)</td>
<td>V(BR)EBO</td>
<td>4.0</td>
<td></td>
<td></td>
<td>Vdc</td>
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<tr>
<td>Collector Cutoff Current (V_CE = 15 Vdc, V_BE = 0, T_C = 25°C)</td>
<td>I_CES</td>
<td></td>
<td>10</td>
<td></td>
<td>mAdc</td>
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<td></td>
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<tr>
<td>DC Current Gain (I_C = 4.0 Adc, V_CE = 5.0 Vdc)</td>
<td>hFE</td>
<td>20</td>
<td>70</td>
<td>150</td>
<td>—</td>
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<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
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<tr>
<td>Output Capacitance</td>
<td>C_0b</td>
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<td>90</td>
<td>125</td>
<td>pF</td>
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<tr>
<td>(V_CB = 12.5 Vdc, I_E = 0, f = 1.0 MHz)</td>
<td></td>
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<tr>
<td><strong>FUNCTIONAL TESTS</strong></td>
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<tr>
<td>Common Emitter Amplifier Power Gain</td>
<td>G_pe</td>
<td>4.8</td>
<td>5.4</td>
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<td>dB</td>
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<tr>
<td>(V_CC = 12.5 Vdc, P_out = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)</td>
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<tr>
<td>Input Power</td>
<td>P_in</td>
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<td>13</td>
<td>15</td>
<td>Watts</td>
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<tr>
<td>(V_CC = 12.5 Vdc, P_out = 45 W, f = 470 MHz)</td>
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<tr>
<td>Collector Efficiency</td>
<td>6</td>
<td>55</td>
<td>60</td>
<td></td>
<td>%</td>
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<tr>
<td>(V_CC = 12.5 Vdc, P_out = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Load Mismatch Stress</td>
<td>2</td>
<td>55</td>
<td>60</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>(V_CC = 16 Vdc, P_in = Note_1, f = 470 MHz, VSWR = 20:1, All Phase Angles)</td>
<td></td>
<td></td>
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<tr>
<td>Series Equivalent Input Impedance</td>
<td>Z_in</td>
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<td>1.4</td>
<td>4.0</td>
<td>Ohms</td>
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<td>(V_CC = 12.5 Vdc, P_out = 45 W, f = 470 MHz)</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Series Equivalent Output Impedance</td>
<td>Z_OL*</td>
<td></td>
<td>1.2</td>
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<td>Ohms</td>
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<tr>
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<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Notes:
1. P_in = 150% of Drive Requirement for 45 W output @ 12.5 V
2. 2 = Mismatch stress factor — the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated with a 20:1 minimum load mismatch at all phase angles.

Figure 1. Typical DC and Functional Specifications

Figure 2. The Effect of Curvature and Resistivity on Breakdown Voltage
DC parameters such as $h_{FE}$ and $C_{OB}$ (output capacitance) need little comment. Typically, for RF devices, $h_{FE}$ is relatively unimportant because the functional parameter of gain at the desired frequency of operation is specified. Note, though, that DC beta is related to AC beta (Figure 3). Functional gain will track DC beta particularly at lower RF frequencies. Generally RF device manufacturers do not like to have tight limits placed on $h_{FE}$. Primarily the reasons that justify this position are:

a) Lack of correlation with RF performance
b) Difficulty in control in wafer processing
c) Other device manufacturing constraints dictated by functional performance specs which preclude tight limits for $h_{FE}$.

A good rule of thumb for $h_{FE}$ is to set a maximum-to-minimum ratio of not less than 3 and not more than 4 with the minimum $h_{FE}$ value determined by an acceptable margin in functional gain.

The value of $V_{(BR)CEO}$ is sometimes misunderstood. Its value can approach or even equal the supply voltage rating of the transistor. The question naturally arises as to how such a low voltage can be used in practical applications. First, $V_{(BR)CEO}$ is the breakdown voltage of the collector-base junction plus the forward drop across the base-emitter junction with the base open, and it is never encountered in amplifiers where the base is at or near the potential of the emitter. That is to say, most amplifiers have the base shorted or they use a low value of resistance such that the breakdown value of interest approaches $V_{(BR)CES}$. Second, $V_{(BR)CEO}$ involves the current gain of the transistor and increases as frequency increases. Thus the value of $V_{(BR)CEO}$ at RF frequencies is always greater than the value at DC.

The maximum rating for power dissipation ($P_{D}$) is closely associated with thermal resistance ($\Theta_{JC}$). Actually maximum $P_{D}$ is in reality a fictitious number — a kind of figure of merit — because it is based on the assumption that case temperature is maintained at 25°C. However, providing everyone arrives at the value in a similar manner, the rating of maximum $P_{D}$ is a useful tool with which to compare devices.

The rating begins with a determination of thermal resistance — die to case. Knowing $\Theta_{JC}$ and assuming a maximum die temperature, one can easily determine maximum $P_{D}$ (based on the previously stated case temperature of 25°C). Measuring $\Theta_{JC}$ is normally done by monitoring case temperature ($T_{C}$) of the device while it operates at or near rated output power ($P_{O}$) in an RF circuit. The die temperature ($T_{J}$) is measured simultaneously using an infra-red microscope (see Figure 6) which has a spot size resolution as small as 1 mil in diameter. Normally several readings are taken over the surface of the die and an average value is used to specify $T_{J}$.

It is true that temperatures over a die will vary typically 10–20°C. A poorly designed die (improper ballasting) could result in hot spot (worst case) temperatures that vary 40–50°C. Likewise, poor die bonds (see Figure 7) can result in hot spots but these are not normal characteristics of a properly designed and assembled transistor die.
The RF Line
NPN Silicon
RF Power Transistor

...designed for 12.5 Volt Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 520 MHz.

- Guaranteed 440, 470, 512 MHz 12.5 Volt Characteristics
  - Output Power = 50 Watts
  - Minimum Gain = 5.2 dB @ 440, 470 MHz
  - Efficiency = 55% @ 440, 470 MHz
  - IRL = 10 dB
- Characterized with Series Equivalent Large-Signal Impedance Parameters from 400 to 520 MHz
- Built-In Matching Network for Broadband Operation
- Triple Ion Implanted for More Consistent Characteristics
- Implanted Emitter Ballast Resistors
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 15.5 Vdc, 2.0 dB Overdrive

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
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<tr>
<td>Collector-Emitter Voltage</td>
<td>VCEO</td>
<td>16.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Emitter Voltage</td>
<td>VCES</td>
<td>38</td>
<td>Vdc</td>
</tr>
<tr>
<td>Emitter-Base Voltage</td>
<td>VEBQ</td>
<td>4.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>Collector-Current — Continuous</td>
<td>IC</td>
<td>12</td>
<td>Adc</td>
</tr>
<tr>
<td>Total Device Dissipation @ TC = 25°C</td>
<td>PD</td>
<td>135</td>
<td>Watts</td>
</tr>
<tr>
<td>Derate above 25°C</td>
<td>PDER</td>
<td>0.77</td>
<td>W/C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>TSTG</td>
<td>-65 to +150</td>
<td>°C</td>
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THERMAL CHARACTERISTICS

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<thead>
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<th>Characteristic</th>
<th>Symbol</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>RJC</td>
<td>1.3</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Figure 5. Maximum Ratings of a Typical RF Power Transistor

By measuring TC and TJ along with PO and PIN — both DC and RF — one can calculate θJC from the formula θJC = (TJ - TC)/(PIN - PO). Typical values for an RF power transistor might be TJ = 130°C; TC = 50°C; VCE = 12.5 V; IC = 12 A; Pin (RF) = 10 W; PO (RF) = 50 W. Thus θJC = (130 - 50)/(10 + (12.5 x 12) - 30) = 80/80 = 1°C/W.

Several reasons dictate a conservative value be placed on θJC. First, thermal resistance increases with temperature (and we realize TC = 25°C is NOT realistic). Second, TJ is not a worst case number. And, third, by using a conservative value of θJC, a realistic value is determined for maximum PD. Generally, Motorola's practice is to publish θJC numbers approximately 25% higher than that determined by the measurements described in the preceding paragraphs, or for the case illustrated, a value of θJC = 1.25°C/W.

Now a few words are in order about die temperature. Reliability considerations dictate a safe value for an all Au (gold) system (die top metal and wire) to be 200°C. Once TJ max is determined, along with a value for θJC, maximum PD is simply

PD (max) = (TJ (max) - 25°C)/θJC.

Specifying maximum PD for TC = 25°C leads to the necessity to derate maximum PD for any value of TC above 25°C. The derating factor is simply the reciprocal of θJC! Maximum collector current (IC) is probably the most subjective maximum rating on the transistor data sheets. It has
been, and is, determined in a number of ways each leading to different maximum values. Actually, the only valid maximum current limitations in an RF transistor have to do with the current handling ability of the wires or the die. However, power dissipation ratings may restrict current to values far below what should be the maximum rating. Unfortunately, many older transistors had their maximum current rating determined by dividing maximum PD by collector voltage (or be V(BR)CEO for added safety) but this is not a fundamental maximum current limitation of the part. Many lower frequency parts have relatively gross top metal on the transistor die, i.e., wide metal runners and the "weak current link" in the part is the current handling capability of the emitter wires (for common emitter parts). The current handling ability of wire (various sizes and material) is well known; thus the maximum current rating may be limited by the number, size and material used for emitter wires.

Most modern, high frequency transistors are die limited because of high current densities resulting from very small current carrying conductors and these densities can lead to metal migration and premature failure. The determination of IC max for these types of transistors results from use of Black's equation for metal migration which determines a mean time between failures (MTBF) based on current density, temperature and type of metal. At Motorola, MTBF is generally set at >7 years and maximum die temperature at 200°C. For plastic packaged transistors, maximum TJ is set at 150°C. The resulting current density along with a knowledge of the die geometry and top metal thickness and material allows the determination of IC max for the device.

It is up to the transistor manufacturer to specify an IC max based on which of the two limitations (die, wire) is paramount. It is recommended that the circuit design engineer consult the semiconductor manufacturer for additional information if IC max is of any concern in his specific use of the transistor.

Storage temperature is another maximum rating that is frequently not given the attention it deserves. A range of -55°C to 200°C has become more or less an industry standard. And for the single metal, hermetic packaged type of device, the upper limit of 200°C creates no reliability problems. However, a lower high temperature limitation exists for plastic encapsulated or epoxy sealed devices. These should not be subjected to temperatures above 150°C to prevent deterioration of the plastic material.

POWER TRANSISTORS —

Functional Characteristics

The selection of a power transistor usually involves choosing one for a frequency of operation, a level of output power, a desired gain, a voltage of operation and preferred package configuration consistent with circuit construction techniques.

Functional characteristics of an RF power transistor are by necessity tied to a specific test circuit (an example is shown in Figure 8). Without specifying a circuit, the functional parameters of gain, reflected power, efficiency — even ruggedness — hold little meaning. Furthermore, most test circuits used by RF transistor manufacturers today (even those used to characterize devices) are designed mechanically to allow for easy insertion and removal of the device under test (D.U.T.). This mechanical restriction sometimes limits achievable device performance which explains why performance by users frequently exceeds that indicated in data sheet curves. On the other hand, a circuit used to characterize a device is usually narrow band and tunable. This results in higher gain than attainable in a broadband circuit. Unless otherwise stated, it can be assumed that characterization data such as PO vs frequency is generated on a point-by-point basis by tuning a narrow band circuit across a band of frequencies and, thus, represents what can be achieved at a specific frequency of interest provided the circuit presents optimum source and load impedances to the D.U.T.

Broadband, fixed tuned test circuits are the most desirable for testing functional performance of an RF transistor. Fixed tuned is particularly important in assuring everyone — the manufacturer and the user — of product consistency, i.e., that devices manufactured tomorrow will be identical to devices manufactured today.

Tunable, narrow band circuits have led to the necessity for device users and device manufacturers to resort to the use of "correlation units" to assure product consistency over
a period of time. Fixed tuned circuits minimize (if not elimi­
nate) the requirements for correlation and in so doing tend to compensate for the increased constraints they place on the device manufacturer. On the other hand, manufacturers like tunable test circuits because their use allows adjustments that can compensate for variations in die fabrication and/or device assembly. Unfortunately gain is normally less in a broadband circuit that it is in a narrow band circuit, and this fact frequently forces transistor manufacturers to use narrow band circuits to make their product have sufficient attraction when compared with other similar devices made by competi­
tors. This is called "specsmanship." One compromise for the transistor manufacturer is to use narrow band circuits with all tuning adjustments "locked" in place. For all of the above reasons, then, in comparing functional parameters of two or more devices, the data sheet reader should observe carefully the test circuit in which specific parameter limits are guaran­
teed.

For RF power transistors, the parameter of ruggedness takes on considerable importance. Ruggedness is the character­
istic of a transistor to withstand extreme mismatch conditions in operation (which causes large amounts of output power to be "dumped back" into the transistor) without altering its performance capability or reliability. Many circuit environments particularly portable and mobile radios have limited control over the impedance presented to the power amplifier by an antenna, at least for some duration of time. In portables, the antenna may be placed against a metal surface; in mobiles, perhaps the antenna is broken off or inadvertently disconnected from the radio. Today’s RF power transistor must be able to survive such load mismatches without any effect on subsequent operation. A truly realistic possibility for mobile radio transistors (although not a normal situation) is the condition whereby an RF power device "sees" a worst case load mismatch (an open circuit, any phase angle) along with maximum VCC AND greater than normal input drive — all at the same time. Thus the ultimate test for ruggedness is to subject a transistor to a test wherein Pin (RF) is increased up to 50% above that value necessary to create rated P0; VCC is increased about 25% (12.5 V to 16 V for mobile transistors) AND then the load reflection coefficient is set at a magnitude of unity while its phase angle is varied through all possible values from 0 degrees to 360 degrees. Many 12 volt (land mobile) transistors are routinely given this test at Motorola Semiconductors by means of a test station similar to the one shown in Figure 9.

Ruggedness specifications come in many forms (or guises). Many older devices (and even some newer ones) simply have NO ruggedness spec. Others are said to be "capable of" withstanding load mismatches. Still others are guaranteed to withstand load mismatches of 2:1 VSWR to 3:1 VSWR at rated output power. A few truly rugged transis­
tors are guaranteed to withstand 30:1 VSWR at all phase angles (for all practical purposes 30:1 VSWR is the same as 3:1 VSWR) with both over voltage and over drive. Once again it is up to the user to match his circuit requirements against device specifications.

Then as if the whole subject of ruggedness is not sufficiently confusing, the semiconductor manufacture slips in the ultimate "muddy the water" condition in stating what consti­
tutes passing the ruggedness test. The words generally say that after the ruggedness test the D.U.T. "shall have no degradation in output power." A better phrase would be "no measurable change in output power." But even this is not the best. Unfortunately the D.U.T. can be "damaged" by the ruggedness test and still have "no degradation in output power." Today’s RF power transistors consist of up to 1K or more low power transistors connected in parallel. Emitter resistors are placed in series with groups of these transistors in order to better control power sharing throughout the transistor die. It is well known by semiconductor manufactur­
ers that a high percentage of an RF power transistor die (say up to 25–30%) can be destroyed with the transistor still able to deliver rated power at rated gain, at least for some period of time. If a ruggedness test destroys a high percentage of cells in a transistor, then it is likely that a 2nd ruggedness test (by the manufacturer or by the user while in his circuit) would result in additional damage leading to premature device failure.

A more scientific measurement of "passing" or "failing" a ruggedness test is called ΔVRE — the change in emitter
resistance before and after the ruggedness test. $V_{RE}$ is
determined to a large extent by the net value of emitter
resistance in the transistor die. Thus if cells are destroyed,
emitter resistance will change with a resultant change in $V_{RE}$.
Changes as small as 1% are readily detectable, with 5% or
less normally considered an acceptable limit. Today’s more
sophisticated device specifications for RF power transistors
use this criteria to determine “success” or “failure” in rugged-
ness testing.

A circuit designer must know the input/output characteris-
tics of the RF power transistor(s) he has selected in order
to design a circuit that “matches” the transistor over the
frequency band of operation. Data sheets provide this infor-
mation in the form of large signal impedance parameters,
$Z_{IN}$ and $Z_{OUT}$ (commonly referred to as $Z_{OL}$). Normally,
these are stated as a function of frequency and are plotted
on a Smith Chart and/or given in tabular form. It should be
noted that $Z_{IN}$ and $Z_{OUT}$ apply only for a specified set of
operating conditions, i.e., $P_{0}$, $V_{CC}$ and frequency. Both $Z_{IN}$
and $Z_{OUT}$ of a device are determined in a similar way, i.e.,
place the D.U.T. in a tunable circuit and tune both input and
output circuit elements to achieve maximum gain for the
desired set of operating conditions. At maximum gain, D.U.T.
impedances will be the conjugate of the input and output
network impedances. Thus, terminate the input and output
ports of the test circuit, remove the device and measure $Z$
looking from the device — first, toward the input to obtain
the conjugate of $Z_{IN}$ and, second, toward the output to obtain
$Z_{OL}$ which is the output load required to achieve maximum
$P_{0}$

A network analyzer is used in the actual measurement
process to determine the complex reflection coefficient of the
circuit using, typically, the edge of the package as a plane
of reference. A typical measurement setup is shown in Figure
10. Figure 11 shows the special fixture used to obtain the
short circuit reference while Figure 12 illustrates the adapter
which allows the circuit impedance to be measured from the
edge of the package.

**Figure 10. The HP Network Analyzer**

Once the circuit designer knows $Z_{IN}$ and $Z_{OL}$ of the
transistor as a function of frequency, he can use computer
aided design programs to design L and C matching networks
for his particular application.

The entire impedance measuring process is somewhat
laborious and time consuming since it must be repeated for
each frequency of interest. Note that the frequency range
permitted for characterization is that over which the circuit
will tune. For other frequencies, additional test circuits must
be designed and constructed, which explains why it is some-
times difficult to get a semiconductor manufacturer to supply
impedance data for special conditions of operation such as
different frequencies, different power levels or different oper-
ating voltages.

**LOW POWER TRANSISTORS —
Functional Characteristics**

Most semiconductor manufacturers characterize low pow-
er RF transistors for linear amplifier and/or low noise amplifier
applications. Selecting a proper low power transistor involves
choosing one having an adequate current rating, in the “right”
package and with gain and noise figure capability that meets
the requirements of the intended application.

One of the most useful means of specifying a linear device
is by means of scattering parameters, commonly referred to
as S-Parameters which are in reality voltage reflection and
transmission coefficients when the device is embedded into a 50 ohm system. See Figure 13. $|S_{11}|$, the magnitude of the input reflection coefficient is directly related to input VSWR by the equation $VSWR = (1 + |S_{11}|) / (1 - |S_{11}|)$. Likewise, $|S_{22}|$, the magnitude of the output reflection coefficient is directly related to output VSWR. $|S_{21}|^2$, which is the square of the magnitude of the input-to-output transfer function, is also the power gain of the device. It is referred to on data sheets as "Insertion Gain." Note, however, that $|S_{21}|^2$ is the power gain of the device when the source and load impedances are 50 ohms. An improvement in gain can always be achieved by matching the device's input and output impedances (which are almost always different from 50 ohms) to 50 ohms by means of matching networks. The larger the linear device, the lower the impedances and the greater is the need to use matching networks to achieve useful gain.

![Figure 13. Two-Port S-Parameter Definitions](image)

Another gain specification shown on low power data sheets is called "Associated Gain." The symbol used for Associated Gain is $G_{NF}$. It is simply the gain of the device when matched for minimum noise figure. Yet another gain term is shown on some data sheets and it is called "Maximum Unilateral Gain." It's symbol is $G_{U\max}$. As you might expect, $G_{U\max}$ is the gain achievable by the transistor when the input and output are conjugately matched for maximum power transfer (and $S_{12} = 0$). One can derive a value for $G_{U\max}$ using scattering parameters:

$$G_{U\max} = |S_{21}|^2 / (1 - |S_{11}|^2 (1 - |S_{22}|^2)).$$

Simply stated, this is the 50 ohm gain increased by a factor which represents matching the input and increased again by a factor which represents matching the output.

Many RF low power transistors are used as low noise amplifiers which has led to several transistor data sheet parameters related to noise figure. $NF_{\min}$ is defined as the minimum noise figure that can be achieved with the transistor. To achieve this $NF$ requires source impedance matching which is usually different from that required to achieve maximum gain. The design of a low noise amplifier, then, always a compromise between gain and $NF$. A useful tool to aid in this compromise is a Smith Chart plot of constant gain and Noise Figure contours which can be drawn for specific operating conditions — typically bias and frequency. A typical Smith Chart plot showing constant gain and $NF$ contours is shown in Figure 14. These contours are circles which are either totally or partially complete within the confines of the Smith Chart. If the gain circles are contained entirely within the Smith Chart, then the device is unconditionally stable. If portions of the gain circles are outside the Smith Chart, then the device is considered to be "conditionally stable" and the device designer must concern himself with instabilities, particularly outside the normal frequency range of operation.

If the data sheet includes Noise Parameters, a value will be given for the optimum input reflection coefficient to achieve minimum noise figure. Its symbol is $\Gamma_0$ or sometimes $\Gamma_{opt}$. But remember if you match this value of input reflection coefficient you are likely to have far less gain than is achievable by the transistor. The input reflection coefficient for maximum gain is normally called $\Gamma_{M\max}$, while the output reflection coefficient for maximum gain is normally called $\Gamma_{M\min}$.

Another important noise parameter is noise resistance which is given the symbol $R_N$ and is expressed in ohms. Sometimes in tabular form, you may see this value normalized to 50 ohms in which case it is designated $r_N$. The significance of $r_N$ can be seen in the formula below which determines noise figure $NF$ of a transistor for any source reflection coefficient $\Gamma_S$ if the three noise parameters —
NF_{\text{min}}, r_n and \Gamma_0 (the source resistance for minimum noise figure) — are known. Typical noise parameters taken from the MRF942 data sheet are shown in Figure 15.

NF = NF_{\text{min}} + \left(4r_n |\Gamma_S - \Gamma_0|^2 / \left(1 - |\Gamma_S|^2\right) \right) |1 + \Gamma_0|^2$.

The locus of points for a given NF turns out to be a circle (the NF_{\text{min}} circle being a point); thus, by choosing different values of NF one can plot a series of noise circles on the Smith Chart. Incidentally, r_n can be measured by measuring noise figure for \Gamma_S = 0 and applying the equation stated above.

<p>| MRF942 |
|---|---|---|---|---|---|---|</p>
<table>
<thead>
<tr>
<th>V_{\text{CE}} (Vdc)</th>
<th>\Gamma_0 (\text{MAG, ANG})</th>
<th>R_N (ohms)</th>
<th>NF_{50} \Omega (dB)</th>
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<tr>
<td>6</td>
<td>16</td>
<td>17.5</td>
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<td>15.5</td>
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<td>4.3</td>
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<tr>
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<td>10.5</td>
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</table>

Figure 14. Gain & Noise Figure Contours

A parameter found on most RF low power data sheets is commonly called the current gain-bandwidth product. Its symbol is \( f_T \). Sometimes it is referred to as the cutoff frequency because it is generally thought to be the product of low frequency current gain and the frequency at which the current gain becomes unity. While this is not precisely true (see Figure 16), it is close enough for practical purposes. And it is true that \( f_T \) is an excellent figure-of-merit which becomes useful in comparing devices for gain and noise figure capability. High values of \( f_T \) are normally required to achieve higher gain at higher frequencies, other factors being equal. To the device designer, high \( f_T \) mean decreased spacings between emitter and base diffusions and it means shallower diffusions — things which are more difficult to achieve in making an RF transistor.

The complete RF low power transistor data sheet will include a plot of \( f_T \) versus collector current. Such a curve (as shown in Figure 17) will increase with current, flatten and then begin to decrease as \( I_C \) increases thereby revealing useful information about the optimum current with which to achieve maximum device gain.

Another group of characteristics associated with linear (or Class "A") transistors has to do with the degree to which the device is linear. Most common are terms such as \( P_{\text{O1 dB Gain Compression Point}} \) and \( 3\text{rd Order Intercept Point (or ITO as it is sometimes called)} \). More will be said about
FUNCTIONAL CHARACTERISTICS

The importance of the "1 dB Gain Compression Point" is that this is generally accepted as the limit of non-linearity that is tolerable in a "linear" amplifier and leads one to the dynamic range of the low power amplifier. The concept of gain compression is illustrated in Figure 18. The frequency band requirements of a CATV amplifier are determined by the number of channels used in the CATV system. Each channel requires 6 MHz bandwidth (to handle conventional color TV signals). Currently available models in the industry have bandwidths extending from 40 to 550 MHz and will accommodate up to 77 channels, the center

Figure 18. Linear Gain and 1 dB Compression Point

high end of dynamic range is the limit imposed by "gain compression."

LINEAR MODULES — Functional Characteristics

Let's turn now to amplifiers and examine some specifications encountered that are unique to specific applications. Amplifiers intended for cable television applications are selected to have the desired gain and distortion characteristics compatible with the cable network requirements. They are linear amplifiers consisting of 2 or more stages of gain each using a push-pull cascade configuration. Remember that a cascade stage is one consisting of 2 transistors in which a common emitter stage drives a common base stage. A basic circuit configuration is shown in Figure 19. Most operate from a standard voltage of 24 volts and are packaged in an industry standard configuration shown in Figure 20. Because they are used to "boost" the RF signals that have been attenuated by the losses in long lengths of coaxial cable (the losses of which increase with frequency), their gain characteristics as a function of frequency are very important. These are defined by the specifications of "slope" and "flatness" over the frequency band of interest. Slope is defined simply as the difference in gain at the high and low end of the frequency band of the amplifier. Flatness, on the other hand, is defined as the deviation (at any frequency in the band) from an ideal gain which is determined theoretically by a universal cable loss function. Motorola normally measures the peak-to-valley (high-to-low) variations in gain across the frequency band, but specifies the flatness as a "plus, minus" quantity because it is assumed that cable television system designers have the capability of adjusting overall gain level.

The frequency band requirements of a CATV amplifier are determined by the number of channels used in the CATV system. Each channel requires 6 MHz bandwidth (to handle conventional color TV signals). Currently available models in the industry have bandwidths extending from 40 to 550 MHz and will accommodate up to 77 channels, the center
frequencies of which are determined by industry standard frequency allocations.

Because CATV amplifiers must amplify TV signals and they must handle many channels simultaneously, these amplifiers must be extremely linear. The more linear, the less distortion that is added to the signal and, thus, the better is the quality of the TV picture being viewed. Distortion is generally specified in 3 conventional ways — 2nd Order Intermodulation Distortion (IMD), Cross Modulation Distortion (XMD) and Composite Triple Beat (CTB). In order to better understand what these terms mean, a few words need to be said about distortion in general.

First, let's consider a perfectly linear amplifier. The output signal is exactly the same as the input except for a constant gain factor. Unfortunately, transistor amplifiers are, even under the best of circumstances, not perfectly linear. If one were to write a transfer function for a transistor amplifier, a typical input-output curve for which is shown in Figure 21, he would find the region near zero to be one best represented by “squared” terms, i.e., the output is proportional to the square of the input. And the region near saturation, i.e., where the amplifier produces less incremental output for incremental increases in input is best represented by “cubed” terms, i.e., the output is proportional to the cube of the input. A mathematically rigorous analysis of the transfer function of an amplifier would include an infinite number of higher order terms. However, an excellent approximation is obtained by considering the first three terms, i.e., make the assumption we can write

\[ F(x) = C_1x + C_2x^2 + C_3x^3, \]

where \( F \) is the output signal and \( x \) is the input signal. \( C_1, C_2 \) and \( C_3 \) are constants that represent the transfer function (gain) for the first, second and third order terms.

Now consider a relatively simple input signal consisting of 3 frequencies each having a constant amplitude \( A \). (In the case of CATV amplifiers, there could be 50–60 channels each having a carrier frequency and associated modulation frequencies spread over a bandwidth approaching 6 MHz.) The input signal \( x \) then equals \( Acos\omega_1t + Acos\omega_2t + Acos\omega_3t \).

If we apply this input signal to the transfer function and calculate \( F(x) \), we will find many terms involving \( x, x^2 \) and \( x^3 \). The “\( x \)” terms represent the “perfect”, linear amplification of the input signal. Terms involving \( x^2 \) when analyzed on a frequency basis result in signal components at two times the frequencies of \( f_1, f_2 \) and \( f_3 \). Also created by \( x^2 \) terms are signal components at sums and difference frequencies of all combinations of \( f_1, f_2 \) and \( f_3 \). These are called 2nd order intermodulation components. Likewise, the terms involving \( x^3 \) result in frequency components at three times the frequencies of \( f_1, f_2 \) and \( f_3 \). And there are also frequency components at sum and difference frequencies (these are called 3rd order IMD). But in addition there are frequency components at \( f_1 +,- f_2 +,- f_3 \). These are called “triple beat” terms. And this is not all! A close examination reveals additional amplitude components at the original frequencies of \( f_1, f_2 \) and \( f_3 \). These terms can both “enhance” gain (expansion) or “reduce” gain (compression). The amplitude of these expansion and compression terms are such that we can divide the group of terms into two categories — “self-expansion/compression” and “cross-expansion/compression.”

Self-expansion/compression terms have amplitudes determined by the amplitude of a single frequency while cross-expansion/compression terms have amplitudes determined by the amplitudes of two frequencies. A summary of the terms that exist in this “simple” example is given in Table 1.
on a log-log scale (or dB/dB scale) will be a straight line with
temperatures that are proportional to the cube of the input signal
level. Hence, it can be concluded that a plot of each response
change in 2nd order distortion; however, a 1 dB change in
3rd order is a· slope of 2. That is to say, for 2nd order
distortion, a 1 dB change in signal level results in a 1 dB
change in 2nd order is a slope of 1 and between fundamental and
2nd order the slope corresponding to the order of the response. Funda­
mental responses will have a slope of 1, the 2nd order
responses will have a slope of 2 and the 3rd order responses
will have the same value unless circuits are used that
suppress even-order spurious responses, etc. However,
include the concept of "intercept point" is that once you know the intercept point, you can
determine the value of distortion for any signal level —
provided you are in a region of operation governed by the
mathematical relationships stated, which typically means
IMD’s greater than 60 dB below the carrier.
Likewise to determine 3rd order intercept point, one must
measure 3rd order distortion at a known signal level. Then
take half the value of the distortion (expressed in dBc) and
add to the signal level. For example, if the signal level is
+10 dBm and the 3rd order distortion is +40 dBc, the 3rd
order intercept point is the same as the 2nd order intercept
point or +10 dBm + 30 dB = 40 dBm. Both 2nd order and 3rd
order intercept points are illustrated in Figure 22 using the
values assumed in the preceding examples. Note, also, that
in general the intercept point for 2nd and 3rd order distortion
will have the same value unless circuits are used that
suppress even-order spurious responses, etc. However,
even in this situation the concept of intercept point is still valid;
the slopes of the responses are still 1, 2 and 3 respectively
and all that needs to be done is to specify a 2nd order
intercept point different from the 3rd order intercept point.

With this background information, let's turn to specific
distortion specifications listed on many RF linear amplifier
data sheets. If the amplifiers are for use in cable television
distribution systems, as previously stated, it is common
practice to specify Second Order Intermodulation Distortion,
Cross Modulation Distortion and Composite Triple Beat. We
will examine these one at a time. First, consider Second
Order Intermodulation Distortion (IMD). Remember these are
unwanted signals created by the sums and differences of any two frequencies present in the amplifier. IMD is normally specified at a given signal output level and involves 3 channels — two for input frequencies and one to measure the resulting distortion frequency. The channel combinations are standardized in the industry but selected in a manner that typically gives a worst case condition for the 2nd order distortion results. An actual measurement consists of creating output signals (unmodulated) in the first two channels listed and looking for the distortion products that appear in the 3rd channel. If one wishes to predict the 2nd order IMD that would occur if the signals were stronger (or weaker), it is only necessary to remember the 1:1 relationship that led to a 2nd Order Intercept Point. In other words, if the specification guarantees an IMD of -68 dB Max. for a Vout = +46 dBmV per channel, then one would expect an IMD of -64 dB Max. for a Vout = +50 dBmV per channel, etc.

Cross Modulation Distortion (XMD) is a result of the cross-compression and cross-expansion terms generated by the third order non-linearity in the amplifier’s input-output transfer function. In general, the XMD test is a measurement of the presence of modulation on an unmodulated carrier caused by the distortion contribution of a large number of modulated carriers. The actual measurement consists of modulating each carrier with 100% square wave modulation at 15.75 kHz. Then the modulation is removed from one channel and the presence of residual modulation is measured with an amplitude modulation (AM) detector such as the commercially available Matrix RX12 distortion analyzer. Power levels and frequency relationships present in the XMD test are shown in Figure 23.

Composite Triple Beat (CTB) is quite similar to XMD except all channel frequencies are set to a specified output level without modulation. Then one channel frequency is removed and the presence of signal at that frequency is measured. The signals existing in the "off" channel are a result of triple beats (the mixing of 3 signals) among the host of carrier frequencies that are present in the amplifier. A graphical representation of the CTB test is shown in Figure 24.

European cable television systems usually invoke an additional specification for linear amplifiers which is called the DIN test. DIN is a German standard meaning Deutsche Industrie Norm (German Industrial Standard) and the standard that applies for CATV amplifiers is DIN45004B. DIN45004B is a special case of a three channel triple beat measurement in which the signal levels are adjusted to produce a -60 dBc distortion level. An additional difference from normal triple beat measurements is the fact that the levels are different for the three combining signals. If we call the four frequencies involved in the measurement F, F1, F2 and Fm, then F is set at the required output level that, along with F1 and F2, lead to a distortion level 60 dB below the level of F, and F1 and F2 are adjusted to a level 6 dB below the level of F. Distortion is measured at the frequency Fm. Frequency relationships (used by Motorola) between F, F1, F2 and Fm are as follows: F1 = F - 18 MHz; F2 = F - 12 MHz and Fm = F + F2 - F1. Figure 25 illustrates the frequency and power level relationships that exist in the DIN test.

Linear amplifiers aimed at television transmitter applications will generally have another distortion test involving 3 frequencies. Basically it is another 3rd order intermodulation test with power levels and frequencies that simulate a TV signal. Relative power levels and frequencies are shown in Figure 26.

Thermal resistance ratings of CATV modules (as well as Power modules described in the next section) are, perhaps,
conspicuous by their absence. Because the amplifiers have several heat sources that are contained within the amplifier, it is necessary for the user to provide sufficient heat sinking to the case of the amplifier such that the operating case temperature never exceeds its maximum rating. Actual power dissipation can be determined by considering the operating voltage and the maximum current rating of the device. Actual RF power output of most CATV modules is at most a few milliwatts which means that most of the power consumed by the module is dissipated in the form of heat. Typically this power dissipation runs in the range of 5 watts for conventional modules such as the MHW5122A but can increase to 10 watts for a power doubler such as the MHW5185.

Because linear (and power) modules have inputs and outputs that are matched to standard system impedances (75 ohms for CATV amplifiers and 50 ohms for power amplifiers), test circuits and fixtures are generally less important than for discrete devices. Basically test fixtures for modules are simply means of making RF and DC power connections to the module being tested. It is important if you build your own test fixture that you carefully decouple the DC power lines and that you provide adequate heat sinking for the device under test (D.U.T.). However, if the fixture is for linear modules involving low values of input and output VSWR, then it is extremely important, for accuracy, that the input and output networks (lines and connectors) be designed to exhibit return losses greater than 35 dB. Motorola modifies the RF connectors used in the fixture and, then, calibrates their fixtures to be sure that the fixture does not introduce errors in measuring module return loss.

**POWER MODULES — Functional Characteristics**

Power modules are generally used to amplify the transmit signals in a 2-way radio to the desired level for radiation by the antenna. They consist of several stages of amplification (usually common emitter, Class C except for some low level stages that are Class A) combined in a hybrid integrated assembly with nominally 50 ohm RF input and output impedances. Selection of a module involves choosing one having the proper operating voltage, frequency range, output power, overall gain and mechanical form factor suitable for a particular application.

Power modules for mobile and portable radios also have unique specifications related to their applications. One of the most significant is that of stability. The stability of a module is affected not only by its design but also by many external factors such as load and source impedances, by the value of supply voltage and by the amount of RF input signal. External factors influencing stability are highlighted in Figure 27. Combinations of these factors over a range of values for each factor must be considered to be certain the module will remain stable under typical conditions of operation. The greater the range of values for which stability is guaranteed, the more stable is the module. Of particular importance is the degree of load mismatch which can be tolerated as evidenced by the stated value of load VSWR (the larger the value, the better). Stability specifications are generally evaluated thoroughly during the pre-production phase and then guaranteed but not tested on a production basis.

**Figure 26. 3rd Order IMD Test for TV**

**Figure 27. External Factors Affecting Stability**

Efficiency is becoming an increasingly important specification particularly in modules for portable radio applications. The correct way to specify efficiency is to divide the net increase in RF power (output power minus input power) by the total DC power consumed by the module. It is generally specified at rated output power because efficiency will decrease when the module is operated at lower power levels. Be careful that the specification includes the current supplied for biasing and for stages other than the output stage. Overlooking these currents (and the DC power they use) results in an artificially high value for module efficiency.

Most power module data sheets include a curve of output power versus temperature. Some modules specify this "power slump" in terms of a minimum power output at a stated maximum temperature; others state the maximum permissible decrease in power (in dB) referenced to rated power output. It is important to note the temperature range and the other conditions applied to the specification before passing judgement on this specification.

Generally power modules, like linear modules, do not have thermal resistance specified from die to heatsink. For multiple stage modules, there would need to be a specific thermal
resistance from heatsink to each die. Thermal design of the module will take care of internal temperature rises provided the user adheres to the maximum rating attached to the operating case temperature range. This is an extremely important specification, particularly at the high temperature end because of two factors. First, exceeding the maximum case temperature can result in die temperatures that exceed 200°C. This, in turn, will lead as a minimum to decreased operating life and as a maximum to catastrophic failure as a result of thermal runaway destroying the die. Second, hybrid modules have components that are normally attached to a circuit board and the circuit board attached to the flange with a low temperature solder which may become liquid at temperatures as low as 125°C. Again, the power to be dissipated can be determined by considering the RF output power and the minimum efficiency of the module. For example, for the MHW607, output power is 7 watts and input power is 1 mW; efficiency is 40% minimum. Thus the DC power input must be 7/0.4 = 17.5 watts. It follows that power dissipation would be 17.5 - 7 = 10.5 watts worst case.

Storage temperature maximum values are also important as a result of the melting temperatures of solder used in assembly of the modules. Another factor is the epoxy seal used to attach the cover to the flange. It is a material similar to that used in attaching caps for discrete transistors and, as stated earlier, is known to deteriorate at temperatures greater than 150°C.

Modules designed for use in cellular radios require wide dynamic range control of output power. Most modules provide for gain control by adjusting the gain of one (or two) stages by means of changing the voltage applied to that stage(s). Usually the control is to vary the collector voltage applied to an intermediate stage. A maximum voltage is stated on the data sheet to limit the control voltage to a safe value. This form of gain control is quite sensitive to small changes in control voltage as is evidenced by viewing the output power versus control voltage curves provided for the user (an example is shown in Figure 28). An alternative control procedure which uses much less current is to vary the base-to-emitter voltage of the input stages (which are generally class A) as illustrated in Figure 29. This is of particular significance in portables because of the power dissipated in the control network external to the module.

While not stated on most data sheets, it is always possible to control the output power of the module by controlling the RF input signal. Normally this is done by means of a PIN diode attenuator. Controlling the RF input signal allows the module to operate at optimum gain conditions regardless of output power. Under these conditions, the module will produce less sideband noise, particularly for small values of output power, when compared to the situation that arises from gain control by gain reduction within the module.

Noise produced by a power module becomes significant in a duplexed radio in the frequency band of the received signal (see Figure 30). A specification becoming more prominent, therefore, in power modules is one that controls the maximum noise power in a specified frequency band a given distance from the transmit frequency. Caution must be taken in making measurements of noise power. Because the levels are generally very low (~85 dBm), one must be assured of a frequency source driving the module that has extremely low noise. Any noise on the input signal is amplified by the module and cannot be discerned from noise generated within the module. Another precaution is to be sure that the noise floor of the spectrum analyzer used to measure the noise power is at least 10 dB below the level to be measured.

**DATA SHEETS OF THE FUTURE**

World class data sheets in the next few years will tend to provide more and more information about characteristics of the RF device; information that will be directly applicable by the engineer in using the device. Semiconductor manufacturers such as Motorola will provide statistical data about parameters showing mean values and sigma deviations. For discrete devices, there will be additional data for computer aided circuit design such as SPICE constants. The use of typical values will become more widespread; and, the availability of statistical data and the major efforts to make more consistent products (six-sigma quality) will increase the usefulness of these values.
SUMMARY

Understanding data sheet specifications and what they mean can be a major asset to the circuit designer as he goes about selecting and using RF semiconductors for his specific application. This paper has emphasized some unique data sheet parameters of RF transistors and amplifiers and has explained what these mean from the semiconductor manufacturer's point-of-view. It is hoped this effort will help the circuit engineer make his selection and use of RF semiconductors more efficient and effective.

The RF transistor and the amplifiers made with RF transistors are unusually complex semiconductor products and difficult to fully characterize. Not all information about RF device characteristics has been explained in this paper. Nor can all be covered in a data sheet. The circuit design engineer should contact the device manufacturer for more detailed information whenever it is appropriate. Most if not all current manufacturers of RF transistors and amplifiers have extensive applications support for the express purpose of assisting the circuit designer whenever and wherever assistance is needed.

Figure 30. Noise Power in Receive Band
MC68HC05B4 RADIO SYNTHESIZER

By: Peter Topping, Microprocessor Applications, Motorola, East Kilbride

The MC68HC05B4 is a general purpose single-chip microcomputer with 4K of ROM. It shares with the other members of the M6805 family of devices a powerful instruction set including versatile bit-manipulation instructions. It incorporates an SCI which is used in this application to control a six digit LCD-driver and a standby mode in which the clock is stopped. This mode has the dual benefits of saving power and, in this application, eliminating the problem of interference with the radio. When a key is pressed the microprocessor "wakes", performs the required function and then goes back into the standby mode. The synthesizer software is included in the mask programmed code in parts marked MC68HC05B4 DEMO. Alternatively it could be programmed into an MC68HC805B6.

Other members of the MC68HC05B family include the 68HC05B6 with 6K of ROM and 256 bytes of EEPROM and the 68HC805B6 which is similar to the 68HC05B6 but with the ROM replaced with EEPROM. The 68HC805B6 is thus suitable for prototyping and small volume production not justifying a mask ROM part.

Synthesis of the local oscillator (LO) in a superheterodyne radio provides many advantages over mechanical tuning. The main benefits are tuning accuracy, stability and the storing of often used frequencies. The accuracy and stability result from the fact that the oscillator is phase locked to a crystal oscillator. Prior to the availability of synthesizers, crystals were used to obtain this degree of accuracy but with the disadvantage that a separate crystal was required for each frequency. Using a PPL synthesizer similar performance can be achieved with an unlimited number of frequencies using only one crystal. The accurate drift-free tuning is particularly important for standby use when nobody is on hand to provide fine tuning.

A synthesizer can be added to almost any design of radio by replacing the tuning capacitor with a varicap diode as shown in figure 1. The voltage biasing this varicap is supplied by the synthesizer and can also be used to provide RF tuning. A simpler solution is to leave the existing tuning control, at least initially, as an RF "preselector." This means that tracking, which can be a problem with multi-band designs, need not be considered.

SYNTHESIZER

The Motorola MC145157 CMOS synthesizer is one of a series offering a variety of options including serial or parallel interfacing and single or dual modulus prescaling. In this synthesizer only single modulus prescaling is used. Serial interfacing was chosen to minimize the number of interconnections required to control the MC145157 from the MC68HC05B4.

Figure 2 shows a block diagram of the MC145157. The counters are both 14 bits long and are loaded from shift registers which are loaded from the microprocessor.
starting with the MSB. After loading the 14 data bits a 15th control bit is loaded and the information is transferred to the selected latch using LE (latch enable). If the control bit is a one then the reference divider latch is loaded, if it is zero the variable divider latch is loaded.

The reference counter divides the crystal oscillator down to the reference frequency (in this case 1kHz) at which the comparison is made with the (also divided down) local oscillator and the filtered output of the phase comparator supplies the tuning voltage to the local oscillator. The numbers chosen as the divide ratios determine the frequency at which this oscillator stabilises. The equation below shows the relationship between the various frequencies where P is the LO prescaler. The received frequency can be changed by altering the LO divide ratio. The microprocessor takes care of the decimal to binary conversion, IF offset and the other required arithmetic.

$$\text{LO freq.} = \text{RF} + \text{IF} = P \times \frac{\text{Xtal freq.}}{\text{ref. div. ratio}} \times \text{LO div. ratio}$$

## REFERENCE FREQUENCY

The synthesizer’s 10 MHz crystal oscillator is divided down by 10,000 to obtain the reference frequency at which the phase comparator operates. By choosing a high reference the filter design is made simpler. The disadvantage is that the minimum step size of the synthesizer is determined by this reference frequency. A reference of 1 kHz is a reasonable compromise for a broadcast receiver.

The MC145157 is specified to operate up to 20 MHz so pre-scaling is required on FM and SW (10.7 MHz IF). For this SW band divide by 5 pre-scaling is used and for FM divide by 10 is used. This increases the minimum step size to 10 kHz of FM which is ideal for this band and to 5 kHz on SW which is suitable for most broadcast stations but too large for some short wave applications. This can, however, be alleviated by the use of an RIT (receiver incremental tuning) control. The low IF SW options do not use pre-scaling and thus have a step of 1 kHz but a maximum frequency of just under 16 MHz (2 to the power 14 – IF).

The RIT adjustment is made by slightly changing the reference frequency. This is accomplished by replacing the usual trimming capacitors on the crystal pins of the MC145157 with varicap diodes. Adjustment is thus by a DC voltage allowing the control to be placed remote from the synthesizer. This type of adjustment necessarily gives a control range which is dependant on the tuned frequency but a high IF ensures that this is not too significant. The circuit shown gives the required range of +/-2.5kHz at the bottom of the SW band (1.6 MHz) and just over twice this range at 15 MHz.

If an RIT control is not required, pins 1 & 2 should have a 47pF capacitor and a 30pF trimmer respectively. The trimmer should be adjusted to provide a reference frequency of 1kHz. This adjustment can be made with a frequency meter or simply by tuning into a strong broadcast of known frequency and adjusting for optimum reception or symmetric off-channel response.

## FILTER

An important part of any phase locked loop is the loop filter. The filter shown in figure 3 is an active filter using the double ended phase detector output from the MC145157 feeding a 741 operational amplifier. An active filter has the advantage of increasing the available voltage swing beyond the supply rail of the MC145157.

The combination of active filter and double ended phase detector outputs makes it simple to select the correct relationship between voltage and frequency. Usually the fixed side of the varicap diode is earthed so increased
voltage increases the frequency of the oscillator but in some oscillator designs, where the varicap is already installed, the fixed side may be taken to the supply rail and increasing the voltage will decrease the frequency. With the filter design shown the choice can be made simply by switching the connections to pins 15 and 16 on the MC145157.

Resistors R1 through R4 may need to be adjusted empirically to stabilize the loop and eliminate any trace of the reference frequency from the output of the radio.

**DISPLAY**

The software controls a 6-digit LCD display (Hamlin type 4200) via an MC145000 display driver. This display indicates the current frequency and memory number and assists with the entry of new frequencies. The MC145000 is fed serially with 48 bits corresponding to 6 digits of 8 segments (including the decimal point). It formats this data into the four backplane and 12 front-plane waveforms required to drive the LCD. This type of display (figure 4) has the advantage of using only one 24-pin driver employing only 16 connections between the display and the driver.

More readily available static displays require about 45 connections and thus normally uses more than one driver IC. The MC14415 driver is based on a shift register and can thus be configured to be compatible in software with the MC145000. The only difference is that it requires an LE (latch enable) signal, but this function can be derived from the clock using the circuit shown in figure 5. The static display also has the advantages of improved contrast and reduced current consumption. The consumption reduces from about 70µA (using an MC145000) to about 40µA (using 3 MC144115s). The 5V supply can be used directly with the static display, there being no need for a contrast adjustment. If the rightmost digit on the display does not have a decimal point this output from the display driver should be connected to an un-used segment, eg. a colon or the decimal point of the next digit. Any un-used segments, eg. colons, should be connected to the backplane.

There are advantages in also incorporating a frequency display module (eg. FC177), as it will show frequency changes due to the use of an RIT control and may also prove useful during fault-finding.

If a frequency display module is used the microprocessor controlled display can be omitted, the main disadvantage being that entered numbers in the direct frequency mode are not seen until the radio has moved to the new frequency.

**PRINCIPLE OF OPERATION**

The keyboard has 16 keys which perform the following functions:
Figure 4. Microprocessor controller
These keys are used both for direct frequency entry and for recalling (or storing) the ten frequencies available on each band (thirty in total).

**UP**
Increment by one channel (5kHz SW, 9kHz MW, 50kHz FM) or 1kHz (10kHz on FM, not applicable to 10.7MHz SW)

**DOWN**
Decrement by one channel (5kHz SW, 9kHz MW, 50kHz FM) or 1kHz (10kHz on FM, not applicable to 10.7MHz SW)

**STORE**
Next key (0-9) stores current frequency at that key, (indicated by a decimal point on the left-most digit)

**CLEAR**
Clear display (frequency mode). Also toggles between channel steps and 1kHz steps in station mode (indicated by the right-most decimal point)

**MODE**
Change between frequency and station mode

**EXECUTE**
Go to frequency, but stay in current mode.

The leftmost digit in the display indicates which mode is current. In the direct frequency mode it is blank, In the station mode it shows the last station stored or recalled or if the current frequency has not been written into or recalled from memory it displays: -o-. A choice of 2 modes permits the minimum number of keystrokes regardless of method of use. In the station mode previously memorised stations can be recalled by pressing only the required button, there is no RECALL button. Storing a frequency requires two presses namely STORE (indicated by a decimal point on the left-most digit) and the memory number.

If direct frequency entry is required first press MODE to enter frequency mode, then enter the required frequency. There is now a choice, press MODE again to jump to the new frequency and return to station mode. Alternatively press EXECUTE to jump to the selected frequency but stay in frequency mode, new frequencies can then be selected with only the EXECUTE button required after each new frequency entered. The store facility also works in the frequency mode.

If it is required to change back from frequency mode to station mode without retuning the radio press STORE then MODE and to display current frequency press EXECUTE. In station mode EXECUTE updates the synthesizer and the display with the current frequency. This can be used when the radio is newly switched on to retune the frequency which was in use when it was switched off even if that

<table>
<thead>
<tr>
<th>Band</th>
<th>PB7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>IF offset</th>
<th>Step</th>
<th>Memory</th>
<th>Use</th>
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<td>0</td>
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<td>5, 1 kHz</td>
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<td>1</td>
<td>SW</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>10,700 kHz</td>
<td>5 kH</td>
<td>1</td>
<td>SW</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-10,700 kHz</td>
<td>50,10 kHz</td>
<td>2</td>
<td>FM</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0 kHz</td>
<td>50,10 kHz</td>
<td>2</td>
<td>FM</td>
<td>10</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-70 kHz</td>
<td>50,10 kHz</td>
<td>2</td>
<td>FM</td>
<td>10</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>10,700 kHz</td>
<td>50,10 kHz</td>
<td>2</td>
<td>FM</td>
<td>10</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>455 kHz</td>
<td>9,1 kHz</td>
<td>3</td>
<td>MW</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>468 kHz</td>
<td>9,1 kHz</td>
<td>3</td>
<td>MW</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>470 kHz</td>
<td>9,1 kHz</td>
<td>3</td>
<td>MW</td>
<td>-</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>10,700 kHz</td>
<td>5 kHz</td>
<td>3</td>
<td>SW</td>
<td>5</td>
</tr>
</tbody>
</table>

Note: A high on PB3 changes the MW channel spacing to 10kHz for use in the USA.
frequency was not stored. This can also be done automatically by designing the hardware to reset the microprocessor whenever the radio is switched on, thus allowing unattended recording etc. A method of achieving this is illustrated in figure 3. When the supply to the MC145157 is rising the BC108 switches on and momentarily pulls the microprocessor's reset low.

**BANDS**

Four of the MC68HC05B4's port B lines are used to provide band information to the CPU. These lines can be tied to the required level if only one band is required, this one band can constitute all the bands which use the same oscillator but select frequency range by switching coils. If however more than one oscillator has to be tuned or the step size has to be changed (eg. between MW and SW) the port lines can be switched using a separate switch or the same switch as that used for switching the other functions required within the radio (if spare contacts are available). Additionally the local oscillator feed to the MC145157 may need to be switched. The DC tuning voltage does not need to be switched as it can be fed in parallel to all varicaps. The following bands are available:

- Bands 0, 1 & 2 are intended for single-conversion (low IF) SW radios and band 3, which assumes an external divide by 5, for dual-conversion (10.7MHz offset) designs.
- Bands 4-7 are intended for FM and assume an external divide by 10, IFs available are ~10.7MHz (oscillator low) for front ends such as the LP1186, 10.7MHz (oscillator high) for most modern front ends (eg. Toko 5803/4 or 5402 or Larssholt 8319 or 7254) and ~70kHz for the low IF TDA7000 FM radio IC.

A selection of 0, 1 & 1 in bits 6, 5 and 4 will select 10.7MHz IF short wave regardless of the state of line 7 so two banks of memory (1 & 3) giving a total of 20 stations can be used provided that the third bank is not being used for medium wave. A control to switch line 7 high is required to utilise this feature. This will also work for the low IF short wave options in which the raising of line 7 will select medium wave with the same IF offset. The only significant difference other than selecting the other bank is a switch to 9kHz steps (if large steps are selected) but this only applies while line 7 is being held high.

**SYNTHESIZER CIRCUIT**

The circuit is in two distinct parts. The circuit of the synthesizer is shown in figure 3, and that of the microprocessor controller in figure 4. The synthesizer board can be made very small and is the only part of the circuit which need actually go into (or close to) the radio. The local oscillator tuning capacitor is replaced with a varicap diode biased by the PLL via the filter (as shown in fig 1). If the LO coil provides a DC ground for the varicap and C is not required as a padder then C and R can be omitted from fig 1.

The only other modification to the radio is the addition of an oscillator output to supply the MC145157. This should be taken from a low impedance point so that the oscillator...
Figure 7 shows a high-impedance amplifier suitable for use with the TDA7000 IC. This is necessary as the LO signal must be taken directly from the tuned circuit. This could be used with any other front end not equipped with an LO output.

MICROPROCESSOR CONTROLLER CIRCUIT

Bits 4-7 on port A are programmed as outputs which scan the keyboard when the microprocessor is interrupted via one of the diodes (see figure 4). When the row which caused the interrupt is identified one of bits 0-3, which are programmed as inputs, indicates which key has been pressed.

Bits 0, 1 and 2 on port B control the synthesizer and bits 4, 5, 6 and 7 input the band information to the microprocessor. Bit 3 on port B selects the channel step size for MW. When it is low the channel spacing is 9kHz as required in Europe, when it is high it selects 10kHz for the USA.

The SCI is used to send serial data to the MC145000 LCD driver. The SCI included in MC68HC05B4/6 devices has the clock required for this type of peripheral. As the MC145000 accepts data into a shift register a clock is required with every data bit. The SCI has a control bit which adds a clock for the last bit in each byte. This is described in more detail below. For comparison the software includes code to drive the MC145000 using port pins and the LCD can also be connected to I/O lines 6 & 7 on port A.

The MC145157 synthesizer is also controlled serially but requires a latch enable pulse to load the counters from the shift register. This cannot be supplied from the SCI which has only data and clock outputs. Port pins were consequently used to communicate with this chip.

The 5v supply to the controller should not be switched off if the station memories are to survive. The supply does not need to be regulated and a battery of 4 zinc-carbon or
Ni-Cad cells will do. The LCD display driver can be switched off if required to increase battery life. When the LCD is subsequently switched on it will display random data but will be written to when any key is pressed (use of the EXECUTE key restores the display to its previous data) or automatically if a reset circuit type shown in figure 3 is used.

SOFTWARE

An assembled listing of the section of code associated with the synthesizer, which is contained in the MC68HC05B4 DEMO, appears at the end of this application note. The MC68HC05B4 is a mask programmed chip and this code is only present in parts marked “DEMO”. This B4 also includes a monitor and some test software. The pin numbers in fig 4 refer to the 52-pin FN part.

The first page of the listing contains no executable code but only hardware address definitions and the allocation of RAM. The B4 has 176 bytes of static RAM of which 108 are used in this application. 62 bytes are used for frequency storage, 2 bytes per frequency. There are 30 stored frequencies the additional one being the current frequency. 31 bytes are used for miscellaneous temporary storage and 15 bytes for the stack.

The second page of the listing contains the main program loop and the code which is executed after power-up or when an external reset occurs. On reset the program starts at address $137C. The ports and the SCI are initialised and the frequency stored in RAM locations SMEM & SMEM+1 is sent to the MC145157 and converted to decimal for displaying on the LCD. If the reset is the result of a power-up this frequency will be meaningless. The B4 then goes into the STOP mode in which the clock and all processing stops.

When a key is pressed the micro is wakened by the interrupt line, the clock is started and program execution commences at address $1354. The routine, KEYSN, which determines which key has been pressed is executed and the function appropriate to that key is executed via the indexed jump at address $1375. After completion of this function the RTI instruction returns the program counter to the address following the STOP instruction from which the micro resumes a standby condition by executing the STOP instruction again.

The third page comprises KEYSN and a table which associates the code of each key with an address. This is the start address of the subroutine required for that key. The routines for particular keys appear on the next four pages.

The PROG routine performs the calculations required to program the MC145157 with the correct divide ratio. Firstly the displayed frequency in BCD is added to the current IF offset. If band 3 is in use this result is divided by five to take the external prescaler into account. This is accomplished by first multiplying by two by adding the frequency to itself and then dividing it by ten by moving all digits down one place. The frequency is then converted to binary and sent to the synthesizer chip along with the reference divide ratio. In the case of band 3 this procedure discards the remainder when the divide by five is carried out. This is because the resolution on this band is 5kHz. If 5977kHz is requested the receiver will tune to 5975kHz. So that the user is aware of this having happened the actual binary frequency used is converted back to BCD and displayed on the LCD. Thus an entry of 5977 will change to 5975 when the receiver is tuned by pressing MODE or EXEC.

The MC145157 synthesizer chip is controlled by a 3-line serial bus. This is a common method of control as few pins are required and several chips can be controlled with only one enable line unique to each chip. The other two lines, clock and data can be common as the data is ignored if no enable is received. The SQRT routing sends data to the MC145157 using bits 0 & 1 on port B for the clock and data. It first sends the binary reference divide ratio (14 bits starting with the MSB) followed by a one for the control register (see fig 2). A one in the control register indicates that it is the reference divider which has to be loaded. This register is loaded by a latch enable signal from bit 2 on port B. The same procedure is repeated for the variable divide ratio except that this time the control bit is a zero.

The MC145000 LCD display driver is also serially controlled but has no enable pin. It can also be controlled by I/O lines and an example of how this can be done is shown on the last page of the listing. This routine is similar to that used for the MC145157. The B4, however, has a versatile serial port well suited to sending data to this type of peripheral. The second routine on the last page shows how this can be done using only less than half the bytes required for the I/O port method. The six bytes are sent by loading them in sequence into the SCI's data register. A wait loop monitoring the TDRE (transmit data register empty) flag is included so that each byte is written to this register only when the previous byte has been transferred to the transmit serial shift register. Once the last byte has been loaded a second wait loop monitoring the TC (transmit complete) flag ensures that transmission is complete before the program proceeds as a return to the STOP mode terminates all processing including that of the SCI. Serial transmission often does not require a clock on the last bit of each byte but this is required for shift-register type peripherals like the MC145000. This is ensured by setting the LBCL (last bit clock) control bit in the SCR1 register. This is done by sending $01 to SCR1 after a reset. The reset code also sets up the baud rate and enables SCI transmission. If the alternative static display is used then port A should be used to drive it as the timing used on the SCI is not appropriate for the MC144115 display drivers.

The remainder of the code consists of subroutines for IF selection, BCD to binary and binary to BCD conversion, and addition and subtraction of BCD numbers.

DEBUG

On reset the left hand digit should display "0" and the other 5 digits should display random numbers. Pressing MODE should blank all but the rightmost digit which should display a zero. The LCD contrast should be adjusted using the 50k potentiometer in figure 4. With the LCD on, the standby current should be about 70µA and with it off, less than 1µA.

The only problems usually experienced with the synthesizer are instability of the LO frequency and audible reference frequency on the output of the radio. Either of these problems should be resolved by empirically adjusting R1 through R4. R1 & R2 should normally be in...
the range 1k to 10k, and R3 & R4 in the range 10k to 50k. Accurate values cannot be predicted as they depend on factors which vary between oscillators. The most significant of these factors is the tuning rate expressed in MHz per volt. The values shown in figure 3 were used with a dual conversion shortwave receiver with a tuning rate of about 1MHz/v.

An effective method of faultfinding a PLL circuit is to initially do the tuning with a potentiometer, leaving the output of the filter disconnected from the VCO. As the radio is tuned through the frequency set up in the synthesizer the filter output should switch from one extreme to the other. Until this test passes it is not useful to close the loop as it is very hard to distinguish the cause of a problem from its effects.

If, after adjusting R1 through R4, the reference frequency can still be heard, the tuning rate may need to be reduced by using a smaller valued C (figure 1) and adding a fixed capacitor across the oscillator coil. This will increase the Q of the oscillator and reduce the phase noise. If the tuning range becomes too small it can be restored by switching oscillator coils.
This program enables the MC68HC05B4 to synthesize the local oscillator of a superhet radio with MW/LW, SW and FM bands each with a choice of IF offsets. It utilises an MC145157 synthesizer and an MC145000 LCD driver with a six-digit four backplane display.

P. Topping 23-11-87

OPT noc

0000  PORTA EQU $00  PORT A ADDRESS
0001  PORTB EQU $01  " B "
0002  PORTC EQU $02  " C "
0004  PORTAD EQU $04  PORT A DATA DIRECTION REG.
0005  PORTBD EQU $05  " B "
0006  PORTCD EQU $06  " C "
000D  BAUD EQU $0D  SCI BAUD RATE REGISTER
000E  SCR1 EQU $0E  " CONTROL REG. No. 1
000F  SCR2 EQU $0F  " "
0010  SCSR EQU $10  " STATUS "
0011  SDAT EQU $11  " DATA "
0050  ORG $0050

0050  Q RMB 6 DISPLAYED NUMBER
0055  P RMB 6 WORKING NUMBER 1
005C  R RMB 6 WORKING NUMBER 2
0062  W1 RMB 1 W
0063  W2 RMB 1 O
0064  W3 RMB 1 R
0065  W4 RMB 1 K
0066  W5 RMB 1 I
0067  W6 RMB 1 N
0068  KEY RMB 1 CODE OF PRESS KEY
0069  CARRY RMB 1 BCD CARRY
006A  COUNT RMB 1 LOOP COUNTER
006B  NUM1 RMB 1 1ST No. POINTER (ADD & SUBTRACT)
006C  NUM2 RMB 1 2ND No. POINTER (ADD & SUBTRACT)
006D  LOGO RMB 1 STATION MODE INDICATOR/NUMBER
006E  STAT RMB 1 STATUS BYTE :-
  0: MODE 1: STATION, 0: FREQ
  1: STEP 1: 1KHZ, 0: CHANNEL
  2: CLRQ 1: CLEAR IF NO. KEYED
  3: STOR 1: STORE, 0: RECALL
006F  SMEM RMB 62 CURRENT FREQ. + 30 MEMORIES
00AD  RMB 6B UNUSED
00F1  STACK RMB 14 15 BYTES USED (1 INTERRUPT (5)
00FF  SP RMB 1 AND 5 NESTED SUBROUTINES (10))
A hardware interrupt occurs with every keystroke and is vectored to start here. The B4 is wakened from STOP and the appropriate function for the key is performed. After the RTI instruction the micro returns to the STOP mode.

```
1354  ORG  $1354

1354  2E 01  STIRQ  BIL  REAL  INTERRUPT  REAL  ?
1355  B0  RTI  NO,  ABORT
1357  CD  13  A9  REAL  JSR  KEYSCH  KEY  PRESSED  ?
135A  24  1F  BCC  AB  NO,  ABORT
135C  5F  CLRX
135D  B7  68  STA  KEY  CODE  OF  PRESSED  KEY
135E  A6  27  LDA  #$27  STATION  MODE
1361  B7  6D  STA  LOGO  INDICATOR
1362  D6  13  CD  RJ  LDA  CTAB,X  FETCH  KEYCODE
1366  81  6B  CMP  KEY  WAS  IT  THIS  ONE  ?
1369  27  0A  BEQ  PJ  YES
136A  A1  77  CMP  #$77  NO,  LAST  CHANCE  ?
136C  27  0D  BEQ  AB  YES,  ABORT
136E  8C  INCX
136F  8C  INCX  TRY
1370  8C  INCX  THE
1371  8C  INCX  NEXT
1372  20  EF  RJX  PJ  RJ  ONE
1374  8C  PJ  INCX
1375  DD  13  CD  JSR  CTAB,X
1378  CD  16  75  JSR  DQ  DISPLAY  Q
137B  80  AB  RTI

Reset  routine  initialises  ports  and  SCI and  puts  the  micro  into  STOP  mode.
```

```
137C  A6  FF  START  LDA  #$FF  DISPLAY
137E  B7  04  STA  PORTAD  OUTPUTS
1380  A6  07  LDA  #$07  BITS  0-2  OUTPUTS  -  SYNTH
1382  07  35  STA  PORTBD  BITS  3-7  INPUTS  -  BANDS
1384  A6  F0  LDA  #$F0  KEYBOARD
1386  B7  06  STA  PORTCD  I/O
1388  3F  02  CLR  PORTC
138A  3F  01  CLR  PORTD
138C  3F  00  CLR  PORTA
138E  3F  00  CLR  BAUD  MAXIMUM  BAUD  RATE
1390  A6  01  LDA  #$01  STA  SCR1  CLOCK  ON  ALL  8  BITS
1392  B7  0E  LDA  #$88  STA  SCR2  SET  TRANSMIT  ENABLE
1394  A6  08  STA  STAT  STATION  MODE
1396  B7  0F  STA  LOGO  INDICATOR
1398  3F  6C  JSR  NEW  PROGRAM  145157
139A  A6  27  JSR  0,STAT  STATION  MODE
139C  D7  6D  JSR  DQ  DISPLAY  Q
139E  CD  14  C2  STP  STOP  STANDBY
13A1  10  GE  STP  STOP  STANDBY
13A3  CD  16  75  STP  STOP  STANDBY
13A6  8E  BRA  STP
13A7  20  FD

457
The keyboard routine returns the code of the pressed key in the accumulator. CTAB points to the required subroutine.

```
13A9 A6 F7 KEYSCL LDA $#F7 SET UP FOR FIRST COLUMN
13AB 48 KEY1 LSLA TRY EACH COLUMN
13AC 24 12 BCC KEY2 COLUMN NOT FOUND
13AE B7 02 STA PORTC SET UP COLUMN
13B0 2F F9 BIH KEY1 NOT THIS ONE
13B2 98 CLC
13B3 B6 02 COLUMN LDA PORTC READ KEYBOARD
13B5 AD 0C BSR DBOUNC WAIT
13B7 2F 07 BIH KEY2 STILL PRESSED?
13B9 2E FE RELEASE BIL RELEASE WAIT FOR RELEASE
13BB AD 06 BSR DBOUNC WAIT
13BD 2E FA BIL RELEASE STILL RELEASED?
13BF 99 SEC SET FLAG
13C0 3F 02 CLR PORTC PREPARE LINES FOR IRQ
13C2 B1 RTS

13C3 AE FF DBOUNC LDX $FFF PAUSE
13C5 21 FE DLOOP BRN * 256X12
13C7 21 FE BRN * CYCLES
13C9 5A DECX
13CA 26 F9 BNE DLOOP
13CC B1 RTS

13CD EE CTAB FCB $EE 0 CODE OF KEY SUBROUTINE
13CE CC 14 0D JMP DIGIT
13D1 EE FCB $DE 1
13D2 CC 14 0D JMP DIGIT
13D5 DD FCB $DD 2
13D6 CC 14 0D JMP DIGIT
13D9 DB FCB $DB 3
13DA CC 14 0D JMP DIGIT
13DB BE FCB $BE 4
13DE CC 14 0D JMP DIGIT
13E1 BD FCB $BD 5
13E2 CC 14 0D JMP DIGIT
13E5 BB FCB $BB 6
13E6 CC 14 0D JMP DIGIT
13E9 7E FCB $7E 7
13EA CC 14 0D JMP DIGIT
13ED 7D FCB $7D 8
13EE CC 14 0D JMP DIGIT
13F1 78 FCB $7B 9
13F2 CC 14 0D JMP DIGIT
13F5 ED FCB $ED F MODE
13F6 CC 14 FA JMP MOD
13F9 07 FCB $D7 E PROGRAM
13FA CC 14 9C JMP PROG
13FD E7 FCB $E7 D DOWN
13FE CC 14 6C JMP DOWN
1401 EB FCB $EB C CLEAR ENTRY/STEP SIZE
1402 CC 15 0B JMP CLEAR
1405 07 FCB $B7 D STORE
1406 1E 6C BSET 3,STAT
1409 81 RTS
1409 77 FCB $77 A UP
140A CC 14 5F JMP UP

458
Number entry routine.

- If in station mode a frequency is read or written (if the store flag is set).
- In frequency mode the entered number is placed in the least significant digit and existing digits are moved up.

```
1400 9F
140E 44
140F 44
1410 00 6E 1E
1413 06 6E 1B
1416 B7 64
1410 05 6E 05
141B 15 6E
141D CD 16 55
1420 CD 16 6C
1423 BE 62
1425 E6 01
1427 F7
1428 SC
1429 83 63
1420 ze re
1420 BS 64
142F F7
1430 81
1431 97
1432 D6 16 62
1435 B7 6D
1437 9F
1438 4C
1439 0F 01 04
143C AB 14
143E 20 05
1440 00 01 02
1443 AB 0A
1445 4B
1446 97
1447 07 6E 0B
144A B6 6F
144C E7 6F
144E B6 70
1450 E7 70
1452 17 6E
1454 81
145B F6 6F
145D 20 B3
```

DIGIT TXA
LSRA
LSRA
BRSET 0,STAT,SKP STATION MODE ?
BRSET 3,STAT,SKP STORING ?
STA W3
BRCLR 2,STAT,SHIFT CLEAR Q ?
BCLR 2,STAT YES, CLEAR FLAG
JSR CLQ AND CLEAR Q
LSR1 LSRL BR SET
BR CLR
ST/I BCLR
JSR
LDX W1
AGS LDA 1,X MOVE ALL DIGITS
STA 0,X UP ONE PLACE
INCX
CPX W2
BNE AGS DONE ?
LDA W3 YES, RECOVER NEW DIGIT
STA 0,X AND PUT IT IN LSD
RTS

SKP TAX X < MEMORY No.
LDA STABL,X REPLACE LOGO WITH
STA LOGO MEMORY NUMBER
TXA
INCA ADD 1 TO SKIP CURRENT FREQ.
BRCLR 7,PORTB,MW6
ADD #20 THIRD BANK OF 10
BRA MW4 STATIONS
MW6 BRCLR 6,PORTB,MW4
ADD #10 SECOND BANK OF 10
MW4 LSLA 2 BYTES PER MEMORY
TXA BACK TO X
BRCLR 3,STAT,RECALL

STORE LDA SMEM WRITE CURRENT
STA SMEM,X FREQUENCY INTO
LDA SMEM+1,X SELECTED STATION
STA SMEM+1,X MEMORY
BCLR 3,STAT CLEAR FLAG
RTS

RECALL LDA SMEM,X RECALL
STA SMEM SELECTED
LDA SMEM+1,X STORED
STA SMEM+1 STATION
BRA NEW

459
Increment and decrement routine.
Step size is 1kHz if the step flag is 1
but 9kHz for MW and 5kHz for SW if 0.
FM steps are 10kHz and 50kHz.
Band 3 is always 5kHz.
If PB3 is high MW channel step is 10kHz
for use in the US of A.

***************

UP
BSR LDXR
INC SMEM INCREMENT LSB
BNE T1 DID IT WRAP ROUND
INC SMEM+1 YES, INCREMENT MSB
T1 DECX
BNE IF ALL DONE?
BRA NEW

DOWN
BSR LDXR
DF TST SMEM IS LSB ZERO
BNE T2 IF NOT LEAVE MSB
DEC SMEM+1 DECREMENT MSB
T2 DEC SMEM DECREMENT LSB
DECX
BNE DF ALL DONE?
BRA NEW

LDXR
LDX #2 1 KHz (FM: 10KHz)
BRSET 1,STAT,SRT:
BSR BAND
CMP #3
BEQ SRT
LDX #10 5 KHz (SW, FM: 50KHz)
BRCLR 7,PORTB,SRT
LDX #18 9 KHz (MW)
BRCLR 3,PORTB,SRT
LDX #20 10 KHz (US MW)

SRT

******************************

* Read band from port B.
*
******************************

BAND LDA PORTB FIND BAND
AND #$70 USE Bits 4, 5 & 6
LSRA MOVE
LSRA DOWN
LSRA INTO
LSRA LS Bits
PROG is executed when EXEC or MODE is pressed. The displayed number is added to the IF offset, converted to binary and stored in SMEM & SMEM+1.

NEW takes the binary working frequency in SMEM & SMEM+1 and sends it to the synthesizer chip using the subroutine SQRT. It also converts it to BCD for the display.

```
149C 00 6E 23  PROG  BRSET 0,STAT,NEW STATION MODE ?
149F CD 15 49  JSR   IFO   P < IF OFFSET
14A2 AE 50  LDX   #Q
14A4 BF 6B  STX   NUM1
14A6 CD 15 EE  JSR   ADD   Q < FREQ + IF
14A9 AD E8  BSR   BAND
14AB A1 03  CMP   #3   BAND 3 ?
14AD 26 10  BNE   ONE   NO
14AF AE 50  LDX   #Q   YES, DIVIDE BY FIVE
14B1 BF 6C  STX   NUM2
14B3 CD 15 EE  JSR   ADD   Q < 2 X (FREQ + IF)
14B6 AE 05  LDX   #5
14B8 EE 4F  LPP   LDA   Q-1,X  MOVE ALL DIGITS
14BA E7 50  STA   Q,X   IN Q DOWN ONE
14BC 5A  DECX   PLACE TO DEVIDE
14BD 26 F9  BNE   LPP   BY 10 (Q < Q/5)
14BF CD 15 9E  ONE  JSR   BCON   CONVERT Q TO BINARY
14C2 A6 21  NEW  LDA   #$21  1 KHZ (10MHZ/10,000)
14C4 B7 5C  STA   R   "
14C6 A6 4E  LDA   #$4E  "
14CB B7 5D  STA   R+1   "
14CA AD 53  BSR   SQRT   SEND NEW FREQUENCY
14CC CD 16 24  JSR   DCON   CONVERT TO BCD IN Q
14CF AD C2  BSR   BAND
14D1 A1 03  CMP   #3   BAND 3 ?
14D3 26 19  BNE   STIF   NO
14D5 AE 50  LDX   #Q   YES, MULTIPLY BY 5
14D7 BF 6B  STX   NUM1
14D9 BF 6C  STX   NUM2
14DB AE 56  LDX   #P
14DD CD 15 EE  JSR   ADD   P < 2Q
14E0 AE 56  LDX   #P
14E2 BF 6B  STX   NUM1
14E4 AE 50  LDX   #Q
14E6 CD 15 EE  JSR   ADD   Q < 3Q
14E8 AE 50  LDX   #Q
14EB CD 15 EE  JSR   ADD   Q < 5Q
14EE CD 15 49  STIF  JSR   IFO   P < IF OFFSET
14F1 AE 50  LDX   #Q
14F3 BF 6B  STX   NUM1
14F5 14 EE  BSET 2,STAT
14F7 CC 15 D5  JMP   SUB   Q < (RATIO X STEP) -IF
```

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Mode change routine.

Routine to send the reference and local oscillator divide ratios to the 145157.
The IF offset is selected according to the required band and placed in "P".
BCD to binary conversion. No. in "Q" is converted to binary in SMEM & SMEM+1.

<table>
<thead>
<tr>
<th>Line</th>
<th>Opcode</th>
<th>Location</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>159E 3F 6F</td>
<td>BCON</td>
<td>CLR SMEM</td>
<td>CLEAR WORKING</td>
</tr>
<tr>
<td>15A0 3F 70</td>
<td>CLR</td>
<td>SMEM+1</td>
<td>FREQUENCY LOCATIONS</td>
</tr>
<tr>
<td>15A2 5F</td>
<td>CLRX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15A3 66 6F</td>
<td>L2</td>
<td>LDA SMEM</td>
<td>LS BYTE</td>
</tr>
<tr>
<td>15A5 48</td>
<td>LSLA</td>
<td>2xLSB</td>
<td></td>
</tr>
<tr>
<td>15A6 B7 62</td>
<td>STA</td>
<td>W1</td>
<td>SAVE 2xLSB</td>
</tr>
<tr>
<td>15A8 39 70</td>
<td>ROL</td>
<td>SMEM+1</td>
<td>2xMS Byte</td>
</tr>
<tr>
<td>15AA B6 70</td>
<td>LDA</td>
<td>SMEM+1</td>
<td></td>
</tr>
<tr>
<td>15AC B7 63</td>
<td>STA</td>
<td>W2</td>
<td>SAVE 2xMSB</td>
</tr>
<tr>
<td>15AE B6 62</td>
<td>LDA</td>
<td>W1</td>
<td>2xLSB</td>
</tr>
<tr>
<td>15B0 48</td>
<td>LSLA</td>
<td>4xLSB</td>
<td></td>
</tr>
<tr>
<td>15B1 39 70</td>
<td>ROL</td>
<td>SMEM+1</td>
<td>4xMSB</td>
</tr>
<tr>
<td>15B3 48</td>
<td>LSLA</td>
<td>8xLSB</td>
<td></td>
</tr>
<tr>
<td>15B4 39 70</td>
<td>ROL</td>
<td>SMEM+1</td>
<td>8xMSB</td>
</tr>
<tr>
<td>15B6 B6 62</td>
<td>ADD</td>
<td>W1</td>
<td>10xLSB</td>
</tr>
<tr>
<td>15BA B7 6F</td>
<td>STA</td>
<td>SMEM</td>
<td></td>
</tr>
<tr>
<td>15BC B9 63</td>
<td>LDA</td>
<td>SMEM+1</td>
<td></td>
</tr>
<tr>
<td>15BE B7 70</td>
<td>ADC</td>
<td>W2</td>
<td>10xMSB</td>
</tr>
<tr>
<td>15C0 5C</td>
<td>STA</td>
<td>SMEM+1</td>
<td></td>
</tr>
<tr>
<td>15C1 E6 50</td>
<td>INCY</td>
<td></td>
<td>FETCH</td>
</tr>
<tr>
<td>15C3 B8 6F</td>
<td>LDA</td>
<td>Q,X</td>
<td>NEXT</td>
</tr>
<tr>
<td>15C5 B7 6F</td>
<td>ADD</td>
<td>SMEM</td>
<td>DIGIT</td>
</tr>
<tr>
<td>15C7 4F</td>
<td>STA</td>
<td>SMEM</td>
<td>AND</td>
</tr>
<tr>
<td>15C8 B9 70</td>
<td>CLRA</td>
<td>SMEM+1</td>
<td>ADD IT TO</td>
</tr>
<tr>
<td>15CA B7 70</td>
<td>ADC</td>
<td>SMEM+1</td>
<td>WORKING</td>
</tr>
<tr>
<td>15CC A3 05</td>
<td>STA</td>
<td>SMEM+1</td>
<td>FREQUENCY</td>
</tr>
<tr>
<td>15CE 26 D3</td>
<td>CPX</td>
<td>#5</td>
<td>DONE ?</td>
</tr>
<tr>
<td>15D0 38 6F</td>
<td>BNE</td>
<td>L2</td>
<td></td>
</tr>
<tr>
<td>15D2 39 70</td>
<td>BSL</td>
<td>SMEM</td>
<td>MOVE UP ONE BIT TO</td>
</tr>
<tr>
<td>15D4 81</td>
<td>ROL</td>
<td>SMEM+1</td>
<td>INCLUDE 145157 CONTROL BIT</td>
</tr>
</tbody>
</table>

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Addition and subtraction of BCD numbers

1505 BF 66 SUB STX W5 ANSWER POINTER
1507 BE 6C COM2 LDX NUM2 9S COMPLIMENT
1509 A6 06 COMP LDA #06 SECOND NUMBER
150B 87 6A STA COUNT
150D A6 09 LOOP3 LDA #09
150F E0 05 SUB 5,X SUBTRACT FROM 9
1511 E7 05 STA 5,X AND PUT IT BACK
1513 5A DECX
1514 3A 5A DEC COUNT
1516 26 F5 BNE LOOP3
1518 3F 69 CLR CARRY SET CARRY TO ONE
151A 3C 69 INC CARRY BEFORE ADDING
151C 20 04 BRA AD ADD FIRST NUMBER
151E 3F 69 ADD CLR CARRY
1520 BF 66 STX W5 ANSWER POINTER
1522 A6 06 AD LDA #06
1524 B7 6A STA COUNT
1526 BE 6B LDX NUM1 1st No. POINTER
1528 BF 64 STX W3
152A BE 6C LDX NUM2 2nd No. POINTER
152C DF 65 STX W4
152E CC CC LOOP LDX W3
1530 EC 6C LDA 5,X
1532 3A CC DEC W3
1534 BE 65 LDX W4
1536 EB 05 ADD 5,X ADD
1538 3A 55 DEC W4
153A BB 69 ADD CARRY SET ON ADDITION OVERFLOW
153C 3F 69 CLR CARRY OR POS. RESULT SUBTRACTION
153E AD 0F BSR ADJ DECIMAL ADJUST
1540 BE 66 LDX W5
1542 E7 05 STA 5,X SAVE ANSWER
1544 3A 66 DEC W5
1546 3A 6A DEC COUNT
1548 BE 6E BNE LOOP DONE?
154A 81 RTS
154C 0A 0A AJ SUB #10 YES, SUBTRACT 10
154E 3C 69 INC CARRY AND REMEMBER CARRY
1550 A1 0A ADJ CMP #10
1552 24 F8 BHS AJ 10 OR MORE?
1554 B1 RTS

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**************

* Current binary divide ratio in SMEM & SMEM+I is converted to decimal in Q. *

**************

1624 B6 70
1626 B7 63
1628 B7 6F
162A B7 62
162C AE 5C
162E BF 6B
1630 AD 25
1632 3C 61
1634 AE SC
1636 BF SB
1638 AD 2S
163A 3C SI
163C AD IF
163E 07 G7
1640 07 63
1642 24 06
1644 AE S0
1646 BF 6C
1648 AD A4
164A AE 50
164C BF 6C
1650 3A 67
1652 26 EA
1654 81

DCON LDA SMEM+I TRANSFER CURRENT
STA W2 FREQUENCY DEVICE
LDA SMEM RATIO INTO
STA W1 WORKING AREA
LDX $R CLEAR
STX NUM1
BSR CLRA R
INC R+S R < 1
BSR CLQ CLEAR Q
LDA $14 14 BITS TO CONVERT
STA W6
LSR W2 MOVE OUT AND IGNORE
STA W6
ROR W1 145157 CONTROL BIT
LOOP2 LSR W2 MOVE OUT
ROR W1 FIRST (LS) BIT
BCC NXT ZERO
LDX $Q ONE, ADD
STX NUM2 CURRENT VALUE
BSR ADD OF R
NXT LDX $R ADD R
STX NUM2 TO
BSR ADD ITSELF
DEC W6 ALL
BNE LOOP2 DONE ?

RTS

**************

* Miscellaneous. *

**************

1655 AE 50
1657 AE 06
1659 B7 6A
165B 7F
165C 5C
165D 3A 6A
165F 26 FA
1661 81

CLQ LDX $Q CLEAR Q
CLRAS LDA $06 CLEAR 6 Bytes
STA COUNT STARTING AT X
CR CLR 0,X
INX
DEC COUNT
BNE CR DONE ?

RTS

1662 EB
1663 60
1664 C7
1665 E5
1666 6C
1667 AD
1668 AF
1669 E0
166A EF
166B ED
166C AE 50
166E B7 62
1670 A6 05
1672 B7 63
1674 81

STABL FCB $EB 0 SEGMENT
FCB $60 1
FCB $C7 2 CODES
FCB $E5 3
FCB $6C 4 FOR THE
FCB $AD 5
FCB $AF 6 MC145000
FCB $E0 7
FCB $EF 8 LCD DRIVER
FCB $ED 9

DR1 LDA $Q STORE POINTERS
STA W1 (USED IN DIGIT AND DQ)
ADD $5
STA W2
RTS

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First part of display subroutine adds the store and kHz flags and station mode indicator, replaces BCD with segment codes and blanks leading zeros.

```
1675 AD F5 DQ  BSR  DR1
1677 AE SC LDX  #R  CLEAR R
1679 AD DC BSR  CLRAS
167B BD 62 LDX  W1  FIND
167D 5A  DECX  LEADING
167F B3 63 RO  INCX  ZEROS
1681 27 03 CPX  W2
1683 F6 BEQ  OUT  LAST ?
1684 27 F8 LDA  $0,X NO
1686 5A BEQ  RO  ZERO ?
1687 BF 67 OUT  DECX  EXIT LOOP
1689 AE 05 LDA  #$05 LEAST SIG. LEADING ZERO
168B 87 65 STA  W4
168D BE 63 LDA  W2  LSB
168F FG  D3 LDA  $0,X
1690 BF 66 STX  W5
1692 97 TAX
1693 D6 16 62 LDA  STABL,X  FIND 7 SEGMENT CODE
1695 BE 65 LDX  W4  PUT IN DISPLAY TABLE
1697 EC 03 STA  R,X
1699 3A 65 DEC  W4
169B BE 66 LDX  W5
169D 5A DECX
169F B3 67 CPX  W6  FINISHED ?
16A1 26 EC BNE  D3
16A3 00 01 09 BRCLR  6,PORTB,NOOPT SW ?
16A6 0E 01 06 BRSET  7,PORTB,NOOPT MW ?
16A9 86 65 LDA  R+3
16AB AA 10 ORA  #$10  DECIMAL POINT FOR FM MHZ
16AD B7 65 STA  R+3
16AF B6 5C NODPT  LDA  R
16B1 01 BE 02 BRCLR  0,STAT,KS
16B4 BD 65 LDA  LOGO  STATION MODE LOGO
16B6 07 6E 02 KS  BRCLR  3,STAT,PIKS
16B9 8E 10 ORA  #$10  STORE FLAG INDICATOR
16BB B7 6C PIKS STA  R
16BD CD 14 93 JSR  BAND
16C0 A1 03 CMP  #3  BAND 3 ?
16C2 27 09 BEQ  OUTT  YES, NO CHOICE
16C4 03 BE 06 BRCLR  1,STAT,OUTT NO, STEP SIZE ?
16C7 B6 51 LDA  R+5
16C9 AA 10 ORA  #$10  KHZ STEP INDICATOR
16CB B7 61 STA  R+5
```
The second part of the display routine sends the 48 bits required by the display driver. For comparison two routines are included, one using port A lines and a second using the SCI.

The SCI LCD driver interface.

```assembly
16CD AE 05 OUTT LDX #5 SEND DISPLAY TABLE TO 145000
16CF E6 5C DISCHR LDA R,X
16D0 BF 64 DISPLAY STX W3 SAVE INDEX
16D1 10 00 BCLR 6,PORTA CLEAR DATA
16D5 AE 08 LDX #8
16D7 44 DIS1 LSRA SET UP
16D8 24 02 BCC DIS2 BIT OF
16DA 1C 00 BSET 6,PORTA ACCUMULATOR
16DC 1E 00 DIS2 BSET 7,PORTA CLOCK
16DE 1F 00 BCLR 7,PORTA IT
16E0 1D 00 BCLR 6,PORTA CLEAR DATA
16E2 5A DECX COMPLETE ?
16E3 26 F2 BNE DIS1 NO
16E5 BE 64 LDW W3 RESTORE INDEX
16E7 5A DECX
16E8 2A E5 BPL DISCHR
16EA AE 05 LDX #5 INITIALISE X
16EC E6 5C MORE LDA R,X FETCH DIGIT
16EE 0F 10 FD BRCLR 7,SCSR, WAIT_UNTIL TDRE = 1
16F1 B7 11 STA SDAT WRITE IT TO SCI TX REG.
16F3 5A DECX NEXT DIGIT
16F4 2A F6 BPL MORE DONE ?
16F6 8D 10 FD BRCLR 6,SCSR, WAIT_UNTIL TC=1
16F9 81 RTS
```
MC2831A is a one-chip FM transmitter system designed for FM communication equipment, such as FM transceiver, cordless telephone, remote control and RF data link.
MC2831A includes the following features:
-- Wide range of operation supply voltage (3.0 Volts to 8.0 Volts).
-- Audio amplifier with limiter.
-- Tone oscillator for Pilot/Data signalling.
-- RF oscillator which operates up to 30 MHz
-- Variable reactance modulator for FM modulation.
-- Battery checker for low battery indication.
-- SOIC package is available for small PCB area application.
Fig. 1 outlines the block diagram of MC2831A.

Figure 1. Functional Block Diagram
FUNCTIONAL BLOCK DESCRIPTION

The RF oscillator is an internally-biased Colpitts type which can be used for crystal in fundamental mode, or used in the conventional L/C Colpitts type.

Fig 2A shows the typical application of direct FM modulation using crystal. The crystal is operating in fundamental mode with parallel resonance at about 30 pF. L1 is applied for compensation of the reactance of the modulator and output frequency fine adjustment. The modulating signal can be applied at pin 3 for FM modulation. Using crystal for direct FM modulation, the max. deviation is +/-2.5 KHz to +/-3.0 KHz for < 2.0 % of modulation distortion. However, to have larger deviation, frequency multiplication technique can be applied. The ratio of the capacitors C1 and C2 is about 1 : 1 for best residual AM modulation suppression.

Figure 2A. Direct FM Modulation Using Crystal
Fig 2B shows another FM modulation approach using phase-lock-loop. The RF oscillator is applied in L/C type to form a V.C.O. with the action of the varicap. The oscillation frequency \( f_0 \) is given by:

\[
f_0 = \frac{1}{2\pi \sqrt{L C_0}}
\]

Where \( C_0 \) is the series combination capacitors of C1 and C2 and the parallel action of the varicap.

The phase-lock-loop is designed such that the RF carrier output has minimal phase-noise and the V.C.O. has good response to modulating signals. The design of the PLL technique is discussed in detail in application notes AN535 and AN553.
The Audio Amp. is a typical op-amp. The gain is determined by the ratio of the external resistors R1 and R2. The frequency response of the amp. is about 35 KHz. The limiter limits the amp. output to 1.4 Vpp for deviation limitation in FM modulation. The amp. output is applied to the modulator input through a variable resistor so that the depth of FM modulation can be adjusted.

\[
R_1 \quad \text{INPUT} \quad R_2 \quad \text{MIC \ AMP} \quad -+ \quad V_A \quad \text{OUTPUT}
\]

The tone oscillator is a typical LC type with oscillation frequency (f_t) given as

\[
f_t = \frac{1}{2\pi \sqrt{L_1 C_T}}
\]

The oscillator output level can be adjusted by external damping resistor R_t. The max. oscillator output level is approximately 1.0 Vpp with R_t = 47KΩ and the level decreases when R_t decreases. The tone oscillator output can be switched on/off by the Tone Switch input which has an internal pull up resistor of 100KΩ.

The Battery Checker is a comparator with the + terminal connected to an internal 1.2 volts reference. The output of the Battery Checker is an open collector output for driving L.E.D.

Fig. 3 shows the MC2831A in a typical transmitter application. The tone oscillator output and the audio mic output can be summed at the input of the Audio Amp. or at the modulator input through resistors.
Figure 3. Cordless Phone Transmitter

- **RF OSCILLATOR**
- **BUFFER**
- **MC2831A**
- **REACTANCE MODULATOR**
- **MIC AMP**
- **TONE SWITCH**
- **BATT CHECK**
- **Data Input**
- **Audio Input**
MC2831A IN 46/49MHz CORDLESS PHONE APPLICATION

A) Low Cost Single Channel With Pulse Dialing

Fig. 4A shows the hand-set schematic of a typical single channel cordless phone. The RF oscillator oscillates at 16.6MHz which through a frequency tripler, generates the 49MHz band for transmission. The tone oscillator can be used as a pilot tone signal for pulse dialing by connecting the pulse output of the Pulse Dialer MC145409 to the Tone Sw. Input of MC2831A.

The mic output and the tone osc. output are summed at the input of the mic amplifier. The output of the mic amp. is applied to the modulator input through a variable resistor for FM modulation depth adjustment. The Battery Checker can be applied to monitor the low battery supply condition.

MC2831A application in base-set of a cordless phone is shown in Fig. 4B. The circuit is similar to the hand-set. The RF oscillator oscillates at 15.5MHz which, after applying to the tripler, produces the 46MHz transmitting carrier. The receiver side can be handled by the MC3361/MC3359/MC3357. The tone oscillator can be used as the ring tone signalling to the hand-set if any incoming call ring signal is detected in the base-set.

The Battery Checker can be used to drive the ON/OFF hook relay for pulse dialing through the output of the pilot tone decoder.

B) High-End 10 Channel Selection with Pulse Tone Dialing Features

MC2831A can also be applied easily in cordless phone with 10 channels, Pulse Tone Dialing using Dual PLL frequency synthesiser MC145160 and Pulse Tone Dialer MC145412. The concept of using Dual PLL frequency synthesiser in the 10 channel 46/49MHz cordless phone is indicated in Fig. 5. The transmitter VCO oscillates at the half of the transmitting carrier frequency. The output of the VCO is applied to the Fin-T which will be divided down through the Prog. Prescaler B to produce a 2.5kHz for phase comparison. The output of the phase detector B PD-T will be low pass filtered to produce a D.C. voltage to control the VCO, thus forms a programmable PLL frequency synthesiser.

The control of the local oscillator VCO in the receiver side is similar to the Tx side. Through the Prog. Prescaler A & B, the following Tx & Rx channels can be generated.

<table>
<thead>
<tr>
<th>CHS</th>
<th>f1 MHz</th>
<th>f2 MHz</th>
<th>f3 (f1-10.695)MHz</th>
<th>f4 (f2-10.695)MHz</th>
<th>f5 (f2/2)MHz</th>
<th>f6 (f1/2)MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>46.610</td>
<td>49.670</td>
<td>35.915</td>
<td>38.975</td>
<td>24.8350</td>
<td>23.3050</td>
</tr>
<tr>
<td>2</td>
<td>46.630</td>
<td>49.845</td>
<td>35.935</td>
<td>39.150</td>
<td>24.9225</td>
<td>23.3150</td>
</tr>
<tr>
<td>3</td>
<td>46.670</td>
<td>49.860</td>
<td>35.975</td>
<td>39.165</td>
<td>24.9300</td>
<td>23.3350</td>
</tr>
<tr>
<td>4</td>
<td>46.710</td>
<td>49.770</td>
<td>36.015</td>
<td>39.075</td>
<td>24.8850</td>
<td>23.3550</td>
</tr>
<tr>
<td>5</td>
<td>46.730</td>
<td>49.875</td>
<td>36.035</td>
<td>39.180</td>
<td>24.9375</td>
<td>23.3650</td>
</tr>
<tr>
<td>6</td>
<td>46.770</td>
<td>49.930</td>
<td>36.075</td>
<td>39.135</td>
<td>24.9150</td>
<td>23.3850</td>
</tr>
<tr>
<td>7</td>
<td>46.830</td>
<td>49.980</td>
<td>36.135</td>
<td>39.195</td>
<td>24.9450</td>
<td>23.4150</td>
</tr>
<tr>
<td>8</td>
<td>46.870</td>
<td>49.930</td>
<td>36.175</td>
<td>39.235</td>
<td>24.9650</td>
<td>23.4350</td>
</tr>
<tr>
<td>9</td>
<td>46.930</td>
<td>49.990</td>
<td>36.235</td>
<td>39.295</td>
<td>24.9950</td>
<td>23.4650</td>
</tr>
<tr>
<td>10</td>
<td>46.970</td>
<td>49.970</td>
<td>36.275</td>
<td>39.275</td>
<td>24.9850</td>
<td>23.4850</td>
</tr>
</tbody>
</table>

Fig. 6A shows the typical circuit configuration of a 10 channel selection pulse tone dialing hand-set. The RF oscillator, with the action of the varicap, forms a VCO as discussed before. The RF output, after buffering, is applied to the frequency doubler for transmitting. The local oscillator of the receiver is also a V.C.O. which is buffered to drive the mixer of the receiver and input to the dual PLL MC145160 Rx-F. The reference osc freq. of the dual PLL is 10.245MHz which can be applied to the mixer of MC3361 for the 2nd conversion. The 5KHz output from the Dual PLL can be used as the page tone in the intercom mode operation. The DTMF Tone generated from the Pulse Tone dialer is applied to the input of the mic amp. for transmitting to the base set in the dialing mode, while the pulse output from the dialer is applied to the Tone SW. Input for gating the Pilot tone in the Pulse Dialing operation. The Battery checker is used as conventional battery low monitoring. MC2831A in the base set of the 10 channels version is very similar to hand set (Fig. 6B). The Channel selection input to the Dual PLL can be controlled by MCU for automatic channels scanning. Security coding can also be added in for channel security.
Figure 4A. MC2831A Application in Single Channel C/T Hand-Set
Figure 48. MC2831A in Single Channel C/T Base-Set
Figure 5. DPLL Application in 46/49MHz Cordless Phone 10 Channels Selection
Figure 6B. MC2831A Application in 10 Channels Selection Base-Set
MC2831A APPLICATION IN SMALL COM-PAGE SYSTEM.

A small com-page system consists of one base station and 6 to 9 small remote receivers. The base station can call any remote set with a particular system security coding and a voice channel is established from base station to remote for voice message. The base station has a rather high RF power output to cover a large area. Operating frequency is usually in the 136-174MHz range or citizen band of 27/49MHz. Applications of this system are in large farm-house, hospital, warehouse and messagers in a large company.

Fig. 7 outlines MC2831A circuit configuration in the base station. MC2831A provides nearly all the facilities in designing the base station, such as, the fundamental RF frequency oscillator, FM modulation through the reactance modulator, audio voice amplification, and the beep tone generator using the tone oscillator.

The calling operation is initiated by pressing the appropriate page no. key. The key board decoder will decode the key information input into binary coding which will trigger the control logic to start the calling sequence by sending out the page no. security code from the MC145026. The security code combination will follow the system address setting and the key no. entered during the calling period. The page no. indicator will also output the calling page no. through the BCD to 7 segment decoder. Meanwhile, the whole logic can be replaced by an MCU, for hardware design simplification.

On the remote receiver side, the low voltage FM receiver MC3361/MC3356 and the security code decoder MC145028 can be applied.

REMOTE CONTROL / DATA LINK APPLICATION

MC2831A also offers a simple design approach in remote control and RF data link. There are 3 major methods in transmitting digital data signalling through RF channels.

1. DTMF signalling (dual tone multiple frequency)
2. Tone burst signal format
3. Dual tone FSK signal scheme

DTMF signalling is the simplest method. By connecting the output of a DTMF generator to the input of the modulator of MC2831A, different combination of digital data will send out the associated dual frequencies for FM transmission.

Fig. 8 shows the configuration of MC2831A tone burst signalling transmission. The digital data is applied to the Tone SW. input for gating the tone output before FM modulation.

While fig. 9 shows the possible circuit in dual tone FSK signalling, an additional capacitor Cp is connected parallel to the LC tank circuit of the tone oscillator to vary the tone oscillation frequency. By switching the capacitor Cp, a FSK dual tone signal can be generated, which can be applied to the FM modulator for remote control, RF Data linkage application, such as key board to PC and PC to printer data linking of which low data rate (< 600 baud) is required. Furthermore, the Audio Amp. can be designed as a band-pass-filter to limit the bandwidth of the dual tone FSK signal before it is applied to the modulator input.
Figure 7. MC2831A in Small Com-Page Application
2.2µ
Digital Data
Tone Brust
Output

Figure 8. Tone Brust Signal Format

Digital Data Input

Tone Brust Output

Figure 8A. Tone Brust Signalling

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Figure 9. Dual Tone FSK Signalling

Digital Data Input

Dual Tone FSK Output

Figure 9A. Dual Tone FSK Format
MC2831A offers full facilities for FM transmitter system. It provides easy design steps, low external component count, and require small PCB area. Such features are most suitable in delicate portable FM transceiver application. Besides, it can be employed in other applications, such as intercom and control through A.C. line, ultrasonic devices etc.
A High Performance Manual-Tuned AM Stereo Receiver for Automotive Application Using MOTOROLA ICs MC13021, MC13020 and MC13041

INTRODUCTION

This article presents a high performance manual-tuned car AM stereo receiver design using MOTOROLA AM stereo ICs MC13021, MC13020 and MC13041. It is intended to provide radio design engineers with a good start in car manual-tuned AM stereo receiver design. The article consists of two parts. The first part describes all relative important principles of manual-tuned AM stereo receiver, and the other one details the car manual-tuned AM stereo receiver design.

PART I: THE CONSIDERATIONS ON MANUAL-TUNED AM STEREO RECEIVER DESIGN

The design of manual-tuned AM stereo receiver confronts several difficult problems, such as the phase noise, centre tuning, microphonics and RF mistracking.

PHASE NOISE Since the AM stereo is in AM/PM format, the phase noise created by frequency fluctuation becomes a noticeable problem which however does not cause serious affect on monophonic (MONO) receiver. Various factors cause frequency fluctuation, the major one being frequency drift of the local oscillator in mono-receiver with a conventional L/C oscillator. The frequency fluctuation is in the range of hundreds of Hz. But in stereo operation, it should be limited to a few Hzs because the 25Hz pilot tone with 4% phase modulation is equivalent to only 1.25Hz deviation. Any greater frequency fluctuation will cause interference to the pilot tone, and thus deteriorating the channel separation, signal to noise ratio (S/N) and distortion performances on stereo mode operation.

Besides the frequency stability requirement during operation, the center tuning during station tune-in and microphonics are equally important to the manual-tuned AM stéréo receiver.
CENTRE TUNING In manual tuning, any small frequency deviation from centre will breed phase noise and subsequent tune-off from stereo mode or chartering in and out of stereo mode. Practical experience has shown that only a small amount (there are few HZs) of deviation from centre frequency is allowed without seriously affecting the stereo performance. Obviously this is extremely difficult or even impossible to operate on a manual-tuned receiver unless some sort of AFC or centre tuning circuit is applied.

MICROPHONICS This effect is much more serious an AM stereo receiver. The drift of a typical variable capacitor tuner or inductance tuner is 1% or 3KHz respectively under vibration test according to a car environment. This introduces 17db higher impulse noise than the condition of 75% single channel, 400Hz modulation and / or 20db higher impulse noise causing by the 25Hz pilot signal. Even in a PLL synthesizer receiver, if a frequency drift caused by vibration is greater than the "Tracking Range", the receiver will lock off the stereo mode. This is obviously unacceptable in receiver operation.

FIGURE 1. MANUAL-TUNED SYSTEM OF MC13020, MC13021.
FIGURE 2. BLOCK DIAGRAM OF MC13021.

FIGURE 3. BLOCK DIAGRAM OF MC13020.
MOTOROLA has introduced the MC13021, interfacing with MC13020 decoder to solve those problems and obtained high performance in manual-tuned receiver. The combination of MC13020 and MC13021 provides a microphonics free manual-tuned AM stereo receiver with low noise oscillator, AFC and tuning aids.

The principle of the manual-tuned system of MC13021/MC13020 is described in figure 1, and figure 2 and 3 give the full circuit block diagram of the two ICs. The system operates at two different modes “Tuning” or “Tuned”. The mode status is controlled by the window detector & switching logic circuit.

In the “TUNING” MODE, the system acts as a FLL (Frequency Lock loop) function. The VCO2 (Voltage Control Oscillator), operating at 4 times of receiver oscillator frequency, feeds to the divider (÷4) which has three outputs; the one with opposite phase goes to the local oscillator of receiver mixer stage, and the other two with the same phase go to the phase detector as a reference frequency and to the L-C local oscillator circuit. In the phase detector the reference frequency is compared with the frequency at the L-C junction which is derived from the reference frequency. If the resonant frequency of the L-C is tuned to the reference frequency and in phase, the output of the phase detector is zero. Otherwise it outputs a correction voltage to VCO2 until the divided VCO2 frequency equals to the L-C resonant frequency.

When a station is tuned into the lock range (Approximately ±/— 2.5K) of the MC13020 AM stereo decoder, the decoder loop locks in, and pin 10 of the MC13020 goes high. Under this condition if the received signal is strong enough, the AGC voltage at pin4 of the MC13020 exceed the threshold voltage at pin16 of the MC13021, the phase detector of the MC13021 will be disconnected from the VCO2 by the Window detector & Switching circuit. Then, the receiver enters the “tuned” mode. The pin9 of the MC13021 goes high, this forces the decoder of MC13020 into “stereo” mode after detecting the 25Hz pilot signal.

The “loop driver” voltage at pin19 of the MC13020 is converted to the control current by the V/A (voltage to current) converter and pulls the VCO2 frequency into centre tuning frequency. Since the phase noise of the VCO2 is limited by the PLL loop in the “tuned mode”, the receiver remains tuned in a frequency until the frequency drift, caused by tuning or microphonics, falls outside the window range of the MC13021 circuit. Then, the phase detector of the MC13021 triggers the window detector circuit and reconnect the phase detector to VCO2. Consequently the decoder goes out of “tuned” mode and pulls low at pin7 of the MC13021. The circuit is once again switched to the “tuning” mode.
The window width of MC13021 depends upon the Q value of the tuning L/C resonant circuit and the VCO2 Varactor gain. The two threshold voltages of the window detector are $\pm V_{be} (=0.7V)$ from the reference voltage at pin12. The resistor across the pins 6,12 of MC13021 is used to set the centre voltage of the window and has significant influence on the performance of microphonics elimination.

The relationship between the window width and the Q of the tuning L/C is as following figure 4:

![Figure 4. WINDOW WIDTH OF MC13021.](image)

In general, the microphonics elimination (Electrical) of the circuit in figure-1 is almost effective by the following formula:

Electrical Microphonics Elimination $= 20 \log_{10} \frac{f_w}{f_c}$ (1)

$f_w = \text{Window Width}$.

$f_c = \text{Loop Corner Frequency}$.

For example, if the loop corner frequency and window width are 10Hz and 10K respectively. Then the microphonics elimination (Electrical) is equivalent to 60db.
PART II: APPLICATION OF THE CAR MANUAL-TUNED AM STEREO RECEIVER

This part describes the manual-tuned car AM stereo receiver design and all the practical applications concerned. To avoid duplication, the discussion emphasizes on the microphonics elimination circuit and other concerned that did not included in the data sheets. The circuit diagram, PCB layout, components layout are shown in the figure 5,6,7.

RF SECTION of the circuit consists of 2 transistors and 1 FET. The transistors Q1, Q3 connect as a common base cascade RF amplifier which isolates the converter from input side. The FET is chosen on Q3 for better overload capability. Q2, driven by the MC13041 AGC output voltage of pin12, attenuates the input signal level under strong signal conditions. To obtain 6KHz RF bandpass for high fidelity while maintaining good selectivity for AM stereo reception, two tuned frequency selective circuits are being used. The first frequency selective circuit consists of L1-1, C2, CT2 and C3. Changing the ratio of C2 and C3 to matches the impedance of the antenna and Q3. The second frequency selective circuit consists of C11, CT1 and L1-2. The output of L1-2 secondary feeds the RF signal to the input of receiver IC MC13041 at pin18.

RECEIVER SECTION uses the MC13041 Car AM receiver IC. It has low phase noise, good phase linearity, wide dynamic AGC range performance, it is particularly suitable for automotive application. It also provides a buffered oscillator output pin13 for connecting to frequency synthesizer. The balanced mixer has high spurious rejection, with low phase noise IF signal output and low Intermodulation. The mixer output of pin19 couples to the recommended IF filter consisted of the IF transformer T4 and ceramic filter CRF1. The IF filter provides a quasi-parabolic bandpass with reasonably constant group delay. Changing the biasing resistor R20 can adjust the overall IF gain and affect the input impedance of the IF stage too. The IF output at pin8 goes to detector circuit pin7 through C23. Detector coil T3 is used as a peak detector as well as a phase shift coil for tuning error detection.

STEREO DECODER MC13020 is a well-known MOTOROLA C-QUAM stereo decoder IC. The important function of the PLL in MC13020 is to lock the phase of the divided VCO1 frequency into the input IF carrier. The manual-tuned AM stereo receiver uses a L-C (T5) circuit for VCO1, it has wider range of linear and symmetrical amplitude to phase characteristic and $+/-2.5$KHz “pull-in” range. A recommended coil of TOKO or MITSUMI MF2928CS-1349Z is used for T5. Since the loop driver is in current mode, the impedance at pin19 is very high so that the current leakage of the loop filter cannot be ignored. Experience has shown that to obtain less than 1% distortion, the leakage current of the loop filter capacitors C53 and C54 should be less than 0.5uA. The loop filter circuit of C53, C54, R36 is used to set the loop corner frequency at 8-10 Hz.

RECEIVER ALIGNMENT is slightly different from the normal one. Firstly, ground the pin10 of MC13020 to force the receiver into the “Tuning Mode” Then turn the L1-3, CT3 and T4 (padding inductor) to the desired receiver local oscillation frequency coverage. The VCO1 coil of the T1 does not need to be accurately adjusted, because the frequency range of the VCO2 has been designed with wider frequency coverage than the usual one. In manufacturing, the recommended VCO1 coil of T1 (Figure-5) can be pre-adjusted at the centre position, where the T1 has better anti-vibration performance.

THE “TUNING LOCK SENSITIVITY” is indicated by the tuning lock LED1. Its threshold voltage is controlled by the level detector output pin4 of the MC13020 and can be slightly adjusted by the voltage divider of R12 and R24.
FIGURE 5. CIRCUIT DIAGRAM OF THE MANUAL-TUNED CAR AM STEREO RECEIVER
PRINCIPLE OF MICROPHONICS ELIMINATION. MC13021 is very effective in reducing phase modulation due to microphonics in the receiver. However, it cannot completely remove all effects, and care must be taken in the mechanical design to reduce microphonics as much as possible. In electrical design, the window width is a determinant factor; a wider window gives a better microphonics elimination effect. It is normally designed at ± 10K or more. When the VCO2 circuit has been selected, the window width is determined by the Q of the L-C resonant circuit at pin 11 of MC13021. To add two resistors in series and parallel with L1-3/T2 can lower the Q and obtain uniform and wider tuning window in whole receiving frequency range. VCO2 must use a coil with excellent anti-vibration performance and the TOKO coil TOKO0291CN-T1101Y is recommended for this application. The window width of the MC13021 affects the anti-vibration requirements for all relative components such as the tuner, VCO components and the mechanical parts. The overall frequency drift caused by vibration of components is required to be within the window or else the receiver will switch from stereo to mono mode. So, special attention must be given to the mechanical design, with rigid assembly technique, anti-vibration mounting, gluing and shielding techniques. The circuit of figure-5 gives approximate 60-80db of microphonics attenuation. If there is a more stringent requirement on anti-microphonics, a separate PCB for T1 and related VCO components should be mounted on an anti-vibration fixture.

PERFORMANCES OF THE APPLICATION DEMO SET (FIGURE-5) is shown as follows and the figure-8,9.

Test conditions: Vsupply = 12V, fc = 1MHz, fm = 1kHz, m = 30%, Vin = 74db u, Vout = 50mw, R=8 ohm.

<table>
<thead>
<tr>
<th>Frequency Coverage</th>
<th>1630 — 530 KHz.</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Signal Current</td>
<td>160 mA.</td>
</tr>
<tr>
<td>20db S/N Sens</td>
<td>20 uV.</td>
</tr>
<tr>
<td>S/N Ratio</td>
<td>mono 52 db.</td>
</tr>
<tr>
<td></td>
<td>stereo 48 db.</td>
</tr>
<tr>
<td>Separation (filtered 25Hz pilot)</td>
<td>30 db.</td>
</tr>
<tr>
<td>IF Rejection</td>
<td>38 db.</td>
</tr>
<tr>
<td>Image Rejection</td>
<td>40 db.</td>
</tr>
<tr>
<td>Audio Frequency Response (+/-10db)</td>
<td>300Hz — 6 Khz.</td>
</tr>
<tr>
<td>THD</td>
<td>mono 0.6 %</td>
</tr>
<tr>
<td></td>
<td>stereo 1 %</td>
</tr>
<tr>
<td>10% THD Output Power</td>
<td>3 W.</td>
</tr>
<tr>
<td>Tuning &quot;lock&quot; Sens</td>
<td>20 uv.</td>
</tr>
<tr>
<td>Stereo &quot;on&quot; Sens</td>
<td>20 uv.</td>
</tr>
<tr>
<td>Tweet 2 IF</td>
<td>26 db.</td>
</tr>
<tr>
<td>3 IF</td>
<td>30 db.</td>
</tr>
<tr>
<td>Overload (80% mod, 10% THD)</td>
<td>&gt;100 db</td>
</tr>
<tr>
<td>AGC</td>
<td>&gt;100 db</td>
</tr>
<tr>
<td>Microphonics elimination (electrical)</td>
<td>75 db.</td>
</tr>
</tbody>
</table>

Dummy ANT

![Diagram](image)
FIGURE 8. PERFORMANCES CHART-1
FIGURE 9. PERFORMANCE CHART-2

CHARACTERISTICS OF SENSITIVITY, S/N RATIO, AGC, DISTORTION, OVERLOAD CAPABILITY

INPUT SIGNAL LEVEL

AUDIO OUTPUT ODB = 0.63V

1 μV, 10 μV, 100 μV, 1 mV, 10 mV, 100 mV, 1 V

S+N+D
D+N
MONO
STEREO
AGC
REFERENCE

1. "Introduction to Motorola C-QUAM AM Stereo System”. M68413
2. "Manually Tuned Radio Considerations" Motorola AM Stereo Application Note No: M68435 by L. Ecklund
3. Motorola Data Sheet of MC13020 C-QUAM Decoder.
Get 600 Watts RF from Four Power FETs

This unique push-pull/parallel circuit produces a power output of four devices without the added loss and cost of power splitters and combiners. Motorola MRF150 RF power FET makes it possible to parallel two or more devices at relatively high power levels. This technique is considered impractical for bipolar transistors due to their low input impedance. In a common-source amplifier configuration, a power FET has approximately five to ten times higher input impedance than a comparable bipolar transistor in a common emitter circuit. The output impedance in both cases is determined by the dc supply voltage and power level. The limit to the number of FETs that can be paralleled is dictated by physical, rather than electrical restrictions, where the mutual inductance between the drains is the most critical aspect, limiting the upper frequency range of operation. The magnitude of these losses is relative to the impedance levels involved, limiting the upper frequency range of operation. Since the minimum mounting distance of the transistors is limited by the package size, the only real improvement would be a multiple die package. For higher frequency circuits, these mutual inductances could be used as a part of the matching network, but it would seriously limit the bandwidth of the amplifier. This technique is popular with many VHF bipolar designs.

In paralleling power FETs another important aspect must be considered: If the unity gain frequency (f<sub>u</sub>) of the device is sufficiently high, an oscillator will be created, where the paralleling inductances together with the gate and drain capacitances will form resonant circuits. The feedback is obtained through the drain to gate capacitance (C<sub>rss</sub>), which will result in 360° phase shift usually somewhere higher than the amplifier bandwidth. Thus, the oscillations may not be directly noticed in the amplifier output, but may have high amplitudes at the drains. This can be cured by isolating the paralleling inductance, which consists of the dc blocking capacitors (C7-C10, Figure 2) and their wiring inductance from the gates. Low value non-inductive resistors which do not appreciably affect the system gain can be used for this purpose.

CIRCUIT DESCRIPTION

Figure 2 shows a detailed schematic of the 600 W RF FET amplifier. It can be operated from supply voltages of 40 to 50 depending on linearity requirements. The bias for each device is independently adjustable, therefore no matching is required for the gate threshold voltages. Since the power gain of a MOSFET is largely dependent on the drain bias current, only g<sub>m</sub> matching is required, and it can be only ± 10%.
The circuit board was designed to allow several different gate biasing configurations (Figure 3). In circuit "a", which is used in the amplifier described here, D1 serves a purpose of preventing positive voltage from getting fed back to the bias source in case of a drain-gate short in a FET. This protects the other three devices from gate overvoltage. C1-R2 combination establishes an RF shunt from the gate to ground, which is required with D1 preventing an open circuit in one direction. R3 is a low value resistor to prevent parasitic oscillations in a parallel FET circuit, as discussed earlier. Variations "b" and "c" are basically the same, except for R2, which can be used to control the amount of RF rectified by D1. In addition to blocking the dc in one direction, D1 can be used for proportional biasing, in which the bias voltage increases with RF drive. This allows the initial idle current to be set to a lower than normal value, increasing the system efficiency.
The gate de-Qing in these circuits is done with R4. Circuit “d” is another variation, where D1 is moved in series with R1 eliminating R4. The value of R1 must be high to prevent destruction from a drain-gate short. The common bias is derived from IC1 (MC1723CP) which provides both line and load regulation. The line voltage regulation is defeated when the voltage to Pin 12 falls below 24 V, and the bias input can be used for Automatic Level Control (ALC) shut-down or linear ALC function. The regulator output voltage is adjustable from 0.5 to 9.0 volts with R5, which can be permanently set to 7.0–8.0 V. This voltage is also controlled by the combination of R10 and R25. R25 is a thermistor, and is tied to the heat sink for bias temperature compensation.

In Figure 2, the input from T1 is fed to the gates through C7-C10 and R15-R18. The input matching is initially done at the high end of the band (30 MHz). In contrast to a bipolar push-pull circuit, where the base-to-base impedance varies with class of operation, the gate-to-gate impedance of a common source FET circuit is always twice that from gate to ground. In this case, where two FETs are in parallel on each side, the gate-to-gate impedance equals the gate-to-ground impedance of one device. From the Smith chart information (Figure 4) this can be established as 3.45 ohms.
The effect of R11-R14 and R21-R24 is minimal and can be disregarded. Considering the standard integers for T1 impedance ratio, 9:1 with its 5.55 ohms secondary appears to be the closest. This would set the values of R15-R18 at 2.0 ohms each, which would result in 3.5 dB gain loss, and about 1.0 W would be dissipated in each resistor. For this reason it was decided to reduce their values to 1.0 ohm, and trim the values of C1 and C2 for lowest input VSWR. As a trade-off, the VSWR will peak slightly at 15-20 MHz, but still remain below 2:1.

Negative feedback is derived from a winding in T2 through R19 and R20. Its purpose is to equalize the load impedance for T1 and reduce the amplifier gain at low frequencies. Since the gate to source capacitance of a MOSFET is fairly constant with frequency, the amount of feedback voltage is inversely proportional to its reactance. This function should be more or less linear, unless the inductive reactance of T1 is too low, or if resonances occur somewhere in the circuit. No computer analysis (as in Reference 2) was performed on the negative feedback system. Instead a simple approach described in Reference 1 was taken, where the gain difference between 2.0 and 30 MHz determines the feedback voltage required to equalize the voltages of the secondary of T1 at these frequencies. With an input impedance of 45 ohms at 2.0 MHz, and the feedback source delivering 15 V(RMS) (Pout = 600 W) the values of R19 and R20 will be around 10 ohms each.

A ferrite toroid or a two hole balun type core can be used for T2. Relatively low µi material with high curie temperature is recommended, since the minimum inductance requirement for the dc feed winding is less than 2.0 µH. Depending on the material, T2 can reach temperatures of 200-250°C, which the wire insulation must also be able to withstand. Several different output transformer configurations (T3) were tried, including a transmission line type in Figure 5. Although difficult to make, it has the advantage that low µ, low loss ferrite can be used with multiple turn windings. At this power level, heat in the output transformer was a major problem. High permeability materials, required in the metal tube and ferrite sleeve transformers could not be used because of their higher losses and low curie temperature. On the other hand, low µ cores with larger cross sectional areas were not readily available. To reach the minimum inductance required for 2.0 MHz, two of these transformers, with low permeability ferrite cores were connected in series. Both have 9:1 impedance ratios. Alternatively the secondaries can be connected in parallel with twice the number of turns (6) in each. C11 must withstand high RF currents, and must be soldered directly across the transformer primary connections. Regular mica or ceramic capacitors cannot be used, unless several smaller values are paralleled.

**PERFORMANCE**

Due to the mechanical proximity of the four MOSFET devices, the RF ground of the circuit board is poor, and results in 1.0-1.5 dB gain loss at 30 MHz, which can be seen in Figure 6. The ground plane can be improved by connecting all source leads together with a metal strap over the transistor caps. Another method is to place solder lugs under each transistor mounting screw, and solder each one to the nearest source lead. In this case, the heat sink will serve as the RF ground. Although the 3rd order IM distortion is not exceptionally good, (Figures 6, 7) the worst case 5th order

![Figure 5 - Number of Turns Shown is not Actual](image-url)
products are better than -30 dB at all frequencies, and as can be expected with FETs, the 9th and higher order products are in the -50 to -60 dB level. It can also be noticed from Figure 6, that the IMD does not increase at reduced power levels, as common with bipolar amplifiers. The even order output harmonic content depends greatly on the device balance as in any push-pull circuit. The worst case is at the low frequencies, where numbers like -30 to -40 dB for the 2nd harmonic is typical. The highest 3rd harmonic amplitude of -12 dB is at 6.0-8.0 MHz carrier frequency. Information on suitable harmonic filters is available in Reference 3. The stability of the amplifier has been tested into a 3:1 load mismatch at all phase angles. It was found to be completely stable, even at reduced supply voltages.

In a MOSFET (common source) the ratio of feedback capacitance to the input impedance is several times higher than that of a bipolar transistor (common emitter). As a result, a properly designed FET circuit should be inherently more stable, especially under varying load conditions. It must be noted, that special attention must be given to the heat sink design for this unit. With the 200-300 watts of heat generated by the transistors in a small physical area, it must be conducted into a heat sink efficiently. This can be only done with high conductance material, such as copper. If aluminum heat sink is used, a copper heat spreader is recommended between the transistor flanges and the heat sink surface.

FIGURE 6

FIGURE 7
FIGURE 8 — Component Locations (not full size)

X denotes feed-through eyelets
X denotes terminal pins
O denotes board spacers
FIGURE 9 — Circuit Board Photo Master (not full size)
REFERENCES
1. "A Two-Stage 1.0 kW Solid-State Linear Amplifier," AN-758, Motorola Semiconductor Products, Inc.
2. "Low-Distortion 1.6 to 30MHz SSB Driver Designs," AN-779, Motorola Semiconductor Products, Inc.

BIBLIOGRAPHY
2. Wetherhold, Low-Pass Filters for Amateur Radio Transmitters, QST, Dec., 1979
Low Cost UHF Device Gives Broadband Performance at 3.0 Watts Output

INTRODUCTION
The major cost element in low-to-medium power (1.0–5.0 W) RF transistors is the package. Several years ago Motorola took a major step in limiting cost increases by introducing the common emitter TO-39 package. Through the use of appropriate circuit design and construction techniques, use of the CE TO-39 can be extended to broadband UHF amplifiers producing up to 3.0 W output power.

This bulletin describes a broadband circuit application of the low cost MRF630 — an all gold metallized, emitter ballasted, high figure of merit transistor capable of 3.0 W output power with 10 dB gain at 512 MHz. A photo of the amplifier is shown in Figure 1. Emphasis is placed on mounting techniques which minimize parasitic inductances and maximize heat transfer.

CONSTRUCTION
TO-39’s used as RF amplifiers are most commonly found in transmitter exciter chains mounted on printed circuit boards. The parts are seated on small disc shaped insulators and are heatsunk using press-fit “top hat” style radiators (Figure 2). Heat is inefficiently conducted upwards through the metal can (Figure 3) and radiated by commercially available heatsinks, called “top hats”. As a result, the $T_J$ is excessive, causing elevated junction temperatures and thermal slump problems. Because the TO-39 is situated above the PC board resulting in long leads, input Q’s are also excessive and combine to limit broadband performance and device gain. In low power applications (<1.0 W) and VHF frequencies or lower, the problems mentioned above may not be noticeable. Higher power devices
such as the MRF630, however, should be treated with the same considerations as any other RF power transistor (i.e., provisions for proper heatsinking and grounding).

When using an SOE power transistor, heatsinking is simplified with the inclusion of a stud or flange. Since TO-39’s have neither, some modifications are required. Figure 4 depicts a means of heatsinking by soldering a “flange” to the bottom side of the TO-39 package, thus providing a path for heat flow directly beneath the transistor die. The “flange” is secured to the amplifier heatsink by one or two screws. With this arrangement, maximum heat dissipation can be provided with a minimum amount of space consumption. This method also creates better electrical grounding as the package is now mechanically connected to chassis ground. The attachment of this “flange” provides improvements in both grounding and heatsinking. Both are fundamental requirements to obtain the expected performance from an RF power TO-39 such as the MRF630.

CIRCUIT DESCRIPTION

The circuit, which was optimized for the MRF630, uses a distributed element design. Tight tolerance control is achieved by substituting transmission lines for inductors and specifying capacitor placement carefully. With this approach, good broadband performance is possible.

Since transmission line characteristics are dependent on line widths, dielectric properties and circuit board thickness, glass teflon circuit board is generally selected, as it offers the best tolerance control over the latter two variables. The major drawbacks of glass teflon circuit board are its low dielectric constant and relatively high price. A less expensive alternative, which was used in the construction of the MRF630 amplifier, is G10 printed circuit board. Its lower price coupled with its higher dielectric constant results in a smaller circuit and lower overall cost. The dielectric constant of G10 is not a controlled parameter, yet G10 is consistent enough to be useful for many applications at UHF frequencies.
"Mini" clamped mica capacitors were chosen for the matching components in this amplifier design because of their low cost, availability and very high "Q". Mica is an extremely good dielectric and these capacitors, if carefully soldered (minimizing capacitor series lead inductance), boast a higher series resonant frequency than some chip capacitors.

The use of G10 printed circuit board, "mini" clamped mica capacitors and the MRF630, enhance component repeatability, affordability, and availability.

**PERFORMANCE**

Broadband circuit performance is displayed in Figure 5 and a typical gain curve is shown in Figure 6. As can be seen, the MRF630 has excellent turn-on characteristics and saturated power capability. The normal gain roll-off above 490 MHz is expected but was minimized by optimizing both input and output impedance matching networks above that frequency. By adding additional matching sections, broadband performance down to 400 MHz could be achieved with respectable input VSWR's.

With the addition of the copper "flange" in the circuit assembly, average device $\theta_J$-HS was limited to 12.3°C/W (dissipated power = 4.0 W, $T_C = 60^\circ$C). The MRF630 was also mounted directly to the bottom of the printed circuit board, which was placed directly against the heatsink. The $\theta_J$-HS degraded to only 15.6°C/W under the same conditions of power dissipation. If the PC board were "floating" using the same technique, higher $\theta_J$-HS's would be observed. Assuming all circuit components were to be mounted in stripline fashion, allowing the PC board to be mounted directly to the heatsink, adequate heatsinking could be obtained without the addition of the "flange". The copper "flange" method of heatsinking is highly recommended for standard printed circuit boards which are isolated from the chassis heatsink.

An exploded view of the amplifier showing printed circuit board, flange and heatsink is shown in Figure 7. Figure 8 is a circuit schematic including parts list, while Figure 9 shows details of part location on the PC board. Finally, as an aid to duplication of the amplifier described herein, Figure 10 is a 1:1 photo master of the printed circuit board.

**SUMMARY**

Outlined in this article are methods of assuring the best possible performance from a low cost package; specifically, the MRF630 TO-39. If good construction practices are followed to ensure proper heatsinking and grounding, performance comparable to an SOE can be demonstrated, taking advantage of the cost benefits offered by a TO-39.
FIGURE 7 — Exploded View of Amplifier Assembly

4-40×1/4" Screw
PC Board

Flange/Transistor Assembly
Heatsink Block

FIGURE 8 — Circuit Schematic and Parts List

FIGURE 9 — Parts Layout (not full size)

C1 C3 — 10 µF Mini-Unelco
C2 — 36 µF Mini-Unelco
C4, C5 — 0.018 µF Chip Capacitor
C6 — 0.1 µF Dipped Capacitor
C7 — 1.0 µF Electrolytic
R1 — 12 Ω — 1/4 W Resistor

RFC1 — 0.15 µH Mini-Molded Choke
RFC2 — 1.0 µH Mini-Molded Choke
RFC3 — 0.15 µH Molded Choke
TL1 — Transmission Line 0.105 × 1.110" (W × L)
TL2 — Transmission Line 0.053 × 0.987" (W × L)
Board Material — 2 Oz. 0.0625" Epoxy Fiberglass (G-10)

FIGURE 10 — Photo Master (not full size)

• Denotes copper eyelets.
• Denotes 4-40 clearance for 4-40 screw mounting.
Additional Information
Additional Information

Additional information relevant to Radio, RF and Video applications may be found in the following Motorola documents, available through your Franchised Distributor by quoting the appropriate reference.

- BR396/D: Discrete Military Products – Chips
- BR503/D: Surface Mount MOS Digital-Analog: Special Functions & Telecommunications (rev. 1)
- BRE262/D: Motorola’s Video/Graphics Peripherals
- BRE316R1/D: TMOS Power FET Design Ideas
- BRE372/D: ECLIPS Mini Data Book
- BRE378/D: UnitPAK Packaging
- BRE504/D: Electronic Tuning Address Systems
- DL110/D: RF Device Data (2 volume set, rev. 4, 1990)
- DL122/D: MECL Device Data (rev. 4)
- DL126/D: Small-Signal Transistors, FETs and Diodes (rev. 2)
- DL128/D: Linear and Interface Integrated Circuits (rev. 3)
- DL130/D: CMOS Application-Specific Standard ICs (rev. 1)
- DL140/D: ECLinPS Device Data (rev. 1, 1991)
- DL148/D: Discrete Military Operations Data
- DL411/D: Communications Applications Manual
- HB205/D: MECL System Design Handbook (rev. 1)
- SG77/D: MECL Selector Guide (rev. 6, 1983)
- SG99/D: MOS Application-Specific Standard ICs Selector Guide (rev. 3)
- SG132/D: Small-Signal Transistors, FETs and Diodes Selector Guide
- SG138/D: Military IC & Discrete Selector Guide
- SG139/D: Surface Mount Discrete Products Selector Guide & Cross Reference
- SGE102R1/D: CMOS System IC Selection Guide
- SGE112/D: Cross Reference for NEC-to-Motorola RF Transistors