NON-VOLATILE MEMORY
PRODUCTS DATA BOOK

1998

MICROCHIP

NON-VOLATILE MEMORY PRODUCTS DATA BOOK

1998

MICROCHIP

The Embedded Control Solutions Company®

MICROCHIP

Non-Volatile Memory Data Book 1998 Edition

DATA SHEET MARKINGS

Microchip uses various data sheet markings to designate each document phase as it relates to the product development stage. The markings appear at the bottom of the data sheet, between the copyright and document and page numbers. The definitions for each marking are provided below for your use.

Marking	Description
Advance Information	The information is on products in the design phase. Your designs should not be finalized with this information as revised information will be published when the product becomes available.
Preliminary	This is preliminary information on new products in production but not yet fully characterized. The specifications in these data sheets are subject to change without notice. Before you finalize your design, please ensure that you have the most current revision of the data sheet by contacting your Microchip sales office, representative or distributor.
No Marking	Information contained in the data sheet is on products in full production.

MICROCHIP

Table of Contents

PAGE

SECTION 1 MICROCHIP TECHNOLOGY INC. COMPANY PROFILE

	Company Profile	1-1
	Product Line Card	1-10

SECTION 2 MEMORY PRODUCTS SELECTION AND CROSS REFERENCE

Serial EEPROMs	Serial EEPROM Selection Guide	2-1
	Serial EEPROM Cross Reference Guide	2-5
Parallel EPROMs	Parallel EEPROM Selection Guide	2-15
EPROMs	EPROM Selection Guide	2-17
	EPROM Cross Reference Guide	2-19

SECTION 3 I^2C^{TM} SERIAL EEPROM PRODUCT SPECIFICATIONS

24AA00	128 Bit 1.8V I^2C^{TM} Bus Serial EEPROM	3-1
24LC00	128 Bit 2.5V I^2C^{TM} Bus Serial EEPROM	3-1
24C00	128 Bit 5V I^2C^{TM} Bus Serial EEPROM	3-1
24C01C	1K 5.0V I^2C^{TM} Serial EEPROM	3-11
24AA01	1K 1.8V I^2C^{TM} Serial EEPROM	3-21
24LC01B	1K 2.5V I^2C^{TM} Serial EEPROM	3-29
24C01SC	1K 5.0V I^2C^{TM} Serial EEPROMs for Smart Cards	3-37
24LCS61	1K Software Addressable I^2C^{TM} Serial EEPROM	3-47
24AA02	1K 1.8V I^2C^{TM} Serial EEPROM	3-21
24LC02B	2K 2.5V I^2C^{TM} Serial EEPROM	3-29
24C02C	2K 5.0V I^2C^{TM} Serial EEPROM	3-61
24C02SC	2K 5.0V I^2C^{TM} Serial EEPROMs for Smart Cards	3-37
24LCS52	2K 2.5V I^2C^{TM} Serial EEPROM with Software Write Protect	3-71
24LC024	2K 2.5V I^2C^{TM} Serial EEPROM	3-81
24LC025	2K 2.5V I^2C^{TM} Serial EEPROM	3-81
24LCS62	2K Software Addressable I^2C^{TM} Serial EEPROM	3-47
24AA04	4K 1.8V I^2C^{TM} Serial EEPROM	3-91
24LC04B	4K 2.5V I^2C^{TM} Serial EEPROM	3-99
24C04A	4K 5.0V I^2C^{TM} Serial EEPROM	3-107
24AA08	8K 1.8V I^2C^{TM} Serial EEPROM	3-91
24LC008B	8K 2.5V I^2C^{TM} Serial EEPROM	3-99
24C08B	8K 5.0V I^2C^{TM} Serial EEPROM	3-117
24AA16	16K 1.8V I^2C^{TM} Serial EEPROM	3-125
24C16B	16K 5.0V I^2C^{TM} Serial EEPROM	3-117
24LC16B	16K 2.5V I^2C^{TM} Serial EEPROM	3-133
24AA164	16K 1.8V Cascadable I^2C^{TM} Serial EEPROM	3-141
24LC164	16K 2.5V Cascadable I^2C^{TM} Serial EEPROM	3-149
24AA174	16K 1.8V Cascadable I^2C^{TM} Serial EEPROM with OTP Security Page	3-157
24LC174	16K 2.5V Cascadable I^2C^{TM} Serial EEPROM with OTP Security Page	3-167
24AA32A	32K 1.8V I^2C^{TM} Serial EEPROM	3-177
24LC32A	32K 2.5V I^2C^{TM} Serial EEPROM	3-187
24C32A	32K 5.0V I^2C^{TM} Serial EEPROM	3-197
24AA32	32K 1.8V I^2C^{TM} Smart Serial™ EEPROM	3-207
24LC32	32K 2.5V I^2C^{TM} Smart Serial™ EEPROM	3-219
24C32	32K 5.0V I^2C^{TM} Smart Serial EEPROM	3-231
24FC32	32K 5.0V 1 MHz I^2C^{TM} Smart Serial™ EEPROM	3-243
24AA64	64K 1.8V I^2C^{TM}CMOS Serial EEPROM	3-255
24LC64	64K 2.5V I^2C^{TM}CMOS Serial EEPROM	3-255
24AA65	64K 1.8V I^2C^{TM} Smart Serial™ EEPROM	3-265
24LC65	64K 2.5V I^2C^{TM} Smart Serial™ EEPROM	3-277

Table of Contents

		PAGE
24C65	64K 5.0V I²C™ Smart Serial™ EEPROM	3-289
24FC65	64K 5.0V 1 MHz I²C™ Smart Serial™ EEPROM	3-301
24AA128	128K 1.8V I²C™CMOS Serial EEPROM	3-313
24LC128	128K 2.5V I²C™CMOS Serial EEPROM	3-313
24AA256	256K 1.8V I²C™CMOS Serial EEPROM	3-323
24LC256	256K 2.5V I²C™CMOS Serial EEPROM	3-323

SECTION 4 MICROWIRE® SERIAL EEPROM PRODUCT SPECIFICATIONS

93AA46	1K 1.8V Microwire® Serial EEPROM	4-1
93LC46A	1K 2.5V Microwire® Serial EEPROM	4-11
93LC46B	1K 2.5V Microwire® Serial EEPROM	4-11
93C46B	1K 5.0V Microwire® Serial EEPROM	4-19
93AA56	2K 1.8V Microwire® Serial EEPROM	4-1
93LC56A	2K 2.5V Microwire® Serial EEPROM	4-27
93LC56B	2K 2.5V Microwire® Serial EEPROM	4-27
93C56A	2K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-35
93C56B	2K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-35
93LCS56	2K 2.5V Microwire® Serial EEPROM with Software Write Protect	4-43
93AA66	4K 1.8V Microwire® Serial EEPROM	4-1
93LC66A	4K 2.5V Microwire® Serial EEPROM	4-55
93LC66B	4K 2.5V Microwire® Serial EEPROM	4-55
93C66A	4K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-63
93C66B	4K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-63
93LCS66	4K 2.5V Microwire® Serial EEPROM with Software Write Protect	4-43
93AA76	8K 1.8V Microwire® Serial EEPROM	4-71
93LC76	8K 2.5V Microwire® Serial EEPROM	4-81
93C76	8K 5.0V Microwire® Serial EEPROM	4-91
93AA86	16K 1.8V Microwire® Serial EEPROM	4-71
93LC86	16K 2.5V Microwire® Serial EEPROM	4-81
93C86	16K 5.0V Microwire® Serial EEPROM	4-91

SECTION 5 SPI™ SERIAL EEPROM PRODUCT SPECIFICATIONS

25AA040	4K SPI™ Bus Serial EEPROM	5-1
25LC040	4K SPI™ Bus Serial EEPROM	5-1
25C040	4K SPI™ Bus Serial EEPROM	5-1
25AA080	8K SPI™ Bus Serial EEPROM	5-13
25LC080	8K SPI™ Bus Serial EEPROM	5-13
25C080	8K SPI™ Bus Serial EEPROM	5-13
25AA160	16K SPI™ Bus Serial EEPROM	5-25
25LC160	16K SPI™ Bus Serial EEPROM	5-25
25C160	16K SPI™ Bus Serial EEPROM	5-25
25LC320	32K SPI™ Bus Serial EEPROM	5-37
25C320	32K SPI™ Bus Serial EEPROM	5-37
25AA640	64K SPI™ Bus Serial EEPROM	5-49
25LC640	64K SPI™ Bus Serial EEPROM	5-49
25C640	64K SPI™ Bus Serial EEPROM	5-49

MICROCHIP

Table of Contents

		PAGE
SECTION 6	**ID SOLUTIONS AND PLUG AND PLAY® PRODUCTS**	
24AA00	128 Bit I²C™ Bus Serial EEPROM	3-1
2424LC00	128 Bit I²C™ Bus Serial EEPROM	3-1
2424C00	128 Bit I²C™ Bus Serial EEPROM	3-1
24LCS61	1K Software Addressable I²C™ Serial EEPROM	3-47
24LC21	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-1
24LC21A	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-13
24LCS21	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-27
24LCS21A	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-39
24LC41	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-53
24LC41A	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-65
24LCS41	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-79
24LCS41A	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-91
24LCS52	2K 2.5V I²C™ Serial EEPROM with Software Write Protect	3-71
24LCS62	2K Software Addressable I²C™ Serial EEPROM	3-47
SECTION 7	**PARALLEL EEPROM PRODUCT SPECIFICATIONS**	
28C04A	4K (512 x 8) CMOS EEPROM	7-1
28C16A	16K (2K x 8) CMOS EEPROM	7-9
28C17A	16K (2K x 8) CMOS EEPROM	7-17
28C64A	64K (8K x 8) CMOS EEPROM	7-25
28LV64A	64K (8K x 8) Low Voltage CMOS EEPROM	7-33
SECTION 8	**EPROM PRODUCT SPECIFICATIONS**	
27C64	64K (8K x 8) CMOS EPROM	8-1
27LV64	64K (8K x 8) Low-Voltage CMOS EPROM	8-9
27C128	128K (16K x 8) CMOS EPROM	8-17
27C256	256K (32K x 8) CMOS EPROM	8-25
27LV256	256K (32K x 8) Low-Voltage CMOS EPROM	8-33
27C512A	512K (64K x 8) CMOS EPROM	8-41
37LV36/65/128	36K, 64K, and 128K Serial EPROM Family	8-49
SECTION 9	**DEVELOPMENT TOOL S**	
On-Line Support	Microchip Internet Connections	9-1
Total Endurance™	Microchip Serial EEPROM Endurance Model	9-3
	Microchip Serial EEPROM Designer's Kit	9-5
SECTION 10	**QUALITY, RELIABILITY, AND ENDURANCE**	
Product Quality		10-1
Product Reliability		10-9
EEPROM Endurance		10-19

Table of Contents

PAGE

SECTION 11 PACKAGING

Commercial/Industrial Outlines and Parameters 11-1
Product Tape and Reel Specifications 11-59
Overview of Microchip Die/Wafer Support 11-61

SECTION 12 WORLDWIDE SALES ADDRESS LISTINGS

Factory Representatives 12-1
Distributors 12-7
Factory Sales 12-21

SECTION 1
MICROCHIP TECHNOLOGY INC. COMPANY PROFILE

Company Profile 1-1
Product Line Card 1-10

Microchip Technology Inc.

Company Profile

The Embedded Control Solutions Company®

Since its inception, Microchip Technology has focused its resources on delivering innovative semiconductor products to the global embedded control marketplace. To do this, we have focused our technology, engineering, manufacturing and marketing resources on two synergistic product lines: PICmicro™ 8-bit microcontrollers (MCUs) and high-endurance Serial EEPROMs. Today, Microchip's expanding product portfolio is aimed at delivering a more comprehensive array of high-value solutions to a growing base of customers.

Highlights

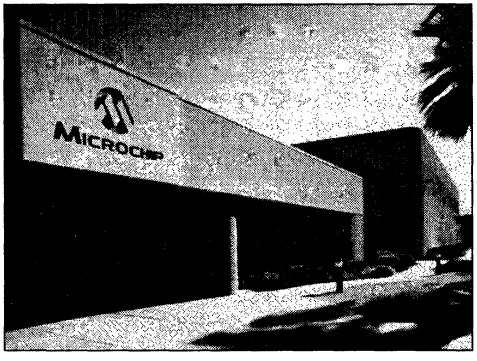
Inside Microchip Technology you will find:

- An experienced executive team focused on innovation and committed to listening to our customers
- A focus on providing high-performance, cost-effective embedded control solutions
- A Complete Product Solution including:
  - 8-bit RISC OTP, *Enhanced* FLASH, EEPROM and ROM MCUs
  - Patented KEELOQ® code hopping technology products
  - A full family of leadership Serial EEPROM products plus Parallel EEPROMs and EPROMs
  - A variety of end-user Application-Specific Standard Products (ASSP)
  - A full line of easy-to-use development tools
- Fully integrated manufacturing capabilities
- A global network of manufacturing and customer support facilities
- A unique corporate culture dedicated to continuous improvement
- Distributor network support worldwide including certified distribution FAEs

Business Scope

Microchip Technology Inc. manufacturers and markets a variety of VLSI CMOS semiconductor components to support the market for cost-effective embedded control solutions. In particular, we specializes in highly integrated, field-programmable RISC MCUs, application-specific standard products, secure data products, application-specific integrated circuits and related Serial EEPROM memory products to meet growing market requirements for high performance, yet economical embedded control capability in products. Microchip's products feature the industry's most economical One-Time-Programmable (OTP) EPROM, reprogrammable Flash and EEPROM, and ROM capability, along with the compact size, integrated functionality, ease of development and technical support so essential to timely and cost-effective product development by our customers.

Chandler, Arizona: Company headquarters near Phoenix, Arizona; executive offices, R&D and wafer fabrication occupy this 242,000-square-foot multi-building facility.



Tempe, Arizona: Microchip's 170,000-square-foot wafer fabrication facility provides increased manufacturing capacity today and for the future.

Microchip Technology Inc.

Market Focus

Microchip targets select markets where our advanced designs, progressive process technology and industry-leading product performance enables us to deliver decidedly superior performance. Our company is positioned to provide a complete product solution for embedded control applications found throughout the consumer, automotive, telecommunication, office automation and industrial control markets. Microchip products are also meeting the unique design requirements of targeted embedded applications including security, battery management and field-programmable gate array conversions.

Certified Quality Systems

Microchip received ISO 9001 Quality System certification for its worldwide headquarters and wafer fabrication facilities in January 1997. Our field-programmable 8-bit MCUs, Serial EEPROMs, related specialty memory products and development systems conform to the stringent quality standards of the International Standards Organization (ISO).

DNV Certification, Inc. USA
DNV MSC The Netherlands Accredited by the RvA
ACCREDITED REGISTRAR ANSI-RAB
DNV
ISO 9001 REGISTERED FIRM

Our assembly and test facility in Kaohsiung, Taiwan is ISO 9002 certified. In addition, Microchip's manufacturing and engineering systems were audited to meet the Automotive Electronics Council A100 guidelines for overall quality, reliability and demonstrated conformance to the requirements of QS-9000.

Fully Integrated Manufacturing

Microchip delivers fast turnaround and consistent quality through total control over all phases of production. Research and development, design, mask making, wafer fabrication, and the major part of assembly and quality assurance testing are conducted at facilities wholly-owned and operated by Microchip. Our integrated approach to manufacturing along with rigorous use of advanced Statistical Process Control (SPC) and a continuous improvement culture has resulted in high and consistent yields which have positioned Microchip as a quality leader in its global markets. Microchip's unique approach to SPC provides customers with excellent pricing, quality, reliability and on-time delivery.

Bangkok, Thailand: Microchip's 140,000-square-foot manufacturing facility houses the technology and assembly/test equipment for high speed testing and packaging.

A Global Network of Plants and Facilities

Microchip is a global competitor providing local services to the world's technology centers. The company's design and technology advancement facilities, and wafer fabrication sites are located in Chandler and Tempe, Arizona.

The Tempe facility provides an additional 170,000 square feet of manufacturing space that meets the increased production requirements of a growing customer base, and provides production capacity which more than doubles that of Chandler.

Microchip facilities in Kaohsiung, Taiwan; Bangkok, Thailand; and Shanghai, China, serve as the foundation of Microchip's extensive assembly and test capability located throughout the Far East. The use of multiple fabrication, assembly and test sites, with over 600,000-square-feet of facilities worldwide, ensures Microchip's ability to meet the increased production requirements of a fast growing customer base.

Microchip supports its global customer base from direct sales and engineering offices in Asia, North America, Europe and Japan. Offices are staffed to meet the high quality expectations of our customers, and can be accessed for technical and business support. The Company also franchises more than 40 distributors and a network of technical manufacturer's representatives serving 24 countries worldwide.

Embedded Control Overview

Unlike "processor" applications such as personal computers and workstations, the computing or controlling elements of embedded control applications are embedded inside the application. The consumer is only concerned with the very top-level user interface such as keypads, displays and high-level commands. Very rarely does an end-user know (or care to know) the embedded controller inside (unlike the conscientious PC users, who are intimately familiar not only with the processor type, but also its clock speed, DMA capabilities and so on).

It is, however, most vital for designers of embedded control products to select the most suitable controller and companion devices. Embedded control products are found in all market segments: consumer, commercial, PC peripherals, telecommunications (including personal telecom products), automotive and industrial. Most embedded control products must meet special requirements: cost effectiveness, low-power, small-footprint and a high level of system integration.

Typically, most embedded control systems are designed around a MCU which integrates on-chip program memory, data memory (RAM) and various peripheral functions, such as timers and serial communication. In addition, these systems usually require complementary Serial EEPROM, display drivers, keypads or small displays.

Microchip has established itself as a leading supplier of field-programmable embedded control solutions. The combination of high-performance MCUs from the PIC12CXXX, PIC16C5X, PIC16CXXX and PIC17CXXX families, along with non-volatile memory products, provide the basis for this leadership.

Microchip is committed to continuous innovation and improvement in design, manufacturing and technical support to provide the best possible embedded control solutions to you.

PICmicro MCU Overview and Roadmap

Microchip PICmicro MCUs combine high-performance, low-cost, and small package size, offering the best price/performance ratio in the industry. More than 120 million of these devices ship each year to cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

Microchip offers four families of 8-bit MCUs to best fit your needs: PIC16C5X 12-bit program word, PIC16CXXX 14-bit program word, PIC17CXXX 16-bit program word and PIC12CXXX 8-pin 12-bit/14-bit program word MCU families.

All families offer OTP, low-voltage and low-power options, with a variety of package options. Selected members are available in ROM or reprogrammable Flash versions.

The widely-accepted PIC16C5X, PIC16CXXX and PIC17CXXX MCU families employ a modified RISC architecture. Today, these families are joined by the industry's first and only 8-pin MCU family – the PIC12CXXX. The PIC12CXXX family combines the 8-bit high-speed RISC architecture of the PICmicro MCUs with the smallest footprint MCU. Microchip pioneered the use of RISC architecture to obtain high speed and instruction efficiency.

PIC12CXXX: 8-Pin, 8-Bit Family

The PIC12CXXX family packs Microchip's powerful RISC-based PICmicro architecture into 8-pin DIP and SOIC packages. These PIC12CXXX products are available with either a 12-bit or 14-bit wide instruction set, a low operating voltage of 2.5V, small package footprints, interrupt handling and a deeper hardware stack. All of these features provide an intelligence level not previously available in applications because of cost or size considerations.

PIC16C5X: 12-Bit Architecture Family

The PIC16C5X is the well established base-line family which offers the most cost-effective solution. These PIC16C5X products have a 12-bit wide instruction set and are currently offered in 18-, 20- and 28-pin packages. In the SOIC and SSOP packaging options, these are among the smallest footprint MCUs. Low-voltage operation, down to 2.0V for OTPs, make this family ideal for battery operated applications.

PIC16CXXX: 14-Bit Architecture Family

The PIC16CXXX family offers a wide-range of options, from 18-pin to 68-pin packages as well as low to high levels of peripheral integration. This family has a 14-bit wide instruction set, interrupt handling capability and a deep, 8-level hardware stack. The PIC16CXXX family provides the performance and versatility to meet the more demanding requirements of todays cost-sensitive marketplace for mid-range 8-bit applications.

The PIC14C000 Programmable Mixed-Signal Controller allows engineers to design intelligent controllers for smart batteries, battery chargers, battery status monitoring, uninterruptible power supplies, HVAC, and other data acquisition and processing required for managing energy. The PIC14C000 can support any battery technology including Li Ion, NiMH, NiCd, Pb acid, Zinc Air. In addition, the product's I^2C™ port enables any system OEM, battery pack VAR, and battery manufacturer to design, build, and market SBD-compliant products supporting the System Management Bus standard.

PIC17CXXX: 16-Bit Architecture Family

The PIC17CXXX family offers the world's fastest execution performance of any 8-bit MCU family in the industry. The PIC17CXXX family extends the PICmicro MCU's high-performance RISC architecture with a 16-bit instruction word, enhanced instruction set and powerful vectored interrupt handling capabilities. A powerful array of precise on-chip peripheral features provide the performance for the most demanding 8-bit applications.

The Mechatronics Revolution and the World's first 8-pin MCU

We are living through a revolutionary period that is impacting almost every aspect of our lives. The nature of the revolution is the momentous shift from analog/electro-mechanical timing and control to digital electronics. It is called the Mechatronics Revolution, and it is being staged in companies throughout the world, with design engineers right on the front lines: Make it smarter, make it smaller, make it do more, make it cost less to manufacture – and make it snappy.

To meet the needs of this growing customer base, Microchip is rapidly expanding its already broad line of 8-bit PICmicro MCUs. The most recent addition, the PIC12CXXX family, is a major breakthrough – it's the world's only 8-bit OTP MCU with just 8-pins. Their size opens up new possibilities for product design.

PICmicro MCU Naming Convention

The PICmicro architecture offers users a wider range of cost/performance options than any 8-bit MCU family.

In order to identify the families, the following naming conventions have been applied to the PICmicro MCUs.

TABLE 1: PICmicro MCU NAMING CONVENTION*

Family		Architectural Features	Name	Technology
PIC17CXXX	8-bit High-Performance MCU Family	• 16-bit wide instruction set • Internal/external vectored interrupts • DC - 33 MHz clock speed • 120 ns instruction cycle (@ 33 MHz) • Hardware multiply	PIC17C4X	OTP program memory, digital only
			PIC17CR4X	ROM program memory, digital only
			PIC17C75X	OTP program memory with mixed-signal functions
			PIC17C76X	OTP program memory with mixed-signal functions
PIC16CXXX	8-bit Mid-Range MCU Family	• 14-bit wide instruction set • Internal/external interrupts • DC - 20 MHz clock speed (Note 1) • 200 ns instruction cycle (@ 20 MHz)	PIC14CXXX	OTP program memory with A/D and D/A functions
			PIC16C55X	OTP program memory, digital only
			PIC16C6X	OTP program memory, digital only
			PIC16CR6X	ROM program memory, digital only
			PIC16C62X	OTP program memory with comparators
			PIC16CE62X	OTP program memory with comparators and EEPROM data memory
			PIC16C64X	OTP program memory with comparators
			PIC16C66X	OTP program memory with comparators
			PIC16C7X	OTP program memory with analog functions (i.e. A/D)
			PIC16F8X	Flash program and EEPROM data memory
			PIC16CR8X	ROM program and EEPROM data memory
			PIC16C9XX	OTP program memory, LCD driver
PIC16C5X	8-bit Base-Line MCU Family	• 12-bit wide instruction set • DC - 20 MHz clock speed • 200 ns instruction cycle (@ 20 MHz)	PIC16C5X PIC16C5XA	OTP program memory, digital only
			PIC16CR5X PIC16CR5XA	ROM program memory, digital only
PIC12CXXX	8-bit, 8-pin MCU Family	• 12- or 14-bit wide instruction set • DC - 10 MHz clock speed • 400 ns instruction cycle (@ 10 MHz)	PIC12C5XX	OTP program memory, digital only
			PIC12C67X	OTP program memory with analog functions
			PIC12CEXXX	OTP program memory with analog functions and EEPROM data memory

Note 1: The maximum clock speed for some devices is less than 20 MHz.

Please check with your local Microchip distributor, sales representative or sales office for the latest product information.

Development Systems

Microchip is committed to providing useful and innovative solutions to your embedded system designs. Our installed base of application development systems has grown to an impressive 120,000 systems worldwide. Significantly, more than half of the total system shipments over the past six years took place within the past 24 months.

Among support products offered are PICMASTER® Real-Time Universal In-circuit Emulator running under the Windows® environment. MPLAB™, a complete Integrated Development Environment (IDE), is provided with PICMASTER. MPLAB allows the user to edit, compile and emulate from a single user interface, making the developer productive very quickly. PICMASTER is designed to provide product development engineers with an optimized design tool for developing target applications. This universal in-circuit emulator provides a complete MCU design toolset for all MCUs in the PIC12CXXX, PIC16C5X, PIC16CXXX and PIC17CXXX families. A CE compliant version of PICMASTER is available for European Union (EU) countries.

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX MCU families. PRO MATE® II, the full-featured, modular device programmer, enables you to quickly and easily program user software into PICmicro MCUs. SIMICE is an entry level non-real-time emulator system for PIC12CXXX and PIC16C5X. PRO MATE II runs under MPLAB IDE and operates as a stand-alone unit or in conjunction with a PC-compatible host system. The PICSTART® Plus development kit, is a low-cost development systems for the PIC12CXXX, PIC16C5X, PIC16CXXX and PIC17CXXX MCUs. PICDEM low-cost demonstration boards are simple boards which demonstrate the basic capabilities of the full range of Microchip's MCUs. Users can program the sample MCUs provided with PICDEM boards, on a PRO MATE II or PICSTART programmer, and easily test firmware. KEELOQ Evaluation and Programming Tools support Microchip's HCS Secure Data Products.

The Serial EEPROM Designer's Kit includes everything necessary to read, write, erase or program special features of any Microchip Serial EEPROM product including *Smart Serials*™ and secure serials. The *Total Endurance*™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

TABLE 2: PICmicro SYNERGISTIC DEVELOPMENT TOOLS

Development Tool	Name	PIC12CXXX	PIC16C5X	PIC16CXXX	PIC17CXXX
Integrated Development Environment (IDE)	MPLAB™	✔	✔	✔	✔
Universal Macro-Assembler	MPASM	✔	✔	✔	✔
C Compiler	MPLAB-C17	—	—	—	✔
Full-Featured, Modular In-Circuit Emulator	PICMASTER®	✔	✔	✔	✔
Low-Cost Modular In-Circuit Emulator	ICEPIC	—	✔	✔	—
Low-Cost Entry Level Hardware Simulator	SIMICE	✔	✔	—	—
Full-Featured, Modular Device Programmer	PRO MATE® II	✔	✔	✔	✔
Entry-Level Development Kit with Programmer	PICSTART® Plus	✔	✔	✔	✔
Fuzzy Logic Development Software	*fuzzy*TECH®-MP	✔	✔	✔	✔

Software Support

MPLAB is a Windows-based development platform for Microchip's PICmicro OTP MCUs. MPLAB IDE offers a project manager and program text editor, a user-configurable toolbar containing four pre-defined sets and a status bar which communicates editing and debugging information.

MPLAB is the common user interface for Microchip development systems tools including MPLAB Editor, MPASM Assembler, MPLAB-SIM Software Simulator, PICMASTER In-Circuit Emulator, PRO MATE II Programmer and PICSTART Plus Development Programmer.

Microchip's PICmicro MCUs are also supported by fuzzy logic development software, an application code generator and a C-Compiler. MP-DriveWay is an easy-to-use Windows-based Application Code Generator for visually configuring all the peripherals in a PICmicro device and, with a click of the mouse, generate all the initialization and many functional code modules in C language.

Microchip endeavors at all times to provide the best service and responsiveness possible to its customers. The Microchip Internet Home Page can provide you with the latest technical information, production released software for development tools, application notes and promotional news on Microchip products and technology. The Microchip World Wide Web address is http://www.microchip.com.

Application-Specific Standard Products (ASSPs)

Secure Data Products Overview

Microchip's patented KEELOQ code hopping technology is the perfect solution for remote keyless entry and logical/physical access control systems. The initial device in the family, HCS300 encoder, will replace current fixed code encoders in transmitter applications and provide a low cost, integrated solution. The KEELOQ family is rapidly expanding with the HCS301 (high voltage encoder), HCS200 (low-end, low-cost encoder), and high-end encoders (HCS360 and HCS361) that meet OEM specifications and requirements.

Microchip provides flexible decoder solutions by providing optimized routines for Microchip's PICmicro MCUs. This allows the designer to combine the decoder and system functionality in a MCU. The decoder routines are available under a license agreement. The HCS500, HCS512 and HCS515 are the first decoder devices in the KEELOQ family. These devices are single chip decoder solutions and simplify designs by handling learning and decoding of transmitters.

The KEELOQ product family is expanding to include enhanced encoders and decoders. Typical applications include automotive RKE, alarm and immobilizer systems, garage door openers and home security systems.

KEELOQ® Rock Solid Security

Serial EEPROM Overview

Microchip offers one of the broadest selections of CMOS Serial EEPROMs on the market for embedded control systems. Serial EEPROMs are available in a variety of densities, operating voltages, bus interface protocols, operating temperature ranges and space saving packages.

Densities:

Currently range from 128 bits to 64K bits with higher density devices in development.

Bus Interface Protocols:

All major protocols are covered: I^2C, Microwire® and SPI.

Operating Voltages:

In addition to standard 5V devices there are two low voltage families. The "LC" devices operate down to 2.5V, while the breakthrough "AA" family operates, in both read and write mode, down to 1.8V, making these devices highly suitable for alkaline and NiCd battery powered applications.

Temperature Ranges:

Like all Microchip devices, Serial EEPROMs are offered in Commercial (0°C to +70°C), Industrial (-40°C to +85°C) and Extended (-40°C to +125°C) operating temperature ranges.

Packages:

Small footprint packages include: industry standard 5-lead SOT-23, 8-lead DIP, 8-lead SOIC in JEDEC and EIAJ body widths, and 14-lead SOIC. The SOIC comes in two body widths; 150 mil and 207 mil.

Technology Leadership:

Microchip's Serial EEPROMs are backed by a 10 million Erase/Write cycle guarantee. Microchip's erase/write cycle endurance is among the best in the world, and only Microchip offers such unique and powerful development tools as the Total Endurance disk. This mathematical software model is an innovative tool used by system designers to optimize Serial EEPROM performance and reliability within the application.

We have also developed the world's first 64K Smart Serial EEPROM. Device densities range from 128 bits up to 64K bits. Another first is the 24LC21, a single chip DDC1/DDC2™-compatible solution for plug-and-play video monitors. In addition, Microchip released a high-speed 1 MHz 2-wire Serial EEPROM device ideal for high-performance embedded systems.

Microchip is a high-volume supplier of Serial EEPROMs to all the major markets worldwide including consumer, automotive, industrial, computer and communications. To date, more than 700 million units have been produced. Microchip continues to develop new Serial EEPROM solutions for embedded control applications.

Parallel EEPROM Overview

CMOS Parallel EEPROM devices from Microchip are available in 4K, 16K and 64K densities. The manufacturing process used for these EEPROMs ensures 10,000 to 100,000 erase/writecycles typical. Data retention is more than 10 years. Fast write times are less than 200 µs. These EEPROMs work reliably under demanding conditions and operate efficiently at temperatures from -40°C to +85°C. Microchip's expertise in advanced SOIC, TSOP and VSOP surface mount packaging supports our customers' needs in space-sensitive applications.

Typical applications include computer peripherals, engine control, telecommunications and pattern recognition.

OTP EPROM Overview

Microchip's CMOS EPROM devices are produced in densities from 64K to 512K. Typical applications include computer peripherals, instrumentation, and automotive devices. Microchip's expertise in surface mount Packaging on SOIC, TSOP and VSOP packages led to the development of the Surface Mount OTP EPROM market where Microchip is a leading supplier today. Microchip is also a leading supplier of low-voltage EPROMs for battery powered applications.

FLEXIBLE PROGRAMMING OPTIONS

As the world's leading supplier of field-programmable MCUs, Microchip has made many innovative programming options available for the embedded systems manufacturer. These programming options give the broadest range of flexibility to meet the unique requirements of your specific design – at all stages of product development, prototyping and production.

The Advantage of Field Programmability

The PICmicro MCU family provides a unique combination of a high-performance RISC processor with cost-effective OTP technology. Cost-effective OTP provides many benefits to the user at prices which can be comparable to competing ROM solutions. The benefits include:

1. Quick time-to-market.
2. Ease of code changes.
3. Ability to provide adaptable solutions to end-customer requirements.
4. Ability to meet upside potential via inventory positions at Microchip or worldwide distribution.
5. Reduced scrappage in manufacturing.
6. Reduced inventory in manufacturing.
7. Reduced work-in-process liability.

For most manufacturers, getting the product to market quickly has become the number one goal as global markets have become more competitive. Time-to-market puts pressure on all functions within the manufacturing process: development, purchasing, production, marketing and sales. Field-programmable OTP technology streamlines the process for all stages in the product life cycle. For example, in the early product development stages, a programmable MCU allows much of the functionality to be implemented in software which can be modified more easily than hardware-only solutions.

In the manufacturing stage, the compression of the product life cycle curve puts pressure on the management of inventory and manufacturing cycle times. Minimizing inventory reduces the ability to meet upside demand. Using a traditional ROM-based MCU limits the ability to respond to the market with product enhancements or semi-customized products for specific customers. Using the standard OTP-based PICmicro MCU solves all these issues. Inventory can be managed effectively by using the same devices for several different systems. Costs can be reduced due to volume purchasing. Upsides can be met from either safety stock, directly from Microchip, or local distributors who regularly inventory all PICmicro MCU devices. A sudden decline in demand means no work-in-process ROM-based inventory and any excess safety stock can be consumed by the other products using the same standard devices.

OTP is the 'Flexible Manufacturing' technology of the MCU world. As competition intensifies, the demand for customer-specific products increases. Having the ability to change (for example, the appearance of LCD displays or add extra features in a timely manner) can be a key competitive advantage. Programming the OTP device on the manufacturing floor allows easy customizing and internal tracking of the devices for each specific customer. Customization can significantly increase the overall product life cycle to provide better return on investment and help minimize the threat of competition.

Ease of Production Utilizing Quick Turn Programming (QTP) and Serialized Quick Turn Programming (SQTP SM)

Recognizing the needs of high-volume manufacturing operations, Microchip has developed two programming methodologies which make the OTP products as easy to use in manufacturing as they are efficient in the system development stage.

Quick Turn Programming allows factory programming of OTP products prior to delivery to the system manufacturing operation. PICmicro MCU, EPROM and Serial EEPROM products can be automatically programmed, with the users program, during the final stages of the test operation at Microchip's assembly and test operations in the Philippine Islands, Taiwan and Thailand. This low-cost programming step allows the elimination of programming during system manufacturing and essentially allows the user to treat the PICmicro and memory products as custom ROM products. With one-to four-week lead times on QTP products, the user no longer needs to plan for the extended ROM masking lead times and masking charges associated with custom ROM products. This capability, combined with the off-the-shelf availability of standard OTP product, ensures the user of product availability and the ability to reduce his time-to-market once product development has been completed.

Unique in the 8-bit MCU market is Microchip's ability to enhance the QTP capability with Serialized Quick Turn Programming (SQTP). SQTP allows for the programming of devices with unique, random or serialized identification codes. As each PICmicro device is programmed with the customers program code, a portion of the program memory space can be programmed with a unique ID, accessible from normal program memory, which will allow the user to provide each device with a unique identification. This capability is ideal for embedded systems applications where the transmission of key codes or identification of the device as a node within a network is essential. Taking advantage of this capability allows the system designer to eliminate the requirement for expensive off-chip code implementation using DIP switches or non-volatile memory components. The SQTP offering, pioneered by Microchip, provides the embedded systems designer with a low cost means of putting a unique and custom device into every system or node.

In-Circuit Serial Programming (ICSP™)

Microchip supports several methods of ICSP on its PICmicro MCUs. ICSP allows you to better respond to changing market conditions by leaving the MCU program memory blank until just prior to system shipment. The devices can then be programmed in-circuit during or after final assembly. Additionally, Microchip's Enhanced FLASH MCUs – with high-endurance program memory – allow in-circuit erase and reprogramming to maximize software update flexibility.

Electrically Reprogrammable

Microchip offers Enhanced FLASH MCUs which allow unlimited erase and reprogramming of the MCU program memory. This feature can be very useful for more complex systems with longer product lives.

Masked ROM

Microchip offers Masked ROM versions of many of its most popular MCUs, giving customers the lowest cost option for high volume products with stable firmware.

Future Products and Technology

Microchip is constantly developing advanced process technology modules and new products that utilize our advanced manufacturing capabilities. Current production technology utilizes lithography dimensions down to 0.7 micron.

Microchip's research and development activities include exploring new process technologies and products that have industry leadership potential. Particular emphasis is placed on products that can be put to work in high-performance broad-based markets.

Equipment is continually updated to bring the most sophisticated process, CAD and testing tools online. Cycle times for new technology development are continuously reduced by using in-house mask generation, a high-speed pilot line within the manufacturing facility and continuously improving methodologies.

Objective specifications for new products are developed by listening to our customers and by close co-operation with our many customer-partners worldwide.

PICmicro™ 8-BIT MICROCONTROLLER FAMILY

Product	Program Memory OTP Bytes	Program Memory OTP Words	E²PROM Data Memory	Data RAM Bytes	Max. Speed MHz	I/O Ports	ADC 8-Bits	Serial I/O	PWM	Brown-Out Detection	Comparators	Timers	ICSP™	Other Features	ROM Equivalent	Packages
PIC12CXXX — 400ns Instruction Execution. 33/35 Instructions																
PIC12C508	768	512x12	—	25	4	6	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12C508A*	768	512x12	—	25	4	6	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12C509	1536	1024x12	—	41	4	6	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12C509A*	1536	1024x12	—	41	4	6	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12CE518*	768	512x12	16	25	4	6	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12CE519*	1536	1024x12	16	41	4	6	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12C671*	1792	1024x14	—	128	10	6	4	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12C672*	3584	2048x14	—	128	10	6	4	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8SM, 8JW
PIC12CE673*	1792	1024x14	16	128	10	6	4	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8JW
PIC12CE674*	3584	2048x14	16	128	10	6	4	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator	—	8P, 8JW
PIC16C5X — 200ns Instruction Execution, 33 Instructions																
PIC16C52	576	384x12	—	25	4	12	—	—	—	—	—	1	—	10mA source/sink per I/O, 2.5V	—	18P, 18SO
PIC16C54	768	512x12	—	25	20	12	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O, 2.5V	PIC16CR54A	18P, 18JW, 18SO, 20SS
PIC16C54A	768	512x12	—	25	20	12	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O, 2.0V	—	18P, 18JW, 18SO, 20SS
PIC16C54B	768	512x12	—	25	20	12	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O	PIC16CR54B	18P, 18JW, 18SO, 20SS
PIC16C55	768	512x12	—	24	20	20	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O, 2.5V	—	28P, 28JW, 28SP, 28SO, 28SS
PIC16C56	1536	1024x12	—	25	20	12	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O, 2.5V	—	18P, 18JW, 18SO, 20SS
PIC16C56A	1536	1024x12	—	25	20	12	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O	PIC16CR56A	18P, 18JW, 18SO, 20SS
PIC16C57	3072	2048x12	—	72	20	20	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O, 2.5V	—	28P, 28JW, 28SP, 28SO, 28SS
—	3072 (ROM)	2048x12	—	72	20	20	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O, 2.5V	PIC16CR57B	28P, 28JW, 28SP, 28SO, 28SS
PIC16C58A	3072	2048x12	—	73	20	12	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O, 2.0V	PIC16CR58A	18P, 18JW, 18SO, 20SS
PIC16C58B	3072	2048x12	—	73	20	12	—	—	—	—	—	1+WDT	—	20mA source and 25mA sink per I/O	PIC16CR58B	18P, 18JW, 18SO, 20SS
PIC16CXXX — 4–12 Interrupts, 200ns Instruction Execution, 35 Instructions. Upwardly Compatible with PIC16C5X																
PIC14C000	7168	4096x14	—	192	20	20	8 SLAC	I²C™/ SMB	—	—	2	2+WDT	Yes	25mA source/sink, temperature sensor, bandgap voltage reference, internal oscillator, 2 Digital-to-Analog Converters	—	28SP, 28SO, 28SS, 28JW
PIC16C554	896	512x14	—	80	20	13	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C554A*	896	512x14	—	96	20	13	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O	—	18P, 18SO, 20SS, 18JW
PIC16C556A*	1792	1024x14	—	96	20	13	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O	—	18P, 18SO, 20SS, 18JW
PIC16C558	3584	2048x14	—	128	20	13	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C558A*	3584	2048x14	—	128	20	13	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O	—	18P, 18SO, 20SS, 18JW
PIC16C61	1792	1024x14	—	36	20	13	—	—	—	—	—	1+WDT	Yes	20mA source and 25mA sink per I/O	—	18P, 18SO, 18JW
PIC16C62A	3584	2048x14	—	128	20	22	—	I²C/SPI™	1	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	PIC16CR62	28SP, 28SO, 28SS, 28JW
PIC16C63	7168	4096x14	—	192	20	22	—	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	PIC16CR63	28SP, 28SO, 28JW
PIC16C64A	3584	2048x14	—	128	20	33	—	I²C/SPI	1	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, Capture/Compare/PWM	PIC16CR64	40P, 40JW, 44L, 44PQ, 44PT
PIC16C65A	7168	4096x14	—	192	20	33	—	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	PIC16CR65	40P, 40JW, 44L, 44PQ, 44PT
PIC16C66	14336	8192x14	—	368	20	22	—	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28SP, 28SO, 28JW
PIC16C67	14336	8192x14	—	368	20	33	—	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, Parallel Slave Port	—	40P, 40JW, 44L, 44PQ, 44PT
PIC16C620	896	512x14	—	80	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C620A*	896	512x14	—	96	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	18P, 18SO, 20SS, 18JW
PIC16C621	1792	1024x14	—	80	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C621A*	1792	1024x14	—	96	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	18P, 18SO, 20SS, 18JW

*Contact Microchip Technology for availability date.

PICmicro 8-BIT MICROCONTROLLER FAMILY

Product	Program Memory OTP Bytes	Program Memory OTP Words	E²PROM Data Memory	Data RAM Bytes	Max. Speed MHz	I/O Ports	ADC 8-Bits	Serial I/O	PWM	Brown-Out Detection	Comparators	Timers	ICSP	Other Features	ROM Equivalent	Packages
PIC16CXXX — 4-12 Interrupts, 200ns Instruction Execution, 35 Instructions, Upwardly Compatible with PIC16C5X (Continued)																
PIC16C622	3584	2048x14	—	128	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, 2.5V	—	18P, 18SO, 20SS, 18JW
PIC16C622A*	3584	2048x14	—	128	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	18P, 18SO, 20SS, 18JW
PIC16CE623*	896	512x14	128	96	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	18P, 18SO, 20SS, 18JW
PIC16CE624*	1792	1024x14	128	96	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	18P, 18SO, 20SS, 18JW
PIC16CE625*	3584	2048x14	128	128	20	13	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	18P, 18SO, 20SS, 18JW
PIC16C641*	3584	2048x14	—	128	20	22	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	28SP, 28SO, 28JW
PIC16C642	7168	4096x14	—	176	20	22	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}	—	28SP, 28SO, 28JW
PIC16C661*	3584	2048x14	—	128	20	33	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, Parallel Slave Port	—	40P, 40JW, 44L, 44PQ, 44PT
PIC16C662	7168	4096x14	—	176	20	33	—	—	—	Yes	2	1+WDT	Yes	25mA source/sink per I/O, programmable V_{REF}, Parallel Slave Port	—	40P, 40JW, 44L, 44PQ, 44PT
PIC16C710	896	512x14	—	36	20	13	4	—	—	Yes	—	1+WDT	Yes	25mA source/sink per I/O	—	18P, 18SO, 20SS, 18JW
PIC16C71	1792	1024x14	—	36	20	13	4	—	—	—	—	1+WDT	Yes	20mA source/sink per I/O	—	18P, 18SO, 18JW
PIC16C711	1792	1024x14	—	68	20	13	4	—	—	Yes	—	1+WDT	Yes	25mA source/sink per I/O	—	18P, 18SO, 20SS, 18JW
PIC16C715	3584	2048x14	—	128	20	13	4	—	—	Yes	—	1+WDT	Yes	25mA source/sink per I/O	—	18P, 18SO, 20SS, 18JW
PIC16C72	3584	2048x14	—	128	20	22	5	I²C/SPI	1	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28SP, 28SO, 28JW, 28SS
PIC16C73A	7168	4096x14	—	192	20	22	5	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, 2 Capture/Compare/PWM	—	28SP, 28SO, 28JW
PIC16C74A	7168	4096x14	—	192	20	33	8	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	—	40P, 40JW, 44L, 44PQ, 44PT
PIC16C76	14336	8192x14	—	368	20	22	5	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28SP, 28SO, 28JW
PIC16C77	14336	8192x14	—	368	20	33	8	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, Parallel Slave Port	—	40P, 40JW, 44L, 44PQ, 44PT
PIC16F83	896 (Flash)	512x14 (Flash)	64	36	10	13	—	—	—	—	—	1+WDT	Yes	20mA source and 25mA sink per I/O, 64 bytes data EEPROM, 2.0V Operation	PIC16CR83	18P, 18SO
PIC16F84	1792 (Flash)	1024x14 (Flash)	64	68	10	13	—	—	—	—	—	1+WDT	Yes	20mA source and 25mA sink per I/O, 64 bytes data EEPROM, 2.0V Operation	PIC16CR84	18P, 18SO
PIC16C923	7168	4096x14	—	176	8	52	—	I²C/SPI	1	—	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, LCD module, static, 1/2, 1/3, 1/4 multiplex	—	64SP, 68L, 64PT
PIC16C924	7168	4096x14	—	176	8	52	5	I²C/SPI	1	—	—	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, LCD module, static, 1/2, 1/3, 1/4 multiplex	—	64SP, 68CL, 68L, 64PT
PIC17CXXX — 120ns Instruction Execution Including Multiply, 58 Instructions, Upwardly Compatible with PIC16CXX/PIC16C5X																
PIC17C42A	4096	2048x16	—	232	33	33	—	USART	2	—	—	4+WDT	—	20mA source and 35mA sink per I/O, 2 I/O with 60mA sink, 2 Capture, externally expandable, 1 cycle 8x8 multiply	PIC17CR42	40P, 40JW, 44L, 44PQ, 44PT
PIC17C43	8192	4096x16	—	454	33	33	—	USART	2	—	—	4+WDT	—	20mA source and 35mA sink per I/O, 2 I/O with 60mA sink, 2 Capture, externally expandable, 1 cycle 8x8 multiply	PIC17CR43	40P, 40JW, 44L, 44PQ, 44PT
PIC17C44	16384	8192x16	—	454	33	33	—	USART	2	—	—	4+WDT	—	20mA source and 35mA sink per I/O, 2 I/O with 60mA sink, 2 Capture, externally expandable, 1 cycle 8x8 multiply	—	40P, 40JW, 44L, 44PQ, 44PT
PIC17C752*	16384	8192x16	—	678	33	50	12 (10 Bits)	USART (2), I²C/SPI	3	Yes	—	4+WDT	—	20mA source and 35mA sink per I/O, 2 I/O with 60mA sink, 4 Capture, externally expandable, 1 cycle 8x8 multiply	—	64SP, 68CL, 68L, 64PT
PIC17C756	32768	16384x16	—	902	33	50	12 (10 Bits)	USART (2), I²C/SPI	3	Yes	—	4+WDT	—	20mA source and 35mA sink per I/O, 2 I/O with 60mA sink, 4 Capture, externally expandable, 1 cycle 8x8 multiply	—	64SP, 68CL, 68L, 64PT
PIC17C762*	16384	8192x16	—	678	33	66	16 (10 Bits)	USART (2)/ I²C/SPI	3	Yes	—	4+WDT	Yes	20mA source and 35mA sink per I/O, 2 I/O with 60mA sink, 4 Capture, externally expandable, 1 cycle 8x8 multiply	—	84CL, 84L, 80PT
PIC17C766*	32768	16384x16	—	902	33	66	16 (10 Bits)	USART (2)/ I²C/SPI	3	Yes	—	4+WDT	Yes	20mA source and 35mA sink per I/O, 2 I/O with 60mA sink, 4 Capture, externally expandable, 1 cycle 8x8 multiply	—	84CL, 84L, 80PT

*Contact Microchip Technology for availability date.

Abbreviation:

ADC = Analog-to-Digital Converter
CAP = Capture
CCP = Capture/Compare/PWM
DAC = Digital-to-Analog Converter
E² = EEPROM (Reprogrammable)
I²C = Inter-Integrated Circuit Bus
PWM = Pulse Width Modulator
SPI = Serial Peripheral Interface
USART = Universal Synchronous/Asynchronous Receiver/Transmitter
WDT = Watchdog Timer
SLAC = Slope A/D Converter, up to 16 bits
SMB = System Management Bus

SECURE DATA PRODUCTS

Product	Transmission Code Length Bits	Code Hopping Bits	Programmable Encryption Key Bits	Seed Length	Operating Voltage	Function	Other Features	Packages
KEELOQ® Encoder Devices								
HCS200	66	32	64	32	3.5V to 13.0V	7	Entry Level, Fixed Code Support, Battery Low Indicator	8P, 8SO
HCS300	66	32	64	32	2.0V to 6.3V	15	LED Drive, Overflow bits, Time-out, Battery Low Indicator	8P, 8SO
HCS301	66	32	64	32	3.5V to 13.0V	15	Same as HCS300	8P, 8SO
HCS360	67	32	64	48	2.0V to 6.6V	15	IR Mode, PWM and Manchester Coding, 2 independent counters, 2-Bit CRC	8P, 8SO
HCS361	67	32	64	48	2.0V to 6.6V	15	IR Mode, PWM and VPWM Coding, 2 independent counters, 2-Bit CRC	8P, 8SO
HCS410	69	32	64	60	2.0V to 6.6V	7	Self-powered transponder, superset of HCS360	8P, 8SO, 8ST

Product	Reception Length Bits	Encoders Supported	Transmitters Supported	Operating Voltage	Functions	Other Features	Packages
KEELOQ Decoder Devices							
HCS500	67	HCS200, HCS300, HCS301, HCS360, HCS361, HCS410	Up to 7	4.5V to 5.5V	15 Serial Functions	Full-featured decoder with serial interface to microcontrollers	8P, 8SO
HCS512	67	HCS200, HCS300, HCS301, HCS360, HCS361, HCS410	Up to 4	3.0V to 6.0V	15 (S0, S1, S2, S3); VLow, Serial	Single-chip decoder with secure learning	18P, 18SO
HCS515*	67	HCS200, HCS300, HCS301, HCS360, HCS361, HCS410	Up to 7	4.5V to 5.5V	15 Serial 3 (S1, S0) Parallel	Full-featured decoder with serial and parallel interface. On-chip 1K transmitter and 1K user EEPROM.	14P, 14SO

Product	Token Units	Cryptographic Key Length	Signature Challenge	Signature Response	User Programmable Area	Operating Voltage	Other Features	Packages
KEELOQ Smart Card Devices								
SCS152	33352	64-bit	32 bits	8 bits	40 bits	4.75V to 5.25V	ISO 7816-3:1989 compliant prepay/disposable card	Die

*Contact Microchip Technology for availability date.

SERIAL ELECTRICALLY ERASABLE PROMs (EEPROM)

Product	E/W Cycles	Density (Organization)	Write Speed	Max. Clock Freq.	Operating Voltage	Unique Features	Packages
3-WIRE SERIAL EEPROM FAMILY							
93C46B	1M	1K bits (x16)	2 ms	2 MHz	4.5V to 5.5V	All devices listed in this group are recommended for extended temperature applications only. All other applications should use 93LCx6A/B devices.	P, SN, SM, ST
93C56A	1M	2K bits (x8)	2 ms	2 MHz	4.5V to 5.5V		P, SN
93C56B	1M	2K bits (x16)	2 ms	2 MHz	4.5V to 5.5V		P, SN
93C66A	1M	4K bits (x8)	2 ms	2 MHz	4.5V to 5.5V		P, SN
93C66B	1M	4K bits (x16)	2 ms	2 MHz	4.5V to 5.5V		P, SN
93C76	10M	8K bits (x8 or x16)	5 ms	2 MHz	4.5V to 5.5V		P, SN
93C86	10M	16K bits (x8 or x16)	5 ms	2 MHz	4.5V to 5.5V		P, SN
93LC56	10M	2K bits (x8 or x16)	10 ms	2 MHz	2.0V to 6.0V	Not recommended for new designs.	P, SN, SM, SL
93LC66	10M	4K bits (x8 or x16)	10 ms	2 MHz	2.0V to 6.0V	Not recommended for new designs.	P, SN, SM, SL
93LC76	10M	8K bits (x8 or x16)	5 ms	2 MHz	2.0V to 6.0V		P, SN
93LC86	10M	16K bits (x8 or x16)	5 ms	2 MHz	2.0V to 6.0V		P, SN
93LC46A	1M	1K bits (x8)	5 ms	2 MHz	2.5V to 6.0V		P, SN, SM, ST
93LC56A	1M	2K bits (x8)	6 ms	2 MHz	2.5V to 6.0V		P, SN, SM, ST
93LC66A	1M	4K bits (x8)	6 ms	2 MHz	2.5V to 6.0V		P, SN, SM, ST
93LC46B	1M	1K bits (x16)	5 ms	2 MHz	2.5V to 6.0V		P, SN, SM, ST
93LC56B	1M	2K bits (x16)	6 ms	2 MHz	2.5V to 6.0V		P, SN, SM, ST
93LC66B	1M	4K bits (x16)	6 ms	2 MHz	2.5V to 6.0V		P, SN, SM, ST
93AA46	1M	1K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN, SM
93AA56	10M	2K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN, SM
93AA66	10M	4K bits (x8 or x16)	10 ms	2 MHz	1.8V to 5.5V		P, SN, SM
93AA76	10M	8K bits (x8 or x16)	5 ms	2 MHz	1.8V to 5.5V		P, SN
93AA86	10M	16K bits (x8 or x16)	5 ms	2 MHz	1.8V to 5.5V		P, SN
93LCS56	1M	2K (x16)	10 ms	2 MHz	2.5V to 6.0V	The "S" indicates software write protection of user defined memory space.	P, SN, SM, SL
93LCS66	1M	4K (x16)	10 ms	2 MHz	2.5V to 6.0V		P, SN, SM, SL

Special Features: Automatic ERAL before WRAL, self-timed erase and write cycle, power on/off data protection circuitry, sequential read function and industry standard 3-wire serial I/O

SERIAL ELECTRICALLY ERASABLE PROMs (EEPROM)

Product	E/W Cycles	Density (Organization)	Write Speed	Max. Clock Freq.	Operating Voltage	Unique Features	Packages
2-WIRE I²C SERIAL EEPROM FAMILY**							
24C00	1M	128 bits (x8)	4 ms	400 kHz	4.5V to 5.5V	5-pin SOT-23 package.	P, SN, ST, OT
24LC00	1M	128 bits (x8)	4 ms	400 kHz	2.5V to 6.0V		P, SN, ST, OT
24AA00	1M	128 bits (x8)	4 ms	400 kHz	1.8V to 6.0V		P, SN, ST, OT
24C01C	1M	1K bits (x8)	1 ms	400 kHz	4.5V to 5.5V	The 24C01C, 24C02C and 24C04A are for applications which require fast byte write and/or extended temperature. I²C compatible. 3 address pins.	P, SN, ST
24C02C	1M	2K bits (x8)	1 ms	400 kHz	4.5V to 5.5V		P, SN, ST
24C04A	1M	4K bits (x8)	1 ms	100 kHz	4.5V to 5.5V		P, SN, SM, SL
24C08B	1M	8K bits (x8)	10 ms	100 kHz	4.5V to 5.5V	The 24C08B and 24C16B versions are for 5.0V only applications which require extended temperature (–40°C to +125°C). I²C compatible.	P, SN, SM, SL
24C16B	1M	16K bits (x8)	10 ms	100 kHz	4.5V to 5.5V		P, SN, SL
24LC01B	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Hardware write protect. Schmitt trigger inputs. 400kHz operation is @ 5.0V ± 10% and commercial grade.	P, SN, SM
24LC02B	1M	2K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM
24LC04B	1M	4K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM, SL
24LC08B	1M	8K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM, SL
24LC16B	1M	16K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN, SM, SL
24AA01	1M	1K bits (x8)	10 ms	400 kHz	1.8V to 5.5V	Hardware write protect. Schmitt trigger inputs. 400kHz operation is @ 5.0V ± 10% and commercial temperature range (–40°C to 85°C).	P, SN, SM
24AA02	1M	2K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM
24AA04	1M	4K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM, SL
24AA08	1M	8K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM, SL
24AA16	1M	16K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN, SM, SL
24C32A	1M	32K bits (x8)	5 ms	400 kHz	4.5V to 5.5V	JEDEC SOIC "SN" (150 mil wide) package and cascadable.	SN, P, SM
24LC32A	1M	32K bits (x8)	5 ms	400 kHz	2.5V to 6.0V		SN, P, SM
24AA32A	1M	32K bits (x8)	5 ms	100 kHz	1.8V to 6.0V		SN, P, SM
24C32	10M/1M	32K bits (x8)	5 ms	400 kHz	4.5V to 5.5V	Incorporates a 4K high endurance block (not relocatable) to ensure 10,000,000 Erase/Write cycles, a 1 page by 8 line input cache (64 bytes) for fast write loads and is cascadable up to 8 parts. 1 MHz Maximum Clock Rate.	P, SM
24LC32	10M/1M	32K bits (x8)	5 ms	400 kHz	2.5V to 6.0V		P, SM
24AA32	10M/1M	32K bits (x8)	5 ms	100 kHz	1.8V to 6.0V		P, SM
24FC32	10M/1M	32K bits (x8)	5 ms	1 MHz	4.5V to 5.5V		P, SM
24LC64	1M	64K bits (x8)	5 ms	400 kHz	2.5V to 5.5V	32 byte page.	P, SN, SM, ST
24AA64	1M	64K bits (x8)	10 ms	100 kHz	1.8V to 5.5V		P, SN, SM, ST
24C65	10M/1M	64K bits (x8)	5 ms	400 kHz	4.5 to 5.5V	Relocatable 4K bit block of ultra high endurance memory to ensure 10,000,000 E/W cycles, 1 page by 8 line input cache (64 bytes) for fast write loads, cascadable up to 512K bits, Erase/Write protection in 4K blocks. 1 MHz Maximum Clock Rate.	P, SM
24LC65	10M/1M	64K bits (x8)	5 ms	400 kHz	2.5 to 6.0V		P, SM
24AA65	10M/1M	64K bits (x8)	5 ms	100 kHz	1.8 to 6.0V		P, SM
24FC65	10M/1M	64K bits (x8)	5 ms	1 MHz	4.5V to 5.5V		P, SM
24LC128	1M	128K bits (x8)	5 ms	400 kHz	2.5V to 5.5V	64 byte page.	P, SN, SM
24AA128	1M	128K bits (x8)	10 ms	100 kHz	1.8V to 5.5V		P, SN, SM
24LC256	100K	256K bits (x8)	5 ms	400 kHz	2.5V to 5.5V	64 byte page.	P, SM
24AA256	100K	256K bits (x8)	10 ms	100 kHz	1.8V to 5.5V		P, SM
24LC164	10M	16K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Cascadable 16K-bit Serial EEPROM.	P, SN
24AA164	10M	16K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN
24LC174	10M	16K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Cascadable 16K-bit Serial EEPROM. Specially addressed one-time-programmable (OTP) 16 byte security block.	P, SN
24AA174	10M	16K bits (x8)	10 ms	400 kHz	1.8V to 5.5V		P, SN
24C01SC	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Smart card specific memory devices. All devices meet ISO7816 pinout requirements.	S, W, WF
24C02SC	1M	2K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		S, W, WF
24LC32SC	1M	32K bits (x8)	5 ms	400 kHz	2.5V to 5.5V		S, W, WF
24LC64SC	1M	64K bits (x8)	5 ms	400 kHz	2.5V to 5.5V		S, W, WF
24LC128SC	1M	128K bits (x8)	5 ms	400 kHz	2.5V to 5.5V		S, W, WF
24LC256SC	100K	256K bits (x8)	5 ms	400 kHz	2.5V to 5.5V		S, W, WF
The B version on the 2-wire (I²C) devices designates: no functional address (A0, A1, A2) pins, 400 kHz operation, Schmitt trigger inputs for greater noise protection, longer byte write cycle time and larger input buffer. **Special Features: Self-timed write cycle and page write mode.							
IDENTIFICATION PRODUCTS (Application-Specific Products for Monitors and Memory Modules)							
24LC21	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Completely implements DDC1™/DDC2™ interface for monitor identification. Improved noise filter. Software enabled Hardware Write Protection pin.	P, SN
24LCS21	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V		P, SN
24LC21A	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Same as 24LC21 with return to DDC1 feature.	P, SN
24LCS21A	1M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Same as 24LCS21 with return to DDC1 feature.	P, SN
24LC41A	1M	1K and 4K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Dual Mode, Dual-Port device. Completely implements DDC1/DDC2 interface for monitor identification (DDC port). Also includes 4K bit MCU port.	P
24LC024	10M	2K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Addressable.	P, SN, ST
24LCS52	10M	2K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Addressable. Software write protect.	P, SN, ST
24LC61	10M	1K bits (x8)	10 ms	400 kHz	2.5V to 5.5V	Software addressable devices for both identification, software WP	P, SN, ST
24LCS62	10M	2K bits (x8)	10 ms	400 kHz	2.5V to 5.5 V	Software addressable devices for both identification, software WP	P, SN, ST

SERIAL ELECTRICALLY ERASABLE PROMs (EEPROM)

Product	E/W Cycles	Density (Organization)	Write Speed	Max. Clock Freq.	Operating Voltage	Unique Features	Packages
SPI™ SERIAL EEPROM FAMILY							
25C040	1M	4K bits (x8)	5 ms	3 MHz	4.5V to 5.5V	Supports SPI Modes 0, 3.	P, SN, ST
25C080	1M	8K bits (x8)	5 ms	3 MHz	4.5V to 5.5V		P, SN
25C160	1M	16K bits (x8)	5 ms	3 MHz	4.5V to 5.5V		P, SN
25C320	1M	32K bits (x8)	5 ms	3 MHz	4.5V to 5.5V		P, SN, ST
25C640*	1M	64K bits (x8)	5 ms	3 MHz	4.5V to 5.5V		P, SN, ST
25LC040	1M	4K bits (x8)	5 ms	2 MHz	2.5V to 5.5V	Supports SPI Modes 0, 3.	P, SN, ST
25LC080	1M	8K bits (x8)	5 ms	2 MHz	2.5V to 5.5V		P, SN
25LC160	1M	16K bits (x8)	5 ms	2 MHz	2.5V to 5.5V		P, SN
25LC320	1M	32K bits (x8)	5 ms	2 MHz	2.5V to 5.5V		P, SN, ST
25LC640*	1M	64K bits (x8)	5 ms	2 MHz	2.5V to 5.5V		P, SN, ST
25AA040	1M	4K bits (x8)	5 ms	1 MHz	1.8V to 5.5V	Supports SPI Modes 0, 3.	P, SN, ST
25AA080	1M	8K bits (x8)	5 ms	1 MHz	1.8V to 5.5V		P, SN
25AA160	1M	16K bits (x8)	5 ms	1 MHz	1.8V to 5.5V		P, SN
25AA640*	1M	64K bits (x8)	5 ms	1 MHz	1.8V to 5.5V		P, SN, ST

Special Features: Page write mode, HOLD pin, software enabled block write protection and hardware write protect pin.
* Contact Microchip Technology Inc. for availability date.

PARALLEL ELECTRICALLY ERASABLE PROMs (EEPROM)

Product	Density (Organization)	Byte Write Time	Number of Pins	Packages	Unique Features
STANDARD SERIES					
28C04A	4K bits (x8)	1 ms	24 32	P L	
28C16A	16K bits (x8)	1 ms	24 28 32	P TS, VS L	
28C17A	16K bits (x8)	1 ms	24 28 32	P, SO TS, VS L	Ready/Busy Pin
28C64A	64K bits (x8)	1 ms	28 32	P, SO, TS, VS L	
28LV64A	64K bits (x8)	1 ms	28 32	P, SO, TS, VS L	Low voltage capability down to 3.0V
FAST BYTE WRITE SERIES					
28C04AF	4K bits (x8)	200 µs	24 32	P L	
28C16AF	16K bits (x8)	200 µs	24 28 32	P TS, VS L	
28C17AF	16K bits (x8)	200 µs	24 28 32	P, SO TS, VS L	Ready/Busy Pin
28C64AF	64K bits (x8)	200 µs	28 32	P, SO, TS, VS L	

Special Features: Access times of 150, 200, 250 ns (Except 28LV64A; Access Time = 300ns) and Commercial and Industrial Temperature Ranges.

ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY (EPROM)

Product	Size	Organization	Access Time (ns)	Operating Voltage	Packages	Temp. Range
STANDARD EPROM FAMILY						
27C64-25	64K bits	8Kx8	250	4.5V to 5.5V	P, SO, L	C, I
27C64-20	64K bits	8Kx8	200	4.5V to 5.5V	P, SO, L	C, I
27C64-17	64K bits	8Kx8	170	4.5V to 5.5V	P, SO, L	C, I
27C64-15	64K bits	8Kx8	150	4.5V to 5.5V	P, SO, L	C, I
27C64-12	64K bits	8Kx8	120	4.5V to 5.5V	P, SO, L	C, I
27C128-25	128K bits	16Kx8	250	4.5V to 5.5V	P, SO, L	C, I
27C128-20	128K bits	16Kx8	200	4.5V to 5.5V	P, SO, L	C, I
27C128-17	128K bits	16Kx8	170	4.5V to 5.5V	P, SO, L	C, I
27C128-15	128K bits	16Kx8	150	4.5V to 5.5V	P, SO, L	C, I
27C128-12	128K bits	16Kx8	120	4.5V to 5.5V	P, SO, L	C, I
27C256-20	256K bits	32Kx8	200	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C256-15	256K bits	32Kx8	150	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C256-12	256K bits	32Kx8	120	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C256-10	256K bits	32Kx8	100	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C256-90	256K bits	32Kx8	90	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C512A-20	512K bits	64Kx8	200	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C512A-15	512K bits	64Kx8	150	4.5V to 5.5V	P, SO, L, TS, VS	C, I, E
27C512A-12	512K bits	64Kx8	120	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C512A-10	512K bits	64Kx8	100	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27C512A-90	512K bits	64Kx8	90	4.5V to 5.5V	P, SO, L, TS, VS	C, I
27LV64-30	64K bits	8Kx8	300	3.0V to 5.5V	P, SO, L, TS	C
27LV64-25	64K bits	8Kx8	250	3.0V to 5.5V	P, SO, L, TS	C
27LV64-20	64K bits	8Kx8	200	3.0V to 5.5V	P, SO, L, TS	C
27LV256-30	256K bits	32Kx8	300	3.0V to 5.5V	P, SO, L, TS, VS	C, I
27LV256-25	256K bits	32Kx8	250	3.0V to 5.5V	P, SO, L, TS, VS	C, I
27LV256-20	256K bits	32Kx8	200	3.0V to 5.5V	P, SO, L, TS, VS	C, I
SERIAL EPROM FAMILY						
37LV36	35K bits	1134x32	10 MHz clock	3.0V to 6.0V	P, SO, L	C, I
37LV65	64K bits	2048x32	10 MHz clock	3.0V to 6.0V	P, SO, L	C, I
37LV128	128K bits	4096x32	10 MHz clock	3.0V to 6.0V	P, SO, L	C, I

DEVELOPMENT SYSTEMS

EMULATORS

Model Name/Part Number	PICMASTER® with PRO MATE®	PICMASTER without PRO MATE	PICMASTER-CE with PRO MATE	PICMASTER-CE without PRO MATE	PICMASTER Probe Kit	PICMASTER-CE Probe Kit	ICEPIC System	ICEPIC Daughter Board
Production Software Version	3.20	3.20	3.20	3.20	3.20	3.20	1.63	1.63
Intermediate Software Version	3.20.01	3.20.01	3.20.01	3.20.01	3.20.01	3.20.01	N/A	N/A
PIC12C508 (*)	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC12C509 (*)	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC14C000	EM147001	EM147002	EM147101	EM147102	AC145001	AC145002	N/A	N/A
PIC16C52	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC16C54	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC16C54A	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC16C55	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC16C554	EM167033	EM167034	EM167113	EM167114	AC165030	AC165020	EM167208	AC165208
PIC16C558	EM167033	EM167034	EM167113	EM167114	AC165030	AC165020	EM167208	AC165208
PIC16C56	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC16C57	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC16C58A	EM167015	EM167016	EM167101	EM167102	AC165004	AC165015	EM167201	AC165201
PIC16C61	EM167021	EM167022	N/A	N/A	AC165007	AC165017	EM167211	AC165211
PIC16C620	EM167023	EM167024	EM167109	EM167110	AC165008	AC165018	EM167202	AC165202
PIC16C621	EM167023	EM167024	EM167109	EM167110	AC165008	AC165018	EM167202	AC165202
PIC16C622	EM167023	EM167024	EM167109	EM167110	AC165008	AC165018	EM167202	AC165202
PIC16C62A	EM167025	EM167026	EM167103	EM167104	AC165009	AC165016	EM167207	AC165207
PIC16C63	EM167025	EM167026	EM167103	EM167104	AC165009	AC165016	EM167207	AC165207
PIC16C642	EM167035	EM167036	EM167115	EM167116	AC165031	AC165021	EM167213	AC165213
PIC16C64A	EM167025	EM167026	EM167103	EM167104	AC165009	AC165016	EM167207	AC165207
PIC16C65A	EM167025	EM167026	EM167103	EM167104	AC165009	AC165016	EM167207	AC165207
PIC16C66	EM167041	EM167042	EM167121	EM167122	AC165034	AC165024	EM167214	AC165214
PIC16C662	EM167035	EM167036	EM167115	EM167116	AC165031	AC165021	EM167213	AC165213
PIC16C67	EM167041	EM167042	EM167121	EM167122	AC165034	AC165024	EM167214	AC165214
PIC16C71	EM167027	EM167028	EM167105	EM167106	AC165010	AC165013	EM167211	AC165211
PIC16C710	EM167027	EM167028	EM167105	EM167106	AC165010	AC165013	EM167211	AC165211
PIC16C711	EM167027	EM167028	EM167105	EM167106	AC165010	AC165013	EM167211	AC165211
PIC16C715	EM167037	EM167038	EM167117	EM167118	AC165032	AC165022	EM167215	AC165215
PIC16C72	EM167025	EM167026	EM167103	EM167104	AC165009	AC165016	EM167207	AC165207
PIC16C73A	EM167025	EM167026	EM167103	EM167104	AC165009	AC165016	EM167207	AC165207
PIC16C74A	EM167025	EM167026	EM167103	EM167104	AC165009	AC165016	EM167207	AC165207
PIC16C76	EM167041	EM167042	EM167121	EM167122	AC165034	AC165024	EM167214	AC165214
PIC16C77	EM167041	EM167042	EM167121	EM167122	AC165034	AC165024	EM167214	AC165214
PIC16C923	EM167031	EM167032	EM167111	EM167112	AC165012	AC165019	EM167210	AC165210
PIC16C924	EM167031	EM167032	EM167111	EM167112	AC165012	AC165019	EM167210	AC165210

* PICMASTER PIC12CXXX emulation support also requires the use of a probe kit daughter board AC122001.
* ICEPIC PIC12CXXX emulation support also requires the use of a kit daughter board adapter AC122002.
** Contact Microchip Technology for availability date.

DEVELOPMENT SYSTEMS (CONTINUED)

EMULATORS (Continued)

Model Name/Part Number	PICMASTER® with PRO MATE®	PICMASTER without PRO MATE	PICMASTER-CE with PRO MATE	PICMASTER-CE without PRO MATE	PICMASTER Probe Kit	PICMASTER-CE Probe Kit	ICEPIC System	ICEPIC Daughter Board
PIC16F83	EM167029	EM167030	EM167107	EM167108	AC165011	AC165014	EM167212	AC165212
PIC16F84	EM167029	EM167030	EM167107	EM167108	AC165011	AC165014	EM167212	AC165212
PIC17C42A	EM177007	EM177008	EM177107	EM177108	AC175002	AC175003	N/A	N/A
PIC17C43	EM177007	EM177008	EM177107	EM177108	AC175002	AC175003	N/A	N/A
PIC17C44	EM177007	EM177008	EM177107	EM177108	AC175002	AC175003	N/A	N/A
PIC17C756	EM177009**	EM177010**	EM177109**	EM177110**	AC175004**	AC175005**	N/A	N/A

* PICMASTER PIC12CXXX emulation support also requires the use of a probe kit daughter board AC122001.
* ICEPIC PIC12CXXX emulation support also requires the use of a kit daughter board adapter AC122002.
** Contact Microchip Technology for availability date.

	PIC12CXXX	PIC14C000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17CXXX	24CXX/25CXX/ 93CXX	HCSXXX
SOFTWARE TOOLS												
MPLAB™ Integrated Development Environment	SW007002	SW007002	SW007002	SW007002	SW007002	SW007002	SW007002	SW007002	SW007002	SW007002	—	—
PIC C (C Compiler)	***	***	***	***	***	***	***	***	***	—	—	—
MPLAB-C17 Compiler	—	—	—	—	—	—	—	—	—	SW006010	—	—
*fuzzy*TECH®-MP Explorer Fuzzy Logic Development Tool	DV005001	DV005001	DV005001	DV005001	DV005001	DV005001	DV005001	DV005001	DV005001	DV005001	—	—
*fuzzy*TECH-MP Edition Fuzzy Logic Development Tool	DV005002	DV005002	DV005002	DV005002	DV005002	DV005002	DV005002	DV005002	DV005002	DV005002	—	—
MP-DriveWay™ Applications Code Generator	—	SW006006	SW006006	SW006006	SW006006**	SW006006	SW006006	SW006006	SW006006	SW006006**	—	—
Total Endurance™ Software Model	—	—	—	—	—	—	—	—	—	—	SW242001	—
PROGRAMMERS												
PICSTART® Lite Ultra Low-Cost Development Kit	—	—	DV162003**	DV162002** DV162003**	—	DV162002** DV162003**	—	—	—	—	—	—
PICSTART Plus Low-Cost Development Kit	DV003001**	DV003001	DV003001	DV003001	DV003001	DV003001	DV003001	DV003001	DV003001	DV003001	—	—
PRO MATE® II Universal Programmer	DV007003	DV007003	DV007003	DV007003	DV007003	DV007003	DV007003	DV007003	DV007003	DV007003	DV007003**	DV007003**
KEELOQ® Programmer	—	—	—	—	—	—	—	—	—	—	—	PG306001
DEMONSTRATION BOARDS												
Serial EEPROM Designer's Kit	—	—	—	—	—	—	—	—	—	—	DV243001	—
PICDEM-1	—	—	DM163001	DM163001 (PIC16C61 only)	DM163001**	—	—	—	—	DM163001**	—	—
PICDEM-2	—	—	—	DM163002**	—	DM163002**	—	—	—	—	—	—
PICDEM-3	—	—	—	—	—	—	—	—	DM163003	—	—	—
PICDEM-14	—	DM143001	—	—	—	—	—	—	—	—	—	—
KeeLoq Evaluation Kit	—	—	—	—	—	—	—	—	—	—	—	DM303002

* Contact Microchip Technology Inc. for availability date.
** Development tool is available on select devices. Please refer to the Microchip *Development Systems Ordering Guide* for device-specific ordering numbers and more information.
*** Microchip Technology Inc., Telephone (602) 786-7627; HI-TECH Software LLC Telephone 1-800-735-5715 U.S.A., Telephone 61 7 3354 2411 Australia or Web Site www.htsoft.com.

MICROCHIP TECHNOLOGY INC. FUTURE PRODUCTS GUIDE* (As of March 1998)

PICmicro CMOS OTP 8-BIT MICROCONTROLLERS*

Product*	Program Memory OTP Bytes	Program Memory OTP Words	Data RAM Bytes	Max. Speed MHz	I/O Ports	ADC 8-Bits	Serial I/O	PWM	Brown-Out Detection	Comparators	Timers	In-Circuit Serial Programming™	Other Features	ROM Equivalent	Packages
PIC16C164	16384	8192x16	512	40	22	—	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	Improved Clock Generation	—	28P, 28SO, 28JW
PIC16C165	16384	8192x16	512	40	33	—	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	Parallel Slave Port, Improved Clock Generation	—	40P, 40JW, 44L, 44PT
PIC16C174	16384	8192x16	512	40	22	5	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	Improved Clock Generation	—	28P, 28SO, 28JW
PIC16C175	16384	8192x16	512	40	33	8	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	Parallel Slave Port, Improved Clock Generation	—	40P, 40JW, 44L, 44PT
PIC16C176	24576	12288x16	1024	40	22	5	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	Improved Clock Generation	—	28P, 28SO, 28JW
PIC16C177	24576	12288x16	1024	40	33	8	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	Parallel Slave Port, Improved Clock Generation	—	40P, 40JW, 44L, 44PT
PIC16C178	32768	16384x16	1536	40	22	5	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	Improved Clock Generation	—	28P, 28SO, 28JW
PIC16C179	32768	16384x16	1536	40	33	8	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	Parallel Slave Port, Improved Clock Generation	—	40P, 40JW, 44L, 44PT
PIC16C185	16384	8192x16	1024	33	50	5 (10-Bit)	USART/ I²C/SPI	3	Yes	—	4+WDT	Yes	CAN 2.0B, Parallel Slave Port, Improved Clock Generation	—	64SP, 68CL, 68L, 64PT
PIC16C471	1792	1024x14	128	20	12	4 (10-bit)	—	1	Yes	—	3+WDT	Yes	25mA source/sink per I/O, internal clock oscillator, Capture/Compare/PWM	—	14P, 14SO, 14JW
PIC16C472	3584	2048x14	128	20	12	4 (10-bit)	—	1	Yes	—	3+WDT	Yes	25mA source/sink per I/O, internal clock oscillator, Capture/Compare/PWM	—	14P, 14SO, 14JW
PIC16C555	896	512x14	80	20	22	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O	—	28SP, 28SO, 28SS, 28JW
PIC16C557	3584	2048x14	128	20	22	—	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O	—	28SP, 28SO, 28SS, 28JW
PIC16C772	3584	2048x14	128	20	22	6 (10-Bit)	I²C/SPI	1	Yes	—	3+WDT	Yes		—	28P, 28SO, 28SS, 28JW
PIC16C773	7168	4096x14	256	20	22	6 (10-Bit)	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes		—	28P, 28SO, 28SS, 28JW
PIC16C774	7168	4096x14	256	20	33	10 (10-Bit)	USART/ I²C/SPI	2	Yes	—	3+WDT	Yes	Parallel Slave Port	—	40P, 40JW, 44L, 44PT

*Contact Microchip Technology for availability date.

MICROCHIP TECHNOLOGY INC. FUTURE PRODUCTS GUIDE* (As of March 1998)

PICmicro *ENHANCED* FLASH 8-BIT MICROCONTROLLERS*

Product*	Program Memory FLASH Bytes	Program Memory FLASH Words	E²PROM Data Memory	Data RAM Bytes	Max. Speed MHz	I/O Ports	ADC 8-Bits	Serial I/O	PWM	Brown-Out Detection	Comparators	Timers	In-Circuit Serial Programming	Other Features	ROM Equivalent	Packages
PIC12F675	1792 (Flash)	1024 x 14 (Flash)	16	128	10	6	4 (10-bit)	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12F676	3584 (Flash)	2048 x 14 (Flash)	16	128	10	6	4 (10-bit)	—	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12F680	896 (Flash)	512 x 14 (Flash)	16	128	10	6	—	SSI	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC12F681	1792 (Flash)	1024 x 14 (Flash)	16	128	10	6	—	SSI	—	—	—	1+WDT	Yes	25mA source/sink per I/O, internal oscillator, 2.5V	—	8P, 8SM
PIC16F627	1792 (Flash)	1024 x 14 (Flash)	128	80	20	16	—	USART/ SCI	1	Yes	2	3+WDT	Yes	25mA source/sink per I/O, internal clock oscillator, 2.5V, Capture/Compare/PWM	—	18P, 18SO, 20SS
PIC16F628	3584 (Flash)	2048 x 14 (Flash)	128	128	20	16	—	USART/ SCI	1	Yes	2	3+WDT	Yes	25mA source/sink per I/O, internal clock oscillator, 2.5V, Capture/Compare/PWM	—	18P, 18SO, 20SS
PIC16F716	3584 (Flash)	2048 x 14 (Flash)	128	128	20	16	4 (10-bit)	—	1	Yes	—	3+WDT	Yes	25mA source/sink per I/O, internal clock oscillator, 2.5V, Capture/Compare/PWM	—	18P, 18SO, 20SS
PIC16F787	7168 (Flash)	4096 x 14 (Flash)	128	128	20	18	4 (10-bit)	USART/ SCI	1	Yes	—	3+WDT	Yes	25mA source/sink per I/O, internal clock oscillator, 2.5V, Capture/Compare/PWM	—	20P, 20SO, 20SS
PIC16F825	3584 (Flash)	2048 x 14 (Flash)	64	128	20	22	—	USART	1	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28P, 28SO, 28SS
PIC16F83A	896 (Flash)	512 x 14 (Flash)	64	36	20	13	—	—	—	—	—	1+WDT	Yes	20mA source and 25mA sink per I/O, 64 bytes data EEPROM, 2.0V Operation	—	18P, 18SO, 20SS
PIC16F84A	1792 (Flash)	1024 x 14 (Flash)	64	68	20	13	—	—	—	—	—	1+WDT	Yes	20mA source and 25mA sink per I/O, 64 bytes data EEPROM, 2.0V Operation	—	18P, 18SO, 20SS
PIC16F863	7168 (Flash)	4096 x 14 (Flash)	128	192	20	22	—	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28P, 28SO, 28SS
PIC16F865	7168 (Flash)	4096 x 14 (Flash)	128	192	20	33	—	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	—	40P, 44L, 44PT
PIC16F866	14336 (Flash)	8192 x 14 (Flash)	256	368	20	22	—	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28P, 28SO, 28SS
PIC16F867	14336 (Flash)	8192 x 14 (Flash)	256	368	20	33	—	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, Parallel Slave Port	—	40P, 44L, 44PT
PIC16F872	3584 (Flash)	2048 x 14 (Flash)	64	128	20	22	5 (10-Bit)	I²C/SPI	1	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28P, 28SO, 28SS
PIC16F873	7168 (Flash)	4096 x 14 (Flash)	128	192	20	22	5 (10-Bit)	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, 2 Capture/Compare/PWM	—	28P, 28SO, 28SS
PIC16F874	7168 (Flash)	4096 x 14 (Flash)	128	192	20	33	8 (10-Bit)	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Parallel Slave Port, 2 Capture/Compare/PWM	—	40P, 44L, 44PT
PIC16F876	14336 (Flash)	8192 x 14 (Flash)	256	368	20	22	5 (10-Bit)	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM	—	28P, 28SO, 28SS
PIC16F877	14336 (Flash)	8192 x 14 (Flash)	256	368	20	33	8 (10-Bit)	USART/ I²C/SPI	2	Yes	2	3+WDT	Yes	25mA source/sink per I/O, Capture/Compare/PWM, Parallel Slave Port	—	40P, 44L, 44PT

*Contact Microchip Technology for availability date.

Abbreviation:

ADC = Analog-to-Digital Converter
CAP = Capture
CCP = Capture/Compare/PWM
DAC = Digital-to-Analog Converter
E² = EEPROM (Reprogrammable)
I²C = Inter-integrated Circuit Bus
PWM = Pulse Width Modulator
SPI = Serial Peripheral Interface
USART = Universal Synchronous/Asynchronous Receiver/Transmitter
WDT = Watchdog Timer
SLAC = Slope A/D Converter, up to 16 bits
SMB = System Management Bus

MICROCHIP

SECTION 2
MEMORY PRODUCTS SELECTION AND CROSS REFERENCE

Serial EEPROMs	Serial EEPROM Selection Guide	2-1
	Serial EEPROM Cross Reference Guide	2-5
Parallel EPROMs	Parallel EEPROM Selection Guide	2-15
EPROMs	EPROM Selection Guide	2-17
	EPROM Cross Reference Guide	2-19

SERIAL EEPROMS

Serial EEPROM Selection Guide

I²C™

Device	Density/ Organization	Page Buffer	Write Speed	Max Clock Frequency	Temp Range	# Pins	Package Types	Operating Voltage
24AA00	128K bits (16 x 8)	N/A	4 ms	400 kHz	C,I	8	OT,P, SN, ST	1.8V – 6.0V
24LC00	128K bits (16 x 8)	N/A	4 ms	400 kHz	C,I	8	OT,P, SN	2.5V – 6.0V
24C00	128K bits (16 x 8)	N/A	4 ms	400 kHz	C,I,E	8	OT,P, SN	4.5V – 5.5V
24AA01	1K bits (128 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P, SM,SN	1.8V – 5.5V
24AA02	2K bits (256 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P,SM,SN	1.8V – 5.5V
24LC01B	1K bits (128 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P,SM,SN	2.5V – 5.5V
24LC02B	2K bits (256 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P,SM,SN	2.5V – 5.5V
24AA04	4K bits (512 x 8)	16 bytes	10 ms	400 kHz	C,I	8,14	P,SL,SM,SN	1.8V – 5.5V
24LCS52	2K bits (256 x 8)	16 bytes	10 ms	400 kHz	C,I	8	P,SN,ST	2.5V – 5.5V
24C04A	4K bits (512 x 8)	8 bytes	1 ms	100 kHz	C,I,E	8,14	P,SN,SM,SL	4.5V – 5.5V
24C01SC	1K bits (128 X 8)	8 bytes	10 ms	400 kHz	C	8	WF	4.5V – 5.5V
24C02SC	2K bits (256 x 8)	8 bytes	10 ms	400 kHz	C	8	WF	4.5V – 5.5V
24LC21	1K bits (128 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.5V
24LC21A	1K bits (128 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P	2.5V – 5.5V
24LCS21	1K bits (128 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.0V
24LCS21A	1K bits (128 x 8)	8 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.0V
24LC41	1K/4K bits	8 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.0V
24LC41A	1K/4K bits	8 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.0V
24LCS41	1K/4K bits	8 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.0V
24LCS41A	1K/4K bits	8 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.0V
24AA08	8K bits (1K x 8)	16 bytes	10 ms	400 kHz	C,I	8,14	P,SL,SM,SN	1.8V – 5.5V
24LC04B	4K bits (512 x 8)	16 bytes	10 ms	400 kHz	C,I	8,14	P,SL,SM,SN	2.5V – 5.5V
24LC08B	8K bits (1K x 8)	16 bytes	10 ms	400 kHz	C,I	8,14	P,SL,SM,SN	2.5V – 5.5V
24C08B	8K bits (1K x 8)	16 bytes	10 ms	100 kHz	E	8,14	P,SL,SN	4.5V – 5.5V
24C16B	16K bits (2K x 8)	16 bytes	10 ms	100 kHz	E	8,14	P,SL,SN	4.5V – 5.5V
24AA16	16K bits (2K x 8)	16 bytes	10 ms	400 kHz	C,I	8,14	P,SL,SN	1.8V – 5.5V
24LC16B	16K bits (2K x 8)	16 bytes	10 ms	400 kHz	C,I	8,14	P,SL,SN	2.5V – 5.5V
24FC16	16K bits (2K x 8)	16 bytes	10 ms	1 MHz	C,I	8, 14	P,SN	4.5V – 5.0V
24AA164	16K bits (2K x 8)	16 bytes	10 ms	400 kHz	C	8	P,SN	1.8V – 5.5V
24LC164	16K bits (2K x 8)	16 bytes	10 ms	400 kHz	C,I	8	P,SN	2.5V – 5.5V
24AA174	16K bits (2K x 8)	16 bytes +16 bytes	10 ms	400 kHz	C	8	P,SN	1.8V – 5.5V
24LC174	16K bits (2K x 8)	16 bytes +16 bytes	10 ms	400 kHz	C	8	P,SN	2.5V – 5.5V
24AA32A	32K bits (4K x 8)	32 bytes	5 ms	400 kHz	C	8	P,SN	1.8V – 5.5V

I²C is a trademark of Philips Corporation.

Serial EEPROMs

I²C™ (Continued)

Device	Density/ Organization	Page Buffer	Write Speed	Max Clock Frequency	Temp Range	# Pins	Package Types	Operating Voltage
24LC32A	32K bits (4K x 8)	32 bytes	5 ms	400 kHz	C,I	8	P,SN	2.5V – 5.5V
24C32A	32K bits (4K x 8)	32 bytes	5 ms	400 kHz	C,I	8	P,SN	4.5V – 5.5V
24AA32	2K bits (4K x 8)	64 bytes	5 ms	100 kHz	C	8	P,SM	1.8V – 5.5V
24LC32	32K bits (4K x 8)	64 bytes	5 ms	400 kHz	C,I	8	P,SM	2.5V – 6.0V
24C32	32K bits (4K x 8)	64 bytes	5 ms	400 kHz	C,I	8	P,SM	4.5V – 5.0V
24FC32	32K bits (4K x 8)	64 bytes	5 ms	1 MHz	C,I	8	P,SM	4.5V – 5.0V
24AA64	64K bits (8K x 8)	32 bytes	5 ms	400 kHz	I	8	P,SN,SM,ST	1.8V – 5.5V
24LC64	64K bits (8K x 8)	32 bytes	5 ms	400 kHz	I,E	8	P,SN,SM,ST	2.5V – 5.5V
24AA65	64K bits (8K x 8)	64 bytes	5 ms	400 kHz	C	8	P,SM	1.8V – 5.5V
24LC65	64K bits (8K x 8)	64 bytes	5 ms	400 kHz	C,I	8	P,SM	2.5V – 6.0V
24C65	64K bits (8K x 8)	64 bytes	5 ms	100 kHz	C,I	8	P,SM	4.5V – 5.5V
24FC65	64K bits (8K x 8)	64 bytes	5 ms	1 MHz	C,I	8	P,SN	4.5V – 5.0V
24AA128	128K bits (16 x 8)	64 bytes	5 ms	400 kHz	I	8	P,SN,SM,ST	1.8V – 5.5V
24LC128	128K bits (16 x 8)	64 bytes	5 ms	400 kHz	I,E	8	P,SN,SM,ST	2.5V – 5.5V
24AA256	256K bits (32 x 8)	64 bytes	5 ms	400 kHz	I	8	P,SM,ST	1.8V – 5.5V
24LC256	256K bits (32 x 8)	64 bytes	5 ms	400 kHz	I,E	8	P,SM,ST	2.5V – 5.5V

Microwire®

Device	Density/ Organization	Page Buffer	Write Speed	Max Clock Frequency	Temp Range	# Pins	Package Types	Operating Voltage
93AA46	1K bits (x8 or x16)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	1.8V – 5.5V
93AA56	2K bits (x8 or x16)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	1.8V – 5.5V
93AA66	4K bits (x8 or x16)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	1.8V – 5.5V
93LC46A	1K bits (128 x 8)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	2.0V – 6.0V
93LC46B	1K bits (64 x 16)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	2.0V – 6.0V
93LC56A	2K bits (256 x 8)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	2.0V – 6.0V
93LC56B	2K bits (128 x 16)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	2.0V – 6.0V
93LC66A	4K bits (512 x 8)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	2.0V – 6.0V
93LC66B	4K bits (256 x 16)	N/A	10 ms	2 MHz	C,I	8	P,SM,SN	2.0V – 6.0V
93LCS56	2K bits (128 x 16)	N/A	10 ms	2 MHz	C,I	8,14	P,SL,SM,SN	2.5V – 6.0V
93LCS66	2K bits (128 x 16)	N/A	10 ms	2 MHz	C,I	8,14	P,SL,SM,SN	2.5V – 6.0V
93AA76	8K bits (1024 x 8 or 512 x 16)	N/A	10 ms	3 MHz	C	8	P, SN	1.8V – 6.0V
93AA86	16K bits (2048 x 8 or 1024 x 16)	N/A	10 ms	3 MHz	C	8	P, SN	1.8V – 6.0V
93LC76	8K bits (1024 x 8 or 512 x 16)	N/A	10 ms	3 MHz	C, I	8	P, SN	2.5V – 6.0V
93LC86	16K bits (2048 x 8 or 1024 x 16)	N/A	10 ms	3 MHz	C, I	8	P, SN	2.5V – 6.0V
93C76	1K bits (64 x 16)	N/A	1 ms	1 MHz	E	8	P,SM,SN	4.5V – 5.5V
93C86	1K bits (64 x 16)	N/A	1 ms	1 MHz	E	8	P,SM,SN	4.5V – 5.5V

Microwire is a registered trademark of National Semiconductor Incorporated.

SPI™

Device	Density/ Organization	Page Buffer	Write Speed	Max Clock Frequency	Temp Range	# Pins	Package Types	Operating Voltage
25AA040	4K bits (512 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN,ST	1.8V – 6.0V
25LC040	4K bits (512 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN,ST	2.5V – 6.0V
25C040	4K bits (512 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN,ST	4.5V – 5.5V
25AA080	8K bits (1024 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN	1.8V – 6.0V
25LC080	8K bits (1024 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN	2.5V – 6.0V
25C080	8K bits (1024 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN	4.5V – 5.5V
25AA160	16K bits (2048 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN	1.8V – 6.0V
25LC160	16K bits (2048 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN	2.5V – 6.0V
25C160	16K bits (2048 x 8)	16 bytes	5 ms	3 MHz	C,I	8	P,SN	4.5V – 5.5V
25AA320	32K bits (4096 x 8)	32 bytes	5 ms	3 MHz	C,I	8	P,SN	1.8V – 6.0V
25LC320	32K bits (4096 x 8)	32 bytes	5 ms	3 MHz	C,I	8	P,SN	2.5V – 6.0V
25C320	32K bits (4096 x 8)	32 bytes	5 ms	3 MHz	C,I	8	P,SN	4.5V – 5.5V
25AA640	64K bits (8192 x 8)	32 bytes	5 ms	1 MHz	C,I	8	P,SN,ST	1.8V – 5.5V
25LC640	64K bits (8192 x 8)	32 bytes	5 ms	2 MHz	C,I	8	P,SN,ST	2.5V – 5.5V
25C640	64K bits (8192 x 8)	32 bytes	5 ms	3 MHz	C,I,E	8	P,SN,ST	4.5V – 5.5V

L = Plastic Leaded Chip Carrier
P = Plastic Dual In-Line Package
S = Die in Waffle Pack
W = Die in Wafer Form
OT = 3-Lead Small Outline Transistor
SL = 14-Lead Small Outline—150 mil
SM = 8-Lead Small Outline—208 mil
SN = 8-Lead Small Outline—150 mil
SO = Small Outline—300 mil
SS = Shrink Small Outline Package—209 mil
ST = Thin Shrink Small Outline Package—4.4 mil
TO = 3-Lead Plastic Transistor Outline
TS = Thin Small Outline—8mm x 20mm
TT = 3-Lead Plastic Small Outline Transistor
VS = Very Small Outline—8mm x 13.4mm
WF = Sawed Wafer on Frame

Note 1: Not All Combinations Of Speed/Temperature Range/Package/etc. are available. Consult Factory For Specific Part Information.

SPI is a trademark of Motorola Corporation.

NOTES:

MICROCHIP

Serial EEPROM Cross Reference Guide

The purpose of this document is to provide a quick way to determine the closest Microchip equivalent to Serial EEPROMs produced by other manufacturers. The cross reference section is broken down by manufacturer and lists all parts from that manufacturer, and the comparable Microchip part number. There is also a listing of manufacturer's part numbering schemes to assist in determining the specifications of a particular part.

There are subtle differences from manufacturer to manufacturer and device to device, so Microchip recommends consulting the respective manufacturer's databook for specific details.

Microchip provides a wide selection of Serial EEPROM devices, both from a density and a packaging standpoint, as well as several different protocols. If you are interested in a part that is not listed in this book, please contact your local distributor or sales representative for assistance.

The manufacturers included in this document are as follows:

AKM	National Semconductor
Atmel	Oki
Catalyst	Philips
Exel	Samsung
ISSI	SGS-Thomson
Microchip	Siemens
Mitsubishi	Xicor

Manufacturer	Part Number	Closest Microchip Equivalent	Size (bits)
AKM	AK6002A	24LC024	2K
AKM	AK6420A	24AA02	2K
AKM	AK6440A	24AA04	4K
AKM	AK6480A	24AA08	8K
AKM	AK93C45A	93AA46	1K
AKM	AK93C55A	93AA56	2K
AKM	AK93C65A	93AA66	4K
AKM	AK93C85A	93AA86	16K
Atmel	AT24C01	24LC01B	1K
Atmel	AT24C01-1.8	24AA01	1K
Atmel	AT24C01-2.5	24LC01B	1K
Atmel	AT24C01-2.7	24LC01B	1K
Atmel	AT24C01A	24C01C	1K
Atmel	AT24C01A-1.8	24LC024	1K
Atmel	AT24C01A-2.5	24LC024	1K
Atmel	AT24C01A-2.7	24LC024	1K
Atmel	AT24C02	24LC024	2K
Atmel	AT24C02-1.8	24LC024	2K
Atmel	AT24C02-2.5	24LC024	2K
Atmel	AT24C02-2.7	24LC034	2K
Atmel	AT24C04	24LC04B	4K
Atmel	AT24C04-1.8	24AA04	4K
Atmel	AT24C04-2.5	24LC04B	4K
Atmel	AT24C04-2.7	24LC04B	4K
Atmel	AT24C08	24LC08B	8K
Atmel	AT24C08-1.8	24AA08	8K
Atmel	AT24C08-2.5	24LC08B	8K
Atmel	AT24C08-2.7	24LC08B	8K
Atmel	AT24C16	24LC16B	16K
Atmel	AT24C16-1.8	24AA16	16K
Atmel	AT24C16-2.5	24LC16B	16K
Atmel	AT24C16-2.7	24LC16B	16K
Atmel	AT24C164	24LC164	16K
Atmel	AT24C164-1.8	24AA164	16K
Atmel	AT24C164-2.5	24LC164	16K
Atmel	AT24C164-2.7	24LC164	16K
Atmel	AT24C32	24LC32	32K
Atmel	AT24C32-1.8	24AA32	32K
Atmel	AT24C32-2.5	24LC32	32K
Atmel	AT24C32-2.7	24LC32	32K

Serial EEPROMs

Manufacturer	Part Number	Closest Microchip Equivalent	Size (bits)
Atmel	AT24C64	24LC64	64K
Atmel	AT24C64-1.8	24AA64	64K
Atmel	AT24C64-2.5	24LC64	64K
Atmel	AT24C64-2.7	24LC64	64K
Atmel	AT24C128	24LC128	128K
Atmel	AT24C128-1.8	24AA128	128K
Atmel	AT24C128-2.7	24LC128	128K
Atmel	AT24C256	24LC256	256K
Atmel	AT24C256-1.8	24AA256	256K
Atmel	AT24C256-2.7	24LC256	256K
Atmel	AT93C46	93LC46	1K
Atmel	AT93C46-1.8	93AA46	1K
Atmel	AT93C46-2.5	93LC46	1K
Atmel	AT93C46-2.7	93LC46	1K
Atmel	AT93C46A	93C46/ 93LC46B	1K
Atmel	AT93C56-1.8	93AA56	2K
Atmel	AT93C56-2.5	93LC56	2K
Atmel	AT93C56-2.7	93LC56	2K
Atmel	AT93C66	93LC66	4K
Atmel	AT93C66-1.8	93AA66	4K
Atmel	AT93C66-2.5	93LC66	4K
Atmel	AT93C66-2.7	93LC66	4K
Atmel	AT25040	25C040	4K
Atmel	AT25040-1.8	25AA040	4K
Atmel	AT25040-2-7	25LC040	4K
Atmel	AT25080	25C080	8K
Atmel	AT25080-1.8	25AA080	8K
Atmel	AT25080-2-7	25LC080	8K
Atmel	AT25160	25C160	16K
Atmel	AT25160-1.8	25AA160	16K
Atmel	AT25160-2-7	25LC160	16K
Atmel	AT25320	25C320	32K
Atmel	AT25320-2-7	25LC320	32K
Atmel	AT25640	25C640	64K
Atmel	AT25640-1.8	25AA640	64K
Atmel	AT25640-2-7	25LC640	64K
Atmel	AT25128	25C128	128K
Atmel	AT25128-1.8	25AA128	128K
Atmel	AT25128-2-7	25LC128	128K
Atmel	AT25256	25C256	256K
Atmel	AT25256-1.8	25AA256	256K
Atmel	AT25256-2-7	25LC256	256K
Catalyst	CAT24WC01	24LC024	1K
Catalyst	CAT24WC01-1.8	24LC024	1K
Catalyst	CAT24WC02	24LC024	2K
Catalyst	CAT24WC02-1.8	24LC024	2K
Catalyst	CAT24WC04	24LC04B	4K

Manufacturer	Part Number	Closest Microchip Equivalent	Size (bits)
Catalyst	CAT24WC04-1.8	24AA04B	4K
Catalyst	CAT24WC08	24LC08B	8K
Catalyst	CAT24WC08-1.8	24AA04B	8K
Catalyst	CAT24WC16	24LC164	16K
Catalyst	CAT24WC16-1.8	24AA164	16K
Catalyst	CAT24WC32	24LC32	32K
Catalyst	CAT24WC32-1.8	24AA32	32K
Catalyst	CAT24WC64	24LC64	64K
Catalyst	CAT24WC64-1.8	24AA64	64K
Catalyst	CAT24WC128	24LC128	128K
Catalyst	CAT24WC128-1.8	24AA128	128K
Catalyst	CAT24WC256	24LC256	256K
Catalyst	CAT24WC256-1.8	24AA256	256K
Catalyst	CAT93C46	93LC46A (X8)/ 93LC46B (X16)	1K
Catalyst	CAT93C46-1.8	93AA46	1K
Catalyst	CAT93C56	93LC56A (X8)/ 93LC56B (X16)	2K
Catalyst	CAT93C56-1.8	93AA56	2K
Catalyst	CAT93C57	93LC56A (X8)/ 93LC56B (X16)	
Catalyst	CAT93C57-2.7	93LC56A (X8)/ 93LC56B (X16)	
Catalyst	CAT93C57-2.5	93LC56A (X8)/ 93LC56B (X16)	
Catalyst	CAT93C57-1.8	93AA56	
Catalyst	CAT93C66	93LC66A (X8)/ 93LC66B (X16)	4K
Catalyst	CAT93C66-1.8	93AA66	4K
Catalyst	CAT93C86	93LC86	16K
Catalyst	CAT93C86-1.8	93AA86	16K
Catalyst	CAT25C64	25LC640	64K
Catalyst	CAT25C64-1.8	25AA640	64K
Catalyst	CAT25C128	25C128	128K
Catalyst	CAT25C128-1.8	25AA128	128K
Exel	XL24164	24LC164	16K
Exel	XL24C01A	24C01C/ 24LC01B	1K
Exel	XL24C02	24C02A/ 24LC02B	2K
Exel	XL24C04	24C04A/ 24LC04B	4K
Exel	XL24C08	24LC08B	8K
Exel	XL24C16	24LC16B	16K
Exel	XL24LC21	24LC21	2K
Exel	XL25081	25LC080	8K
Exel	XL25161	25LC160	16K
Exel	XL93LC06A	93C06	256 bits
Exel	XL93LC46	93LC46B	1K

Manufacturer	Part Number	Closest Microchip Equivalent	Size (bits)
Exel	XL93LC46A	93C46/ 93LC46B	1K
Exel	XL93LC46B	93AA46B	1K
Exel	XL93LC56	93LC56B	2K
Exel	XL93LC56A	93LC56B	2K
Exel	XL93LC56B	93AA56B	2K
Exel	XL93LC66	93LC66B	4K
Exel	XL93LC66A	93LC66B	4K
Exel	XL93LC66B	93AA66B	4K
National	NM24C02	24LC024	2K
National	NM24C02L	24LC024	2K
National	NM24C03	24LC024	2K
National	NM24C03L	24LC024	2K
National	NM24C04	24LC04B	4K
National	NM24C04L	24LC04B	4K
National	NM24C05	24LC04B	4K
National	NM24C05L	24LC04B	4K
National	NM24C08	24LC08B	8K
National	NM24C08L	24LC08B	8K
National	NM24C09	24LC08B	8K
National	NM24C09L	24LC08B	8K
National	NM24C16	24LC16B	16K
National	NM24C16L	24LC16B	16K
National	NM24C17	24LC16B	16K
National	NM24C17L	24LC16B	16K
National	NM24C65	24C65/ 24C64	64K
National	NM24C65L	24LC64	64K
National	NM24C65LZ	24LC64	64K
National	NM24C65XLZ	24AA64	64K
National	NM25C040	25C040	4K
National	NM25C040L	25LC040	4K
National	NM25C160	25C160	16K
National	NM25C160L	25LC160	16K
National	NM93C46	93LC46B	1K
National	NM93C46A	93LC46A (X8)/ 93LC46B (X16)	1K
National	NM93C46AL	93LC46A (X8)/ 93LC46B (X16)	1K
National	NM93C46L	93LC46B	1K
National	NM93C46LZ	93LC46B	1K
National	NM93C46XLZ	93LC46B	1K
National	NM93C56	93LC56B	2K
National	NM93C56A	93LC56A (X8)/ 93LC56B (X16)	2K
National	NM93C56L	93C56B	2K
National	NM93C56LZ	93LC56B	2K
National	NM93C66	93C66B	4K
National	NM93C66L	93LC66B	4K
National	NM93C66LZ	93LC66B	4K

Manufacturer	Part Number	Closest Microchip Equivalent	Size (bits)
National	NM93C86	93C86	16K
National	NM93C86A	93C86	16K
National	NM93CS56	93LCS56	2K
National	NM93CS56L	93LCS56	2K
National	NM93CS56LZ	93LCS56	2K
National	NM93CS66	93LCS66	4K
National	NM93CS66L	93LCS66	4K
National	NM93CS66LZ	93LCS66	4K
Philips-Signetics	PCA8581	24C01C	1K
Philips-Signetics	PCA8581C	24LC024	1K
Philips-Signetics	PCB2421	24LCS21	1K
Philips-Signetics	PCF85116-3	24LC16B	16K
Philips-Signetics	PCF8582C-2	24LC024	2K
Philips-Signetics	PCF8594C-2	24C04A	4K
Philips-Signetics	PCF8598C-2	24LC164	16K
SGS-Thomson	M24C01	24C01C	1K
SGS-Thomson	M24C01-W	24LC024	1K
SGS-Thomson	M24C01-R	24LC024	1K
SGS-Thomson	M24C02	24C02C	2K
SGS-Thomson	M24C02-W	24LC024	2K
SGS-Thomson	M24C02-R	24LC024	2K
SGS-Thomson	M24C04	24C04A	4K
SGS-Thomson	M24C04-W	24LC04B	4K
SGS-Thomson	M24C04-R	24AA04	4K
SGS-Thomson	M24C08	24C08B	8K
SGS-Thomson	M24C08-W	24LC08B	8K
SGS-Thomson	M24C08-R	24AA08	8K
SGS-Thomson	M24C16	24LC164	16K
SGS-Thomson	M24C16-W	24LC164	16K
SGS-Thomson	M24C16-R	24AA164	16K
SGS-Thomson	M24C32	24C32	32K
SGS-Thomson	M24C32-W	24LC32	32K
SGS-Thomson	M24C32-R	24AA32	32K
SGS-Thomson	M24C64	24C64	64K
SGS-Thomson	M24C64-W	24LC64	64K
SGS-Thomson	M24C64-R	24AA64	64K
SGS-Thomson	M24C128	24C128	128K
SGS-Thomson	M24C128-W	24LC128	128K
SGS-Thomson	M24C128-R	24AA128	128K
SGS-Thomson	M24C256	24C256	256K
SGS-Thomson	M24C256-W	24LC256	256K
SGS-Thomson	M24C256-R	24AA256	256K
SGS-Thomson	M93C46	93C46B	1K
SGS-Thomson	M93C46-W	93LC46A (X8) 93LC46B (X16)	1K
SGS-Thomson	M93C46-R	93AA46	1K
SGS-Thomson	M93C56	93C56A (X8) 93C56B (X16)	2K

Serial EEPROMs

Manufacturer	Part Number	Closest Microchip Equivalent	Size (bits)
SGS-Thomson	M93C56-W	93LC56A (X8) 93LC56B (X16)	2K
SGS-Thomson	M93C56-R	93AA56	2K
SGS-Thomson	M93S56	93LCS56	2K
SGS-Thomson	M93C66	93C66A (X8) 93C66B (X16)	4K
SGS-Thomson	M93C66-W	93LC66A (X8) 93LC66B (X16)	4K
SGS-Thomson	M93C66-R	93AA66	4K
SGS-Thomson	M93S66	93LCS66	4K
SGS-Thomson	M93C76	93C76	8K
SGS-Thomson	M93C76-W	93LC76	8K
SGS-Thomson	M93C76-R	93AA76	8K
SGS-Thomson	M93C86	93C86	16K
SGS-Thomson	M93C86-W	93LC86	16K
SGS-Thomson	M93C86-R	93AA66	16K
SGS-Thomson	ST95040	25C040	4K
SGS-Thomson	ST95040-W	25LC040	4K
SGS-Thomson	ST95080	25C080	8K
SGS-Thomson	ST95080-W	25LC080	8K
SGS-Thomson	M34C02	24LCS52	2K
SGS-Thomson	M34C02-W	24LCS52	2K
SGS-Thomson	ST24LC21B	24LC21	1K
SGS-Thomson	ST24FC21	24LC21A	1K
SGS-Thomson	ST24LW21	24LCS21	1K
SGS-Thomson	ST24FW21	24LCS21A	1K
SGS-Thomson	M24164	24LC164	16K
SGS-Thomson	M24164-W	24LC164	16K
SGS-Thomson	M24164-R	24AA164	16K
Xicor	X24C00	24LC00	128 bit
Xicor	X24C01	24C01C/ 24LC01B	1K
Xicor	X24C01-3.0	24LC01B	1K
Xicor	X24C01-3.5	24LC01B	1K
Xicor	X24C01A	24C01C/ 24LC01B	1K
Xicor	X24C01A-2.7	24LC01B	1K
Xicor	X24C01A-3.0	24LC01B	1K
Xicor	X24C01A-3.5	24LC01B	1K
Xicor	X24012	24LC024	1K
Xicor	X24C02	24C02C/ 24LC024	2K
Xicor	X24C02-2.7	24LC024	2K
Xicor	X24C02-3.0	24LC024	2K
Xicor	X24C02-3.5	24LC024	2K
Xicor	X24022	24LC024	2K
Xicor	X24C04	24C04A/ 24LC04B	4K
Xicor	X24C04-2.7	24LC04B	4K
Xicor	X24C04-3.0	24LC04B	4K
Xicor	X24C04-3.5	24LC04B	4K
Xicor	X24C08	24LC08B	8K
Xicor	X24C08-2.7	24LC08B	8K
Xicor	X24C08-3.0	24LC08B	8K
Xicor	X24C08-3.5	24LC08B	8K
Xicor	X24C16	24LC16B	16K
Xicor	X24C16-2.7	24LC16B	16K
Xicor	X24C16-3.0	24LC16B	16K
Xicor	X24C16-3.5	24LC16B	16K
Xicor	X24164	24LC164	16K
Xicor	X24164-2.7	24LC164	16K
Xicor	X24164-3.0	24LC164	16K
Xicor	X24164-3.5	24LC164	16K
Xicor	X24321	24C32	32K
Xicor	X24321-2.5	24LC32	32K
Xicor	X24321-1.8	24AA32	32K
Xicor	X24641	24C64	64K
Xicor	X24641-2.5	24LC64	64K
Xicor	X24641-1.8	24AA64	64K
Xicor	X24645	24LC65/ 24LC64	64K
Xicor	X24128	24C128	128K
Xicor	X24128-2.5	24LC128	128K
Xicor	X24128-1.8	24AA128	128K
Xicor	X25040	25LC040	4K
Xicor	X25040-3.0	25LC040	4K
Xicor	X25040-2.7	25LC040	4K
Xicor	X25080	25C080	8K
Xicor	X25080-2.7	24LC080	8K
Xicor	X25160	25C080	16K
Xicor	X25160-2.7	24LC160	16K
Xicor	X25320	25LC320	32K
Xicor	X25320-2.7	25LC320	32K
Xicor	X25640	25LC640	64K
Xicor	X25640-2.7	25LC640	64K
Xicor	X25642	25LC640	64K
Xicor	X25642-2.7	25LC640	64K
Xicor	X25128	25LC128	128K
Xicor	X25128-2.7	25LC128	128K

COMPETITIVE PART NUMBER BREAKDOWN

FIGURE 1: AKM – NOT AVAILABLE

FIGURE 2: ATMEL

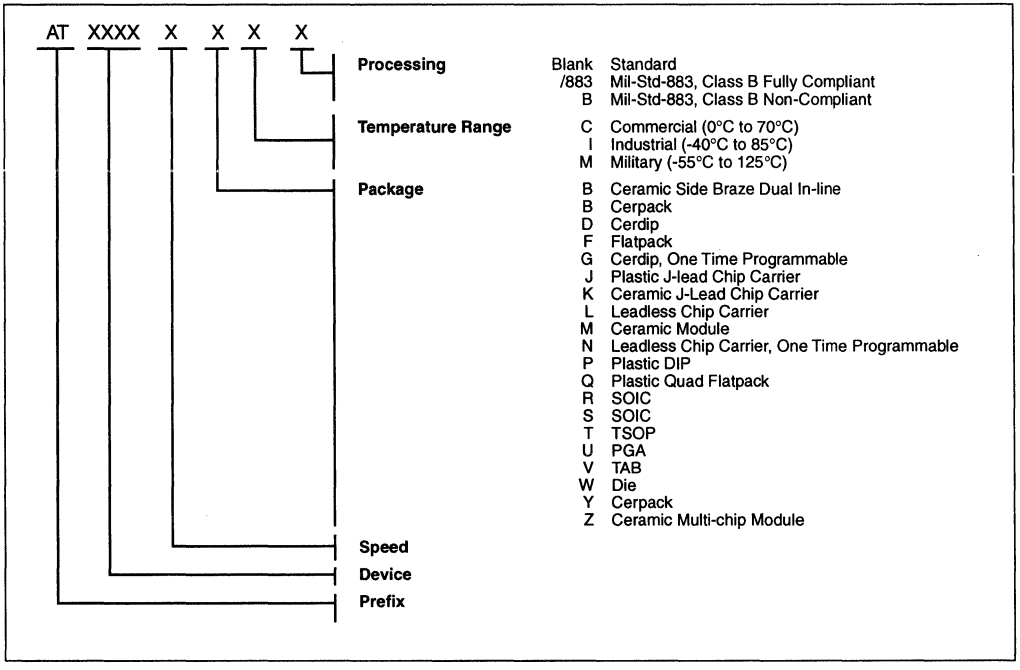


FIGURE 3: CATALYST SEMICONDUCTOR

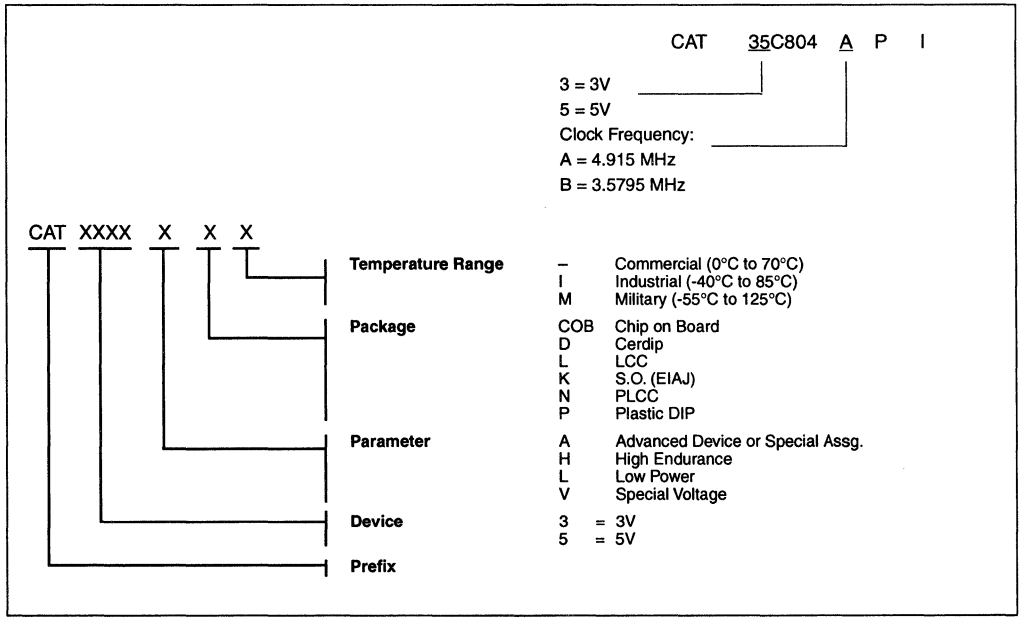


FIGURE 4: EXEL

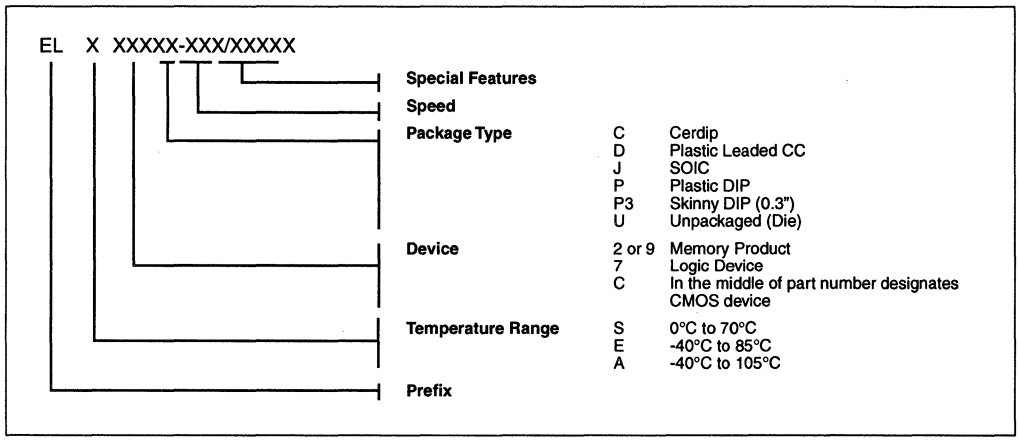


FIGURE 5: ISSI—NOT AVAILABLE

FIGURE 6: MICROCHIP SERIAL EEPROM PART NUMBER GUIDE

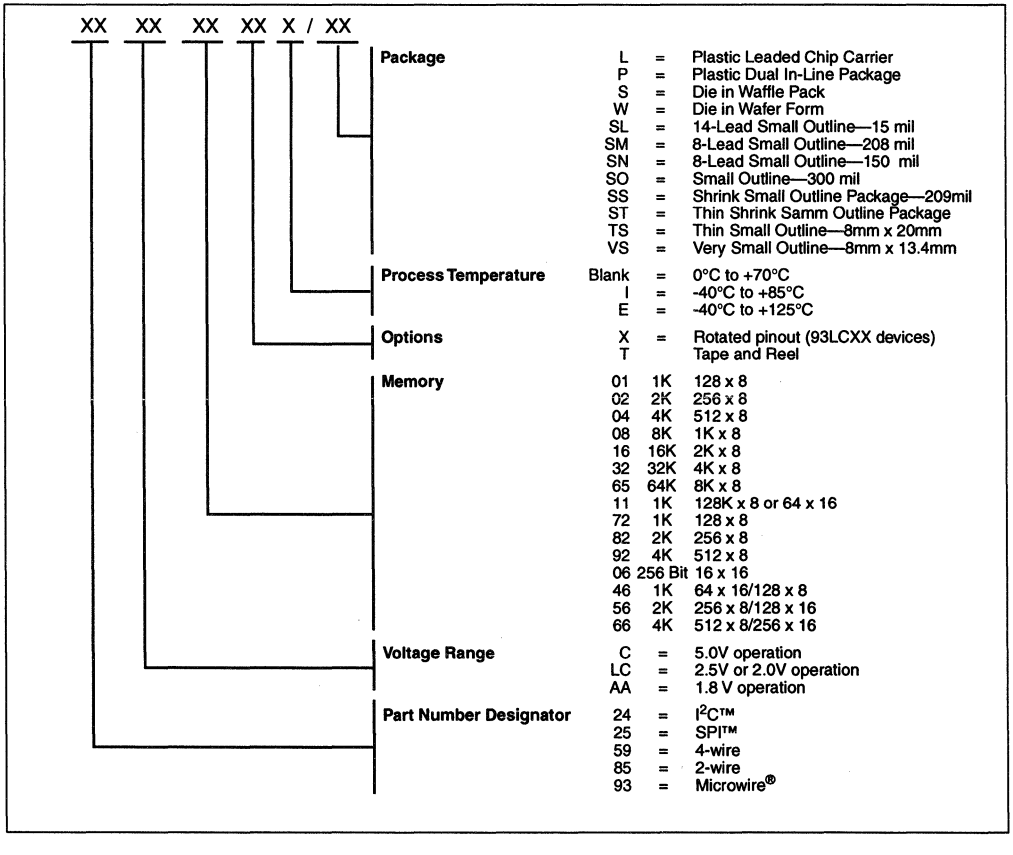


FIGURE 7: NATIONAL SEMICONDUCTOR CORPORATION

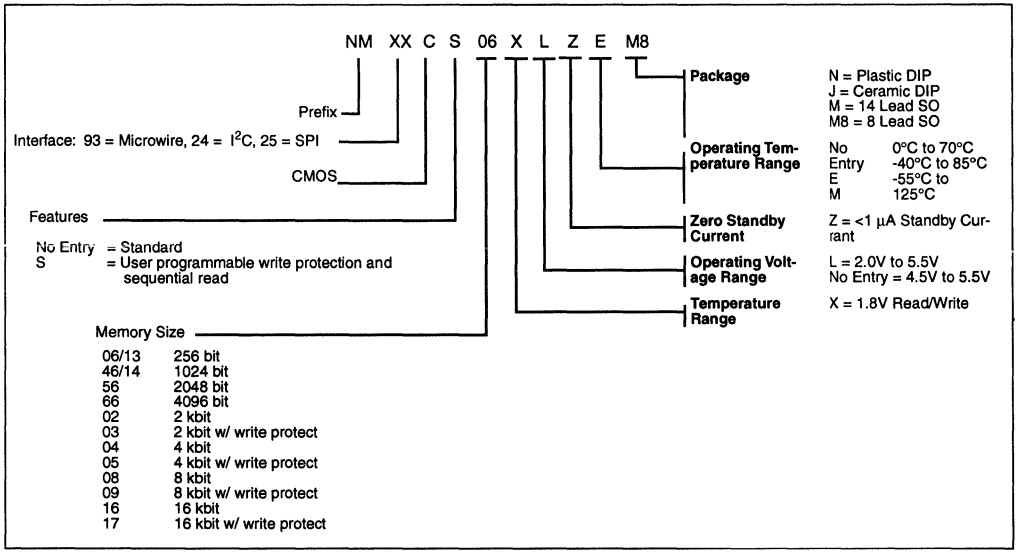


FIGURE 8: MITSUBISHI—NOT AVAILABLE

FIGURE 9: OKI—NOT AVAILABLE

FIGURE 10: PHILIPS

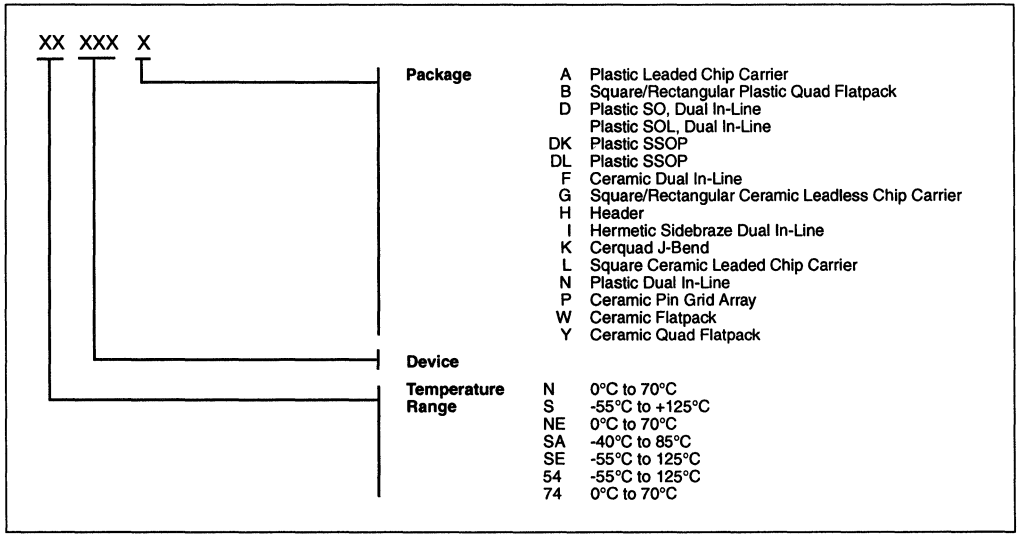


FIGURE 11: SAMSUNG

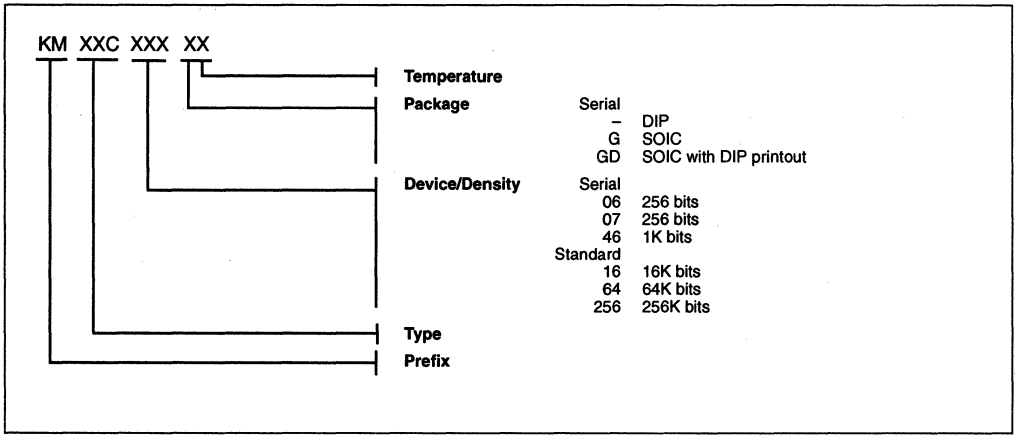


FIGURE 12: SEEQ

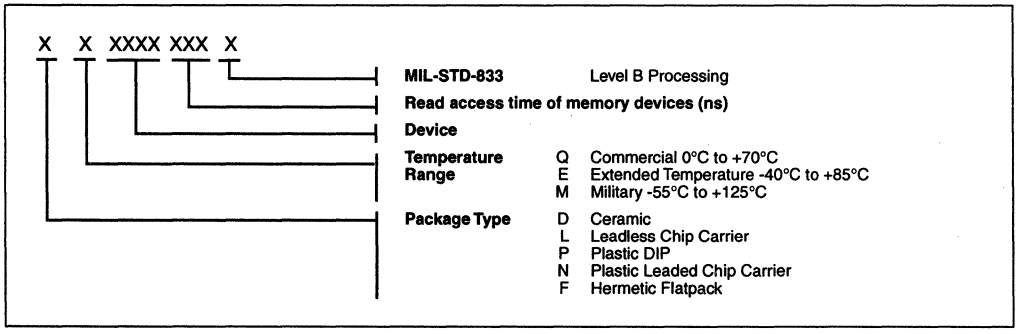


FIGURE 13: SIEMENS – NOT AVAILABLE

FIGURE 14: SGS-THOMSON

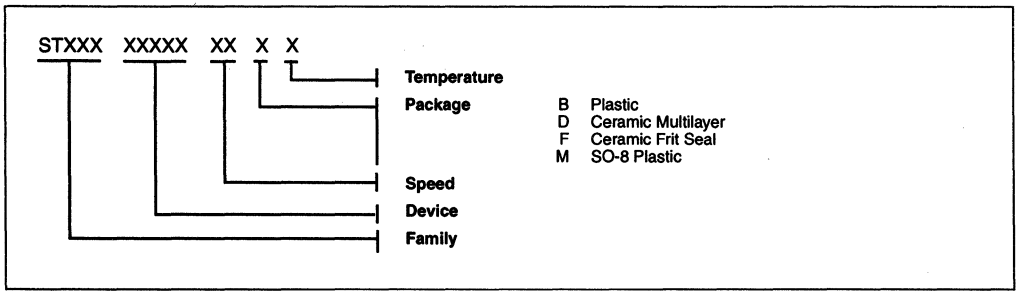
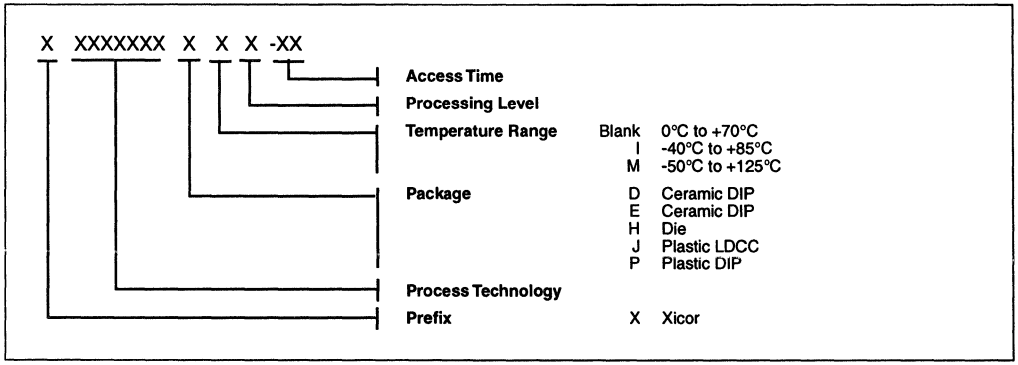


FIGURE 15: XICOR



NOTES:

PARALLEL EEPROMS

Parallel EEPROM Selection Guide

CMOS PARALLEL EEPROMS

Device	Density/ Organization	Access Time (ns)	Icc (Active/ Standby)	Byte Write Time	Endurance (cycles) *	Temp Range	# Pins	Package Types	Operating Voltage
28C04A	4K bits (512 x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	24,32	P,L	4.5V - 5.5V
28C16A	16K bits (2K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	24,28,32	P,L,TS,VS	4.5V - 5.5V
28C17A	16K bits (2K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	28,32	P,L,SO,TS,VS	4.5V - 5.5V
28C64A	64K bits (8K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	28,32	P,L,SO,TS,VS	4.5V - 5.5V
28C64AX	64K bits (8K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	28,32	P,L,SO,TS,VS	4.5V - 5.5V
28C04AF	4K bits (512 x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C,I	24,32	P,L	4.5V - 5.5V
28C16AF	16K bits (2K x 8)	150/200/250	30 mA/100 uA	200 µs	10K	C,I	24,28,32	P,L,TS,VS	4.5V - 5.5V
28C17AF	16K bits (2K x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C,I	28,32	P,L,SO,TS,VS	4.5V - 5.5V
28C64AF	64K bits (8K x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C,I	28,32	P,L,SO,TS,VS	4.5V - 5.5V

PACKAGES

L = Plastic Leaded Chip Carrier
P = Plastic Dual In-Line Package
S = Die in Waffle Pack
W = Die in Wafer Form

SL = 14-Lead Small Outline—150 mil
SM = 8-Lead Small Outline—208 mil
SN = 8-Lead SSmall Outline—150 mil
SO = Small Outline—300 mil

TS = Thin Small Outline—8mm x 20mm
VS = Very Samall Outline—8mm x 13.4mm

* Endurance is guaranteed to 10K cycles at extended (-40°C to +125°C) temperature.

Note: Not All Combinations Of Speed/Temperature Range/Package/etc. are available. Consult Factory For Specific Part Information.

NOTES:

EPROM Selection Guide

CMOS PARALLEL EPROMS

Part Number	QTP Avail.	Size	Org.	Access Time (ns)	Supply Voltage	Package	Temp. Range	Standby Current
27C64	Yes	64K	8K x 8	120-250	+5V	L,P,SO	C,I	2mA/100 µA
27C128	Yes	128K	16K x 8	120-250	+5V	L,P,SO	C,I	2mA/100 µA
27C256	Yes	256K	32K x 8	90-200	+5V	L,P,SO,TS,VS	C,I,E	2mA/100 µA
27C512A	Yes	512K	64K x 8	90-150	+5V	L,P,SO,TS,VS	C,I,E	2mA/30 µA
27LV64	Yes	64K	8K x 8	200-300	+3V to +5V	L,P,SO	C,I	1mA/100 µA
27LV256	Yes	256K	32K x 8	200-300	+3V to +5V	L,P,SO,TS,VS	C,I	1mA/100 µA

CMOS SERIAL EPROM

Part Number	QTP Avail.	Size	Org.	Max. Clock Freq. (MHz)	Supply Voltage	Package	Temperature Range
37LV36	Yes	36K	1134x32	10	+3V to +5V	P, SN, L	C,I
37LV65	Yes	64K	2048x32	10	+3V to +5V	P, SN, L	C,I
37LV128	Yes	128K	4096x32	10	+3V to +5V	P, SN, L	C,I

PACKAGES

L = Plastic Leaded Chip Carrier
P = Plastic Dual In-Line Package
S = Die in Waffle Pack
W = Die in Wafer Form
SN = 8-Lead SSmall Outline—150 mil
SO = Small Outline—300 mil
TS = Thin Small Outline—8mm x 20mm
VS = Very Small Outline—8mm x 13.4mm

* Endurance is guaranteed to 10K cycles at extended (-40°C to +125°C) temperature.

Note: Not All Combinations Of Speed/Temperature Range/Package/etc. are available. Consult Factory For Specific Part Information.

NOTES:

EPROM Cross Reference Guide

INTRODUCTION

The purpose of this document is to provide a quick way to determine which EPROM parts are mechanical and electrical equivalents to Microchip devices. There is also a listing of manufacturer's part numbering schemes to assist in determining the specifications of a particular part. The cross reference section is broken down by manufacturer and lists all parts from that manufacturer, and the plug compatible Microchip part number.

The one exception to plug compatibility listed in this cross-reference concerns the 28 pin SOIC package. Microchip, along with other manufacturers, make this part in a .300" (JEDEC Standard) width. There are other manufacturers that produce this device in a .330" (EIAJ Standard) wide package. In many cases, the PCB can be laid out to accommodate both versions. The devices that are offered in the .330" package are listed in this reference with an asterisk.

Microchip provides a wide selection of EPROM devices, both from a density and a packaging standpoint. If you are interested in a part that is not listed in this book, please refer to the Microchip data book, or contact your local distributor or sales representative for assistance.

Legend:	
AMD®	= Advanced Micro Devices
Atmel®	= Atmel Corporation
Hitachi®	= Hitachi Corporation
Intel®	= Intel Corporation
National®	= National Semiconductor Corporation
SGS	= ST® SGS-Thomson
T.I.	= Texas Instruments
Toshiba®	= Toshiba Corporation

The information contained in this publication regarding competitor devices was obtained from the respective EPROM manufacturer's latest available published technical information and may be subject to updates.

1.0 CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

AMD Part Number	Description	Microchip Part Number	
Am27C64-120JC	OTP 64K EPROM,120NS	PLCC 32	**27C64-12/L**
Am27C64-120PC	OTP 64K EPROM,120NS	PDIP 28	**27C64-12/P**
Am27C64-150JC	OTP 64K EPROM,150NS	PLCC 32	**27C64-15/L**
Am27C64-150PC	OTP 64K EPROM,150NS	PDIP 28	**27C64-15/P**
Am27C64-200JC	OTP 64K EPROM,200NS	PLCC 32	**27C64-20/L**
Am27C64-200PC	OTP 64K EPROM,200NS	PDIP 28	**27C64-20/P**
Am27C64-250JC	OTP 64K EPROM,250NS	PLCC 32	**27C64-25/L**
Am27C64-250PC	OTP 64K EPROM,250NS	PDIP 28	**27C64-25/P**
Am27C64-150JI	OTP 64K EPROM,150NS,IND	PLCC 32	**27C64-15I/L**
Am27C64-150PI	OTP 64K EPROM,150NS,IND	PDIP 28	**27C64-15I/P**
Am27C64-200JI	OTP 64K EPROM,200NS,IND	PLCC 32	**27C64-20I/L**
Am27C64-200PI	OTP 64K EPROM,200NS,IND	PDIP 28	**27C64-20I/P**
Am27C64-250JI	OTP 64K EPROM,250NS,IND	PLCC 32	**27C64-25I/L**
Am27C64-250PI	OTP 64K EPROM,250NS,IND	PDIP 28	**27C64-25I/P**
Am27C128-120JC	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
Am27C128-120PC	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
Am27C128-150JC	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
Am27C128-150PC	OTP 128K EPROM,150NS	PDIP 28	**27C128-15/P**
Am27C128-200JC	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
Am27C128-200PC	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
Am27C128-250JC	OTP 128K EPROM,250NS	PLCC 32	**27C128-25/L**
Am27C128-250PC	OTP 128K EPROM,250NS	PDIP 28	**27C128-25/P**
Am27C128-150JI	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
Am27C128-150PI	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
Am27C128-200JI	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
Am27C128-200PI	OTP 128K EPROM,200NS,IND	PDIP 28	**27C128-20I/P**
Am27C128-250JI	OTP 128K EPROM,250NS,IND	PLCC 32	**27C128-25I/L**
Am27C128-250PI	OTP 128K EPROM,250NS,IND	PDIP 28	**27C128-25I/P**
Am27C256-90LC	OTP 256K EPROM,90NS	PLCC 32	**27C256-90/L**
Am27C256-90JC	OTP 256K EPROM,90NS	PDIP 28	**27C256-90/P**
Am27C256-90PC	OTP 256K EPROM,90NS	SOIC 28	**27C256-90/SO**
Am27C256-100JC	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
Am27C256-100PC	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**

AMD Part Number	Description	Microchip Part Number	
Am27C256-120JC	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
Am27C256-120PC	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
Am27C256-150JC	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
Am27C256-150PC	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
Am27C256-200JC	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
Am27C256-200PC	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
Am27C256-100JI	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
Am27C256-100PI	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
Am27C256-120JI	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
Am27C256-120PI	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
Am27C256-150JI	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
Am27C256-150PI	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
Am27C256-200JI	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
Am27C256-200PI	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
Am27C512-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
Am27C512-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
Am27C512-120JC	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
Am27C512-120PC	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
Am27C512-150JC	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
Am27C512-150PC	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
Am27C512-200JC	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
Am27C512-200PC	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**
Am27C512-120JI	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512A-12I/L**
Am27C512-120PI	OTP 512K EPROM,120NS,IND	PDIP 28	**27C512A-12I/P**
Am27C512-150JI	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512A-15I/L**
Am27C512-150PI	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512A-15I/P**
Am27C512-200JI	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512A-20I/L**
Am27C512-200PI	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512A-20I/P**
Am27C512-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
Am27C512-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
Am27C512-120JC	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
Am27C512-120PC	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
Am27C512-150JC	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
Am27C512-150PC	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
Am27C512-200JC	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**

AMD Part Number	Description	Microchip Part Number	
Am27C512-200PC	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**

Atmel Part Number	Description	Microchip Part Number	
AT27C256R-90JC	OTP 256K EPROM,90NS	PLCC 32	**27C256-90/L**
AT27C256R-90PC	OTP 256K EPROM,90NS	PDIP 28	**27C256-90/P**
AT27C256R-90RC*	OTP 256K EPROM,90NS	SOIC 28	**27C256-90/SO**
AT27C256R-90TC	OTP 256K EPROM,90NS	VSOP 28	**27C256-90/VS**
AT27C256R-12JC	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
AT27C256R-12PC	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
AT27C256R-12RC*	OTP 256K EPROM,120NS	SOIC 28	**27C256-12/SO**
AT27C256R-12TC	OTP 256K EPROM,120NS	VSOP 28	**27C256-12/VS**
AT27C256R-15JC	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
AT27C256R-15PC	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
AT27C256R-15RC*	OTP 256K EPROM,150NS	SOIC 28	**27C256-15/SO**
AT27C256R-15TC	OTP 256K EPROM,150NS	VSOP 28	**27C256-15/VS**
AT27C256R-20JC	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
AT27C256R-20PC	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
AT27C256R-20RC*	OTP 256K EPROM,200NS	SOIC 28	**27C256-20/SO**
AT27C256R-20TC	OTP 256K EPROM,200NS	VSOP 28	**27C256-20/VS**
AT27C256R-12JI	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
AT27C256R-12PI	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
AT27C256R-12RI*	OTP 256K EPROM,120NS,IND	SOIC 28	**27C256-12I/SO**
AT27C256R-15JI	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
AT27C256R-15PI	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
AT27C256R-15RI*	OTP 256K EPROM,150NS,IND	SOIC 28	**27C256-15I/SO**
AT27C256R-20JI	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
AT27C256R-20PI	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
AT27C256R-20RI*	OTP 256K EPROM,200NS,IND	SOIC 28	**27C256-20I/SO**
AT27C512R-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
AT27C512R-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
AT27C512R-90RC*	OTP 512K EPROM,90NS	SOIC 28	**27C512A-90/SO**
AT27C512R-90TC	OTP 512K EPROM,90NS	VSOP 28	**27C512A-90/VS**
AT27C512R-12JC	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
AT27C512R-12PC	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
AT27C512R-12RC*	OTP 512K EPROM,120NS	SOIC 28	**27C512A-12/SO**

Atmel Part Number	Description	Microchip Part Number	
AT27C512R-12TC	OTP 512K EPROM,120NS	VSOP 28	**27C512A-12/VS**
AT27C512R-15JC	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
AT27C512R-15PC	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
AT27C512R-15RC*	OTP 512K EPROM,150NS	SOIC 28	**27C512A-15/SO**
AT27C512R-15TC	OTP 512K EPROM,150NS	VSOP 28	**27C512A-15/VS**
AT27C512R-20JC	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
AT27C512R-20PC	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**
AT27C512R-20RC*	OTP 512K EPROM,200NS	SOIC 28	**27C512A-20/SO**
AT27LV256R-20JC	OTP 256K EPROM,3V,200NS	PLCC 32	**27LV256-20/L**
AT27LV256R-20PC	OTP 256K EPROM,3V,200NS	PDIP 28	**27LV256-20/P**
AT27LV256R-20RC*	OTP 256K EPROM,3V,200NS	SOIC 28	**27LV256-20/SO**
AT27LV256R-20TC	OTP 256K EPROM,3V,200NS	VSOP 28	**27LV256-20/VS**
AT27LV256R-25JC	OTP 256K EPROM,3V,250NS	PLCC 32	**27LV256-25/L**
AT27LV256R-25PC	OTP 256K EPROM,3V,250NS	PDIP 28	**27LV256-25/P**
AT27LV256R-25RC*	OTP 256K EPROM,3V,250NS	SOIC 28	**27LV256-25/SO**
AT27LV256R-25TC	OTP 256K EPROM,3V,250NS	VSOP 28	**27LV256-25/VS**

Hitachi Part Number	Description	Microchip Part Number	
HN27C256HP-10	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
HN27C256FP-10T*	OTP 256K EPROM,100NS	SOIC 28	**27C256-10/SO**
HN27C256FP-25T/-30T*	OTP 256K EPROM,200NS	SOIC 28	**27C256-20/SO**
HN27512G-25/-30	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
HN27512P-25/-30	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**

National Part Number	Description	Microchip Part Number	
NM27C64N150	OTP 64K EPROM,150NS	PDIP 28	**27C64-15/P**
NM27C64N200	OTP 64K EPROM,200NS	PDIP 28	**27C64-20/P**
NM27C64NE150	OTP 64K EPROM,150NS,IND	PDIP 28	**27C64-15I/P**
NM27C128N150	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
NM27C128N200	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
NM27C128NE150	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
NM27C256V100	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
NM27C256N100	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
NM27C256V120	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
NM27C256N120	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
NM27C256V150	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**

National Part Number	Description	Microchip Part Number	
NM27C256N150	OTP 256K EPROM,150NS	PDIP 28	27C256-15/P
NM27C256V200	OTP 256K EPROM,200NS	PLCC 32	27C256-20/L
NM27C256N200	OTP 256K EPROM,200NS	PDIP 28	27C256-20/P
NM27C256VE100	OTP 256K EPROM,100NS,IND	PLCC 32	27C256-10I/L
NM27C256NE100	OTP 256K EPROM,100NS,IND	PDIP 28	27C256-10I/P
NM27C256VE120	OTP 256K EPROM,120NS,IND	PLCC 32	27C256-12I/L
NM27C256NE120	OTP 256K EPROM,120NS,IND	PDIP 28	27C256-12I/P
NM27C256VE150	OTP 256K EPROM,150NS,IND	PLCC 32	27C256-15I/L
NM27C256NE150	OTP 256K EPROM,150NS,IND	PDIP 28	27C256-15I/P
NM27C256VE200	OTP 256K EPROM,200NS,IND	PLCC 32	27C256-20I/L
NM27C256NE200	OTP 256K EPROM,200NS,IND	PDIP 28	27C256-20I/P
NM27C512V120	OTP 512K EPROM,120NS	PLCC 32	27C512-12/L
NM27C512N120	OTP 512K EPROM,120NS	PDIP 28	27C512-12/P
NM27C512V150	OTP 512K EPROM,150NS	PLCC 32	27C512-15/L
NM27C512N150	OTP 512K EPROM,150NS	PDIP 28	27C512-15/P
NM27C512V200	OTP 512K EPROM,200NS	PLCC 32	27C512-20/L
NM27C512N200	OTP 512K EPROM,200NS	PDIP 28	27C512-20/P
NM27C512VE120	OTP 512K EPROM,120NS,IND	PLCC 32	27C512-12I/L
NM27C512NE120	OTP 512K EPROM,120NS,IND	PDIP 28	27C512-12I/P
NM27C512VE150	OTP 512K EPROM,150NS,IND	PLCC 32	27C512-15I/L
NM27C512NE150	OTP 512K EPROM,150NS,IND	PDIP 28	27C512-15I/P
NM27C512VE200	OTP 512K EPROM,200NS,IND	PLCC 32	27C512-20I/L
NM27C512NE200	OTP 512K EPROM,200NS,IND	PDIP 28	27C512-20I/P
NM27C512V120	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
NM27C512N120	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
NM27C512V150	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
NM27C512N150	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P
NM27C512V200	OTP 512K EPROM,200NS	PLCC 32	27C512A-20/L
NM27C512N200	OTP 512K EPROM,200NS	PDIP 28	27C512A-20/P

SGS Part Number	Description	Microchip Part Number	
M27C64A-15C1	OTP 64K EPROM,150NS	PLCC 32	27C64-15/L
M27C64A-15C1TR	OTP 64K EPROM,150NS	PLCC 32	27C64T-15/L
M27C64A-20C1	OTP 64K EPROM,200NS	PLCC 32	27C64-20/L
M27C64A-20C1TR	OTP 64K EPROM,200NS	PLCC 32	27C64T-20/L
M27C64A-25C1	OTP 64K EPROM,250NS	PLCC 32	27C64-25/L

SGS Part Number	Description	Microchip Part Number	
M27C64A-25C1TR	OTP 64K EPROM,250NS	PLCC 32	27C64T-25/L
M27C64A-15C6	OTP 64K EPROM,150NS,IND	PLCC 32	27C64-15I/L
M27C64A-15C6TR	OTP 64K EPROM,150NS,IND	PLCC 32	27C64T-15I/L
M27C64A-20C6	OTP 64K EPROM,200NS,IND	PLCC 32	27C64-20I/L
M27C64A-20C6TR	OTP 64K EPROM,200NS,IND	PLCC 32	27C64T-20I/L
M27C64A-25C6	OTP 64K EPROM,250NS,IND	PLCC 32	27C64-25I/L
M27C64A-25C6TR	OTP 64K EPROM,250NS,IND	PLCC 32	27C64T-25I/L
M27C128A-12C1	OTP 128K EPROM,120NS	PLCC 32	27C128-12/L
M27C128A-15C1	OTP 128K EPROM,150NS	PLCC 32	27C128-15/L
M27C128A-20C1	OTP 128K EPROM,200NS	PLCC 32	27C128-20/L
M27C128A-15C6	OTP 128K EPROM,150NS,IND	PLCC 32	27C128-15I/L
M27C128A-20C6	OTP 128K EPROM,200NS,IND	PLCC 32	27C128-20I/L
M27C256B-90C1	OTP 256K EPROM,90NS	PLCC 32	27C256-90/L
M27C256B-90B1	OTP 256K EPROM,90NS	PDIP 28	27C256-90/P
M27C256B-90C1	OTP 256K EPROM,90NS	PLCC 32	27C256T-90/L
M27C256B-10C1	OTP 256K EPROM,100NS	PLCC 32	27C256-10/L
M27C256B-10B1	OTP 256K EPROM,100NS	PDIP 28	27C256-10/P
M27C256B-10N1	OTP 256K EPROM,100NS	VSOP 28	27C256-10/VS
M27C256B-10C1	OTP 256K EPROM,100NS	PLCC 32	27C256T-10/L
M27C256B-12C1	OTP 256K EPROM,120NS	PLCC 32	27C256-12/L
M27C256B-12B1	OTP 256K EPROM,120NS	PDIP 28	27C256-12/P
M27C256B-12M1*	OTP 256K EPROM,120NS	SOIC 28	27C256-12/SO
M27C256B-12N1	OTP 256K EPROM,120NS	VSOP 28	27C256-12/VS
M27C256B-12C1	OTP 256K EPROM,120NS	PLCC 32	27C256T-12/L
M27C256B-15C1	OTP 256K EPROM,150NS	PLCC 32	27C256-15/L
M27C256B-15B1	OTP 256K EPROM,150NS	PDIP 28	27C256-15/P
M27C256B-15M1*	OTP 256K EPROM,150NS	SOIC 28	27C256-15/SO
M27C256B-15N1	OTP 256K EPROM,150NS	VSOP 28	27C256-15/VS
M27C256B-15C1	OTP 256K EPROM,150NS	PLCC 32	27C256T-15/L
M27C256B-20C1	OTP 256K EPROM,200NS	PLCC 32	27C256-20/L
M27C256B-20B1	OTP 256K EPROM,200NS	PDIP 28	27C256-20/P
M27C256B-20M1*	OTP 256K EPROM,200NS	SOIC 28	27C256-20/SO
M27C256B-20C1	OTP 256K EPROM,200NS	PLCC 32	27C256T-20/L
M27C256B-10C6	OTP 256K EPROM,100NS,IND	PLCC 32	27C256-10I/L
M27C256B-10B6	OTP 256K EPROM,100NS,IND	PDIP 28	27C256-10I/P
M27C256B-10C6	OTP 256K EPROM,100NS,IND	PLCC 32	27C256T-10I/L
M27C256B-12C6	OTP 256K EPROM,120NS,IND	PLCC 32	27C256-12I/L
M27C256B-12B6	OTP 256K EPROM,120NS,IND	PDIP 28	27C256-12I/P
M27C256B-12C6	OTP 256K EPROM,120NS,IND	PLCC 32	27C256T-12I/L
M27C256B-15C6	OTP 256K EPROM,150NS,IND	PLCC 32	27C256-15I/L

SGS Part Number	Description	Microchip Part Number	
M27C256B-15B6	OTP 256K EPROM,150NS,IND	PDIP 28	27C256-15I/P
M27C256B-15C6	OTP 256K EPROM,150NS,IND	PLCC 32	27C256T-15I/L
M27C256B-20C6	OTP 256K EPROM,200NS,IND	PLCC 32	27C256-20I/L
M27C256B-20B6	OTP 256K EPROM,200NS,IND	PDIP 28	27C256-20I/P
M27C256B-20C6	OTP 256K EPROM,200NS,IND	PLCC 32	27C256T-20I/L
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512-90/L
M27C512-90B1	OTP 512K EPROM,90NS	PDIP 28	27C512-90/P
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512T-90/L
M27C512-10C1	OTP 512K EPROM,100NS	PLCC 32	27C512-10/L
M27C512-10B1	OTP 512K EPROM,100NS	PDIP 28	27C512-10/P
M27C512-10C1	OTP 512K EPROM,100NS	PLCC 32	27C512T-10/L
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
M27C512-12B1	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512AT-12/L
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
M27C512-15B1	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	27C512AT-15/L
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	27C512A-20/L
M27C512-20B1	OTP 512K EPROM,200NS	PDIP 28	27C512A-20/P
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	27C512AT-20/L
M27C512-10C6	OTP 512K EPROM,100NS,IND	PLCC 32	27C512A-10I/L
M27C512-10B6	OTP 512K EPROM,100NS,IND	PDIP 28	27C512A-10I/P
M27C512-10C6	OTP 512K EPROM,100NS,IND	PLCC 32	27C512AT-10I/L
M27C512-12C6	OTP 512K EPROM,120NS,IND	PLCC 32	27C512A-12I/L
M27C512-12B6	OTP 512K EPROM,120NS,IND	PDIP 28	27C512A-12I/P
M27C512-12C6	OTP 512K EPROM,120NS,IND	PLCC 32	27C512AT-12I/L
M27C512-15C6	OTP 512K EPROM,150NS,IND	PLCC 32	27C512A-15I/L
M27C512-15B6	OTP 512K EPROM,150NS,IND	PDIP 28	27C512A-15I/P
M27C512-15C6	OTP 512K EPROM,150NS,IND	PLCC 32	27C512AT-15I/L
M27C512-20C6	OTP 512K EPROM,200NS,IND	PLCC 32	27C512A-20I/L
M27C512-20B6	OTP 512K EPROM,200NS,IND	PDIP 28	27C512A-20I/P
M27C512-20C6	OTP 512K EPROM,200NS,IND	PLCC 32	27C512AT-20I/L
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512A-90/L
M27C512-90B1	OTP 512K EPROM,90NS	PDIP 28	27C512A-90/P
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	27C512AT-90/L
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
M27C512-12B1	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	27C512AT-12/L
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
M27C512-15B1	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P

SGS Part Number	Description	Microchip Part Number	
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	**27C512AT-15/L**
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
M27C512-20B1	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	**27C512AT-20/L**
N27C256-120V10Q	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
P27C256-120V10Q	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
N27C256-150V10Q	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
P27C256-150V10Q	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
N27C256-200V10Q	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
P27C256-200V10Q	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
N27C256-120V10T	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
P27C256-120V10T	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
N27C256-150V10T	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
P27C256-150V10T	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
N27C256-200V10T	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
P27C256-200V10T	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**

TI Part Number	Description	Microchip Part Number	
TMS27PC128-12FML	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
TMS27PC128-12NL	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
TMS27PC128-15FML	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
TMS27PC128-15NL	OTP 128K EPROM,150NS	PDIP 28	**27C128-15/P**
TMS27PC128-20FML	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
TMS27PC128-20NL	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
TMS27PC128-25FML	OTP 128K EPROM,250NS	PLCC 32	**27C128-25/L**
TMS27PC128-25NL	OTP 128K EPROM,250NS	PDIP 28	**27C128-25/P**
TMS27PC128-15FME	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
TMS27PC128-15NE	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
TMS27PC128-20FME	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
TMS27PC128-20NE	OTP 128K EPROM,200NS,IND	PDIP 28	**27C128-20I/P**
TMS27PC128-25FME	OTP 128K EPROM,250NS,IND	PLCC 32	**27C128-25I/L**
TMS27PC128-25NE	OTP 128K EPROM,250NS,IND	PDIP 28	**27C128-25I/P**
TMS27PC256-10FML	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
TMS27PC256-10NL	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
TMS27PC256-12FML	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
TMS27PC256-12NL	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
TMS27PC256-15FML	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**

TI Part Number	Description	Microchip Part Number	
TMS27PC256-15NL	OTP 256K EPROM,150NS	PDIP 28	27C256-15/P
TMS27PC256-20FML	OTP 256K EPROM,200NS	PLCC 32	27C256-20/L
TMS27PC256-20NL	OTP 256K EPROM,200NS	PDIP 28	27C256-20/P
TMS27PC256-10FME	OTP 256K EPROM,100NS,IND	PLCC 32	27C256-10I/L
TMS27PC256-10NE	OTP 256K EPROM,100NS,IND	PDIP 28	27C256-10I/P
TMS27PC256-12FME	OTP 256K EPROM,120NS,IND	PLCC 32	27C256-12I/L
TMS27PC256-12NE	OTP 256K EPROM,120NS,IND	PDIP 28	27C256-12I/P
TMS27PC256-15FME	OTP 256K EPROM,150NS,IND	PLCC 32	27C256-15I/L
TMS27PC256-15NE	OTP 256K EPROM,150NS,IND	PDIP 28	27C256-15I/P
TMS27PC256-20FME	OTP 256K EPROM,200NS,IND	PLCC 32	27C256-20I/L
TMS27PC256-20NE	OTP 256K EPROM,200NS,IND	PDIP 28	27C256-20I/P
TMS27PC512-10FML	OTP 512K EPROM,100NS	PLCC 32	27C512A-10/L
TMS27PC512-10NL	OTP 512K EPROM,100NS	PDIP 28	27C512A-10/P
TMS27PC512-12FML	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
TMS27PC512-12NL	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
TMS27PC512-15FML	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
TMS27PC512-15NL	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P
TMS27PC512-20FML	OTP 512K EPROM,200NS	PLCC 32	27C512A-20/L
TMS27PC512-20NL	OTP 512K EPROM,200NS	PDIP 28	27C512A-20/P
TMS27PC512-10FME	OTP 512K EPROM,100NS,IND	PLCC 32	27C512A-10I/L
TMS27PC512-10NE	OTP 512K EPROM,100NS,IND	PDIP 28	27C512A-10I/P
TMS27PC512-12FME	OTP 512K EPROM,120NS,IND	PLCC 32	27C512A-12I/L
TMS27PC512-12NE	OTP 512K EPROM,120NS,IND	PDIP 28	27C512A-12I/P
TMS27PC512-15FME	OTP 512K EPROM,150NS,IND	PLCC 32	27C512A-15I/L
TMS27PC512-15NE	OTP 512K EPROM,150NS,IND	PDIP 28	27C512A-15I/P
TMS27PC512-20FME	OTP 512K EPROM,200NS,IND	PLCC 32	27C512A-20I/L
TMS27PC512-20NE	OTP 512K EPROM,200NS,IND	PDIP 28	27C512A-20I/P
TMS27PC512-10FML	OTP 512K EPROM,90NS	PLCC 32	27C512A-90/L
TMS27PC512-10NL	OTP 512K EPROM,90NS	PDIP 28	27C512A-90/P
TMS27PC512-12FML	OTP 512K EPROM,120NS	PLCC 32	27C512A-12/L
TMS27PC512-12NL	OTP 512K EPROM,120NS	PDIP 28	27C512A-12/P
TMS27PC512-15FML	OTP 512K EPROM,150NS	PLCC 32	27C512A-15/L
TMS27PC512-15NL	OTP 512K EPROM,150NS	PDIP 28	27C512A-15/P
TMS27PC512-20FML	OTP 512K EPROM,200NS	PLCC 32	27C512A-20/L
TMS27PC512-20NL	OTP 512K EPROM,200NS	PDIP 28	27C512A-20/P

Toshiba Part Number	Description	Microchip Part Number	
TC54256AP-15	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
TC54256AF-20*	OTP 256K EPROM,150NS,IND	SOIC 28	**27C256-15I/SO**
TC54512AP-15	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
TC54512AF-15*	OTP 512K EPROM,150NS	SOIC 28	**27C512-15/SO**
TC54512AP-20	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
TC54512AF-20*	OTP 512K EPROM,200NS	SOIC 28	**27C512-20/SO**
TC54512AP-17	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
TC54512AP-20	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**

FIGURE 1: ADVANCED MICRO DEVICES

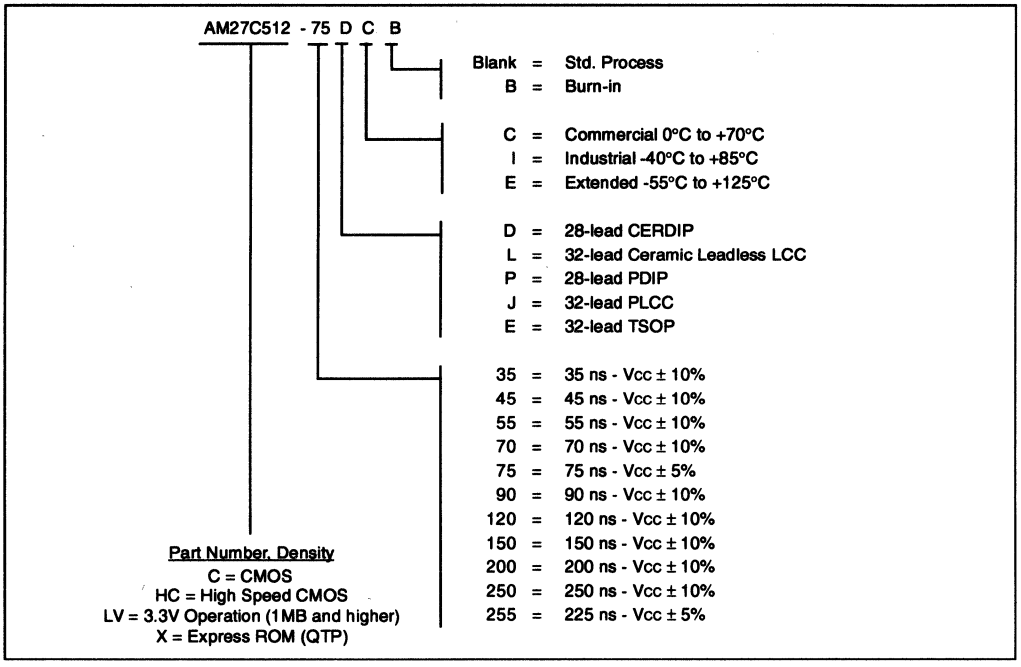


FIGURE 2: ATMEL CORPORATION

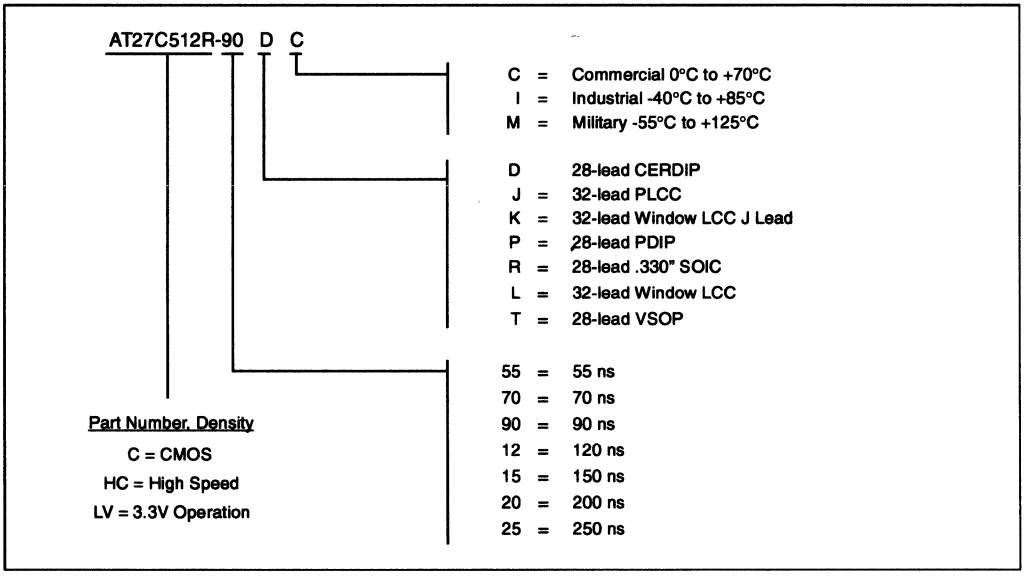


FIGURE 3: HITACHI CORPORATION

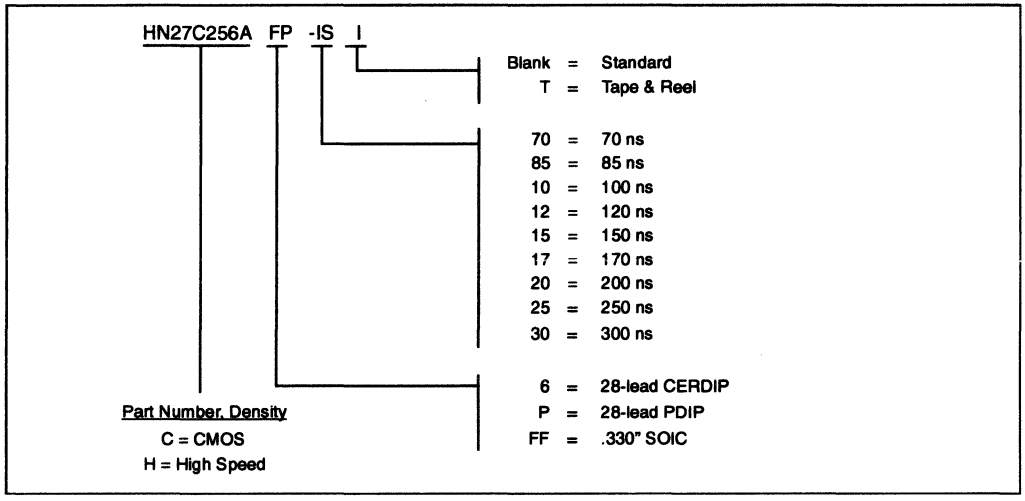


FIGURE 4: INTEL CORPORATION

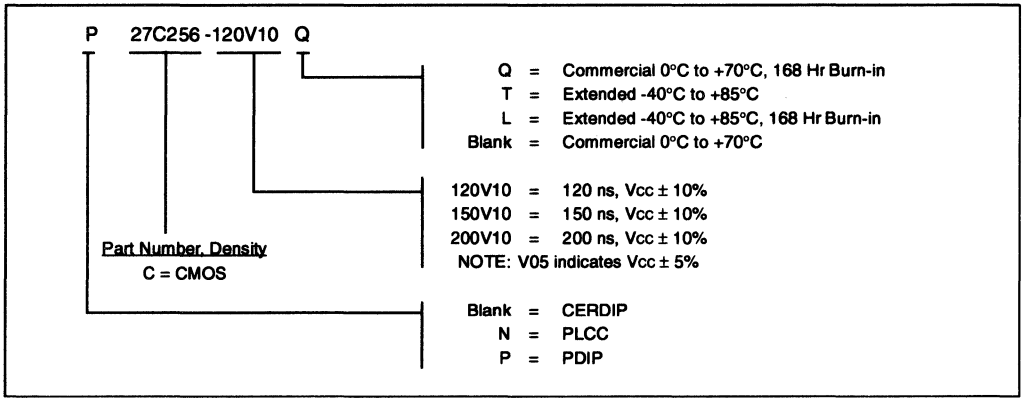


FIGURE 5: MICROCHIP TECHNOLOGY INCORPORATED

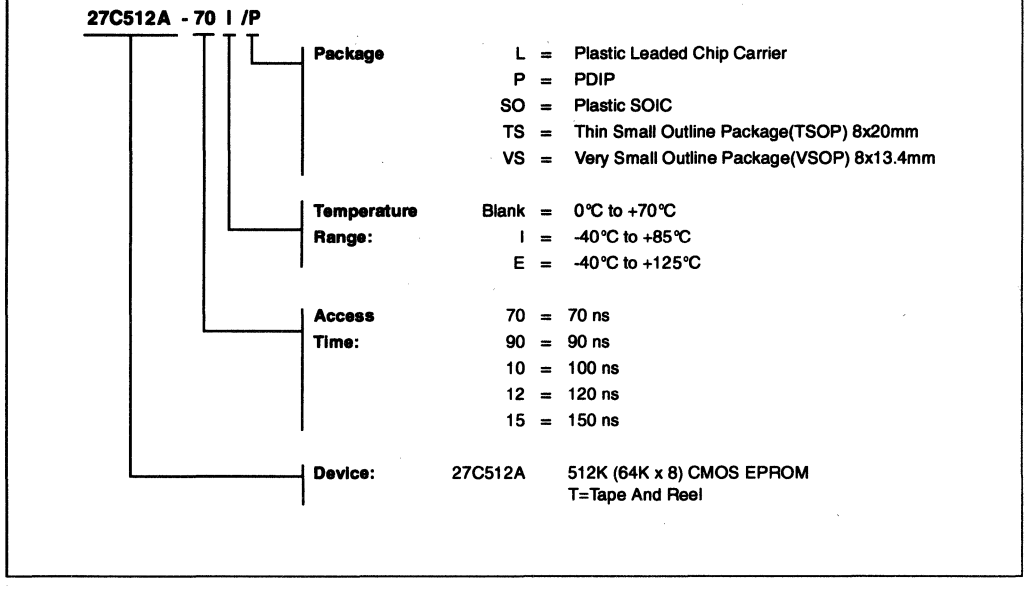


FIGURE 6: NATIONAL SEMICONDUCTOR CORPORATION

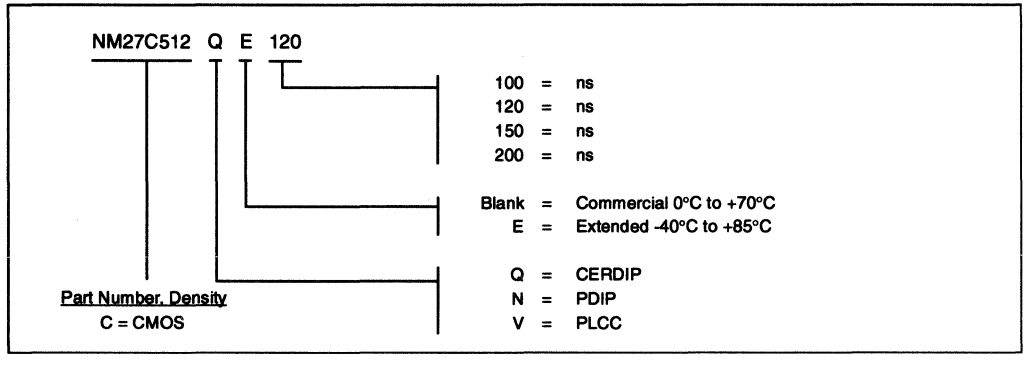


FIGURE 7: SGS-THOMSON

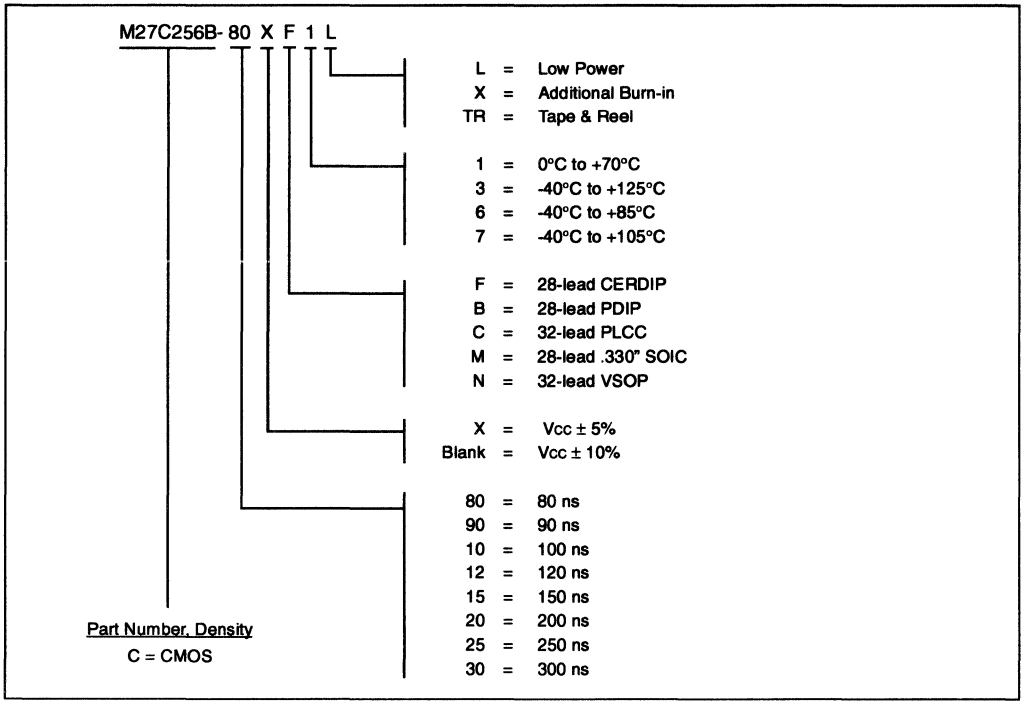


FIGURE 8: TEXAS INSTRUMENTS

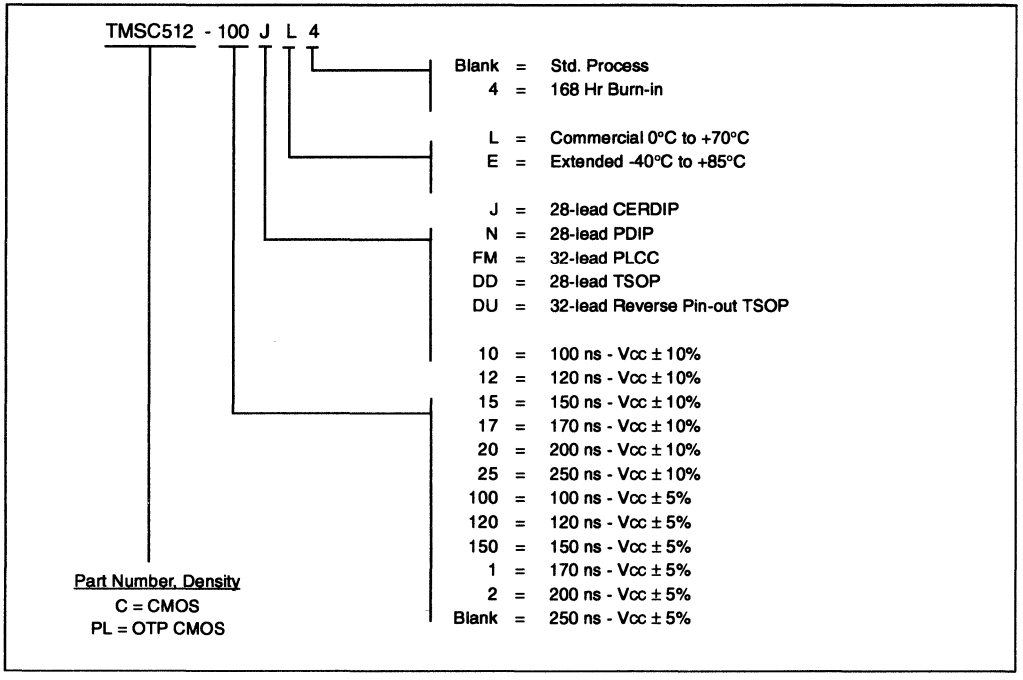
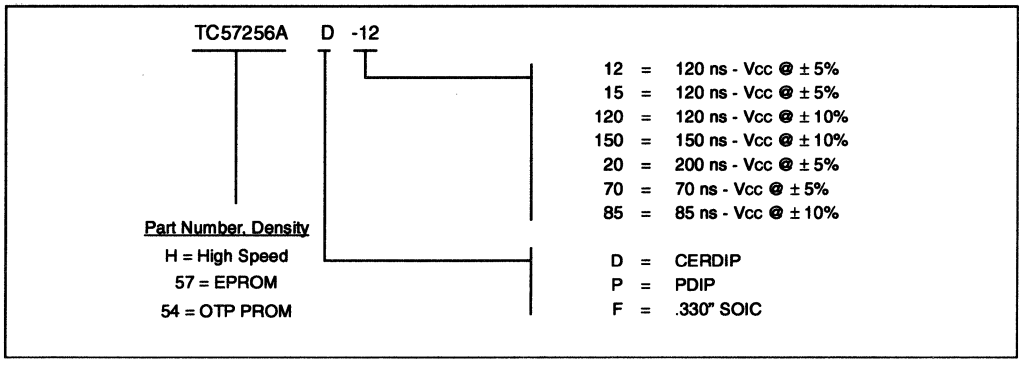


FIGURE 9: TOSHIBA CORPORATION



MICROCHIP

SECTION 3
I²C™ SERIAL EEPROM PRODUCT SPECIFICATIONS

24AA00	128 Bit 1.8V I²C™ Bus Serial EEPROM	3-1
24LC00	128 Bit 2.5V I²C™ Bus Serial EEPROM	3-1
24C00	128 Bit 5V I²C™ Bus Serial EEPROM	3-1
24C01C	1K 5.0V I²C™ Serial EEPROM	3-11
24AA01	1K 1.8V I²C™ Serial EEPROM	3-21
24LC01B	1K 2.5V I²C™ Serial EEPROM	3-29
24C01SC	1K 5.0V I²C™ Serial EEPROMs for Smart Cards	3-37
24LCS61	1K Software Addressable I²C™ Serial EEPROM	3-47
24AA02	1K 1.8V I²C™ Serial EEPROM	3-21
24LC02B	2K 2.5V I²C™ Serial EEPROM	3-29
24C02C	2K 5.0V I²C™ Serial EEPROM	3-61
24C02SC	2K 5.0V I²C™ Serial EEPROMs for Smart Cards	3-37
24LCS52	2K 2.5V I²C™ Serial EEPROM with Software Write Protect	3-71
24LC024	2K 2.5V I²C™ Serial EEPROM	3-81
24LC025	2K 2.5V I²C™ Serial EEPROM	3-81
24LCS62	2K Software Addressable I²C™ Serial EEPROM	3-47
24AA04	4K 1.8V I²C™ Serial EEPROM	3-91
24LC04B	4K 2.5V I²C™ Serial EEPROM	3-99
24C04A	4K 5.0V I²C™ Serial EEPROM	3-107
24AA08	8K 1.8V I²C™ Serial EEPROM	3-91
24LC008B	8K 2.5V I²C™ Serial EEPROM	3-99
24C08B	8K 5.0V I²C™ Serial EEPROM	3-117
24AA16	16K 1.8V I²C™ Serial EEPROM	3-125
24C16B	16K 5.0V I²C™ Serial EEPROM	3-117
24LC16B	16K 2.5V I²C™ Serial EEPROM	3-133
24AA164	16K 1.8V Cascadable I²C™ Serial EEPROM	3-141
24LC164	16K 2.5V Cascadable I²C™ Serial EEPROM	3-149
24AA174	16K 1.8V Cascadable I²C™ Serial EEPROM with OTP Security Page	3-157
24LC174	16K 2.5V Cascadable I²C™ Serial EEPROM with OTP Security Page	3-167
24AA32A	32K 1.8V I²C™ Serial EEPROM	3-177
24LC32A	32K 2.5V I²C™ Serial EEPROM	3-187
24C32A	32K 5.0V I²C™ Serial EEPROM	3-197
24AA32	32K 1.8V I²C™ Smart Serial™ EEPROM	3-207

I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

24LC32	32K 2.5V I²C™ Smart Serial™ EEPROM	3-219
24C32	32K 5.0V I²C™ Smart Serial EEPROM	3-231
24FC32	32K 5.0V 1 MHz I²C™ Smart Serial™ EEPROM	3-243
24AA64	64K 1.8V I²C™CMOS Serial EEPROM	3-255
24LC64	64K 2.5V I²C™CMOS Serial EEPROM	3-255
24AA65	64K 1.8V I²C™ Smart Serial™ EEPROM	3-265
24LC65	64K 2.5V I²C™ Smart Serial™ EEPROM	3-277
24C65	64K 5.0V I²C™ Smart Serial™ EEPROM	3-289
24FC65	64K 5.0V 1 MHz I²C™ Smart Serial™ EEPROM	3-301
24AA128	128K 1.8V I²C™CMOS Serial EEPROM	3-313
24LC128	128K 2.5V I²C™CMOS Serial EEPROM	3-313
24AA256	256K 1.8V I²C™CMOS Serial EEPROM	3-323
24LC256	256K 2.5V I²C™CMOS Serial EEPROM	3-323

24AA00/24LC00/24C00

128 Bit I²C™ Bus Serial EEPROM

DEVICE SELECTION TABLE

Device	Vcc Range	Temp Range
24AA00	1.8 - 6.0	C,I
24LC00	2.5 - 6.0	C,I
24C00	4.5 - 5.5	C,I,E

FEATURES

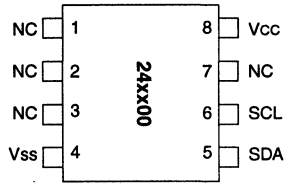
- Low power CMOS technology
  - 500 µA typical active current
  - 250 nA typical standby current
- Organized as 16 bytes x 8 bits
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- 4 ms maximum byte write cycle time
- 1,000,000 erase/write cycles guaranteed
- ESD protection > 4 kV
- Data retention > 200 years
- 8L DIP, SOIC, TSSOP and 5L SOT-23 packages
- Temperature ranges available:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

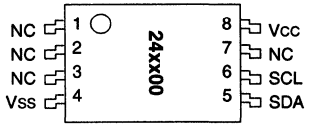
The Microchip Technology Inc. 24AA00/24LC00/24C00 (24xx00*) is a 128-bit Electrically Erasable PROM memory organized as 16 x 8 with a 2-wire serial interface. Low voltage design permits operation down to 1.8 volts for the 24xx00 version, and every version maintains a maximum standby current of only 1 µA and typical active current of only 500 µA. This device was designed for where a small amount of EEPROM is needed for the storage of calibration values, ID numbers or manufacturing information, etc. The 24xx00 is available in 8-pin PDIP, 8-pin SOIC (150 mil), 8-pin TSSOP and the 5-pin SOT-23 packages.

PACKAGE TYPES

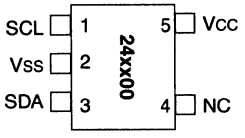
8-PIN PDIP/SOIC



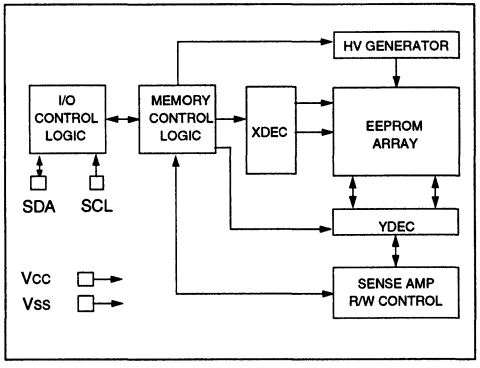
8-PIN TSSOP



5-PIN SOT-23



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.
*24xx00 is used in this document as a generic part number for the 24AA00/24LC00/24C00 devices.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds).....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
Vcc	+1.8V to 6.0V (24AA00) +2.5V to 6.0V (24LC00) +4.5V to 5.5V (24C00)
NC	No Internal Connection

TABLE 1-2 DC CHARACTERISTICS

All Parameters apply across the recommended operating ranges unless otherwise noted	Commercial (C): Tamb = 0°C to +70°C, Vcc = 1.8V to 6.0V Industrial (I): Tamb = -40°C to +85°C, Vcc = 1.8V to 6.0V Automotive (E) Tamb = -40°C to +125°C, Vcc = 4.5V to 5.5V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	0.7 Vcc		V	(Note)
Low level input voltage	VIL		0.3 Vcc	V	(Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	Vcc ≥ 2.5V (Note)
Low level output voltage	VOL		.40	V	IOL = 3.0 mA, Vcc = 4.5V IOL = 2.1 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = Vcc or Vss
Output leakage current	ILO	-10	10	µA	VOUT = Vcc or Vss
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note) Tamb = 25°C, f = 1 MHz
Operating current	ICC Write	—	2	mA	Vcc = 5.5V, SCL = 400 kHz
	ICC Read	—	1	mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	1	µA	Vcc = 5.5V, SDA = SCL = Vcc

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING DATA

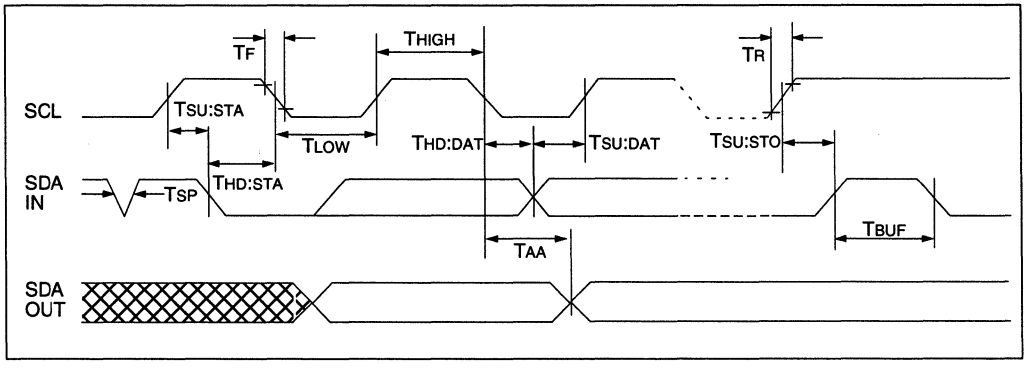


TABLE 1-3 AC CHARACTERISTICS

All Parameters apply across all recommended operating ranges unless otherwise noted	Commercial (C): Tamb = 0°C to +70°C, Vcc = 1.8V to 6.0V Industrial (I): Tamb = -40°C to +85°C, Vcc = 1.8V to 6.0V Automotive (E): Tamb = -40°C to +125°C, Vcc = 4.5V to 5.5V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
START condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
STOP condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 4.5V 4.5V ≤ Vcc ≤ 6.0V
Output fall time from VIH minimum to VIL maximum	TOF	20+0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1, 3)
Write cycle time	TWC	—	4	ms	
Endurance		1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's BBS or website.

2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 Noise Protection

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24xx00 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24xx00 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

0.1 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

4.3 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

4.4 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24xx00 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

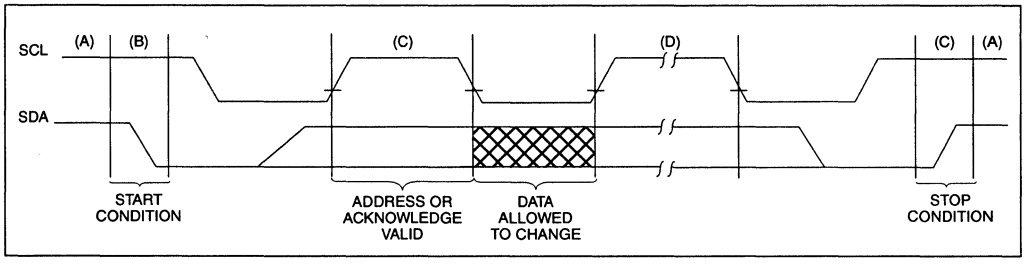
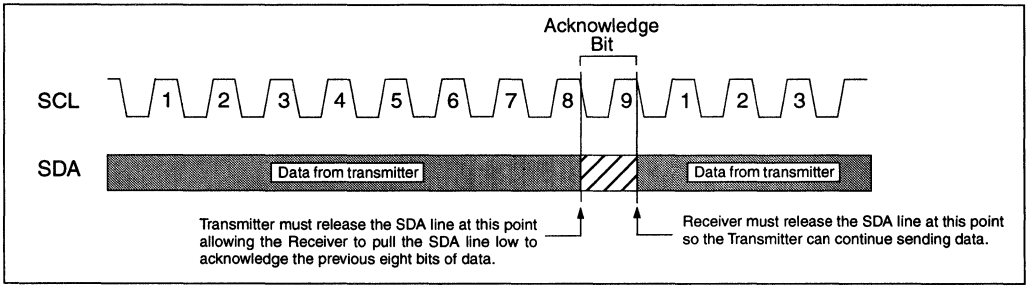


FIGURE 4-2: ACKNOWLEDGE TIMING

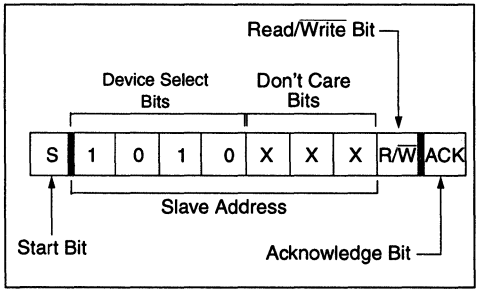


5.0 DEVICE ADDRESSING

After generating a START condition, the bus master transmits a control byte consisting of a slave address and a Read/$\overline{\text{Write}}$ bit that indicates what type of operation is to be performed. The slave address for the 24xx00 consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 5-1). The 24xx00 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 5-1: CONTROL BYTE FORMAT



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{\text{W}}$ bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24xx00. Only the lower four address bits are used by the device, and the upper four bits are don't cares. The 24xx00 will acknowledge the address byte and the master device will then transmit the data word to be written into the addressed memory location. The 24xx00 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24xx00 will not generate acknowledge signals (Figure 7-2). After a byte write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a full eight data bits have been transmitted, then the write command will abort and no data will be written. The 24xx00 employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5V (24AA00 and 24LC00) or 3.8V (24C00) at nominal conditions.

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW

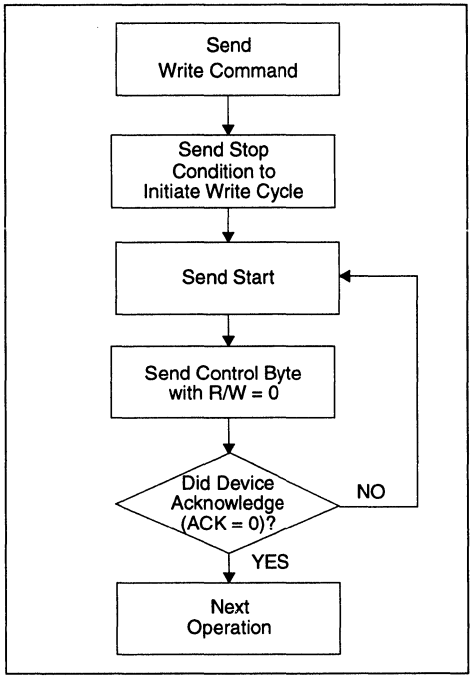
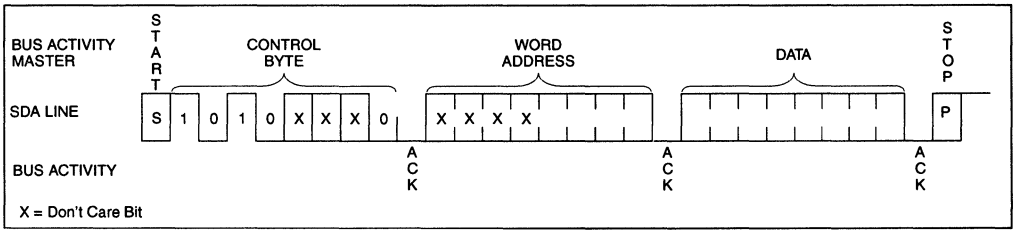


FIGURE 7-2: BYTE WRITE



3

I²C™

8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24xx00 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24xx00 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the device transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the device to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24xx00 contains an internal address pointer which is incremented by one at the completion of each read operation. This address pointer allows the entire memory contents to be serially read during one operation.

FIGURE 8-1: CURRENT ADDRESS READ

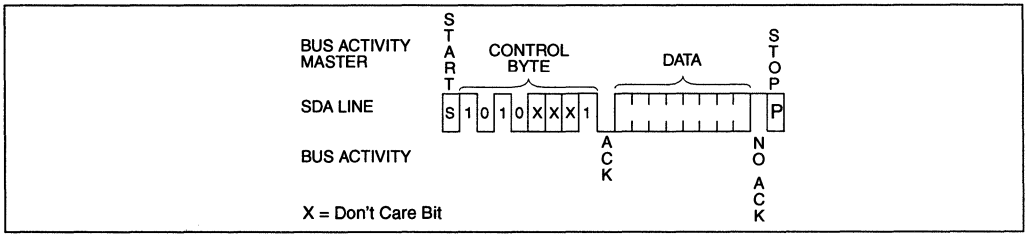


FIGURE 8-2: RANDOM READ

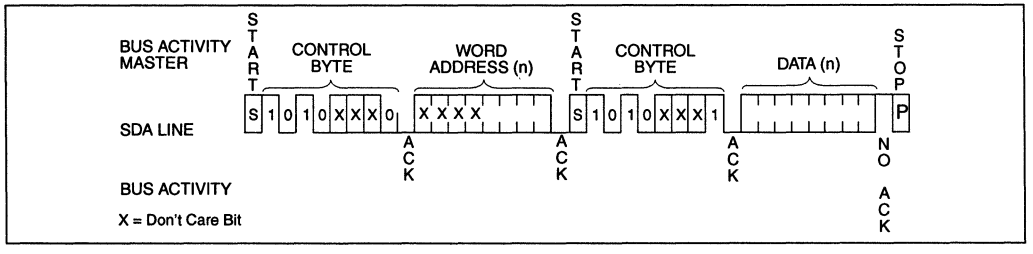
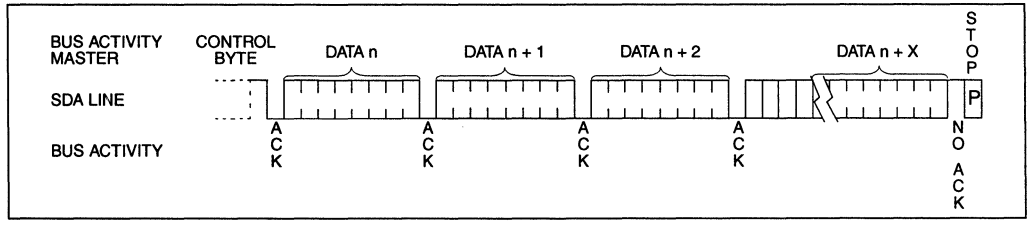


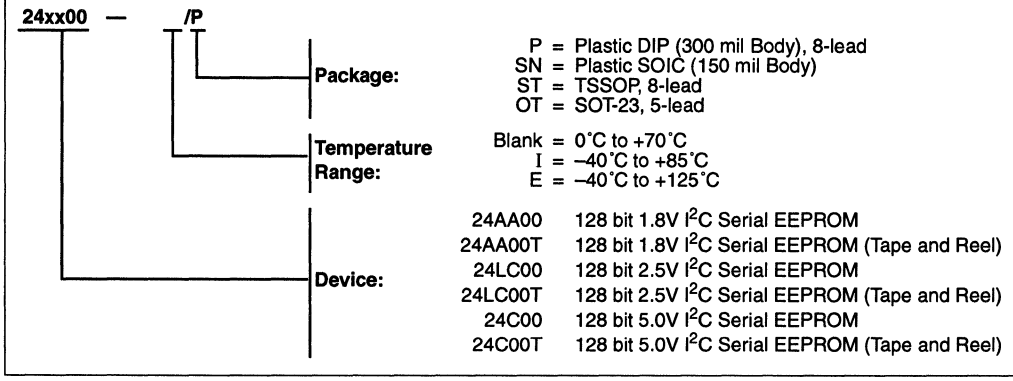
FIGURE 8-3: SEQUENTIAL READ



NOTES:

24XX00 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24C01C

1K 5.0V I²C™ Serial EEPROM

FEATURES

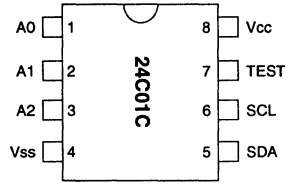
- Single supply with operation from 4.5 to 5.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as a single block of 128 bytes (128 x 8)
- 2-wire serial interface bus, I²C compatible
- 100 kHz and 400 kHz compatibility
- Page-write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- Fast 1 mS write cycle time for byte or page mode
- Address lines allow up to eight devices on bus
- 1,000,000 erase/write cycles guaranteed
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC or TSSOP packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

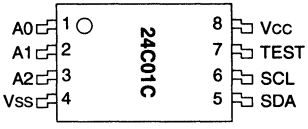
The Microchip Technology Inc. 24C01C is a 1K bit Serial Electrically Erasable PROM with a voltage range of 4.5V to 5.5V. The device is organized as a single block of 128 x 8-bit memory with a 2-wire serial interface. Low current design permits operation with typical standby and active currents of only 10 µA and 1 mA respectively. The device has a page-write capability for up to 16 bytes of data and has fast write cycle times of only 1 mS for both byte and page writes. Functional address lines allow the connection of up to eight 24C01C devices on the same bus for up to 8K bits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), and TSSOP packages.

PACKAGE TYPES

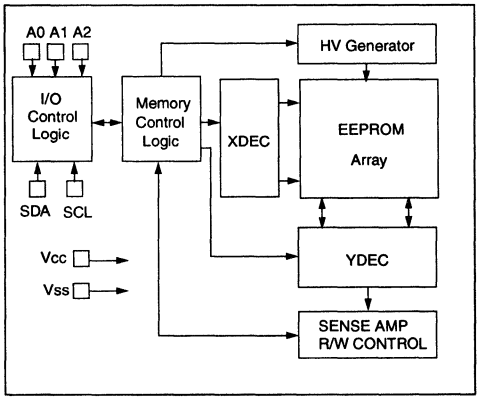
PDIP/SOIC



TSSOP



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
A0, A1, A2	Chip Selects
Test	Test Pin: may be tied high, low or left floating

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC		V	
Low level input voltage	VIL		.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC	—	V	(Note)
Low level output voltage	VOL		.40	V	IOL = 3.0 mA, VCC = 4.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to 5.5V, WP = VSS
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, f = 1 MHz
Operating current	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Write	—	3	mA	VCC = 5.5V
Standby current	ICCS	—	50	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Vcc = 4.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Tamb > +85°C		-40°C ≤ Tamb ≤ +85°C		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 C_B	250	ns	(Note 1), $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	1.5	—	1	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

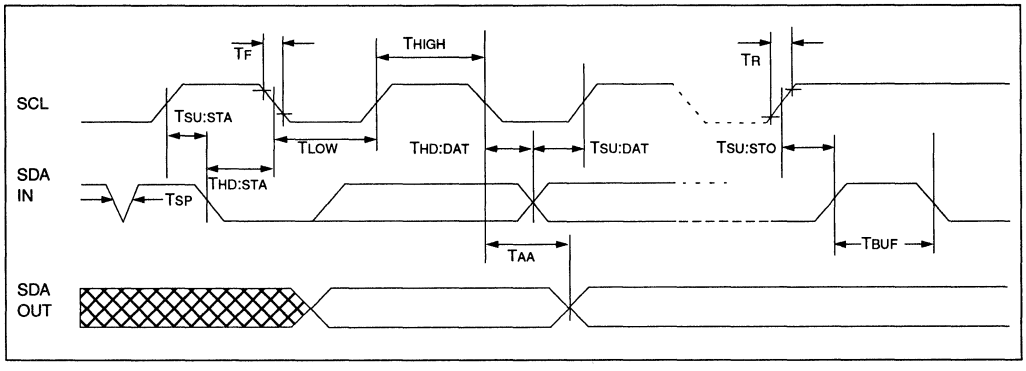
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C01C devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either Vcc or Vss.

2.4 Test

This pin is utilized for testing purposes only. It may be tied high, tied low or left floating.

2.5 Noise Protection

The 24C01C employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 3.8 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24C01C supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01C works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01C does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS

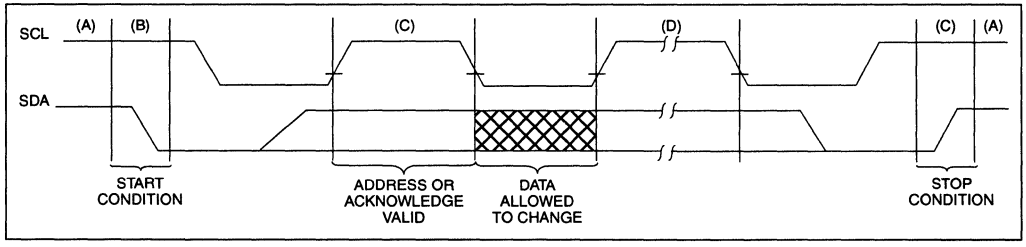
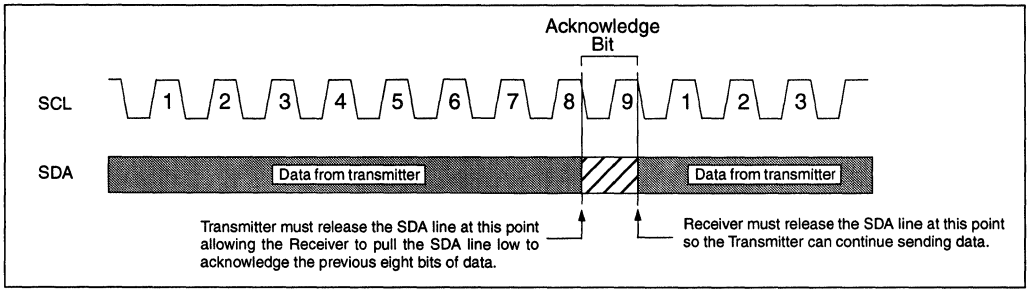


FIGURE 4-2: ACKNOWLEDGE TIMING



3

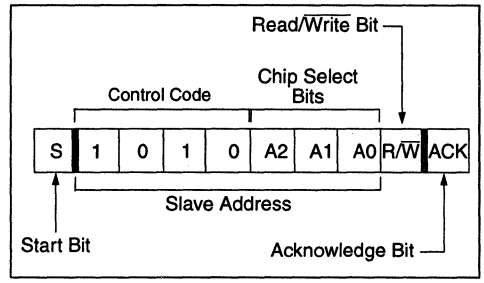
I²C™

5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a four bit control code; for the 24C01C this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24C01C devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the start condition, the 24C01C monitors the SDA bus checking the control byte being transmitted. Upon receiving a 1010 code and appropriate chip select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C01C will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 8K bits by adding up to eight 24C01C devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to write or read across device boundaries.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the device code(4 bits), the chip select bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01C. After receiving another acknowledge signal from the 24C01C the master device will transmit the data word to be written into the addressed memory location. The 24C01C acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C01C will not generate acknowledge signals (Figure 6-1).

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C01C in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 15 additional data bytes to the 24C01C which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remains constant. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 6-2).

FIGURE 6-1: BYTE WRITE

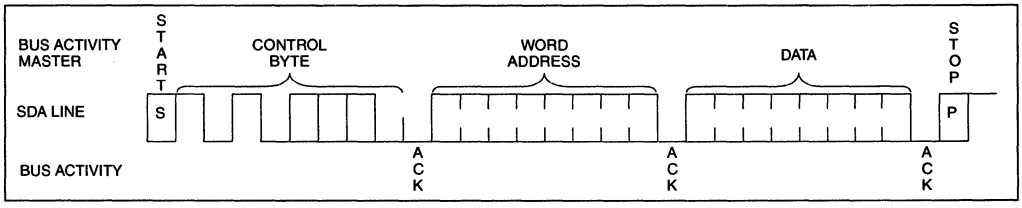
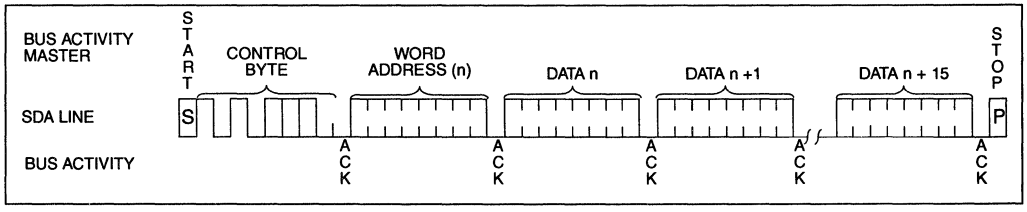


FIGURE 6-2: PAGE WRITE



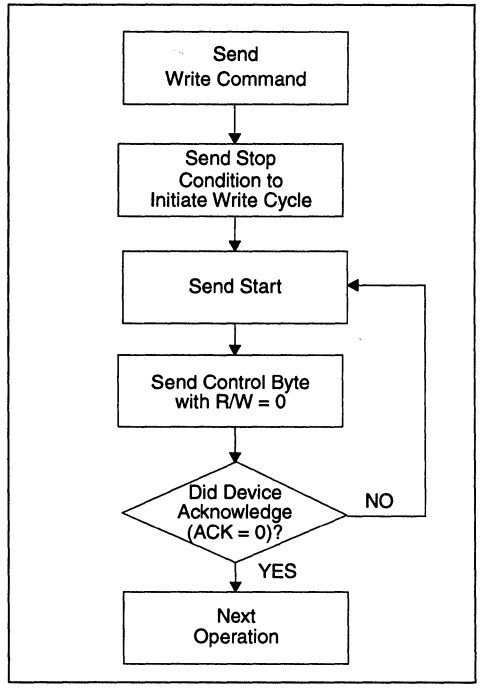
3

I²C™

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24C01C contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the 24C01C issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C01C discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C01C as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C01C will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C01C discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C01C transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C01C to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24C01C contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 7F to address 00.

FIGURE 8-1: CURRENT ADDRESS READ

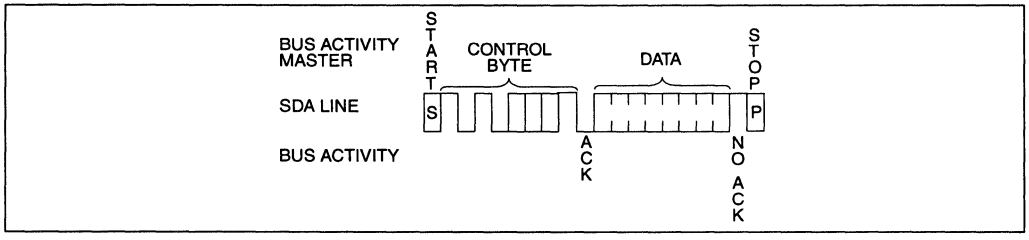


FIGURE 8-2: RANDOM READ

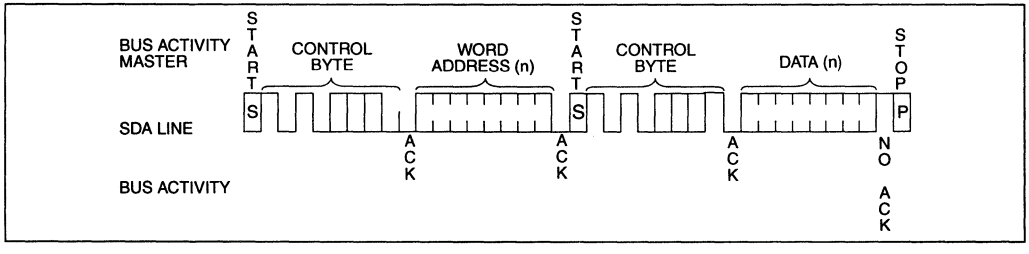
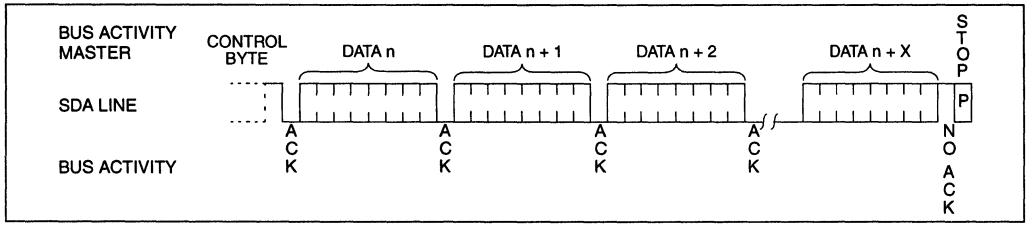
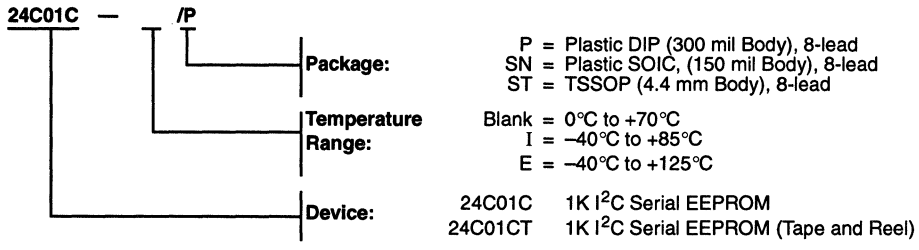


FIGURE 8-3: SEQUENTIAL READ



24C01C PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA01/02

1K 1.8V I²C™ Serial EEPROM

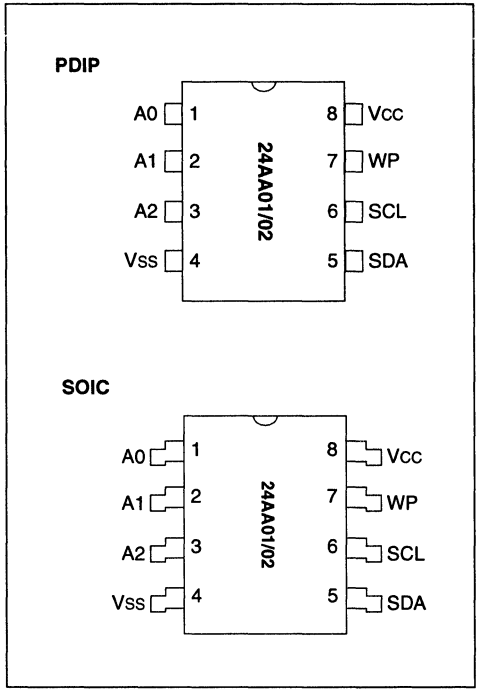
FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection > 3,000V
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data retention > 200 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

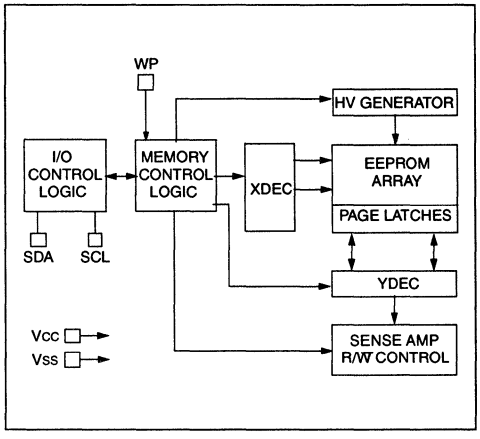
DESCRIPTION

The Microchip Technology Inc. 24AA01 and 24AA02 are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8-bit or 256 x 8-bit memory with a two wire serial interface. Low-voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA, respectively. The 24AA01 and 24AA02 also have page-write capability for up to 8 bytes of data. The 24AA01 and 24AA02 are available in the standard 8-pin DIP and 8-pin surface mount SOIC packages.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°CC
Soldering temperature of leads (10 seconds).....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data/I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	No Internal Connection

TABLE 1-2: DC CHARACTERISTICS

		VCC = +1.8V to +5.5V Commercial (C):Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:						
High level input voltage	VIH	.7 VCC	—	—	V	
Low level input voltage	VIL	—	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VDD	—	—	V	(Note)
Low level output voltage	VOL	—	—	.40	V	IOL = 3.0 mA, VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = .1V to 5.5V
Output leakage current	ILO	-10	—	10	µA	VOUT = .1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.5	—	mA	VCC = 1.8V, SCL = 100 kHz
	ICC Read	—	—	1	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.05	—	mA	VCC = 1.8V, SCL = 100 kHz
Standby current	ICCS	—	—	100	µA	VCC = 5.5V, SDA = SCL = VCC
		—	—	30	µA	VCC = 3.0V, SDA = SCL = VCC
		—	3	—	µA	VCC = 1.8V, SDA = SCL = VCC WP = VSS

Note:This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

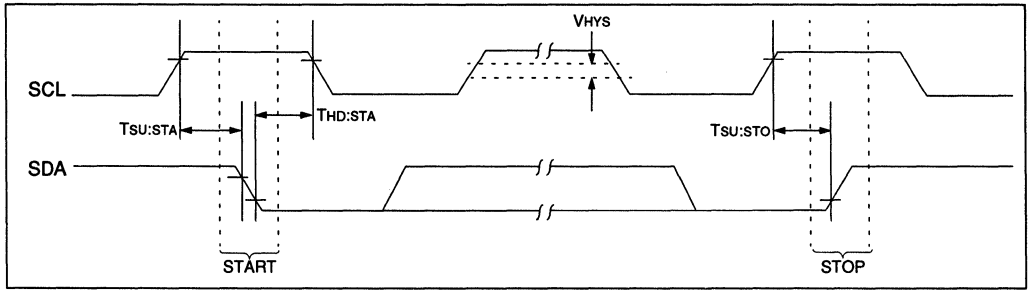


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc = 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.5V, Block Mode (Note 4)

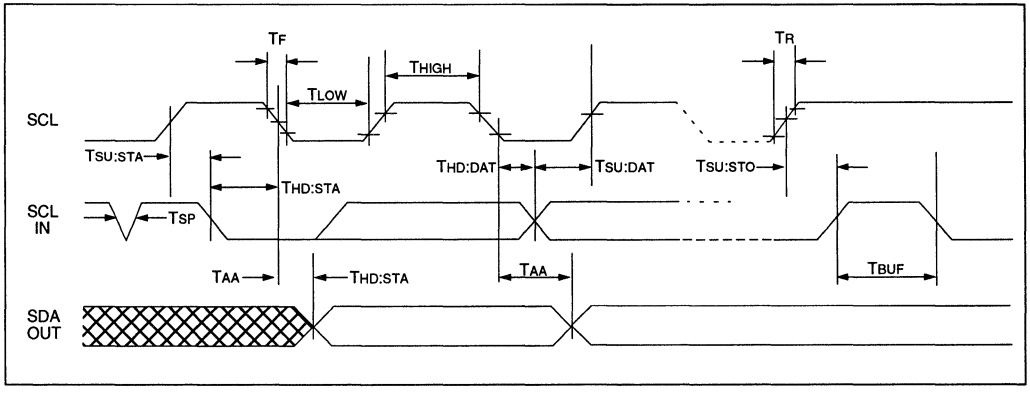
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24AA01/02 supports a bi directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA01/02 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

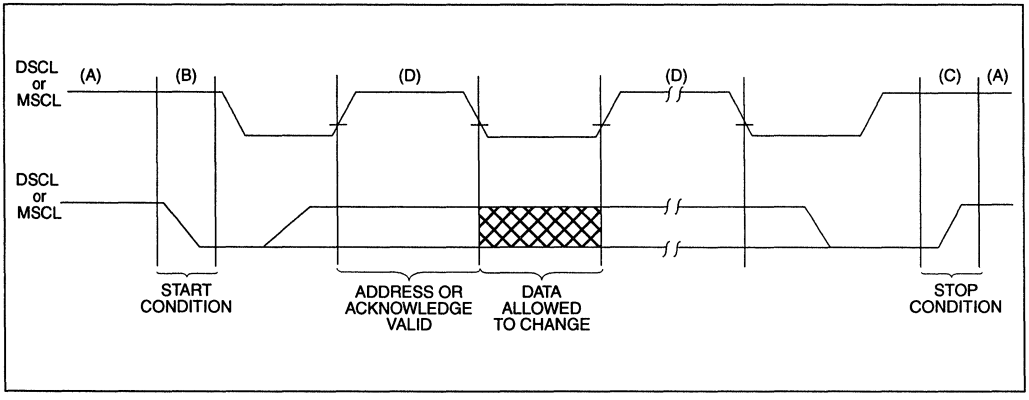
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24AA01/02 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Address

The 24AA01/02 are software-compatible with older devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24AA02 can be used in place of two 24LC01's, for example, without any modifications to software. The "chip select" portion of the control byte becomes a don't care.

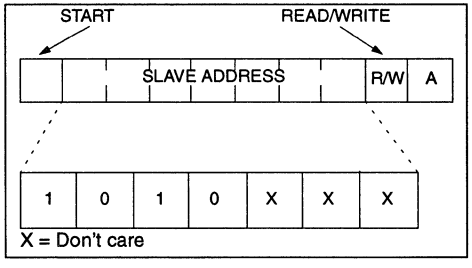
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24AA01/02, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24AA01/02 (Figure 3-2).

The 24AA01/02 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA01/02. After receiving another acknowledge signal from the 24AA01/02 the master device will transmit the data word to be written into the addressed memory location. The 24AA01/02 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA01/02 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA01/02 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24AA01/02 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 7-1).

FIGURE 4-1: BYTE WRITE

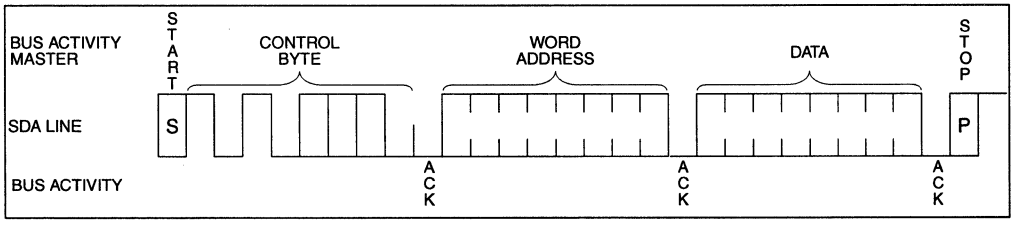
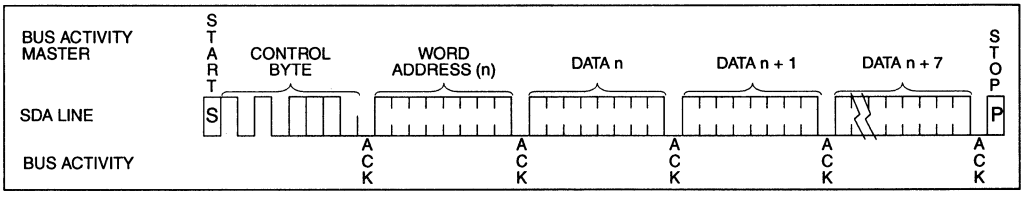


FIGURE 4-2: PAGE WRITE



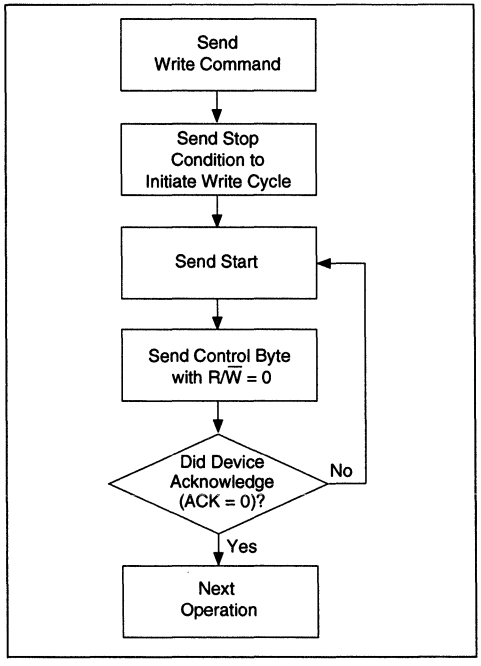
3

I²C™

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24AA01/02 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24AA01/02 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA01/02 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA01/02 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA01/02 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA01/02 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA01/02 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24AA01/02 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24AA01/02 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

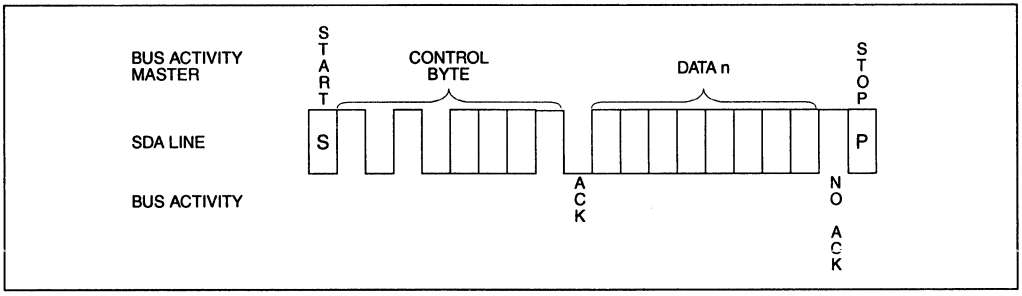


FIGURE 7-2: RANDOM READ

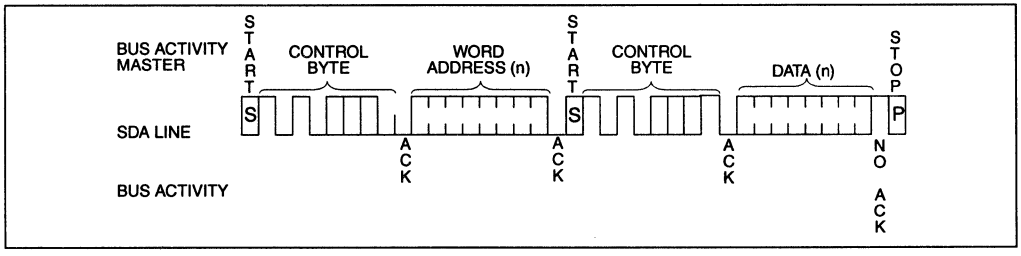
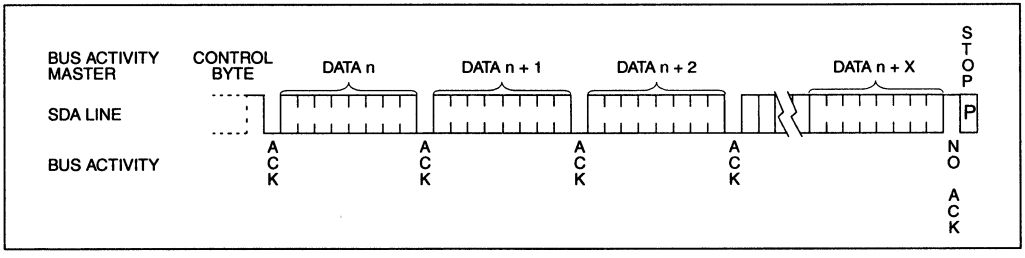


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 2K for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA01/02 as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

These pins are not used by the 24AA01/02. They may be left floating or tied to either VSS or VCC.

24AA01/02 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

24AA01/02 — /P

Package:	P	= Plastic DIP (300 mil Body), 8-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	SM	= Plastic SOIC (207 mil Body), 8-lead
Temperature Range:	Blank	= 0°C to +70°C
	I	= -40°C to +85°C
Device:	24AA01	1.8V, 1K I^2C Serial EEPROM
	24AA01T	1.8V, 1K I^2C Serial EEPROM (Tape and Reel)
	24AA02	1.8V, 2K I^2C Serial EEPROM
	24AA02T	1.8V, 2K I^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC01B/02B

1K/2K 2.5V I²C™ Serial EEPROM

FEATURES

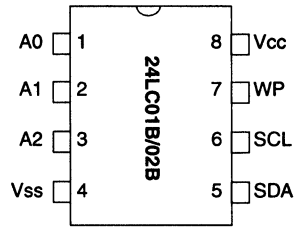
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (2.5V) and 400kHz (5.0V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection > 3,000V
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8 pin DIP or SOIC package
- Available for temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

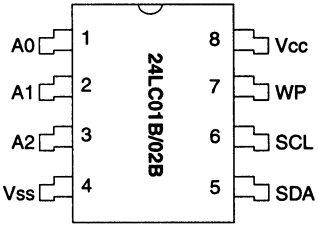
The Microchip Technology Inc. 24LC01B and 24LC02B are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8 bit or 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 5 µA and 1 mA respectively. The 24LC01B and 24LC02B also have page-write capability for up to 8 bytes of data. The 24LC01B and 24LC02B are available in the standard 8-pin DIP and an 8-pin surface mount SOIC package.

PACKAGE TYPES

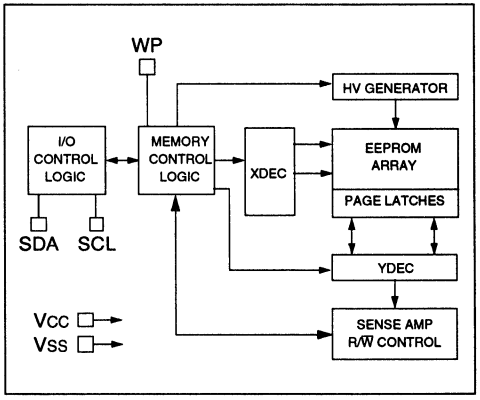
PDIP



SOIC



BLOCK DIAGRAM



3

I²C™

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-1: DC CHARACTERISTICS

	VCC = +2.5V to +5.5V		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
WP, SCL and SDA pins: High level input voltage	VIH	.7 VCC		V	
Low level input voltage	VIL		.3 VCC	V	
Hysteresis of Schmidt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL		.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to 5.5V
Output leakage current	ILO	-10	10	µmA	VOUT = .1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Read	—	1	mA	
Standby current	ICCS	—	30	µA	VCC = 3.0V, SDA = SCL = VCC
			100	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

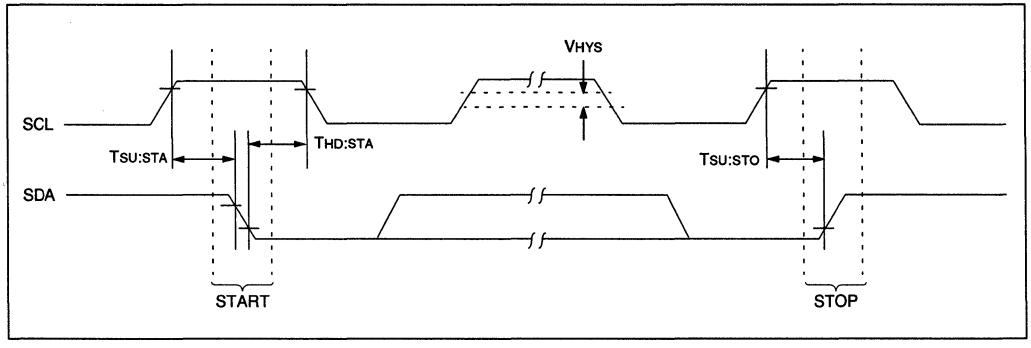
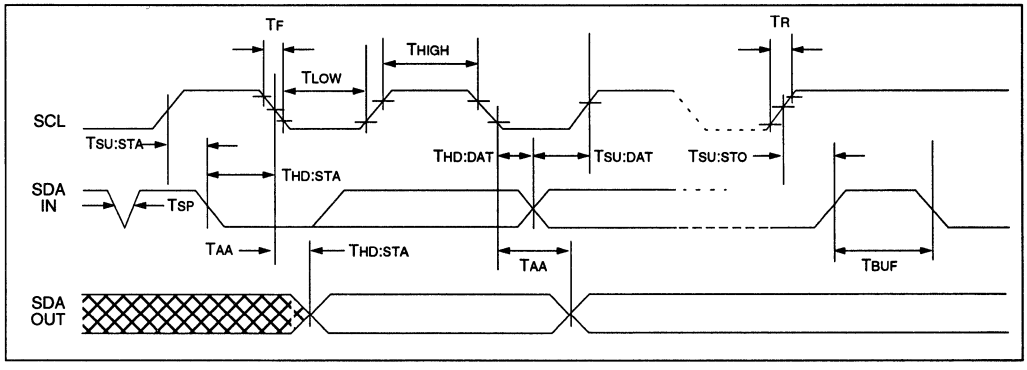


TABLE 1-2: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.
4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24LC01B/02B supports a bi-directional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC01B/02B works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus Not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

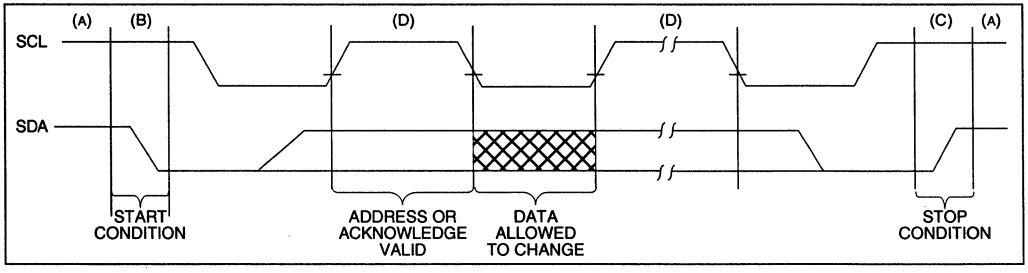
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC01B/02B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Devide Address

The 24LC01B/02B are software-compatible with older devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24LC02B can be used in place of two 24LC01's, for example, without any modifications to software. The "chip select" portion of the control byte becomes a don't care.

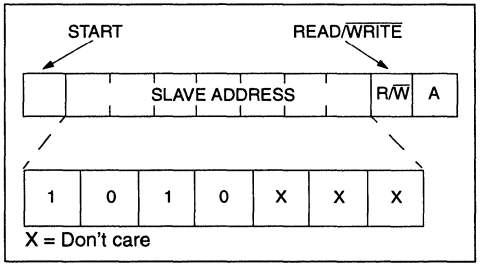
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24LC01B/02B, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC01B/02B (Figure 3-2).

The 24LC01B/02B monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC01B/02B. After receiving another acknowledge signal from the 24LC01B/02B the master device will transmit the data word to be written into the addressed memory location. The 24LC01B/02B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC01B/02B will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC01B/02B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC01B/02B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

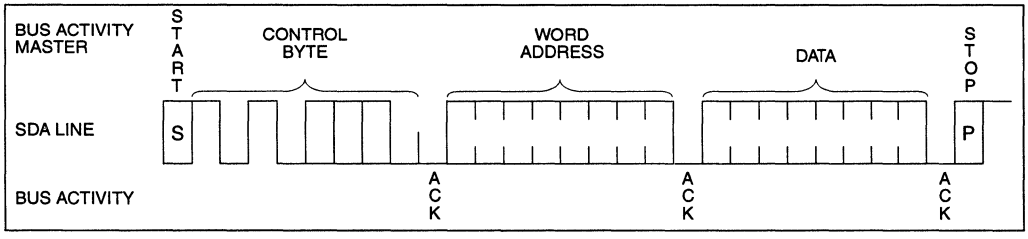
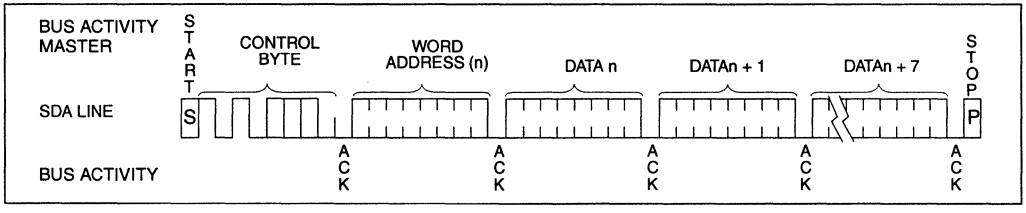


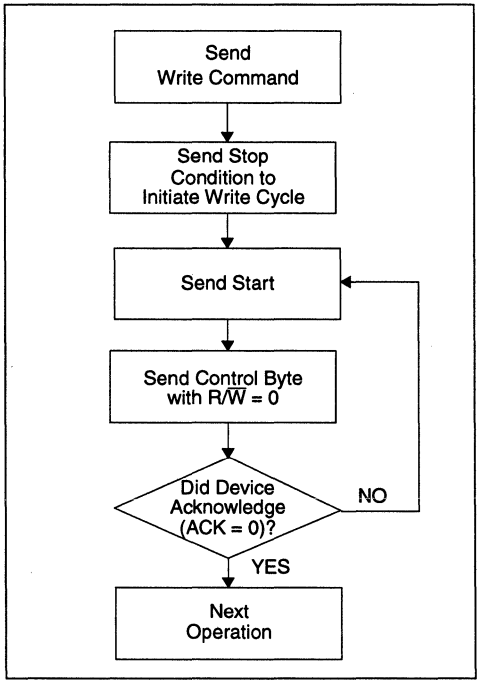
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24LC01B/02B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24LC01B/02B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with $R/\overline{W}$ bit set to one, the 24LC01B/02B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC01B/02B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24LC01B/02B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC01B/02B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC01B/02B to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LC01B/02B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC01B/02B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

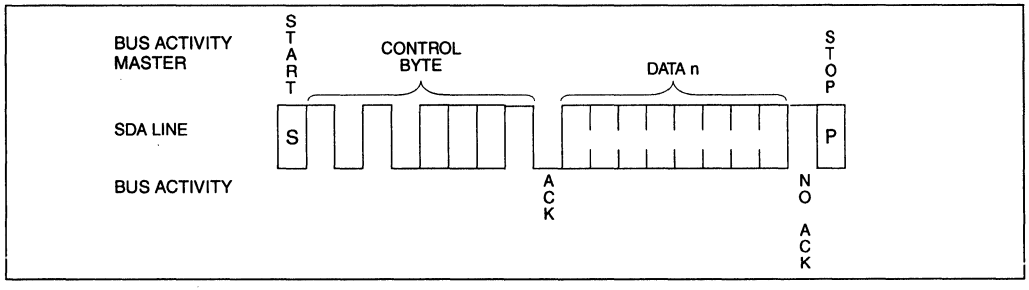


FIGURE 7-2: RANDOM READ

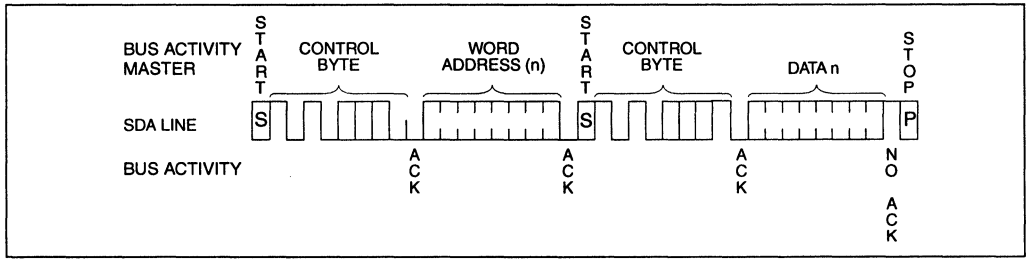
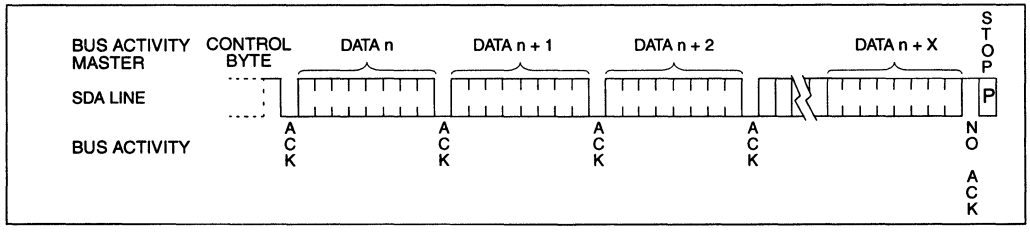


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory).

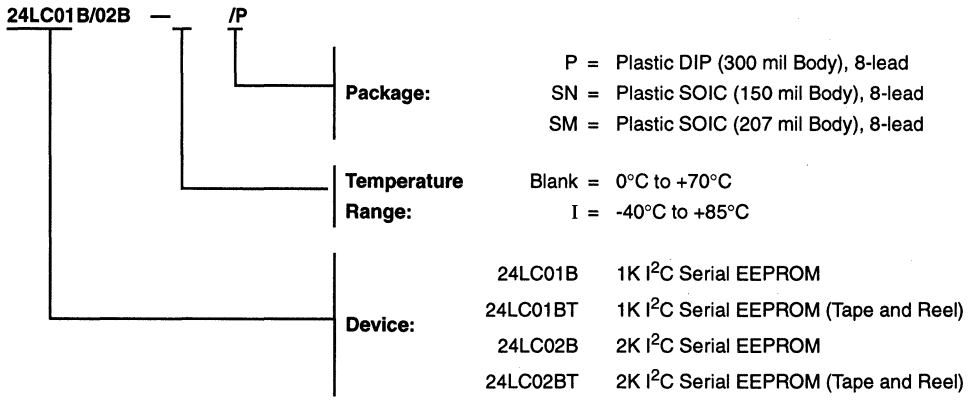
If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC01B/02B as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

These pins are not used by the 24LC01B/02B. They may be left floating or tied to either VSS or VCC.

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office..



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24C01SC/02SC

1K/2K 5.0V I²C™ Serial EEPROMs for Smart Cards

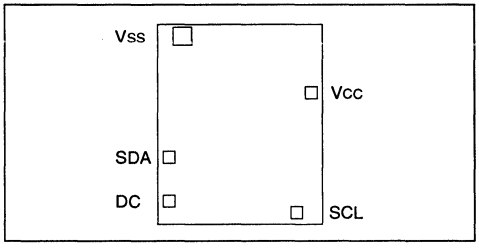
FEATURES

- **ISO Standard 7816 pad locations**
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz and 400 kHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- ESD protection > 4 kV
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C

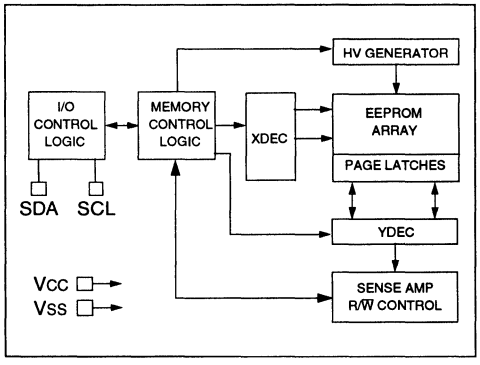
DESCRIPTION

The Microchip Technology Inc. 24C01SC and 24C02SC are 1K-bit and 2K-bit Electrically Erasable PROMs with bondpad positions optimized for smart card applications. The devices are organized as a single block of 128 x 8-bit or 256 x 8-bit memory with a two-wire serial interface. The 24C01SC and 24C02SC also have page-write capability for up to 8 bytes of data.

DIE LAYOUT



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
ESD protection on all pads.....≥4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PAD FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
DC	Don't connect

TABLE 1-2: DC CHARACTERISTICS

	VCC = +4.5V to +5.5V		Commercial (C): Tamb = 0°C to +70°C		
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pads:					
High level input voltage	VIH	.7 VCC	—	—	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmidt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, VCC = 4.5V
Input leakage current (SCL)	ILI	-10	10	µA	VIN = .1V to 5.5V
Output leakage current (SDA)	ILO	-10	10	µA	VOUT = .1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V
	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 KHz
Standby current	ICCS	—	100	µA	VCC = 5.5V, SDA = SCL = VCC

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

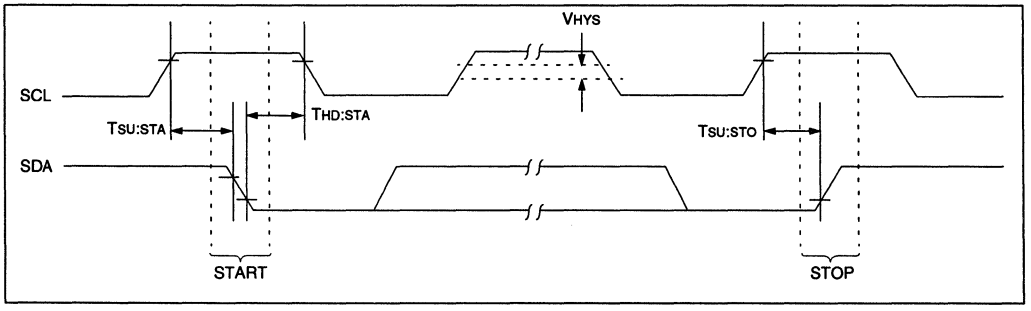


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Units	Remarks
Clock frequency	FCLK	—	400	kHz	
Clock high time	THIGH	600	—	ns	
Clock low time	TLOW	1300	—	ns	
SDA and SCL rise time	TR	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	100	—	ns	
STOP condition setup time	TSU:STO	600	—	ns	
Output valid from clock	TAA	—	900	ns	(Note 2)
Bus free time	TBUF	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	ms	Byte or Page mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5V, Block Mode (Note 4)

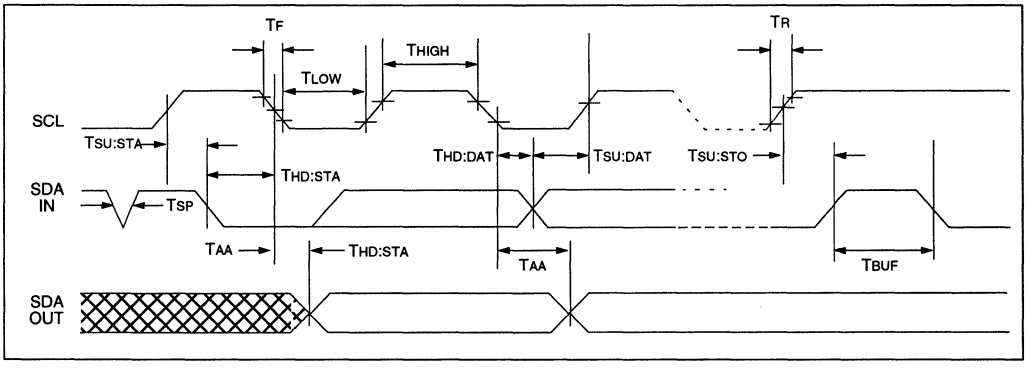
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24C01SC/02SC supports a bi-directional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01SC/02SC works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

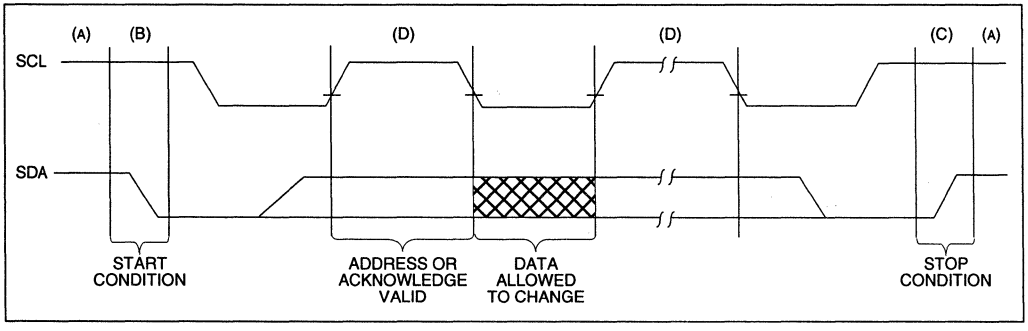
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24C01SC/02SC does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Slave Address

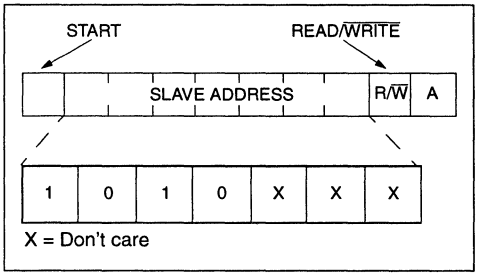
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01SC/02SC, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01SC/02SC (Figure 4-1).

The 24C01SC/02SC monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true, and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

5.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit, which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01SC/02SC. After receiving another acknowledge signal from the 24C01SC/02SC, the master device will transmit the data word to be written into the addressed memory location. The 24C01SC/02SC acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C01SC/02SC will not generate acknowledge signals (Figure 5-1).

5.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24C01SC/02SC in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight data bytes to the 24C01SC/02SC, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 5-2).

FIGURE 5-1: BYTE WRITE

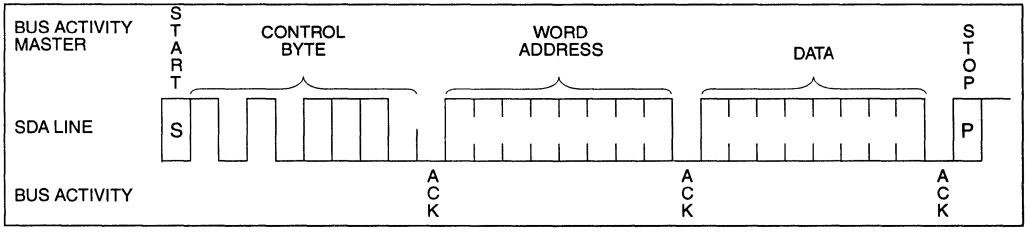
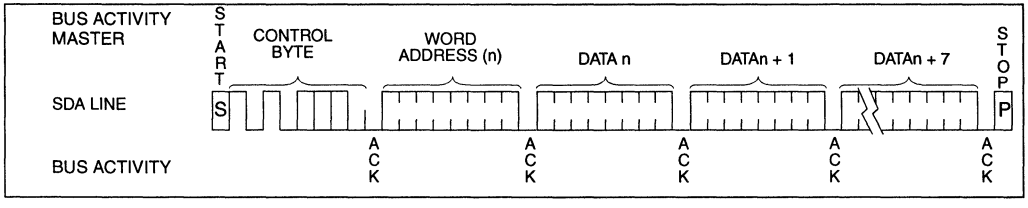


FIGURE 5-2: PAGE WRITE



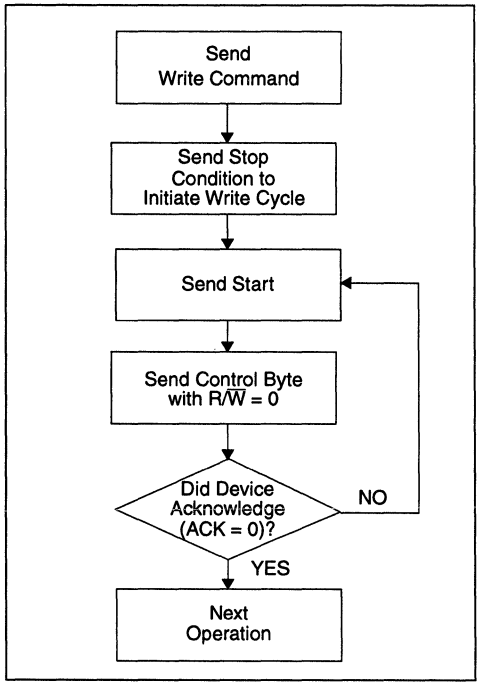
3

I²C™

6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then NO ACK will be returned. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24C01SC/02SC contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with $R/\overline{W}$ bit set to one, the 24C01SC/02SC issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C01SC/02SC discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C01SC/02SC as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then, the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24C01SC/02SC will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C01SC/02SC discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C01SC/02SC transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C01SC/02SC to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24C01SC/02SC contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24C01SC/02SC employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

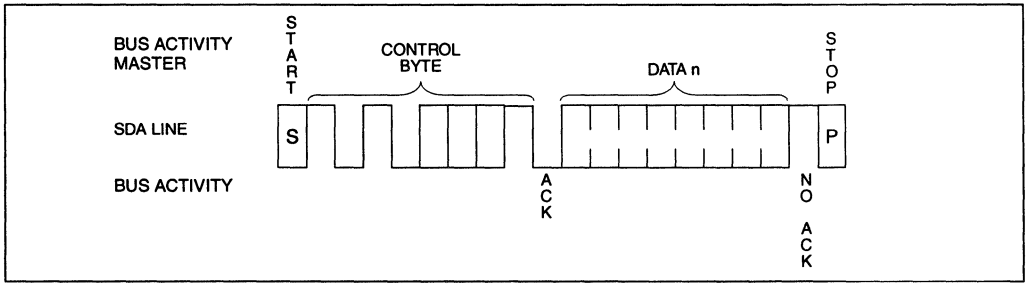


FIGURE 7-2: RANDOM READ

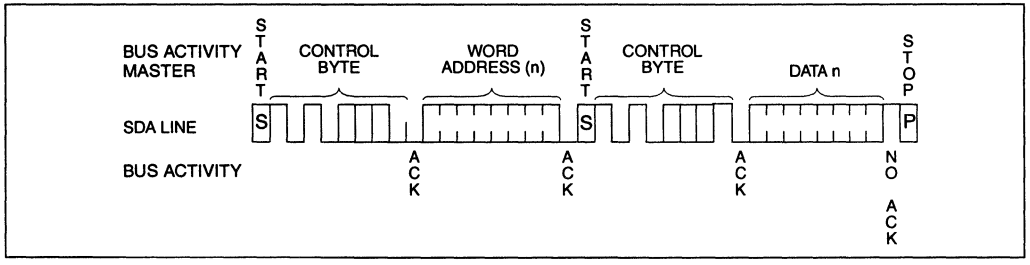
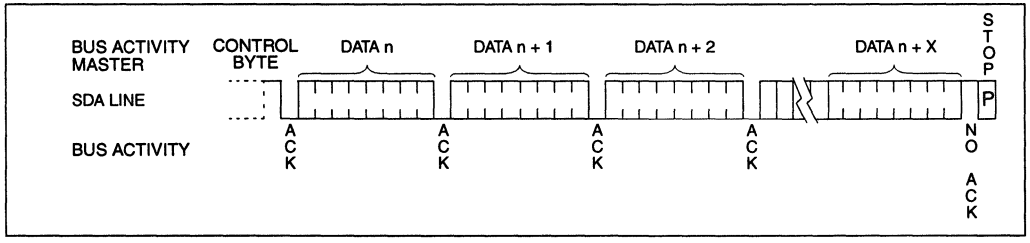


FIGURE 7-3: SEQUENTIAL READ



3

I²C™

8.0 PAD DESCRIPTIONS

8.1 SDA Serial Address/Data Input/Output

This is a bi-directional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 DC Don't Connect

This pad is used for test purposes and should not be bonded out. It is pulled down to Vss through an internal resistor.

9.0 DIE CHARACTERISTICS

Figure 9-1 shows the die layout of the 24C01SC/02SC, including bondpad positions. Table 9-1 shows the actual coordinates of the bondpad midpoints with respect to the center of the die.

FIGURE 9-1: DIE LAYOUT

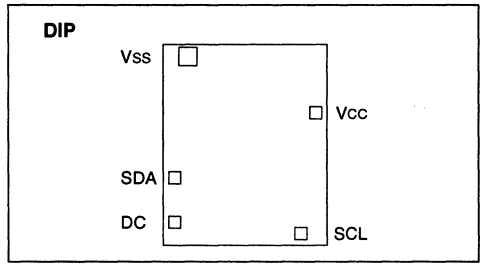


TABLE 9-1: BONDPAD COORDINATES

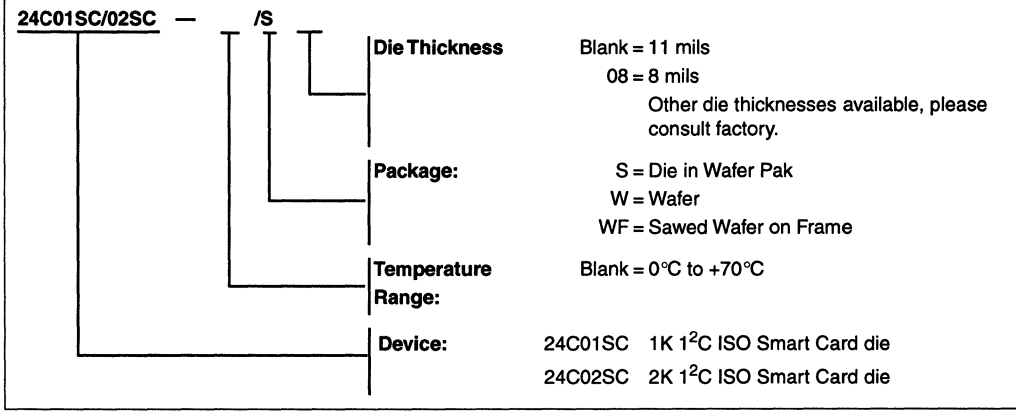
Pad Name	Pad Midpoint, X dir.	Pad Midpoint, Y dir.
Vss	-495.000	749.130
SDA	-605.875	-271.875
SCL	479.875	-746.625
Vcc	605.875	-261.375

Note 1: Dimensions are in microns.
2: Center of die is at the 0,0 point.

NOTES:

24C01SC/02SC Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LCS61/24LCS62

1K/2K Software Addressable I²C™ Serial EEPROM

PRODUCT OFFERING

Device	Array Size	Voltage Range	Software Write Protection
24LCS61	1K bits	2.5V-5.5V	Entire Array
24LCS62	2K bits	2.5V-5.5V	Lower Half

FEATURES

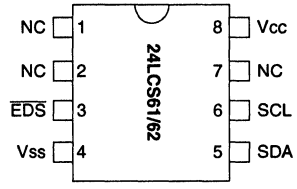
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Software addressability allows up to 255 devices on the same bus
- 2-wire serial interface bus, I²C compatible
- Automatic bus arbitration
- Wakes up to control code 0110
- General purpose output pin can be used to enable other circuitry
- 100 kHz and 400 kHz compatibility
- Page-write buffer for up to 16 bytes
- 10 ms max write cycle time for byte or page write
- 1,000,000 erase/write cycles guaranteed
- 8-pin PDIP, SOIC or TSSOP packages
- Temperature ranges supported:
  - Industrial (I): -40°C to +85°C

DESCRIPTION

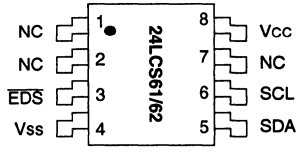
The Microchip Technology Inc. 24LCS61/62 is a 1K/2K bit Serial EEPROM developed for applications that require many devices on the same bus but do not have the I/O pins required to address each one individually. These devices contain an 8 bit address register that is set upon power-up and allows the connection of up to 255 devices on the same bus. When the process of assigning ID values to each device is in progress, the device will automatically handle bus arbitration if more than one device is operating on the bus. In addition, an external open drain output pin is available that can be used to enable other circuitry associated with each individual system. Low current design permits operation with typical standby and active currents of only 10 µA and 1 mA respectively. The device has a page-write capability for up to 16 bytes of data. The device is available in the standard 8-pin PDIP, SOIC (150 mil), and TSSOP packages.

PACKAGE TYPES

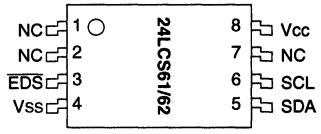
PDIP



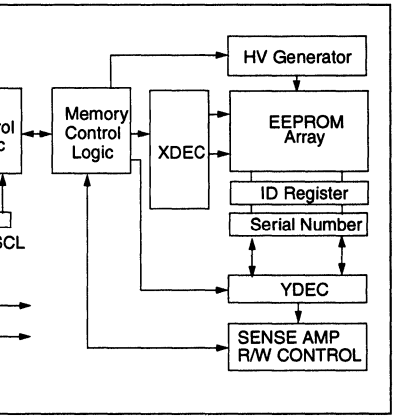
SOIC



TSSOP



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss.....-0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
Vcc	+2.5V to 5.5V Power Supply
NC	No Internal Connection
$\overline{EDS}$	External Device Select Output

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Vcc = +2.5V to +5.5V Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	0.7 Vcc		V	
Low level input voltage	VIL		.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 Vcc	—	V	
Low level output voltage (SDA and $\overline{EDS}$ pins)	VOL		.40	V	IOL = 12 mA, Vcc = 4.5V IOL = 8 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = Vss or Vcc
Output leakage current	ILO	-10	10	µA	VOUT = Vss or Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note) Tamb = 25°C, f = 1 MHz
Operating current	Icc Write	—	4	mA	Vcc = 5.5V
	Icc Read	—	1	mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	Iccs	—	50	µA	Vcc = 5.5V, SDA = SCL = Vcc $\overline{EDS}$ = Vcc

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.		Vcc = +2.5V to 5.5V Industrial (I): Tamb = -40°C to +85°C					
Parameter	**Symbol**	**Vcc = 2.5V - 5.5V STD MODE**		**Vcc = 4.5V - 5.5V FAST MODE**		**Units**	**Remarks**
		Min.	**Max.**	**Min.**	**Max.**		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	From VIL to VIH (Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	From VIL to VIH (Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time (from 0.7 VCC to 0.3 VCC)	TOF	—	250	20 +0.1 C_B	250	ns	(Note 1), $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Notes 1, 3)
Write cycle time	TWC	—	10	—	10	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

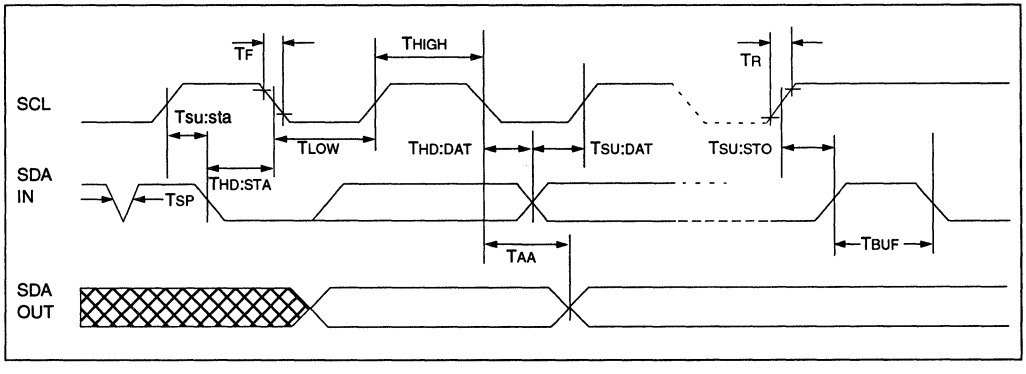
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-1: BUS TIMING DATA



3

I²C™

2.0 PIN DESCRIPTIONS

2.1 SDA (Serial Data)

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions. The SDA pin has Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus

2.2 SCL (Serial Clock)

This input is used to synchronize the data transfer from and to the device. The SCL pin has Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

2.3 $\overline{\text{EDS}}$ (External Device Select)

The External Device Select ($\overline{\text{EDS}}$) pin is an open drain output that is controlled by using the OE bit in the control byte. It can be used to enable other circuitry when the device is selected. A pull-up resistor must be added to this pin for proper operation. This pin should not be pulled up to a voltage higher than Vcc+1V. See Section 9.0 for more details.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

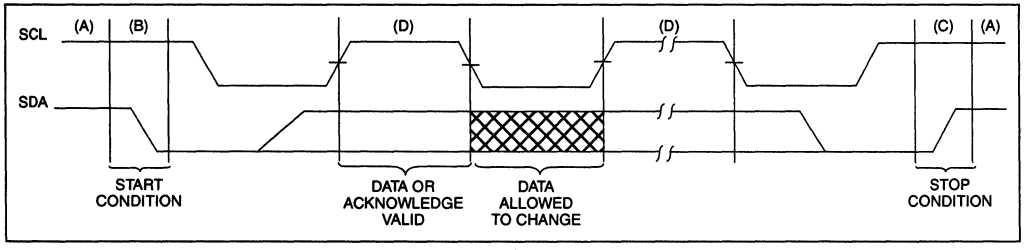
3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



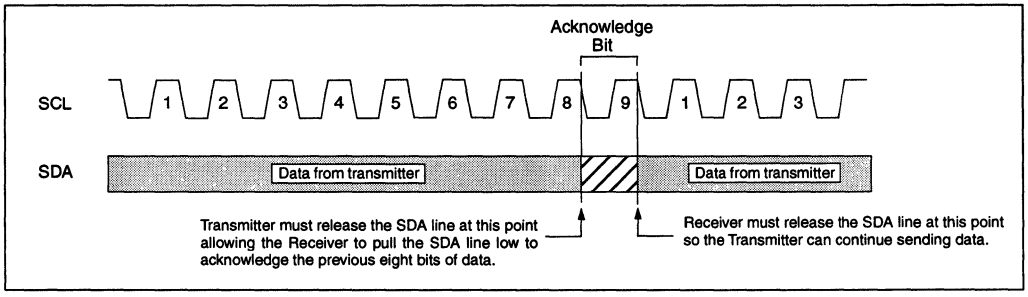
3.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LCS61/62 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 3-2).

FIGURE 3-2: ACKNOWLEDGE TIMING



3

I²C™

4.0 FUNCTIONAL DESCRIPTION

The 24LCS61/62 supports a bi-directional 2-wire bus and data transmission protocol compatible with the I^2C protocol. The device is configured to reside on a common I^2C bus with up to 255 total 24LCS61/62 devices on the bus. Each device has a unique serial number assigned to it when delivered from the factory. In an actual system, this serial number will be used to assign a separate 8-bit ID byte to each device in the system. After an ID byte is assigned to each device in the system, standard read and write commands can be sent to each device individually.

4.1 Device Serial Number

The device serial number is stored in a 48-bit (6 byte) register that is separate from the data array. The serial number register is non-volatile and cannot be changed by the user. Before shipment from the factory, this register is programmed with a unique value for every device. The 48 bit register allows for $2.8 \bullet 10^{14}$ different combinations. The serial number is used at power-up to assign the device an ID byte which is then used for all standard read and write commands sent to that specific device.

4.2 Device ID Byte

The Device ID byte is an 8-bit value that provides the means for every device on the bus to be accessed individually. The ID byte is stored in a RAM register separate from the data array. The ID byte register will always default to address 00 upon power-up.

4.3 Device Addressing

Each command to the device must begin with a start bit. A control byte is the first byte received following the start condition from the master device (Figure 4-1). The control byte consists of a four-bit control code, the OE bit, and three command select bits. For the 24LCS61/62, the control code is set to 0110 binary for all operations. The device will not acknowledge any commands sent with any other control code. The next bit is the Output Enable (OE) bit. This bit controls the operation of the $\overline{EDS}$ pin. See Section 9.0 for more details. The last three bits of the control byte are the command select bits (C0-C2). The command select bits determine which command will be executed. See Table 4-1. Following a valid control byte, the 24LCS61/62 will acknowledge the command.

FIGURE 4-1: CONTROL BYTE FORMAT

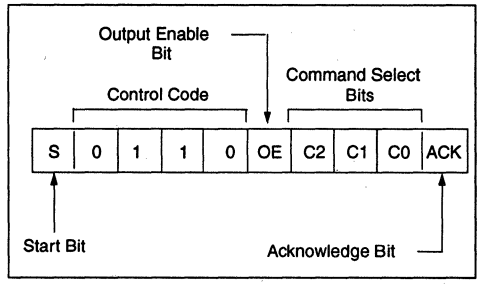


TABLE 4-1: COMMAND CODES

Command	Command Select Bits (C2 C1 C0)
Set Write Protection Fuse	000
Read	001
Write (Byte or Page)	010
Assign Address	100
Clear Address	110

5.0 ASSIGNING THE ID BYTE

The 24LCS61/62 device contains a special register which holds an 8-bit ID byte that is used as an address to communicate with a specific device on the bus. All read and write commands to the device must include this ID address byte. Upon power-up, the ID byte will default to 00h. Communicating with the device using the default address is typically done only at testing or programming time and not when it is connected to a bus with more than one device. Before the device can be used on a common bus with other devices, a unique ID byte address must be assigned to every device.

5.1 Assign Address Command

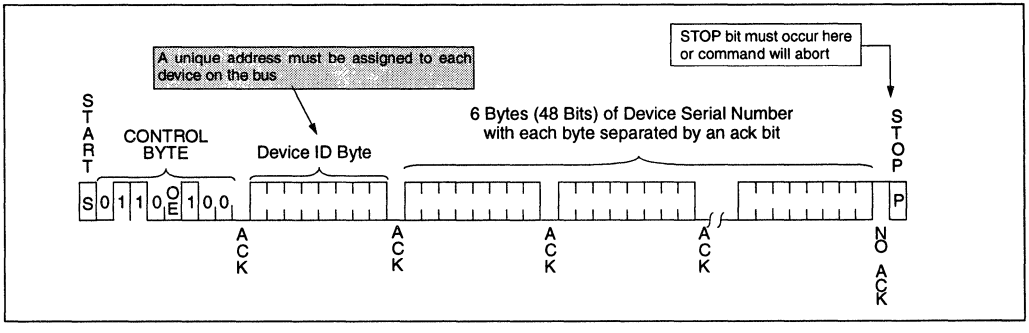
The ID byte is assigned by sending the Assign Address command. This command queries any device connected to the bus and utilizing the automatic bus arbitration feature, assigns an ID byte to the device that remains on the bus after arbitration is complete. Once a device has been assigned an ID byte, it will no longer respond to Assign Address commands until power is cycled or the Clear Address command is sent. The Assign Address command must be repeated for each device on the bus until all devices have been assigned an ID byte.

The format for the Assign Address command is shown in Figure 5-1. The command consists of the control byte, the ID byte to be assigned to the device remaining when the arbitration is complete, and 48 bits of data being transmitted by devices on the bus. If the OE bit is set to a 1, then any device who has not been assigned an address will assert their respective $\overline{EDS}$ pin after the acknowledge bit following the Device ID byte. After the control byte and ID byte are sent, each device will begin to transmit its unique 48-bit serial number. The 24LCS61/62 must acknowledge the control byte and the device ID byte, and the master must acknowledge each byte of the serial number transmitted by the device. As each bit is clocked out, each device will monitor the bus to detect if another device is also transmitting. If any device is outputting a logic '1' on the bus and it detects that the bus is at a logic '0', then it assumes that another device is controlling the bus. As soon as any device detects that it is not controlling the bus it will immediately stop transmitting data and return to standby mode. The master must end the command by sending a no ack after all 6 bytes of the serial number have been transmitted, followed by a Stop bit. Sending the Stop bit in any other position of the command will result in the command aborting and all devices releasing the bus with no address assigned. If a device transmits its entire 48 bit serial number without releasing the bus to another device, then the ID byte transmitted within the command is transferred to the internal ID byte register upon receipt of the Stop bit and it will now respond only to commands that contain this ID byte (or the Clear Address command). Once a device has been assigned an ID byte, it will no longer respond to Assign Address commands until power is cycled or the Clear Address command is sent.

This process of assigning ID bytes is repeated by the controller until no more devices respond to the Assign Address command. At this point, all devices on the bus have been assigned an ID byte and standard read and write commands can be executed to each individual device.

The ID byte is stored in a volatile SRAM register, and if power is removed from the device or the Clear Address command is sent, then the ID byte will default to address 00 and the process of assigning an ID value must be repeated.

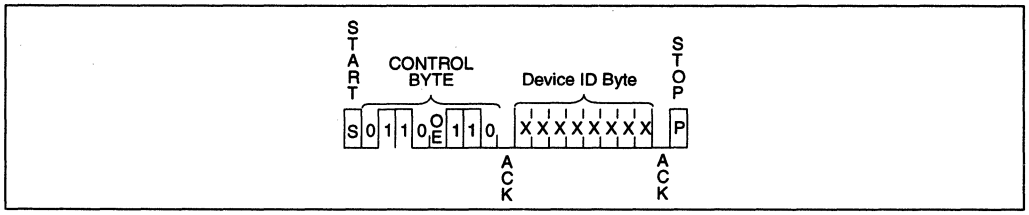
FIGURE 5-1: ASSIGN ADDRESS COMMAND



5.2 Clear Address Command

The clear address command will clear the device ID byte from all devices on the bus and will enable all devices to respond to the Assign Address command. The master must end the command by sending an ack after 8 don't care bits have been transmitted, followed by a Stop bit. Sending the Stop bit in any other position of the command will result in the command aborting and the device releasing the bus.

FIGURE 5-2: CLEAR ADDRESS COMMAND



5.3 Operation State Diagram

The diagram below shows the state diagram for basic operation of the 24LCS61/62. This diagram shows possible states and operational flow once power is applied to the device. Table 5-1 summarizes operation of each command for the assigned and unassigned states.

FIGURE 5-3: OPERATIONAL STATE DIAGRAM

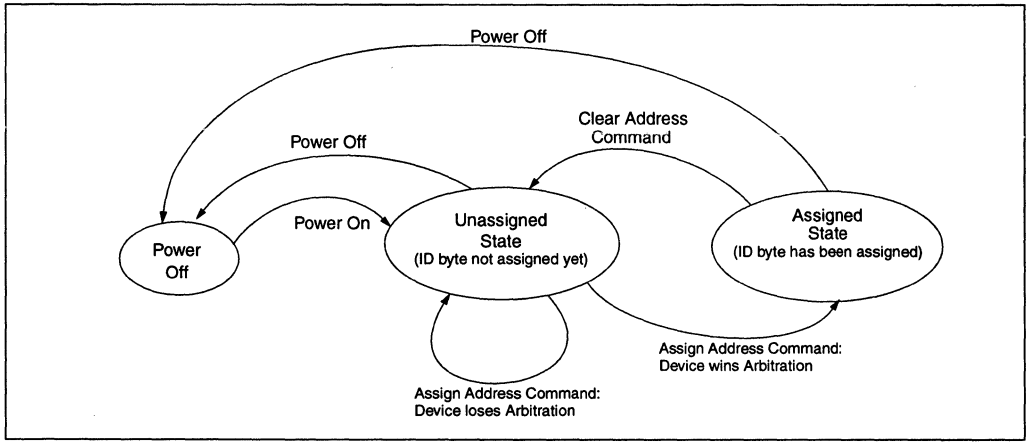


TABLE 5-1: COMMAND SUMMARY TABLE

Command	Result if Device Has Not Yet Been Assigned an ID Byte	Result if Device Has Already Been Assigned an ID Byte
Assign Address command	If device wins arbitration, then ID byte will become xxh. If device loses arbitration, then ID byte will revert back to 00h.	Device will not acknowledge command.
Clear Address command	Device will remain with ID byte set to 00h.	Device ID byte will revert back to 00h and will then acknowledge Assign Address commands.
Read or Write command with ID byte set to 00h	Since the default ID byte for the device is 00h, the device will execute the command.	Device will acknowledge the control byte, but it will not acknowledge any further bytes and will not respond to the command.
Read or Write command with ID byte set to xxh (other than 00h)	Device will acknowledge the control byte, but it will not acknowledge any further bytes and will not respond to the command.	If the device ID byte matches the ID byte in the command (xxh), the device will execute the command. If the device ID byte does not match the ID byte in the command, then the device will acknowledge the control byte, but it will not acknowledge any further bytes and will not respond to the command.
Set Write Protect command with ID byte set to 00h	Since the default ID address for the device is 00h, the device will execute the command.	Device will acknowledge the control byte, but it will not acknowledge any further bytes and will not respond to the command.
Set Write Protection command with ID byte set to xxh (other than 00h)	Device will acknowledge the control byte, but it will not acknowledge any further bytes and will not respond to the command.	If the device ID byte matches the ID byte in the command (xxh), the device will execute the command. If the device ID byte does not match the ID byte in the command, then the device will acknowledge the control byte, but it will not acknowledge any further bytes and will not respond to the command. Note: Once this command has been executed successfully for a device, the device will no longer acknowledge any part of this command again.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the control byte for a write command is sent by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the ID byte for the device. After receiving another acknowledge signal from the 24LCS61/62, the master device will transmit the address and then the data word to be written into the addressed memory location. The 24LCS61/62 acknowledges between each byte, and the master then generates a stop condition. This initiates the internal write cycle, and during this time the 24LCS61/62 will not generate acknowledge signals (Figure 6-1).

6.2 Page Write

The control byte, ID byte, word address, and the first data byte are transmitted to the 24LCS61/62 in the same way as in a byte write. But, instead of generating a stop condition, the master transmits up to 15 additional data bytes to the 24LCS61/62, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 6-2) and the 24LCS61/62 will not generate acknowledge.

6.3 Low Voltage Write Protection

The 24LCS61/62 employs a Vcc threshold detector circuit which disables the internal erase/write logic, if the Vcc is below 1.5 volts at nominal conditions.

6.4 Set Write Protection Command

The Set Write Protection command allows the user to write protect a portion of the array. For the 24LCS61 this command will write protect the entire array. For the 24LCS62 this command will protect the lower half of the array. This command is illustrated in Figure 6-3. **This is a one time only command and cannot be reversed once the protection fuse has been set.** Once the Write protect feature has been set, the device will no longer acknowledge the control byte (or any of the other bytes) of this command. The STOP bit of this command initiates an internal write cycle, and during this time the 24LCS61/62 will not generate acknowledge signals.

FIGURE 6-1: BYTE WRITE

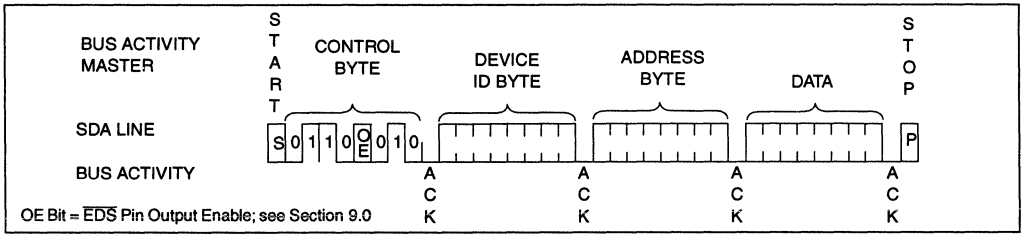


FIGURE 6-2: PAGE WRITE

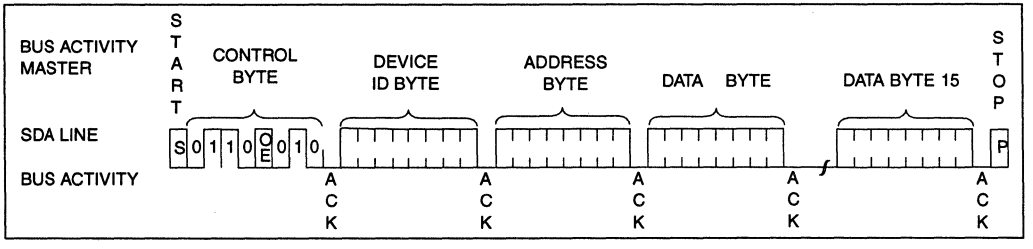
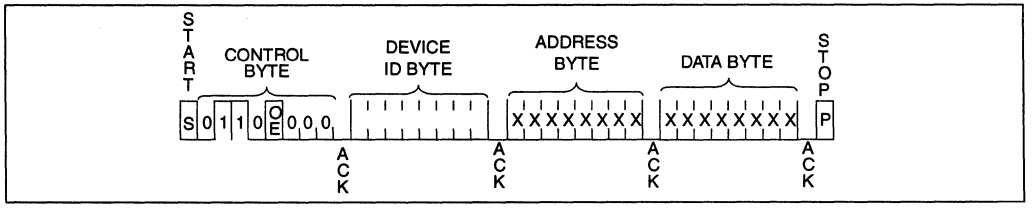


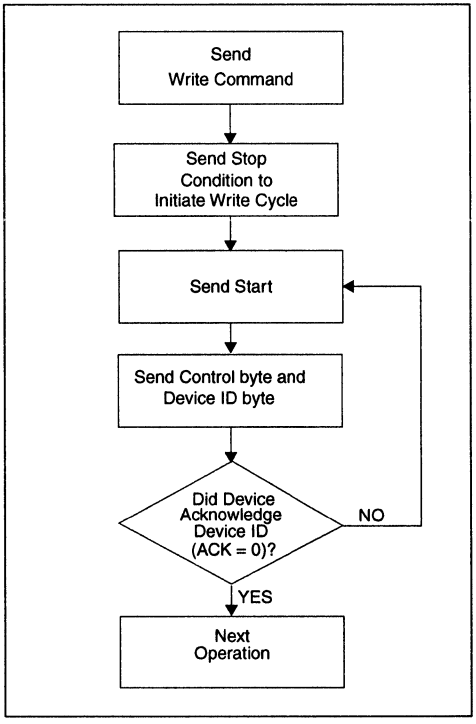
FIGURE 6-3: SET WRITE PROTECTION COMMAND



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command and then sending the Device ID byte for that particular device. If the device is still busy with the write cycle, then no ACK will be returned after the Device ID byte. If no ACK is returned, then the start bit, control byte and ID byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATIONS

Read operations are initiated in a similar way as the write operations. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LCS61/62 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the correct control byte and ID byte, the 24LCS61/62 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS61/62 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LCS61/62 as part of a write operation. After the ID byte and word address are sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master sends the control byte and ID byte for a read command. The 24LCS61/62 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS61/62 discontinues transmission (Figure 8-2).

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LCS61/62 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LCS61/62 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24LCS61/62 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 7Fh (24LCS61) or FFh (24LCS62) to address 00h.

FIGURE 8-1: CURRENT ADDRESS READ

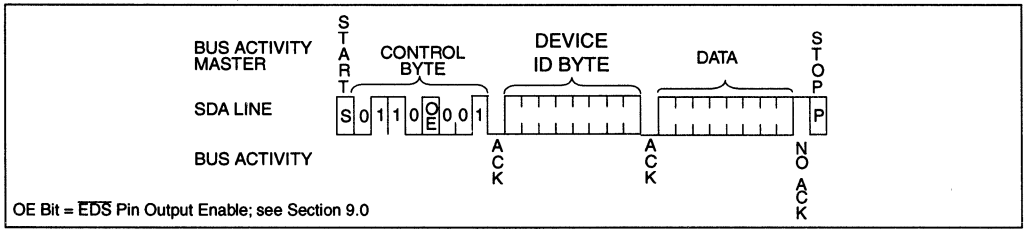


FIGURE 8-2: RANDOM READ

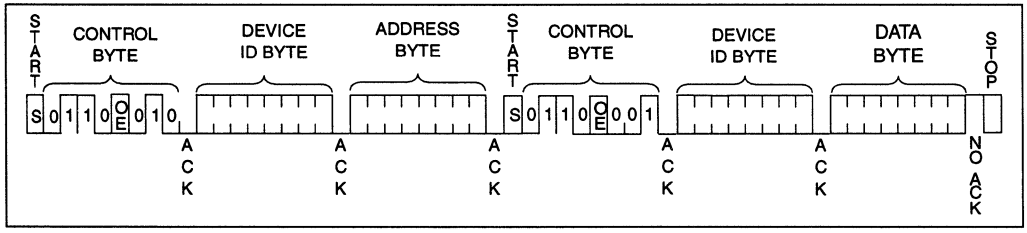
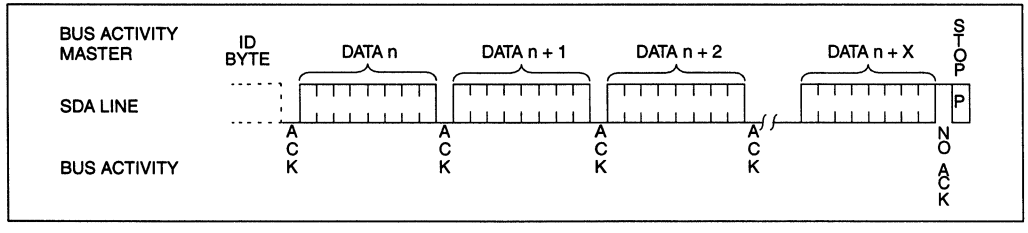


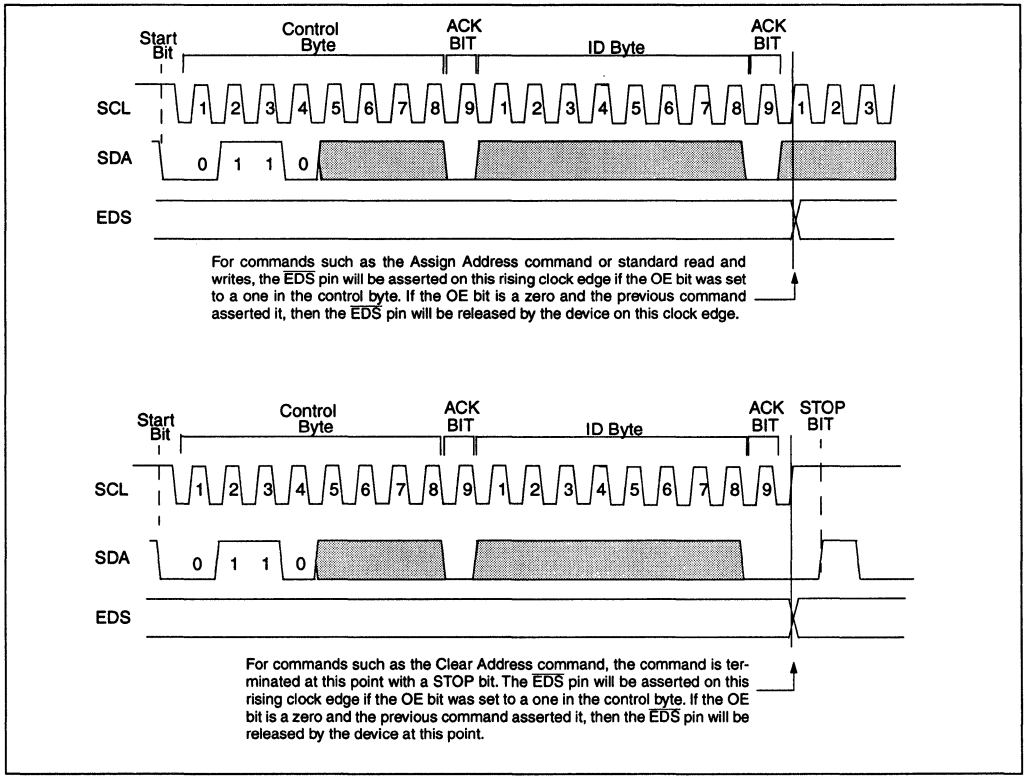
FIGURE 8-3: SEQUENTIAL READ



9.0 EXTERNAL DEVICE SELECT ($\overline{EDS}$) PIN AND OUTPUT ENABLE (OE) BIT

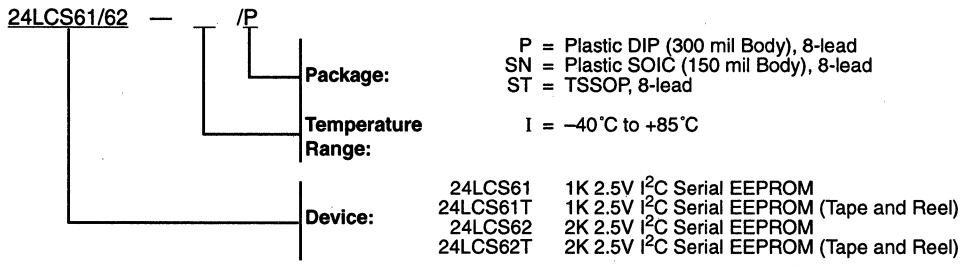
The External Device Select ($\overline{EDS}$) pin is an open drain, low active output and may be used by the system designer for functions such as enabling other circuitry when the 24LCS61/62 is being accessed. Because the pin is an open drain output, a pull-up resistor is required for proper operation of this pin. When the device is powered up, the $\overline{EDS}$ pin will always be in the high impedance state (off). The $\overline{EDS}$ pin function is controlled by using the output enable (OE) bit in the control byte of each command. If the OE bit is high, the $\overline{EDS}$ pin is enabled and if the OE bit is low the pin is disabled. For the Assign Address command and standard read or write commands, the $\overline{EDS}$ pin will pull low (providing that the OE bit is set high) on the rising clock edge after the ack bit following the ID byte. See Figure 9-1. For commands such as the Clear Address command, the $\overline{EDS}$ pin will change states at the rising clock edge just before the Stop bit. It is also possible to control the $\overline{EDS}$ pin by sending a partial command such as the control byte and ID byte for a write command followed by the Stop bit. The $\overline{EDS}$ pin would change states just before the Stop bit as shown in the lower portion of Figure 9-1. When the $\overline{EDS}$ pin has changed states, it is latched and will remain in a given state until another command is sent to the device with the OE bit set to change the state of the pin, or power to the device is removed.

FIGURE 9-1: $\overline{EDS}$ PIN OPERATION



24LCS61/62 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24C02C

2K 5.0V I^2C^{TM} Serial EEPROM

FEATURES

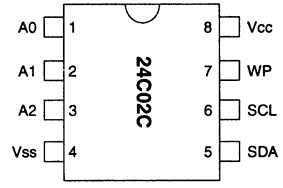
- Single supply with operation from 4.5 to 5.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as a single block of 256 bytes (256 x 8)
- Hardware write protection for upper half of array
- 2-wire serial interface bus, I^2C compatible
- 100 kHz and 400 kHz compatibility
- Page-write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- Fast 1 mS write cycle time for byte or page mode
- Address lines allow up to eight devices on bus
- 1,000,000 erase/write cycles guaranteed
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC or TSSOP packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

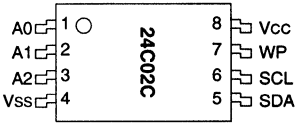
The Microchip Technology Inc. 24C02C is a 2K bit Serial Electrically Erasable PROM with a voltage range of 4.5V to 5.5V. The device is organized as a single block of 256 x 8-bit memory with a 2-wire serial interface. Low current design permits operation with typical standby and active currents of only 10 µA and 1 mA respectively. The device has a page-write capability for up to 16 bytes of data and has fast write cycle times of only 1 mS for both byte and page writes. Functional address lines allow the connection of up to eight 24C02C devices on the same bus for up to 16K bits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), and TSSOP packages.

PACKAGE TYPES

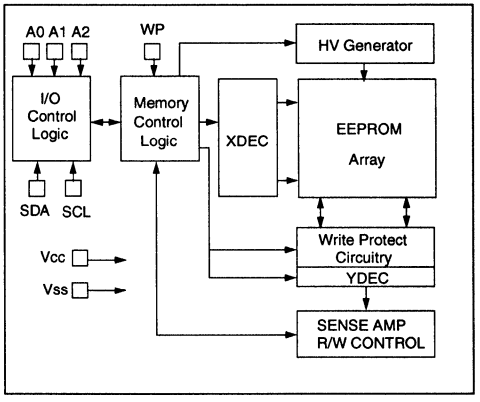
PDIP/SOIC



TSSOP



BLOCK DIAGRAM



3

I^2C^{TM}

I^2C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write Protect

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC	—	V	
Low level input voltage	VIL	—	0.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	0.40	V	IOL = 3.0 mA, VCC = 4.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to 5.5V, WP = VSS
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, f = 1 MHz
Operating current	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Write	—	3	mA	VCC = 5.5V
Standby current	ICCS	—	50	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.		Vcc = 4.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C					
Parameter	**Symbol**	**Tamb > +85°C**		**-40°C ≤ Tamb ≤ +85°C**		**Units**	**Remarks**
		Min.	**Max.**	**Min.**	**Max.**		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock iow time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 C_B	250	ns	(Note 1), $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	1.5	—	1	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

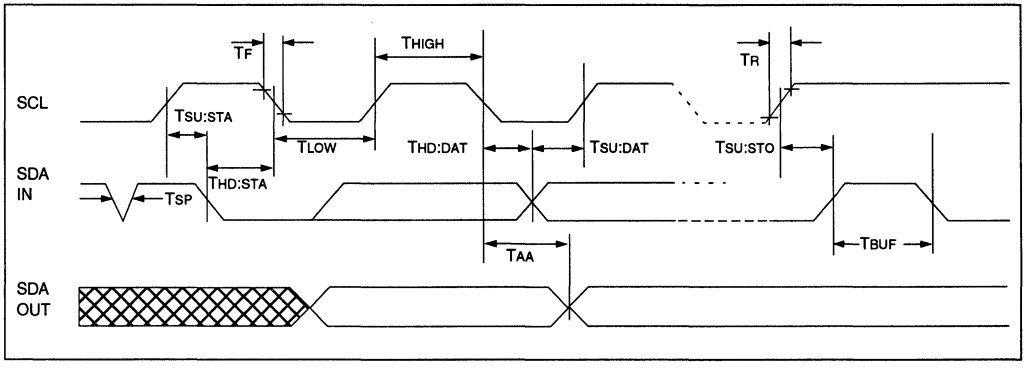
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C02C devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either Vcc or Vss.

2.4 WP

This is the hardware write protect pin. It must be tied to Vcc or Vss. If tied to Vcc, the hardware write protection is enabled. If the WP pin is tied to Vss the hardware write protection is disabled.

2.5 Noise Protection

The 24C02C employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 3.8 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24C02C supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C02C works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C02C does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS

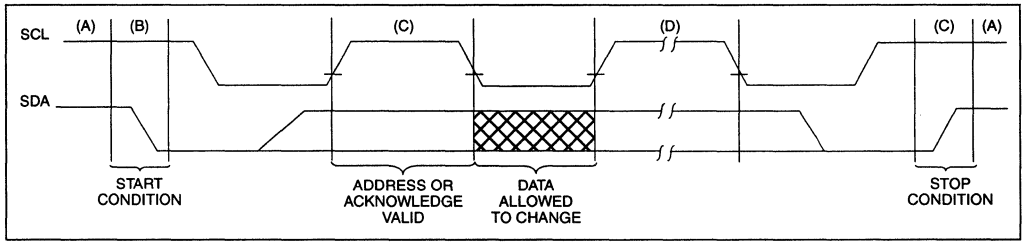
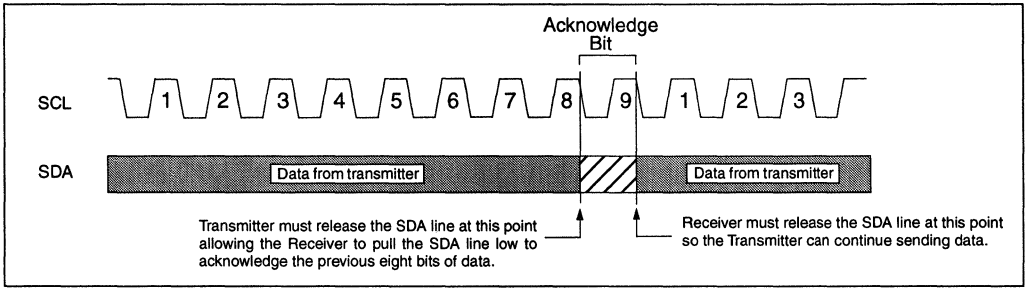


FIGURE 4-2: ACKNOWLEDGE TIMING



3

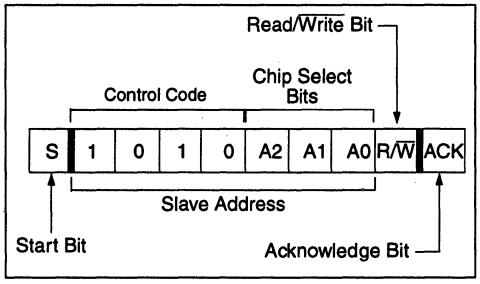
I²C™

5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a four bit control code; for the 24C02C this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24C02C devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the start condition, the 24C02C monitors the SDA bus checking the control byte being transmitted. Upon receiving a 1010 code and appropriate chip select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C02C will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24C02C devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to write or read across device boundaries.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the device code (4 bits), the chip select bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the address pointer of the 24C02C. After receiving another acknowledge signal from the 24C02C the master device will transmit the data word to be written into the addressed memory location. The 24C02C acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C02C will not generate acknowledge signals (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C02C in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 15 additional data bytes to the 24C02C which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remains constant. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

6.3 WRITE PROTECTION

The WP pin must be tied to VCC or VSS. If tied to VCC, the upper half of the array (080-0FF) will be write protected. If the WP pin is tied to VSS, then write operations to all address locations are allowed.

FIGURE 6-1: BYTE WRITE

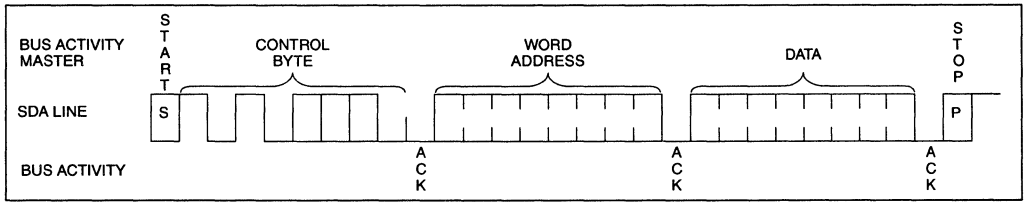
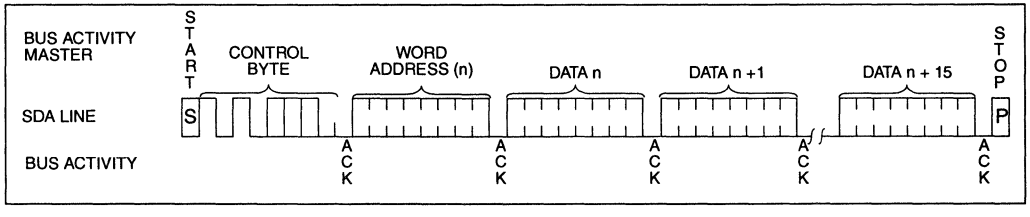


FIGURE 6-2: PAGE WRITE



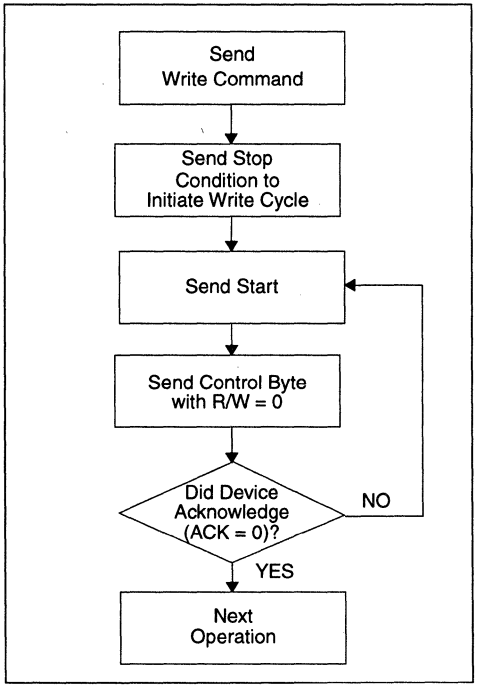
3

I²C™

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24C02C contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the 24C02C issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C02C discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C02C as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C02C will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C02C discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C02C transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C02C to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24C02C contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address FF to address 00.

FIGURE 8-1: CURRENT ADDRESS READ

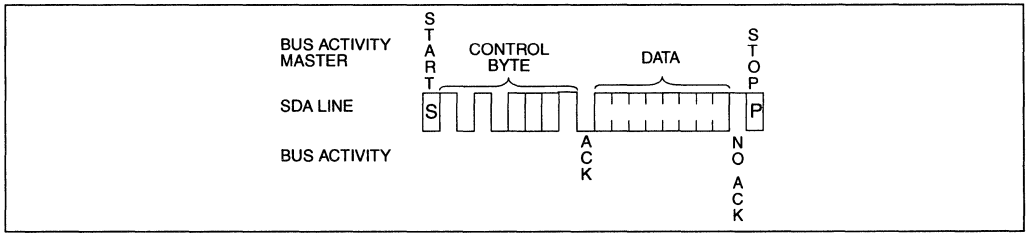


FIGURE 8-2: RANDOM READ

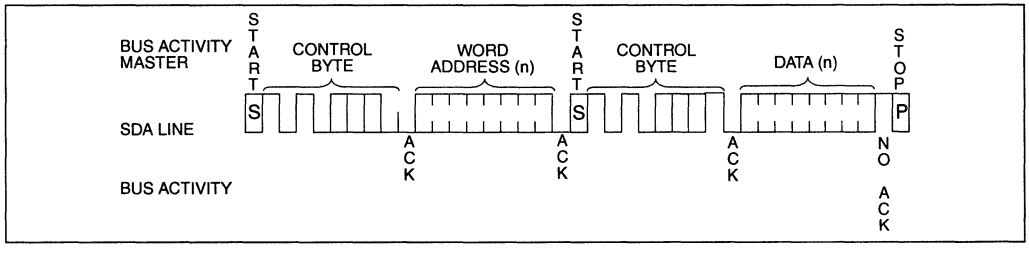
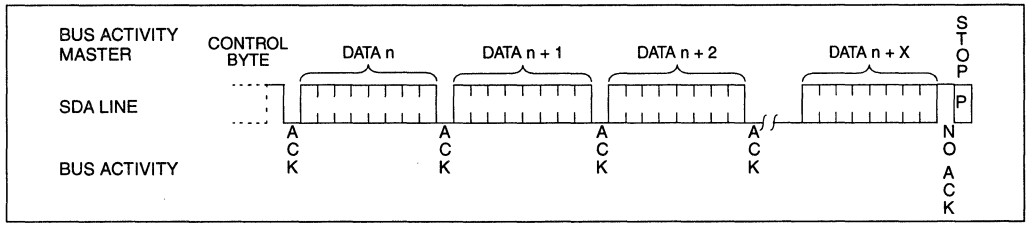


FIGURE 8-3: SEQUENTIAL READ

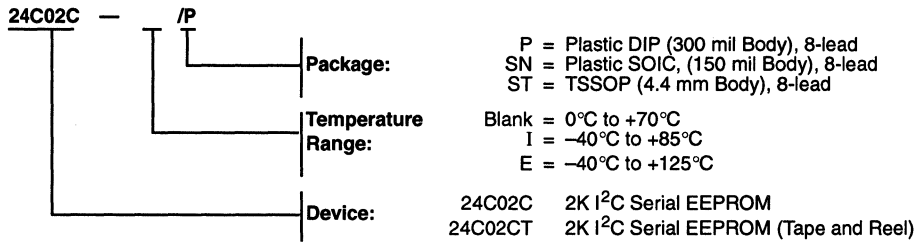


3

I²C™

24C02C PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LCS52

2K 2.5V I²C™ Serial EEPROM with Software Write Protect

FEATURES

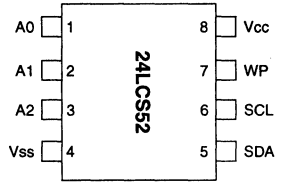
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as a single block of 256 bytes (256 x 8)
- Software write protection for lower 128 bytes
- Hardware write protection for entire array
- 2-wire serial interface bus, I²C™ compatible
- 100kHz (2.5V) and 400kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 3.5 ms typical write cycle time for page-write
- 1,000,000 erase/write cycles guaranteed
- ESD protection >4,000V
- Data retention > 200 years
- 8-pin DIP, SOIC or TSSOP packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

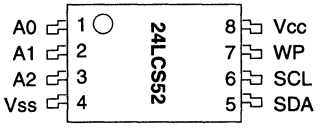
The Microchip Technology Inc. 24LCS52 is a 2K bit Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 5.5V). This device has a software write protect feature for the lower half of the array, as well as an external pin that can be used to write protect the entire array. The software write protect feature is enabled by sending the device a special command, and once this feature has been enabled, it cannot be reversed. In addition to the software protect feature, there is a WP pin that can be used to write protect the entire array, regardless of whether the software write protect register has been written or not. This allows the system designer to protect none, half or all of the array, depending on the application. The device is organized as a single block of 256 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 2.5 volts with typical standby and active currents of only 5 µA and 1 mA respectively. The device has a page-write capability for up to 16 bytes of data. The device is available in the standard 8-pin DIP, 8-pin SOIC and TSSOP packages.

PACKAGE TYPES

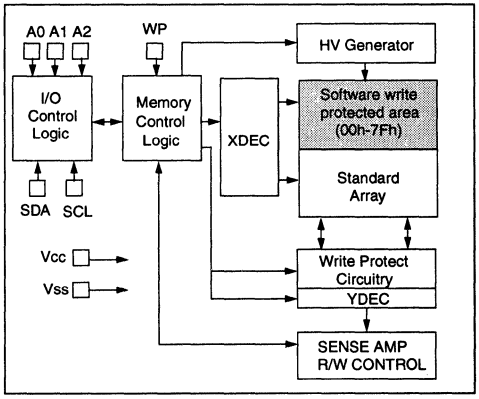
PDIP/SOIC



TSSOP



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write Protect

TABLE 1-2: DC CHARACTERISTICS

	Vcc = +2.5V to +5.5V		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc		V	
Low level input voltage	VIL		.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	(Note)
Low level output voltage	VOL		.40	V	IOL = 3.0 mA, Vcc = 2.5V
Input leakage current					
All I/O pins	ILI	-10	10	µA	VIN = 0.1V to 5.5V, WP = Vss
WP pin	ILI	-10	50	µA	WP = Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note) Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write	—	3	mA	Vcc = 5.5V, SCL = 400 kHz
	Icc Read	—	1	mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	Iccs	—	30	µA	Vcc = 3.0V, SDA = SCL = Vcc
			100	µA	Vcc = 5.5V, SDA = SCL = Vcc WP = Vss, A0, A1, A2 = Vss

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

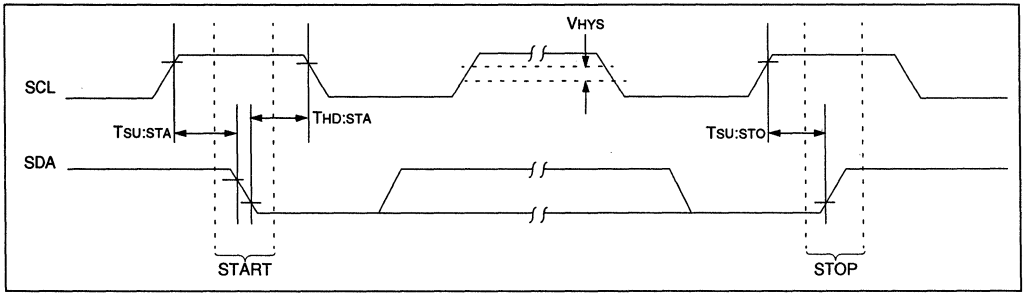


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 2.5-5.5V STD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

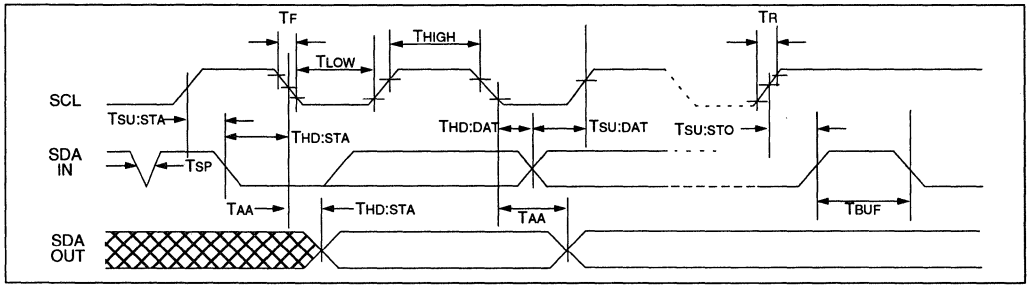
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24LCS52 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LCS52 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus Not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

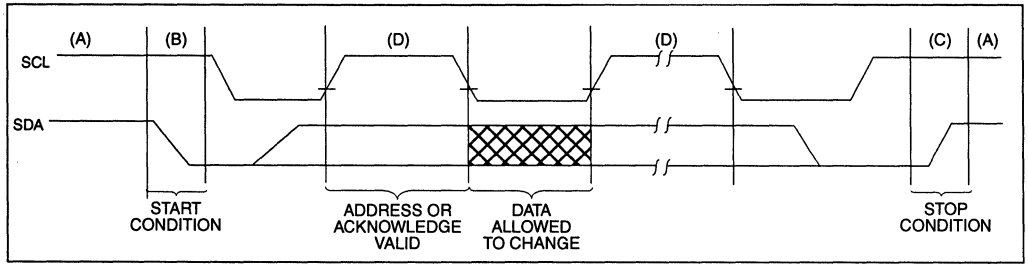
Note:	The 24LCS52 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

3.6 Device Addressing

A control byte is the first byte received following the START condition from the master device. The first part of the control byte consists of a 4-bit control code which is set to 1010 for normal read and write operations and 0110 for writing to the write protect register. The control byte is followed by three chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24LCS52 devices on the same bus and are used to determine which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. The device will not acknowledge if you attempt a read command with the control code set to 0110.

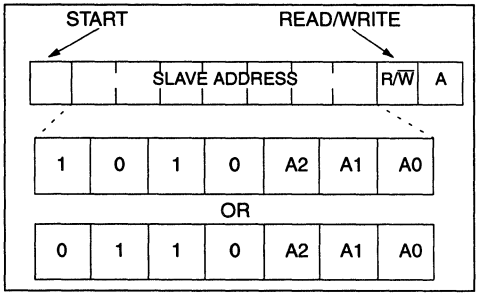
FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS



The eighth bit of slave address determines if the master device wants to read or write to the 24LCS52 (Figure 3-2). When set to a one a read operation is selected and when set to a zero a write operation is selected.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0
Set Write Protect Register	0110	A2 A1 A0	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATIONS

4.1 Byte Write

Following the start signal from the master, the device code (4 bits), the chip select bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LCS52. After receiving another acknowledge signal from the 24LCS52 the master device will transmit the data word to be written into the addressed memory location. The 24LCS52 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LCS52 will not generate acknowledge signals (Figure 4-1). If an attempt is made to write to the array when the software or hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LCS52 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 15 additional data bytes to the 24LCS52 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remains constant. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2). If an attempt is made to write to the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

FIGURE 4-1: BYTE WRITE

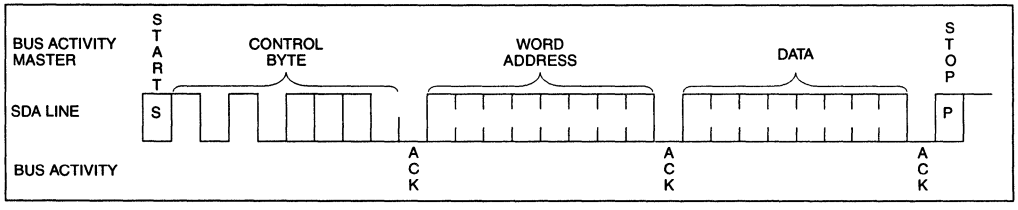
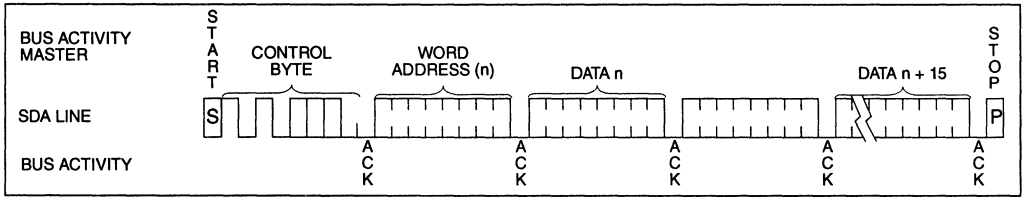


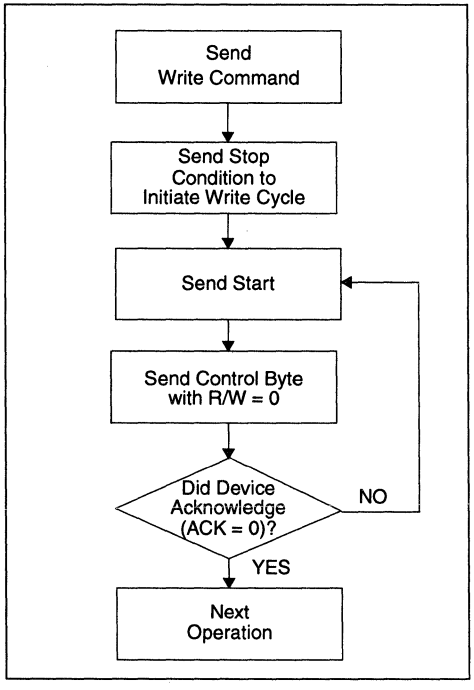
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24LCS52 has a software write protect feature that allows the lower half of the array (addresses 00h - 7Fh) to be permanently write protected, as well as a WP pin that can be used to protect the entire array.

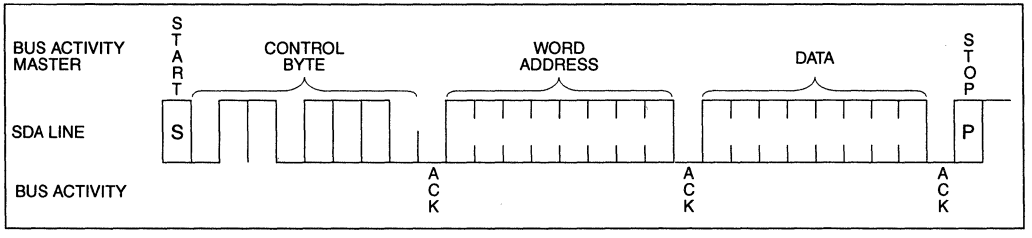
6.1 Software Write Protect

The software write protect feature is invoked by writing to the write protect register. This is done by sending a command similar to a normal write command. As shown in Figure 6-1, the write protect register is written by sending a write command with the slave address set to 0110 instead of 1010 and the address bits and data bits are don't cares. Once the software write protect register has been written, the device will not acknowledge the 0110 control byte. **Once the software write protect register has been written, the write protection is enabled and cannot be reversed, even if the device is powered down.**

6.2 Hardware Write Protect

The WP pin can be tied to Vcc, Vss, or left floating. If tied to Vcc, the entire array will be write protected, regardless of whether the software write protect register has been written or not. If the WP pin is set to Vcc, it will prevent the software write protect register from being written. If the WP is tied to Vss or left floating, then write protection is determined by the status of the software write protect register.

FIGURE 6-1: SETTING WRITE PROTECT REGISTER



7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24LCS52 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the 24LCS52 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS52 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LCS52 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LCS52 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS52 discontinues transmission (Figure 7-2). After this command, the internal address counter will point to the address location following the one that was just read.

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LCS52 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LCS52 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LCS52 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

FIGURE 7-1: CURRENT ADDRESS READ

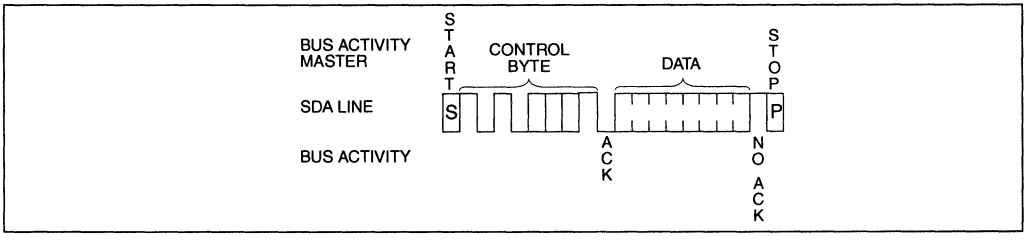


FIGURE 7-2: RANDOM READ

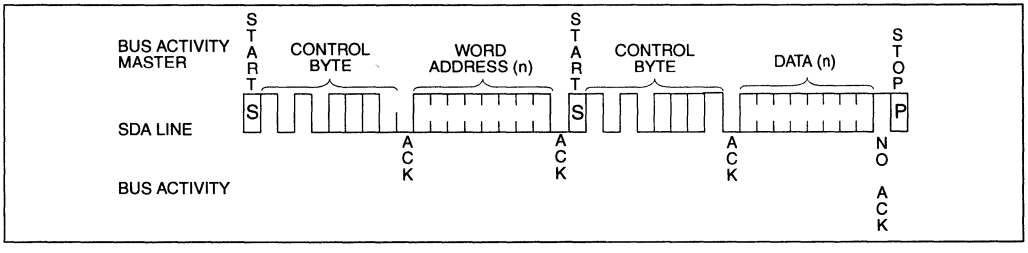
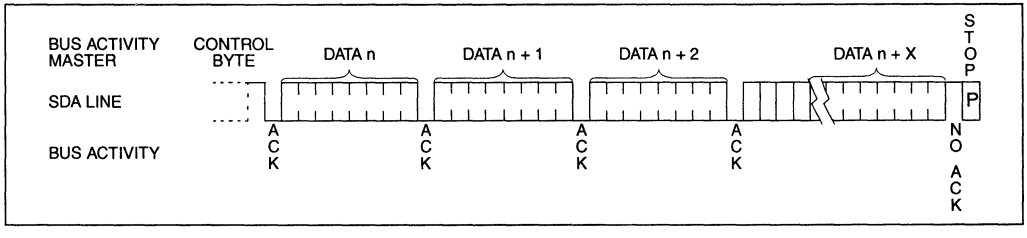


FIGURE 7-3: SEQUENTIAL READ



7.4 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24LCS52 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24LCS52 devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either Vcc or Vss.

8.4 WP

This is the hardware write protect pin. It can be tied to Vcc, Vss, or left floating. If tied to Vcc, the hardware write protection is enabled. If the WP pin is tied to Vss the hardware write protection is disabled. If the WP pin is left floating, an internal pull down resistor will pull the WP pin to Vss and the hardware write protection will be disabled.

8.5 Noise Protection

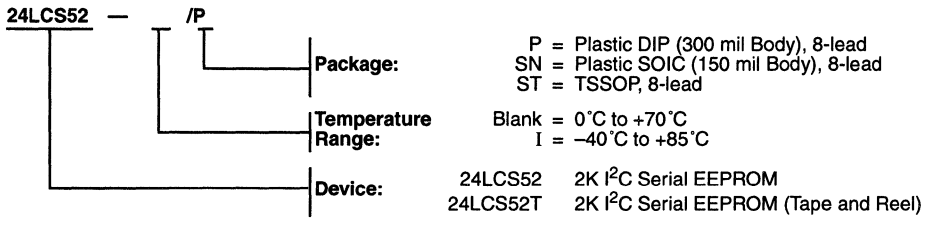
The 24LCS52 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

NOTES:

24LCS52 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC024/24LC025

2K 2.5V I²C™ Serial EEPROM

FEATURES

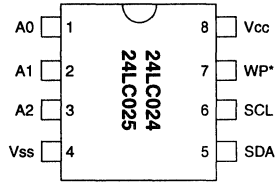
- Single supply with operation from 2.5 to 5.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as a single block of 128 bytes (256 x 8)
- Hardware write protection for entire array (24LC024)
- 2-wire serial interface bus, I²C compatible
- 100kHz and 400kHz compatibility
- Page-write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- 3.5 ms typical write cycle time for page write
- Address lines allow up to eight devices on bus
- 1,000,000 erase/write cycles guaranteed
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC or TSSOP packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

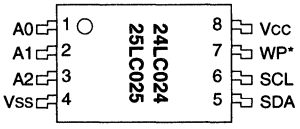
The Microchip Technology Inc. 24LC024/24LC025 is a 2K bit Serial Electrically Erasable PROM with a voltage range of 2.5V to 5.5V. The device is organized as a single block of 256 x 8-bit memory with a 2-wire serial interface. Low current design permits operation with typical standby and active currents of only 10 µA and 1 mA respectively. The device has a page-write capability for up to 16 bytes of data. Functional address lines allow the connection of up to eight 24LC024/24LC025 devices on the same bus for up to 16K bits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), and TSSOP packages.

PACKAGE TYPES

PDIP/SOIC

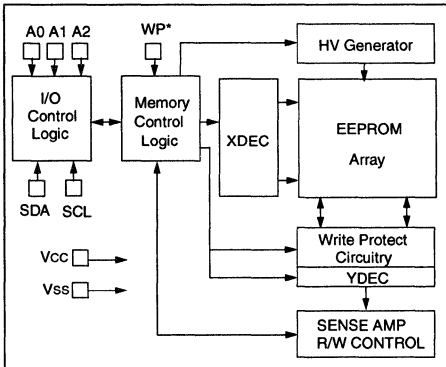


TSSOP



*WP pin available only on 24LC024. This pin has no internal connection on 24LC025

BLOCK DIAGRAM



*WP pin available only on 24LC024. This pin has no internal connection on 24LC025

3

I²C™

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write Protect (24LC024)
NC	No internal connection

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	VCC = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC		V	
Low level input voltage	VIL		0.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	0.05 VCC	—	V	(Note)
Low level output voltage	VOL		0.40	V	IOL = 3.0 mA, VCC = 4.5V IOL = 2.1 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to 5.5V, WP = VSS
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, f = 1 MHz
Operating current	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Write	—	3	mA	VCC = 5.5V
Standby current	ICCS	—	50	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS, A0, A1, A2 = VSS
Note: This parameter is periodically sampled and not 100% tested.					

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.		Vcc = 2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C					
Parameter	**Symbol**	**Vcc = 2.5V - 5.5V STD MODE**		**Vcc = 4.5V - 5.5V FAST MODE**		**Units**	**Remarks**
		Min.	**Max.**	**Min.**	**Max.**		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 C_B	250	ns	(Note 1), $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWC	—	10	—	10	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

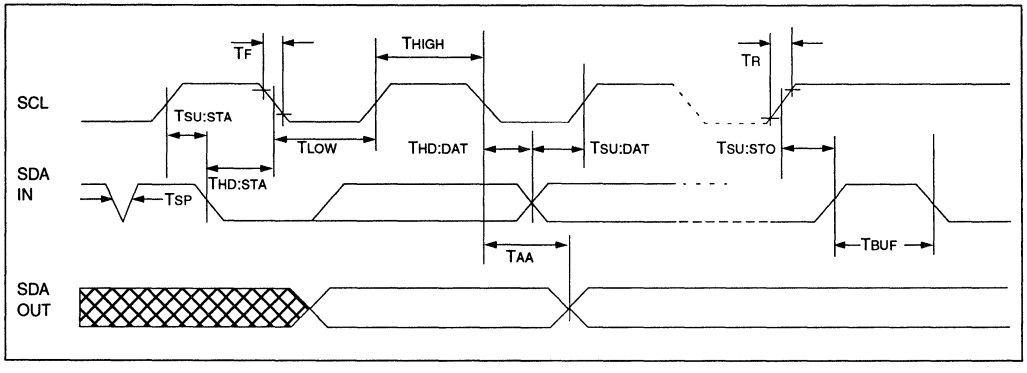
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24LC024/24LC025 devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either Vcc or Vss.

2.4 WP (24LC024 only)

This is the hardware write protect pin. It must be tied to Vcc or Vss. If tied to Vcc, the hardware write protection is enabled. If the WP pin is tied to Vss the hardware write protection is disabled. Note that the WP pin is available only on the 24LC024. This pin is not internally connected on the 24LC025.

2.5 Noise Protection

The 24LC024/24LC025 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24LC024/24LC025 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC024/24LC025 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC024/24LC025 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS

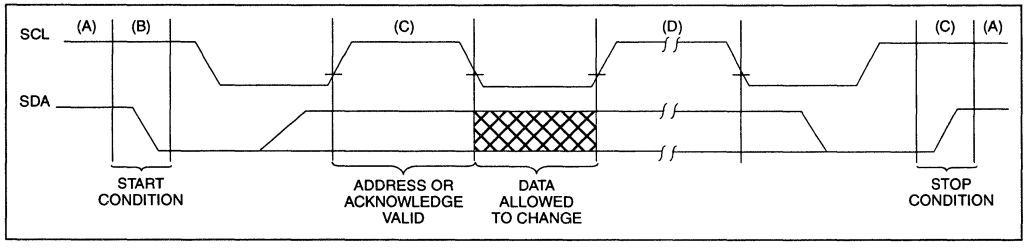
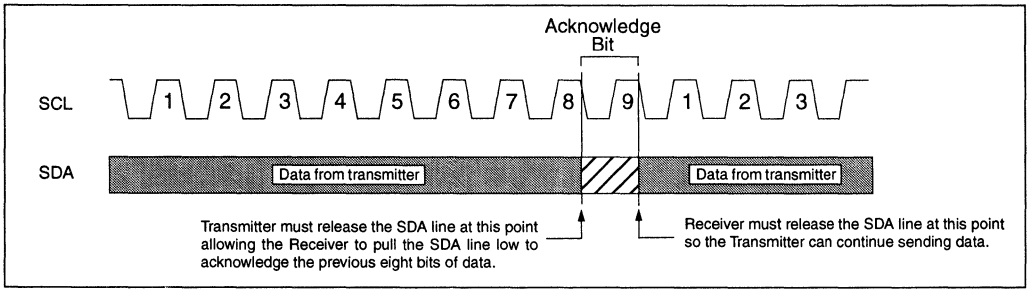


FIGURE 4-2: ACKNOWLEDGE TIMING

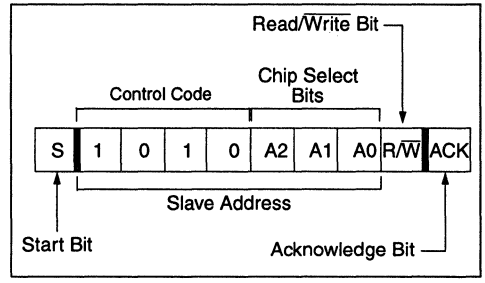


5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a four bit control code; for the 24LC024/24LC025 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24LC024/24LC025 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the start condition, the 24LC024/24LC025 monitors the SDA bus checking the control byte being transmitted. Upon receiving a 1010 code and appropriate chip select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC024/24LC025 will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24LC024/24LC025 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the device code(4 bits), the chip select bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC024/24LC025. After receiving another acknowledge signal from the 24LC024/24LC025 the master device will transmit the data word to be written into the addressed memory location. The 24LC024/24LC025 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC024/24LC025 will not generate acknowledge signals (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection (24LC024 only) has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC024/24LC025 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 15 additional data bytes to the 24LC024/24LC025 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remains constant. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

6.3 WRITE PROTECTION

The WP pin (available on 24LC024 only) must be tied to VCC or VSS. If tied to VCC, the entire array will be write protected. If the WP pin is tied to VSS, then write operations to all address locations are allowed.

FIGURE 6-1: BYTE WRITE

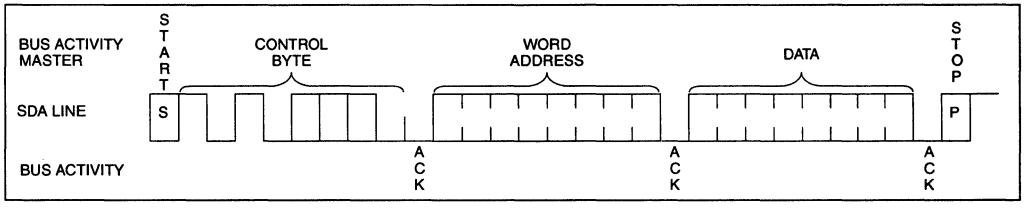
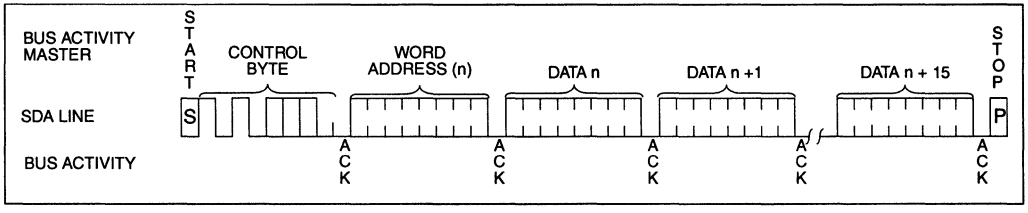


FIGURE 6-2: PAGE WRITE



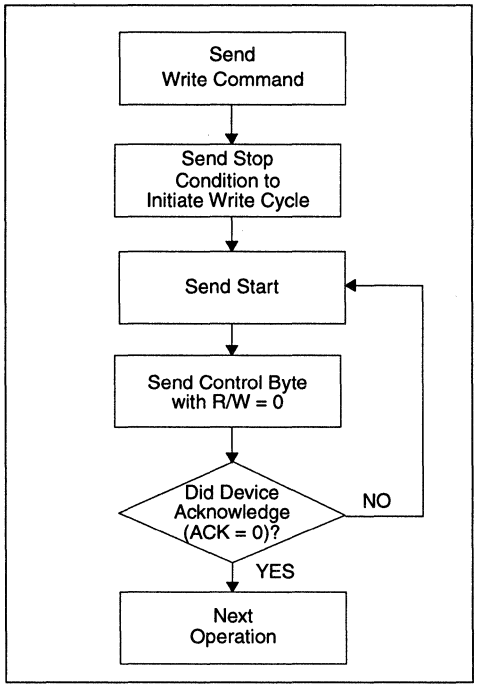
3

I²C™

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LC024/24LC025 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the 24LC024/24LC025 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC024/24LC025 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC024/24LC025 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC024/24LC025 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC024/24LC025 discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC024/24LC025 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC024/24LC025 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24LC024/24LC025 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFh to address 000h.

FIGURE 8-1: CURRENT ADDRESS READ

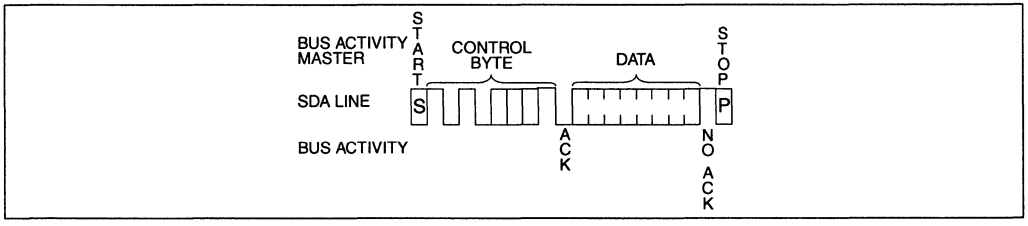


FIGURE 8-2: RANDOM READ

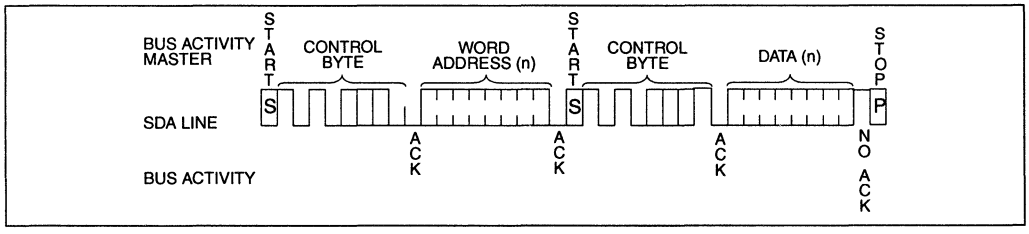
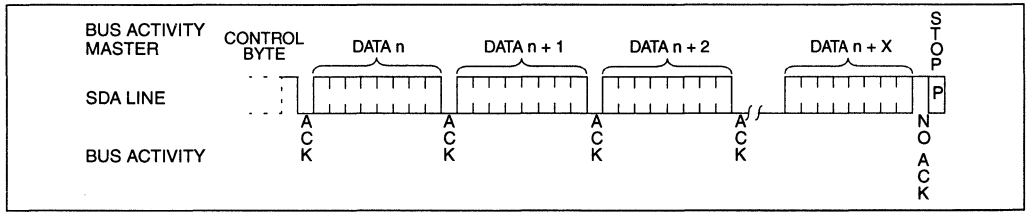
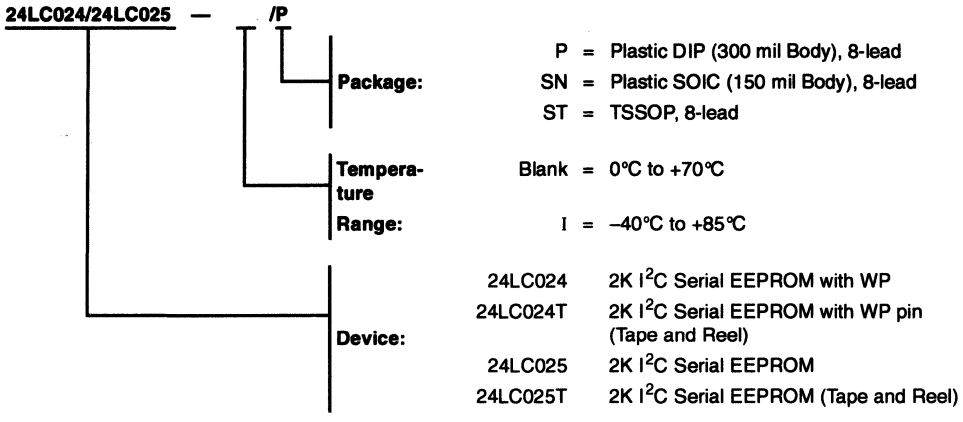


FIGURE 8-3: SEQUENTIAL READ



24LC024/24LC025 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA04/08

4K/8K 1.8V I²C™ Serial EEPROMs

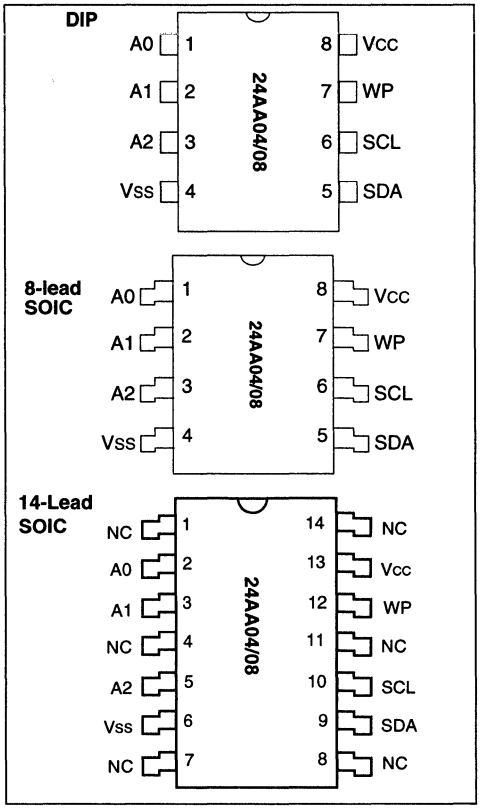
FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as 2 or 4 blocks of 256 bytes (2 x 256 x 8) or (4 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

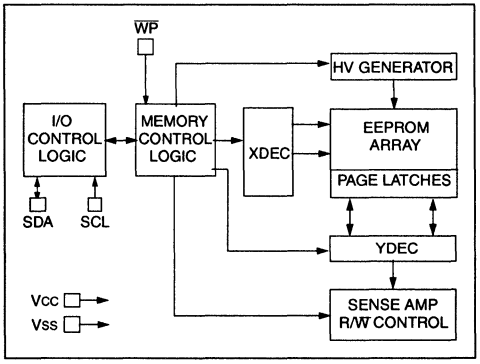
DESCRIPTION

The Microchip Technology Inc. 24AA04/08 is a 4K bit or 8K bit Electrically Erasable PROM. The device is organized as two or four blocks of 256 x 8-bit memory with a two wire serial interface. Low voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA respectively. The 24AA04/08 also has a page-write capability for up to 16 bytes of data. The 24AA04/08 is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	No Internal Connection

TABLE 1-2: DC CHARACTERISTICS

				VCC = +1.8V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:						
High level input voltage	VIH	.7 VCC	—	—	V	
Low Level input voltage	VIL	—	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	—	V	(Note)
Low level output voltage	VOL	—	—	.40	V	IOL = 3.0 mA, VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	—	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC WRITE	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.5	—	mA	VCC = 1.8V, SCL = 100 kHz
	ICC READ	—	—	1	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.05	—	mA	VCC = 1.8V, SCL = 100 kHz
Standby current	ICCS	—		100	µA	VCC = 5.5V, SDA=SCL=VCC
		—		30	µA	VCC = 3.0V, SDA=SCL=VCC
		—	3	—	µA	VCC = 1.8V, SDA=SCL=VCC WP = VSS

Note:This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

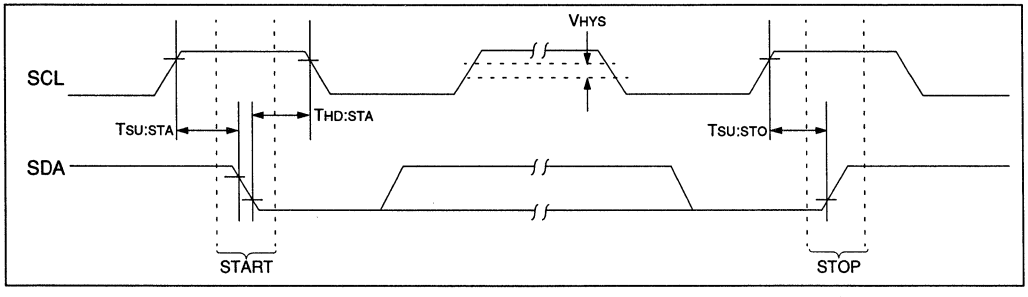
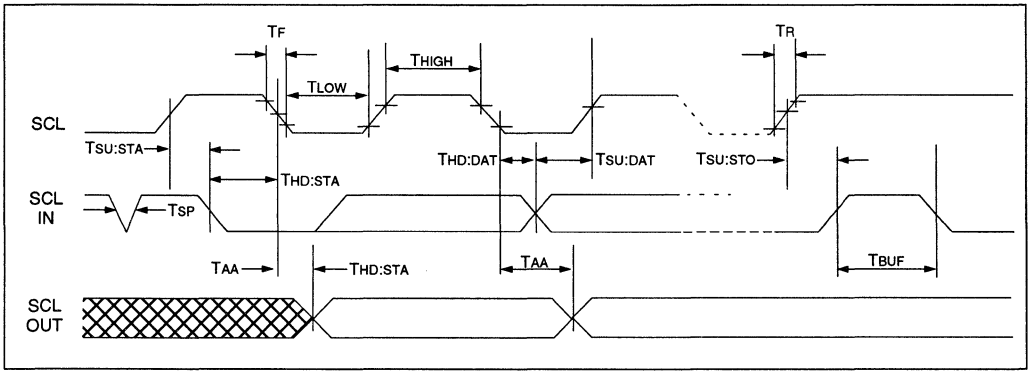


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc = 4.5-5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	Fclk	—	100	—	400	kHz	
Clock high time	Thigh	4000	—	600	—	ns	
Clock low time	Tlow	4700	—	1300	—	ns	
SDA and SCL rise time	Tr	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	Tf	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.
4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24AA04/08 supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA04/08 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

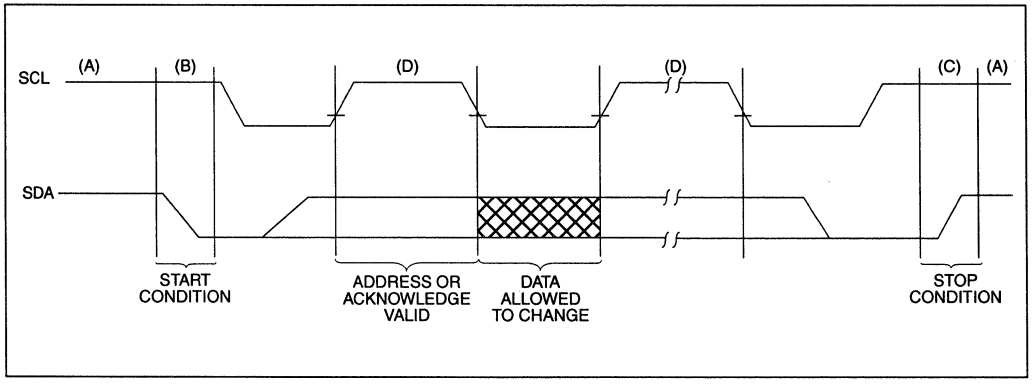
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24AA04/08 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



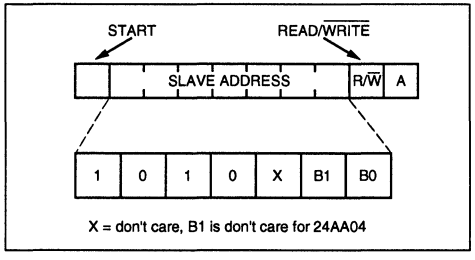
3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA04/08 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for both the 24AA04 and 24AA08; B1 is a don't care for the 24AA04. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA04/08 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA04/08 will select a read or write operation.

Operation	Control Code	Block Select	R/W
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA04/08. After receiving another acknowledge signal from the 24AA04/08 the master device will transmit the data word to be written into the addressed memory location. The 24AA04/08 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA04/08 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24AA04/08 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 16 data bytes to the 24AA04/08 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

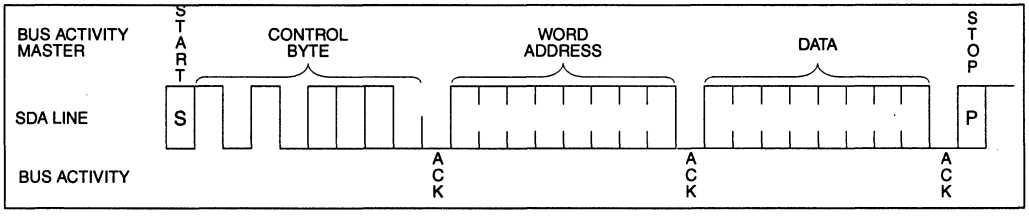
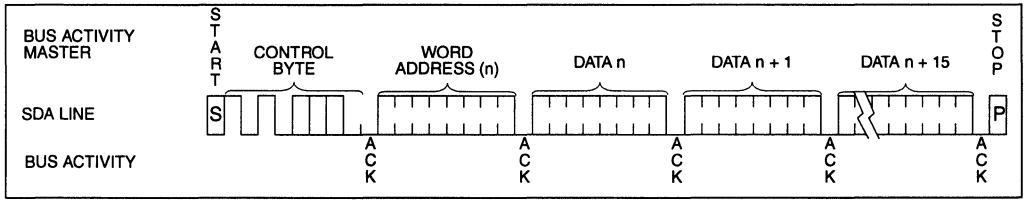


FIGURE 4-2: PAGE WRITE



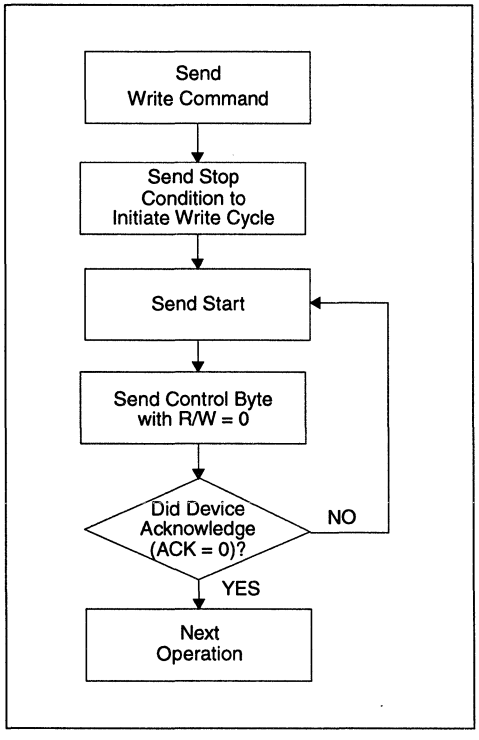
3

I²C™

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24AA04/08 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24AA04/08 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA04/08 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA04/08 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA04/08 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA04/08 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA04/08 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA04/08 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA04/08 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24AA04/08 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24AA04/08 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

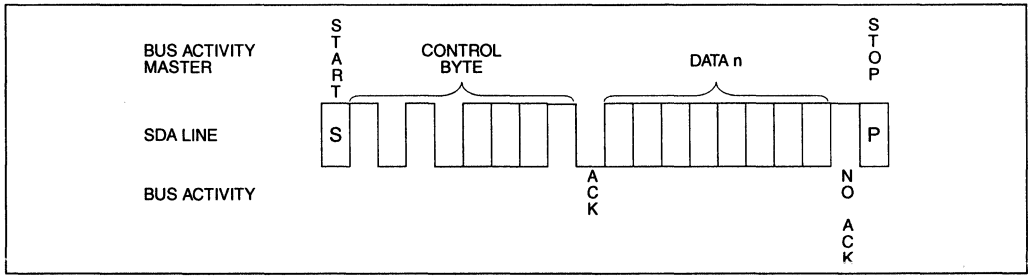


FIGURE 7-2: RANDOM READ

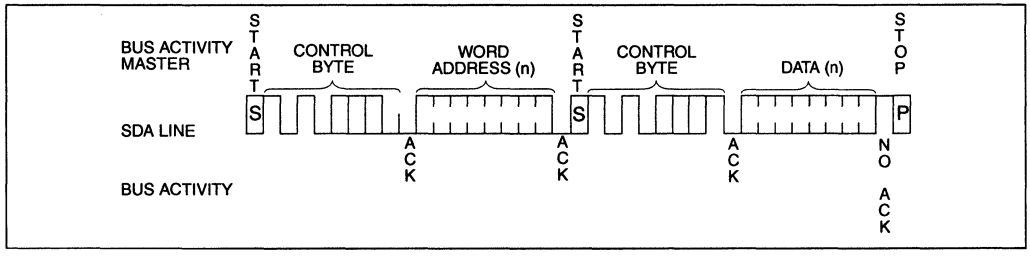
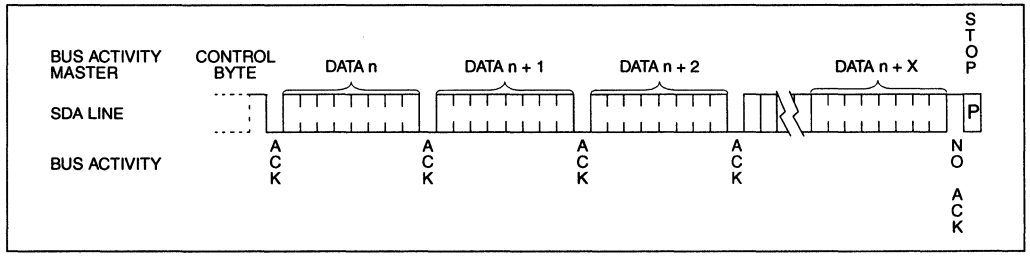


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

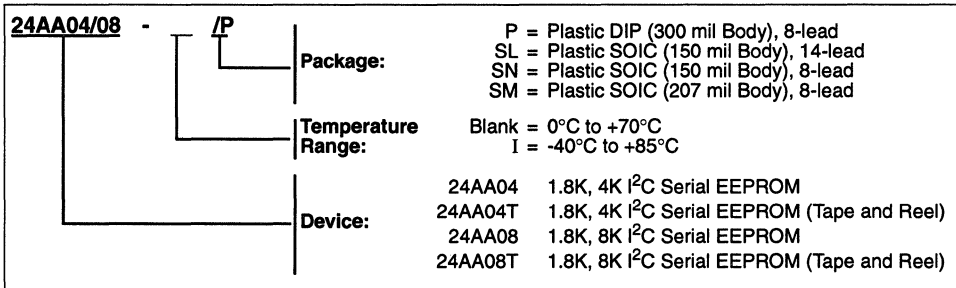
This feature allows the user to use the 24AA04/08 as a serial ROM when WP is enabled (tied to Vcc).

8.4 A0, A1, A2

These pins are not used by the 24AA04/08. They may be left floating or tied to either Vss or Vcc.

24AA04/08 Product Identification System

To order or obtain information (e.g., on pricing or delivery), please use listed part numbers, and refer to factory or listed sales offices.Sales and Support



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC04B/08B

4K/8K 2.5V I²C™ Serial EEPROMs

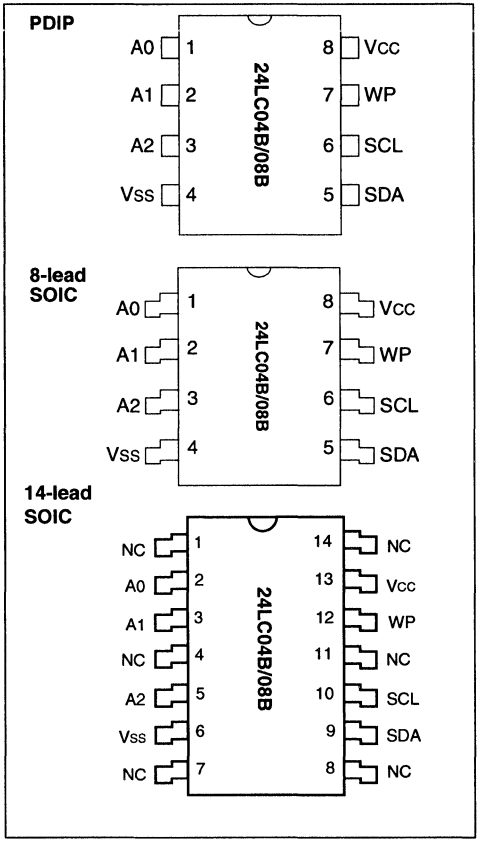
FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as two or four blocks of 256 bytes (2 x 256 x 8) and (4 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available temperature ranges:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

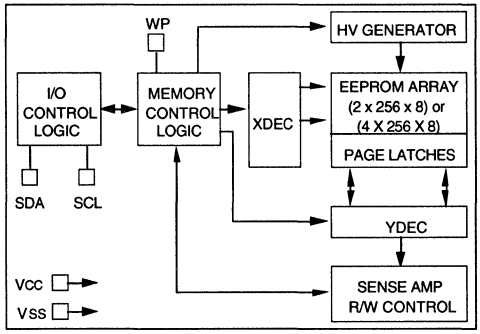
DESCRIPTION

The Microchip Technology Inc. 24LC04B/08B is a 4K or 8K bit Electrically Erasable PROM. The device is organized as two or four blocks of 256 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 2.5 volts with typical standby and active currents of only 5 µA and 1 mA respectively. The 24LC04B/08B also has a page-write capability for up to 16 bytes of data. The 24LC04B/08B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.3V to VCC + 1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

					VCC = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
Parameter	**Symbol**	**Min**	**Max**	**Units**	
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt trigger Inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE	—	3	mA	VCC = 5.5V, SCL = 400 kHz
	ICC READ	—	1	mA	
Standby current	ICCS	—	30	µA	VCC = 3.0V, SDA = SCL = VCC
		—	100	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

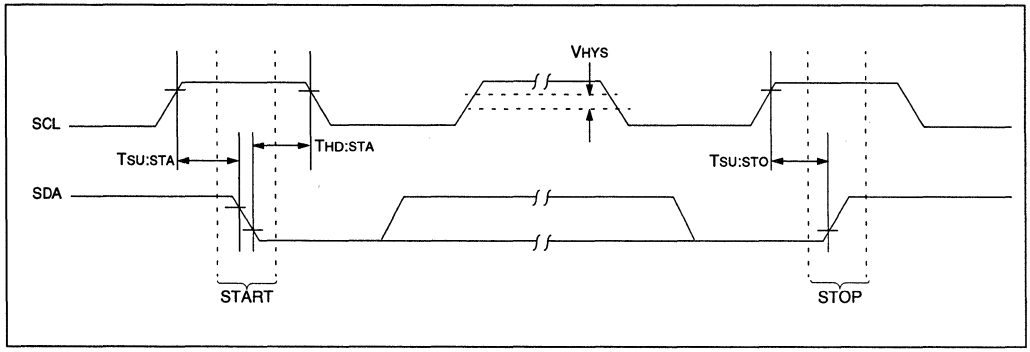


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

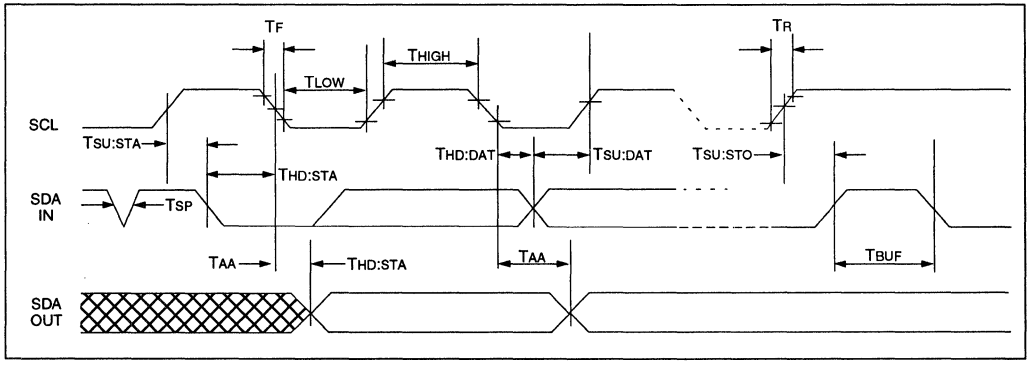
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model whcih can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24LC04B/08B supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC04B/08B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

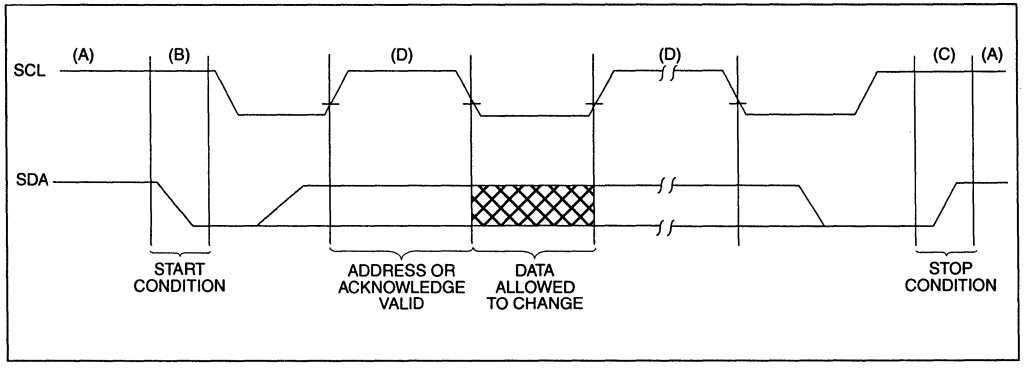
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC04B/08B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



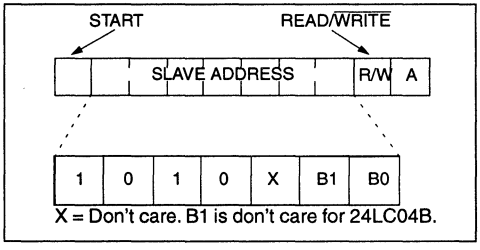
3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code, for the 24LC04B/08B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for both the 24LC04B and 24LC08B; B1 is a don't care for the 24LC04B. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC04B/08B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC04B/08B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC04B/08B. After receiving another acknowledge signal from the 24LC04B/08B the master device will transmit the data word to be written into the addressed memory location. The 24LC04B/08B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC04B/08B will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC04B/08B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC04B/08B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

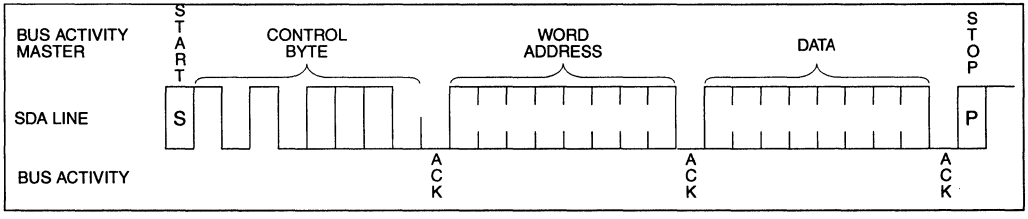
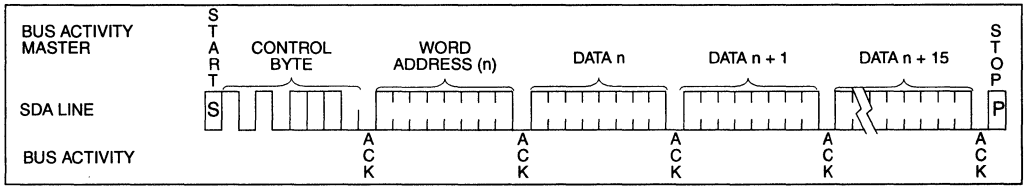


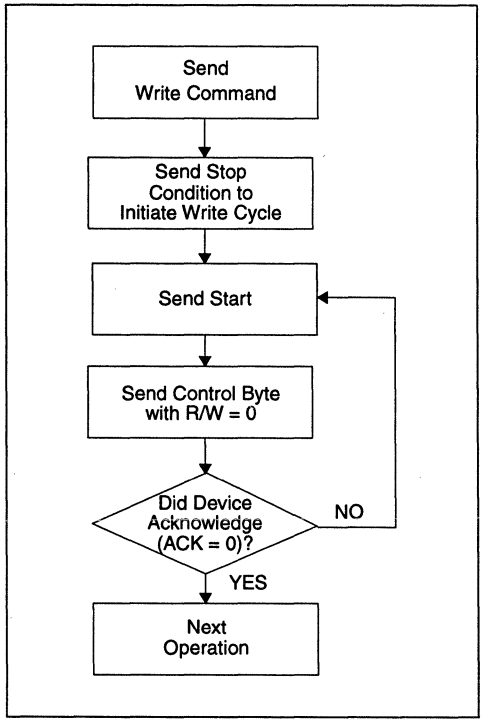
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24LC04B/08B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24LC04B/08B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC04B/08B issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC04B/08B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC04B/08B will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC04B/08B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC04B/08B to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LC04B/08B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC04B/08B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

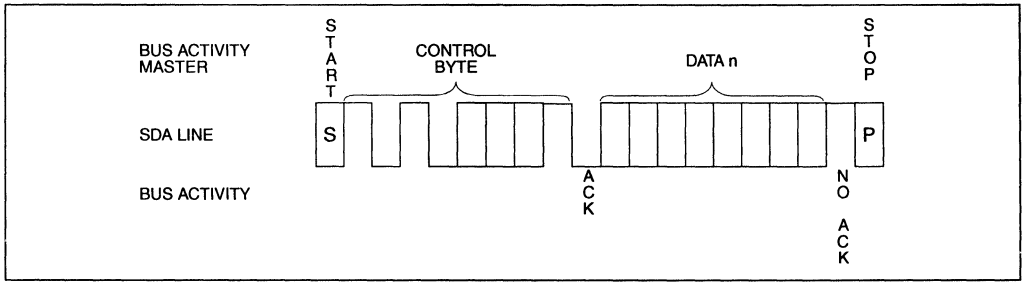


FIGURE 7-2: RANDOM READ

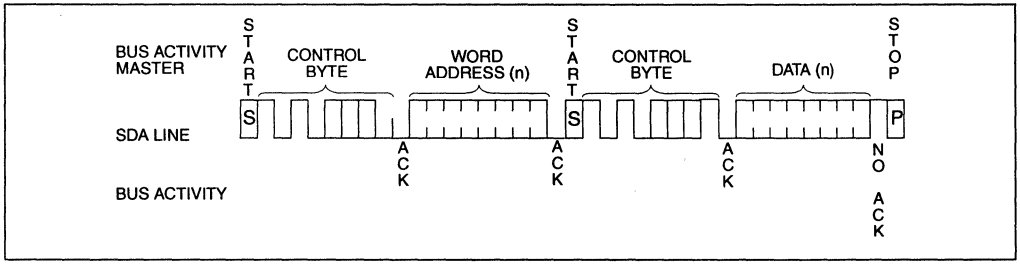
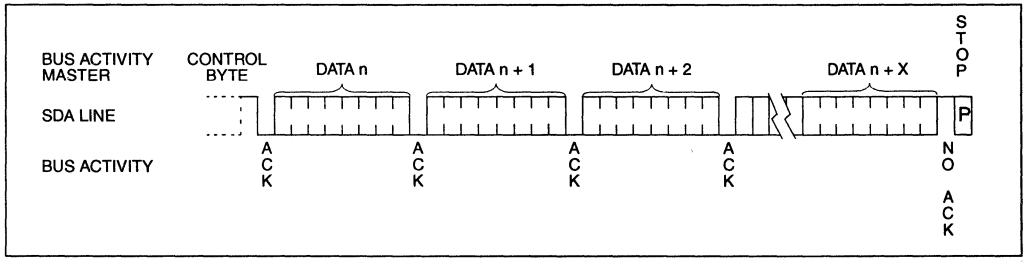


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC04B/08B as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

These pins are not used by the 24LC04B/08B. They may be left floating or tied to either VSS or VCC.

24LC04B/08B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC04B/08B – /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SM =	Plastic SOIC (207 mil Body), 8-lead
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Device:	24LC04B	4K I^2C Serial EEPROM
	24LC04BT	4K1 ^2C Serial EEPROM (Tape and Reel)
	24LC08B	8K1 ^2C Serial EEPROM
	24LC04BT	8K 1^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24C04A

4K 5.0V I²C™ Serial EEPROM

FEATURES

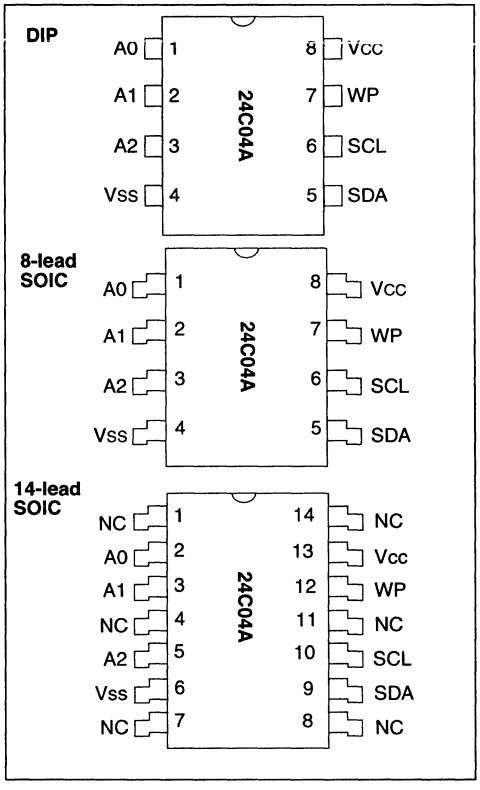
- Low power CMOS technology
- Hardware write protect
- Two wire serial interface bus, I²C™ compatible
- 5.0V only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1 ms write cycle time for single byte
- 1,000,000 Erase/Write cycles guaranteed
- Data retention >200 years
- 8-pin DIP/SOIC packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

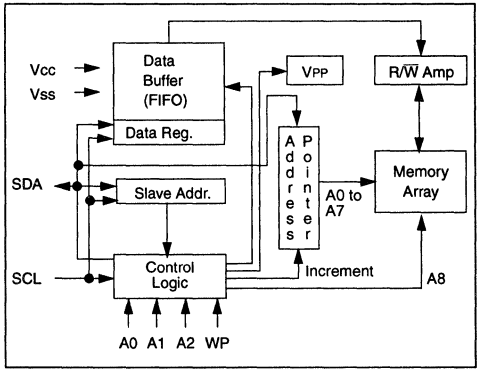
The Microchip Technology Inc. 24C04A is a 4K bit Electrically Erasable PROM. The device is organized as with a standard two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature provides hardware write protection for the upper half of the block. The 24C04A has a page write capability of up to eight bytes, and up to four 24C04A devices may be connected to the same two wire bus.

This device offers fast (1ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 24LC04B.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0	No Function - Must be connected to VCC or VSS
A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

VCC = +5V (±10%)		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C			
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI	—	10	µA	VIN = 0V to VCC
Output leakage current	ILO	—	10	µA	VOUT = 0V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7.0	pF	VIN/VOUT = 0V (Note) Tamb = +25°C, f = 1 MHz
Operating current	ICC Write	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = 0°C to +70°C
	ICC Write	—	4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = (I) and (E)
	ICC Read	—	750	µA	VCC = 5V, Tamb= (C), (I) and (E)
Standby current	ICCS	—	100	µA	SDA=SCL=VCC=5V (no PROGRAM active) WP/TEST = VSS, A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested

FIGURE 1-1: BUS TIMING START/STOP

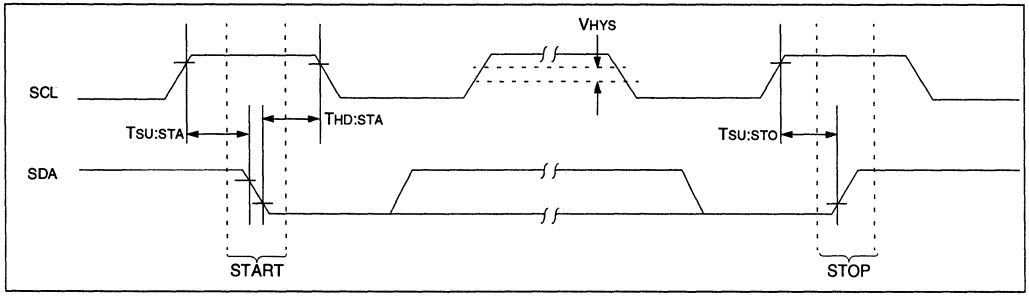


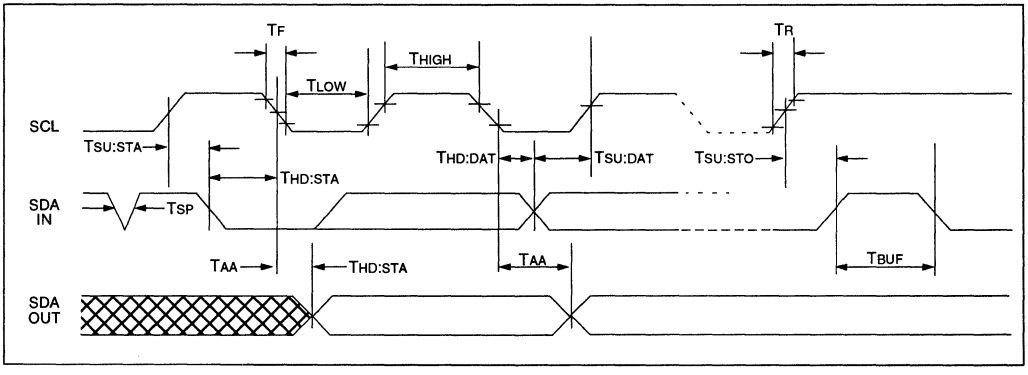
TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min.	Typ	Max.	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	TR	—	—	1000	ns	
SDA and SCL fall time	TF	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TAA	300	—	3500		(Note 1)
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI	—	—	100	ns	
Program cycle time	TWC	—	.4 .4N	1 N	ms ms	Byte mode Page mode, N=# of bytes
Endurance	—	1M	—	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24C04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C04A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 24C04As can be connected to the bus, selected by A1 and A2 chip address inputs. A0 must be tied to VCC or VSS.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

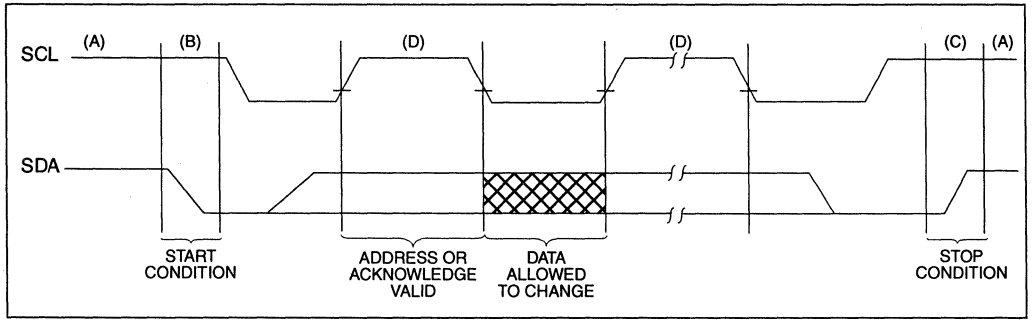
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24C04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



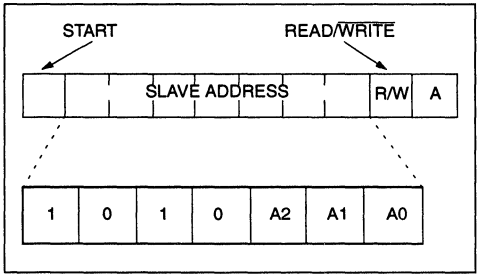
4.0 SLAVE ADDRESS

The chip address inputs A1 and A2 must be externally connected to either Vcc or ground (Vss), thereby assigning a unique address to each device. A0 is not used on the 24C04A and must be connected to either Vcc or Vss. Up to four 24C04A devices may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hard-wired logic levels of the selected 24C04A. After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010), followed by the chip address bits A0, A1 and A2. The seventh bit of that byte (A0) is used to select the upper block (addresses 100—1FF) or the lower block (addresses 000—0FF) of the array.

The eighth bit of the slave address determines if the master device wants to read or write to the 24C04A (Figure 4-1).

The 24C04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 4-1: SLAVE ADDRESS ALLOCATION



5.0 BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C04A.

Following the START signal from the master, the device code (4-bits), the slave address (3-bits), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C04A. After receiving the acknowledge, the master device transmits the data word to be written into the addressed memory location. The 24C04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle (Figure 6-1).

6.0 PAGE PROGRAM MODE

To program the master sends addresses and data to the 24C04A which is the slave (Figure 6-1 and Figure 6-2). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The A0 bit transmitted with the slave address is the ninth bit of the address pointer). The 24C04A will generate an acknowledge after every 8-bits received and store them consecutively in a RAM (8 bytes maximum) buffer until a STOP condition is detected. This STOP condition initiates the internal programming cycle.. If more than 8 bytes are transmitted by the master, the 24C04A will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 6-1), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received data bytes in the page buffer will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes.

FIGURE 6-1: BYTE WRITE

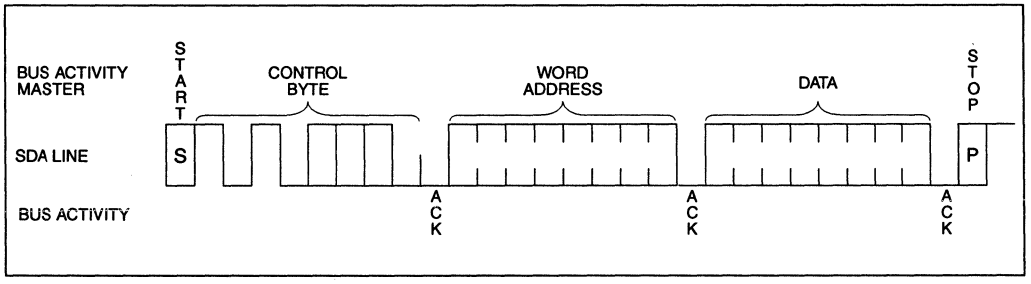
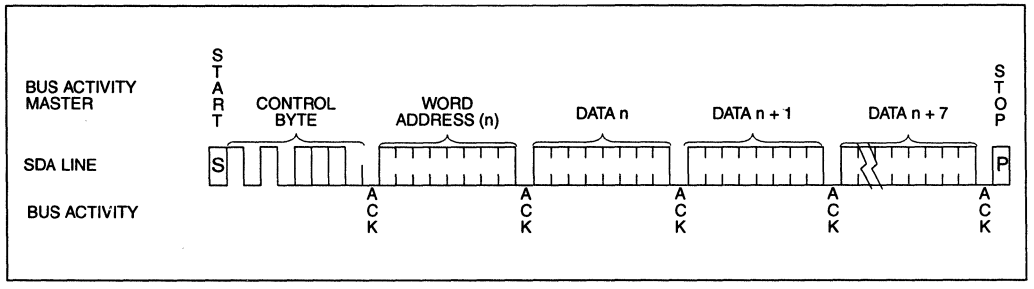


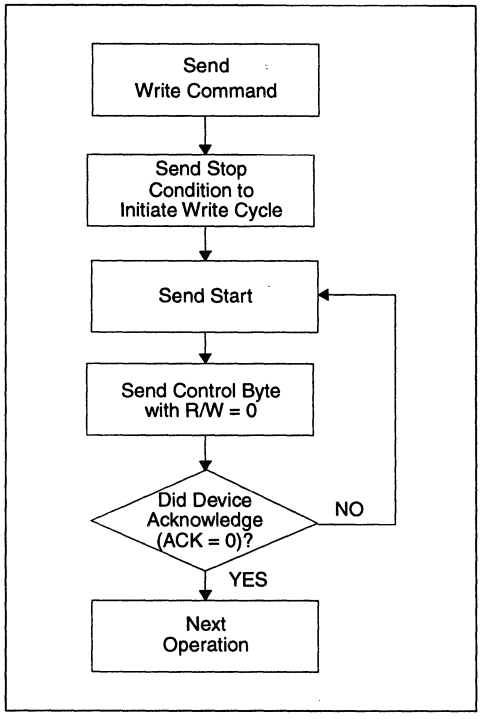
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin is connected to VCC (+5.0V). The device will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted.

9.0 READ MODE

In this mode the 24C04A transmits data to the master devide.

As can be seen from Figure 9-2 and Figure 9-3, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to). During this period the 24C04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This auto-increment sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note 1: If the master knows where the address pointer is, it can begin the read sequence at the current address (Figure 9-1) and save time transmitting the slave and word addresses.

Note 2: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

FIGURE 9-1: CURRENT ADDRESS READ

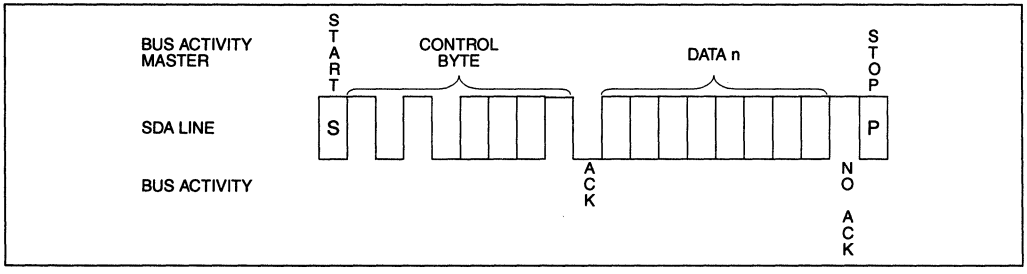


FIGURE 9-2: RANDOM READ

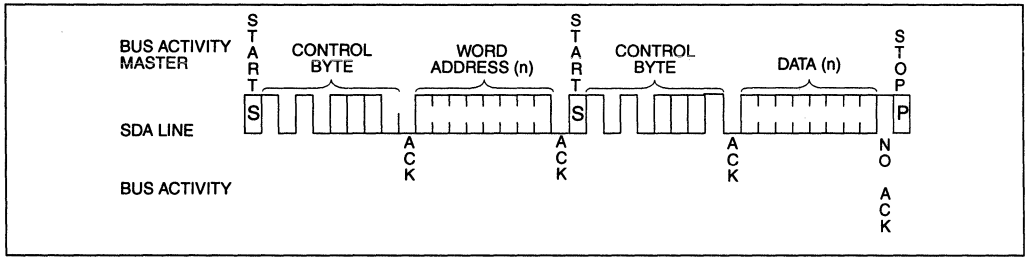
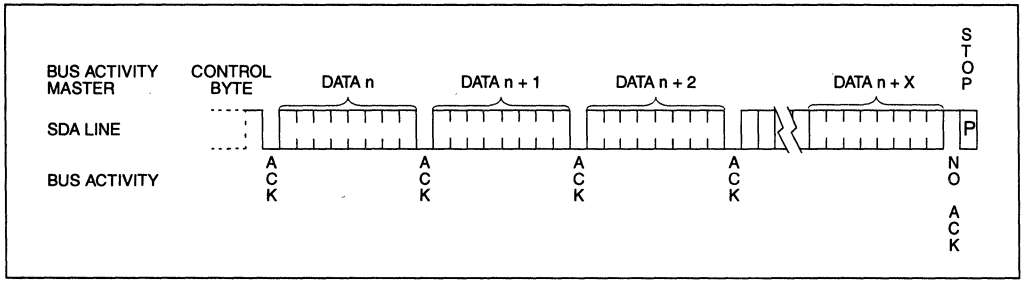


FIGURE 9-3: SEQUENTIAL READ



10.0 PIN DESCRIPTION

10.1 A0, A1, A2 Chip Address Inputs

A0 is not used as a chip select bit and must be tied to either Vss or Vcc. The levels on the remaining two address inputs(A1, A2) are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. These inputs must be connected to either Vss or Vcc.

These two address inputs allow up to four 24C04A's can be connected to the bus

10.2 SDA Serial Address/Data Input/ Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10KΩ).

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

10.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

10.4 WP Write Protection

This pin must be connected to either Vcc or Vss. If tied to Vcc, write operations to the upper memory block will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

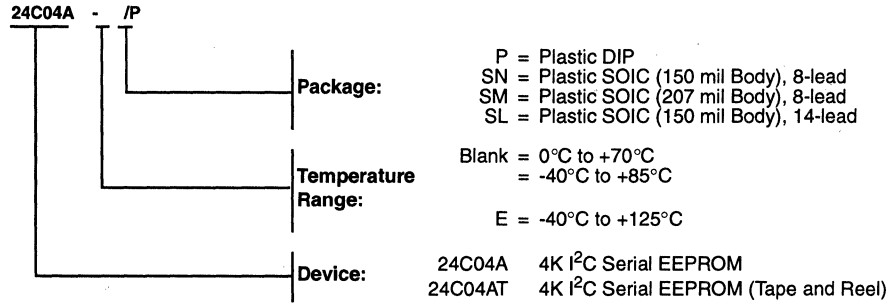
This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Note 1: A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long.

Note 2: A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C04A has two blocks, 256 bytes each.

24C04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24C08B/16B

8K/16K 5.0V I²C™ Serial EEPROMs

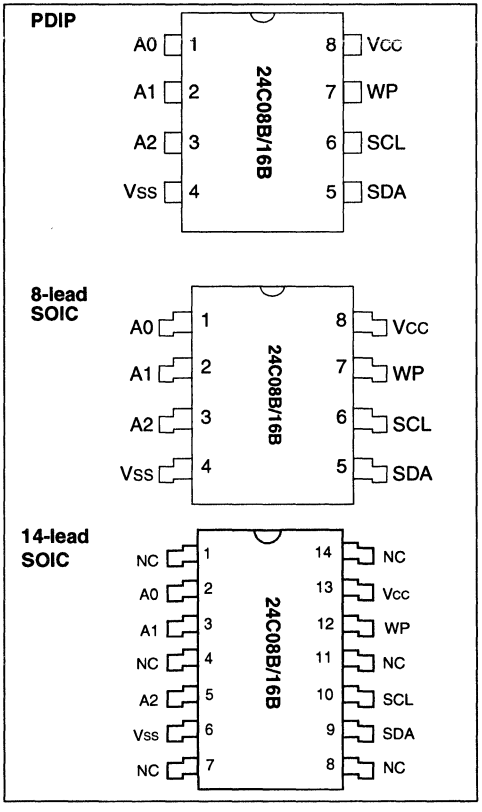
FEATURES

- Single supply with operation from 4.5-5.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as 4 or 8 blocks of 256 bytes (4 x 256 x 8) or (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection > 4,000V
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature range
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

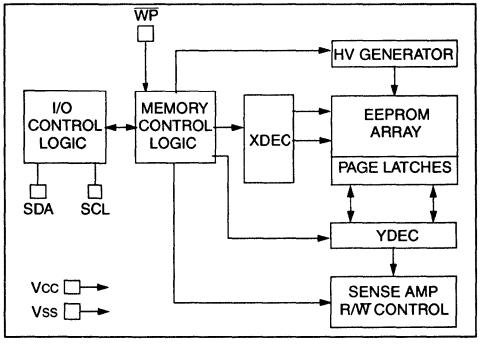
DESCRIPTION

The Microchip Technology Inc. 24C08B/16B is an 8K or 16K bit Electrically Erasable PROM intended for use in extended/automotive temperature ranges. The device is organized as four or eight blocks of 256 x 8-bit memory with a 2-wire serial interface. The 24C08B/16B also has a page-write capability for up to 16 bytes of data. The 24C08B/16B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+4.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low Level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, VCC=4.5V
Input leakage current	ILI	-10	10	µA	VIN =.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK=1 MHz
Operating current	ICC write ICC read	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	100	µA	VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

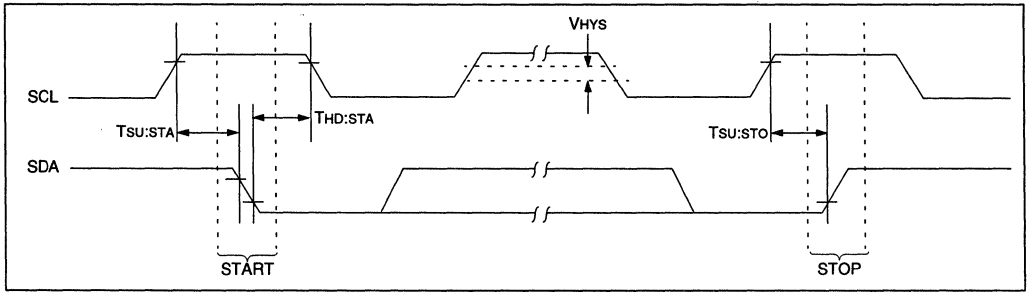
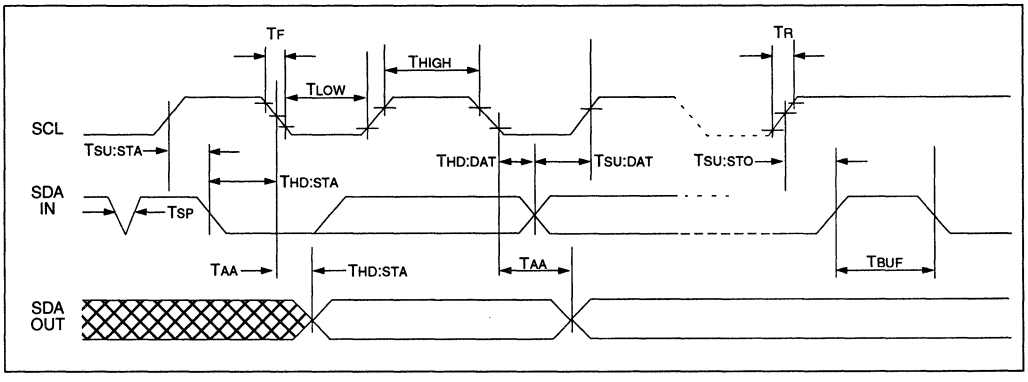


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Remarks
Clock frequency	FCLK	—	100	kHz	
Clock high time	THIGH	4000	—	ns	
Clock low time	TLOW	4700	—	ns	
SDA and SCL rise time	TR	—	1000	ns	(Note1)
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	ns	
Data input setup time	TSU:DAT	250	—	ns	
STOP condition setup time	TSU:STO	4000	—	ns	
Output valid from clock	TAA	—	3500	ns	(Note 2)
Bus free time	TBUF	4700	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	ms	Byte or Page mode
Endurance	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification.
4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24C08B/16B supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C08B/16B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

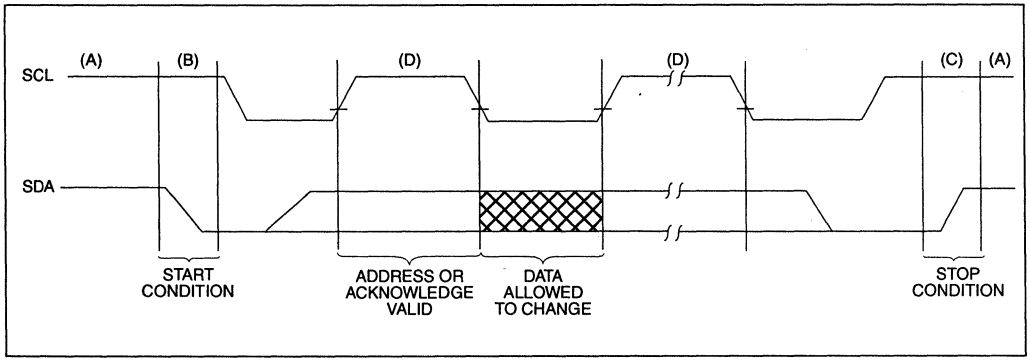
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24C08B/16B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C08B/16B) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



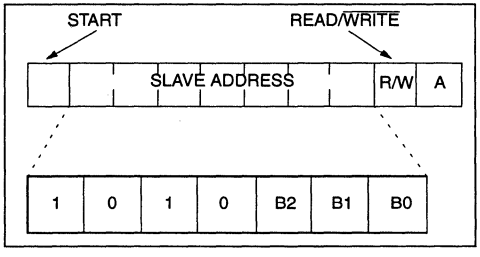
3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code, for the 24C08B/16B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24C08B/16B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C08B/16B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C08B/16B. After receiving another acknowledge signal from the 24C08B/16B the master device will transmit the data word to be written into the addressed memory location. The 24C08B/16B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C08B/16B will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C08B/16B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24C08B/16B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

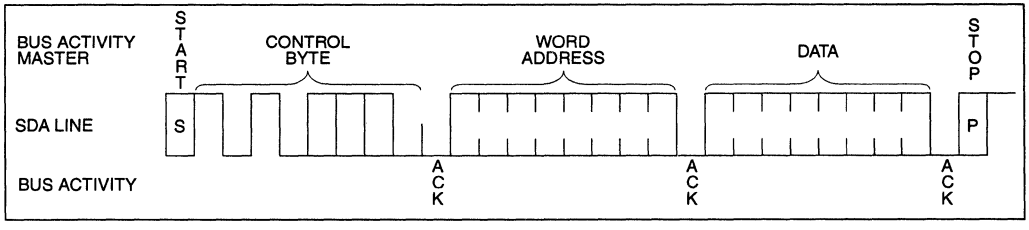
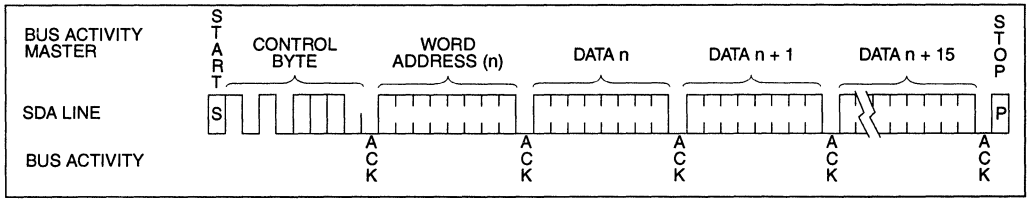


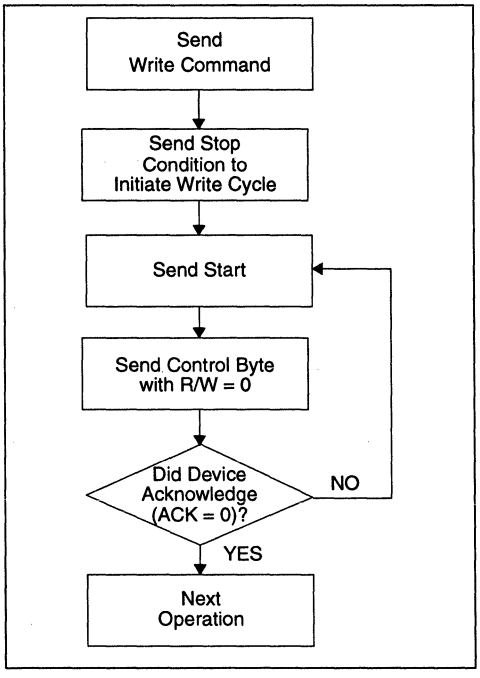
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24C08B/16B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24C08B/16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C08B/16B issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C08B/16B discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C08B/16B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C08B/16B will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C08B/16B discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C08B/16B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C08B/16B to transmit the next sequentially addressed 8 bit word (Figure 7-3).

To provide sequential reads the 24C08B/16B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24C08B/16B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

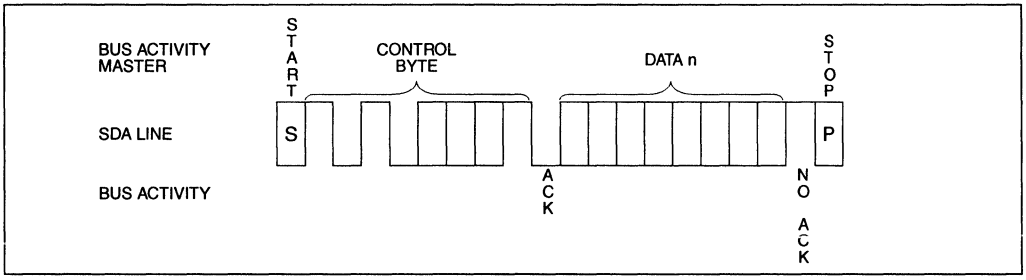


FIGURE 7-2: RANDOM READ

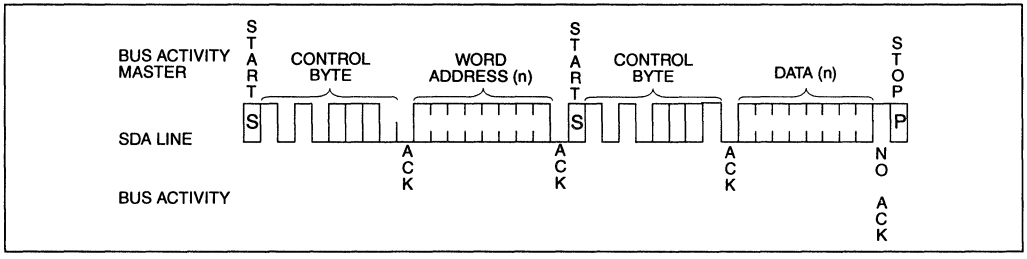
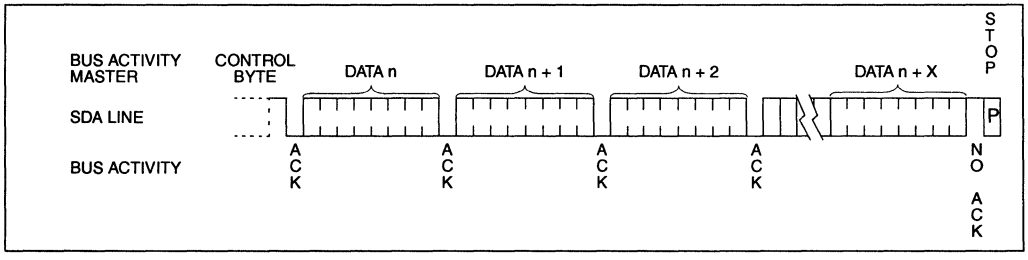


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24C08B/16B as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

These pins are not used by the 24C08B/16B. They may be left floating or tied to either VSS or VCC.

24C08B/16B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24C08B/16B – E /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
	E =	-40°C to +125°C
Device:	24C08B	8K I^2C Serial EEPROM
	24C08BT	8K I^2C Serial EEPROM (Tape and Reel)
	24C16B	16K I^2C Serial EEPROM
	24C16BT	16K I^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA16

16K 1.8V I²C™ Serial EEPROM

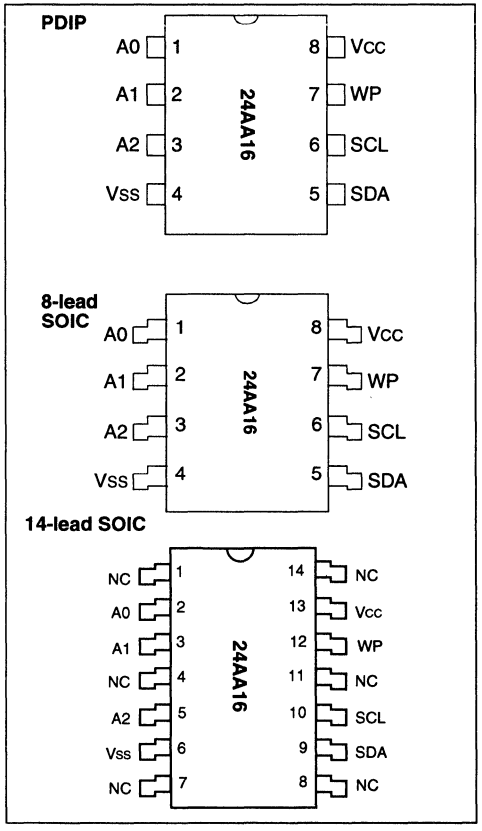
FEATURES

- Singie supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection > 4,000V
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

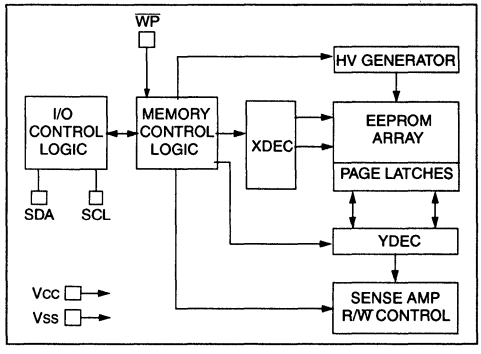
DESCRIPTION

The Microchip Technology Inc. 24AA16 is a 1.8 volt 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA, respectively. The 24AA16 also has a page-write capability for up to 16 bytes of data. The 24AA16 is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	No Internal Connection

TABLE 1-2: DC CHARACTERISTICS

			VCC = 1.8V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:						
High level input voltage	VIH	.7 VCC		—	V	
Low level input voltage	VIL	—		.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC		—	V	(Note)
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA, VCC = 1.8V
Input leakage current	ILI	-10		10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10		10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—		10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.5	—	mA	VCC = 1.8V, SCL = 100 kHz
	ICC Read	—	—	1	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.05	—	mA	VCC = 1.8V, SCL = 100 kHz
Standby current	ICCS	—	—	100	µA	VCC = 5.5V, SDA=SCL=VCC
		—	—	30	µA	VCC = 3.0V, SDA=SCL=VCC
		—	3	—	µA	VCC = 1.8V, SDA=SCL=VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

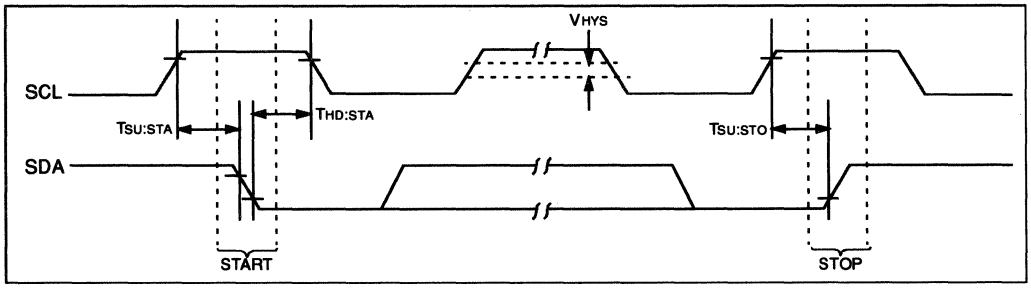
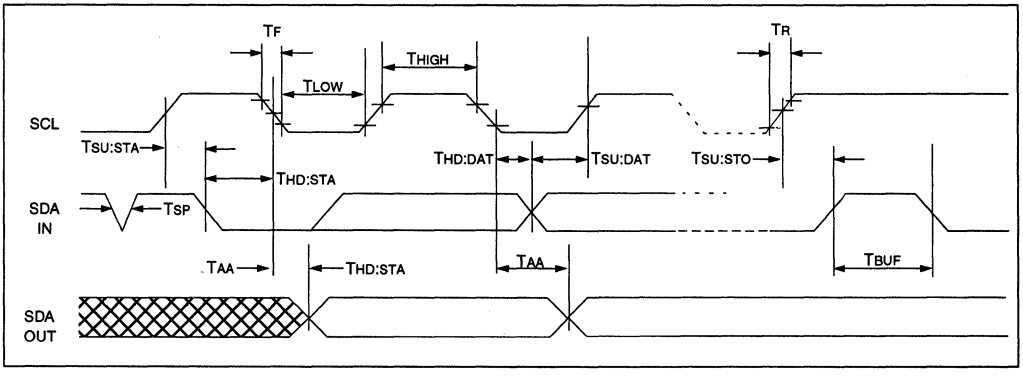


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5-5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions
3: The combined TSP and VHYS =specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.
4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA16 supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA16 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

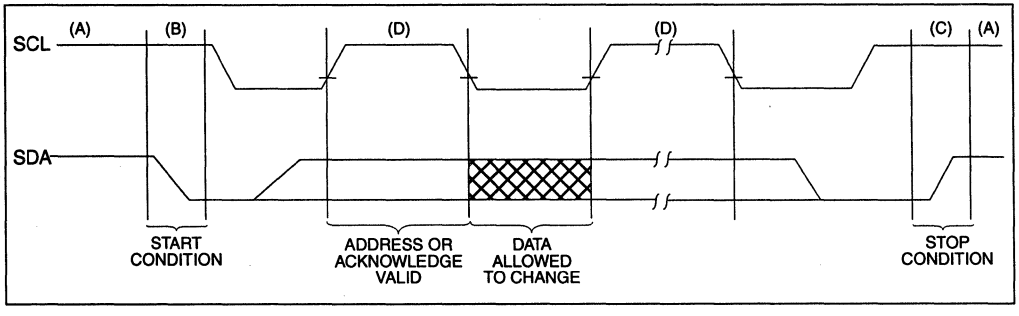
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA16 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



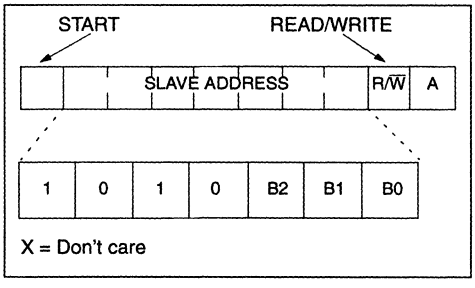
3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code, for the 24AA16 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24AA16 per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA16 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA16 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA16. After receiving another acknowledge signal from the 24AA16 the master device will transmit the data word to be written into the addressed memory location. The 24AA16 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA16 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA16 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24AA16 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

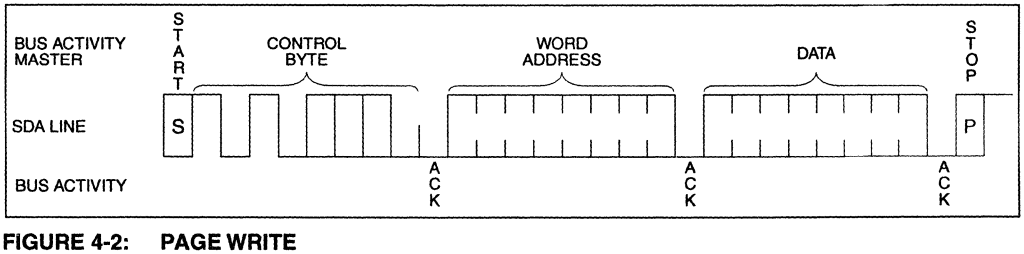
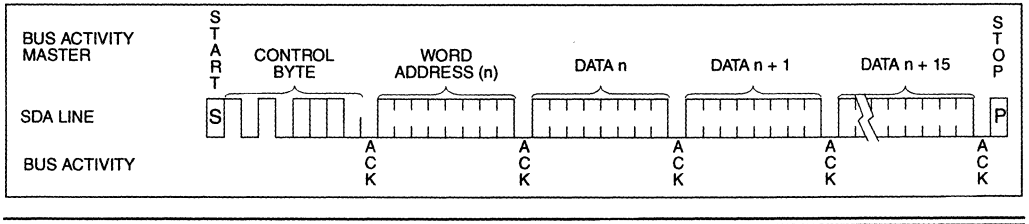


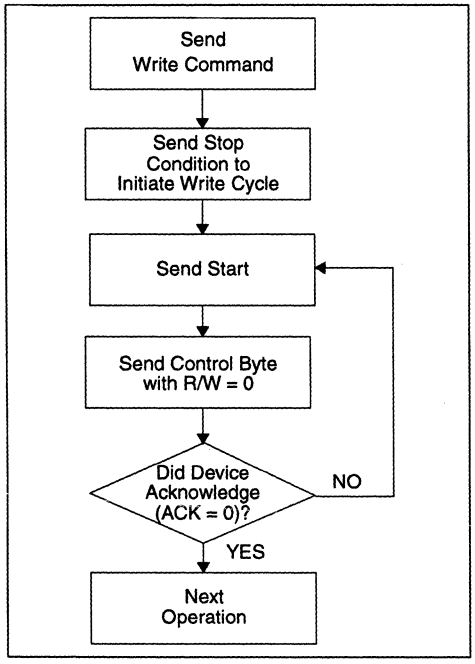
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24AA16 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24AA16 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA16 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA16 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA16 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA16 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA16 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA16 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA16 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24AA16 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24AA16 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

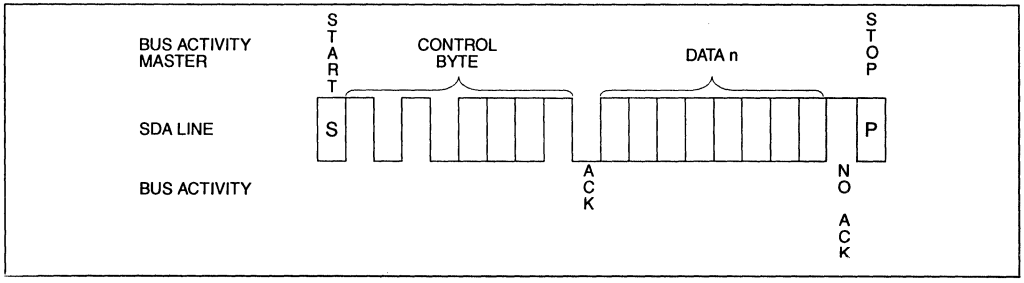


FIGURE 7-2: RANDOM READ

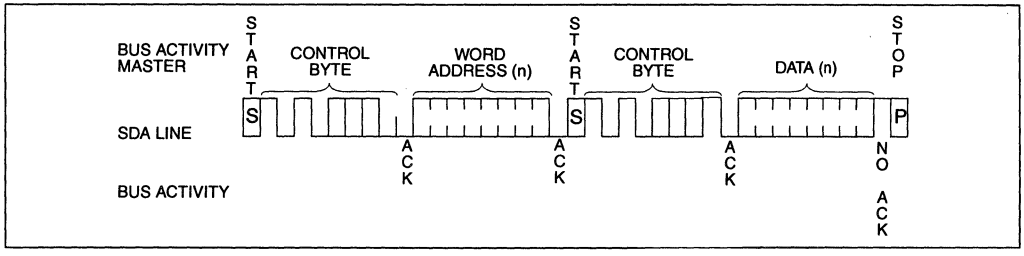
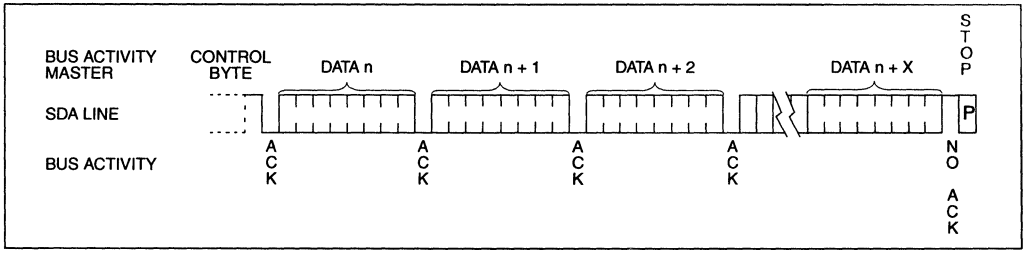


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz) from 24LC04B/08B.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

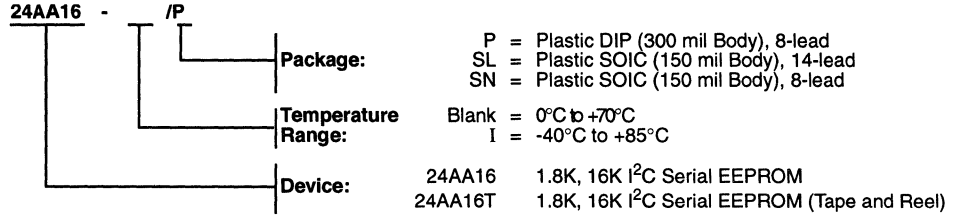
This feature allows the user to use the 24AA16 as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

These pins are not used by the 24AA16. They may be left floating or tied to either VSS or VCC.

24AA16 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24LC16B

16K 2.5V I²C™ Serial EEPROM

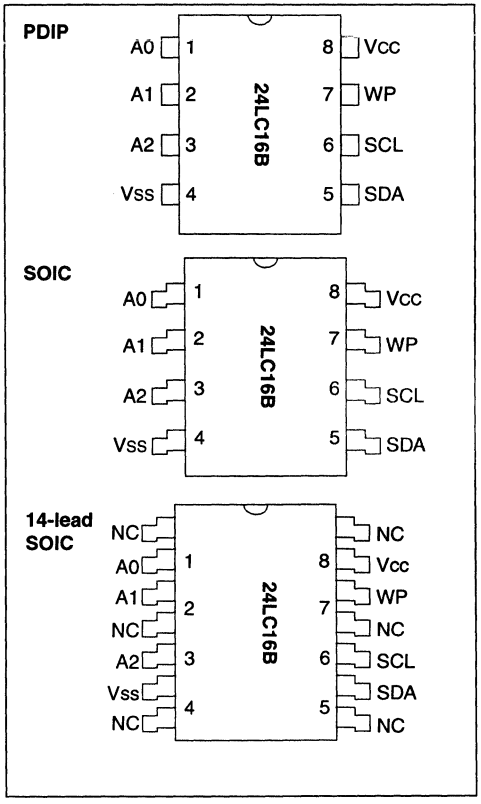
FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

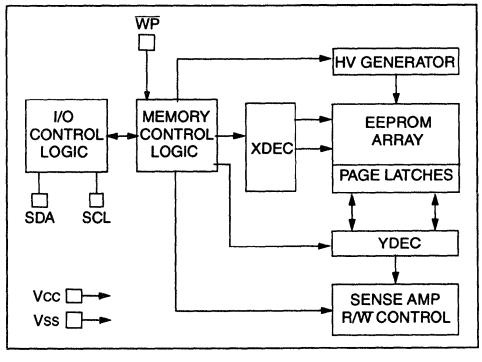
DESCRIPTION

The Microchip Technology Inc. 24LC16B is a 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8 bit memory with a 2-wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC16B also has a page-write capability for up to 16 bytes of data. The 24LC16B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.3V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	No Internal Connection

TABLE 1-2: DC CHARACTERISTICS

			VCC = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, FCLK = 1MHz
Operating current	ICC write ICC read	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

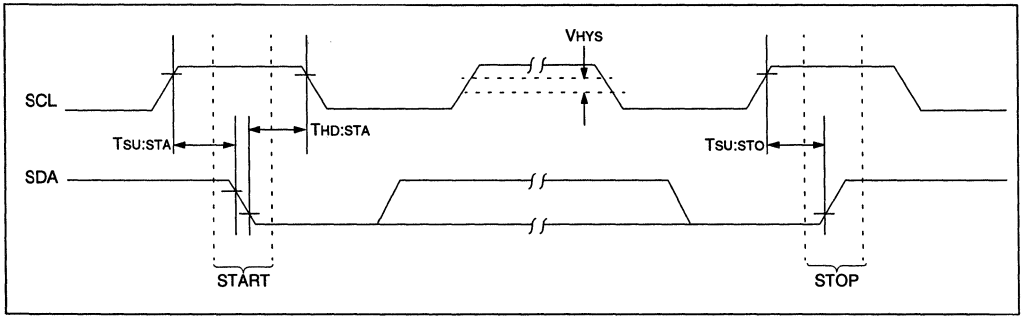


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5V - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

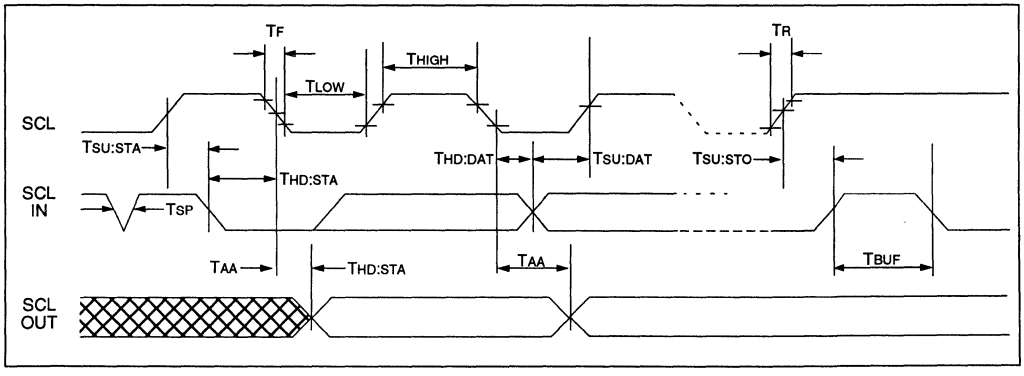
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC16B supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC16B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

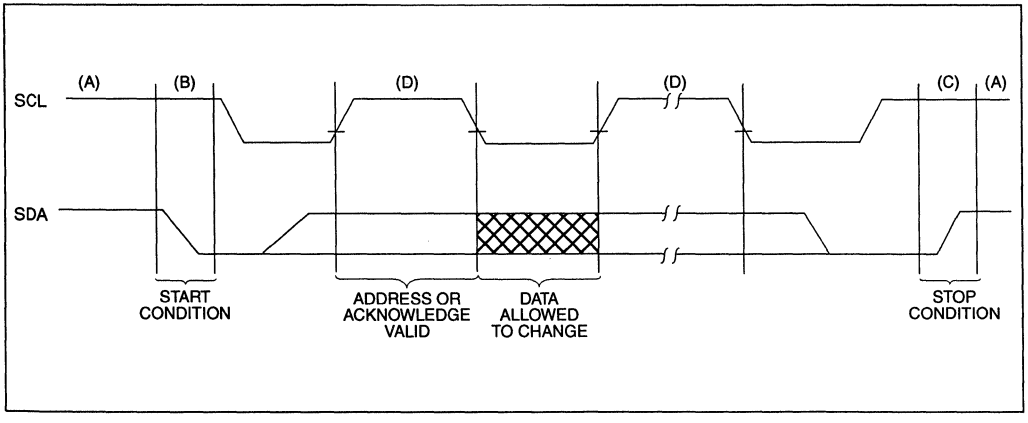
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC16B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC16B) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



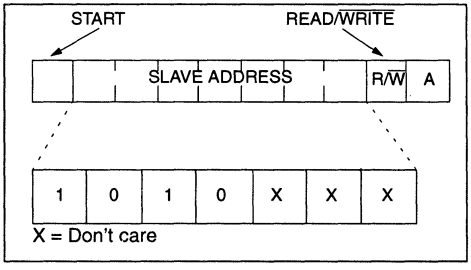
3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC16B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24LC16B per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC16B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC16B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC16B. After receiving another acknowledge signal from the 24LC16B the master device will transmit the data word to be written into the addressed memory location. The 24LC16B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC16B will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC16B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC16B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

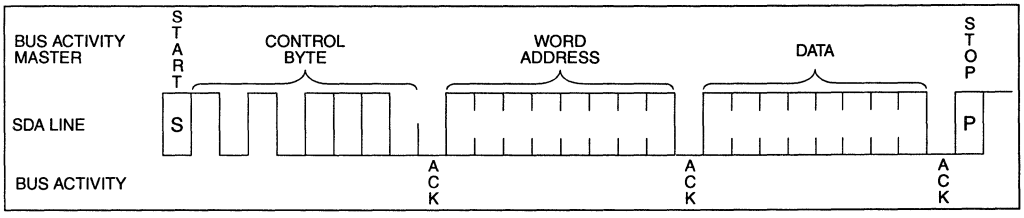
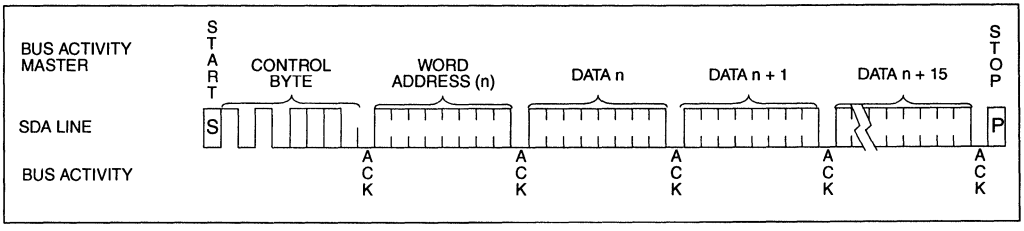


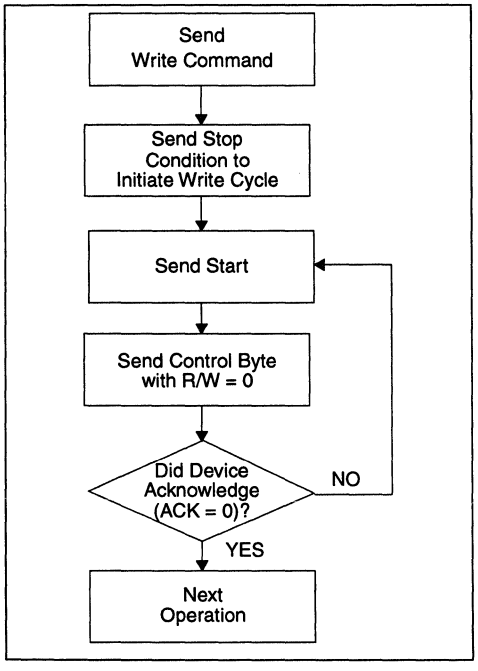
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24LC16B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24LC16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC16B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC16B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC16B will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC16B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC16B to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LC16B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC16B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

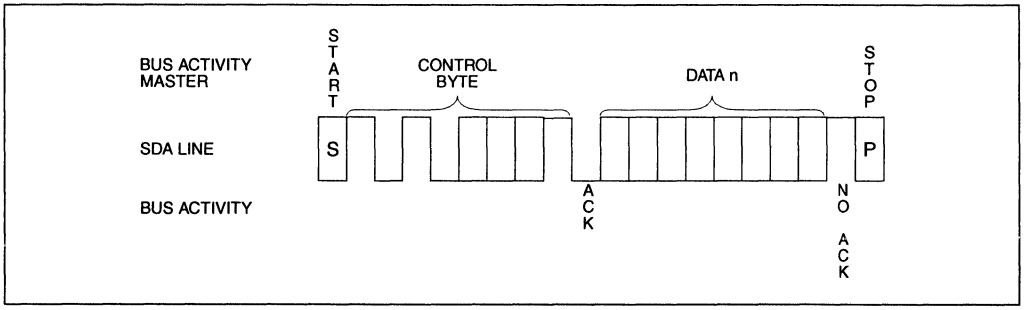


FIGURE 7-2: RANDOM READ

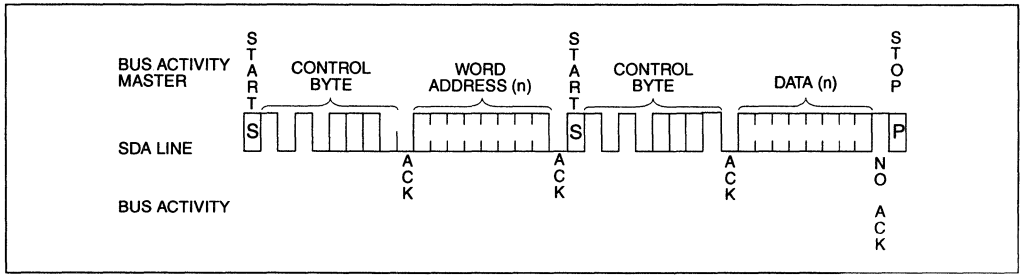
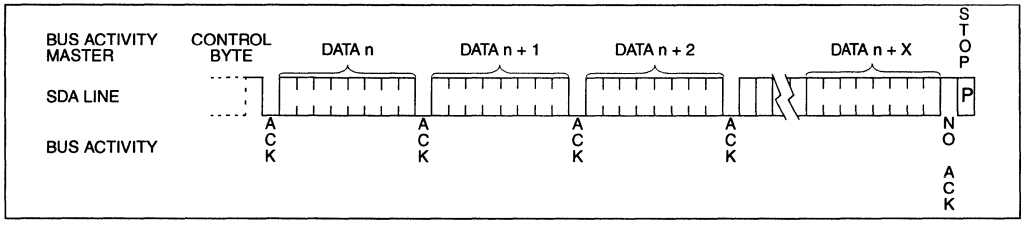


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

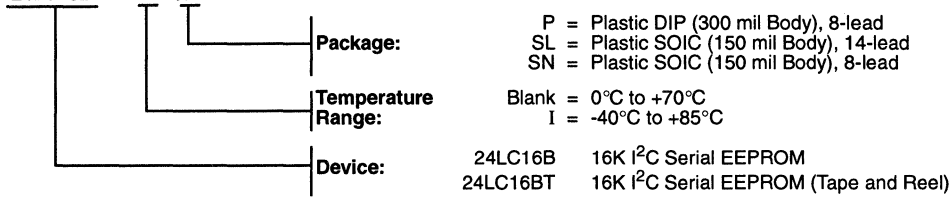
This feature allows the user to use the 24LC16B as a serial ROM when WP is enabled (tied to Vcc).

8.4 A0, A1, A2

These pins are not used by the 24LC16B. They may be left floating or tied to either Vss or Vcc.

24LC16B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA164

16K 1.8V Cascadable I²C™ Serial EEPROM

FEATURES

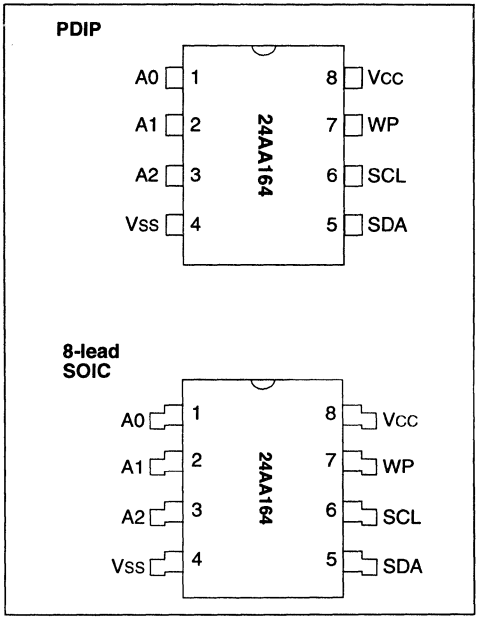
- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 Erase/Write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead SOIC packages
- Available for commercial temperature range
  - Commercial (C): 0°C to +70°C

DESCRIPTION

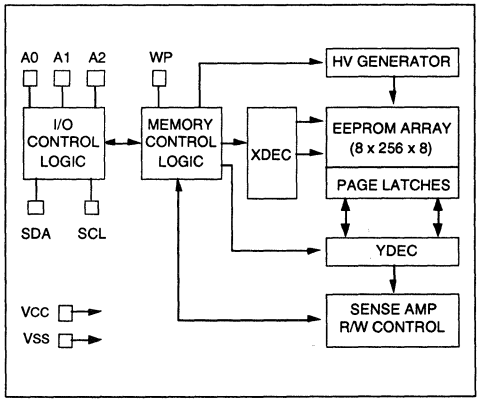
The Microchip Technology Inc. 24AA164 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 1.8 volts (end-of-life voltage for most popular battery technologies) with standby and active currents of only 5 µA and 1 mA respectively. The 24AA164 also has a page-write capability for up to 16 bytes of data. The 24AA164 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPES



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.3V to VCC +1.0V
Storage temperature.....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds).....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	1.8V to 6.0V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

			VCC = 1.8V to +6.0 Commercial (C): Tamb = 0°C to +70°C			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:						
High level input voltage	VIH	.7 VCC		—	V	
Low level input voltage	VIL	—		.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC		—	V	(Note)
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA, VCC = 1.8V
Input leakage current	ILI	-10		10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10		10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs	CIN, COUT	—		10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.5	—	mA	VCC = 1.8V, SCL = 100 kHz
	ICC Read	—	—	1	mA	VCC = 5.5V, SCL = 400 kHz
		—	0.05	—	mA	VCC = 1.8V, SCL = 100 kHz
Standby current	ICCS	—	—	100	µA	VCC = 5.5V, SDA = SCL=VCC
		—	—	30	µA	VCC = 3.0V, SDA = SCL=VCC
		—	3	—	µA	VCC = 1.8V, SDA = SCL=VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

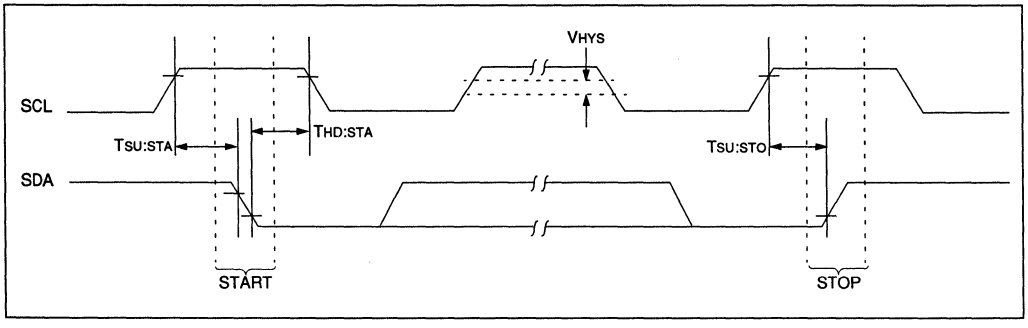


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		VCC = 4.5-5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode ((Note 4)

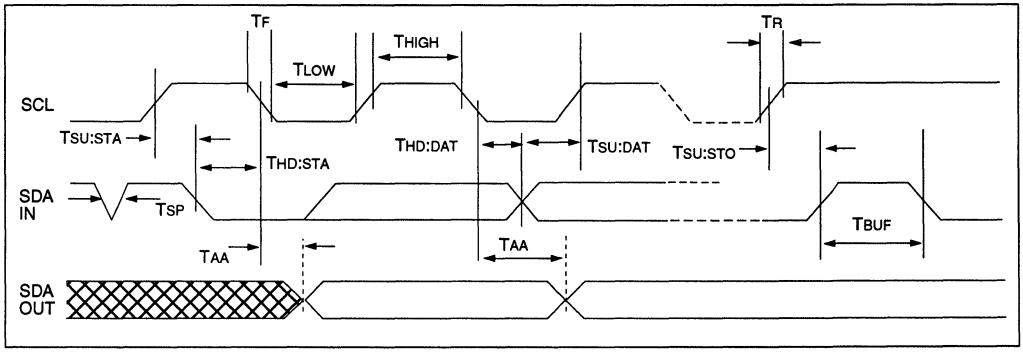
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS =specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24AA164 supports aBi-directional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA164 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

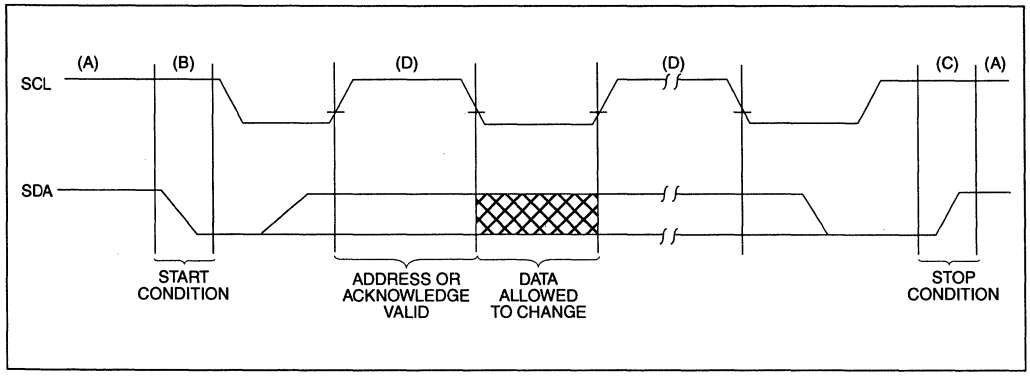
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24AA164 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA164) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

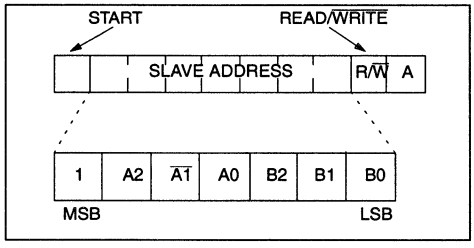
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA164 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24AA164 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $\overline{A1}$ A0	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA164. After receiving another acknowledge signal from the 24AA164 the master device will transmit the data word to be written into the addressed memory location. The 24AA164 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA164 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA164 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24AA164 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

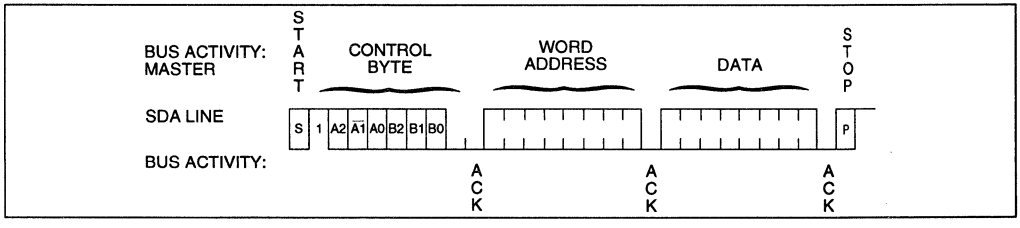
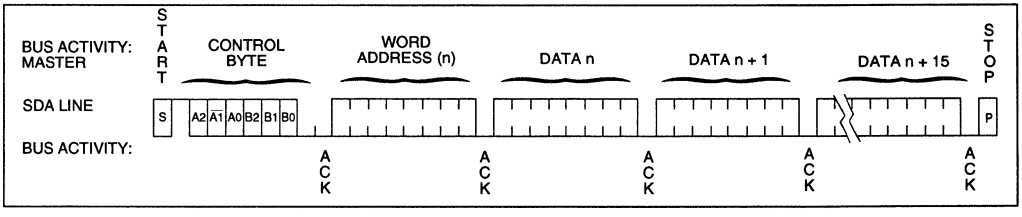


FIGURE 4-2: PAGE WRITE



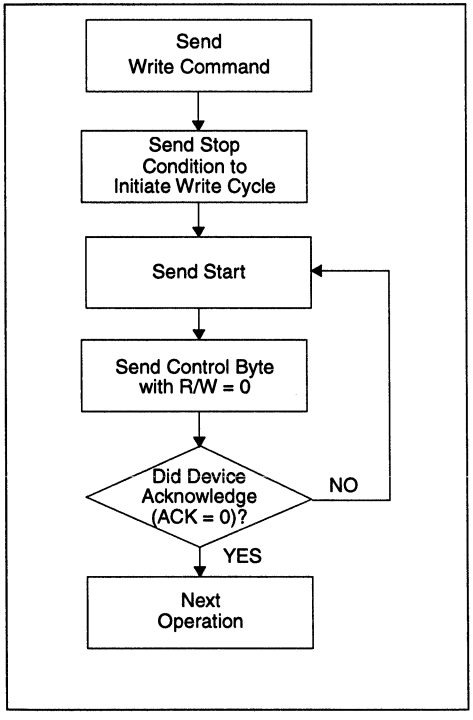
3

I²C™

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24AA164 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24AA164 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA164 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA164 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA164 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA164 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA164 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA164 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA164 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24AA164 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

7.4 Noise Protection

The 24AA164 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

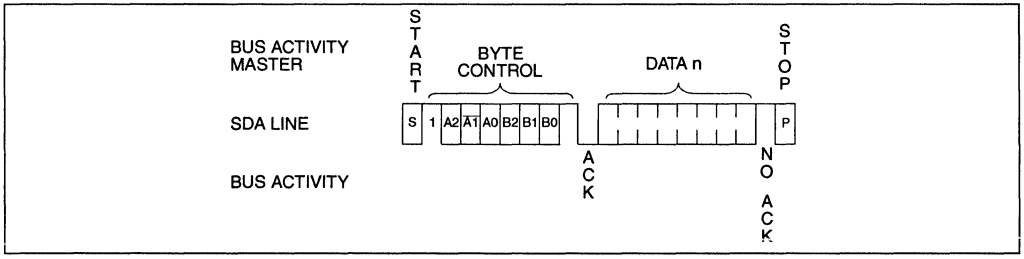


FIGURE 7-2: RANDOM READ

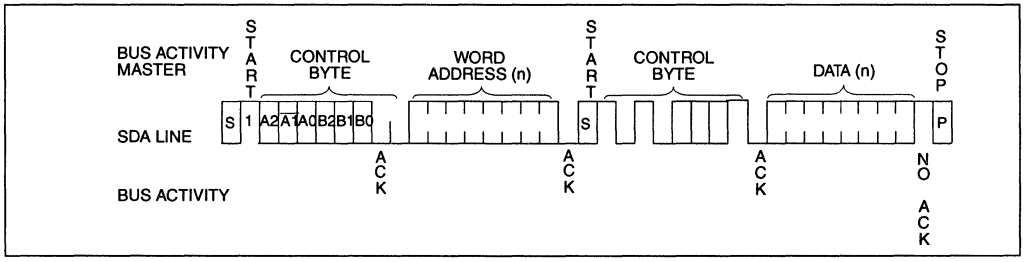
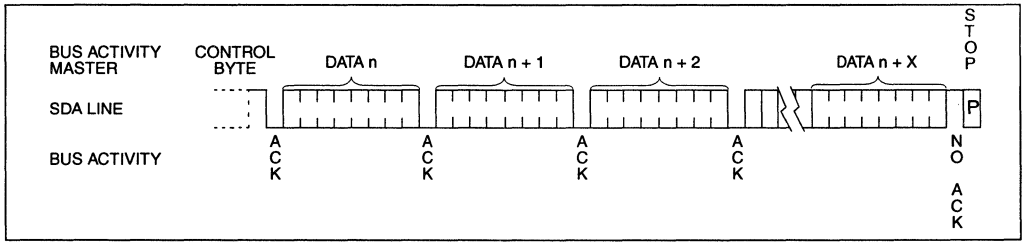


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA164 as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

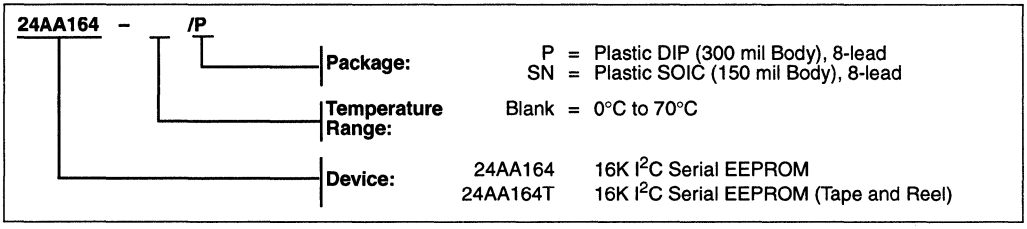
These pins are used to configure the proper chip address in multiple-chip applications (more than one 24AA164 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24AA164s may be connected to the same bus. These pins must be connected to either VSS or VCC.

24AA164 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC164

16K 2.5V Cascadable I²C™ Serial EEPROM

FEATURES

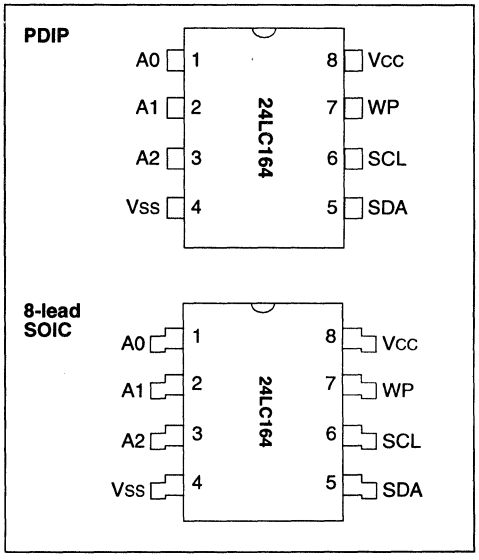
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as eight blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 Erase/Write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead SOIC packages
- Available temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

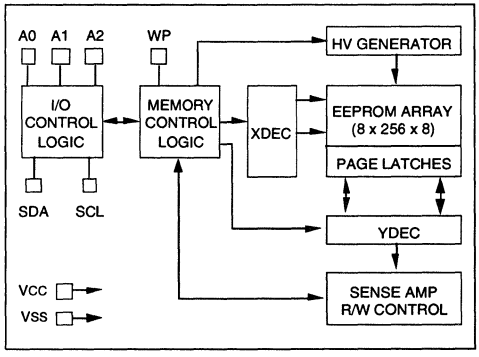
The Microchip Technology Inc. 24LC164 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC164 also has a page-write capability for up to 16 bytes of data. The 24LC164 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPES



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.3V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds).....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

			VCC = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC WP = VSS

Note: is parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

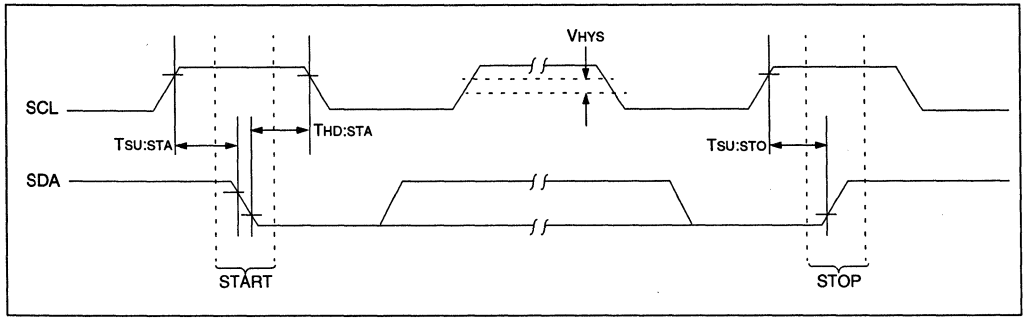


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5V - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

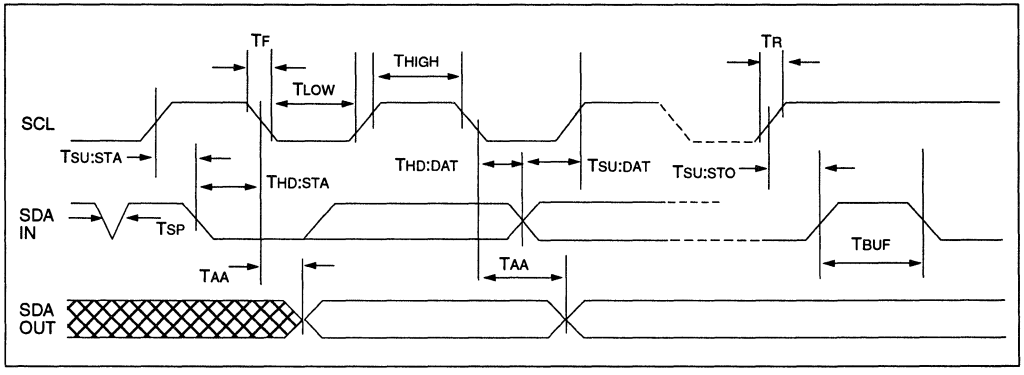
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed my characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC164 supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC164 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

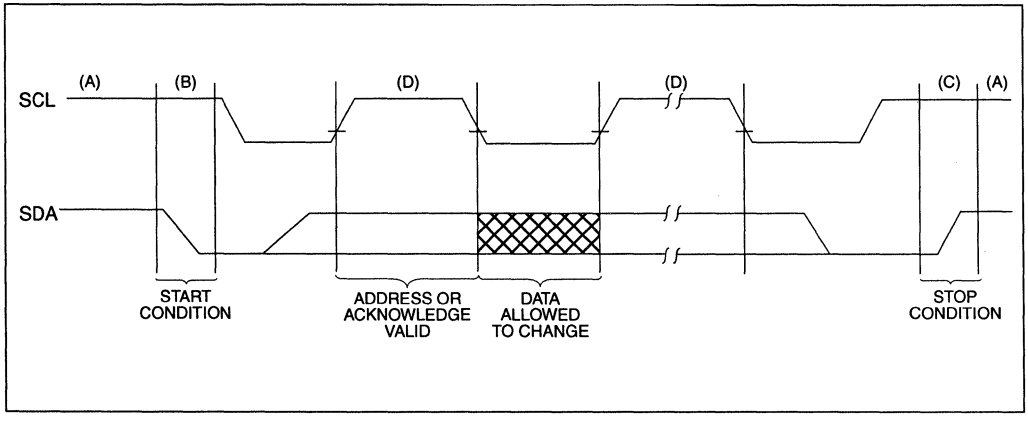
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC164 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC164) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

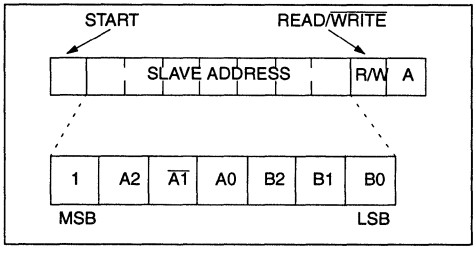
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC164 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24LC164 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $\overline{A1}$ A0	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC164. After receiving another acknowledge signal from the 24LC164 the master device will transmit the data word to be written into the addressed memory location. The 24LC164 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC164 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC164 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC164 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

FIGURE 4-1: BYTE WRITE

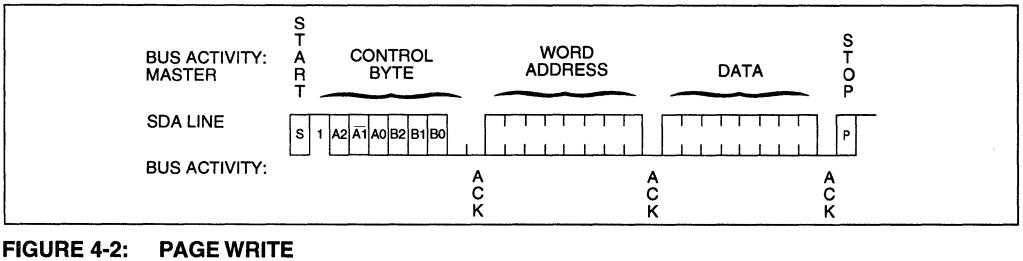
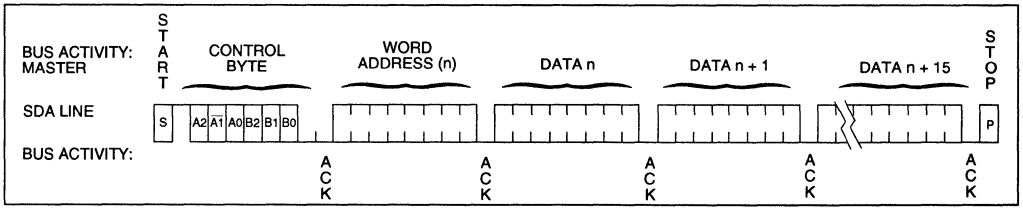


FIGURE 4-2: PAGE WRITE



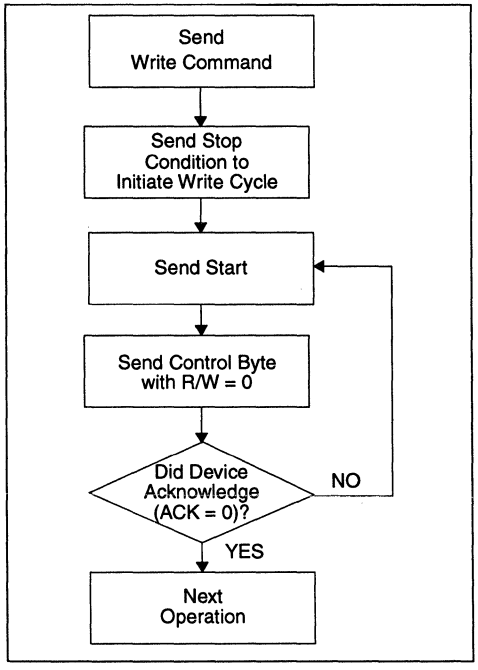
3

I²C™

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24LC164 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24LC164 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC164 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC164 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC164 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC164 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC164 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC164 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC164 to transmit the next sequentially addressed 8 bit word (Figure 7-3).

To provide sequential reads the 24LC164 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC164 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

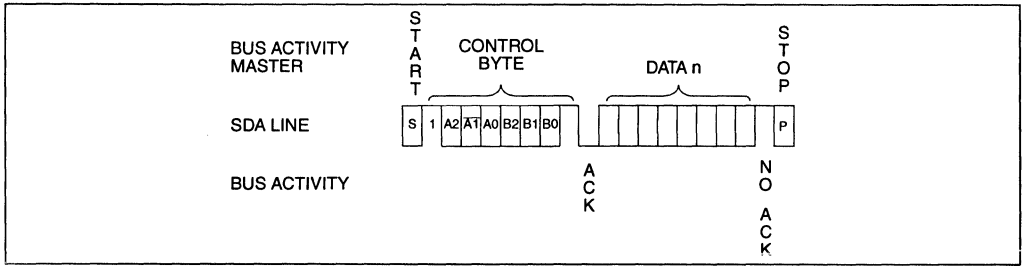


FIGURE 7-2: RANDOM READ

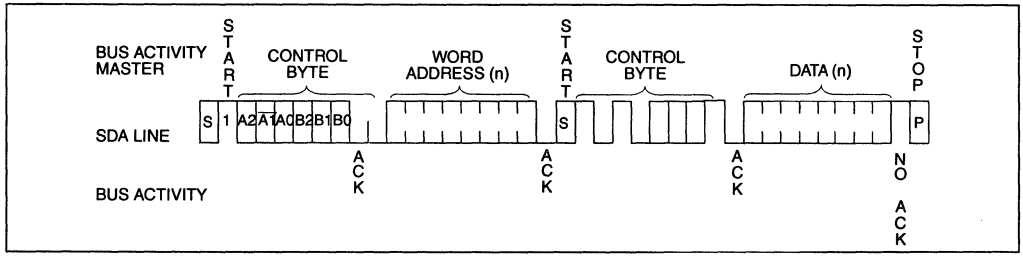
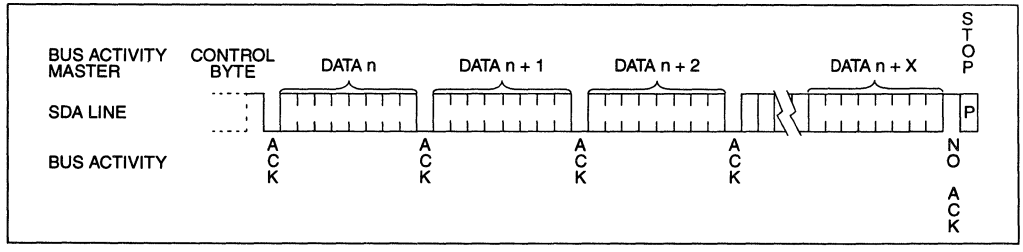


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC164 as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

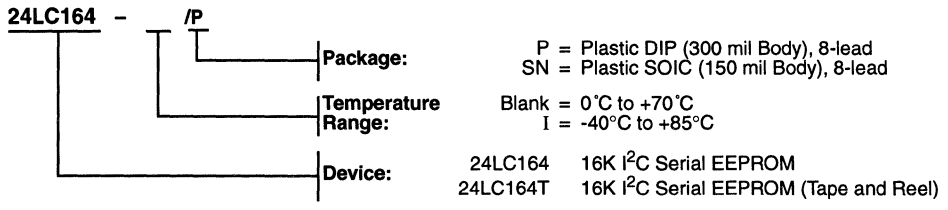
These pins are used to configure the proper chip address in multiple-chip applications (more than one 24LC164 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24LC164s may be connected to the same bus. These pins must be connected to either VSS or VCC.

24LC164 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA174

16K 1.8V Cascadable I²C™ Serial EEPROM with OTP Security Page

FEATURES

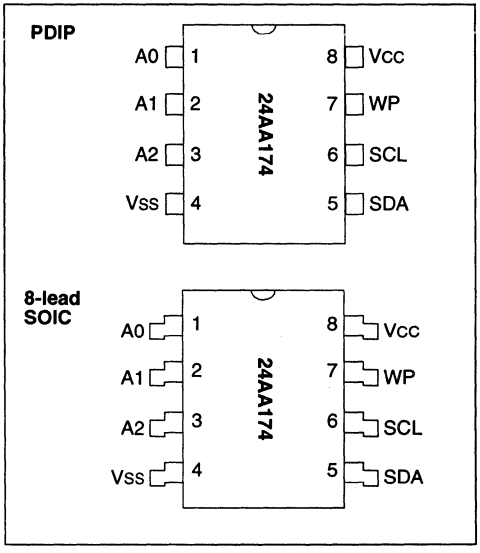
- Single supply with operation down to 1.8V
- 16 bytes OTP Secure Memory
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as eight blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 Erase/Write cycles guaranteed
- Data retention > 200 years
- 8 pin DIP, 8-lead SOIC packages
- Available for commercial temperature range
  - Commercial (C): 0°C to +70°C

DESCRIPTION

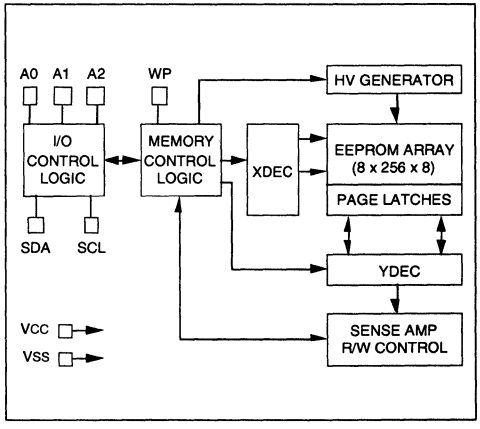
The Microchip Technology Inc. 24AA174 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface and provides a specially addressed OTP (one-time programmable) 16 byte security block. Low voltage design permits operation down to 1.8 volts (end-of-life voltage for most popular battery technologies) with standby and active currents of only 5 µA and 1 mA respectively. The 24AA174 also has a page-write capability for up to 16 bytes of data. The 24AA174 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPES



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.3V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds).....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+1.8V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

	Vcc = +1.8V to 5.5V Commercial (C): Tamb = 0°C to +70°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note1) Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write Icc Read	— —	3 1	mA mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	Iccs	— —	30 100	µA µA	Vcc = 3.0V, SDA = SCL = Vcc Vcc = 5.5V, SDA = SCL = Vcc WP=Vss

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

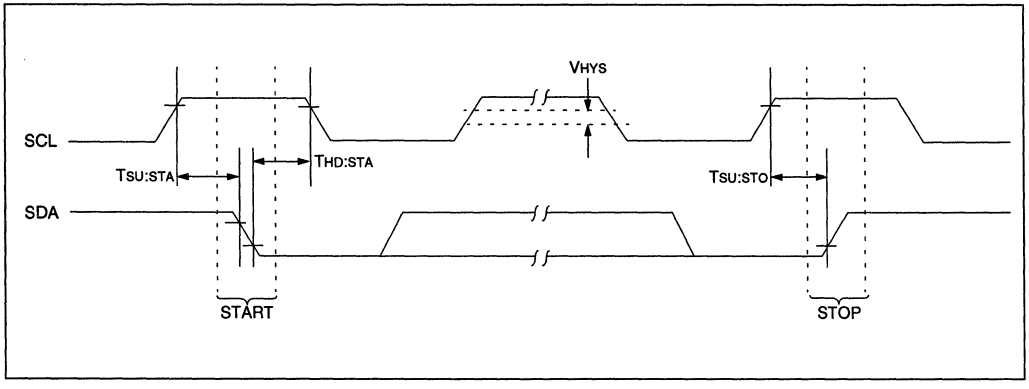
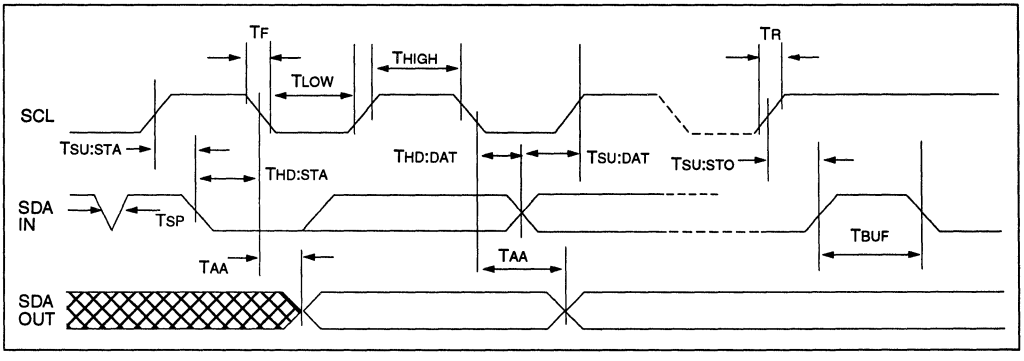


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		V cc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	Cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

1: Not 100% tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.
4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24AA174 supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA174 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

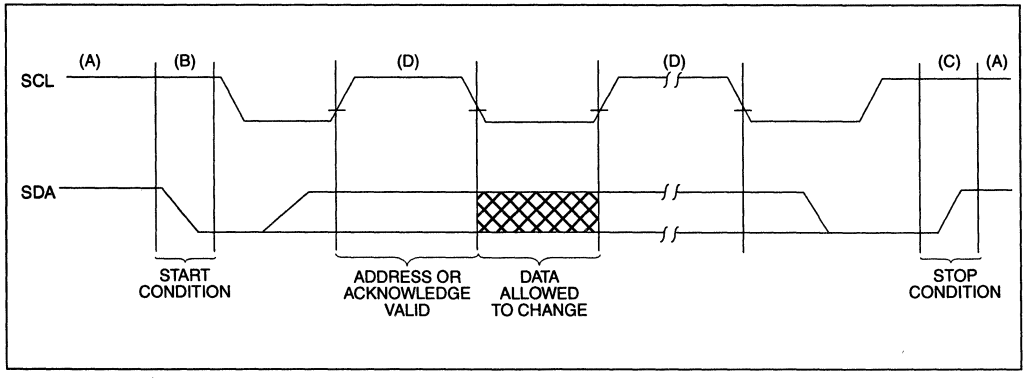
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24AA174 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA174) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

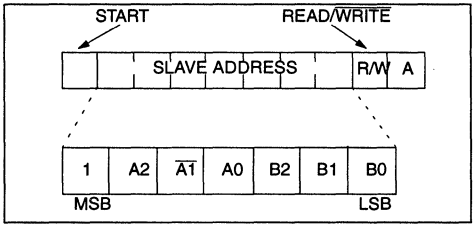
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA174 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24AA174 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $\overline{A1}$ A0	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA174. After receiving another acknowledge signal from the 24AA174 the master device will transmit the data word to be written into the addressed memory location. The 24AA174 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA174 will not generate acknowledge signals (see Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA174 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24AA174 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 4-2).

FIGURE 4-1: BYTE WRITE

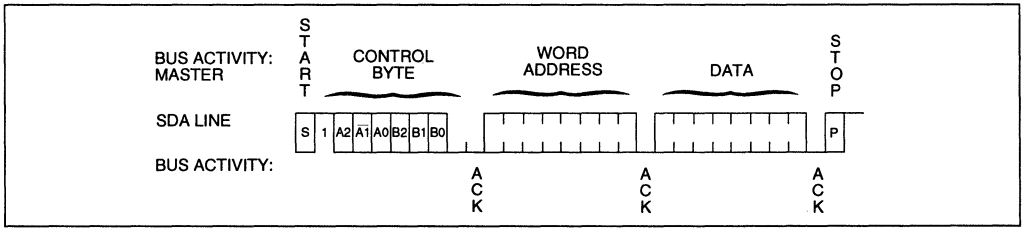
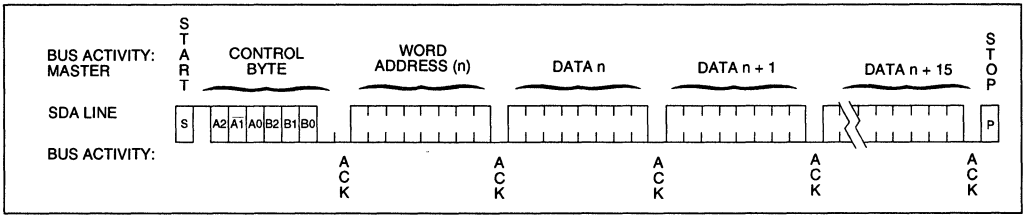


FIGURE 4-2: PAGE WRITE



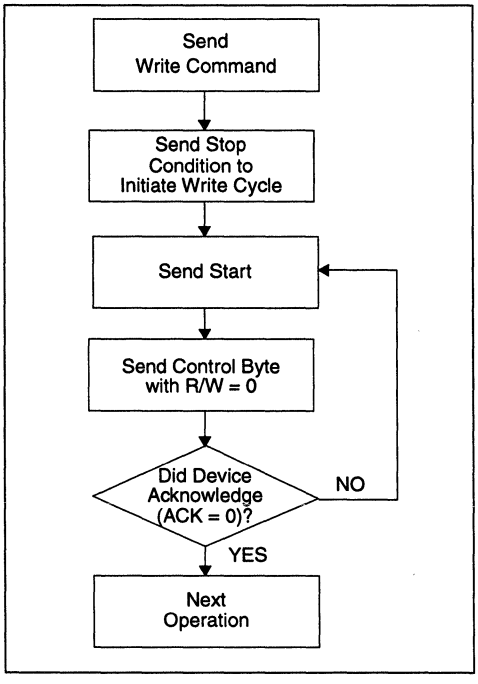
3

I²C™

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24AA174 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24AA174 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA174 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA174 discontinues transmission (Figure 8-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA174 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA174 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA174 discontinues transmission (Figure 8-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA174 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA174 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24AA174 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

7.4 Noise Protection

The 24AA174 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA174 as a serial ROM when WP is enabled (tied to VCC).

8.4 A0, A1, A2

These pins are used to configure the proper chip address in multiple-chip applications (more than one 24AA174 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24AA174s may be connected to the same bus. These pins must be connected to either VSS or VCC.

8.5 Security Access Control

The security row is enabled by sending the control sequence with the I^2C slave address of 0110. Bit 0 of the control byte must be set to a one for a READ OPERATION or a zero for the OTP WRITE OPERATION. The SECURITY ACCESS DATA is always read starting at byte 0 for N bytes up to and including byte 15. (See Figure 4-2).

8.6 Security Access Write

The S.A.W. data is written to the device using a normal page write following the proper control access sequence. Upon receiving the final stop bit, the internal write sequence will commence. At the completion of the internal write sequence a fuse will be set disabling the write function for the 16 byte security page.

8.7 Security Access Read

The security access read is accomplished by executing the normal read sequences, following the security access control sequence with bit 0 set to a one. The security page read starts at data byte 0.

FIGURE 8-1: CURRENT ADDRESS READ

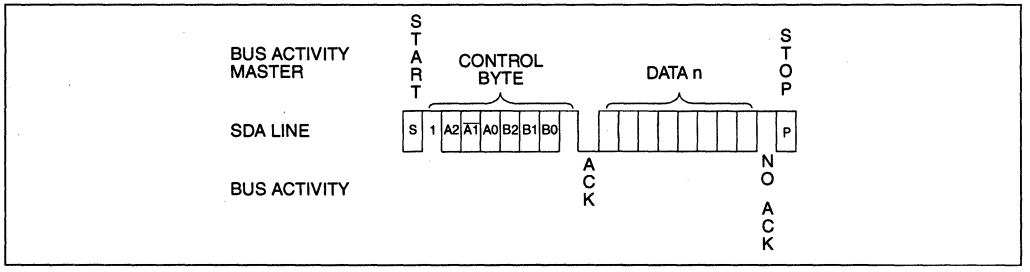


FIGURE 8-2: RANDOM READ

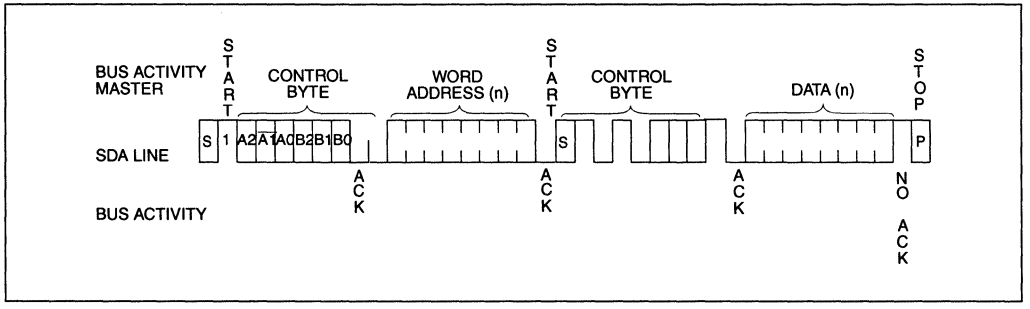


FIGURE 8-3: SEQUENTIAL READ

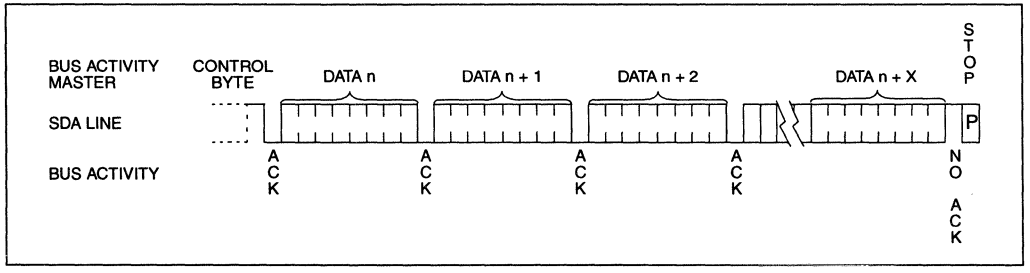


FIGURE 8-4: SECURITY CONTROL BYTE ALLOCATION

Operation	Control Code	Block Select	R/$\overline{W}$
Read	0110	000	1
Write	0110	000	0

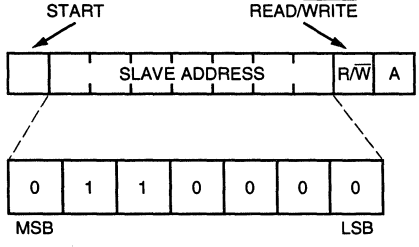


FIGURE 8-5: SECURITY PAGE READ

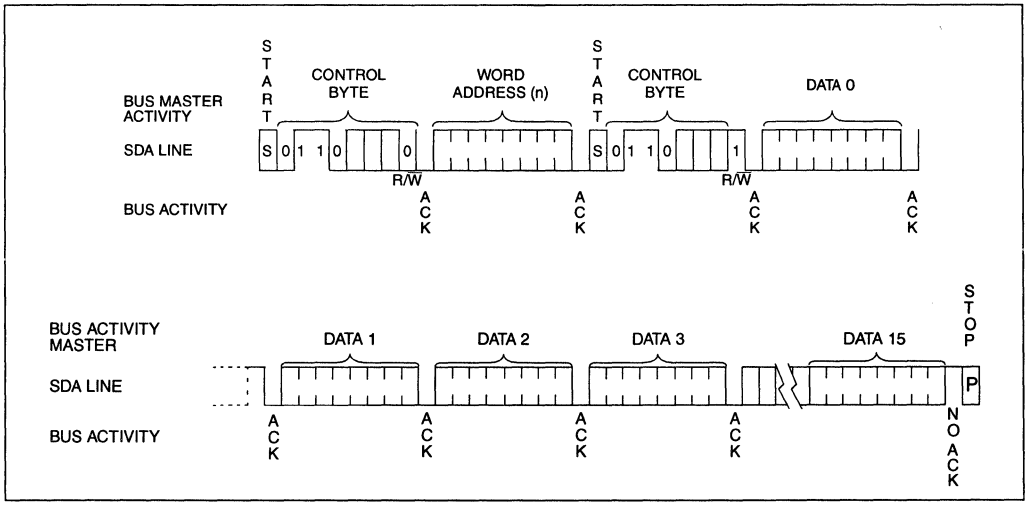
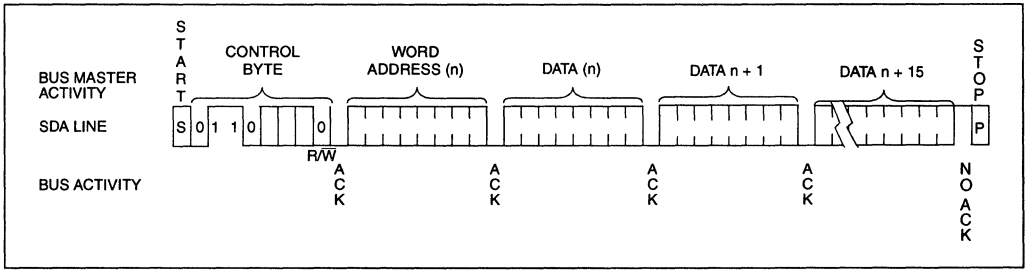


FIGURE 8-6: SECURITY PAGE WRITE

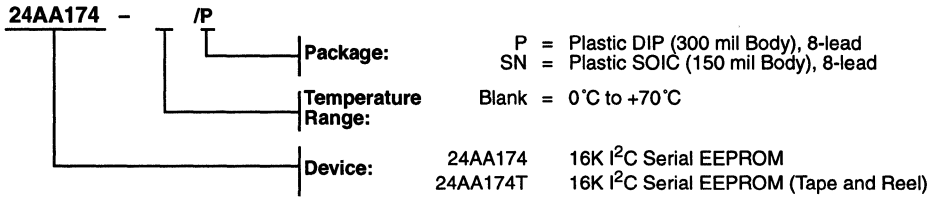


3

I²C™

24AA174 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC174

16K 2.5V Cascadable I²C™ Serial EEPROM with OTP Security Page

FEATURES

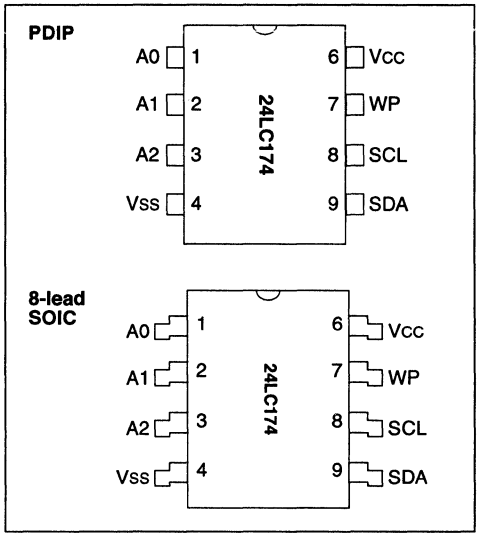
- Single supply with operation down to 2.5V
- 16 bytes OTP Secure Memory
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as eight blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 Erase/Write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead SOIC packages
- Available temperature ranges:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40° to +85°

DESCRIPTION

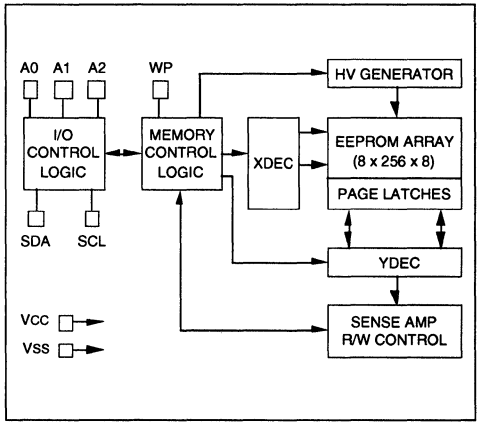
The Microchip Technology Inc. 24LC174 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface and provides a specially addressed OTP (one-time programmable) 16 byte security block. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC174 also has a page-write capability for up to 16 bytes of data. The 24LC174 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPES



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss ..... -0.3V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

	Vcc = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note1), Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write Icc Read	— —	3 1	mA mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	Iccs	— —	30 100	µA µA	Vcc = 3.0V, SDA = SCL = Vcc Vcc = 5.5V, SDA = SCL = Vcc WP = Vss

Note:This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

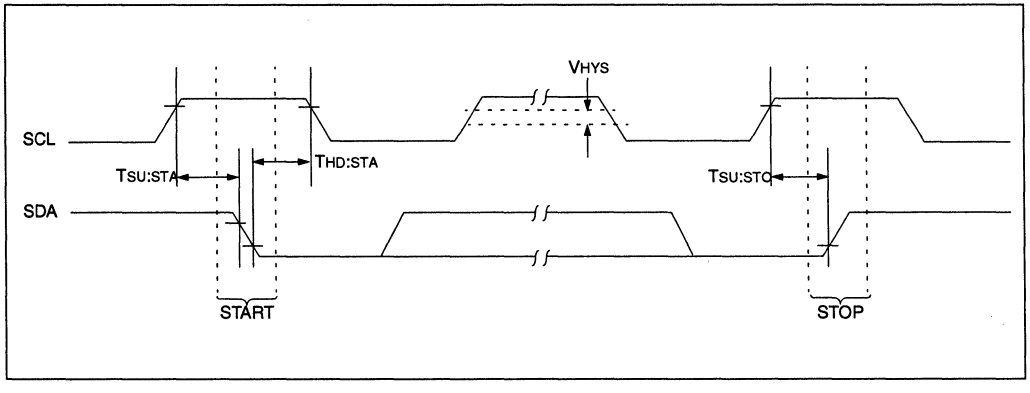


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

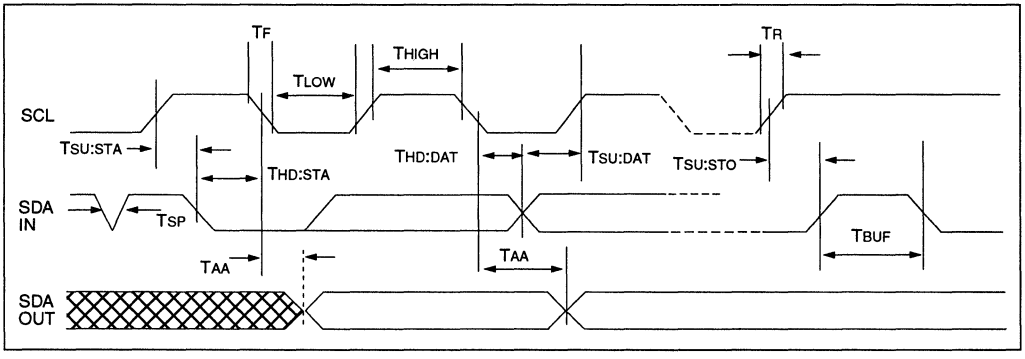
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24LC174 supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC174 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

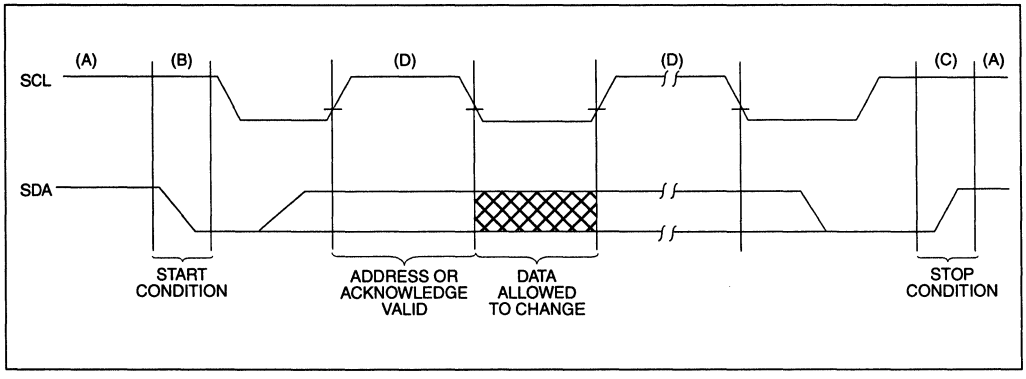
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC174 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC174) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation

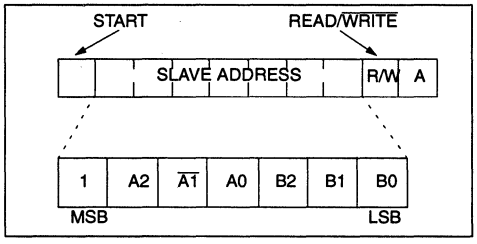
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC174 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24LC174 will select a read or write operation.

Operation	Control Code				Block Select	R/$\overline{W}$
Read	1	A2	$\overline{A1}$	A0	Block Address	1
Write	1	A2	$\overline{A1}$	A0	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC174. After receiving another acknowledge signal from the 24LC174 the master device will transmit the data word to be written into the addressed memory location. The 24LC174 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC174 will not generate acknowledge signals (Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC174 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC174 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 8.3).

FIGURE 5-1: BYTE WRITE

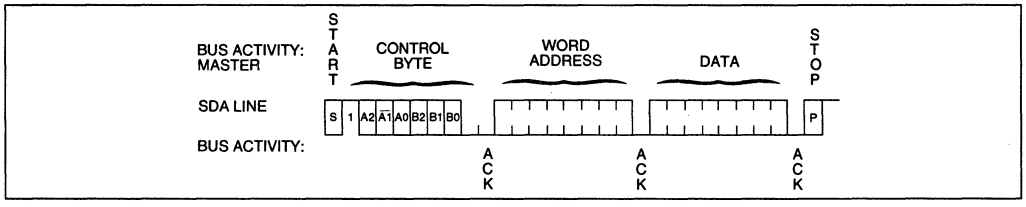
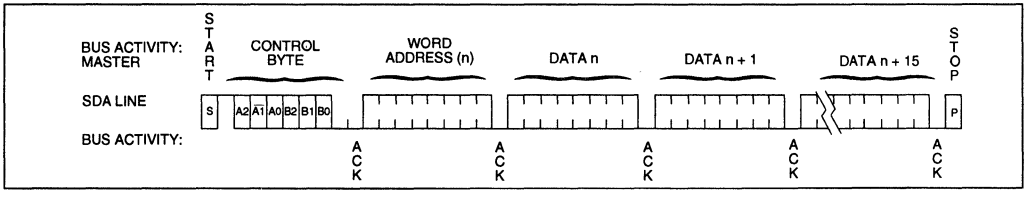


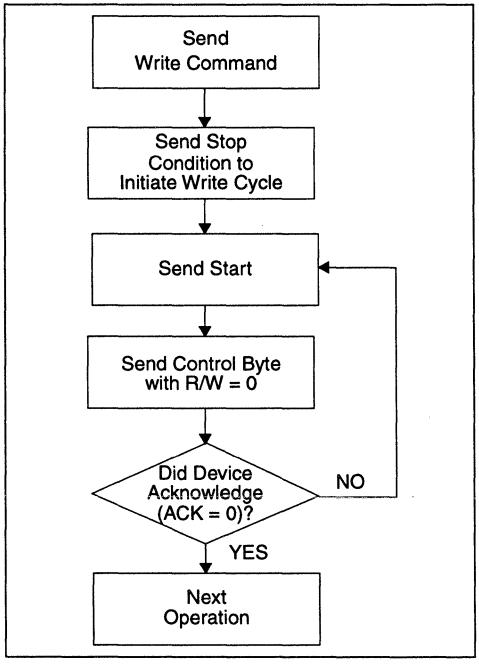
FIGURE 5-2: PAGE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24LC174 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LC174 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC174 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC174 discontinues transmission (Figure 9-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC174 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC174 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC174 discontinues transmission (Figure 9-2).

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC174 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC174 to transmit the next sequentially addressed 8-bit word (Figure 9-3).

To provide sequential reads the 24LC174 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC174 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC174 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are used to configure the proper chip address in multiple-chip applications (more than one 24LC174 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note:	The level on A1 is compared to the inverse of the slave address.

Up to eight 24LC174s may be connected to the same bus. These pins must be connected to either Vss or Vcc.

9.5 Security Access Control

The security row is enabled by sending the control sequence with the I^2C slave address of 0110. Bit 0 of the control byte must be set to a one for a READ OPERATION or a zero for the OTP WRITE OPERATION. The SECURITY ACCESS DATA is always read starting at byte 0 for N bytes up to and including byte 15. (See Figure 9-3).

9.6 Security Access Write

The S.A.W. data is written to the device using a normal page write following the proper control access sequence. Upon receiving the final stop bit, the internal write sequence will commence. At the completion of the internal write sequence a fuse will be set disabling the write function for the 16 byte security page.

9.7 Security Access Read

The security access read is accomplished by executing the normal read sequences, following the security access control sequence with bit 0 set to a one. The security page read starts at data byte 0.

FIGURE 9-1: CURRENT ADDRESS READ

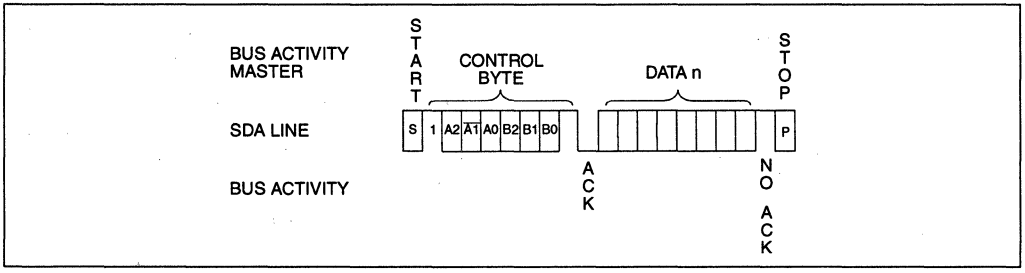


FIGURE 9-2: RANDOM READ

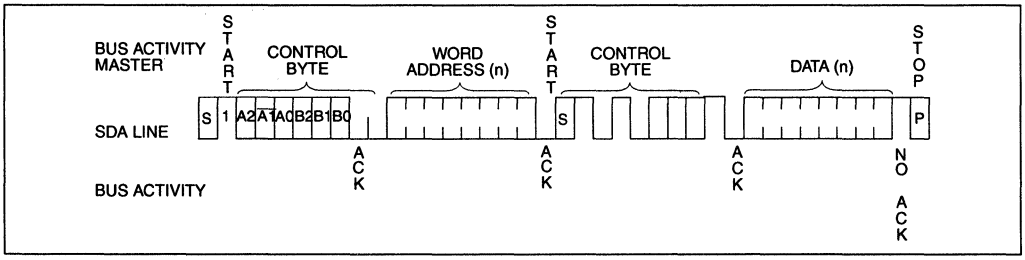


FIGURE 9-3: SEQUENTIAL READ

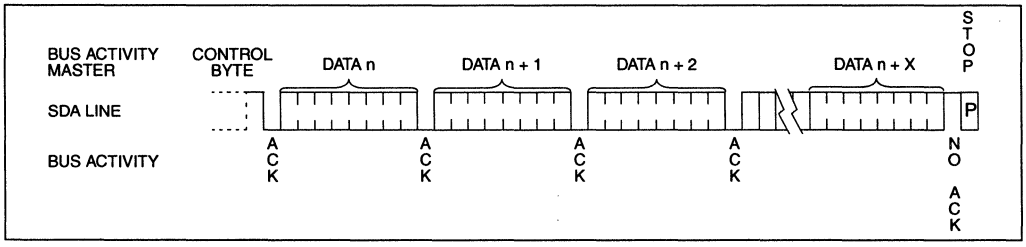


FIGURE 9-4: SECURITY CONTROL BYTE ALLOCATION

Operation	Control Code	Block Select	R/$\overline{W}$
Read	0110	000	1
Write	0110	000	0

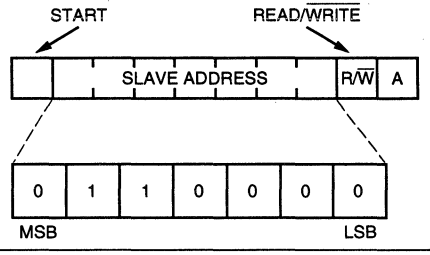


FIGURE 9-5: SECURITY PAGE READ

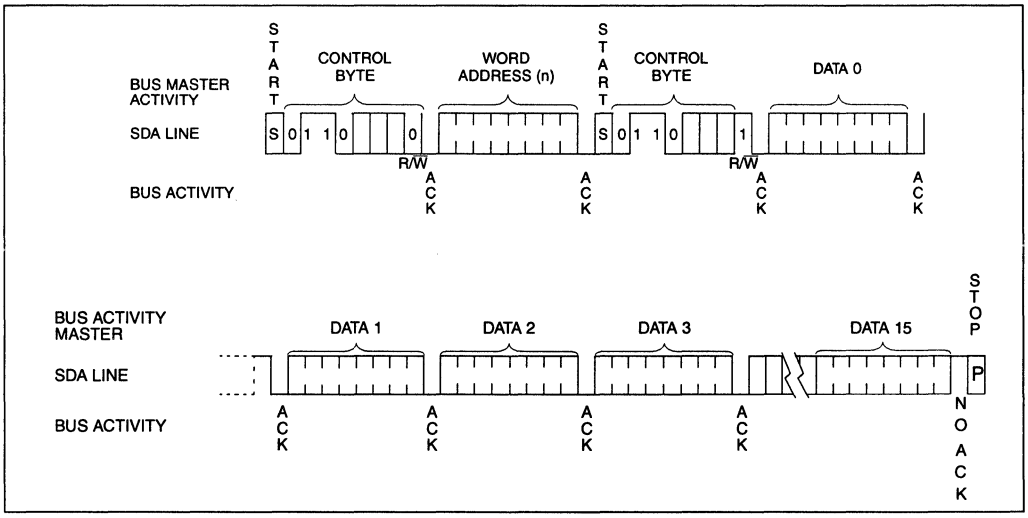
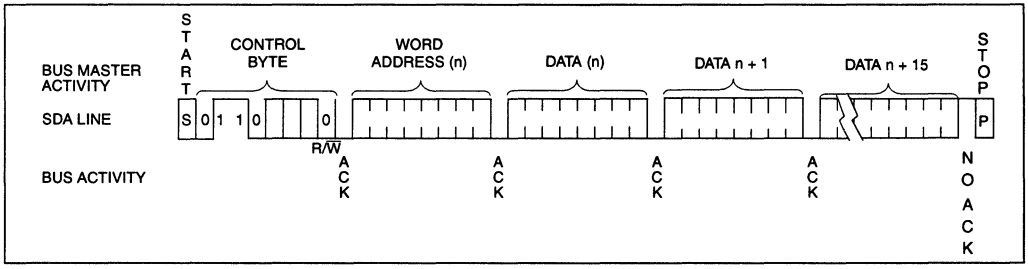


FIGURE 9-6: SECURITY PAGE WRITE

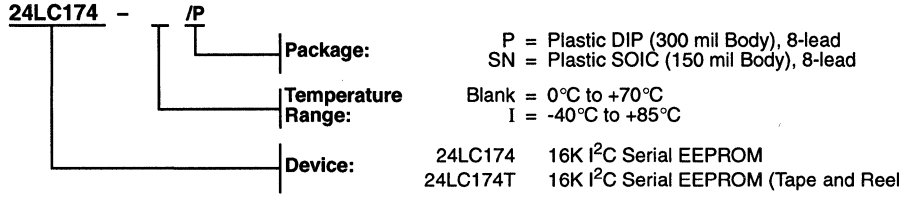


3

I²C™

24LC174 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA32A

32K 1.8V I²C™ Serial EEPROM

FEATURES

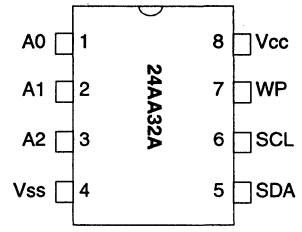
- Single supply with operation down to 1.8V
  - Maximum write current 3 mA at 6.0V
  - Standby current 1 µA max at 1.8V
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Hardware write protect
- 1,000,000 Erase/Write cycles guaranteed
- 32 byte page or byte write modes available
- Schmitt trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to eight devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C

DESCRIPTION

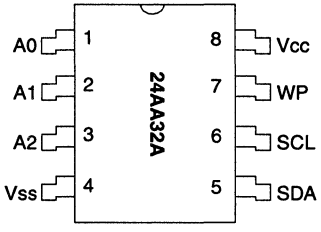
The Microchip Technology Inc. 24AA32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 6.0V). It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24AA32A also has a page-write capability of up to 32 bytes of data. The 24AA32A is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24AA32A devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low-voltage, nonvolatile code and data applications. The 24AA32A is available in the standard 8-pin plastic DIP and both 150 mil and 200 mil SOIC packages.

PACKAGE TYPE

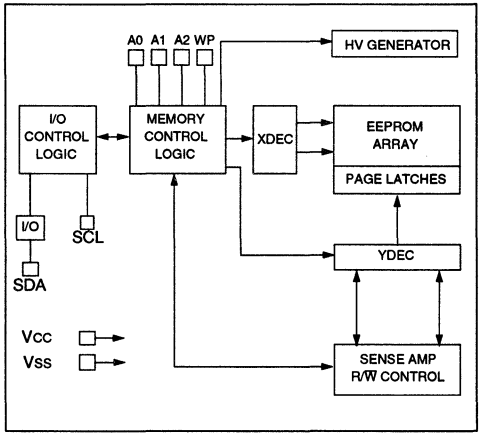
PDIP



SOIC



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+1.8V to 6.0V Power Supply

TABLE 1-2: DC CHARACTERISTICS

Vcc = +1.8V to 6.0V
Commercial (C) Tamb = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
A0, A1, A2, SCL , SDA and WP pins:						
High level input voltage	VIH	.7 Vcc		—	V	
Low level input voltage	VIL1	—		.3 Vcc	V	Vcc ≥ 2.5V
	VIL2	—		.2 Vcc	V	Vcc < 2.5V
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc		—	V	(Note)
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10		10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10		10	µA	VOUT = .1V to Vcc
Pin capacitance (all inputs/outputs)	CIN,COUT	—		10	pF	Vcc = 5.0V (Note) Tamb = 25°C, F_c = 1 MHz
Operating current	Icc Write	—		3	mA	Vcc = 6.0V
	Icc Read	—		0.5	mA	Vcc = 6.0V, SCL = 400kHz
Standby current	Iccs	—	1	5	µA	SCL = SDA = Vcc = 5.5V
	Iccs			1	µA	Vcc = 1.8V (Note) WP = Vss, A0, A1, A2 = Vss

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

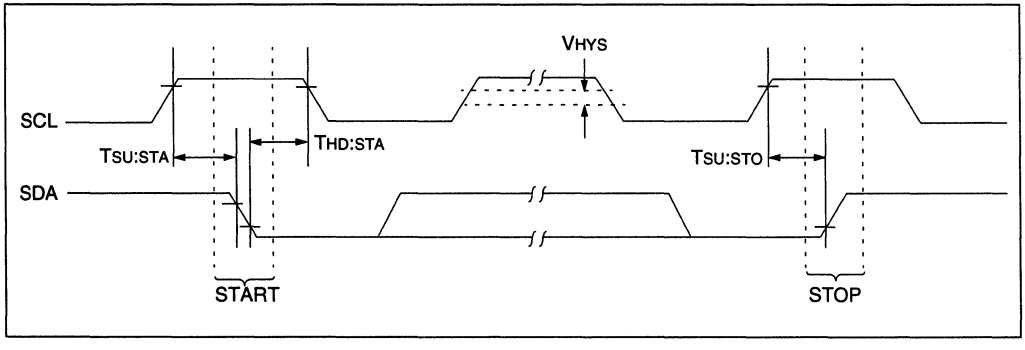


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 1.8-6.0V STD. MODE		Vcc = 4.5-6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms	Byte or Page Mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

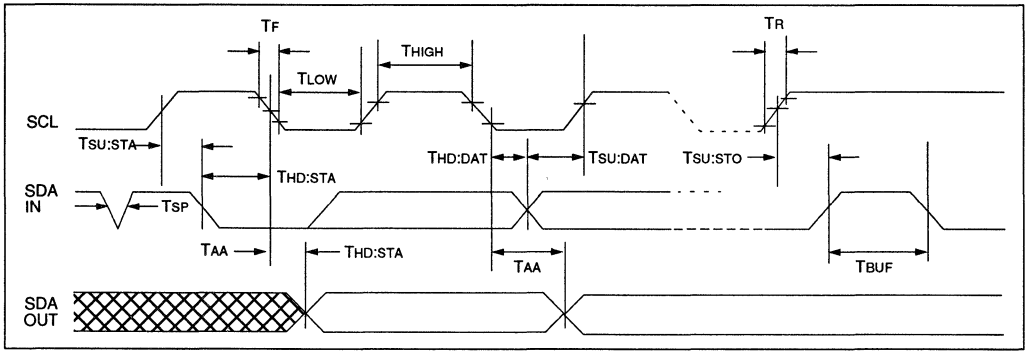
Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

2: As a trasmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

4: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24AA32A supports a Bi-directional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA32A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

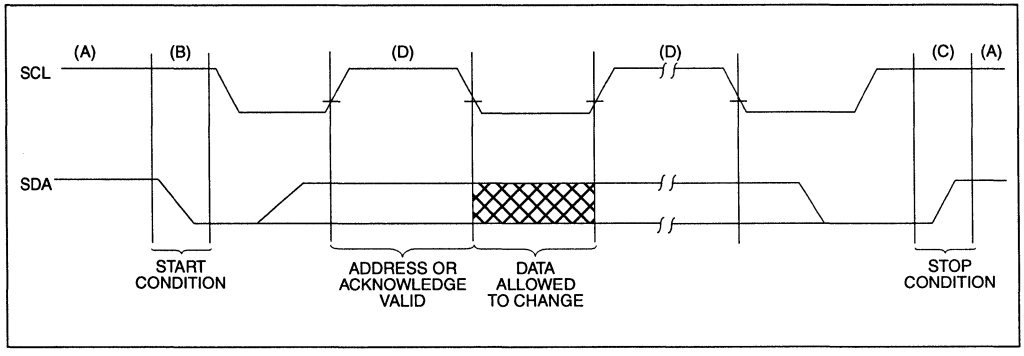
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA32A does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA32A) will leave the data line HIGH to enable the master to generate the STOP condition.

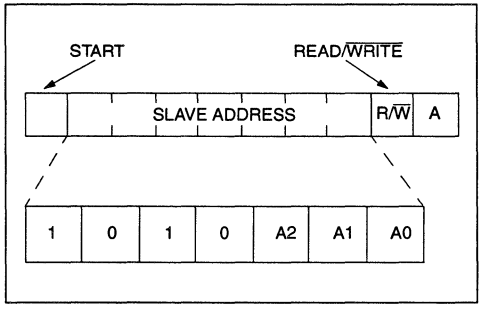
FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code; for the 24AA32A this is set as 1010 binary for read and write (R/$\overline{W}$) operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

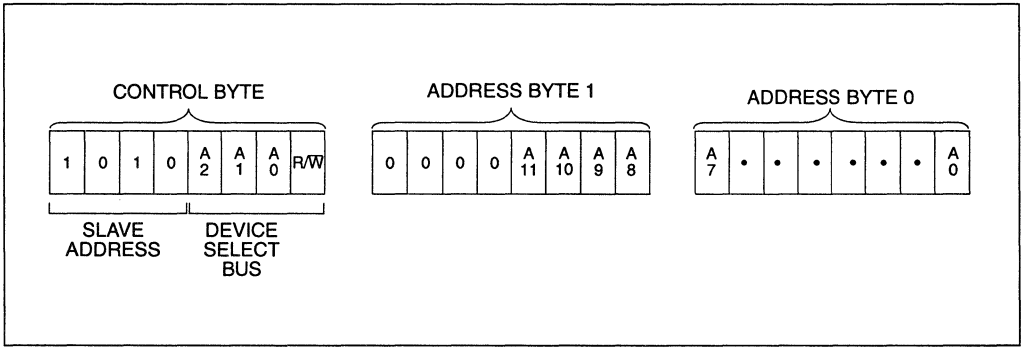
FIGURE 3-2: CONTROL BYTE ALLOCATION



Following the start condition, the 24AA32A monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA32A will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



3

I²C™

4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24AA32A. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24AA32A the master device will transmit the data word to be written into the addressed memory location.

The 24AA32A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA32A will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA32A in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 32 bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin. (Figure 4-2).

FIGURE 4-1: BYTE WRITE

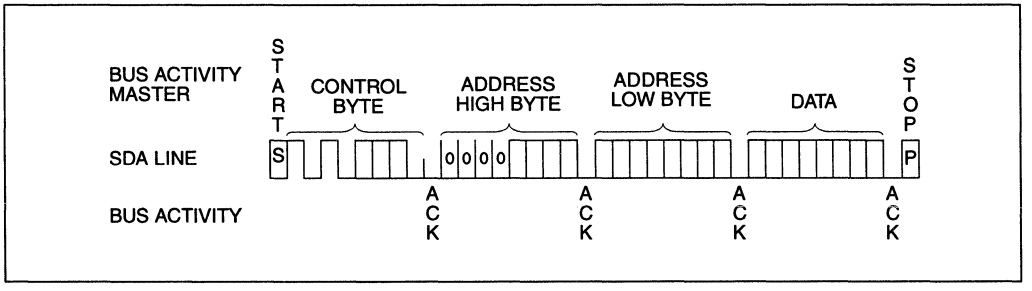
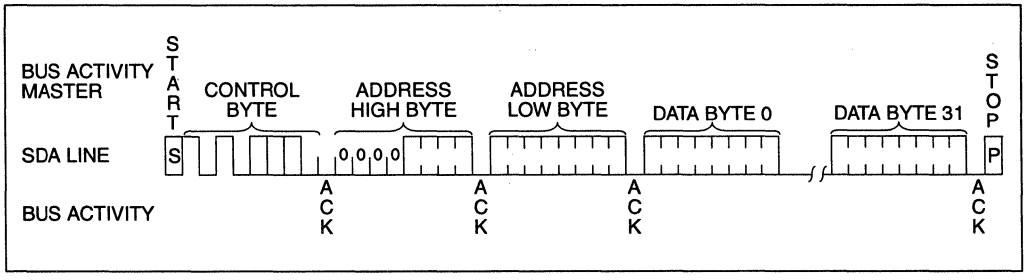


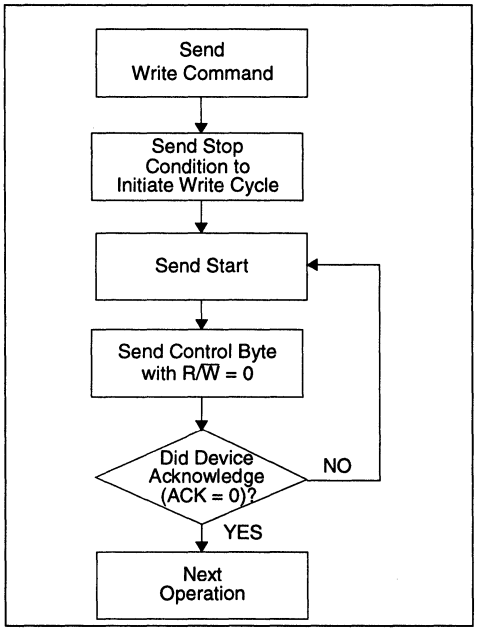
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. Acknowledge Polling (ACK) can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

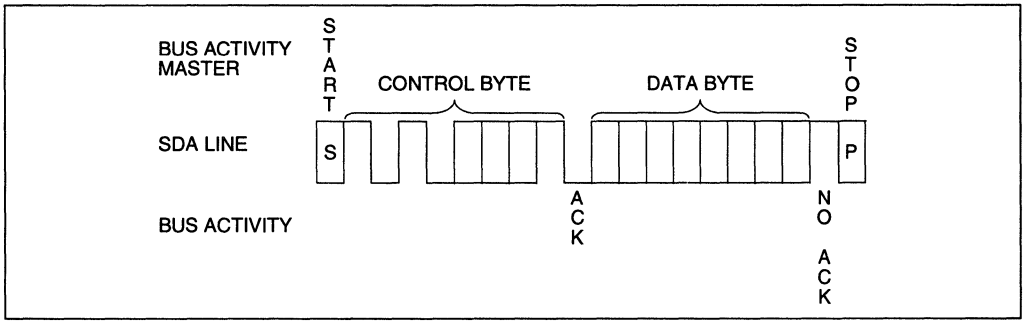
6.1 Current Address Read

The 24AA32A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA32A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA32A discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA32A as part of a write operation (R/$\overline{W}$ bit set to zero). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA32A will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24AA32A to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24AA32A's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA32A transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24AA32A to transmit the next sequentially addressed 8-bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24AA32A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFF to address 000 if the master acknowledges the byte received from the array address 0FFF.

FIGURE 6-2: RANDOM READ

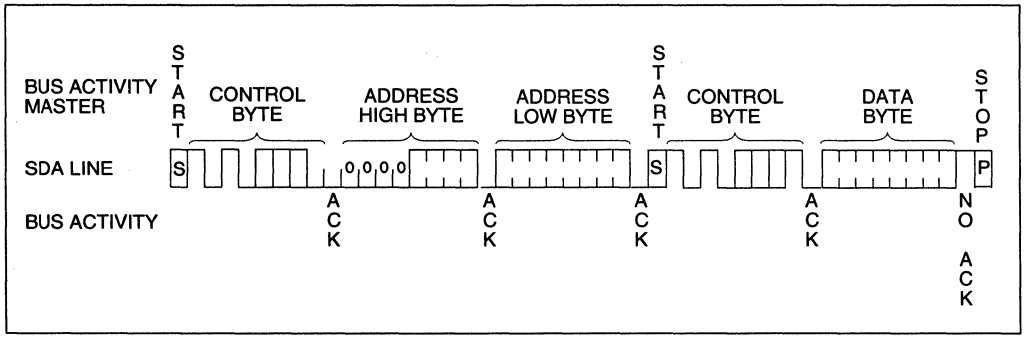
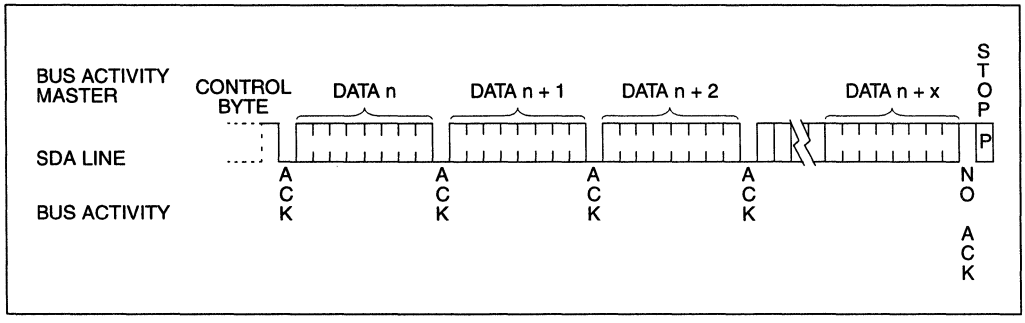


FIGURE 6-3: SEQUENTIAL READ



7.0 PIN DESCRIPTIONS

7.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24AA32A for multiple device operation and conform to the 2-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

7.2 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

7.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

7.4 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-FFF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

8.0 NOISE PROTECTION

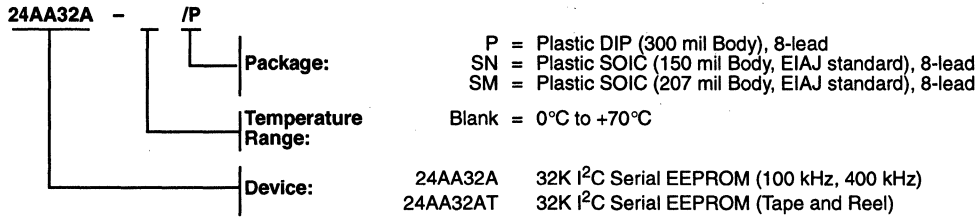
The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

9.0 POWER MANAGEMENT

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e., not receiving an acknowledge or stop condition per the 2-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

24AA32A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC32A

32K 2.5V I²C™ Serial EEPROM

FEATURES

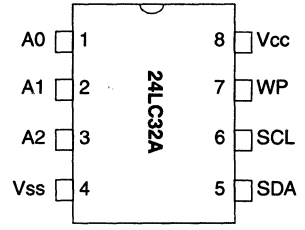
- Single supply with operation down to 2.5V
  - Maximum write current 3 mA at 6.0V
  - Standby current 1 µA max at 2.5V
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Hardware write protect
- 1,000,000 Erase/Write cycles guaranteed
- 32 byte page or byte write modes available
- Schmitt trigger filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to eight devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +75°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

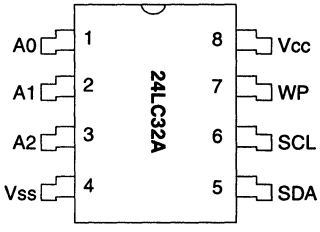
The Microchip Technology Inc. 24LC32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V). It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24LC32A also has a page-write capability of up to 32 bytes of data. The 24LC32A is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24LC32A devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low-voltage, nonvolatile code and data applications. The 24LC32A is available in the standard 8-pin plastic DIP and both 150 mil and 200 mil SOIC packaging.

PACKAGE TYPES

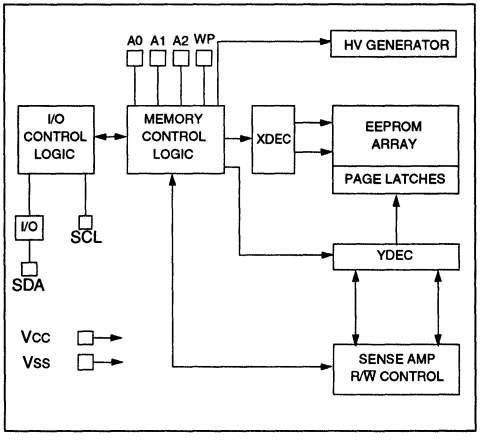
PDIP



SOIC



BLOCK DIAGRAM



3

I²C™

I²C is a trakemark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 6.0V Power Supply

TABLE 1-2: DC CHARACTERISTICS

VCC = +2.5V to 6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
A0, A1, A2, SCL , SDA and WP pins:						
High level input voltage	VIH	.7 VCC		—	V	
Low level input voltage	VIL	—		.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC		—	V	(Note)
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10		10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10		10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN,COUT	—		10	pF	VCC = 5.0V (Note) Tamb = 25°C, F_c = 1 MHz
Operating current	ICC Write	—		3	mA	VCC = 6.0V
	ICC Read	—		0.5	mA	VCC = 6.0V, SCL = 400 KHz
Standby current	ICCS	—	1	5	µA	SCL = SDA = VCC = 5.5V
	ICCS			1	µA	VCC = 2.5V (Note) WP = VSS, A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

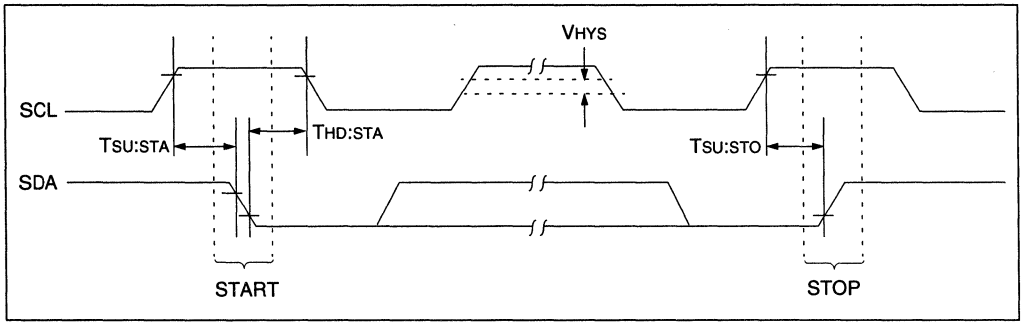
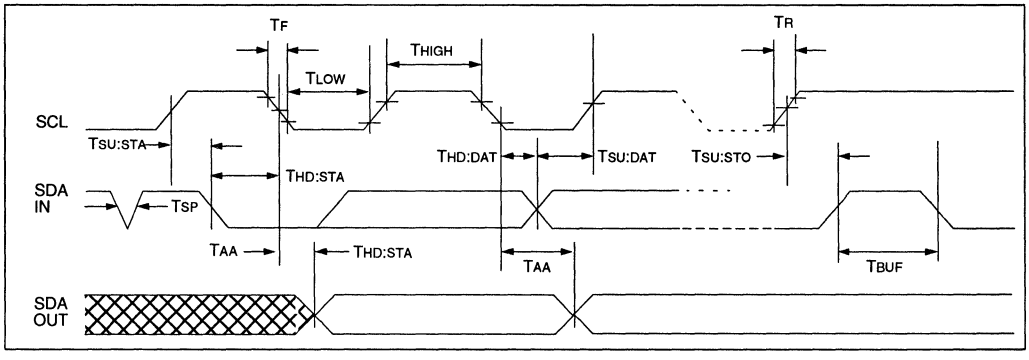


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 2.5-6.0V Standard Mode		Vcc = 4.5-6.0V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode Cycle (Note 4)

Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.
4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC32A supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC32A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

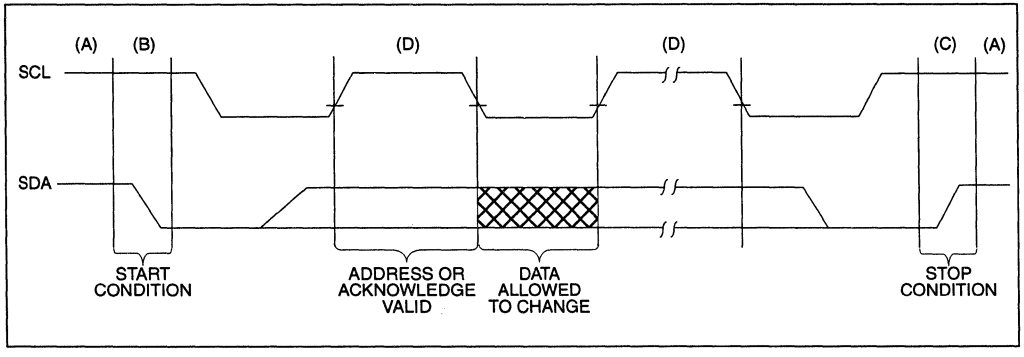
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC32A does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC32A) will leave the data line HIGH to enable the master to generate the STOP condition.

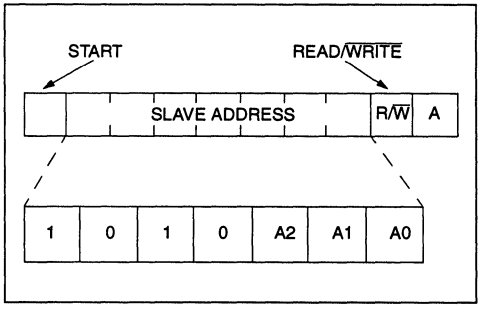
FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code; for the 24LC32A this is set as 1010 binary for read and write (R/$\overline{W}$) operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

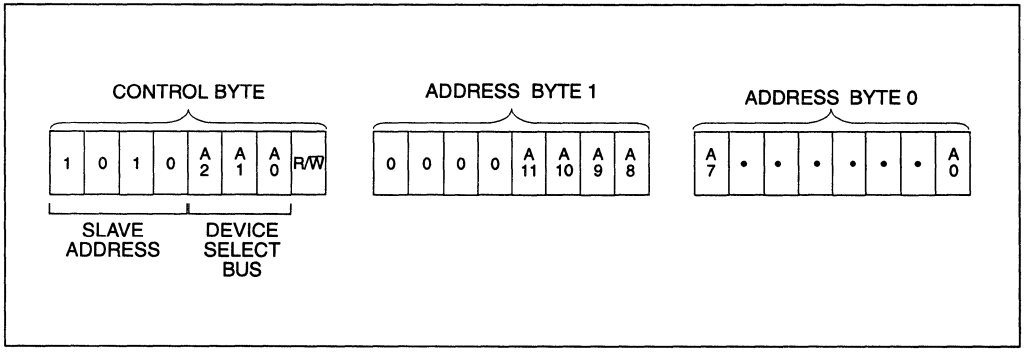
FIGURE 3-2: CONTROL BYTE ALLOCATION



Following the start condition, the 24LC32A monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC32A will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC32A. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC32A the master device will transmit the data word to be written into the addressed memory location.

The 24LC32A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC32A will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC32A in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 32 bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin. (Figure 4-2).

FIGURE 4-1: BYTE WRITE

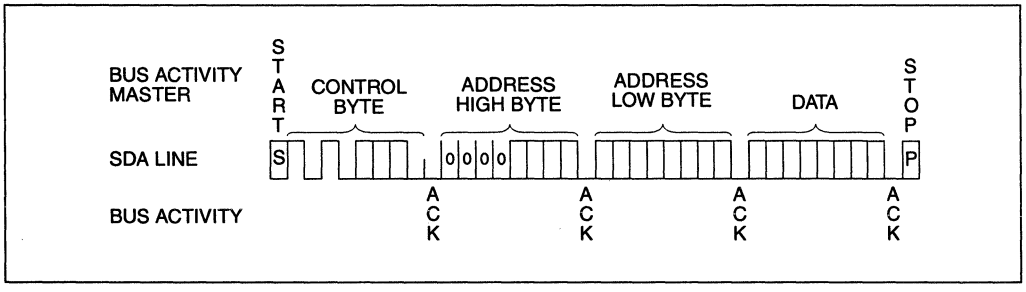
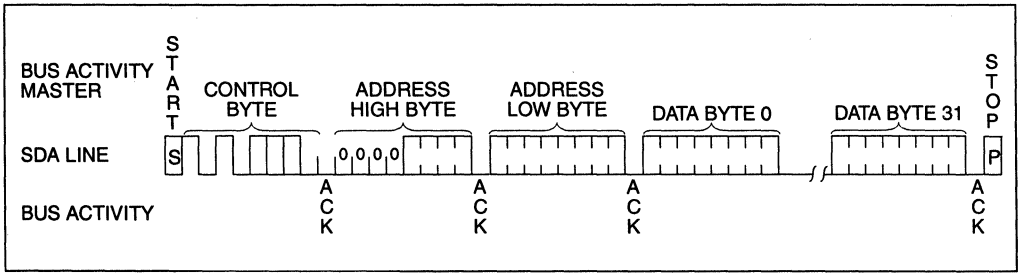


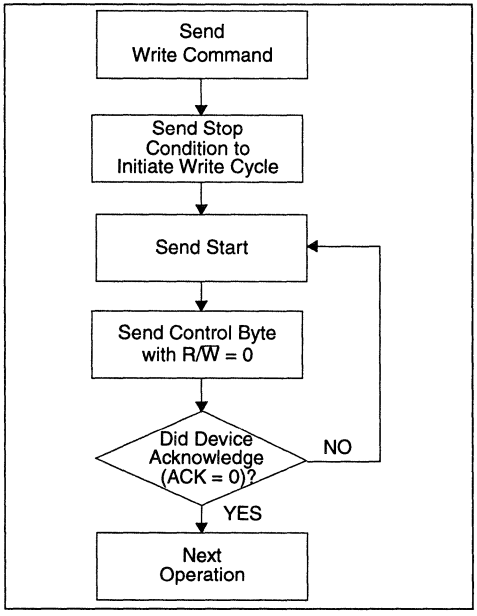
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. Acknowledge Polling (ACK) can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then NO ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

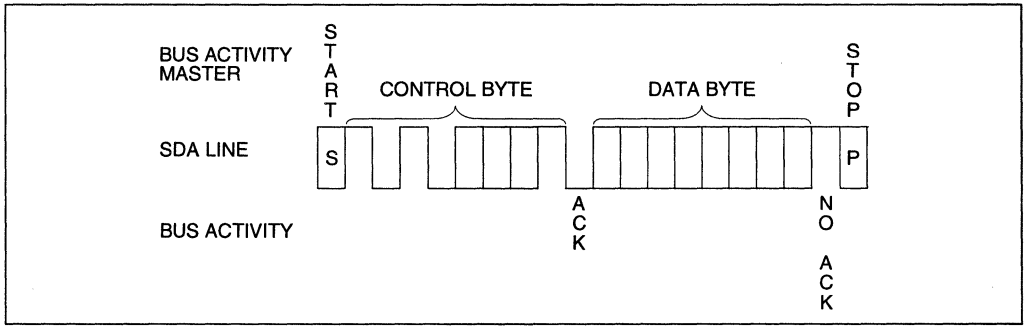
6.1 Current Address Read

The 24LC32A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC32A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC32A discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC32A as part of a write operation (R/$\overline{W}$ bit set to zero). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC32A will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC32A to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24LC32A's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC32A transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC32A to transmit the next sequentially addressed 8-bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC32A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFF to address 000 if the master acknowledges the byte received from the array address 0FFF.

FIGURE 6-2: RANDOM READ

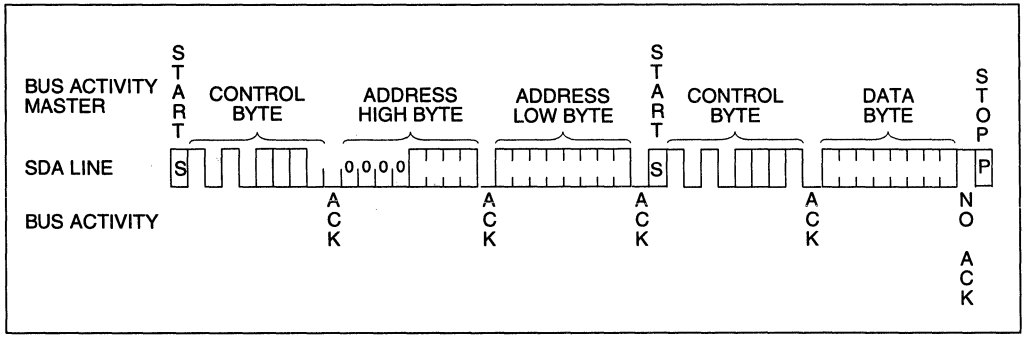
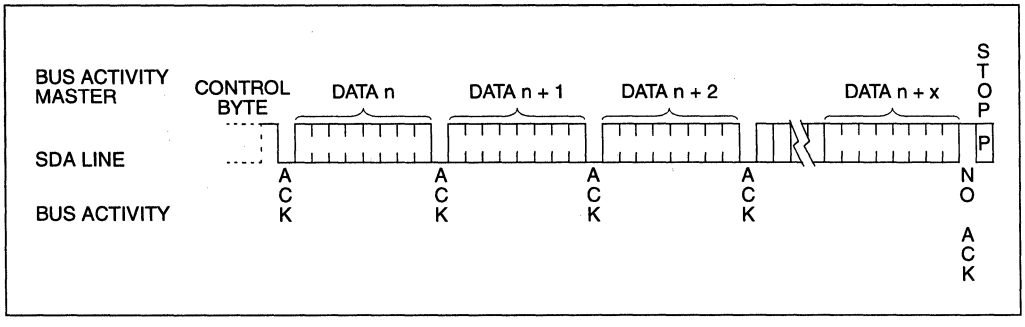


FIGURE 6-3: SEQUENTIAL READ



7.0 PIN DESCRIPTIONS

7.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC32A for multiple device operation and conform to the 2-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

7.2 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

7.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

7.4 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-FFF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

8.0 NOISE PROTECTION

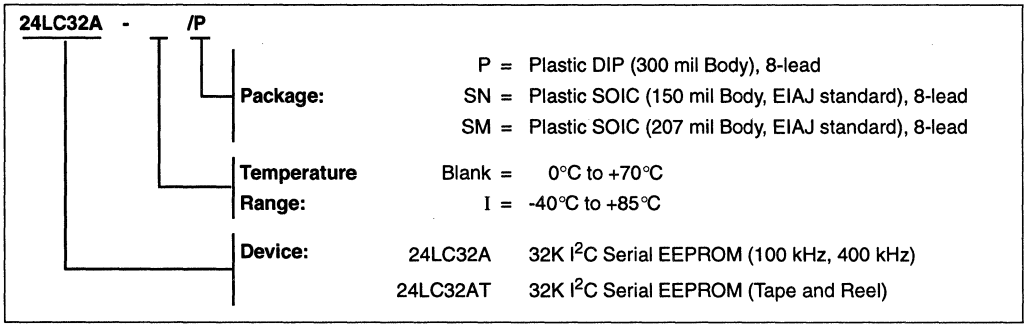
The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

9.0 POWER MANAGEMENT

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e., not receiving an acknowledge or stop condition per the 2-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

24LC32A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24C32A

32K 5.0V I²C™ Serial EEPROM

FEATURES

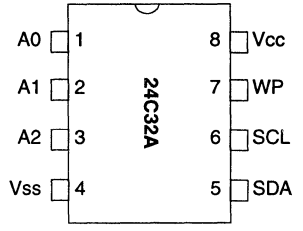
- Voltage operating range: 4.5V to 5.5V
  - Maximum write current 3 mA at 5.5V
  - Standby current 1 µA typical at 5.0V
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz and 400 kHz compatibility
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Hardware write protect
- 1,000,000 Erase/Write cycles guaranteed
- 32-byte page or byte write modes available
- Schmitt trigger filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to eight devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to 70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

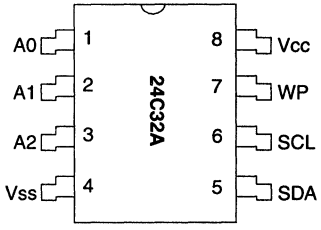
The Microchip Technology Inc. 24C32A is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. It has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32A also has a page-write capability of up to 32 bytes of data. The 24C32A is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24C32A devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low-voltage, nonvolatile code and data applications. The 24C32A is available in the standard 8-pin plastic DIP and both 150 mil and 200 mil SOIC packaging.

PACKAGE TYPES

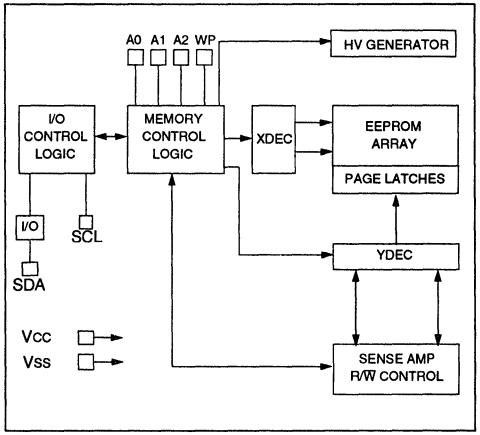
PDIP



SOIC



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+4.5V to 5.5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

VCC = +4.5V to 5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive(E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
A0, A1, A2, SCL , SDA and WP pins:						
High level input voltage	VIH	.7 VCC		—	V	
Low level input voltage	VIL	—		.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC		—	V	(Note)
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10		10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10		10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—		10	pF	VCC = 5.0V (Note) Tamb = 25°C, F_c = 1 MHz
Operating current	ICC Write	—		3	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Read	—		0.5	mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	1	5	µA	SCL = SDA = VCC = 5.5V WP = VSS, A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

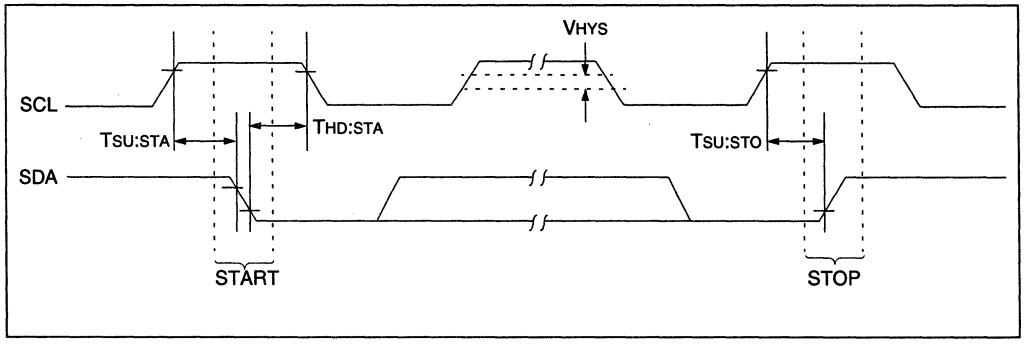


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 4.5-5.5		Units	Remarks
		Min	Max		
Clock frequency	FCLK	—	100	kHz	
Clock high time	THIGH	4000	—	ns	
Clock low time	TLOW	4700	—	ns	
SDA and SCL rise time	TR	—	1000	ns	(Note 1)
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	ns	
Data input setup time	TSU:DAT	250	—	ns	
STOP condition setup time	TSU:STO	4000	—	ns	
Output valid from clock	TAA	—	3500	ns	(Note 2)
Bus free time	TBUF	4700	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	ms	
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

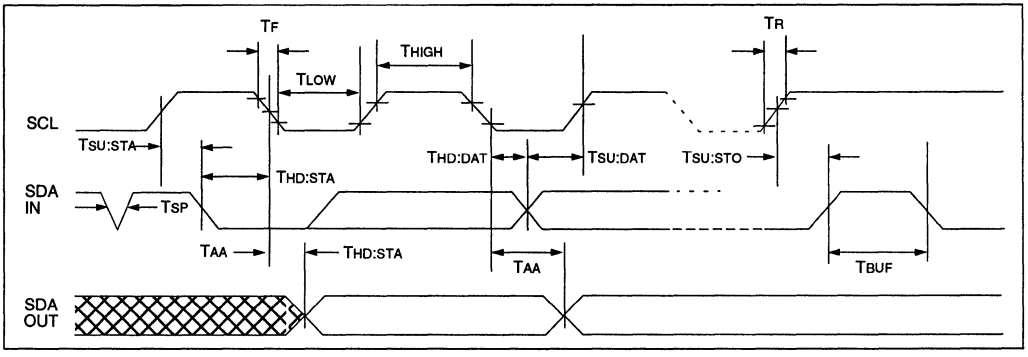
Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24C32A supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C32A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

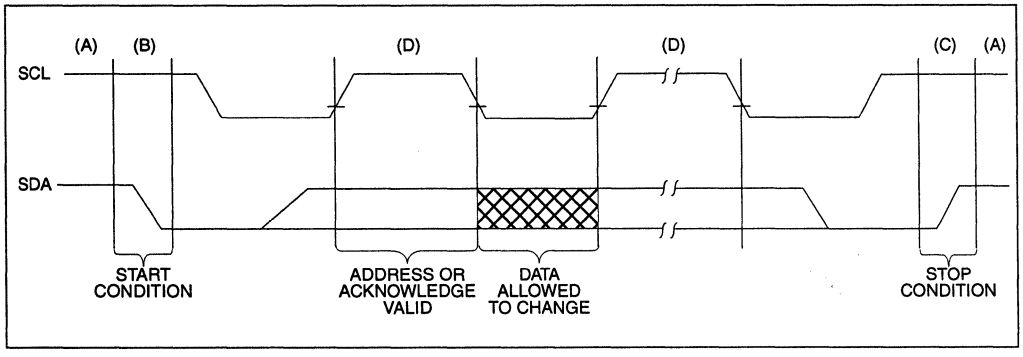
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24C32A does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C32A) will leave the data line HIGH to enable the master to generate the STOP condition.

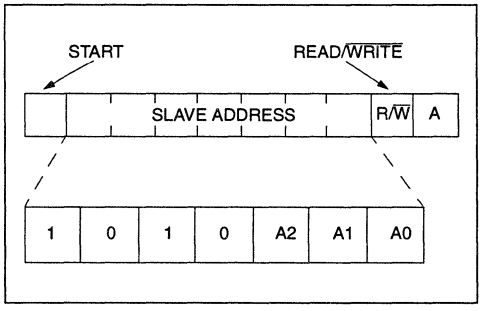
FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code; for the 24C32A this is set as 1010 binary for read and write (R/$\overline{W}$) operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

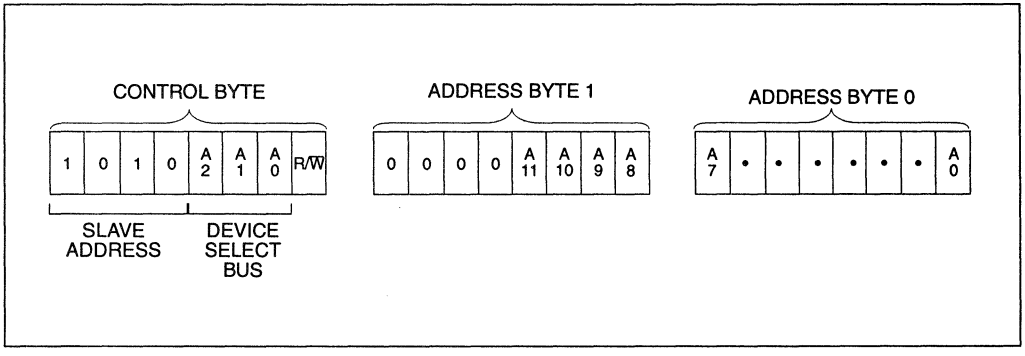
FIGURE 3-2: CONTROL BYTE ALLOCATION



Following the start condition, the 24C32A monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C32A will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24C32A. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24C32A the master device will transmit the data word to be written into the addressed memory location.

The 24C32A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C32A will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C32A in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 32 bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin. (Figure 4-2).

FIGURE 4-1: BYTE WRITE

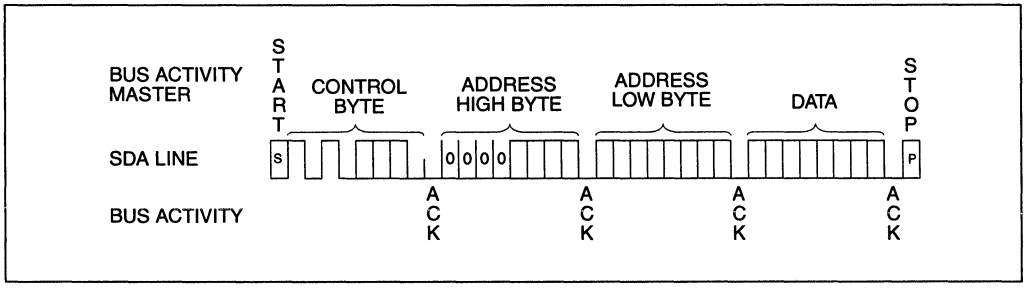
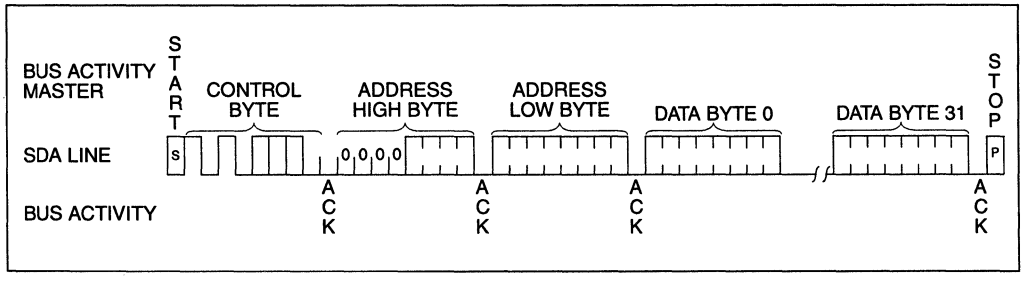


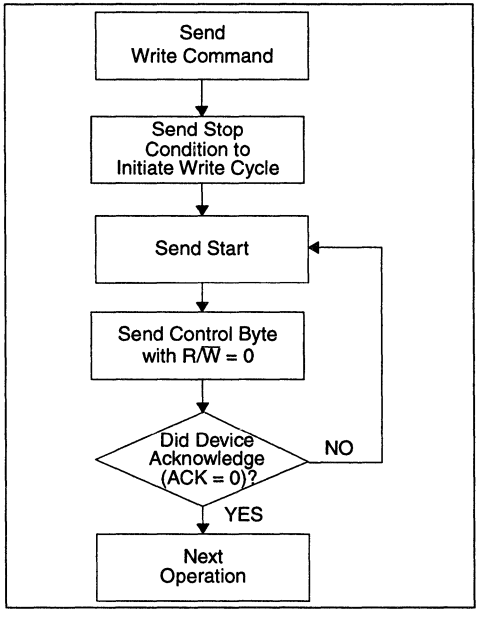
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. Acknowledge Polling (ACK) can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then NO ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

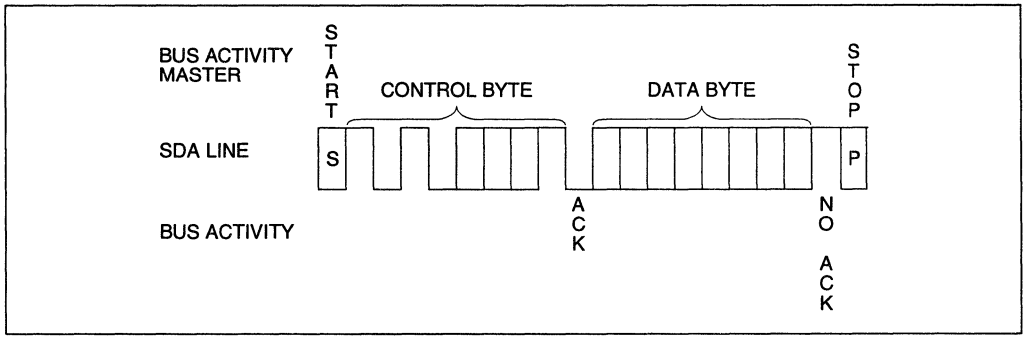
6.1 Current Address Read

The 24C32A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C32A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C32A discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C32A as part of a write operation (R/$\overline{W}$ bit set to zero). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C32A will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24C32A to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24C32A's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C32A transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24C32A to transmit the next sequentially addressed 8-bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24C32A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFF to address 000 if the master acknowledges the byte received from the array address 0FFF.

FIGURE 6-2: RANDOM READ

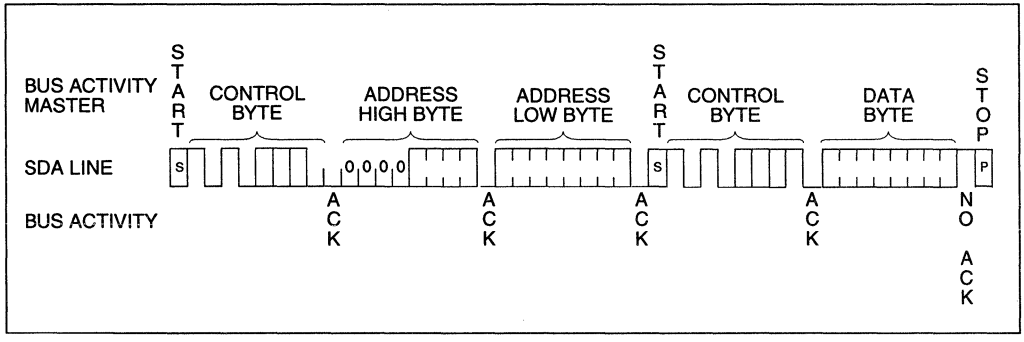
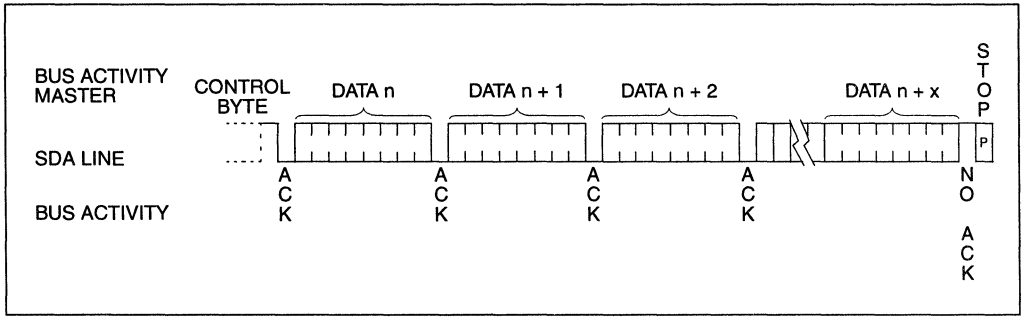


FIGURE 6-3: SEQUENTIAL READ



7.0 PIN DESCRIPTIONS

7.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24C32A for multiple device operation and conform to the 2-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

7.2 SDA Serial Address/Data Input/ Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

7.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

7.4 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-FFF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

8.0 NOISE PROTECTION

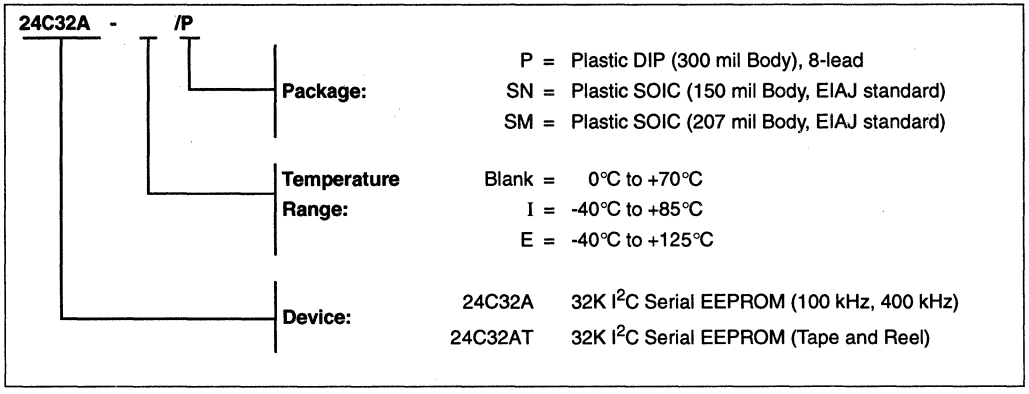
The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

9.0 POWER MANAGEMENT

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e., not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

24C32A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24AA32

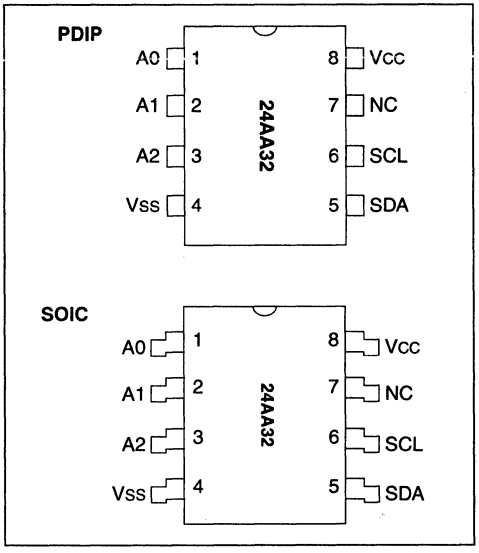
32K 1.8V I²C™ Smart Serial™ EEPROM

FEATURES

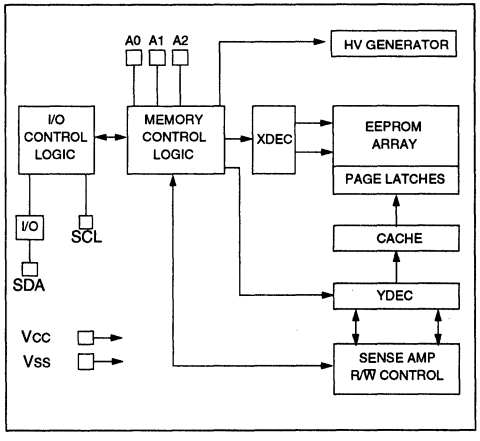
- Voltage operating range: 1.8V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 kHz (1.8V) and 400 kHz (5V) modes
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 Erase/Write (E/W) cycles guaranteed for High Endurance Block
  - 1,000,000 E/W cycles guaranteed for Standard Endurance Block
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Factory programming (QTP) available
- Up to 8 devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C

DESCRIPTION

The Microchip Technology Inc. 24AA32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 6.0V). This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24AA32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K bit block of ultra-high endurance memory for data that changes frequently. The 24AA32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24AA32 devices on the same bus, for up to 256K bits address space.



BLOCK DIAGRAM



Advanced CMOS technology and broad voltage range make this device ideal for low-power/low voltage, non-volatile code PACKAGE TYPEsand data applications. The 24AA32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+1.8V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +1.8V to 6.0V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC Write ICC Read	— —	3 150	mA µA	VCC = 6.0V, SCL = 400 kHz VCC = 6.0V, SCL = 400 kHz
Standby current	ICCS	—	5 2	µA µA	VCC = 5.0V, SCL = SDA = VCC A0, A1, A2 = VSS (Note) VCC = 1.8V, SCL = SDA = VCC A0, A1, A2 = VSS (Note)

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

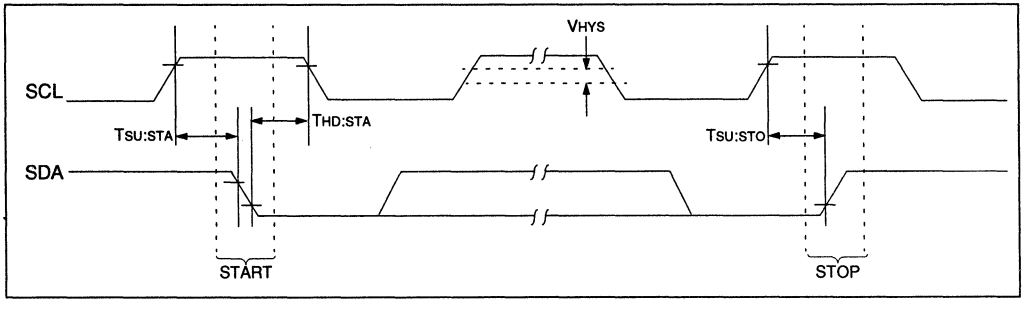
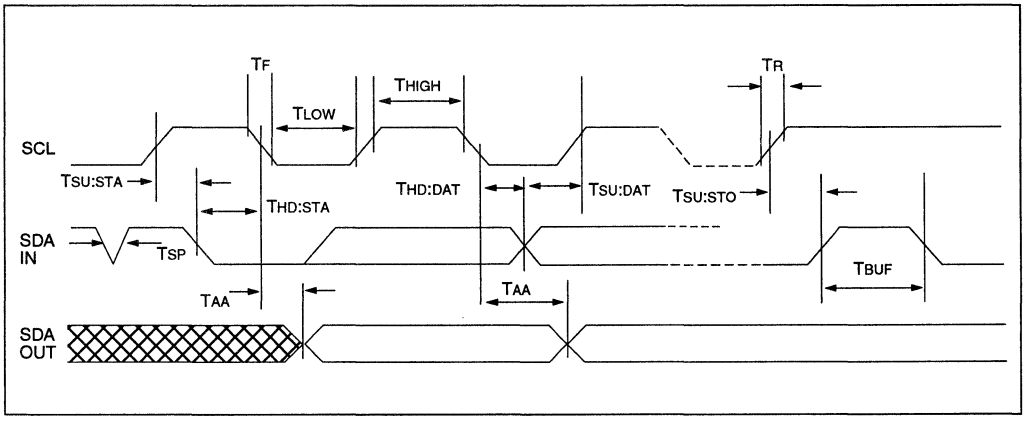


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 1.8V-6.0V STD. MODE		Vcc = 4.5 - 6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms/page	(Note 4)
Endurance High Endurance Block Rest of Array	 — —	 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Cycle Mode (Note 5)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.
4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.
5: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24AA32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

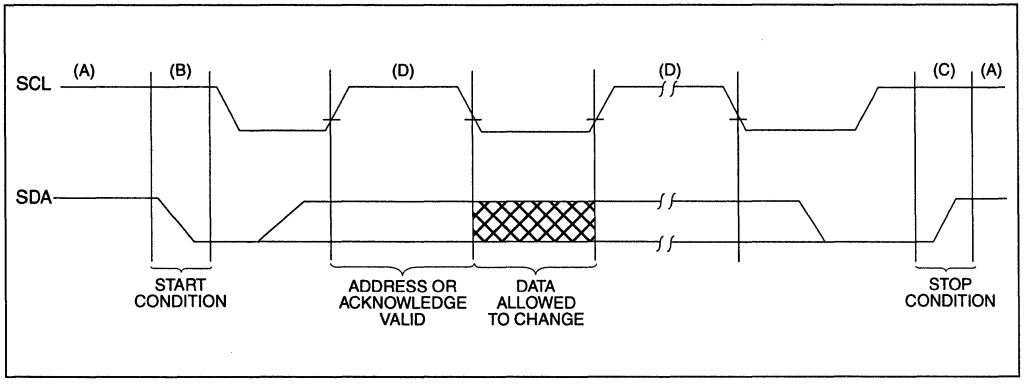
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24AA32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

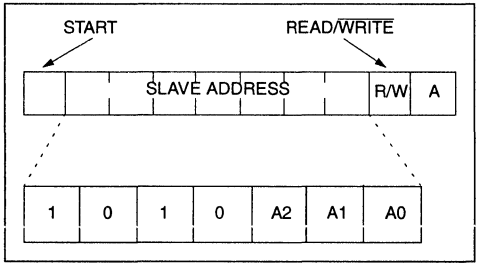


3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24AA32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

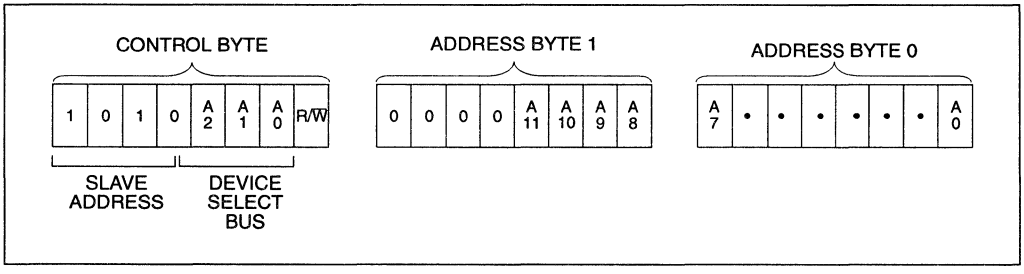
Following the start condition, the 24AA32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA32 will select a read or write operation.

FIGURE 3-2: CONTROL BYTE ALLOCATION



Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATION

4.1 Split Endurance

The 24AA32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 10,000,000 E/W cycles guaranteed. The remainder of the array, 28K bits, is rated at 100,000 E/W cycles guaranteed. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

4.2 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24AA32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24AA32 the master device will transmit the data word to be written into the addressed memory location.

The 24AA32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA32 will not generate acknowledge signals (Figure 4-1).

4.3 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24AA32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE

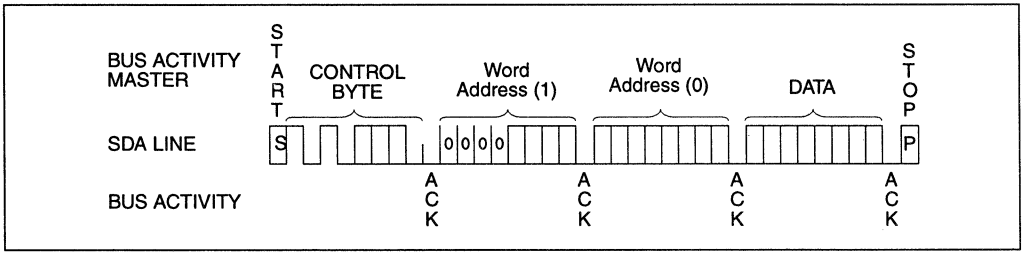
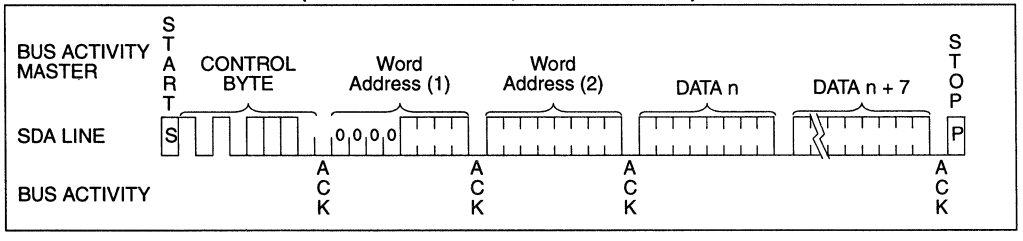


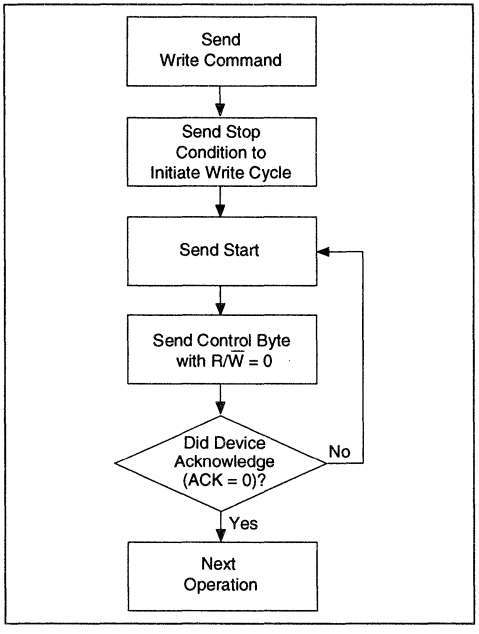
FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 7-1)



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

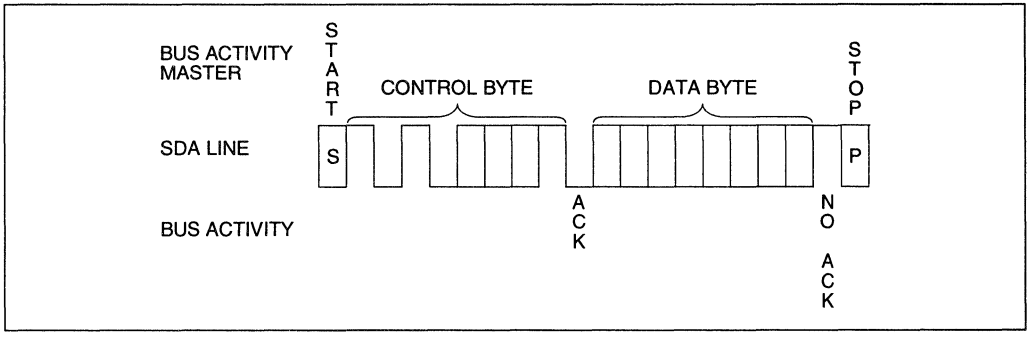
6.1 Current Address Read

The 24AA32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA32 discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24AA32 to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24AA32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24AA32 to transmit the next sequentially addressed 8 bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24AA32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

6.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

FIGURE 6-2: RANDOM READ

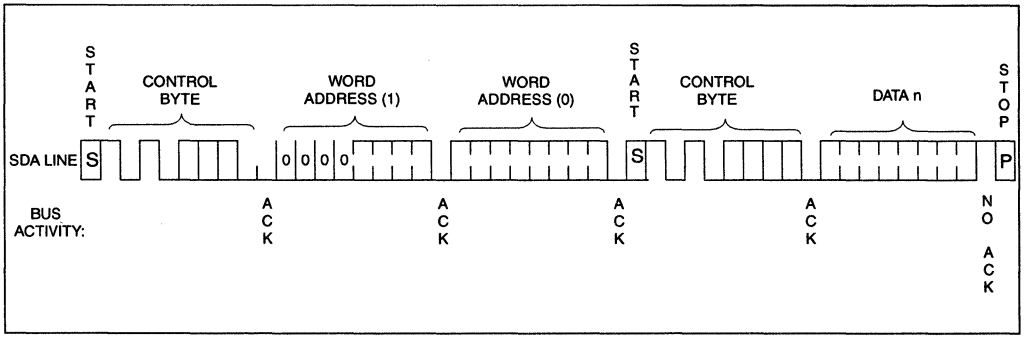
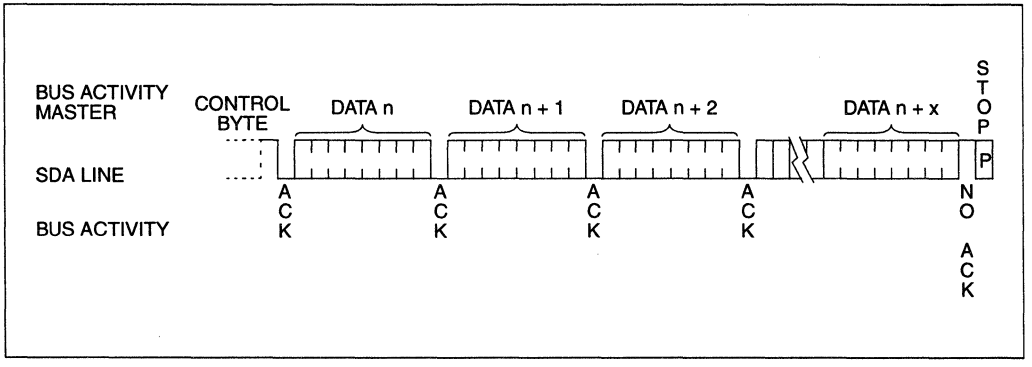


FIGURE 6-3: SEQUENTIAL READ



6.6 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

6.7 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 4-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

6.8 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 7-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

6.9 Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

7.0 PIN DESCRIPTIONS

7.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24AA32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

7.2 SDA Serial Address/Data Input/ Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

7.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 7-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

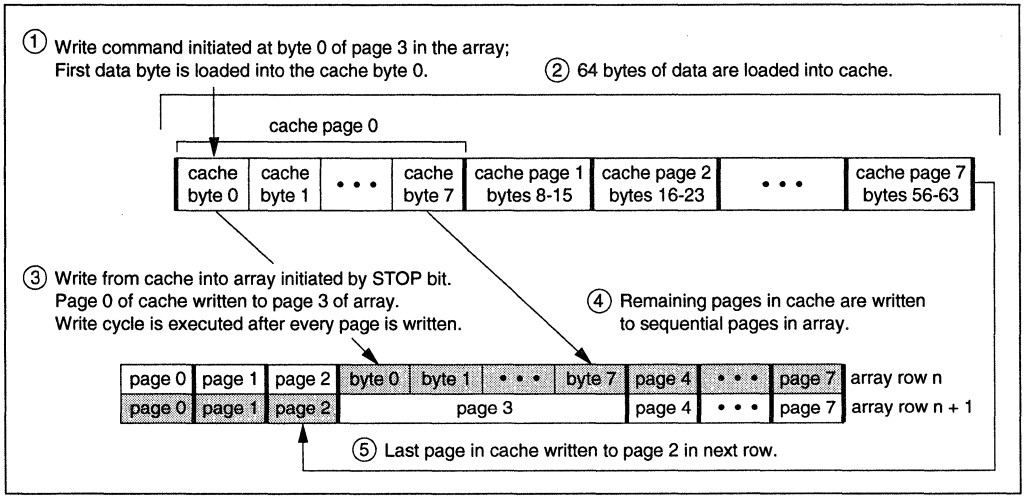
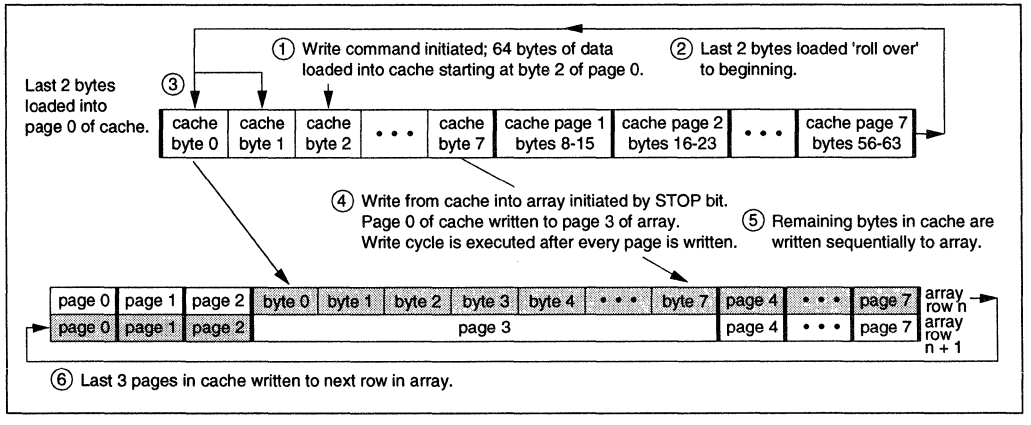


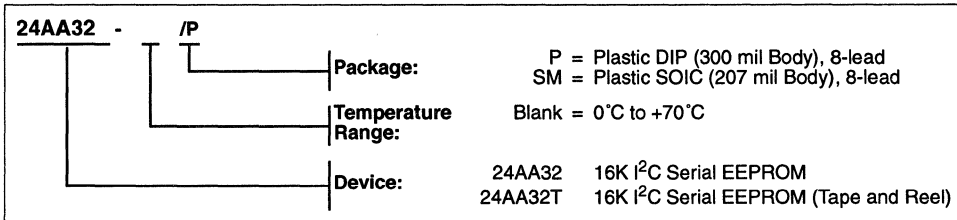
FIGURE 7-2: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



NOTES:

24AA32 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC32

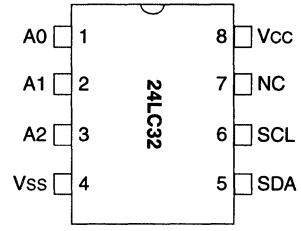
32K 2.5V I²C™ Smart Serial EEPROM

FEATURES

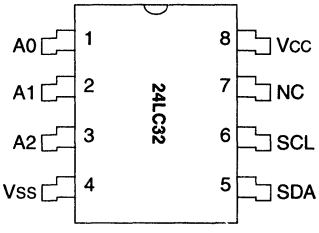
- Voltage operating range: 2.5V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 kHz (2.5V) and 400 kHz (5V) modes
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 Erase/Write cycles guaranteed for High Endurance Block
  - 1,000,000 E/W cycles guaranteed for Standard Endurance Block
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Factory programming (QTP) available
- Up to 8 devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40° to +85°

PACKAGE TYPES

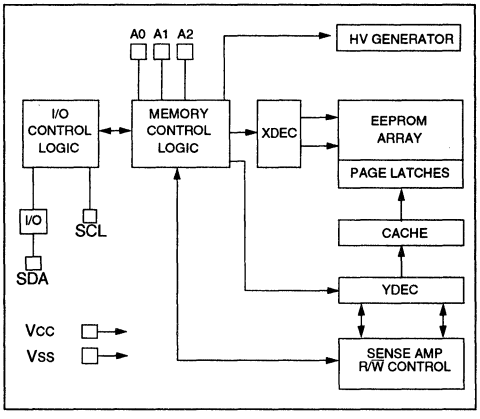
PDIP



SOIC



BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 24LC32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V). This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24LC32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24LC32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24LC32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low voltage, non-volatile code and data applications. The 24LC32 is available the standard 8-pin in plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation. Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+2.5V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +2.5V to 6.0V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC Write ICC Read	— —	3 150	mA µA	VCC = 6.0V, SCL = 400 kHz VCC = 6.0V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.0V, SCL = SDA = VCC A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

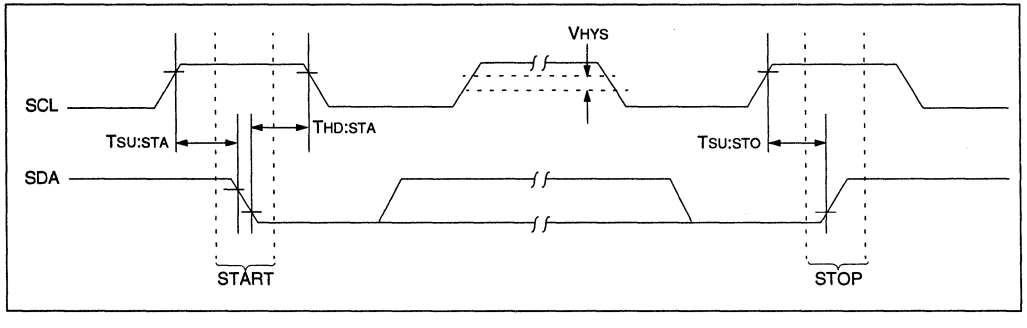


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 2.5V-6.0V STD. MODE		Vcc = 4.5 - 6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms/page	(Note 4)
Endurance High Endurance Block Rest of Array	 — —	 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 5)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

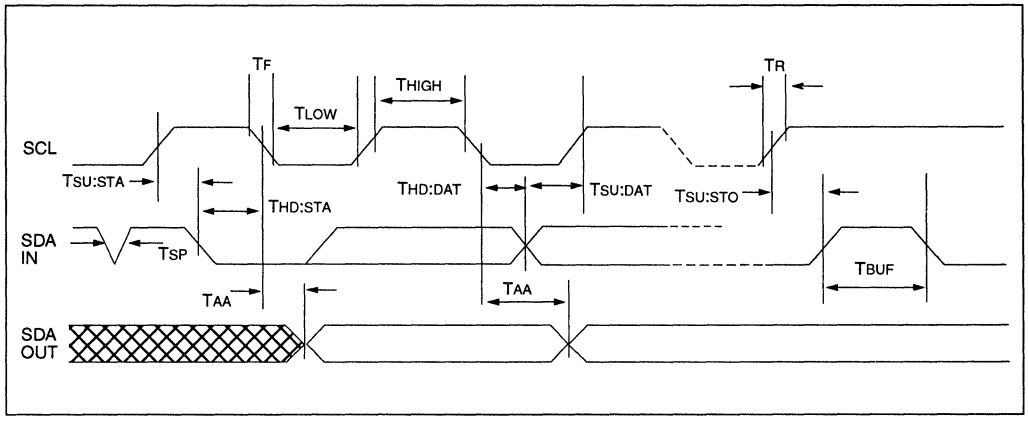
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

5: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained from our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

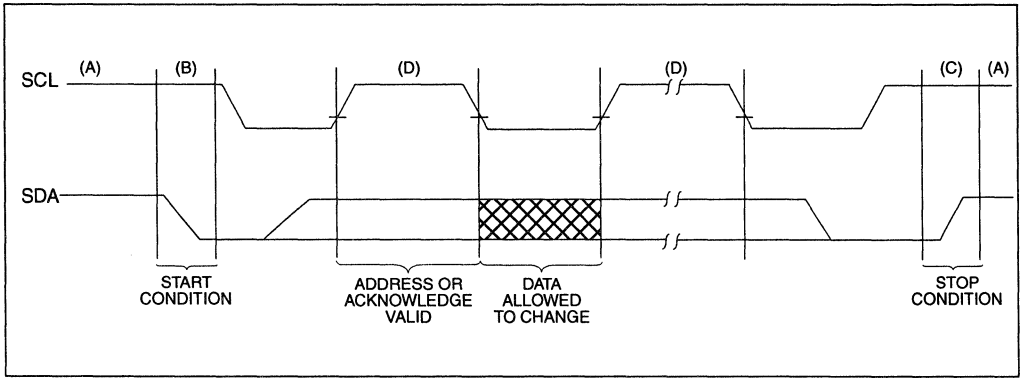
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

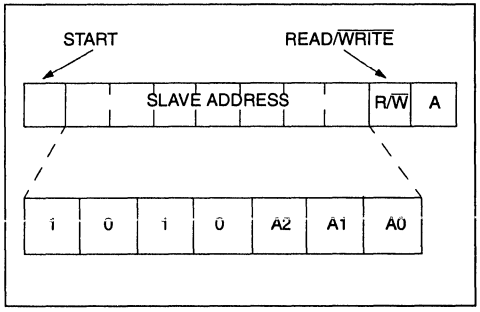


3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24LC32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

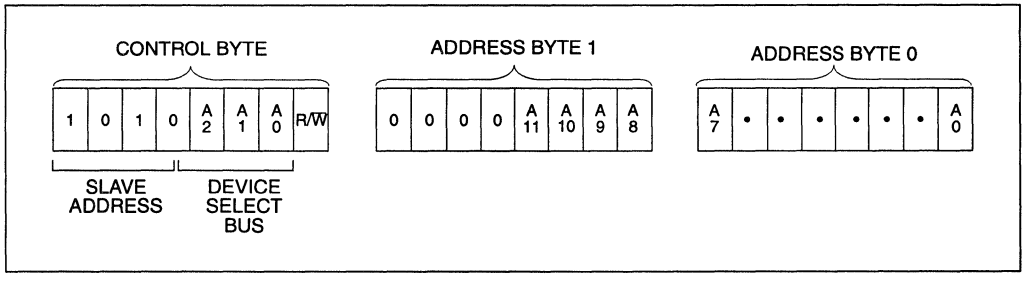
Following the start condition, the 24LC32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC32 will select a read or write operation.

FIGURE 3-2: CONTROL BYTE ALLOCATION



Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATION

4.1 Split Endurance

The 24LC32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 10,000,000 E/W cycles guaranteed. The remainder of the array, 28K bits, is rated at 100,000 E/W cycles guaranteed. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

4.2 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC32 the master device will transmit the data word to be written into the addressed memory location.

The 24LC32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC32 will not generate acknowledge signals (Figure 4-1).

4.3 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24LC32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE

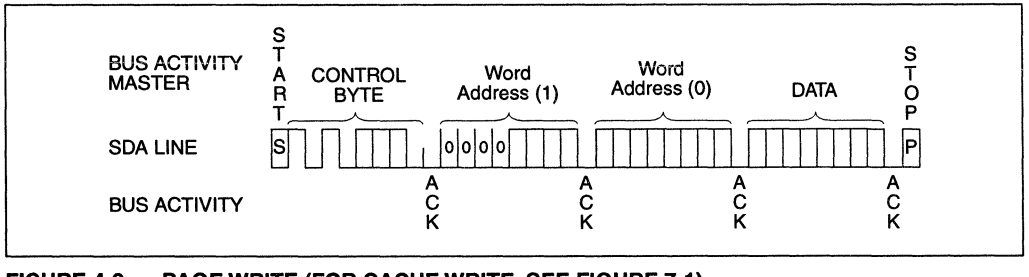
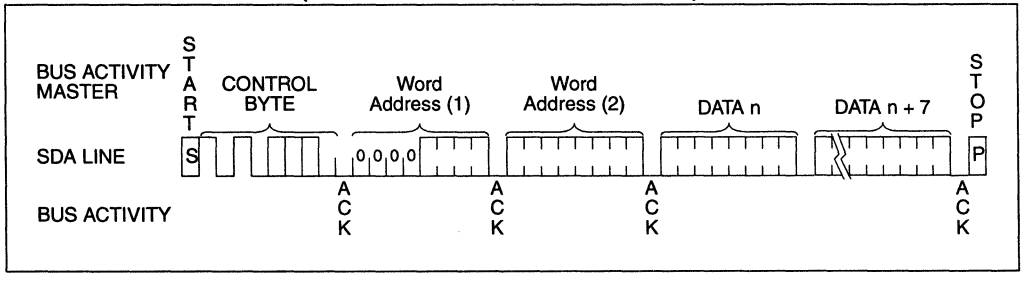


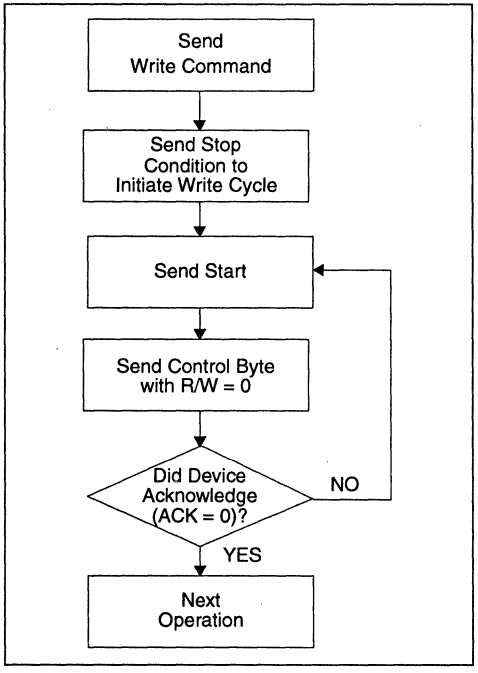
FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 7-1)



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

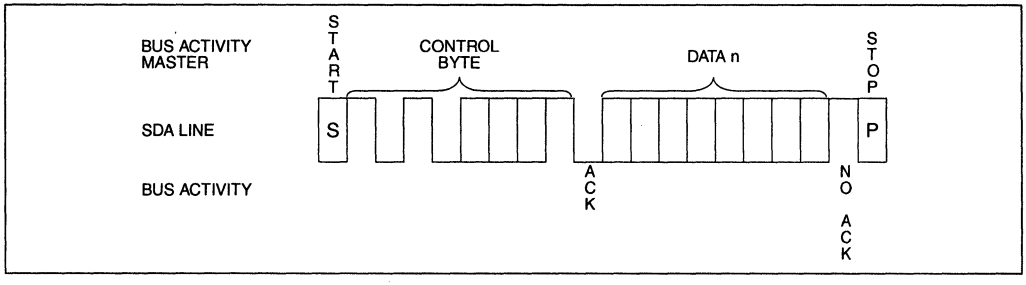
6.1 Current Address Read

The 24LC32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC32 discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC32 to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24LC32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC32 to transmit the next sequentially addressed 8 bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

6.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

FIGURE 6-2: RANDOM READ

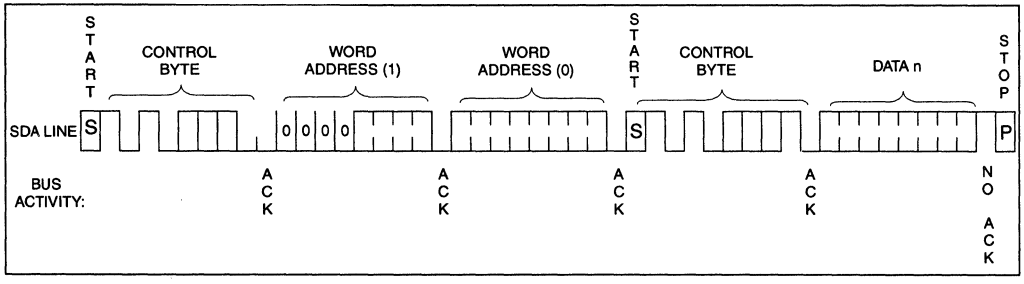
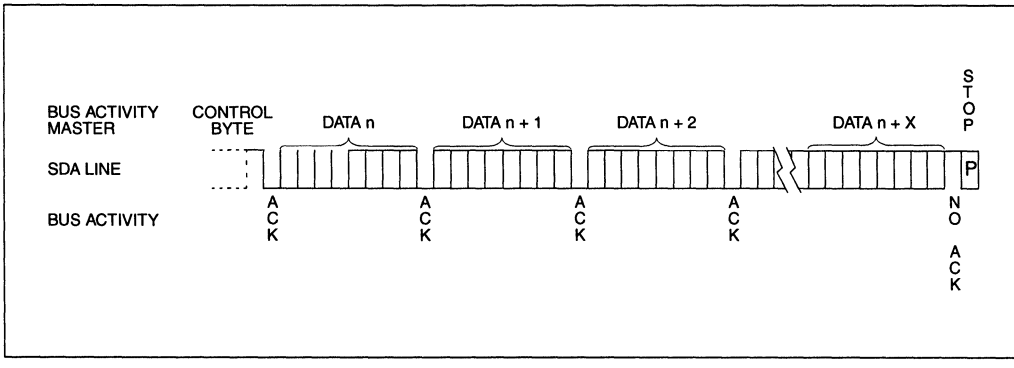


FIGURE 6-3: SEQUENTIAL READ



6.6 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

6.7 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 4-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

6.8 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 7-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

6.9 Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

7.0 PIN DESCRIPTIONS

7.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

7.2 SDA Serial Address/Data Input/ Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

7.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 7-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

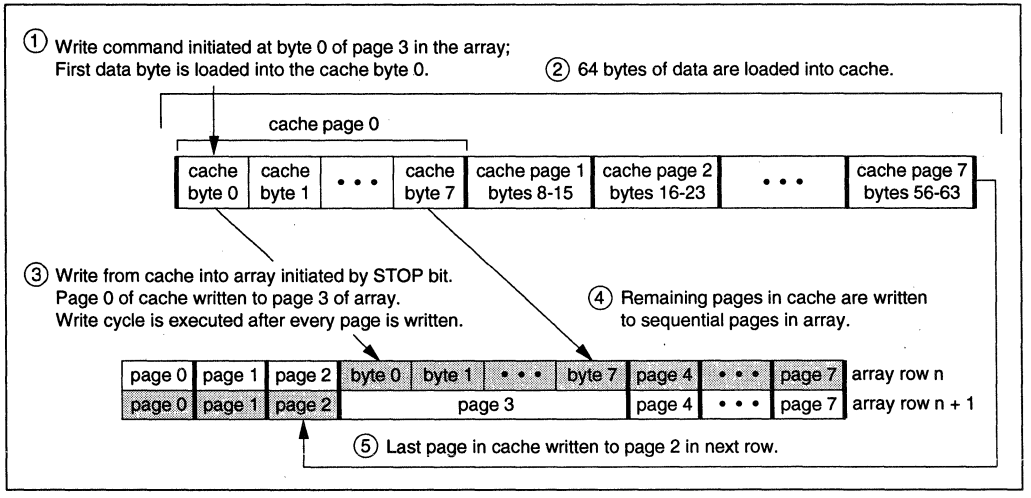
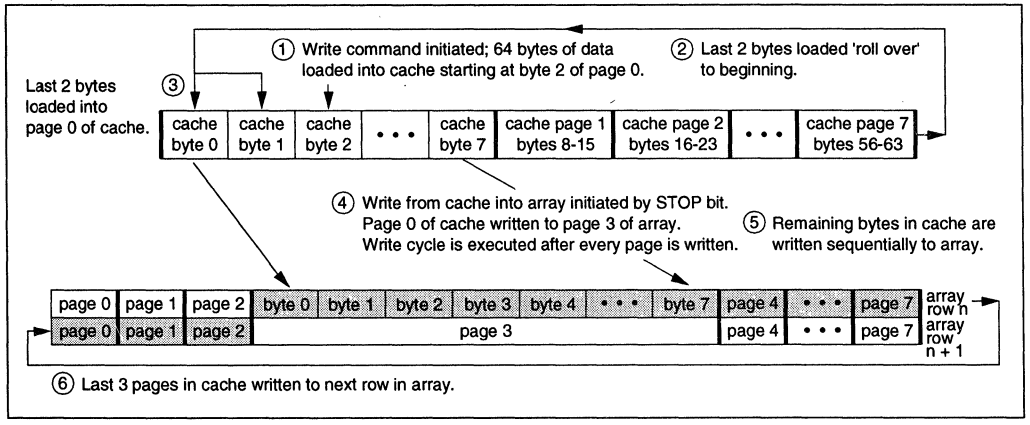


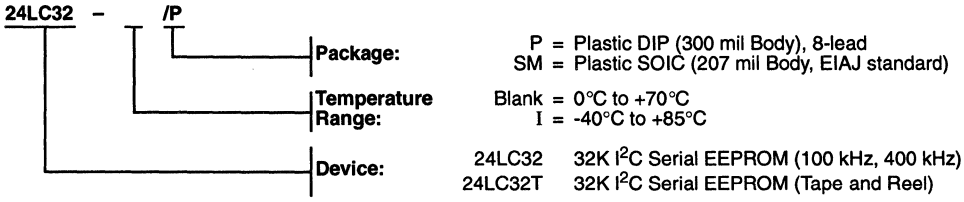
FIGURE 7-2: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



NOTES:

24LC32 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24C32

32K 5.0V I²C™ Smart Serial™ EEPROM

FEATURES

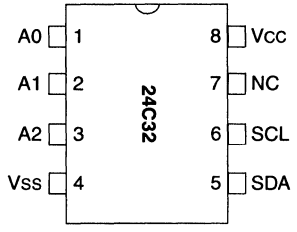
- Voltage operating range: 4.5V to 5.5V
  - Peak write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 1 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 kHz and 400 kHz modes
- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 Erase/Write cycles guaranteed for High Endurance Block
  - 1,000,000 E/W cycles guaranteed for Standard Endurance Block
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

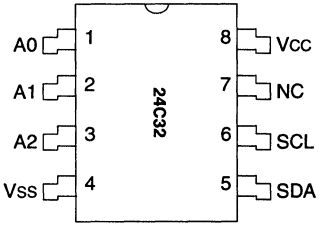
The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24C32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package

PACKAGE TYPES

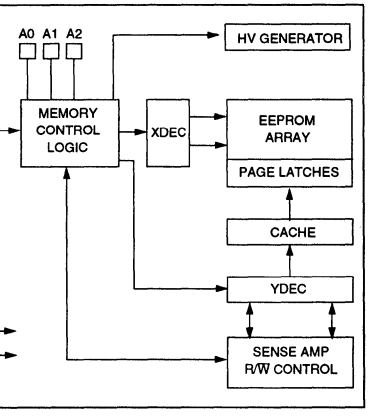
PDIP



SOIC



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V TO VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE ICC Read	— —	3 150	mA µA	VCC = 5.5V, SCL = 400 kHz VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.5V, SCL = SDA = VCC A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

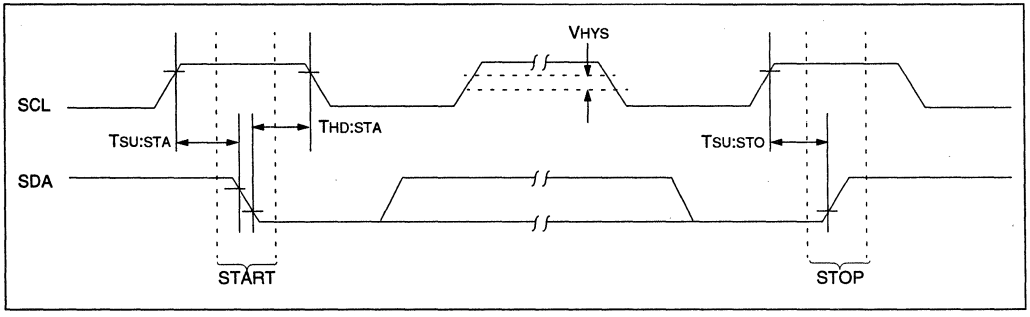


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STD. MODE		FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms/page	(Note 4)
Endurance High Endurance Block Rest of Array	 — —	 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 5)

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

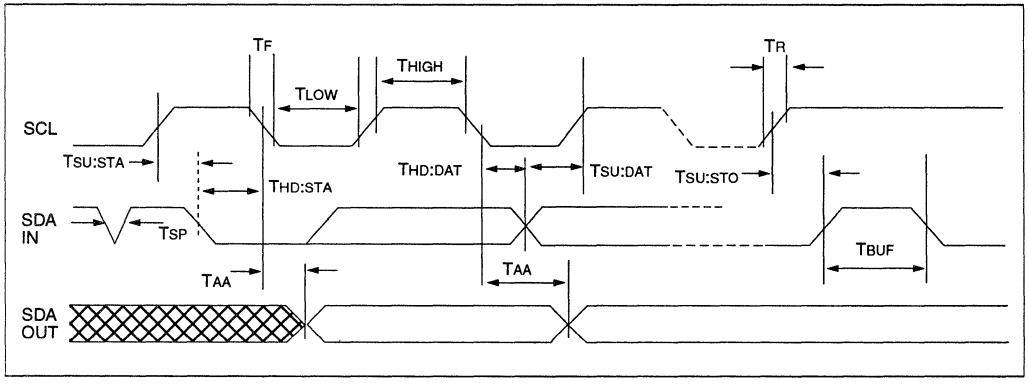
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

5: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24C32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

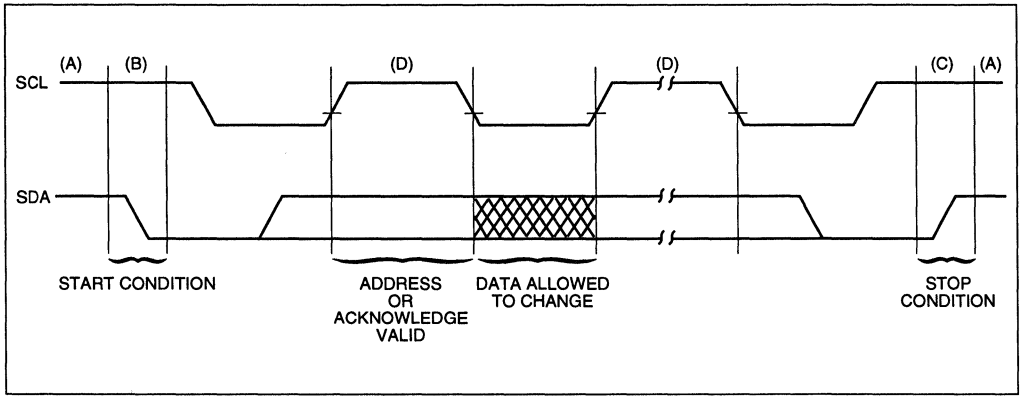
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24C32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24C32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11..A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first. Following the start condition, the 24C32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C32 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION

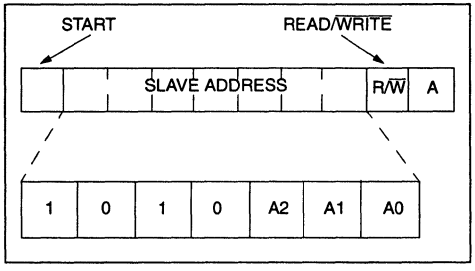
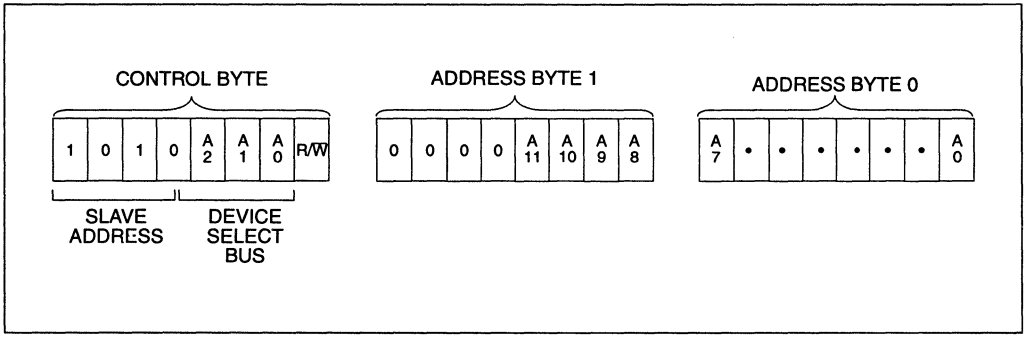


FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATION

4.1 Split Endurance

The 24C32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 10,000,000 E/W cycles guaranteed. The remainder of the array, 28K bits, is rated at 100,000 E/W cycles guaranteed. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

4.2 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24C32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24C32 the master device will transmit the data word to be written into the addressed memory location. The 24C32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C32 will not generate acknowledge signals (Figure 4-1).

4.3 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24C32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE

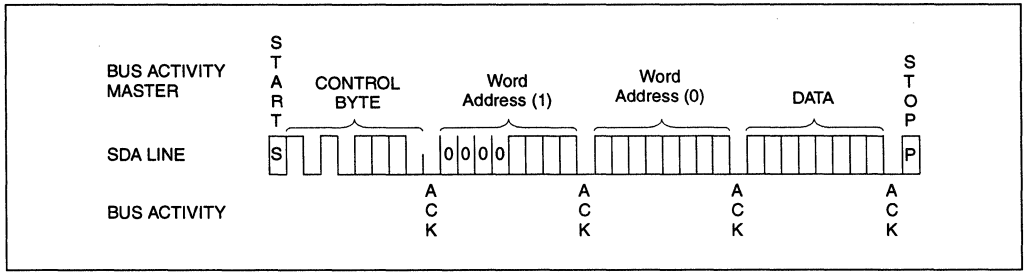
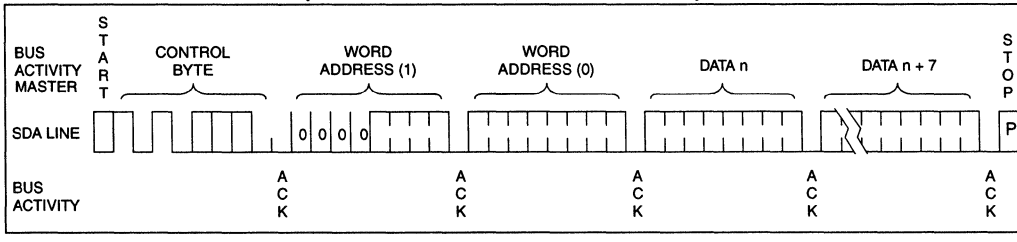


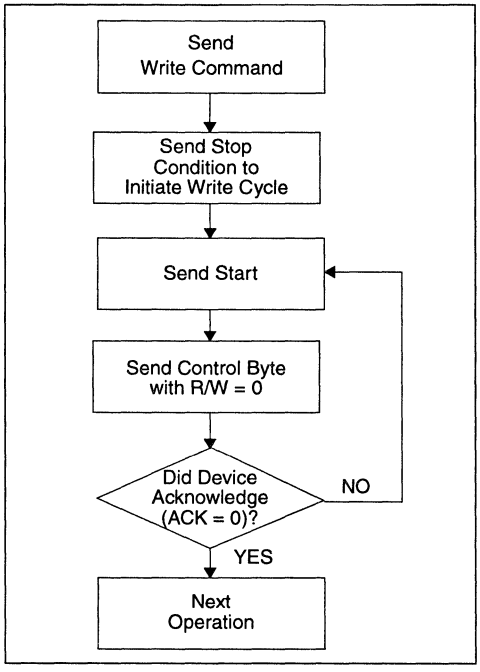
FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 8-1)



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

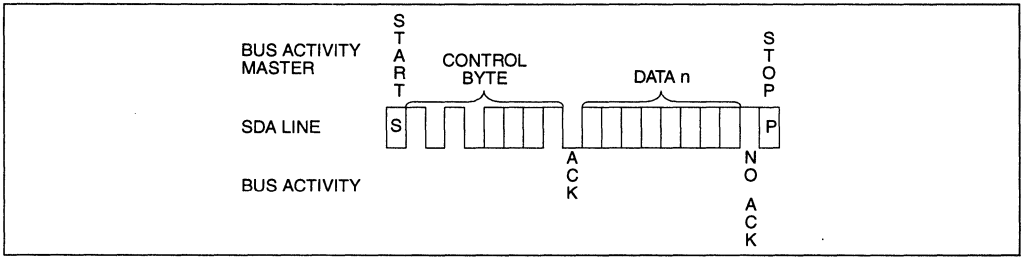
6.1 Current Address Read

The 24C32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C32 discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24C32 to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24C32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24C32 to transmit the next sequentially addressed 8 bit word. (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24C32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

6.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

FIGURE 6-2: RANDOM READ

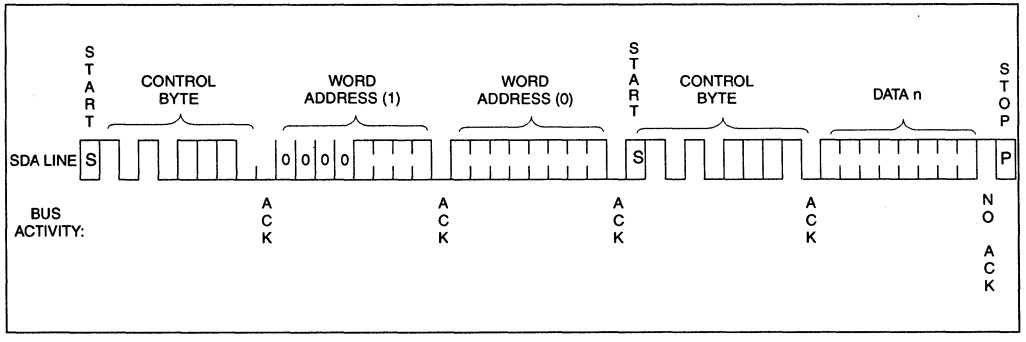
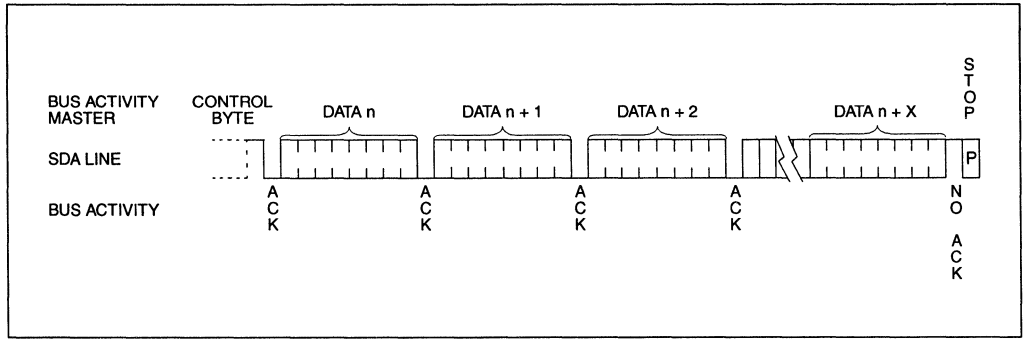


FIGURE 6-3: SEQUENTIAL READ



7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 8-1) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache wil l'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24C32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

8.2 SDA Serial Address/Data Input/ Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to V_{CC} (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

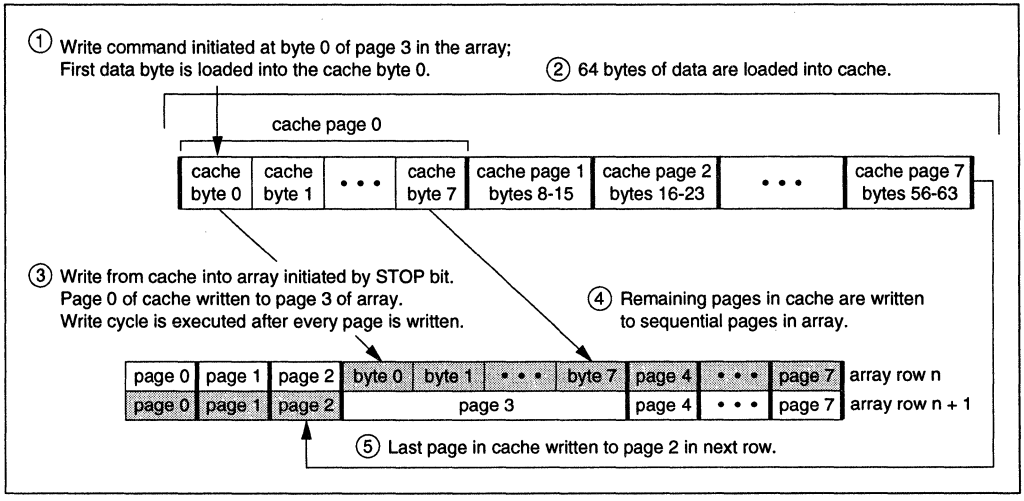
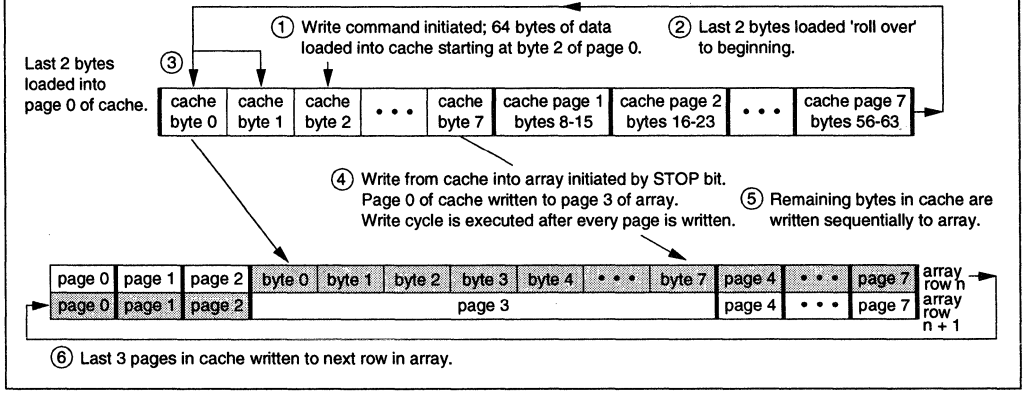


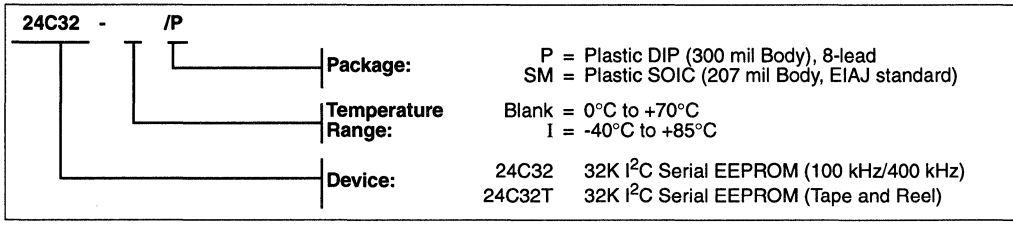
FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



NOTES:

24C32 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24FC32

32K 5.0V 1 MHz I²C™ Smart Serial™ EEPROM

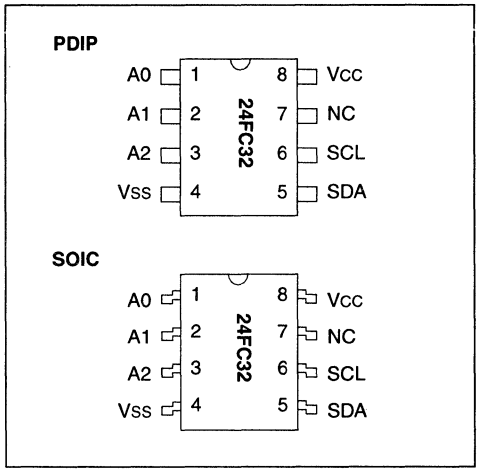
FEATURES

- Voltage operating range: 4.5V to 5.5V
  - Maximum write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 1 µA typical
- 1 MHz SE2.bus two wire protocol
- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 Erase/Write cycles guaranteed for a 4K block
  - 1,000,000 E/W cycles guaranteed for a 28K block
- 8-byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger inputs for noise suppression
- 2 ms typical write cycle time, byte or page
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

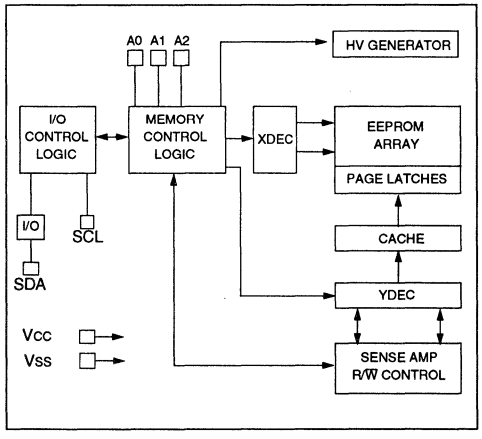
DESCRIPTION

The Microchip Technology Inc. 24FC32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM (EEPROM) with a high-speed 1 MHz SE2.bus whose protocol is functionally equivalent to the industry-standard I²C bus. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24FC32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24FC32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24FC32 devices on the same bus, for up to 256K bits address space. The 24FC32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

PACKAGE TYPES



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	0.7 Vcc	—	V	
Low level input voltage	VIL	—	0.3 Vcc	V	
Hysteresis of SCL and SDA	VHYS	0.05 Vcc	—	V	(Note)
Low level output voltage of SDA	VOL	—	0.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = 0.1V TO VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE ICC Read	— —	3 150	mA µA	VCC = 5.5V, SCL = 1 MHz VCC = 5.5V, SCL = 1 MHz
Standby current	ICCS	—	5 (1 typical)	µA	VCC = 5.5V, SCL = SDA = VCC A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

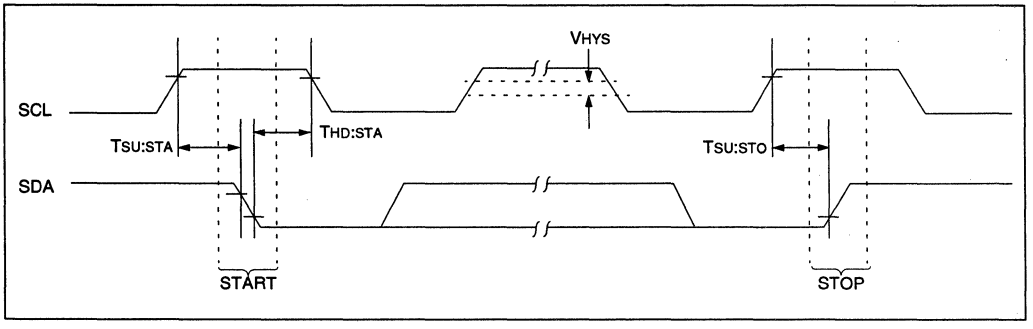


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	1 MHz Bus		Units	Remarks
		Min	Max		
Clock frequency	FCLK	0	1000	kHz	
Clock high time	THIGH	500	—	ns	
Clock low time	TLOW	500	—	ns	
SDA and SCL rise time	TR	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	100	ns	(Note 1)
START condition hold time	THD:STA	250	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	250	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	ns	
Data input setup time	TSU:DAT	100	—	ns	
STOP condition setup time	TSU:STO	250	—	ns	
Output valid from clock	TAA	—	350	ns	(Note 2)
Bus free time	TBUF	500	—	ns	Time the bus must be free before a new transmission can start
Write cycle time	TWR	—	5	ms/page	Note 3
Endurance High Endurance Block Rest of Array	 — —	 10M 1M	 — —	 10M 1M	 25°C, Vcc = 5.0V, Block Mode (Note 4)

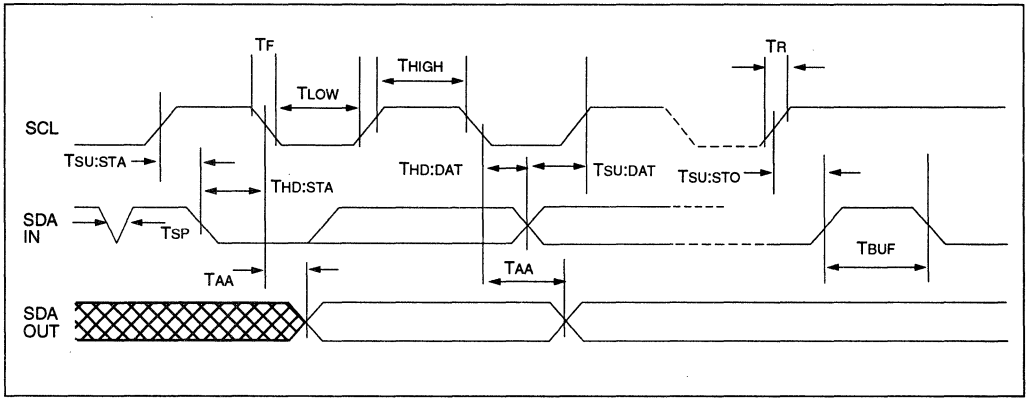
Note 1: Not 100 percent tested.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 100 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24FC32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24FC32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

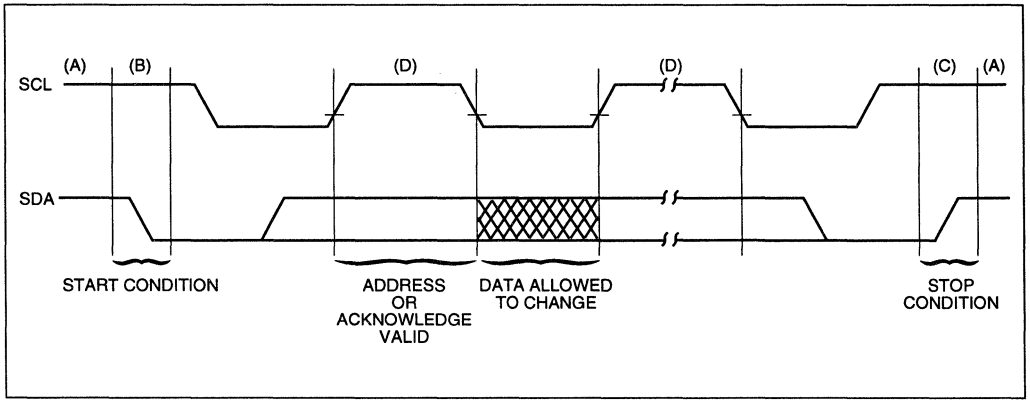
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24FC32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24FC32) will leave the data line HIGH to enable the master to generate the STOP condition.

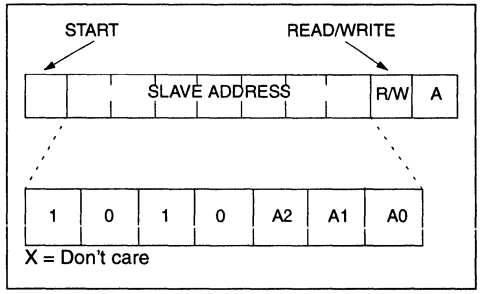
FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

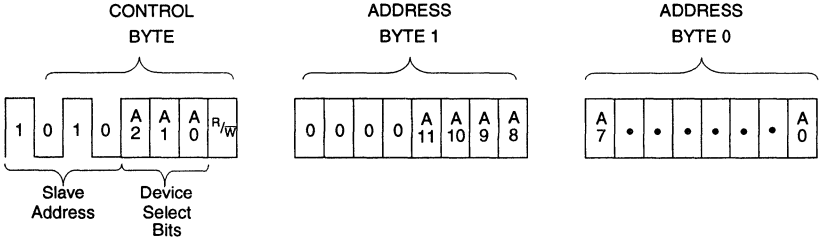
A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24FC32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 3-3). Because only A11..A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first. Following the start condition, the 24FC32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24FC32 will select a read or write operation.

FIGURE 3-2: CONTROL BYTE ALLOCATION



Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.0 WRITE OPERATION

4.1 Split Endurance

The 24FC32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 10,000,000 E/W cycles guaranteed. The remainder of the array, 28K bits, is rated at 100K E/W cycles guaranteed. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

4.2 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24FC32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24FC32 the master device will transmit the data word to be written into the addressed memory location. The 24FC32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24FC32 will not generate acknowledge signals (Figure 4-1).

4.3 Page Write

The write control byte, word address and the first data byte are transmitted to the 24FC32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24FC32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE

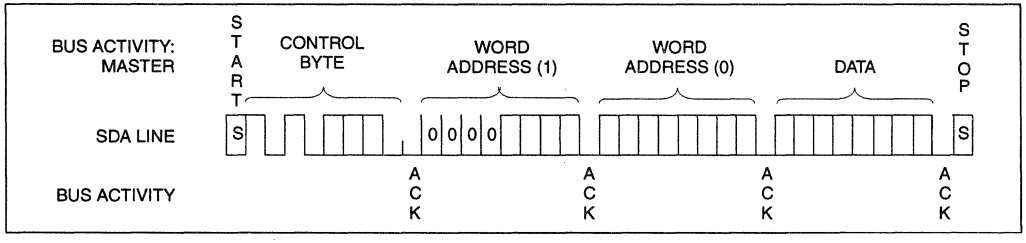
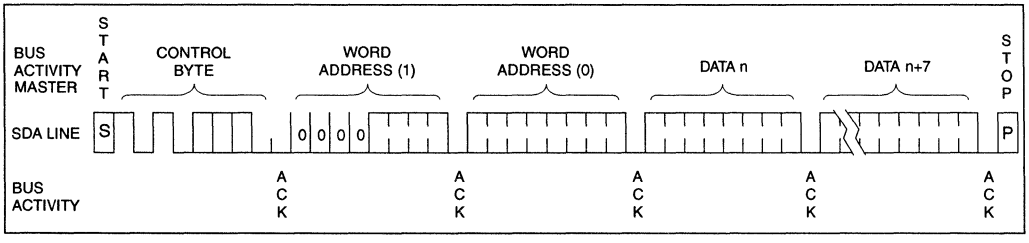


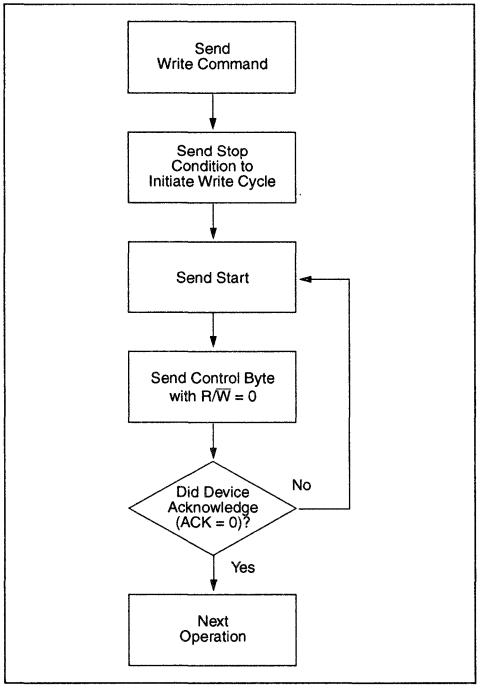
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

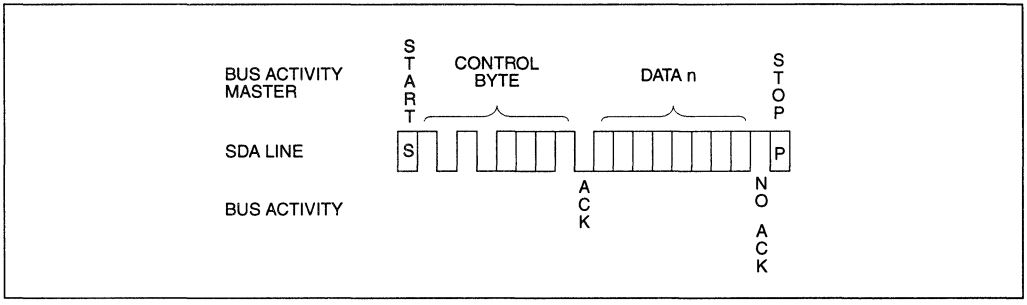
6.1 Current Address Read

The 24FC32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24FC32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24FC32 discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24FC32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24FC32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24FC32 to discontinue transmission (Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24FC32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24FC32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24FC32 to transmit the next sequentially addressed 8 bit word (Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24FC32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

6.5 Noise Protection

The SCL and SDA inputs incorporate Schmitt triggers which suppress noise spikes to ensure proper device operation even on a noisy bus.

FIGURE 6-2: RANDOM READ

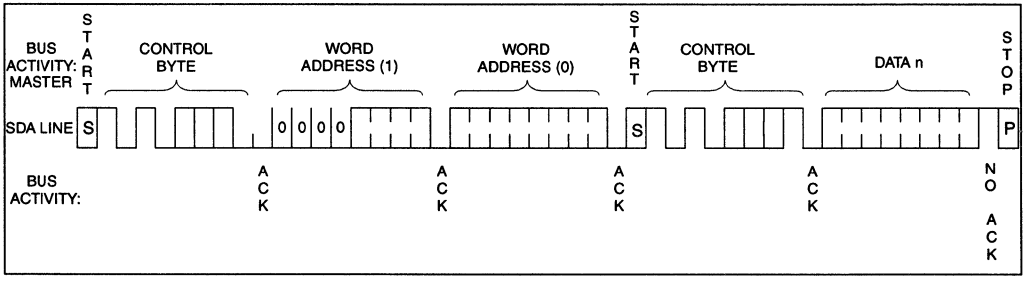
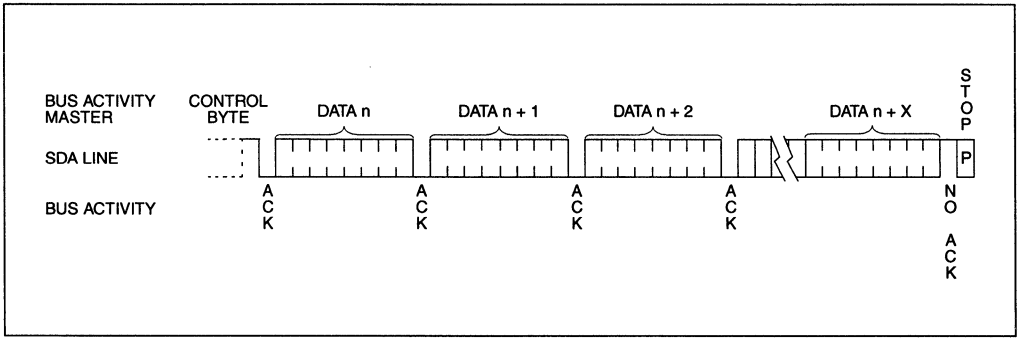


FIGURE 6-3: SEQUENTIAL READ



7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will' wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 7-1) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 7-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

FIGURE 7-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

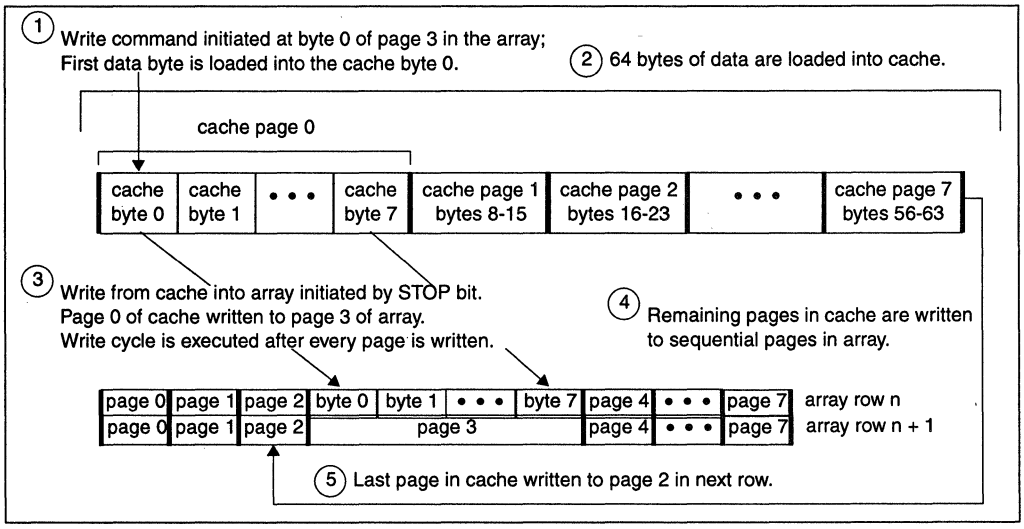
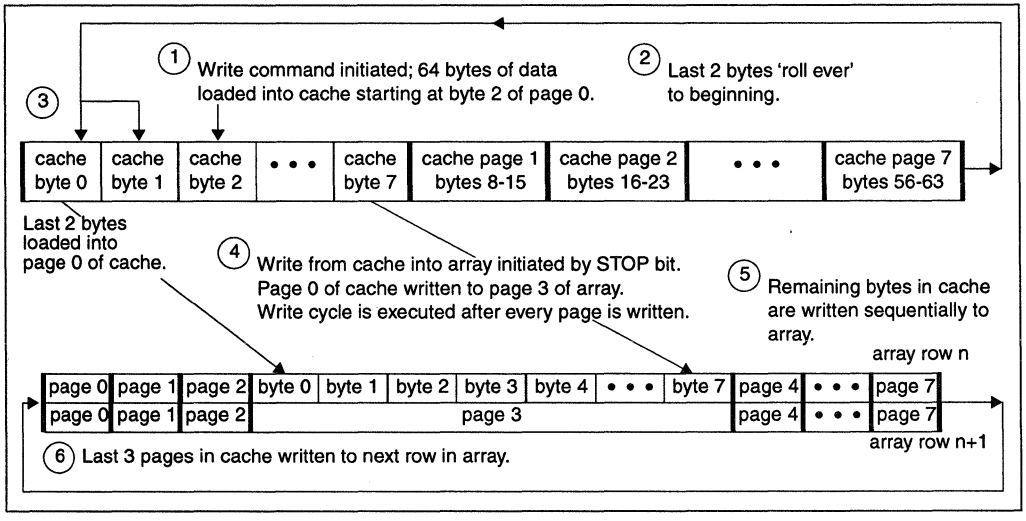


FIGURE 7-2: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24FC32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-3).

8.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 2 KΩ, must consider total bus capacitance and maximum rise/fall times).

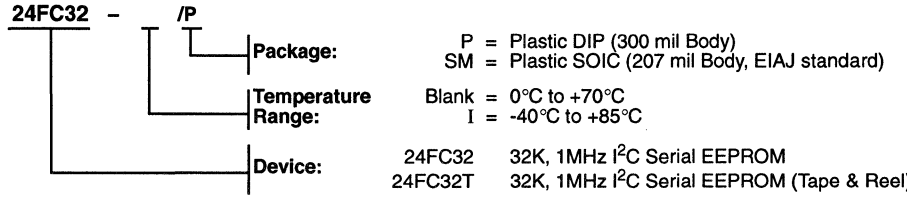
For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

24FC32 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24AA64/24LC64

64K I²C™ CMOS Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA64	1.8-5.5V	400 kHz†	I
24LC64	2.5-5.5V	400 kHz‡	I, E

†100 kHz for Vcc < 2.5V.
‡100 kHz for E temperature range.

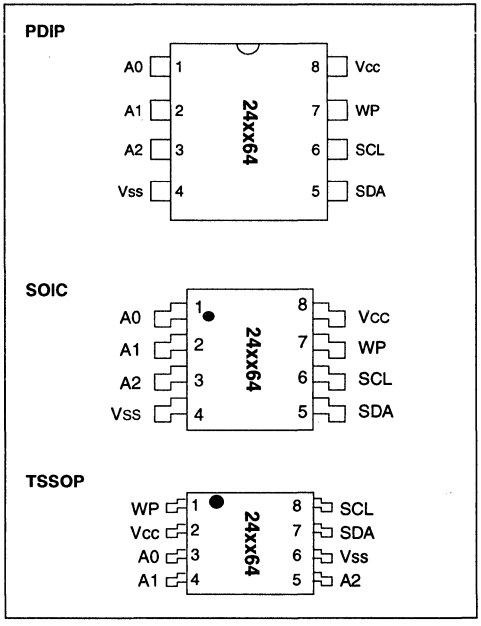
FEATURES

- Low power CMOS technology
  - Maximum write current 3 mA at 5.5V
  - Maximum read current 400 µA at 5.5V
  - Standby current 100 nA typical at 5.5V
- 2-wire serial interface bus, I²C compatible
- Cascadable for up to eight devices
- Self-timed ERASE/WRITE cycle
- 32-byte page or byte write modes available
- 5 ms max write cycle time
- Hardware write protect for entire array
- Output slope control to eliminate ground bounce
- Schmitt trigger inputs for noise suppression
- 1,000,000 erase/write cycles guaranteed
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP, SOIC (150 and 208 mil) and TSSOP packages; 14-pin SOIC package
- Temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

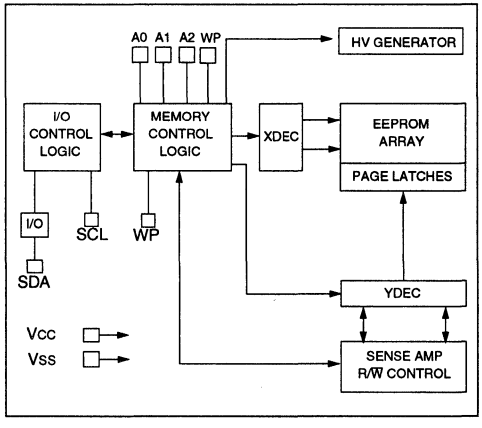
DESCRIPTION

The Microchip Technology Inc. 24AA64/24LC64 (24xx64*) is a 8K x 8 (64K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 5.5V). It has been developed for advanced, low power applications such as personal communications or data acquisition. This device also has a page-write capability of up to 32 bytes of data. This device is capable of both random and sequential reads up to the 64K boundary. Functional address lines allow up to eight devices on the same bus, for up to 512 Kbits address space. This device is available in the standard 8-pin plastic DIP, 8-pin SOIC (150 and 208 mil), and 8-pin TSSOP.

PACKAGE TYPE



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

*24xx64 is used in this document as a generic part number for the 24AA64/24LC64 devices.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect Input
Vcc	+1.8 to 5.5V (24AA64) +2.5 to 5.5V (24LC64)

TABLE 1-2 DC CHARACTERISTICS

All parameters apply across the recommended operating ranges unless otherwise noted.	Industrial (I): Vcc = +1.8V to 5.5V Tamb = -40°C to +85°C Automotive (E): Vcc = 4.5V to 5.5V Tamb = -40°C to 125°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL, SDA, and WP pins:					
High level input voltage	VIH	0.7 Vcc	—	V	
Low level input voltage	VIL	—	0.3 Vcc	V	Vcc ≥ 2.5V
			0.2 Vcc	V	Vcc < 2.5V
Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	VHYS	0.05 Vcc	—	V	Vcc > 2.5V (Note)
Low level output voltage	VOL	—	0.40	V	IOL = 3.0 mA @ Vcc = 4.5V IOL = 2.1 mA @ Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = Vss to Vcc, WP = Vss VIN = Vss or Vcc, WP = Vcc
Output leakage current	ILO	-10	10	µA	VOUT = Vss to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note) Tamb = 25°C, f_c = 1 MHz
Operating current	ICC Write	—	3	mA	Vcc = 5.5V
	ICC Read	—	400	µA	Vcc = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	1	µA	SCL = SDA = Vcc = 5.5V A0, A1, A2, WP = Vss

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING DATA

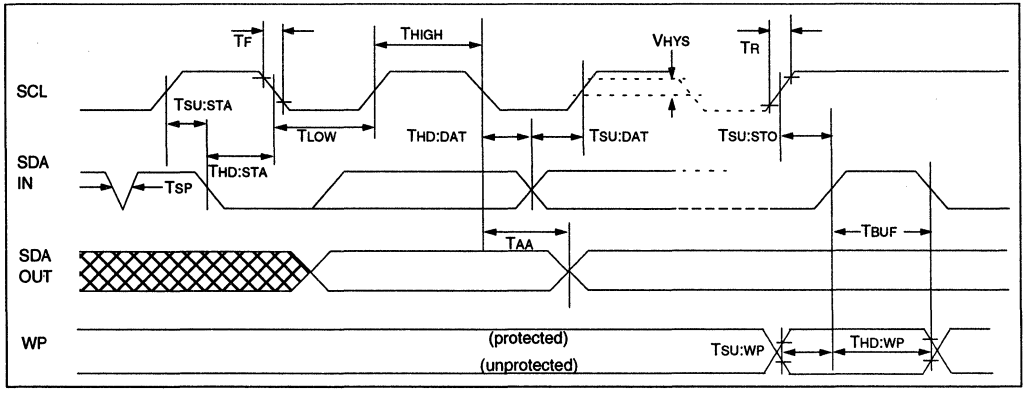


TABLE 1-3 AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Industrial (I): VCC = +1.8V to 5.5V Tamb = -40°C to +85°C Automotive (E): VCC = +4.5V to 5.5V Tamb = -40°C to 125°C				
Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
START condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
STOP condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
WP setup time	TSU:WP	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
WP hold time	THD:WP	4700 4000 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Output fall time from VIH minimum to VIL maximum	TOF	10	250	ns	C_B ≤ 100 pF (Note 1)
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1 and 3)
Write cycle time (byte or page)	TWC	—	5	ms	
Endurance		1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 PIN DESCRIPTIONS

2.1 A0, A1, A2 Chip Address Inputs

The A0,A1,A2 inputs are used by the 24xx64 for multiple device operation. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either Vcc or Vss.

2.2 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pullup resistor to Vcc (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.4 WP

This pin can be connected to either Vss, Vcc or left floating. An internal pull-down resistor on this pin will keep the device in the unprotected state if left floating. If tied to Vss or left floating, normal memory operation is enabled (read/write the entire memory 0000-1FFF).

If tied to Vcc, WRITE operations are inhibited. Read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24xx64 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions while the 24xx64 works as a slave. Both master and slave can operate as a transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must end with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24xx64 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24xx64) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

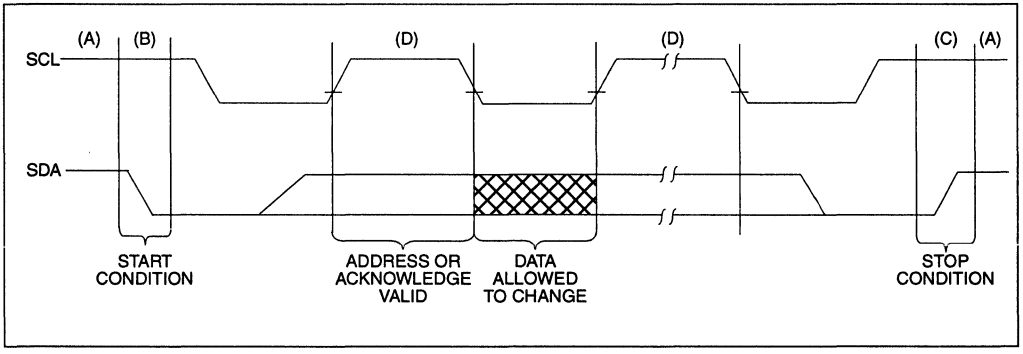
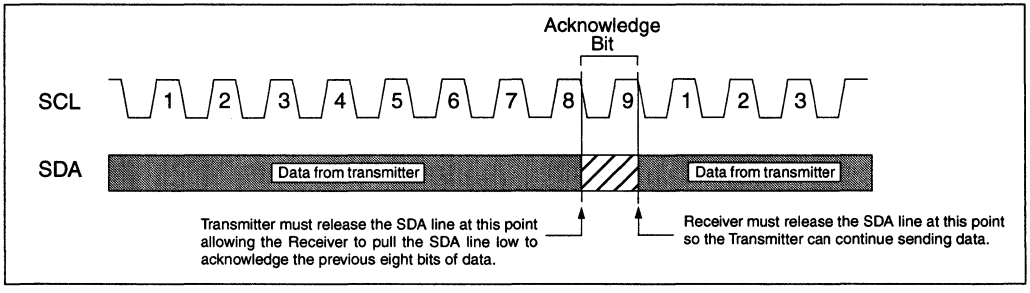


FIGURE 4-2: ACKNOWLEDGE TIMING



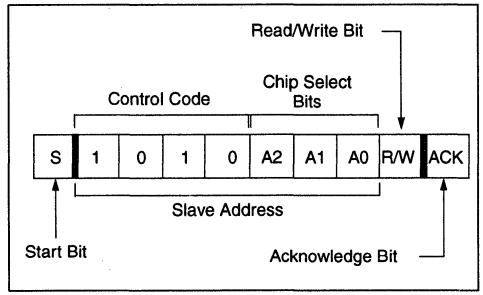
5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a four bit control code; for the 24xx64 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24xx64 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A12...A0 are used, the upper three address bits are don't care bits. The upper address bits are transferred first, followed by the less significant bits.

Following the start condition, the 24xx64 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24xx64 will select a read or write operation.

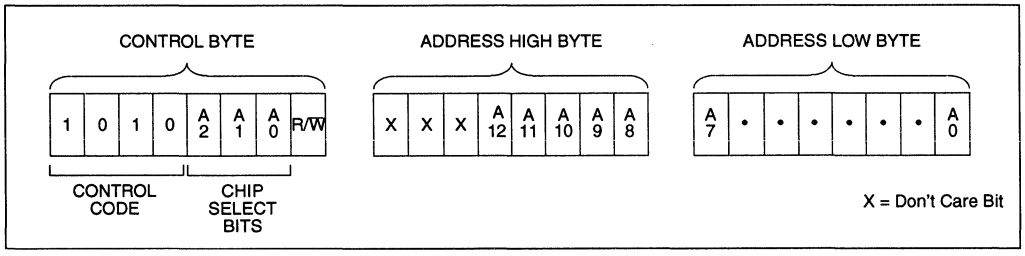
FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24xx64's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15. It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start condition from the master, the control code (four bits), the chip select (three bits), and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24xx64. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24xx64 the master device will transmit the data word to be written into the addressed memory location. The 24xx64 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24xx64 will not generate acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24xx64 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 31 additional bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written and the device will immediately accept a new command.

6.3 Write Protection

The WP pin allows the user to write protect the entire array (0000-1FFF) when the pin is tied to Vcc. If tied to Vss or left floating, the write protection is disabled. The WP pin is sampled at the STOP bit for every write command (Figure 1-1) Toggling the WP pin after the STOP bit will have no effect on the execution of the write cycle.

FIGURE 6-1: BYTE WRITE

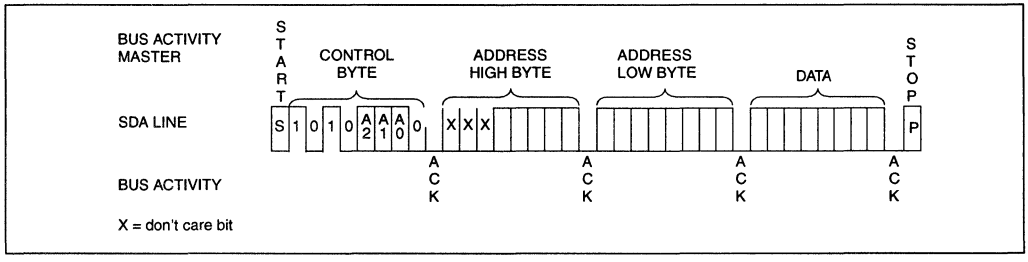
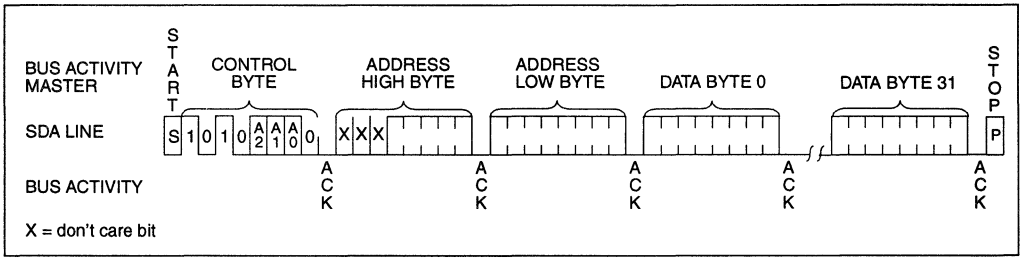


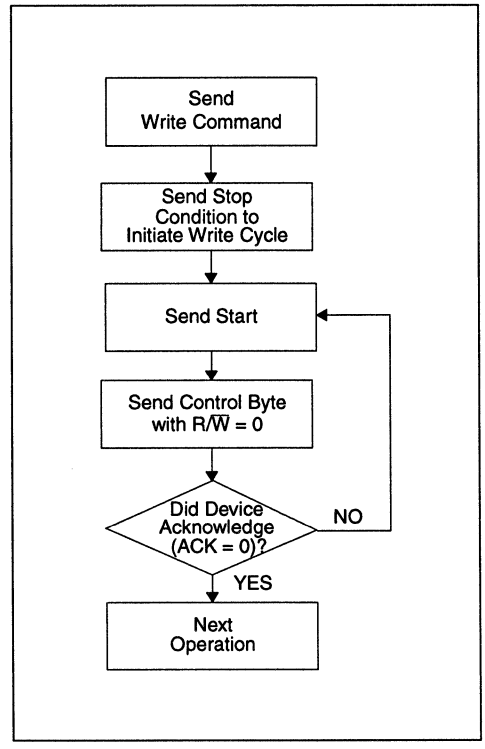
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

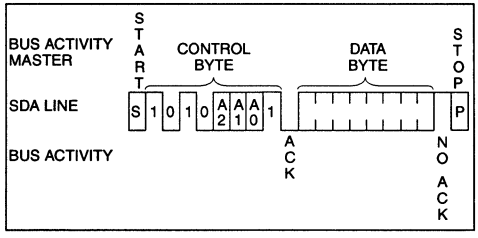
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24xx64 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the 24xx64 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24xx64 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24xx64 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24xx64 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24xx64 to discontinue transmission (Figure 8-2). After a random read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24xx64 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24xx64 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition. To provide sequential reads the 24xx64 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 1FFF to address 0000 if the master acknowledges the byte received from the array address 1FFF.

FIGURE 8-2: RANDOM READ

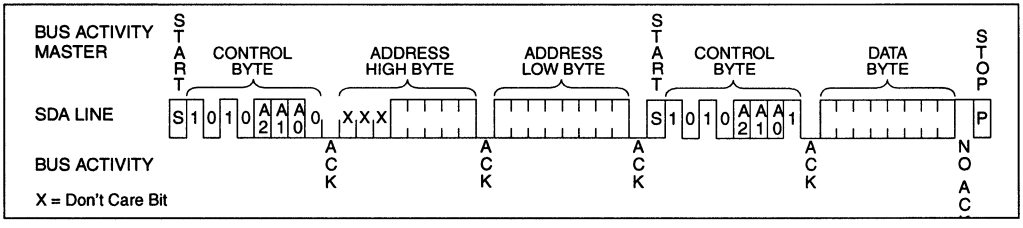
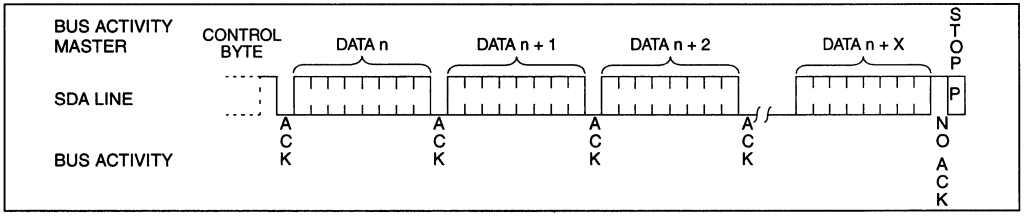


FIGURE 8-3: SEQUENTIAL READ

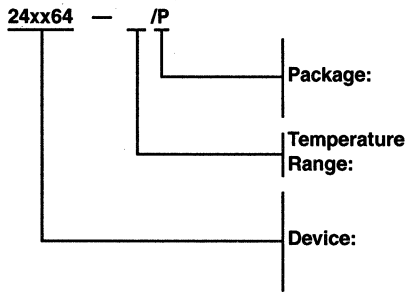


3

I²C™

24xx64 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	P = Plastic DIP (300 mil Body), 8-lead SN = Plastic SOIC (150 mil Body, EIAJ standard), 8-lead SM = Plastic SOIC (208 mil Body, EIAJ standard), 8-lead ST = TSSOP, 8-lead
Temperature Range:	I = -40°C to +85°C E = -40°C to -125°C
Device:	24AA64 64K bit 1.8V I^2C Serial EEPROM 24AA64T 64K bit 1.8V I^2C Serial EEPROM (Tape and Reel) 24LC64 64K bit 2.5V I^2C Serial EEPROM 24LC64T 64K bit 2.5V I^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24AA65

64K 1.8V I²C™ Smart Serial™ EEPROM

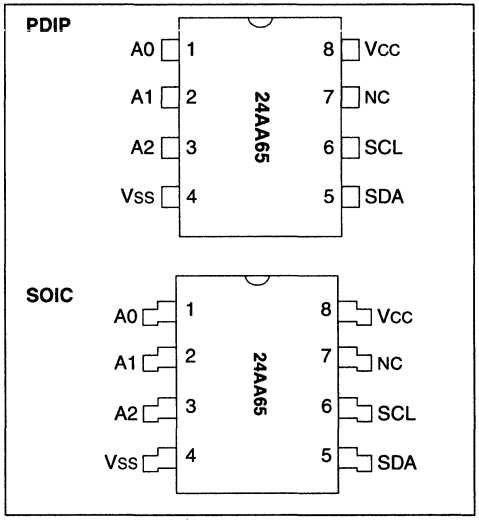
FEATURES

- Voltage operating range: 1.8V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two wire bus protocol I²C™ compatible
- 8 byte page, or byte modes available
- 2 ms typical write cycle time, byte or page
- 64-byte line input cache for fast write loads
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory
- 100 kHz (1.8V) and 400 kHz (5.0V) compatibility
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 E/W cycles guaranteed for a High Endurance Block
  - 1,000,000 E/W cycles guaranteed for a Standard Endurance Block
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C

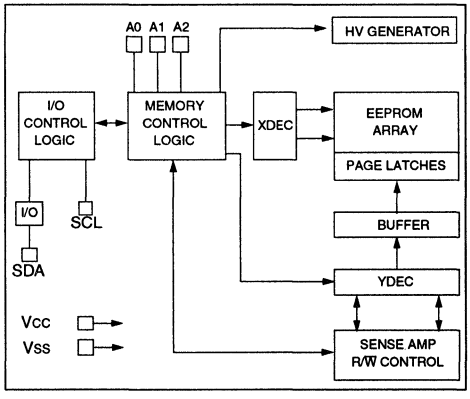
DESCRIPTION

The Microchip Technology Inc. 24AA65 is a "smart" 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. It is capable of operation down to 1.8V, the end-of-life voltage for 2 "AA" battery cells for most popular battery technologies.The 24AA65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 1,000,000 ERASE/WRITE (E/W) cycles guaranteed. The 24AA65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24LC65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24AA65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to+150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice**: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+1.8V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

					VCC = +1.8V to +6.0V Commercial(C): Tamb = 0°C to +70°C
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating Current	ICC Write	—	3	mA	VCC = 6.0V, SCL = 400 kHz
	ICC Read	—	150	µA	VCC = 6.0V, SCL = 400 kHz
Standby current		—	5	µA	VCC = 5.0V, SCL = SDA = VCC
			2	µA	VCC = 1.8V, SCL = SDA = VCC A0, A1, A2 = VSS (Note)

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

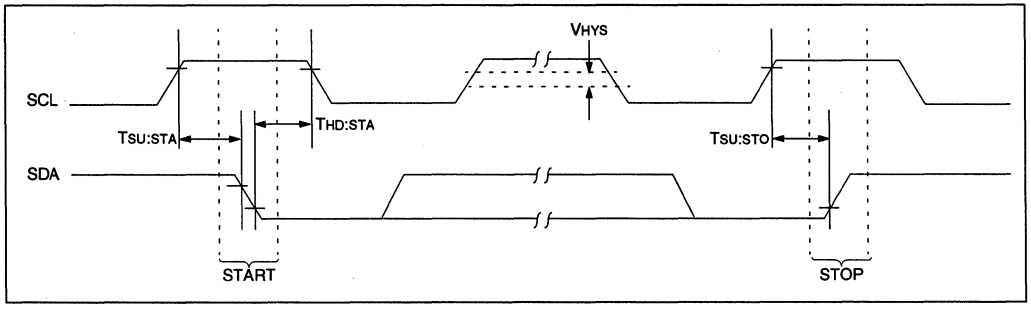


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 1.8V - 6.0V STD. MODE		Vcc = 4.5V - 6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time fro VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3
Write cycle time	TWR	—	5	—	5	ms/ page	(Note 4)
Endurance High Endurance Block Rest of Array		 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 5)

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

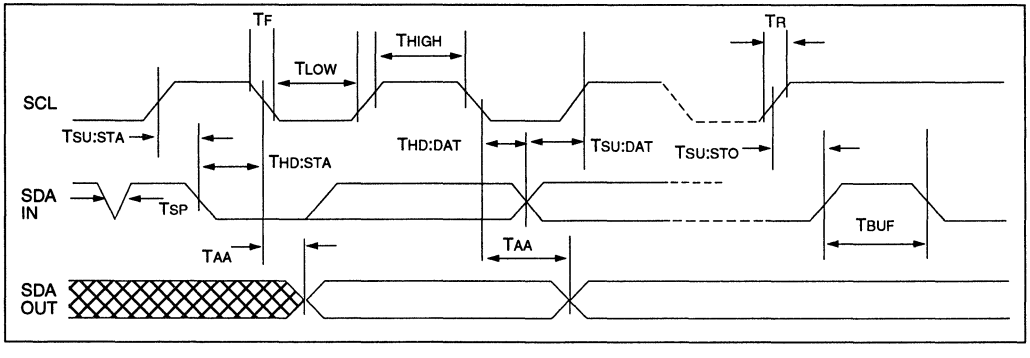
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

5: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24AA65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

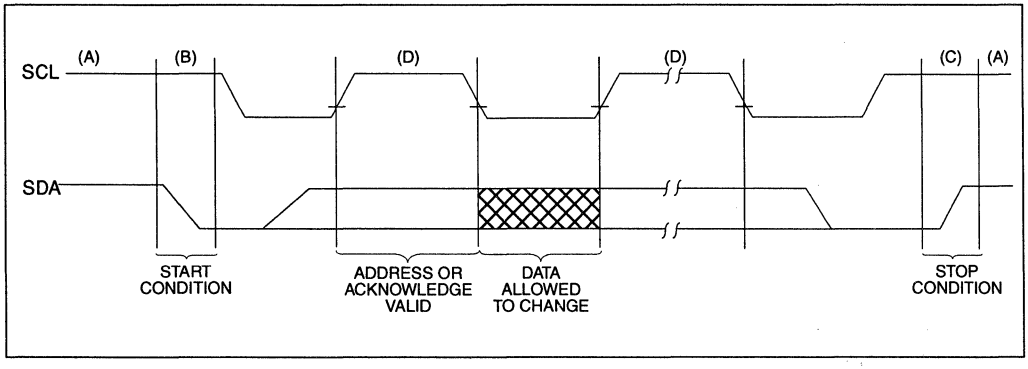
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

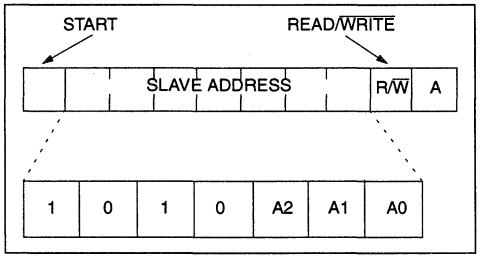


3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 4-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24AA65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24AA65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24AA65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24AA65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24AA65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24AA65 the master device will transmit the data word to be written into the addressed memory location. The 24AA65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA65 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24AA65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE

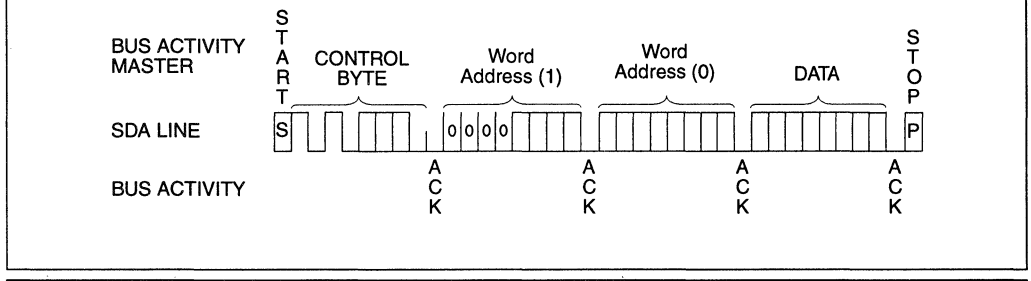


FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 8-2)

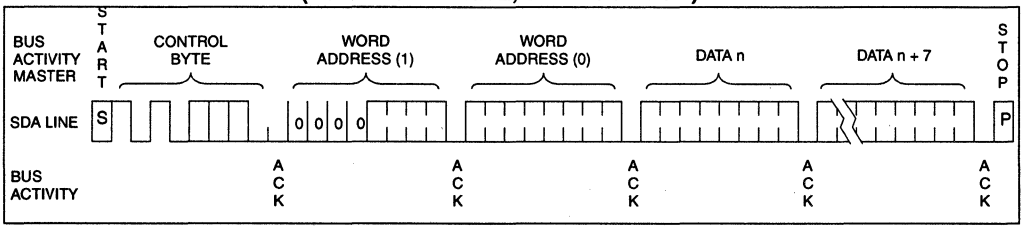


FIGURE 4-3: CURRENT ADDRESS READ

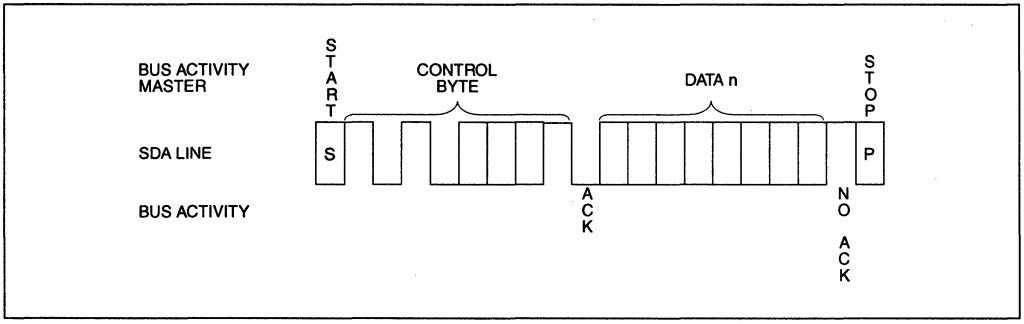


FIGURE 4-4: RANDOM READ

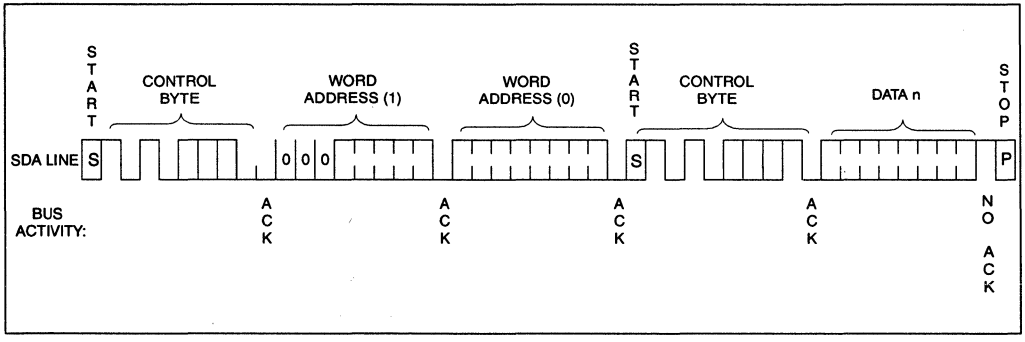
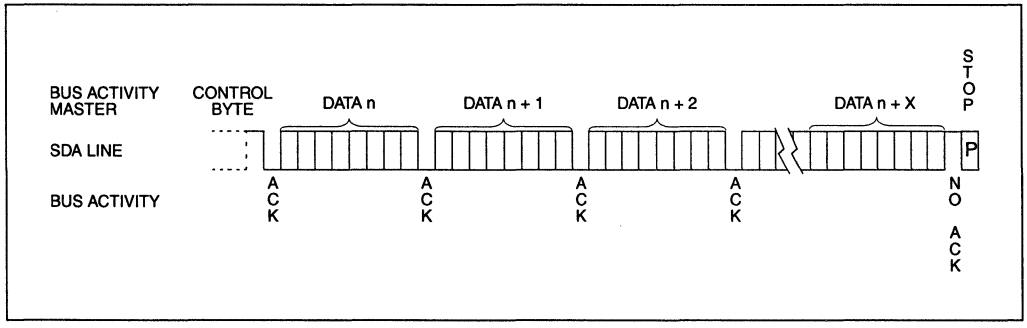


FIGURE 4-5: SEQUENTIAL READ



5.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

5.1 Current Address Read

The 24AA65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA65 discontinues transmission (Figure 4-3).

5.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24AA65 to discontinue transmission (Figure 4-4).

5.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24AA65 to transmit the next sequentially addressed 8 bit word (Figure 4-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24AA65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

5.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24LC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

5.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

5.6 High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance. This block will be capable of 10,000,000 ERASE/WRITE cycles (Figure 8-1).

Note:	The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

5.7 Security Options

The 24AA65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (Figure 8-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/HE) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

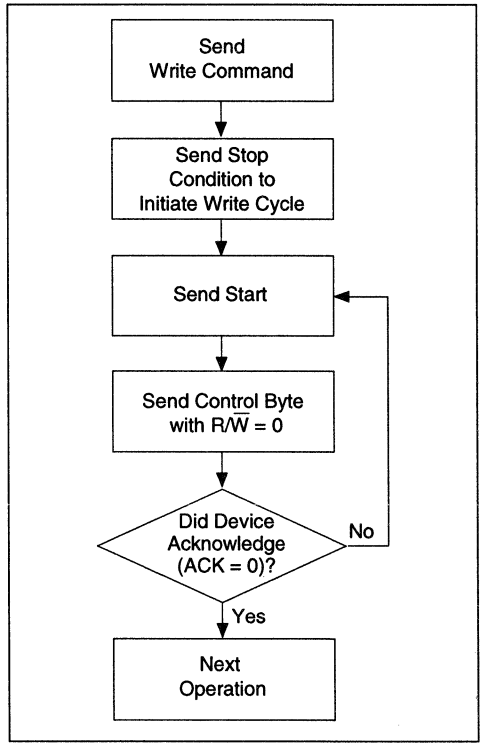
5.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as'1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (Figure 8-1).

6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 8-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-3, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24AA65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-2 and Figure 8-1).

8.2 SDA Serial Address/Data Input/ Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1: CONTROL SEQUENCE BIT ASSIGNMENTS

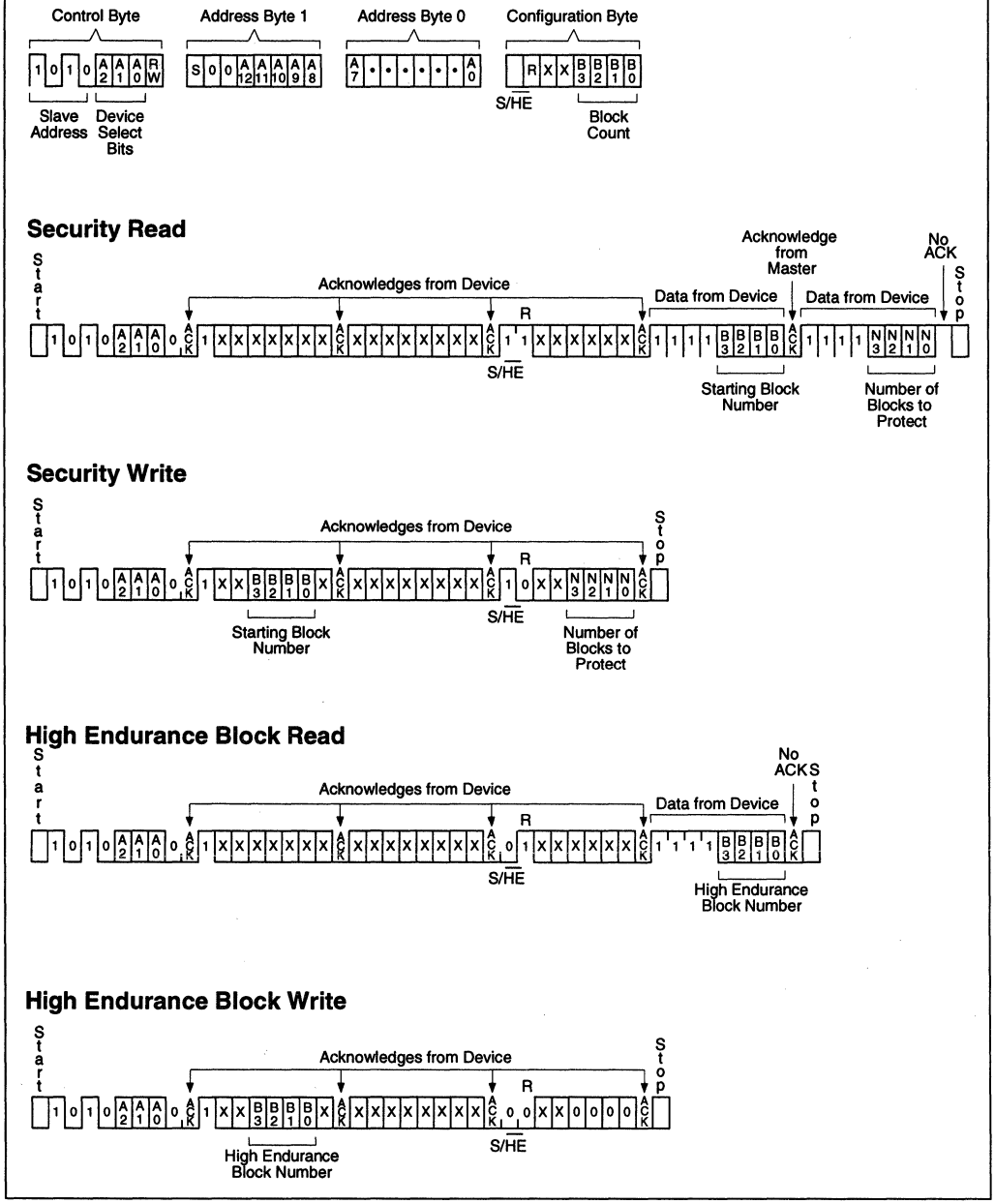


FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

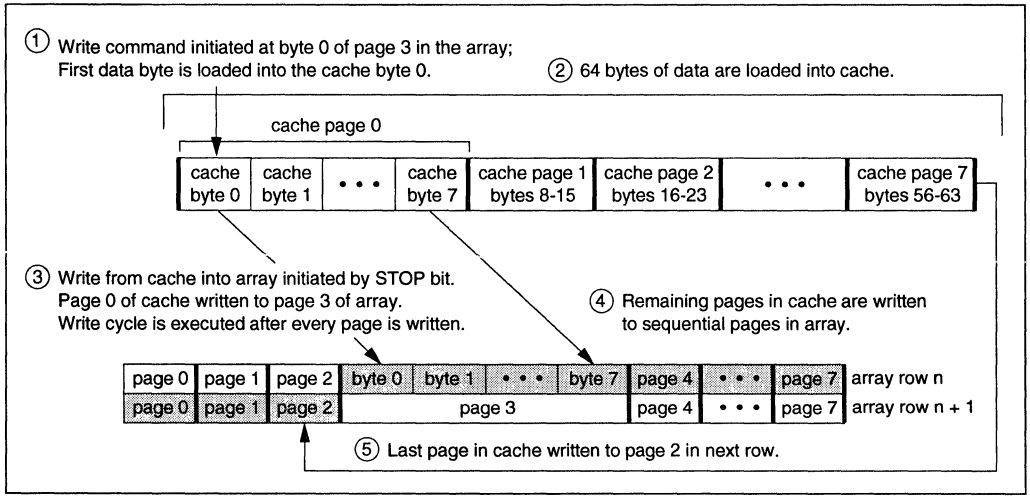
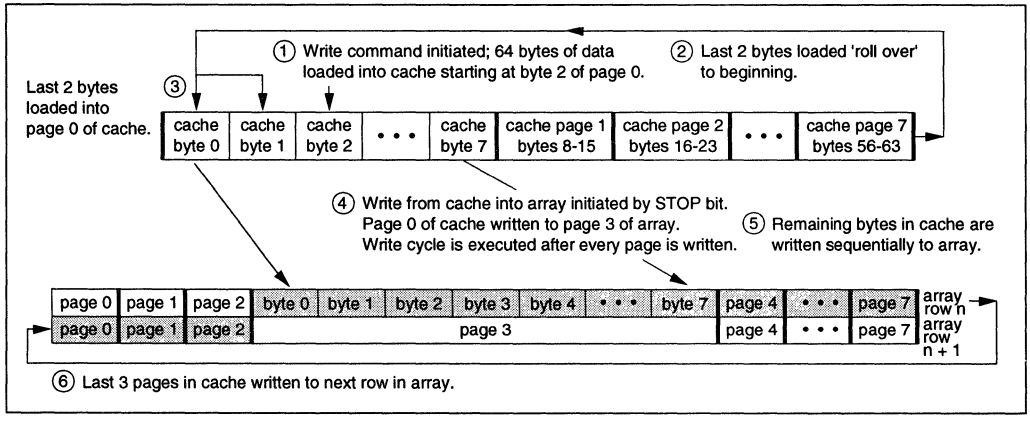


FIGURE 8-3: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY

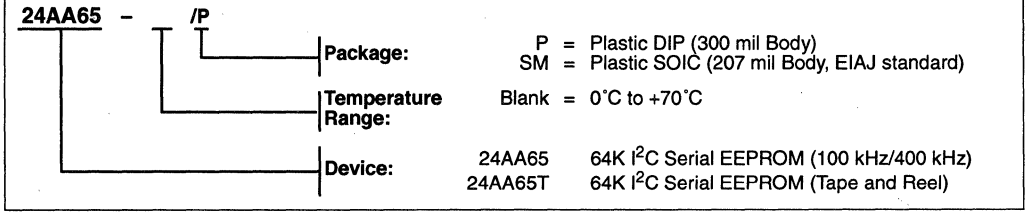


3

I²C™

24AA65 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

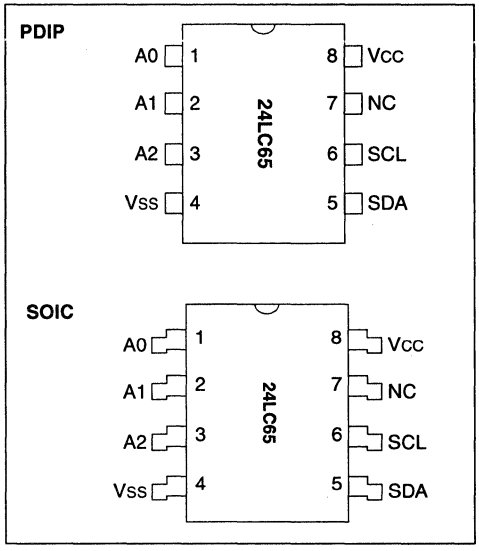
24LC65

64K 2.5V I²C™ Smart Serial™ EEPROM

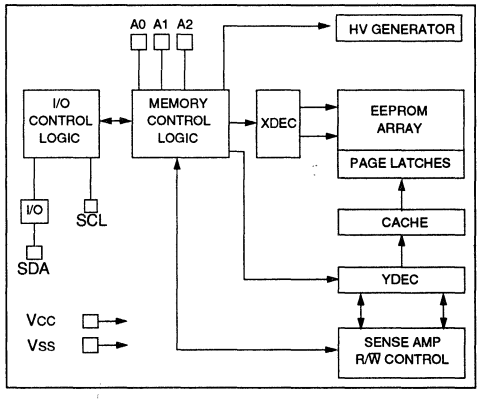
FEATURES

- Voltage operating range: 2.5V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two wire bus protocol I²C™ compatible
- 8 byte page, or byte modes available
- 2 ms typical write cycle time, byte or page
- 64-byte input cache for fast write loads
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory
- Including 100 kHz (2.5V) and 400 kHz (5.0V) compatibility
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 E/W cycles guaranteed for a High Endurance Block
  - 1,000,000 E/W cycles guaranteed for a Standard Endurance Block
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

PACKAGE TYPES



BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 24LC65 is a "smart" 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24LC65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 1,000,000 ERASE/WRITE (E/W) cycles guaranteed. The 24LC65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24LC65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24LC65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to+150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data/I/O
SCL	Serial Clock
VCC	+2.5V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +2.5V to +6.0V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Sym**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	(Note 1)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE	—	3	mA	VCC = 6.0V, SCL = 400 kHz
	ICC Read	—	150	µA	VCC = 6.0V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.0V, SCL = SDA = VCC A0, A1, A2 = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

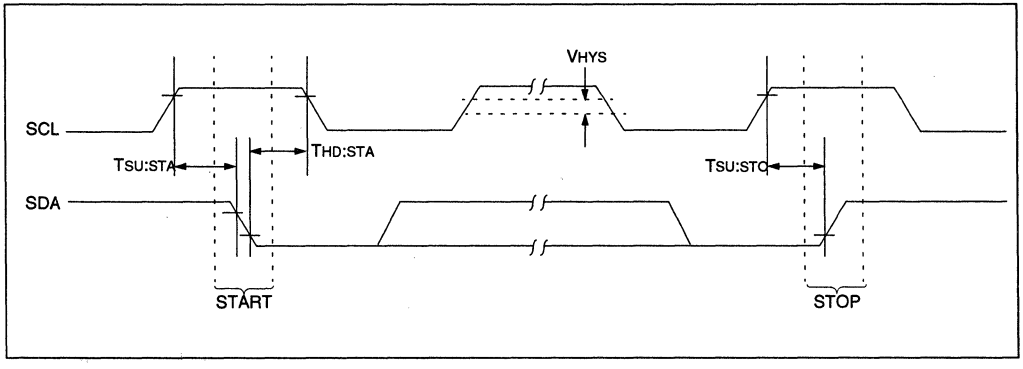
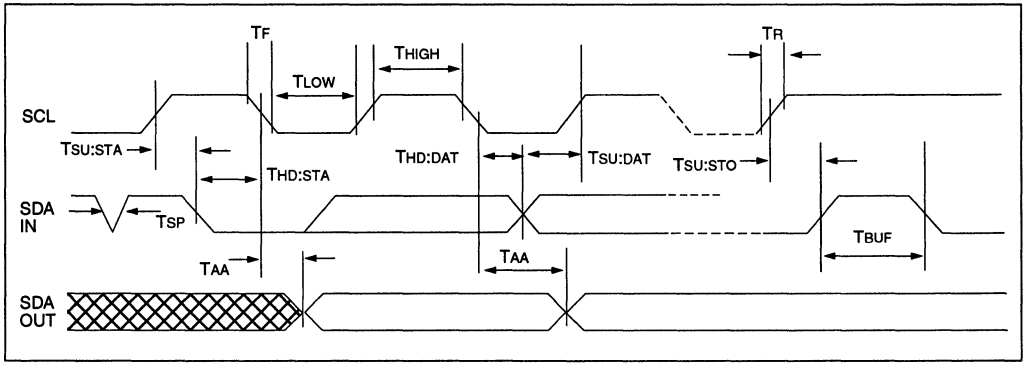


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 2.5V-6.0V STD. MODE		Vcc = 4.5-6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition setup time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	(Note 4)
Endurance High Endurance Block Rest of Array		 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 5)

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.
4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.
5: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24LC65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

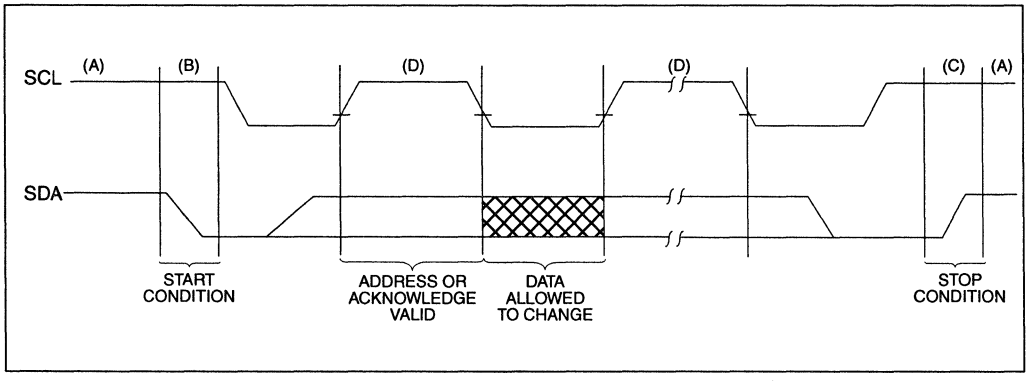
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

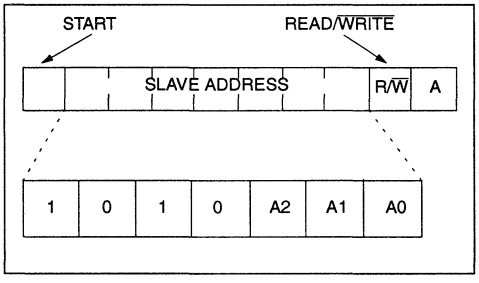


3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 4-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24LC65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24LC65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24LC65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24LC65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC65 the master device will transmit the data word to be written into the addressed memory location. The 24LC65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC65 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24LC65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE

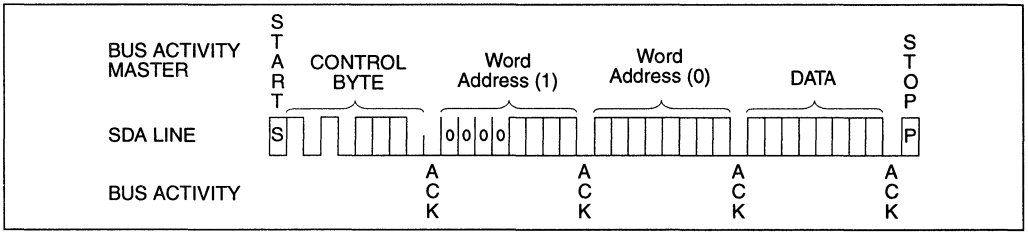


FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 8-2)

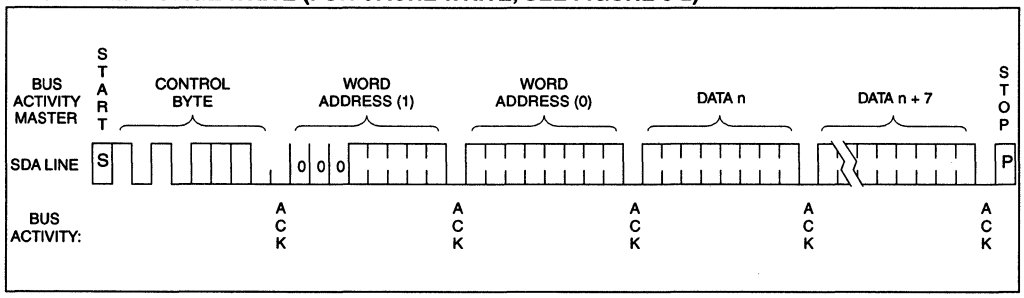


FIGURE 4-3: CURRENT ADDRESS READ

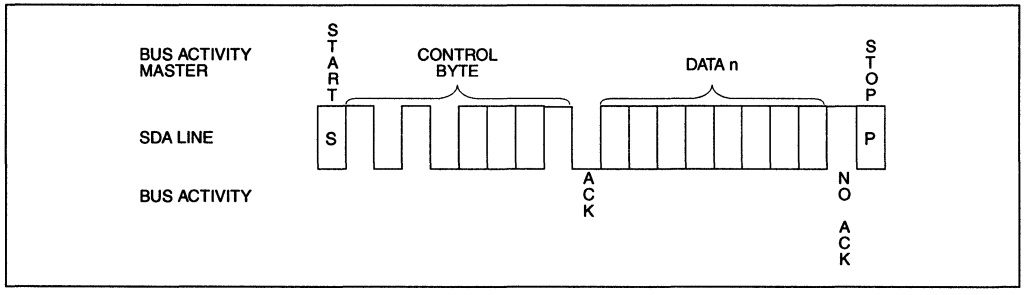


FIGURE 4-4: RANDOM READ

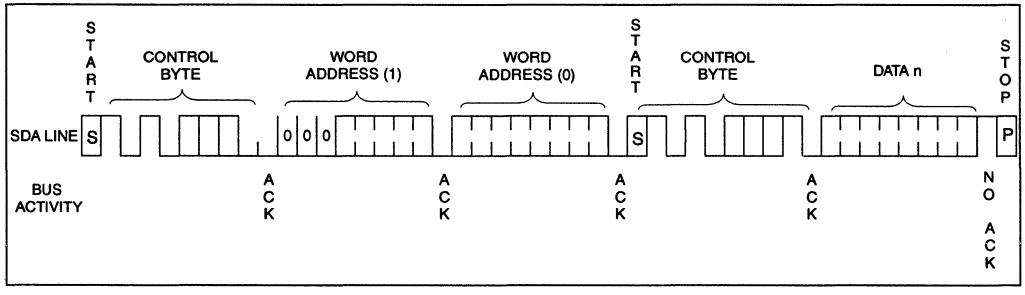
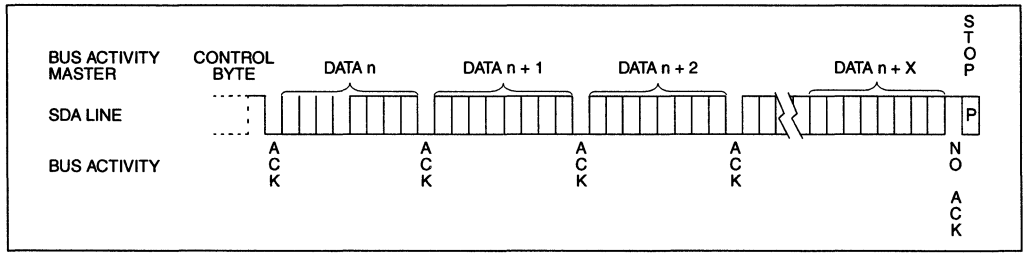


FIGURE 4-5: SEQUENTIAL READ



5.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

5.1 Current Address Read

The 24LC65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC65 discontinues transmission (Figure 4-3).

5.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC65 to discontinue transmission (Figure 4-4).

5.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC65 to transmit the next sequentially addressed 8 bit word (Figure 4-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

5.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24LC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

5.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

5.6 High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance. This block will be capable of 10,000,000 ERASE/WRITE cycles typical (Figure 8-1).

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

5.7 Security Options

The 24LC65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (Figure 8-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/HE) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

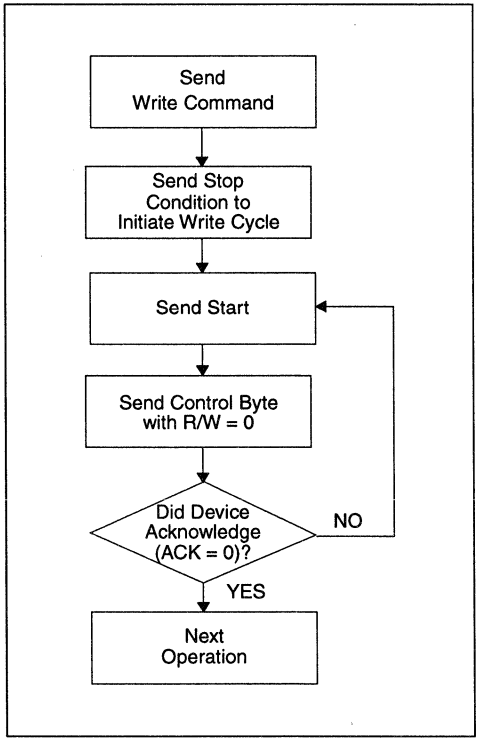
5.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (Figure 8-1).

6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 8-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-3, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-2 and Figure 8-1).

8.2 SDA Serial Address/Data Input/Output

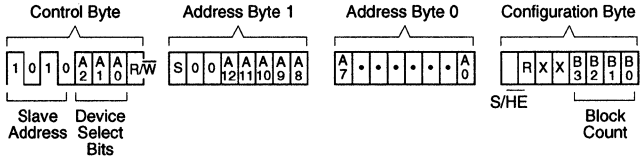
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

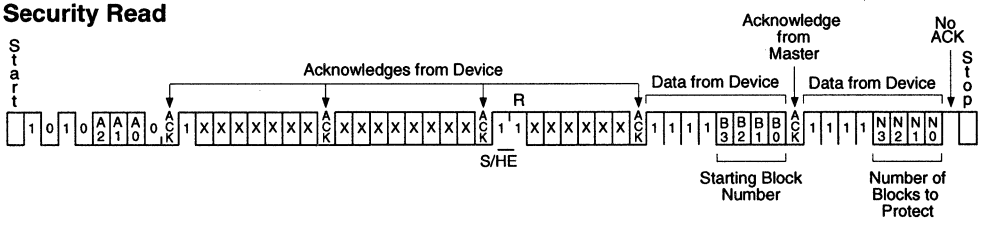
8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

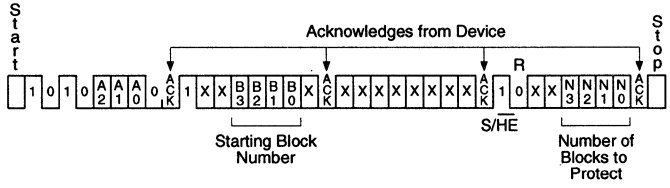
FIGURE 8-1: CONTROL SEQUENCE BIT ASSIGNMENTS



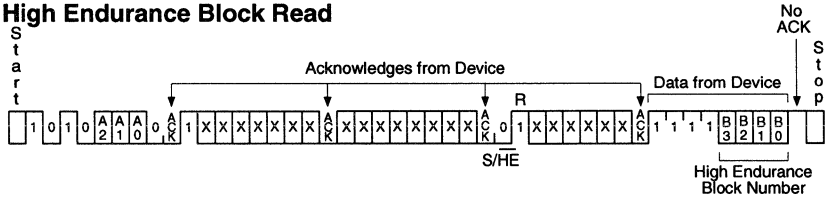
Security Read



Security Write



High Endurance Block Read



High Endurance Block Write

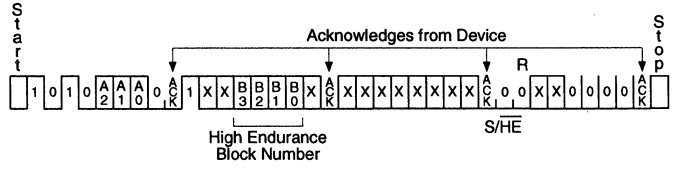


FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

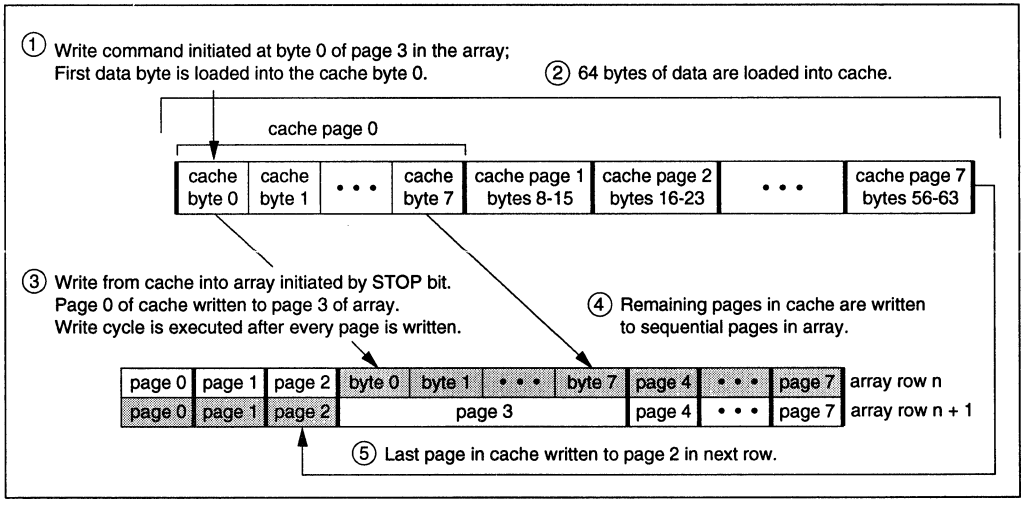
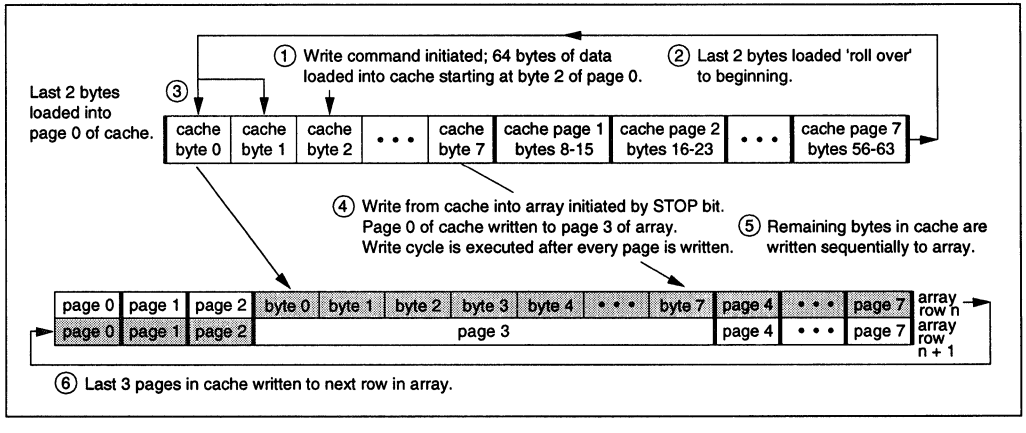
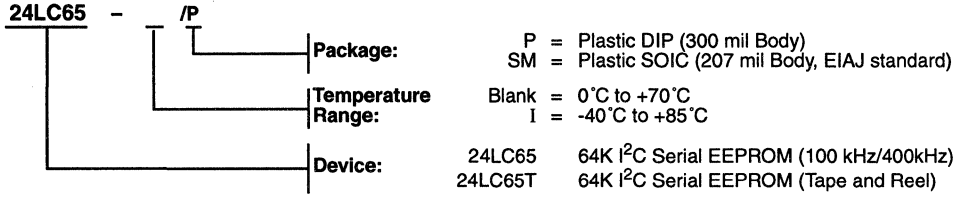


FIGURE 8-3: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



24LC65 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24C65

64K 5.0V I²C™ Smart Serial™ EEPROM

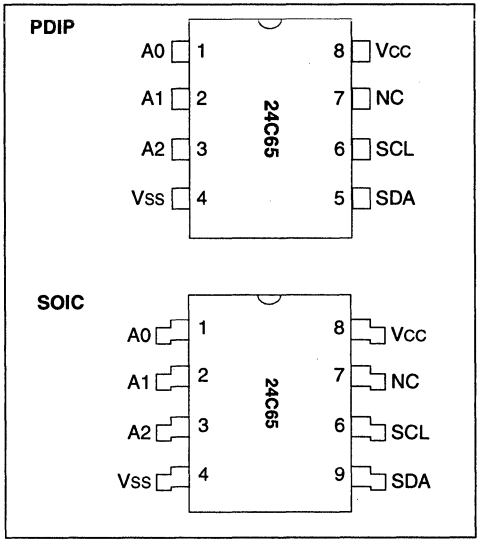
FEATURES

- Voltage operating range: 4.5V to 5.5V
  - Peak write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 1 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
- 8 byte page, or byte modes available
- 2 ms typical write cycle time, byte or page
- 64-byte input cache for fast write loads
- Up to eight devices may be connected to the same bus for up to 512K bits total memory
- Including 400 KHz compatibility
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 E/W cycles guaranteed for High Endurance Block
  - 100,000 E/W cycles guaranteed for a Standard Endurance Block
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I) -40°C to +85°C
  - Automotive (E): -40°C to +125°C

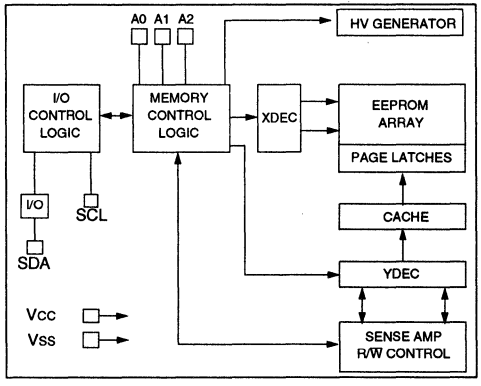
DESCRIPTION

The Microchip Technology Inc. 24C65 is a "smart" 8K x 8 Serial Electrically Erasable PROM (EEPROM). This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24C65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 1,000,000 ERASE/WRITE (E/W) cycles guaranteed. The 24C65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24C65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power nonvolatile code and data applications. The 24C65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40° to +85°C Automotive (E): Tamb = -40°C to +125°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Read	—	150	µA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.5V, SCL = SDA =VCC A0, A1, A2 = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

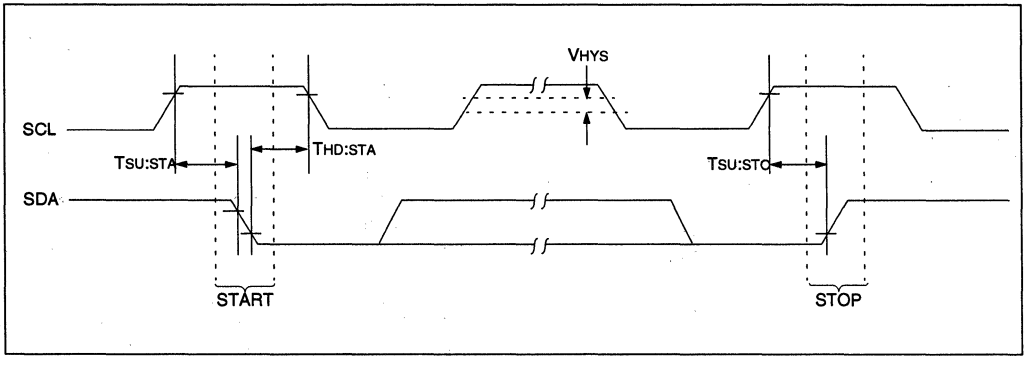


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STD. MODE		FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms/page	(Note 4)
Endurance High Endurance Block Rest of Array		 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 5)

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.

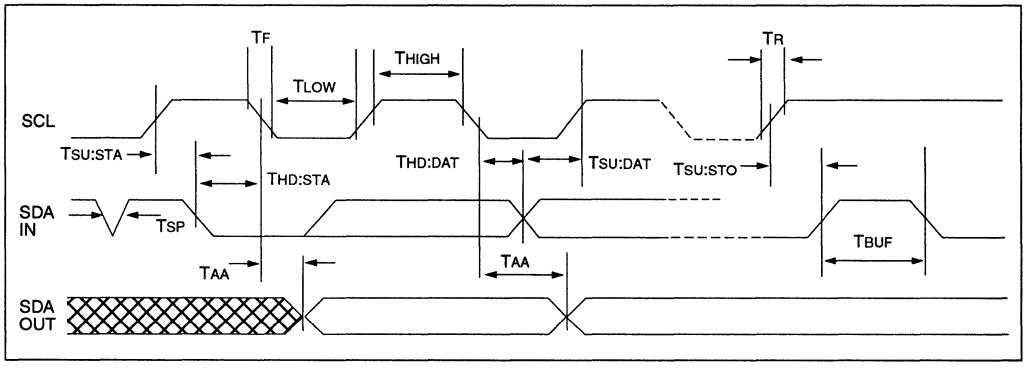
2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

5: This parameter is not tested but guaranteed by characterization. For endurance estimates on a specific application, please consult the Total Endurance Mode which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24C65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

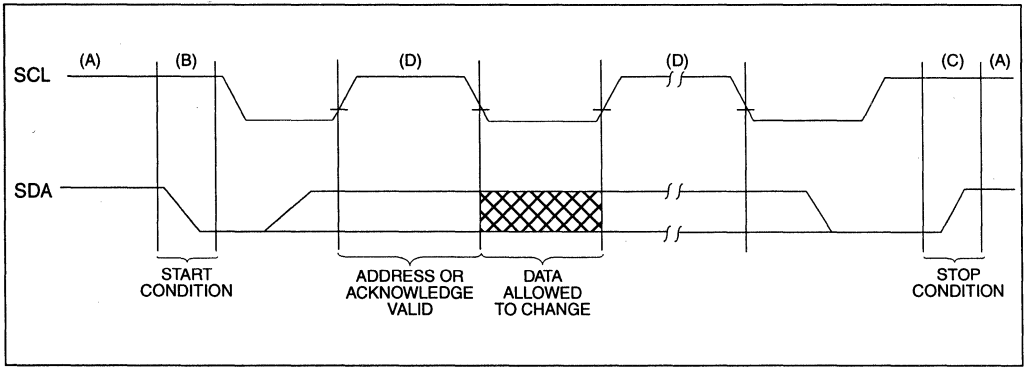
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24C65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

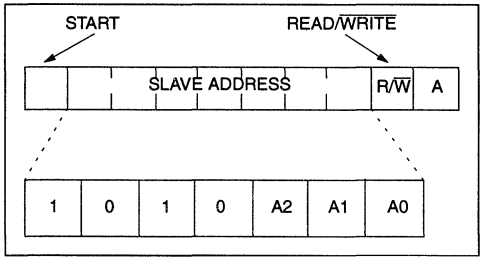


3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24C65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 4-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24C65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24C65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24C65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

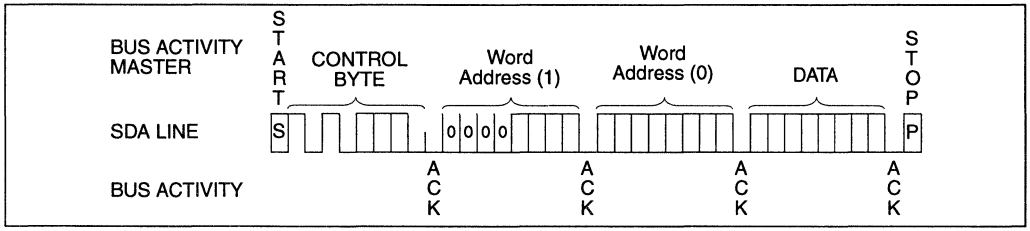
4.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24C65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24C65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24C65 the master device will transmit the data word to be written into the addressed memory location. The 24C65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C65 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24C65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE



3

I²C™

FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 8-2)

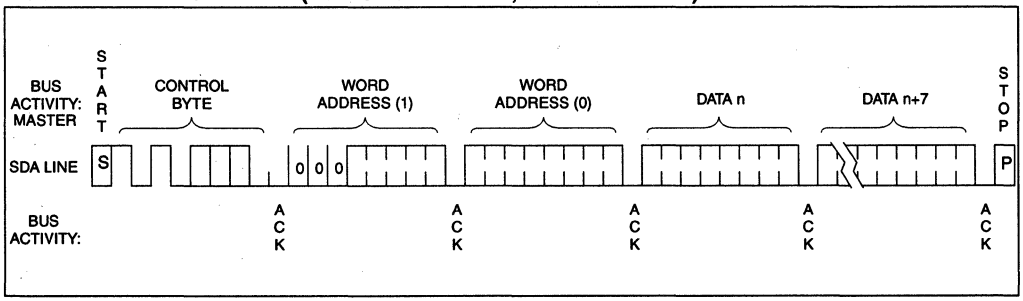


FIGURE 4-3: CURRENT ADDRESS READ

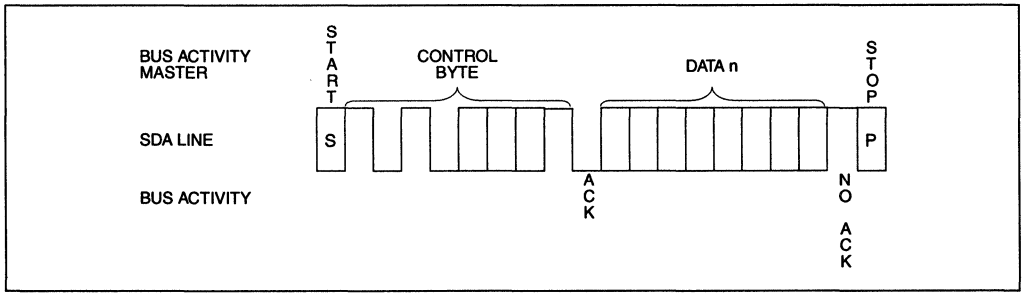


FIGURE 4-4: RANDOM READ

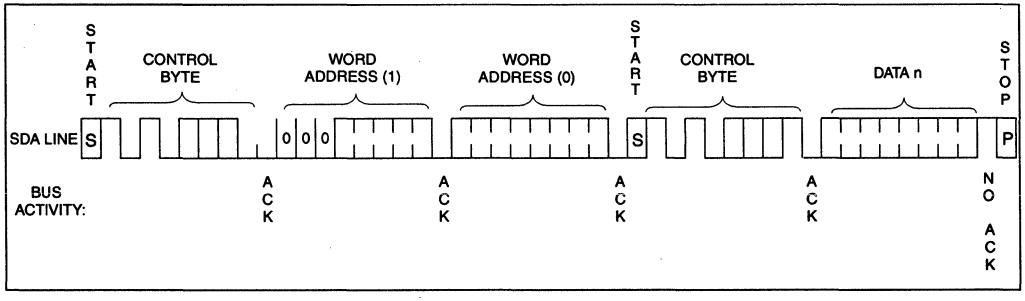
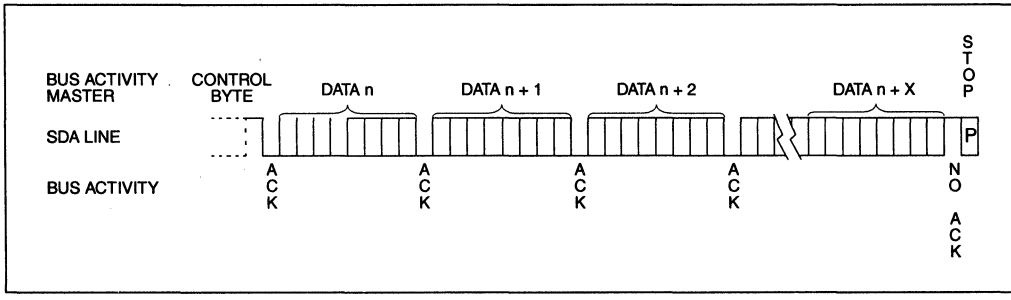


FIGURE 4-5: SEQUENTIAL READ



5.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

5.1 Current Address Read

The 24C65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C65 discontinues transmission (Figure 4-3).

5.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24C65 to discontinue transmission (Figure 4-4).

5.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24C65 to transmit the next sequentially addressed 8 bit word (Figure 4-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24C65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

5.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24C65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

5.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

5.6 High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance (Figure 8-1). This block will be capable of 10,000,000 erase/write cycles.

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

5.7 Security Options

The 24C65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (Figure 8-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/$\overline{HE}$) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write pro-

tected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

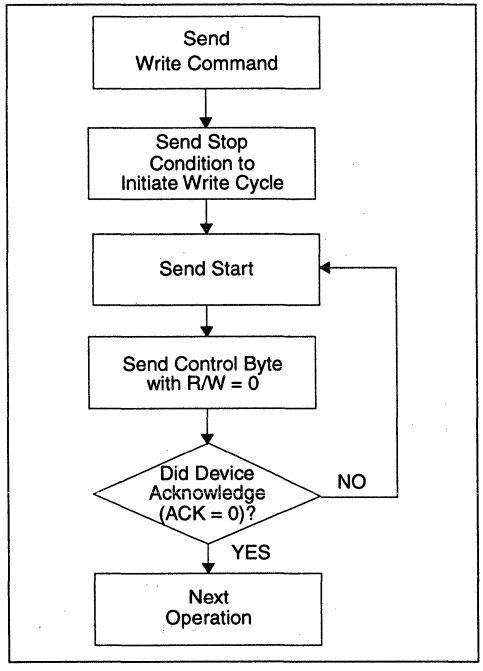
5.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (Figure 8-1).

6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 8-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-3, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24C65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-2 and Figure 8-1).

8.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 KHz, 2 KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1: CONTROL SEQUENCE BIT ASSIGNMENTS

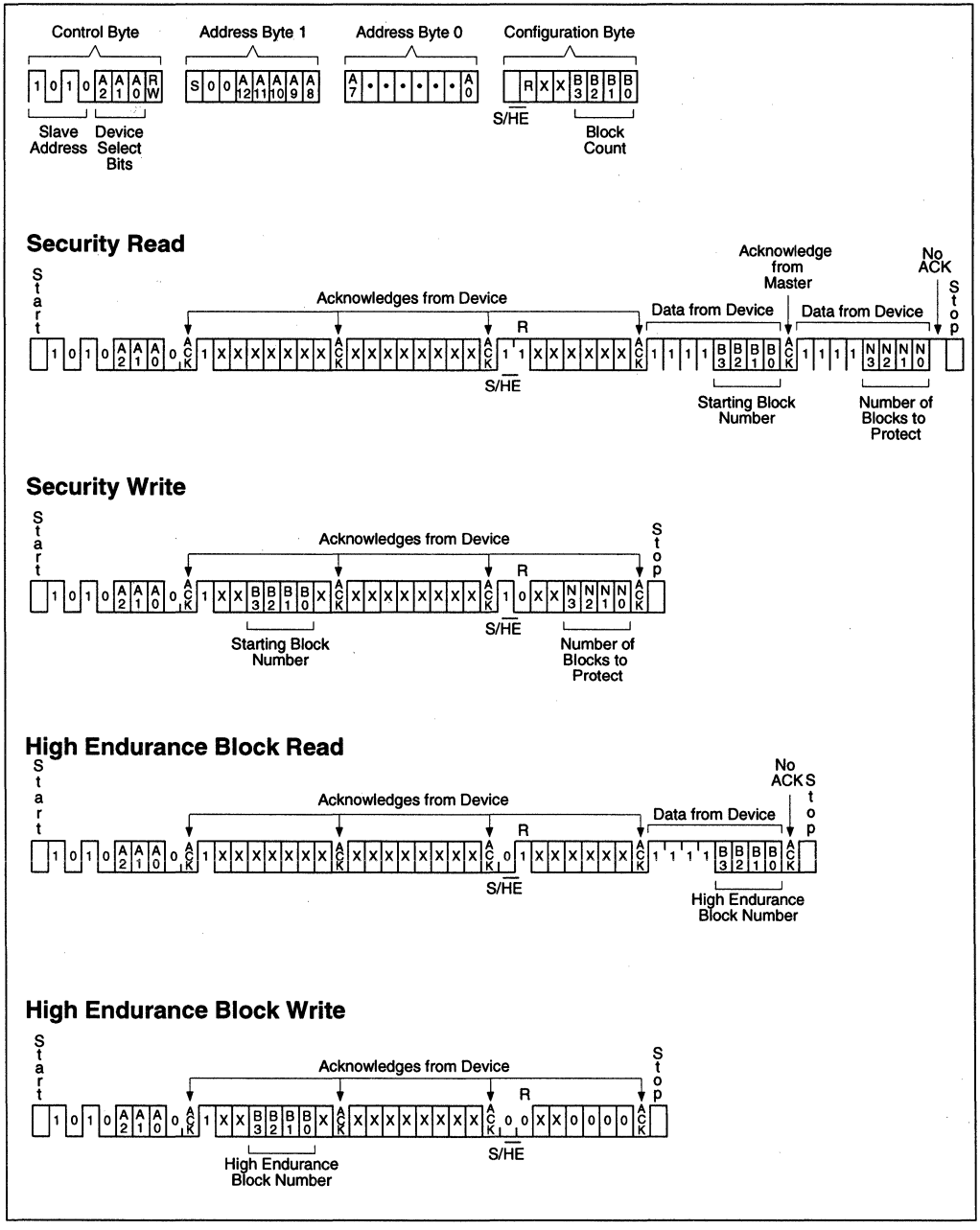


FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

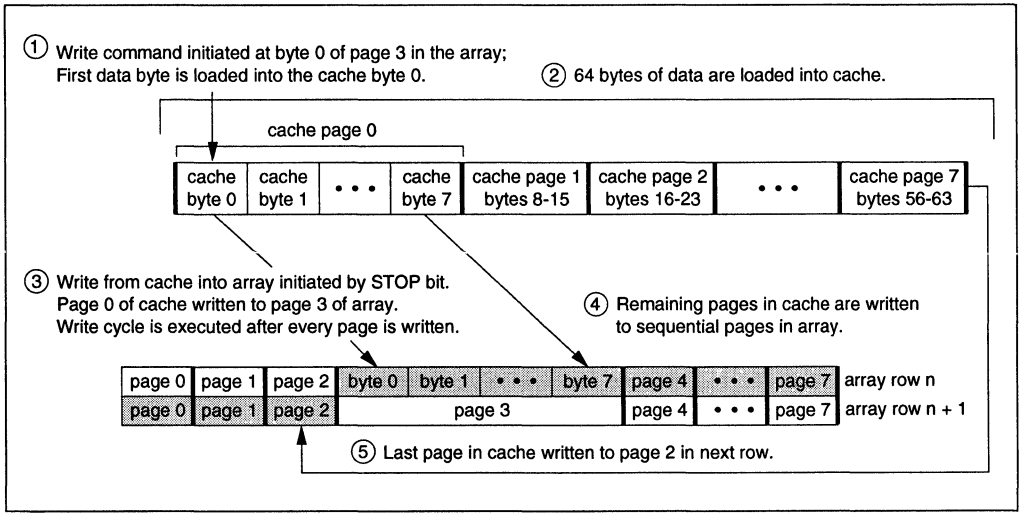
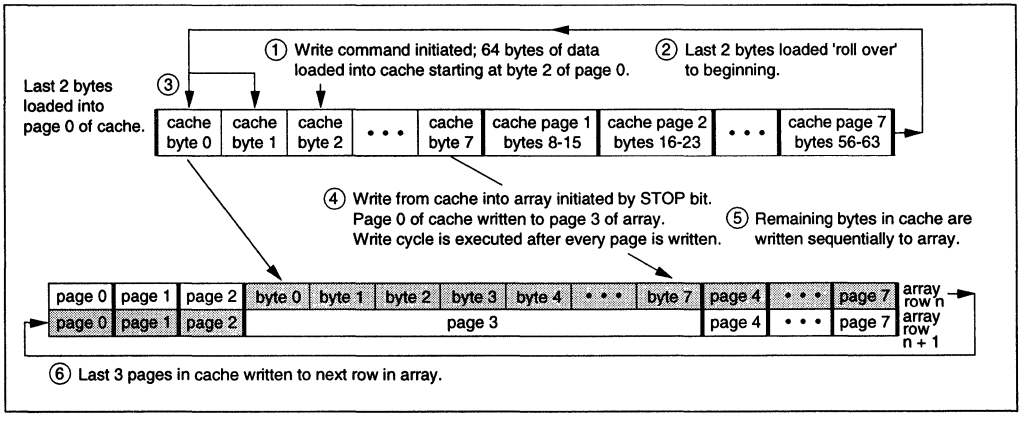
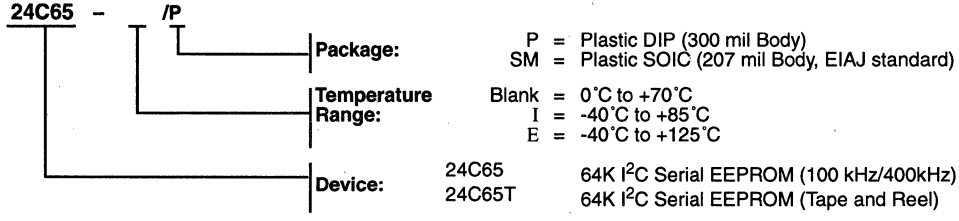


FIGURE 8-3: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



24C65 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

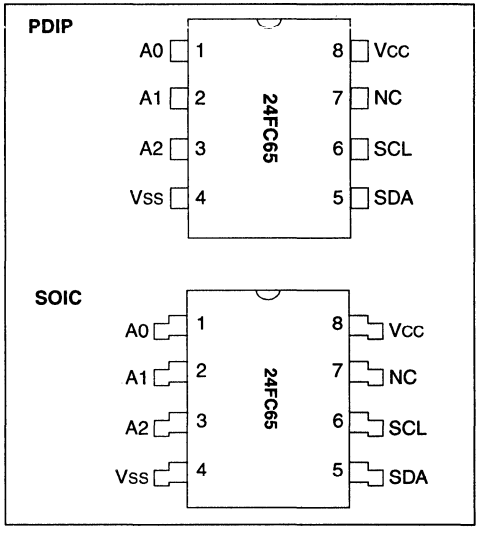
24FC65

64K 5.0V 1 MHz I²C™ Smart Serial™ EEPROM

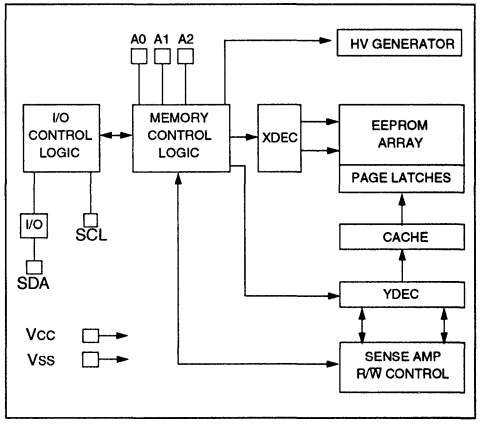
FEATURES

- Voltage operating range: 4.5V to 5.5V
  - Maximum write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 1 µA typical
- 1 MHz SE2.bus two wire protocol
- Up to eight devices may be connected to the same bus for up to 512K bits total memory
- Programmable block security options
- Programmable endurance options
- Schmitt trigger inputs for noise suppression
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - 10,000,000 E/W cycles guaranteed for a 4K block
  - 1,000,000 E/W cycles guaranteed for a 60K block
- Variable page size up to 64 bytes
- 8 byte x 8 line input cache (64 bytes) for fast write loads
- <3 ms typical write cycle time, byte or page
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

PACKAGE TYPES



BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 24FC65 is a "smart" 8K 8x 8 Serial Electrically Erasable PROM (EEPROM) with a high-speed 1MHz SE2.bus whose protocol is functionally equivalent to the industry-standard I²C bus. This device has been developed for advanced applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24FC65 offers a relocatable 4K-bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 1,000,000 ERASE/WRITE (E/W) cycles guaranteed. The 24FC65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks. Functional address lines allow the connection of up to eight 24FC65's on the same bus for up to 512K bits contiguous EEPROM memory. The 24FC65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC	—	V	
Low level input voltage	VIL	—	0.3 VCC	V	
Hysteresis of SCL and SDA	VHYS	0.05 VCC	—	V	(Note)
Low level output voltage of SDA	VOL	—	0.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V, SCL = 1 MHz
	ICC Read	—	150	µA	VCC = 5.5V, SCL = 1 MHz
Standby current	ICCS	—	5	µA	VCC = 5.5V, SCL = SDA =VCC A0, A1, A2 = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

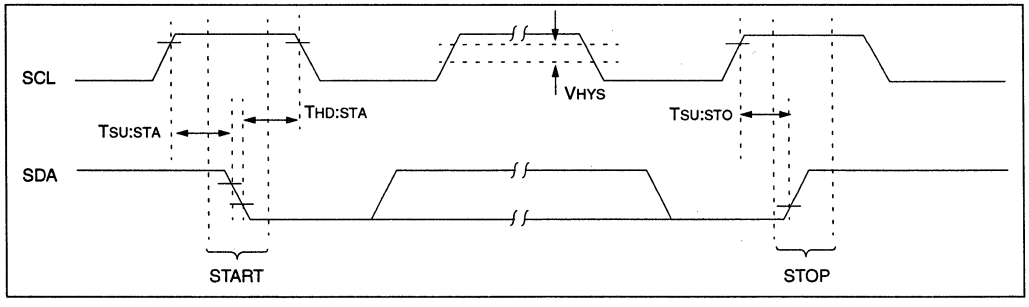


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	1 MHz Bus		Units	Remarks
		Min	Max		
Clock frequency	FCLK	0	1000	kHz	
Clock high time	THIGH	500	—	ns	
Clock low time	TLOW	500	—	ns	
SDA and SCL rise time	TR	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	100	ns	(Note 1)
START hold time	THD:STA	250	—	ns	After this period the first clock pulse is generated
START setup time	TSU:STA	250	—	ns	Only relevant for repeated START
Data input hold time	THD:DAT	0	—	ns	
Data input setup time	TSU:DAT	100	—	ns	
STOP setup time	TSU:STO	250	—	ns	
Output valid from clock	TAA	—	350	ns	(Note 2)
Bus free time	TBUF	500	—	ns	Time the bus must be free before a new transmission can start
Write cycle time	TWR	—	5	ms/page	(Note 3)
Endurance High Endurance Block Rest of Array		 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 4)

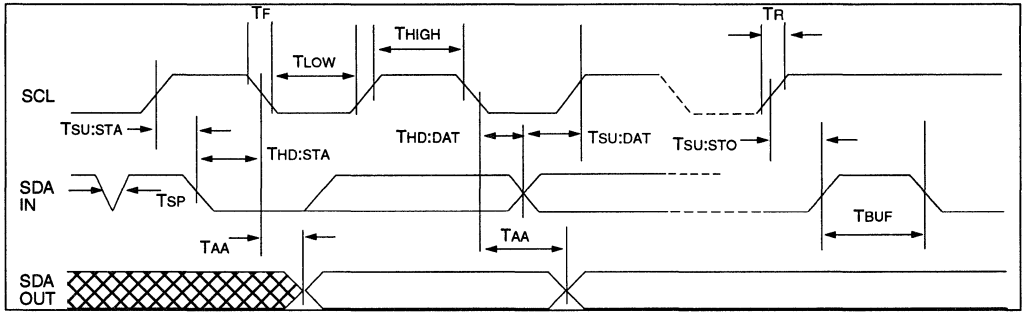
Note 1: Not 100 percent tested.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 100 ns) of the falling edge of SCL to avoid unintended generation of START or STOPs.

3: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



3

I²C™

2.0 FUNCTIONAL DESCRIPTION

The 24FC65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOPs, while the 24FC65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START. All commands must be preceded by a START.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP. All operations must be ended with a STOP.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START and terminated with a STOP. The number of the data bytes transferred between the START and STOPs is determined by the master device.

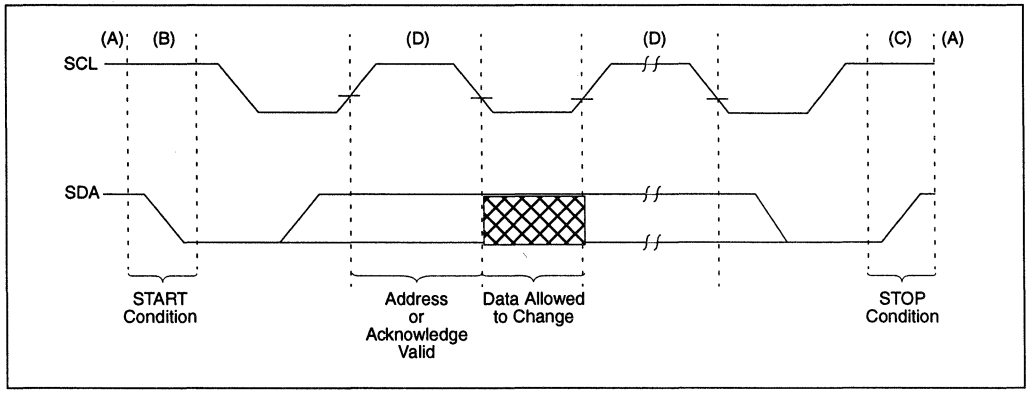
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24FC65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24FC65) must leave the data line HIGH to enable the master to generate the STOP.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

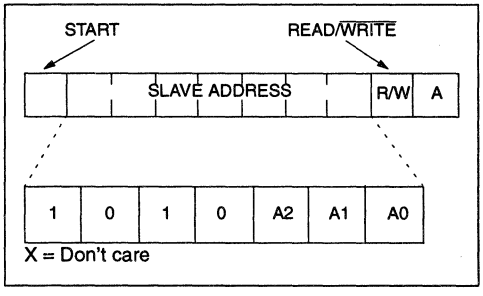


3.6 Device Addressing

A control byte is the first byte received following the START from the master device. The control byte consists of a four bit control code, for the 24FC65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 4-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the START, the 24FC65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24FC65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24FC65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the START from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24FC65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24FC65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24FC65 the master device will transmit the data word to be written into the addressed memory location. The 24FC65 acknowledges again and the master generates a STOP. This initiates the internal write cycle, and during this time the 24FC65 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24FC65 in the same way as in a byte write. But instead of generating a STOP the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24FC65. They will be written from the cache into the EEPROM array after the master has transmitted a STOP. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the STOP (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a STOP should be generated by the master. If a STOP is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The STOP can be sent at any time during the transfer. As with the byte write operation, once the STOP is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a STOP occurs or the operation is aborted (Figure 4-2).

FIGURE 4-1: BYTE WRITE

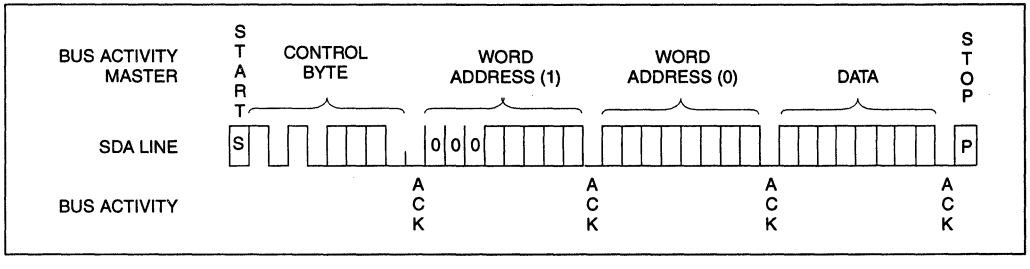


FIGURE 4-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 7-1)

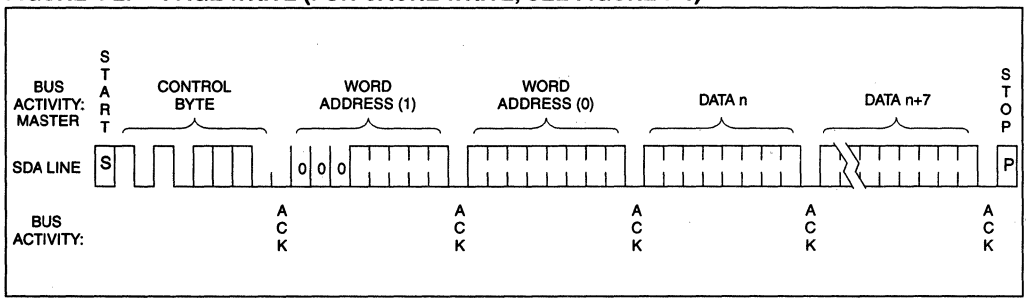


FIGURE 4-3: CURRENT ADDRESS READ

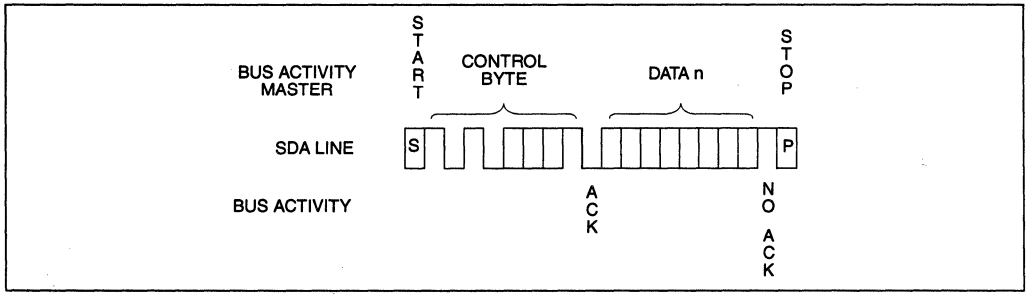


FIGURE 4-4: RANDOM READ

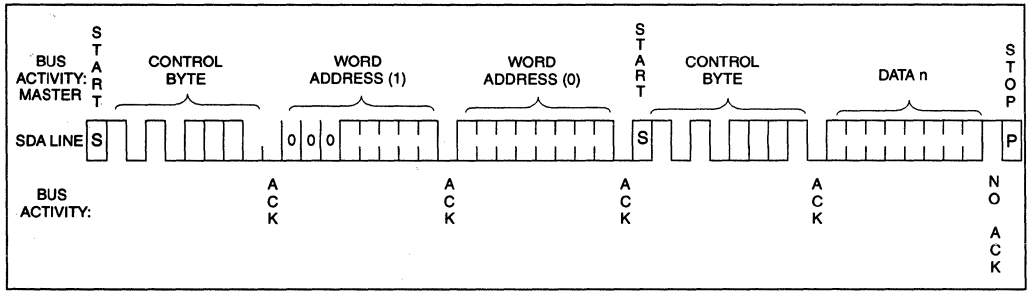
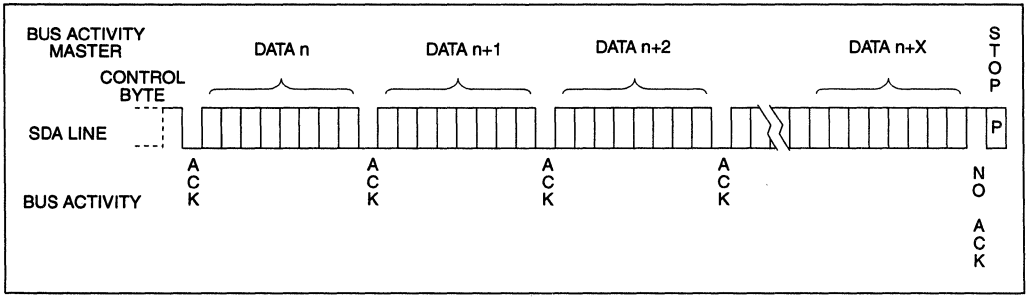


FIGURE 4-5: SEQUENTIAL READ



5.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

5.1 Current Address Read

The 24FC65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24FC65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a STOP and the 24FC65 discontinues transmission (Figure 4-3).

5.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24FC65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a START following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24FC65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a STOP which causes the 24FC65 to discontinue transmission (Figure 4-4).

5.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24FC65 transmits the first data byte, the master issues an acknowledge as opposed to the STOP used in a random read. This acknowledge directs the 24FC65 to transmit the next sequentially addressed 8 bit word (Figure 4-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a STOP.

To provide sequential reads the 24FC65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

5.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K-bits by adding up to eight 24FC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

5.5 Noise Protection

The SCL and SDA inputs incorporate Schmitt triggers which suppress noise spikes to assure proper device operation even on a noisy bus.

5.6 High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance (Figure 8-1). This block will be capable of 10,000,000 erase/write cycles guaranteed.

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

5.7 Security Options

The 24FC65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit7) of the first address byte set to a 1 (Figure 8-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit7 (S/$\overline{HE}$) set high and bit6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the

third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

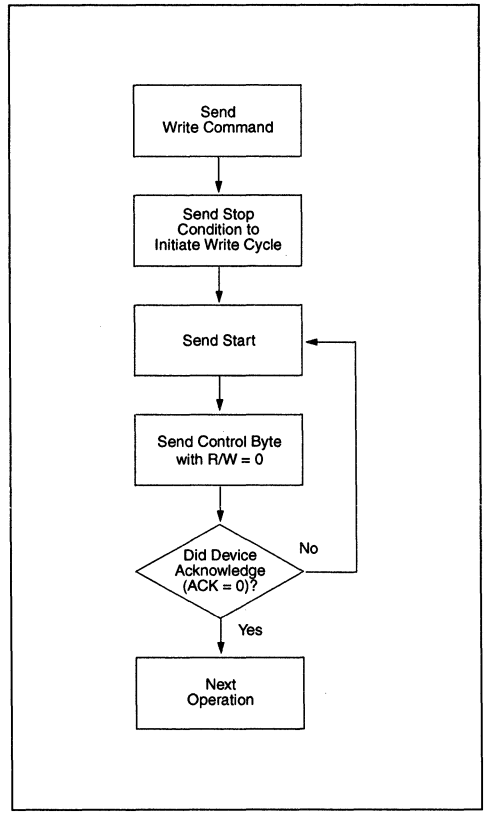
5.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (Figure 8-1).

6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a START followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (Figure 7-1) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 7-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or STOP per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

FIGURE 7-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

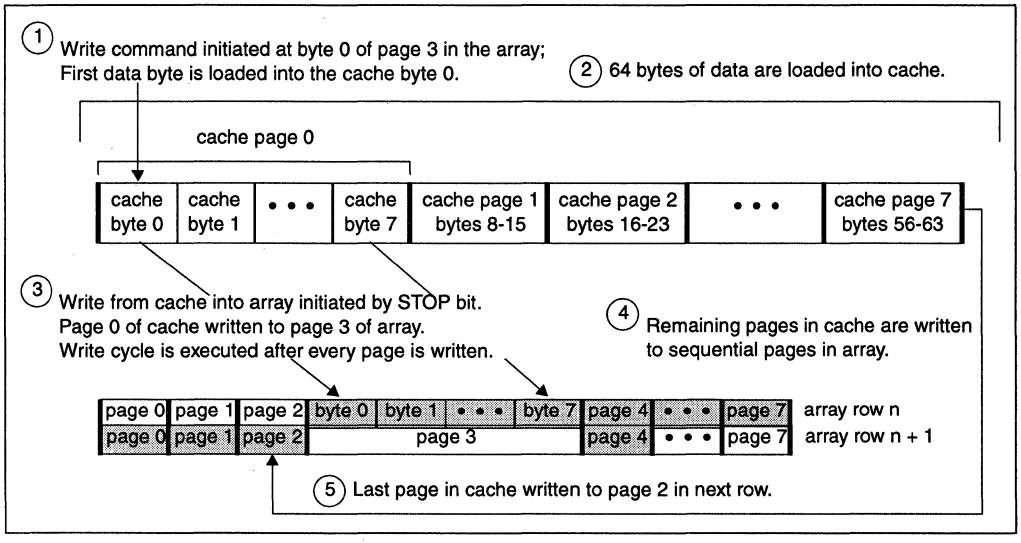
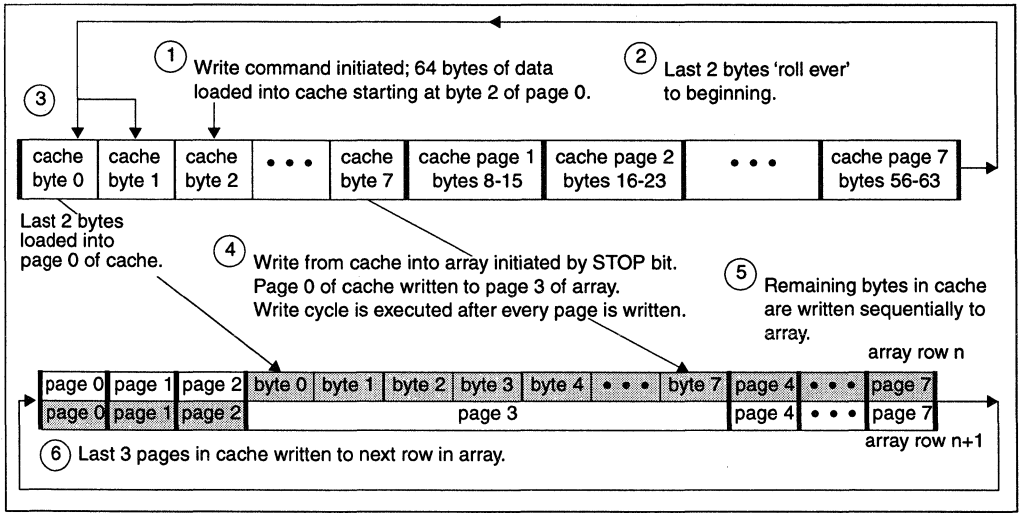


FIGURE 7-2: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24FC65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (Figure 3-2 and Figure 8-1).

8.2 SDA Serial Address/Data Input/Output

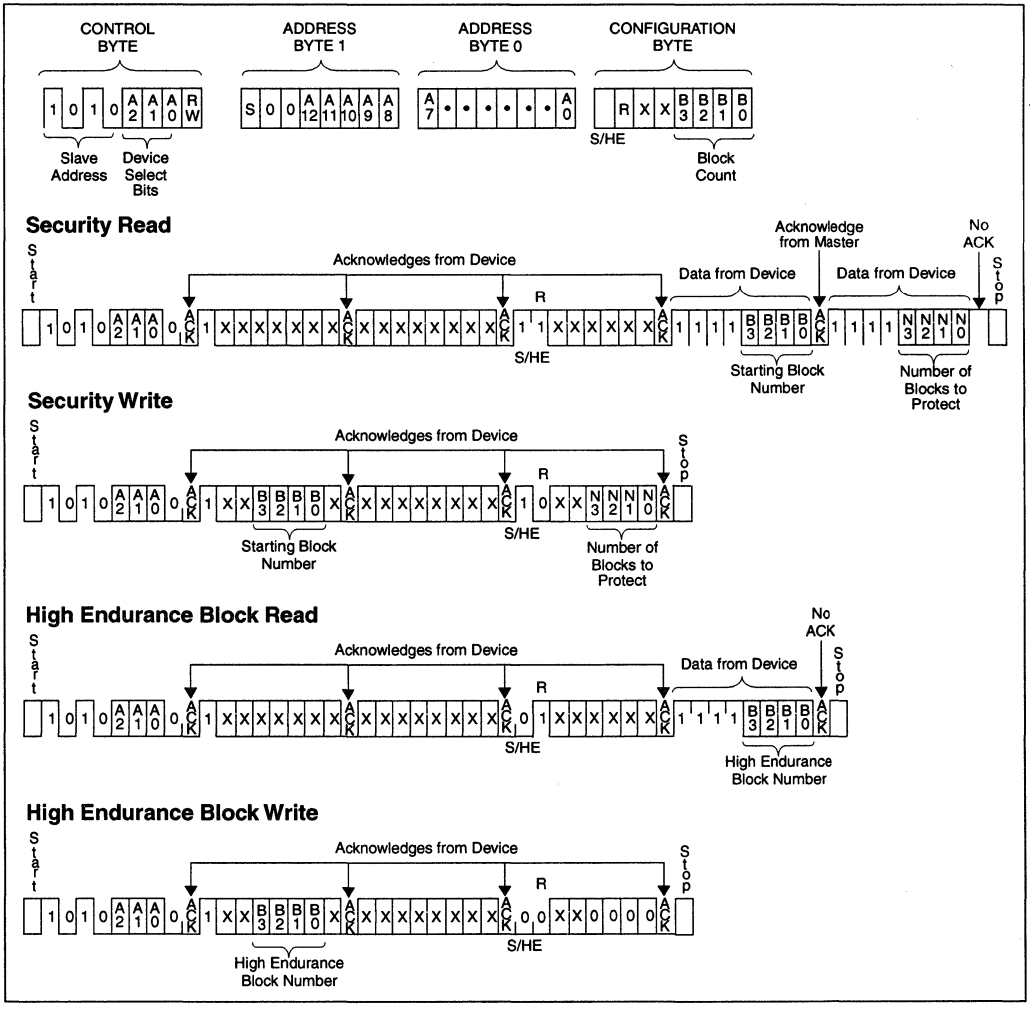
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 2 KΩ, must consider total bus capacitance and maximum rise/fall times).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOPs.

8.3 SCL Serial Clock

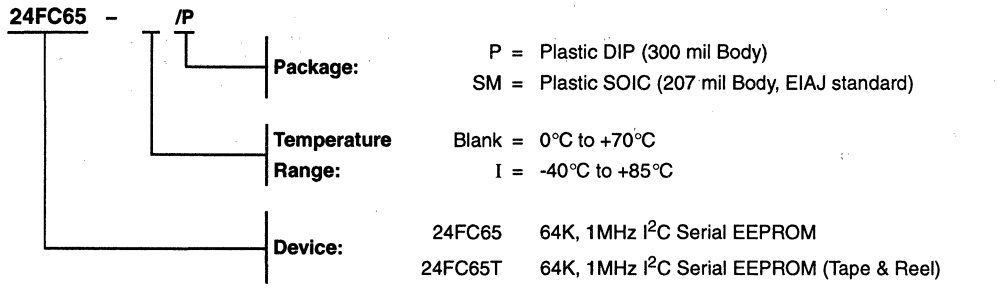
This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1: CONTROL SEQUENCE BIT ASSIGNMENTS



24FC65 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA128/24LC128

128K I^2C^{TM} CMOS Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA128	1.8-5.5V	400 kHz†	I
24LC128	2.5-5.5V	400 kHz‡	I, E

†100 kHz for Vcc < 2.5V.
‡100 kHz for E temperature range.

FEATURES

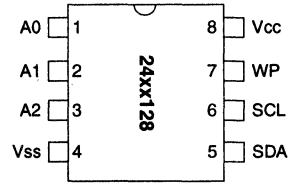
- Low power CMOS technology
  - Maximum write current 3 mA at 5.5V
  - Maximum read current 400 µA at 5.5V
  - Standby current 100 nA typical at 5.5V
- 2-wire serial interface bus, I^2C compatible
- Cascadable for up to eight devices
- Self-timed ERASE/WRITE cycle
- 64-byte page-write mode available
- 5 ms max write-cycle time
- Hardware write protect for entire array
- Output slope control to eliminate ground bounce
- Schmitt trigger inputs for noise suppression
- 1,000,000 erase/write cycles guaranteed
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC (150 and 208 mil) packages
- 14-pin TSSOP package
- Temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

DESCRIPTION

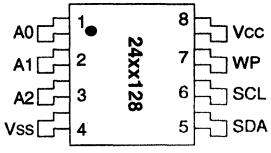
The Microchip Technology Inc. 24AA128/24LC128 (24xx128*) is a 16K x 8 (128K bit) Serial Electrically Erasable PROM, capable of operation across a broad voltage range (1.8V to 5.5V). It has been developed for advanced, low power applications such as personal communications or data acquisition. This device also has a page-write capability of up to 64 bytes of data. This device is capable of both random and sequential reads up to the 128K boundary. Functional address lines allow up to eight devices on the same bus, for up to 1M bit address space. This device is available in the standard 8-pin plastic DIP, 8-pin SOIC (150 and 208 mil), and 14-pin TSSOP packages.

PACKAGE TYPE

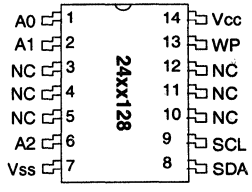
PDIP



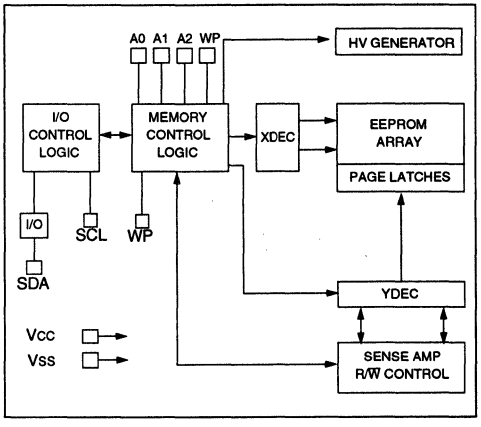
SOIC



TSSOP



BLOCK DIAGRAM



I^2C is a trademark of Philips Corporation.
*24xx128 is used in this document as a generic part number for the 24AA128/24LC128 devices.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
A0, A1, A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8 to 5.5V (24AA128) +2.5 to 5.5V (24LC128)

TABLE 1-2 DC CHARACTERISTICS

All parameters apply across the specified operating ranges, unless otherwise noted.	Industrial (I): VCC = +1.8V to 5.5V Tamb = -40°C to +85°C Automotive (E): VCC = +4.5V to 5.5V Tamb = -40°C to 125°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL, SDA, and WP pins:					
High level input voltage	VIH	0.7 VCC	—	V	
Low level input voltage	VIL	—	0.3 VCC	V	VCC ≥ 2.5V
			0.2 VCC	V	VCC < 2.5V
Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	VHYS	0.05 VCC	—	V	VCC ≥ 2.5V (Note)
Low level output voltage	VOL	—	0.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = VSS or VCC, WP = VSS VIN = VSS or VCC, WP = VCC
Output leakage current	ILO	-10	10	µA	VOUT = VSS or VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, f_c = 1 MHz
Operating current	ICC Read	—	400	µA	VCC = 5.5V, SCL = 400 kHz
	ICC Write	—	3	mA	VCC = 5.5V
Standby current	ICCS	—	1	µA	SCL = SDA = VCC = 5.5V A0, A1, A2, WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING DATA

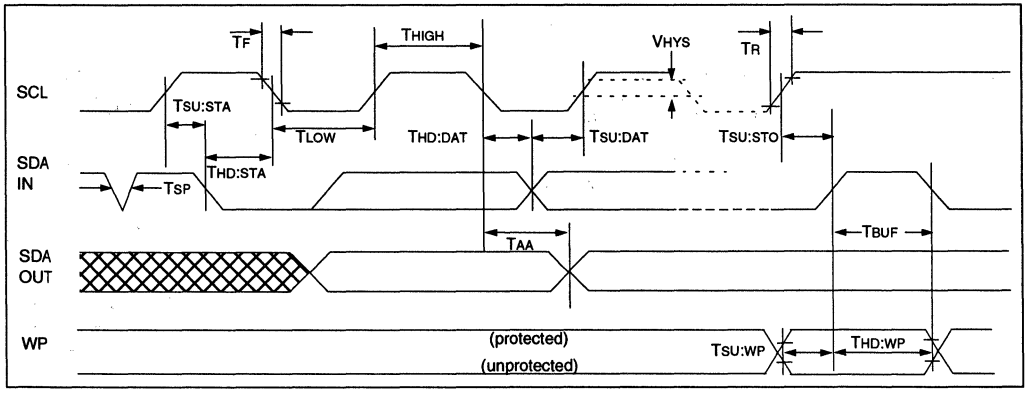


TABLE 1-3 AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Industrial (I): VCC = +1.8V to 5.5V Tamb = -40°C to +85°C Automotive (E): VCC = +4.5V to 5.5V Tamb = -40°C to 125°C				
Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
START condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
STOP condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
WP setup time	TSU:WP	4000 4000 600	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
WP hold time	THD:WP	4700 4700 1300	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ VCC ≤ 5.5V (E Temp range) 1.8V ≤ VCC ≤ 2.5V 2.5V ≤ VCC ≤ 5.5V
Output fall time from VIH minimum to VIL maximum	TOF	10	250	ns	C_B ≤ 100 pF (Note 1)
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1 and 3)
Write cycle time (byte or page)	TWC	—	5	ms	
Endurance		1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's website.

2.0 PIN DESCRIPTIONS

2.1 A0, A1, A2 Chip Address Inputs

The A0, A1, A2 inputs are used by the 24xx128 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different chip select bit combinations. If left unconnected, these inputs will be pulled down internally to VSS.

2.2 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pullup resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.4 WP

This pin can be connected to either VSS, VCC or left floating. An internal pull-down resistor on this pin will keep the device in the unprotected state if left floating. If tied to VSS or left floating, normal memory operation is enabled (read/write the entire memory 0000-3FFF).

If tied to VCC, WRITE operations are inhibited. Read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24xx128 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions while the 24xx128 works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must end with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24xx128 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24xx128) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

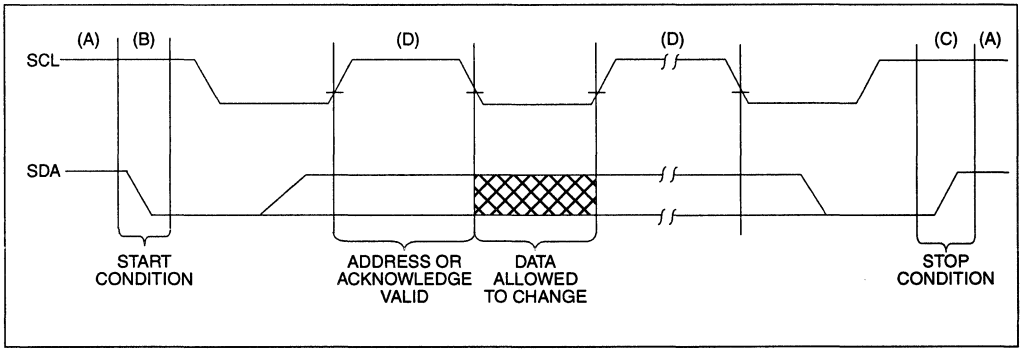
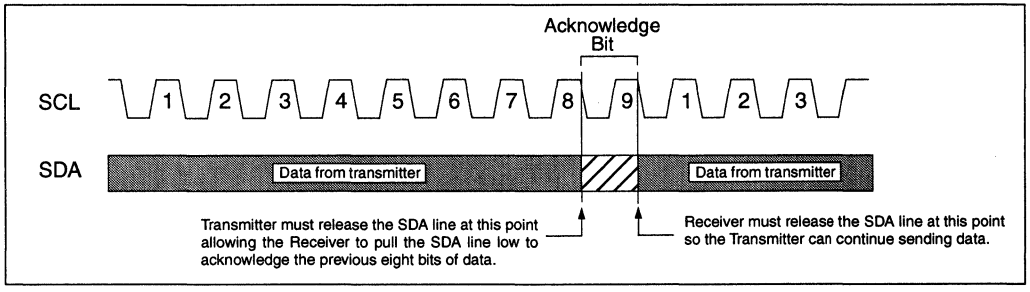


FIGURE 4-2: ACKNOWLEDGE TIMING



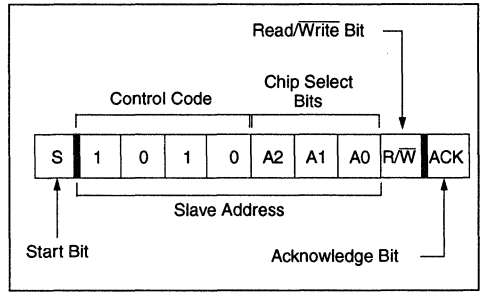
5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a 4-bit control code; for the 24xx128 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24xx128 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A13...A0 are used, the upper two address bits are don't care bits. The upper address bits are transferred first, followed by the less significant bits.

Following the start condition, the 24xx128 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24xx128 will select a read or write operation.

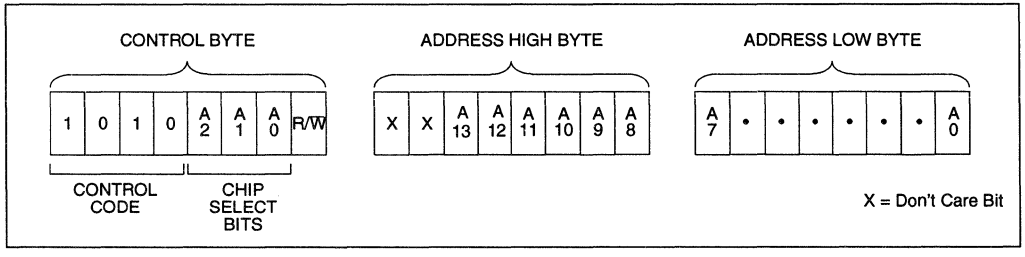
FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 1 Mbit by adding up to eight 24xx128's on the same bus. In this case, software can use A0 of the control byte as address bit A14; A1, as address bit A15; and A2, as address bit A16. It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start condition from the master, the control code (four bits), the chip select (three bits), and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24xx128. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24xx128, the master device will transmit the data word to be written into the addressed memory location. The 24xx128 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and, during this time, the 24xx128 will not generate acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24xx128 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 63 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the six lower address pointer bits are internally incremented by one. If the master should transmit more than 64 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (0000-3FFF) when the pin is tied to Vcc. If tied to Vss or left floating, the write protection is disabled. The WP pin is sampled at the STOP bit for every write command (Figure 1-1) Toggling the WP pin after the STOP bit will have no effect on the execution of the write cycle.

FIGURE 6-1: BYTE WRITE

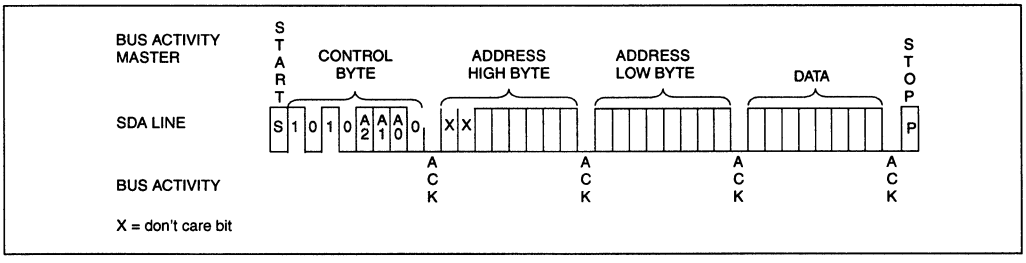
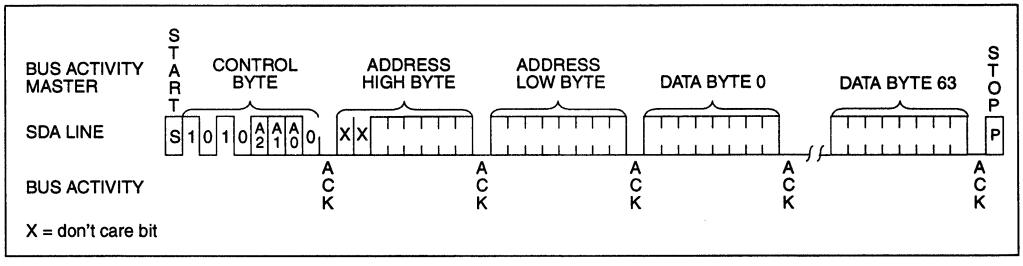


FIGURE 6-2: PAGE WRITE



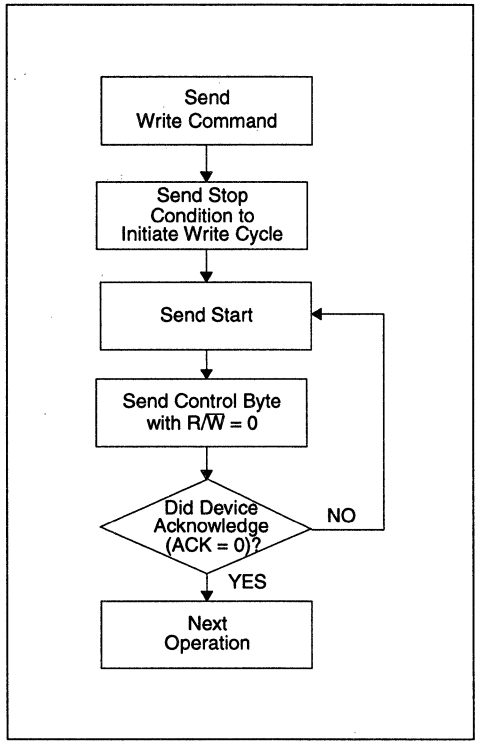
3

I²C™

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (This feature can be used to maximize bus throughput.) Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition, followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

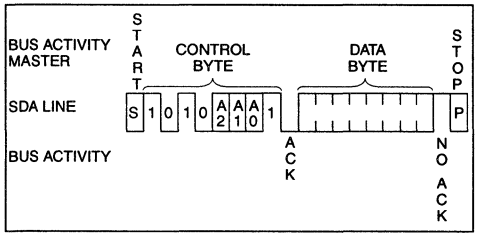
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24xx128 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the 24xx128 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24xx128 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24xx128 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then, the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24xx128 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24xx128 to discontinue transmission (Figure 8-2). After a random read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24xx128 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24xx128 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition. To provide sequential reads, the 24xx128 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 3FFF to address 0000 if the master acknowledges the byte received from the array address 3FFF.

FIGURE 8-2: RANDOM READ

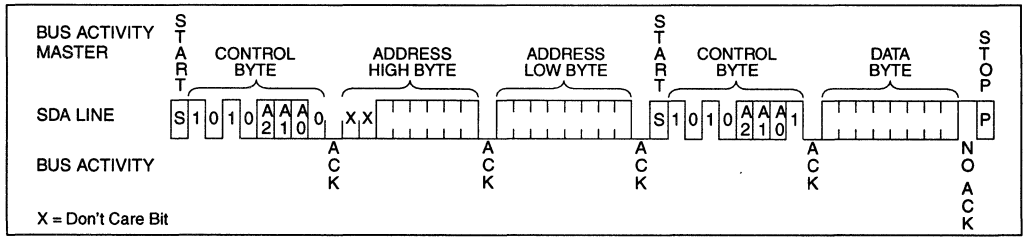
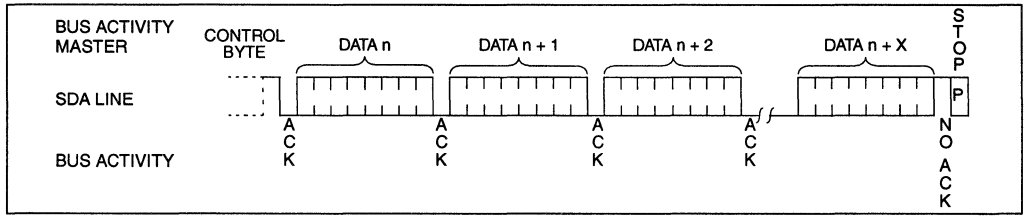
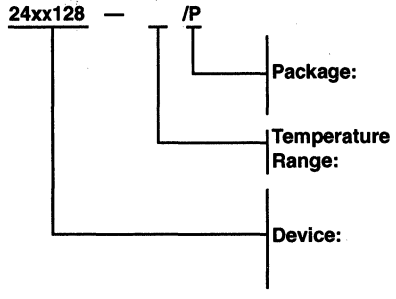


FIGURE 8-3: SEQUENTIAL READ



24xx128 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	P = Plastic DIP (300 mil Body), 8-lead SM = Plastic SOIC (208 mil Body, EIAJ standard), 8-lead SN = Plastic SOIC (150 mil Body), 8-lead ST = TSSOP, 14-lead
Temperature Range:	I = -40°C to +85°C E = -40°C to +125°C
Device:	24AA128 128K bit 1.8V I^2C Serial EEPROM 24AA128T 128K bit 1.8V I^2C Serial EEPROM (Tape and Reel) 24LC128 128K bit 2.5V I^2C Serial EEPROM 24LC128T 128K bit 2.5V I^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24AA256/24LC256

256K I²C™ CMOS Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA256	1.8-5.5V	400 kHz†	I
24LC256	2.5-5.5V	400 kHz‡	I, E

† 100 kHz for Vcc < 2.5V.
‡ 100 kHz for E temperature range.

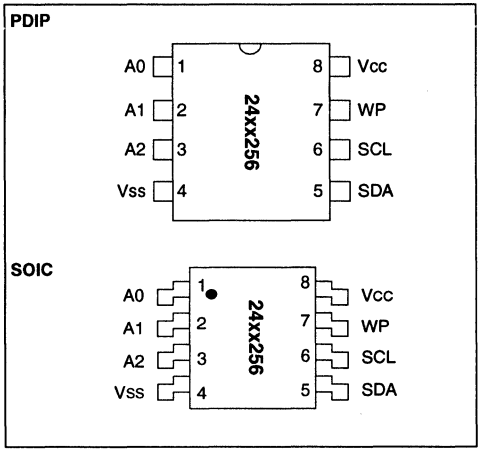
FEATURES

- Low power CMOS technology
  - Maximum write current 3 mA at 5.5V
  - Maximum read current 400 µA at 5.5V
  - Standby current 100 nA typical at 5.5V
- 2-wire serial interface bus, I²C compatible
- Cascadable for up to eight devices
- Self-timed ERASE/WRITE cycle
- 64-byte page-write mode available
- 5 ms max write-cycle time
- Hardware write protect for entire array
- Schmitt trigger inputs for noise suppression
- 100,000 erase/write cycles guaranteed
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP and SOIC (208 mil) packages
- Temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

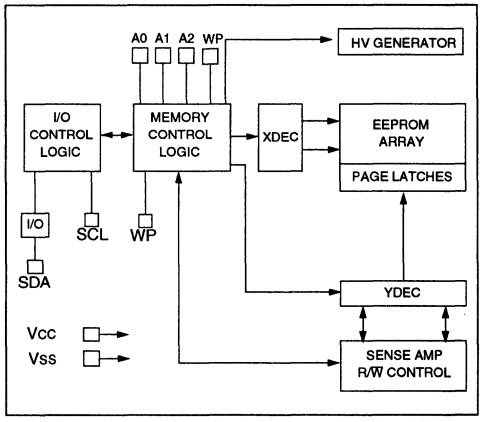
DESCRIPTION

The Microchip Technology Inc. 24AA256/24LC256 (24xx256*) is a 32K x 8 (256K bit) Serial Electrically Erasable PROM, capable of operation across a broad voltage range (1.8V to 5.5V). It has been developed for advanced, low power applications such as personal communications or data acquisition. This device also has a page-write capability of up to 64 bytes of data. This device is capable of both random and sequential reads up to the 256K boundary. Functional address lines allow up to eight devices on the same bus, for up to 2 Mbit address space. This device is available in the standard 8-pin plastic DIP, and 8-pin SOIC (208 mil) packages.

PACKAGE TYPE



BLOCK DIAGRAM



3

I²C™

I²C is a trademark of Philips Corporation.
*24xx256 is used in this document as a generic part number for the 24AA256/24LC256 devices.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
A0, A1, A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect Input
Vcc	+1.8 to 5.5V (24AA256) +2.5 to 5.5V (24LC256)

TABLE 1-2 DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Industrial (I): Vcc = +1.8V to 5.5V Tamb = -40°C to +85°C Automotive (E): Vcc = +4.5V to 5.5V Tamb = -40°C to 125°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL, SDA, and WP pins:					
High level input voltage	VIH	0.7 Vcc	—	V	
Low level input voltage	VIL	—	0.3 Vcc	V	Vcc ≥ 2.5V
			0.2 Vcc	V	Vcc < 2.5V
Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	VHYS	0.05 Vcc	—	V	Vcc ≥ 2.5V (Note)
Low level output voltage	VOL	—	0.40	V	IOL = 3.0 mA @ Vcc = 4.5V IOL = 2.1 mA @ Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = Vss or Vcc, WP = Vss VIN = Vss or Vcc, WP = Vcc
Output leakage current	ILO	-10	10	µA	VOUT = Vss or Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note) Tamb = 25°C, f_c= 1 MHz
Operating current	Icc Write	—	3	mA	Vcc = 5.5V
	Icc Read	—	400	µA	Vcc = 5.5V, SCL = 400 kHz
Standby current	Iccs	—	1	µA	SCL = SDA = Vcc = 5.5V A0, A1, A2, WP = Vss

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING DATA

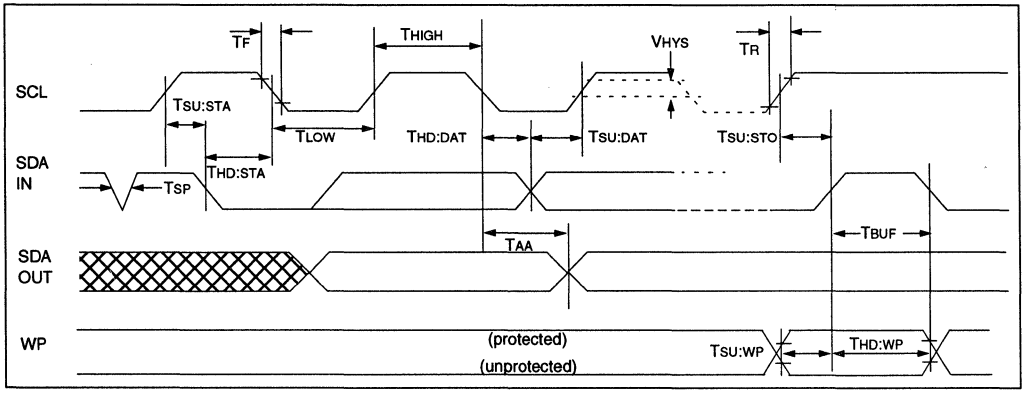


TABLE 1-3 AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Industrial (I): Vcc = +1.8V to 5.5V Tamb = -40°C to +85°C Automotive (E): Vcc = +4.5V to 5.5V Tamb = -40°C to 125°C				
Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK	— — —	100 100 400	kHz	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Clock high time	THIGH	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Clock low time	TLOW	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
SDA and SCL rise time (Note 1)	TR	— — —	1000 1000 300	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
SDA and SCL fall time	TF	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
START condition setup time	TSU:STA	4700 4700 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Data input hold time	THD:DAT	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250 250 100	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
STOP condition setup time	TSU:STO	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
WP setup time	TSU:WP	4000 4000 600	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
WP hold time	THD:WP	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Output valid from clock (Note 2)	TAA	— — —	3500 3500 900	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Bus free time: Time the bus must be free before a new transmission can start	TBUF	4700 4700 1300	— — —	ns	4.5V ≤ Vcc ≤ 5.5V (E Temp range) 1.8V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V
Output fall time from VIH minimum to VIL maximum	TOF	10	250	ns	C_B ≤ 100 pF (Note 1)
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	ns	(Notes 1 and 3)
Write cycle time (byte or page)	TWC	—	5	ms	
Endurance		100,000	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 PIN DESCRIPTIONS

2.1 A0, A1, A2 Chip Address Inputs

The A0, A1, A2 inputs are used by the 24xx256 for multiple device operation. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different chip select bit combinations. If left unconnected, these inputs will be pulled down internally to VSS.

2.2 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.4 WP

This pin can be connected to either VSS, VCC or left floating. An internal pull-down on this pin will keep the device in the unprotected state if left floating. If tied to VSS or left floating, normal memory operation is enabled (read/write the entire memory 0000-7FFF).

If tied to VCC, WRITE operations are inhibited. Read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24xx256 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions while the 24xx256 works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must end with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24xx256 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24xx256) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

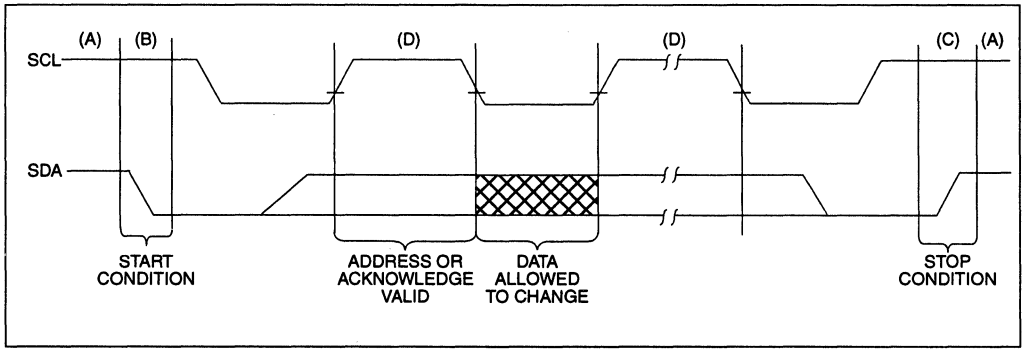
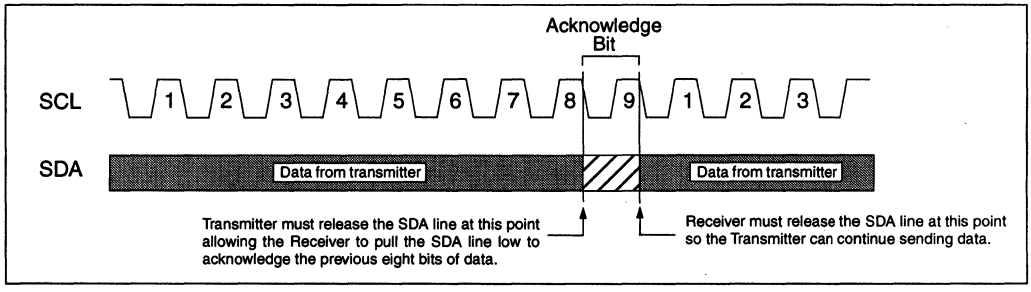


FIGURE 4-2: ACKNOWLEDGE TIMING



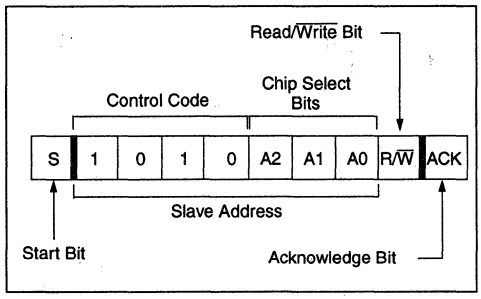
5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a 4-bit control code; for the 24xx256 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24xx256 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A14...A0 are used, the upper address bit is a don't care bit. The upper address bits are transferred first, followed by the less significant bits.

Following the start condition, the 24xx256 monitors the SDA bus checking the control byte being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24xx256 will select a read or write operation.

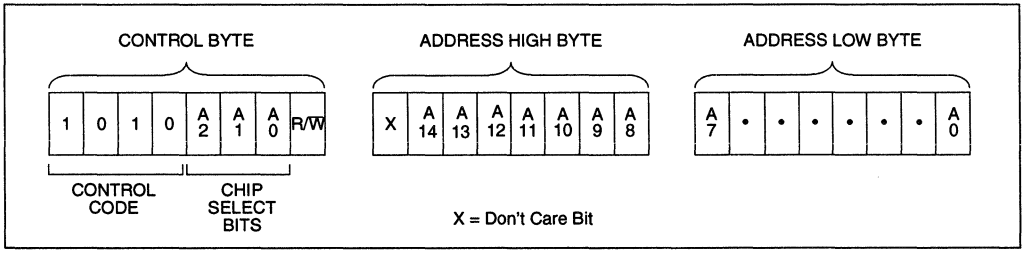
FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 2 Mbit by adding up to eight 24xx256's on the same bus. In this case, software can use A0 of the control byte as address bit A15; A1, as address bit A16; and A2, as address bit A17. It is not possible to read or write across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start condition from the master, the control code (four bits), the chip select (three bits), and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24xx256. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24xx256, the master device will transmit the data word to be written into the addressed memory location. The 24xx256 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and, during this time, the 24xx256 will not generate acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24xx256 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 63 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the six lower address pointer bits are internally incremented by one. If the master should transmit more than 64 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command subject to TBUF.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (0000-7FFF) when the pin is tied to VCC. If tied to VSS or left floating, the write protection is disabled. The WP pin is sampled at the STOP bit for every write command (Figure 1-1) Toggling the WP pin after the STOP bit will have no effect on the execution of the write cycle.

FIGURE 6-1: BYTE WRITE

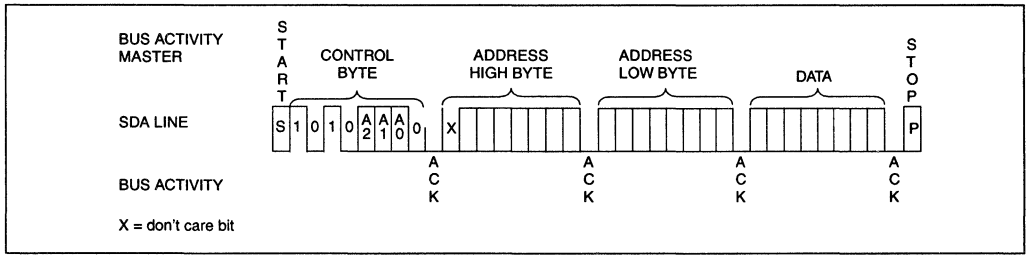
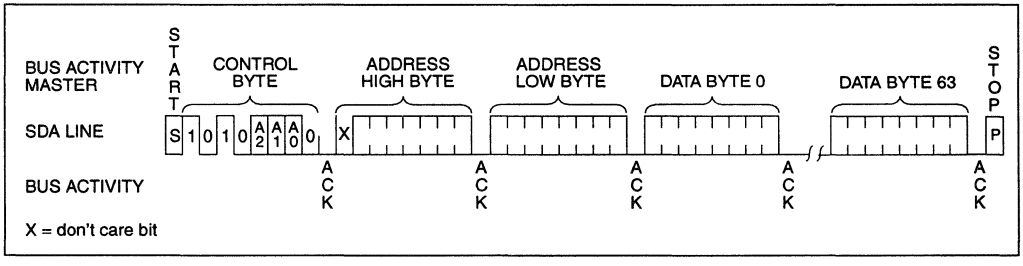


FIGURE 6-2: PAGE WRITE



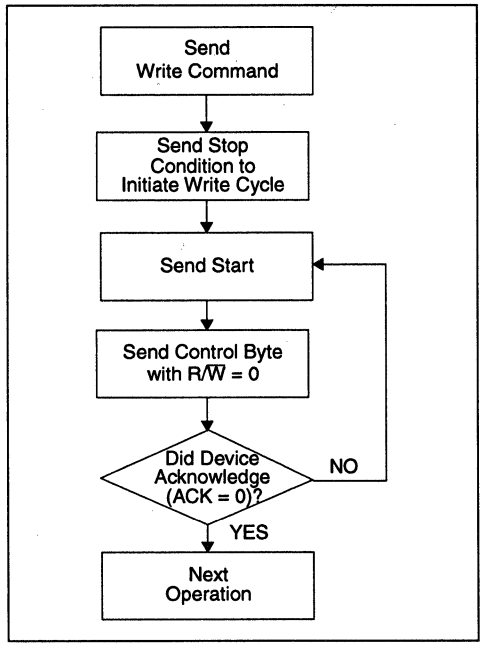
3

I²C™

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (This feature can be used to maximize bus throughput.) Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition, followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

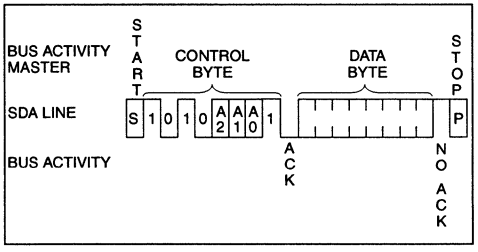
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24xx256 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the 24xx256 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24xx256 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24xx256 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then, the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24xx256 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24xx256 to discontinue transmission (Figure 8-2). After a random read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24xx256 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24xx256 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition. To provide sequential reads, the 24xx256 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 7FFF to address 0000 if the master acknowledges the byte received from the array address 7FFF.

FIGURE 8-2: RANDOM READ

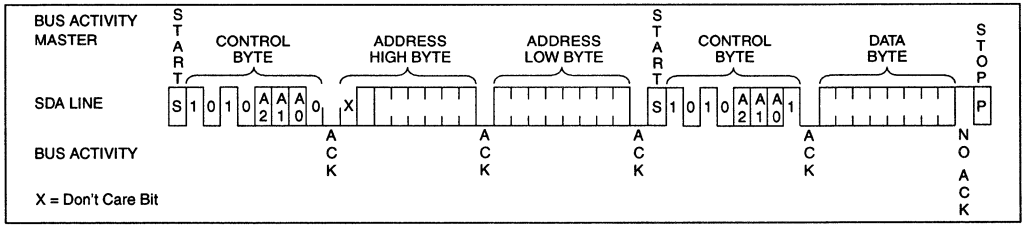
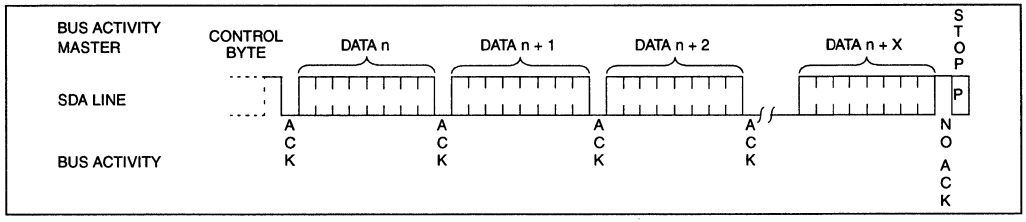
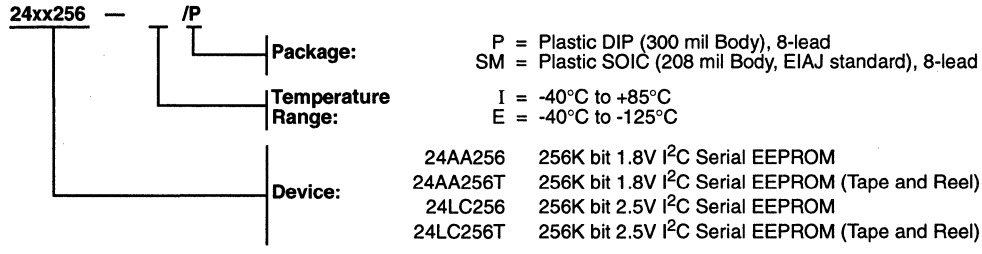


FIGURE 8-3: SEQUENTIAL READ



24xx256 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

SECTION 4
MICROWIRE® SERIAL EEPROM PRODUCT SPECIFICATIONS

93AA46	1K 1.8V Microwire® Serial EEPROM	4-1
93LC46A	1K 2.5V Microwire® Serial EEPROM	4-11
93LC46B	1K 2.5V Microwire® Serial EEPROM	4-11
93C46B	1K 5.0V Microwire® Serial EEPROM	4-19
93AA56	2K 1.8V Microwire® Serial EEPROM	4-1
93LC56A	2K 2.5V Microwire® Serial EEPROM	4-27
93LC56B	2K 2.5V Microwire® Serial EEPROM	4-27
93C56A	2K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-35
93C56B	2K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-35
93LCS56	2K 2.5V Microwire® Serial EEPROM with Software Write Protect	4-43
93AA66	4K 1.8V Microwire® Serial EEPROM	4-1
93LC66A	4K 2.5V Microwire® Serial EEPROM	4-55
93LC66B	4K 2.5V Microwire® Serial EEPROM	4-55
93C66A	4K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-63
93C66B	4K 5.0V Automotive Temperature Microwire® Serial EEPROM	4-63
93LCS66	4K 2.5V Microwire® Serial EEPROM with Software Write Protect	4-43
93AA76	8K 1.8V Microwire® Serial EEPROM	4-71
93LC76	8K 2.5V Microwire® Serial EEPROM	4-81
93C76	8K 5.0V Microwire® Serial EEPROM	4-91
93AA86	16K 1.8V Microwire® Serial EEPROM	4-71
93LC86	16K 2.5V Microwire® Serial EEPROM	4-81
93C86	16K 5.0V Microwire® Serial EEPROM	4-91

Microwire is a registered trademark of National Semiconductor Incorporated.

93AA46/56/66

1K/2K/4K 1.8V Microwire® Serial EEPROM

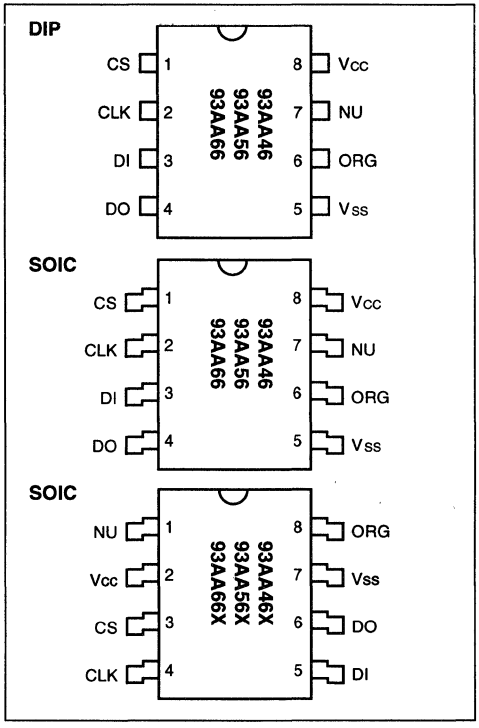
FEATURES

- Single supply with programming operation down to 1.8V
- Low power CMOS technology
  - 70 µA typical active READ current at 1.8V
  - 2 µA typical standby current at 1.8V
- ORG pin selectable memory configuration
  - 128 x 8- or 64 x 16-bit organization (93AA46)
  - 256 x 8- or 128 x 16-bit organization (93AA56)
  - 512 x 8 or 256 x 16 bit organization (93AA66)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC (SOIC in JEDEC and EIAJ standards)
- Temperature ranges supported
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

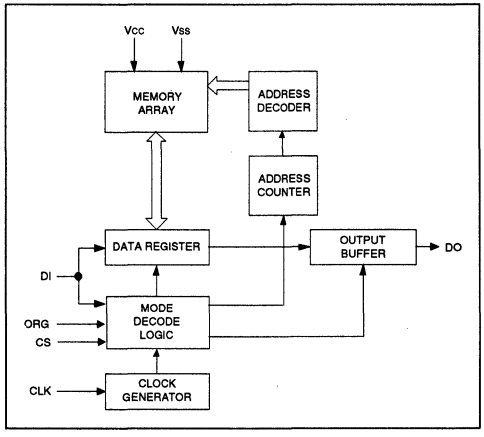
DESCRIPTION

The Microchip Technology Inc. 93AA46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93AA Series is available in standard 8-pin DIP and surface mount SOIC packages. The rotated pin-out 93AA46X/56X/66X are offered in the "SN" package only.

PACKAGE TYPES



BLOCK DIAGRAM



Microwire is a registered trademark of National Semiconductor Incorporated.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
ORG	Memory Configuration
NU	Not Utilized
VCC	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

VCC = +1.8V to +5.5V Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
High level input voltage	VIH1	2.0	—	VCC+1	V	VCC ≥ 2.7V
	VIH2	0.7 VCC	—	VCC+1	V	VCC < 2.7V
Low level input voltage	VIL1	-0.3	—	0.8	V	VCC ≥ 2.7V
	VIL2	-0.3	—	0.2 VCC	V	VCC < 2.7V
Low level output voltage	VOL1	—	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
	VOL2	—	—	0.2	V	IOL = 100µA; VCC = 1.8V
High level output voltage	VOH1	2.4	—	—	V	IOH = -400 µA; VCC = 4.5V
	VOH2	VCC-0.2	—	—	V	IOH = -100 µA; VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	—	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	—	7	pF	VIN/VOUT = 0V (Note 1 & 2) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	—	3	mA	FCLK=2 MHz; VCC=5.5V (Note 2)
	ICC read	—	—	1	mA	FCLK = 2 MHz; VCC = 5.5V
				500	µA	FCLK = 1 MHz; VCC = 3.0V
			70		µA	FCLK = 1 MHz; VCC = 1.8V
Standby current	ICCS			100	µA	CLK = CS = 0V; VCC = 5.5V
				30	µA	CLK = CS = 0V; VCC = 3.0V
			2		µA	CLK = CS = 0V; VCC = 1.8V
						ORG, DI = VSS or VCC
Clock frequency	FCLK			2	MHz	VCC ≥ 4.5V
				1	MHz	VCC < 4.5V
Clock high time	TCKH	250			ns	
Clock low time	TCKL	250			ns	
Chip select setup time	TCSS	50			ns	Relative to CLK
Chip select hold time	TCSH	0			ns	Relative to CLK
Chip select low time	TCSL	250			ns	
Data input setup time	TDIS	100			ns	Relative to CLK
Data input hold time	TDIH	100			ns	Relative to CLK
Data output delay time	TPD			400	ns	CL = 100 pF
Data output disable time	TCZ			100	ns	CL = 100 pF (Note 2)
Status valid time	TSV			500	ns	CL = 100 pF
Program cycle time	TWC		4	10	ms	ERASE/WRITE mode
	TEC		8	15	ms	ERAL mode (VCC = 5V ± 10%)
	TWL		16	30	ms	WRAL mode (VCC = 5V ± 10%)
Endurance	—	1M	—	1M	—	25°C, VCC = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

TABLE 1-3: INSTRUCTION SET FOR 93AA46: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	9
ERAL	1	00	1 0 X X X X	—	(RDY/BSY)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/BSY)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

TABLE 1-4: INSTRUCTION SET FOR 93AA46: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/BSY)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/BSY)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

TABLE 1-5: INSTRUCTION SET FOR 93AA56: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-6: INSTRUCTION SET FOR 93AA56: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

TABLE 1-7: INSTRUCTION SET FOR 93AA66: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-8: INSTRUCTION SET FOR 93AA66: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

2.4 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

2.5 Erase/Write Enable and Disable (EWEN,EWDS)

The 93AA46/56/66 power up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.6 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word typical.

2.7 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word typical.

2.8 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete.

The ERAL cycle takes (8 ms typical).

2.9 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 16 ms typical.

FIGURE 2-1: SYNCHRONOUS DATA TIMING

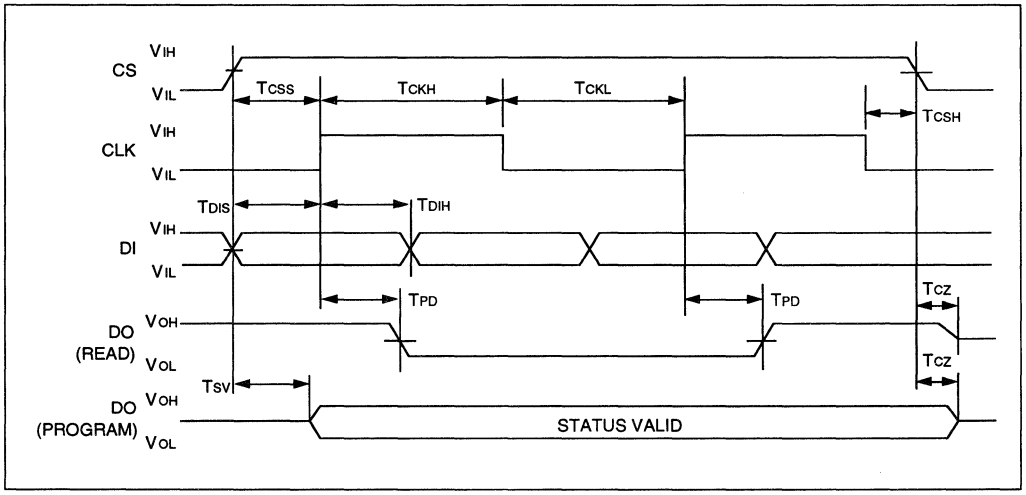
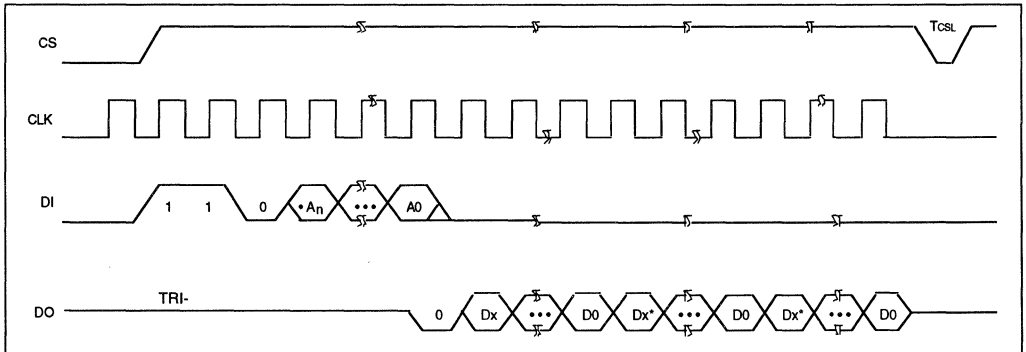


FIGURE 2-2: READ TIMING



Tri-State is a registered trademark of National Semiconductor Incorporated.

FIGURE 2-3: EWEN TIMING

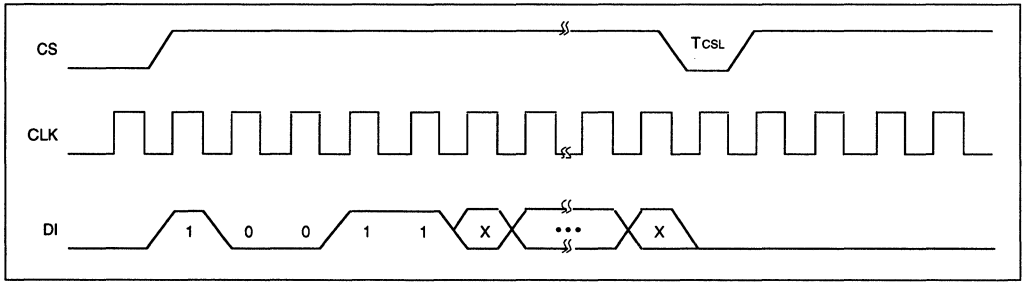


FIGURE 2-4: EWDS TIMING

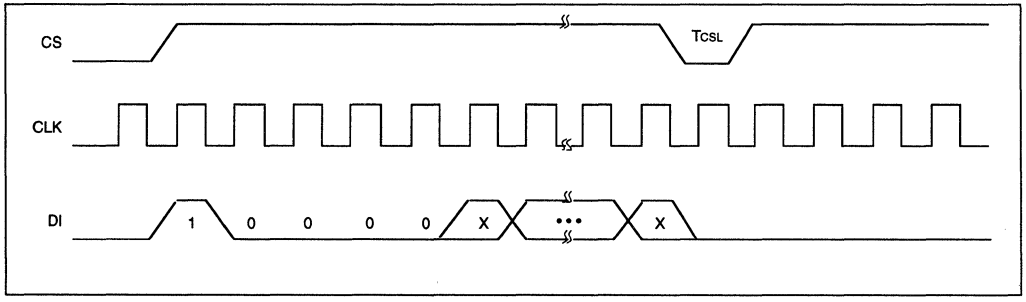


FIGURE 2-5: WRITE TIMING

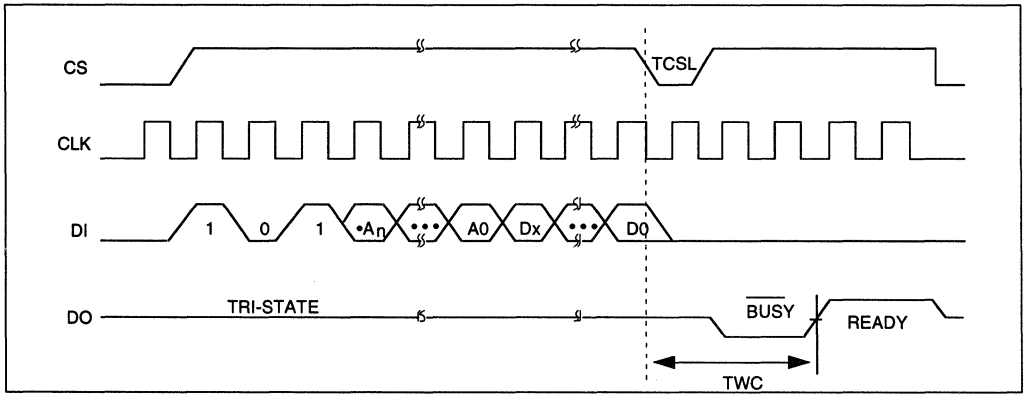
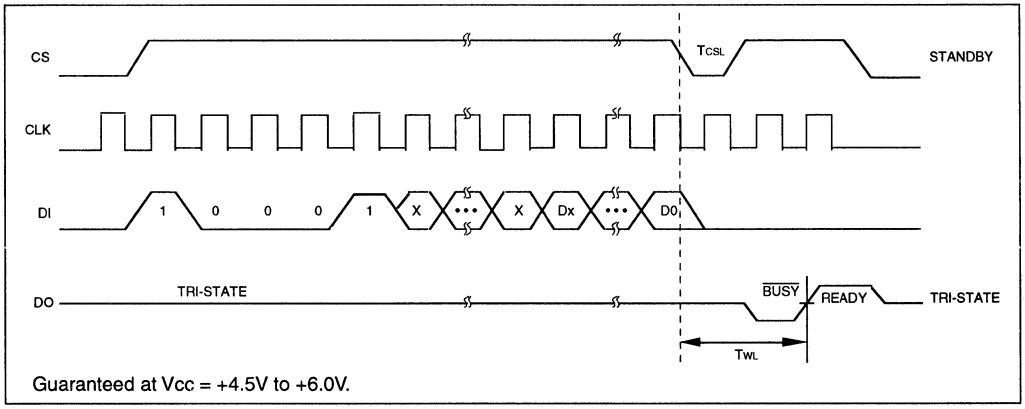


FIGURE 2-6: WRAL TIMING



Guaranteed at Vcc = +4.5V to +6.0V.

FIGURE 2-7: ERASE TIMING

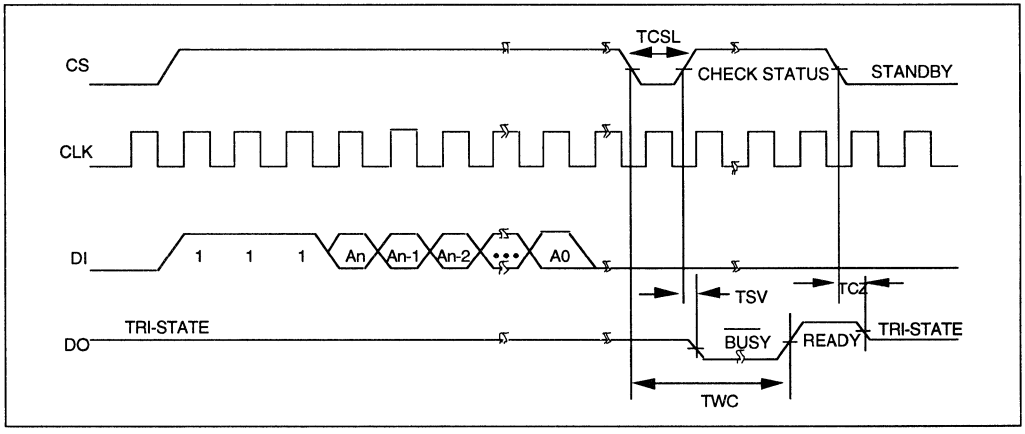
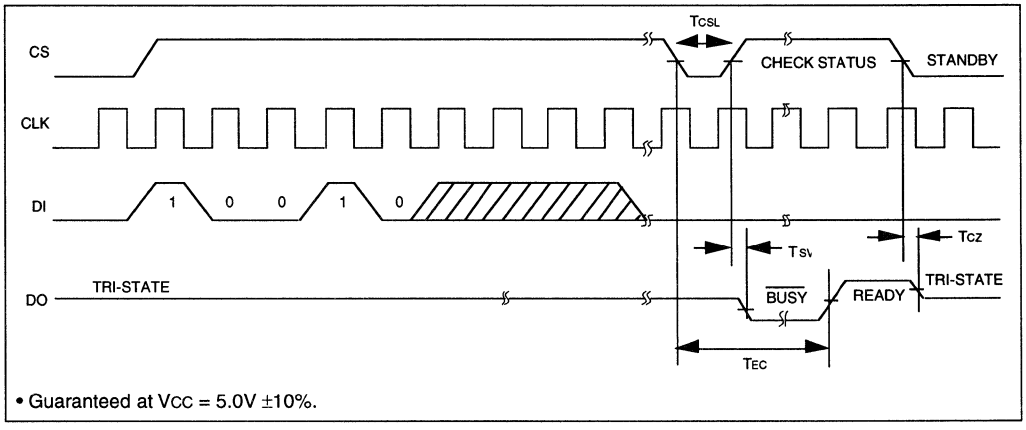


FIGURE 2-8: ERAL TIMING



• Guaranteed at VCC = 5.0V ±10%.

3.0 PIN DESCRIPTION

3.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93AAXX. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note:	CS must go LOW between consecutive instructions.

3.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

3.5 Organization (ORG)

When ORG is connected to VCC, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1MHz or less for the (x16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to VCC or VSS.

NOTES:

93AA46/56/66 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93AA46/56/66 - /P

Package:

P	=	Plastic DIP (300 mil Body), 8-lead
SN	=	Plastic SOIC (150 mil Body), 8-lead
SM	=	Plastic SOIC (207 mil Body), 8-lead (93AA46/56/66)

Temperature Range:

Blank	=	0°C to +70°C

Devic

93AA46/56/66	Microwire Serial EEPROM
93AA46/56/66X	Microwire Serial EEPROM in alternate pinouts (SN package only)
93AA46T/56T/66T	Microwire Serial EEPROM (Tape and Reel)
93AA46XT/56XT/66XT	Microwire Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

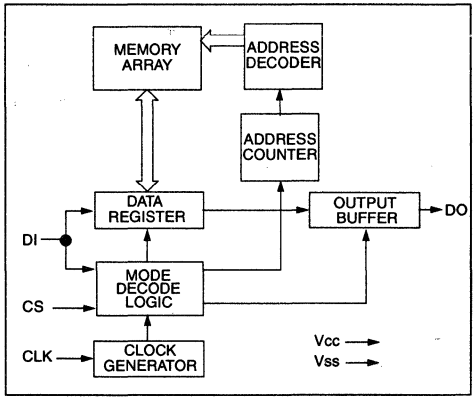
93LC46A/B

1K 2.5V Microwire® Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1 µA standby current (maximum)
- 128 x 8 bit organization (93LC46A)
- 64 x 16 bit organization (93LC46B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC and 8-pin TSSOP packages
- Available for the following temperature ranges:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

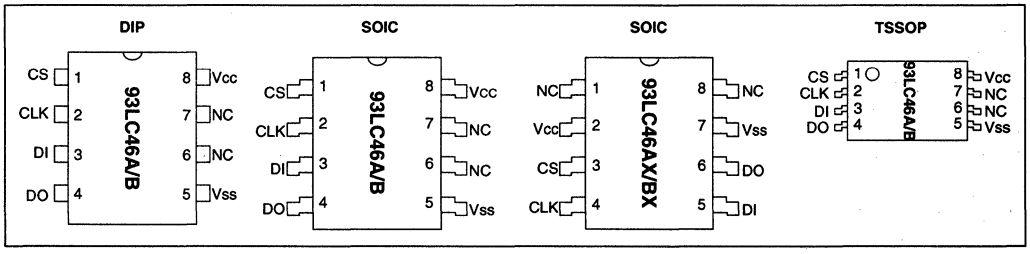
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93LC46AX/BX are 1K-bit, low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 (93LC46A) or x16 bits (93LC46B). Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. The 93LC46AX/BX is available in standard 8-pin DIP, 8-pin surface mount SOIC, and TSSOP packages. The 93LC46AX/BX are offered only in a 150-mil SOIC package.

PACKAGE TYPE



Microwire is a registered trademark of National Semiconductor Incorporated.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No Connect
Vcc	Power Supply

TABLE 1-2 DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted	Commercial (C): Vcc = +2.5V to +6.0V Tamb = 0°C to +70°C Industrial (I): Vcc = +2.5V to +6.0V Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	Vcc +1	V	2.7V < Vcc ≤ 6.0V (Note 2)
	VIH2	0.7 Vcc	Vcc +1	V	Vcc < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	Vcc > 2.7V (Note 2)
	VIL2	-0.3	0.2 Vcc	V	Vcc < 2.7V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc = Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = Vss to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0 V (Notes 1 & 2) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	1.5	mA	
	ICC read	—	1 500	mA µA	FCLK = 2 MHz; Vcc = 6.0V FCLK = 1 MHz; Vcc = 3.0V
Standby current	ICCS	—	1	µA	CS = Vss; DI = Vss
Clock frequency	FCLK	—	2 1	MHz MHz	Vcc > 4.5V Vcc < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 2)
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	6	ms	ERASE/WRITE mode
	TEC	—	6	ms	ERAL mode
	TWL	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at Tamb = 25°C and Fclk = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LC46AX/BX. Opcodes, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but the START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

2.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1 INSTRUCTION SET FOR 93LC46A

Instruction	SB	Opcode	Address							Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	10
ERAL	1	00	1	0	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	10
EWDS	1	00	0	0	X	X	X	X	X	—	HIGH-Z	10
EWEN	1	00	1	1	X	X	X	X	X	—	HIGH-Z	10
READ	1	10	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	18
WRITE	1	01	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18
WRAL	1	00	0	1	X	X	X	X	X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18

TABLE 2-2 INSTRUCTION SET FOR 93LC46B

Instruction	SB	Opcode	Address						Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	9
ERAL	1	00	1	0	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	9
EWDS	1	00	0	0	X	X	X	X	—	HIGH-Z	9
EWEN	1	00	1	1	X	X	X	X	—	HIGH-Z	9
READ	1	10	A5	A4	A3	A2	A1	A0	—	D15 - D0	25
WRITE	1	01	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
WRAL	1	00	0	1	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcodes, addresses, and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data In (DI) and Data Out (DO)

It is possible to connect the Data In (DI) and Data Out (DO) pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

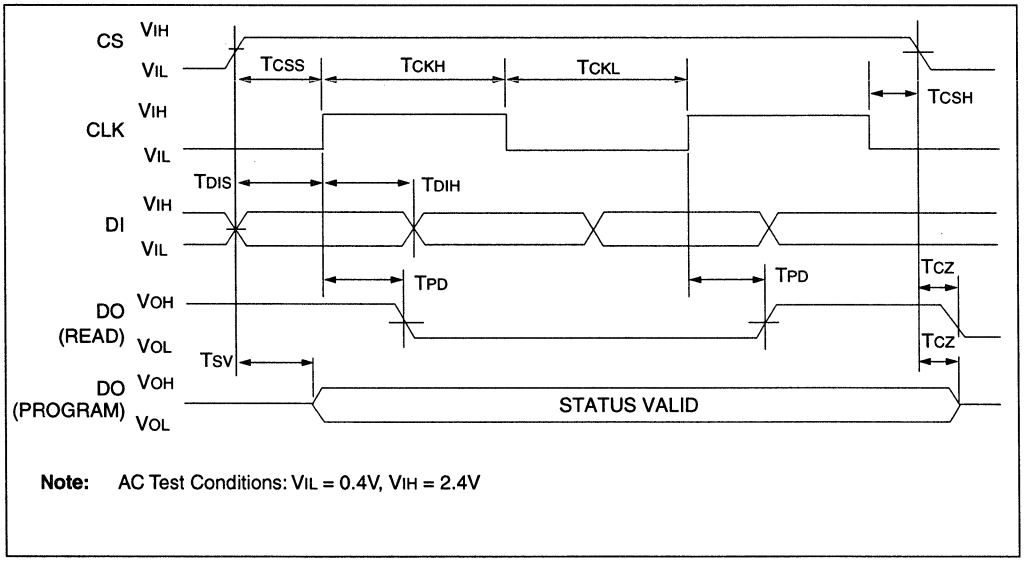
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 2.2V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 2.2V at nominal conditions.

The ERASE/WRITE Disable (EWDS) and ERASE/WRITE Enable (EWDS) commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



Note: AC Test Conditions: VIL = 0.4V, VIH = 2.4V

3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

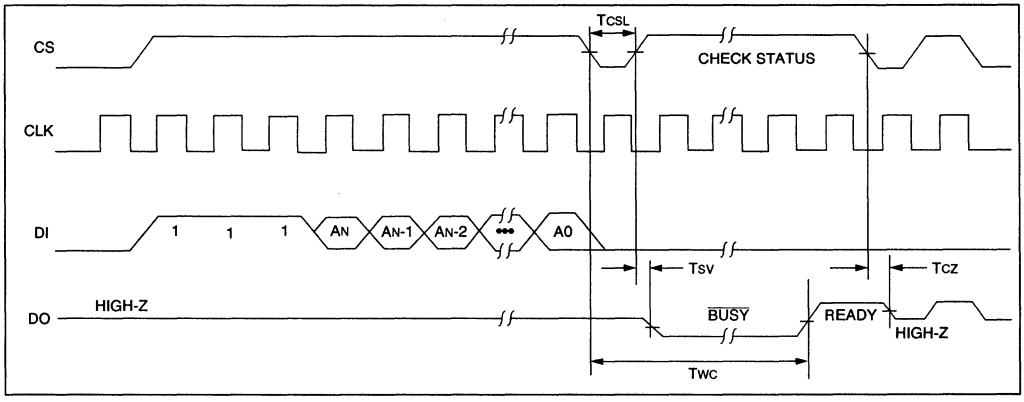
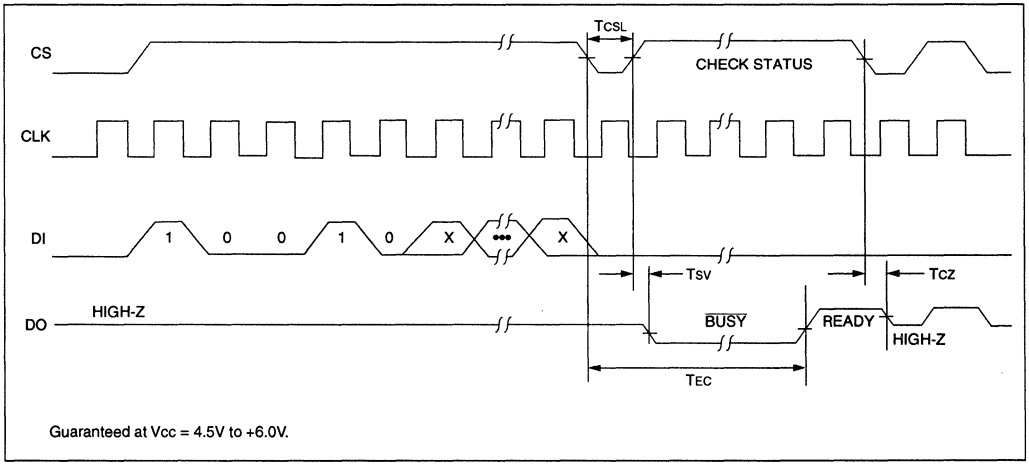


FIGURE 3-3: ERAL TIMING



Guaranteed at Vcc = 4.5V to +6.0V.

3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The 93LC46A/B powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93LC46A) or 16-bit (93LC46B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

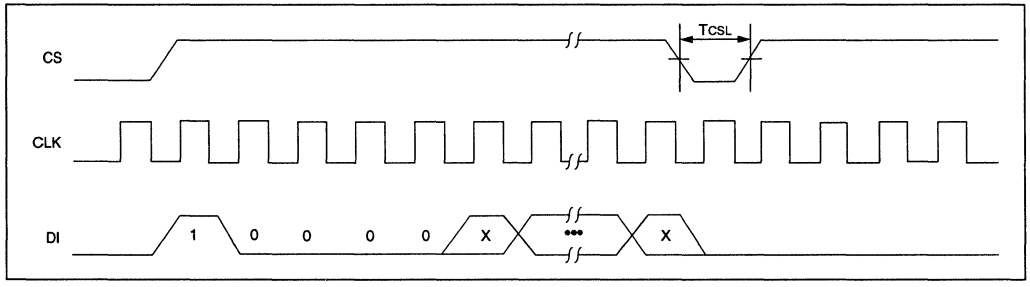


FIGURE 3-5: EWEN TIMING

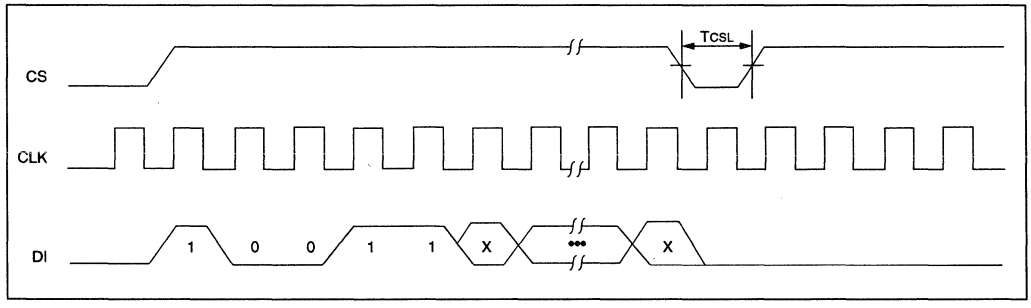
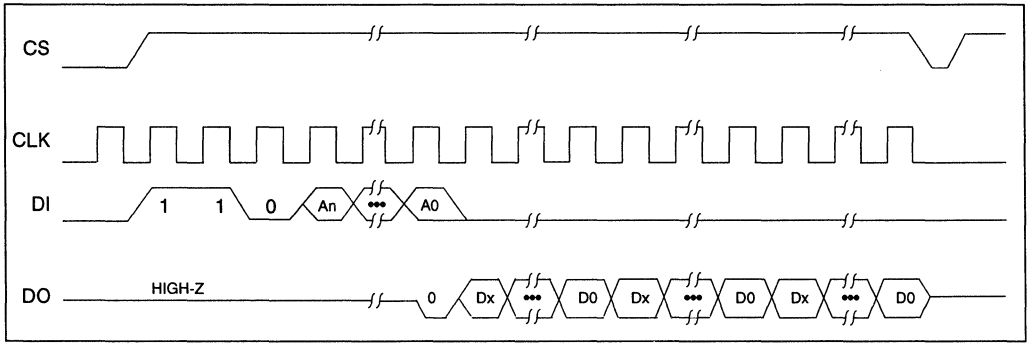


FIGURE 3-6: READ TIMING



3.8 WRITE

The WRITE instruction is followed by 8 bits (93LC46A) or 16 bits (93LC46B) of data which are written into the specified address. After the last data bit is put on the DI pin, the falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 3-7: WRITE TIMING

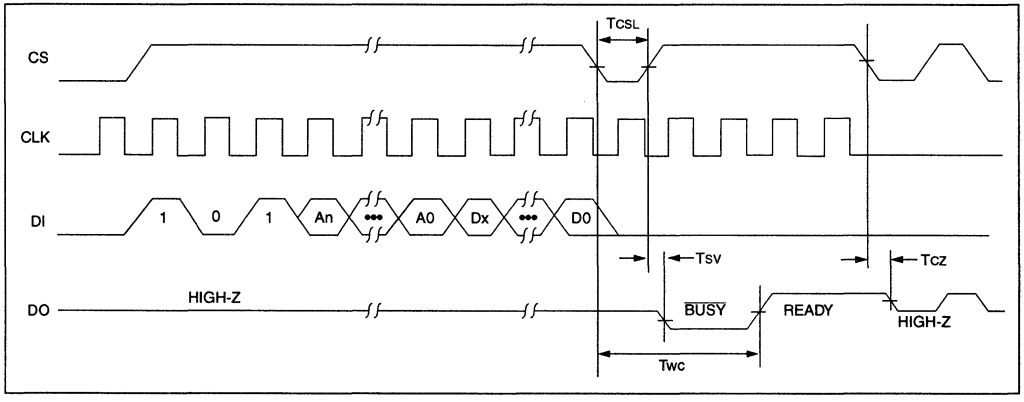
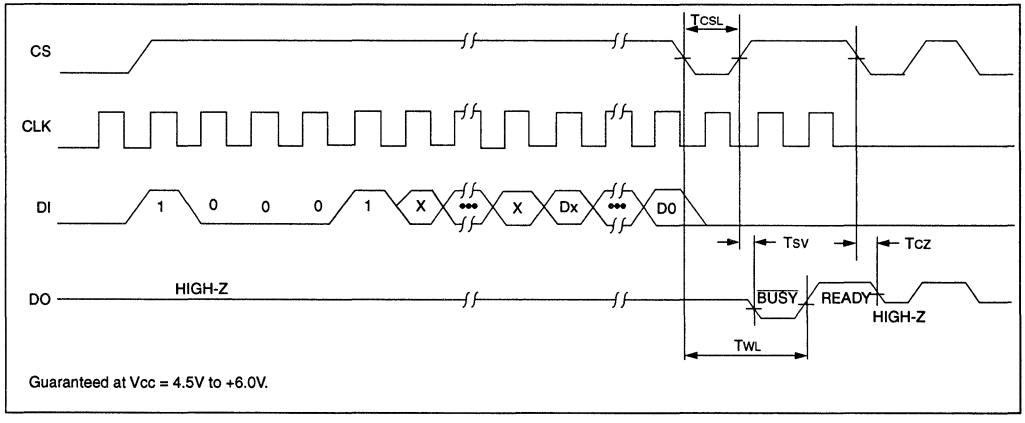
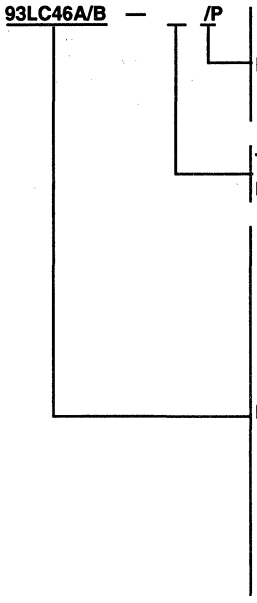


FIGURE 3-8: WRAL TIMING



93LC46A/B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	P	= Plastic DIP (300 mil Body), 8-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	SM	= Plastic SOIC (208 mil Body), 8-lead
	ST	= TSSOP, 8-lead
Temperature Range:	Blank	= 0°C to +70°C
	I	= -40°C to +85°C
Device:	93LC46A	1K Microwire Serial EEPROM (x8)
	93LC46AT	1K Microwire Serial EEPROM (x8) Tape and Reel
	93LC46AX	1K Microwire Serial EEPROM (x8) in alternate pinout (SN only)
	93LC46AXT	1K Microwire Serial EEPROM (x8) in alternate pinout, Tape and Reel (SN only)
	93LC46B	1K Microwire Serial EEPROM (x16)
	93LC46BT	1K Microwire Serial EEPROM (x16) Tape and Reel
	93LC46BX	1K Microwire Serial EEPROM (x16) in alternate pinout (SN only)
	93LC46BXT	1K Microwire Serial EEPROM (x16) in alternate pinout, Tape and Reel (SN only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

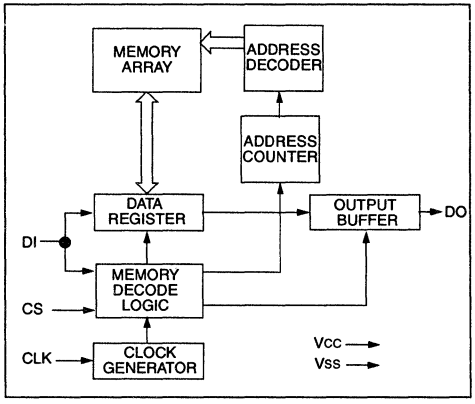
93C46B

1K 5.0V Microwire® Serial EEPROM

FEATURES

- Single supply 5.0V operation
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1 µA standby current (maximum)
- 64 x 16 bit organization
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC and 8-pin TSSOP packages
- Available for the following temperature ranges:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

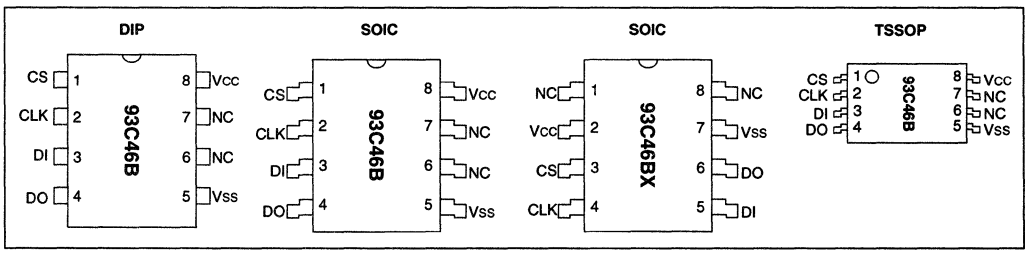
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93C46B is a 1K-bit, low-voltage serial Electrically Erasable PROM. The device memory is configured as 64 x 16 bits. Advanced CMOS technology makes this device ideal for low-power, nonvolatile memory applications. The 93C46B is available in standard 8-pin DIP, surface mount SOIC, and TSSOP packages. The 93C46BX are only offered in a 150 mil SOIC package.

PACKAGE TYPE



Microwire is a registered trademark of National Semiconductor Incorporated.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds).....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No Connect
Vcc	Power Supply

TABLE 1-2 DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted	Commercial (C) Vcc = +4.5V to +5.5V Tamb = 0°C to +70°C Industrial (I) Vcc = +4.5V to +5.5V Tamb = -40°C to +85°C Automotive (E) Vcc = +4.5V to +5.5V Tamb = -40°C to +125°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH	2.0	Vcc +1	V	(Note 2)
Low level input voltage	VIL	-0.3	0.8	V	
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
High level output voltage	VOH	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
Input leakage current	ILI	-10	10	µA	VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = Vss to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0 V (Notes 1 & 2) Tamb = +25°C, FCLK = 1 MHz
	Icc read	—	1	mA	
Operating current	Icc write	—	1.5	mA	
Standby current	Iccs	—	1	µA	CS = Vss; DI = Vss
Clock frequency	FCLK	—	2	MHz	Vcc = 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 2)
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	2	ms	ERASE/WRITE mode
	TEC	—	6	ms	ERAL mode
	TWL	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock (CLK) is used to synchronize the communication between a master device and the 93C46B. Opcodes, addresses, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing the opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but START condition has not been detected, any number of clock cycles can be received by the device, without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detecting a START condition, the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcodes, addresses, and data bits before an instruction is executed (Table 2-1). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

Note: CS must go low between consecutive instructions.

2.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1 INSTRUCTION SET FOR 93C46B

Instruction	SB	Opcode	Address						Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	9
ERAL	1	00	1	0	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	9
EWDS	1	00	0	0	X	X	X	X	—	HIGH-Z	9
EWEN	1	00	1	1	X	X	X	X	—	HIGH-Z	9
READ	1	10	A5	A4	A3	A2	A1	A0	—	D15 - D0	25
WRITE	1	01	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
WRAL	1	00	0	1	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcodes, addresses, and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data In (DI) and Data Out (DO)

It is possible to connect the Data In (DI)and Data Out (DO) pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition, the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

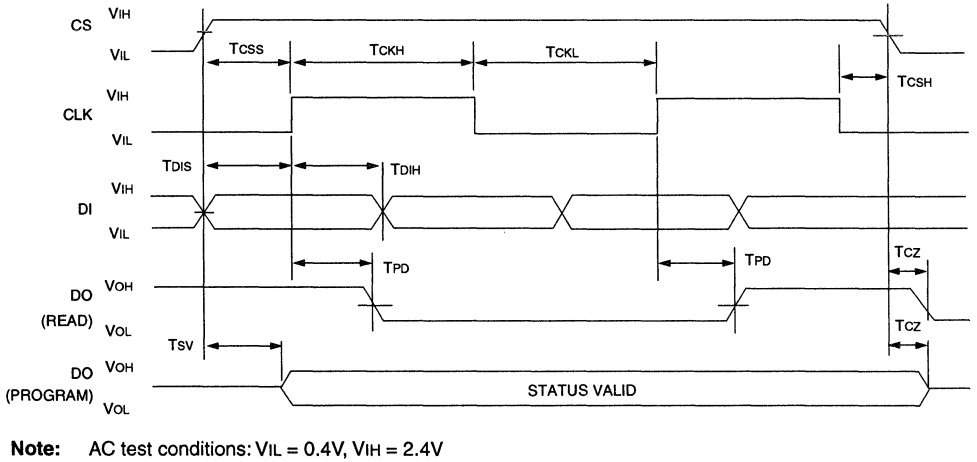
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 3.8V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 3.8V at nominal conditions.

The ERASE/SRITE Disable (EWDS) and ERASE/WRITE Enable (EWEN) commands give additional protection against accidental programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



Note: AC test conditions: V_{IL} = 0.4V, V_{IH} = 2.4V

3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. This cycle begins on the rising clock edge of the last address bit.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the rising clock edge of the last address bit. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

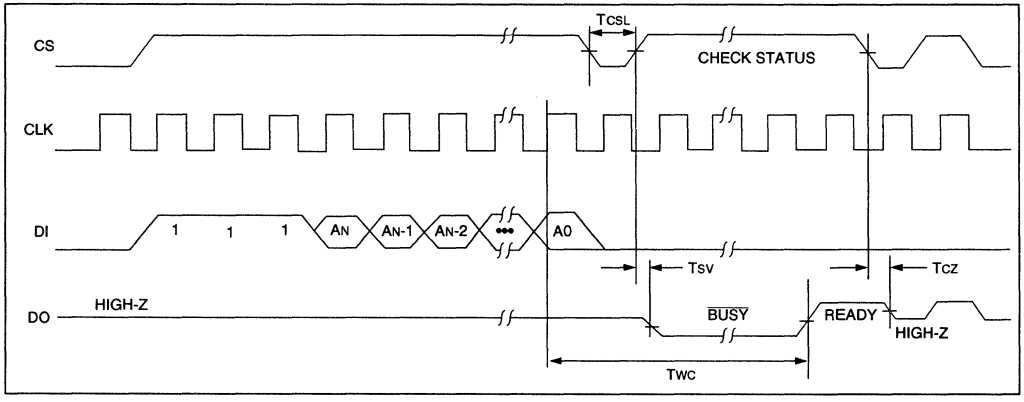
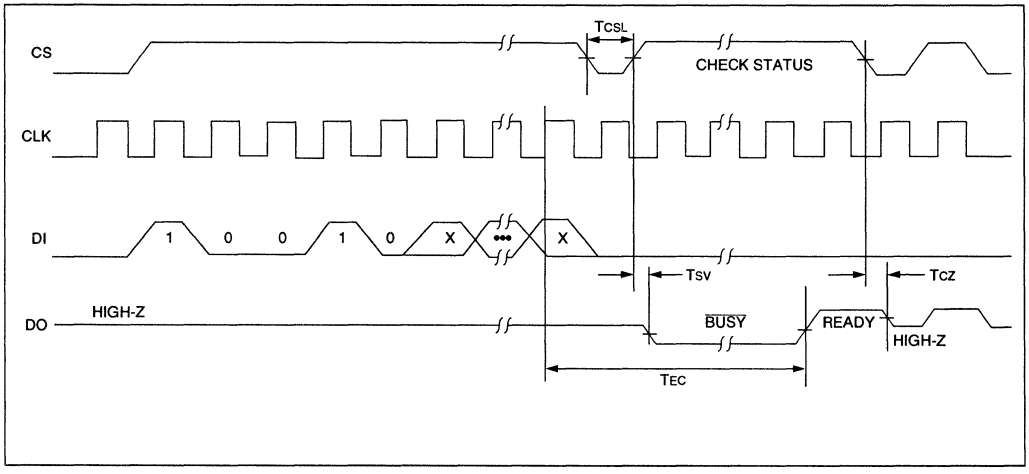


FIGURE 3-3: ERAL TIMING



3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The device powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWDS and EWEN instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16-bit output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

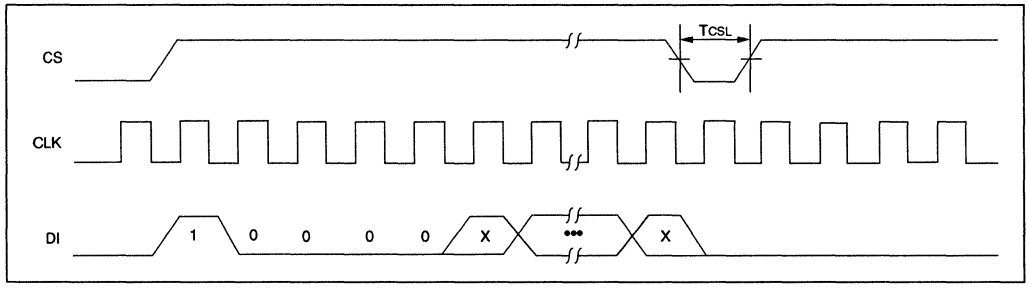


FIGURE 3-5: EWEN TIMING

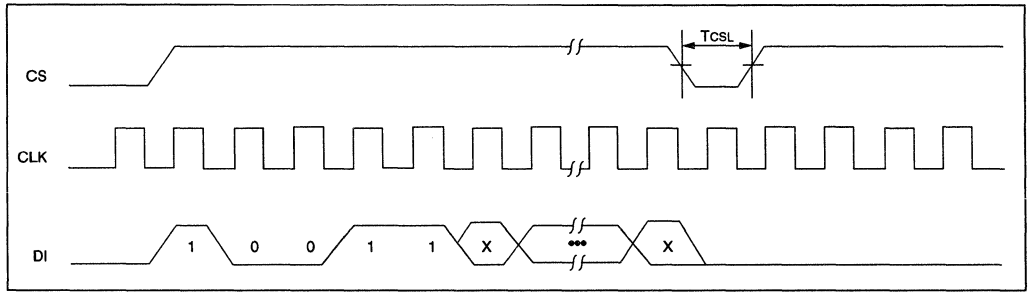
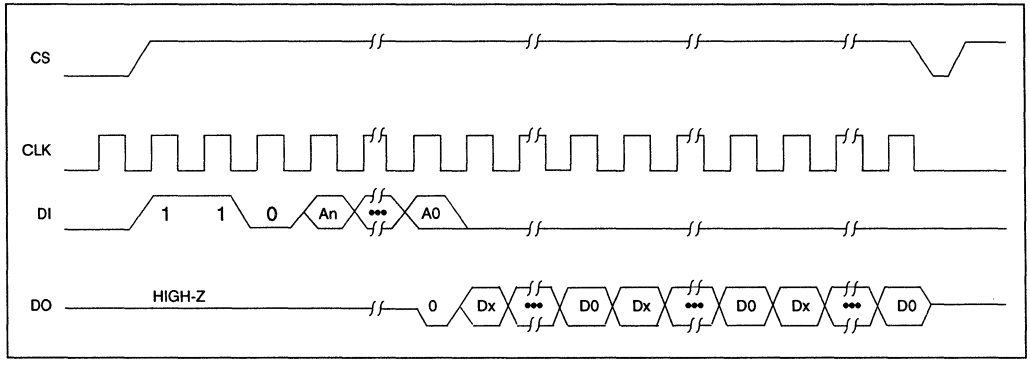


FIGURE 3-6: READ TIMING



3.8 WRITE

The WRITE instruction is followed by 16 bits of data, which are written into the specified address. After the last data bit is clocked into the DI pin, the self-timed auto-erase and programming cycle begins.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the rising clock edge of the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 3-7: WRITE TIMING

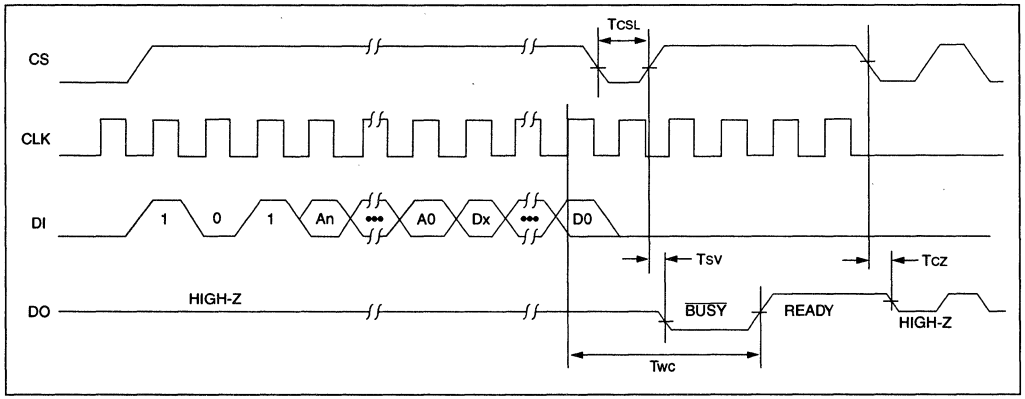
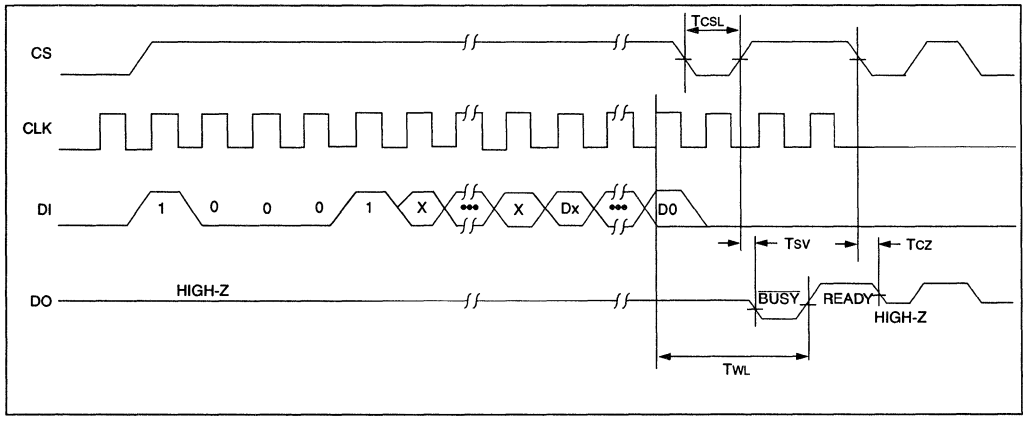
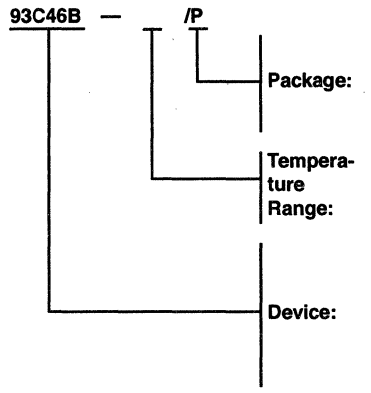


FIGURE 3-8: WRAL TIMIN



93C46B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	P	= Plastic DIP (300 mil Body), 8-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	SM	= Plastic SOIC (208 mil Body), 8-lead
	ST	= TSSOP, 8-lead
Temperature Range:	Blank	= 0°C to +70°C
	I	= -40°C to +85°C
	E	= -40°C to +125°C
Device:	93C46B	= 1K Microwire Serial EEPROM
	93C46BT	= 1K Microwire Serial EEPROM Tape and Reel
	93C46BX	= 1K Microwire Serial EEPROM in alternate pinout (SN only)
	93C46BXT	= 1K Microwire Serial EEPROM in alternate pinout, Tape and Reel (SN only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

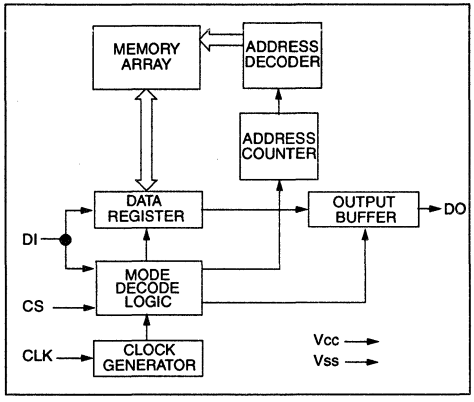
93LC56A/B

2K 2.5V Microwire® Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1 µA standby current (maximum)
- 256 x 8 bit organization (93LC56A)
- 128 x 16 bit organization (93LC56B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC and 8-pin TSSOP packages
- Available for the following temperature ranges:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

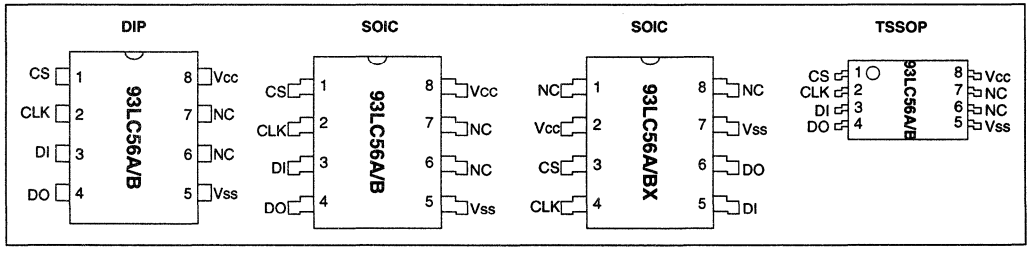
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93LC56A/B are 2K-bit, low-voltage serial Electrically Erasable PROMs. The device memory is configured as x8 (93LC56A) or x16 bits (93LC56B). Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. The 93LC56A/B is available in standard 8-pin DIP, surface mount SOIC, and TSSOP packages. The 93LC56AX/BX are only offered in a 150-mil SOIC package.

PACKAGE TYPE



Microwire is a registered trademark of National Semiconductor.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
NC	No Connect
VCC	Power Supply

TABLE 1-2 DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted	Commercial (C): VCC = +2.5V to +6.0V Tamb = 0°C to +70°C Industrial (I): VCC = +2.5V to +6.0V Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	VCC +1	V	2.7V ≤ VCC ≤ 6.0V (Note 2)
	VIH2	0.7 VCC	VCC +1	V	VCC < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	VCC > 2.7V (Note 2)
	VIL2	-0.3	0.2 VCC	V	VCC < 2.7V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; VCC = VCC Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; VCC = 4.5V
	VOH2	VCC-0.2	—	V	IOH = -100 µA; VCC = VCC Min.
Input leakage current	ILI	-10	10	µA	VIN = VSS
Output leakage current	ILO	-10	10	µA	VOUT = VSS
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0 V (Notes 1 & 2) Tamb = +25°C, Fclk = 1 MHz
Operating current	ICC read	—	1 500	mA µA	FCLK = 2 MHz; VCC = 6.0V FCLK = 1 MHz; VCC = 3.0V
	ICC write	—	1.5	mA	
Standby current	ICCS	—	1	µA	CS = VSS; DI = VSS
Clock frequency	FCLK	—	2 1	MHz MHz	VCC > 4.5V VCC < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CI = 100 pF
Data output disable time	TCZ	—	100	ns	CI = 100 pF (Note 2)
Status valid time	TSV	—	500	ns	CI = 100 pF
Program cycle time	TWC	—	6	ms	ERASE/WRITE mode
	TEC	—	6	ms	ERAL mode
	TWL	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LC56A/B. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

2.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1 INSTRUCTION SET FOR 93LC56A

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1	0	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	12
EWDS	1	00	0	0	X	X	X	X	X	X	X	—	HIGH-Z	12
EWEN	1	00	1	1	X	X	X	X	X	X	X	—	HIGH-Z	12
READ	1	10	X	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	20
WRITE	1	01	X	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0	1	X	X	X	X	X	X	X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20

TABLE 2-2 INSTRUCTION SET FOR 93LC56B

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	HIGH-Z	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	HIGH-Z	11
READ	1	10	X	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	27
WRITE	1	01	X	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 DATA IN (DI) AND DATA OUT (DO)

It is possible to connect the Data In (DI) and Data Out (DO) pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition, the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

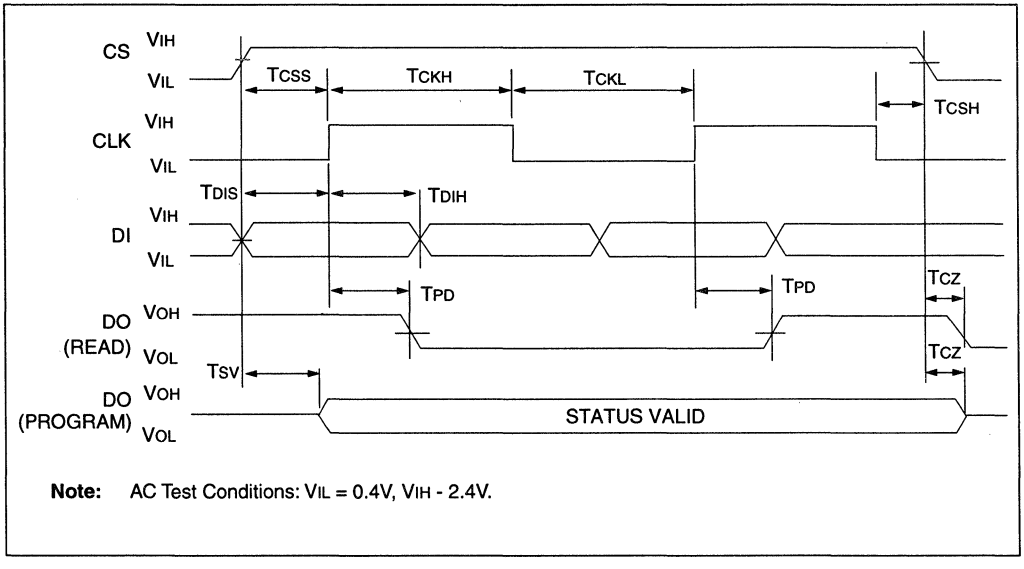
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 2.2V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 2.2V at nominal conditions.

The EWDS and EWEN commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



Note: AC Test Conditions: V_{IL} = 0.4V, V_{IH} - 2.4V.

3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

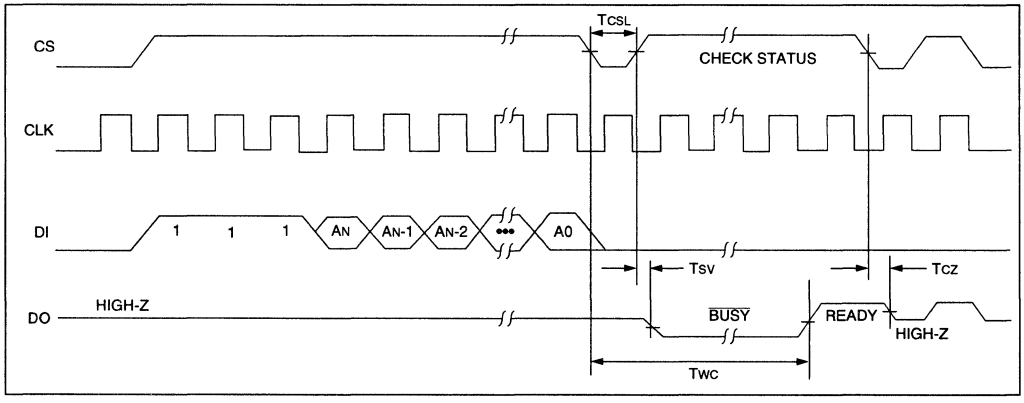
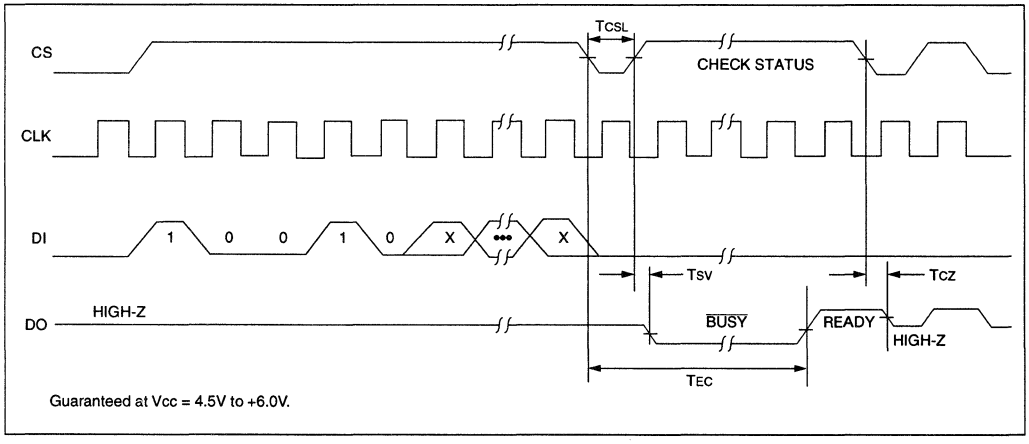


FIGURE 3-3: ERAL TIMING



3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The 93LC56A/B powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWDS and EWEN instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93LC56A) or 16-bit (93LC56B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

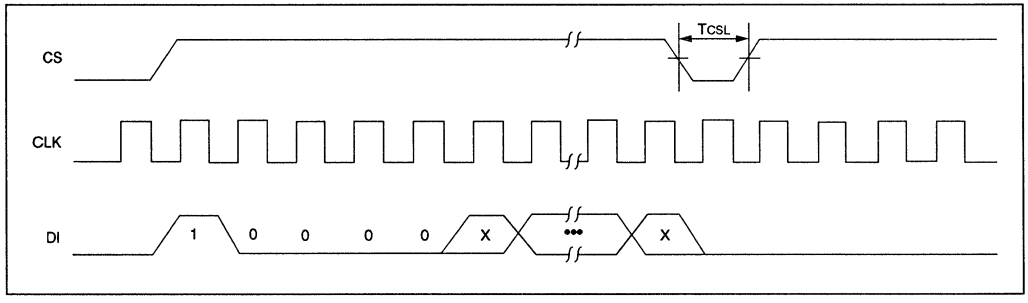


FIGURE 3-5: EWEN TIMING

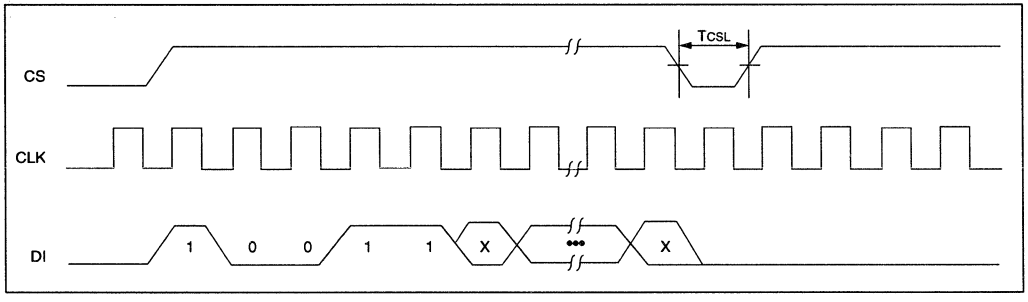
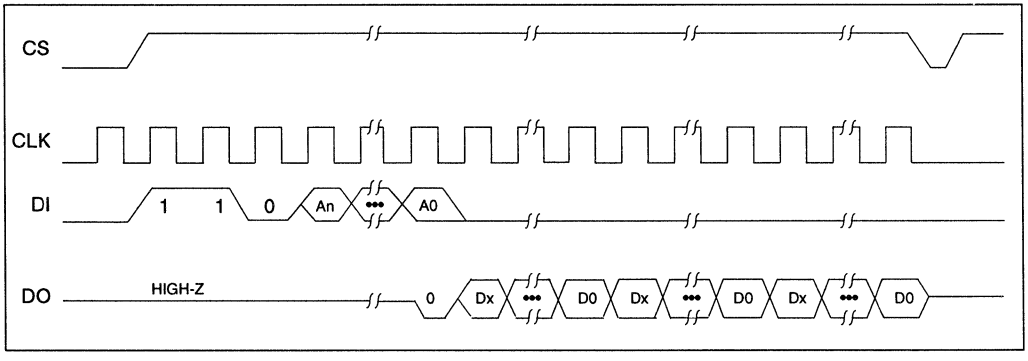


FIGURE 3-6: READ TIMING



3.8 WRITE

The WRITE instruction is followed by 8 bits (93LC56A) or 16 bits (93LC56B) of data which are written into the specified address. After the last data bit is put on the DI pin, the falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 3-7: WRITE TIMING

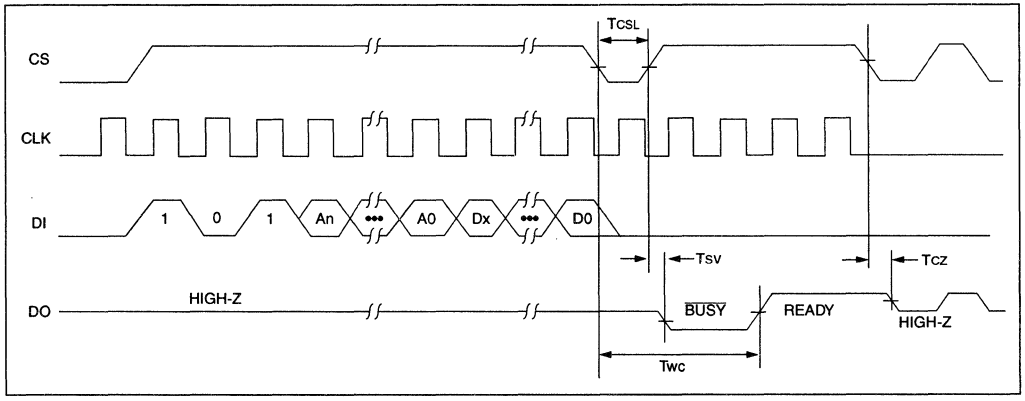
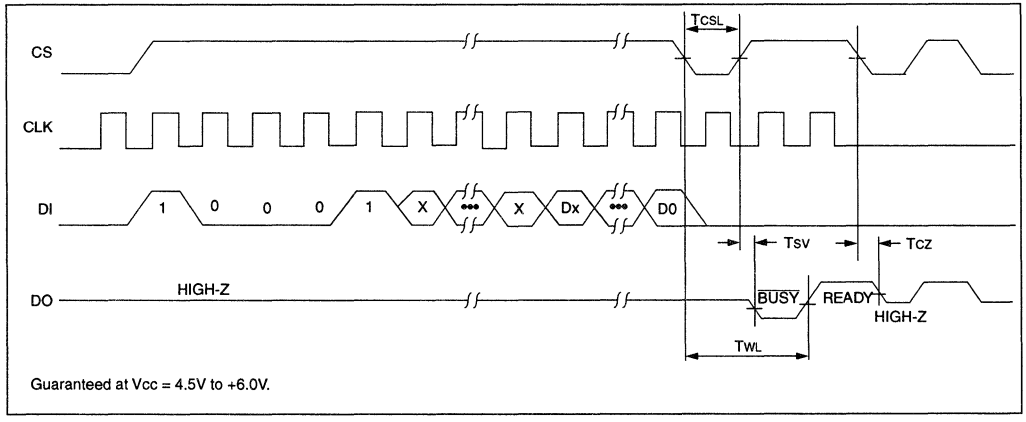
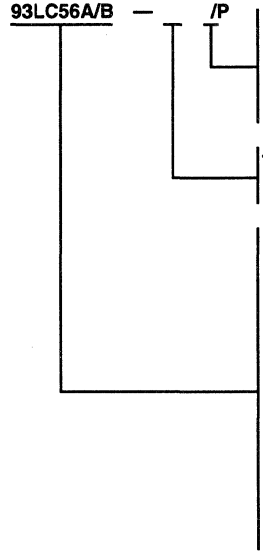


FIGURE 3-8: WRAL TIMING



93LC56A/B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	
P	Plastic DIP (300 mil Body), 8-lead
SN	Plastic SOIC (150 mil Body), 8-lead
SM	Plastic SOIC (208 mil Body), 8-lead
ST	TSSOP, 8-lead
Temperature Range:	
Blank	0°C to +70°C
I	-40°C to +85°C
Device:	
93LC56A	2K Microwire Serial EEPROM (x8)
93LC56AT	2K Microwire Serial EEPROM (x8) Tape and Reel
93LC56AX	2K Microwire Serial EEPROM (x8) in alternate pinout (SN only)
93LC56AXT	2K Microwire Serial EEPROM (x8) in alternate pinout, Tape and Reel (SN only)
93LC56B	2K Microwire Serial EEPROM (x16)
93LC56BT	2K Microwire Serial EEPROM (x16) Tape and Reel
93LC56BX	2K Microwire Serial EEPROM (x16) in alternate pinout (SN only)
93LC56BXT	2K Microwire Serial EEPROM (x16) in alternate pinout, Tape and Reel (SN only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

93C56A/B

2K 5.0V Automotive Temperature Microwire® Serial EEPROM

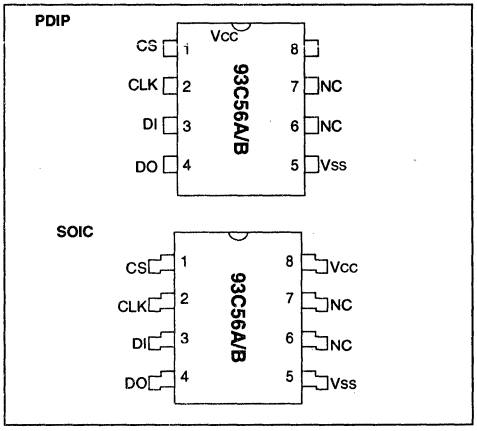
FEATURES

- Single supply 5.0V operation
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1 µA standby current (maximum)
- 256 x 8 bit organization (93C56A)
- 128 x 16 bit organization (93C56B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Available for the following temperature ranges:
  - Automotive (E): -40°C to +125°C

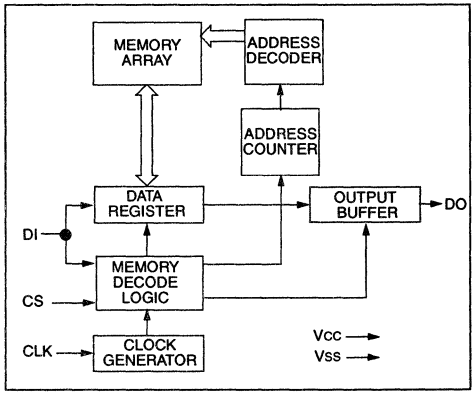
DESCRIPTION

The Microchip Technology Inc. 93C56A/B is a 2K-bit, low-voltage serial Electrically Erasable PROM. The device memory is configured as 256 x 8 bits (93C56A) or 128 x 16 bits (93C56B). Advanced CMOS technology makes this device ideal for low-power, nonvolatile memory applications. The 93C56A/B is available in standard 8-pin DIP and surface mount SOIC packages. **This device is only recommeded for 5V automotive temperature applications. For all commercial and industrial applications, the 93LC56A/B is recommended.**

PACKAGE TYPE



BLOCK DIAGRAM



4

Microwire®

Microwire is a registered trademark of National Semiconductor.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No Connect
Vcc	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted	Automotive (E)Vcc = +4.5V to +5.5VTamb = -40°C to +125°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH	2.0	Vcc +1	V	(Note 2)
Low level input voltage	VIL	-0.3	0.8	V	
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
High level output voltage	VOH	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
Input leakage current	ILI	-10	10	µA	VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = Vss to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0 V (Notes 1 & 2) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	1.5	mA	
	ICC read	—	1	mA	
Standby current	ICCS	—	1	µA	CS = Vss; DI = Vss
Clock frequency	FCLK	—	2	MHz	
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 2)
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	2	ms	ERASE/WRITE mode
	TEC	—	6	ms	ERAL mode
	TWL	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device. A low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the CS input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C56A/B. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but the START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detecting a START condition, the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

Note: CS must go low between consecutive instructions.

2.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated. The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1: INSTRUCTION SET FOR 93C56A

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1	0	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	12
EWDS	1	00	0	0	X	X	X	X	X	X	X	—	HIGH-Z	12
EWEN	1	00	1	1	X	X	X	X	X	X	X	—	HIGH-Z	12
READ	1	10	X	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	20
WRITE	1	01	X	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0	1	X	X	X	X	X	X	X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20

TABLE 2-2: INSTRUCTION SET FOR 93C56B

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	X	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	HIGH-Z	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	HIGH-Z	11
READ	1	10	X	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	27
WRITE	1	01	X	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data IN (DI) and Data Out (DO)

It is possible to connect the Data In (DI) and Data Out (DO) pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition, the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

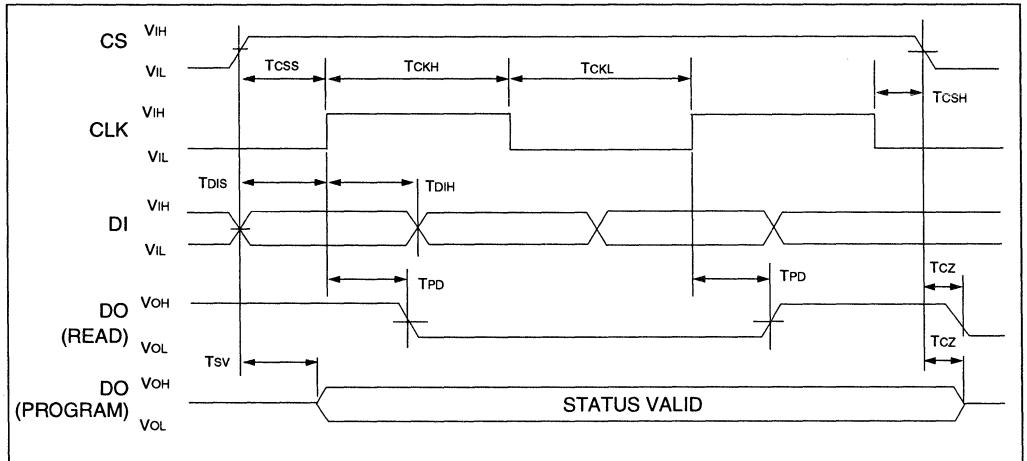
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 3.8V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 3.8V at nominal conditions.

The ERASE/WRITE Disable (EWDS) and ERASE WRTE Enable (EWEN) commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



Note: AC Test Conditions: V_{IL} = 0.4V, V_{IH} = 2.4V.

3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. This cycle begins on the rising clock edge of the last address bit.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the rising clock edge of the last address bit. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

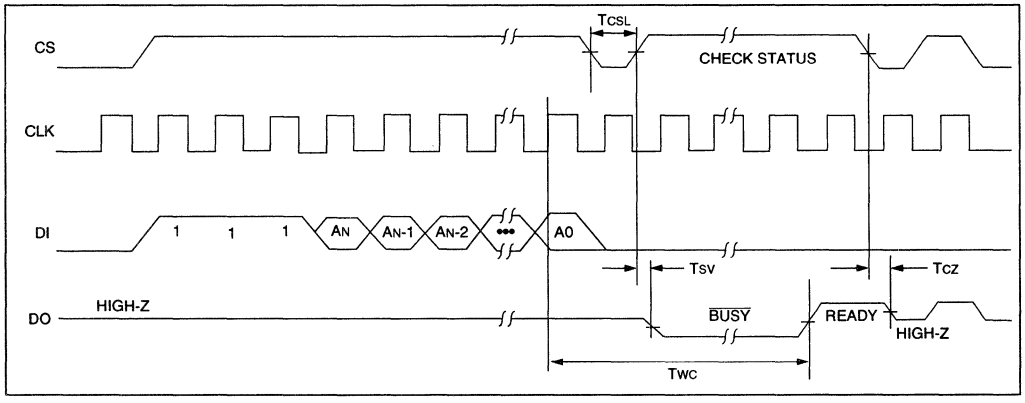
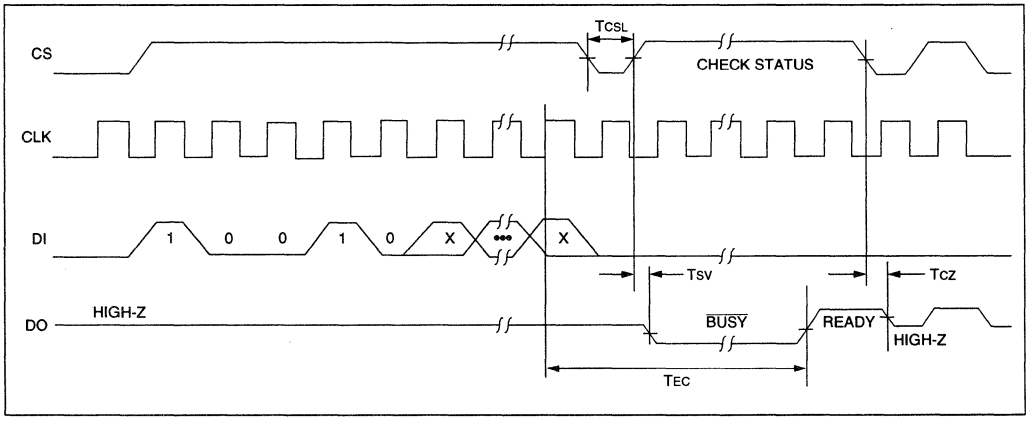


FIGURE 3-3: ERAL TIMING



3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The device powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93C56A) or 16-bit (93C56B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: READ TIMING

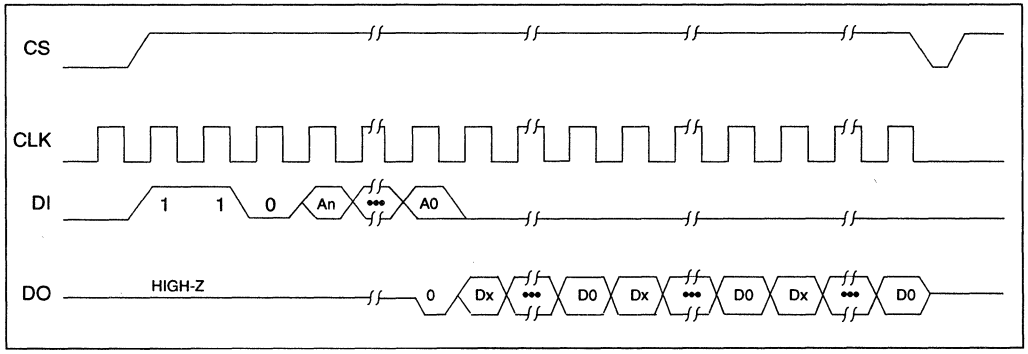


FIGURE 3-5: EWDS TIMING

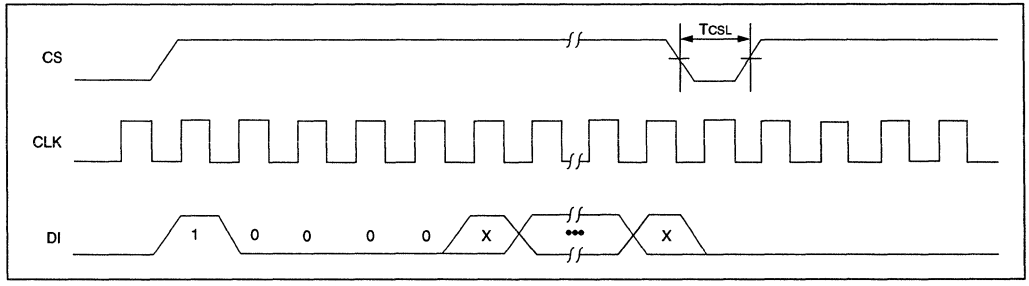
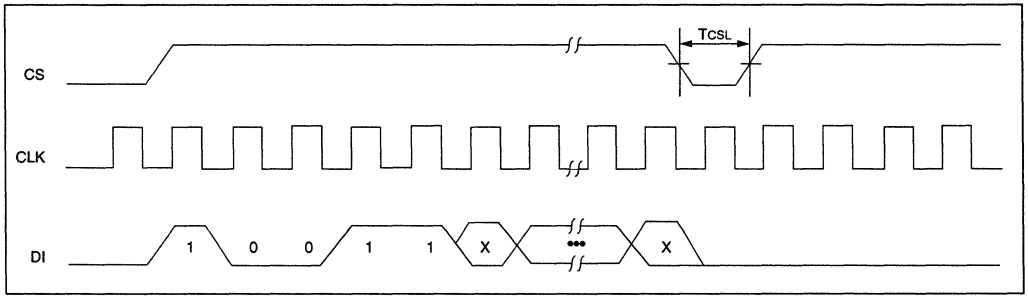


FIGURE 3-6: EWEN TIMING



3.8 WRITE

The WRITE instruction is followed by 8-bits (93C56A) 16-bits (93C56B) of data which are written into the specified address. After the last data bit is clocked into the DI pin, the self-timed auto-erase and programming cycle begins.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the rising clock edge of the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 3-7: WRITE TIMING

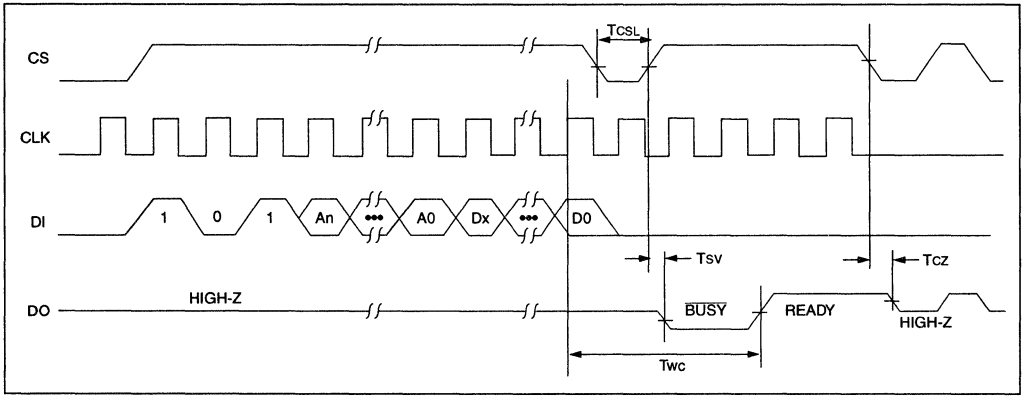
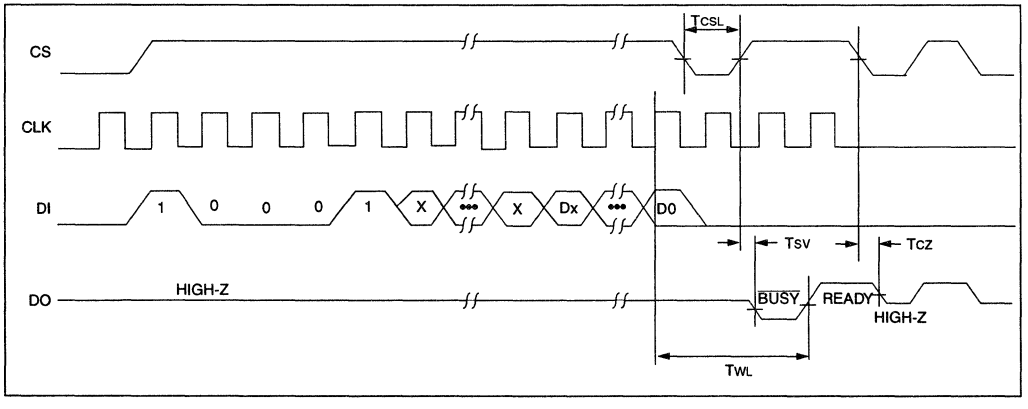
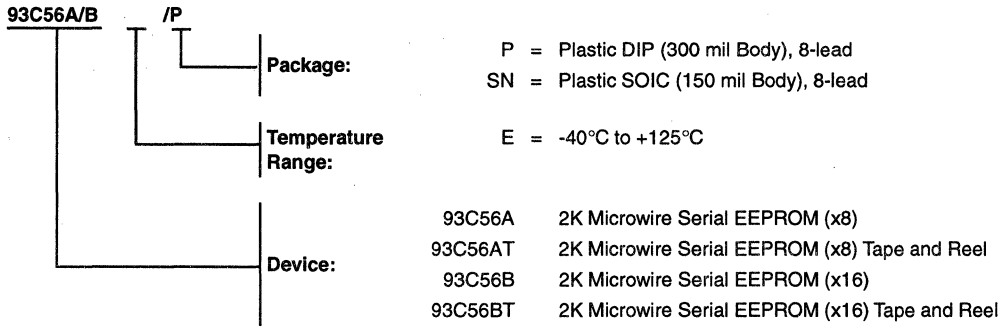


FIGURE 3-8: WRAL TIMING



93C56A/B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

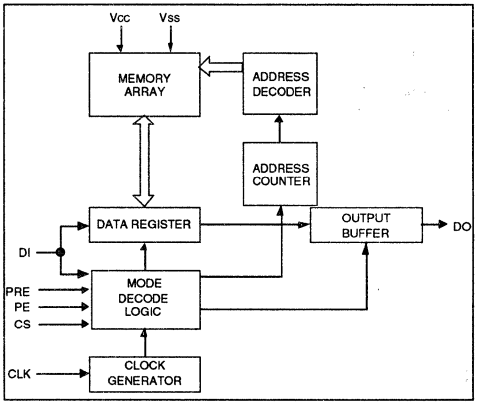
93LCS56/66

2K/4K 2.5V Microwire® Serial EEPROM with Software Write Protect

FEATURES

- Single supply with programming operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0V
- x16 memory organization
  - 128x16 (93LCS56)
  - 256x16 (93LCS66)
- Software write protection of user defined memory space
- Self timed erase and write cycles
- Automatic ERAL before WRAL
- Power on/off data protection
- Industry standard 3-wire serial I/O
- Device status signal during E/W
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC and 14-pin SOIC packages
- Temperature ranges supported
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

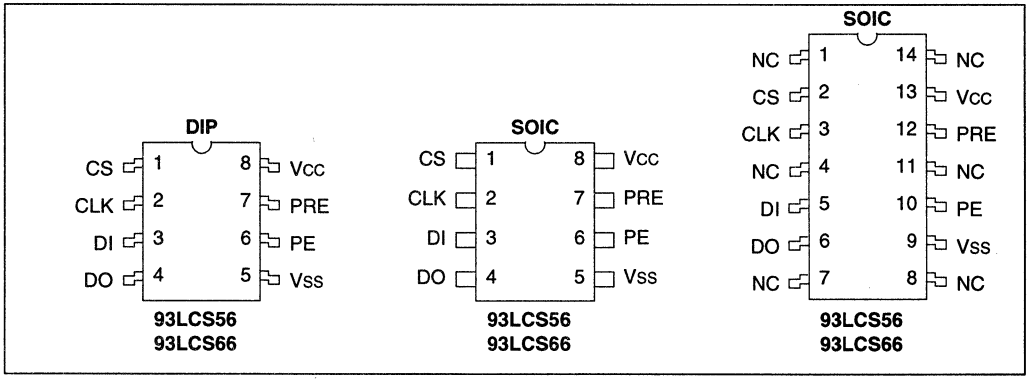
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93LCS56/66 are low voltage Serial Electrically Erasable PROMs with memory capacities of 2K bits/4K bits respectively. A write protect register is included in order to provide a user defined region of write protected memory. All memory locations greater than or equal to the address placed in the write protect register will be protected from any attempted write or erase operation. It is also possible to protect the address in the write protect register permanently by using a one time only instruction (PRDS). Any attempt to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications.

PACKAGE TYPES



Microwire is a registered trademark of National Semiconductor Incorporated.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

	Vcc = +2.5V to +6.0V Commercial(C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
High level input voltage	VIH	2.0	Vcc +1	V	Vcc ≥ 2.5V
Low level input voltage	VIL	-0.3	0.8	V	Vcc ≥ 2.5V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL = 100 µA; Vcc = 2.5V
High level output voltage	VOH1	2.4	—	V	IOH = -400µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100µA; Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0V (Note 1 & 2) Tamb = +25°C; FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	FCLK = 2 MHz; Vcc = 3.0V (Note 2)
	ICC Read	—	1 500	mA µA	FCLK = 2 MHz; Vcc = 6.0V FCLK = 1 MHz; Vcc = 3.0V
Standby current	ICCS	—	100 30	µA µA	CLK = CS = 0V; Vcc = 6.0V CLK = CS = 0V; Vcc = 3.0V DI = PE = PRE = Vss
Clock frequency	FCLK	—	2 1	MHz MHz	Vcc ≥ 4.5V Vcc < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
PRE setup time	TPRES	100	—	ns	Relative to CLK
PE setup time	TPES	100	—	ns	Relative to CLK
PRE hold time	TPREH	0	—	ns	Relative to CLK
PE hold time	TPEH	500	—	ns	Relative to CLK
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL=100 pF
Data output disable time	TCZ	—	100	ns	CL=100 pF (Note 2)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

	Vcc = +2.5V to +6.0V Commercial(C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Status valid time	Tsv		500	ns	CL=100 pF
Program cycle time	Twc		10	ms	ERASE/WRITE mode (Note 3)
	Tec		15	ms	ERAL mode
	Twl		30	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

3: Typical program cycle time is 4 ms per word.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

TABLE 1-3: INSTRUCTION SET FOR 93LCS56*/66

93LCS56/66 (x 16 organization)								
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**PRE**	**PE**	**Comments**
READ	1	10	A7 - A0	—	D15-D0	0	X	Reads data stored in memory, starting at specified address (.Note).
EWEN	1	00	11XXXXXX	—	High-Z	0	1	Erase/Write Enable must precede all programming modes.
ERASE	1	11	A7 - A0	—	(RDY/$\overline{BSY}$)		1	Erase data at specified address location if address is unprotected (Note).
ERAL	1	00	10XXXXXX	—	(RDY/$\overline{BSY}$)	0	1	Erase all registers to "FF". Valid only when Protect Register is cleared.
WRITE	1	01	A7 - A0*	D15 - D0	(RDY/$\overline{BSY}$)	0	1	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15 - D0	(RDY/$\overline{BSY}$)	0	1	Writes all registers. Valid only when Protect Register is cleared.
EWDS	1	00	00XXXXXX	—	High-Z	0	X	Erase/Write Disable deactivates all programming instructions.
PRREAD	1	10	XXXXXXXX	—	A7-A0	1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX	—	High-Z	1	1	Must immediately precede PRCLEAR, PRWRITE and PRDS instructions.
PRCLEAR	1	11	11111111	—	(RDY/$\overline{BSY}$)	1	1	Clears the Protect Register such that all data are NOT write-protected.
PRWRITE	1	01	A7 - A0*	—	(RDY/$\overline{BSY}$)	1	1	Programs address into Protect Register. Thereafter, memory addresses greater than or equal to the address in Protect Register are write-protected.
PRDS	1	00	00000000	—	(RDY/$\overline{BSY}$)	1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

Note: Address A7 bit is a "don't care" on 93LCS56.

2.0 FUNCTIONAL DESCRIPTION

The 93LCS56/66 is organized as 128/256 registers by 16 bits. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, WRAL, PRREAD, PREN, PRCLEAR, PRWRITE, and PRDS). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

2.4 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

2.5 Erase/Write Enable and Disable (EWEN, EWDS)

The 93LCS56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. The PE pin MUST be held "high" while loading the EWEN instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.6 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle. The PE pin MUST be latched "high" during loading the ERASE instruction but becomes a "don't care" after loading the instruction.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCLS). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction. ERASE instruction is valid if specified address is unprotected.

The ERASE cycle takes 4 ms per word typical.

2.7 WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. Both CS and CLK must be low to initiate the self-timed auto-erase and programming cycle. The PE pin MUST be latched "high" while loading the WRITE instruction but becomes a "don't care" thereafter.

The DO pin indicates the READY/$\overline{BUSY}$ status of the device if CS is brought high after a minimum of 250 ns (T_{CSL}) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction. WRITE instruction is valid only if specified address is unprotected.

The WRITE cycle takes 4 ms per word typical.

2.8 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. PE pin MUST be held "high" while loading the instruction but becomes "don't care" thereafter. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at V_{CC} = 4.5 to 6V and valid only when Protect Register is cleared.

The DO pin indicates the READY/$\overline{BUSY}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}) and before the entire write cycle is complete.

The ERAL cycle takes 15 ms maximum (8 ms typical).

2.9 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. PE pin MUST be held "high" while loading the instruction but becomes "don't care" thereafter. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at V_{CC} = 4.5 to 6V and valid only when Protect Register is cleared.

The DO pin indicates the READY/$\overline{BUSY}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}).

The WRAL cycle takes 30 ms maximum (16 ms typical).

Note:	In order to execute either READ, EWEN, ERAL, WRITE, WRAL, or EWDS instructions, the Protect Register Enable (PRE) pin must be held LOW.

2.10 Protect Register Read (PRREAD)

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin MUST be held HIGH when loading the instruction and remains HIGH until CS goes LOW. A dummy zero bit precedes the 8-bit output string. The output data bits in the memory Protect Register will toggle on the rising edge of the CLK as in the READ mode.

2.11 Protect Register Enable (PREN)

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the device must be in the EWEN mode. Both PRE and PE pins MUST be held "high" while loading the instruction. The PREN instruction MUST immediately precede a PRCLEAR, PRWRITE, or PRDS instruction.

2.12 Protect Register Clear (PRCLEAR)

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables all registers for programming instructions such as ERASE, ERAL, WRITE, and WRAL. The PRE and PE pin MUST be held HIGH when loading the instruction. Thereafter, PRE and PE pins become "don't care". A PREN instruction must immediately precede a PRCLEAR instruction.

2.13 Protect Register Write (PRWRITE)

The Protect Register Write (PRWRITE) instruction writes into the Protect Register the address of the first register to be protected. After this instruction is executed, all registers whose memory addresses are greater than or equal to the address pointer specified in the Protect register are protected from any programming instructions. Note that a PREN instruction must be executed before a PRWRITE instruction and, the Protect Register must be cleared (by a PRCLEAR instruction) before executing the PRWRITE instruction. The PRE and PE pins MUST be held HIGH while loading PRWRITE instruction. After the instruction is loaded, they become "don't care".

2.14 Protect Register Disable (PRDS)

The Protect Register Disable (PRDS) instruction is a ONE TIME ONLY instruction to permanently set the address specified in the Protect Register. Any attempts to change the address pointer will be aborted. The PRE and PE pins MUST be held HIGH while loading PRDS instruction. After the instruction is loaded, they become "don't care". Note that a PREN instruction must be executed before a PRDS instruction.

FIGURE 2-1: SYNCHRONOUS DATA TIMING

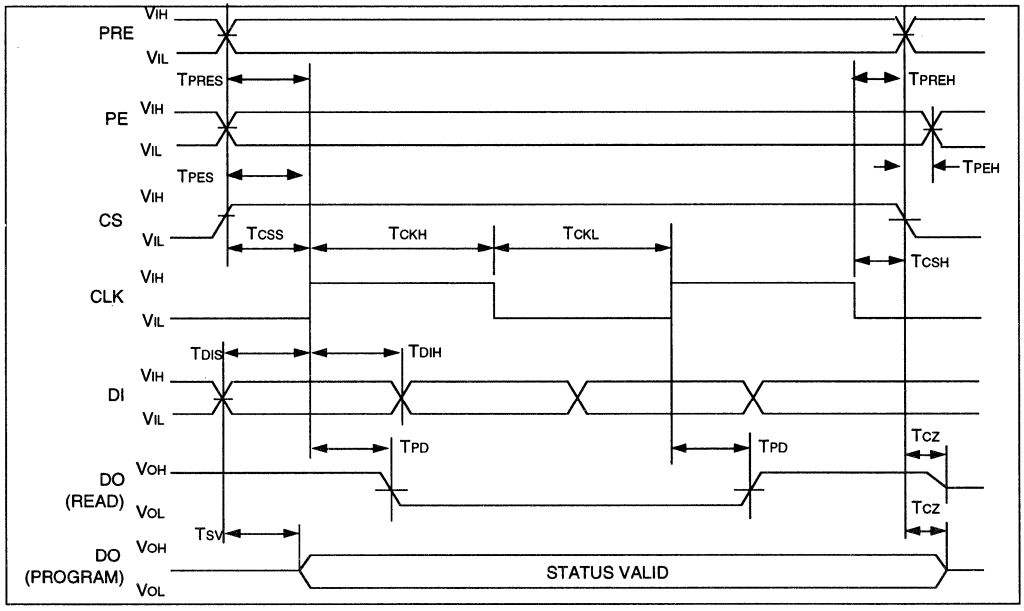
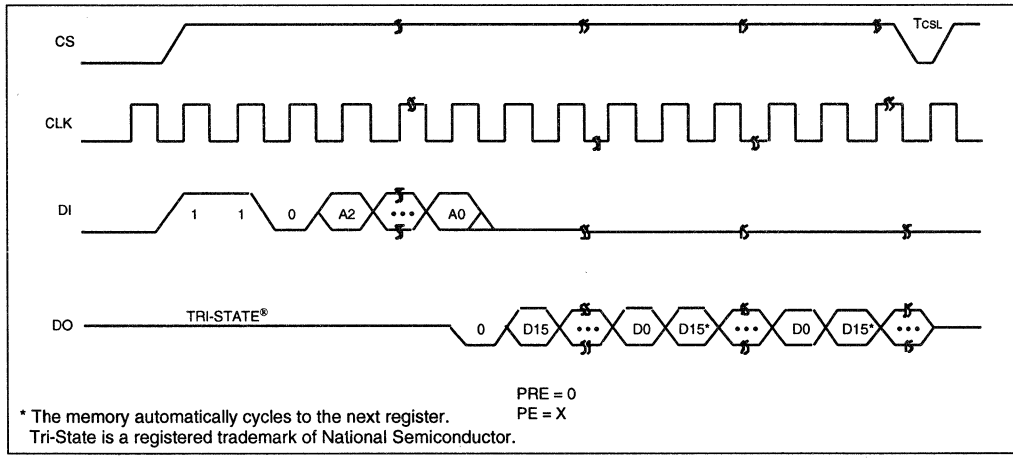


FIGURE 2-2: READ TIMING



* The memory automatically cycles to the next register.
Tri-State is a registered trademark of National Semiconductor.

FIGURE 2-3: EWEN TIMING

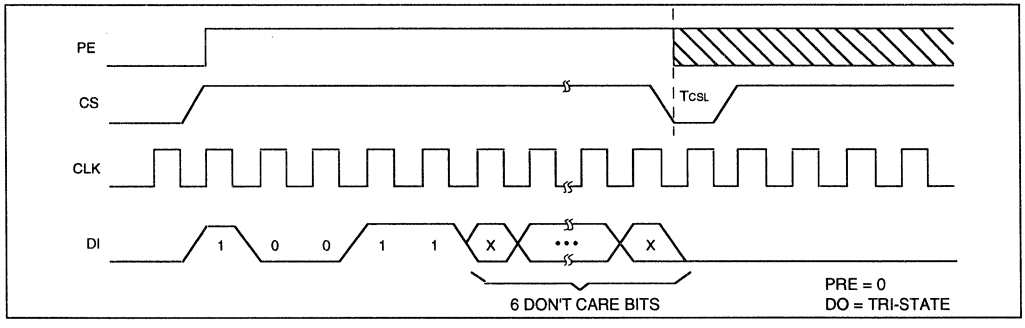


FIGURE 2-4: EWDS TIMING

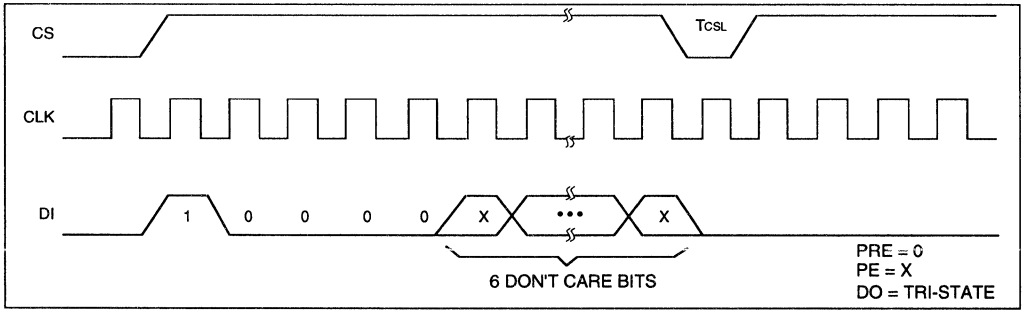


FIGURE 2-5: WRITE TIMING

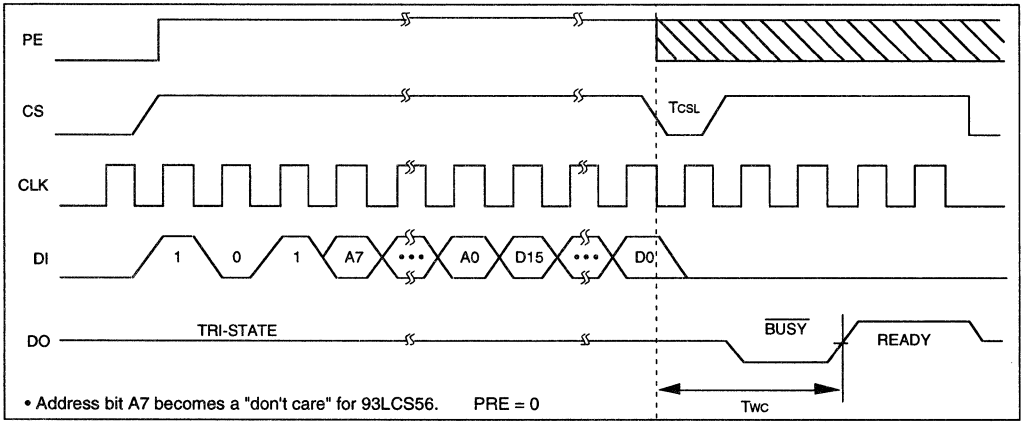


FIGURE 2-6: WRAL TIMING

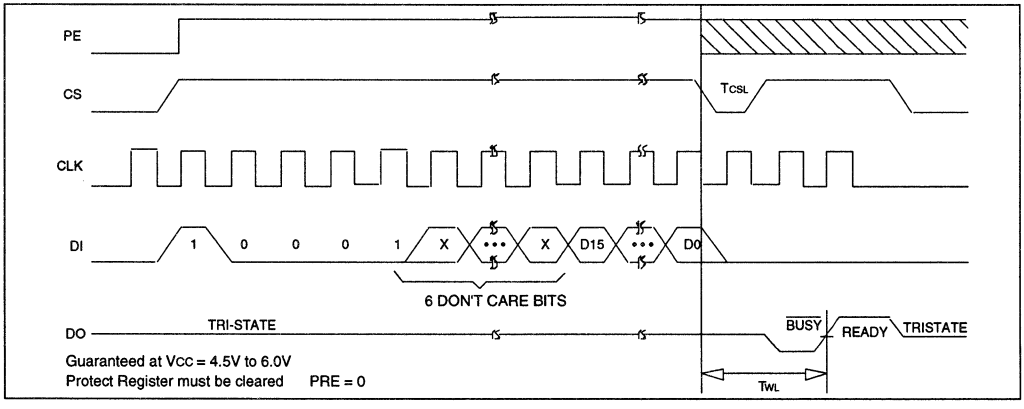


FIGURE 2-7: ERASE TIMING

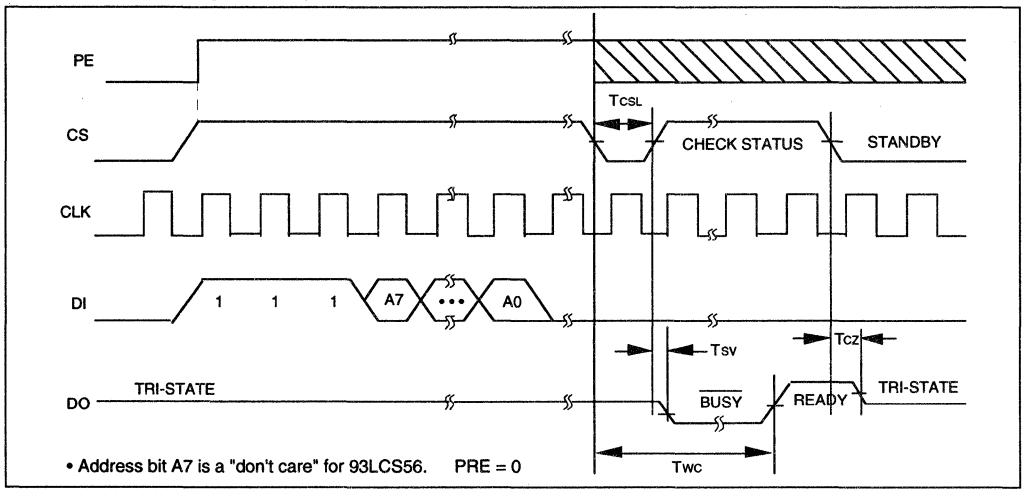


FIGURE 2-8: ERAL TIMING

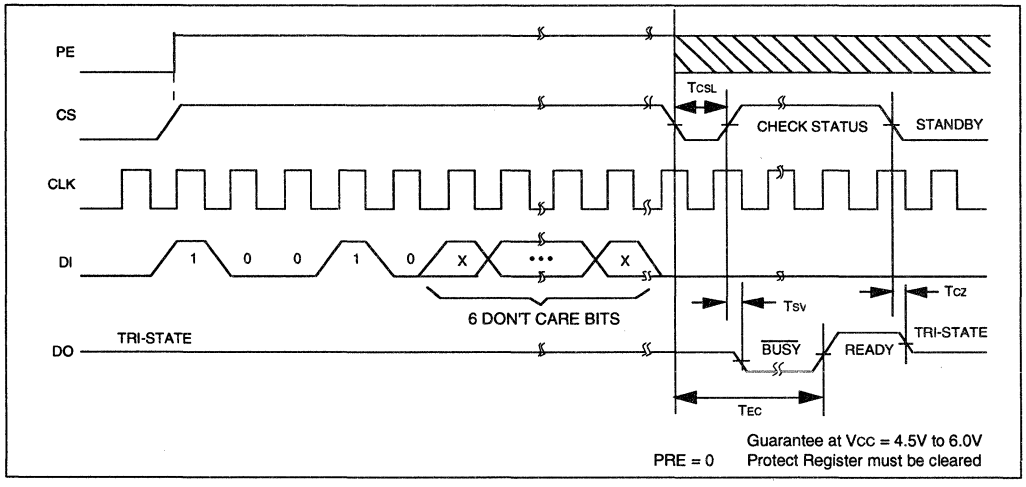


FIGURE 2-9: PRREAD TIMING

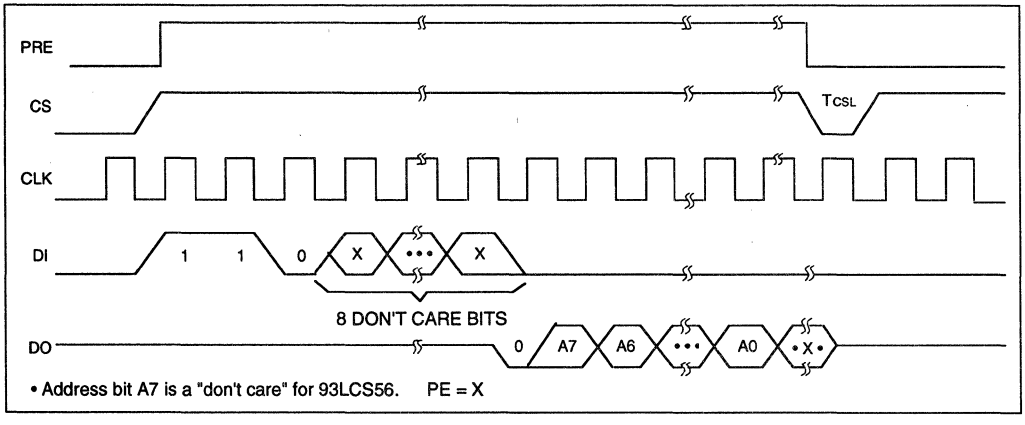


FIGURE 2-10: PREN TIMING

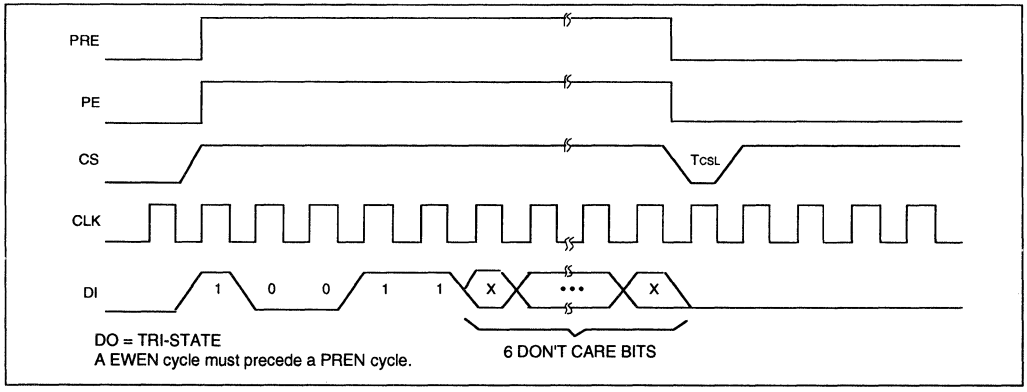


FIGURE 2-11: PRCLEAR TIMING

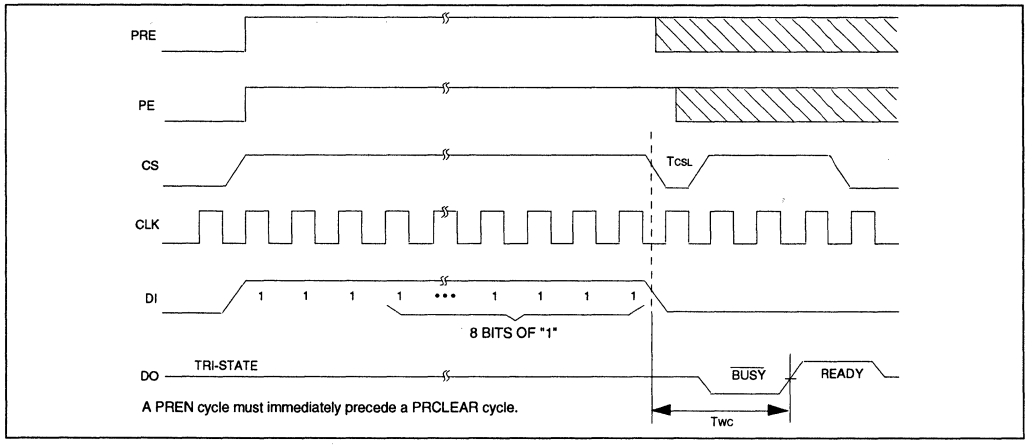


FIGURE 2-12: PRWRITE TIMING

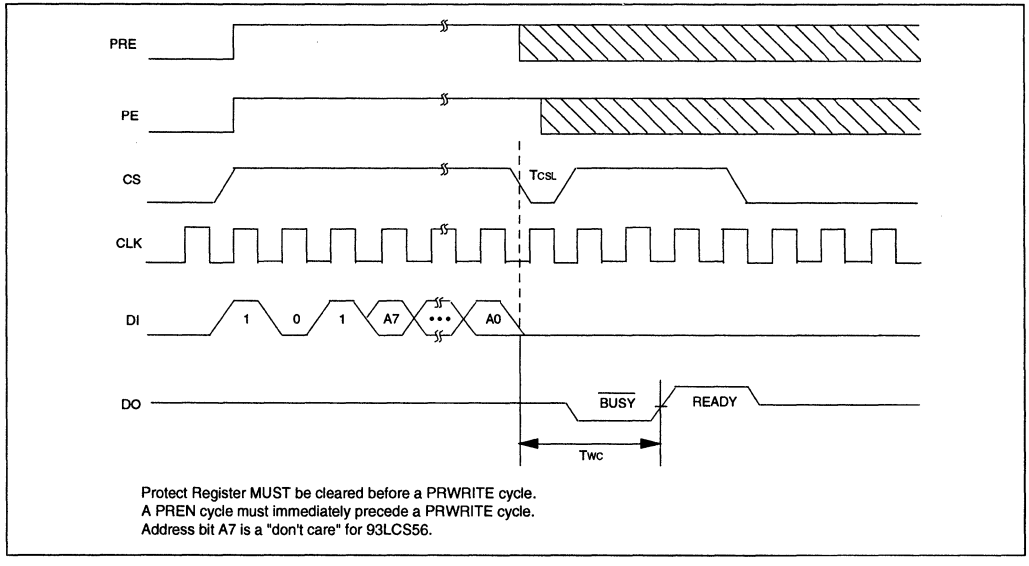
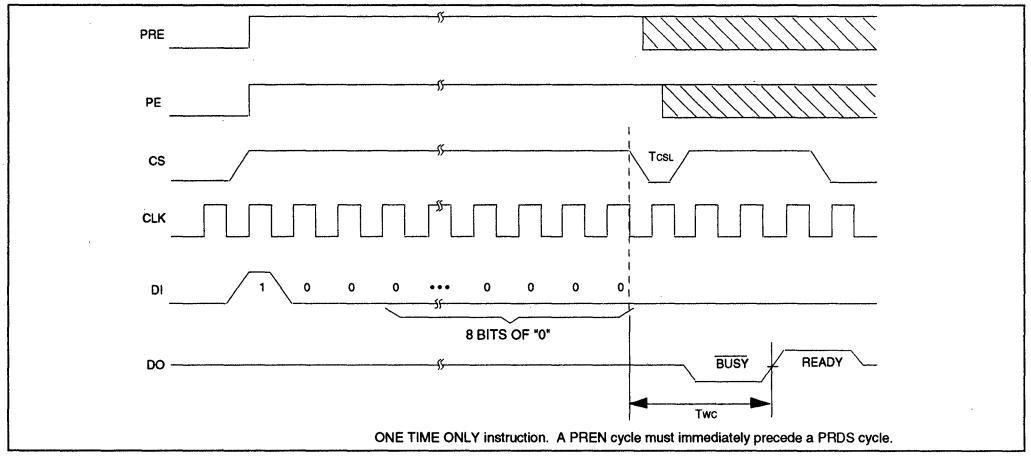


FIGURE 2-13: PRDS TIMING



ONE TIME ONLY instruction. A PREN cycle must immediately precede a PRDS cycle.

3.0 PIN DESCRIPTION

3.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCS56/66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCDD) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

3.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out is used in the READ and PRREAD mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after held LOW for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

3.5 Program Enable (PE)

This pin should be held HIGH in the programming mode or when executing the Protect Register programming instructions.

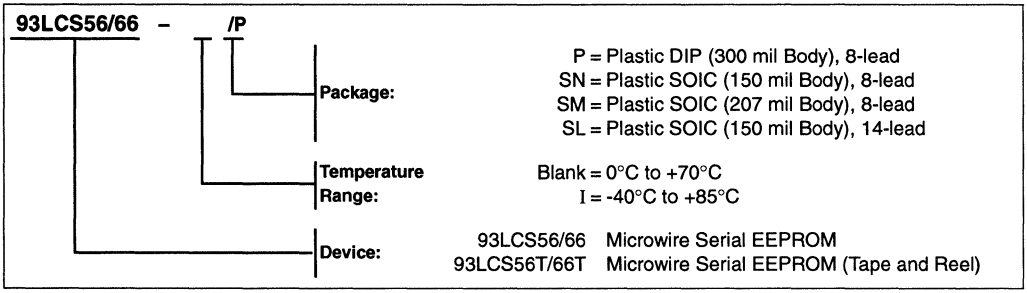
3.6 Protect Register Enable (PRE)

This pin should be held HIGH when executing all Protect Register instructions. Otherwise, it must be held LOW for normal operations.

NOTES:

93LCS56/66 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

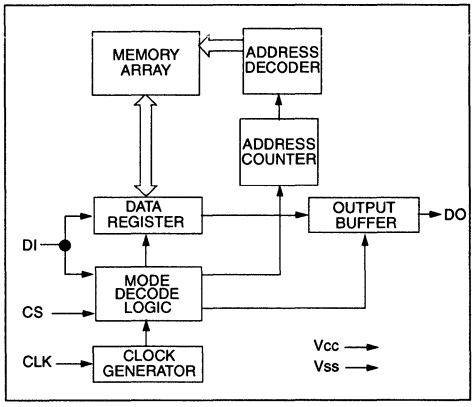
93LC66A/B

4K 2.5V Microwire® Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1 µA standby current (maximum)
- 512 x 8 bit organization (93LC66A)
- 256 x 16 bit organization (93LC66B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC and 8-pin TSSOP packages
- Available for the following temperature ranges:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

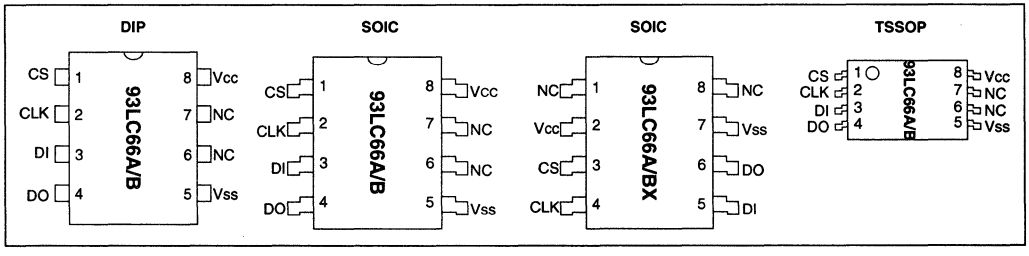
BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 93LC66A/B are 4K-bit, low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 (93LC66A) or x16 bits (93LC66B). Advanced CMOS technology makes these devices ideal for low power nonvolatile memory applications. The 93LC66A/B is available in standard 8-pin DIP, surface mount SOIC, and TSSOP packages. The 93LC66AX/BX are only offered in a 150-mil SOIC package.

PACKAGE TYPE



Microwire is a registered trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No Connect
Vcc	Power Supply

TABLE 1-2 DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted	Commercial (C): Vcc = +2.5V to +6.0V Tamb = 0°C to +70°C Industrial (I): Vcc = +2.5V to +6.0V Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	Vcc +1	V	2.7V ≤ Vcc ≤ 6.0V (Note 2)
	VIH2	0.7 Vcc	Vcc +1	V	Vcc < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	Vcc > 2.7V (Note 2)
	VIL2	-0.3	0.2 Vcc	V	Vcc < 2.7V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 µA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc = Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = Vss to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0 V (Notes 1 & 2) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC read	—	1 500	mA µA	FCLK = 2 MHz; Vcc = 6.0V FCLK = 1 MHz; Vcc = 3.0V
	ICC write	—	1.5	mA	
Standby current	ICCS	—	1	µA	CS = Vss; DI = Vss
Clock frequency	FCLK	—	2 1	MHz MHz	Vcc > 4.5V Vcc < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 2)
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	6	ms	ERASE/WRITE mode
	TEC	—	6	ms	ERAL mode
	TWL	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at Tamb = 25°C and Fclk = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock (CLK) is used to synchronize the communication between a master device and the 93LC66A/B. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

2.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1 INSTRUCTION SET FOR 93LC66A

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1	0	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	12
EWDS	1	00	0	0	X	X	X	X	X	X	X	—	HIGH-Z	12
EWEN	1	00	1	1	X	X	X	X	X	X	X	—	HIGH-Z	12
READ	1	10	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	20
WRITE	1	01	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0	1	X	X	X	X	X	X	X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20

TABLE 2-2 INSTRUCTION SET FOR 93LC66B

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	HIGH-Z	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	HIGH-Z	11
READ	1	10	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	27
WRITE	1	01	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcodes, addresses, and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data In (DI) Data Out (DO)

It is possible to connect the Data In (DI)and Data Out (DO)pins together. However, with this configuration, if A0 is a logic-high level, it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

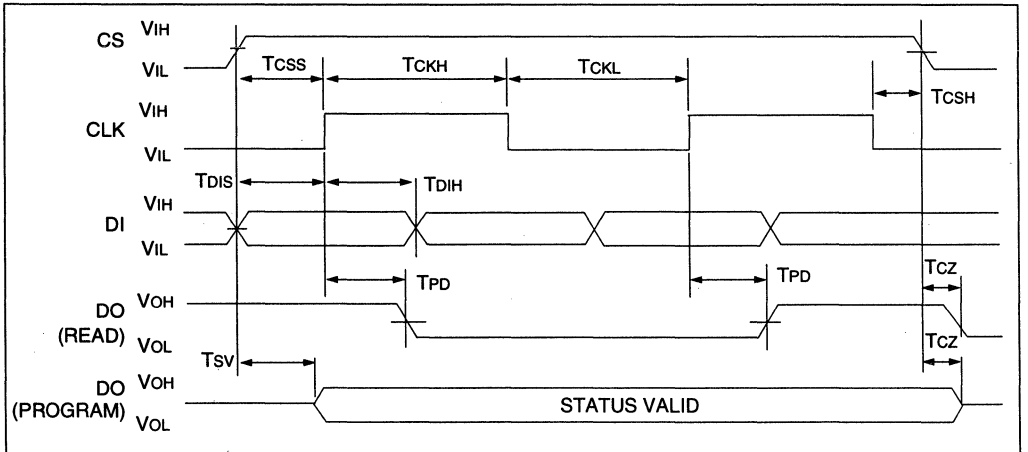
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 2.2V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 2.2V at nominal conditions.

The ERASE/WRITE Disable (EWDS) and ERASE/WRITE Enable (EWEN) commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



Note: AC Test Conditions: V_{IL} = 0.4V, V_{IH} = 2.4V.

3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{BUSY}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{BUSY}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

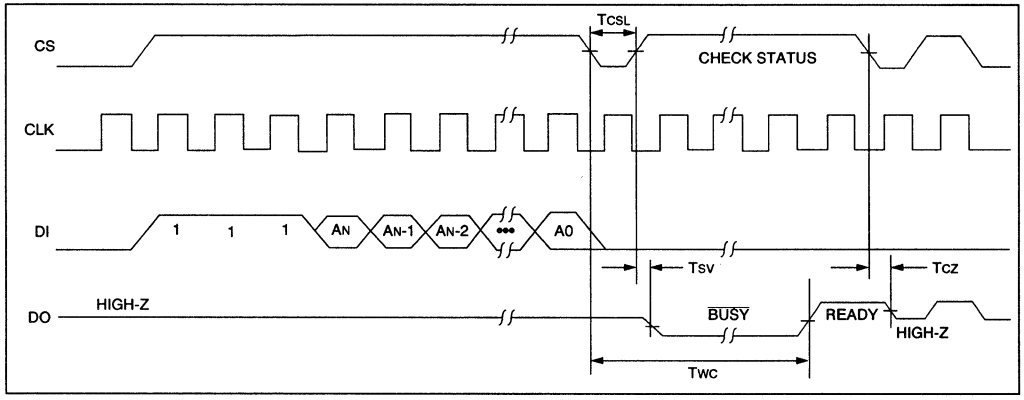
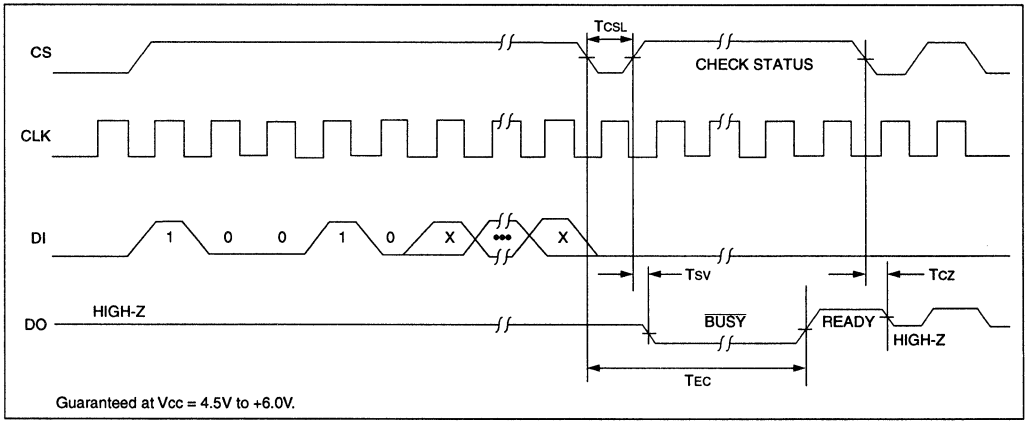


FIGURE 3-3: ERAL TIMING



Guaranteed at Vcc = 4.5V to +6.0V.

3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The 93LC66A/B powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWDS and EWEN instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93LC66A) or 16-bit (93LC66B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

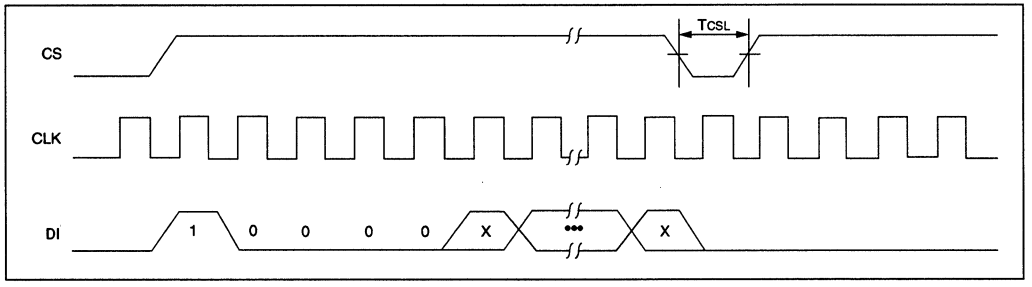


FIGURE 3-5: EWEN TIMING

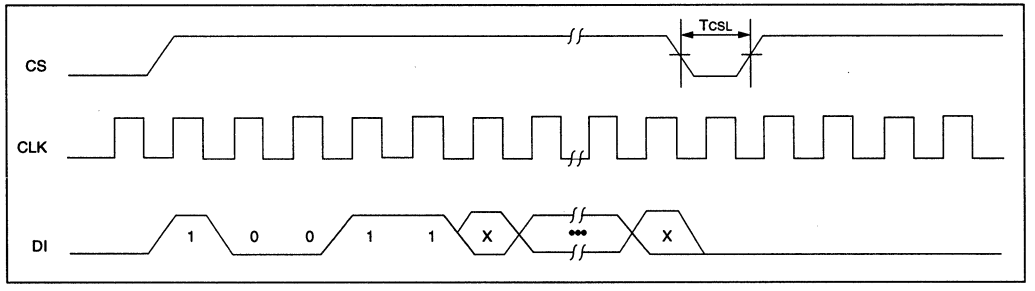
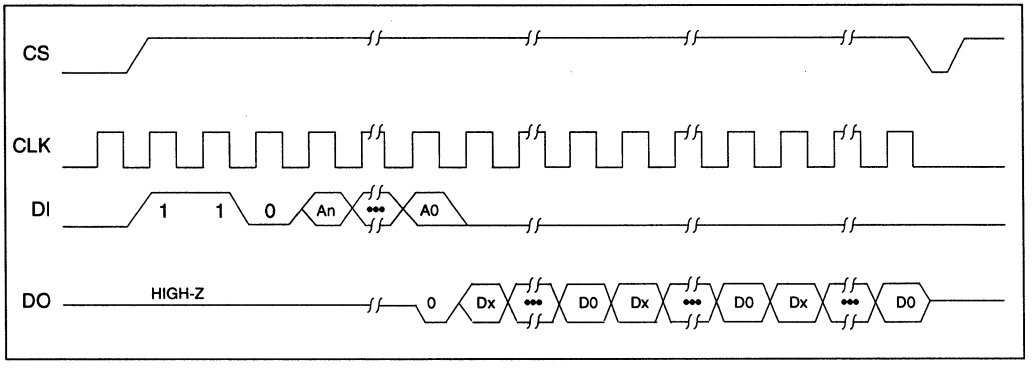


FIGURE 3-6: READ TIMING



3.8 WRITE

The WRITE instruction is followed by 8 bits (93LC66A) or 16 bits (93LC66B) of data which are written into the specified address. After the last data bit is put on the DI pin, the falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 3-7: WRITE TIMING

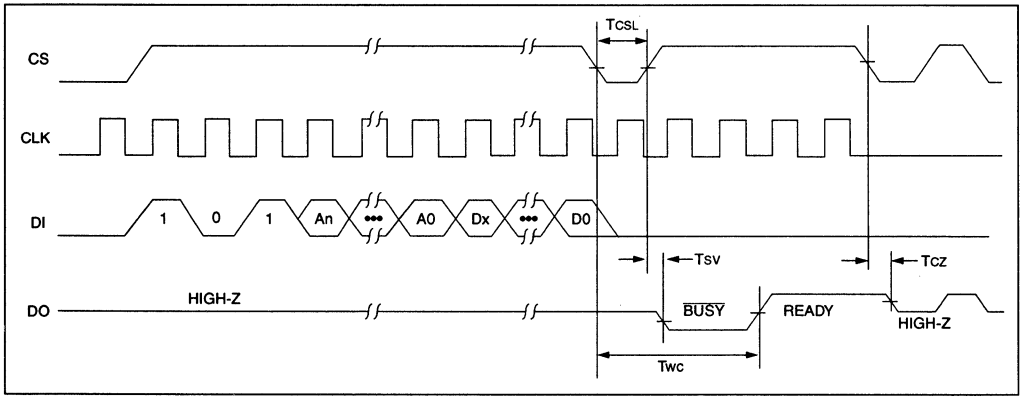
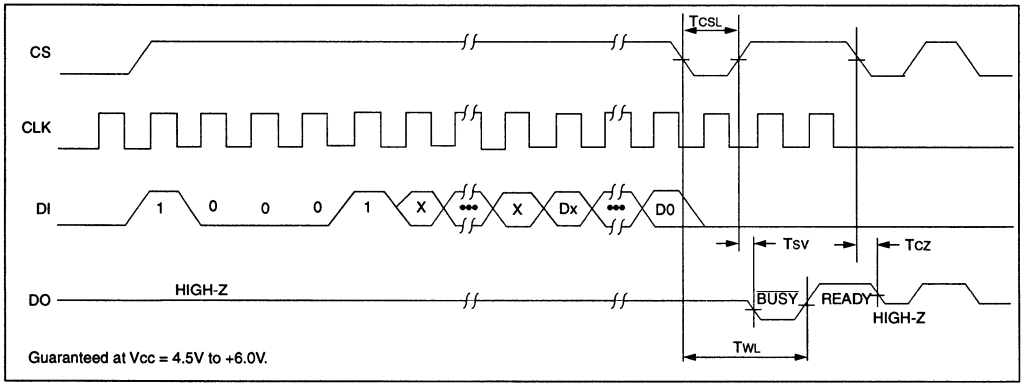
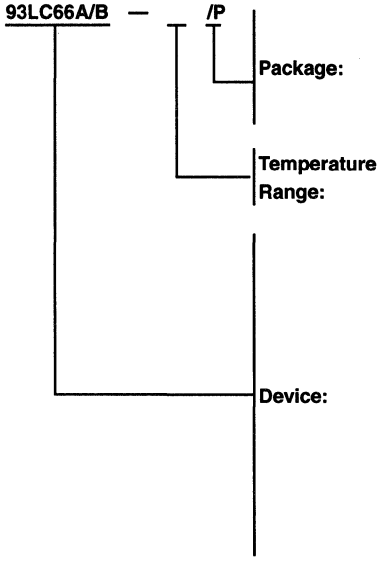


FIGURE 3-8: WRAL TIMING



93LC66A/B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	
P	= Plastic DIP (300 mil Body), 8-lead
SN	= Plastic SOIC (150 mil Body), 8-lead
SM	= Plastic SOIC (208 mil Body), 8-lead
ST	= TSSOP, 8-lead
Temperature Range:	
Blank	= 0°C to +70°C
I	= -40°C to +85°C
Device:	
93LC66A	4K Microwire Serial EEPROM (x8)
93LC66AT	4K Microwire Serial EEPROM (x8) Tape and Reel
93LC66AX	4K Microwire Serial EEPROM (x8) in alternate pinout (SN only)
93LC66AXT	4K Microwire Serial EEPROM (x8) in alternate pinout, Tape and Reel (SN only)
93LC66B	4K Microwire Serial EEPROM (x16)
93LC66BT	4K Microwire Serial EEPROM (x16) Tape and Reel
93LC66BX	4K Microwire Serial EEPROM (x16) in alternate pinout (SN only)
93LC66BXT	4K Microwire Serial EEPROM (x16) in alternate pinout, Tape and Reel (SN only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

93C66A/B

4K 5.0V Automotive Temperature Microwire® Serial EEPROM

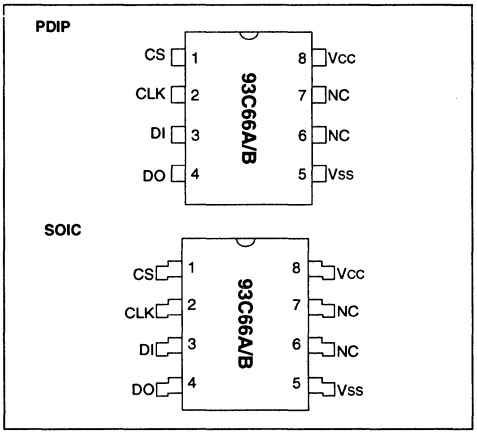
FEATURES

- Single supply 5.0V operation
- Low power CMOS technology
  - 1 mA active current (typical)
  - 1 µA standby current (maximum)
- 512x 8 bit organization (93C66A)
- 256x 16 bit organization (93C66B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial interface
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP and SOIC packages
- Available for the following temperature ranges:
  - Automotive (E): -40°C to +125°C

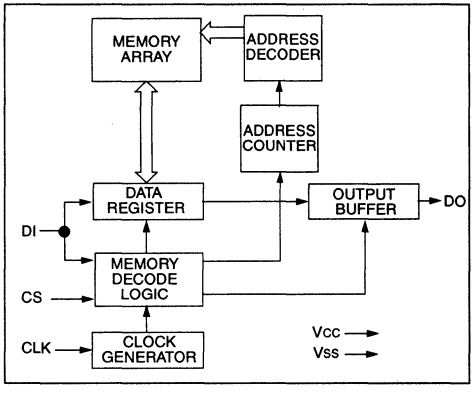
DESCRIPTION

The Microchip Technology Inc. 93C66A/B is a 4K-bit, low-voltage serial Electrically Erasable PROM. The device memory is configured as 512 x 8 bits (93C66A) or 256 x 16 bits (93C66B). Advanced CMOS technology makes this device ideal for low-power, nonvolatile memory applications. The 93C66A/B is available in standard 8-pin DIP and surface mount SOIC packages. **This device is only recommended for 5V automotive temperature applications. For all commercial and industrial temperature applications, the 93LC66A/B is recommended.**

PACKAGE TYPE



BLOCK DIAGRAM



4

Microwire®

Microwire is a registered trademark of National Semiconductor.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
NC	No Connect
VCC	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted	Automotive (E):VCC = +4.5V to +5.5VTamb = -40°C to +125°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH	2.0	VCC +1	V	(Note 2)
Low level input voltage	VIL	-0.3	0.8	V	
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
High level output voltage	VOH	2.4	—	V	IOH = -400 µA; VCC = 4.5V
Input leakage current	ILI	-10	10	µA	VIN = VSS to VCC
Output leakage current	ILO	-10	10	µA	VOUT = VSS to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7	pF	VIN/VOUT = 0 V (Notes 1 & 2) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	1.5	mA	
	ICC read	—	1	mA	
Standby current	ICCS	—	1	µA	CS = VSS; DI = VSS
Clock frequency	FCLK	—	2	MHz	
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 2)
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	2	ms	ERASE/WRITE mode
	TEC	—	6	ms	ERAL mode
	TWL	—	15	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 3)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
2: This parameter is periodically sampled and not 100% tested.
3: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which may be obtained on our website.

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock (CLK) is used to synchronize the communication between a master device and the 93C66A/B. Opcodes, addresses, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is low (device deselected). If CS is high, but the START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detecting a START condition, the specified number of clock cycles (respectively low to high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcodes, addresses, and data bits before an instruction is executed (Table 2-1 and Table 2-2). CLK and DI then become don't care inputs waiting for a new START condition to be detected.

Note: CS must go low between consecutive instructions.

2.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated. The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

TABLE 2-1: INSTRUCTION SET FOR 93C66A

Instruction	SB	Opcode	Address									Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1	0	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	12
EWDS	1	00	0	0	X	X	X	X	X	X	X	—	HIGH-Z	12
EWEN	1	00	1	1	X	X	X	X	X	X	X	—	HIGH-Z	12
READ	1	10	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	20
WRITE	1	01	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0	1	X	X	X	X	X	X	X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20

TABLE 2-2: INSTRUCTION SET FOR 93C66B

Instruction	SB	Opcode	Address								Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1	0	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	11
EWEN	1	00	1	1	X	X	X	X	X	X	—	HIGH-Z	11
EWDS	1	00	0	0	X	X	X	X	X	X	—	HIGH-Z	11
READ	1	10	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	27
WRITE	1	01	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0	1	X	X	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27

3.0 FUNCTIONAL DESCRIPTION

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an ERASE/WRITE operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the HIGH-Z state on the falling edge of the CS.

3.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (ERASE, ERAL, EWDS, EWEN, READ, WRITE, and WRAL). As soon as CS is high, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcodes, addresses, and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

3.2 Data In (DI) and Data Out (DO)

It is possible to connect the Data In (DI) and Data Out (DI) pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic-high level. Under such a condition the voltage level seen at DO is undefined and will depend upon the relative impedances of DO and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the DO pin.

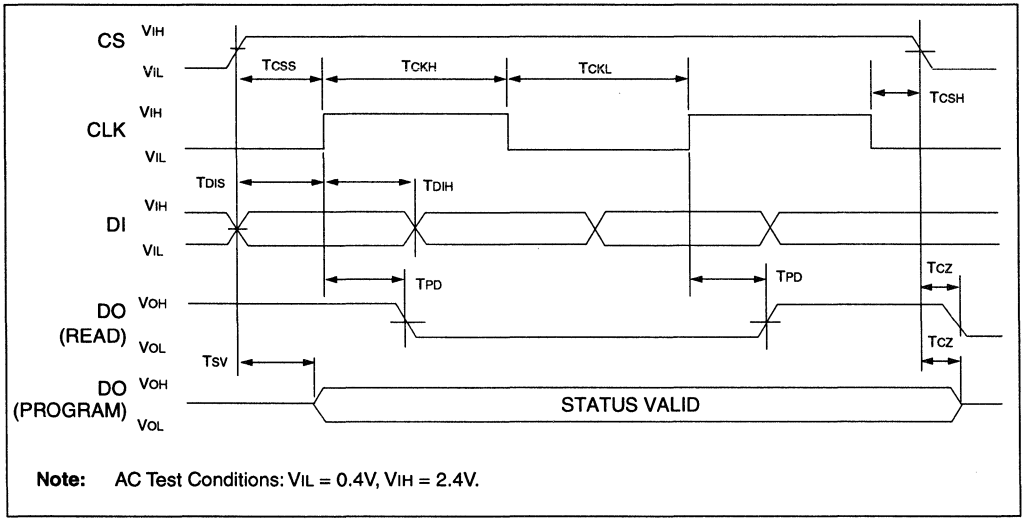
3.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 3.8V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 3.8V at nominal conditions.

The ERASE/WRITE Disable (EWDS) and ERASE/WRITE Enable (EWEN) commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

FIGURE 3-1: SYNCHRONOUS DATA TIMING



Note: AC Test Conditions: V_{IL} = 0.4V, V_{IH} = 2.4V.

3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. This cycle begins on the rising clock edge of the last address bit.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

3.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the rising clock edge of the last address bit. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire ERAL cycle is complete.

FIGURE 3-2: ERASE TIMING

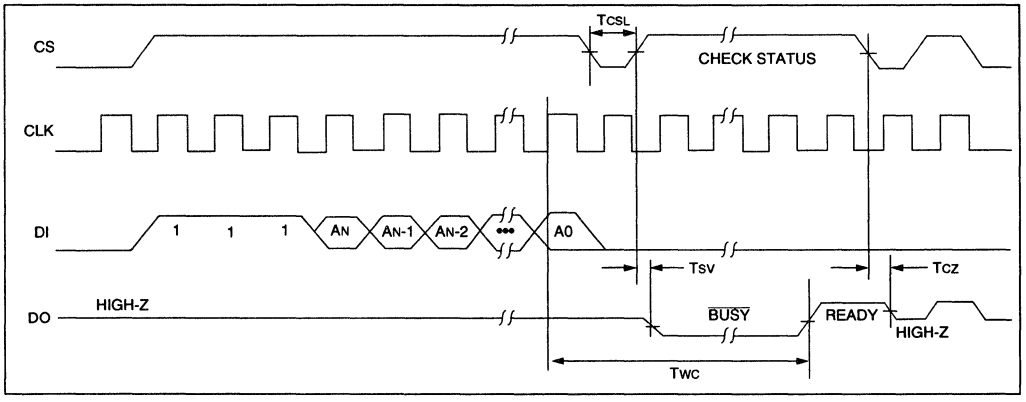
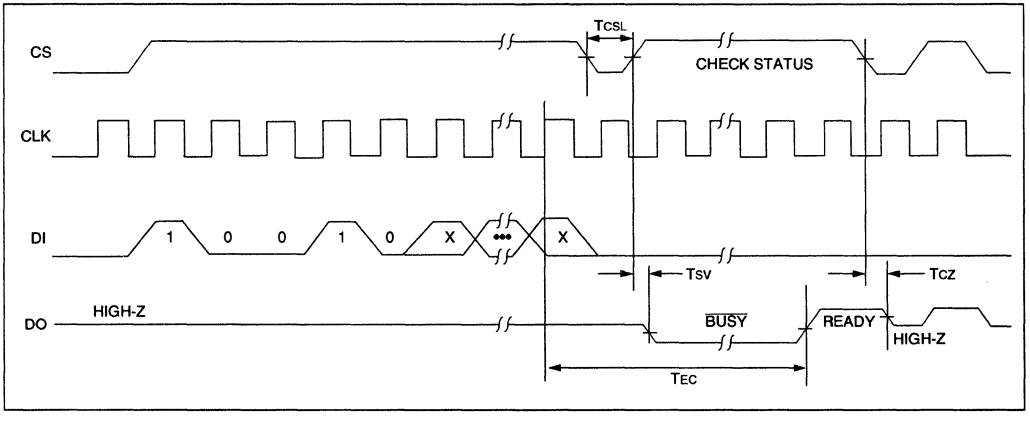


FIGURE 3-3: ERAL TIMING



3.6 ERASE/WRITE Disable and Enable (EWDS/EWEN)

The device powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (93C66A) or 16-bit (93C66B) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-4: EWDS TIMING

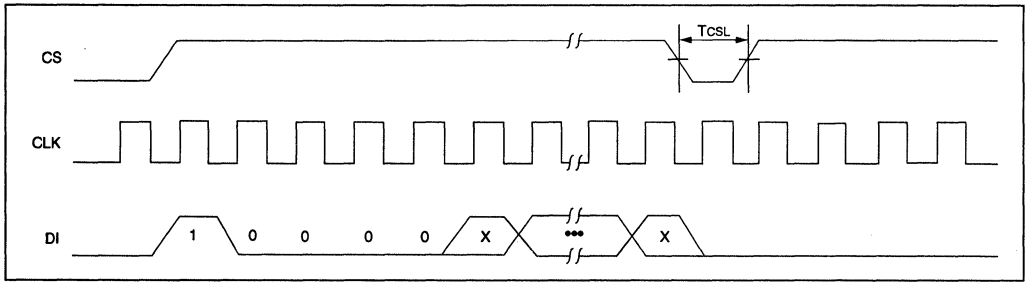


FIGURE 3-5: EWEN TIMING

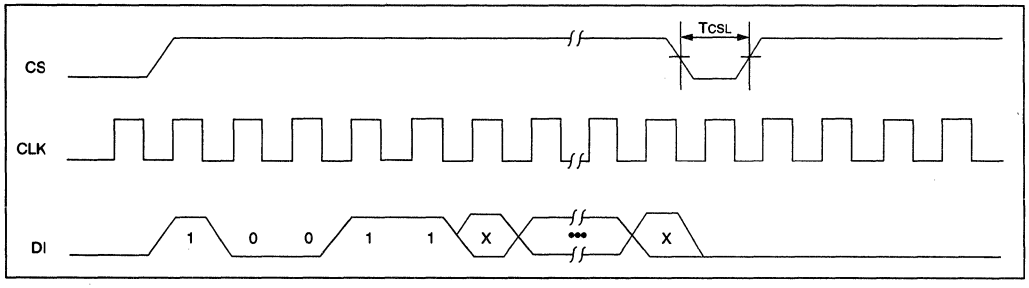
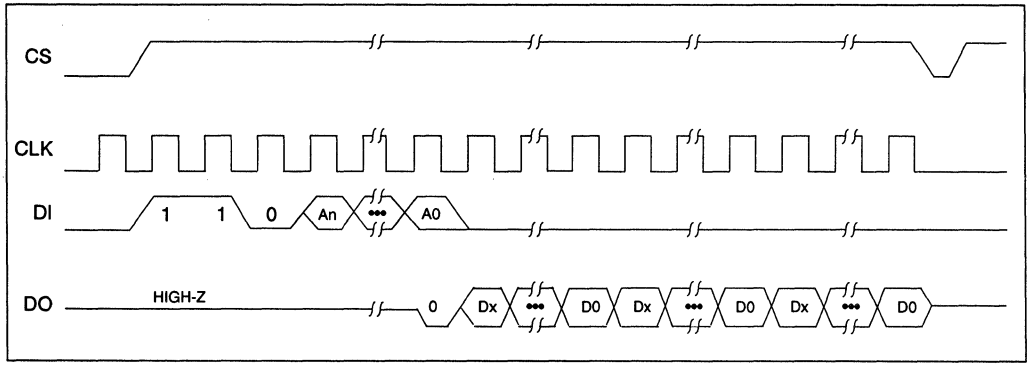


FIGURE 3-6: READ TIMING



3.8 WRITE

The WRITE instruction is followed by 8 bits (93C66A) or 16 bits (93C66B) of data which are written into the specified address. After the last data bit is clocked into the DI pin the self-timed auto-erase and programming cycle begins.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

3.9 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the rising clock edge of the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

FIGURE 3-7: WRITE TIMING

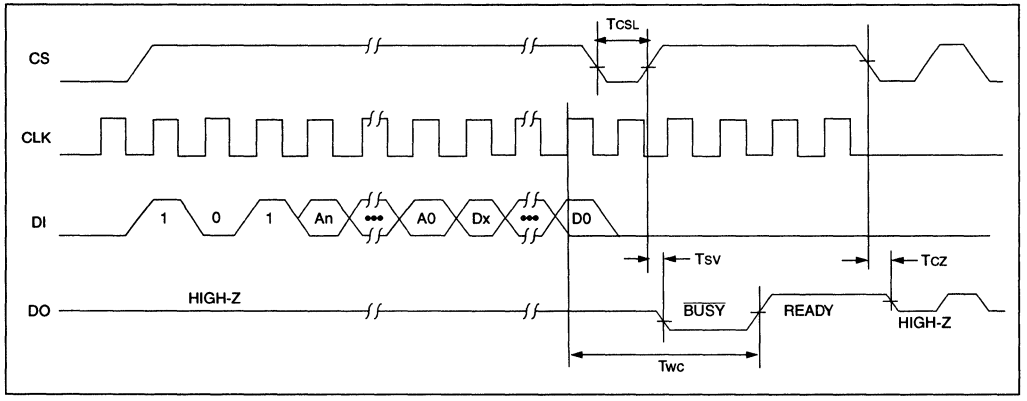
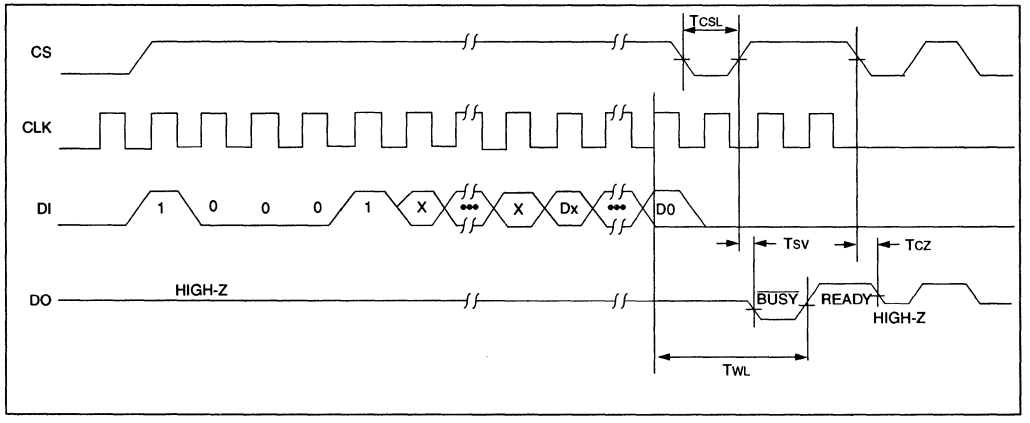
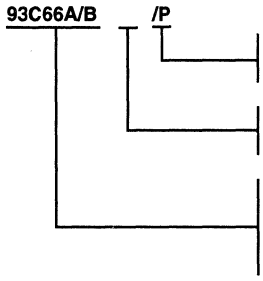


FIGURE 3-8: WRAL TIMING



93C66A/B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	E =	-40°C to +125°C
Device:	93C66A	4K Microwire Serial EEPROM (x8)
	93C66AT	4K Microwire Serial EEPROM (x8) Tape and Reel
	93C66B	4K Microwire Serial EEPROM (x16)
	93C66BT	4K Microwire Serial EEPROM (x16) Tape and Reel

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

93AA76/86

8K/16K 1.8V Microwire® Serial EEPROM

FEATURES

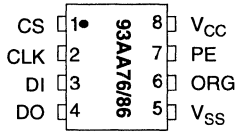
- Singie supply operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0V
- ORG pin selectable memory configuration
  - 1024 x 8 or 512 x 16-bit organization (93AA76)
  - 2048 x 8 or 1024 x 16-bit organization (93AA86)
- Self-timed ERASE and WRITE cycles
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC package
- Temperature ranges available:
  - Commercial (C): 0°C to +70°C

DESCRIPTION

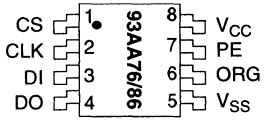
The Microchip Technology Inc. 93AA76/86 are 8K and 16K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. These devices also have a Program Enable (PE) pin to allow the user to write protect the entire contents of the memory array. The 93AA76/86 is available in standard 8-pin DIP and 8-pin surface mount SOIC packages.

PACKAGE TYPES

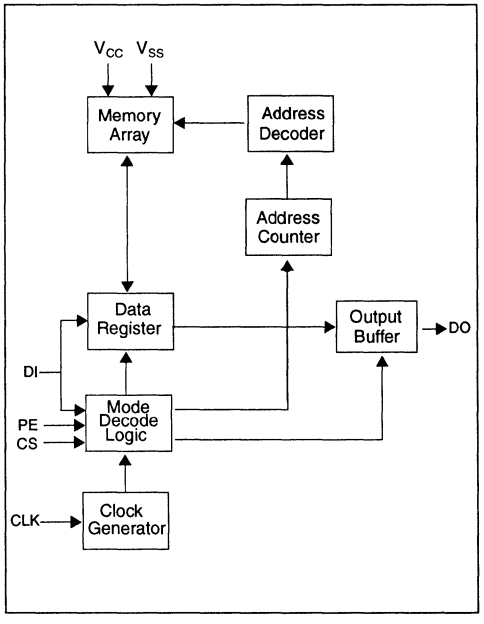
DIP Package



SOIC Package



BLOCK DIAGRAM



Microwire is a registered trademark of National Semiconductor Incorporated.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
ORG	Memory Configuration
PE	Program Enable
VCC	Power Supply

1.2 AC Test Conditions

AC Waveform:

VLO = 2.0V
VHI = VCC - 0.2V (Note 1)
VHI = 4.0V for (Note 2)

Timing Measurement Reference Level

Input 0.5 VCC
Output 0.5 VCC

Note 1: For VCC ≤ 4.0V
2: For VCC > 4.0V

TABLE 1-2: DC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted:
VCC = +1.8V to +6.0V
Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Min.	Max.	Units	Conditions
High level input voltage	VIH1	2.0	VCC +1	V	VCC ≥ 2.7V
	VIH2	0.7 VCC	VCC +1	V	VCC < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	VCC ≥ 2.7V
	VIL2	-0.3	0.2 VCC	V	VCC < 2.7V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; VCC = VCC Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; VCC = 4.5V
	VOH2	VCC-0.2	—	V	IOH = -100 µA; VCC = VCC Min.
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	CINT	—	7	pF	(Note Note:) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	3	mA	VCC = 5.5V
	ICC read	—	1 500	mA µA	FCLK = 3 MHz; VCC = 5.5V FCLK = 1 MHz; VCC = 3.0V
Standby current	ICCS	—	100 30	µA µA	CLK = CS = 0V; VCC = 5.5V CLK = CS = 0V; VCC = 3.0V DI = PE = VSS ORG = VSS or VCC

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted: Vcc = +1.8V to +6.0V Commercial (C): Tamb = 0°C to +70°C					
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Clock frequency	FCLK	—	3 2 1	MHz MHz Mhz	4.5V ≤ Vcc ≤ 6.0V 2.5V ≤ Vcc ≤ 4.5V 1.8V ≤ Vcc < 2.5V
Clock high time	TCKH	200 300 500	—	ns ns ns	4.5V ≥ Vcc ≤ 6.0V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
Clock low time	TCKL	100 200 500	—	ns ns ns	4.5V ≤ Vcc ≤ 6.0V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
Chip select setup time	TCSS	50 100 250	—	ns ns ns	4.5V ≤ Vcc ≤ 6.0V, Relative to CLK 2.5V ≤ Vcc < 4.5V, Relative to CLK 1.8V ≤ Vcc < 2.5V, Relative to CLK
Chip select hold time	TCSH	0	—	ns	1.8V ≤ Vcc ≤ 6.0V
Chip select low time	TCSL	250	—	ns	1.8V ≤ Vcc ≤ 6.0V, Relative to CLK
Data input setup time	TDIS	50 100 250	—	ns ns ns	4.5V ≤ Vcc ≤ 6.0V, Relative to CLK 2.5V ≤ Vcc <4.5V, Relative to CLK 1.8V ≤ Vcc < 2.5V, Relative to CLK
Data input hold time	TDIH	50 100 250	—	ns ns ns	4.5V ≤ Vcc ≤ 6.0V, Relative to CLK 2.5V ≤ Vcc < 4.5V, Relative to CLK 1.8V ≤ Vcc < 2.5V, Relative to CLK
Data output delay time	TPD	—	100 250 500	ns ns ns	4.5V ≤ Vcc ≤ 6.0V, CL = 100 pF 2.5V ≤ Vcc < 4.5V, CL = 100 pF 1.8V ≤ Vcc < 2.5V, CL = 100 pF
Data output disable time	TCZ	—	100 500	ns ns	4.5V ≤ Vcc ≤ 5.5V (Note 1) 1.8V ≤ Vcc < 4.5V (Note 1)
Status valid time	TSV	—	200 300 500	ns ns ns	4.5V ≥ Vcc ≤ 6.0V, CL = 100 pF 2.5V ≤ Vcc < 4.5V, CL = 100 pF 1.8V ≤ Vcc < 2.5V, CL = 100 pF
Program cycle time	TWC	—	5	ms	ERASE/WRITE mode
	TEC	—	15	ms	ERAL mode
	TWL	—	30	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

TABLE 1-4: INSTRUCTION SET FOR 93AA76: ORG=1 (X16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	X A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

TABLE 1-5: INSTRUCTION SET FOR 93AA76: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	14
ERASE	1	11	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	14

TABLE 1-6: INSTRUCTION SET FOR 93AA86: ORG=1 (X16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

TABLE 1-7: INSTRUCTION SET FOR 93AA86: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	14
ERASE	1	11	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	14

2.0 PRINCIPLES OF OPERATION

When the ORG pin is connected to Vcc, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high impedance state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction are clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Erase/Write Enable and Disable (EWEN, EWDS)

The 93AA76/86 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.4 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

3.0 DEVICE OPERATION

3.1 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high and clock transitions continue. The memory address pointer will automatically increment and output data sequentially.

3.2 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of CLK as the last address bit (A0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 3 ms per word (Typical).

3.3 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data to be written into the specified address. The self-timed programming cycle is initiated on the rising edge of CLK as the last data bit (D0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written and the device is ready for another instruction.

The WRITE cycle takes 3 ms per word (Typical).

3.4 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't care bits, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been erased and is ready for another instruction.

The ERAL cycle takes 15 ms maximum (8 ms typical).

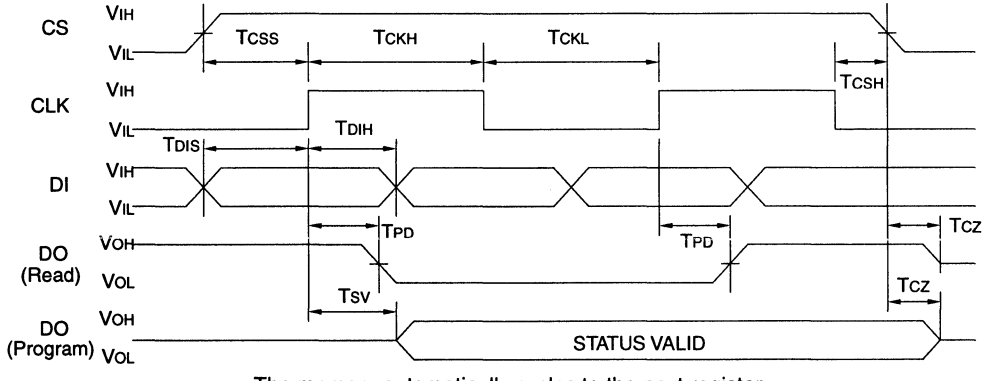
3.5 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't cares, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been written and is ready for another instruction.

The WRAL cycle takes 30 ms maximum (16 ms typical).

FIGURE 3-1: SYNCHRONOUS DATA TIMING



The memory automatically cycles to the next register.

FIGURE 3-2: READ

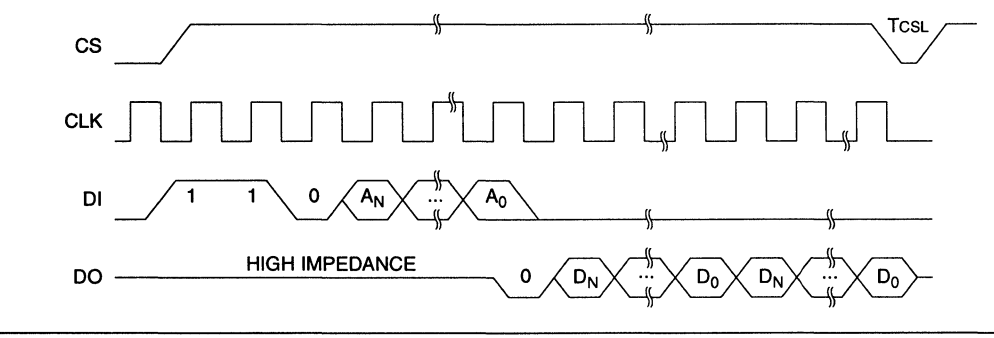


FIGURE 3-3: EWEN

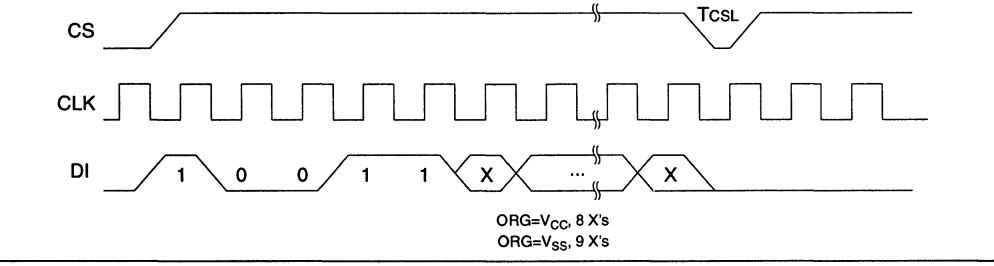


FIGURE 3-4: EWDS

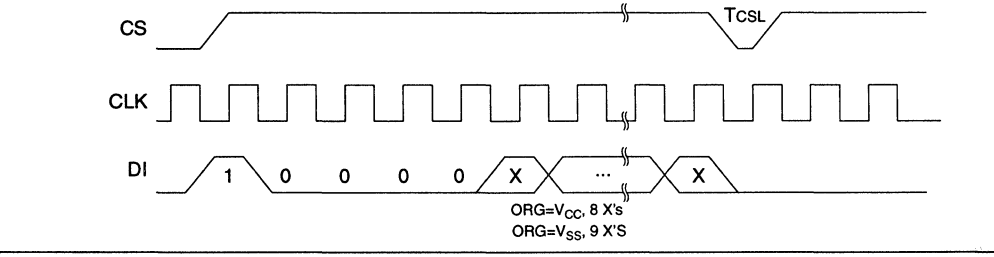


FIGURE 3-5: WRITE

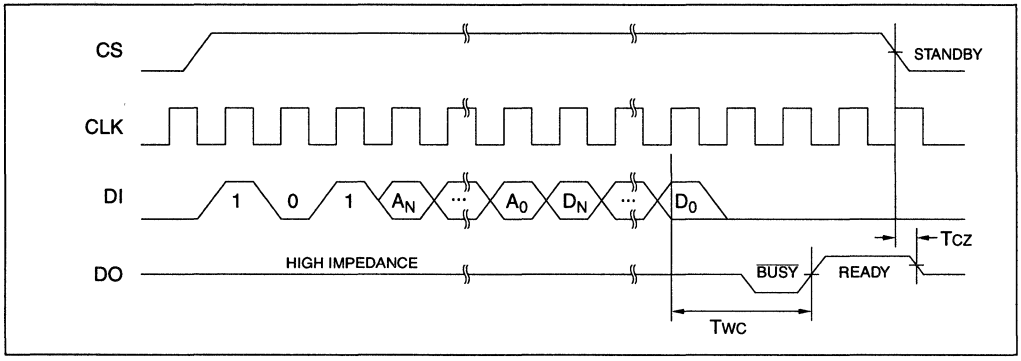


FIGURE 3-6: WRAL

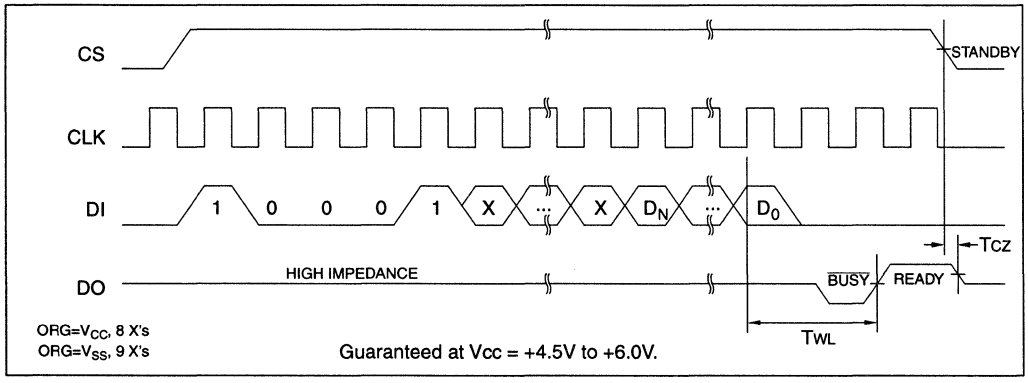


FIGURE 3-7: ERASE

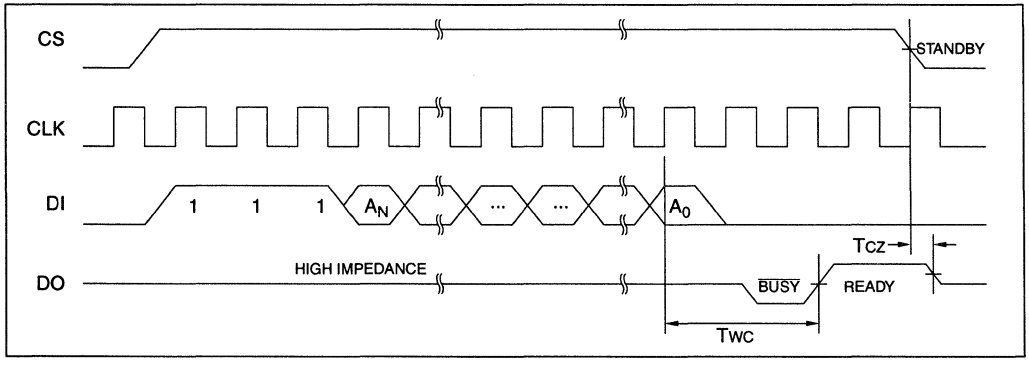
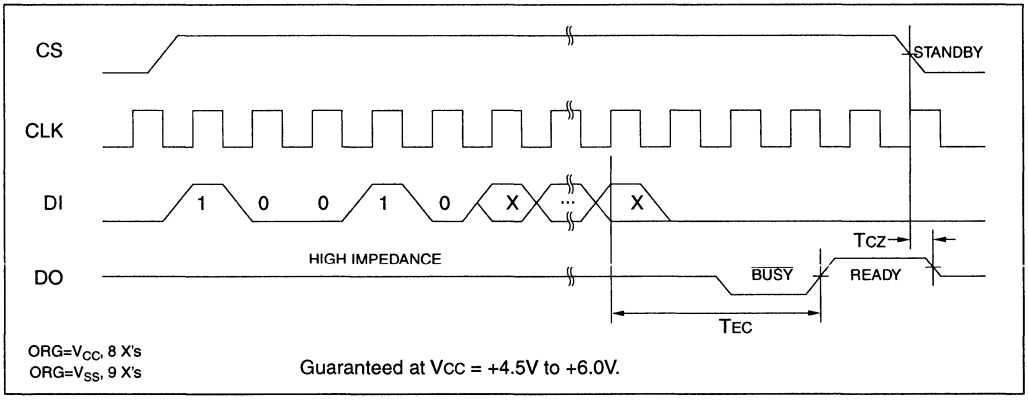


FIGURE 3-8: ERAL



4.0 PIN DESCRIPTIONS

4.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93AA76/86. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all opcode, address, and data bits before an instruction is executed (see Table 1-4 through Table 1-7 for more details). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions, except when performing a sequential read (Refer to Section 3.1 for more detail on sequential reads).

4.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

4.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available when CS is high. It will be displayed until the next start bit occurs as long as CS stays high.

4.5 Organization (ORG)

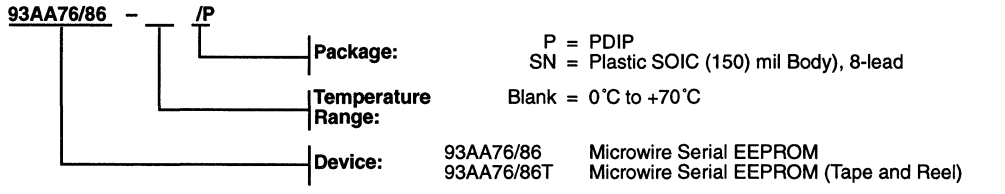
When ORG is connected to VCC, the x16 memory organization is selected. When ORG is tied to VSS, the x8 memory organization is selected. There is an internal pull-up resistor on the ORG pin that will select x16 organization when left unconnected.

4.6 Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is floated or tied to VCC, the device can be programmed. If the PE pin is tied to VSS, programming will be inhibited. There is an internal pull-up on this device that enables programming if this pin is left floating.

93AA76/86 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

93LC76/86

8K/16K 2.5V Microwire® Serial EEPROM

FEATURES

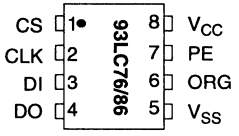
- Singie supply with programming operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0V
- ORG pin selectable memory configuration
  1024 x 8 or 512 x 16 bit organization (93LC76)
  2048 x 8 or 1024 x 16 bit organization (93LC86)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC package
- Temperature ranges available
  - Commercial (C) 0°C to +70°C
  - Industrial (I) -40°C to +85°C

DESCRIPTION

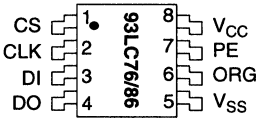
The Microchip Technology Inc. 93LC76/86 are 8K and 16K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. These devices also have a Program Enable (PE) pin to allow the user to write protect the entire contents of the memory array. The 93LC76/86 is available in standard 8-pin DIP and 8-pin surface mount SOIC packages.

PACKAGE TYPES

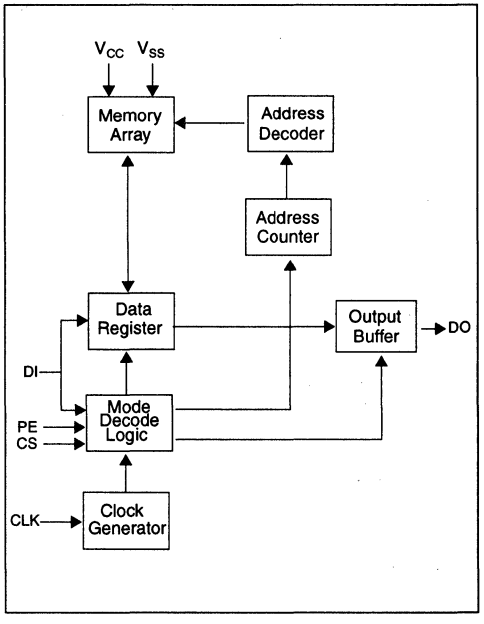
DIP Package



SOIC Package



BLOCK DIAGRAM



Microwire is a registered trademark of National Semiconductor Incorporated.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Configuration
PE	Program Enable
Vcc	Power Supply

1.2 AC Test Conditions

AC Waveform:

VLO = 2.0V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V for (Note 2)

Timing Measurement Reference Level

Input 0.5 Vcc
Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V
2: For Vcc > 4.0V

TABLE 1-2: DC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted:
Vcc = +2.5V to +6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
High level input voltage	VIH1	2.0	Vcc +1	V	Vcc ≥ 2.7V
	VIH2	0.7 Vcc	Vcc +1	V	Vcc < 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.7V
	VIL2	-0.3	0.2 Vcc	V	Vcc < 2.7V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc = Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Pin capacitance (all inputs/outputs)	CINT	—	7	pF	(Note Note:) Tamb = +25°C, FCLK = 1 MHz
Operating current	Icc write	—	3	mA	Vcc = 5.5V
	Icc read	—	1 500	mA µA	FCLK = 3 MHz; Vcc = 5.5V FCLK = 1 MHz; Vcc = 3.0V
Standby current	Iccs	—	100 30	µA µA	CLK = CS = 0V; Vcc = 5.5V CLK = CS = 0V; Vcc = 3.0V DI = PE = Vss ORG = Vss or Vcc

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted:
Vcc = +2.5V to +6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
Clock frequency	FCLK	—	3 2	MHz MHz	4.5V ≤ Vcc ≤ 6.0V 2.5V ≤ Vcc < 4.5V
Clock high time	TCKH	200 300	—	ns ns	4.5V ≤ Vcc ≤ 6.0V 2.5V ≤ Vcc < 4.5V
Clock low time	TCKL	100 200	—	ns ns	4.5V ≥ Vcc ≤ 6.0V 2.5V ≤ Vcc < 4.5V
Chip select setup time	TCSS	50 100	—	ns ns	4.5V ≤ Vcc ≤ 6.0V, Relative to CLK 2.5V ≤ Vcc < 4.5V, Relative to CLK
Chip select hold time	TCSH	0	—	ns	
Chip select low time	TCSL	250	—	ns	Relative to CLK
Data input setup time	TDIS	50 100	—	ns ns	4.5V ≤ Vcc ≤ 6.0V, Relative to CLK 2.5V ≤ Vcc <4.5V, Relative to CLK
Data input hold time	TDIH	50 100	—	ns ns	4.5V ≤ Vcc ≤ 6.0V, Relative to CLK 2.5V ≤ Vcc < 4.5V, Relative to CLK
Data output delay time	TPD	—	100 250	ns ns	4.5V ≤ Vcc ≤ 6.0V, CL = 100 pF 2.5V ≤ Vcc < 4.5V, CL = 100 pF
Data output disable time	TCZ	—	100 500	ns ns	4.5V ≤ Vcc ≤ 6.0V 2.5V ≤ Vcc < 4.5V (Note 1)
Status valid time	TSV	—	200 300	ns ns	4.5V ≥ Vcc ≤ 6.0V, CL = 100 pF 2.5V ≤ Vcc <4.5V, CL = 100 pF
Program cycle time	TWC	—	5	ms	ERASE/WRITE mode
	TEC	—	15	ms	ERAL mode
	TWL	—	30	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.
2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be found on our website.

TABLE 1-4: INSTRUCTION SET FOR 93LC76: ORG=1 (1X16 ORGANIZATION)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	29
EWEN	1	00	1	1	X	X	X	X	X	X	X	X	—	High-Z	13
ERASE	1	11	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	13
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	—	(RDY/BSY)	13
WRITE	1	01	X	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0	1	X	X	X	X	X	X	X	X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0	0	X	X	X	X	X	X	X	X	—	High-Z	13

TABLE 1-5: INSTRUCTION SET FOR 93LC76: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	22
EWEN	1	00	1	1	X	X	X	X	X	X	X	X		—	High-Z	14
ERASE	1	11	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	14
ERAL	1	00	1	0	X	X	X	X	X	X	X	X		—	(RDY/BSY)	14
WRITE	1	01	X	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0	1	X	X	X	X	X	X	X	X		D7 - D0	(RDY/BSY)	22
EWDS	1	00	0	0	X	X	X	X	X	X	X	X		—	High-Z	14

TABLE 1-6: INSTRUCTION SET FOR 93LC86: ORG=1 (X16 ORGANIZATION)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 - D0	29
EWEN	1	00	1	1	X	X	X	X	X	X	X	X	—	High-Z	13
ERASE	1	11	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	13
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	—	(RDY/BSY)	13
WRITE	1	01	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0	1	X	X	X	X	X	X	X	X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0	0	X	X	X	X	X	X	X	X	—	High-Z	13

TABLE 1-7: INSTRUCTION SET FOR 93LC86: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address											Data In	Data Out	Req. CLK Cycles
READ	1	10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	22
EWEN	1	00	1	1	X	X	X	X	X	X	X	X		—	High-Z	14
ERASE	1	11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/BSY)	14
ERAL	1	00	1	0	X	X	X	X	X	X	X	X		—	(RDY/BSY)	14
WRITE	1	01	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0	1	X	X	X	X	X	X	X	X		D7 - D0	(RDY/BSY)	22
EWDS	1	00	0	0	X	X	X	X	X	X	X	X		—	High-Z	14

2.0 PRINCIPLES OF OPERATION

When the ORG pin is connected to Vcc, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the $\overline{\text{READY/BUSY}}$ status during a programming operation. The $\overline{\text{READY/BUSY}}$ status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high impedance state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction are clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Erase/Write Enable and Disable (EWEN, EWDS)

The 93LC76/86 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.4 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

3.0 DEVICE OPERATION

3.1 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high and clock transitions continue. The memory address pointer will automatically increment and output data sequentially.

3.2 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of CLK as the last address bit (A0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 3 ms per word (Typical).

3.3 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data to be written into the specified address. The self-timed programming cycle is initiated on the rising edge of CLK as the last data bit (D0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written and the device is ready for another instruction.

The WRITE cycle takes 3 ms per word (Typical).

3.4 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't care bits, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been erased and is ready for another instruction.

The ERAL cycle takes 15 ms maximum (8 ms typical).

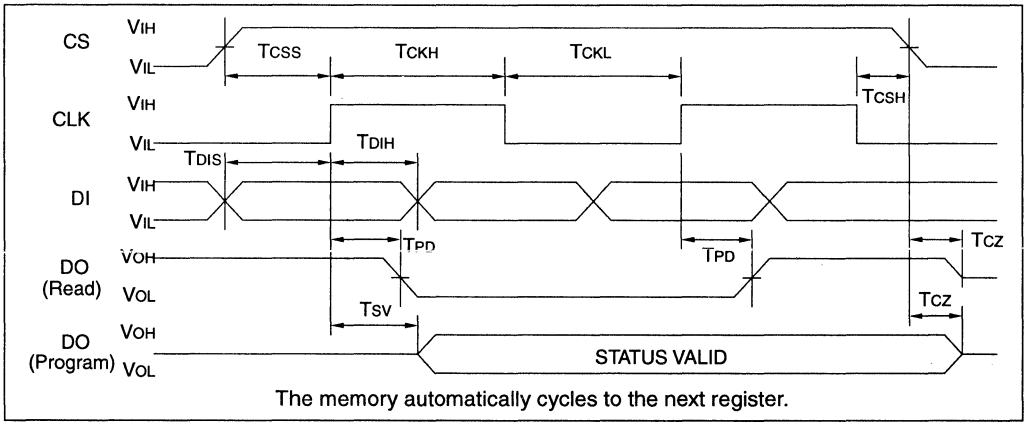
3.5 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't cares, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been written and is ready for another instruction.

The WRAL cycle takes 30 ms maximum (16 ms typical).

FIGURE 3-1: SYNCHRONOUS DATA TIMING



The memory automatically cycles to the next register.

FIGURE 3-2: READ

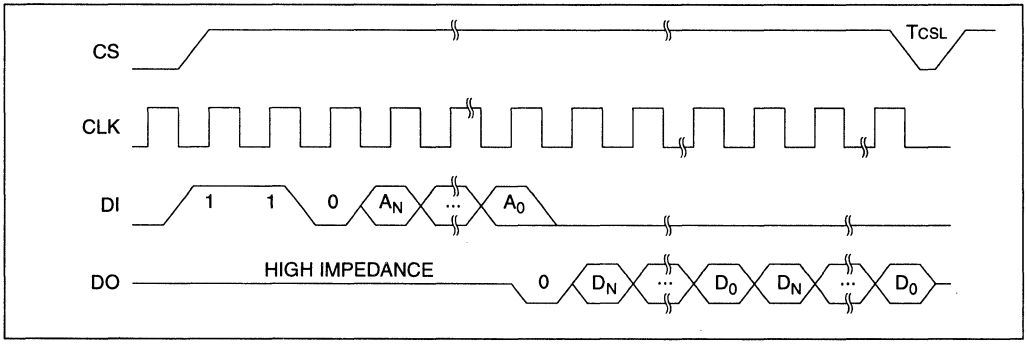


FIGURE 3-3: EWEN

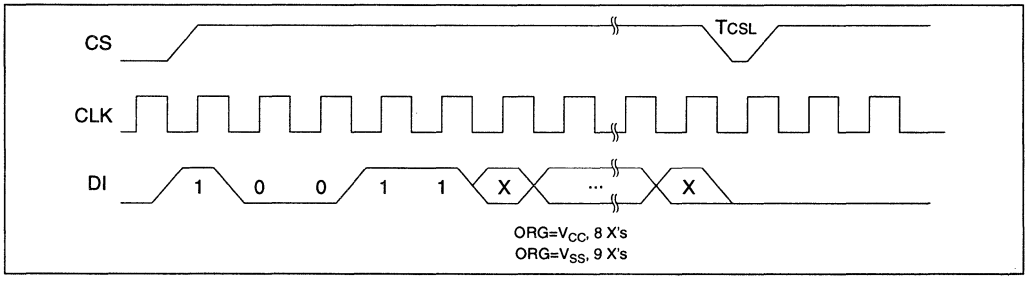


FIGURE 3-4: EWDS

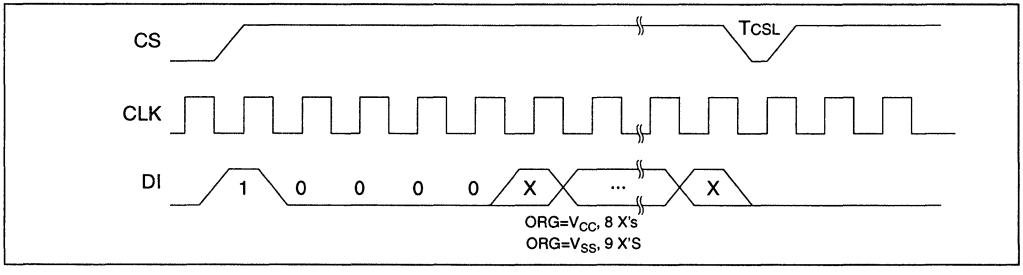


FIGURE 3-5: WRITE

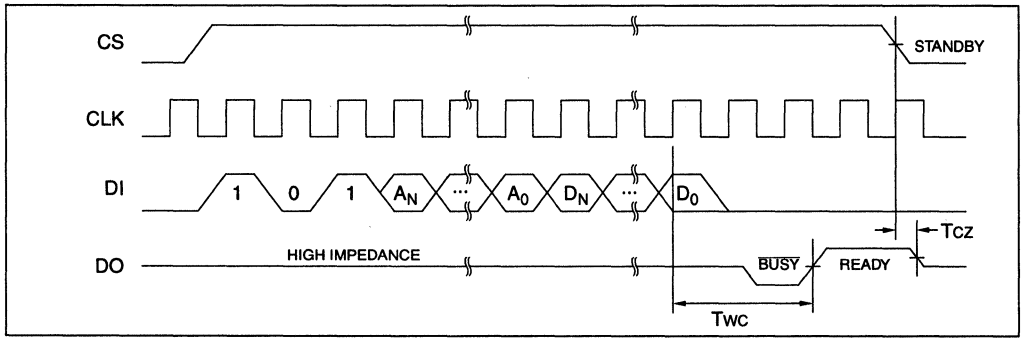


FIGURE 3-6: WRAL

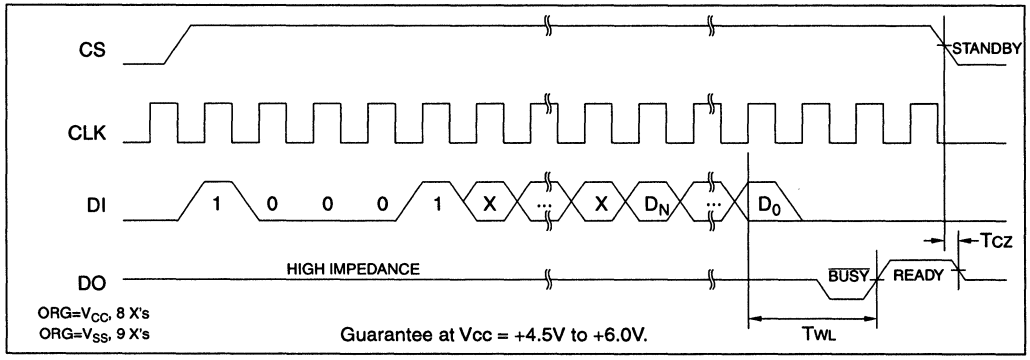


FIGURE 3-7: ERASE

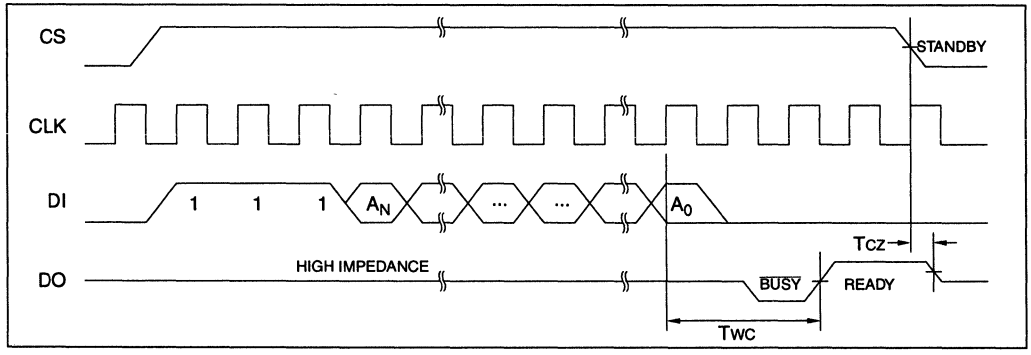
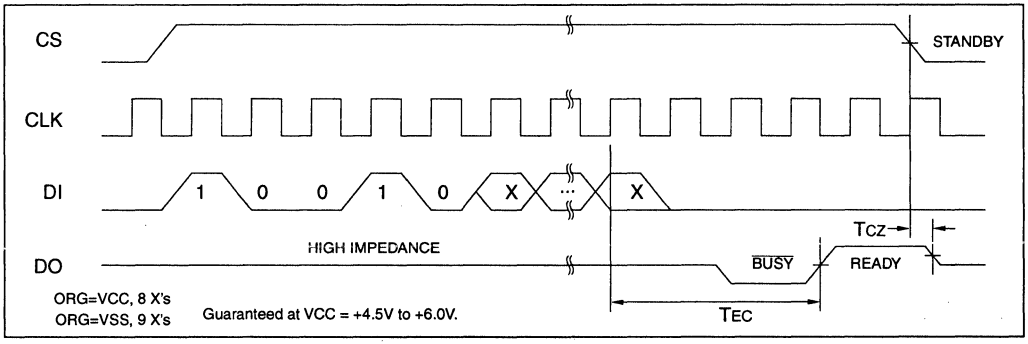


FIGURE 3-8: ERAL



4.0 PIN DESCRIPTIONS

4.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LC76/86. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all opcode, address, and data bits before an instruction is executed (see Table 1-4 through Table 1-7 for more details). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions, except when performing a sequential read (Refer to Section 3.1 for more detail on sequential reads).

4.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

4.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available when CS is high. It will be displayed until the next start bit occurs as long as CS stays high.

4.5 Organization (ORG)

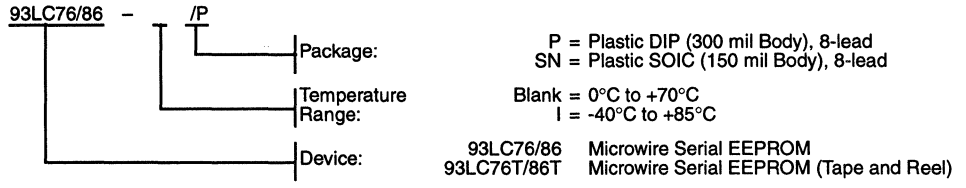
When ORG is connected to VCC, the x16 memory organization is selected. When ORG is tied to VSS, the x8 memory organization is selected. There is an internal pull-up resistor on the ORG pin that will select x16 organization when left unconnected.

4.6 Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is floated or tied to VCC, the device can be programmed. If the PE pin is tied to VSS, programming will be inhibited. There is an internal pull-up on this device that enables programming if this pin is left floating.

93LC76/86 Product Identification System

To order or obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

93C76/86

8K/16K 5.0V Microwire® Serial EEPROM

FEATURES

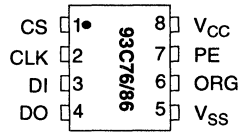
- Single 5.0V supply
- Low power CMOS technology
  - 1 mA active current typical
- ORG pin selectable memory configuration
  1024 x 8- or 512 x 16-bit organization (93C76)
  2048 x 8- or 1024 x 16-bit organization (93C86)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP/SOIC package
- Temperature ranges supported
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) -40°C to +125°C

DESCRIPTION

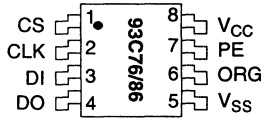
The Microchip Technology Inc. 93C76/86 are 8K and 16K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. These devices also have a Program Enable (PE) pin to allow the user to write protect the entire contents of the memory array. The 93C76/86 is available in standard 8-pin DIP and 8-pin surface mount SOIC packages.

PACKAGE TYPES

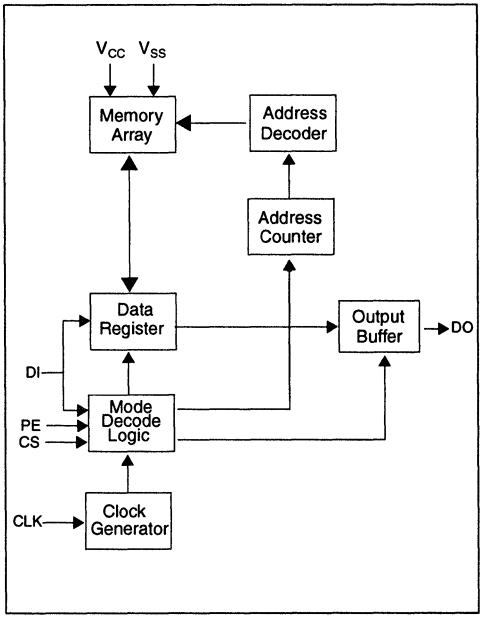
DIP Package



SOIC Package



BLOCK DIAGRAM



Microwire is a registered trademark of National Semiconductor Incorporated.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Configuration
PE	Program Enable
Vcc	Power Supply

1.2 AC Test Conditions

AC Waveform:

VLO = 2.0V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V for (Note 2)

Timing Measurement Reference Level

Input 0.5 Vcc
Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V
2: For Vcc > 4.0V

TABLE 1-2: DC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted:
Vcc = +4.5V to +5.5V
Commercial (C): Tamb = 0°C to -40°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min.	Max.	Units	Conditions
High level input voltage	VIH1	2.0	Vcc +1	V	—
Low level input voltage	VIL1	-0.3	0.8	V	—
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; Vcc = 4.5V
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc = 4.5V.
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Pin capacitance (all inputs/outputs)	CINT	—	7	pF	(Note) Tamb = +25°C, FCLK = 1 MHz
Operating current	Icc write	—	3	mA	FCLK = 2 MHz; Vcc = 5.5V
	Icc read	—	1.5	mA	FCLK = 2 MHz; Vcc = 5.5V
Standby current	Iccs	—	100	µA	CLK = CS = 0V; Vcc = 5.5V DI = PE = Vss ORG = Vss or Vcc

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted:
V_{CC} = +4.5V to +5.5V
Commercial (C): Tamb = 0°C to -40°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min.	Max.	Units	Conditions
Clock frequency	F_{CLK}	—	2	MHz	$V_{CC} \geq 4.5V$
Clock high time	T_{CKH}	300	—	ns	
Clock low time	T_{CKL}	200	—	ns	
Chip select setup time	T_{CSS}	50	—	ns	Relative to CLK
Chip select hold time	T_{CSH}	0	—	ns	
Chip select low time	T_{CSL}	250	—	ns	Relative to CLK
Data input setup time	T_{DIS}	100	—	ns	Relative to CLK
Data input hold time	T_{DIH}	100	—	ns	Relative to CLK
Data output delay time	T_{PD}	—	400	ns	C_L = 100 pF
Data output disable time	T_{CZ}	—	100	ns	(Note 1)
Status valid time	T_{SV}	—	500	ns	C_L = 100 pF
Program cycle time	T_{WC}	—	10	ms	ERASE/WRITE mode (Note 2)
	T_{EC}	—	15	ms	ERAL mode
	T_{WL}	—	30	ms	WRAL mode
Endurance	—	1M	—	cycles	25°C, V_{CC} = 5.0V, Block Mode (Note 3)

Note 1: This parameter is periodically sampled and not 100% tested.
2: Typical program cycle is 4 ms per word.
3: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

TABLE 1-4: INSTRUCTION SET FOR 93C76: ORG=1 (X16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	X A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	X A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

TABLE 1-5: INSTRUCTION SET FOR 93C76: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X X	—	High-Z	14
ERASE	1	11	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	X A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X X	—	High-Z	14

TABLE 1-6: INSTRUCTION SET FOR 93C86: ORG=1 (X16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	29
EWEN	1	00	1 1 X X X X X X X X	—	High-Z	13
ERASE	1	11	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	13
ERAL	1	00	1 0 X X X X X X X X	—	(RDY/BSY)	13
WRITE	1	01	A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	29
WRAL	1	00	0 1 X X X X X X X X	D15 - D0	(RDY/BSY)	29
EWDS	1	00	0 0 X X X X X X X X	—	High-Z	13

TABLE 1-7: INSTRUCTION SET FOR 93C86: ORG=0 (X8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	22
EWEN	1	00	1 1 X X X X X X X X X	—	High-Z	14
ERASE	1	11	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	14
ERAL	1	00	1 0 X X X X X X X X X	—	(RDY/BSY)	14
WRITE	1	01	A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	22
WRAL	1	00	0 1 X X X X X X X X X	D7 - D0	(RDY/BSY)	22
EWDS	1	00	0 0 X X X X X X X X X	—	High-Z	14

2.0 PRINCIPLES OF OPERATION

When the ORG pin is connected to Vcc, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The READY/$\overline{\text{BUSY}}$ status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high impedance state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction are clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Erase/Write Enable and Disable (EWEN, EWDS)

The 93C76/86 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

2.4 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

3.0 DEVICE OPERATION

3.1 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high and clock transitions continue. The memory address pointer will automatically increment and output data sequentially.

3.2 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of CLK as the last address bit (A0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 3 ms per word (Typical).

3.3 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data to be written into the specified address. The self-timed programming cycle is initiated on the rising edge of CLK as the last data bit (D0) is clocked in. At this point, the CLK, CS, and DI inputs become don't cares.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written and the device is ready for another instruction.

The WRITE cycle takes 3 ms per word (Typical).

3.4 Erase All (ERAL)

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't care bits, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at Vcc = +4.5V to +5.5V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been erased and is ready for another instruction.

The ERAL cycle takes 15 ms maximum (8 ms typical).

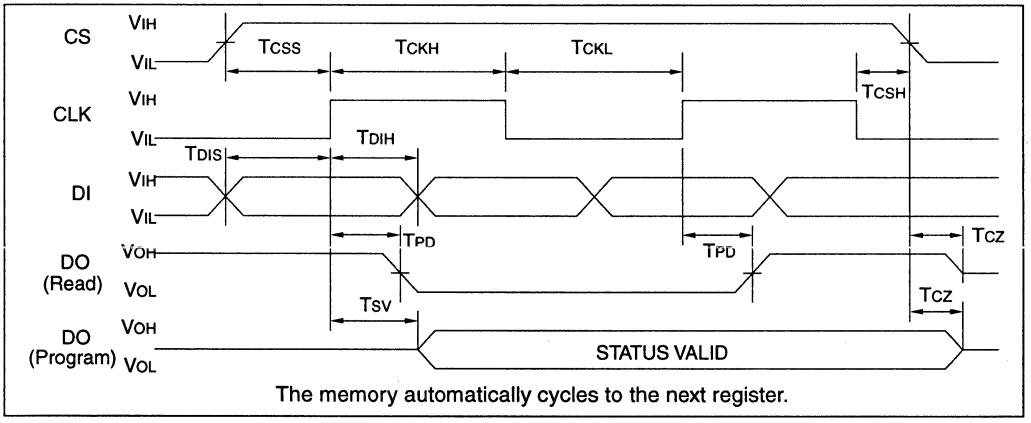
3.5 Write All (WRAL)

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences on the rising edge of the last address bit (A0). Note that the least significant 8 or 9 address bits are don't cares, depending on selection of x16 or x8 mode. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at Vcc = +4.5V to +5.5V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if the CS is high. The READY/$\overline{\text{BUSY}}$ status will be displayed on the DO pin until the next start bit is received as long as CS is high. Bringing the CS low will place the device in standby mode and cause the DO pin to enter the high impedance state. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the entire device has been written and is ready for another instruction.

The WRAL cycle takes 30 ms maximum (16 ms typical).

FIGURE 3-1: SYNCHRONOUS DATA TIMING



The memory automatically cycles to the next register.

FIGURE 3-2: READ

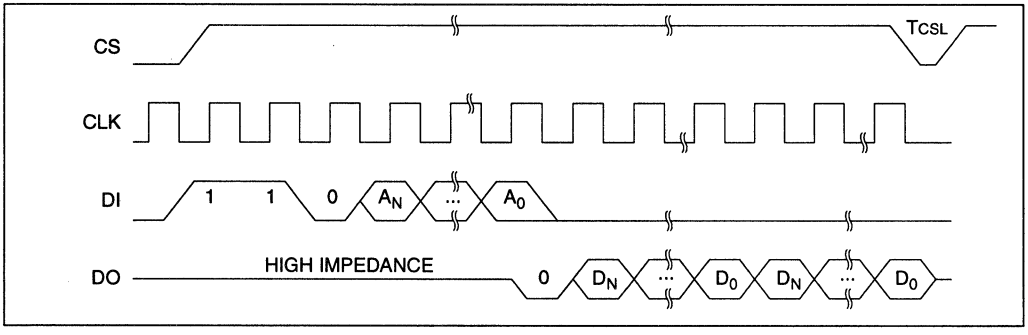


FIGURE 3-3: EWEN

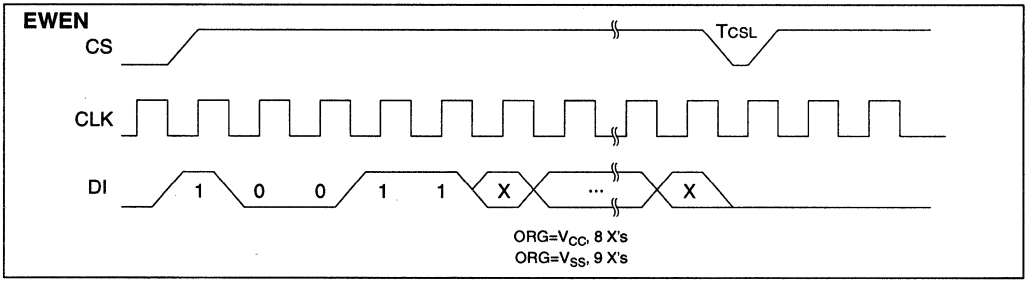


FIGURE 3-4: EWDS

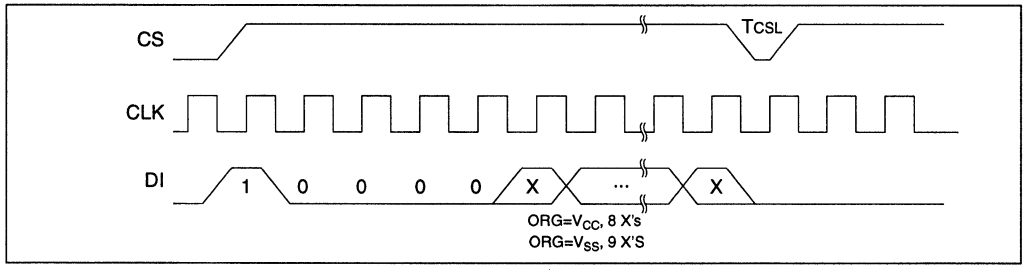


FIGURE 3-5: WRITE

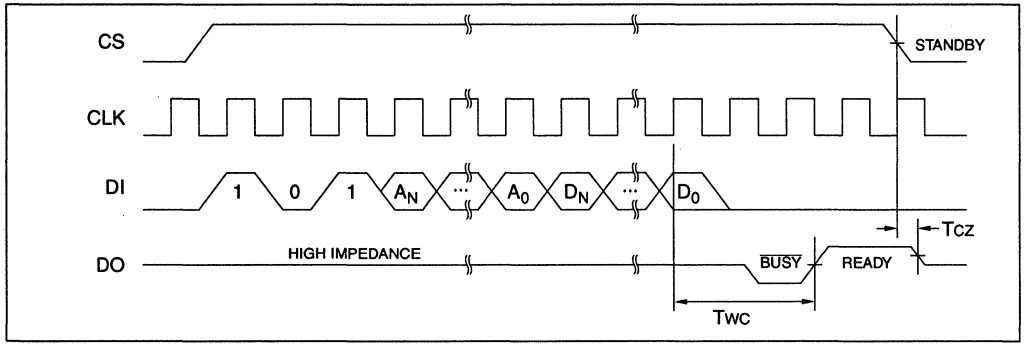


FIGURE 3-6: WRAL

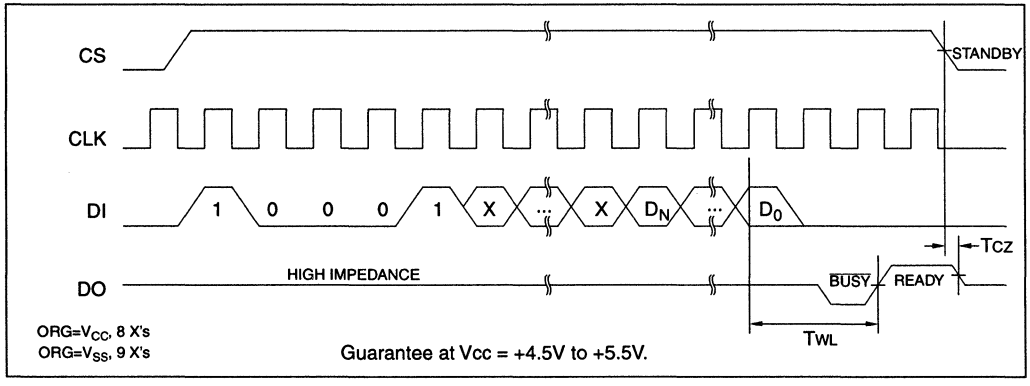


FIGURE 3-7: ERASE

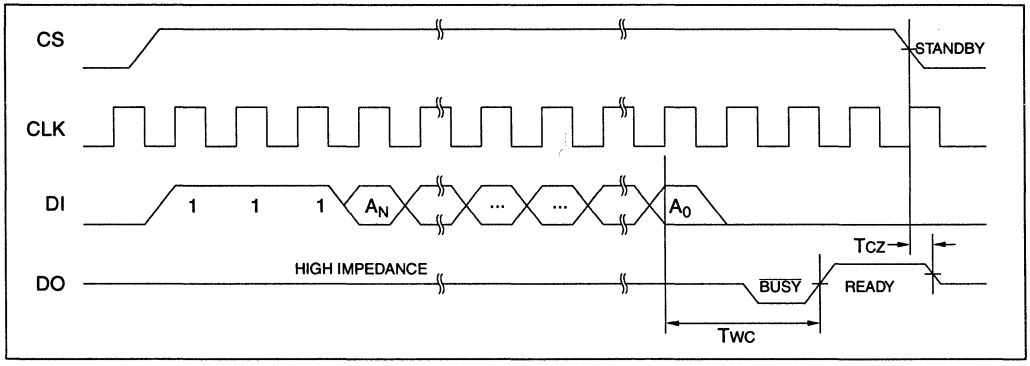
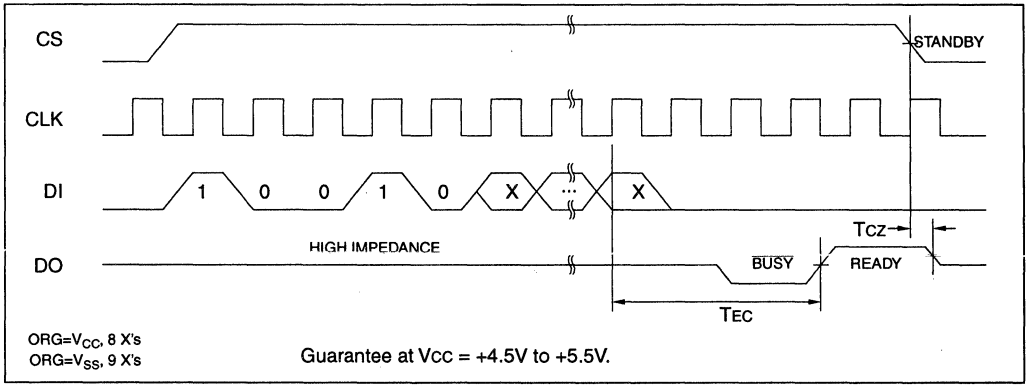


FIGURE 3-8: ERAL



4.0 PIN DESCRIPTIONS

4.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C76/86. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all opcode, address, and data bits before an instruction is executed (see Table 1-4 through Table 1-7 for more details). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions, except when performing a sequential read (Refer to Section 3.1 for more detail on sequential reads).

4.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

4.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available when CS is high. It will be displayed until the next start bit occurs as long as CS stays high.

4.5 Organization (ORG)

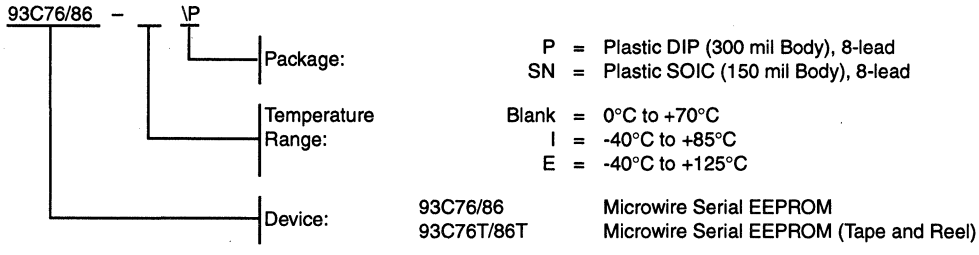
When ORG is connected to Vcc, the x16 memory organization is selected. When ORG is tied to Vss, the x8 memory organization is selected. There is an internal pull-up resistor on the ORG pin that will select x16 organization when left unconnected.

4.6 Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is floated or tied to Vcc, the device can be programmed. If the PE pin is tied to Vss, programming will be inhibited. There is an internal pull-up on this device that enables programming if this pin is left floating.

93C76/86 Product Identification System

To order or obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

SECTION 5
SPI™ SERIAL EEPROM
PRODUCT SPECIFICATIONS

25AA040	4K SPI™ Bus Serial EEPROM	5-1
25LC040	4K SPI™ Bus Serial EEPROM	5-1
25C040	4K SPI™ Bus Serial EEPROM	5-1
25AA080	8K SPI™ Bus Serial EEPROM	5-13
25LC080	8K SPI™ Bus Serial EEPROM	5-13
25C080	8K SPI™ Bus Serial EEPROM	5-13
25AA160	16K SPI™ Bus Serial EEPROM	5-25
25LC160	16K SPI™ Bus Serial EEPROM	5-25
25C160	16K SPI™ Bus Serial EEPROM	5-25
25LC320	32K SPI™ Bus Serial EEPROM	5-37
25C320	32K SPI™ Bus Serial EEPROM	5-37
25AA640	64K SPI™ Bus Serial EEPROM	5-49
25LC640	64K SPI™ Bus Serial EEPROM	5-49
25C640	64K SPI™ Bus Serial EEPROM	5-49

SPI is a trademark of Motoroloa Corporation.

25AA040/25LC040/25C040

4K SPI™ Bus Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
25AA040	1.8-5.5V	1 MHz	C,I
25LC040	2.5-5.5V	2 MHz	C,I
25C040	4.5-5.5V	3 MHz	C,I,E

FEATURES

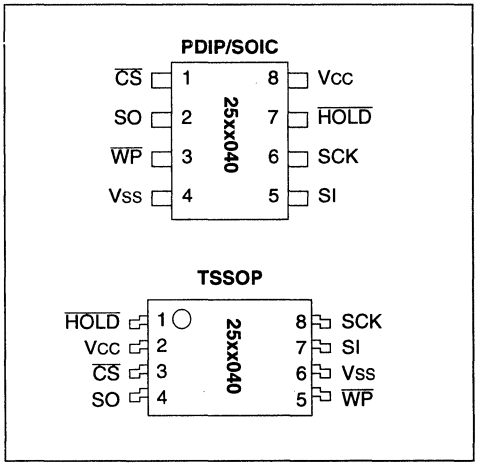
- Low power CMOS technology
  - Write current: 3 mA typical
  - Read current: 500 µA typical
  - Standby current: 500 nA typical
- 512 x 8 bit organization
- 16 byte page
- Write cycle time: 5ms max.
- Self-timed ERASE and WRITE cycles
- Block write protection
  - Protect none, 1/4, 1/2, or all of array
- Built-in write protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write protect pin
- Sequential read
- High reliability
  - Endurance: 1M cycles (guaranteed)
  - Data retention: > 200 years
  - ESD protection: > 4000 V
- 8-pin PDIP, SOIC, and TSSOP packages
- Temperature ranges supported:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) (25C040): -40°C to +125°C

DESCRIPTION

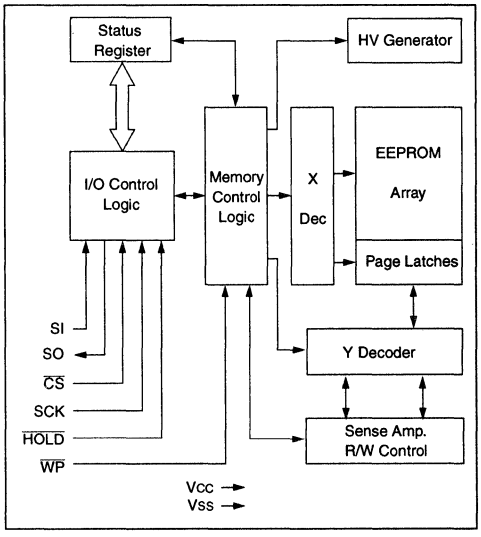
The Microchip Technology Inc. 25AA040/25LC040/25C040 (25xx040*) is a 4K bit serial Electrically Erasable PROM. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select (CS) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts. Also, write operations to the device can be disabled via the write protect pin (WP).

PACKAGE TYPES



BLOCK DIAGRAM



*25xx040 is used in this document as a generic part number for the 25AA040/25LC040/25C040 devices.
SPI is a trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

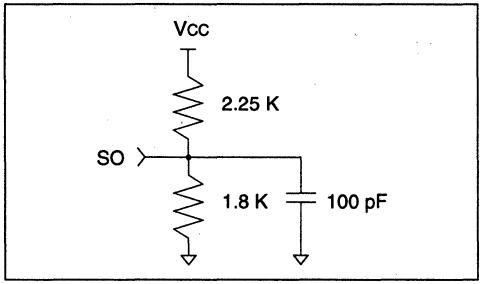
Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc+1.0V
Storage temperature ..... -65°C to 150°C
Ambient temperature under bias ..... -65°C to 125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins 4kV

***Notice:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Pin
Vss	Ground
Vcc	Supply Voltage
$\overline{HOLD}$	Hold Input

FIGURE 1-2: AC TEST CIRCUIT



1.2 AC Test Conditions

AC Waveform:
VLO = 0.2V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V (Note 2)
Timing Measurement Reference Level
Input 0.5 Vcc
Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V
2: For Vcc > 4.0V

TABLE 1-3: DC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): TAMB = 0°C to +70°C Vcc = 1.8V to 5.5V Industrial (I): TAMB = -40°C to +85°C Vcc = 1.8V to 5.5V Automotive (E): TAMB = -40°C to +125°C Vcc = 4.5V to 5.5V (25C040 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
High level input voltage	VIH1	2.0	Vcc+1	V	Vcc ≥ 2.7V (Note)
	VIH2	0.7 Vcc	Vcc+1	V	Vcc< 2.7V (Note)
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.7V (Note)
	VIL2	-0.3	0.3 Vcc	V	Vcc < 2.7V (Note)
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
	VOL	—	0.2	V	IOL = 1.0 mA, Vcc < 2.5V
High level output voltage	VOH	Vcc -0.5	—	V	IOH =-400 µA
Input leakage current	ILI	-10	10	µA	$\overline{CS}$ = Vcc, VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	$\overline{CS}$ = Vcc, VOUT = Vss to Vcc
Internal Capacitance (all inputs and outputs)	CINT	—	7	pF	TAMB = 25°C, CLK = 1.0 MHz, Vcc = 5.0V (Note)
Operating Current	ICC Read	— —	1 500	mA µA	Vcc = 5.5V; FCLK=3.0 MHz; SO = Open Vcc = 2.5V; FCLK=2.0 MHz; SO = Open
	ICC Write	— —	5 3	mA mA	Vcc= 5.5V Vcc = 2.5V
Standby Current	ICCS	— —	5 2	µA µA	$\overline{CS}$ = Vcc = 5.5V, Inputs tied to Vcc or Vss $\overline{CS}$ = Vcc = 2.5V, Inputs tied to Vcc or Vss

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-4: AC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): Tamb = 0°C to +70°C Vcc = 1.8V to 5.5V Industrial (I): Tamb = -40°C to +85°C Vcc = 1.8V to 5.5V Automotive (E): Tamb = -40°C to +125°C Vcc = 4.5V to 5.5V (25C040 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
Clock Frequency	FCLK	—	3	MHz	Vcc = 4.5V to 5.5V
		—	2	MHz	Vcc = 2.5V to 4.5V
		—	1	MHz	Vcc = 1.8V to 2.5V
$\overline{CS}$ Setup Time	TCSS	100	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		500	—	ns	Vcc = 1.8V to 2.5V
$\overline{CS}$ Hold Time	TCSH	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
$\overline{CS}$ Disable Time	TCSD	500	—	ns	
Data Setup Time	TSU	30	—	ns	Vcc = 4.5V to 5.5V
		50	—	ns	Vcc = 2.5V to 4.5V
		50	—	ns	Vcc = 1.8V to 2.5V
Data Hold Time	THD	50	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		100	—	ns	Vcc = 1.8V to 2.5V
CLK Rise Time	TR	—	2	µs	(Note 1)
CLK Fall Time	TF	—	2	µs	(Note 1)
Clock High Time	THI	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
Clock Low Time	TLO	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
Clock Delay Time	TCLD	50	—	ns	
Clock Enable Time	TCLE	50	—	ns	
Output Valid from Clock Low	TV	—	150	ns	Vcc = 4.5V to 5.5V
		—	250	ns	Vcc = 2.5V to 4.5V
		—	475	ns	Vcc = 1.8V to 2.5V
Output Hold Time	THO	0	—	ns	(Note 1)
Output Disable Time	TDIS	—	200	ns	Vcc = 4.5V to 5.5V (Note 1)
		—	250	ns	Vcc = 2.5V to 4.5V (Note 1)
		—	500	ns	Vcc = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ Setup Time	THS	100	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
$\overline{HOLD}$ Hold Time	THH	100	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
$\overline{HOLD}$ Low to Output High-Z	THZ	100	—	ns	Vcc = 4.5V to 5.5V (Note 1)
		150	—	ns	Vcc = 2.5V to 4.5V (Note 1)
		200	—	ns	Vcc = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ High to Output Valid	THV	100	—	ns	Vcc = 4.5V to 5.5V
		150	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
Internal Write Cycle Time	TWC	—	5	ms	
Endurance	—	1M	—	E/W Cycles	(Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-5: HOLD TIMING

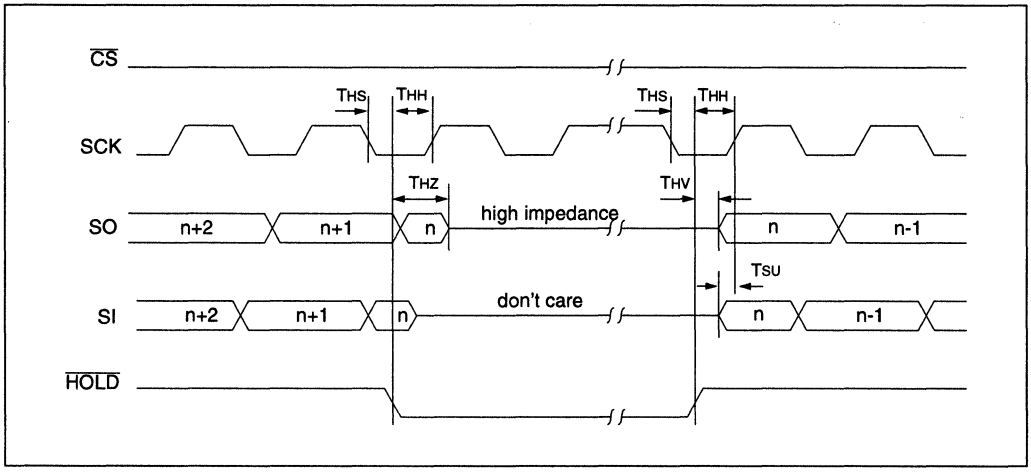


FIGURE 1-6: SERIAL INPUT TIMING

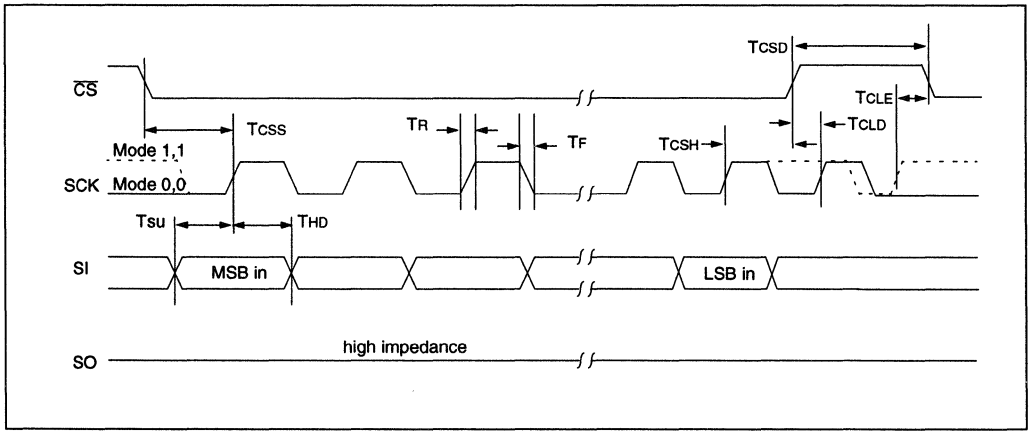
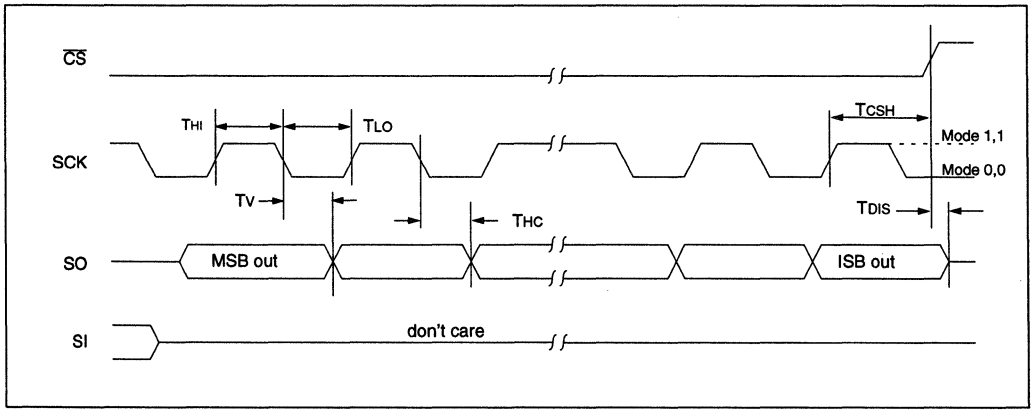


FIGURE 1-7: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in standby mode as soon as the programming cycle is complete. As soon as the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. A low to high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.3 Serial Output (SO)

The SO pin is used to transfer data out of the 25xx040. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25xx040. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.5 Write Protect ($\overline{WP}$)

This pin is a hardware write protect input pin. When $\overline{WP}$ is low, all writes to the array or status register are disabled, but any other operation functions normally. When $\overline{WP}$ is high, all functions, including non-volatile writes operate normally. $\overline{WP}$ going low at any time will reset the write enable latch and inhibit programming, except when an internal write has already begun. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write. See Table 3-7 for Write Protect Functionaiity Matrix.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25xx040 while in the middle of a serial sequence without having to re-transmit the entire sequence over at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high to low transition. The 25xx040 must remain selected during this sequence. The SI, SCK, and SO pins are in a high impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 PRINCIPLES OF OPERATION

The 25xx040 is a 512 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25xx040 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation. The $\overline{WP}$ pin must be held high to allow writing to the memory array.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. The most significant address bit (A8) is located in the instruction byte. All instructions, addresses, and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25xx040 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction with the A8 address bit is transmitted to the 25xx040 followed by the lower 8-bit address (A7 through A0). After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-2).

3.3 Write Sequence

Prior to any attempt to write data to the 25xx040, the write enable latch must be set by issuing the WREN instruction (Figure 3-5). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25xx040. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a write instruction, followed by the address, and then the data to be written. Keep in mind that the most significant address bit (A8) is included in the instruction byte. Up to 16 bytes of data can be sent to the 25xx040 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXXX 0000 and ends with XXXX 1111. If the internal address counter reaches XXXX 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-3 and Figure 3-4 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the status register may be read to check the status of the WIP, WEL, BP1, and BP0 bits (Figure 3-8). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 $A_8$011	Read data from memory array beginning at selected address
WRITE	0000 $A_8$010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

Note: A_8 is the 9^{th} address bit necessary to fully address 512 bytes.

FIGURE 3-2: READ SEQUENCE

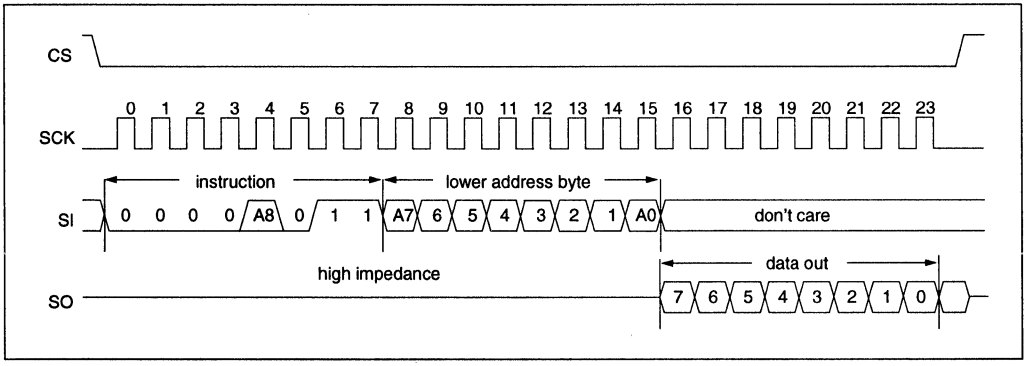


FIGURE 3-3: BYTE WRITE SEQUENCE

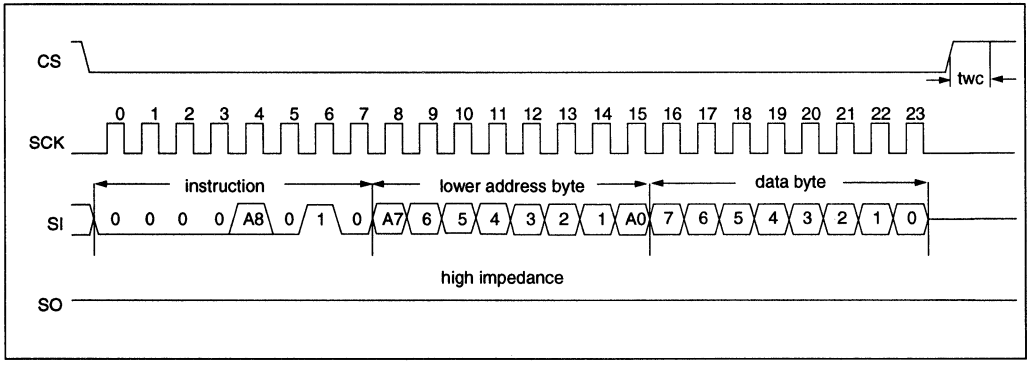
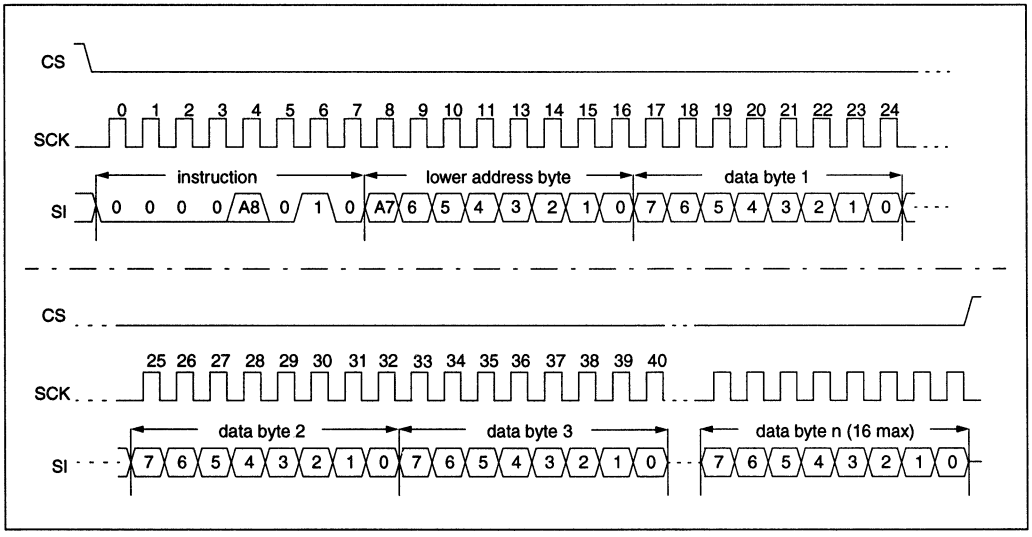


FIGURE 3-4: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25xx040 contains a write enable latch. See Table 3-10 for the Write Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- $\overline{WP}$ line is low

FIGURE 3-5: WRITE ENABLE SEQUENCE

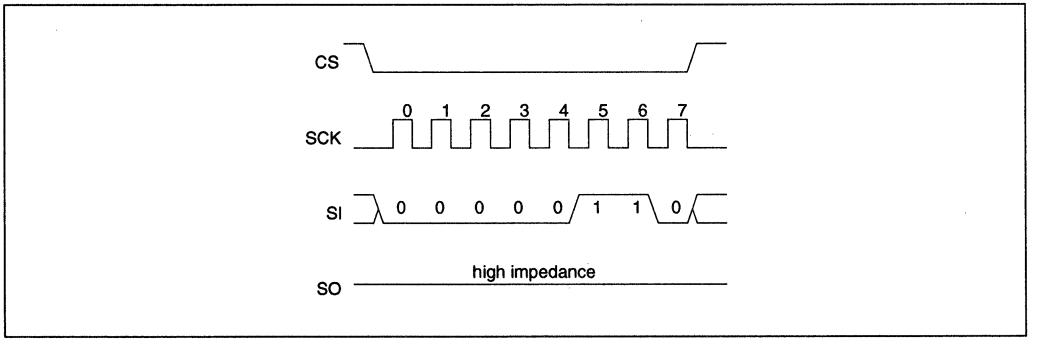
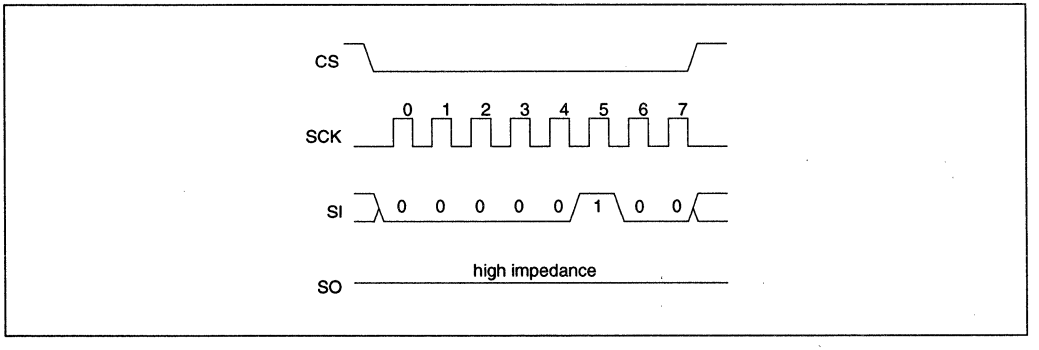


FIGURE 3-6: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the 25xx040 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array, when set to a '0' the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

See Figure 3-8 for RDSR timing sequence

3.6 Write Status Register(WRSR)

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-7.

See Figure 3-9 for WRSR timing sequence

TABLE 3-7: ARRAY PROTECTION

BP1	BP0	Array Addresses Write Protected
0	0	none
0	1	upper 1/4 (0180h - 01FFh)
1	0	upper 1/2 (0100h - 01FFh)
1	1	all (0000h - 01FFh)

FIGURE 3-8: READ STATUS REGISTER SEQUENCE

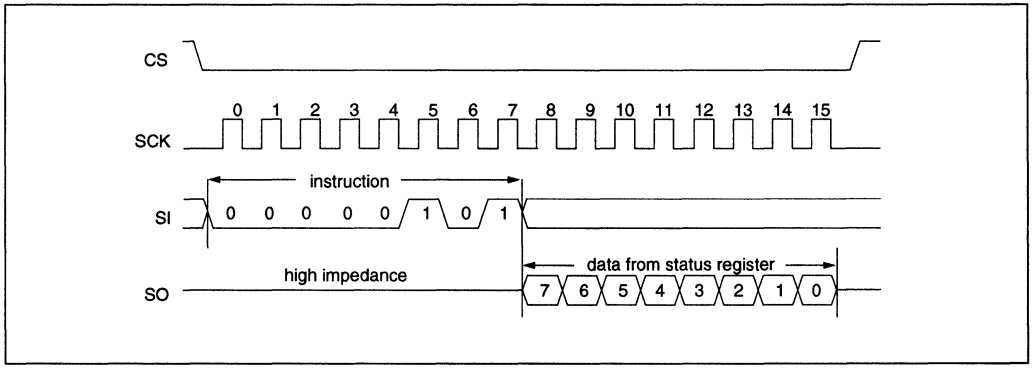
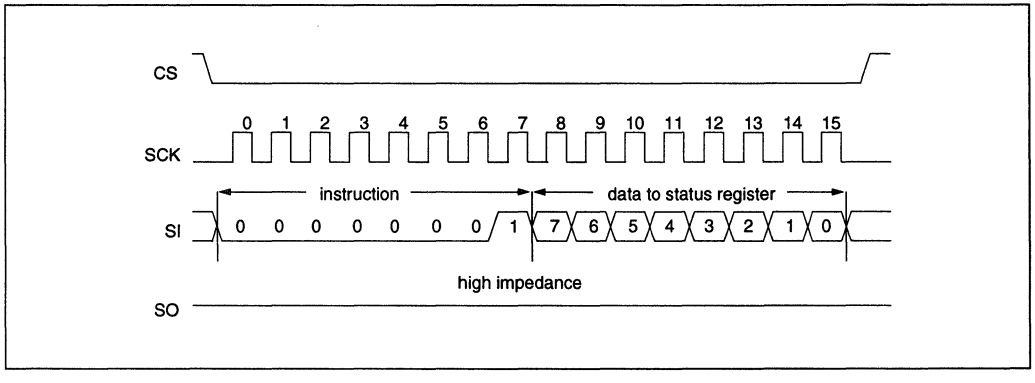


FIGURE 3-9: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up.
- A write enable instruction must be issued to set the write enable latch.
- After a byte write, page write, or status register write, the write enable latch is reset.
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle.
- Access to the array during an internal write cycle is ignored and programming is continued.
- The write enable latch is reset when the $\overline{WP}$ pin is low.

3.8 Power On State

The 25xx040 powers on in the following state:

- The device is in low power standby mode ($\overline{CS}$ = 1).
- The write enable latch is reset.
- SO is in high impedance state.
- A low level on $\overline{CS}$ is required to enter active state.

TABLE 3-10: WRITE PROTECT FUNCTIONALITY MATRIX

WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
Low	X	Protected	Protected	Protected
High	0	Protected	Protected	Protected
High	1	Protected	Writable	Writable

NOTES:

25AA040/25LC040/25C040 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

25xx040 — /P

Package:

P	= Plastic DIP (300 mil Body), 8-lead
SN	= Plastic SOIC (150 mil Body), 8-lead
ST	= TSSOP, 8-lead

Temperature Range:

Blank	= 0°C to +70°C
I	= –40°C to +85°C
E	= –40°C to +125°C

Devices:

25AA040	4096 bit 1.8V SPI Serial EEPROM
25AA040T	4096 bit 1.8V SPI Serial EEPROM Tape and Reel
25AA040X	4096 bit 1.8V SPI Serial EEPROM in alternate pinout (ST only)
25AA040XT	4096 bit 1.8V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25LC040	4096 bit 2.5V SPI Serial EEPROM
25LC040T	4096 bit 2.5V SPI Serial EEPROM Tape and Reel
25LC040X	4096 bit 2.5V SPI Serial EEPROM in alternate pinout (ST only)
25LC040XT	4096 bit 2.5V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25C040	4096 bit 5.0V SPI Serial EEPROM
25C040T	4096 bit 5.0V SPI Serial EEPROM Tape and Reel
25C040X	4096 bit 5.0V SPI Serial EEPROM in alternate pinout (ST only)
25C040XT	4096 bit 5.0V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP 25AA080/25LC080/25C080

8K SPI™ Bus Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
25C080	4.5-5.5V	3 MHz	C,I,E
25LC080	2.5-5.5V	2 MHz	C,I
25AA080	1.8-5.5V	1 MHz	C,I

FEATURES

- Low power CMOS technology
  - Write current: 3 mA maximum
  - Read current: 500 µA typical
  - Standby current: 500 nA typical
- 1024 x 8 bit organization
- 16 byte page
- Write cycle time: 5ms max.
- Self-timed ERASE and WRITE cycles
- Block write protection
  - Protect none, 1/4, 1/2, or all of array
- Built-in write protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write protect pin
- Sequential read
- High reliability
  - Endurance: 1M cycles (guaranteed)
  - Data retention: > 200 years
  - ESD protection: > 4000 V
- 8-pin PDIP and SOIC
- Temperature ranges supported:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) (25C080): -40°C to +125°C

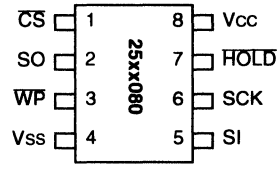
DESCRIPTION

The Microchip Technology Inc. 25AA080/25LC080/25C080 (25xx080*) are 8K bit serial Electrically Erasable PROMs. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input.

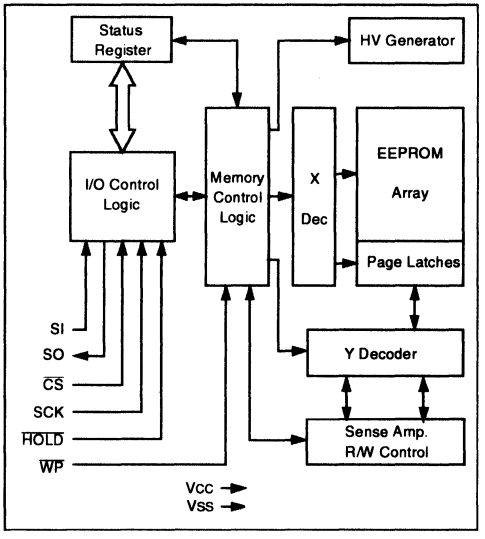
Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts.

PACKAGE TYPES

PDIP/SOIC



BLOCK DIAGRAM



*25xx080 is used in this document as a generic part number for the 25AA080/25LC080/25C080 devices.
SPI is a trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

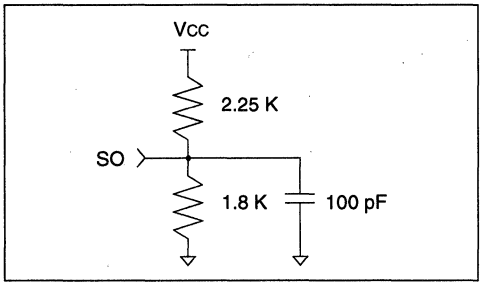
Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc+1.0V
Storage temperature ..... -65°C to 150°C
Ambient temperature under bias ..... -65°C to 125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins 4kV

***Notice:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Pin
Vss	Ground
Vcc	Supply Voltage
$\overline{HOLD}$	Hold Input

FIGURE 1-2: AC TEST CIRCUIT



1.2 AC Test Conditions

AC Waveform:
VLO = 0.2V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V (Note 2)
Timing Measurement Reference Level
Input 0.5 Vcc
Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V
2: For Vcc > 4.0V

TABLE 1-3: DC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): TAMB = 0°C to +70°C Vcc = 1.8V to 5.5V Industrial (I): TAMB = -40°C to +85°C Vcc = 1.8V to 5.5V Automotive (E): TAMB = -40°C to +125°C Vcc = 4.5V to 5.5V (25C080 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
High level input voltage	VIH1	2.0	Vcc+1	V	Vcc ≥ 2.7V (Note)
	VIH2	0.7 Vcc	Vcc+1	V	Vcc< 2.7V (Note)
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.7V (Note)
	VIL2	-0.3	0.3 Vcc	V	Vcc < 2.7V (Note)
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
	VOL	—	0.2	V	IOL = 1.0 mA, Vcc < 2.5V
High level output voltage	VOH	Vcc -0.5	—	V	IOH =-400 µA
Input leakage current	ILI	-10	10	µA	$\overline{CS}$ = Vcc, VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	$\overline{CS}$ = Vcc, VOUT = Vss to Vcc
Internal Capacitance (all inputs and outputs)	CINT	—	7	pF	TAMB = 25°C, CLK = 1.0 MHz, Vcc = 5.0V (Note)
Operating Current	Icc Read	— —	1 500	mA µA	Vcc = 5.5V; FCLK=3.0 MHz; SO = Open Vcc = 2.5V; FCLK=2.0 MHz; SO = Open
	Icc Write	— —	5 3	mA mA	Vcc= 5.5V Vcc = 2.5V
Standby Current	Iccs	— —	5 1	µA µA	$\overline{CS}$ = Vcc = 5.5V, Inputs tied to Vcc or Vss $\overline{CS}$ = Vcc = 2.5V, Inputs tied to Vcc or Vss

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-4: AC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): Tamb = 0°C to +70°C Vcc = 1.8V to 5.5V Industrial (I): Tamb = -40°C to +85°C Vcc = 1.8V to 5.5V Automotive (E): Tamb = -40°C to +125°C Vcc = 4.5V to 5.5V (25C080 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
Clock Frequency	FCLK	—	3	MHz	VCC = 4.5V to 5.5V
		—	2	MHz	VCC = 2.5V to 4.5V
		—	1	MHz	VCC = 1.8V to 2.5V
$\overline{CS}$ Setup Time	TCSS	100	—	ns	VCC = 4.5V to 5.5V
		250	—	ns	VCC = 2.5V to 4.5V
		500	—	ns	VCC = 1.8V to 2.5V
$\overline{CS}$ Hold Time	TCSH	150	—	ns	VCC = 4.5V to 5.5V
		250	—	ns	VCC = 2.5V to 4.5V
		475	—	ns	VCC = 1.8V to 2.5V
$\overline{CS}$ Disable Time	TCSD	500	—	ns	
Data Setup Time	TSU	30	—	ns	VCC = 4.5V to 5.5V
		50	—	ns	VCC = 2.5V to 4.5V
		50	—	ns	VCC = 1.8V to 2.5V
Data Hold Time	THD	50	—	ns	VCC = 4.5V to 5.5V
		100	—	ns	VCC = 2.5V to 4.5V
		100	—	ns	VCC = 1.8V to 2.5V
CLK Rise Time	TR	—	2	µs	(Note 1)
CLK Fall Time	TF	—	2	µs	(Note 1)
Clock High Time	THI	150	—	ns	VCC = 4.5V to 5.5V
		250	—	ns	VCC = 2.5V to 4.5V
		475	—	ns	VCC = 1.8V to 2.5V
Clock Low Time	TLO	150	—	ns	VCC = 4.5V to 5.5V
		250	—	ns	VCC = 2.5V to 4.5V
		475	—	ns	VCC = 1.8V to 2.5V
Clock Delay Time	TCLD	50	—	ns	
Clock Enable Time	TCLE	50	—	ns	
Output Valid from Clock Low	TV	—	150	ns	VCC = 4.5V to 5.5V
		—	250	ns	VCC = 2.5V to 4.5V
		—	475	ns	VCC = 1.8V to 2.5V
Output Hold Time	THO	0	—	ns	(Note 1)
Output Disable Time	TDIS	—	200	ns	VCC = 4.5V to 5.5V (Note 1)
		—	250	ns	VCC = 2.5V to 4.5V (Note 1)
		—	500	ns	VCC = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ Setup Time	THS	100	—	ns	VCC = 4.5V to 5.5V
		100	—	ns	VCC = 2.5V to 4.5V
		200	—	ns	VCC = 1.8V to 2.5V
$\overline{HOLD}$ Hold Time	THH	100	—	ns	VCC = 4.5V to 5.5V
		100	—	ns	VCC = 2.5V to 4.5V
		200	—	ns	VCC = 1.8V to 2.5V
$\overline{HOLD}$ Low to Output High-Z	THZ	100	—	ns	VCC = 4.5V to 5.5V (Note 1)
		150	—	ns	VCC = 2.5V to 4.5V (Note 1)
		200	—	ns	VCC = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ High to Output Valid	THV	100	—	ns	VCC = 4.5V to 5.5V
		150	—	ns	VCC = 2.5V to 4.5V
		200	—	ns	VCC = 1.8V to 2.5V
Internal Write Cycle Time	TWC	—	5	ms	
Endurance	—	1M	—	E/W Cycles	(Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-5: HOLD TIMING

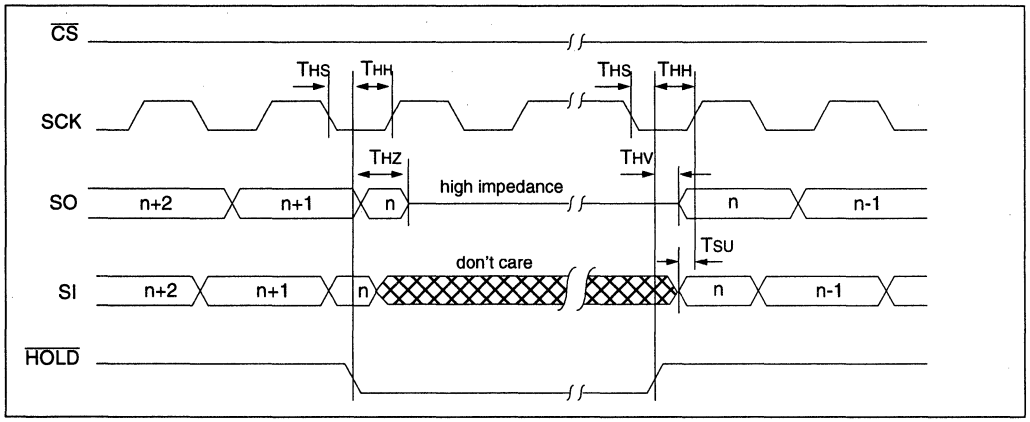


FIGURE 1-6: SERIAL INPUT TIMING

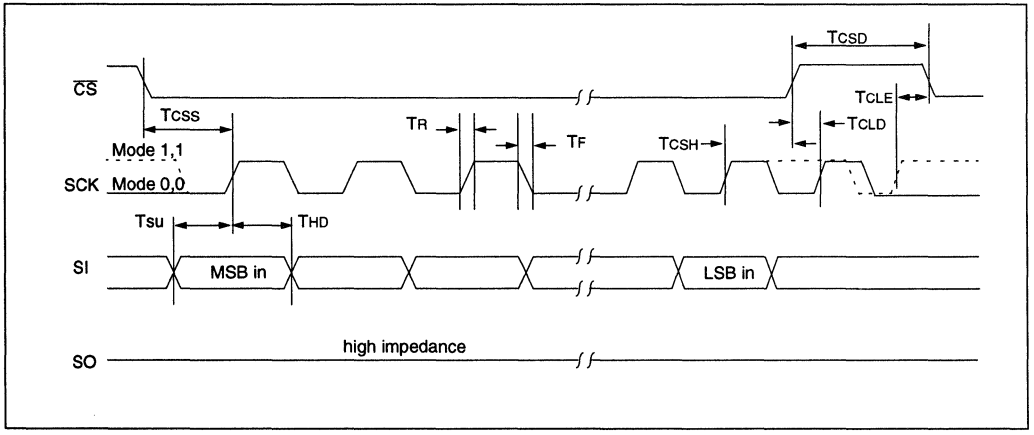
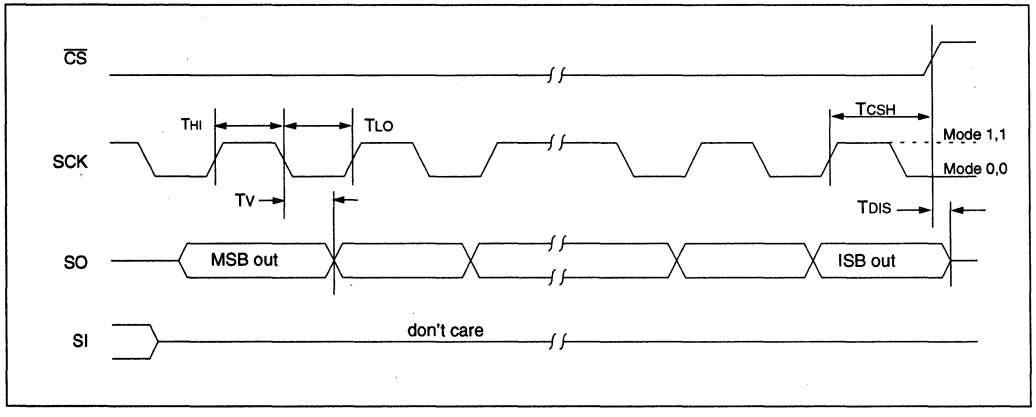


FIGURE 1-7: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in standby mode as soon as the programming cycle is complete. As soon as the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. A low to high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.3 Serial Output (SO)

The SO pin is used to transfer data out of the 25xx080. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25xx080. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.5 Write Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the status register to prohibit writes to the non-volatile bits in the status register. When $\overline{WP}$ is low and WPEN is high, writing to the non-volatile bits in the status register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the non-volatile bits in the status register operate normally. If the WPEN bit is set, $\overline{WP}$ low during a status register write sequence will disable writing to the status register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is low. This allows the user to install the 25xx080 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25xx080 while in the middle of a serial sequence without having to re-transmit the entire sequence over at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high to low transition. The 25xx080 must remain selected during this sequence. The SI, SCK, and SO pins are in a high impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 PRINCIPLES OF OPERATION

The 25xx080 are 1024 byte Serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25xx080 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation. The $\overline{WP}$ pin must be held high to allow writing to the memory array.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25xx080 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the 25xx080 followed by the 16-bit address, with the six MSBs of the address being don't care bits. After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (03FFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-2).

3.3 Write Sequence

Prior to any attempt to write data to the 25xx080, the write enable latch must be set by issuing the WREN instruction (Figure 3-5). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25xx080. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a write instruction, followed by the 16-bit address, with the six MSBs of the address being don't care bits, and then the data to be written. Up to 16 bytes of data can be sent to the 25xx080 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXXX XXXX XXXX 0000 and ends with XXXX XXXX XXXX 1111. If the internal address counter reaches XXXX XXXX XXXX 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-3 and Figure 3-4 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the status register may be read to check the status of the WPEN, WIP, WEL, BP1, and BP0 bits (Figure 3-7). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

FIGURE 3-2: READ SEQUENCE

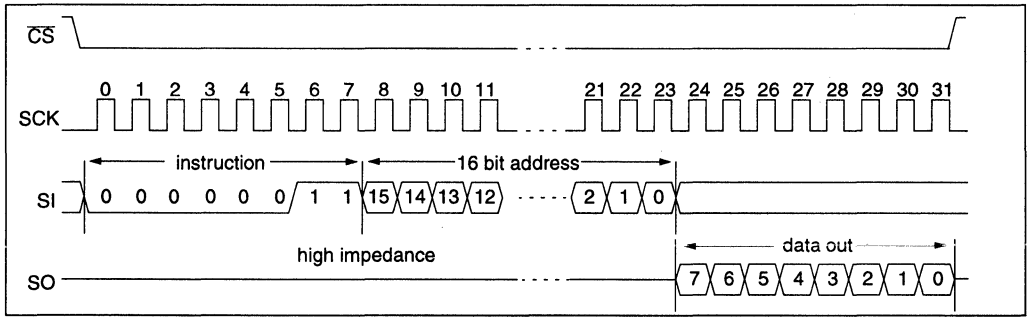


FIGURE 3-3: BYTE WRITE SEQUENCE

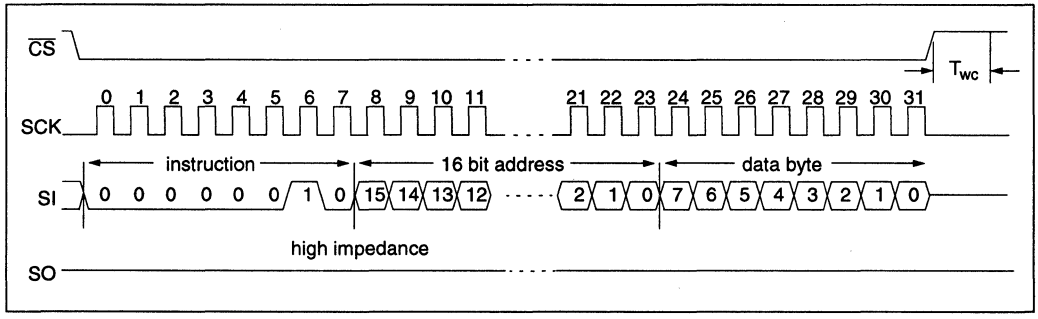
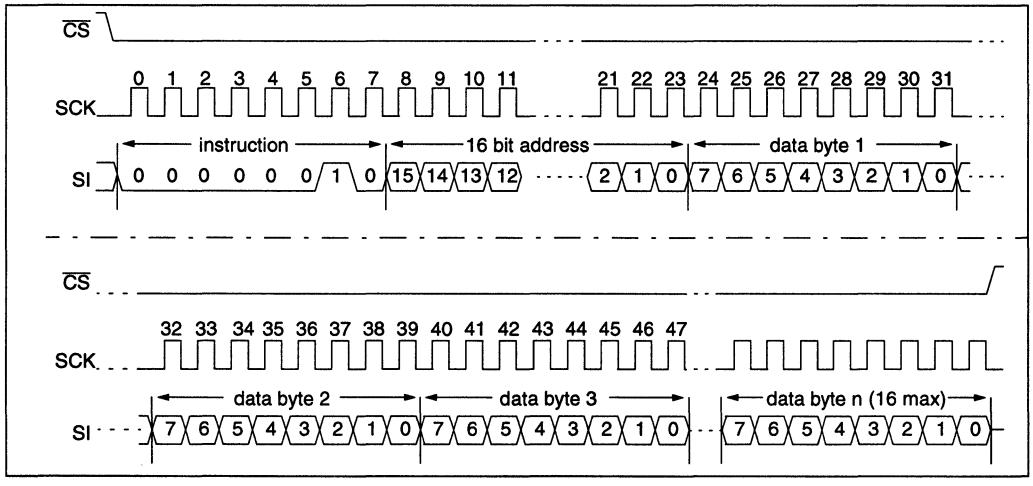


FIGURE 3-4: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25xx080 contains a write enable latch. See Table 3-10 for the Write Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 3-5: WRITE ENABLE SEQUENCE

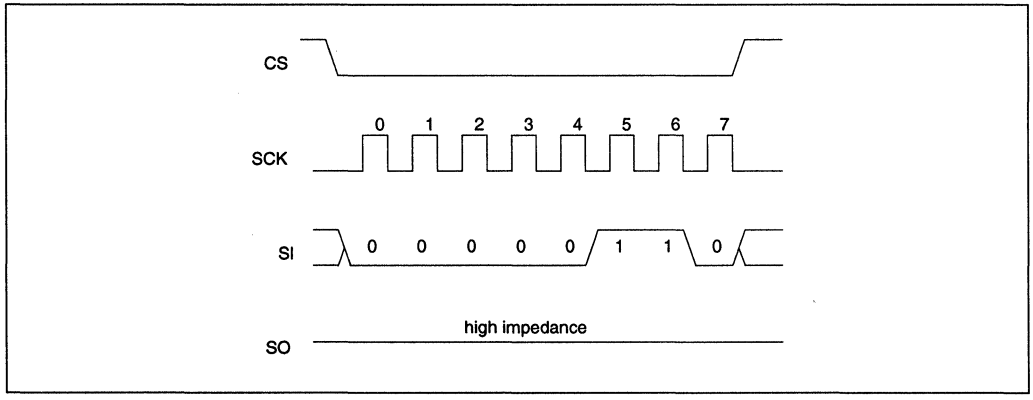
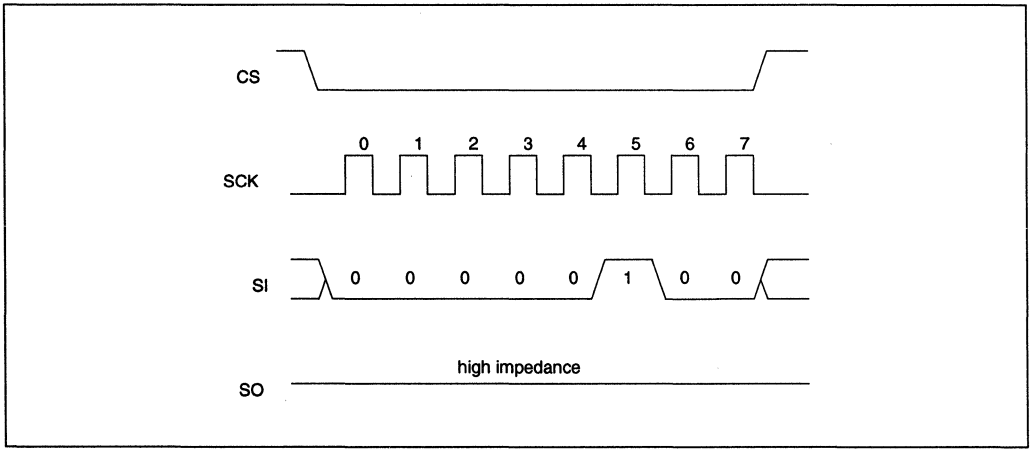


FIGURE 3-6: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

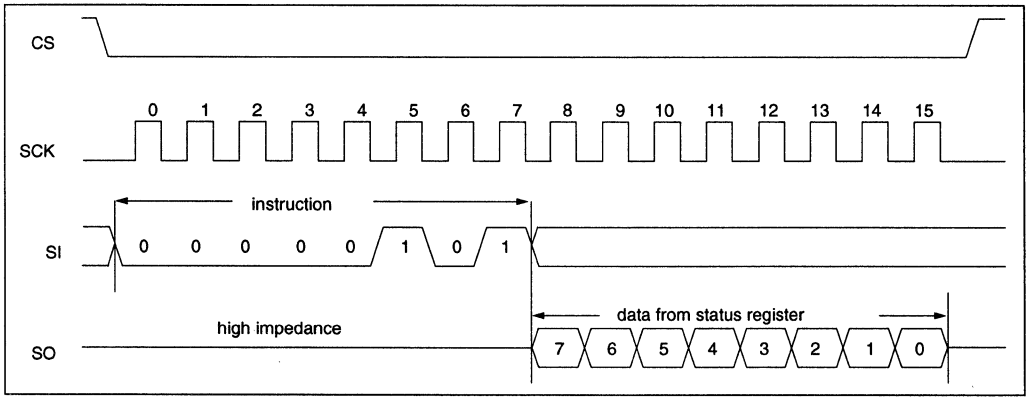
The **Write-In-Process (WIP)** bit indicates whether the 25xx080 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array, when set to a '0' the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

See Figure 3-7 for the RDSR timing sequence.

FIGURE 3-7: READ STATUS REGISTER SEQUENCE



3.6 Write Status Register(WRSR)

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-8.

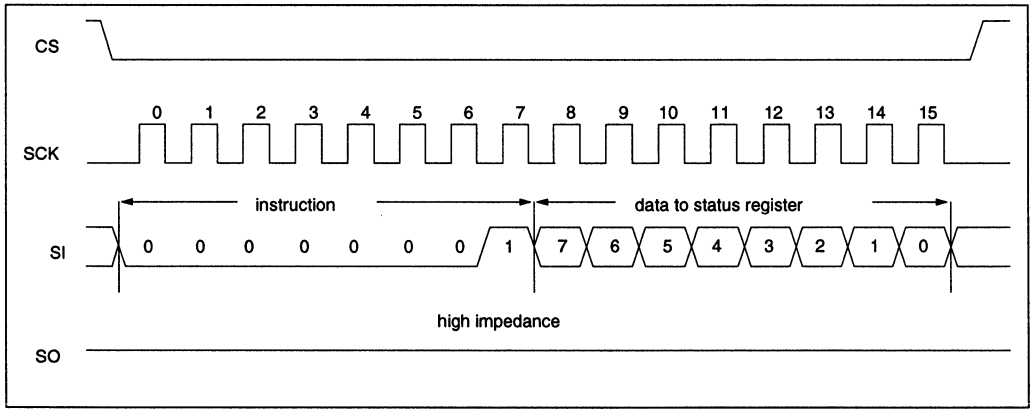
The Write Protect Enable (WPEN) bit is a non-volatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write Protect ($\overline{WP}$) pin and the Write Protect Enable (WPEN) bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write protected, only writes to non-volatile bits in the status register are disabled. See Table 3-3 for a matrix of functionality on the WPEN bit.

See Figure 3-9 for the WRSR timing sequence.

TABLE 3-8: ARRAY PROTECTION

BP1	BP0	Array Addresses Write Protected
0	0	none
0	1	upper 1/4 (0300h - 03FFh)
1	0	upper 1/2 (0200h - 03FFh)
1	1	all (0000h - 03FFh)

FIGURE 3-9: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up.
- A write enable instruction must be issued to set the write enable latch.
- After a byte write, page write, or status register write, the write enable latch is reset.
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle.
- Access to the array during an internal write cycle is ignored and programming is continued.

3.8 Power On State

The 25xx080 powers on in the following state:

- The device is in low power standby mode ($\overline{CS}$ = 1).
- The write enable latch is reset.
- SO is in high impedance state.
- A high to low level transition on $\overline{CS}$ is required to enter active state.

TABLE 3-10: WRITE PROTECT FUNCTIONALITY MATRIX

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	1	Protected	Writable	Protected
X	High	1	Protected	Writable	Writable

25AA080/25LC080/25C080 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

25xx080 — /P

Package:

P	= Plastic DIP (300 mil Body), 8-lead
SN	= Plastic SOIC (150 mil Body), 8-lead

Temperature Range:

Blank	= 0°C to +70°C
I	= –40°C to +85°C
E	= –40°C to +125°C

Devices:

25AA080	8K bit 1.8V SPI Serial EEPROM
25AA080T	8K bit 1.8V SPI Serial EEPROM Tape and Reel
25LC080	8K bit 2.5V SPI Serial EEPROM
25LC080T	8K bit 2.5V SPI Serial EEPROM Tape and Reel
25C080	8K bit 5.0V SPI Serial EEPROM
25C080T	8K bit 5.0V SPI Serial EEPROM Tape and Reel

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP 25AA160/25LC160/25C160

16K SPI™ Bus Serial EEPROM

DEVICE SELECTION TABLE

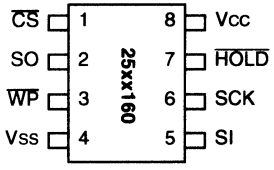
Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
25C160	4.5-5.5V	3 MHz	C,I,E
25LC160	2.5-5.5V	2 MHz	C,I
25AA160	1.8-5.5V	1 MHz	C,I

FEATURES

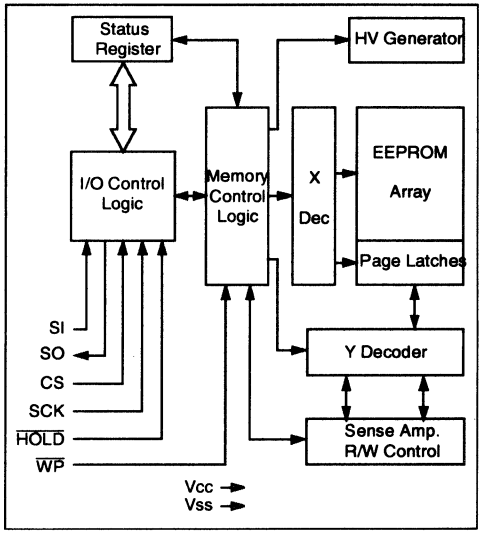
- Low power CMOS technology
  - Write current: 3 mA maximum
  - Read current: 500 µA typical
  - Standby current: 500 nA typical
- 2048 x 8 bit organization
- 16 byte page
- Write cycle time: 5ms max.
- Self-timed ERASE and WRITE cycles
- Block write protection
  - Protect none, 1/4, 1/2, or all of array
- Built-in write protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write protect pin
- Sequential read
- High reliability
  - Endurance: 1M cycles (guaranteed)
  - Data retention: > 200 years
  - ESD protection: > 4000 V
- 8-pin PDIP and SOIC packages
- Temperature ranges supported:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) (25C160): -40°C to +125°C

PACKAGE TYPES

PDIP/SOIC



BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 25AA160/25LC160/25C160 (25xx160*) are 16K bit serial Electrically Erasable PROMs. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select (CS) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts.

*25xx160 is used in this document as a generic part number for the 25AA160/25LC160/25C160 devices.
SPI is a trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

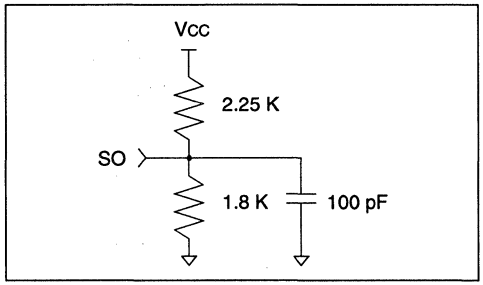
Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc+1.0V
Storage temperature ..... -65°C to 150°C
Ambient temperature under bias ..... -65°C to 125°C
Soldering temperature of leads (10 seconds) ....., +300°C
ESD protection on all pins 4kV

***Notice:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Pin
Vss	Ground
Vcc	Supply Voltage
$\overline{HOLD}$	Hold Input

FIGURE 1-1: AC TEST CIRCUIT



1.2 AC Test Conditions

AC Waveform:
VLO = 0.2V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V (Note 2)
Timing Measurement Reference Level
Input 0.5 Vcc
Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V
2: For Vcc > 4.0V

TABLE 1-2: DC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): TAMB = 0°C to +70°C Vcc = 1.8V to 5.5V Industrial (I): TAMB = -40°C to +85°C Vcc = 1.8V to 5.5V Automotive (E): TAMB = -40°C to +125°C Vcc = 4.5V to 5.5V (25C160 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
High level input voltage	VIH1	2.0	Vcc+1	V	Vcc ≥ 2.7V (Note)
	VIH2	0.7 Vcc	Vcc+1	V	Vcc< 2.7V (Note)
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.7V (Note)
	VIL2	-0.3	0.3 Vcc	V	Vcc < 2.7V (Note)
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
	VOL	—	0.2	V	IOL = 1.0 mA, Vcc < 2.5V
High level output voltage	VOH	Vcc -0.5	—	V	IOH =-400 µA
Input leakage current	ILI	-10	10	µA	$\overline{CS}$ = Vcc, VIN = Vss TO Vcc
Output leakage current	ILO	-10	10	µA	$\overline{CS}$ = Vcc, VOUT = Vss TO Vcc
Internal Capacitance (all inputs and outputs)	CINT	—	7	pF	TAMB = 25°C, CLK = 1.0 MHz, Vcc = 5.0V (Note)
Operating Current	Icc Read	— —	1 500	mA µA	Vcc = 5.5V; FCLK=3.0 MHz; SO = Open Vcc = 2.5V; FCLK=2.0 MHz; SO = Open
	Icc Write	— —	5 3	mA mA	Vcc= 5.5V Vcc = 2.5V
Standby Current	Iccs	— —	5 1	µA µA	$\overline{CS}$ = Vcc = 5.5V, Inputs tied to Vcc or Vss $\overline{CS}$ = Vcc = 2.5V, Inputs tied to Vcc or Vss

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): Industrial (I): Automotive (E):	Tamb = 0°C to +70°C Tamb = -40°C to +85°C Tamb = -40°C to +125°C		Vcc = 1.8V to 5.5V Vcc = 1.8V to 5.5V Vcc = 4.5V to 5.5V (25C160 only)	
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
Clock Frequency	FCLK	—	3	MHz	Vcc = 4.5V to 5.5V
		—	2	MHz	Vcc = 2.5V to 4.5V
		—	1	MHz	Vcc = 1.8V to 2.5V
$\overline{CS}$ Setup Time	TCSS	100	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		500	—	ns	Vcc = 1.8V to 2.5V
$\overline{CS}$ Hold Time	TCSH	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
$\overline{CS}$ Disable Time	TCSD	500	—	ns	
Data Setup Time	TSU	30	—	ns	Vcc = 4.5V to 5.5V
		50	—	ns	Vcc = 2.5V to 4.5V
		50	—	ns	Vcc = 1.8V to 2.5V
Data Hold Time	THD	50	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		100	—	ns	Vcc = 1.8V to 2.5V
CLK Rise Time	TR	—	2	µs	(Note 1)
CLK Fall Time	TF	—	2	µs	(Note 1)
Clock High Time	THI	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
Clock Low Time	TLO	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
Clock Delay Time	TCLD	50	—	ns	
Clock Enable Time	TCLE	50	—	ns	
Output Valid from Clock Low	TV	—	150	ns	Vcc = 4.5V to 5.5V
		—	250	ns	Vcc = 2.5V to 4.5V
		—	475	ns	Vcc = 1.8V to 2.5V
Output Hold Time	THO	0	—	ns	(Note 1)
Output Disable Time	TDIS	—	200	ns	Vcc = 4.5V to 5.5V (Note 1)
		—	250	ns	Vcc = 2.5V to 4.5V (Note 1)
		—	500	ns	Vcc = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ Setup Time	THS	100	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
$\overline{HOLD}$ Hold Time	THH	100	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
$\overline{HOLD}$ Low to Output High-Z	THZ	100	—	ns	Vcc = 4.5V to 5.5V (Note 1)
		150	—	ns	Vcc = 2.5V to 4.5V (Note 1)
		200	—	ns	Vcc = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ High to Output Valid	THV	100	—	ns	Vcc = 4.5V to 5.5V
		150	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
Internal Write Cycle Time	TWC	—	5	ms	
Endurance	—	1M	—	E/W Cycles	(Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on ourwebsite.

FIGURE 1-2: HOLD TIMING

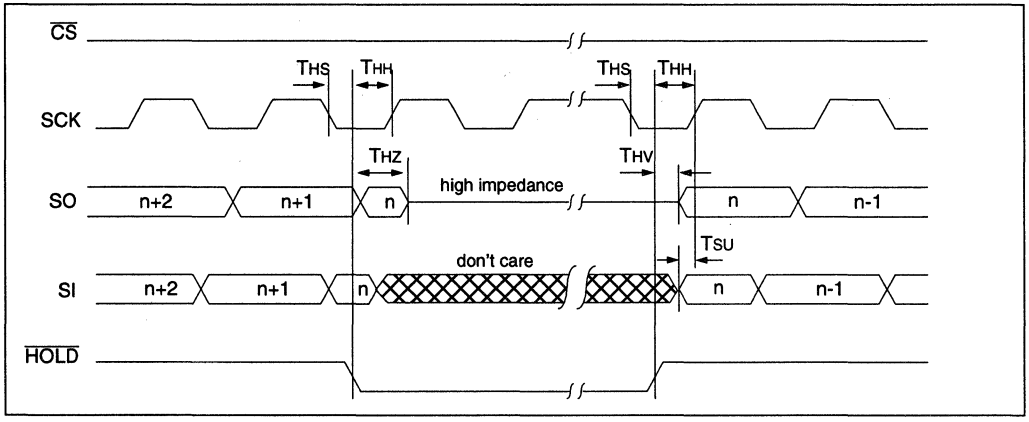


FIGURE 1-3: SERIAL INPUT TIMING

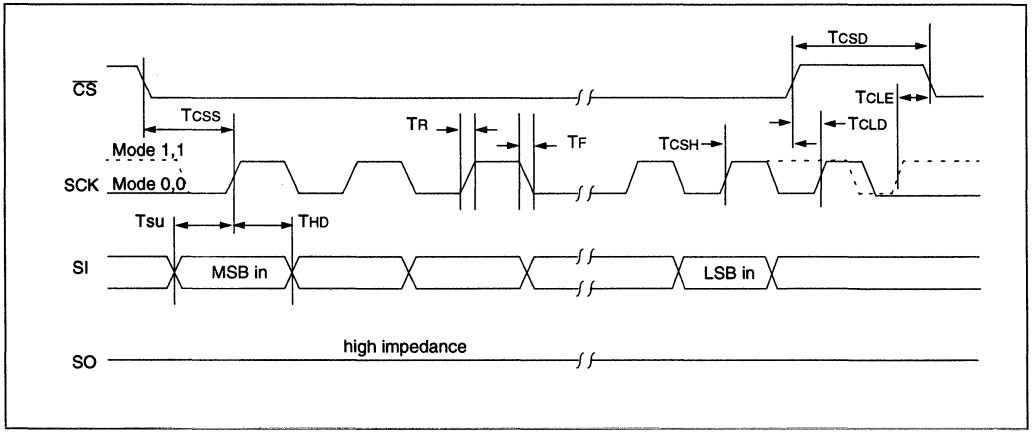
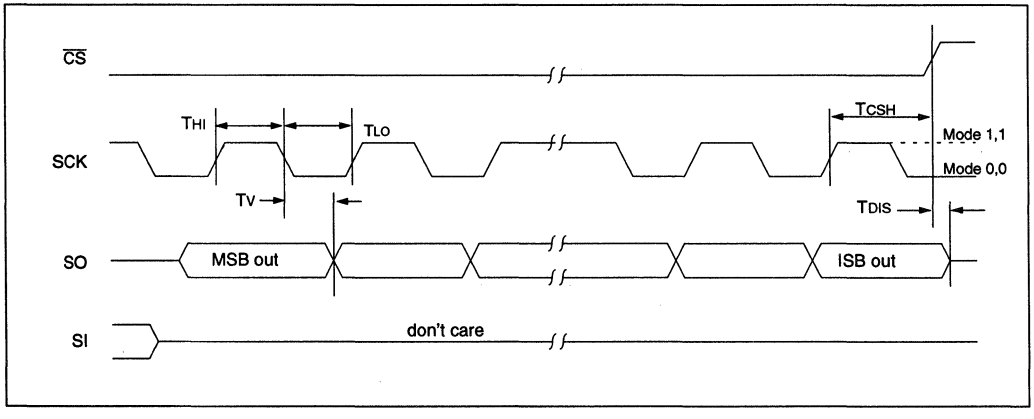


FIGURE 1-4: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in standby mode as soon as the programming cycle is complete. As soon as the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. A low to high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.3 Serial Output (SO)

The SO pin is used to transfer data out of the 25xx160. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25xx160. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.5 Write Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the status register to prohibit writes to the non-volatile bits in the status register. When $\overline{WP}$ is low and WPEN is high, writing to the non-volatile bits in the status register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the non-volatile bits in the status register operate normally. If the WPEN bit is set, $\overline{WP}$ low during a status register write sequence will disable writing to the status register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is low. This allows the user to install the 25xx160 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25xx160 while in the middle of a serial sequence without having to re-transmit the entire sequence over at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high to low transition. The 25xx160 must remain selected during this sequence. The SI, SCK, and SO pins are in a high impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 PRINCIPLES OF OPERATION

The 25xx160 are 2048 byte Serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25xx160 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation. The $\overline{WP}$ pin must be held high to allow writing to the memory array.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25xx160 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the 25xx160 followed by the 16-bit address, with the five MSBs of the address being don't care bits. After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (07FFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25xx160, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25xx160. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a write instruction, followed by the 16-bit address, with the five MSBs of the address being don't care bits, and then the data to be written. Up to 16 bytes of data can be sent to the 25xx160 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXXX XXXX XXXX 0000 and ends with XXXX XXXX XXXX 1111. If the internal address counter reaches XXXX XXXX XXXX 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the status register may be read to check the status of the WPEN, WIP, WEL, BP1, and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

FIGURE 3-1: READ SEQUENCE

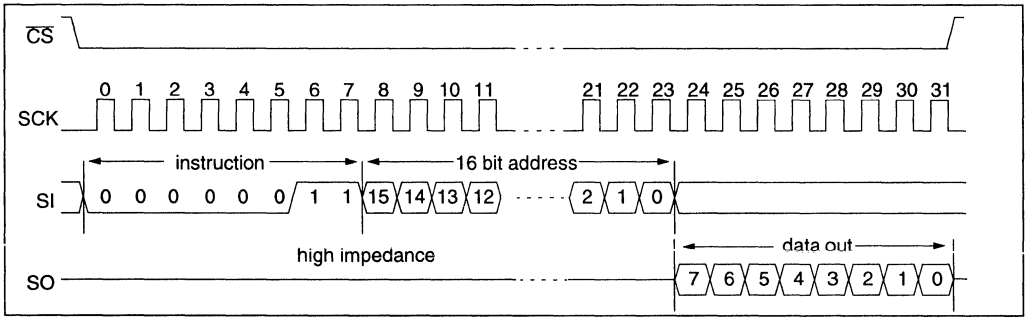


FIGURE 3-2: BYTE WRITE SEQUENCE

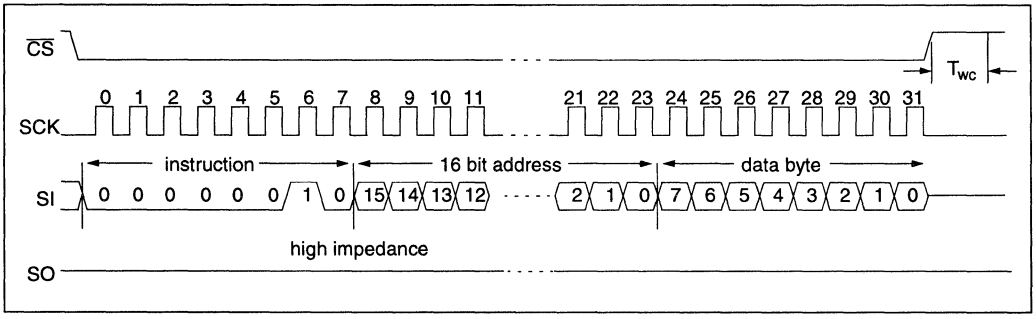
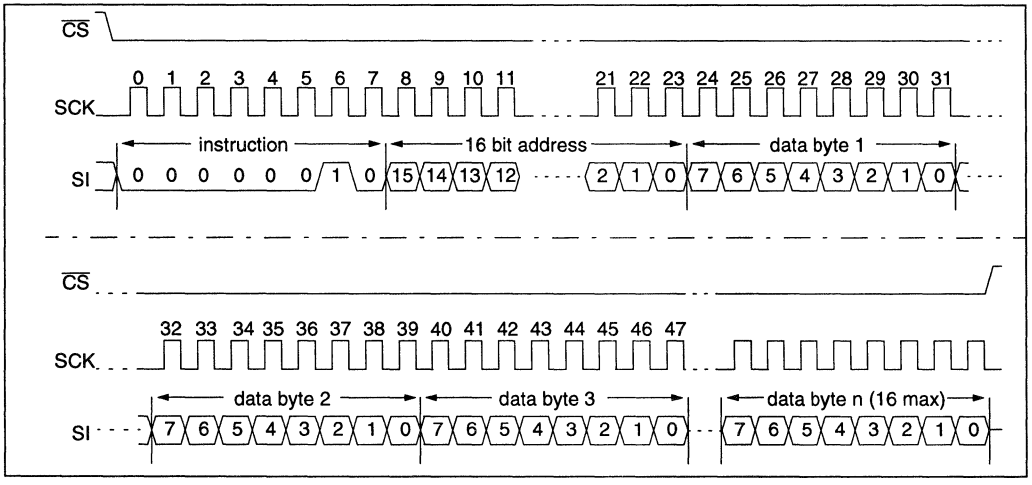


FIGURE 3-3: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25xx160 contains a write enable latch. See Table 3-3 for the Write Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE

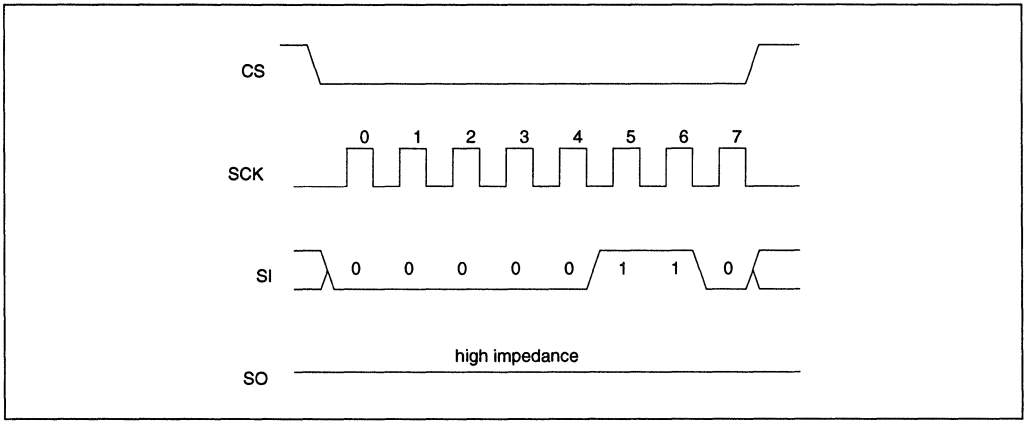
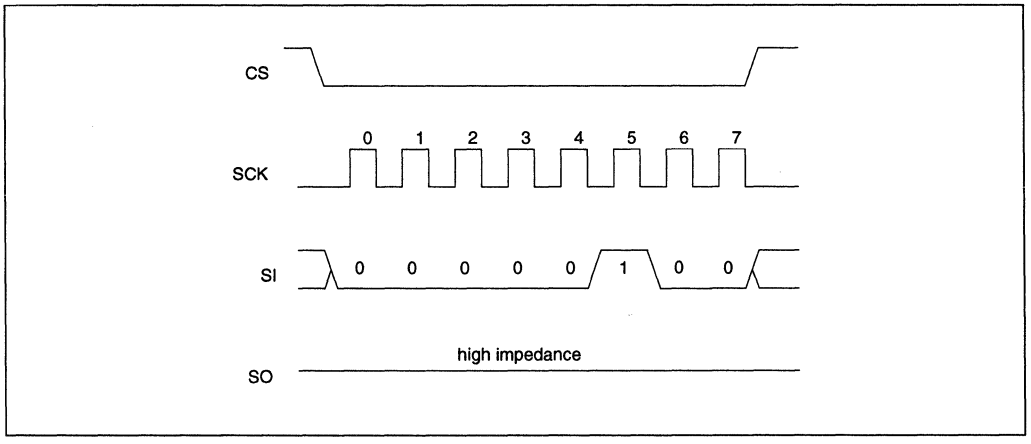


FIGURE 3-5: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

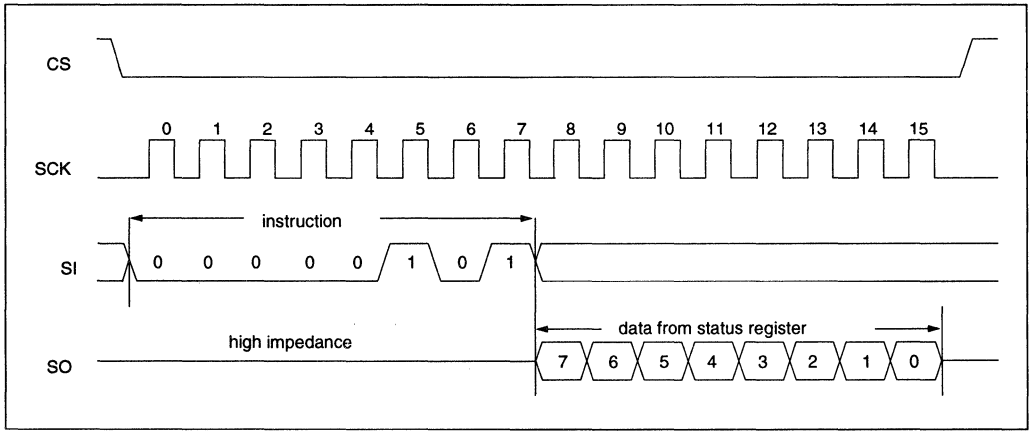
The **Write-In-Process (WIP)** bit indicates whether the 25xx160 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array, when set to a '0' the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

See Figure 3-6 for the RDSR timing sequence.

FIGURE 3-6: READ STATUS REGISTER SEQUENCE



3.6 Write Status Register(WRSR)

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-2.

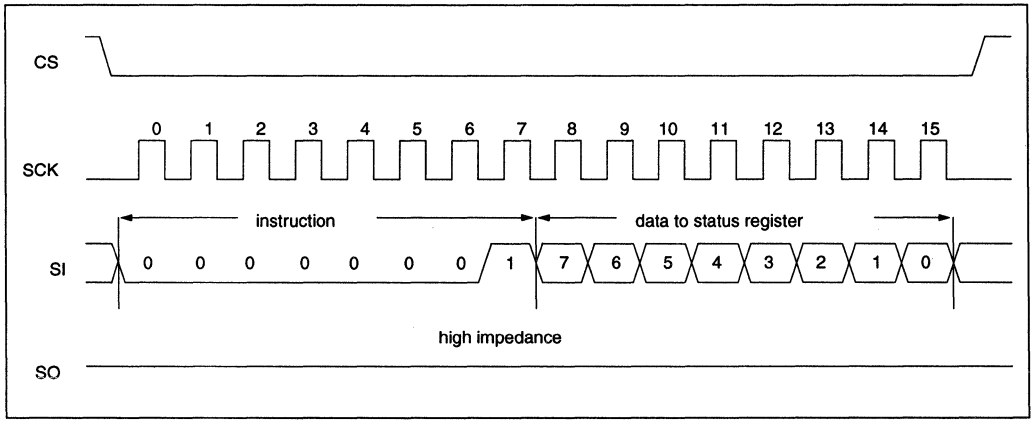
The Write Protect Enable (WPEN) bit is a non-volatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write Protect ($\overline{WP}$) pin and the Write Protect Enable (WPEN) bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write protected, only writes to non-volatile bits in the status register are disabled. See Table 3-3 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for the WRSR timing sequence.

TABLE 3-2: ARRAY PROTECTION

BP1	BP0	Array Addresses Write Protected
0	0	none
0	1	upper 1/4 (0600h - 07FFh)
1	0	upper 1/2 (0400h - 07FFh)
1	1	all (0000h - 07FFh)

FIGURE 3-7: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up.
- A write enable instruction must be issued to set the write enable latch.
- After a byte write, page write, or status register write, the write enable latch is reset.
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle.
- Access to the array during an internal write cycle is ignored and programming is continued.

3.8 Power On State

The 25xx160 powers on in the following state:

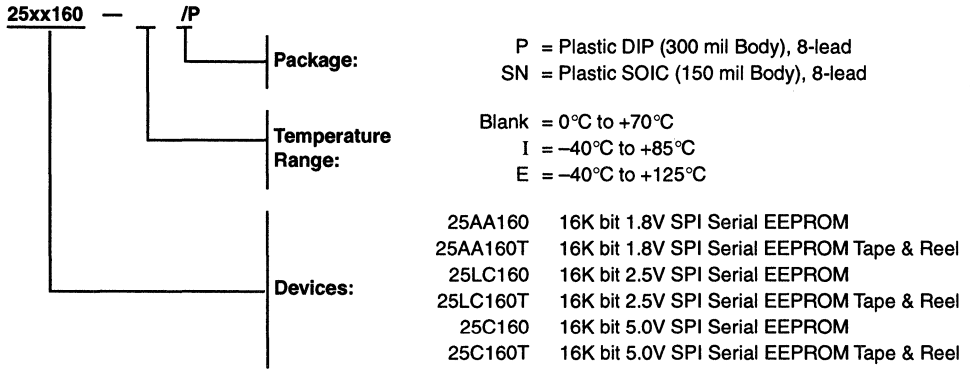
- The device is in low power standby mode ($\overline{CS} = 1$).
- The write enable latch is reset.
- SO is in high impedance state.
- A low level on $\overline{CS}$ is required to enter active state.

TABLE 3-3: WRITE PROTECT FUNCTIONALITY MATRIX

WPEN	WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	1	Protected	Writable	Protected
X	High	1	Protected	Writable	Writable

25AA160/25LC160/25C160 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

25LC320/25C320

32K SPI™ Bus Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
25C320	4.5-5.5V	3 MHz	C,I,E
25LC320	2.5-5.5V	2 MHz	C,I

FEATURES

- Low power CMOS technology
  - Write current: 3 mA maximum
  - Read current: 500 µA typical
  - Standby current: 500 nA typical
- 4096 x 8 bit organization
- 32 byte page
- Write cycle time: 5ms max.
- Self-timed ERASE and WRITE cycles
- Block write protection
  - Protect none, 1/4, 1/2, or all of array
- Built-in write protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write protect pin
- Sequential read
- High reliability
  - Endurance: 1M cycles (guaranteed)
  - Data retention: > 200 years
  - ESD protection: > 4000 V
- 8-pin PDIP, SOIC, and 14 lead TSSOP packages
- Temperature ranges supported:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) (25C320): -40°C to +125°C

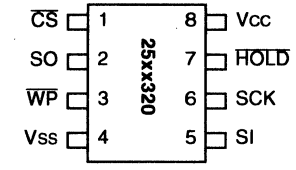
DESCRIPTION

The Microchip Technology Inc. 25LC320/25C320 (25xx320*) are 32K bit serial Electrically Erasable PROMs. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input.

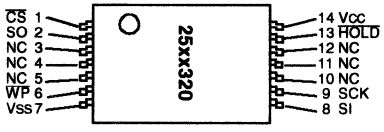
Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts.

PACKAGE TYPES

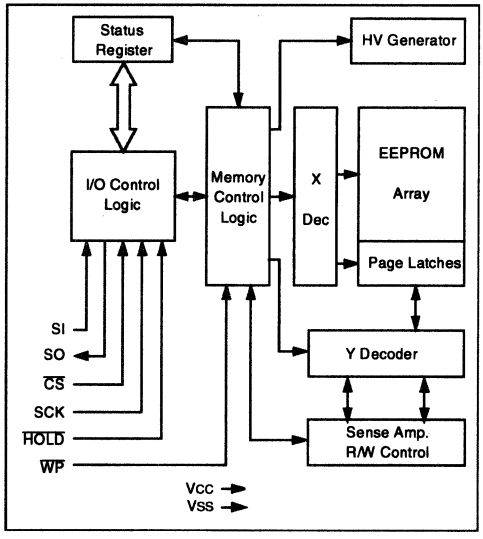
PDIP, SOIC



TSSOP



BLOCK DIAGRAM



*25xx320 is used in this document as a generic part number for the 25LC320/25C320 devices.
SPI is a trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

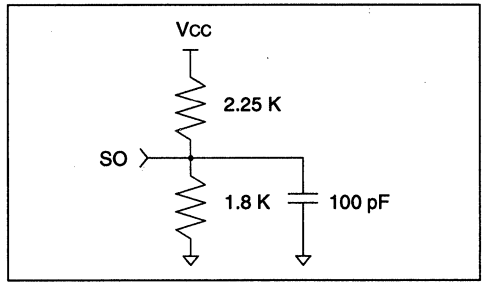
Vcc 7.0V
All inputs and outputs w.r.t. Vss ..... -0.6V to Vcc+1.0V
Storage temperature ..... -65°C to 150°C
Ambient temperature under bias ..... -65°C to 125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins 4kV

***Notice:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Pin
Vss	Ground
Vcc	Supply Voltage
$\overline{HOLD}$	Hold Input

FIGURE 1-1: AC TEST CIRCUIT



1.2 AC Test Conditions

AC Waveform:
VLO = 0.2V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V (Note 2)
Timing Measurement Reference Level
Input 0.5 Vcc
Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V
2: For Vcc > 4.0V

TABLE 1-2: DC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): TAMB = 0°C to +70°C Vcc = 2.5V to 5.5V Industrial (I): TAMB = -40°C to +85°C Vcc = 2.5V to 5.5V Automotive (E): TAMB = -40°C to +125°C Vcc = 4.5V to 5.5V (25C320 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
High level input voltage	VIH1	2.0	Vcc+1	V	Vcc ≥ 2.7V (Note)
	VIH2	0.7 Vcc	Vcc+1	V	Vcc< 2.7V (Note)
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.7V (Note)
	VIL2	-0.3	0.3 Vcc	V	Vcc < 2.7V (Note)
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
High level output voltage	VOH	Vcc -0.5	—	V	IOH =-400 µA
Input leakage current	ILI	-10	10	µA	$\overline{CS}$ = Vcc, VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	$\overline{CS}$ = Vcc, VOUT = Vss to Vcc
Internal Capacitance (all inputs and outputs)	CINT	—	7	pF	TAMB = 25°C, CLK = 1.0 MHz, Vcc = 5.0V (Note)
Operating Current	ICC Read	— —	1 500	mA µA	Vcc = 5.5V; FCLK=3.0 MHz; SO = Open Vcc = 2.5V; FCLK=2.0 MHz; SO = Open
	ICC Write	— —	5 3	mA mA	Vcc= 5.5V Vcc = 2.5V
Standby Current	ICCS	— —	5 1	µA µA	$\overline{CS}$ = Vcc = 5.5V, Inputs tied to Vcc or Vss $\overline{CS}$ = Vcc = 2.5V, Inputs tied to Vcc or Vss

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): Tamb = 0°C to +70°C Vcc = 2.5V to 5.5V Industrial (I): Tamb = -40°C to +85°C Vcc = 2.5V to 5.5V Automotive (E): Tamb = -40°C to +125°C Vcc = 4.5V to 5.5V (25C320 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
Clock Frequency	FCLK	— —	3 2	MHz MHz	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
$\overline{CS}$ Setup Time	TCSS	100 250	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
$\overline{CS}$ Hold Time	TCSH	150 250	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
$\overline{CS}$ Disable Time	TCSD	500	—	ns	
Data Setup Time	TSU	30 50	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
Data Hold Time	THD	50 100	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
CLK Rise Time	TR	—	2	µs	(Note 1)
CLK Fall Time	TF	—	2	µs	(Note 1)
Clock High Time	THI	150 250	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
Clock Low Time	TLO	150 250	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
Clock Delay Time	TCLD	50	—	ns	
Clock Enable Time	TCLE	50	—	ns	
Output Valid from Clock Low	TV	— —	150 250	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
Output Hold Time	THO	0	—	ns	(Note 1)
Output Disable Time	TDIS	— —	200 250	ns ns	Vcc = 4.5V to 5.5V (Note 1) Vcc = 2.5V to 4.5V (Note 1
$\overline{HOLD}$ Setup Time	THS	100 100	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
$\overline{HOLD}$ Hold Time	THH	100 100	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
$\overline{HOLD}$ Low to Output High-Z	THZ	100 150	— —	ns ns	Vcc = 4.5V to 5.5V (Note 1) Vcc = 2.5V to 4.5V (Note 1)
$\overline{HOLD}$ High to Output Valid	THV	100 150	— —	ns ns	Vcc = 4.5V to 5.5V Vcc = 2.5V to 4.5V
Internal Write Cycle Time	TWC	—	5	ms	
Endurance	—	1M	—	E/W Cycles	(Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's BBS or website.

FIGURE 1-2: HOLD TIMING

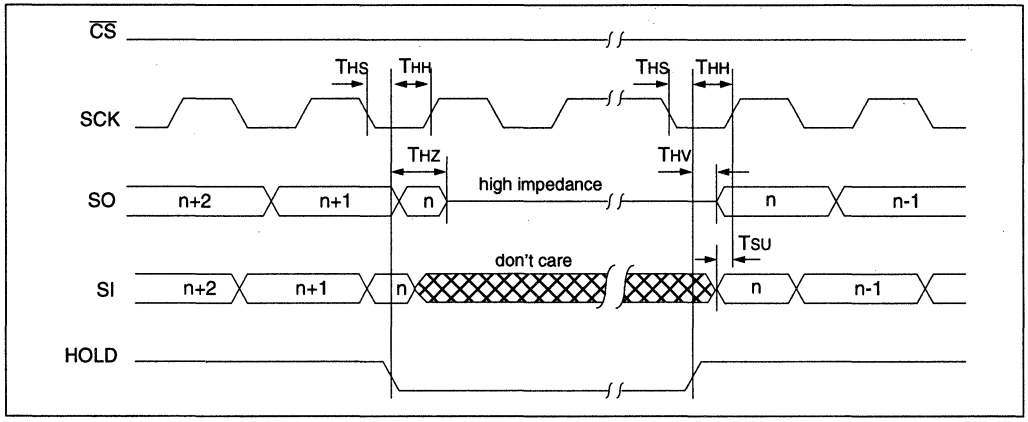


FIGURE 1-3: SERIAL INPUT TIMING

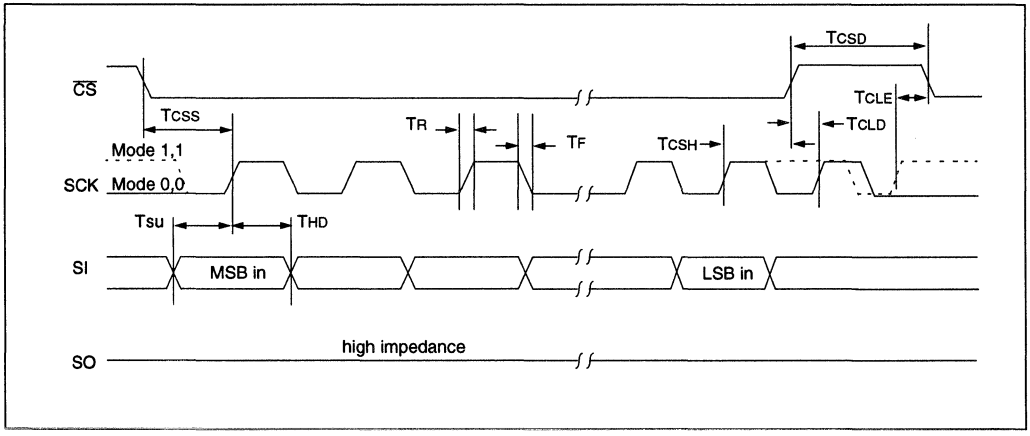
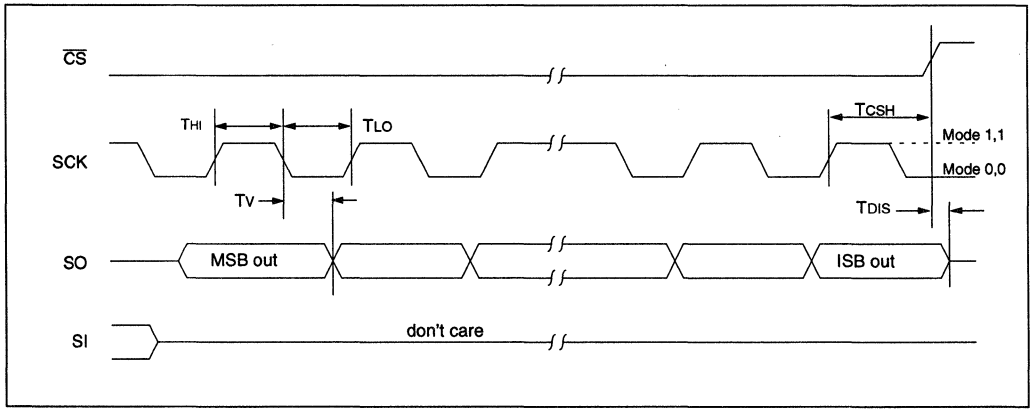


FIGURE 1-4: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in standby mode as soon as the programming cycle is complete. As soon as the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. A low to high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.3 Serial Output (SO)

The SO pin is used to transfer data out of the 25xx320. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25xx320. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.5 Write Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the status register to prohibit writes to the non-volatile bits in the status register. When $\overline{WP}$ is low and WPEN is high, writing to the non-volatile bits in the status register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the non-volatile bits in the status register operate normally. If the WPEN bit is set, $\overline{WP}$ low during a status register write sequence will disable writing to the status register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is low. This allows the user to install the 25xx320 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25xx320 while in the middle of a serial sequence without having to re-transmit the entire sequence over at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high to low transition. The 25xx320 must remain selected during this sequence. The SI, SCK, and SO pins are in a high impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 PRINCIPLES OF OPERATION

The 25xx320 are 4096 byte Serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25xx320 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25xx320 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the 25xx320 followed by the 16-bit address, with the four MSBs of the address being don't care bits. After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (0FFFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25xx320, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25xx320. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a write instruction, followed by the 16-bit address, with the four MSBs of the address being don't care bits, and then the data to be written. Up to 32 bytes of data can be sent to the 25xx320 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXXX XXXX XXX0 0000 and ends with XXXX XXXX XXX1 1111. If the internal address counter reaches XXXX XXXX XXX1 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the status register may be read to check the status of the WPEN, WIP, WEL, BP1, and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

FIGURE 3-1: READ SEQUENCE

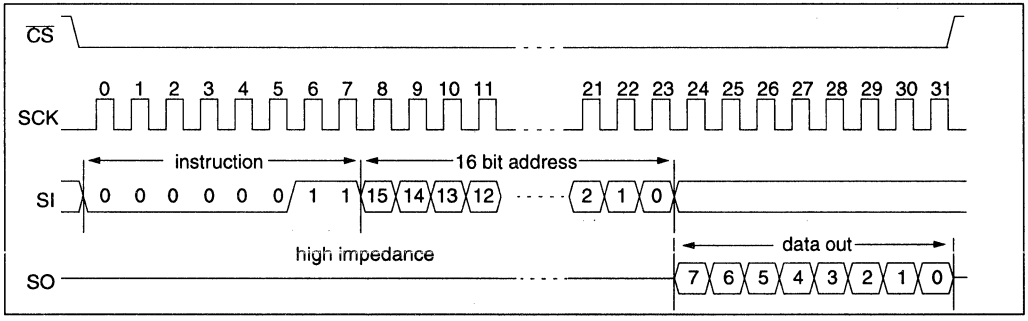


FIGURE 3-2: BYTE WRITE SEQUENCE

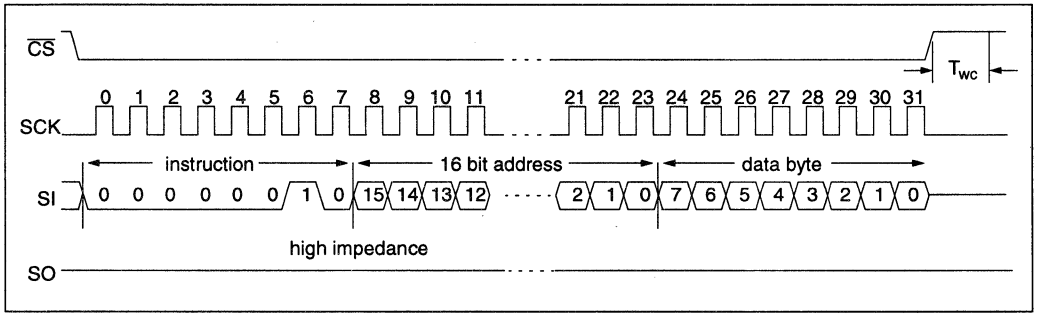
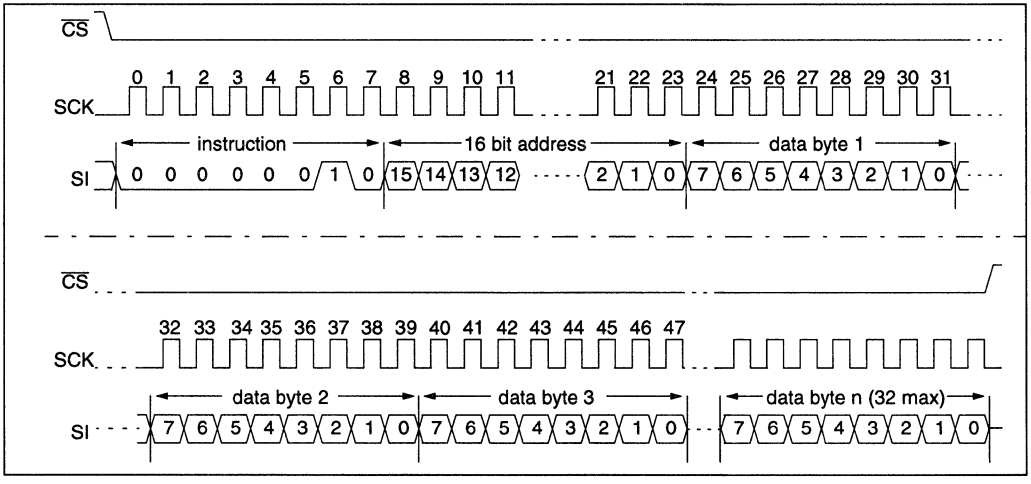


FIGURE 3-3: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25xx320 contains a write enable latch. See Table 3-3 for the Write Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE

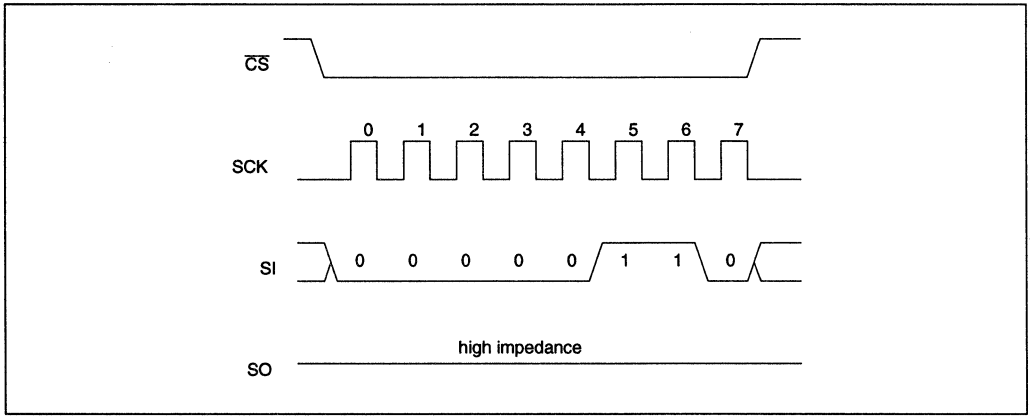
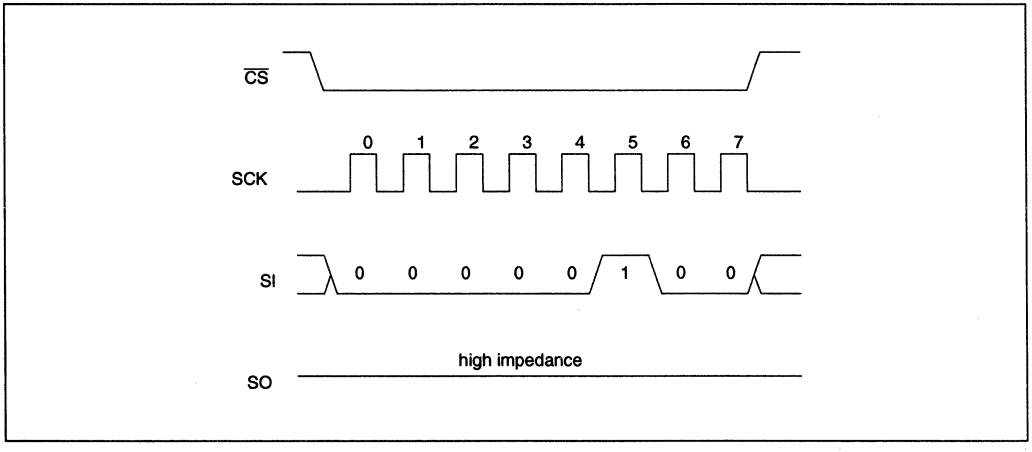


FIGURE 3-5: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

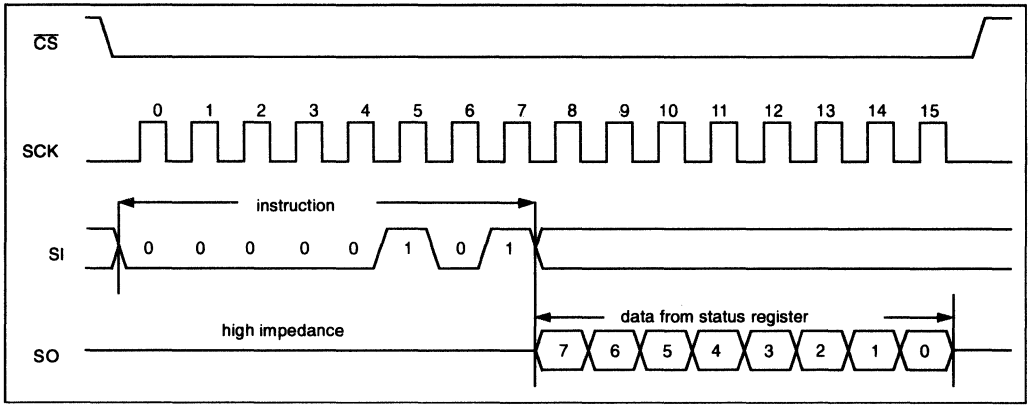
The **Write-In-Process (WIP)** bit indicates whether the 25xx320 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array, when set to a '0' the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

See Figure 3-6 for the RDSR timing sequence.

FIGURE 3-6: READ STATUS REGISTER SEQUENCE



3.6 Write Status Register(WRSR)

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-2.

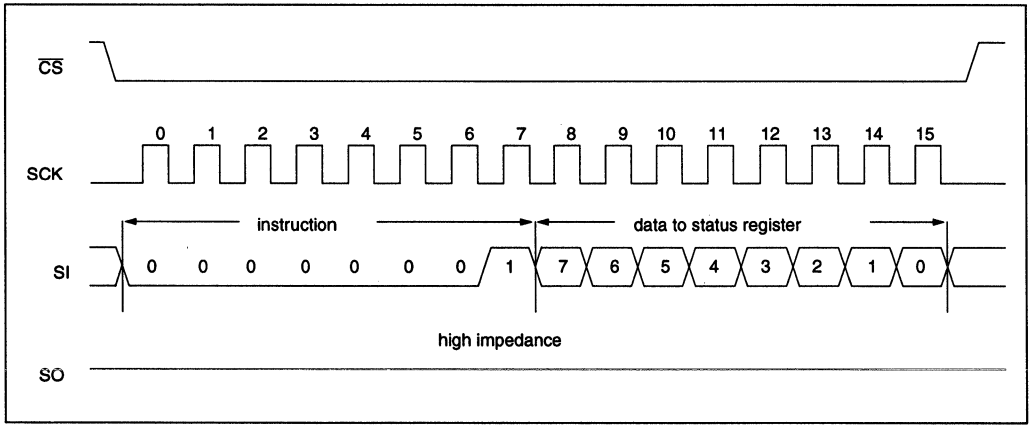
The Write Protect Enable (WPEN) bit is a non-volatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write Protect ($\overline{WP}$) pin and the Write Protect Enable (WPEN) bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write protected, only writes to non-volatile bits in the status register are disabled. See Table 3-3 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for the WRSR timing sequence.

TABLE 3-2: ARRAY PROTECTION

BP1	BP0	Array Addresses Write Protected
0	0	none
0	1	upper 1/4 (0C00h - 0FFFh)
1	0	upper 1/2 (0800h - 0FFFh)
1	1	all (0000h - 0FFFh)

FIGURE 3-7: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up.
- A write enable instruction must be issued to set the write enable latch.
- After a byte write, page write, or status register write, the write enable latch is reset.
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle.
- Access to the array during an internal write cycle is ignored and programming is continued.

3.8 Power On State

The 25xx320 powers on in the following state:

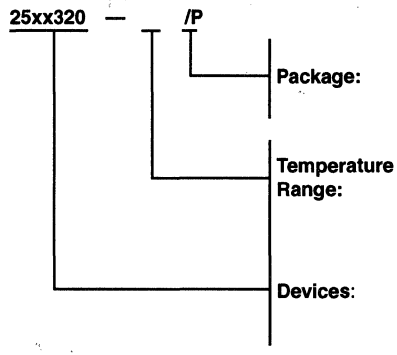
- The device is in low power standby mode ($\overline{CS} = 1$).
- The write enable latch is reset.
- SO is in high impedance state.
- A low level on $\overline{CS}$ is required to enter active state.

TABLE 3-3: WRITE PROTECT FUNCTIONALITY MATRIX

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	1	Protected	Writable	Protected
X	High	1	Protected	Writable	Writable

25LC320/25C320 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Package:	
P	= Plastic DIP (300 mil Body), 8-lead
SN	= Plastic SOIC (150 mil Body), 8-lead
ST	= TSSOP, 14-lead
Temperature Range:	
Blank	= 0°C to +70°C
I	= –40°C to +85°C
E	= –40°C to +125°C
Devices:	
25LC320	32K bit 2.5V SPI Serial EEPROM
25LC320T	32K bit 2.5V SPI Serial EEPROM Tape and Reel
25C320	32K bit 5.0V SPI Serial EEPROM
25C320T	32K bit 5.0V SPI Serial EEPROM Tape and Reel

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

25AA640/25LC640/25C640

64K SPI™ Bus Serial EEPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
25AA640	1.8-5.5V	1 MHz	C,I
25LC640	2.5-5.5V	2 MHz	C,I
25C640	4.5-5.5V	3 MHz	C,I,E

FEATURES

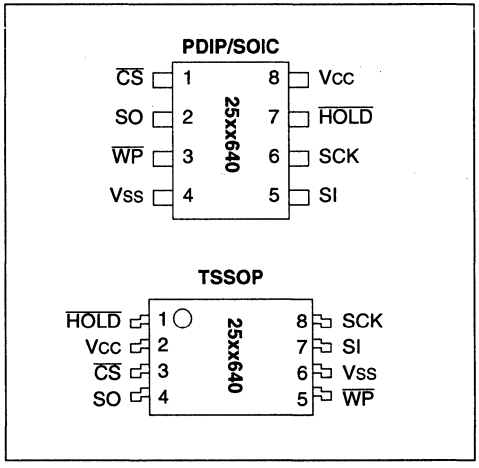
- Low power CMOS technology
  - Write current: 3 mA typical
  - Read current: 500 µA typical
  - Standby current: 500 nA typical
- 8192 x 8 bit organization
- 32 byte page
- Write cycle time: 5ms max.
- Self-timed ERASE and WRITE cycles
- Block write protection
  - Protect none, 1/4, 1/2, or all of array
- Built-in write protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write protect pin
- Sequential read
- High reliability
  - Endurance: 1M cycles (guaranteed)
  - Data retention: > 200 years
  - ESD protection: > 4000 V
- 8-pin PDIP, SOIC, and TSSOP packages
- Temperature ranges supported:
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E) (25C640): -40°C to +125°C

DESCRIPTION

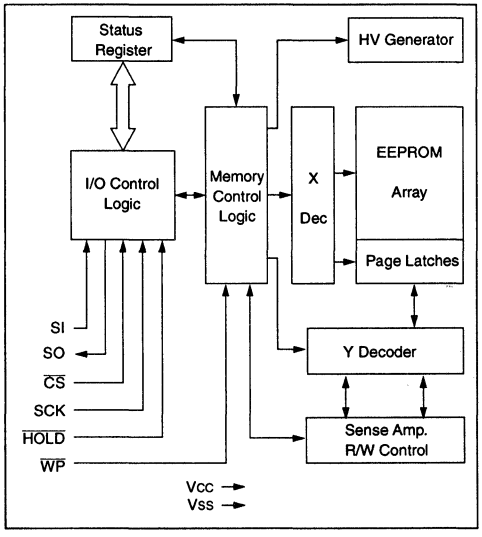
The Microchip Technology Inc. 25AA640/25LC640/25C640 (25xx640*) is a 64K bit serial Electrically Erasable PROM. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts.

PACKAGE TYPES



BLOCK DIAGRAM



*25xx640 is used in this document as a generic part number for the 25AA640/25LC640/25C640 devices.
SPI is a trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

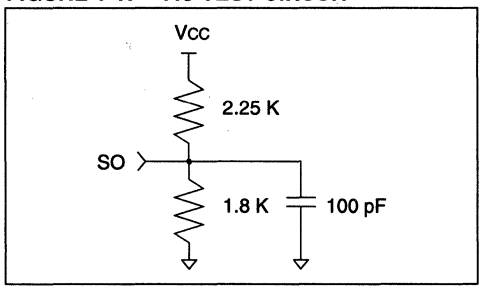
Vcc 7.0V
All inputs and outputs w.r.t. Vss..... -0.6V to Vcc+1.0V
Storage temperature ..... -65°C to 150°C
Ambient temperature under bias..... -65°C to 125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....4kV

***Notice:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Pin
Vss	Ground
Vcc	Supply Voltage
$\overline{HOLD}$	Hold Input

FIGURE 1-1: AC TEST CIRCUIT



1.2 AC Test Conditions

AC Waveform:
VLO = 0.2V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V (Note 2)
Timing Measurement Reference Level
Input 0.5 Vcc
Output 0.5 Vcc

Note 1: For Vcc ≤ 4.0V
2: For Vcc > 4.0V

TABLE 1-2: DC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): Tamb = 0°C to +70°C Vcc = 1.8V to 5.5V Industrial (I): Tamb = -40°C to +85°C Vcc = 1.8V to 5.5V Automotive (E): Tamb = -40°C to +125°C Vcc = 4.5V to 5.5V (25C640 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
High level input voltage	VIH1	2.0	Vcc+1	V	Vcc ≥ 2.7V (Note)
	VIH2	0.7 Vcc	Vcc+1	V	Vcc< 2.7V (Note)
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.7V (Note)
	VIL2	-0.3	0.2 Vcc	V	Vcc < 2.7V (Note)
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
	VOL	—	0.2	V	IOL = 1.0 mA, Vcc < 2.5V
High level output voltage	VOH	Vcc -0.5	—	V	IOH =-400 µA
Input leakage current	ILI	-10	10	µA	$\overline{CS}$ = Vcc, VIN = Vss to Vcc
Output leakage current	ILO	-10	10	µA	$\overline{CS}$ = Vcc, VOUT = Vss to Vcc
Internal Capacitance (all inputs and outputs)	CINT	—	7	pF	TAMB = 25°C, CLK = 1.0 MHz, Vcc = 5.0V (Note)
Operating Current	Icc Read	— —	1 500	mA µA	Vcc = 5.5V; FCLK=3.0 MHz; SO = Open Vcc = 2.5V; FCLK=2.0 MHz; SO = Open
	Icc Write	— —	5 3	mA mA	Vcc= 5.5V Vcc = 2.5V
Standby Current	Iccs	— —	5 1	µA µA	$\overline{CS}$ = Vcc = 5.5V, Inputs tied to Vcc or Vss $\overline{CS}$ = Vcc = 2.5V, Inputs tied to Vcc or Vss

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

All parameters apply over the specified operating ranges unless otherwise noted.	Commercial (C): Tamb = 0°C to +70°C Vcc = 1.8V to 5.5V Industrial (I): Tamb = -40°C to +85°C Vcc = 1.8V to 5.5V Automotive (E): Tamb = -40°C to +125°C Vcc = 4.5V to 5.5V (25C640 only)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Test Conditions**
Clock Frequency	FCLK	—	3	MHz	Vcc = 4.5V to 5.5V (Note 2)
		—	2	MHz	Vcc = 2.5V to 4.5V
		—	1	MHz	Vcc = 1.8V to 2.5V
$\overline{CS}$ Setup Time	TCSS	100	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		500	—	ns	Vcc = 1.8V to 2.5V
$\overline{CS}$ Hold Time	TCSH	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
$\overline{CS}$ Disable Time	TCSD	500	—	ns	
Data Setup Time	TSU	30	—	ns	Vcc = 4.5V to 5.5V
		50	—	ns	Vcc = 2.5V to 4.5V
		50	—	ns	Vcc = 1.8V to 2.5V
Data Hold Time	THD	50	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		100	—	ns	Vcc = 1.8V to 2.5V
CLK Rise Time	TR	—	2	µs	(Note 1)
CLK Fall Time	TF	—	2	µs	(Note 1)
Clock High Time	THI	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
Clock Low Time	TLO	150	—	ns	Vcc = 4.5V to 5.5V
		250	—	ns	Vcc = 2.5V to 4.5V
		475	—	ns	Vcc = 1.8V to 2.5V
Clock Delay Time	TCLD	50	—	ns	
Clock Enable Time	TCLE	50	—	ns	
Output Valid from Clock Low	TV	—	150	ns	Vcc = 4.5V to 5.5V
		—	250	ns	Vcc = 2.5V to 4.5V
		—	475	ns	Vcc = 1.8V to 2.5V
Output Hold Time	THO	0	—	ns	(Note 1)
Output Disable Time	TDIS	—	200	ns	Vcc = 4.5V to 5.5V (Note 1)
		—	250	ns	Vcc = 2.5V to 4.5V (Note 1)
		—	500	ns	Vcc = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ Setup Time	THS	100	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
$\overline{HOLD}$ Hold Time	THH	100	—	ns	Vcc = 4.5V to 5.5V
		100	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
$\overline{HOLD}$ Low to Output High-Z	THZ	100	—	ns	Vcc = 4.5V to 5.5V (Note 1)
		150	—	ns	Vcc = 2.5V to 4.5V (Note 1)
		200	—	ns	Vcc = 1.8V to 2.5V (Note 1)
$\overline{HOLD}$ High to Output Valid	THV	100	—	ns	Vcc = 4.5V to 5.5V
		150	—	ns	Vcc = 2.5V to 4.5V
		200	—	ns	Vcc = 1.8V to 2.5V
Internal Write Cycle Time	TWC	—	5	ms	
Endurance	—	1M	—	E/W Cycles	(Note 3)

Note 1: This parameter is periodically sampled and not 100% tested.

2: FCLK max. = 2.5 MHz for Tamb > 85°C

3: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Microchip's BBS or website.

FIGURE 1-2: HOLD TIMING

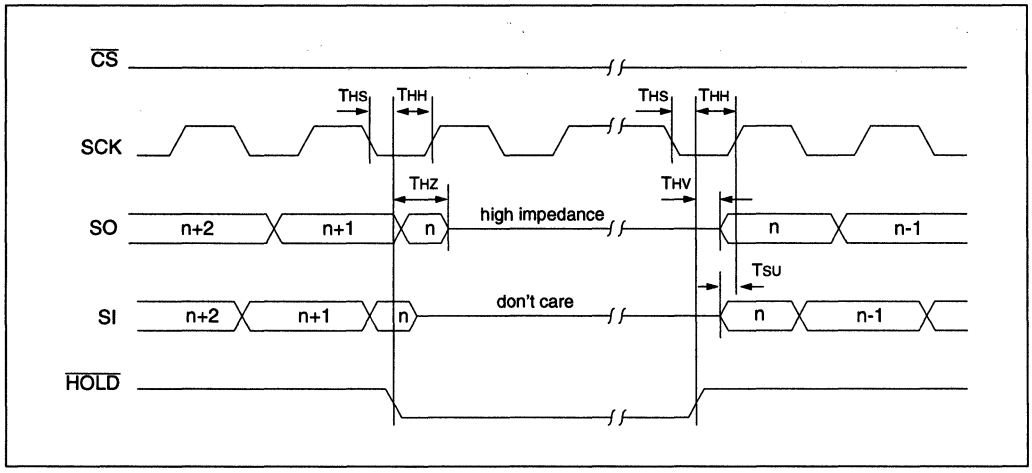


FIGURE 1-3: SERIAL INPUT TIMING

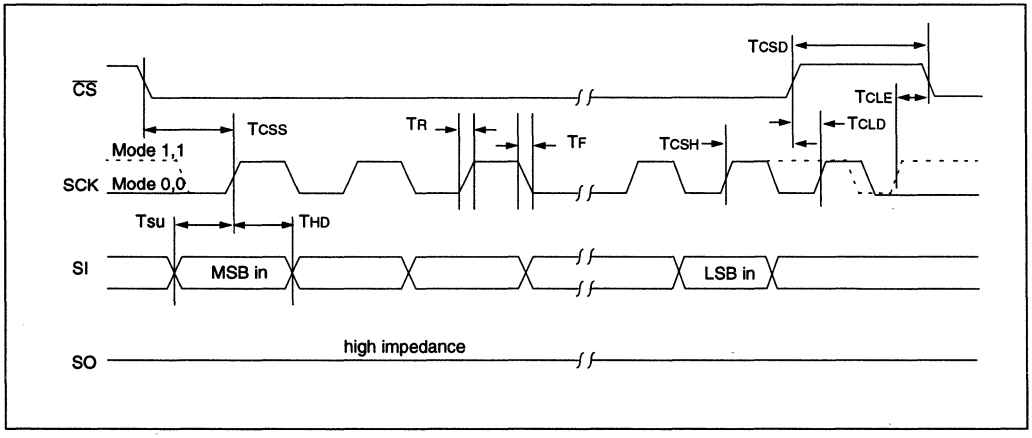
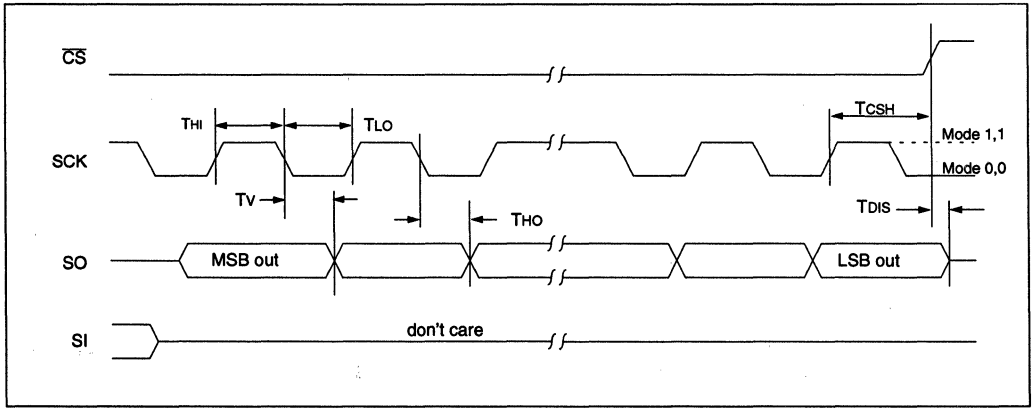


FIGURE 1-4: SERIAL OUTPUT TIMING



2.0 PIN DESCRIPTIONS

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go in standby mode as soon as the programming cycle is complete. As soon as the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. A low to high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a high to low transition on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.3 Serial Output (SO)

The SO pin is used to transfer data out of the 25xx640. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25xx640. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.5 Write Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the status register to prohibit writes to the non-volatile bits in the status register. When $\overline{WP}$ is low and WPEN is high, writing to the non-volatile bits in the status register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the non-volatile bits in the status register operate normally. If the WPEN bit is set, $\overline{WP}$ low during a status register write sequence will disable writing to the status register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is low. This allows the user to install the 25AA640/25LC640/25C640 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25xx640 while in the middle of a serial sequence without having to re-transmit the entire sequence over at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the $\overline{HOLD}$ function will not be invoked until the next SCK high to low transition. The 25xx640 must remain selected during this sequence. The SI, SCK, and SO pins are in a high impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the $\overline{HOLD}$ line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 PRINCIPLES OF OPERATION

The 25xx640 is a 8192 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25xx640 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25xx640 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the 25xx640 followed by the 16-bit address with the three MSB's of the address being don't care bits. After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25xx640 array or status register, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25xx640. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a write instruction, followed by the address, and then the data to be written. Up to 32 bytes of data can be sent to the 25xx640 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXX0 0000 and ends with XXX1 1111. If the internal address counter reaches XXX1 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the status register may be read to check the status of the WPEN, WIP, WEL, BP1, and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WREN	0000 0110	Set the write enable latch (enable write operations)
WRDI	0000 0100	Reset the write enable latch (disable write operations)
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

FIGURE 3-1: READ SEQUENCE

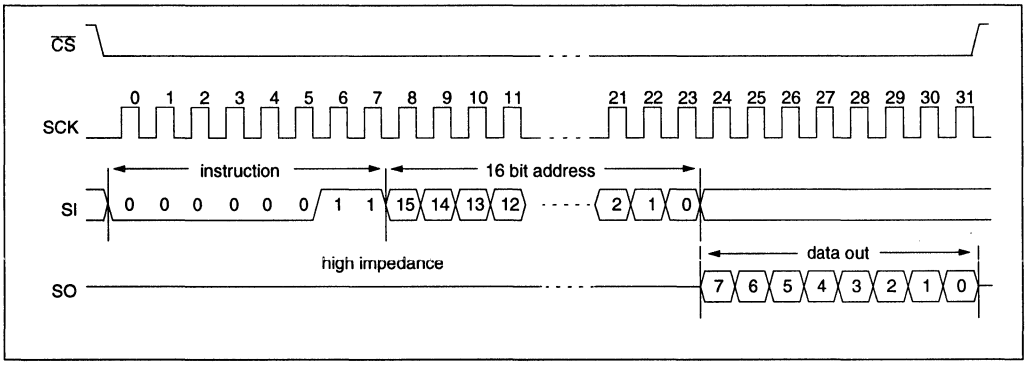


FIGURE 3-2: BYTE WRITE SEQUENCE

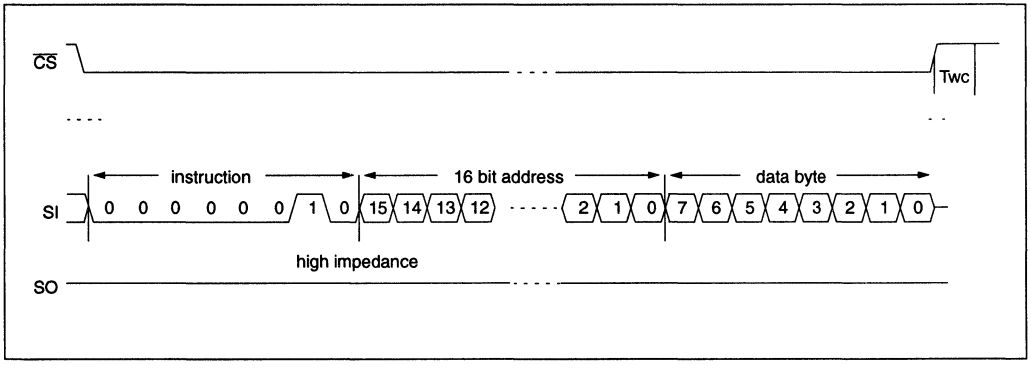
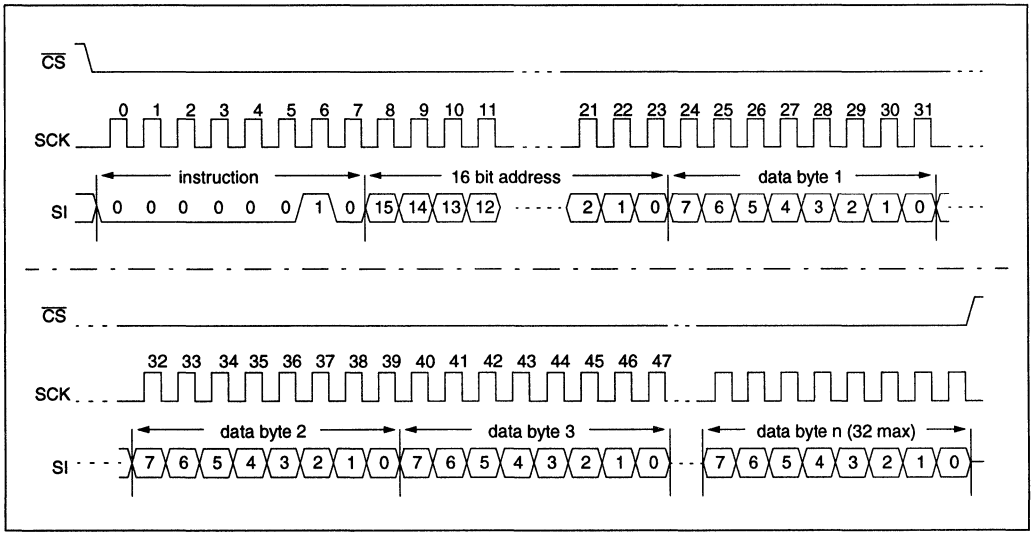


FIGURE 3-3: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25xx640 contains a write enable latch. See Table 3-3 for the Write Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE

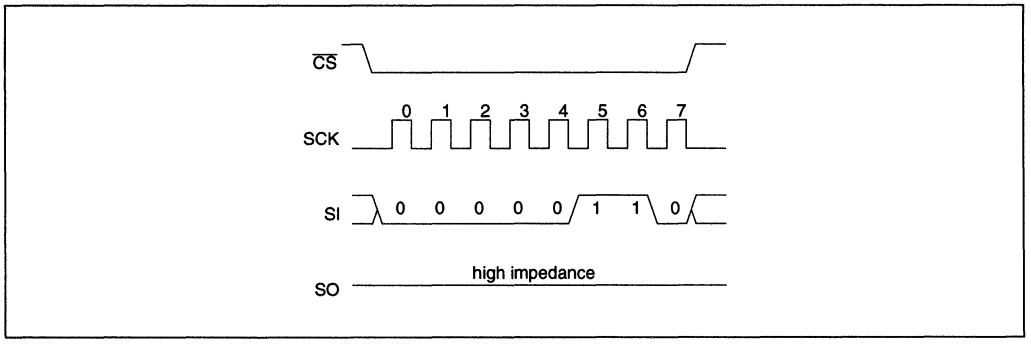
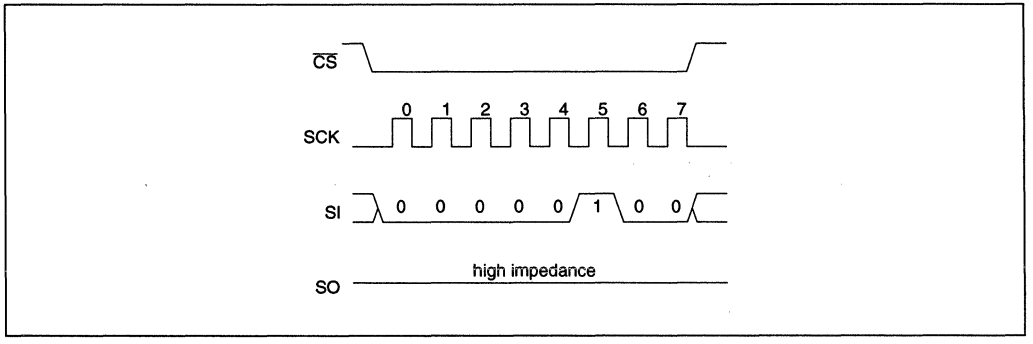


FIGURE 3-5: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the 25xx640 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array and status register, when set to a '0' the latch prohibits writes to the array and status register. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

See Figure 3-6 for RDSR timing sequence

3.6 Write Status Register(WRSR)

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-2.

The **Write Protect Enable (WPEN)** bit is a non-volatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write Protect ($\overline{WP}$) pin and the Write Protect Enable (WPEN) bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write protected, only writes to non-volatile bits in the status register are disabled. See Table 3-3 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for WRSR timing sequence

TABLE 3-2: ARRAY PROTECTION

BP1	BP0	Array Addresses Write Protected
0	0	none
0	1	upper 1/4 (1800h - 1FFFh)
1	0	upper 1/2 (1000h - 1FFFh)
1	1	all (0000h - 1FFFh)

FIGURE 3-6: READ STATUS REGISTER SEQUENCE

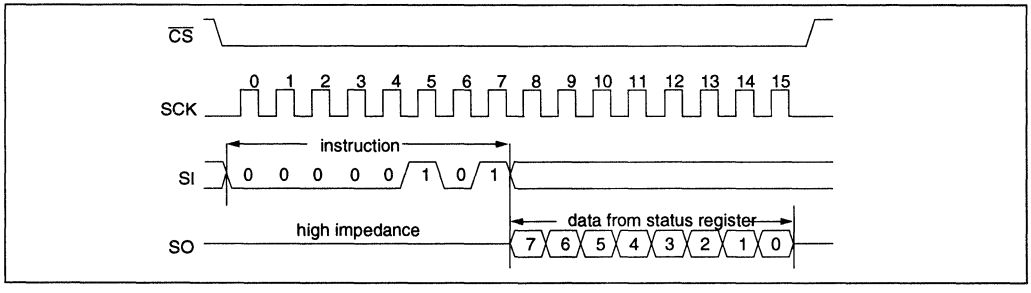
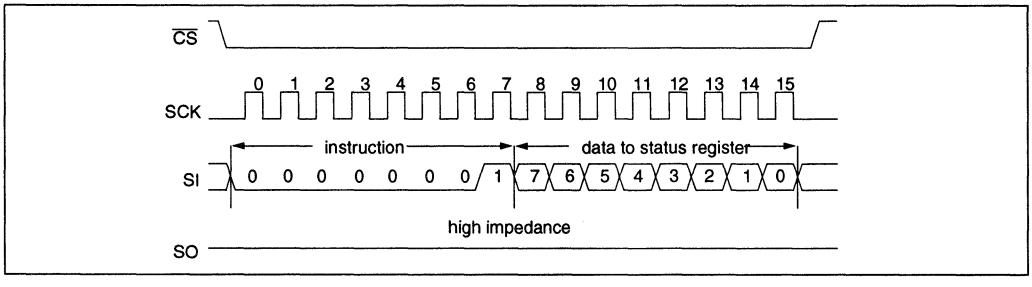


FIGURE 3-7: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up.
- A write enable instruction must be issued to set the write enable latch.
- After a byte write, page write, or status register write, the write enable latch is reset.
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle.
- Access to the array during an internal write cycle is ignored and programming is continued.

3.8 Power On State

The 25xx640 powers on in the following state:

- The device is in low power standby mode ($\overline{CS}$ = 1).
- The write enable latch is reset.
- SO is in high impedance state.
- A high to low transition on $\overline{CS}$ is required to enter the active state.

TABLE 3-3: WRITE PROTECT FUNCTIONALITY MATRIX

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	1	Protected	Writable	Protected
X	High	1	Protected	Writable	Writable

NOTES:

25AA640/25LC640/25C640 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

25xx640 — /P

Package:

P	= Plastic DIP (300 mil Body), 8-lead
SN	= Plastic SOIC (150 mil Body), 8-lead
ST	= TSSOP, 8-lead

Temperature Range:

Blank	= 0°C to +70°C
I	= –40°C to +85°C
E	= –40°C to +125°C

Devices:

25AA640	64K bit 1.8V SPI Serial EEPROM
25AA640T	64K bit 1.8V SPI Serial EEPROM Tape and Reel
25AA640X	64K bit 1.8V SPI Serial EEPROM in alternate pinout (ST only)
25AA640XT	64K bit 1.8V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25LC640	64K bit 2.5V SPI Serial EEPROM
25LC640T	64K bit 2.5V SPI Serial EEPROM Tape and Reel
25LC640X	64K bit 2.5V SPI Serial EEPROM in alternate pinout (ST only)
25LC640XT	64K bit 2.5V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
25C640	64K bit 5.0V SPI Serial EEPROM
25C640T	64K bit 5.0V SPI Serial EEPROM Tape and Reel
25C640X	64K bit 5.0V SPI Serial EEPROM in alternate pinout (ST only)
25C640XT	64K bit 5.0V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

SECTION 6
ID SOLUTIONS AND PLUG AND PLAY® PRODUCTS

24AA00	128 Bit I²C™ Bus Serial EEPROM	3-1
2424LC00	128 Bit I²C™ Bus Serial EEPROM	3-1
2424C00	128 Bit I²C™ Bus Serial EEPROM	3-1
24LCS61	1K Software Addressable I²C™ Serial EEPROM	3-47
24LC21	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-1
24LC21A	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-13
24LCS21	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-27
24LCS21A	1K 2.5V Dual Mode I²C™ Serial EEPROM	6-39
24LC41	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-53
24LC41A	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-65
24LCS41	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-79
24LCS41A	1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM	6-91
24LCS52	2K 2.5V I²C™ Serial EEPROM with Software Write Protect	3-71
24LCS62	2K Software Addressable I²C™ Serial EEPROM	3-47

Plug and Play is a registered trademark of Microsoft Corporation.
I²C is a trademark of Philips Corporation.

24LC21

1K 2.5V Dual Mode I²C™ Serial EEPROM

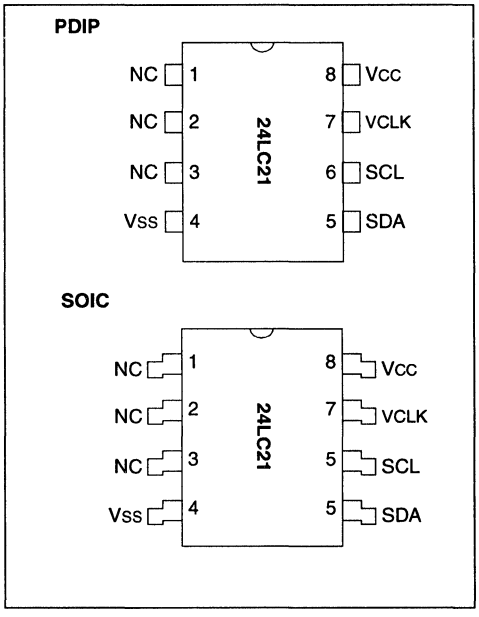
FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Factory programming (QTP) available
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

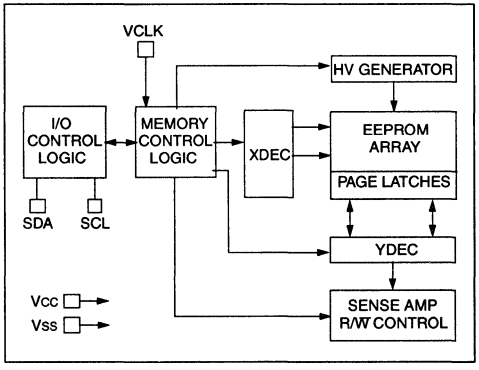
DESCRIPTION

The Microchip Technology Inc. 24LC21 is a 128 x 8 bit Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit Only Mode and Bi-Directional Mode. Upon power-up, the device will be in the Transmit Only Mode, sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the Bi-Directional Mode, with byte selectable read/write capability of the memory array. The 24LC21 is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

PACKAGE TYPES



BLOCK DIAGRAM



DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bi-Directional Mode)
VCLK	Serial Clock (Transmit-Only Mode)
Vcc	+2.5V to 5.5V Power Supply
NC	No Connection

TABLE 1-2: DC CHARACTERISTICS

	Vcc = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
SCL and SDA pins: High level input voltage Low level input voltage	 VIH VIL	 .7 Vcc —	 — .3 Vcc	 V V	
Input levels on VCLK pin: High level input voltage Low level input voltage	 VIH VIL	 2.0 —	 .8 .2 Vcc	 V V	 Vcc ≥ 2.7V (Note 1) Vcc < 2.7V (Note 1)
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	(Note 1)
Low level output voltage	VOL1	—	.4	V	IOL = 3 mA, Vcc = 2.5V (Note 1)
Low level output voltage	VOL2	—	.6	V	IOL = 6 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note1), Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write Icc Read	— —	3 1	mA mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	Vcc = 3.0V, SDA = SCL = Vcc Vcc = 5.5V, SDA = SCL = Vcc (Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.
2: VLCK must be grounded.

TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + .1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

The 24LC21 operates in two modes, the Transmit-Only Mode and the Bi-Directional Mode. There is a separate two wire protocol to support each mode, each having a separate clock input and sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bi-Directional Mode. The only way to switch the device back to the Transmit-Only Mode is to remove power from the device.

2.1 Transmit-Only Mode

The device will power up in the Transmit-Only Mode. This mode supports a unidirectional two wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (see Initialization Procedure, below). In this mode, data is transmitted on the SDA pin in 8 bit bytes, each followed by a ninth, null bit (see Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The Bi-Directional Mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.2 Initialization Procedure

After VCC has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal synchronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address. (Figure 2-2).

FIGURE 2-1: TRANSMIT ONLY MODE

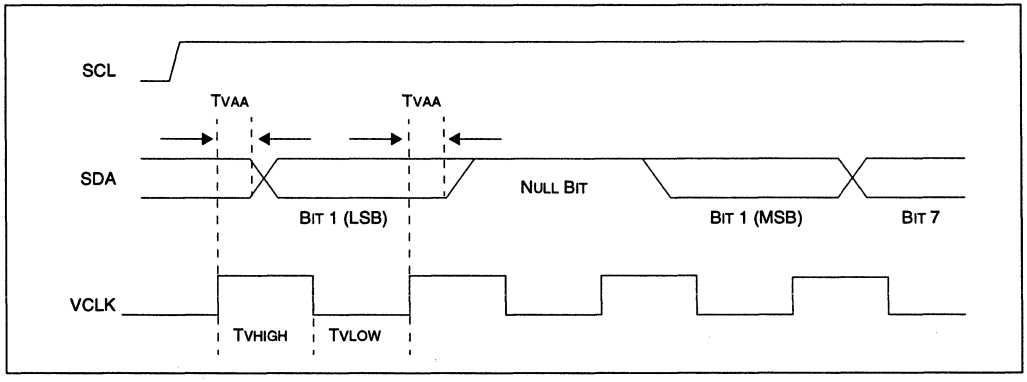
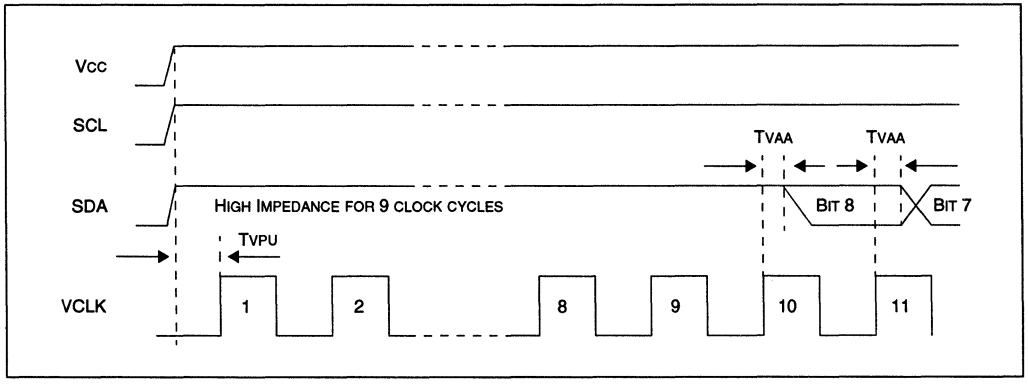


FIGURE 2-2: DEVICE INITIALIZATION



3.0 BI-DIRECTIONAL MODE

The 24LC21 can be switched into the Bi-Directional Mode (see Figure 3-1) by applying a valid high to low transition on the Bi-Directional Mode Clock (SCL). When the device has been switched into the Bi-Directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two wire bi-directional data transmission protocol. In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-Directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the 24LC21 acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.1 Bi-Directional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-2).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

3.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

FIGURE 3-1: MODE TRANSITION

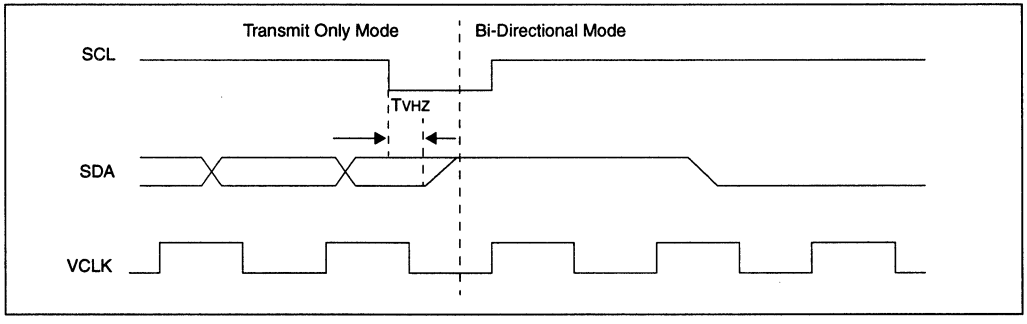
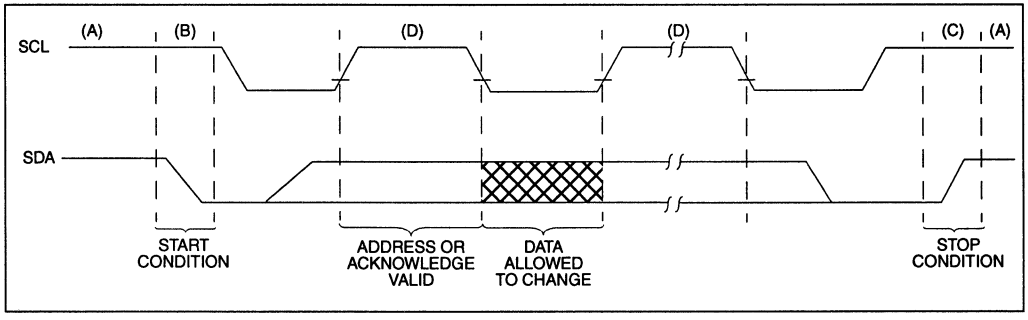


FIGURE 3-2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC21 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-3: BUS TIMING START/STOP

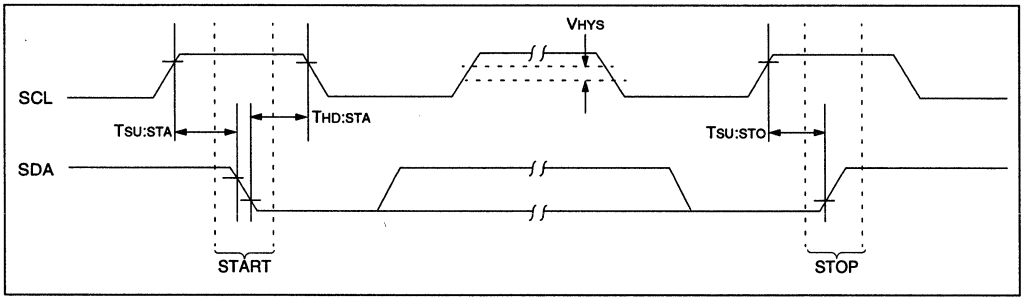
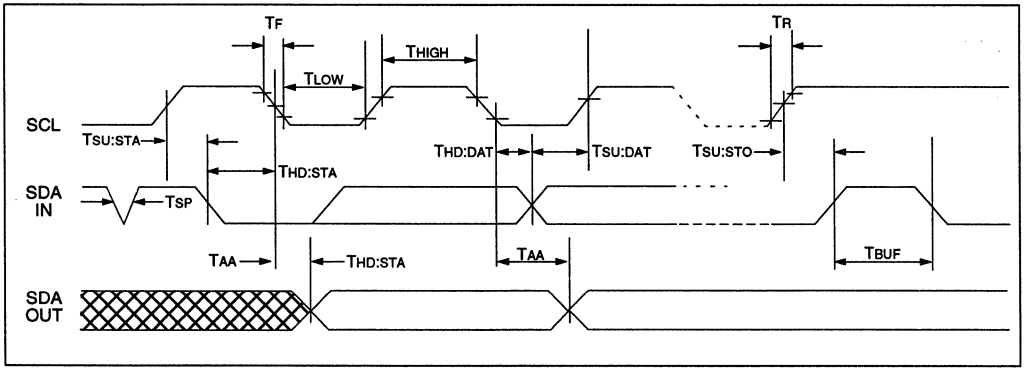


FIGURE 3-4: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

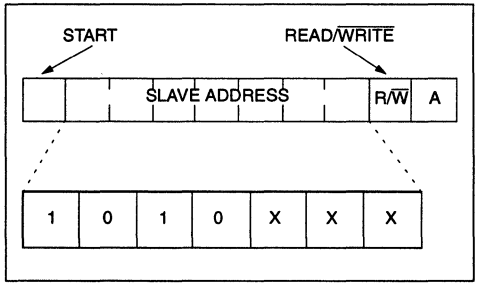
After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010) for the 24LC21, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC21 (Figure 3-5).

The 24LC21 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 3-5: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the slave address (4 bits), the don't care bits (3 bits) and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC21. After receiving another acknowledge signal from the 24LC21 the master device will transmit the data word to be written into the addressed memory location. The 24LC21 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC21 will not generate acknowledge signals (Figure 4-1).

It is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC21 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC21 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

It is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

FIGURE 4-1: BYTE WRITE

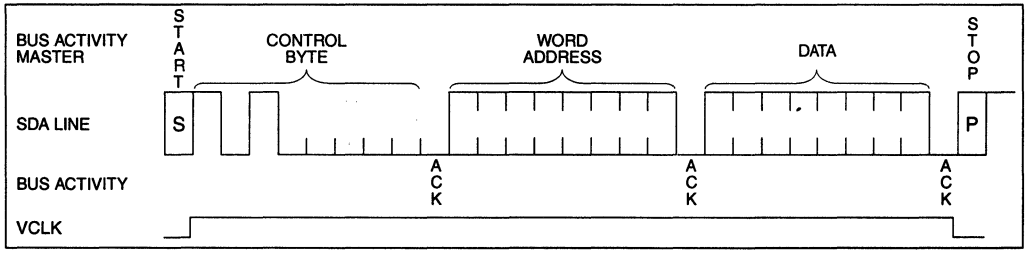
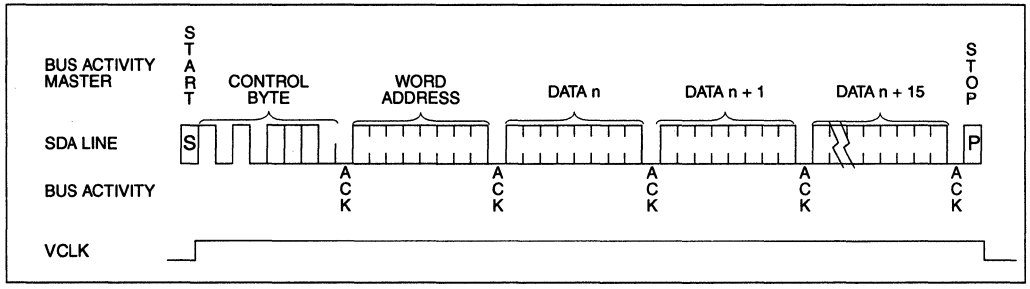


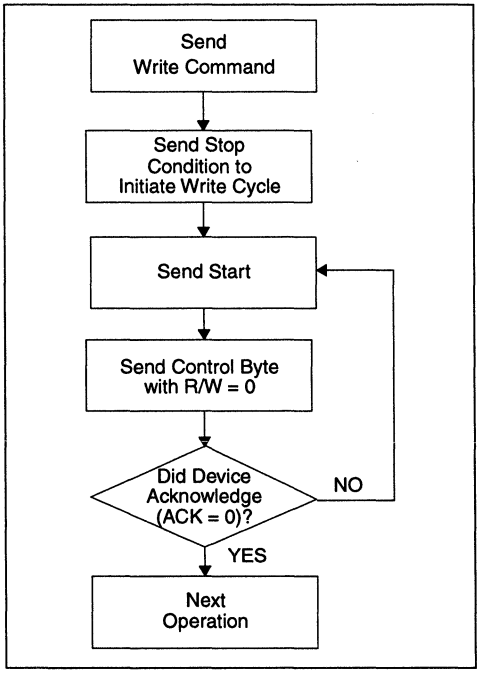
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

When using the 24LC21 in the Bi-Directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the 24LC21 to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LC21 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC21 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC21 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC21 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC21 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC21 discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC21 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC21 to transmit the next sequentially addressed 8 bit word (see Figure 7-3).

To provide sequential reads the 24LC21 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC21 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

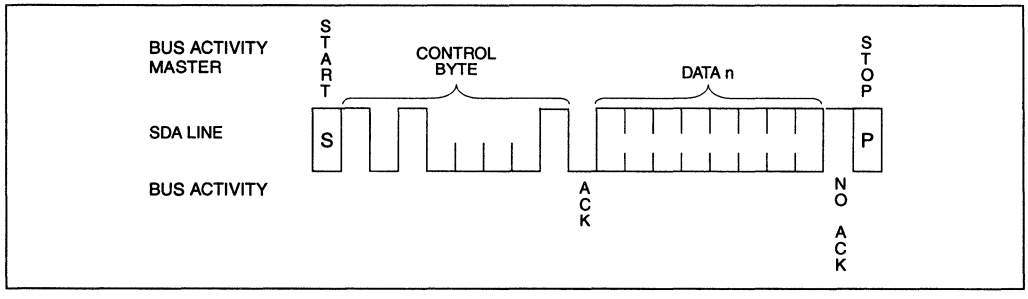


FIGURE 7-2: RANDOM READ

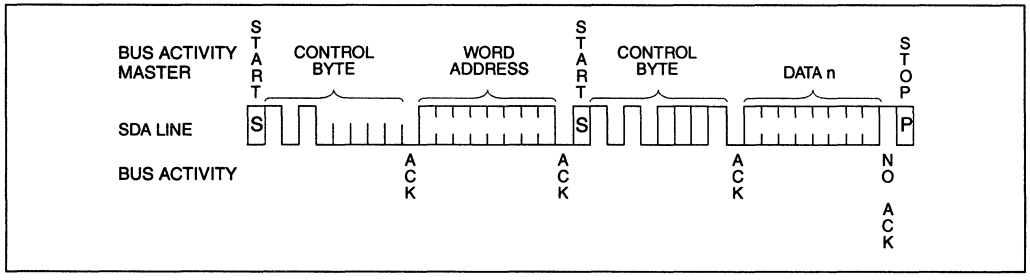
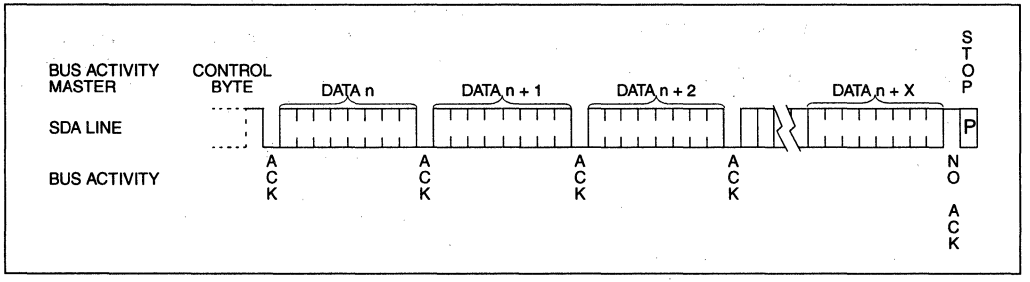


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bi-Directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2KΩ for 400 kHz).

For normal data transfer in the Bi-Directional Mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL

This pin is the clock input for the Bi-Directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit Only Mode to the Bi-Directional Mode. It must remain high for the chip to continue operation in the Transmit Only Mode.

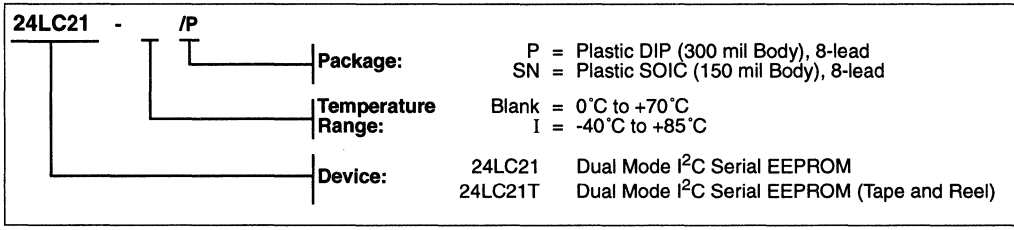
8.3 VCLK

This pin is the clock input for the Transmit Only Mode. In the Transmit Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-Directional Mode, a high logic level is required on this pin to enable write capability.

NOTES:

24LC21 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24LC21A

1K 2.5V Dual Mode I²C™ Serial EEPROM

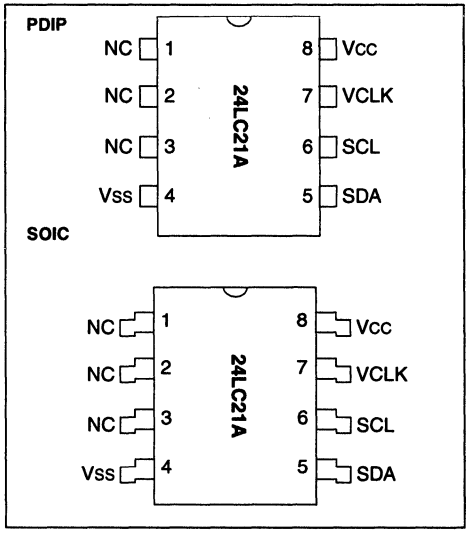
FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification, including recovery to DDC1
- Pin and function compatible with 24LC21
- Low power CMOS technology
  - 1 mA typical active current
  - 10 µA standby current typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to eight bytes
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- ESD Protection > 4000V
- 8-pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

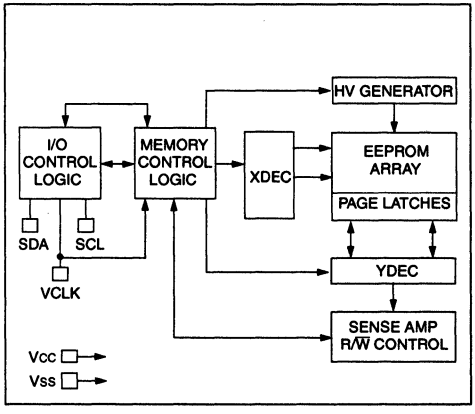
DESCRIPTION

The Microchip Technology Inc. 24LC21A is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit-Only Mode and Bi-directional Mode. Upon power-up, the device will be in the Transmit-Only Mode, sending a serial bit stream of the memory array from 00h to 7Fh, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the transition mode, and look for a valid control byte on the I²C bus. If it detects a valid control byte from the master, it will switch into Bi-directional Mode, with byte selectable read/write capability of the memory array using SCL. If no control byte is received, the device will revert to the Transmit-Only Mode after it receives 128 consecutive VCLK pulses while the SCL pin is idle. The 24LC21A is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

PACKAGE TYPES



BLOCK DIAGRAM



DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bi-directional Mode)
VCLK	Serial Clock (Transmit-Only Mode)
VCC	+2.5V to 5.5V Power Supply
NC	No Connection

TABLE 1-2: DC CHARACTERISTICS

VCC = +2.5V to 5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb =-40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC	—	V	
Low level input voltage	VIL	—	0.3 VCC	V	
Input levels on VCLK pin:					
High level input voltage	VIH	2.0	—	V	VCC ≥ 2.7V (Note)
Low level input voltage	VIL	—	0.2 VCC	V	VCC < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL1	—	0.4	V	IOL = 3 mA, VCC = 2.5V (Note)
Low level output voltage	VOL2	—	0.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	Cin, Cout	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V
	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	30	µA	VCC = 3.0V, SDA = SCL = VCC
		—	100	µA	VCC = 5.5V, SDA = SCL = VCC VCLK = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc= 2.5-5.5V Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	1000	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

The 24LC21A is designed to comply to the DDC Standard proposed by VESA (Figure 3-3) with the exception that it is not Access.bus capable. It operates in two modes, the Transmit-Only Mode and the Bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input but sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bi-directional Mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bi-directional Mode. Otherwise, it will revert to the Transmit-Only Mode after it sees 128 VCLK pulses.

2.1 Transmit-Only Mode

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional 2-wire protocol for continuous transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (Section 2.2). In this mode, data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. After address 7Fh in the memory array is transmitted, the internal address pointers will wrap around to the first memory location (00h) and continue. The Bi-directional Mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.2 Initialization Procedure

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit in address 00h. (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

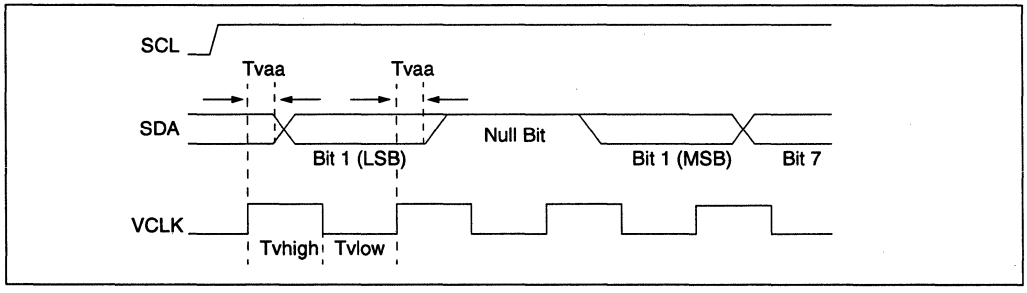
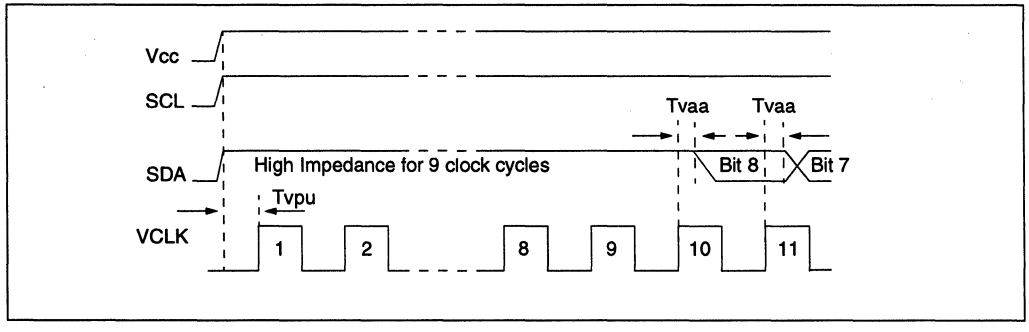


FIGURE 2-2: DEVICE INITIALIZATION



3.0 BI-DIRECTIONAL MODE

Before the 24LC21A can be switched into the Bi-directional Mode (Figure 3-1), it must enter the transition mode, which is done by applying a valid high to low transition on the Bi-directional Mode Clock (SCL). As soon it enters the transition mode, it looks for a control byte 1010 000X on the I^2C™ bus, and starts to count pulses on VCLK. Any high to low transition on the SCL line will reset the count. If it sees a pulse count of 128 on VCLK while the SCL line is idle, it will revert back to the Transmit-Only Mode, and transmit its contents starting with the most significant bit in address 00h. However, if it detects the control byte on the I^2C™ bus, (Figure 3-2) it will switch to the in the Bi-directional Mode. Once the device has made the transition to the Bi-directional mode, the only way to switch the device back to the Transmit-Only Mode is to remove power from the device. The mode transition process is shown in detail in Figure 3-3.

Once the device has switched into the Bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire Bi-directional data transmission protocol (I^2C™). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the 24LC21A acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bi-directional mode, the 24LC21A only responds to commands for device 1010 000X.

FIGURE 3-1: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE

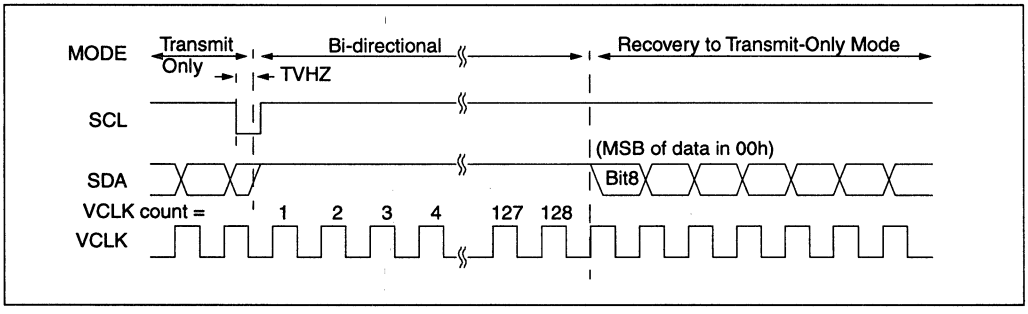


FIGURE 3-2: SUCCESSFUL MODE TRANSITION TO BI-DIRECTIONAL MODE

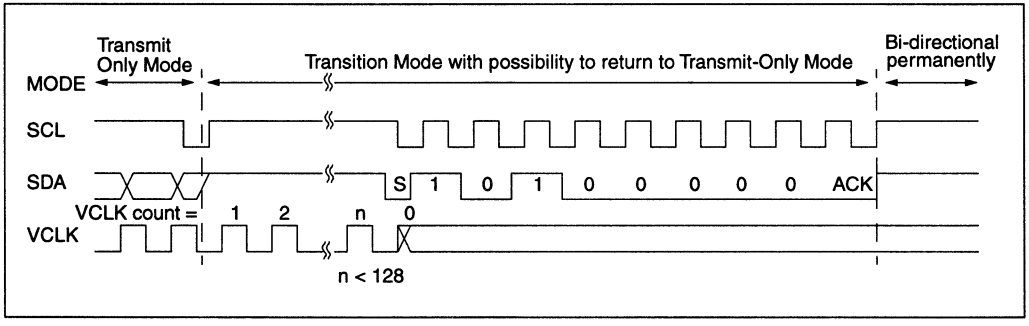
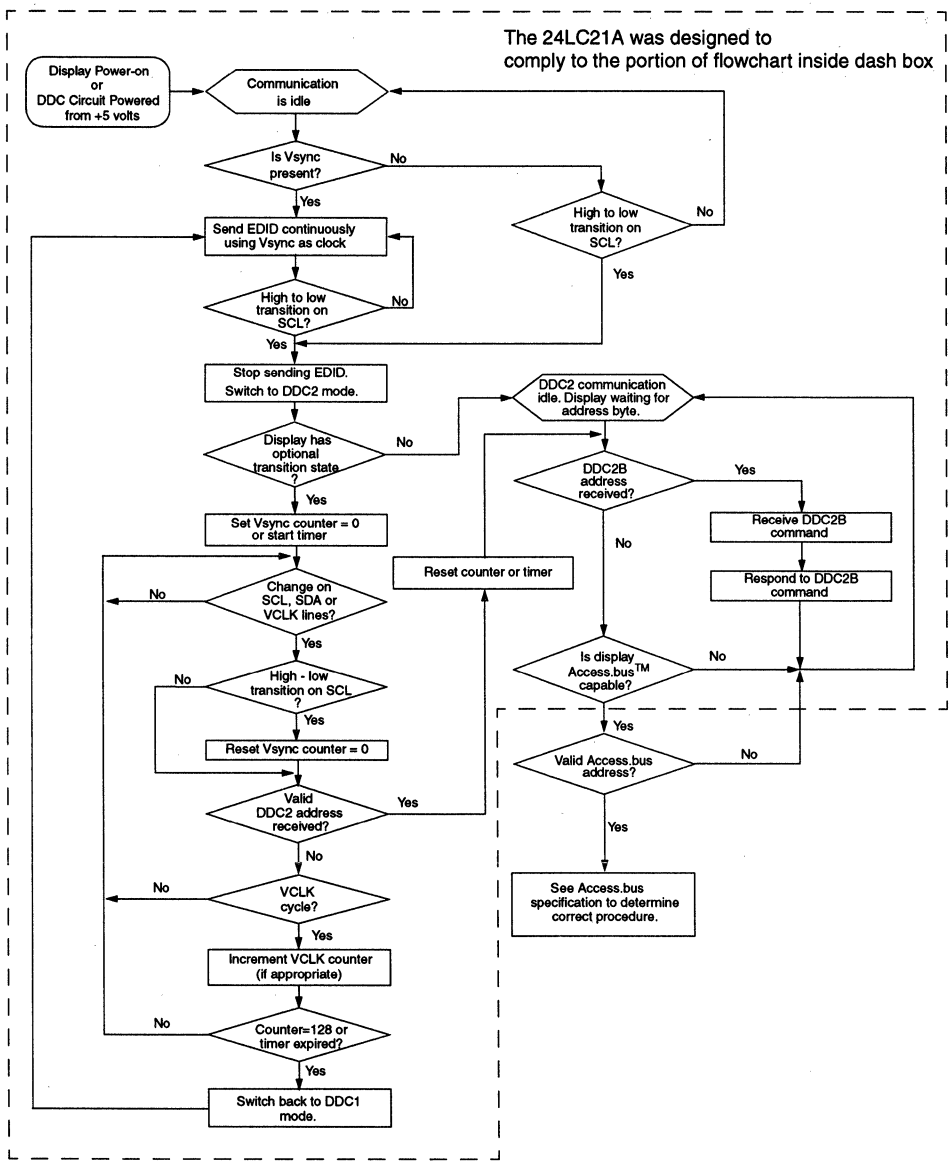


FIGURE 3-3: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA



Note 1: The base flowchart is copyright © 1993, 1994, 1995 Video Electronic Standard Association (VESA) from VESA's Display Data Channel (DDC) Standard Proposal ver. 2p rev. 0, used by permission of VESA.

2: The dash box and text "The 24LC21A and... inside dash box." are added by Microchip Technology, Inc.

3: Vsync signal is normally used to derive a signal for VCLK pin on the 24LC21A.

3.1 Bi-directional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-4).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

3.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

Note: Once switched into Bi-directional Mode, the 24LC21A will remain in that mode until power is removed. Removing power is the only way to reset the 24LC21A into the Transmit-only mode.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC21A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-4: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

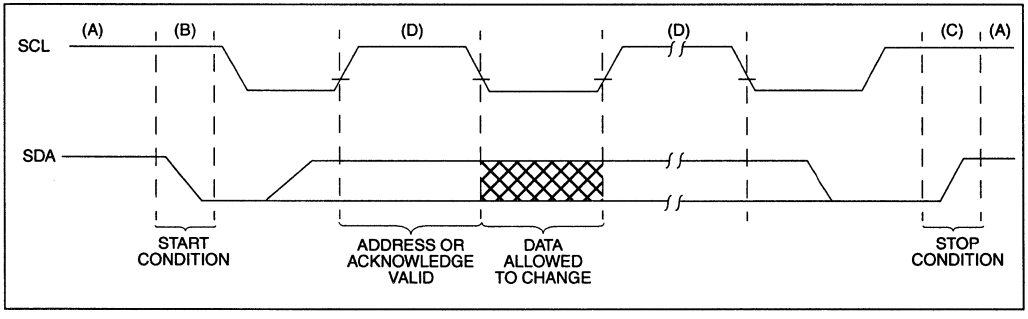


FIGURE 3-5: BUS TIMING START/STOP

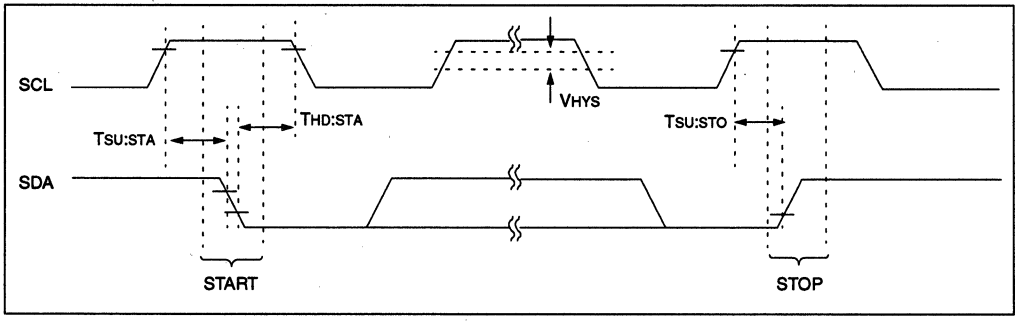
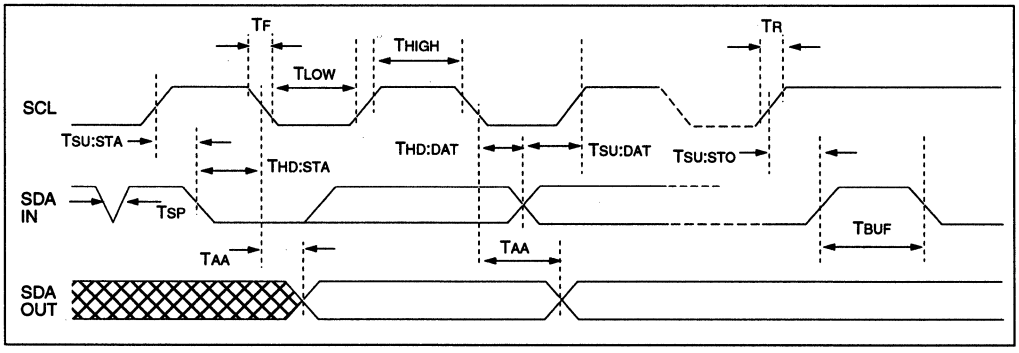


FIGURE 3-6: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

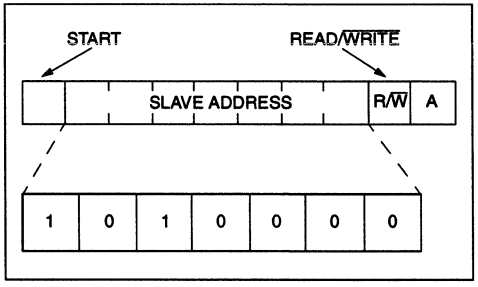
After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010000) for the 24LC21A.

The eighth bit of slave address determines whether the master device wants to read or write to the 24LC21A (Figure 3-7).

The 24LC21A monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Slave Address	R/$\overline{W}$
Read	1010000	1
Write	1010000	0

FIGURE 3-7: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the slave address (four bits), three zero bits (000) and the R/$\overline{W}$ bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC21A. After receiving another acknowledge signal from the 24LC21A the master device will transmit the data word to be written into the addressed memory location. The 24LC21A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC21A will not generate acknowledge signals (Figure 4-1).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC21A in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC21A which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-3).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

FIGURE 4-1: BYTE WRITE

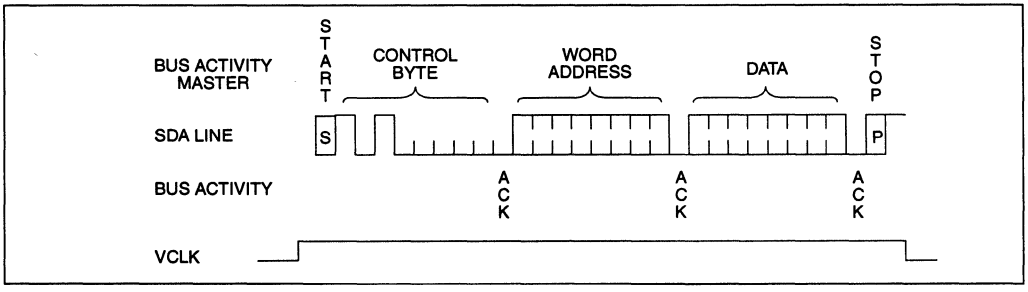


FIGURE 4-2: VCLK WRITE ENABLE TIMING

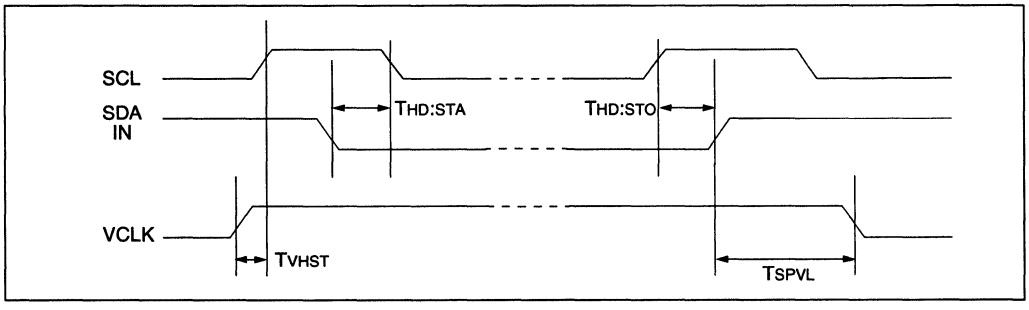
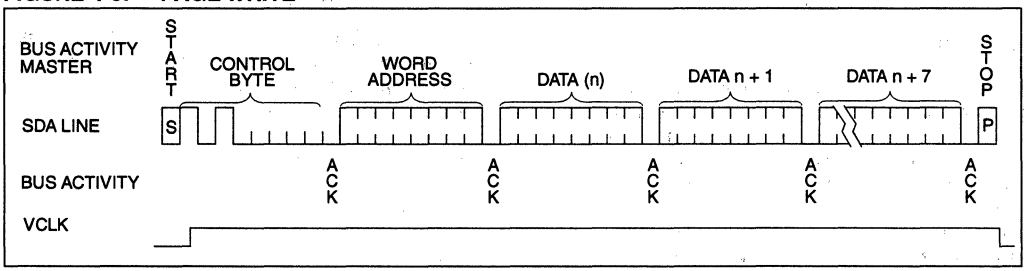


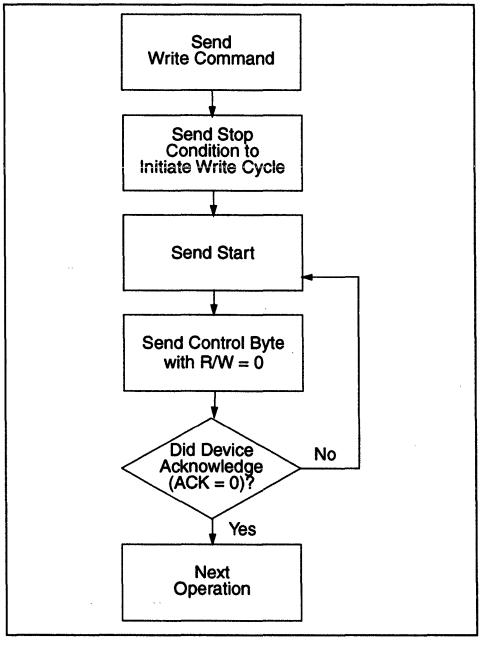
FIGURE 4-3: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

When using the 24LC21A in the Bi-directional Mode, the VCLK pin can be used as a write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to V_{SS} would allow the 24LC21A to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

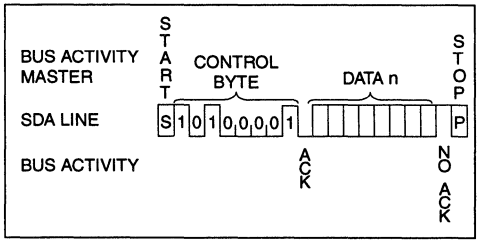
7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LC21A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC21A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC21A discontinues transmission (Figure 7-1).

FIGURE 7-1: CURRENT ADDRESS READ



7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC21A as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC21A will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC21A discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC21A transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC21A to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LC21A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC21A employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SDA, SCL and VCLK inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-2: RANDOM READ

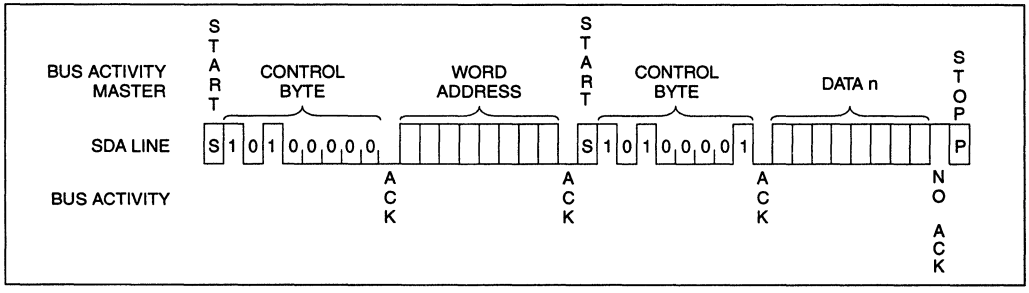
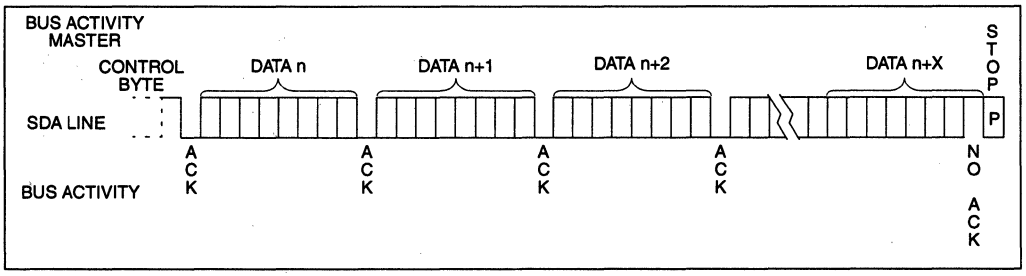


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer in the Bi-directional Mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL

This pin is the clock input for the Bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the Bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

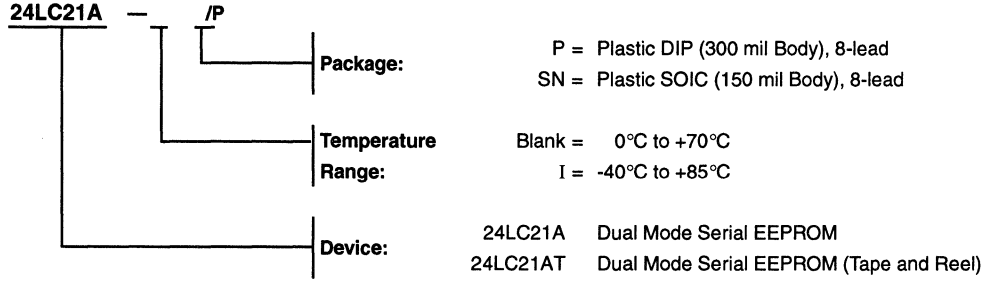
8.3 VCLK

This pin is the clock input for the Transmit-Only Mode (DDC1). In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-directional Mode, a high logic level is required on this pin to enable write capability.

NOTES:

24LC21A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LCS21

1K 2.5V Dual Mode I²C™ Serial EEPROM

FEATURES

- Completely implements DDC1™/DDC2™ interface for monitor identification
- Hardware write-protect pin
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible (SCL)
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 100 kHz (2.5V) and 400 kHz (5V) compatibility (SCL)
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

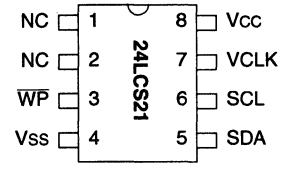
DESCRIPTION

The Microchip Technology Inc. 24LCS21 is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit Only Mode and bi-directional Mode. Upon power-up, the device will be in the Transmit Only Mode, sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the bi-directional Mode, with byte selectable read/write capability of the memory array in standard I²C protocol.

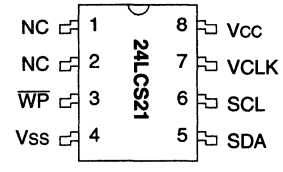
The 24LCS21 also enables the user to write-protect the entire memory contents using its write-protect pin. The 24LCS21 is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

PACKAGE TYPES

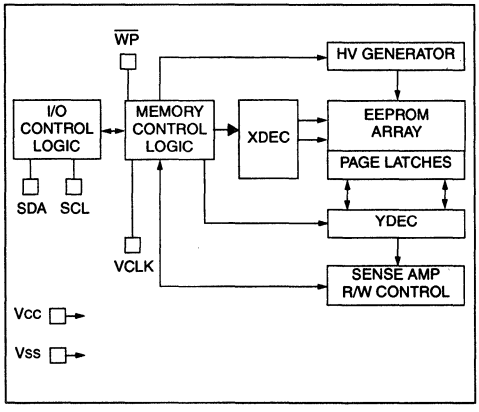
PDIP



SOIC



BLOCK DIAGRAM



DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{WP}$	Write Protect (active low)
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bi-directional Mode)
VCLK	Serial Clock (Transmit-Only Mode)
VCC	+2.5V to 5.5V Power Supply
NC	No Connection

TABLE 1-2: DC CHARACTERISTICS

	VCC = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC		V	
Low level input voltage	VIL		0.3 VCC	V	
Input levels on VCLK pin:					
High level input voltage	VIH	2.0	0.8	V	VCC ≥ 2.7V (Note)
Low level input voltage	VIL		0.2 VCC	V	VCC < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL1		0.4	V	IOL = 3 mA, VCC = 2.5V (Note 1)
Low level output voltage	VOL2		0.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	CINT		10	pF	VCC = 5.0V (Note1), Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Read	—	1	mA	
Standby current	ICCS	—	30	µA	VCC = 3.0V, SDA = SCL = VCC
			100	µA	VCC = 5.5V, SDA = SCL = VCC VCLK = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc= 2.5-5.5V		Vcc= 4.5 - 5.5V		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	100	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	
Endurance	—	1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

The 24LCS21 operates in two modes, the Transmit-Only Mode and the bi-directional Mode. There is a separate two wire protocol to support each mode, each having a separate clock input but sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the bi-directional Mode. The only way to switch the device back to the Transmit-Only Mode is to remove power from the device.

2.1 Transmit-Only Mode

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional two wire protocol for continuous transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (see Initialization Procedure, below). In this mode, data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the internal address pointers will wrap around to the first memory location (00H) and continue. The bi-directional Mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.2 Initialization Procedure

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit in address 00h. (Figure 2-2).

FIGURE 2-1: TRANSMIT ONLY MODE

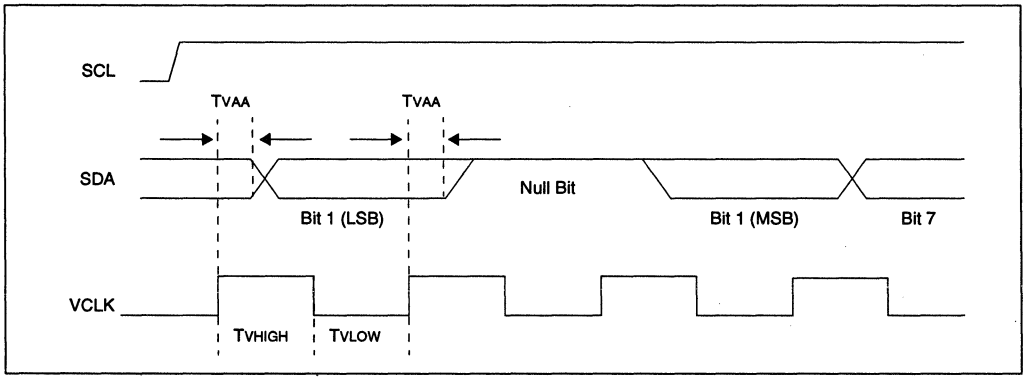
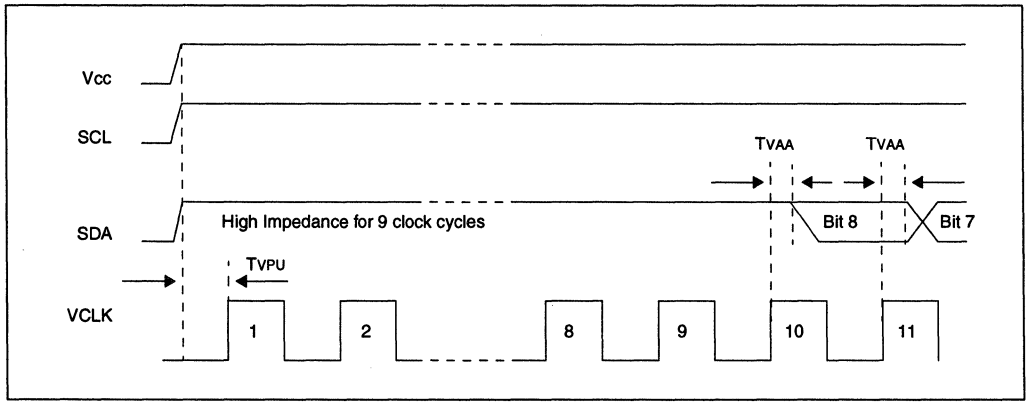


FIGURE 2-2: DEVICE INITIALIZATION



3.0 BI-DIRECTIONAL MODE

The 24LCS21 can be switched into the bi-directional Mode (Figure 3-1) by applying a valid high to low transition on the bi-directional Mode Clock (SCL). When the device has been switched into the bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire bi-directional data transmission protocol (I^2C™). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the bi-directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the 24LCS21 acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

In this mode, the 24LCS21 only responds to commands for device 1010 000X.

3.1 Bi-directional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-2).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

3.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

FIGURE 3-1: MODE TRANSITION

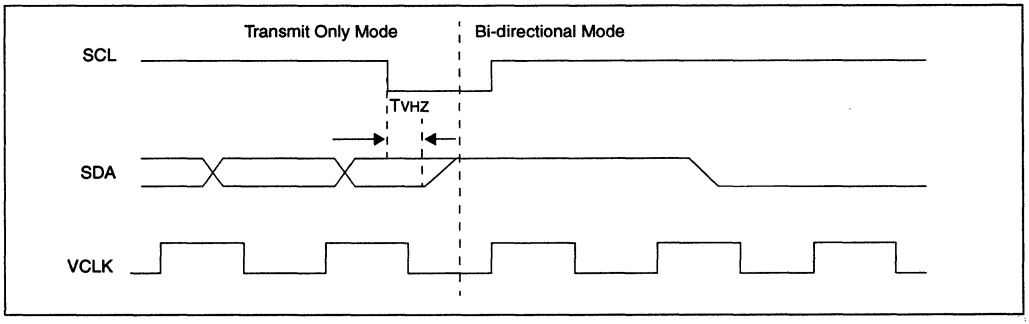
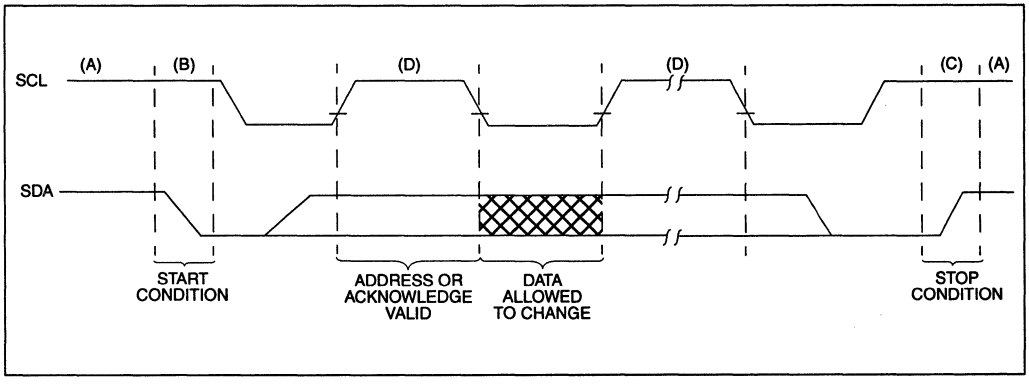


FIGURE 3-2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

Note: Once switched into bi-directional Mode, the 24LCS21 will remain in that mode until power goes away. Removing power is the only way to reset the 24LCS21 into the Transmit-only mode.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LCS21 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-3: BUS TIMING START/STOP

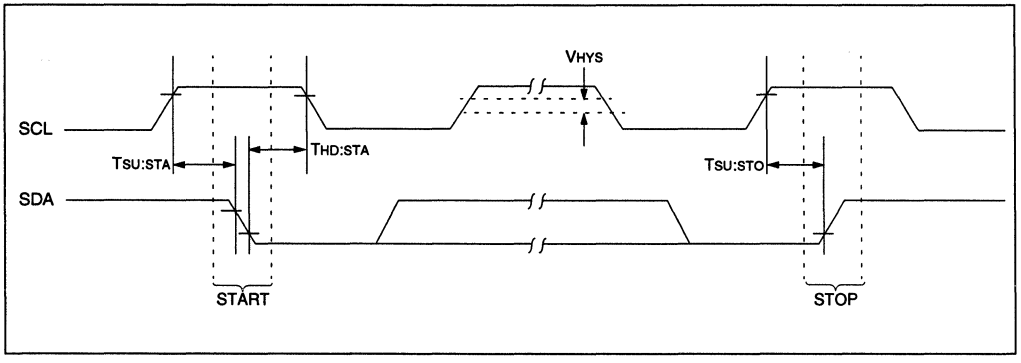
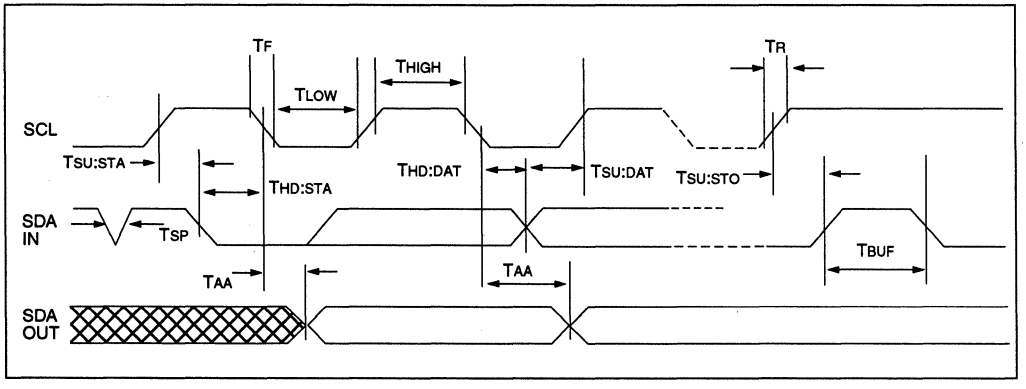


FIGURE 3-4: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

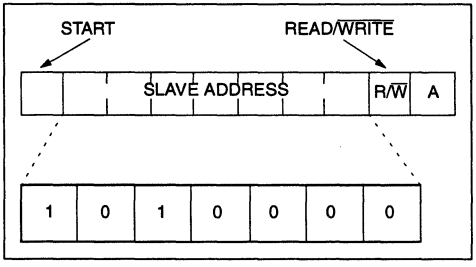
After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010000) for the 24LCS21.

The eighth bit of slave address determines whether the master device wants to read or write to the 24LCS21 (Figure 3-5).

The 24LCS21 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Slave Address	R/$\overline{W}$
Read	1010000	1
Write	1010000	0

FIGURE 3-5: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the slave address (4 bits), three zero bits (000) and the R/$\overline{W}$ bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LCS21. After receiving another acknowledge signal from the 24LCS21 the master device will transmit the data word to be written into the addressed memory location. The 24LCS21 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LCS21 will not generate acknowledge signals (Figure 4-1).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

FIGURE 4-1: BYTE WRITE

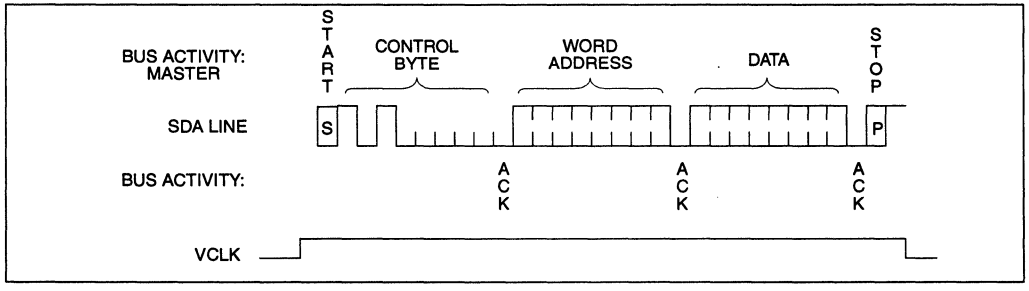
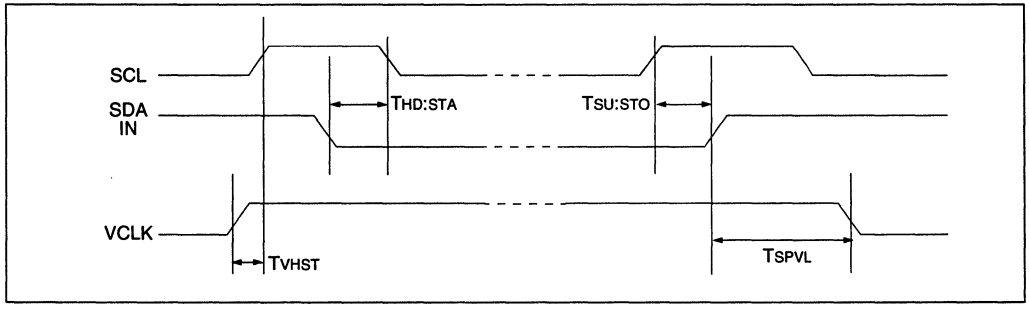


FIGURE 4-2: VCLK WRITE ENABLE TIMING



4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LCS21 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LCS21 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 5-2).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW

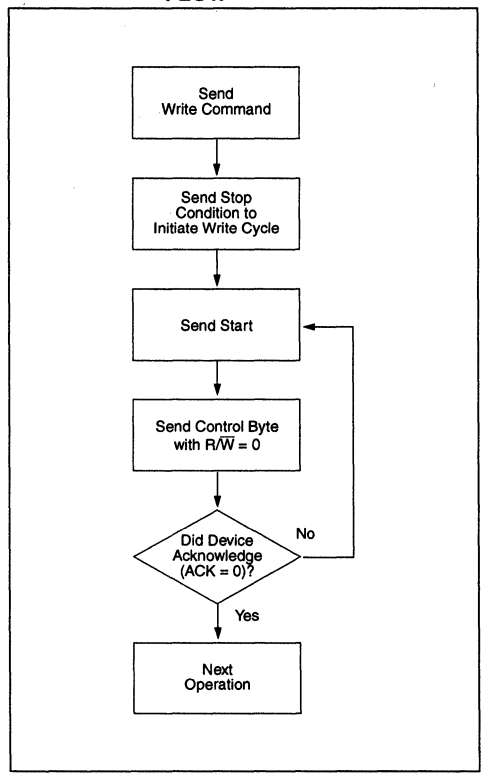
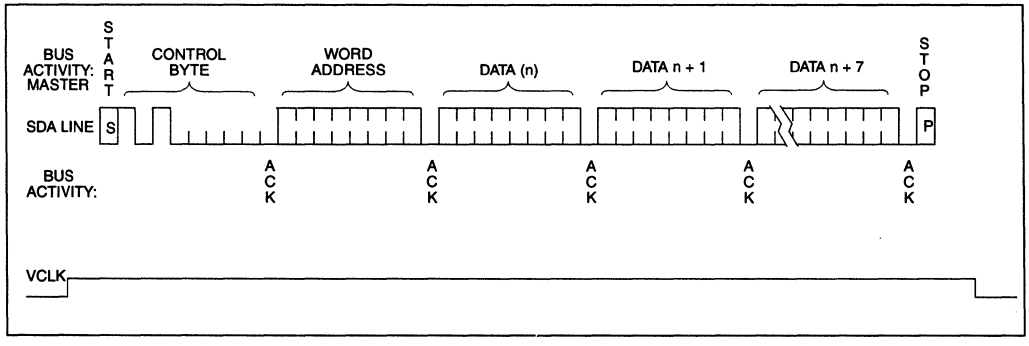


FIGURE 5-2: PAGE WRITE



6.0 WRITE PROTECTION

When using the 24LCS21 in the bi-directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the 24LCS21 to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

Additionally, Pin 3 performs a flexible write protect function. The 24LCS21 contains a write-protection control fuse whose factory default state is cleared. Writing any data to address 7Fh (normally the checksum in DDC applications) sets the fuse which enables the $\overline{WP}$ pin. Until this fuse is set, the 24LCS21 is always write enabled (if VCLK = 1). After the fuse is set, the write capability of the 24LCS21 is determined by $\overline{WP}$ (Figure 6-1).

FIGURE 6-1: WRITE PROTECT TRUTH TABLE

VCLK	$\overline{WP}$	Add. 7Fh Written	Mode
0	X	X	Read Only
1	X	No	R/$\overline{W}$
1	1/open	Yes	R/$\overline{W}$
1	0	Yes	Read Only

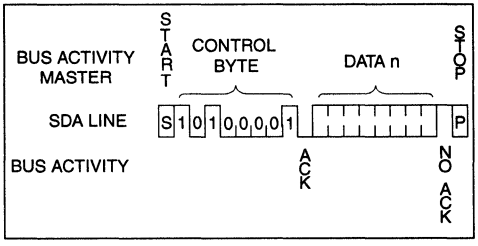
7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LCS21 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LCS21 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21 discontinues transmission (Figure 7-1).

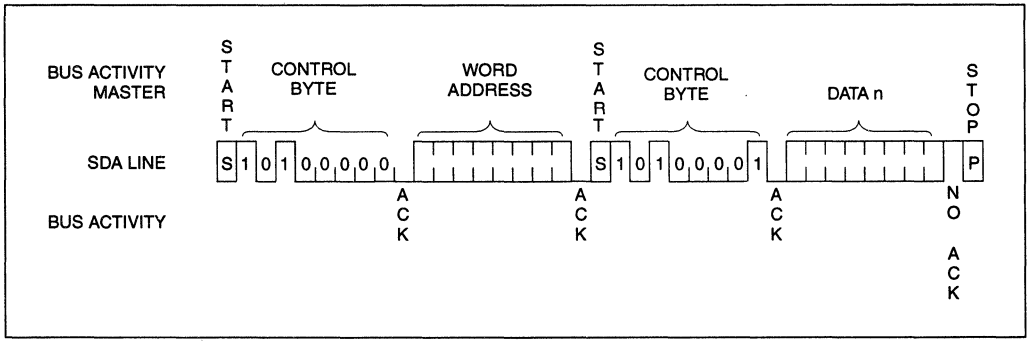
FIGURE 7-1: CURRENT ADDRESS READ



7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LCS21 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LCS21 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21 discontinues transmission (Figure 7-2).

FIGURE 7-2: RANDOM READ



7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LCS21 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LCS21 to transmit the next sequentially addressed 8-bit word (Figure 8-1).

To provide sequential reads the 24LCS21 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LCS21 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SDA, SCL and VCLK inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

8.0 PIN DESCRIPTIONS

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer in the bi-directional Mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL

This pin is the clock input for the bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit Only Mode to the bi-directional Mode. It must remain high for the chip to continue operation in the Transmit Only Mode.

8.3 VCLK

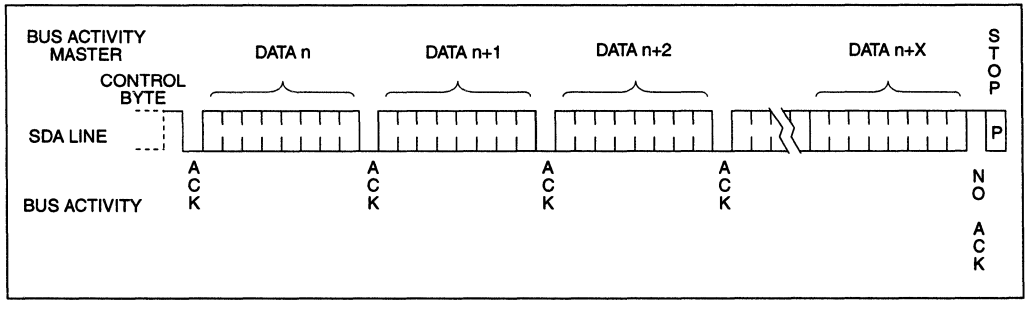
This pin is the clock input for the Transmit Only Mode (DDC1). In the Transmit Only Mode, each bit is clocked out on the rising edge of this signal. In the bi-directional Mode, a high logic level is required on this pin to enable write capability.

8.4 $\overline{WP}$

This pin is used for flexible write protection of the 24LCS21. When the last memory location (7Fh) is written with any data, this pin is enabled and determines the write capability of the 24LCS21 (Figure 6-1).

The $\overline{WP}$ pin has an internal pull up resistor which will allow write capability (assuming VCLK = 1) at all times if this pin is floated.

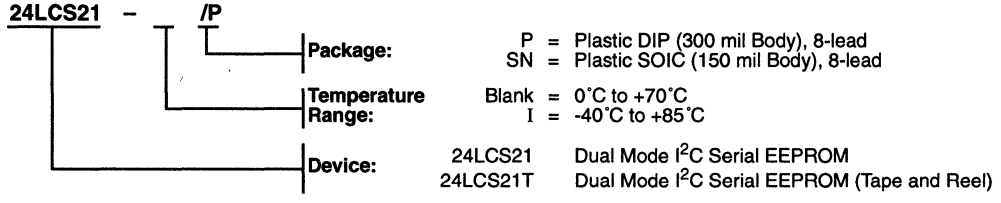
FIGURE 8-1: SEQUENTIAL READ



NOTES:

24LCS21 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LCS21A

1K 2.5V Dual Mode I²C™ Serial EEPROM

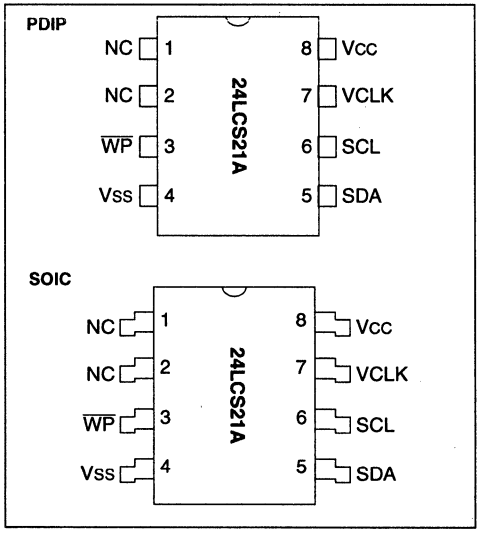
FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification, including recovery to DDC1
- Low power CMOS technology
  - 1 mA typical active current
  - 10 µA standby current typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Hardware write-protect pin
- Page-write buffer for up to eight bytes
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- ESD Protection > 4000V
- 8-pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +70°C

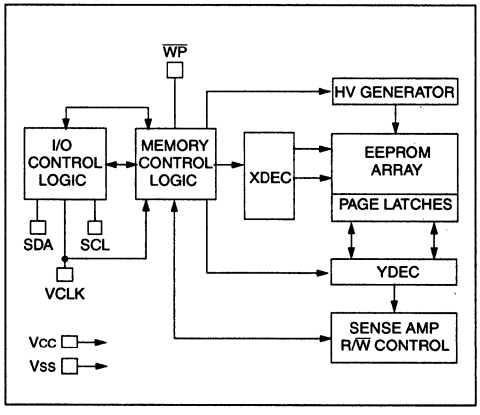
DESCRIPTION

The Microchip Technology Inc. 24LCS21A is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit-Only Mode and Bi-directional Mode. Upon power-up, the device will be in the Transmit-Only Mode, sending a serial bit stream of the memory array from 00h to 7Fh, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the transition mode, and look for a valid control byte on the I²C bus. If it detects a valid control byte from the master, it will switch into Bi-directional Mode, with byte selectable read/write capability of the memory array using SCL. If no control byte is received, the device will revert to the Transmit-Only Mode after it receives 128 consecutive VCLK pulses while the SCL pin is idle. The 24LCS21A also enables the user to write-protect the entire memory array using its write-protect pin. The 24LCS21A is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

PACKAGE TYPES



BLOCK DIAGRAM



DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{WP}$	Write Protect (active low)
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bi-directional Mode)
VCLK	Serial Clock (Transmit-Only Mode)
VCC	+2.5V to 5.5V Power Supply
NC	No Connection

TABLE 1-2: DC CHARACTERISTICS

VCC = +2.5V to 5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb =-40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
SCL and SDA pins:					
High level input voltage	VIH	0.7 VCC	—	V	
Low level input voltage	VIL	—	0.3 VCC	V	
Input levels on VCLK pin:					
High level input voltage	VIH	2.0	—	V	VCC ≥ 2.7V (Note)
Low level input voltage	VIL	—	0.2 VCC	V	VCC < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	(Note)
Low level output voltage	VOL1	—	0.4	V	IOL = 3 mA, VCC = 2.5V (Note)
Low level output voltage	VOL2	—	0.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to VCC
Pin capacitance (all inputs/outputs)	Cin, Cout	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V
	ICC Read	—	1	mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	30	µA	VCC = 3.0V, SDA = SCL = VCC
		—	100	µA	VCC = 5.5V, SDA = SCL = VCC VCLK = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc= 2.5-4.5V Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	1000	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

The 24LCS21A is designed to comply to the DDC Standard proposed by VESA (Figure 3-3) with the exception that it is not Access.bus capable. It operates in two modes, the Transmit-Only Mode and the Bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input but sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bi-directional Mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bi-directional Mode. Otherwise, it will revert to the Transmit-Only Mode after it sees 128 VCLK pulses.

2.1 Transmit-Only Mode

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional 2-wire protocol for continuous transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (Section 2.2). In this mode, data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. After address 7Fh in the memory array is transmitted, the internal address pointers will wrap around to the first memory location (00h) and continue. The Bi-directional Mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.2 Initialization Procedure

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit in address 00h. (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

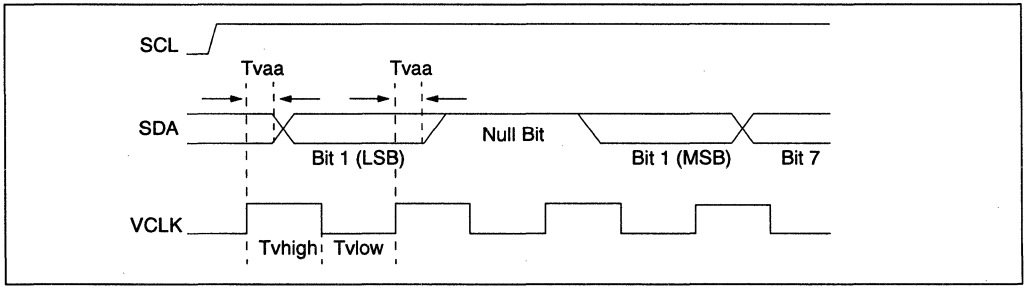
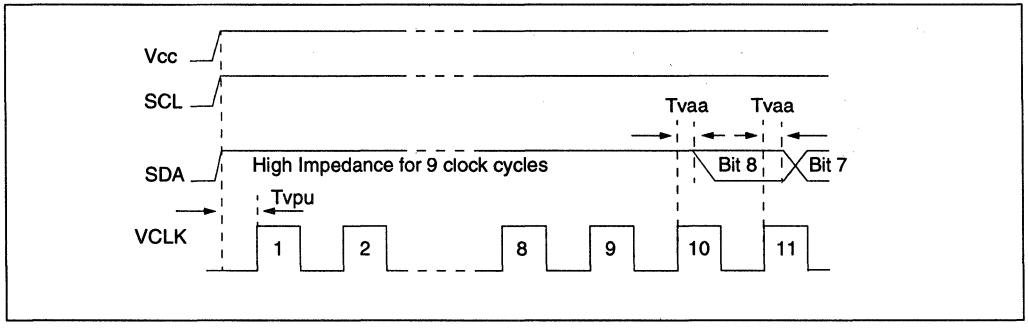


FIGURE 2-2: DEVICE INITIALIZATION



3.0 BI-DIRECTIONAL MODE

Before the 24LCS21A can be switched into the Bi-directional Mode (Figure 3-1), it must enter the transition mode, which is done by applying a valid high to low transition on the Bi-directional Mode Clock (SCL). As soon it enters the transition mode, it looks for a control byte 1010 000X on the I^2C™ bus, and starts to count pulses on VCLK. Any high to low transition on the SCL line will reset the count. If it sees a pulse count of 128 on VCLK while the SCL line is idle, it will revert back to the Transmit-Only Mode, and transmit its contents starting with the most significant bit in address 00h. However, if it detects the control byte on the I^2C™ bus, (Figure 3-2) it will switch to the in the Bi-directional Mode. Once the device has made the transition to the Bi-directional mode, the only way to switch the device back to the Transmit-Only Mode is to remove power from the device. The mode transition process is shown in detail in Figure 3-3.

Once the device has switched into the Bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire Bi-directional data transmission protocol (I^2C™). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the 24LCS21A acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bi-directional mode, the 24LCS21A only responds to commands for device 1010 000X.

FIGURE 3-1: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE

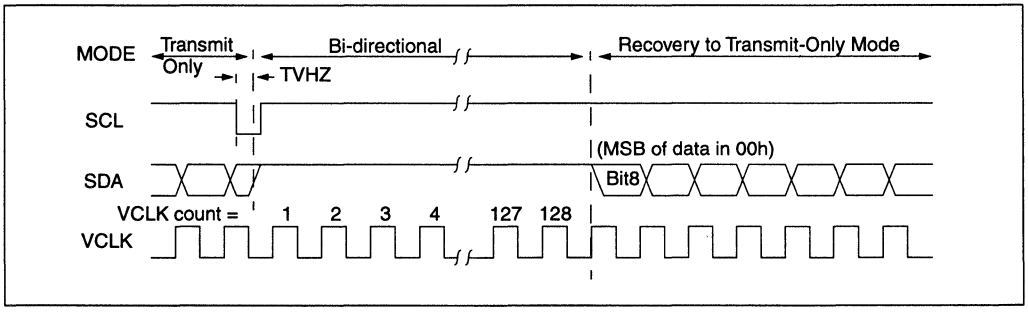


FIGURE 3-2: SUCCESSFUL MODE TRANSITION TO BI-DIRECTIONAL MODE

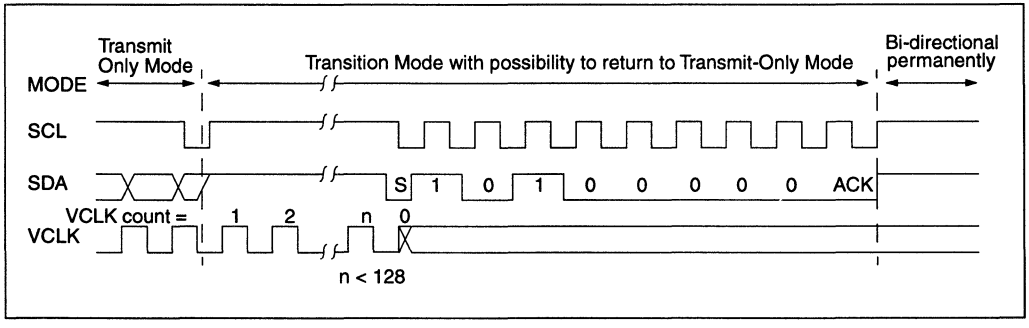
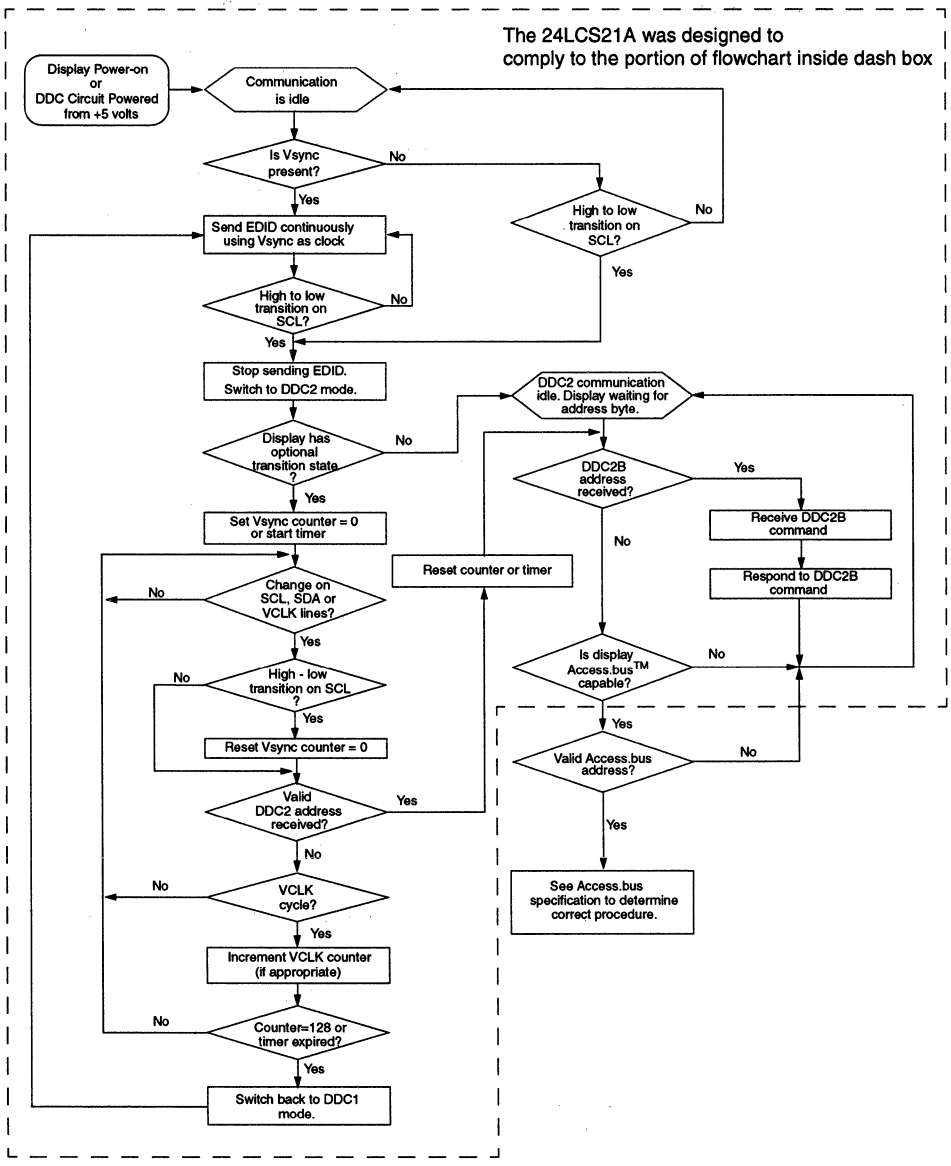


FIGURE 3-3: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA



Note 1: The base flowchart is copyright © 1993, 1994, 1995 Video Electronic Standard Association (VESA) from VESA's Display Data Channel (DDC) Standard Proposal ver. 2p rev. 0, used by permission of VESA.

2: The dash box and text "The 24LCS21A and... inside dash box." are added by Microchip Technology, Inc.

3: Vsync signal is normally used to derive a signal for VCLK pin on the 24LCS21A.

3.1 Bi-directional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-4).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

3.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

Note: Once switched into Bi-directional Mode, the 24LCS21A will remain in that mode until power is removed. Removing power is the only way to reset the 24LCS21A into the Transmit-only mode.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LCS21A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-4: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

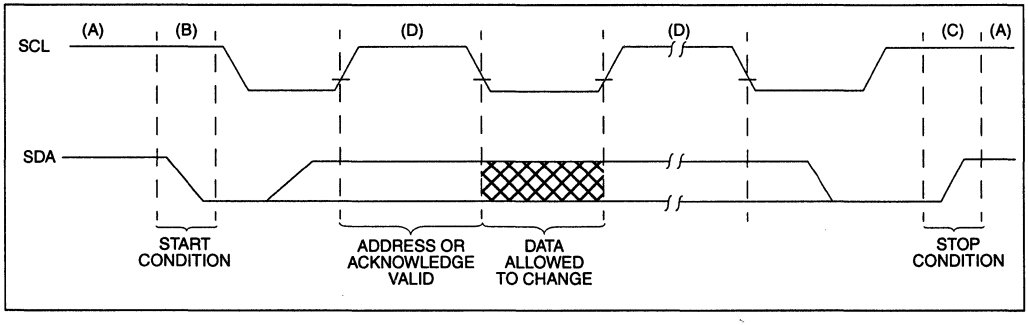


FIGURE 3-5: BUS TIMING START/STOP

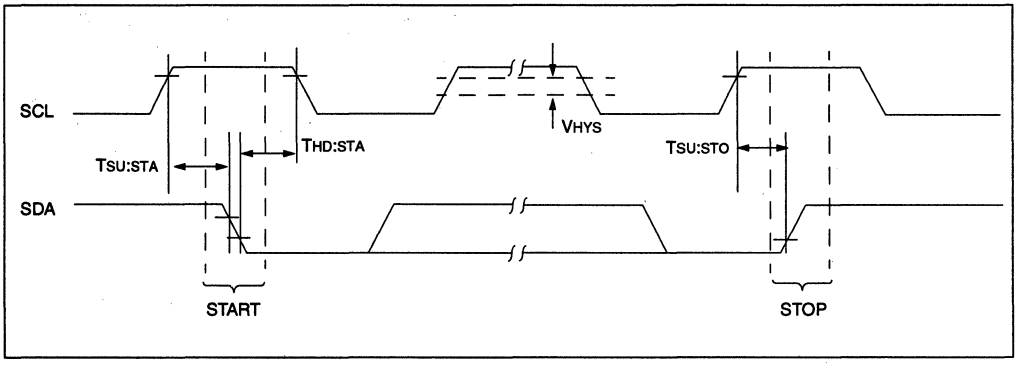
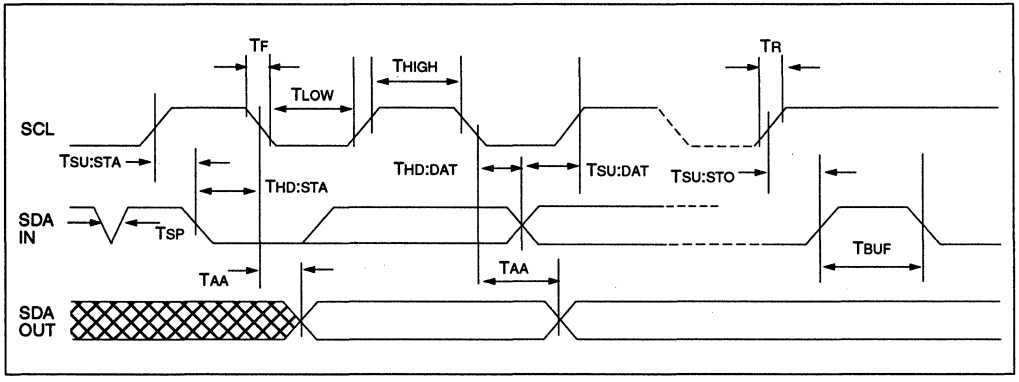


FIGURE 3-6: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

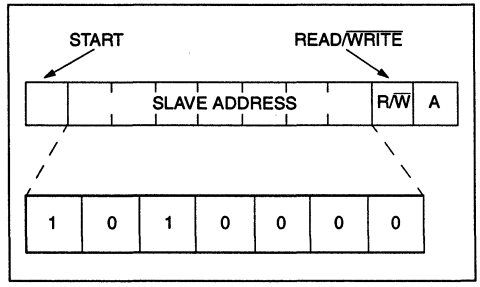
After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010000) for the 24LCS21A.

The eighth bit of slave address determines whether the master device wants to read or write to the 24LCS21A (Figure 3-7).

The 24LCS21A monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Slave Address	R/$\overline{W}$
Read	1010000	1
Write	1010000	0

FIGURE 3-7: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the slave address (four bits), three zero bits (000) and the R/$\overline{W}$ bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LCS21A. After receiving another acknowledge signal from the 24LCS21A the master device will transmit the data word to be written into the addressed memory location. The 24LCS21A acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LCS21A will not generate acknowledge signals (Figure 4-1).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LCS21A in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LCS21A which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 5-2).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high to low during the self-timed program operation will not halt programming of the device.

FIGURE 4-1: BYTE WRITE

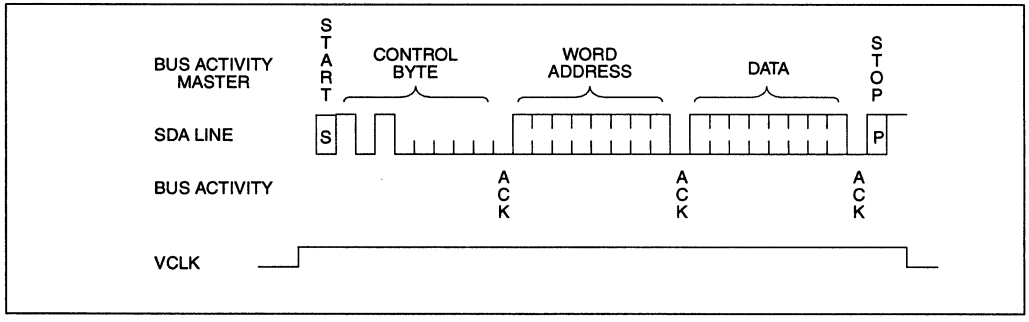
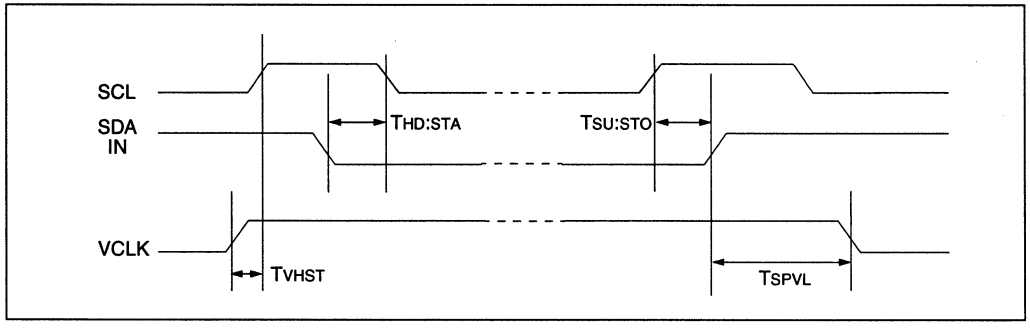


FIGURE 4-2: VCLK WRITE ENABLE TIMING



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW

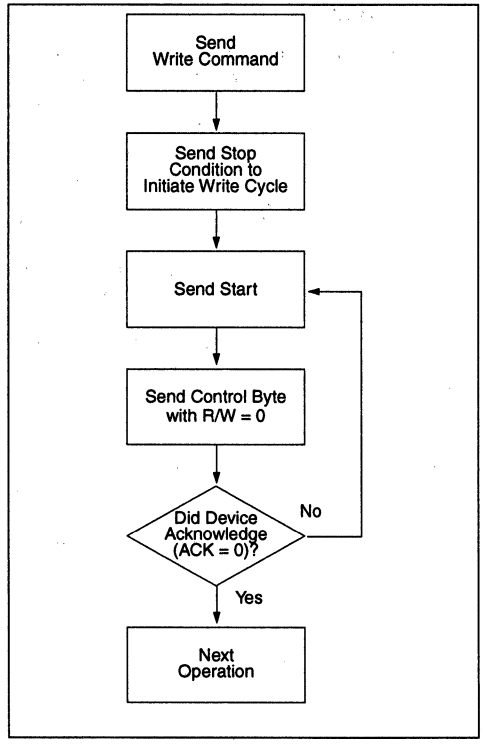
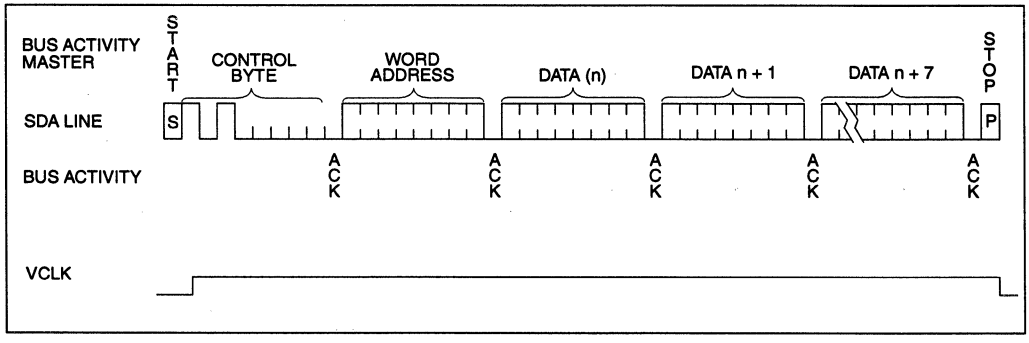


FIGURE 5-2: PAGE WRITE



6.0 WRITE PROTECTION

When using the 24LCS21A in the Bi-directional Mode, the VCLK pin can be used as a write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the 24LCS21A to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

Additionally, Pin three performs a flexible write protect function. The 24LCS21A contains a write-protection control fuse whose factory default state is cleared. Writing any data to address 7Fh (normally the checksum in DDC applications) sets the fuse which enables the $\overline{WP}$ pin. Until this fuse is set, the 24LCS21A is always write enabled (if VCLK = 1). After the fuse is set, the write capability of the 24LCS21A is determined by both VCLK and $\overline{WP}$ pins (Table 6-1).

TABLE 6-1: WRITE PROTECT TRUTH TABLE

VCLK	$\overline{WP}$	Address 7Fh Written	Mode for 00h - 7Fh
0	X	X	Read Only
1	X	No	R/$\overline{W}$
1	1/open	X	R/$\overline{W}$
1	0	Yes	Read Only

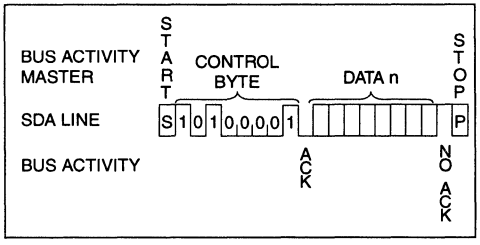
7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LCS21A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LCS21A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21A discontinues transmission (Figure 7-1).

FIGURE 7-1: CURRENT ADDRESS READ



7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LCS21A as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LCS21A will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LCS21A discontinues transmission (Figure 7-2).

FIGURE 7-2: RANDOM READ

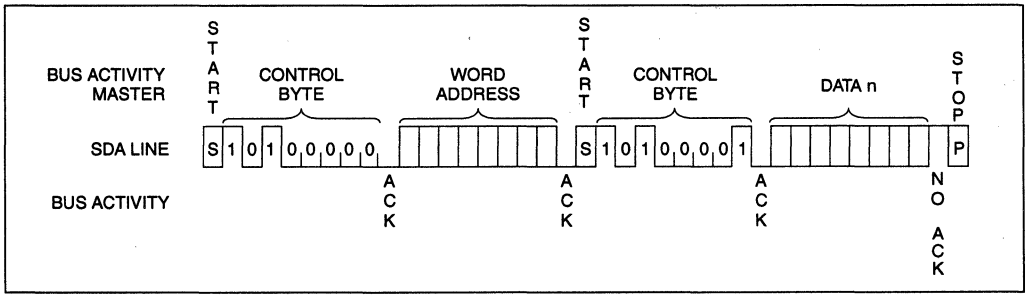
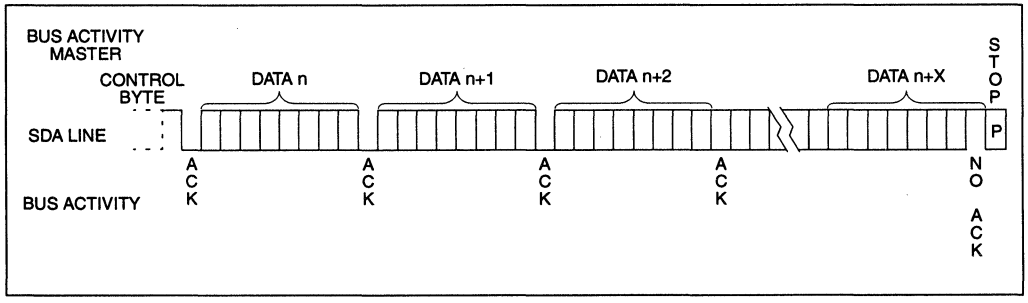


FIGURE 7-3: SEQUENTIAL READ



7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LCS21A transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LCS21A to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LCS21A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LCS21A employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SDA, SCL and VCLK inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

8.0 PIN DESCRIPTIONS

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10 KΩ for 100 kHz, 1 KΩ for 400 kHz).

For normal data transfer in the Bi-directional Mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL

This pin is the clock input for the Bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the Bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

8.3 VCLK

This pin is the clock input for the Transmit-Only Mode (DDC1). In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-directional Mode, a high logic level is required on this pin to enable write capability.

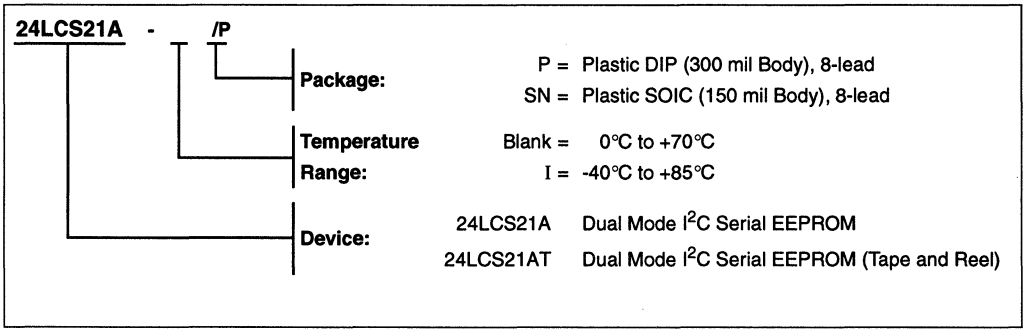
8.4 $\overline{WP}$

This pin is used for flexible write protection of the 24LCS21A. When the last memory location (7Fh) is written with any data, this pin is enabled and determines the write capability of the 24LCS21A (Table 6-1).

The $\overline{WP}$ pin has an internal pull up resistor which will allow write capability (assuming VCLK = 1) at all times if this pin is floated.

24LCS21A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

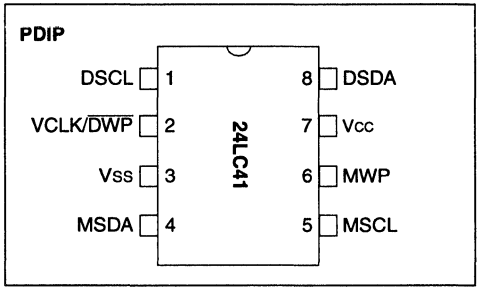
24LC41

1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM

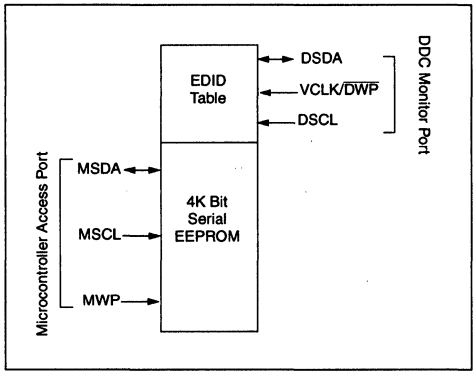
FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification
- Separate high speed 2-wire bus for microcontroller access to 4K-bit Serial EEPROM
- Low power CMOS technology
- 2 mA active current typical
- 20 µA standby current typical at 5.5V
- Dual 2-wire serial interface bus
- Hardware write-protect for both ports
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes (DDC port) or 16 bytes (4K Port)
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- 1,000,000 erase/write cycles guaranteed
- Data retention > 40 years
- 8-pin PDIP package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

PACKAGE TYPE



BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 24LC41 is a dual-port 128 x 8 and 512 x 8-bit Electrically Erasable PROM (EEPROM). This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Three modes of operation have been implemented:

- Transmit-Only Mode for the DDC Monitor Port
- Bi-directional Mode for the DDC Monitor Port
- Bi-directional, industry-standard 2-wire bus for the 4K Microcontroller Access Port

Upon power-up, the DDC Monitor Port will be in the Transmit-Only Mode, repeatedly sending a serial bit stream of the entire memory array contents, clocked by the VCLK/$\overline{DWP}$ pin. A valid high to low transition on the DSCL pin will cause the device to enter the bi-directional Mode, with byte-selectable read/write capability of the memory array. The 4K-bit microcontroller port is completely independent of the DDC port, therefore, it can be accessed continuously by a microcontroller without interrupting DDC transmission activity. The 24LC41 is available in a standard 8-pin PDIP package in both commercial and industrial temperature ranges.

DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
DSCL	Serial Clock for DDC Bi-directional Mode (DDC2)
DSDA	Serial Address and Data I/O (DDC Bus)
VCLK/$\overline{DWP}$	Serial Clock for DDC transmit-only mode (DDC1)/Write Protect
MSCL	Serial clock for 4K-bit MCU port
MSDA	Serial Address and Data I/O for 4K-bit MCU port
MWP	Hardware write-protect for 4K-bit MCU port
VSS	Ground
VCC	+2.5V to +5.5V power supply

TABLE 1-2: DC CHARACTERISTICS

	VCC = +2.5V to 5.5V Commercial (C): Industrial (I):		Tamb = 0°C to +70°C Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
DSCL, DSDA, MSCL & MSDA pins: High level input voltage Low level input voltage	 VIH VIL	 .7 VCC —	 — .3 VCC	 V V	
Input levels on VCLK/$\overline{DWP}$ pin: High level input voltage Low level input voltage	 VIH VIL	 2.0 —	 .8 .2 VCC	 V V	 VCC ≥ 2.7V (Note) VCC < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL1	—	.4	V	IOL = 3 mA, VCC = 2.5V (Note)
Low level output voltage	VOL2	—	.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN =.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT =.1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note), Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, DSCL or MSCL = 400 kHz
Standby current	ICCS	— —	60 200	µA µA	VCC = 3.0V, DSDA or MSDA = DSCL or MSCL = VCC VCC = 5.5V, DSDA or MSDA = DSCL or MSCL = VCC VCLK = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS (DDC MONITOR AND MICROCONTROLLER ACCESS PORTS)

DDC Monitor Port (Bi-directional Mode) and Microcontroller Access Port							
Parameter	**Symbol**	**Standard Mode**		**Vcc = 4.5 - 5.5V Fast Mode**		**Units**	**Remarks**
		Min	**Max**	**Min**	**Max**		
Clock frequency (DSCL and MSCL)	FCLK	—	100	—	400	kHz	
Clock high time (DSCL and MSCL)	THIGH	4000	—	600	—	ns	
Clock low time (DSCL and MSCL)	TLOW	4700	—	1300	—	ns	
DSCL, DSDA, MSCL & MSDA rise time	TR	—	1000	—	300	ns	(Note 1)
DSCL, DSDA, MSCL & MSDA fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + .1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (DSCL, DSDA, MSCL & MSDA pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
DDC Monitor Port Transmit-Only Mode Parameters							
Output valid from VCLK/$\overline{DWP}$	TVAA	—	2000	—	1000	ns	
VCLK/$\overline{DWP}$ high time	TVHIGH	4000	—	600	—	ns	
VCLK/$\overline{DWP}$ low time	TVLOW	4700	—	1300	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of DSCL or MSCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

2.1 DDC Monitor Port

The DDC Monitor Port operates in two modes, the Transmit-Only Mode and the bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input and sharing a common data line (DSDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the DSDA pin in response to a clock signal on the VCLK/$\overline{DWP}$ pin. The device will remain in this mode until a valid high to low transition is placed on the DSCL input. When a valid transition on DSCL is recognized, the device will switch into the bi-directional Mode. The only way to switch the device back to the Transmit-Only Mode is to remove power from the device.

2.1.1 TRANSMIT-ONLY MODE

The device will power up in the Transmit-Only Mode. This mode supports a unidirectional 2-wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (Section 2.1.2).

In this mode, data is transmitted on the DSDA pin in 8-bit bytes, each followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK/$\overline{DWP}$ pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted by most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The bi-directional Mode Clock (DSCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.1.2 INITIALIZATION PROCEDURE

After V_{CC} has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK/$\overline{DWP}$ pin must be given to the device for it to perform internal sychronization. During this period, the DSDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

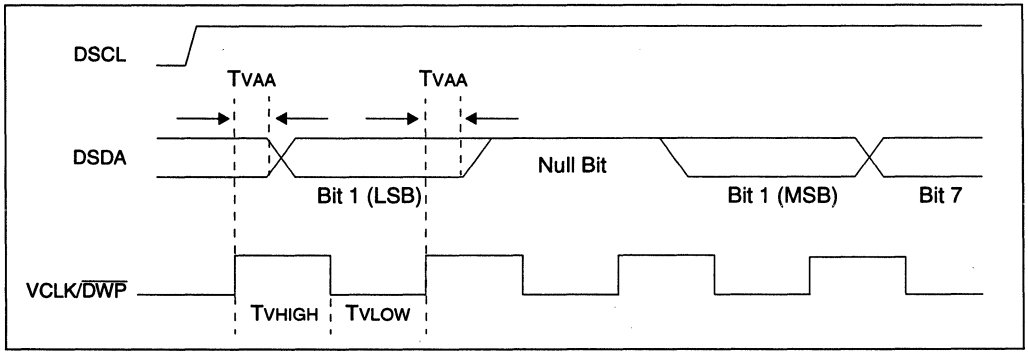
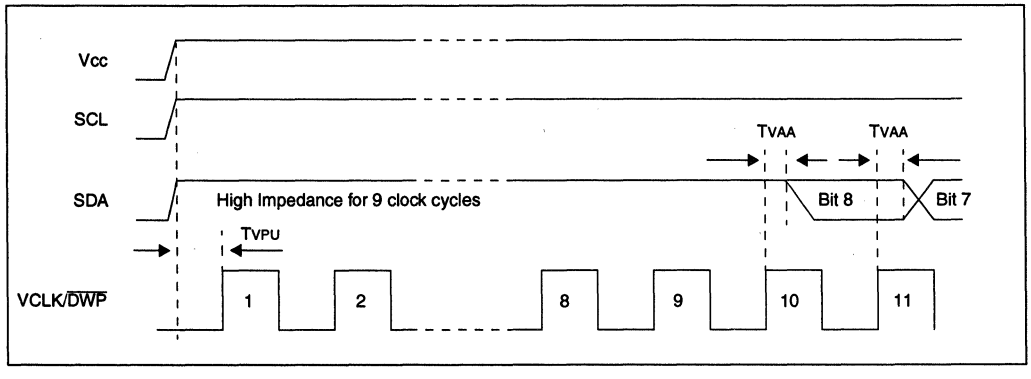


FIGURE 2-2: DEVICE INITIALIZATION



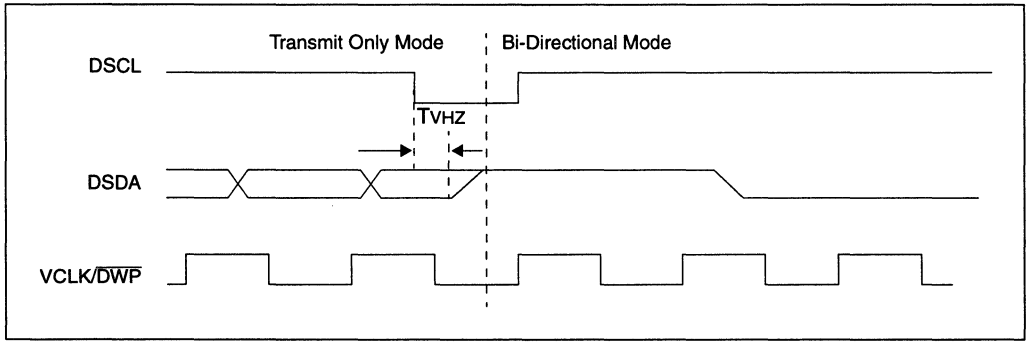
2.1.3 BI-DIRECTIONAL MODE

The DDC Monitor Port can be switched into the bi-directional Mode (Figure 2-3) by applying a valid high to low transition on the bi-directional Mode Clock (DSCL). When the device has been switched into the bi-directional Mode, the VCLK/$\overline{DWP}$ input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a 2-wire bi-directional data transmission protocol. In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the bi-directional Mode Clock (DSCL), controls access to the bus and generates the START and STOP conditions, while the DDC Monitor Port acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

2.2 Microcontroller Access Port

The Microcontroller Access Port supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (MSCL), controls the bus access, and generates the START and STOP conditions, while the Microcontroller Access Port works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

FIGURE 2-3: MODE TRANSITION



3.0 BI-DIRECTIONAL BUS CHARACTERISTICS

Characteristics for the bi-directional bus are identical for both the DDC Monitor Port (in bi-directional Mode) and the Microcontroller Access Port The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit

.

Note:	The microcontroller access port and the DDC Monitor Port (in bi-directional Mode) will not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the DSDA or MSDA line during the acknowledge clock pulse in such a way that the DSDA or MSDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The first part of the control byte consists of a 4-bit control code. This control code is set as 1010 for both read and write operations and is the same for both the DDC Monitor Port and Microcontroller Access Port. The next three bits of the control byte are block select bits (B1, B2, and B0). All three of these bits are don't care bits for the DDC Monitor Port. The B2 and B1 bits are don't care bits for the Microcontroller Access Port, and the B0 bit is used by the Microcontroller Access Port to select which of the two 256 word blocks of memory are to be accessed (Figure 3-4). The B0 bit is effectively the most significant bit of the word address. The last bit of the control byte defines the operation to be performed. When set to one, a read operation is selected; when set to zero, a write operation is selected. Following the start condition, the device monitors the DSDA or MSDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the device will select a read or a write operation. The DDC Monitor Port and Microcontroller Access Port can be accessed simultaneously because they are completely independent of one another.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXB0	1
Write	1010	XXB0	0

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

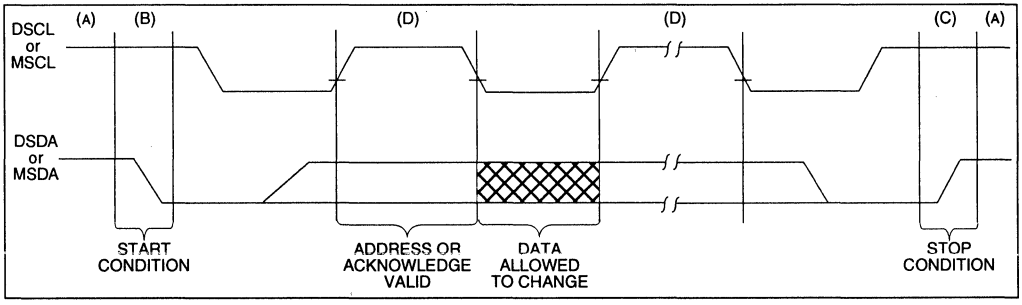


FIGURE 3-2: BUS TIMING START/STOP

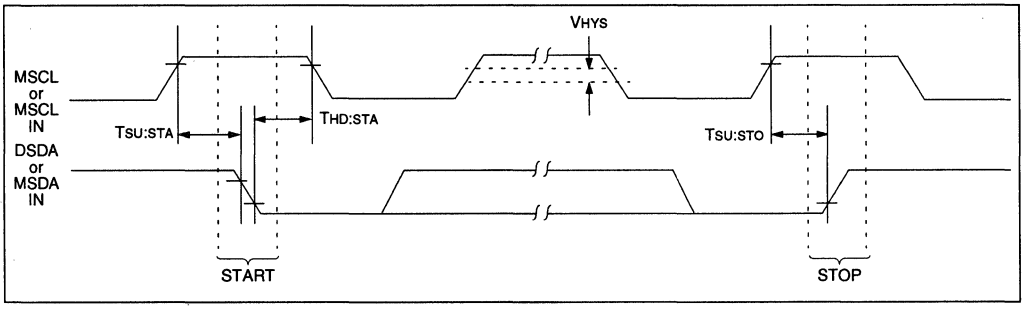


FIGURE 3-3: BUS TIMING DATA

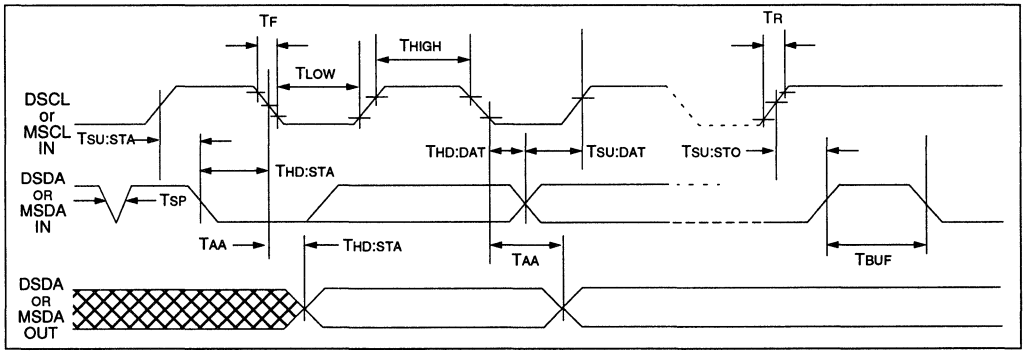
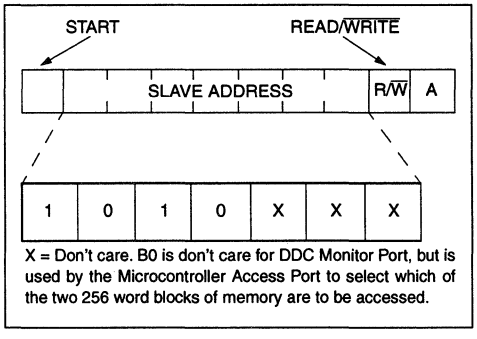


FIGURE 3-4: CONTROL BYTE ALLOCATION



X = Don't care. B0 is don't care for DDC Monitor Port, but is used by the Microcontroller Access Port to select which of the two 256 word blocks of memory are to be accessed.

4.0 WRITE OPERATION

Write operations are identical for the DDC Monitor Port (when in bi-directional Mode) and the Microcontroller Access Port, with the exception of the VCLK/$\overline{DWP}$ and MWP pins noted in the next sections. Data can be written using either a byte write or page write command. Write commands for the DDC Monitor Port and the Microcontroller Access Port are completely independent of one another.

4.1 Byte Write

Following the start signal from the master, the slave address (4-bits), the chip select bits (3-bits) and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the port. After receiving another acknowledge signal from the port, the master device will transmit the data word to be written into the addressed memory location. The port acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time, the port will not generate acknowledge signals (Figure 4-1).

For the DDC Monitor Port it is required that VCLK/$\overline{DWP}$ be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK/$\overline{DWP}$ can go low while the device is in its self-timed program operation and not affect programming.

For the Microcontroller Access Port, the MWP pin must be held to Vss during the entire write operation.

4.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the port in the same way as in a byte write. But, instead of generating a stop condition, the master transmits up to eight data bytes to the DDC Monitor Port or 16 bytes to the Microcontroller Access Port, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order 5-bits of the word address remains constant. If the master should transmit more than eight words to the DDC Monitor Port or 16 words to the Microcontroller Access Port prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

For the DDC Monitor Port, it is required that VCLK/$\overline{DWP}$ be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK/$\overline{DWP}$ can go low while the device is in its self-timed program operation and not affect programming.

For the Microcontroller Access Port, the MWP pin must be held to Vss during the entire write operation.

FIGURE 4-1: BYTE WRITE

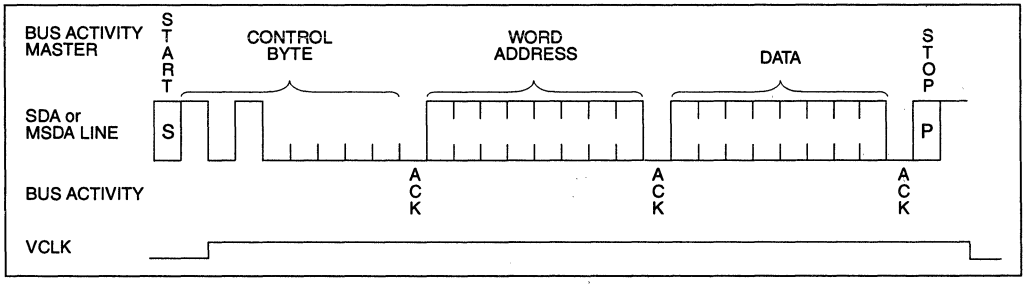
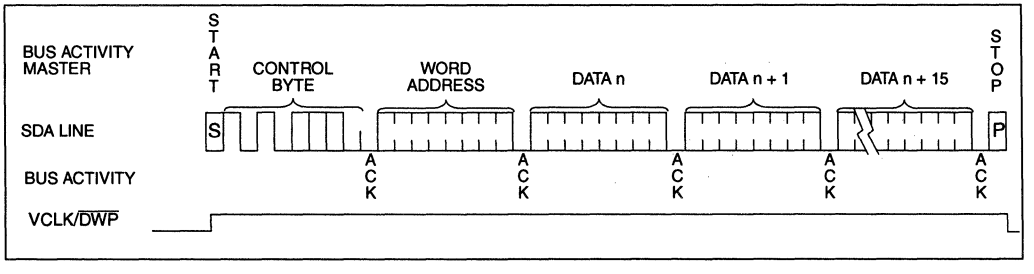


FIGURE 4-2: PAGE WRITE

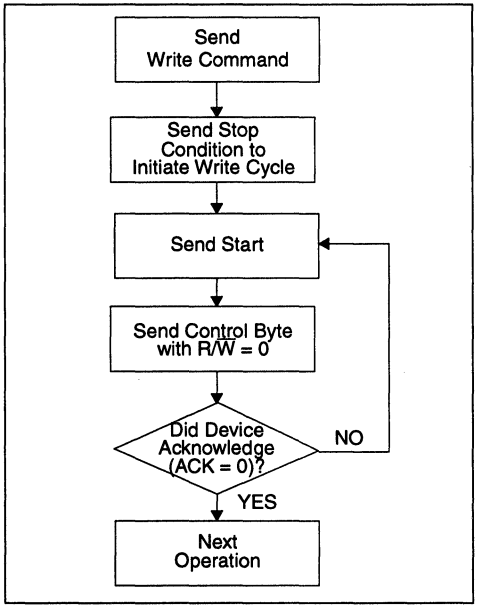


5.0 ACKNOWLEDGE POLLING

Acknowledge polling can be done for both the DDC Monitor Port (when in bi-directional Mode) and the Microcontroller Access Port.

Since the port will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize but throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This invoives the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$=0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

6.1 DDC Monitor Port

When using the DDC Monitor Port in the bi-directional Mode, the VCLK/$\overline{DWP}$ pin operates as the write protect control pin. Setting VCLK/$\overline{DWP}$ high allows normal write operations, while setting VCLK/$\overline{DWP}$ low prevents writing to any location in the array. Connecting the VCLK/$\overline{DWP}$ pin to Vss would allow the DDC Monitor Port to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

6.2 Microcontroller Access Port

The Microcontroller Access Port can be used as a serial ROM when the MWP pin is connected to Vcc. Programming will be inhibited and the entire memory associated with the Microcontroller Access Port will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read. These operations are identical for both the DDC Monitor Port (in bi-directional Mode) and the Microcontroller Access Port and are completely independent of one another.

7.1 Current Address Read

The port contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the port issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the port as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The port then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the port transmits the first data byte, and the master issues an acknowledge as opposed to a stop condition in a random read. This directs the port to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads, the port contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

Both the DDC Monitor Port and Microcontroller Access Port employ a Vcc threshold detector circuit which disables the internal erase/write logic, if the Vcc is below 1.5 volts at nominal conditions.

The DSCL, MSCL, DSDA, and MSDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

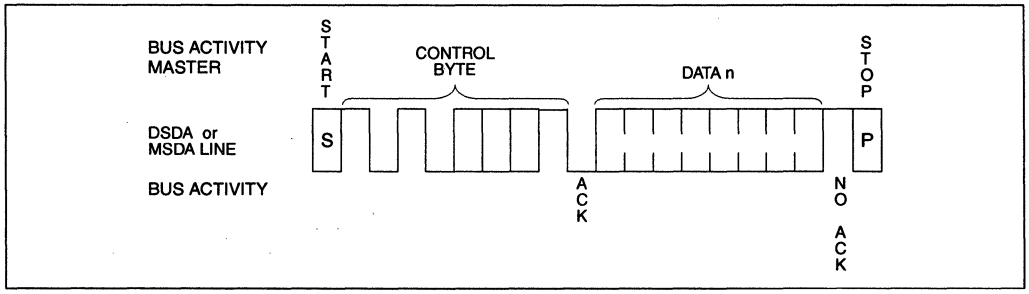


FIGURE 7-2: RANDOM READ

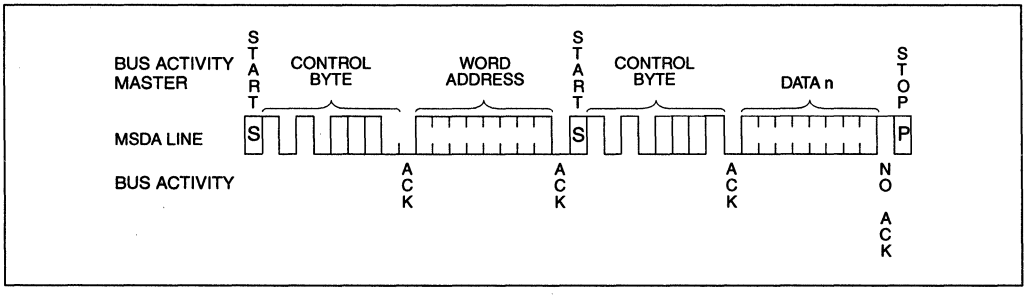
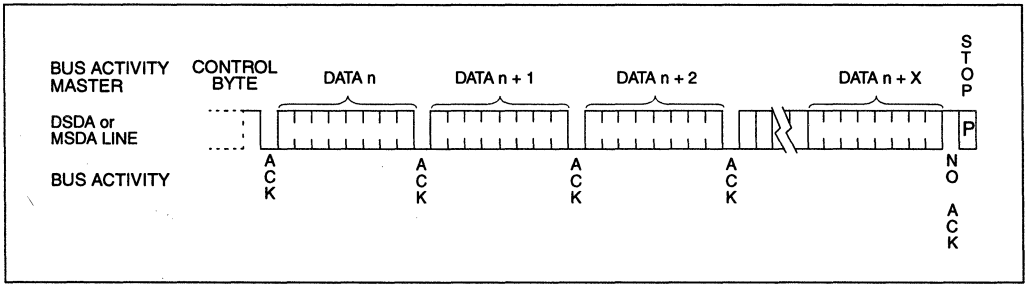


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 DSDA

This pin is used to transfer addresses and data into and out of the DDC Monitor Port, when the device is in the bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the DSDA pin. This pin is an open drain terminal, therefore the DSDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer in the bi-directional Mode, DSDA is allowed to change only during DSCL or MSDA low. Changes during DSCL high are reserved for indicating the START and STOP conditions.

8.2 DSCL

This pin is the clock input for the DDC Monitor Port while in the bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

8.3 VCLK/$\overline{\text{DWP}}$

This pin is the clock input for the DDC Monitor Port while in the Transmit-Only Mode. In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the bi-directional Mode, a high logic level is required on this pin to enable write capability.

8.4 MSCL

This pin is the clock input for the Microcontroller Access Port, and is used to synchronize data transfer to and from the device.

8.5 MSDA

This pin is used to transfer addresses and data into and out of the Microcontroller Access Port. This pin is an open drain terminal, therefore the MSDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2KΩ for 400 kHz).

MSDA is allowed to change only during MSCL low. Changes during MSCL high are reserved for indicating the START and STOP conditions.

8.6 MWP

This pin is used to write protect the 4K memory array for the Microcontroller Access Port.

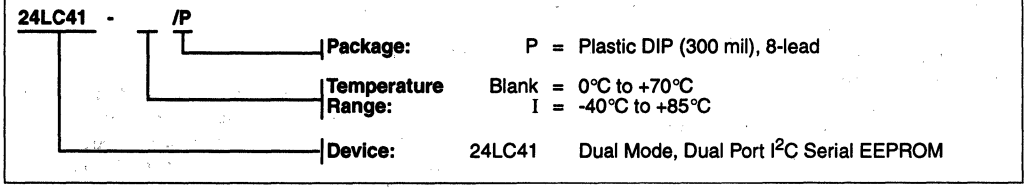
This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

24LC41 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LC41A

1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification, including recovery to DDC1
- Improved noise immunity
- Separate high speed 2-wire bus for microcontroller access to 4K-bit Serial EEPROM
- Low power CMOS technology
- 2 mA active current typical
- 20 µA standby current typical at 5.5V
- Dual 2-wire serial interface bus, I²C™ compatible
- Hardware write-protect for Microcontroller Access Port
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes (DDC port) or 16 bytes (4K Port)
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- 1,000,000 erase/write cycles guaranteed
- Data retention > 40 years
- 8-pin PDIP package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

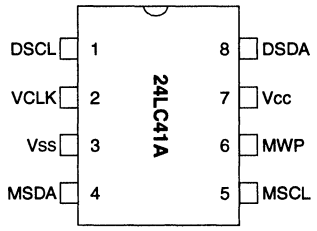
The Microchip Technology Inc. 24LC41A is a dual-port 128 x 8 and 512 x 8-bit Electrically Erasable PROM (EEPROM). This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Three modes of operation have been implemented:

- Transmit-Only Mode for the DDC Monitor Port
- Bi-directional Mode for the DDC Monitor Port
- Bi-directional, industry-standard 2-wire bus for the 4K Microcontroller Access Port

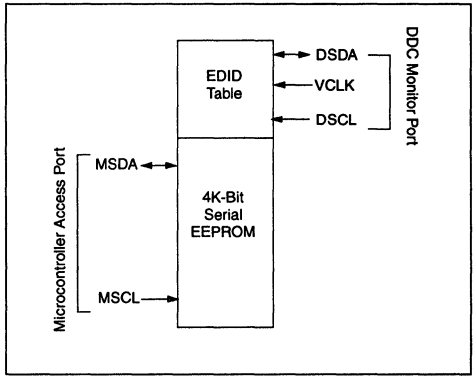
Upon power-up, the DDC Monitor Port will be in the Transmit-Only Mode, repeatedly sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the DSCL pin will cause the device to enter the transition mode, an look for a valid control byte on the I²C bus. If it detects a valid control byte from the master, it will switch to Bi-directional Mode, with byte selectable read/write capability of the memory array using DSCL. If no control byte is received, the device will revert to the Transmit-Only Mode after it received 128 consecutive VCLK pulses while the DSCL pin is idle. The 4K-bit microcontroller port is completely independent of the DDC port, therefore, it can be accessed continuously by a microcontroller without interrupting DDC transmission activity. The 24LC41A is available in a standard 8-pin PDIP package in both commercial and industrial temperature ranges.

PACKAGE TYPE

PDIP



BLOCK DIAGRAM



DDC is a trademark of Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
DSCL	Serial Clock for DDC Bi-directional Mode (DDC2)
DSDA	Serial Address and Data I/O (DDC Bus)
VCLK	Serial Clock for DDC transmit-only mode (DDC1)
MSCL	Serial clock for 4K-bit MCU port
MSDA	Serial Address and Data I/O for 4K-bit MCU port
MWP	Hardware write-protect for Microcontroller Access Port
VSS	Ground
VCC	+2.5V to +5.5V power supply

TABLE 1-2: DC CHARACTERISTICS

	VCC = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
DSCL, DSDA, MSCL & MSDA pins: High level input voltage Low level input voltage	 VIH VIL	 .7 VCC —	 — .3 VCC	 V V	
Input levels on VCLK pin: High level input voltage Low level input voltage	 VIH VIL	 2.0 —	 .8 .2 VCC	 V V	 VCC ≥ 2.7V (Note) VCC < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL1	—	.4	V	IOL = 3 mA, VCC = 2.5V (Note)
Low level output voltage	VOL2	—	.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN =.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT =.1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note), Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, DSCL or MSCL = 400 kHz
Standby current	ICCS	— —	60 200	µA µA	VCC = 3.0V, DSDA or MSDA = DSCL or MSCL = VCC VCC = 5.5V, DSDA or MSDA = DSCL or MSCL = VCC VCLK = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS (DDC MONITOR AND MICROCONTROLLER ACCESS PORTS)

DDC Monitor Port (Bi-directional Mode) and Microcontroller Access Port							
Parameter	**Symbol**	**Standard Mode**		**Vcc = 4.5 - 5.5V Fast Mode**		**Units**	**Remarks**
		Min	**Max**	**Min**	**Max**		
Clock frequency (DSCL and MSCL)	FCLK	—	100	—	400	kHz	
Clock high time (DSCL and MSCL)	THIGH	4000	—	600	—	ns	
Clock low time (DSCL and MSCL)	TLOW	4700	—	1300	—	ns	
DSCL, DSDA, MSCL & MSDA rise time	TR	—	1000	—	300	ns	(Note 1)
DSCL, DSDA, MSCL & MSDA fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + .1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (DSCL, DSDA, MSCL & MSDA pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)
DDC Monitor Port Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of DSCL or MSCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

2.1 DDC Monitor Port

The DDC Monitor Port operates in two modes, the Transmit-Only Mode and the Bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input and sharing a common data line (DSDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the DSDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the DSCL input. When a valid transition on DSCL is recognized, the device will switch into the Bi-directional Mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bi-directional Mode. Otherwise, it will revert to the Transmit-Only Mode after it sees 128 VCLK pulses.

2.1.1 TRANSMIT-ONLY MODE

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional 2-wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (see Section 2.1.2). In this mode, data is transmitted on the DSDA pin in 8-bit bytes, each followed by a ninth, null bit (see Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted by most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The Bi-directional Mode Clock (DSCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.1.2 INITIALIZATION PROCEDURE

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the DSDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

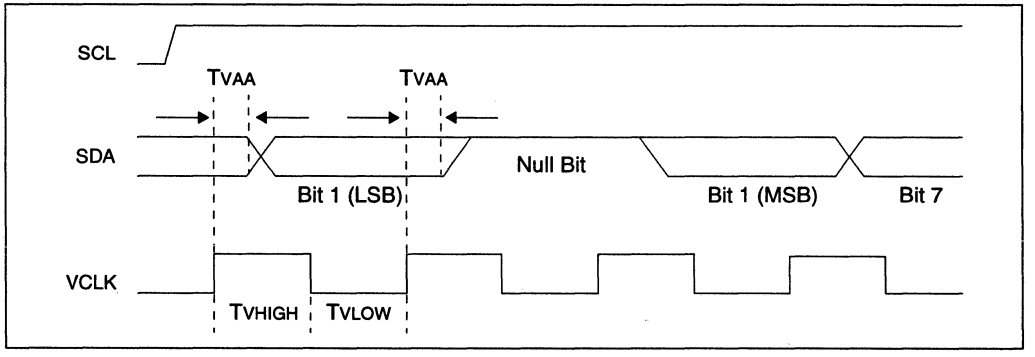
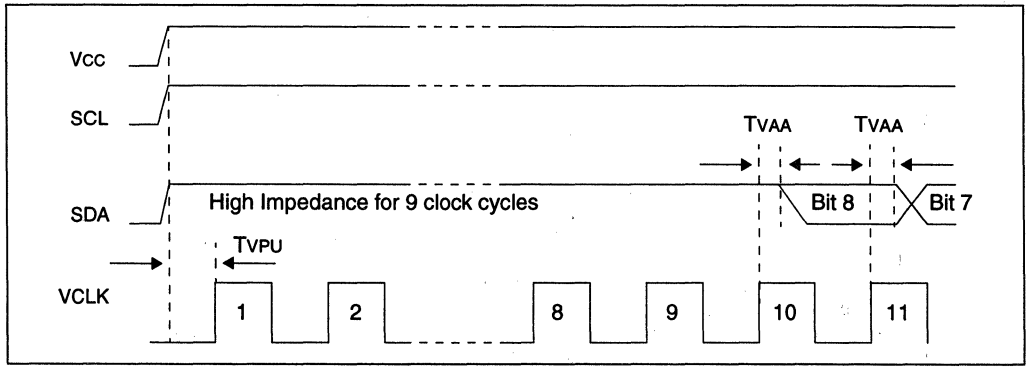


FIGURE 2-2: DEVICE INITIALIZATION



2.1.3 BI-DIRECTIONAL MODE

Before the 24LC41A can be switched into the Bi-directional Mode (Figure 2-4), it must enter the transition mode, which is done by applying a valid high to low transition on the Bi-directional Mode Clock (DSCL). As soon it enters the transition mode, it looks for a control byte 1010 000X on the I^2C™ bus, and starts to count pulses on VCLK. Any high to low transition on the DSCL line will reset the count. If it sees a pulse count of 128 on VCLK while the DSCL line is idle, it will revert back to the Transmit-Only Mode, and transmit its contents starting with the most significant bit in address 00h. However, if it detects the control byte on the I^2C bus, (Figure 2-3) it will switch to the in the Bi-directional Mode. Once the device has made the transition to the Bi-directional mode, the only way to switch the device back to the Transmit-Only Mode is to remove power from the device. The mode transition process is shown in detail in Figure 2-4.

Once the device has switched into the Bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire Bi-directional data transmission protocol (I^2C). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-directional Mode Clock (DSCL), controls access to the bus and generates the START and STOP conditions, while the monitor port acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bi-directional mode, the monitor port only responds to commands for device 1010 000X.

2.2 Microcontroller Access Port

The Microcontroller Access Port supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (MSCL), controls the bus access, and generates the START and STOP conditions, while the Microcontroller Access Port works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

FIGURE 2-3: SUCCESSFUL MODE TRANSITION TO BI-DIRECTIONAL MODE

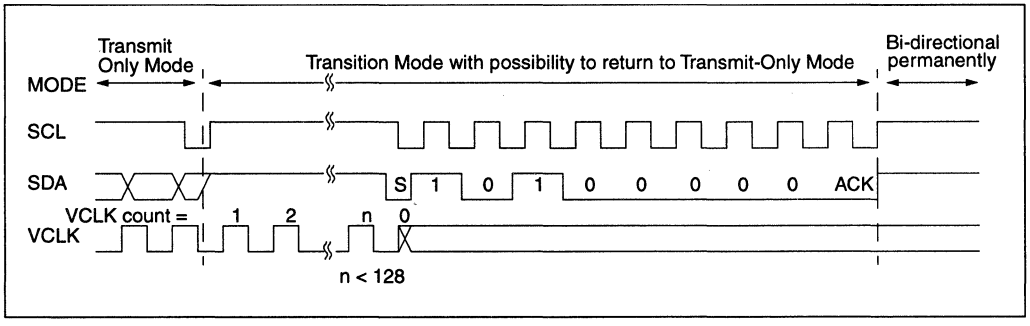


FIGURE 2-4: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE

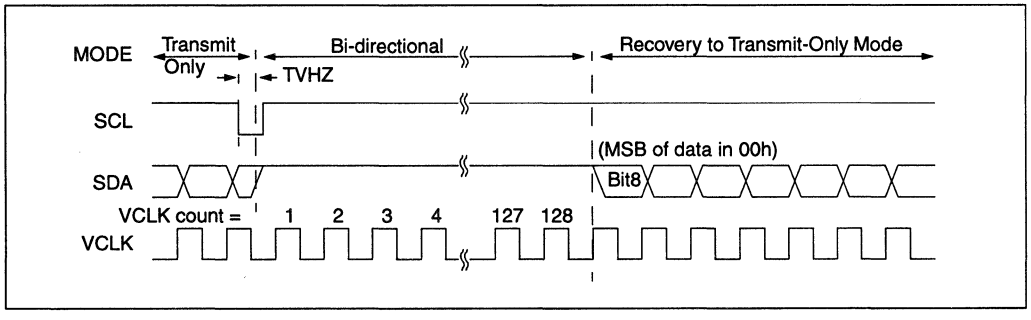
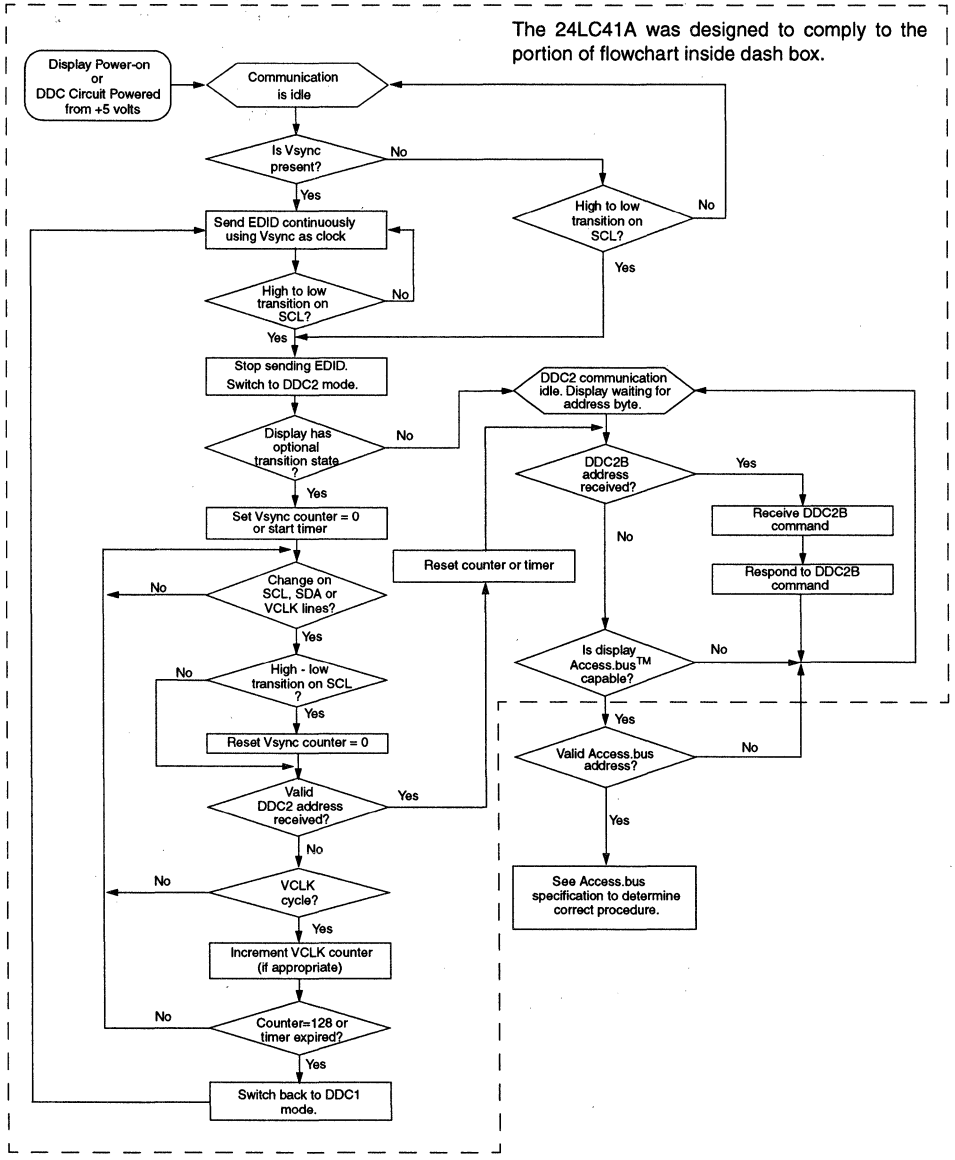


FIGURE 2-5: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA



Note 1: The base flowchart is copyright © 1993, 1994, 1995 Video Electronic Standard Association (VESA) from VESA's Display Data Channel (DDC) Standard Proposal ver. 2p rev. 0, used by permission of VESA.

2: The dash box and text "The 24LC41A and ... inside dash box." are added by Microchip Technology, Inc.

3: Vsync signal is normally used to derive a signal for VCLK pin on the 24LC41A.

3.0 BI-DIRECTIONAL BUS CHARACTERISTICS

Characteristics for the Bi-directional bus are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The microcontroller access port and the DDC Monitor Port (in Bi-directional Mode) will not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the DSDA or MSDA line during the acknowledge clock pulse in such a way that the DSDA or MSDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The first part of the control byte consists of a 4-bit control code. This control code is set as 1010 for both read and write operations and is the same for both the DDC Monitor Port and Microcontroller Access Port. The next three bits of the control byte are block select bits (B1, B2, and B0). All three of these bits are zero for the DDC Monitor Port. The B2 and B1 bits are don't care bits for the Microcontroller Access Port, and the B0 bit is used by the Microcontroller Access Port to select which of the two 256 word blocks of memory are to be accessed (see Figure 3-4). The B0 bit is effectively the most significant bit of the word address. The last bit of the control byte defines the operation to be performed. When set to one, a read operation is selected; when set to zero, a write operation is selected. Following the start condition, the device monitors the DSDA or MSDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the device will select a read or a write operation. The DDC Monitor Port and Microcontroller Access Port can be accessed simultaneously because they are completely independent of one another.

Operation	Control Code	Chip Select	R/W
Read	1010	B1B2B0	1
Write	1010	B1B2B0	0

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

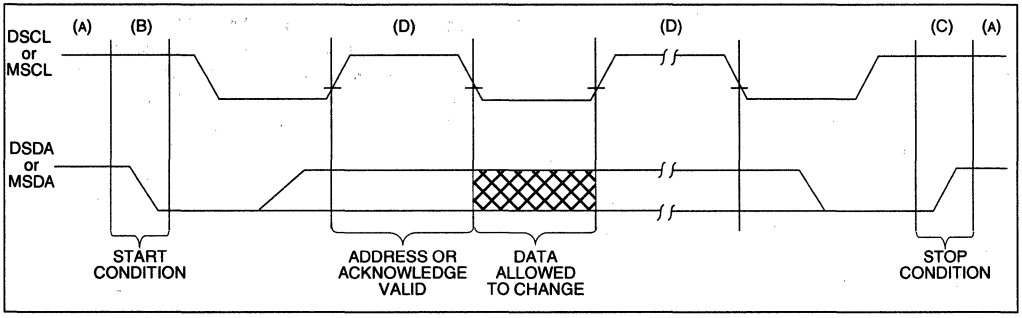


FIGURE 3-2: BUS TIMING START/STOP

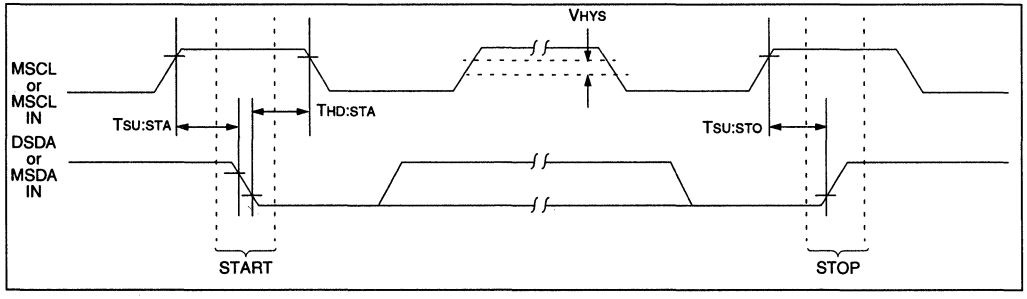


FIGURE 3-3: BUS TIMING DATA

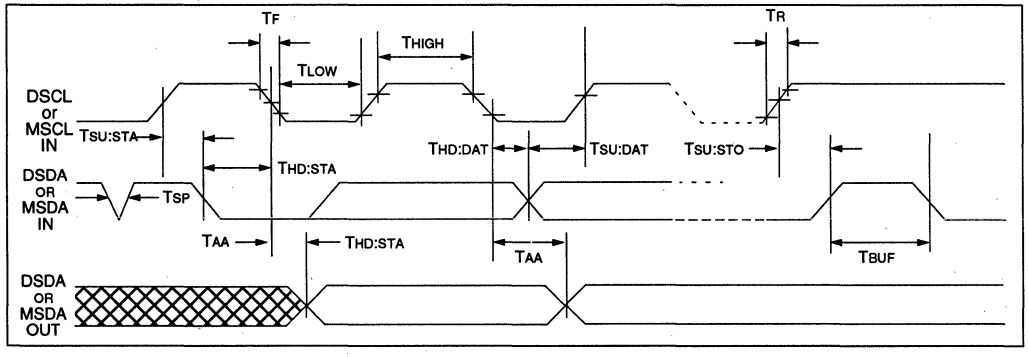
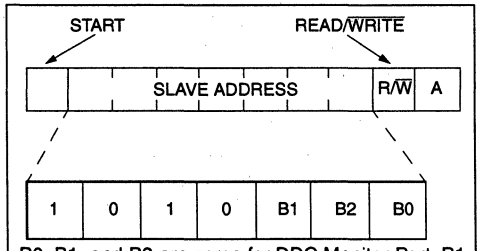


FIGURE 3-4: CONTROL BYTE ALLOCATION



B0, B1, and B2 are zeros for DDC Monitor Port. B1 and B2 are don't care bits for the Microcontroller Access Port, and B0 is used to select which of the two 256 word blocks of memory are to be accessed.

4.0 WRITE OPERATION

Write operations are identical for the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port, with the exception of the VCLK and MWP pins noted in the next sections. Data can be written using either a byte write or page write command. Write commands for the DDC Monitor Port and the Microcontroller Access Port are completely independent of one another.

4.1 Byte Write

Following the start signal from the master, the slave address (4-bits), the chip select bits (3-bits) and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the port. After receiving another acknowledge signal from the port, the master device will transmit the data word to be written into the addressed memory location. The port acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time, the port will not generate acknowledge signals (see Figure 4-1).

For the DDC Monitor Port it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming. The MWP pin must be held high for the duration of the write protection.

4.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the port in the same way as in a byte write. But, instead of generating a stop condition, the master transmits up to eight data bytes to the DDC Monitor Port or 16 bytes to the Microcontroller Access Port, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order 5-bits of the word address remains constant. If the master should transmit more than eight words to the DDC Monitor Port or 16 words to the Microcontroller Access Port prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 4-2).

For the DDC Monitor Port, it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming. For the DDC Monitor Port, the MWP pin must be held high for the duration of the write cycle.

FIGURE 4-1: BYTE WRITE

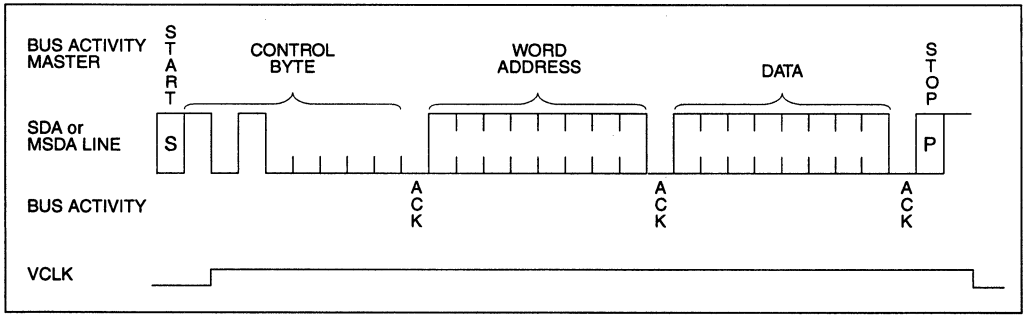


FIGURE 4-2: PAGE WRITE

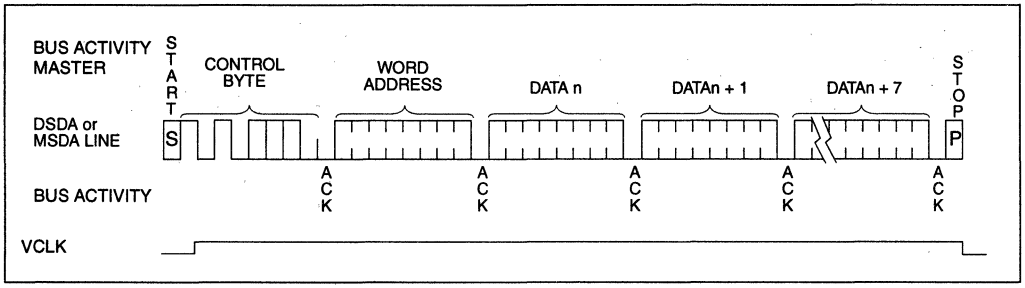
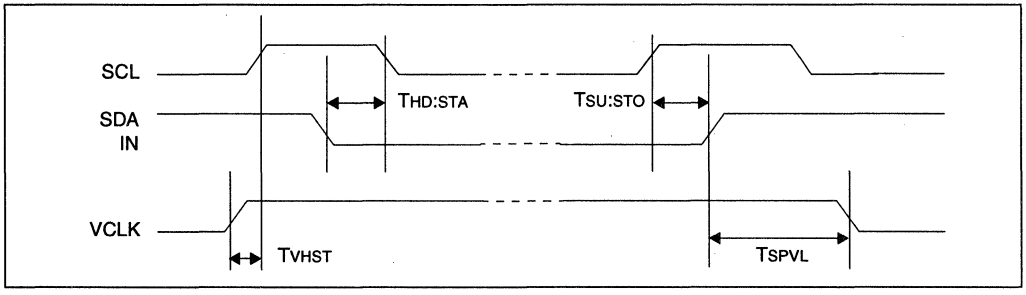


FIGURE 4-3: VCLK WRITE ENABLE TIMING

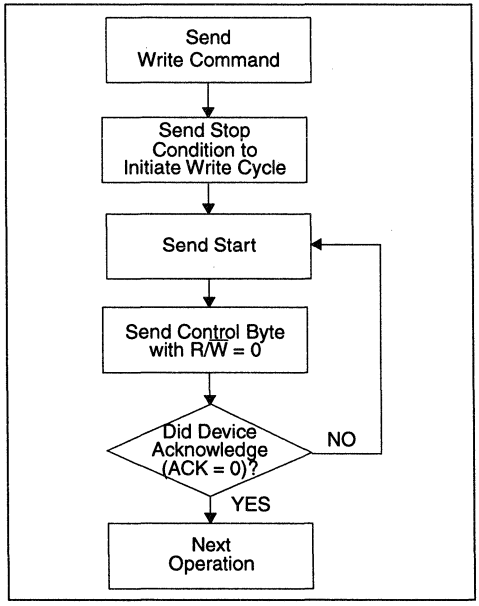


5.0 ACKNOWLEDGE POLLING

Acknowledge polling can be done for both the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port.

Since the port will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize but throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$=0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

6.1 DDC Monitor Port

When using the DDC Monitor Port in the Bi-directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the monitor port to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read. These operations are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port and are completely independent of one another.

7.1 Current Address Read

The port contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the port issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the port as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The port then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (see Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the port transmits the first data byte, and the master issues an acknowledge as opposed to a stop condition in a random read. This directs the port to transmit the next sequentially addressed 8-bit word (see Figure 7-3).

To provide sequential reads, the port contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

Both the DDC Monitor Port and Microcontroller Access Port employ a Vcc threshold detector circuit which disables the internal erase/write logic, if the Vcc is below 1.5 volts at nominal conditions.

The VCLK, DSCL, MSCL, DSDA, and MSDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

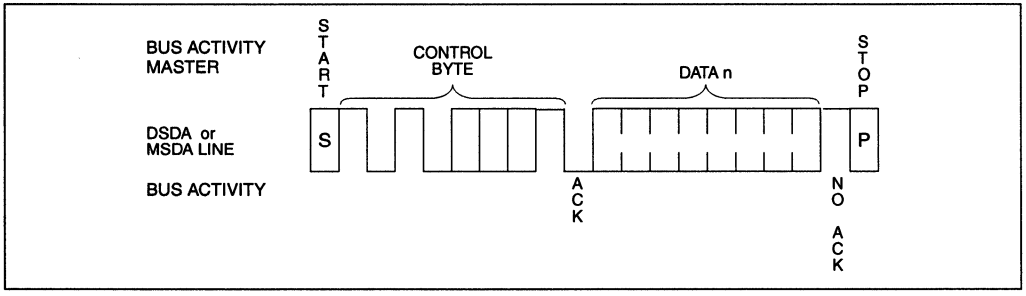


FIGURE 7-2: RANDOM READ

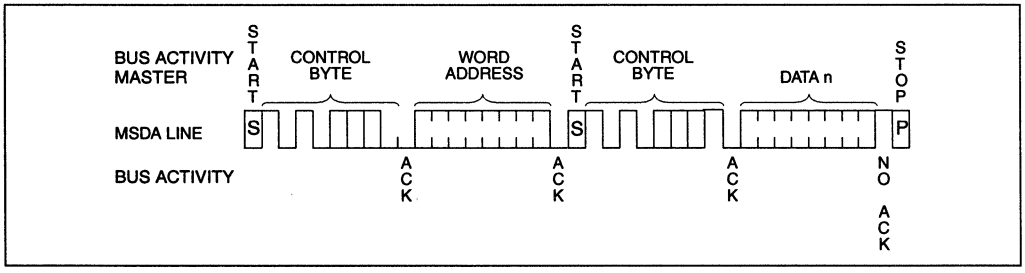
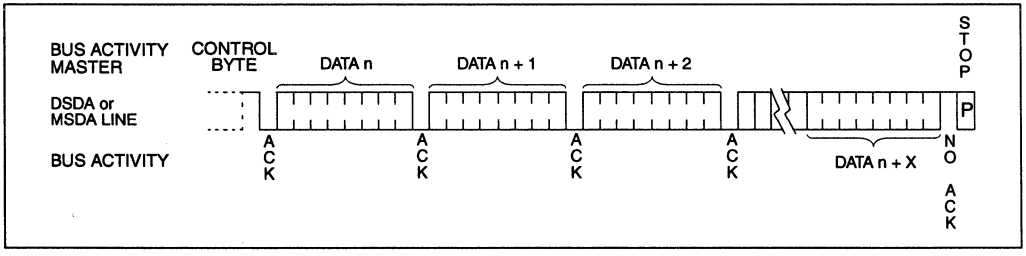


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 DSDA

This pin is used to transfer addresses and data into and out of the DDC Monitor Port, when the device is in the Bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the DSDA pin. This pin is an open drain terminal, therefore the DSDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2KΩ for 400 kHz).

For normal data transfer in the Bi-directional Mode, DSDA is allowed to change only during DSCL or MSDA low. Changes during DSCL high are reserved for indicating the START and STOP conditions.

8.2 DSCL

This pin is the clock input for the DDC Monitor Port while in the Bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the Bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

8.3 VCLK

This pin is the clock input for the DDC Monitor Port while in the Transmit-Only Mode. In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-directional Mode, a high logic level is required on this pin to enable write capability.

8.4 MWP

This pin is used to write protect the 4K memory array for the Microcontroller Access Port.

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

8.5 MSCL

This pin is the clock input for the Microcontroller Access Port, and is used to synchronize data transfer to and from the device.

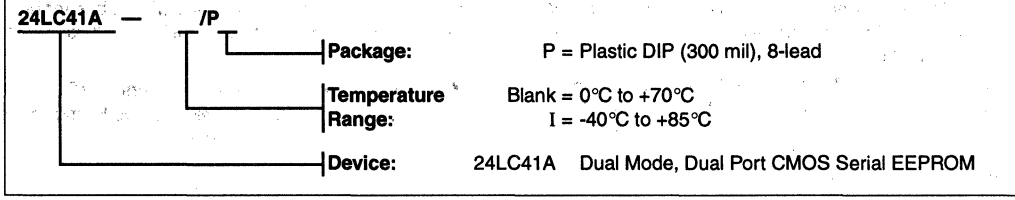
8.6 MSDA

This pin is used to transfer addresses and data into and out of the Microcontroller Access Port. This pin is an open drain terminal, therefore the MSDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2KΩ for 400 kHz).

MSDA is allowed to change only during MSCL low. Changes during MSCL high are reserved for indicating the START and STOP conditions.

24LC41A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

24LCS41

1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification
- Improved noise immunity
- Separate high speed 2-wire bus for microcontroller access to 4K-bit Serial EEPROM
- Low power CMOS technology
- 2 mA active current typical
- 20 µA standby current typical at 5.5V
- Dual 2-wire serial interface bus
- Hardware write-protect for DDS monitor ports
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes (DDC port) or 16 bytes (4K Port)
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- 1,000,000 erase/write cycles guaranteed
- Data retention > 40 years
- 8-pin PDIP package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

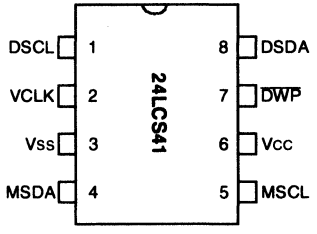
The Microchip Technology Inc. 24LCS41 is a dual-port 128 x 8 and 512 x 8-bit Electrically Erasable PROM (EEPROM). This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Three modes of operation have been implemented:

- Transmit-Only Mode for the DDC Monitor Port
- Bi-directional Mode for the DDC Monitor Port
- Bi-directional, industry-standard 2-wire bus for the 4K Microcontroller Access Port

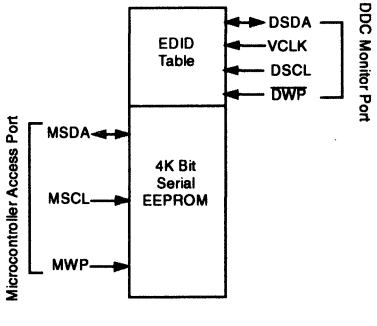
Upon power-up, the DDC Monitor Port will be in the Transmit-Only Mode, repeatedly sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the DSCL pin will cause the device to enter the bi-directional Mode, with byte-selectable read/write capability of the memory array. The 4K-bit microcontroller port is completely independent of the DDC port, therefore, it can be accessed continuously by a microcontroller without interrupting DDC transmission activity. The

PACKAGE TYPE

PDIP



BLOCK DIAGRAM



24LCS41 is available in a standard 8-pin PDIP package in both commercial and industrial temperature ranges.

DDC is a trademark of Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
DSCL	Serial Clock for DDC bi-directional Mode (DDC2)
DSDA	Serial Address and Data I/O (DDC Bus)
VCLK	Serial Clock for DDC transmit-only mode (DDC1)
MSCL	Serial clock for 4K-bit MCU port
MSDA	Serial Address and Data I/O for 4K-bit MCU port
$\overline{DWP}$	Hardware write-protect for 4K-bit DDC monitor port
Vss	Ground
Vcc	+2.5V to +5.5V power supply

TABLE 1-2: DC CHARACTERISTICS

	Vcc = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
DSCL, DSDA, MSCL & MSDA pins: High level input voltage Low level input voltage	 VIH VIL	 .7 Vcc —	 — .3 Vcc	 V V	
Input levels on VCLK pin: High level input voltage Low level input voltage	 VIH VIL	 2.0 —	 .8 .2 Vcc	 V V	 Vcc ≥ 2.7V (Note) Vcc < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL1	—	.4	V	IOL = 3 mA, Vcc = 2.5V (Note)
Low level output voltage	VOL2	—	.6	V	IOL = 6 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN =.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT =.1V to Vcc
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	Vcc = 5.0V (Note), Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write Icc Read	— —	3 1	mA mA	Vcc = 5.5V, DSCL or MSCL = 400 kHz
Standby current	ICCS	— —	60 200	µA µA	Vcc = 3.0V, DSDA or MSDA = DSCL or MSCL = Vcc Vcc = 5.5V, DSDA or MSDA = DSCL or MSCL = Vcc VCLK = Vss

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS (DDC MONITOR AND MICROCONTROLLER ACCESS PORTS)

DDC Monitor Port (Bi-directional Mode) and Microcontroller Access Port							
Parameter	**Symbol**	**Standard Mode**		**Vcc = 4.5 - 5.5V Fast Mode**		**Units**	**Remarks**
		Min	**Max**	**Min**	**Max**		
Clock frequency (DSCL and MSCL)	FCLK	—	100	—	400	kHz	
Clock high time (DSCL and MSCL)	THIGH	4000	—	600	—	ns	
Clock low time (DSCL and MSCL)	TLOW	4700	—	1300	—	ns	
DSCL, DSDA, MSCL & MSDA rise time	TR	—	1000	—	300	ns	(Note 1)
DSCL, DSDA, MSCL & MSDA fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + .1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (DSCL, DSDA, MSCL & MSDA pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)
DDC Monitor Port Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	0	—	0	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of DSCL or MSCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

2.1 DDC Monitor Port

The DDC Monitor Port operates in two modes, the Transmit-Only Mode and the bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input and sharing a common data line (DSDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the DSDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the DSCL input. When a valid transition on DSCL is recognized, the device will switch into the bi-directional Mode. The only way to switch the device back to the Transmit-Only Mode is to remove power from the device.

2.1.1 TRANSMIT-ONLY MODE

The device will power up in the Transmit-Only Mode. This mode supports a unidirectional 2-wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (Section 2.1.2).

In this mode, data is transmitted on the DSDA pin in 8-bit bytes, each followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted by most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The bi-directional Mode Clock (DSCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.1.2 INITIALIZATION PROCEDURE

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the DSDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

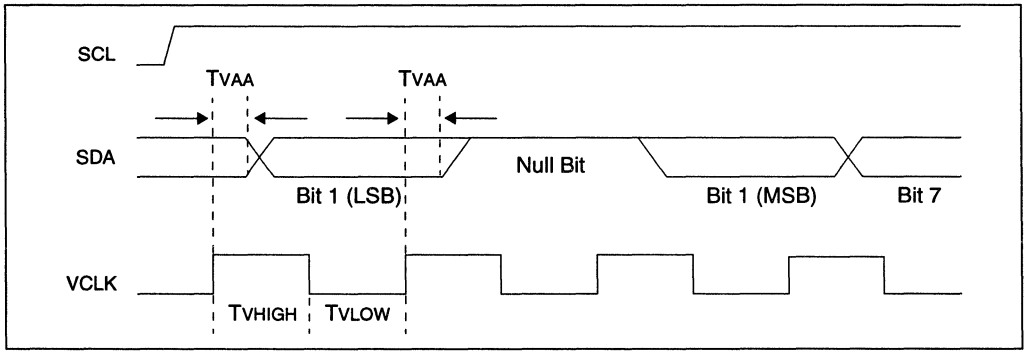
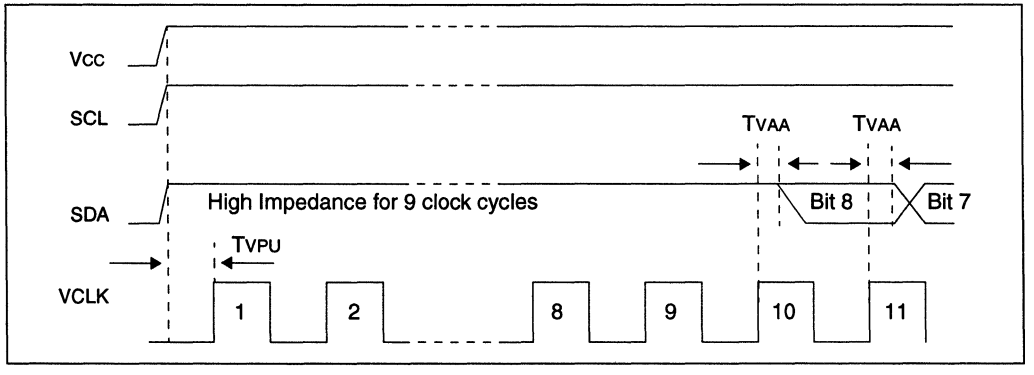


FIGURE 2-2: DEVICE INITIALIZATION



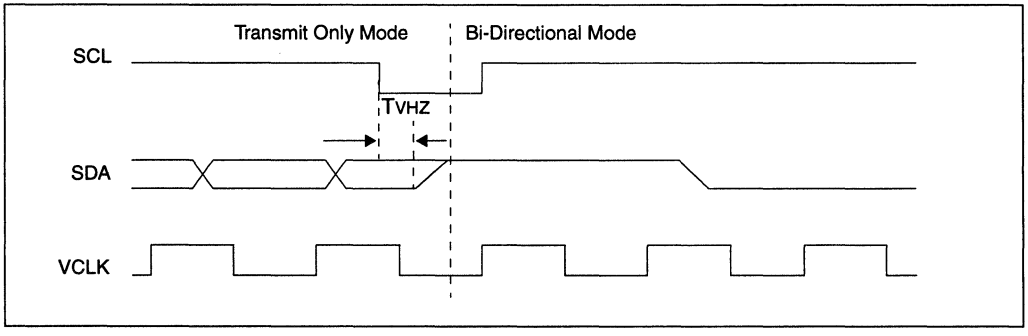
2.1.3 BI-DIRECTIONAL MODE

The DDC Monitor Port can be switched into the bi-directional Mode (Figure 2-3) by applying a valid high to low transition on the Bi-directional Mode Clock (DSCL). When the device has been switched into the Bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a 2-wire bi-directional data transmission protocol. In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-directional Mode Clock (DSCL), controls access to the bus and generates the START and STOP conditions, while the DDC Monitor Port acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

2.2 Microcontroller Access Port

The Microcontroller Access Port supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (MSCL), controls the bus access, and generates the START and STOP conditions, while the Microcontroller Access Port works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

FIGURE 2-3: MODE TRANSITION



3.0 BI-DIRECTIONAL BUS CHARACTERISTICS

Characteristics for the bi-directional bus are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The microcontroller access port and the DDC Monitor Port (in Bi-directional Mode) will not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the DSDA or MSDA line during the acknowledge clock pulse in such a way that the DSDA or MSDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The first part of the control byte consists of a 4-bit control code. This control code is set as 1010 for both read and write operations and is the same for both the DDC Monitor Port and Microcontroller Access Port. The next three bits of the control byte are block select bits (B1, B2, and B0). All three of these bits are don't care bits for the DDC Monitor Port. The B2 and B1 bits are don't care bits for the Microcontroller Access Port, and the B0 bit is used by the Microcontroller Access Port to select which of the two 256 word blocks of memory are to be accessed (Figure 3-4). The B0 bit is effectively the most significant bit of the word address. The last bit of the control byte defines the operation to be performed. When set to one, a read operation is selected; when set to zero, a write operation is selected. Following the start condition, the device monitors the DSDA or MSDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the device will select a read or a write operation. The DDC Monitor Port and Microcontroller Access Port can be accessed simultaneously because they are completely independent of one another.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXB0	1
Write	1010	XXB0	0

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

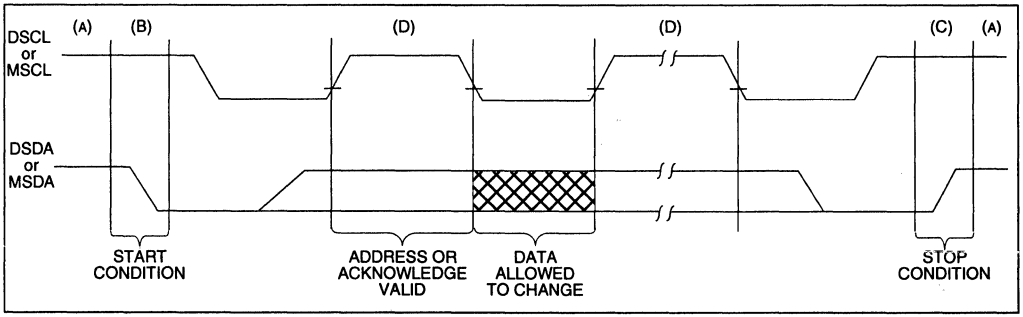


FIGURE 3-2: BUS TIMING START/STOP

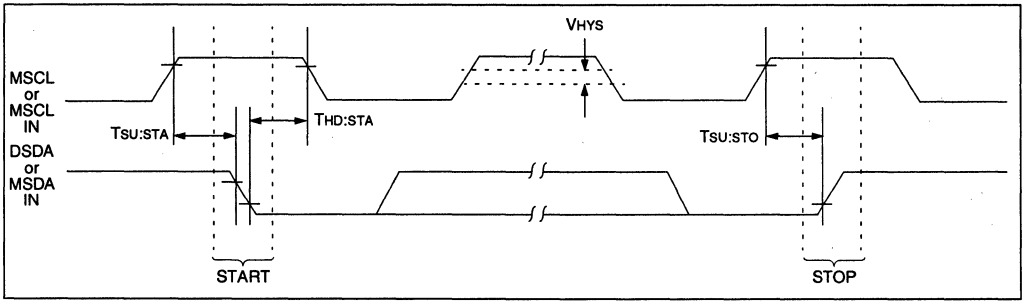


FIGURE 3-3: BUS TIMING DATA

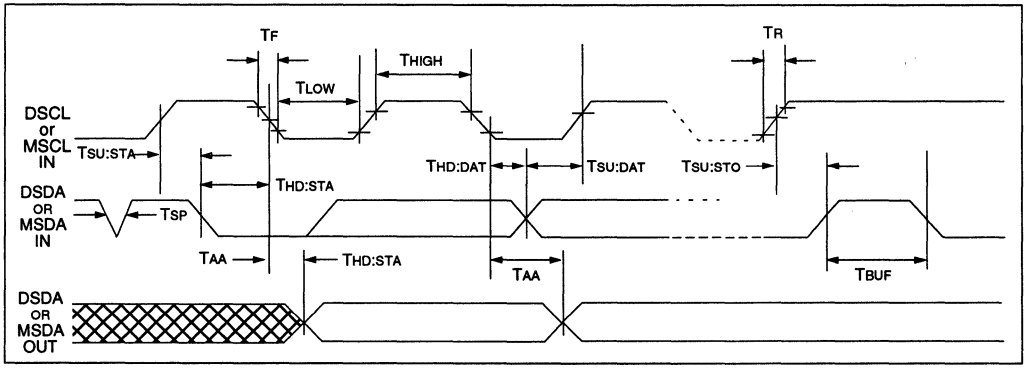
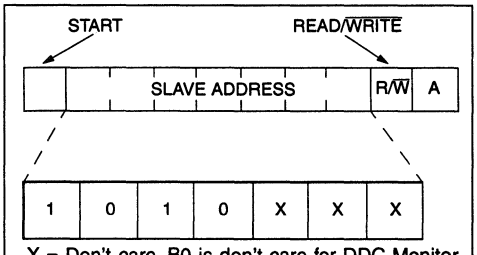


FIGURE 3-4: CONTROL BYTE ALLOCATION



X = Don't care. B0 is don't care for DDC Monitor Port, but is used by the Microcontroller Access Port to select which of the two 256 word blocks of memory are to be accessed.

4.0 WRITE OPERATION

Write operations are identical for the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port, with the exception of the VCLK and MWP pins noted in the next sections. Data can be written using either a byte write or page write command. Write commands for the DDC Monitor Port and the Microcontroller Access Port are completely independent of one another.

4.1 Byte Write

Following the start signal from the master, the slave address (4-bits), the chip select bits (3-bits) and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the port. After receiving another acknowledge signal from the port, the master device will transmit the data word to be written into the addressed memory location. The port acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time, the port will not generate acknowledge signals (Figure 4-1).

For the DDC Monitor Port it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming. The $\overline{DWP}$ pin must be held high for the duration of the write protection.

4.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the port in the same way as in a byte write. But, instead of generating a stop condition, the master transmits up to eight data bytes to the DDC Monitor Port or 16 bytes to the Microcontroller Access Port, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order 5-bits of the word address remains constant. If the master should transmit more than eight words to the DDC Monitor Port or 16 words to the Microcontroller Access Port prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

For the DDC Monitor Port, it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

For the Microcontroller Access Port, the MWP pin must be held to Vss during the entire write operation.

FIGURE 4-1: BYTE WRITE

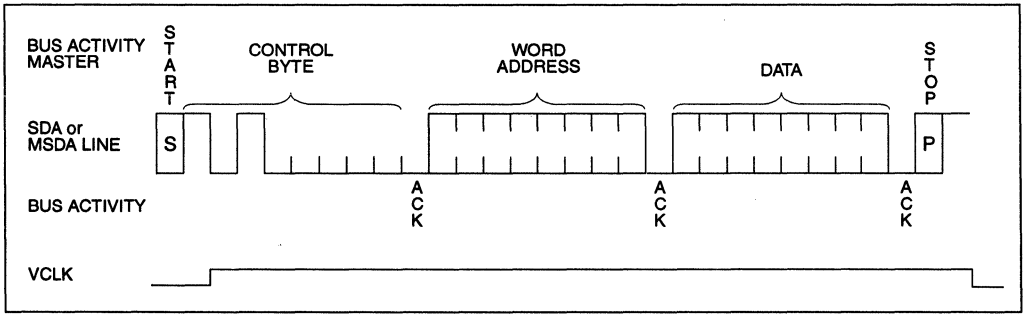


FIGURE 4-2: PAGE WRITE

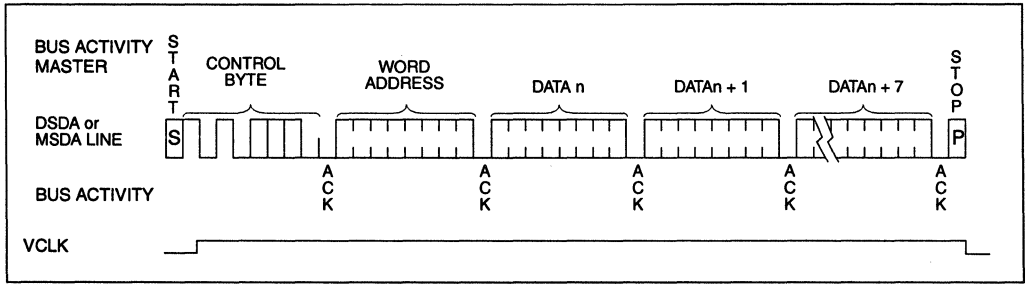
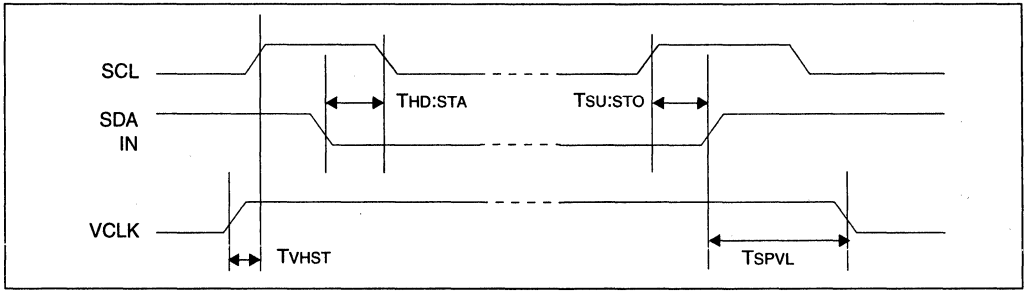


FIGURE 4-3: VCLK WRITE ENABLE TIMING

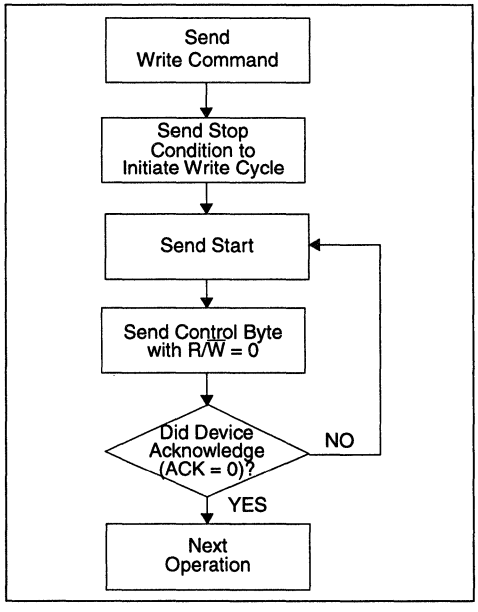


5.0 ACKNOWLEDGE POLLING

Acknowledge polling can be done for both the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port.

Since the port will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize but throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$=0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

6.1 DDC Monitor Port

When using the DDC Monitor Port in the Bi-Directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the port to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

Additionally, Pin 3 performs a flexible write protect function. The monitor port contains a write-protection control fuse whose factory default state is cleared. Writing any data to address 7Fh (normally the checksum in DDC applications) sets the fuse which enables the $\overline{WP}$ pin. Until this fuse is set, the monitor port is always write enabled (if VCLK = 1). After the fuse is set, the write capability of the 24LCS41 is determined by $\overline{WP}$ (Figure 6-1).

FIGURE 6-1: WRITE PROTECT TRUTH TABLE

VCLK	$\overline{WP}$	Add. 7Fh Written	Mode
0	X	X	Read Only
1	X	No	R/$\overline{W}$
1	1/open	Yes	R/$\overline{W}$
1	0	Yes	Read Only

6.2 Microcontroller Access Port

The Microcontroller Access Port can be used as a serial ROM when the MWP pin is connected to Vcc. Programming will be inhibited and the entire memory associated with the Microcontroller Access Port will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read. These operations are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port and are completely independent of one another.

7.1 Current Address Read

The port contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the port issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the port as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The port then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the port transmits the first data byte, and the master issues an acknowledge as opposed to a stop condition in a random read. This directs the port to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads, the port contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

Both the DDC Monitor Port and Microcontroller Access Port employ a Vcc threshold detector circuit which disables the internal erase/write logic, if the Vcc is below 1.5 volts at nominal conditions.

The DSCL, MSCL, DSDA, and MSDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

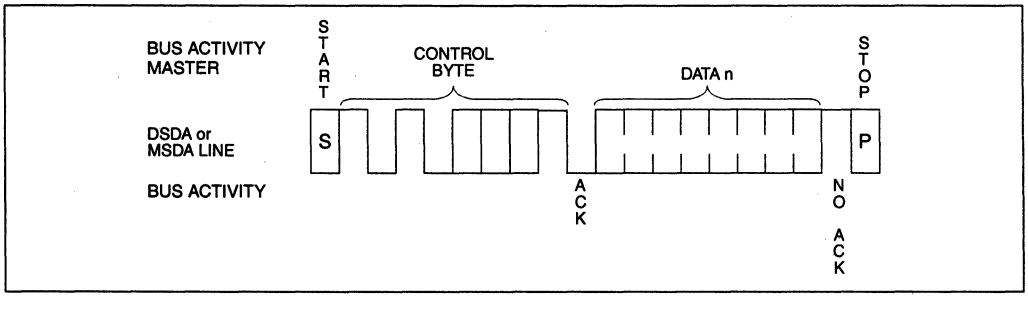


FIGURE 7-2: RANDOM READ

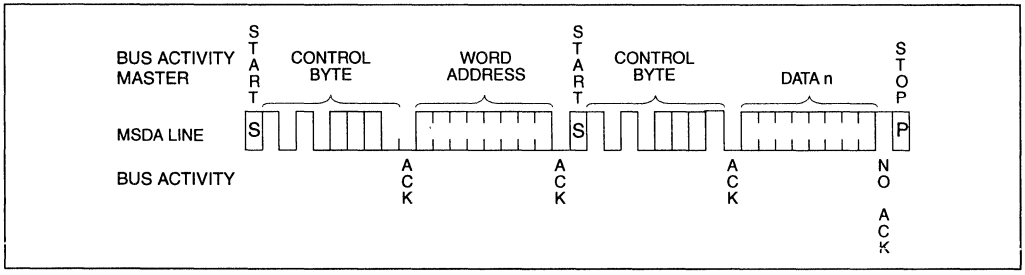
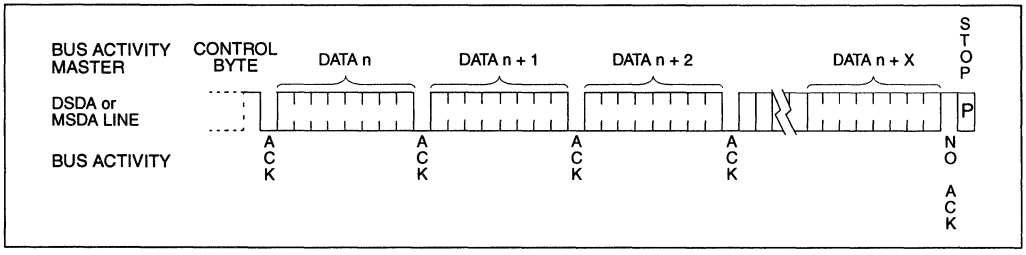


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 DSDA

This pin is used to transfer addresses and data into and out of the DDC Monitor Port, when the device is in the bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the DSDA pin. This pin is an open drain terminal, therefore the DSDA bus requires a pullup resistor to Vcc (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer in the Bi-directional Mode, DSDA is allowed to change only during DSCL or MSDA low. Changes during DSCL high are reserved for indicating the START and STOP conditions.

8.2 DSCL

This pin is the clock input for the DDC Monitor Port while in the bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

8.3 VCLK

This pin is the clock input for the DDC Monitor Port while in the Transmit-Only Mode. In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the bi-directional Mode, a high logic level is required on this pin to enable write capability.

8.4 $\overline{\text{DWP}}$

This pin is used for flexible write protection of the DDC Monitor Port. When the last memory location (7Fh) is written with any data, this pin is enabled and determines the write capability of the 24LCS41.

The $\overline{\text{WP}}$ pin has an internal pull up resistor which will allow write capability (assuming VCLK = 1 at all times if this pin is floated.

8.5 MSCL

This pin is the clock input for the Microcontroller Access Port, and is used to synchronize data transfer to and from the device.

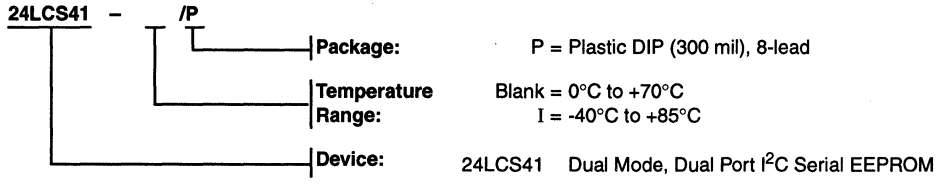
8.6 MSDA

This pin is used to transfer addresses and data into and out of the Microcontroller Access Port. This pin is an open drain terminal, therefore the MSDA bus requires a pullup resistor to Vcc (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

MSDA is allowed to change only during MSCL low. Changes during MSCL high are reserved for indicating the START and STOP conditions.

24LCS41 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

24LCS41A

1K/4K 2.5V Dual Mode, Dual Port I²C™ Serial EEPROM

FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification, including recovery to DDC1
- Improved noise immunity
- Separate high speed 2-wire bus for microcontroller access to 4K-bit Serial EEPROM
- Low power CMOS technology
- 2 mA active current typical
- 20 µA standby current typical at 5.5V
- Dual 2-wire serial interface bus, I²C™ compatible
- Hardware write-protect for DDC Monitor Port
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes (DDC port) or 16 bytes (4K Port)
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- 1,000,000 erase/write cycles guaranteed
- Data retention > 40 years
- 8-pin PDIP package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

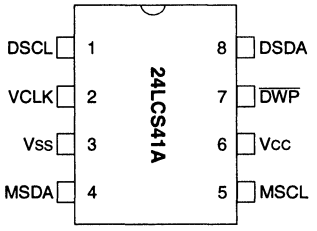
The Microchip Technology Inc. 24LCS41A is a dual-port 128 x 8 and 512 x 8-bit Electrically Erasable PROM (EEPROM). This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Three modes of operation have been implemented:

- Transmit-Only Mode for the DDC Monitor Port
- Bi-directional Mode for the DDC Monitor Port
- Bi-directional, industry-standard 2-wire bus for the 4K Microcontroller Access Port

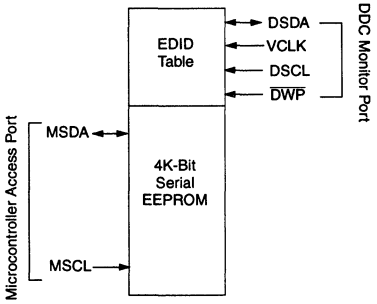
Upon power-up, the DDC Monitor Port will be in the Transmit-Only Mode, repeatedly sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the DSCL pin will cause the device to enter the transition mode, an look for a valid control byte on the I²C bus. If it detects a valid control byte from the master, it will switch to Bi-directional Mode, with byte selectable read/write capability of the memory array using DSCL. If no control byte is received, the device will revert to the Transmit-Only Mode after it received 128 consecutive VCLK pulses while the DSCL pin is idle. The 4K-bit microcontroller port is completely independent of the DDC port, therefore, it can be accessed continuously by a microcontroller without interrupting DDC transmission activity. The 24LCS41A is available in a standard 8-pin PDIP package in both commercial and industrial temperature ranges.

PACKAGE TYPE

PDIP



BLOCK DIAGRAM



DDC is a trademark of Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
DSCL	Serial Clock for DDC Bi-directional Mode (DDC2)
DSDA	Serial Address and Data I/O (DDC Bus)
VCLK	Serial Clock for DDC transmit-only mode (DDC1)
MSCL	Serial clock for 4K-bit MCU port
MSDA	Serial Address and Data I/O for 4K-bit MCU port
$\overline{DWP}$	Hardware write-protect for DDC Monitor Port
VSS	Ground
VCC	+2.5V to +5.5V power supply

TABLE 1-2: DC CHARACTERISTICS

	VCC = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
DSCL, DSDA, MSCL & MSDA pins: High level input voltage Low level input voltage	 VIH VIL	 .7 VCC —	 — .3 VCC	 V V	
Input levels on VCLK pin: High level input voltage Low level input voltage	 VIH VIL	 2.0 —	 .8 .2 VCC	 V V	 VCC ≥ 2.7V (Note) VCC < 2.7V (Note)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL1	—	.4	V	IOL = 3 mA, VCC = 2.5V (Note)
Low level output voltage	VOL2	—	.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN =.1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT =.1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note), Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, DSCL or MSCL = 400 kHz
Standby current	ICCS	— —	60 200	µA µA	VCC = 3.0V, DSDA or MSDA = DSCL or MSCL = VCC VCC = 5.5V, DSDA or MSDA = DSCL or MSCL = VCC VCLK = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS (DDC MONITOR AND MICROCONTROLLER ACCESS PORTS)

DDC Monitor Port (Bi-directional Mode) and Microcontroller Access Port							
Parameter	**Symbol**	**Standard Mode**		**Vcc = 4.5 - 5.5V Fast Mode**		**Units**	**Remarks**
		Min	**Max**	**Min**	**Max**		
Clock frequency (DSCL and MSCL)	FCLK	—	100	—	400	kHz	
Clock high time (DSCL and MSCL)	THIGH	4000	—	600	—	ns	
Clock low time (DSCL and MSCL)	TLOW	4700	—	1300	—	ns	
DSCL, DSDA, MSCL & MSDA rise time	TR	—	1000	—	300	ns	(Note 1)
DSCL, DSDA, MSCL & MSDA fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + .1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (DSCL, DSDA, MSCL & MSDA pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)
DDC Monitor Port Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of DSCL or MSCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

2.0 FUNCTIONAL DESCRIPTION

2.1 DDC Monitor Port

The DDC Monitor Port operates in two modes, the Transmit-Only Mode and the Bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input and sharing a common data line (DSDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the DSDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the DSCL input. When a valid transition on DSCL is recognized, the device will switch into the Bi-directional Mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bi-directional Mode. Otherwise, it will revert to the Transmit-Only Mode after it sees 128 VCLK pulses.

2.1.1 TRANSMIT-ONLY MODE

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional 2-wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (Section 2.1.2). In this mode, data is transmitted on the DSDA pin in 8-bit bytes, each followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted by most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The Bi-directional Mode Clock (DSCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.1.2 INITIALIZATION PROCEDURE

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the DSDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

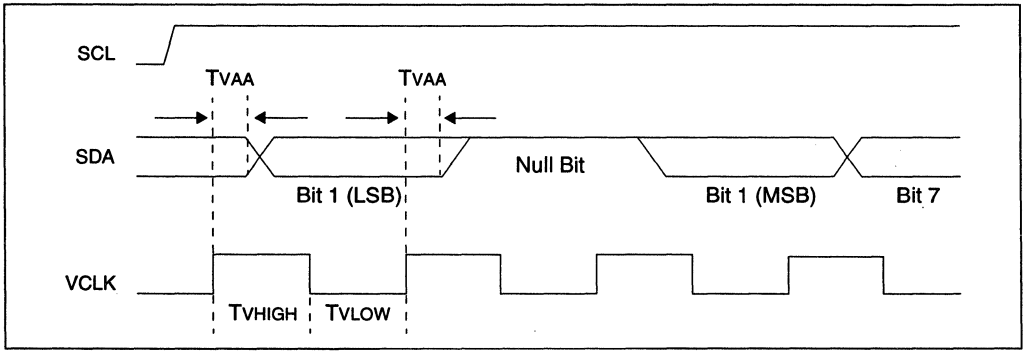
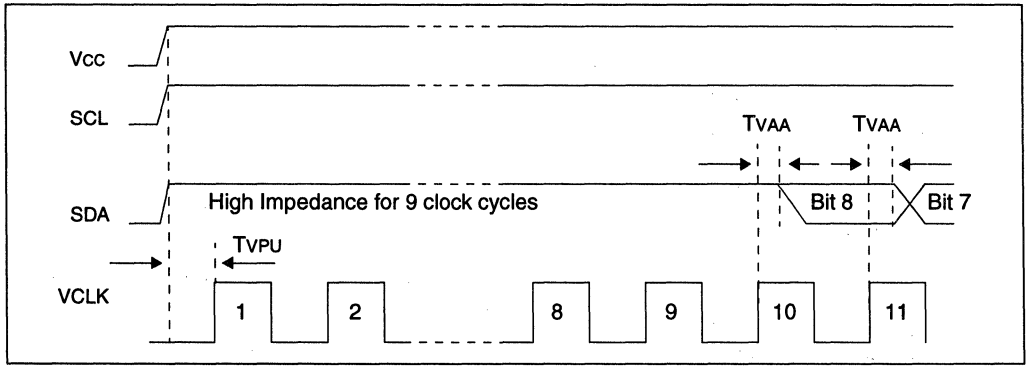


FIGURE 2-2: DEVICE INITIALIZATION



2.1.3 BI-DIRECTIONAL MODE

Before the 24LCS41A can be switched into the Bi-directional Mode (Figure 2-4), it must enter the transition mode, which is done by applying a valid high to low transition on the Bi-directional Mode Clock (DSCL). As soon it enters the transition mode, it looks for a control byte 1010 000X on the I^2C™ bus, and starts to count pulses on VCLK. Any high to low transition on the DSCL line will reset the count. If it sees a pulse count of 128 on VCLK while the DSCL line is idle, it will revert back to the Transmit-Only Mode, and transmit its contents starting with the most significant bit in address 00h. However, if it detects the control byte on the I^2C bus, (Figure 2-3) it will switch to the in the Bi-directional Mode. Once the device has made the transition to the Bi-directional mode, the only way to switch the device back to the Transmit-Only Mode is to remove power from the device. The mode transition process is shown in detail in Figure 2-4.

Once the device has switched into the Bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire Bi-directional data transmission protocol (I^2C). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-directional Mode Clock (DSCL), controls access to the bus and generates the START and STOP conditions, while the monitor port acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bi-directional mode, the monitor port only responds to commands for device 1010 000X.

2.2 Microcontroller Access Port

The Microcontroller Access Port supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (MSCL), controls the bus access, and generates the START and STOP conditions, while the Microcontroller Access Port works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

FIGURE 2-3: SUCCESSFUL MODE TRANSITION TO BI-DIRECTIONAL MODE

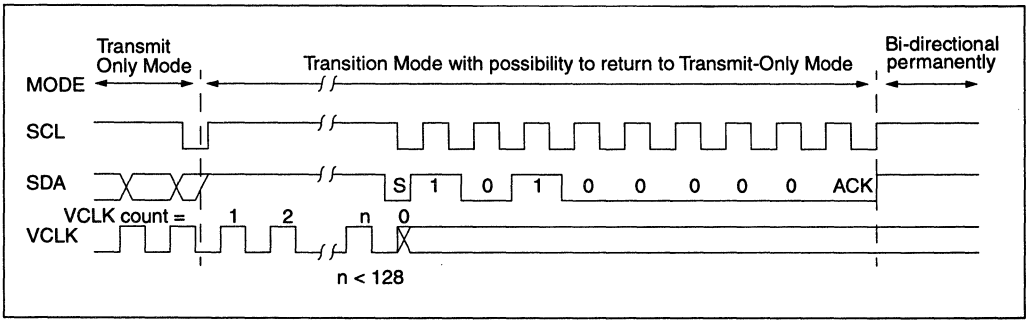


FIGURE 2-4: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE

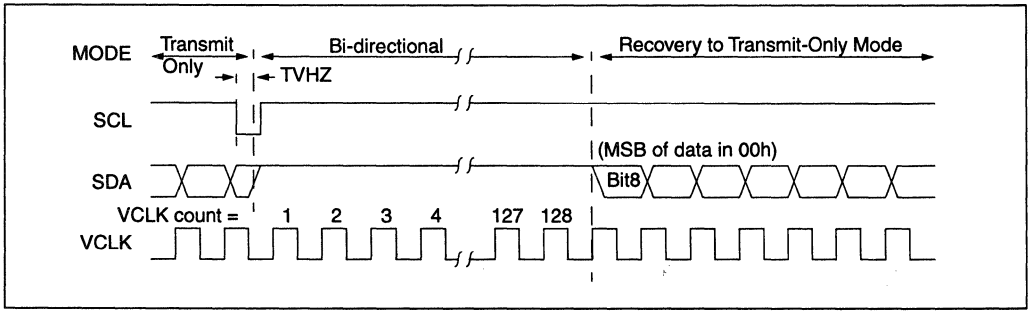
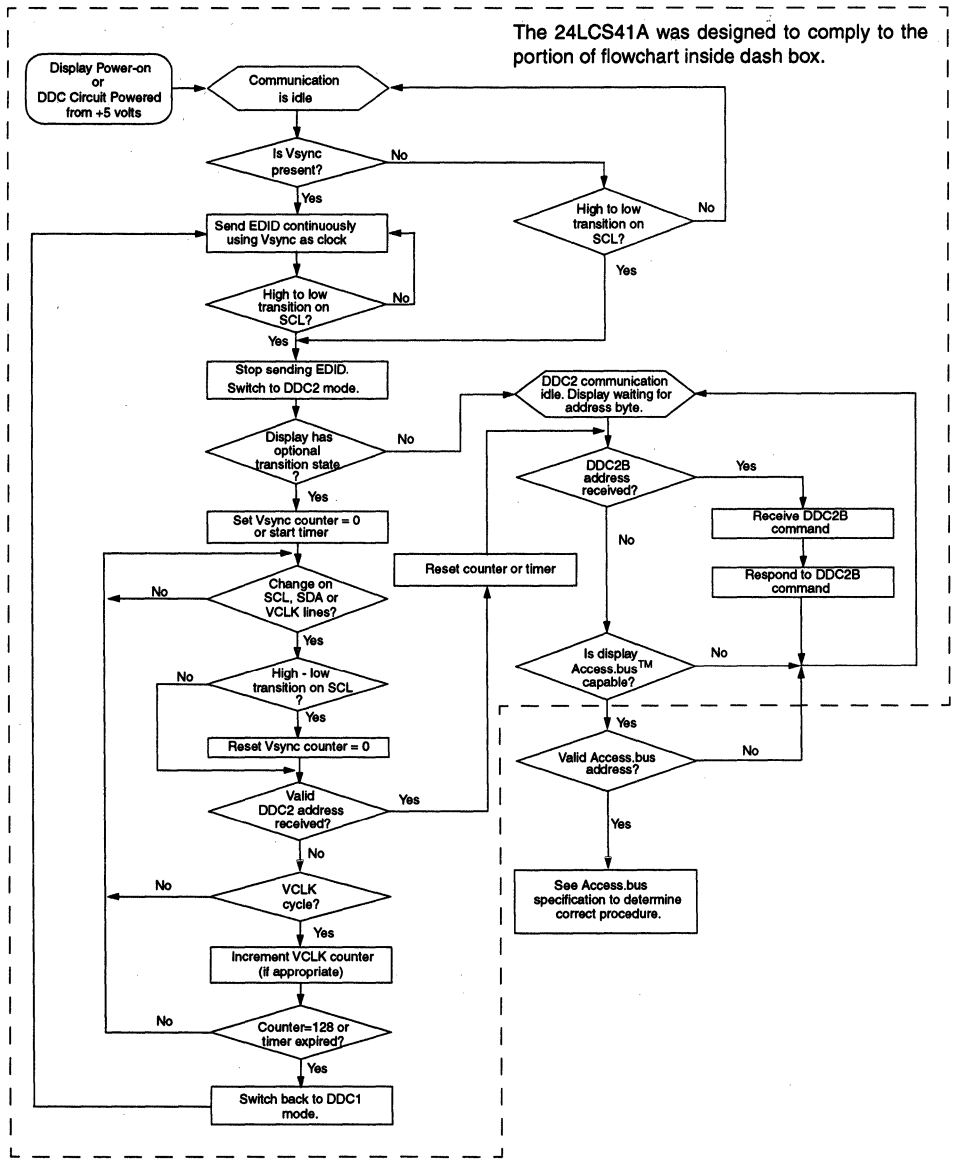


FIGURE 2-5: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA



Note 1: The base flowchart is copyright © 1993, 1994, 1995 Video Electronic Standard Association (VESA) from VESA's Display Data Channel (DDC) Standard Proposal ver. 2p rev. 0, used by permission of VESA.

2: The dash box and text "The 24LCS41A and ... inside dash box." are added by Microchip Technology, Inc.

3: Vsync signal is normally used to derive a signal for VCLK pin on the 24LCS41A.

3.0 BI-DIRECTIONAL BUS CHARACTERISTICS

Characteristics for the Bi-directional bus are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus Not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The microcontroller access port and the DDC Monitor Port (in Bi-directional Mode) will not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the DSDA or MSDA line during the acknowledge clock pulse in such a way that the DSDA or MSDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The first part of the control byte consists of a 4-bit control code. This control code is set as 1010 for both read and write operations and is the same for both the DDC Monitor Port and Microcontroller Access Port. The next three bits of the control byte are block select bits (B1, B2, and B0). All three of these bits are zero for the DDC Monitor Port. The B2 and B1 bits are don't care bits for the Microcontroller Access Port, and the B0 bit is used by the Microcontroller Access Port to select which of the two 256 word blocks of memory are to be accessed (Figure 3-4). The B0 bit is effectively the most significant bit of the word address. The last bit of the control byte defines the operation to be performed. When set to one, a read operation is selected; when set to zero, a write operation is selected. Following the start condition, the device monitors the DSDA or MSDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the device will select a read or a write operation. The DDC Monitor Port and Microcontroller Access Port can be accessed simultaneously because they are completely independent of one another.

Operation	Control Code	Chip Select	R/W
Read	1010	B1B2B0	1
Write	1010	B1B2B0	0

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

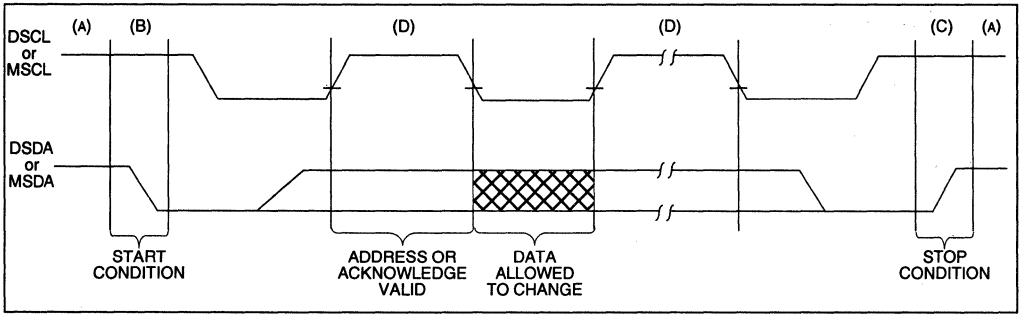


FIGURE 3-2: BUS TIMING START/STOP

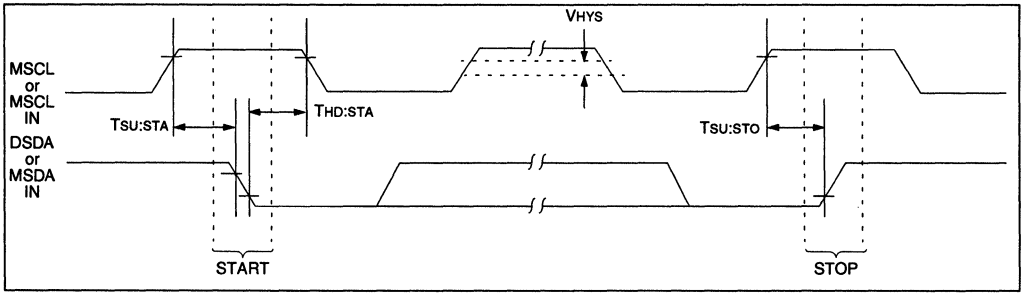


FIGURE 3-3: BUS TIMING DATA

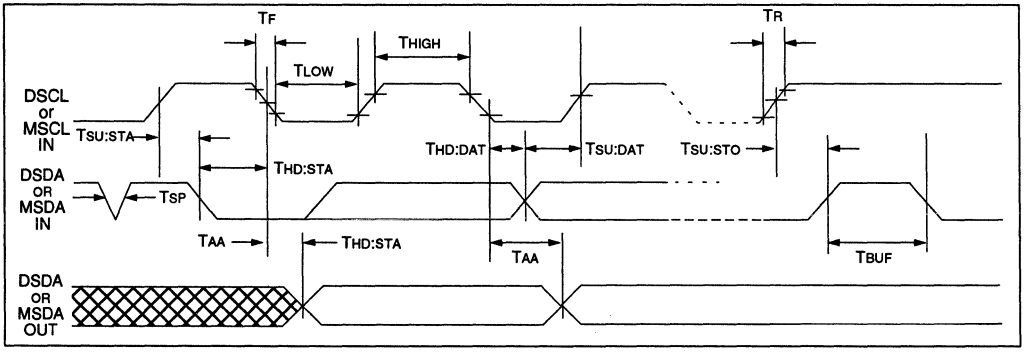
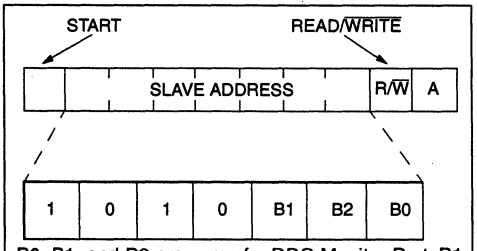


FIGURE 3-4: CONTROL BYTE ALLOCATION



B0, B1, and B2 are zeros for DDC Monitor Port. B1 and B2 are don't care bits for the Microcontroller Access Port, and B0 is used to select which of the two 256 word blocks of memory are to be accessed.

4.0 WRITE OPERATION

Write operations are identical for the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port, with the exception of the VCLK and $\overline{DWP}$ pins noted in the next sections. Data can be written using either a byte write or page write command. Write commands for the DDC Monitor Port and the Microcontroller Access Port are completely independent of one another.

4.1 Byte Write

Following the start signal from the master, the slave address (4-bits), the chip select bits (3-bits) and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the port. After receiving another acknowledge signal from the port, the master device will transmit the data word to be written into the addressed memory location. The port acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time, the port will not generate acknowledge signals (Figure 4-1).

For the DDC Monitor Port it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming. The $\overline{DWP}$ pin must be held high for the duration of the write protection.

4.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the port in the same way as in a byte write. But, instead of generating a stop condition, the master transmits up to eight data bytes to the DDC Monitor Port or 16 bytes to the Microcontroller Access Port, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order 5-bits of the word address remains constant. If the master should transmit more than eight words to the DDC Monitor Port or 16 words to the Microcontroller Access Port prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).

For the DDC Monitor Port, it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming. For the DDC Monitor Port, the $\overline{DWP}$ pin must be held high for the duration of the write cycle.

FIGURE 4-1: BYTE WRITE

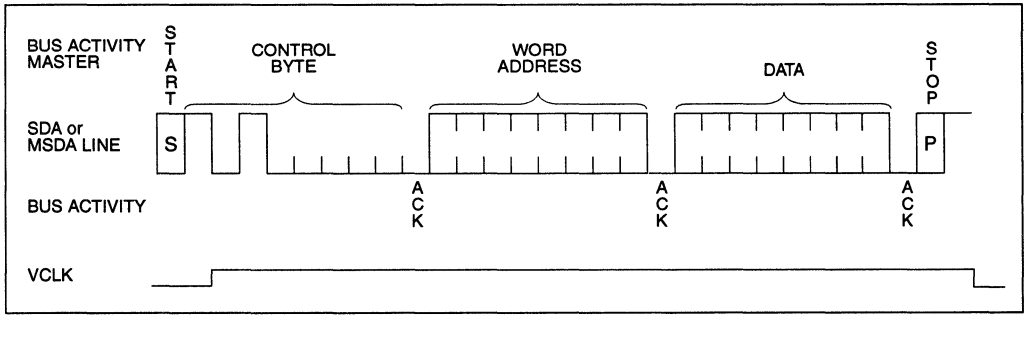


FIGURE 4-2: PAGE WRITE

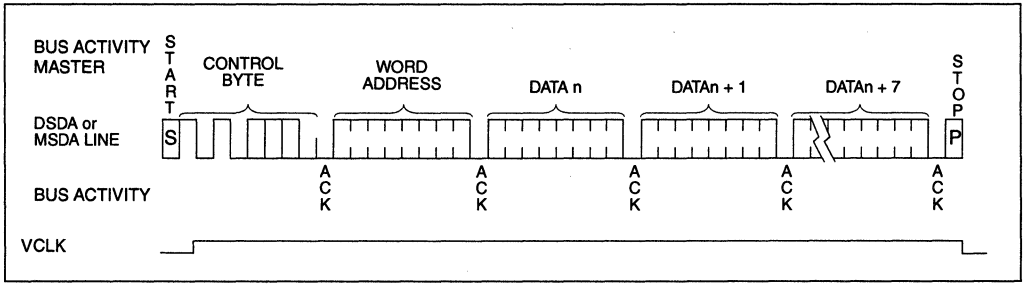
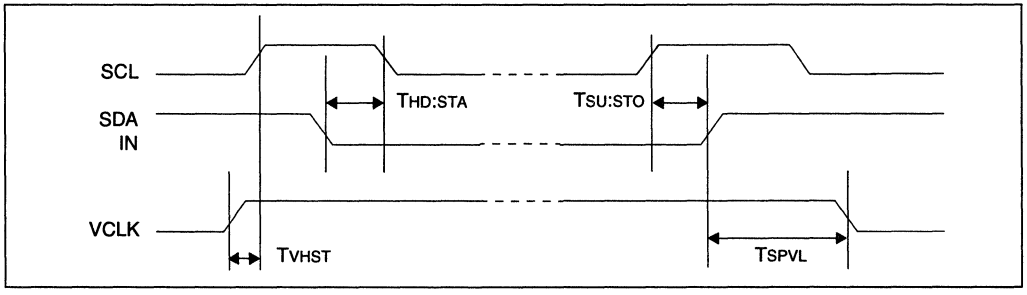


FIGURE 4-3: VCLK WRITE ENABLE TIMING

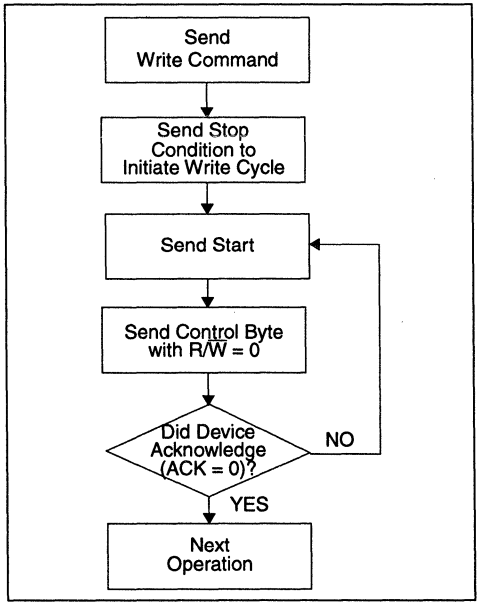


5.0 ACKNOWLEDGE POLLING

Acknowledge polling can be done for both the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port.

Since the port will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize but throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$=0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

6.1 DDC Monitor Port

When using the DDC Monitor Port in the Bi-directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the monitor port to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

Additionally, the $\overline{DWP}$ pin performs a flexible write protect function. The port contains a write-protection control fuse whose factory default state is cleared. Writing any data to address 7Fh (normally the checksum in DDC applications) sets the fuse which enables the $\overline{DWP}$ pin. Until this fuse is set, the monitor port is always write enabled (if VCLK = 1). After the fuse is set, the write capability of the 24LCS41A is determined by $\overline{DWP}$ (Table 6-1).

TABLE 6-1: WRITE PROTECT TRUTH TABLE

VCLK	$\overline{WP}$	Add. 7Fh Written	Mode
0	X	X	Read Only
1	X	No	R/$\overline{W}$
1	1/open	Yes	R/$\overline{W}$
1	0	Yes	Read Only

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read. These operations are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port and are completely independent of one another.

7.1 Current Address Read

The port contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the port issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the port as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The port then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the port transmits the first data byte, and the master issues an acknowledge as opposed to a stop condition in a random read. This directs the port to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads, the port contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

Both the DDC Monitor Port and Microcontroller Access Port employ a Vcc threshold detector circuit which disables the internal erase/write logic, if the Vcc is below 1.5 volts at nominal conditions.

The VCLK, DSCL, MSCL, DSDA, and MSDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

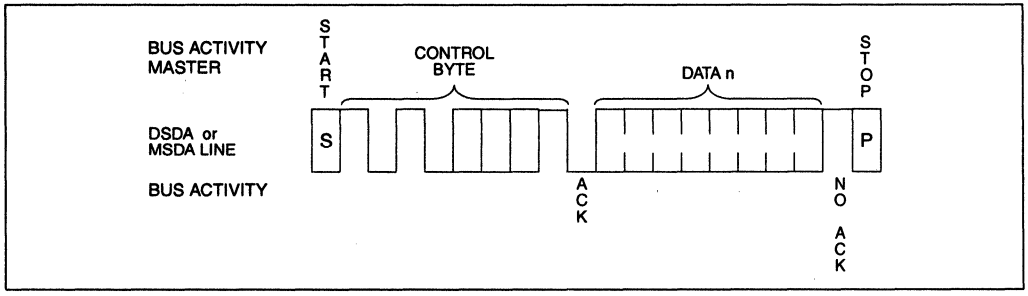


FIGURE 7-2: RANDOM READ

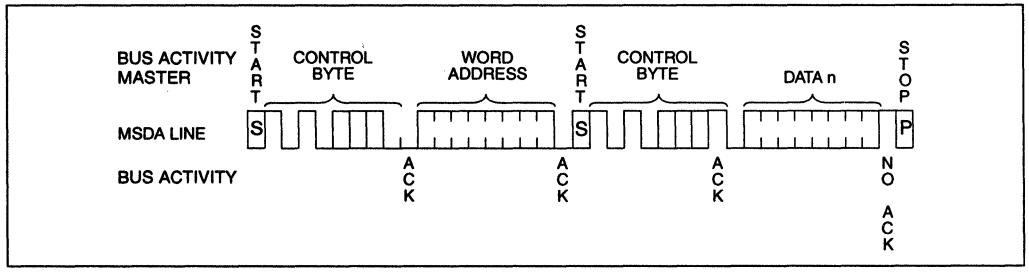
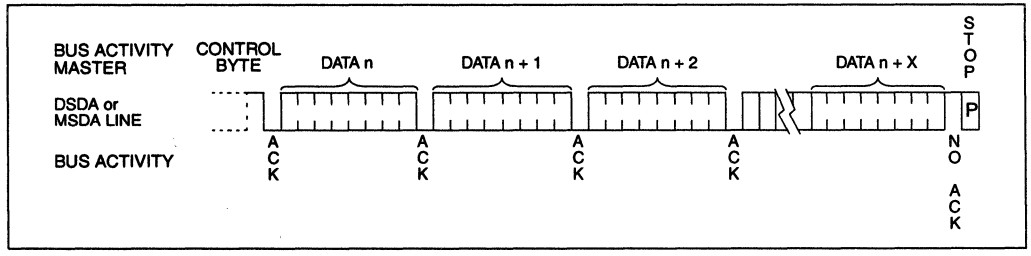


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 DSDA

This pin is used to transfer addresses and data into and out of the DDC Monitor Port, when the device is in the Bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the DSDA pin. This pin is an open drain terminal, therefore the DSDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2KΩ for 400 kHz).

For normal data transfer in the Bi-directional Mode, DSDA is allowed to change only during DSCL or MSDA low. Changes during DSCL high are reserved for indicating the START and STOP conditions.

8.2 DSCL

This pin is the clock input for the DDC Monitor Port while in the Bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the Bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

8.3 VCLK

This pin is the clock input for the DDC Monitor Port while in the Transmit-Only Mode. In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-directional Mode, a high logic level is required on this pin to enable write capability.

8.4 $\overline{\text{DWP}}$

This pin is used for flexible write protection of the DDC Monitor Port. When the last memory location (7Fh) is written with any data, this pin is enabled and determines the write capability of the DDC port.

The $\overline{\text{DWP}}$ pin has an internal pull up resistor which will allow write capability (assuming VCLK = 1) at all times if this pin is floated.

8.5 MSCL

This pin is the clock input for the Microcontroller Access Port, and is used to synchronize data transfer to and from the device.

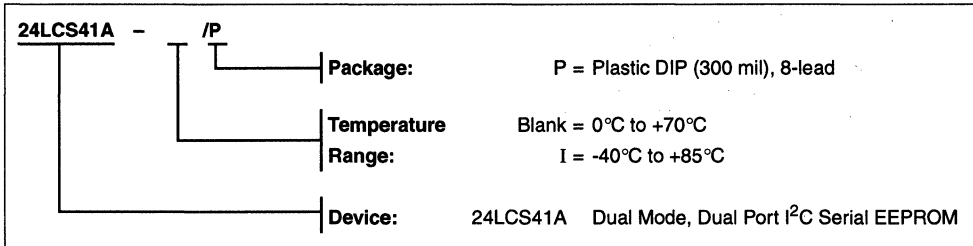
8.6 MSDA

This pin is used to transfer addresses and data into and out of the Microcontroller Access Port. This pin is an open drain terminal, therefore the MSDA bus requires a pullup resistor to Vcc (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

MSDA is allowed to change only during MSCL low. Changes during MSCL high are reserved for indicating the START and STOP conditions.

24LCS41A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Web Site (www.microchip.com)

MICROCHIP

SECTION 7
PARALLEL EEPROM
PRODUCT SPECIFICATIONS

28C04A	4K (512 x 8) CMOS EEPROM	7-1
28C16A	16K (2K x 8) CMOS EEPROM	7-9
28C17A	16K (2K x 8) CMOS EEPROM	7-17
28C64A	64K (8K x 8) CMOS EEPROM	7-25
28LV64A	64K (8K x 8) Low Voltage CMOS EEPROM	7-33

28C04A

4K (512 x 8) CMOS EEPROM

FEATURES

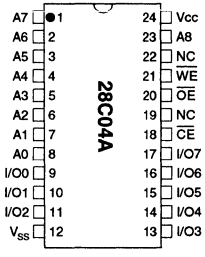
- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >200 years
- Endurance - Minimum 10^4 Erase/Write Cycles
  - Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- 5-Volt-Only Operation
- Organized 512x8 JEDEC standard pinout
  - 24-pin Dual-In-Line Package
  - 32-pin PLCC Package
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

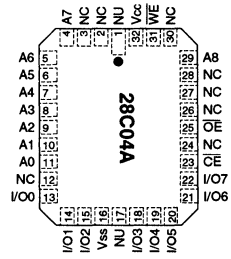
The Microchip Technology Inc. 28C04A is a CMOS 4K non-volatile electrically Erasable and Programmable Read Only Memory (EEPROM). The 28C04A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C04A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES

DIP

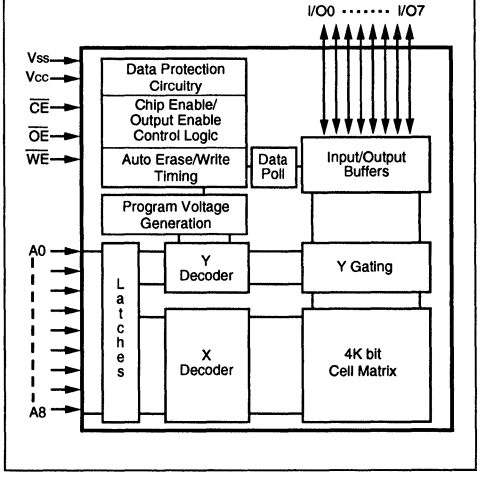


PLCC



• Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



7

Parallel EEPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss.....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V

Output Voltage w.r.t. Vss.....-0.6V to Vcc+0.6V

Storage temperature .....-65°C to +125°C

Ambient temp. with power applied.....-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

			Vcc = +5V ±10% Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic '1' Logic '0'	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V TO Vcc + 0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; TAMB = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1 $\overline{OE}$ = Vcc All inputs equal Vcc or Vss

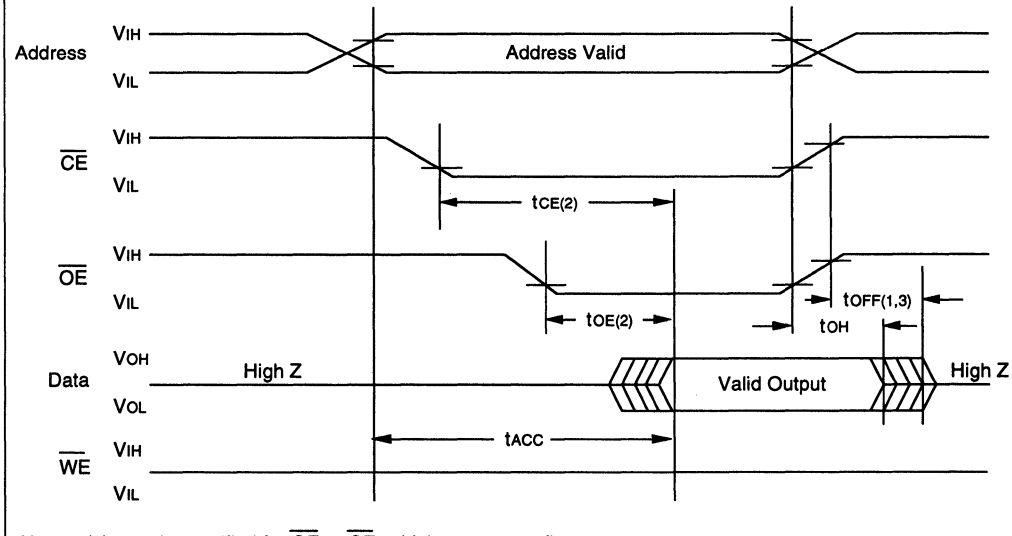
Note 1: AC power supply current above 5 MHz; 1 mA/MHz.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C									
Parameter	**Sym**	**28C04A-15**		**28C04A-20**		**28C04A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ to $\overline{OE}$ High Output Float	tOFF	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0		0		0		ns	
Endurance	—	1M	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note)

Note: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise/Fall Times:	20 nsec	
Ambient Temperature:	Commercial (C): Tamb= 0°C to 70°C	
	Industrial (I): Tamb= -40°C to 85°C	

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C04A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	t_{WC}		200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

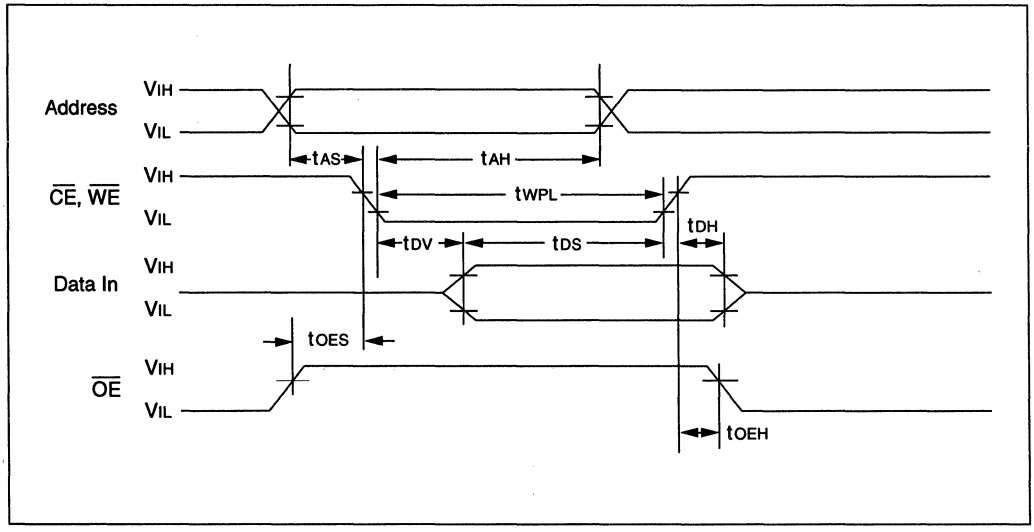


FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

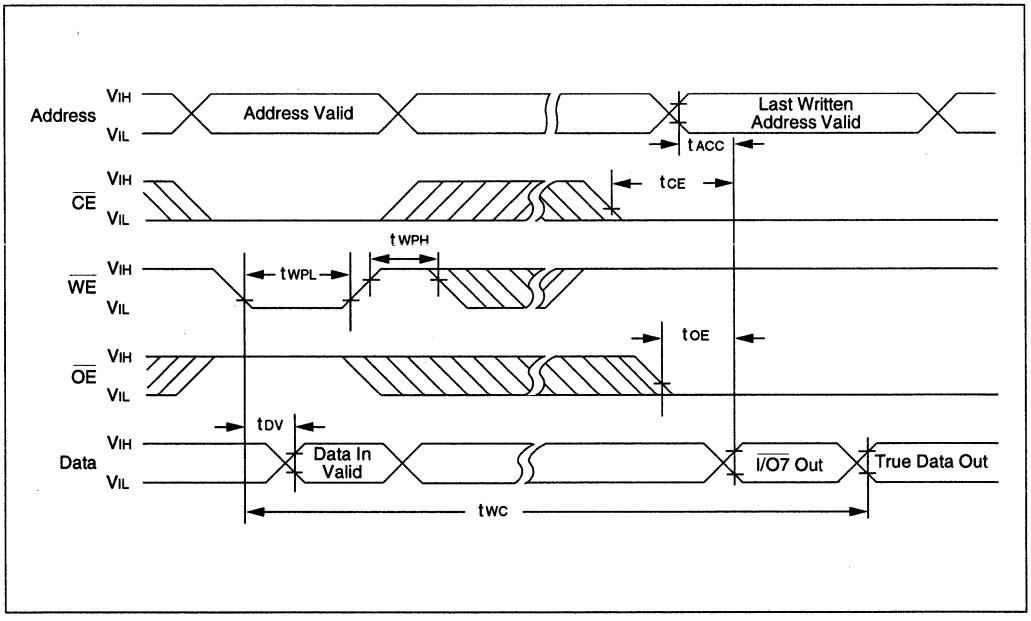
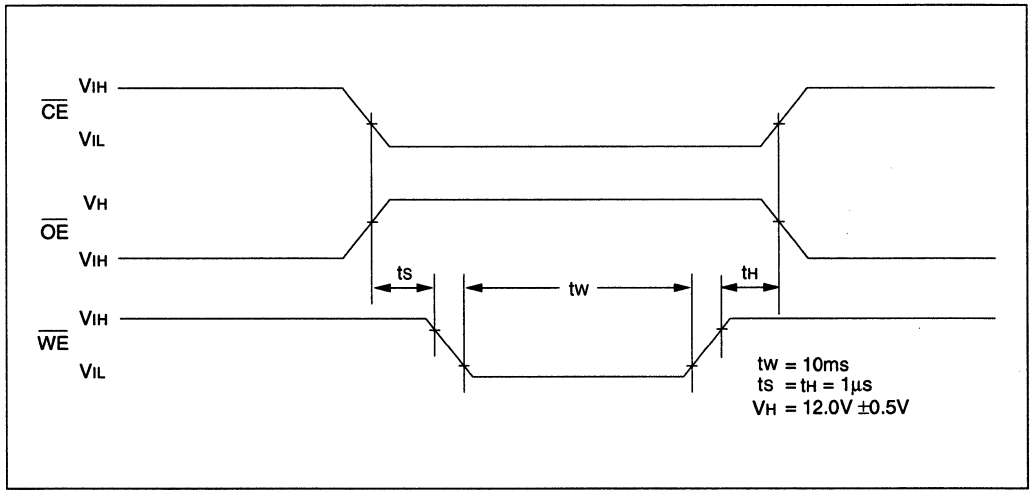


FIGURE 1-4: CHIP CLEAR WAVEFORMS



7

Parallel EEPROM

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{IE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

2.1 Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

2.2 Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

2.4 Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

2.5 Data Polling

The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

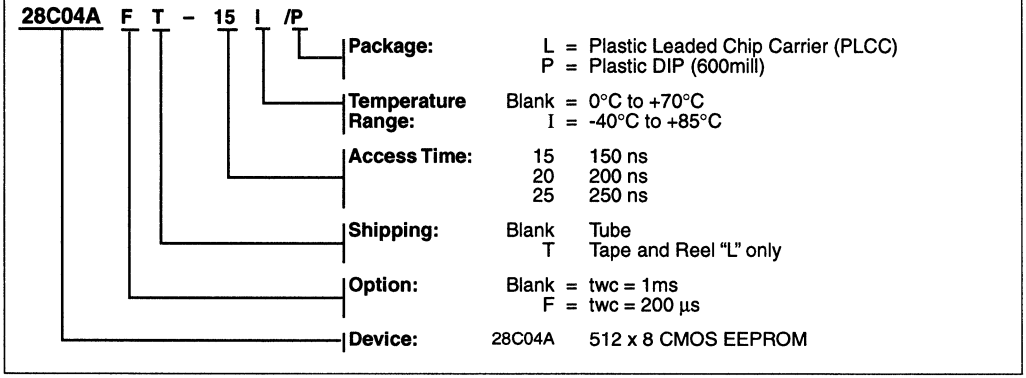
2.6 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

NOTES

28C04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

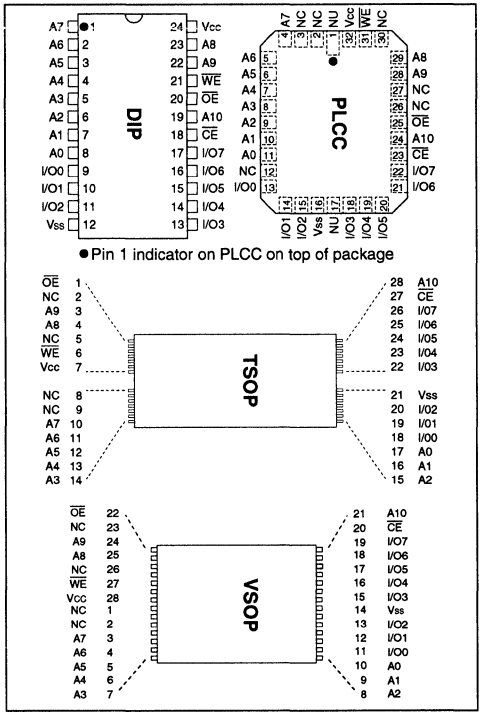
28C16A

16K (2K x 8) CMOS EEPROM

FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >200 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ polling
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
- 24-pin Dual-In-Line Package
- 32-pin PLCC Package
- 28-pin Thin Small Outline Package (TSOP) 8x20mm
- 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

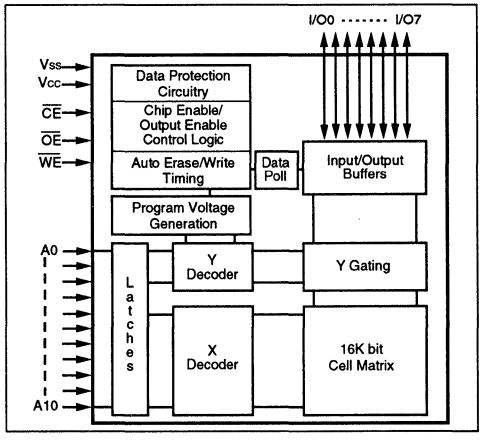
PACKAGE TYPES



DESCRIPTION

The Microchip Technology Inc. 28C16A is a CMOS 16K non-volatile electrically Erasable PROM. The 28C16A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C16A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

BLOCK DIAGRAM



7

Parallel EEPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss.....-0.6V to +13.5V

Voltage on A9 w.r.t. Vss.....-0.6V to +13.5V

Output Voltage w.r.t. Vss.....-0.6V to Vcc+0.6V

Storage temperature .....-65°C to +125°C

Ambient temp. with power applied.....-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

Vcc = +5V ±10%
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic '1' Logic '0;	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1 $\overline{OE}$ = Vcc Other inputs equal Vcc or Vss

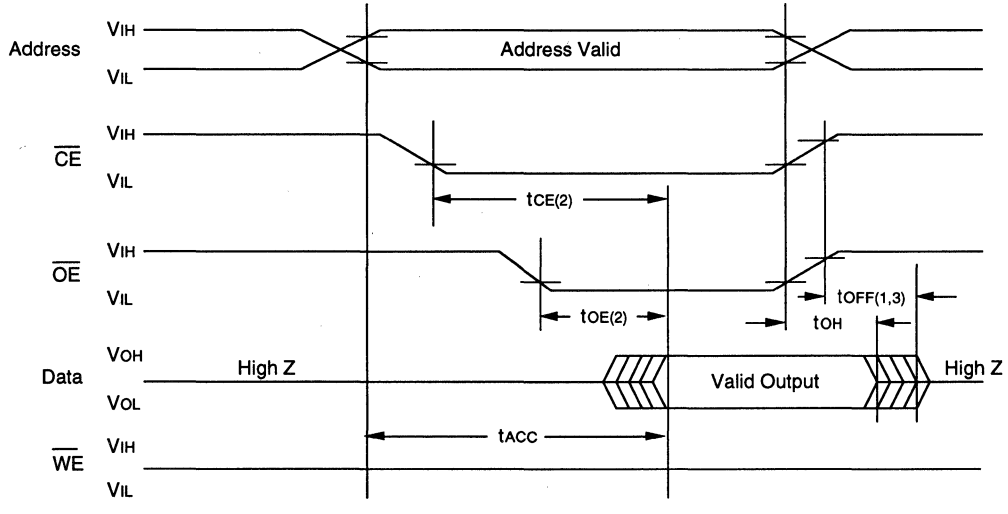
Note 1: AC power supply current above 5 MHz; 1 mA/MHz.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; Vol = 0.8V Output Load: 1 TTL Load + 100pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): Tamb = 0°C to +70°0°C Industrial (I): Tamb = -40°C to +85°C								
Parameter	**Sym**	**28C16A-15**		**28C16A-20**		**28C16A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	tOFF	0	50	0	55	0	70	ns	
Output Hold from $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0	—	0	—	0	—	ns	
Endurance	—	1M	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note)

Note: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise/Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C			
		Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	10	—	ns	
Address Hold Time	tAH	50	—	ns	
Data Set-Up Time	tDS	50	—	ns	
Data Hold Time	tDH	10	—	ns	
Write Pulse Width	tWPL	100	—	ns	Note 1
Write Pulse High Time	tWPH	50	—	ns	
$\overline{OE}$ Hold Time	tOEH	10	—	ns	
$\overline{OE}$ Set-Up Time	tOES	10	—	ns	
Data Valid Time	tDV	—	1000	ns	Note 2
Write Cycle Time (28C16A)	tWC	—	1	ms	0.5 ms typical
Write Cycle Time (28C16AF)	tWC	—	200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until tDH after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

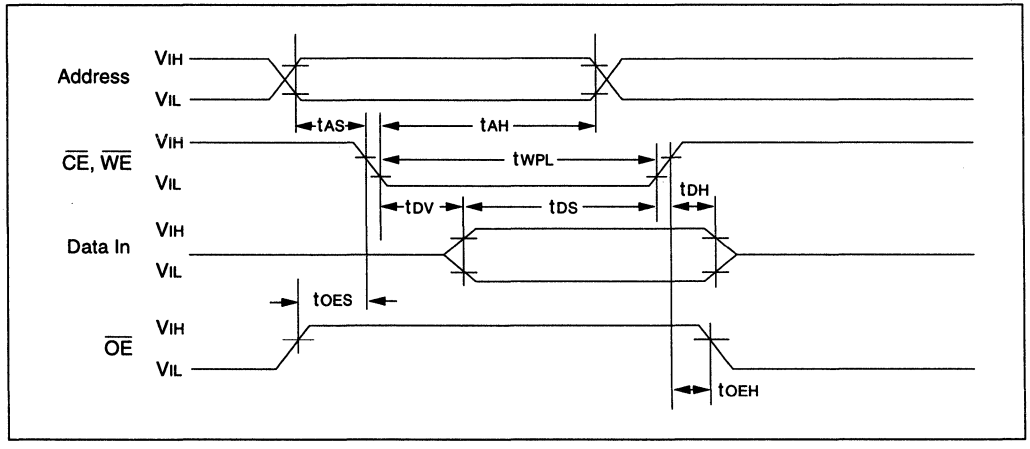


FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

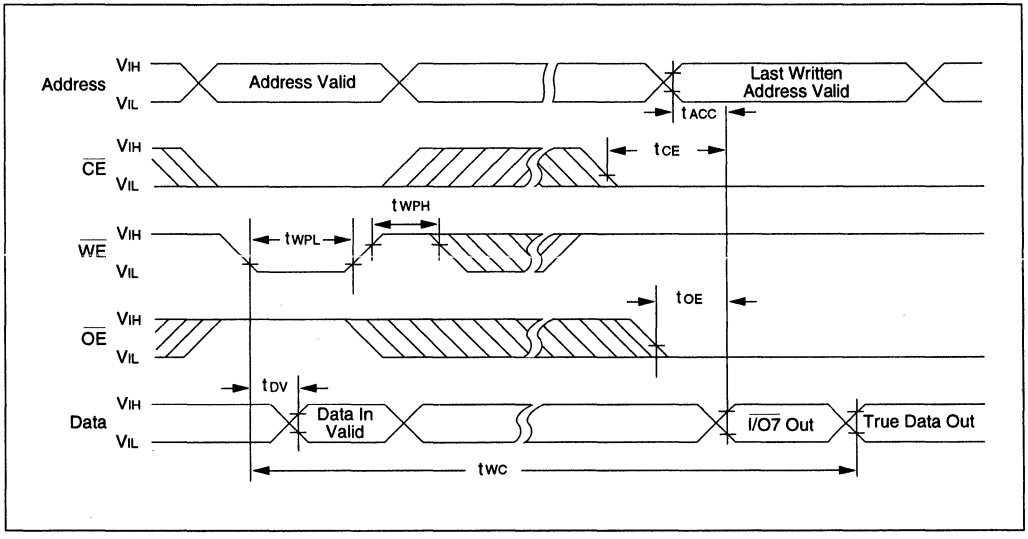


FIGURE 1-4: CHIP CLEAR WAVEFORMS

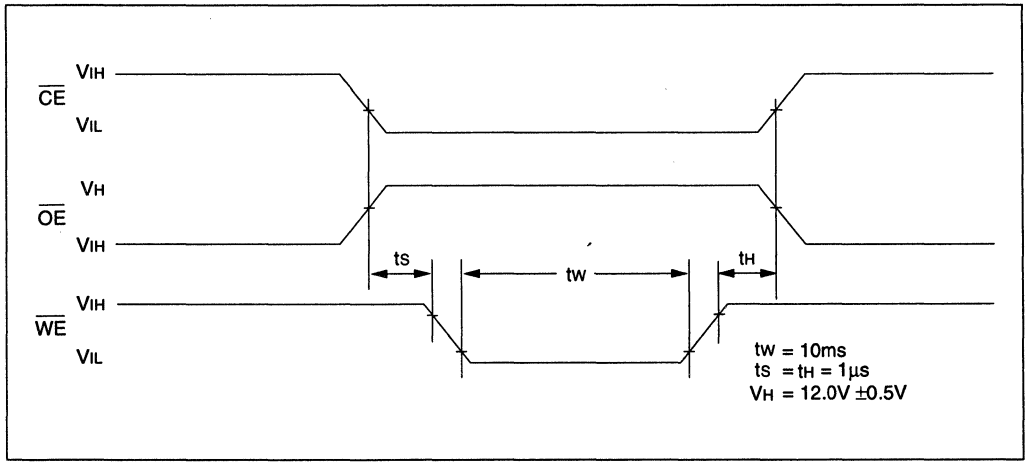


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In
Note 1: VH = 12.0V±0.5V		* Pulsed per programming waveforms.				

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C16A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

2.1 Read Mode

The 28C16A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

2.2 Standby Mode

The 28C16A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

2.4 Write Mode

The 28C16A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

2.5 Data Polling

The 28C16A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

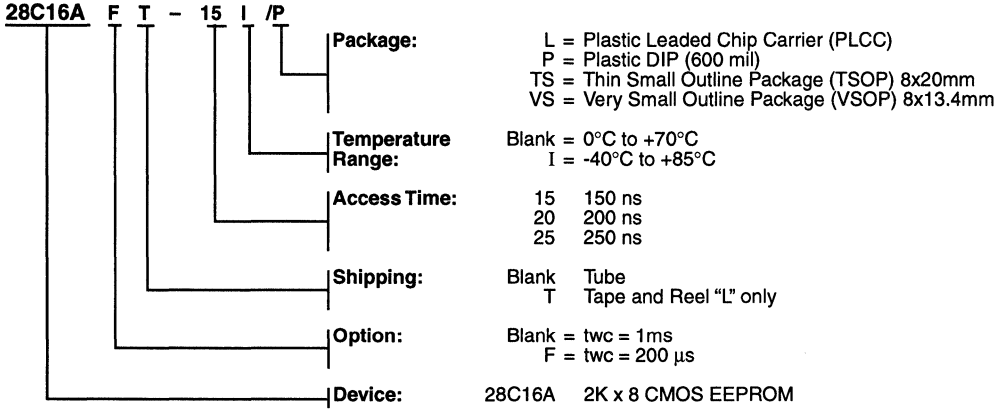
2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

28C16A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

28C17A

16K (2K x 8) CMOS EEPROM

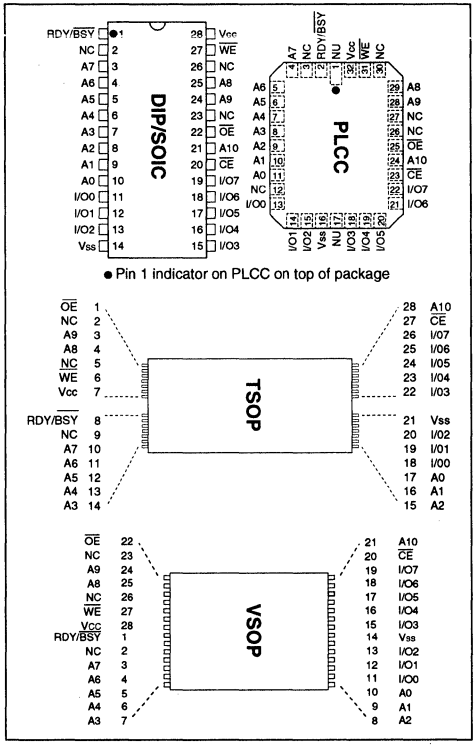
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >200 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- Data Polling; Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - 28 Pin Dual-In-Line Package
  - 32-Pin PLCC Package
  - 28-Pin Thin Small Outline Package (TSOP) 8x20mm
  - 28-Pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

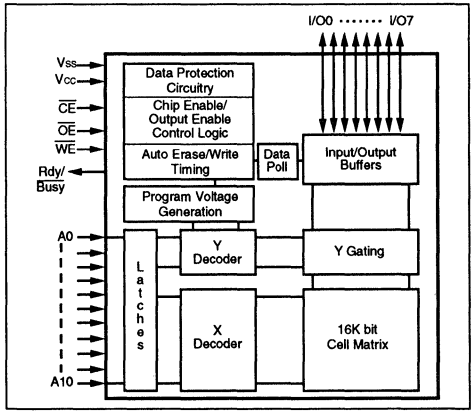
The Microchip Technology Inc. 28C17A is a CMOS 16K non-volatile electrically Erasable PROM. The 28C17A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES



● Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



7

Parallel EEPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V

Voltage on A9 w.r.t. Vss.....-0.6V to +13.5V

Output Voltage w.r.t. Vss.....-0.6V to Vcc+0.6V

Storage temperature .....-65°C to +125°C

Ambient temp. with power applied.....-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

			Vcc = +5V ±10% Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic '1' Logic '0'	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc +1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc +0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc +1 $\overline{OE}$ = Vcc All other inputs equal Vcc or Vss

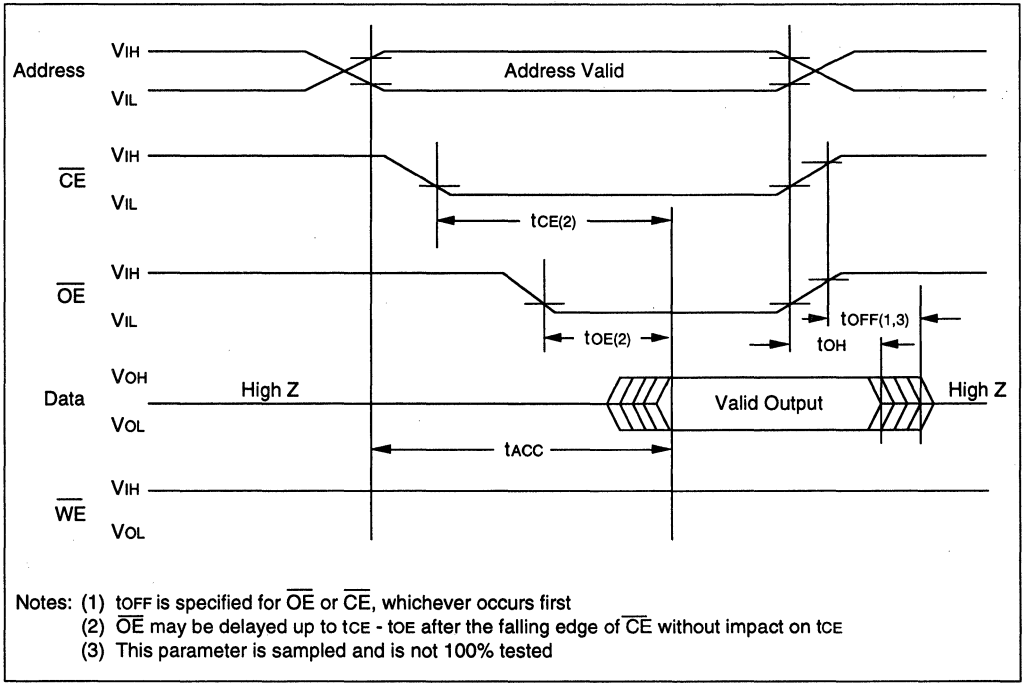
Note 1: AC power supply current above 5MHz: 1mA/MHz.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V							
	Output Load:	1 TTL Load + 100 pF							
	Input Rise and Fall Times:	20 ns							
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C							
Parameter	**Symbol**	**28C17A-15**		**28C17A-20**		**28C17A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	tOFF	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	tOH	0	—	0	—	0	—	ns	
Endurance	—	1M	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note)

Note: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:		V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V		
	Output Load:		1 TTL Load + 100 pF		
	Input Rise/Fall Times:		20 ns		
	Ambient Temperature:		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	10	—	ns	
Address Hold Time	tAH	50	—	ns	
Data Set-Up Time	tDS	50	—	ns	
Data Hold Time	tDH	10	—	ns	
Write Pulse Width	tWPL	100	—	ns	Note 1
Write Pulse High Time	tWPH	50	—	ns	
$\overline{OE}$ Hold Time	tOEH	10	—	ns	
$\overline{OE}$ Set-Up Time	tOES	10	—	ns	
Data Valid Time	tDV	—	1000	ns	Note 2
Time to Device Busy	tDB	2	50	ns	
Write Cycle Time (28C17A)	tWC	—	1	ms	0.5 ms typical
Write Cycle Time (28C17AF)	tWC	—	200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until tDH after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

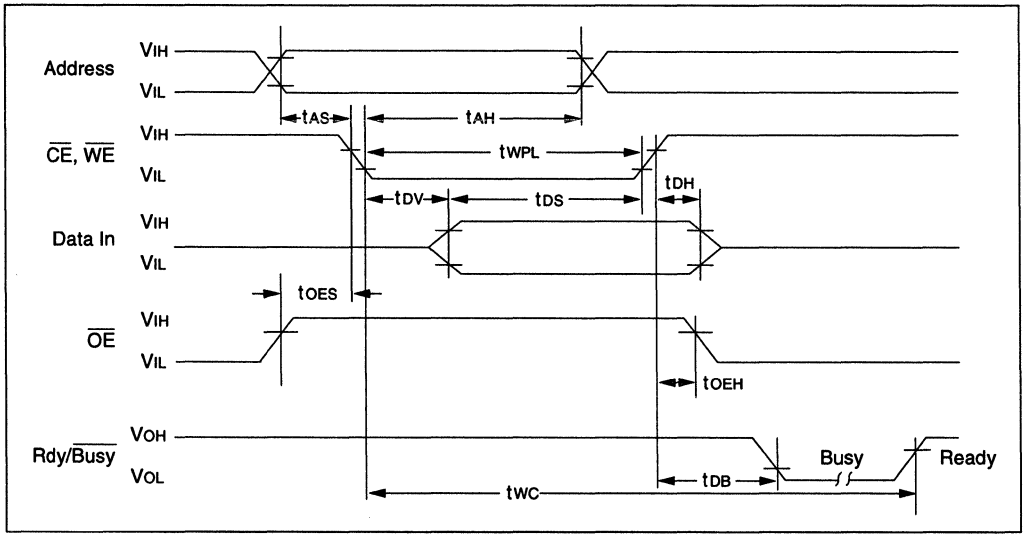


FIGURE 1-3: DATA POLLING WAVEFORMS

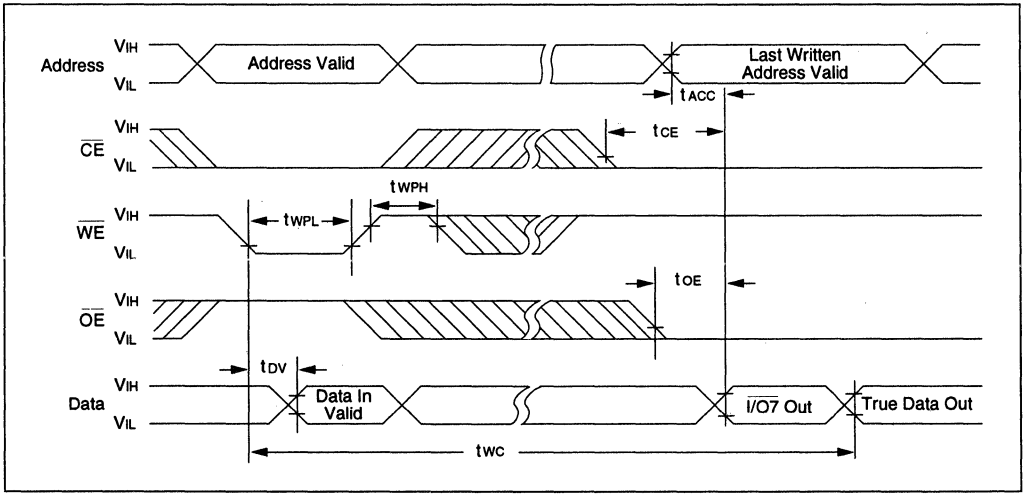


FIGURE 1-4: CHIP CLEAR WAVEFORMS

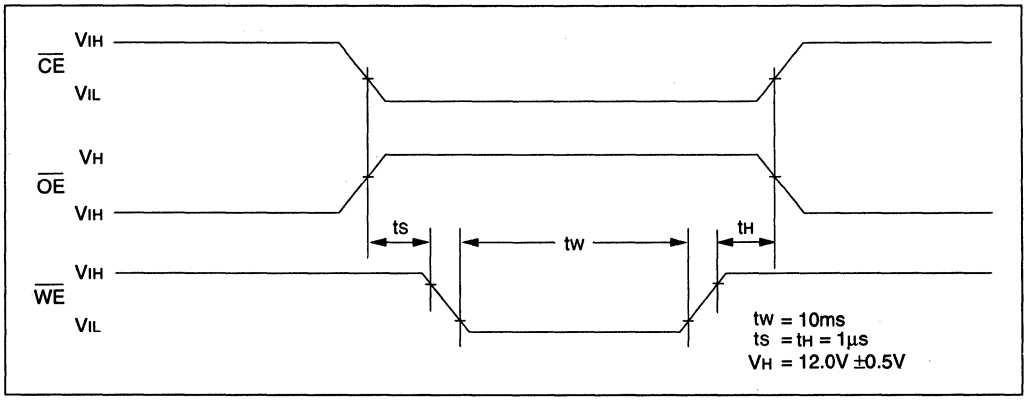


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	VCC	
Extra Row Read	VIL	VIL	VIH	A9 = VH	VCC	Data Out
Extra Row Write	*	VIH	*	A9 = VH	VCC	Data In

Note 1: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C17A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$ (1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note 1: Open drain output.
2: X = Any TTL level.

2.1 Read Mode

The 28C17A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that CE has been low and addresses have been stable for at least tACC-tOE.

2.2 Standby Mode

The 28C17A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

2.4 Write Mode

The 28C17A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C17A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C17A has completed writing and is ready to accept another cycle.

2.5 $\overline{Data}$ Polling

The 28C17A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

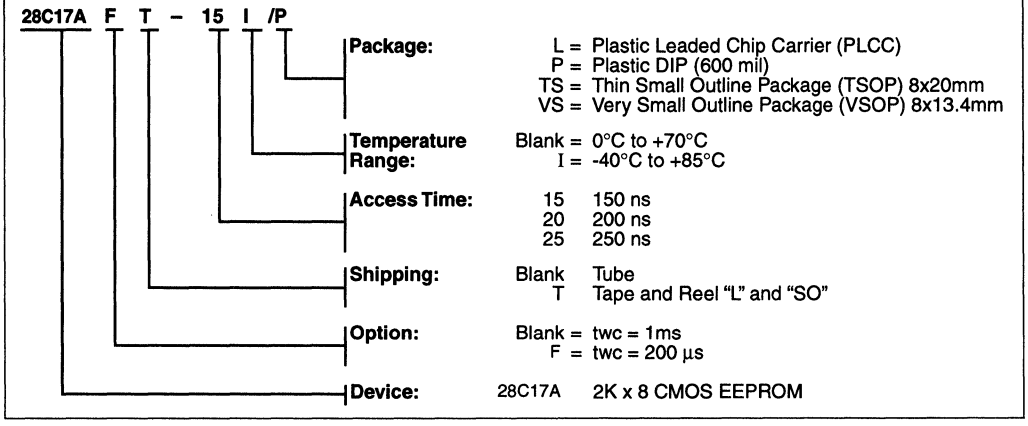
2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

28C17A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



28C64A

64K (8K x 8) CMOS EEPROM

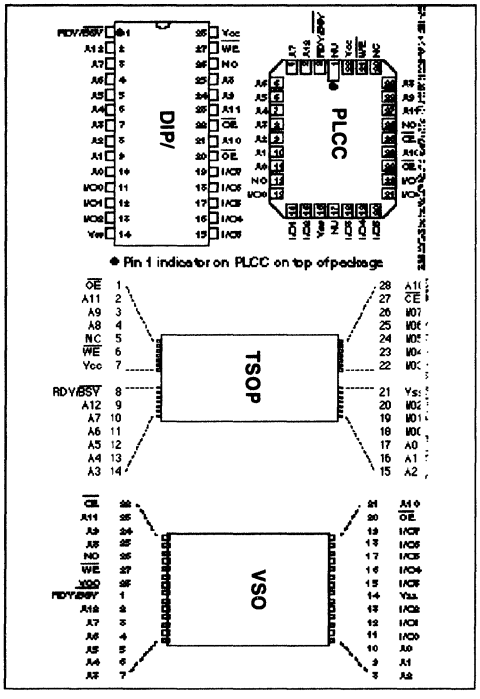
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >200 years
- High Endurance - Minimum 100,000 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 8Kx8 JEDEC Standard Pinout
  - 28-pin Dual-In-Line Package
  - 32-pin PLCC Package
  - 28-pin Thin Small Outline Package (TSOP) 8x20mm
  - 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

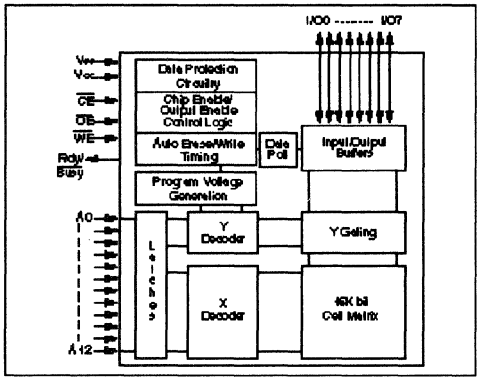
DESCRIPTION

The Microchip Technology Inc. 28C64A is a CMOS 64K non-volatile electrically Erasable PROM. The 28C64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES



BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V

Voltage on A9 w.r.t. Vss .....-0.6V to +13.5V

Output Voltage w.r.t. Vss.....-0.6V to Vcc+0.6V

Storage temperature .....-65°C to +125°C

Ambient temp. with power applied.....-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTIC

Vcc = +5V ±10%
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic '1' Logic '0'	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc +1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz (Note 2)
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc +0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz (Note 2)
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc +1 $\overline{OE}$ = $\overline{WE}$ = Vcc All other inputs equal Vcc or Vss

Note 1: AC power supply current above 5MHz: 2mA/MHz.
2: Not 100% tested.

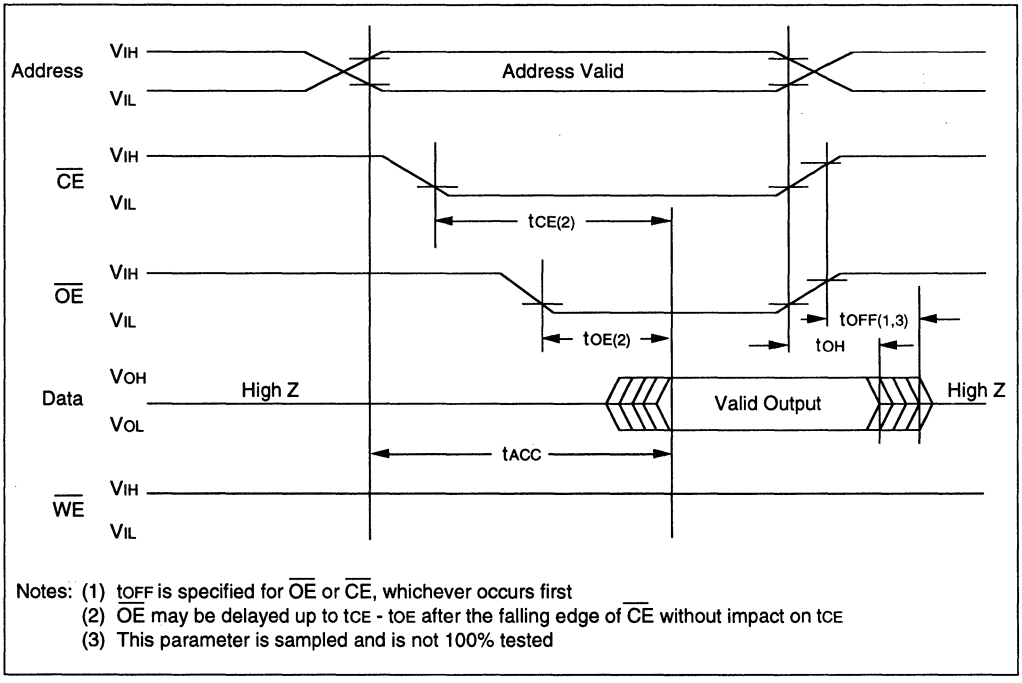
TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V							
	Output Load:	1 TTL Load + 100 pF							
	Input Rise and Fall Times:	20 ns							
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C							
		Industrial (I): Tamb = -40°C to +85°C							
Parameter	**Symbol**	**28C64A-15**		**28C64A-20**		**28C64A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	(Note 1)
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0	—	0	—	0	—	ns	(Note 1)
Endurance	—	1M	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: Not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first

(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}

(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise/Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	10	—	ns	
Address Hold Time	tAH	50	—	ns	
Data Set-Up Time	tDS	50	—	ns	
Data Hold Time	tDH	10	—	ns	
Write Pulse Width	tWPL	100	—	ns	Note 1
Write Pulse High Time	tWPH	50	—	ns	
$\overline{OE}$ Hold Time	tOEH	10	—	ns	
$\overline{OE}$ Set-Up Time	tOES	10	—	ns	
Data Valid Time	tDV	—	1000	ns	Note 2
Time to Device Busy	tDB	2	50	ns	
Write Cycle Time (28C64A)	tWC	—	1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	tWC	—	200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge $\overline{WE}$, whichever occurs first.

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until tDH after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

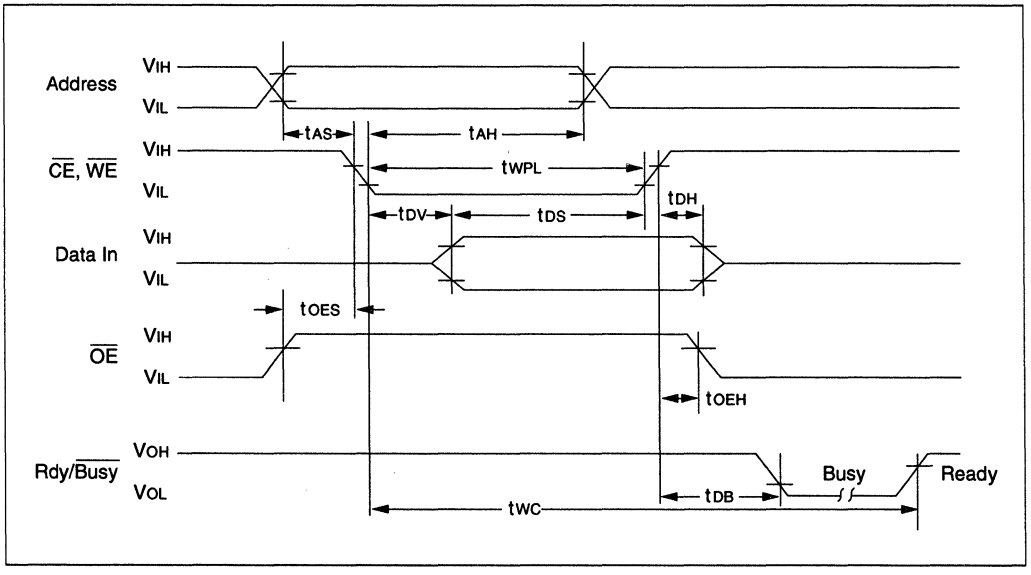


FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

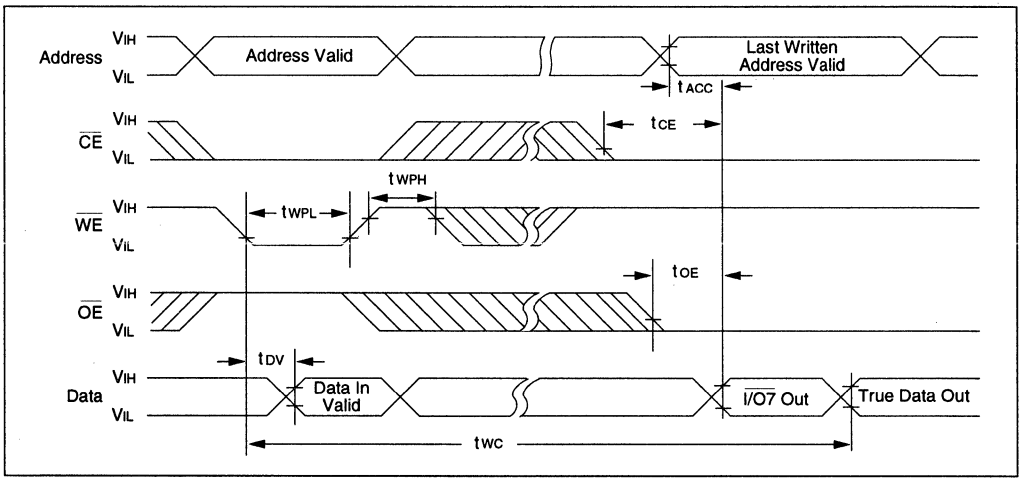


FIGURE 1-4: CHIP CLEAR WAVEFORMS

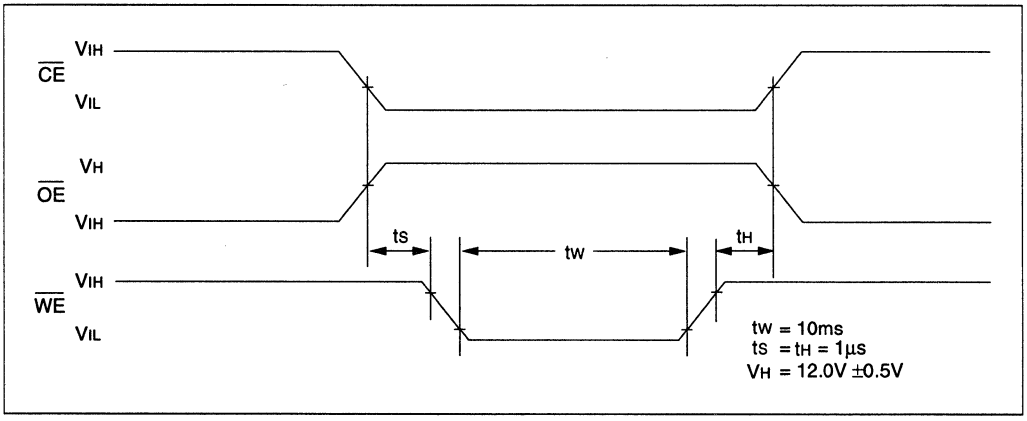


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VIH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V±0.5V. *Pulsed per programming waveforms.

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$ (1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note 1: Open drain output.
2: X = Any TTL level.

2.1 Read Mode

The 28C64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

2.2 Standby Mode

The 28C64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

2.4 Write Mode

The 28C64A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64A has completed writing and is ready to accept another cycle.

2.5 $\overline{Data}$ Polling

The 28C64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FEO to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

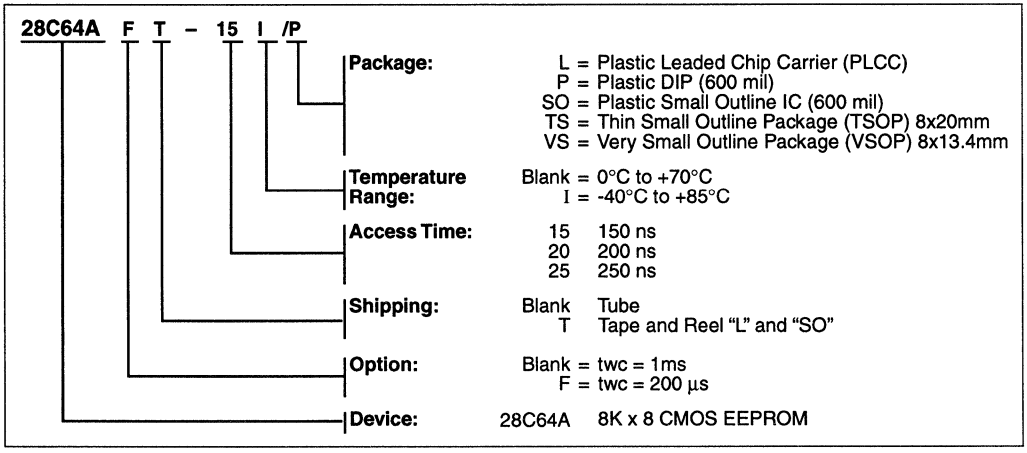
2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

28C64A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



28LV64A

64K (8K x 8) Low Voltage CMOS EEPROM

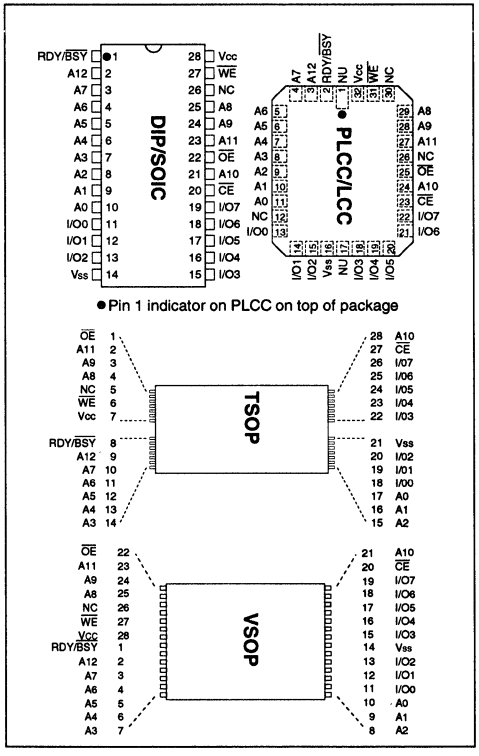
FEATURES

- 2.7V to 3.6V Supply
- Read Access Time—300 ns
- CMOS Technology for Low Power Dissipation
  - 8 mA Active
  - 50 µA CMOS Standby Current
- Byte Write Time—3 ms
- Data Retention >200 years
- High Endurance - Minimum 100,000 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Ready/$\overline{\text{Busy}}$
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- Organized 8Kx8 JEDEC Standard Pinout
  - 28-pin Dual-In-Line Package
  - 32-pin Chip Carrier (Leadless or Plastic)
  - 28-pin Thin Small Outline Package (TSOP) 8x20mm
  - 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

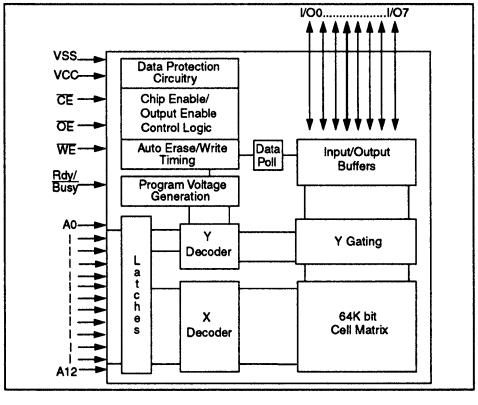
The Microchip Technology Inc. 28LV64A is a CMOS 64K non-volatile electrically Erasable PROM organized as 8K words by 8 bits. The 28LV64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/$\overline{\text{Busy}}$ output or using $\overline{\text{Data}}$ polling. The Ready/$\overline{\text{Busy}}$ pin is an open drain output, which allows easy configuration in 'wired-or' systems. Alternatively, $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES



● Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



7

Parallel EEPROM

1.0 ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

VCC and input voltages w.r.t. Vss .....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V

Voltage on A9 w.r.t. Vss.....-0.6V to +13.5V

Output Voltage w.r.t. Vss.....-0.6V to VCC+0.6V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied.....-55°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUCTION TABLE

Name	Function
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
Vcc	+ Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

Vcc = 2.7 to 3.6V
Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "2"	VIH VIL	2.0	 0.6	V V	
Input Leakage	—	ILI	—	5	µA	VIN = 0V to VCC+1
Input Capacitance	—	CIN	—	6	pF	Vin = 0V; Tamb = 25°C; f = 1 MHz (Note 1)
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.0	 0.3	V V	IOH = -100µA IOL = 1.0 mA IOL = 2.0 mA for RDY/$\overline{Busy}$
Output Leakage	—	ILO	—	5	µA	VOUT = 0V to VCC+0.1V
Output Capacitance	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz (Note 1)
Power Supply Current, Activity	TTL input	ICC	—	8	mA	f = 5 MHz (Note 2) IO = OmA VCC = 3.3 $\overline{CE}$ = VIL
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to 70°C°) $\overline{CE}$ = VIH (-40°C to 85°C°) $\overline{CE}$ = VCC -3.0 to VCC+1 $\overline{OE}$ = $\overline{WE}$ = VCC All other inputs equal VCC or VSS

Note 1: Not 100% tested.
2: AC power supply current above 5 MHz: 2 mA/Mhz.

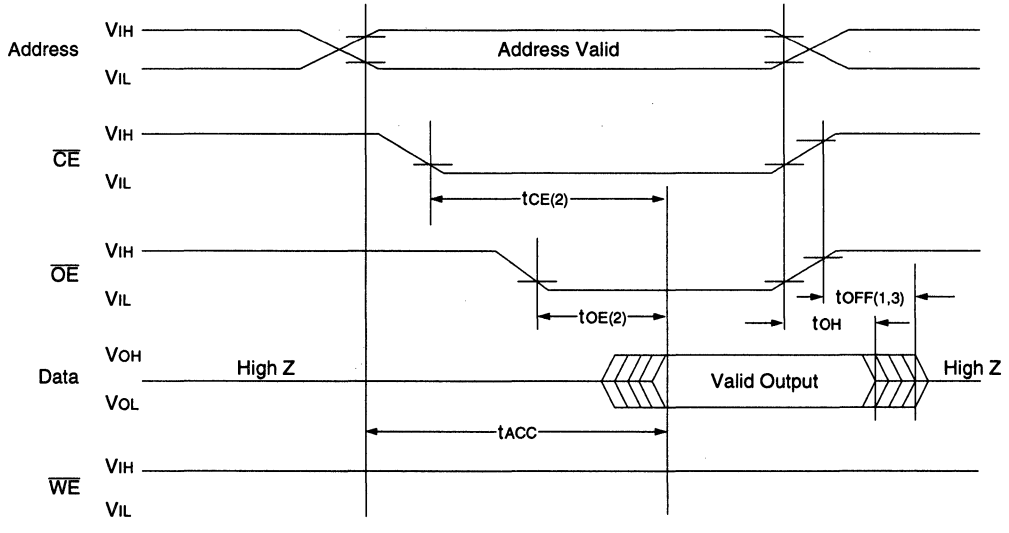
TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.0V; V_{IL} = 0.6V; V_{OH} = V_{OL} = V_{CC}/2			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise and Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C Industrial (I) : Tamb = -40°C to +85°C			
Parameter	**Sym**	**28LV64-30**		**Units**	**Conditions**
		Min	**Max**		
Address to Output Delay	tACC	—	300	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	150	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	tOFF	0	60	ns	(Note 1)
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	tOH	0	—	ns	(Note 1)
Endurance	—	10M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: Not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first

(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE

(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.0V; V_{IL} = 0.6V; V_{OH} = V_{OL} = V_{CC}/2			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise/Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C Industrial (I) : Tamb = -40°C to +85°C			
Parameter	**Sym**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	100		ns	
Data Set-Up Time	t_{DS}	120		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	150		ns	(Note 1)
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	(Note 2)
Time to Device Busy	t_{DB}		50	ns	
Write Cycle Time (28LV64A)	t_{WC}		3	ms	1.5 ms typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

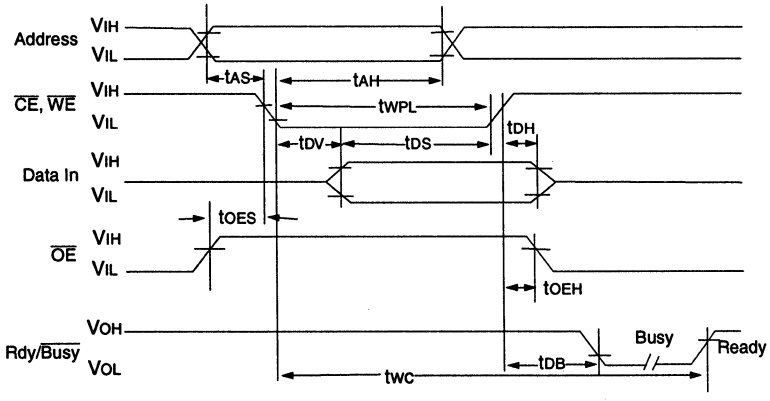


FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

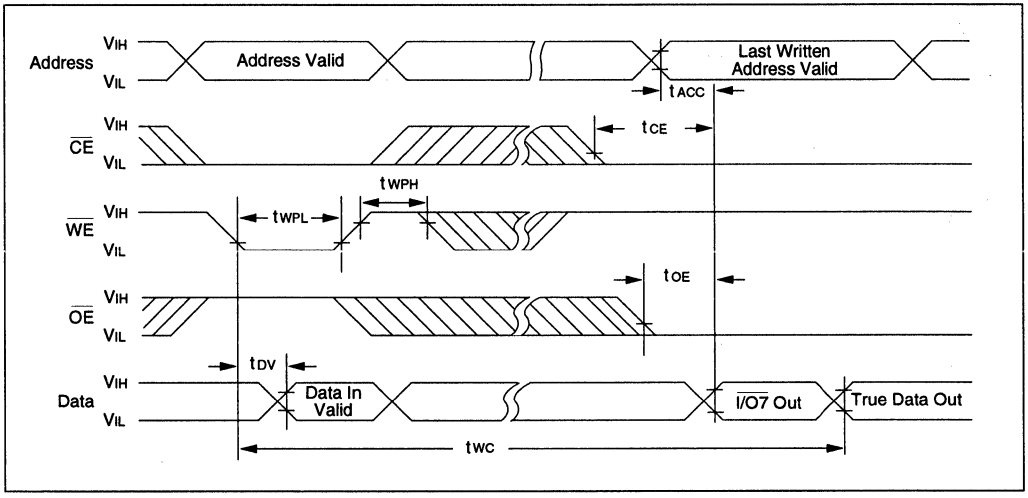


FIGURE 1-4: CHIP CLEAR WAVEFORMS

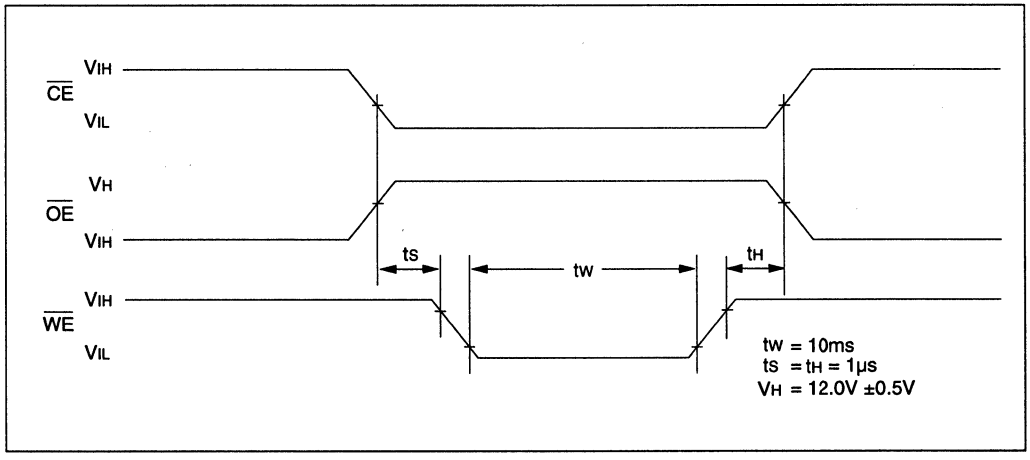


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	AI	VCC	I/OI
Chip Clear	VIL	VH		X	VCC	
Extra Row Read	VIL	VIL	VIH	A9 = VH	VCC	Data Out
Extra Row Write		VIH		A9 = VH	VCC	Data In
Note: VH = 12.0V ± 0.5V						

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28LV64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.

2.1 Read Mode

The 28LV64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (t$\overline{CE}$). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

2.2 Standby Mode

The 28LV64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (2.0 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

2.4 Write Mode

The 28LV64A has a write cycle similar to that of a static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28LV64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28LV64A has completed writing and is ready to accept another cycle.

2.5 $\overline{Data}$ Polling

The 28LV64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 can not be determined). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FE0 to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

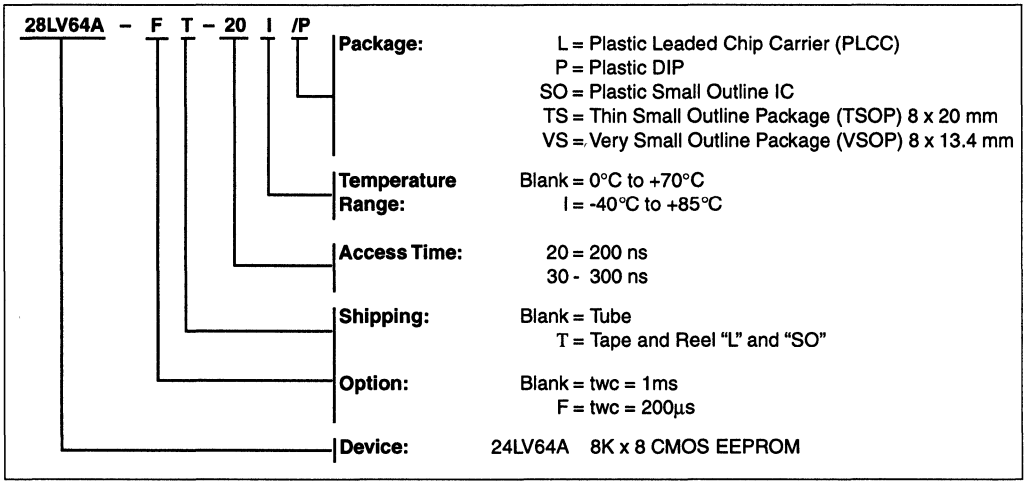
2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and CE low. This procedure clears all data, except for the extra row.

NOTES:

28LV64A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

SECTION 8
EPROM PRODUCT SPECIFICATIONS

27C64	64K (8K x 8) CMOS EPROM	8-1
27LV64	64K (8K x 8) Low-Voltage CMOS EPROM	8-9
27C128	128K (16K x 8) CMOS EPROM	8-17
27C256	256K (32K x 8) CMOS EPROM	8-25
27LV256	256K (32K x 8) Low-Voltage CMOS EPROM	8-33
27C512A	512K (64K x 8) CMOS EPROM	8-41
37LV36/65/128	36K, 64K, and 128K Serial EPROM Family	8-49
Memory Products	EPROM Programming Guide	8-61

MICROCHIP

27C64

64K (8K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 120 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - Tape and reel
- Available for the following temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

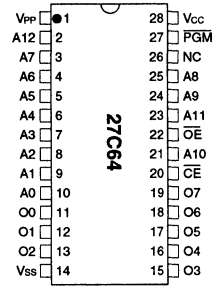
DESCRIPTION

The Microchip Technology Inc. 27C64 is a CMOS 64K bit (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

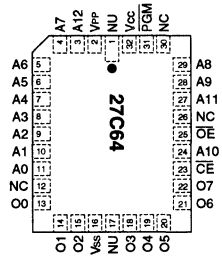
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

DIP/SOIC



PLCC



8

EPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V

VPP voltage w.r.t. VSS during programming .....-0.6V to +14V

Voltage on A9 w.r.t. VSS.....-0.6V to +13.5V

Output voltage w.r.t. VSS.....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied.....-65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S) — —	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V

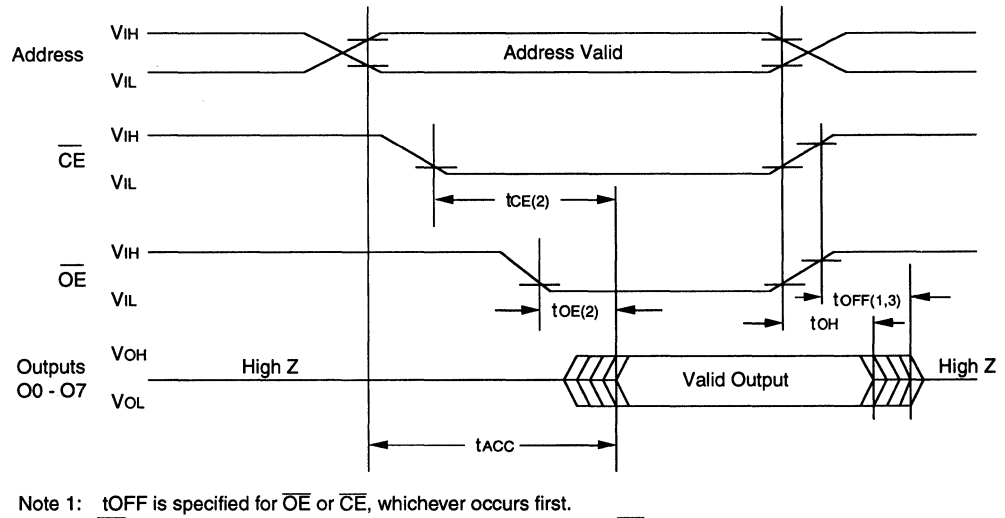
* Parts: C=Commercial Temperature Range; I =Industrial Temperature Range.

Note 1: Typical active current increases .5 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C													
Parameter	**Sym**	**27C64-12**		**27C64-15**		**27C64-17**		**27C64-20**		**27C64-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Note 1: tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
2: $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE.
3: This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4 —	— 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

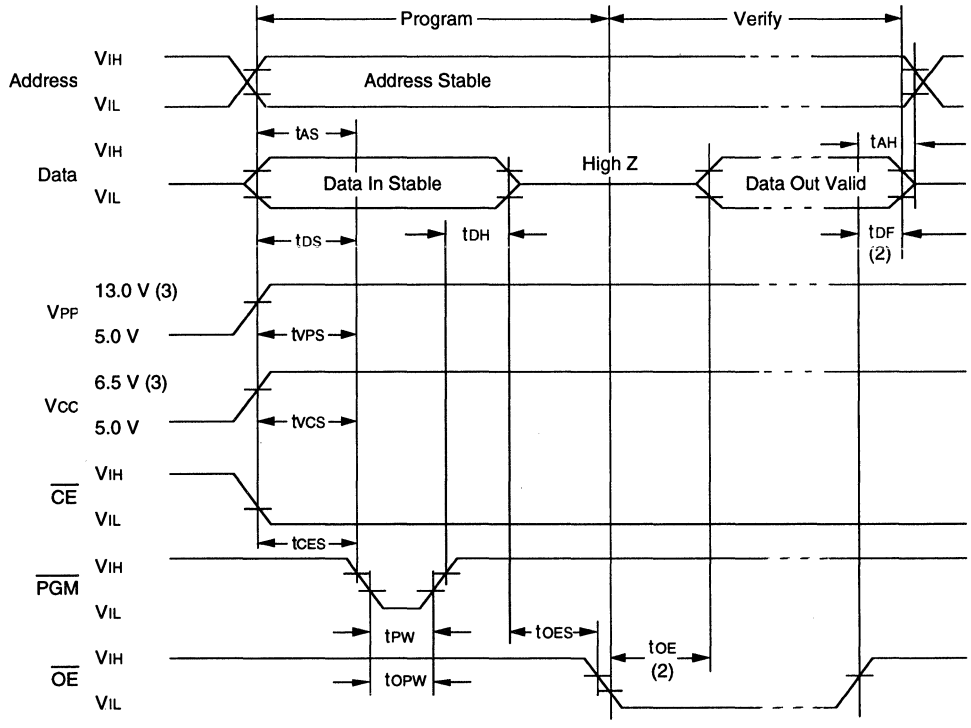
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: Tamb=25°C ±5°C VCC= 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8 V for VIL and 2.0 V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.5 V ±0.25 V, VPP = VH = 13.0 V ±0.25 V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

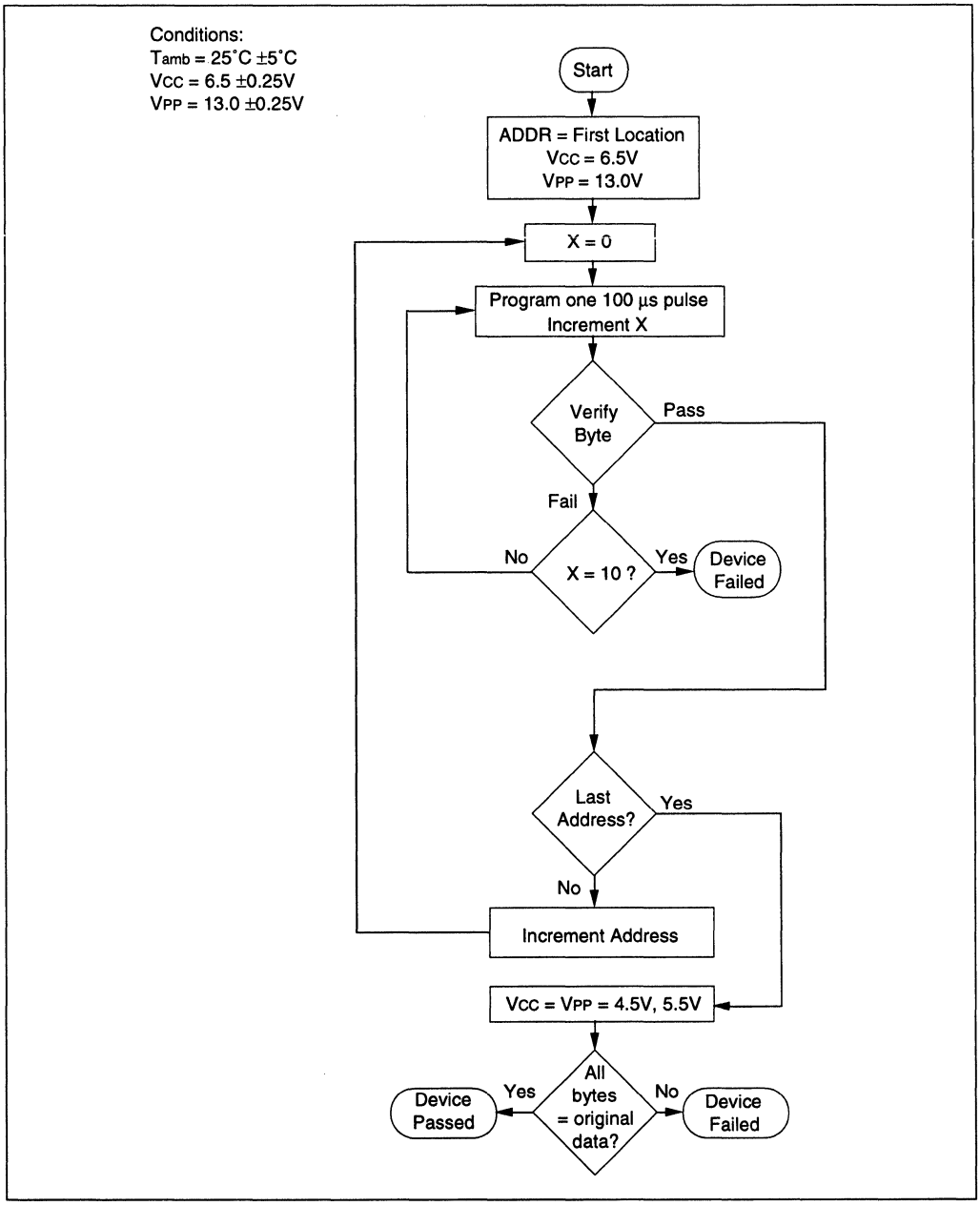
1.9 Identity Mode

In this mode, specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	0	0	1	0	02

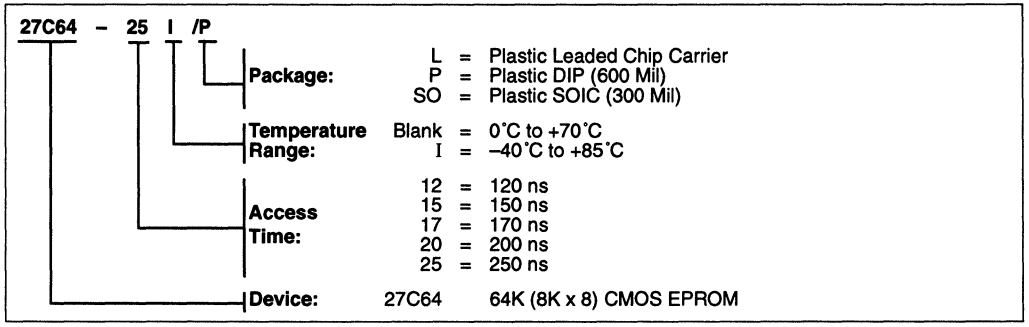
* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C64 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

27LV64

64K (8K x 8) Low-Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  - 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - 8 mA active current at 3.0V
  - 20 mA active current at 5.5V
  - 100 µA standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

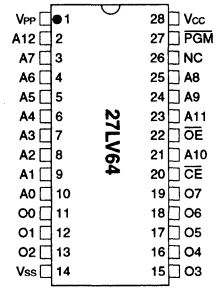
DESCRIPTION

The Microchip Technology Inc. 27LV64 is a low-voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as 8K x 8 (8K-Byte) non-volatile memory product. The 27LV64 consumes only 8mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMs can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0V.This device allows system designers the ability to use low voltage non-volatile memory with today's low voltage microprocessors and peripherals in battery powered applications.

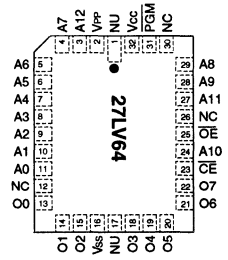
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

DIP/SOIC



PLCC



8

EPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to + 7.25V

VPP voltage w.r.t. VSS during programming .....-0.6V to +14V

Voltage on A9 w.r.t. VSS.....-0.6V to +13.5V

Output voltage w.r.t. VSS.....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied.....-65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = 3.0V to 5.5V unless otherwise specified
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)	—	1 @ 3.0V 2@ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V

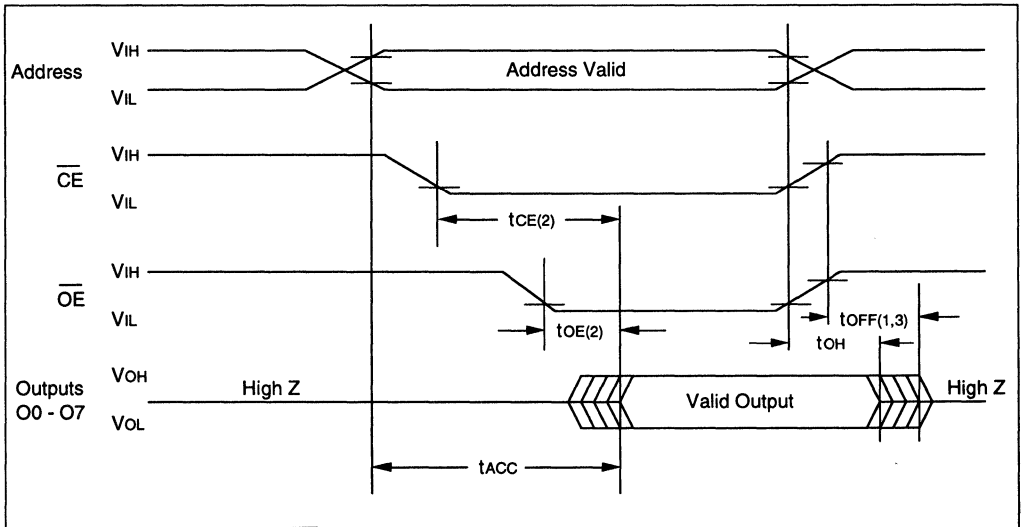
* Parts: C=Commercial Temperature Range; I=Industrial Temperature Range

Note 1: Typical active current increases .5 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C									
Parameter	**Sym**	**27LV64-20**		**27LV64-25**		**27LV64-30**		**Units**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	100	—	125	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

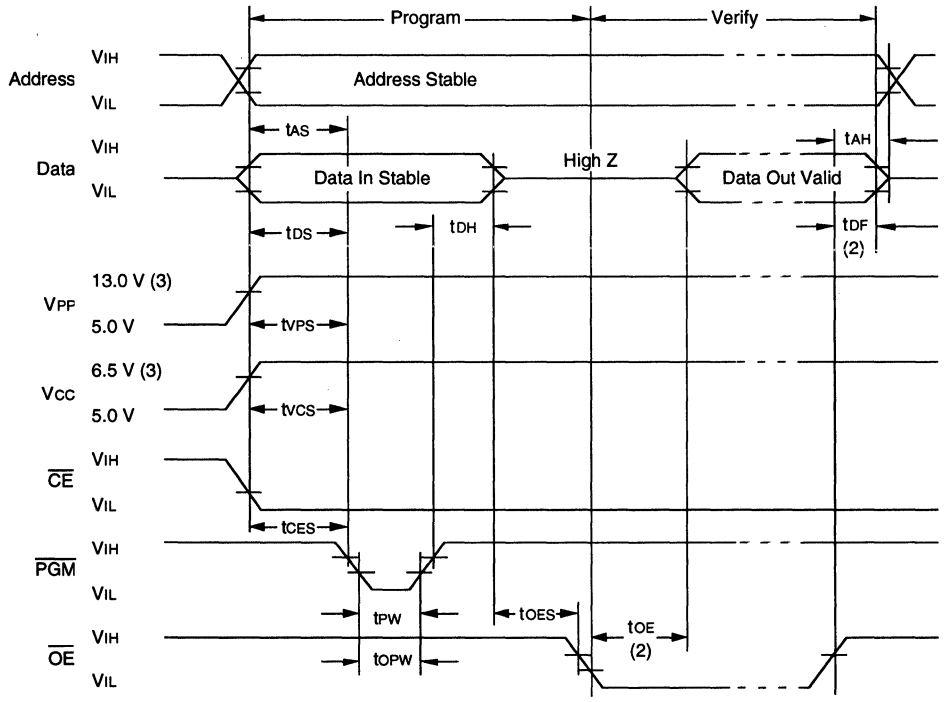
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: Tamb=25°C ± 5°C VCC= 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE		100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) V_{CC} is brought to the proper voltage,
b) V_{PP} is brought to the proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

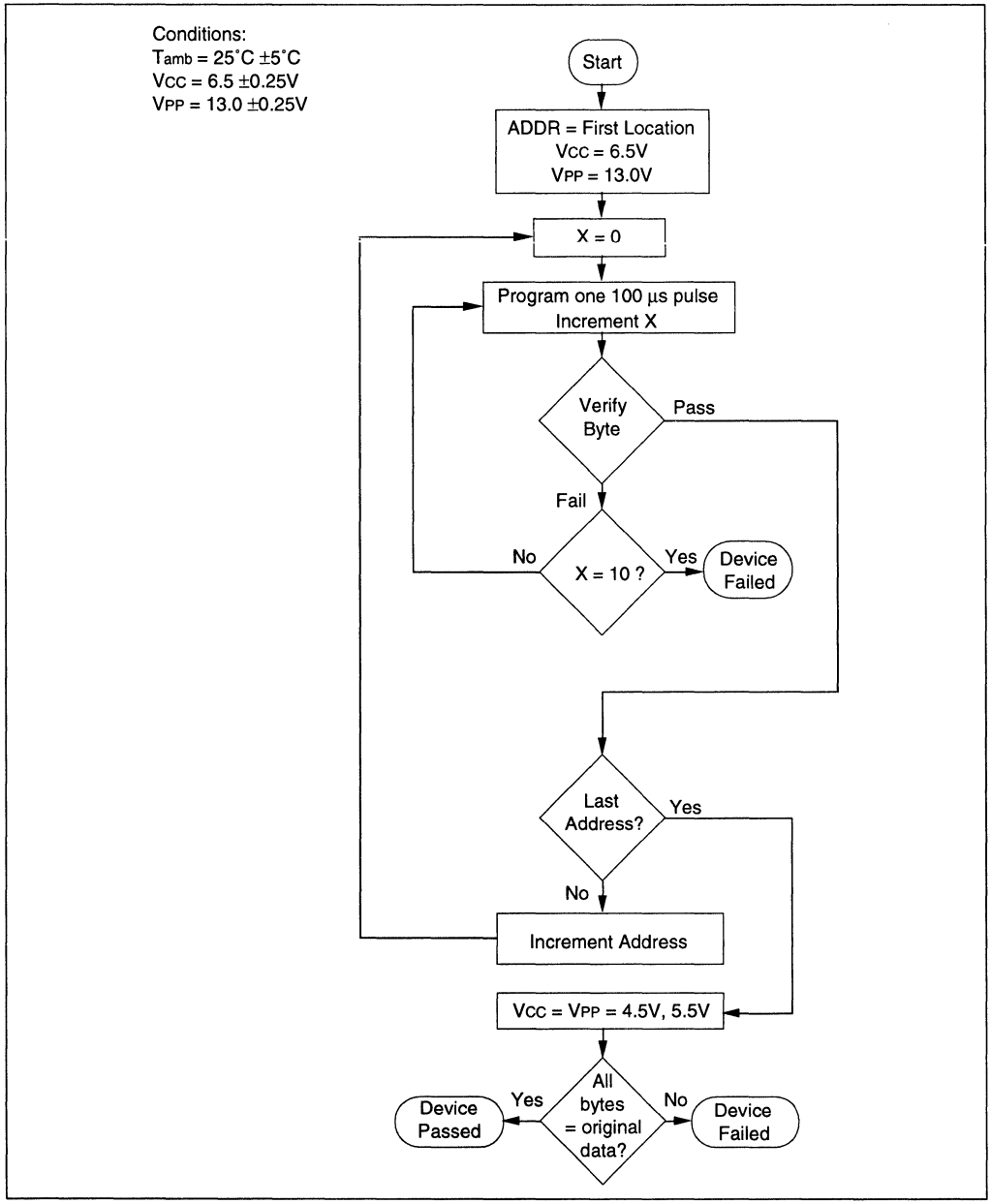
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin → / Identity ↓	Input	Output								
	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	0	1	0	02

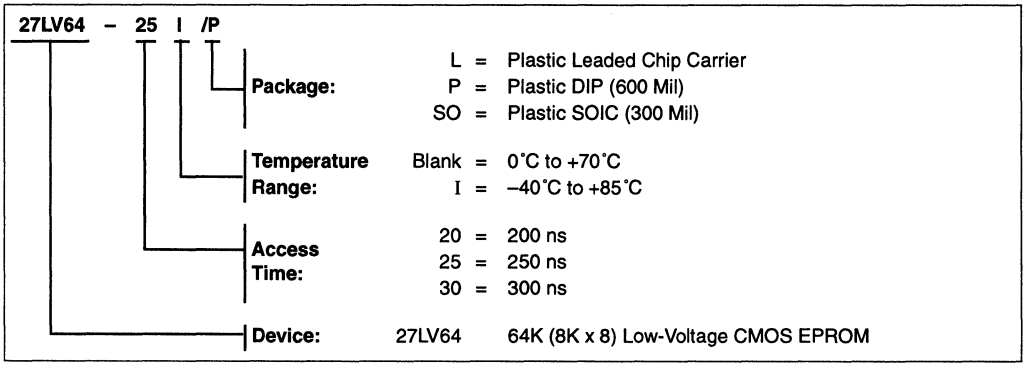
* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27LV64 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

27C128

128K (16K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 120 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

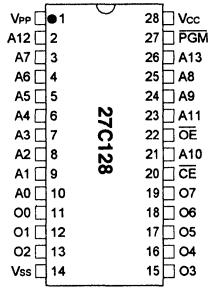
DESCRIPTION

The Microchip Technology Inc. 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

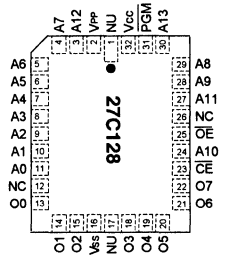
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

DIP/SOIC



PLCC



8

EPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

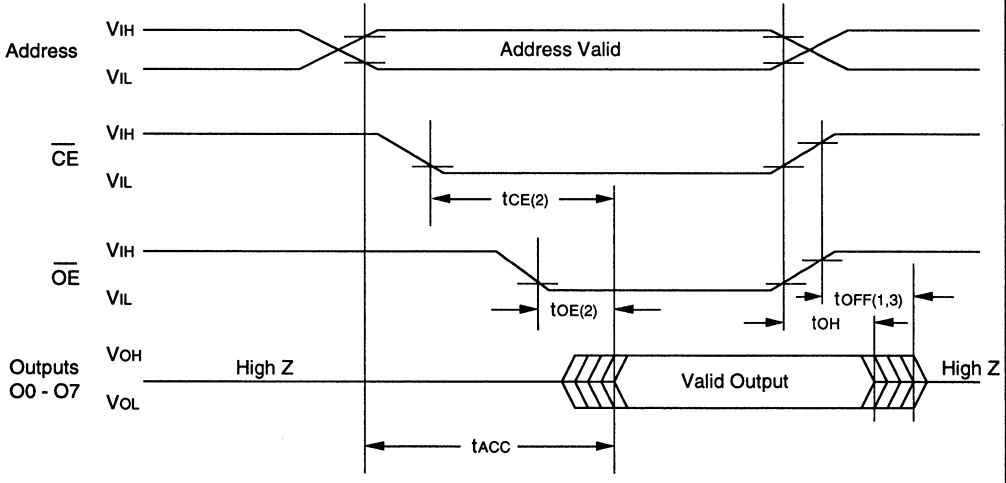
Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise and Fall Times:	10 ns	
Ambient Temperature:	Commercial:	Tamb = 0°C to +70°C
	Industrial:	Tamb = -40°C to +85°C
	Extended (Automotive):	Tamb = -40°C to +125°C

Parameter	Sym	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$=V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$=V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic"1" Logic"0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

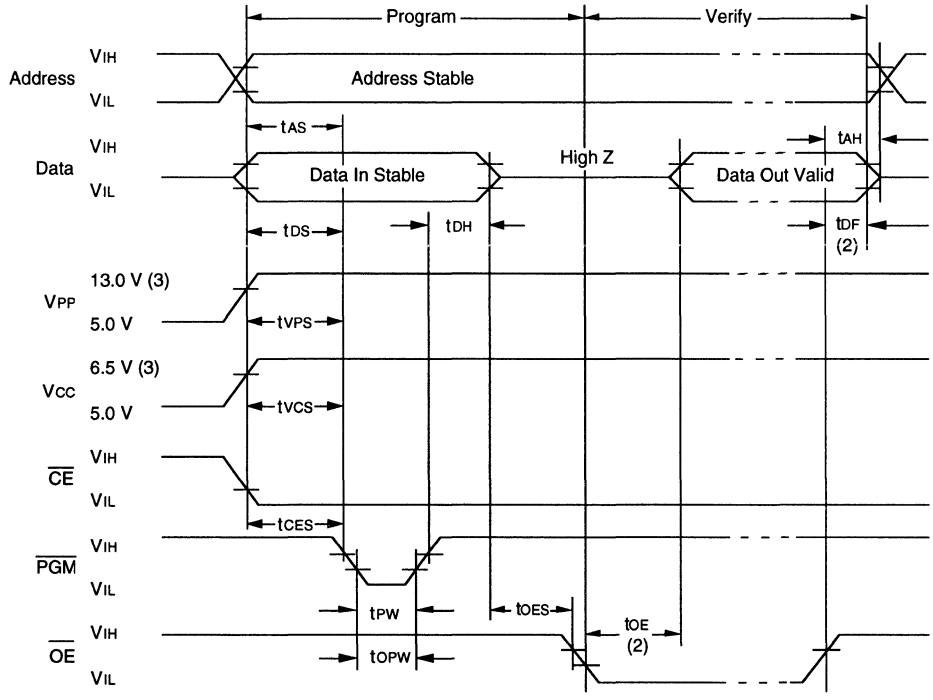
Note 1: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH}=2.4V and V_{IL}=0.45V; V_{OH}=2.0V; V_{OL}=0.8V Ambient Temperature: Tamb=25°C± 5°C V_{CC}= 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8V for VIL and 2.0V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) Vcc = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	Vcc	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	Vcc	X	High Z
Output Disable	VIL	VIH	VIH	Vcc	X	High Z
Identity	VIL	VIL	VIH	Vcc	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

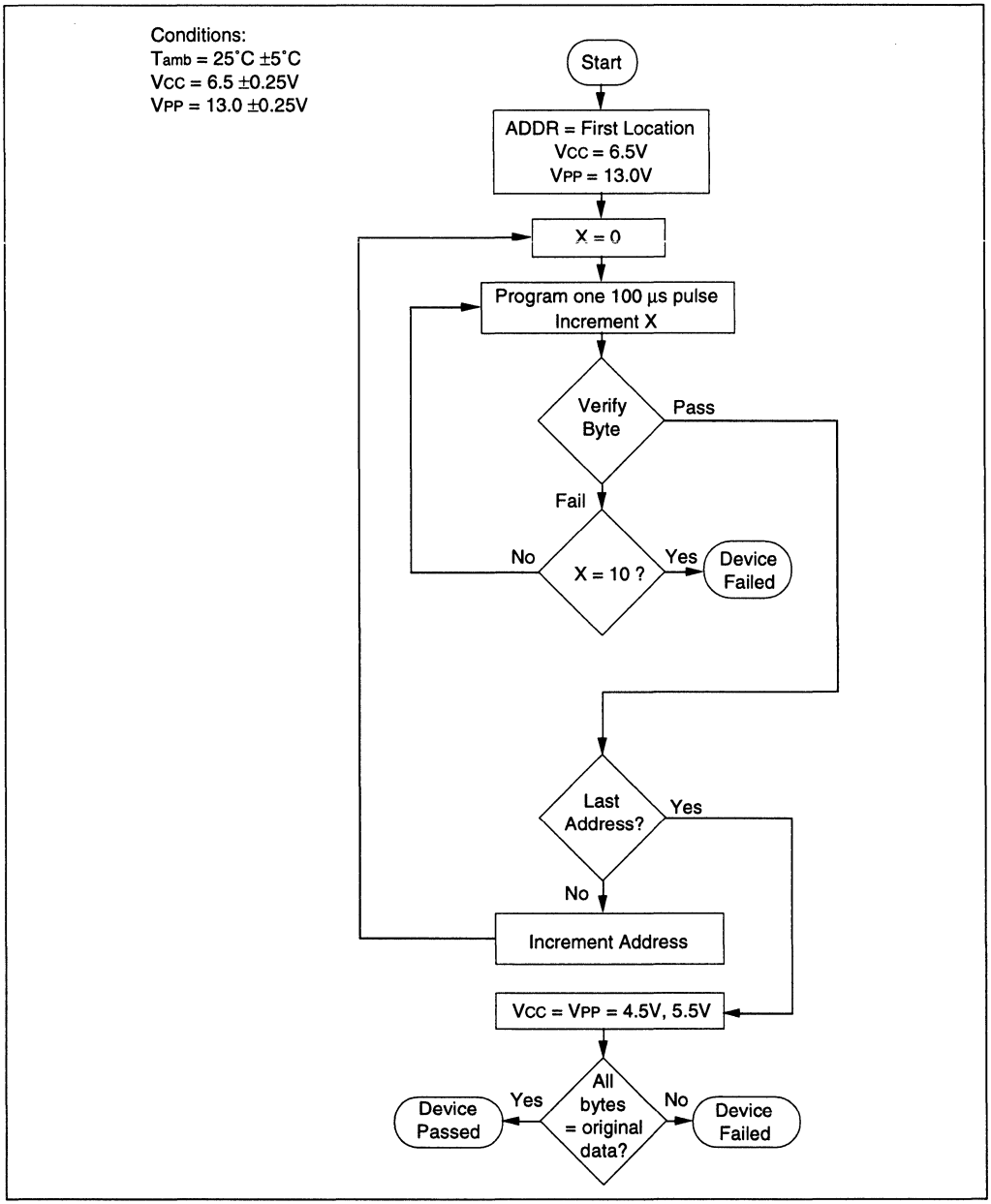
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	0	0	1	1	83

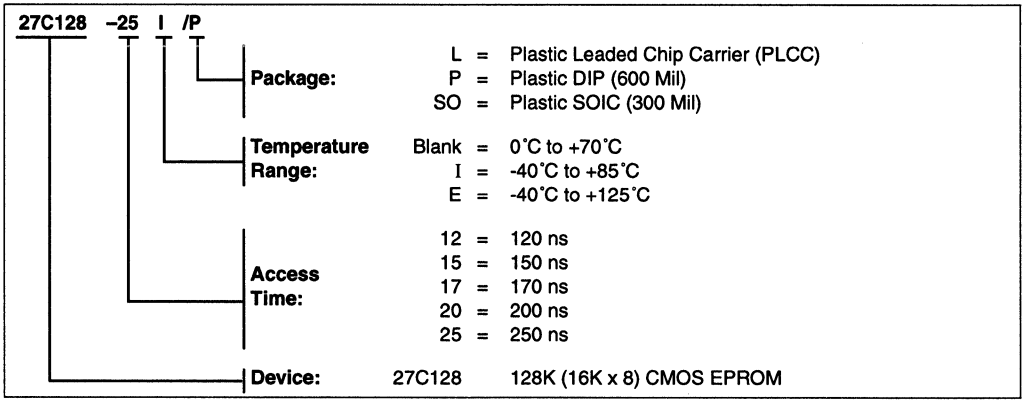
* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



27C256

256K (32K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 90 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - 28-pin Thin Small Outline Package (TSOP)
  - 28-pin Very Small Outline Package (VSOP)
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

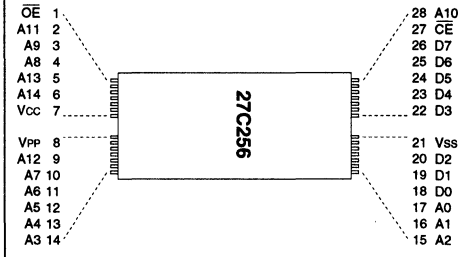
DESCRIPTION

The Microchip Technology Inc. 27C256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

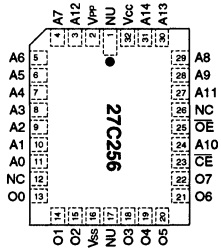
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, VSOP or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

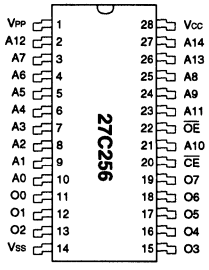
TSOP



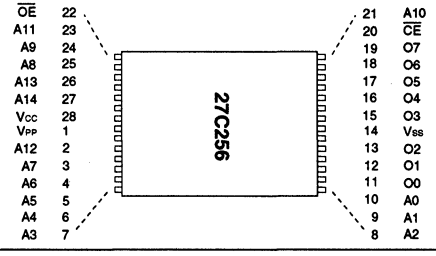
PLCC



DIP/SOIC



VSOP



8

EPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V

VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V

Voltage on A9 w.r.t. VSS.....-0.6V to +13.5V

Output voltage w.r.t. VSS.....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied.....-65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)	—	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

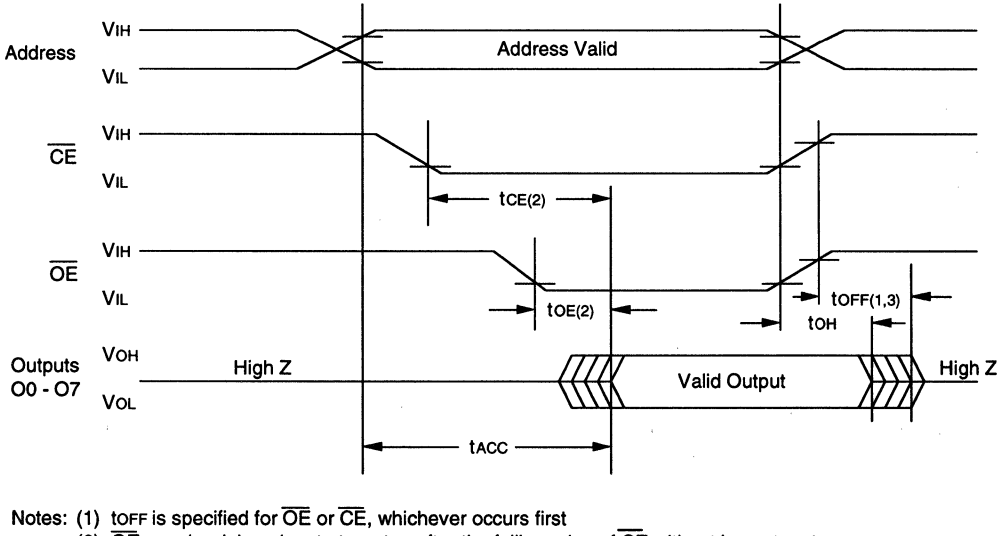
Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Automotive: Tamb = -40°C to +125°C													
Parameter	**Sym**	**27C256-90***		**27C256-10***		**27C256-12**		**27C256-15**		**27C256-20**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}$=$\overline{OE}$ =V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

* -10, -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30pF

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V						
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

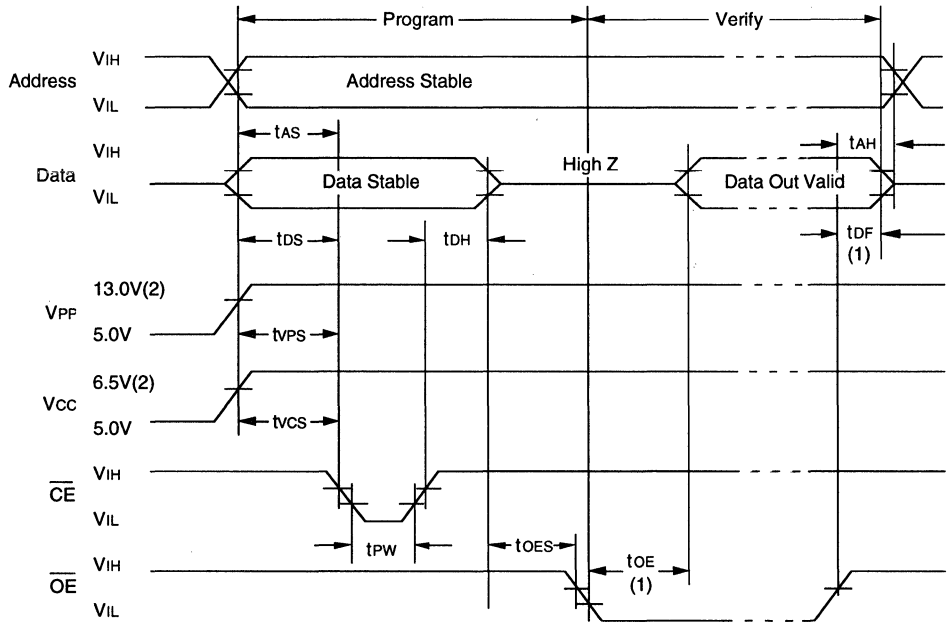
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Output Load: 1 TTL Load + 100pF Ambient Temperature: Tamb=25°C ± 5°C VCC= 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	OE	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when:

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and the program mode is not defined.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{OE}$ pin is high, and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is high, and
d) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

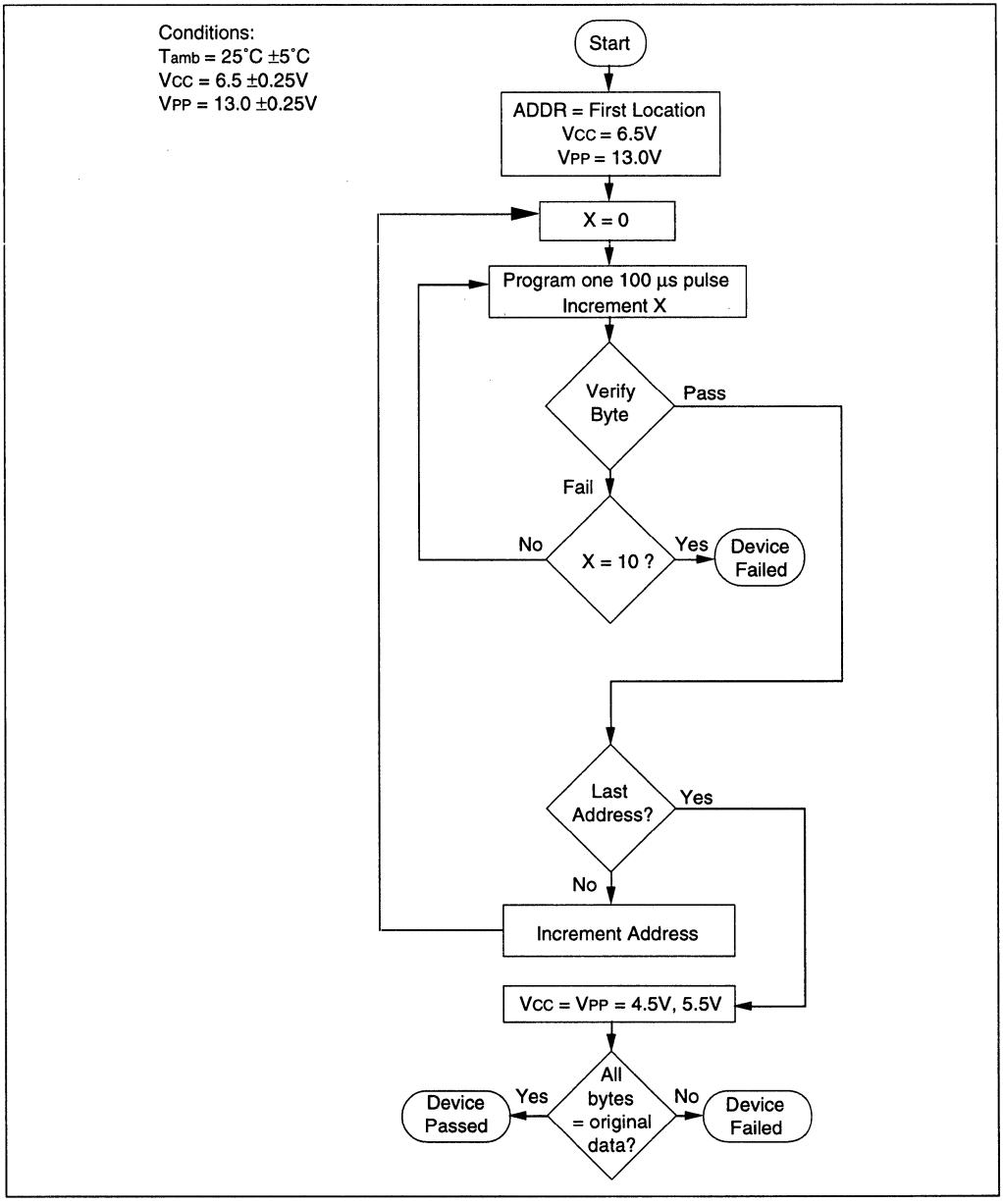
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	8C

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C256 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use listed part numbers, and refer to factory or listed sales offices.

27C256 – 90 I /TS

Package:	L	=	Plastic Leaded Chip Carrier
	P	=	Plastic DIP (Mil 600)
	SO	=	Plastic SOIC (Mil 300)
	TS	=	Thin Small Outline Package (TSOP) 8x20mm
	VS	=	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Access Time:	90	=	90 ns
	10	=	100 ns
	12	=	120 ns
	15	=	150 ns
	20	=	200 ns
Device	27C256		256K (32K x 8) CMOS EPROM

MICROCHIP

27LV256

256K (32K x 8) Low-Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  - 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - 8 mA Active current at 3.0V
  - 20 mA Active current at 5.5V
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC package
  - 28-pin SOIC package
  - 28-pin VSOP package
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

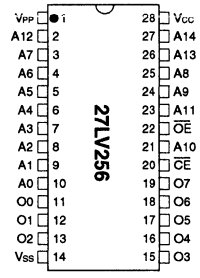
DESCRIPTION

The Microchip Technology Inc. 27LV256 is a low voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 32K x 8 (32K-Byte) non-volatile memory product. The 27LV256 consumes only 8 mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMS can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0V. This device allows systems designers the ability to use low voltage non-volatile memory with today's' low voltage microprocessors and peripherals in battery powered applications.

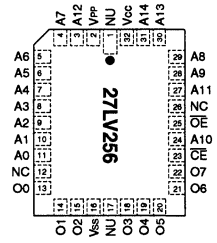
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, VSOP or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

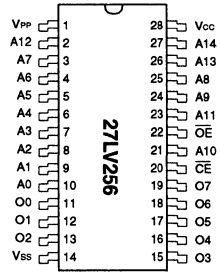
PDIP



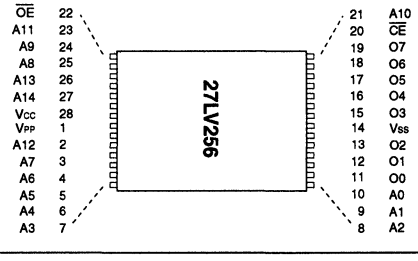
PLCC



SOIC



VSOP



8

EPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V ±10% or 3.0V where indicated
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)	—	1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$=VCC ± 0.2V

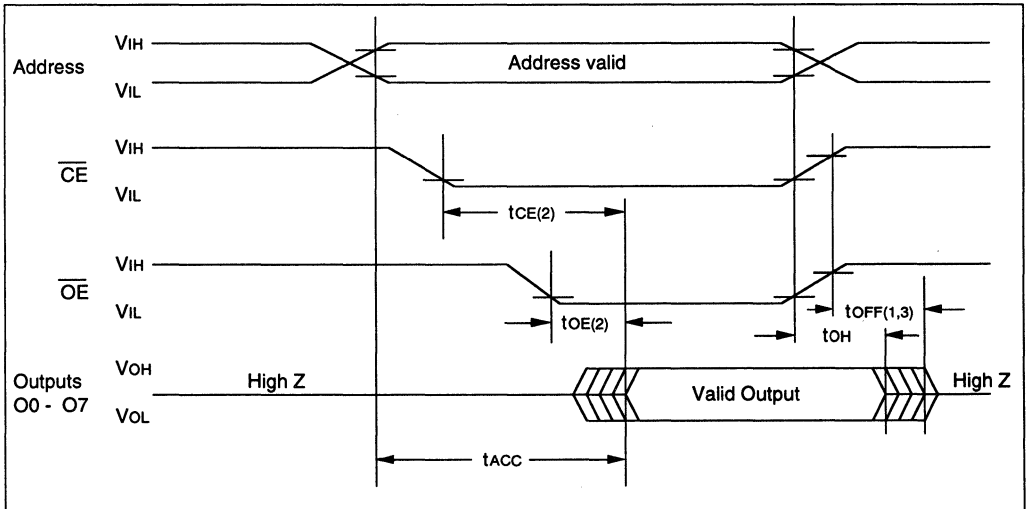
* Parts: C=Commercial Temperature Range
I =Industrial Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C									
Parameter	**Sym**	**27HC256-20**		**27HC256-25**		**27HC256-30**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	100	—	125	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

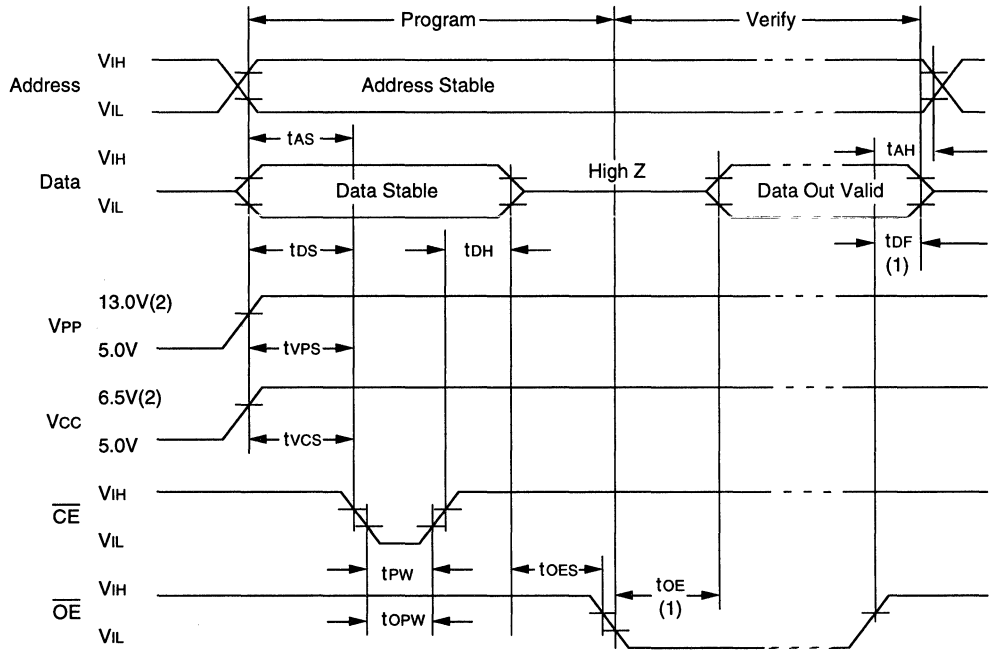
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Output Load: 1 TLL Load + 100pF Ambient Temperature: Tamb=25°C±5°C VCC= 6.5V ± 0.25V, VPP =13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when:

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined. Output Disable

1.4 Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and program mode is not defined.

1.5 Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No over-programming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to the proper voltage
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

1.6 Verify

After the array has been programmed it must be verified to ensure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

1.7 Inhibit

When Programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

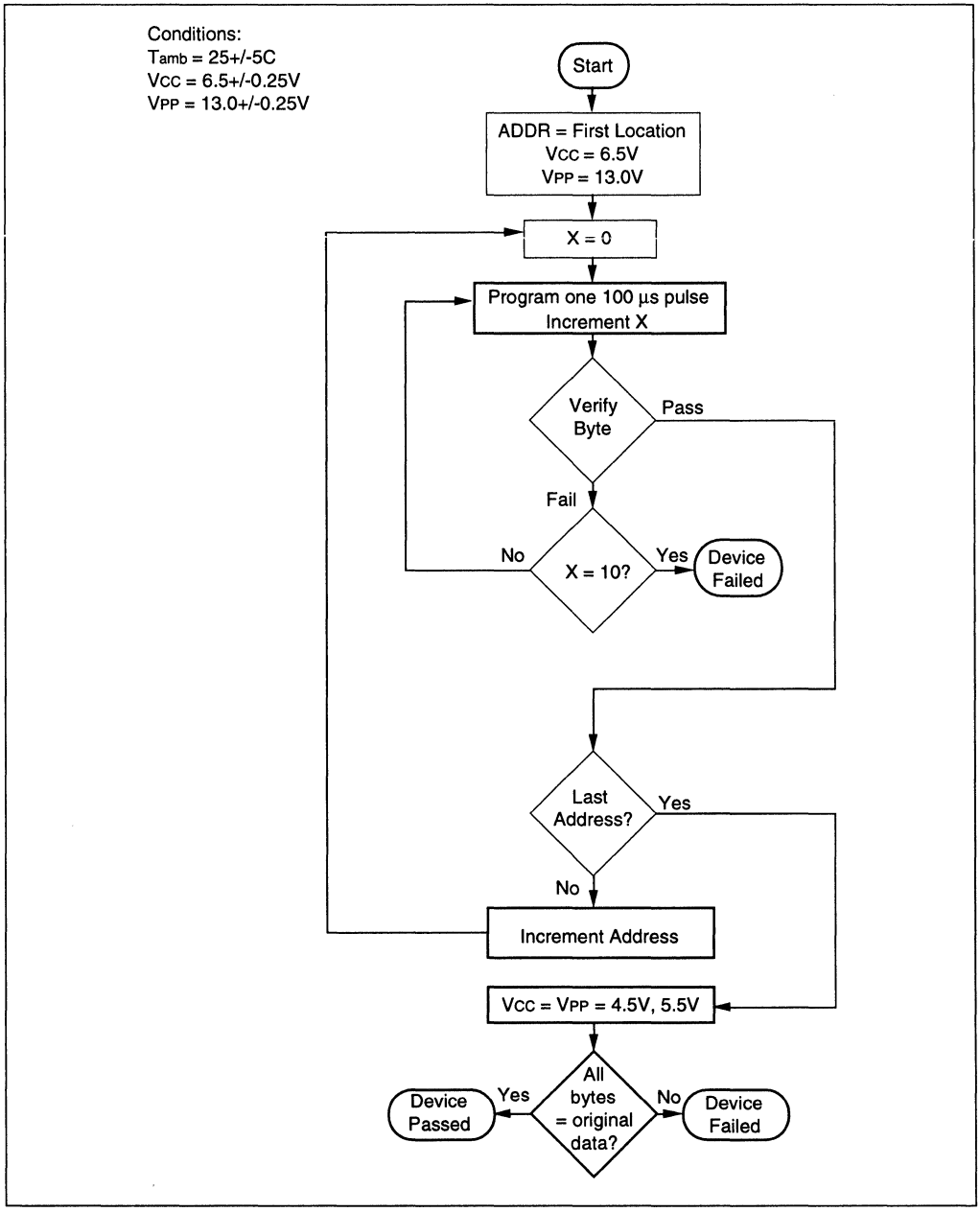
1.8 Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin	Input	Output								
Identity	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

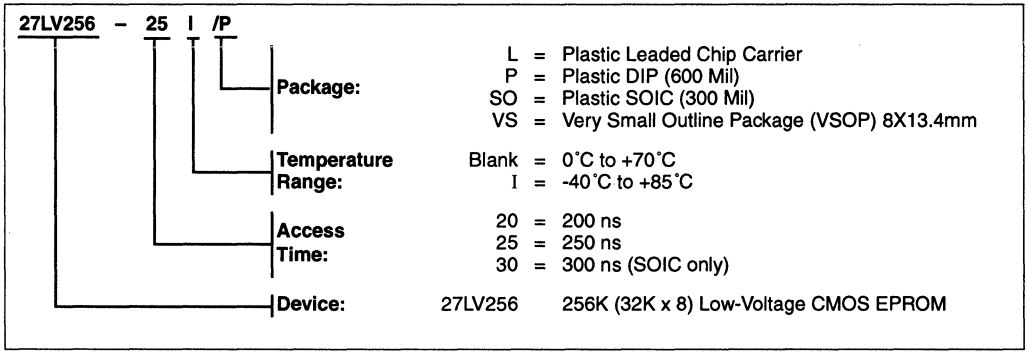
* Code subject to change.

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27LV256 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

27C512A

512K (64K x 8) CMOS EPROM

FEATURES

- High speed performance
- CMOS Technology for low power consumption
  - 25 mA Active current
  - 30 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- High speed express programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - 28-pin TSOP package
  - 28-pin VSOP package
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

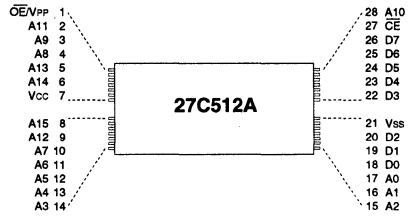
DESCRIPTION

The Microchip Technology Inc. 27C512A is a CMOS 512K bit electrically Programmable Read Only Memory (EPROM). The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

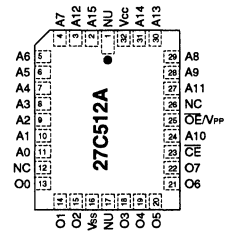
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, VSOP, TSOP or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

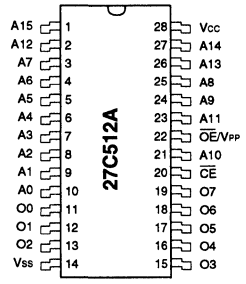
TSOP



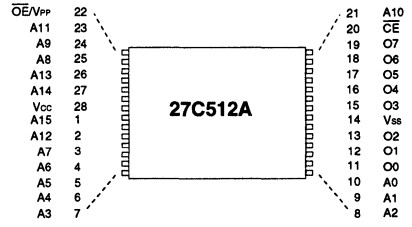
PLCC



DIP/SOIC



VSOP



8

EPROM

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V ±10%
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	ICC ICC	— —	25 35	mA mA	VCC = 5.5V f = 1 MHz; $\overline{OE}$/VPP = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	— — —	1 2 30	mA mA µA	 $\overline{CE}$ = VCC±0.2V

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

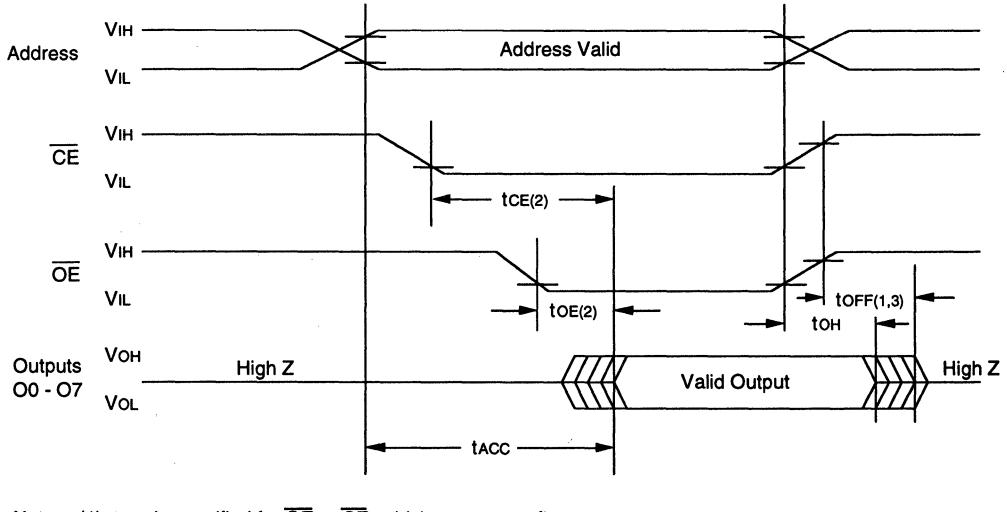
Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V and V_{OL} = 0.8V									
	Output Load:	1 TTL Load + 100 pF									
	Input Rise and Fall Times:	10 ns									
	Ambient Temperature:	Commercial: Tamb = 0°C to +70°C									
		Industrial: Tamb = -40°C to +85°C									
		Extended (Automotive): Tamb = -40°C to +125°C									
Parameter	**Sym**	**27C512-90***		**27C512-10***		**27C512-12**		**27C512-15**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}	—	90	—	100	—	120	—	150	ns	$\overline{CE}$ = $\overline{OE}$/V_{PP} = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	90	—	100	—	120	—	150	ns	$\overline{OE}$/V_{PP} = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	40	—	40	—	50	—	60	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to Output High Impedance	t_{OFF}	0	35	0	35	0	40	0	45	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$/V_{PP}, whichever occurred first	t_{OH}	0	—	0	—	0	—	0	—	ns	

*90/10 AC Testing Waveforms: V_{IH} = 3.0V and V_{IL} = 0V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, $\overline{OE}$/VPP = VH = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions (See Note 1)**
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4 —	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	35	mA	$\overline{CE}$ = VIL
$\overline{OE}$/VPP Current, program	—	IPP2	—	25	mA	
A9 Product Identification	—	VID	11.5	12.5	V	

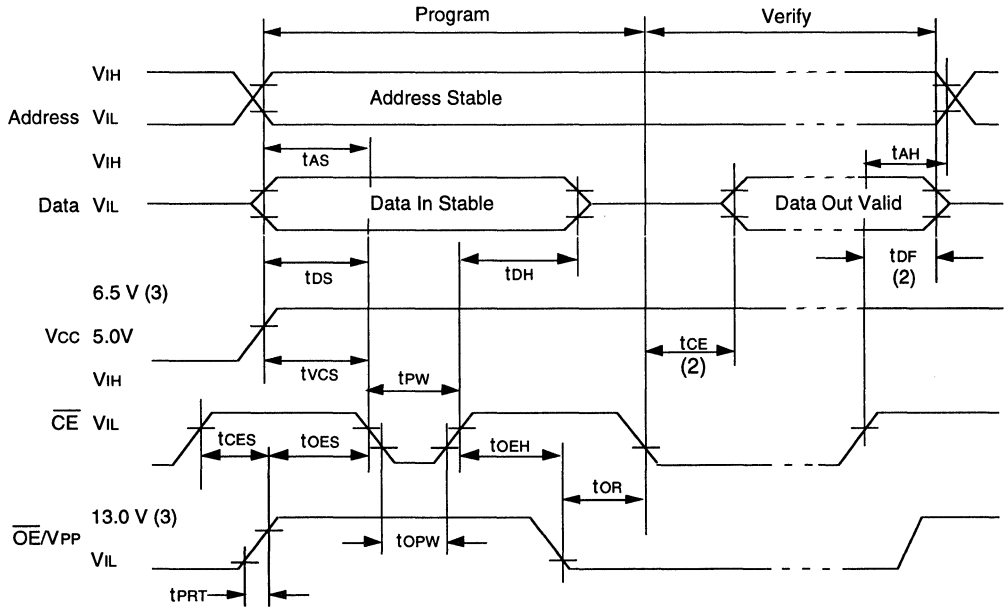
Note 1: VCC must be applied simultaneously or before VPP voltage on $\overline{OE}$/VPP and removed simultaneously or after the VPP voltage on $\overline{OE}$/VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: 25°C ±5°C VCC = 6.5V ± 0.25V, $\overline{OE}$/VPP = VH = 13.0V ± 0.25 V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
$\overline{OE}$ Hold Time	tOEH	2	—	µs	
$\overline{OE}$ Recovery Time	tOR	2	—	µs	
$\overline{OE}$ /VPP Rise Time During Programming	tPRT	50	—	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
2: This parameter is only sampled and not 100% teted. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.5V for express programming algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A9	O0 - O7
Read	V_{IL}	V_{IL}	X	D_{OUT}
Program	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	X	High Z
Output Disable	V_{IL}	V_{IH}	X	High Z
Identity	V_{IL}	V_{IL}	V_H	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the CE pin is low to power up (enable) the chip
b) the OE/V_{PP} pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}/V_{PP}$.

1.3 Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not identified.

When this conditions are met, the supply current will drop from 25 mA to 30 µA.

1.4 Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprocessor systems and the outputs go to high impedance when:

- the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

1.5 Erase Mode (UV Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1's" state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 mW/cm^2 for approximately 40 minutes.

1.6 Programming Mode

The Express algorithm must be used for best results. It has been developed to improve programming yields and throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

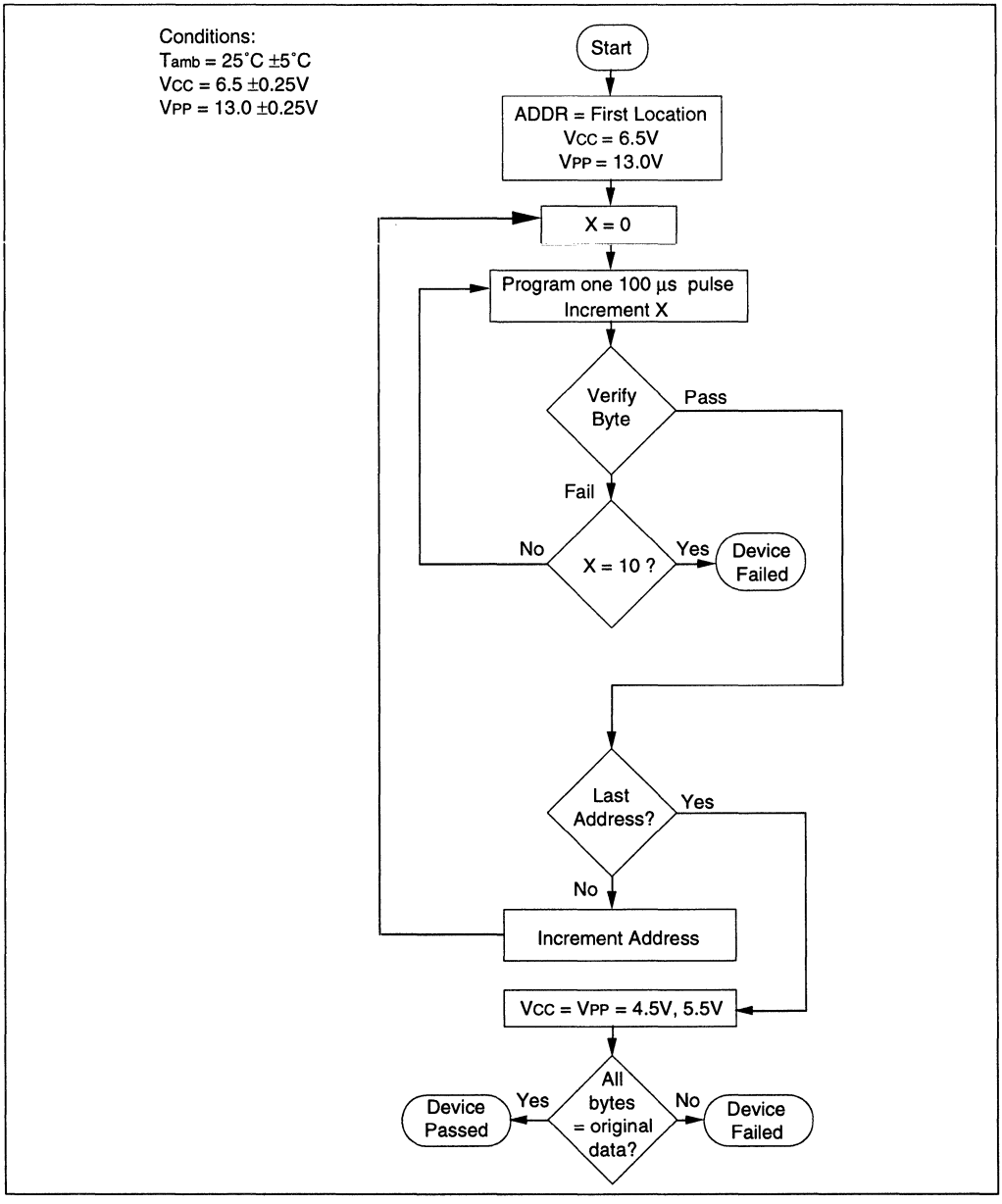
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	0D

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C512A Product Identification System

To order or to obtain information (e.g., on pricing or delivery),, please use listed part numbers, and refer to factory or listed sales offices.

27C512A – 70 I /P

Package:	L	=	Plastic Leaded Chip Carrier
	P	=	Plastic DIP (600 Mil)
	SO	=	Plastic SOIC (300 Mil)
	TS	=	Thin Small Outline Package(TSOP) 8x20mm
	VS	=	Very Small Outline Package(VSOP) 8x13.4mm
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Access Time:	90	=	90 ns
	10	=	100 ns
	12	=	120 ns
	15	=	150 ns
Device:	27C512A		512K (64K x 8) CMOS EPROM

37LV36/65/128

36K, 64K, and 128K Serial EPROM Family

FEATURES

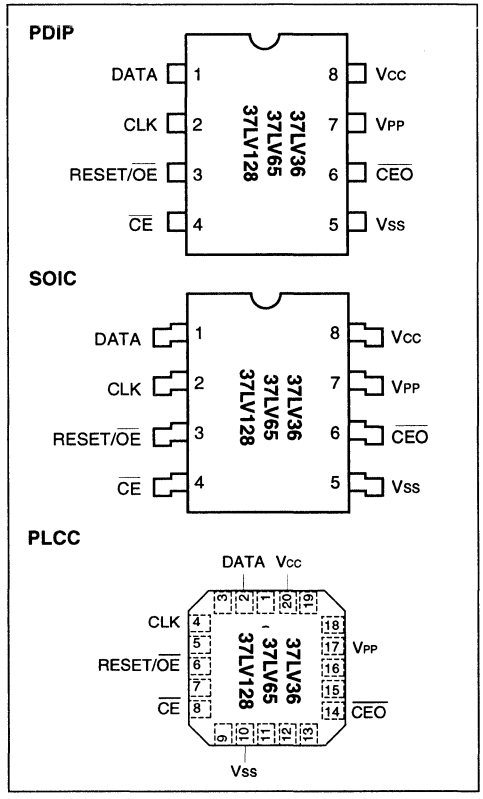
- Operationally equivalent to Xilinx® XC1700 family
- Wide voltage range 3.0 V to 6.0 V
- Maximum read current 10 mA at 5.0 V
- Standby current 100 µA typical
- Industry standard Synchronous Serial Interface/ 1 bit per rising edge of clock
- Full Static Operation
- Sequential Read/Program
- Cascadable Output Enable
- 10 MHz Maximum Clock Rate @ 5.0 Vdc
- Programmable Polarity on Hardware Reset
- Programming with industry standard EPROM programmers
- Electrostatic discharge protection > 4,000 volts
- 8-pin PDIP/SOIC and 20-pin PLCC packages
- Data Retention > 200 years
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

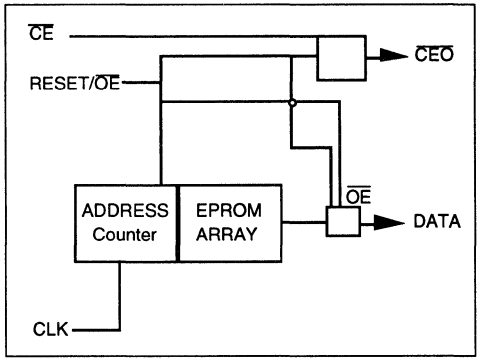
The Microchip Technology Inc. 37LV36/65/128 is a family of Serial OTP EPROM devices organized internally in a x32 configuration. The family also features a cascadable option for increased memory storage where needed. The 37LV36/65/128 is suitable for many applications in which look-up table information storage is desirable and provides full static operation in the 3.0V to 6.0V Vcc range. The devices also support the industry standard serial interface to the popular RAM-based Field Programmable Gate Arrays (FPGA). Advanced CMOS technology makes this an ideal bootstrap solution for today's high speed SRAM-based FPGAs. The 37LV36/65/128 family is available in the standard 8-pin plastic DIP, 8-pin SOIC and 20-pin PLCC packages.

Device	Bits	Programming Word
37LV36	36,288	1134 x 32
37LV65	65,536	2048 x 32
37LV128	131,072	4096 x 32

PACKAGE TYPES



BLOCK DIAGRAM



Xilinx is a registered trademark of Xilinx Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +0.6V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V

Output voltage w.r.t. VSS..... -0.6V to VCC +0.6V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied..... -65°C to +125°C

Soldering temperature of leads (10 sec.) ..... +300°C

ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function	8	20
DATA	Data I/O	1	2
CLK	Clock Input	2	4
RESET/$\overline{OE}$	Reset Input and Output Enable	3	6
$\overline{CE}$	Chip Enable Input	4	8
VSS	Ground	5	10
$\overline{CEO}$	Chip Enable Output	6	14
VPP	Programming Voltage Supply	7	17
VCC	+3.0V to 6.0V Power Supply	8	20
Not Labeled	Not utilized, not connected		

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +3.0 to 6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
DATA, $\overline{CE}$, $\overline{CEO}$ and Reset pins:					
High level input voltage	VIH	2.0	VCC	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH1	3.86		V	IOH = -4 mA VCC ≥ 4.5V
	VOH2	2.4			IOH = -4 mA VCC ≥ 3.0V
Low level output voltage	VOL	—	.32	V	IOL = 4.0 mA
Input Leakage	ILI	-10	10	µA	VIN = .1V to VCC
Output Leakage	ILO	-10	10	µA	VOUT = .1V to VCC
Input Capacitance (all inputs/outputs)	CINT	—	10	pF	Tamb = 25°C; FCLK = 1 MHz (Note 1)
Operating Current	ICC Read	—	10	mA	VCC = 6.0V, CLK = 10 MHz
		—	2	mA	VCC = 3.6V, CLK = 2.5 MHz
					Outputs open
Standby Current	ICCS	—	100	µA	VCC = 6.0V, CE = 5.8V
			50	µA	VCC = 3.6V, CE = 3.4V

Note 1: This parameter is initially characterized and not 100% tested.

2.0 DATA

2.1 Data I/O

Three-state DATA output for reading and input during programming.

3.0 CLK

3.1 Clock Input

Used to increment the internal address and bit counters for reading and programming.

4.0 RESET/$\overline{OE}$

4.1 Reset Input and Output Enable

A LOW level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A HIGH level on RESET/$\overline{OE}$ resets both the address and bit counters. In the 37LVXXX, the logic polarity of this input is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. This document describes the pin as RESET/$\overline{OE}$ although the opposite polarity is also possible. This option is defined and set at device program time.

5.0 $\overline{CE}$

5.1 Chip Enable Input

$\overline{CE}$ is used for device selection. A LOW level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A HIGH level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.

6.0 $\overline{CEO}$

6.1 Chip Enable Output

This signal is asserted LOW on the clock cycle following the last bit read from the memory. It will stay LOW as long as $\overline{CE}$ and $\overline{OE}$ are both LOW. It will then follow $\overline{CE}$ until $\overline{OE}$ goes HIGH. Thereafter, $\overline{CEO}$ will stay HIGH until the entire EPROM is read again. This pin also used to sense the status of RESET polarity when Programming Mode is entered.

7.0 VPP

7.1 Programming Voltage Supply

Used to enter programming mode (+13 volts) and to program the memory (+13 volts). Must be connected directly to Vcc for normal Read operation. No overshoot above +14 volts is permitted.

8.0 CASCADING SERIAL EPROMS

Cascading Serial EPROMs provide additional memory for multiple FPGAs configured as a daisy-chain, or for future applications requiring larger configuration memories.

When the last bit from the first Serial EPROM is read, the next clock signal to the Serial EPROM asserts its $\overline{CEO}$ output LOW and disables its DATA line. The second Serial EPROM recognizes the LOW level on its $\overline{CE}$ input and enables its DATA output.

When configuration is complete, the address counters of all cascaded Serial EPROMs are reset if RESET goes LOW forcing the RESET/$\overline{OE}$ on each Serial EPROM to go HIGH. If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground.

Additional logic may be required if cascaded memories are so large that the rippled chip enable is not fast enough to activate successive Serial EPROMs.

9.0 STANDBY MODE

The 37LVXXX enters a low-power Standby Mode whenever $\overline{CE}$ is HIGH. In Standby Mode, the Serial EPROM consumes less than 100 µA of current. The output will remain in a high-impedance state regardless of the state of the $\overline{OE}$ input.

10.0 PROGRAMMING MODE

Programming Mode is entered by holding VPP HIGH (+13 volts) for two clock edges and then holding VPP = VDD for one clock edge. Programming mode is exited by driving a LOW on both $\overline{CE}$ and $\overline{OE}$ and then removing power from the device. Figures 4 through 7 show the programming algorithm.

11.0 37LVXXX RESET POLARITY

The 37LVXXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{OE}$/RESET. Any third-party commercial programmer should prompt the user for the desired reset polarity.

The programming of the overflow word should be handled transparently by the EPROM programmer; it is mentioned here as supplemental information only.

The polarity is programmed into the first overflow word location, maximum address+1. 00000000 in these locations makes the reset active LOW, FFFFFFFF in these locations makes the reset active HIGH. The default condition is RESET active HIGH.

FIGURE 11-1: READ CHARACTERISTICS TIMING

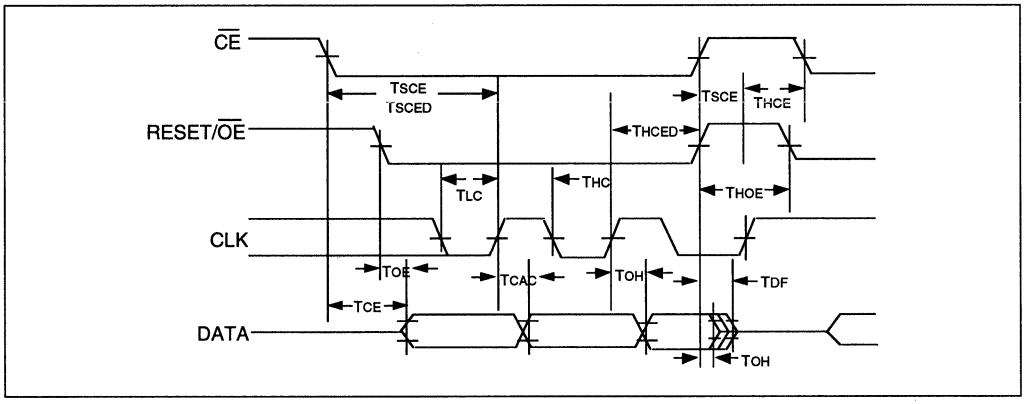


TABLE 11-1: READ CHARACTERISTICS

		AC Testing Waveform: V_{IL} = 0.2V; V_{IH} = 3.0V AC Test Load: 50 pF V_{OL} = V_{OL_MAX}; V_{OH} = V_{OH_MIN}					
Symbol	**Parameter**	**Limits 3.0V ≤ Vcc ≤ 6.0V**		**Limits 4.5V ≤ Vcc ≤ 6.0V**		**Units**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**		
TOE	$\overline{OE}$ to Data Delay	—	45	—	45	ns	
TCE	$\overline{CE}$ to Data Delay	—	60	—	50	ns	
TCAC	CLK to Data Delay	—	200	—	60	ns	
TOH	Data Hold from $\overline{CE}$, $\overline{OE}$ or CLK	0	—	0	—	ns	
TDF	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay	—	50	—	50	ns	Notes 1, 2
TLC	CLK Low Time	100	—	25	—	ns	
THC	CLK High Time	100	—	25	—	ns	
TSCE	$\overline{CE}$ Set up Time to CLK (to guarantee proper counting)	40	—	25	—	ns	Note 1
TSCED	$\overline{CE}$ setup time to CLK (to guarantee proper DATA read)	100	—	80	—	ns	
THCE	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0	—	0	—	ns	Note 1
THCED	$\overline{CE}$ hold time to CLK (to guarantee proper DATA read)	50	—	0	—	ns	
THOE	$\overline{OE}$ High Time (Guarantees counters are Reset)	100		20	—	ns	
CLK max	Clock Frequency	—	2.5	—	10	MHz	

Note 1: This parameter is periodically sampled and not 100% tested.
2: Float delays are measured with output pulled through 1kΩ to V_{LOAD} = Vcc/2.

FIGURE 11-2: READ CHARACTERISTICS AT END OF ARRAY TIMING

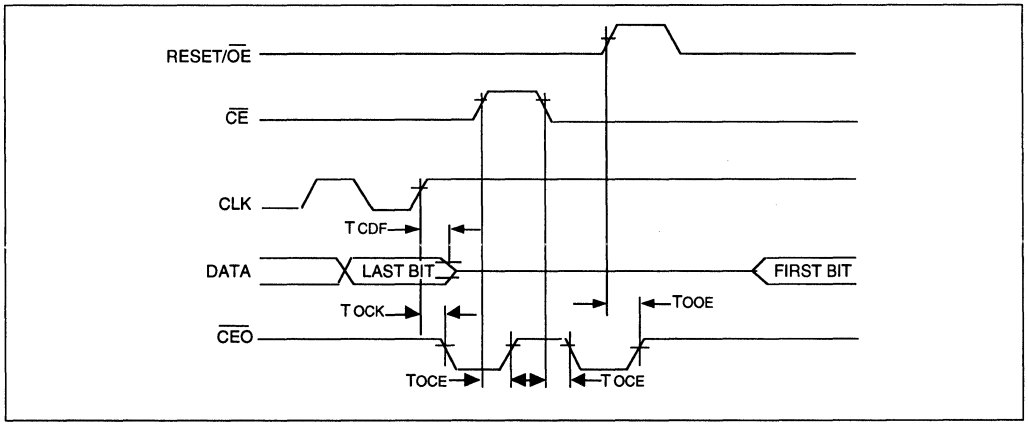


TABLE 11-2: READ CHARACTERISTICS AT END OF ARRAY

		AC Testing Waveform: VIL = 0.2V; VIH = 3.0V AC Test Load: 50 pF VOL = VOL_MAX; VOH = VOH_MIN					
Symbol	**Parameter**	**Limits 3.0V ≤ Vcc ≤ 6.0V**		**Limits 4.5V ≤ Vcc ≤ 6.0V**		**Units**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**		
TCDF	CLK to Data Float Delay	—	50	—	50	ns	Notes 1, 2
TOCK	CLK to $\overline{CEO}$ Delay	—	65	—	40	ns	
TOCE	$\overline{CE}$ to $\overline{CEO}$ Delay	—	45	—	40	ns	
TOOE	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay	—	45	—	40	ns	

Note 1: This parameter is periodically sampled and not 100% tested.
2: Float delays are measured with output pulled through 1kΩ to VLOAD = VCC/2.

TABLE 11-3: PIN ASSIGNMENTS IN THE PROGRAMMING MODE

DIP/SOIC Pin	PLCC Pin	Name	I/O	Description
1	2	DATA	I/O	The rising edge of the clock shifts a data word in or out of the EPROM one bit at a time.
2	4	CLK	I	Clock Input. Used to increment the internal address/word counter for reading and programming operation.
3	6	RESET/$\overline{OE}$	I	The rising edge of CLK shifts a data word into the EPROM when $\overline{CE}$ and $\overline{OE}$ are HIGH; it shifts a data word out of the EPROM when $\overline{CE}$ is LOW and $\overline{OE}$ is HIGH. The address/ word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held HIGH and $\overline{OE}$ is held LOW. Note 1: Any modified polarity of the RESET/$\overline{OE}$ pin is ignored in the programming mode.
4	8	$\overline{CE}$	I	The rising edge of CLK shifts a data word into the EPROM when $\overline{CE}$ and $\overline{OE}$ are HIGH; it shifts a data word out of the EPROM when $\overline{CE}$ is LOW and $\overline{OE}$ is HIGH. The address/ word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held HIGH and $\overline{OE}$ is held LOW.
5	10	VSS		Ground pin.
6	14	$\overline{CEO}$	O	The polarity of the RESET/$\overline{OE}$ pin can be read by sensing the $\overline{CEO}$ pin. Note 1: The polarity of the RESET/$\overline{OE}$ pin is ignored while in the Programming Mode. In final verification, this pin must be monitored to go LOW one clock cycle after the last data bit has been read.
7	17	VPP		Programming Voltage Supply. Programming Mode is entered by holding $\overline{CE}$ and $\overline{OE}$ HIGH and VPP at VPP1 for two rising clock edges and then lowering VPP to VPP2 for one more rising clock edge. A word is programmed by strobing the device with VPP for the duration TPGM. VPP must be tied to VCC for normal read operation.
8	20	VCC		+5 V power supply input.

TABLE 11-4: DC PROGRAMMING SPECIFICATIONS

Symbol	Parameter Ambient Temperature: Tamb = 25°C ±5°C	Limits		Units
		Min.	Max.	
VCCP	Supply voltage during programming	5.0	6.0	V
VIL	Low-level input voltage	0.0	0.5	V
VIH	High-level input voltage	2.4	VCC	V
VOL	Low-level output voltage	—	0.4	V
VOH	High-level output voltage	3.7	—	V
VPP1	Programming voltage*	12.5	13.5	V
VPP2	Programming Mode access voltage	VCCP	VCCP+1	V
IPPP	Supply current in Programming Mode	—	100	mA
IL	Input or output leakage current	-10	10	µA
VCCL	First pass Low-level supply voltage for final verification	2.8	3.0	V
VCCH	Second pass High-level supply voltage for final verification	6.4	6.6	V

* No overshoot is permitted on this signal. VPP must not be allowed to exceed 14 volts.

TABLE 11-5: AC PROGRAMMING SPECIFICATIONS (SEE NOTE 2)

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
TRPP	10% to 90% Rise Time of VPP	1		µs	Note 1
TFPP	90% to 10% Fall Time of VPP	1		µs	Note 1
TPGM	VPP Programming Pulse Width	.50	1.05	ms	
TSVC	VPP Setup to CLK for Entering Programming Mode	100		ns	Note 1
TSVCE	$\overline{CE}$ Setup to CLK for Entering Programming Mode	100		ns	Note 1
TSVOE	$\overline{OE}$ Setup to CLK for Entering Programming Mode	100		ns	Note 1
THVC	VPP Hold from CLK for Entering Programming Mode	300		ns	Note 1
TSDP	Data Setup to CLK for Programming	50		ns	
THDP	Data Hold from CLK for Programming	0		ns	
TLCE	$\overline{CE}$ Low time to clear data latches	100		ns	
TSCC	$\overline{CE}$ Setup to CLK for Programming/Verifying	100		ns	
TSIC	$\overline{OE}$ Setup to CLK for Incrementing Address Counter	100		ns	
THIC	$\overline{OE}$ Hold from CLK for Incrementing Address Counter	0		ns	
THOV	$\overline{OE}$ Hold from VPP	200		ns	Note 1
TPCAC	CLK to Data Valid		400	ns	
TPOH	Data Hold from CLK	0		ns	
TPCE	$\overline{CE}$ Low to Data Valid		250	ns	

Note 1: This parameter is periodically sampled and not 100% tested.

Note 2: While in Programming Mode, $\overline{CE}$ should only be changed while $\overline{OE}$ is HIGH and has been HIGH for 200 ns, and $\overline{OE}$ should only be changed while $\overline{CE}$ is HIGH and has been HIGH for 200 ns.

FIGURE 11-3: ENTER AND EXIT PROGRAMMING MODES

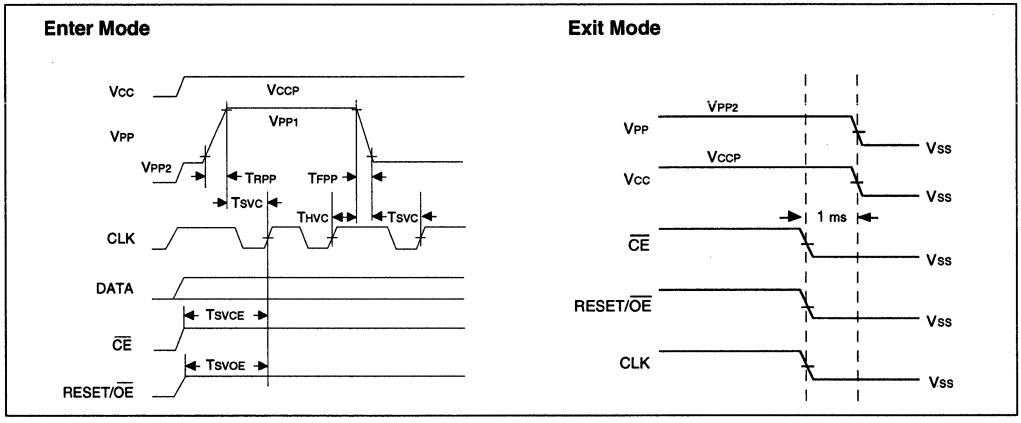


FIGURE 11-4: PROGRAMMING CYCLE OVERVIEW (NO VERIFY UNTIL ENTIRE ARRAY IS PROGRAMMED)

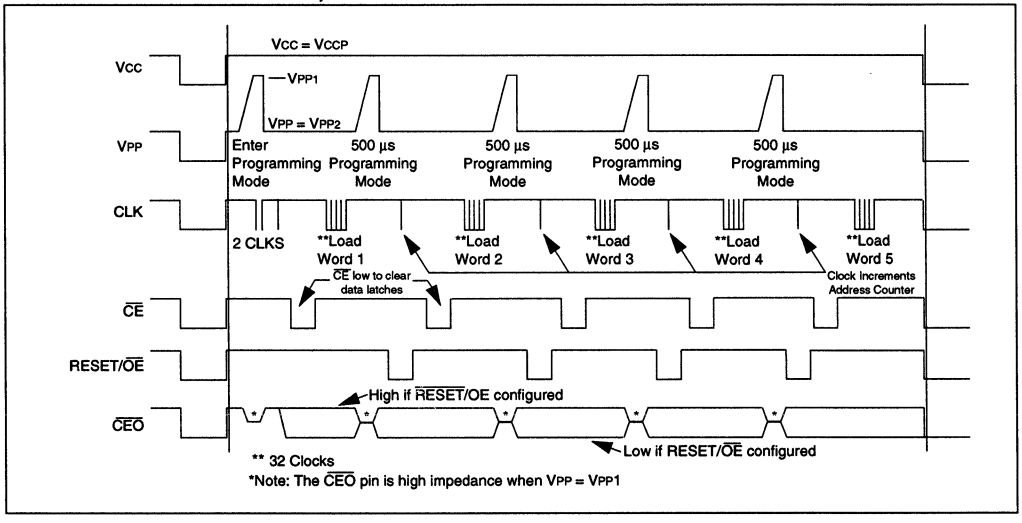


FIGURE 11-5: DETAILS OF PROGRAM CYCLE

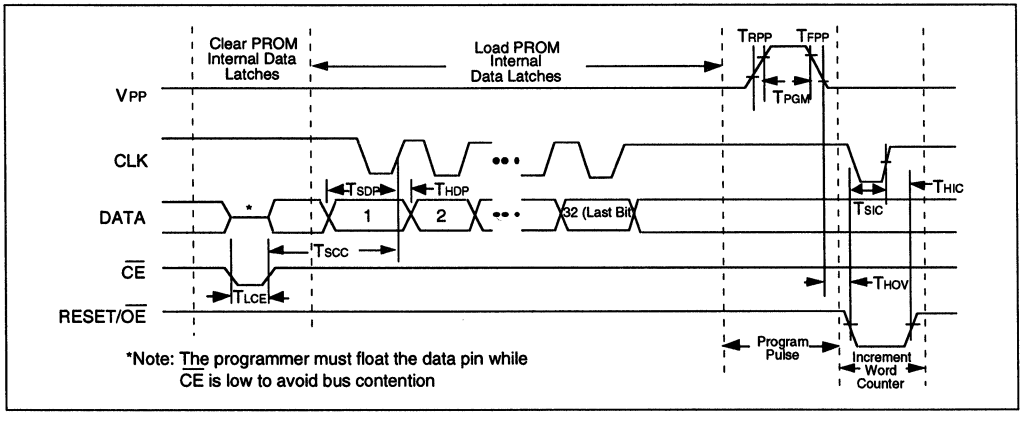


FIGURE 11-6: READ MANUFACTURER AND DEVICE ID OVERVIEW

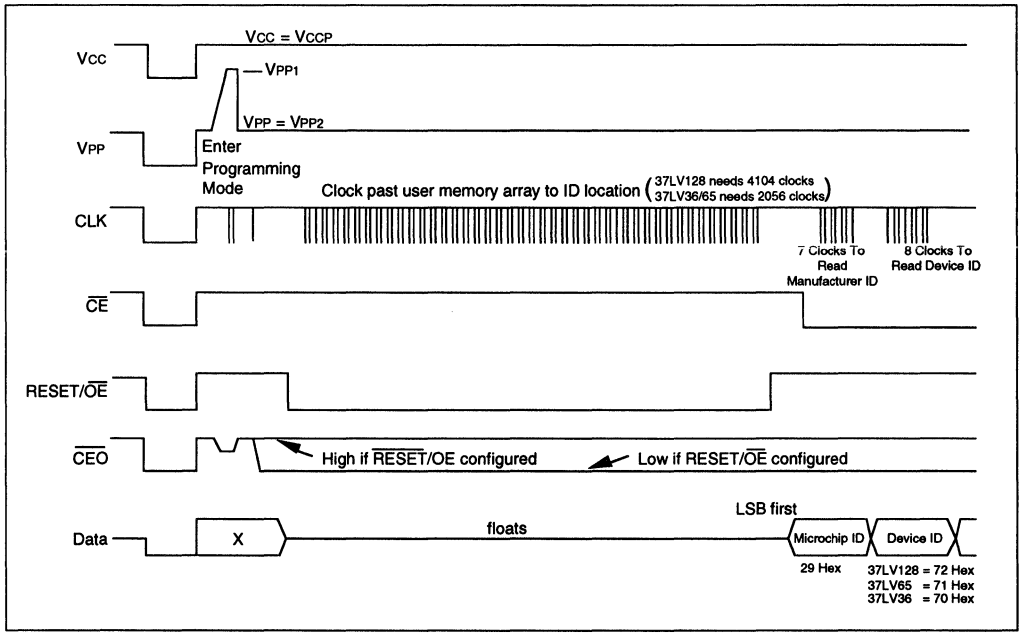


FIGURE 11-7: DETAILS OF READ MANUFACTURER AND DEVICE ID

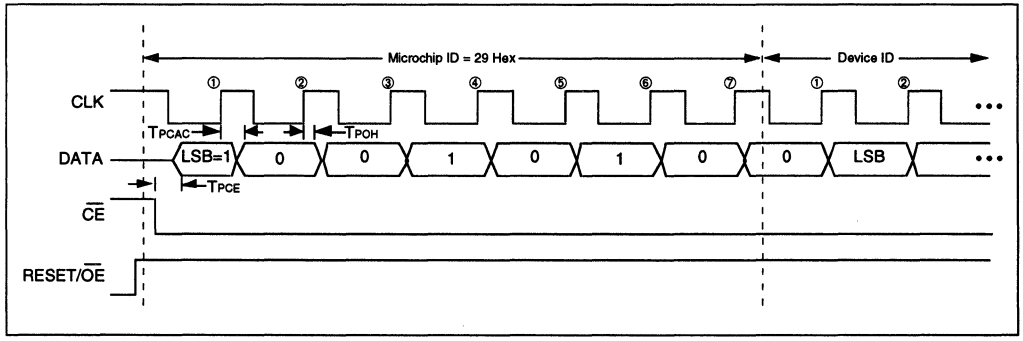
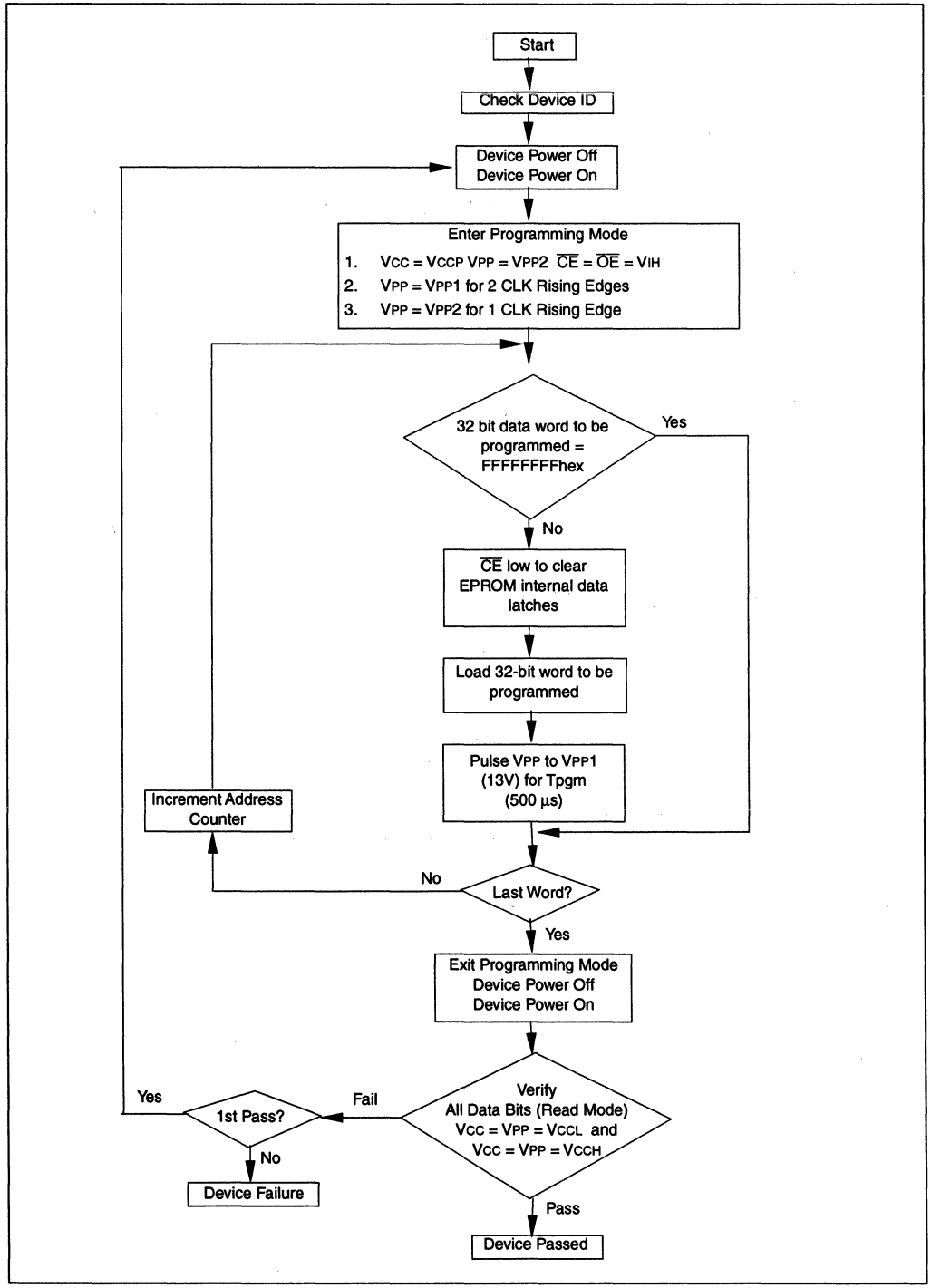


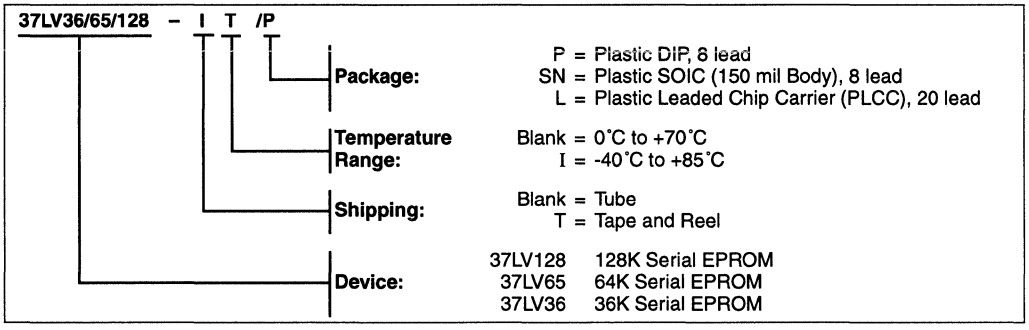
FIGURE 11-8: 37LVXXX PROGRAMMING SPECIFICATIONS



NOTES:

37LV36/65/128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



EPROM Programming Guide

All Microchip EPROMs should be programmed using the Express algorithm (shown on reverse side). Other algorithms can cause high programming fallout and even retention failures due to undue stress on the chips. This list will be updated as information becomes available. Programmer models and revisions shown are subject to change by the manufacturers at any time.

Manufacturer	Model	Software Rev	Status
DATA I/O	S1000	24 or 25	Verified Express
DATA I/O	29B	24	Verified Express
DATA I/O	288	1.0	Vendor specifies Express
DATA I/O	2900	1.1, 1.2, 1.7	Vendor specifies Express
DATA I/O	3900	1.0, 1.4	Vendor specifies Express
DATA I/O	Autosite	1.0, 1.5	Vendor specifies Express
DATA I/O	Unisite	3.0, 3.1, 3.2	Vendor specifies Express
STAG	PP42	8.0	Verified close to Express, but user must manually select double-voltage verify
STAG	PP39		Same
ELAN	5000/932 Turbo	6.02V1	Vendor specifies Express
ELAN	5000/932	5.05V1	Vendor specifies Express
EPRO	Model 124		User-programmable to Express
LOGIC DEVICES	AllPro 88, 40	2.2	Express AND Low Voltage Support No Express support for Windows version (Exar)
LOGIC DEVICES	GangPro 8+	1.1	Vendor specifies Express on latest release
LOGIC DEVICES	GangPro S		Fast, Rapid only
LOGIC DEVICES	GangPro S,	1.0	Vendor specifies Express on latest release
LOGIC DEVICES	Husky		Fast, Rapid only
BYTEK	Multitrk-4000		Vendor specifies Express on latest release
BP MICROSYSTEMS	1148,1200	3.06	Vendor specifies Express on latest release.

ADAPTERS

PLCC-to-DIP

Emulation Technology
32-28-01-P600

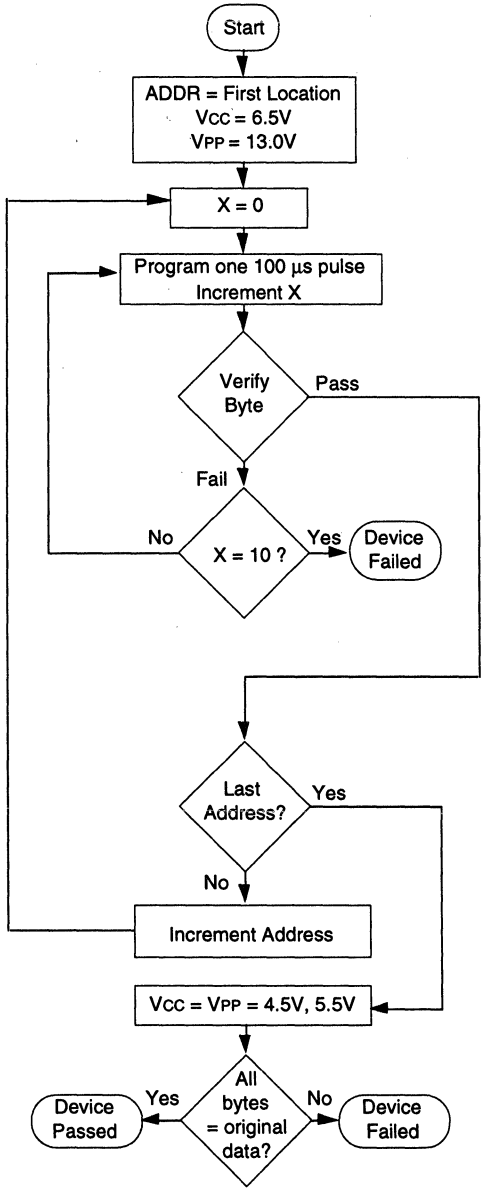
TSOP-to-DIP

Emulation Technology
AS-32-28-02TS-6ENP-GANG-S

Emulation Technology
Phone 408-982-0660, FAX 408-982-0664

EXPRESS ALGORITHM

Conditions:
T_{amb} = 25°C ±5°C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



SECTION 9
DEVELOPMENT TOOLS

On-Line Support — Microchip Internet Connections 9-1
Total Endurance™ — Microchip Serial EEPROM Endurance Model 9-3
Microchip Serial EEPROM Designer's Kit 9-5

ON-LINE SUPPORT

Microchip Internet Connections

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.futureone.com/pub/microchip

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits.The Hot Line Numbers are:

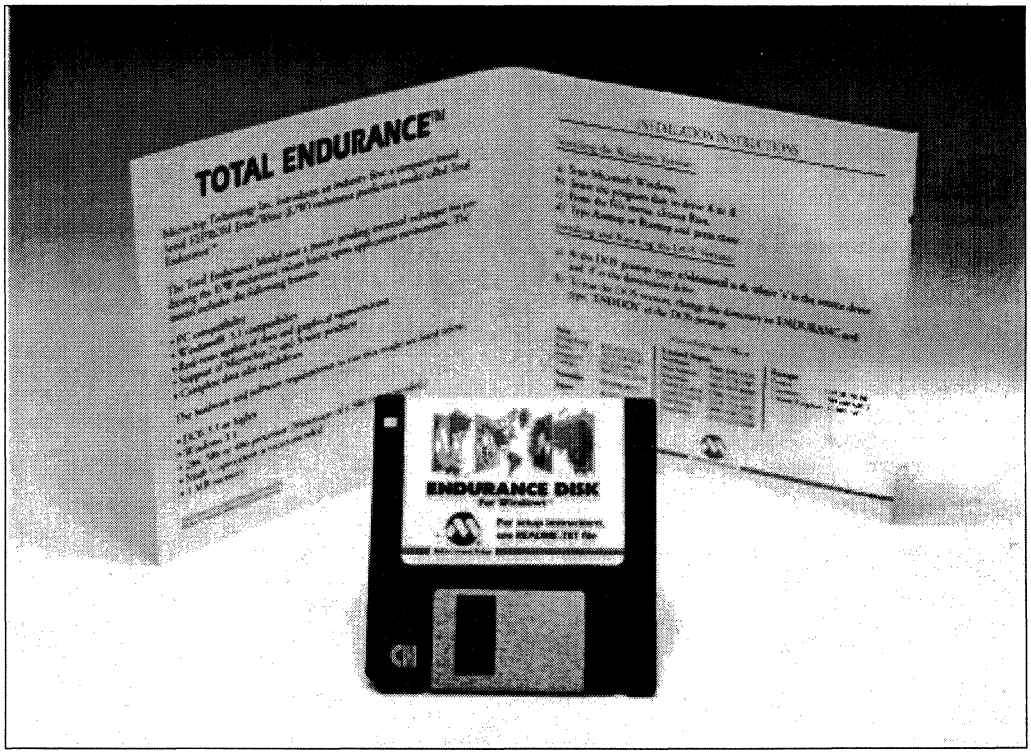
1-800-755-2345 for U.S. and most of Canada, and

1-602-786-7302 for the rest of the world.

MICROCHIP

TOTAL ENDURANCE™

Microchip Serial EEPROM Endurance Model



FEATURES

- IBM® PC compatibility
- Windows® 3.1 or DOS 3.1 compatibility
- Automatic or manual recalculation
- Real-time update of data
- Full-screen or windowed graphical view
- Hypertext on-screen help
- Key or slide-bar entry of parameters
- On-screen editing of parameters
- Single-click copy of plot to clipboard
- Numeric export to delimited text file
- On-disk Endurance Tutorial

SYSTEM REQUIREMENTS

- DOS 3.1 or higher
- Windows 3.1
- 1MB memory
- 386 or 486 processor recommended
- Math coprocessor recommended

DEVICE SUPPORT

- Microchip 2-wire 24CXX/24LCXXB/24AAXX/ 85CXX
- Microchip 3-wire 93CXX/93LCXX/93AAXX Series
- Microchip 4-wire 59C11

Total Endurance™

DESCRIPTION

Microchip's revolutionary Total Endurance Model provides electronic systems designers with unprecedented visibility into Serial EEPROM-based applications. This advanced software model (with a very friendly user interface) eliminates time and guesswork from Serial EEPROM-based designs by accurately predicting the device's performance and reliability within a user-defined application environment. Design trade-off analysis which formerly consumed days or weeks can now be performed in minutes...with a level of accuracy that delivers a truly robust design.

Users may input the following application parameters:

- Serial EEPROM device type
- Bytes to be written per cycle
- Cycling mode - byte or page
- Data pattern type - random or worst-case
- Temperature in °C
- Erase/Write cycles per day
- Application lifetime or target PPM level

The model will respond with FIT rate, PPM level, application life and a plot of the PPM level vs. number of cycles. The model is available in both DOS and Windows versions.

BACKGROUND

Microchip's research into the Erase/Write endurance of Serial EEPROMs has resulted in the conclusion that endurance depends upon three primary effects: the physical properties of the EEPROM cell, the internal error-correction technology employed, and the application environment. EEPROM endurance specified as a "typical" value in device data sheets must therefore be evaluated on a case-by-case basis, taking into account the manner in which the device will be used in the application. The Microchip Total Endurance™ software applies the user-defined application parameters to a complex mathematical model in order to emulate the EEPROM's performance and reliability in the system.

USING THE MODEL

The user has simply to choose a Microchip Serial EEPROM device from the device-list menu and begin entering the application parameters. The entire process can take literally seconds to complete, and the model will output the PPM level and FIT rate of the device vs. the number of Erase/Write cycles. If the user has specified an application lifetime, the model will output PPM and FIT rates at that point in time. Alternately, the user may input a desired PPM level and the model will calculate the application lifetime which will result in that survival rate. The user may then trade-off any of the parameters (device type, voltage, application life, temperature, # of bytes per cycle, # of cycles per day etc.) to arrive at an optimal solution for the intended application.

Whenever a parameter is changed, calculation of the ppm/application life is automatic. An "update" box will appear inside the graph to indicate that new data has been entered and the graph should be redrawn. A single click in the "draw" box will redraw the plot of ppm vs. cycles; a click in the "Resize" box will take the plot to full-screen display for a closer view. The plot data can be saved to a file or the plot itself can be copied to the clipboard to be pasted into another application.

ACCURACY OF THE MODEL

The accuracy of the Microchip Total Endurance model has been verified against test data to within ten percent of the actual values. However, Microchip makes no warranty as to its accuracy or applicability of the information to any given application. It is intended to be used as a guide to aid designers of Serial EEPROM-based systems in performing trade-off analysis and developing robust and reliable designs.

Order Information:

Description	Part Number
Total Endurance Software Disk	SW242001

SEEVAL® DESIGNER'S KIT

Microchip Serial EEPROM Designer's Kit

FEATURES

- Includes everything necessary to begin developing Serial EEPROM-based applications
- Microchip *Total Endurance*™ software model
- Microchip *SEEVAL* evaluation and programming board
- Microchip *SEEVAL* software
- Microchip Serial EEPROM handbook
- Microchip Serial EEPROM sample pack
- RS-232 serial cable
- Power supply

SYSTEM REQUIREMENTS

- DOS 3.1 or higher
- Windows® 3.1
- VGA monitor
- 386 or 486 processor recommended
- Math coprocessor recommended

DEVICE SUPPORT

- Microchip 2-wire 24CXX/24LCXXB/85CXX
- Microchip *Smart Serial*™ 24XX65
- Microchip 3-wire 93CXX/93LCXX series
- Microchip 4-wire 59C11

Designer's Kit

DESCRIPTION

Now designers of Serial EEPROM-based applications can enjoy the increased productivity, reduced time to market, and the ability to create a rock-solid design that only a well-thought-out development system can provide. Microchip's new Serial EEPROM Designer's Kit includes everything necessary to quickly develop a robust and reliable Serial EEPROM-based design and greatly reduce the time required for system integration and hardware/software debug.

The **Total Endurance software model** enables designers to quickly choose the best Serial EEPROM for the specific application and perform trade-off analysis with voltage, temperature, write cycle and other system parameters in order to achieve the desired Erase/Write endurance (specific ppm rate) or product lifetime. Total Endurance is the new standard of excellence in understanding and predicting the Erase/Write endurance of Serial EEPROMs. An on-line endurance tutorial is included, along with hypertext help files.

Microchip's **SEEVAL Serial EEPROM evaluation and programming system** will accept any Microchip Serial EEPROM in DIP package and enable the designer or system integrator to read, write, or erase any byte or the entire array. SEEVAL also provides the following advanced features to aid in system integration and debug:

- Program special user functions like *Smart Serial* configurations
- Hexadecimal display of array contents
- Pre-set or user-defined repeating patterns
- User-configurable functions like continuous read/write, programmable delay, etc.
- Upload/download files between the Serial EEPROM and disk

Another industry first, the **Microchip Serial EEPROM Handbook** provides a plethora of information crucial to the designers of Serial EEPROM-based systems. Along with data sheets on Microchip Serial EEPROMs, this resource provides application notes regarding Erase/Write endurance, interfacing with different protocols and many, many others. A cross-reference and selector guide are also included, plus article reprints and qualification reports on Microchip Serial EEPROMs.

USING SEEVAL AND TOTAL ENDURANCE

Both software packages can be loaded from Windows by choosing FILE RUN and entering SETUP.EXE from the Program Manager. The applications will install themselves; then a double mouse-click will start either application. The first step in either program is to select a device from the device list.

In Total Endurance, the user has simply to choose a Microchip Serial EEPROM device from the device-list menu and begin entering the application parameters. The entire process can take literally seconds to complete, and the model will output the PPM level and FIT rate of the device vs. the number of Erase/Write cycles. If the user has specified an application lifetime, the model will output PPM and FIT rates at that point in time. Alternately, the user may input a desired PPM level and the model will calculate the application lifetime which will result in that survival rate. The user may then trade-off any of the parameters (device type, voltage, application life, temperature, # of bytes per cycle, # of cycles per day etc.) to arrive at an optimal solution for the intended application.

Whenever a parameter is changed, calculation of the ppm/application life is automatic. An "update" box will appear inside the graph to indicate that new data has been entered and the graph should be redrawn. A single click in the "draw" box will redraw the plot of ppm vs. cycles; a click in the "Resize" box will take the plot to full-screen display for a closer view. The plot data can be saved to a file or the plot itself can be copied to the clipboard to be pasted into another application.

In **SEEVAL**, the user may choose to load a file from disk to program the Serial EEPROM, or read data from the EEPROM and save it to disk. The screen displays the contents of a software buffer. The buffer may be manipulated before programming data to the Serial EEPROM, or data can be written to the Serial EEPROM directly on-line. An area of memory can be highlighted (selected) and programmed with a predefined pattern or user-specified pattern. Alternately, the entire device can be programmed with any repeating pattern.

Both SEEVAL and Total Endurance allow the user to save any configuration as default. This configuration (device and application settings) will then automatically load at boot time.

Order Information:

Description	Part Number
Serial EEPROM Designer's Kit	DV243001

SECTION 10
QUALITY, RELIABILITY, AND ENDURANCE

Product Quality 10-1
Product Reliability 10-9
EEPROM Endurance 10-19

MICROCHIP

Product Quality

A CORPORATE COMMITMENT

Microchip Technology Inc. has evolved a culture where a commitment to quality is an integral part. By empowering every employee to be responsible for the quality of their work, the entire corporation is involved in the quality process. This interaction creates an environment for continuous improvement throughout the organization. The benefits of the system are then not only enhanced product quality and reliability but also product services.

THE CHALLENGE OF COMPLEXITY

Integrating an Ideal

Microchip's quality programs and business plan are vertically integrated and touch all levels of the company. From the top down, the President and CEO actively lead programs to ensure continuous improvement is a perpetual process. Improvement and cross functional teams work to enhance performance at every department level. Incorporating the improvement objectives into the business plan creates a unity of purpose and mandates that the two merge as one measurement.

Determination to be the Best

A fundamental concept at Microchip is the commitment to continuous improvement. All areas are constantly looking for ways to improve every aspect of the company. This has allowed products and processes to become world class in quality and reliability. These programs are the foundation for success.

PROCESS TECHNOLOGY

All the products manufactured at Microchip make use of a common N-Well CMOS baseline process to which modules are added in order to create the specific functions required by the product (EEPROM, Microcontroller, Logic and EPROM).

The baseline process, which has been in Manufacturing since 1988, uses minimum dimensions of 1.5µm, 360Å gate oxide thickness, N+ doped polysilicon gates and arsenic implanted source-drain diffusions for the N-channel devices.

A more advanced process uses minimum dimensions of 1µm, 250Å gate oxide thickness, polycide gate and LDD junction for the N-channel devices. A double level metal module can be added to both processes.

All of these devices utilize a proprietary passivation suitable for a wide variety of package types. Microchip's processes have been developed with reliability and manufacturability as their primary goals.

EEPROM

Microchip's CMOS floating gate EEPROM technology produces a non-volatile memory cell by storing or removing charge from the floating gate. Charge is transferred bidirectionally to the floating gate by Fowler-Nordheim tunneling through a sub-10 nm oxide over the drain of the transistor. This technology produces a memory cell with a typical endurance of > 10^7 cycles and greater than 40 years of data retention. (See EEPROM application note for details).

EPROM

This technology uses a non-volatile memory cell which stores charge on a self aligned floating gate. Electrons are provided to the floating gate via hot electron injection from the drain depletion region. Each byte can typically be programmed in 100 microseconds, and can retain that data for more than 10 years with unlimited reads. Block erasing is accomplished with a high intensity UV source through the package window. Windowed parts can be erased and reprogrammed more than 100 times.

Microcontroller and Logic

Logic products are built on a variety of Microchip's processes and their derivatives. These products have process modules for production of controllers that feature ROM, Analog, EPROM, and EEPROM. By utilizing the standard processing modules, the designs meld these technologies and their flexibility while maintaining the high quality and reliability standards expected.

QUALITY

Design for Quality and Reliability

Product reliability is designed into all Microchip processes and products. Design margins are established to guarantee every product can be produced economically, error-free and within the tolerances of the manufacturing process. Product Introduction Teams representing manufacturing, engineering, quality and product divisions ensure that exacting standards are met for each specific product.

Microwire is a registered trademark of National Semiconductor.

Documentation and Procurement Specifications

Microchip's documentation control program assures the correct and current document always is available at the point of use. Active documents are revision coded and serialized. Procurement specifications bear the same requirements. These document control procedures, which are common in the industry for military and high reliability products, are employed by Microchip, system wide.

In Line Controls and Process Assessment

Product integrity is assured by sampling and inspection plans performed in-line. This enables Microchip to control and improve product quality levels as product moves through the manufacturing operation. Microchip's acceptance sampling plans in assembly emphasize the attempt to eliminate defective product as it is discovered. Acceptance and sampling plans are based on proprietary low fraction defective (<1000ppm) quality statistics.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at selected process steps. In-process controls are performed by operators in the wafer fabrication and assembly operations. Operators take immediate corrective action if a process step is out of its control limit. Through these in-line controls the true capability of a process is generated. (See Appendix A:In Line Controls)

Control of Customer Quality is attained through a statistical program based on minimum defect capability levels. These levels are defined as the error levels associated with the circuit design and science limitations of the chemistry and physics of processing.

Material controls prevent defective piece parts from getting into the line. Microchip's assembly material control sample plan is typical of the emphasis placed on safeguards. (See Appendix B:Material Controls Package).

Testing for Margin

Microchip conducts a product's initial test under stringent requirements. All quality assurance tests are run to tighter limits than customer specifications. As part of an outgoing quality assurance program, products are tested at least two machine tolerances tighter than those limits specified by the customer on every parameter. Margin testing accounts for normal tolerances of any particular test system and provides the assurance that Microchip's products meet a customer's specifications.

Variation from Expectation

Microchip works to make variation from target as small as possible. The better process is the one that holds the narrowest dispersion. Processes are targeted to maintain Cpk's of >1.5 and currently have typical values of >2.0. Higher process capability values are continually strived for indicating that better process control is being obtained.

Outgoing Quality

Quality Control samples all outgoing product from final testing. These samples measure in-line defect levels after screens have been applied. Root cause analysis follows, initiating technical change to effect continuous improvement.

Programmability Yield

Using programmable devices adds a complexity to the Quality Level interpretation. It is not unlikely that some programmable devices will not program. The programmability yield is dependent on (but not limited to): programmers, technology, array size, and handling.

Any device that does not program properly will not be used in the end system. Therefore, programmability yields should not be used to calculate AQLs.

For convenience, Microchip offers programming services for certain devices. This service is an advantage to the customer since it not only eliminates programmability rejects, but also reduces the handling of the parts. See the individual data sheets for details on our Quick-Turnaround-Production (QTP) service.

RELIABILITY

Process Qualification

No priority is more important than the one where processes under which Microchip products are built operate without fail. All products are stressed beyond normal use limits when undergoing high temperature operating life and retention bake tests. This is done to ensure that the devices meet the strictest reliability guidelines and will maintain industry low failure rates.

Package Qualification

Package qualification measures a component's ability to withstand extreme thermal and mechanical stresses. All products are stressed to high level industrial specifications to ensure reliability.

Ongoing Sampling of Key Reliability Variables

Microchip conducts accelerated mechanical tests, operating life tests and memory retention tests to explore the many ways failures might occur. Data obtained from continuous testing is used to identify potential reliability problems and for defining action courses to improve product. Microchip's reliability knowledge is shared with customers. This data is available for use in customer's own quality and reliability improvement programs and is published in regular quarterly and yearly reports.

RELIABILITY CONCEPTS

Definition

Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The reliability (or probability of survival) range runs from 0 (no chance of survival) to 1 (no chance of failure). Current microelectronic circuits are manufactured and controlled to such tight specifications that reliability figures for the total operation time approaching 1 (i.e., 0.9999) are common. As a result, the complement of reliability, or the failure probability, is more often quoted in current literature.

The failure rate is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per unit circuit-hour would generally be very small. To avoid reporting such small numbers, failure rates have been defined for greater circuit-hours. One thousand circuit-hours is defined as one circuit operating for one thousand hours, or 1,000 circuits operating for 1 hour, etc. The numbers of circuit-hours is the number of circuits multiplied by the number of operation hours for each circuit.

Two methods to define failure rate are commonly used:

- Percent failures per thousand circuit-hours
- Absolute failures per billion circuit-hours, or FITs.

Note that a failure rate of 0.0001%/1000 hours and 1 FIT are equivalent numbers.

Bathtub Curve: Failure Rate Over Time

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. (See Figure 1).

The early failure rate (infant mortality) period starts from initial operation (time T0) and decreases as time goes on.

Time T1 signifies the end of the infant mortality period. The next phase of the curve occurs between time T1 and T2. This long period of time is distinguished by a nearly constant and very low failure rate. After T2 is passed, the failure rate starts to increase slowly. This last phase of failure rate vs. time is known as the wear-out period.

Temperature Dependency

In order to establish failure rates in a reasonable time, it is necessary to accelerate the incidence of the failure modes. Higher environmental stress levels than those encountered under normal conditions are needed. The accelerating parameter most employed is junction temperature, although voltage and humidity, for example, are also used. Higher temperatures are capable of accelerating many common failure modes dramatically.

Arrhenius Equation

A number of mathematical models were developed to quantify the relationship between accelerated failure rates and increased junction temperatures. The one model most commonly used employs the Arrhenius Equation. It is as follows:

$$AF = e^{x}, \text{ where } x = \frac{E_A}{K}\left[\frac{1}{T_N} - \frac{1}{T_A}\right]$$

AF = Acceleration Factor (non-dimensional)

e = 2.718281828... (non-dimensional constant)

E_A = Activation energy level (electron volts)

k = Boltzmann's constant = 8.6172 x 10-5 (electron-volts/degree Kelvin)

T_N = Normal junction temperature (degrees Kelvin)

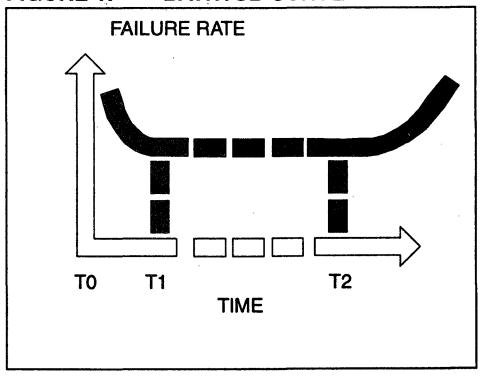
T_A = Accelerated junction temperature (degrees Kelvin)

Thus, the time to achieve a certain probability of failure at time T1 under temperature TN can be compressed to T1 divided by AF at the accelerated temperature, TA.

Note that for true acceleration, the acceleration factor AF is independent of the probability of the fail point specified.

AF, the dependent variable of the Arrhenius Equation is a function of several variables. TN and TA are specified for the situation under consideration. EA is a function of the particular mode of failure, and is determined by experimental evaluation.

FIGURE 1: BATHTUB CURVE



Activation Energy Level

Activation energy levels in semiconductors generally are in the 0.3 - 1.1 electron-volt range. Each failure mode has its own activation energy. Some typical examples are:

FAILURE MECHANISM	E_A (eV)
Oxide/Dielectric Breakdown	0.3
Electromigration	0.5 to 0.7
Surface Related Contamination	1.0
Intermetallics	1.0
Floating Gate Charge Loss	0.6 to 1.2
Hot Electron Trapping	-.1
Charge Trapping	0.12

A compromise value of 0.6 electron-volts is often used when there is no specific information relating to the failure modes being accelerated.

RELIABILITY TESTS

Operating Life Test (Dynamic Life)

The High Temperature Test is run under dynamic bias conditions where inputs are clocked. The test is conducted at high temperature to accelerate the failure mechanisms. The normal temperature for the test is +125°C for 1,000 hours. Readouts occur at 168 and 1,000 hours. Early hour failures are usually associated with manufacturing defects or otherwise marginal material.

Retention Bake

The Retention Bake Test is performed to accelerate data loss on floating gate devices. The test consists of unbiased baking at elevated temperature. This test is performed at 150°C with typical readpoints at 168 and 1000 hours.The failure mechanism that is accelerated is charge leakage from a stored element.

Endurance Cycling

Endurance Cycling establishes the number of times a device can be programmed and erased. Normally the test is conducted at rated temperature conditions and is followed by retention bake. The standard cycling at Microchip is done at 85°C using a page cycle mode and is followed by a bake of both a checkerboard and an inverse checkerboard of 48 hours at 150°C.

Temperature Cycle

The Temperature Cycle test simulates stresses which occur to systems during power up/power down sequences. The test is intended to reveal any deficiencies resulting from thermal expansion mismatch of the die/package structure. Normally the test is conducted by cycling between -65°C and +150°C in an air ambient. Duration for the test is typically 50 cycles for both plastic and ceramic packages. Endpoint criteria are both electrical and visual/mechanical.

Thermal Shock

The Thermal Shock test is similar to the Temperature Cycle test except that the ambient during cycling is liquid-to-liquid. This stimulates rapid thermal environmental changes. The mechanisms accelerated are identical to those in the Temperature Cycle test except that the Thermal Shock test is a more accelerated test with temperatures normally +125°C to -55°C. The number of cycles are 100 for qualification testing.

Autoclave

The autoclave test determines the survivability of devices in molded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121.5°C and 15 pounds per square inch (one atmosphere) gauge pressure. The 168 or more hours of testing allows moisture to penetrate into the die. Chemical corrosion of the die metallization may occur if ionic contaminants are present and the die surface protection is deficient or damaged. Charge leaks from floating devices usually happen before a corrosion mechanism develops.

HAST

The Highly Accelerated Stress Test is similar to the Temperature Humidity Test but with more stringent temperature exposure. Devices are subjected to 130°C with 85% relative humidity and an alternating bias of 5 volts and ground on device pins. The duration of the test is 168 hours. This tests for ionic contamination and corrosion, but floating gate devices may also fail for charge loss, due to the high temperature.

QUALIFICATION CATEGORIES

In general, qualification is required for new design, major changes in old design, process or material when either wafer fabrication or package assembly operations are affected. Cross functional teams which include reliability develop new products for introduction. In other areas, Microchip utilizes the concept of a Change Control Board which meets regularly to establish which criteria is to be used for all specific proposed changes. This board is made up of representative leaders of various groups and departments throughout Microchip to insure all concerns are heard early during the process.

QUALIFICATION PROGRAMS

Qualifications guarantee changes to our new processes and technologies are properly evaluated for reliability performance.

Reliability Monitoring

Microchip's reliability monitoring program is a comprehensive effort to measure the reliability of all process families with strict regularity. The program strives to improve performance through failure analysis and corrective action. Numerous screening procedures are used and estimates of product life and expected failure rates are provided.

Typical tests and frequencies include:

- Die Monitor on selected product for:
  - Dynamic Life
  - Retention Bake
  - Endurance
- Periodic (weekly, monthly and quarterly) package monitors to evaluate:
  - Mechanical stresses
  - Alignment
  - Temperature and moisture stresses
  - Corrosion resistance
  - Marking permanency

APPENDIX A: IN LINE CONTROLS

TABLE 2: CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% sample LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	4X/Lot/Machine LTPD 15	X	—	N/A
Wire Bond	Machine Shut Down	1% AQL each 1/2 shift	X	—	MIL-STD-883C Method 2010
Post Wire Bond	Reject defectives 100% rescreen per LTPD	LTPD 15	X	—	MIL-STD-883C Method 2010
Mold Press	Machine Shut Down	One sample /4 hrs	X	—	N/A
Die Plating	Reject defectives 100% rescreen per LTPD	Every 4 hrs LTPD 10	X	—	N/A
Trim and Form	Reject defectives 100% rescreen per LTPD	Once/ 2 hrs LTPD 10	X	—	N/A
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

TABLE 3: CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	Non-destruct each 2 hrs destruct each shift	X	—	MIL-STD-883C Method 2010
Wire Bond	Machine Shut Down	4X/shift/machine	X	—	MIL-STD-883C Method 2010
Preseal Visual	Reject defectives 100% rescreen per LTPD	100% LTPD 15	— X	X —	MIL-STD-883C Method 2010
Package Seal	Machine Shut Down	LTPD 15	X	—	N/A
Environmental Stress Centrifuge Temp Cycle	Machine Shut Down	LTPD 5 84(0) 84(0)	X	—	MIL-STD-883C Method 2001 Method 1010
Fine Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Gross Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Lead Trim	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2009
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

APPENDIX B: MATERIAL CONTROLS PACKAGE

TABLE 4: MATERIALS CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Lead Frame	Reject defectives 100% rescreen per LTPD	Visual, LTPD 2 Functional, LTPD 10 and material spec	X	—	N/A
Die Attach Epoxy	Reject	Functional, LTPD 15 and material spec	X	—	N/A
Gold Wire	Reject	Per material spec	X	—	N/A
Molding Compound	Reject	Spiral flow, 3X/lot Functional, 1X/lot and material spec	X	—	N/A

TABLE 5: MATERIALS CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Base/Lead Frame	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Package	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Preform	Reject	Visual, LTPD 10 Functional, LTPD 15	X	—	MIL-M-38510
Bond Wire	Reject	Per material spec 2 spools/lot	X	—	MIL-M-38510
Lid	Reject	Visual, LTPD 7 Functional, LTPD 10 and material spec	X	—	MIL-M-38510

MICROCHIP

Product Reliability

OVERVIEW

Microchip Technology Inc.'s products provide competitive leadership in quality and reliability, with demonstrated performance of less than 100 FITs (Failures in Time) operating life for most products. The designed-in reliability of Microchip's products are supported by ongoing reliability data monitors. This document presents current data for your use - to provide you with results you can count on.

The test descriptions included in this document explain Microchip's quality and reliability system. The product data demonstrates its results.

The customer's quality requirements are Microchip's top priority. Ongoing customer feedback and device performance monitoring drive Microchip, leading to continuing improvements in the long-term quality and reliability.

FAILURE RATE CALCULATION

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arhenius equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip Technology agree closely with those published in the literature. For complex CMOS devices in production at Microchip Technology, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. This activation energy also applies to some of our retention bake failures, though most are 1.2eV. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink, or air flow by convection is used.

Environment	Typical Failure Mechanism
Dynamic Life	Process parameter drift/shift Metal electromigration Internal leakage path Lifted bond/ball bond chip-out
Temperature Cycle	Lifted bond/ball chip-out Cracked die or surface cracks Bond pad corrosion
Autoclave	Inter-pin leakage Charge loss
Retention. Bake	Charge loss
High Temp. Reverse Bias	Charge gain, Parameter drift/ shift

DEFINITIONS

FIT (Failure In Time): Expresses the estimated field failure rate in number of failures per billion power-on device-hours. 100 FITS equals 0.01% fail per 1,000 device-hours.

Dynamic Life Test: The device is dynamically exercised at a high ambient temperature (usually 125°C) to quickly simulate field life. Derating from high temperature, an ambient use condition failure rate can be calculated.

Temperature Cycle: The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 10 minutes, 150°C for 10 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

Autoclave (pressure cooker): Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121.5°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Microwire is a registered trademark of National Semiconductor.

Thermal Shock: Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media.

Retention Bake: A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

HAST: Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 Volts and ground on alternating pins.

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system ensures that released products are designed, processed, packaged and tested to meet both design functionality and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability.

RELIABILITY DATA SUMMARY

Introduction

This section provides a reliability summary of Microchip Technology's product. Included is reliability data and packaging information obtained over the recent past.

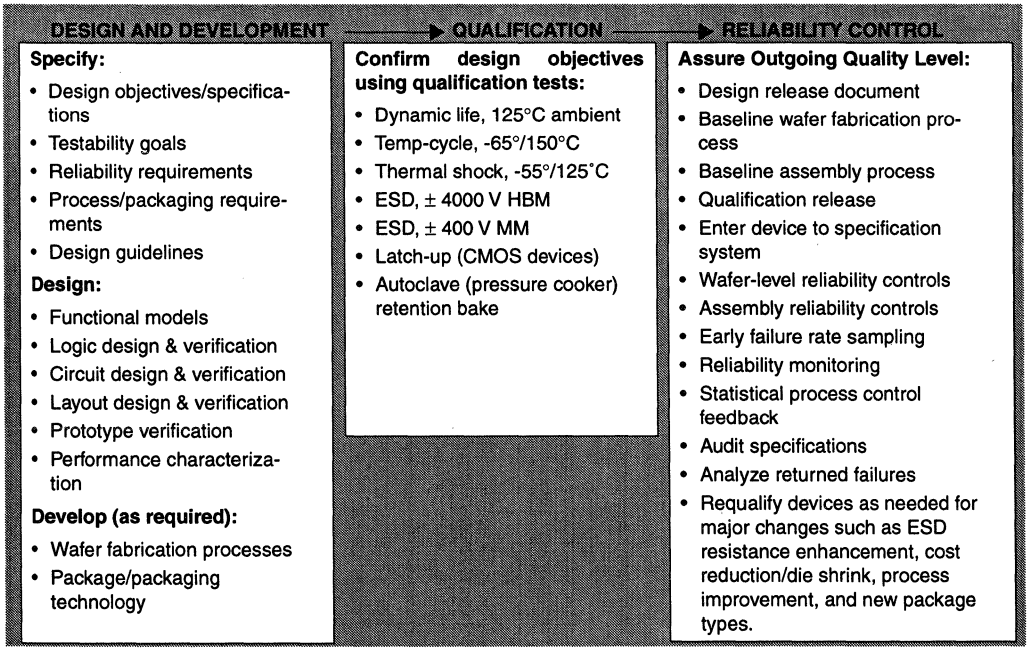
Plastic Package Characteristics and Codes

As part of an on going product program, Microchip Technology will apply its Quality and Reliability process in evaluating the latest developments in plastic packaging technology, and implement the highest reliability materials and assembly techniques. The plastic packages that are currently available from Microchip are listed in the table below.

Package Description Identification Code

Package Description	Identification Code
Plastic Leadless Chip Carrier	L
Plastic Dual In Line (600)	P
Plastic Dual In Line (300)	SP
Plastic SOIC (.150)	SL/SN
Plastic SOIC (.207)	SM
Plastic SOIC (.300)	SO
Plastic TSOP (8 x 20mm)	TS
Plastic SSOP (.207)	SS

FIGURE 1: RELIABILITY CONTROL SYSTEM DIAGRAM



HIGH TEMPERATURE (125°C) DYNAMIC LIFE TEST

Graph set for EEPROM, PICmicro™ and EPROM for all conditions

High temperature dynamic life testing accelerates random failure modes which would occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems.

FIGURE 2: EEPROM DYNAMIC LIFE

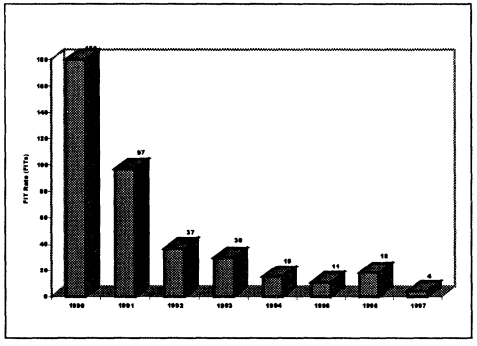


FIGURE 3: EPROM DYNAMIC LIFE

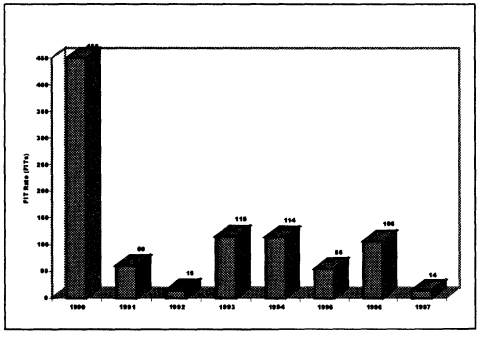
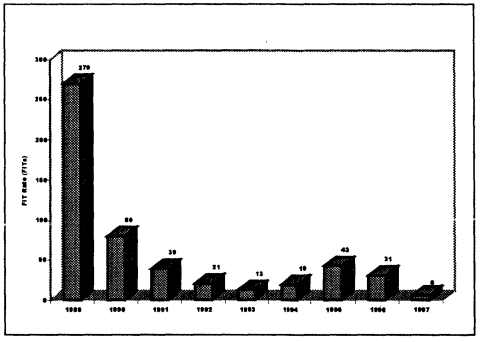


FIGURE 4: PICMICRO™ MCU DYNAMIC LIFE



PICmicro is a trademark of Microchip Technology Inc.

DATA RETENTION BAKE

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of zeroes to ones. This bake accelerates charge loss in the memory cell and 168 hours at 150°C is equivalent to greater than 250 years in the field at 55°C.

FIGURE 5: EEPROM RETENTION BAKE

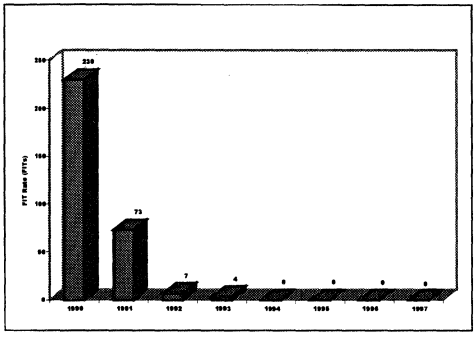


FIGURE 6: EPROM RETENTION BAKE

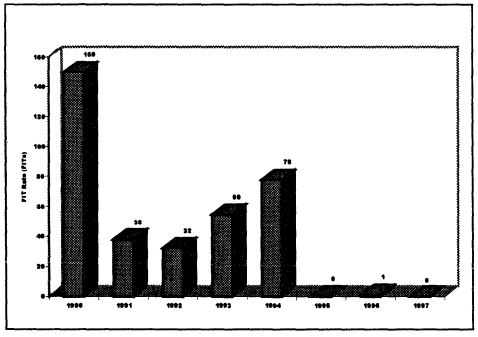
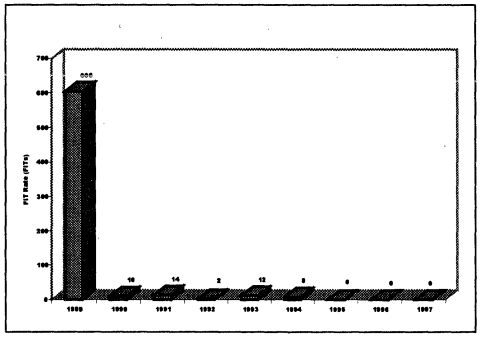


FIGURE 7: PICMICRO MCU RETENTION BAKE



PCT (PRESSURE COOKER AUTOCLAVE)

Autoclave testing is used to determine the resistance of the package to moisture under high temperature and humidity conditions. This test accelerates failure modes caused by delamination, corrosion or ionic contamination.

Operating Hours		
Package	**24**	**168**
QFP	0/2200	0/2199
PDIP	0/8092	1/8134
PLCC	0/2746	0/2746
SOIC	0/14042	7/14085
TSOP	0/250	0/250

PCT Failure Modes:

1 Unit of 8L PDIP (24LC02B) failed due to high IDDs.
1 Unit of 28L SOIC (97064) failed due to die surface delamination.
4 Units of 8L SOIC (24LC04B) failed due to column defects
1 Unit of 8L SOIC (24LC04B) failed due to oxice breakdown in the charge pump.
1 Unit of 8L SOIC (24LC04B) failed functinality at high speed.

TEMPERATURE CYCLING

This thermal tests evaluates air to air rapid temperature change evaluating built in material stresses. This is a worst case simulation of system power up/power down and is based on stringent military packaging requirements.

Operating Results	
Package	**100 Cycles**
QFP	0/500
PDIP	0/2006
PLCC	0/752
SOIC	1/3346

TC Failure Modes:

1 Unit of 18L SOIC (PIC16C620) failed programming a bit column.

THERMAL SHOCK

Thermal shock is the most extreme case of temperature cycling by using liquid immersion for the technique to change the device environment. This accelerates any stress related failures with the rapidly changing gradient. After the temperature stressing a constant force centrifuge test is also preformed prior to final electrical testing to further uncover any defects that may have occurred under stress.

Operating Results	
Package	**100 Cycles**
QFP	0/530
PDIP	0/690
PLCC	0/3230
SOIC	0/80

HAST (130°/85% R.H.)

Highly Accelerated Stress Testing evaluates plastic encapsulated devices' ability to withstand extreme high temperature, high humidity environments while under electrical bias. This stress is designed to create corrosion of the metal or internal device leakage if ionic contaminants are present but also may cause charge loss in memory cells.

Operating Results		
Package	**48 Hours**	**168 Hours**
QFP	0/1075	0/1068
PDIP	1/4323	0/4301
PLCC	0/1857	0/1854
SOIC	0/8168	0/8142
TSOP	0/209	0/209

HAST Failure Modes:

1 Unit of 8L SOIC (24LC32A) failed due to oxice breakdown in the charge pump.

PRODUCT RELIABILITY DATA

PICmicro MCUs						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hours	Fit Rates, 60% CL @ 55°C
ALL PICS	Dynamic Life	4/23200	0/10578	4	12,783,120	6
	Retention Bake	3/31596	0/6403	3	10,686,648	<1
ALL 90k PICS	Dynamic Life	0/14718	0/6633	0	8,044,344	1
	Retention Bake	2/20279	0/4216	2	6,948,312	<1
ALL 77k PICS	Dynamic Life	4/4589	0/2155	4	2,581,152	49
	Retention Bake	0/5161	0/1038	0	1,738,968	<1
ALL 57k PICS	Dynamic Life	0/3893	0/1790	0	2,157,624	10
	Retention Bake	1/6156	0/1149	1	1,999,368	<1
PIC16C924	Dynamic Life	0/1578	0/660	0	819,504	14
	Retention Bake	0/2157	0/390	0	689,976	<1
PIC16C622	Dynamic Life	0/2436	0/1066	0	1,304,688	9
	Retention Bake	0/3223	0/660	0	1,095,864	<1
PIC16C84A	Dynamic Life	2/760	0/380	2	446,880	167
	Retention Bake	0/0	0/0	0	0	N/A
PIC16C74A	Dynamic Life	0/1264	0/610	0	724,752	16
	Retention Bake	0/1730	0/409	0	624,200	<1
PIC16C71	Dynamic Life	0/0	0/0	0	0	N/A
	Retention Bake	0/1045	0/200	0	343,560	<1
PIC16C70	Dynamic Life	0/0	0/0	0	0	N/A
	Retention Bake	0/1178	0/215	0	378,504	<1
PIC16C64	Dynamic Life	0/0	0/0	0	0	N/A
	Retention Bake	0/0	0/0	0	0	N/A
PIC16C63/65A	Dynamic Life	0/1173	0/460	0	583,464	20
	Retention Bake	0/1567	0/299	0	514,416	<1
PIC16C62A/64A	Dynamic Life	0/1132	0/441	0	560,616	21
	Retention Bake	0/1346	0/304	0	481,488	<1
PIC16C61	Dynamic Life	0/760	0/380	0	446,880	26
	Retention Bake	0/2114	0/445	0	728,952	<1
PIC16C58A	Dynamic Life	0/2399	0/1139	0	1,359,792	12
	Retention Bake	0/2468	0/515	0	847,224	<1
PIC16C57	Dynamic Life	0/1519	0/725	0	864,192	25
	Retention Bake	0/2113	0/408	0	697,704	<1
PIC16C56	Dynamic Life	0/1959	0/948	0	1,125,432	20
	Retention Bake	0/2393	0/400	0	738,024	11
PIC16C55	Dynamic Life	0/1174	0/462	0	585,312	38
	Retention Bake	1/1649	0/304	1	532,392	32
PIC16C54	Dynamic Life	2/2310	0/1050	2	1,270,080	59
	Retention Bake	0/3048	0/630	0	1,041,264	<1
PIC16C54A	Dynamic Life	0/1787	0/950	0	1,098,216	11
	Retention Bake	0/2516	0/530	0	867,888	<1

PICmicro MCUs						
		Operating Hours				
Device	**Operation**	**168**	**1008**	**Fails**	**Device Hours**	**Fit Rates, 60% CL @ 55°C**
PIC17C42	Dynamic Life	0/0	0/0	0	0	N/A
	Retention Bake	0/0	0/0	0	0	N/A
PIC17C44	Dynamic Life	0/2025	0/810	0	1,020,600	12
	Retention Bake	2/1932	0/368	2	633,696	<1
PIC12C508	Dynamic Life	0/924	0/497	0	572,712	21
	Retention Bake	0/1117	0/326	0	461,496	<1
Failure Modes:	Dynamic Life	2 units of PIC16C84A failed to single bit charge loss 2 units of PIC16C54 failed to verify programming				
	Retention Bake	2 units of PIC17C44 failed due to marginal programming 1 unit of PIC16C55 failed due to single bit charge loss				

Serial EEPROMs						
		Operating Hours				
Device	Operation	168 Hrs.	1008 Hrs.	Fails	Device Hrs.	Fit Rates, 60% CL @ 55°C
ALL SERIAL	Dynamic Life	1/32806	1/13440	2	16,801,008	4
EEPROMS	Retention Bake	37/36007	0/7300	37	12,181,176	<1
57k SERIAL	Dynamic Life	0/5074	0/2080	0	2,599,632	8
EEPROMS	Retention Bake	1/6485	0/1300	1	2,181,480	<1
77k SERIAL	Dynamic Life	1/27732	1/11360	2	14,201,376	5
EEPROMS	Retention Bake	36/29522	0/6000	36	9,999,696	<1
24C01A/02A	Dynamic Life	0/3134	0/1280	0	1,601,712	14
	Retention Bake	0/4052	0/800	0	1,352,736	<1
24C04	Dynamic Life	0/1940	0/800	0	997,920	22
	Retention Bake	1/2433	0/500	1	828,744	<1
93C06/46	Dynamic Life	0/0	0/0	0	0	N/A
	Retention Bake	0/0	0/0	0	0	N/A
93LC46	Dynamic Life	0/2348	0/960	0	1,200,864	18
	Retention Bake	0/3027	0/600	0	1,012,536	<1
93LC56/66	Dynamic Life	0/3522	0/1440	0	1,801,296	12
	Retention Bake	0/3562	0/700	0	1,186,416	<1
93LCS56/66	Dynamic Life	0/0	0/0	0	0	N/A
	Retention Bake	0/0	0/0	0	0	N/A
24LC01B	Dynamic Life	0/3107	0/1280	0	1,597,176	14
	Retention Bake	0/3008	0/600	0	1,009,344	<1
24LC02B	Dynamic Life	0/3532	0/1440	0	1,802,976	12
	Retention Bake	0/3464	0/700	0	1,169,952	<1
24LC04B	Dynamic Life	1/3116	0/1280	1	1,598,688	30
	Retention Bake	0/3529	0/700	0	1,180,872	<1
24LC08B	Dynamic Life	0/1950	0/800	0	999,600	22
	Retention Bake	0/2475	0/500	0	835,800	<1
24LC16B	Dynamic Life	0/1577	0/640	0	802,536	27
	Retention Bake	0/1988	0/400	0	669,984	<1
24LC32A	Dynamic Life	0/2316	1/960	1	1,195,488	41
	Retention Bake	1/1960	0/500	1	749,280	<1
24LC65	Dynamic Life	0/2725	0/1120	0	1,398,600	16
	Retention Bake	35/3534	0/700	35	1,181,712	2
24LCS21	Dynamic Life	0/2747	0/1120	0	1,402,296	16
	Retention Bake	0/2481	0/500	0	836,808	<1
24LCS52	Dynamic Life	0/384	0/160	0	198,912	111
	Retention Bake	0/494	0/100	0	166,992	<1
25LC08/16/162	Dynamic Life	0/408	0/160	0	202,944	108
	Retention Bake	0/0	0/0	0	0	N/A

Failure Modes:	Dynamic Life	1 unit of 24LC04B failed due to a column defect 1 unit of 24LC32A failed programming
	Retention Bake	35 units of 24LC65 failed due to single bit charge loss 1 unit of 24LC32A failed due to single bit charge loss 1 unit of 24LC04A failed due to single bit charge loss

Parallel EEPROMs						
		Operating Hours				
Device	Operation	168 Hrs.	1008 Hrs.	Fails	Device Hrs.	Fit Rates, 60% CL @ 55°C
ALL PARALLEL	Dynamic Life	0/1989	0/800	0	1,006,152	22
EEPROMS	Retention Bake	0/1958	0/400	0	664,944	<1
28C64	Dynamic Life	0/1989	0/800	0	1,006,152	22
	Retention Bake	0/1958	0/400	0	664,944	<1
Failure Modes:	Dynamic Life	N/A				
	Retention Bake	N/A				

EPROMS						
		Operating Hours				
Device	Operation	168	1008	Fails	Device Hrs.	Fit Rates, 60% CL @ 55°C
ALL EPROMS	Dynamic Life	0/2818	0/1120	0	1,414,224	14
	Retention Bake	5/3186	0/702	5	1,124,928	<1
ALL 90k EPROMS	Dynamic Life	0/423	0/160	0	205,464	57
	Retention Bake	3/496	0/100	3	167,328	2
ALL 77k EPROMS	Dynamic Life	0/2395	0/960	0	1,208,760	18
	Retention Bake	2/2690	0/602	2	957,600	<1
27C256	Dynamic Life	0/2395	0/960	0	1,208,760	18
	Retention Bake	2/2690	0/602	2	957,600	<1
27C512A	Dynamic Life	0/423	0/160	0	205,464	57
	Retention Bake	3/496	0/100	3	167,328	2
Failure Modes:	Dynamic Life	N/A				
	Retention Bake	2 units of 27C256 failed due to single bit charge loss 3 units of 27C512A failed due to single/multiple bit charge loss				

NOTES:

EEPROM Endurance

INTRODUCTION

A unique feature of non-volatile memory devices is the dual requirement both to change and to maintain data states. It is this combination of requirements that provides the contrasting nature that defines the complexities involved in change and maintaining such change. Anything that enhances the physics to allow a data state change in contrast degrades the retention of that change. It also holds that any retention enhancements inhibit the data changing capabilities. A balance must be struck between the combinations to achieve the field requirements of customer applications.

Erase/Write cycling has many variables which greatly effect the lifetime of the device. To accurately make comparisons between specifications and the actual requirements, or any other comparisons, these factors must be well understood and taken into account.

TECHNOLOGY OVERVIEW

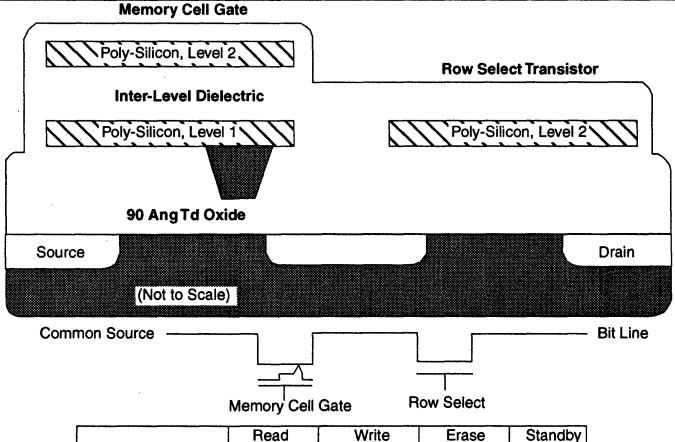
Silicon Technology

The basic technology employed by Microchip Technology for EEPROM's is a FLOTOX structure as drawn below. This is a an industry standard architecture base which has been enhanced by Microchip to provide improvements to the quality and reliability of the devices produced.

Circuit Technology

These cells are then structured in either an 8 or 16 bit word organization for data storage with between 32 words (256 byte device) and 8K words (64K device) using standard binary decoding schemes found industry wide on memory devices. Data can then be transmitted either into the device for storage or read from the device when needed along a single DATA pin, (I^2C bus) or a dual Data in/Data out configuration (3-wire bus). The device has no restriction on the number of read cycles that can be processed per byte without damage but the storage process does have finite limitations.

Currently two different schemes of error correction are being utilized on Microchip EEPROM's. The 24CXX, 93CXX, 85CXX, 59CXX and 28CXX device types utilize a modified Hamming code redundancy scheme with four parity bits per eight bit byte. This has been the industry standard correction scheme for enhancement of cycling lifetimes by eliminating single bit per word errors. An alternative approach has been developed utilizing an AND cell concept of redundant memory cells. This further enhances the write/erase lifetime over the Hamming code and has been implemented on the 24LCXX and 93LCXX circuits.



	Read	Write	Erase	Standby
Bit Line	1.6 volts	18.0 volts	0.0 volts	0.0 volts
Row Select Gate	5.0 volts	20.0 volts	20.0 volts	0.0 volts
Memory Cell Gate	5.0 volts	0.0 volts	20.0 volts	0.0 volts
Common Source	0.0 volts	Float	0.0 volts	0.0 volts

Reliability Endurance

The endurance failure rate curve for the Microchip devices is presented in the standard form for this curve from EEPROM FLOTOX manufacturers. Microchip does write/erase cycle all EEPROM devices prior to shipment to remove the infant mortality endurance failures from the population. This characteristic curve, with two failure increase sections, is shown below for reference. Both sections have single bits failing as the dominant mechanism.

The first of the failure increase sections is usually related to breakdown of oxides from latent oxide defects that are inherent to any process. These oxides have reached a time dependent dielectric breakdown condition and permanently rupture. This generally characterizes the first 200K write/erase cycles under any conditions. The second curve is the standard trap up of electrons within the tunnel dielectric which closes the write/erase threshold window until the device no longer adequately programs or erases.

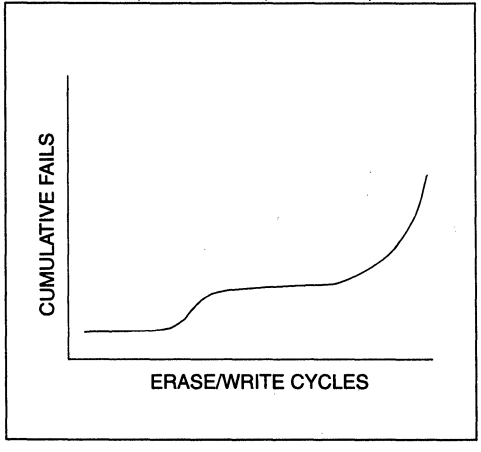
This curve depends on multiple parameters, but the trap up failure increase portion often does not occur until ten million write/erase cycles or greater.

The first failures from endurance cycling and the long term end of life failures are due to different mechanisms.

The failures from 200K to 500K cycles have historically been attributed to "fast trap up" around the industry. Analysis at Microchip has shown that these failures are not actually trap up but oxide breakdown in nature. They most often manifest themselves as single bit charge loss or charge pump failure, both due to the formation of a conductive path within the gate oxide layer.

These oxide breakdown failures can be related to defects of three types of categories.

Type 1 is a residual chemical stain left behind on the wafer after processing due to an inadequate rinse. These are very difficult to physically detect and are best inferred from a pattern of bits (a bit cluster) that fail.



Type 2 is a physical defect which can be found upon microscopic or SEM analysis resulting in the failure. This is most often a particle, polysilicon nodule or metal short.

Type 3 is a physical defect with low activation energy that cannot be detected until end of life evaluation because of it's change in state (subsequent consumption) during latter processing steps.

The end of life mechanism is called "oxide trap up". This is where the tunnel dielectric oxide layer loses it's ability to pass charge and begins to retain some portion of the charge that it passes to the floating gate. These excess electrons within the oxide act as a charge shield, resulting in insufficient charge movement while significantly raising the voltage required to continue transmitting a constant charge level. Since the programming voltage is not adjustable this results in less charge movement for either the write or erase state. These states, whether charged negatively or charged positively, approach a central point and become indistinguishable to the detection circuitry of the device. This results in a failure to read the correct pattern, (impossible to distinguish between a programmed one and a programmed zero) beginning with the extreme voltage values of the operating specification.

Microchip strives to offer the lowest failure rate for both early life and wearout fails. Early fails in Microchip products are in the PPM range, and wearout does not set in most applications until after ten million cycles.

MEASUREMENT OF CYCLING

Microchip Technology defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. All units shipped from Microchip have Error Correction circuitry engaged for customer use. Error Correction amends any one error per byte for Hamming and one error per bit for AND cell which allows the device to read correct data. An endurance failure is determined when any one bit is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices, (Microchip currently uses a cumulative 2.5 percent), have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from every wafer lot of material manufactured for shipment. Samples are subjected to byte cycling of a checkerboard pattern at 85°C in rapid succession to the specified number of guaranteed cycles. These units then are baked in both checkerboard and inverse checkerboard forms and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a monthly basis and reviewed to measure both results of continuous improvement programs and conformance against the device standards.

ENDURANCE VARIABLES

a) **Temperature:** Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b) **Delay between cycles:** This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies this does have a positive effect, however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c) **Write timing:** The decrease in write time to the device correlates directly with write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.
Please note that the rise time of the signal, which the customer does not have control over is also a dominant effect.

d) **Vcc voltage:** The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.

Lower voltages this has the opposite effects on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at Vcc=5.5 Volts.

e) **Pattern effect:** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a non-volatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric. (Please note that to write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to it's original state!) Conversely writing a one from a one then passes no charge through the cell and therefore does no damage to the cell but does stress the charge pump.

From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles that an all zero patterned device would last. In general this appears to be approximately correct but does negiect the charge pump and other peripheral wearout mechanisms.

f) **Cycling mode:** Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field. A second technique exists called block mode which exercises all the cells of the array simultaneously. The lifetime expectations are approximately ten times as long for these block cycled devices as equivalently cycled byte cycled circuits based on experimental findings. This effect has been traced back to the rise time of the programming signal at the memory cell. The faster this voltage rise occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate. Page mode offers the best balance of endurance and write cycle times.

g) **Array Size:** This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are therefore not directly related to array size.

FIELD RESULTS

Microchip Technology, after significant experimentation, has developed a model of the Endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called Total Endurance™. This allows the customer to bypass confusing information and conditions other than their application and directly predict the failures seen in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system. Results for a typical application (obtained from the Total Endurance model are listed at right for reference).

Device	Application Life	Cumulative Percent
24C02A	10 years	154 PPM
24C04A	10 years	172 PPM
93C46	10 years	136 PPM
24LC02B	10 years	108 PPM
24LC04B	10 years	131 PPM
24LC16B	10 years	668 PPM
93LC46B	10 years	374 PPM
93LC56B	10 years	108 PPM
24LC65HE	10 years	131 PPM
24LC65SE	10 years	4061 PPM

Typical conditions used are 25°C, Byte mode operation with 24 cycles per day, V_{CC} = 4.5 Volts with a random pattern writing one quarter of the array at each occasion. The failure rates quoted are the expected failure rate at the end of the application life using an unlimited number of read cycles. For more information on Endurance, it is recommended that the user obtain a copy of Total Endurance.

MICROCHIP

SECTION 11
PACKAGING

Commercial/Industrial Outlines and Parameters 11-1
Product Tape and Reel Specifications 11-59
Overview of Microchip Die/Wafer Support 11-61

PACKAGING

Commercial/Industrial Outlines and Parameters

PART NUMBER SUFFIX DESIGNATIONS:

XXXXXXXXXX	-XX	X	/XX	XXX
Device Type / Options	Speed or Frequency	Temperature	Package	Pattern

Examples:

24LC65-I/SN
PIC16C54-RCI/SO

Memory Products

Device Type
C = CMOS
FC = 5.0, 1 MHz
LC = Low Power CMOS
AA = 1.8V
LV = Low Voltage EPROM
HC = High Speed EPROM
LCS = Low Power Security

Options
F = twc = 200 µs (28CXX devices)
X = Rotated pinout (93LCXX devices)
T = Tape and Reel

Speed (Parallel Devices Only)
55 = 55 ns
70 = 70 ns
90 = 90 ns
10 = 100 ns
12 = 120 ns
15 = 150 ns
17 = 170 ns
20 = 200 ns
25 = 250 ns
30 = 300 ns

Temperature
Blank = 0°C to +70°C
I = -40°C to +85°C
E = -40°C to +125°C

Package
L = Plastic Leaded Chip Carrier
P = Plastic Dual In-Line Package
S = Die in Waffle Pack
W = Die in Wafer Form
MR = 8-Contact Chip-On-Board 35 mm Tape
MT = 8-Contact Sigulated Chip-On-Board
OT = 5-Lead Small Outline Transistor (SOT)
SL = 14-Lead Small Outline - 150 mil
SM = 8-Lead Small Outline - 208 mil
SN = 8-Lead Small Outline - 150 mil
SO = Small Outline - 300 mil
SS = Shrink Small Outline Package - 209 mil
ST = Thin Shrink Small Outline Package - 4.4 mm
TO = 3-Lead Plastic Transistor Outline
TS = Thin Small Outline - 8mm x 20mm
TT = 3-Lead Plastic Small Outline Transistor
VS = Very Small Outline - 8mm x 13.4mm
WF = Sawed Wafer on Frame

Pattern
QTP, SQTP, ROM Code or Special Requirements

Mircocontroller Products

Device Type
C = CMOS
LC = Low Power CMOS
CR = CMOS ROM
LCR = Low Power CMOS ROM
LV = Low Voltage
F = Flash Program Memory
FR = Flex ROM

Options
T = Tape and Reel

Crystal Frequency Designator
LP = Low Power Crystal
RC = Resistor Capacitor
XT = Standard Crystal/Resonator
HS = High Speed Crystal
02 = 2MHz
04 = 200kHz (LP mode)
04 = 4 MHz (XT & RC mode)
10 = 10 MHz
20 = 20 MHz
25 = 25 MHz
33 = 33 MHz

Temperature
Blank = 0°C to +70°C
I = -40°C to +85°C
E = -40°C to +125°C

Package
L = Plastic Leaded Chip Carrier (PLCC)
P = Plastic Dual In-Line Package (PDIP)
S = Die in Waffle Pack
W = Die in Wafer Form
CB = Chip On Board (COB)
CL = 68-Lead Ceramic Quad (CERQUAD) with Window
JW = Ceramic Dual In-Line Package (CERDIP) with Window
PQ = Plastic Metric Quad Flat Pack (MQFP)
PT = Thin Quad Flatpack (TQFP)
SM = 8-Lead Small Outline - 208 mil
SO = Small Outline (SOIC) - 300 mil
SP = Skinny PDIP
SS = Shrink Small Outline Package (SSOP) - 209 mil
TS = Thin Small Outline (TSOP) - 8mm x 20mm

Pattern
QTP, SQTP, ROM Code or Special Requirements

Packaging Diagrams and Parameters

CERAMIC SIDE BRAZED DUAL IN-LINE FAMILY

K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil 11-4
K04-083 28-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil 11-5

CERAMIC DUAL IN-LINE (CERDIP) FAMILY

K04-010 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil 11-6
K04-080 28-Lead Ceramic Dual In-line with Window (JW) – 300 mil 11-7
K04-013 28-Lead Ceramic Dual In-line with Window (JW) – 600 mil 11-8
K04-014 40-Lead Ceramic Dual In-line with Window (JW) – 600 mil 11-9

CERAMIC CHIP CARRIER FAMILY

K04-097 68-Lead Ceramic Leaded (CL) Chip Carrier with Window – Square 11-10

8-CONTACT SINGULATED CHIP-ON-BOARD

K04-099 8-Contact Singulated Chip-On-Board (MT) 11-11
K04-100 8-Contact Chip-On-Board 35 mm Tape (MR) 11-12

SMALL OUTLINE TRANSISTOR

K04-101 3-Lead Plastic Transistor Outline (TO) 11-13
K04-104 3-Lead Plastic Small Outline Transistor (TT) 11-14
K04-091 5-Lead Plastic Small Outline Transistor (OT) 11-15

PLASTIC DUAL IN-LINE (PDIP) FAMILY

K04-018 8-Lead Plastic Dual In-line (P) – 300 mil 11-16
K04-005 14-Lead Plastic Dual In-line (P) – 300 mil 11-17
K04-017 16-Lead Plastic Dual In-line (P) – 300 mil 11-18
K04-007 18-Lead Plastic Dual In-line (P) – 300 mil 11-19
K04-019 20-Lead Plastic Dual In-line (P) – 300 mil 11-20
K04-008 22-Lead Plastic Dual In-line (P) – 400 mil 11-21
K04-081 24-Lead Plastic Dual In-line (P) – 600 mil 11-22
K04-043 24-Lead Skinny Plastic Dual In-line (SP) – 300 mil 11-23
K04-070 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil 11-24
K04-079 28-Lead Plastic Dual In-line (P) – 600 mil 11-25
K04-016 40-Lead Plastic Dual In-line (P) – 600 mil 11-26
K04-022 48-Lead Plastic Dual In-line (P) – 600 mil 11-27
K04-090 64-Lead Shrink Plastic Dual In-line (SP) – 750 mil 11-28

PLASTIC LEADED CHIP CARRIER (PLCC) FAMILY

K04-064 20-Lead Plastic Leaded Chip Carrier (L) – Square 11-29
K04-026 28-Lead Plastic Leaded Chip Carrier (L) – Square 11-30
K04-023 32-Lead Plastic Leaded Chip Carrier (L) – Rectangle 11-31
K04-048 44-Lead Plastic Leaded Chip Carrier (L) – Square 11-32
K04-049 68-Lead Plastic Leaded Chip Carrier (L) – Square 11-33
K04-093 84-Lead Plastic Leaded Chip Carrier (L) – Square 11-34

Packaging Diagrams and Parameters

PLASTIC SMALL OUTLINE (SOIC) FAMILY

K04-057 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil 11-35
K04-056 8-Lead Plastic Small Outline (SM) – Medium, 208 mil 11-36
K04-065 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil 11-37
K04-102 16-Lead Plastic Small Outline (SO) – Wide, 300 mil Body 11-38
K04-051 18-Lead Plastic Small Outline (SO) – Wide, 300 mil 11-39
K04-094 20-Lead Plastic Small Outline (SO) – Wide, 300 mil 11-40
K04-098 24-Lead Plastic Small Outline (SO) – Wide, 300 mil 11-41
K04-052 28-Lead Plastic Small Outline (SO) – Wide, 300 mil 11-42
K04-066 28-Lead Plastic Small Outline (SO) – Wide, 330 mil 11-43

PLASTIC SHRINK SMALL OUTLINE (SSOP) FAMILY

K04-103 14-Lead Plastic Shrink Small Outline (SS) – 5.30 mm 11-44
K04-072 20-Lead Plastic Shrink Small Outine (SS) – 5.30 mm 11-45
K04-073 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm 11-46

PLASTIC THIN SHRINK SMALL OUTLINE (TSSOP) FAMILY

K04-086 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm 11-47
K04-087 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm 11-48
K04-088 20-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm 11-49
K04-089 28-Lead Thin Shrink Small Outline (ST) – 4.4 mm 11-50

PLASTIC THIN SMALL OUTLINE (TSOP) AND VERY SMALL OUTLINE (VSOP) FAMILY

K04-067 28-Lead Plastic Thin Small Outline (TS) – 8 x 20 mm 11-51
K04-068 32-Lead Plastic Thin Small Outline (TS) – 8 x 20 mm 11-52
K04-075 28-Lead Plastic Very Small Outline (VS) – 8 x 13.4 mm 11-53

PLASTIC QUAD FLATPACK (QFP) FAMILY

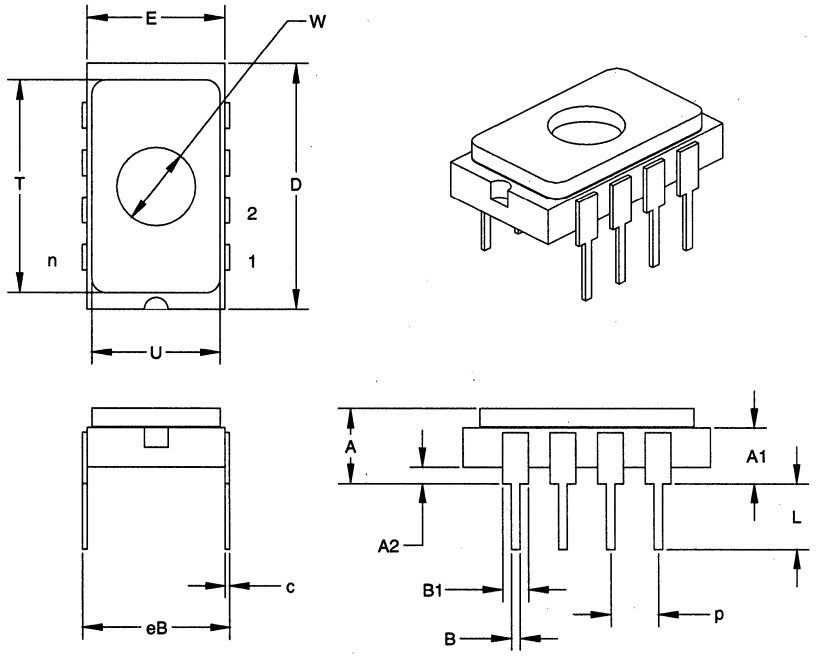
K04-071 44-Lead Plastic Quad Flatpack (PQ)
10x10x2 mm Body, 1.6/0.15 mm Lead Form 11-54

PLASTIC THIN QUAD FLATPACK (TQFP) FAMILY

K04-076 44-Lead Plastic Thin Quad Flatpack (PT)
10x10x1 mm Body, 1.0/0.1 mm Lead Form 11-55
K04-085 64-Lead Plastic Thin Quad Flatpack (PT)
10x10x1 mm Body, 1.0/0.1 mm Lead Form 11-56
K04-092 80-Lead Plastic Thin Quad Flatpack (PT)
12x12x1 mm Body, 1.0/0.1 mm Lead Form 11-57

Packaging Diagrams and Parameters

Package Type: K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil

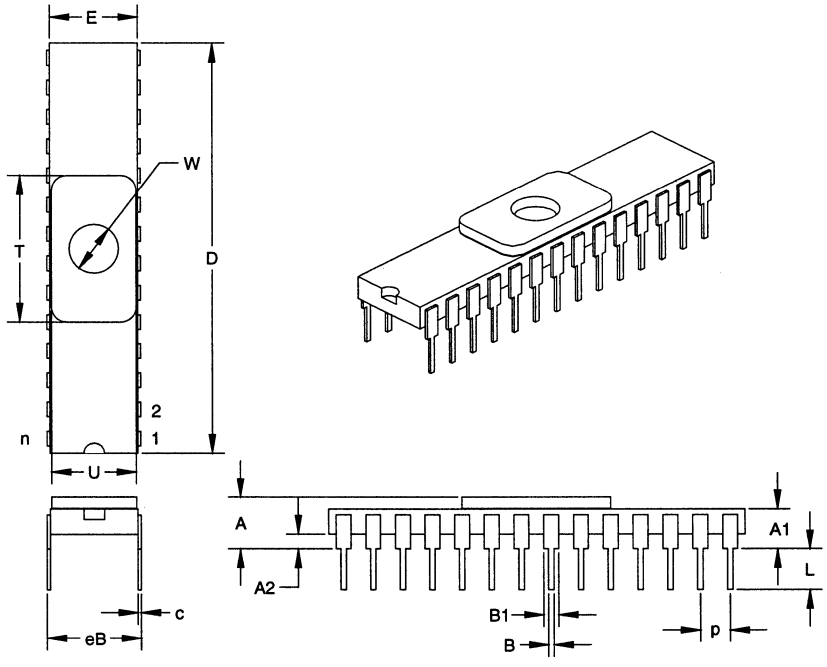


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.145	0.165	0.185	3.68	4.19	4.70
Top of Body to Seating Plane	A1	0.103	0.123	0.143	2.62	3.12	3.63
Base to Seating Plane	A2	0.025	0.035	0.045	0.64	0.89	1.14
Tip to Seating Plane	L	0.130	0.140	0.150	3.30	3.56	3.81
Package Length	D	0.510	0.520	0.530	12.95	13.21	13.46
Package Width	E	0.280	0.290	0.300	7.11	7.37	7.62
Overall Row Spacing	eB	0.310	0.338	0.365	7.87	8.57	9.27
Window Diameter	W	0.161	0.166	0.171	4.09	4.22	4.34
Lid Length	T	0.440	0.450	0.460	11.18	11.43	11.68
Lid Width	U	0.260	0.270	0.280	6.60	6.86	7.11

* Controlling Parameter.
JEDEC equivalent: MS-015 AH

Packaging Diagrams and Parameters

Package Type: KC4-083 28-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil

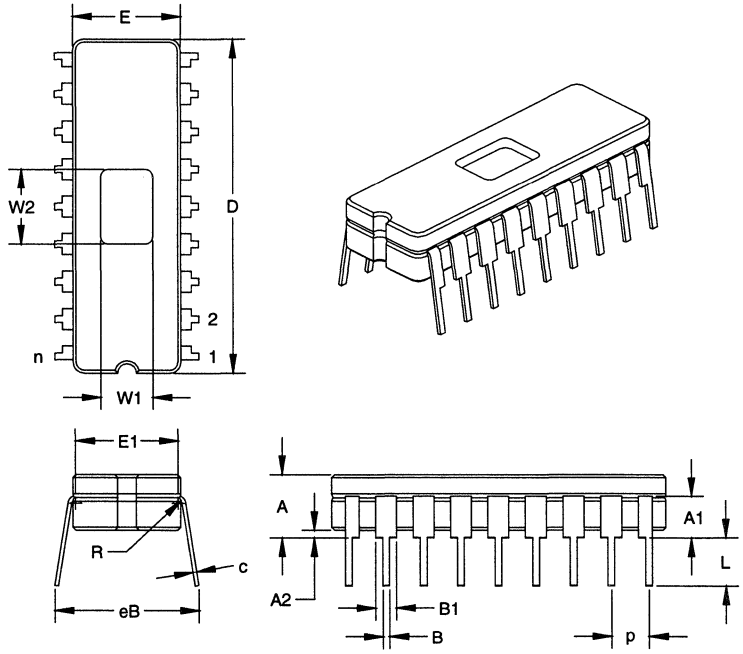


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1	0.048	0.050	0.052	1.22	1.27	1.32
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.155	0.177	0.198	3.94	4.48	5.03
Top of Body to Seating Plane	A1	0.115	0.135	0.155	2.91	3.42	3.92
Base to Seating Plane	A2	0.040	0.050	0.060	1.02	1.27	1.52
Tip to Seating Plane	L	0.130	0.140	0.150	3.30	3.56	3.81
Package Length	D	1.386	1.400	1.414	35.20	35.56	35.92
Package Width	E	0.280	0.290	0.300	7.11	7.37	7.62
Overall Row Spacing	eB	0.310	0.316	0.322	7.87	8.03	8.18
Window Diameter	W	0.161	0.166	0.171	4.09	4.22	4.34
Lid Length	T	0.490	0.500	0.510	12.45	12.70	12.95
Lid Width	U	0.275	0.285	0.295	6.99	7.24	7.49

* Controlling Parameter.
JEDEC equivalent: MS-015 AA

Packaging Diagrams and Parameters

Package Type: K04-010 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil

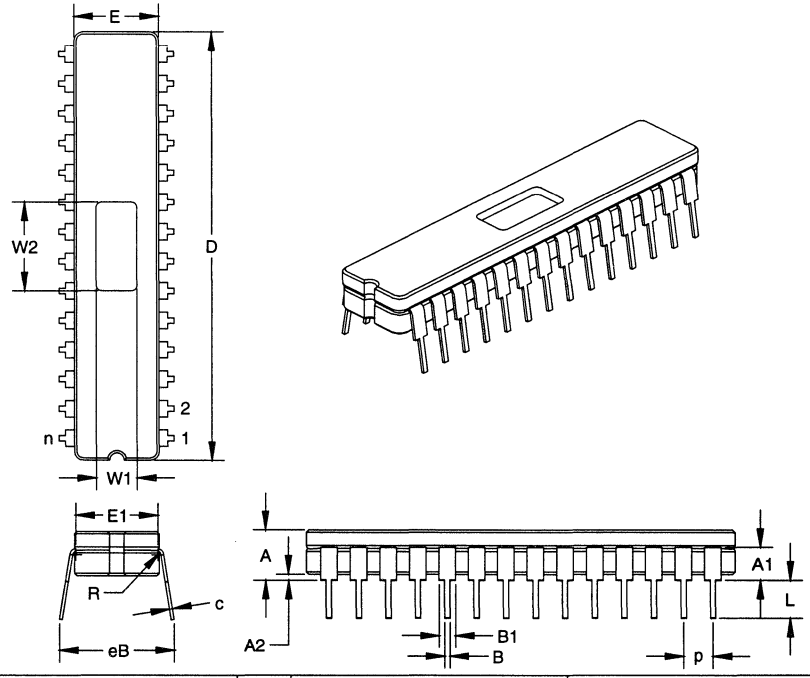


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		18			18	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.019	0.021	0.41	0.47	0.53
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Shoulder Radius	R	0.010	0.013	0.015	0.25	0.32	0.38
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.175	0.183	0.190	4.45	4.64	4.83
Top of Lead to Seating Plane	A1	0.091	0.111	0.131	2.31	2.82	3.33
Base to Seating Plane	A2	0.015	0.023	0.030	0.00	0.57	0.76
Tip to Seating Plane	L	0.125	0.138	0.150	3.18	3.49	3.81
Package Length	D	0.880	0.900	0.920	22.35	22.86	23.37
Package Width	E	0.285	0.298	0.310	7.24	7.56	7.87
Radius to Radius Width	E1	0.255	0.270	0.285	6.48	6.86	7.24
Overall Row Spacing	eB	0.345	0.385	0.425	8.76	9.78	10.80
Window Width	W1	0.130	0.140	0.150	0.13	0.14	0.15
Window Length	W2	0.190	0.200	0.210	0.19	0.2	0.21

* Controlling Parameter.
JEDEC equivalent: MO-036 AE

Packaging Diagrams and Parameters

Package Type: K04-080 28-Lead Ceramic Dual In-line with Window (JW) – 300 mil



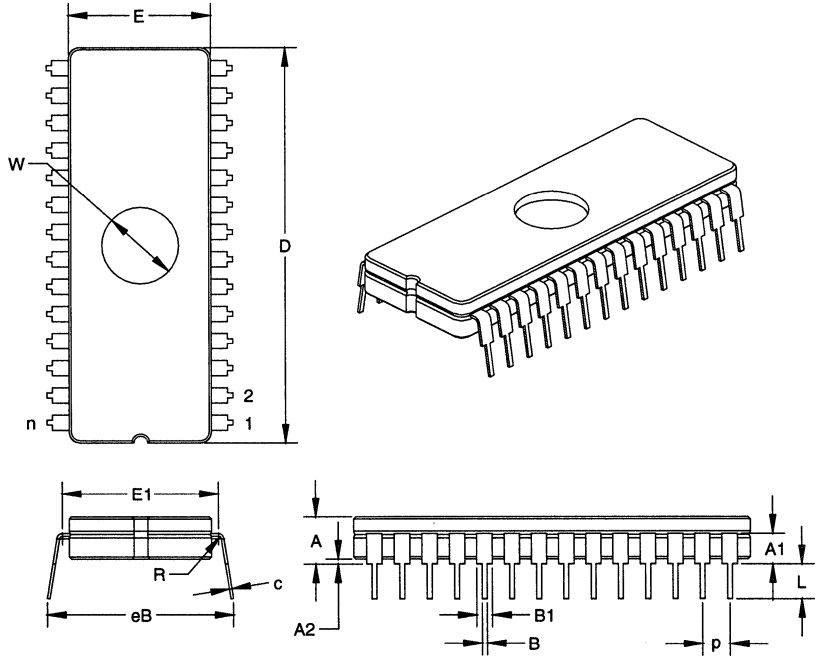
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.019	0.021	0.41	0.47	0.53
Upper Lead Width	B1	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Radius	R	0.010	0.013	0.015	0.25	0.32	0.38
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.170	0.183	0.195	4.32	4.64	4.95
Top of Lead to Seating Plane	A1	0.107	0.125	0.143	2.72	3.18	3.63
Base to Seating Plane	A2	0.015	0.023	0.030	0.00	0.57	0.76
Tip to Seating Plane	L	0.135	0.140	0.145	3.43	3.56	3.68
Package Length	D	1.430	1.458	1.485	36.32	37.02	37.72
Package Width	E	0.285	0.290	0.295	7.24	7.37	7.49
Radius to Radius Width	E1	0.255	0.270	0.285	6.48	6.86	7.24
Overall Row Spacing	eB	0.345	0.385	0.425	8.76	9.78	10.80
Window Width	W1	0.130	0.140	0.150	0.13	0.14	0.15
Window Length	W2	0.290	0.300	0.310	0.29	0.3	0.31

* Controlling Parameter.

JEDEC equivalent: MO-058 AB

Packaging Diagrams and Parameters

Package Type: K04-013 28-Lead Ceramic Dual In-line with Window (JW) – 600 mil



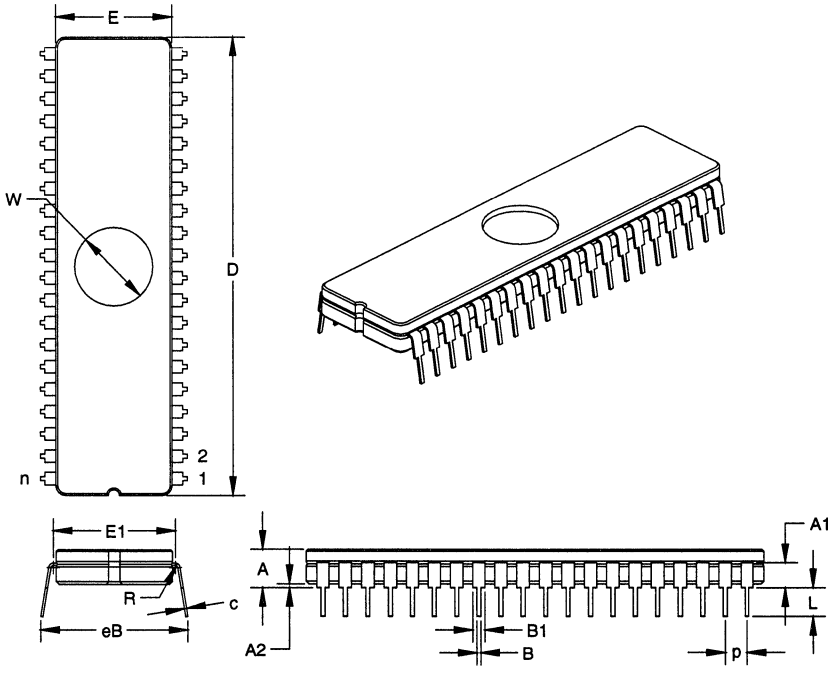
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		28			28	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.019	0.021	0.41	0.47	0.53
Upper Lead Width	B1	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.170	0.185	0.200	4.32	4.70	5.08
Top of Lead to Seating Plane	A1	0.110	0.128	0.146	2.78	3.24	3.70
Base to Seating Plane	A2	0.015	0.038	0.060	0.00	0.95	1.52
Tip to Seating Plane	L	0.125	0.138	0.150	3.18	3.49	3.81
Package Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Package Width	E	0.514	0.520	0.526	13.06	13.21	13.36
Radius to Radius Width	E1	0.560	0.580	0.600	14.22	14.73	15.24
Overall Row Spacing	eB	0.610	0.660	0.710	15.49	16.76	18.03
Window Diameter	W	0.270	0.280	0.290	6.86	7.11	7.37

* Controlling Parameter.

JEDEC equivalent: MO-103 AB

Packaging Diagrams and Parameters

Package Type: K04-014 40-Lead Ceramic Dual In-line with Window (JW) – 600 mil



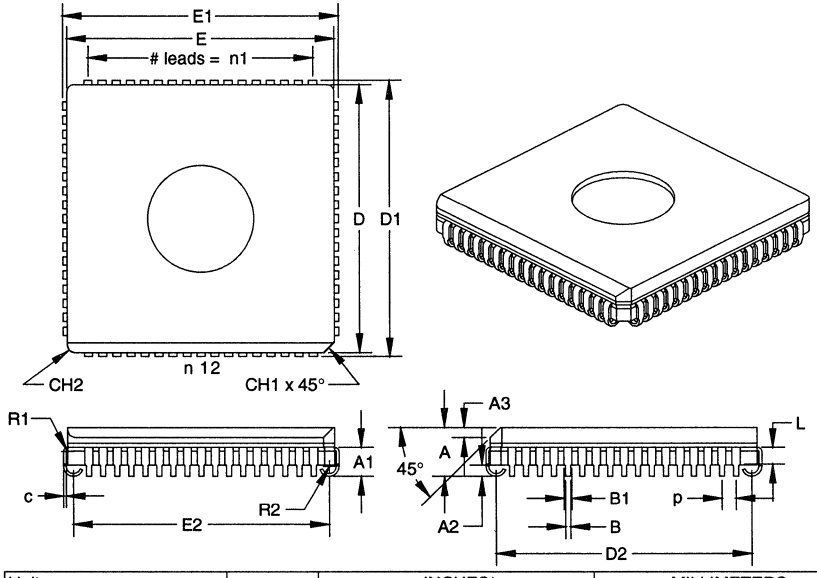
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		40			40	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.020	0.023	0.41	0.50	0.58
Upper Lead Width	B1	0.050	0.053	0.055	1.27	1.33	1.40
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.011	0.014	0.20	0.28	0.36
Top to Seating Plane	A	0.190	0.205	0.220	4.83	5.21	5.59
Top of Lead to Seating Plane	A1	0.117	0.135	0.153	2.97	3.43	3.89
Base to Seating Plane	A2	0.030	0.045	0.060	0.00	1.14	1.52
Tip to Seating Plane	L	0.135	0.140	0.145	3.43	3.56	3.68
Package Length	D	2.040	2.050	2.060	51.82	52.07	52.32
Package Width	E	0.514	0.520	0.526	13.06	13.21	13.36
Radius to Radius Width	E1	0.560	0.580	0.600	14.22	14.73	15.24
Overall Row Spacing	eB	0.610	0.660	0.710	15.49	16.76	18.03
Window Diameter	W	0.340	0.350	0.360	8.64	8.89	9.14

* Controlling Parameter.

JEDEC equivalent: MO-103 AC

Packaging Diagrams and Parameters

Package Type: K04-097 68-Lead Ceramic Leaded (CL) Chip Carrier with Window – Square



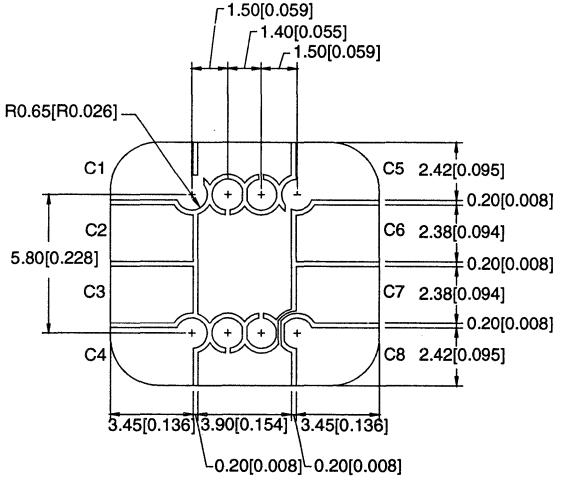
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		68			68	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.165	0.175	0.185	4.19	4.45	4.70
Shoulder Height	A1	0.090	0.105	0.120	2.29	2.67	3.05
Standoff	A2	0.03	0.040	0.050	0.76	1.02	1.27
Side 1 Chamfer Dim.	A3	0.030	0.035	0.040	0.76	0.89	1.02
Corner Chamfer (1)	CH1	0.030	0.040	0.050	0.76	1.02	1.27
Corner Chamfer(other)	CH2	0.020	0.025	0.030	0.51	0.64	0.76
Overall Pack. Width	E1	0.983	0.988	0.993	24.97	25.10	25.22
Overall Pack. Length	D1	0.983	0.988	0.993	24.97	25.10	25.22
Ceramic Pack. Width	E	0.942	0.950	0.958	23.93	24.13	24.33
Ceramic Pack. Length	D	0.942	0.950	0.958	23.93	24.13	24.33
Footprint Width	E2	0.890	0.910	0.930	22.61	23.11	23.62
Footprint Length	D2	0.890	0.910	0.930	22.61	23.11	23.62
Pins along Width	n1		17			17	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1	0.026	0.029	0.031	0.66	0.72	0.79
Lower Lead Width	B	0.015	0.018	0.021	0.38	0.46	0.53
Upper Lead Length	L	0.045	0.050	0.055	1.14	1.27	1.40
Shoulder Inside Radius	R1	0.003	0.005	0.010	0.08	0.13	0.25
J-Bend Inside Radius	R2	0.020	0.030	0.040	0.51	0.76	1.02
Window Diameter	W	0.370	0.380	0.390	9.40	9.65	9.91

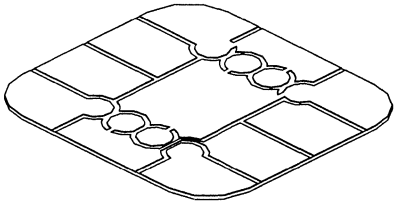
* Controlling Parameter.

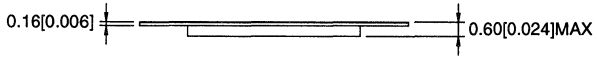
Packaging Diagrams and Parameters

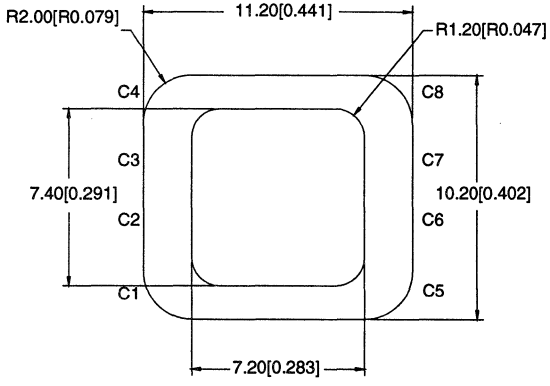
Package Type: K04-099 8-Contact Singulated Chip-On-Board (MT)

Controlling units: millimeters; [Reference units: inches]
Tolerances: ±0.13[0.005]









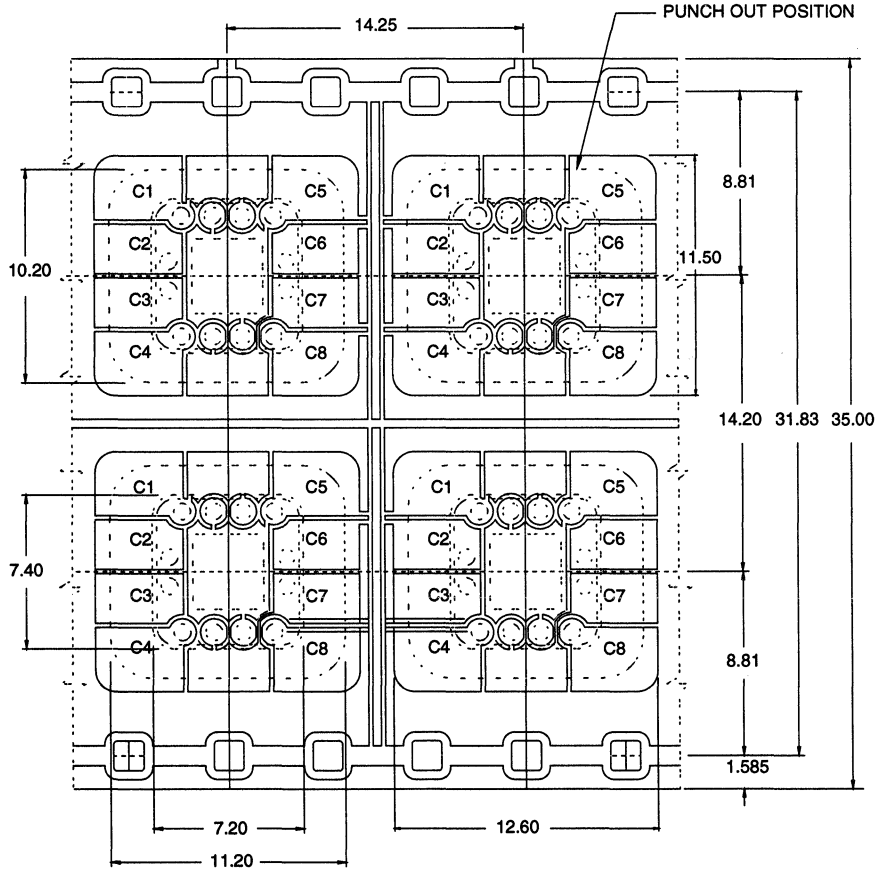
11

Packaging

Packaging Diagrams and Parameters

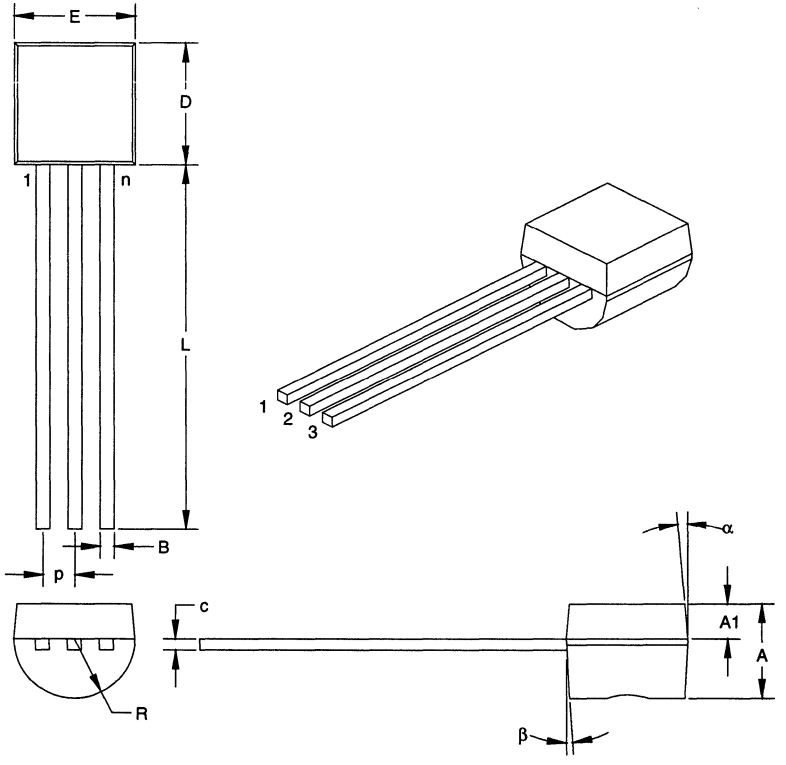
Package Type: K04-100 8-Contact Chip-On-Board 35 mm Tape (MR)

Controlling units: millimeters
Tolerances: ± 0.13[0.005]



Packaging Diagrams and Parameters

Package Type: K04-101 3-Lead Plastic Transistor Outline (TO)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		3			3	
Pitch	p		0.100			2.54	
Bottom to Package Flat	A	0.130	0.143	0.155	3.30	3.62	3.94
Top of Lead to Package Flat	A1	0.045	0.053	0.060	1.14	1.33	1.52
Molded Package Length	D‡	0.170	0.183	0.195	4.32	4.64	4.95
Molded Package Width	E‡	0.175	0.185	0.195	4.45	4.70	4.95
Molded Package Radius	R	0.085	0.090	0.095	2.16	2.29	2.41
Lead Width	B†	0.016	0.019	0.022	0.41	0.48	0.56
Lead Thickness	c	0.014	0.017	0.020	0.36	0.43	0.51
Tip to Seating Plane	L	0.500	0.555	0.610	12.70	14.10	15.49
Mold Draft Angle Top	α	4	5	6	4	5	6
Mold Draft Angle Bottom	β	2	3	4	2	3	4

* Controlling Parameter.

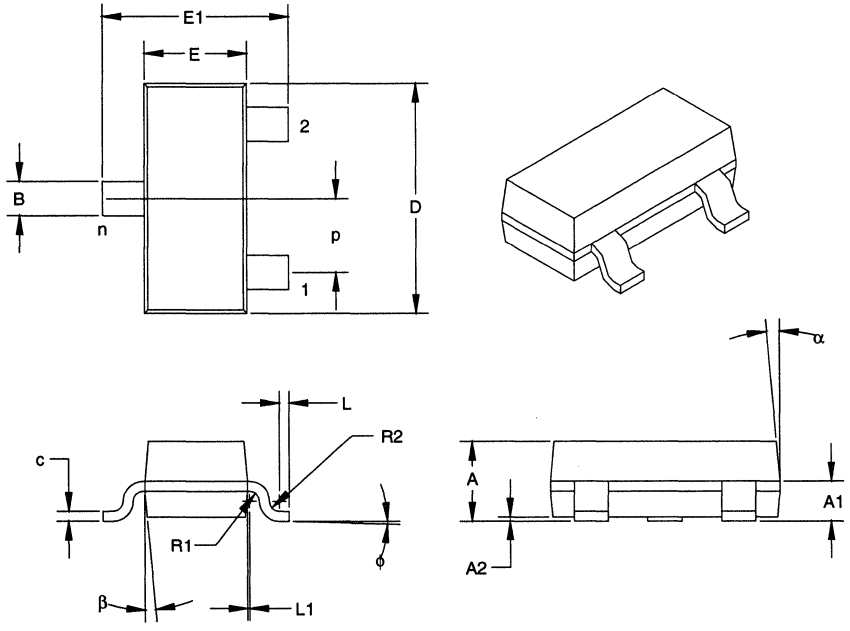
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: TO-92

Packaging Diagrams and Parameters

Package Type: K04-104 3-Lead Plastic Small Outline Transistor (TT)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.037			0.95	
Number of Pins	n		3			3	
Overall Pack. Height	A	0.035	0.040	0.044	0.89	1.01	1.12
Shoulder Height	A1	0.010	0.020	0.030	0.25	0.50	0.75
Standoff	A2	0.001	0.002	0.004	0.01	0.06	0.10
Molded Package Length	D‡	0.110	0.115	0.120	2.80	2.92	3.04
Molded Package Width	E‡	0.047	0.051	0.055	1.20	1.30	1.40
Outside Dimension	E1	0.083	0.093	0.104	2.10	2.37	2.64
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.002	0.006	0.011	0.04	0.16	0.28
Foot Angle	φ	0	5	10	0	5	10
Radius Centerline	L1	0.000	0.001	0.005	0.00	0.03	0.13
Lead Thickness	c	0.003	0.005	0.007	0.09	0.13	0.18
Lower Lead Width	B†	0.015	0.017	0.020	0.37	0.44	0.51
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

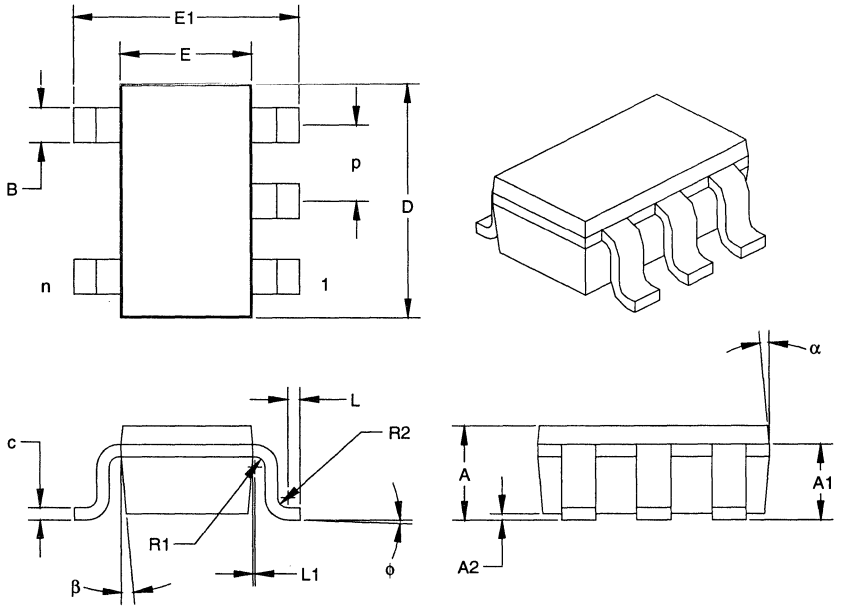
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: TO-236 AB

Packaging Diagrams and Parameters

Package Type: K04-091 5-Lead Plastic Small Outline Transistor (OT)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.037			0.95	
Number of Pins	n		5			5	
Overall Pack. Height	A	0.035	0.046	0.057	0.90	1.18	1.45
Shoulder Height	A1	0.027	0.037	0.047	0.69	0.94	1.19
Standoff	A2	0.000	0.003	0.006	0.00	0.08	0.15
Molded Package Length	D‡	0.110	0.114	0.118	2.80	2.90	3.00
Molded Package Width	E‡	0.059	0.064	0.069	1.50	1.63	1.75
Outside Dimension	E1	0.102	0.110	0.118	2.60	2.80	3.00
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.004	0.014	0.024	0.10	0.35	0.60
Foot Angle	ϕ	0	5	10	0	5	10
Radius Centerline	L1	0.000	0.001	0.005	0.00	0.03	0.13
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.014	0.017	0.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

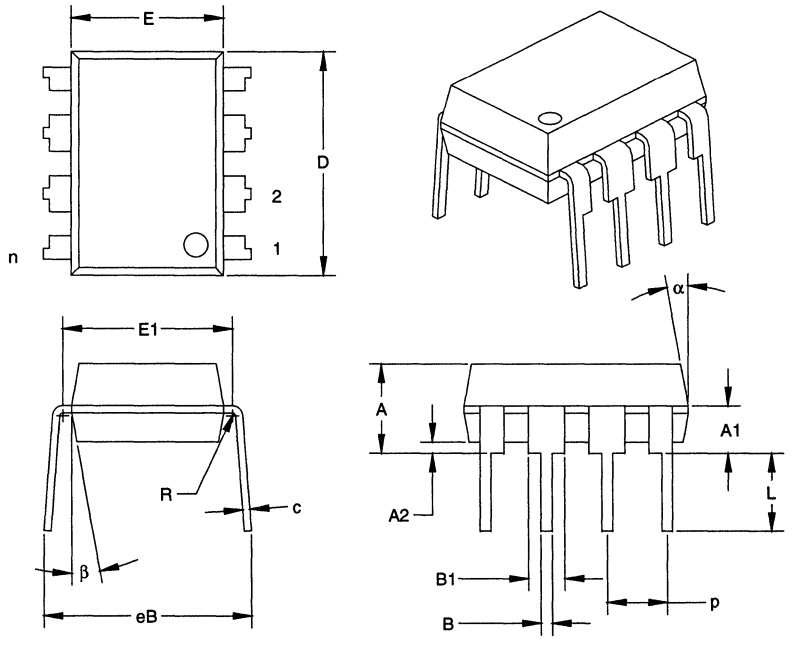
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-178 AA

Packaging Diagrams and Parameters

Package Type: K04-018 8-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.006	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.060	0.080	0.100	1.52	2.03	2.54
Base to Seating Plane	A2	0.005	0.020	0.035	0.13	0.51	0.89
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D‡	0.355	0.370	0.385	9.02	9.40	9.78
Molded Package Width	E‡	0.245	0.250	0.260	6.22	6.35	6.60
Radius to Radius Width	E1	0.267	0.280	0.292	6.78	7.10	7.42
Overall Row Spacing	eB	0.310	0.342	0.380	7.87	8.67	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

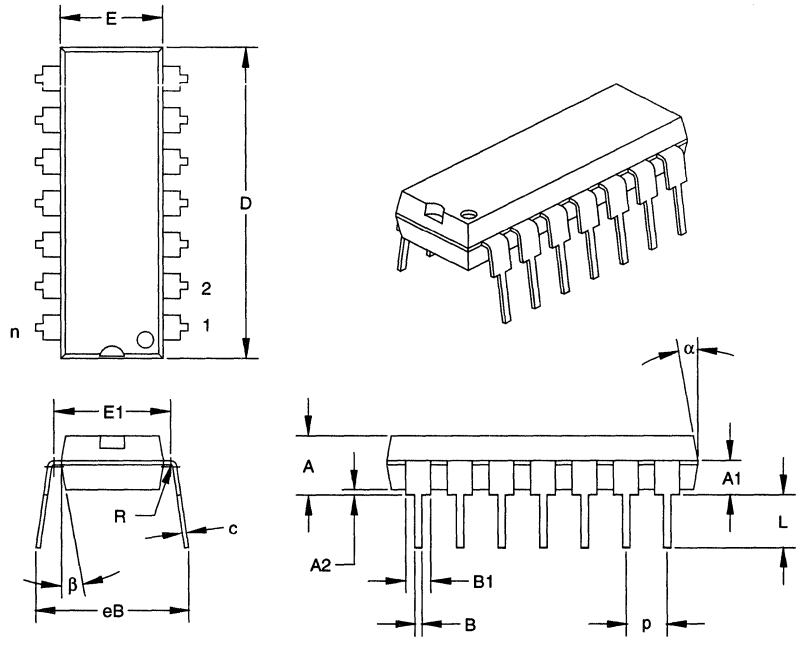
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-001 BA

Packaging Diagrams and Parameters

Package Type: K04-005 14-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		14			14	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46	0.58
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.006	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.120	0.145	0.170	3.05	3.68	4.32
Top of Lead to Seating Plane	A1	0.065	0.085	0.105	1.65	2.16	2.67
Base to Seating Plane	A2	0.000	0.015	0.035	0.00	0.38	0.89
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	0.740	0.750	0.760	18.80	19.05	19.30
Molded Package Width	E‡	0.240	0.245	0.250	6.10	6.22	6.35
Radius to Radius Width	E1	0.260	0.280	0.300	6.60	7.11	7.62
Overall Row Spacing	eB	0.310	0.368	0.425	7.87	9.33	10.80
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

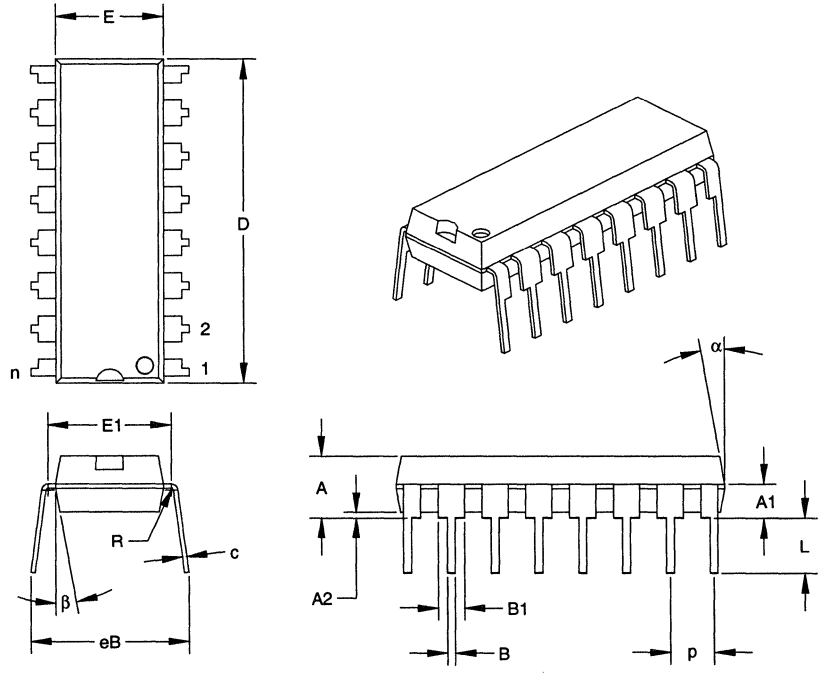
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010"(0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-001 AA

Packaging Diagrams and Parameters

Package Type: K04-017 16-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		16			16	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46	0.58
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.006	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.120	0.145	0.170	3.05	3.68	4.32
Top of Lead to Seating Plane	A1	0.060	0.080	0.100	1.52	2.03	2.54
Base to Seating Plane	A2	0.000	0.015	0.035	0.00	0.38	0.89
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	0.740	0.750	0.760	18.80	19.05	19.30
Molded Package Width	E‡	0.240	0.245	0.250	6.10	6.22	6.35
Radius to Radius Width	E1	0.260	0.280	0.300	6.60	7.11	7.62
Overall Row Spacing	eB	0.310	0.361	0.412	7.87	9.17	10.46
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

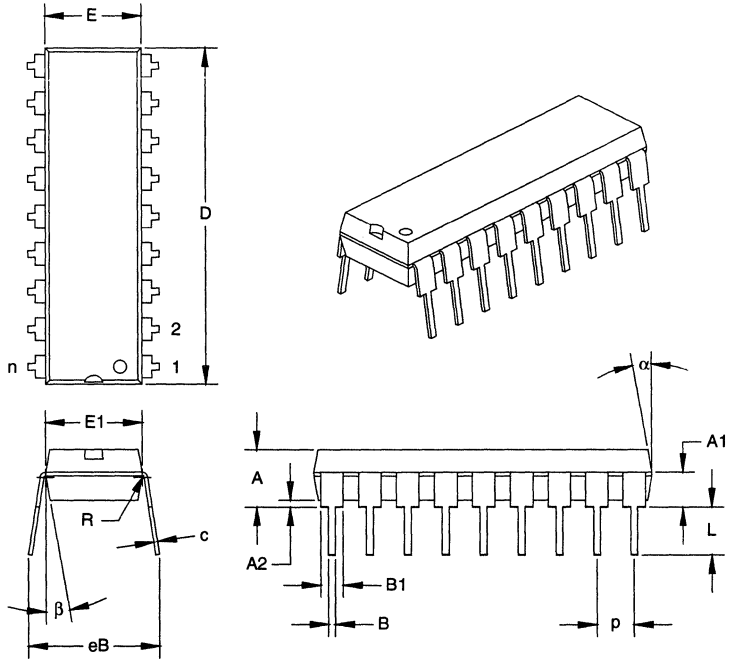
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-001 BB

Packaging Diagrams and Parameters

Package Type: K04-007 18-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		18			18	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46	0.58
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.010	0.015	0.13	0.25	0.38
Top to Seating Plane	A	0.110	0.155	0.155	2.79	3.94	3.94
Top of Lead to Seating Plane	A1	0.075	0.095	0.115	1.91	2.41	2.92
Base to Seating Plane	A2	0.000	0.020	0.020	0.00	0.51	0.51
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	0.890	0.895	0.900	22.61	22.73	22.86
Molded Package Width	E‡	0.245	0.255	0.265	6.22	6.48	6.73
Radius to Radius Width	E1	0.230	0.250	0.270	5.84	6.35	6.86
Overall Row Spacing	eB	0.310	0.349	0.387	7.87	8.85	9.83
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

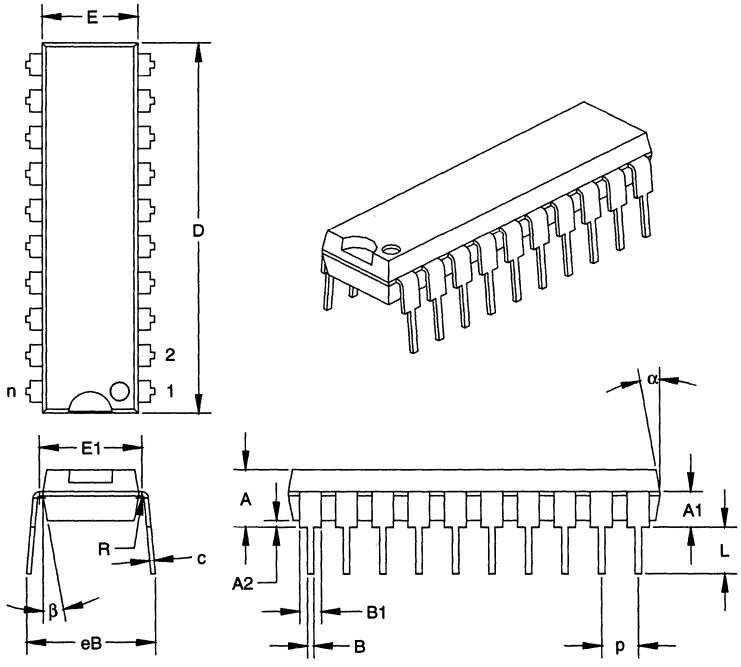
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-001 AC

Packaging Diagrams and Parameters

Package Type: K04-019 20-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		20			20	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.110	0.160	0.160	2.79	4.06	4.06
Top of Lead to Seating Plane	A1	0.080	0.100	0.120	2.03	2.54	3.05
Base to Seating Plane	A2	0.000	0.020	0.040	0.00	0.51	1.02
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D‡	0.980	1.020	1.060	24.89	25.91	26.92
Molded Package Width	E‡	0.240	0.260	0.280	6.10	6.60	7.11
Radius to Radius Width	E1	0.267	0.280	0.292	6.78	7.10	7.42
Overall Row Spacing	eB	0.310	0.350	0.390	7.87	8.89	9.91
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

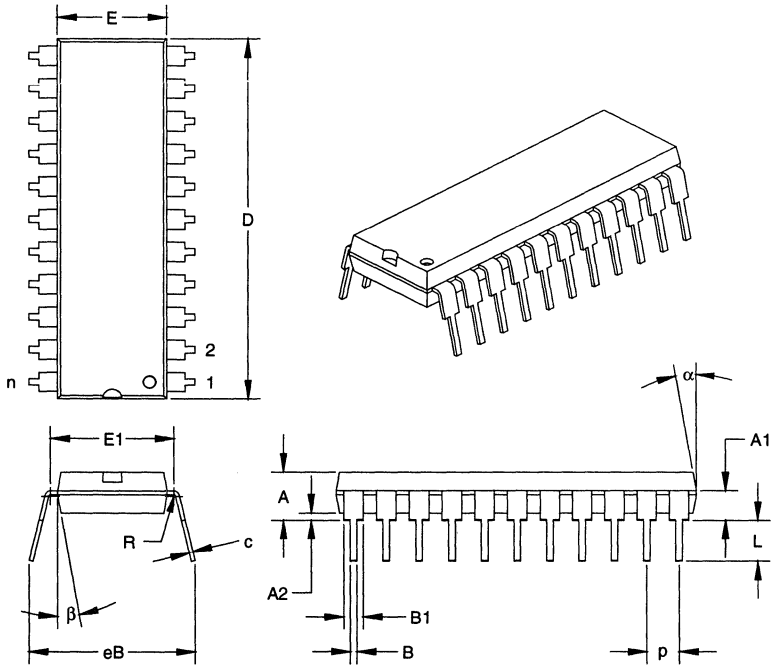
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-001 AD

Packaging Diagrams and Parameters

Package Type: K04-008 22-Lead Plastic Dual In-line (P) – 400 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.400			10.16	
Number of Pins	n		22			22	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.018	0.020	0.022	0.46	0.51	0.56
Upper Lead Width	B1†	0.058	0.060	0.062	1.47	1.52	1.57
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.150	0.152	0.154	3.81	3.86	3.91
Top of Lead to Seating Plane	A1	0.075	0.095	0.115	1.91	2.41	2.92
Base to Seating Plane	A2	0.023	0.026	0.029	0.58	0.66	0.74
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D‡	1.100	1.105	1.110	27.94	28.07	28.19
Molded Package Width	E‡	0.330	0.335	0.340	8.38	8.51	8.64
Radius to Radius Width	E1	0.367	0.379	0.391	9.32	9.63	9.93
Overall Row Spacing	eB	0.500	0.512	0.524	12.70	13.00	13.31
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

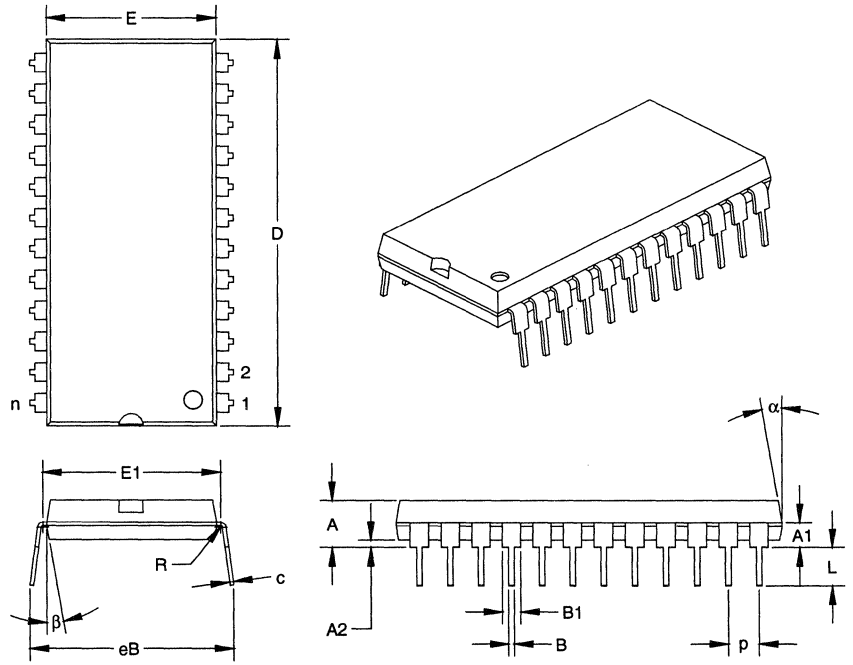
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-010 AA

Packaging Diagrams and Parameters

Package Type: K04-081 24-Lead Plastic Dual In-line (P) – 600 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		24			24	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.140	0.165	0.190	3.56	4.19	4.83
Top of Lead to Seating Plane	A1	0.064	0.084	0.104	1.61	2.12	2.63
Base to Seating Plane	A2	0.020	0.025	0.030	0.51	0.64	0.76
Tip to Seating Plane	L	0.115	0.125	0.135	2.92	3.18	3.43
Package Length	D‡	1.245	1.250	1.255	31.62	31.75	31.88
Molded Package Width	E‡	0.540	0.550	0.560	13.72	13.97	14.22
Radius to Radius Width	E1	0.562	0.577	0.592	14.27	14.66	15.04
Overall Row Spacing	eB	0.630	0.660	0.690	16.00	16.76	17.53
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

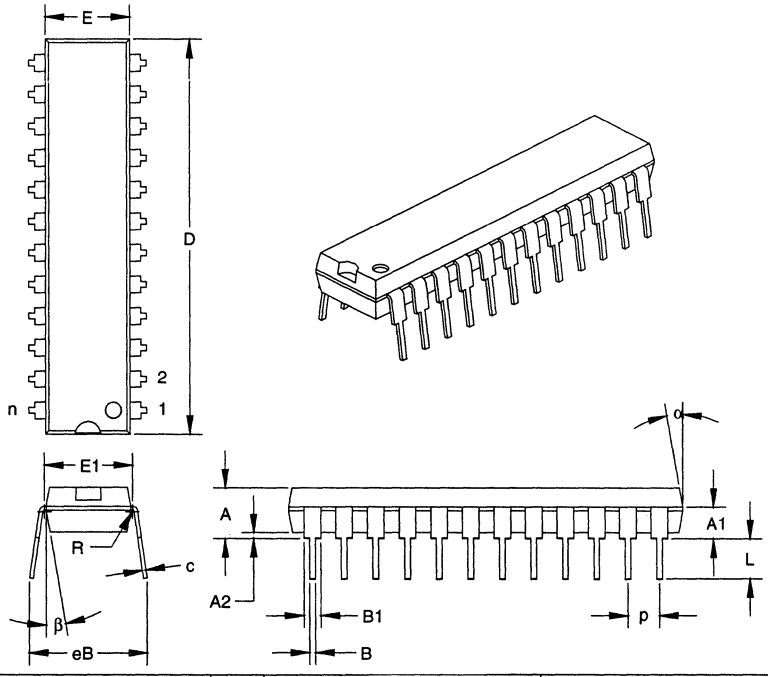
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-011 AA

Packaging Diagrams and Parameters

Package Type: K04-043 24-Lead Skinny Plastic Dual In-line (SP) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		24			24	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1†	0.045	0.053	0.060	1.14	1.33	1.52
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.150	0.163	0.175	3.81	4.13	4.45
Top of Lead to Seating Plane	A1	0.083	0.103	0.123	2.10	2.60	3.11
Base to Seating Plane	A2	0.015	0.020	0.025	0.38	0.51	0.64
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D‡	1.245	1.250	1.255	31.63	31.76	31.88
Molded Package Width	E‡	0.255	0.268	0.280	6.48	6.79	7.11
Radius to Radius Width	E1	0.267	0.280	0.292	6.78	7.10	7.42
Overall Row Spacing	eB	0.370	0.375	0.380	9.40	9.53	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

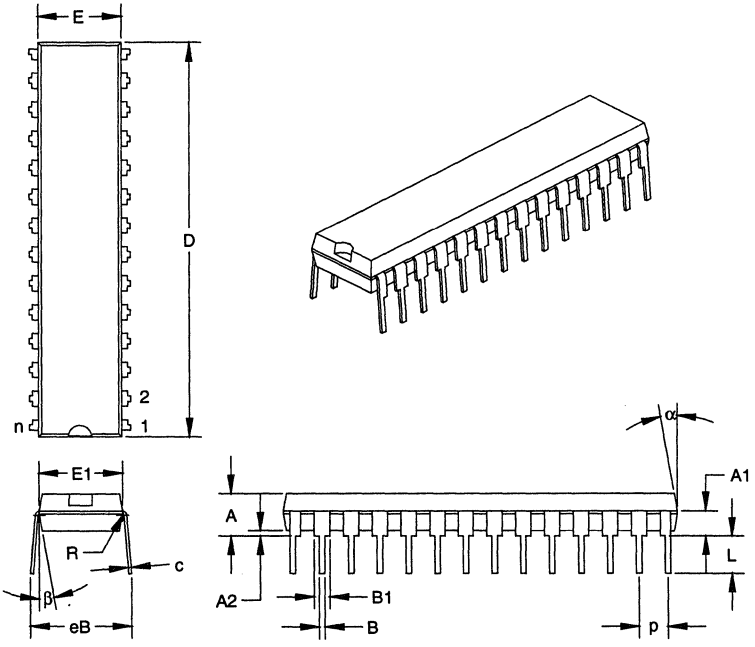
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-001 AF

Packaging Diagrams and Parameters

Package Type: K04-070 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.016	0.019	0.022	0.41	0.48	0.56
Upper Lead Width	B1†	0.040	0.053	0.065	1.02	1.33	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.070	0.090	0.110	1.78	2.29	2.79
Base to Seating Plane	A2	0.015	0.020	0.025	0.38	0.51	0.64
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	1.345	1.365	1.385	34.16	34.67	35.18
Molded Package Width	E‡	0.280	0.288	0.295	7.11	7.30	7.49
Radius to Radius Width	E1	0.270	0.283	0.295	6.86	7.18	7.49
Overall Row Spacing	eB	0.320	0.350	0.380	8.13	8.89	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

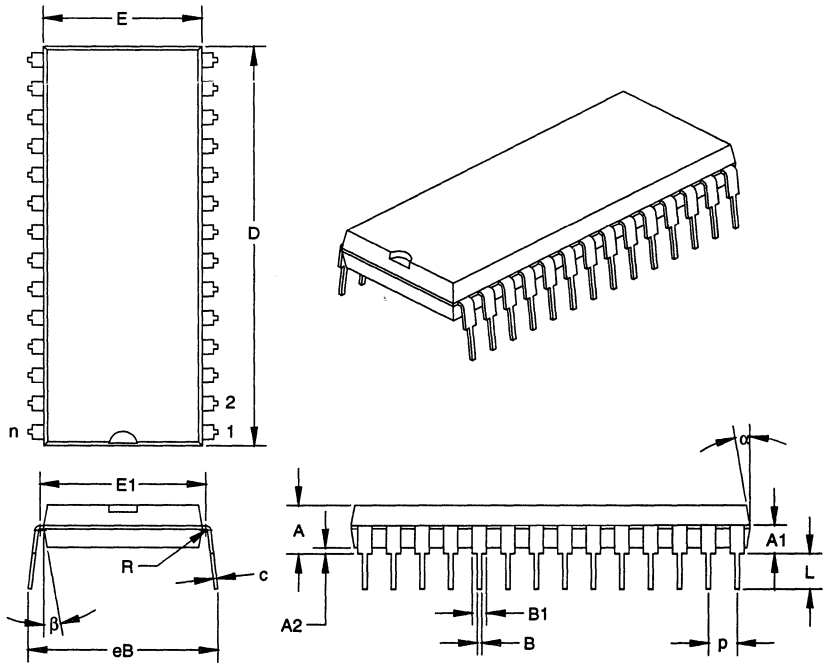
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-095 AH

Packaging Diagrams and Parameters

Package Type: K04-079 28-Lead Plastic Dual In-line (P) – 600 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		28			28	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.016	0.018	0.36	0.41	0.46
Upper Lead Width	B1†	0.040	0.050	0.060	1.02	1.27	1.52
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.160	0.173	0.185	4.06	4.38	4.70
Top of Lead to Seating Plane	A1	0.081	0.101	0.121	2.04	2.55	3.06
Base to Seating Plane	A2	0.015	0.023	0.030	0.38	0.57	0.76
Tip to Seating Plane	L	0.115	0.125	0.135	2.92	3.18	3.43
Package Length	D‡	1.380	1.395	1.465	35.05	35.43	37.20
Molded Package Width	E‡	0.505	0.550	0.555	12.80	13.97	14.10
Radius to Radius Width	E1	0.567	0.577	0.587	14.40	14.66	14.91
Overall Row Spacing	eB	0.640	0.660	0.680	16.26	16.76	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

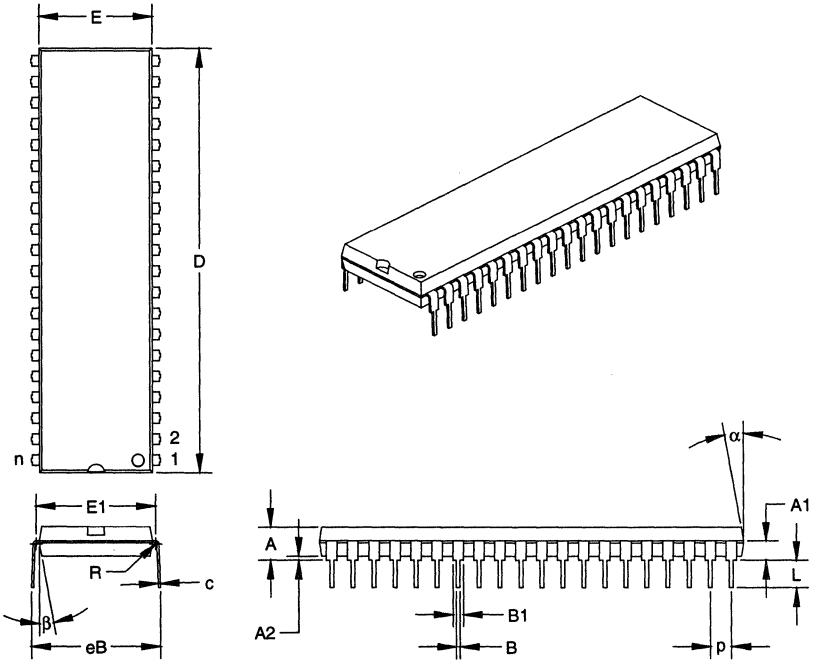
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-011 AB

Packaging Diagrams and Parameters

Package Type: K04-016 40-Lead Plastic Dual In-line (P) – 600 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		40			40	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1†	0.045	0.050	0.055	1.14	1.27	1.40
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.009	0.010	0.011	0.23	0.25	0.28
Top to Seating Plane	A	0.110	0.160	0.160	2.79	4.06	4.06
Top of Lead to Seating Plane	A1	0.073	0.093	0.113	1.85	2.36	2.87
Base to Seating Plane	A2	0.020	0.020	0.040	0.51	0.51	1.02
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	2.013	2.018	2.023	51.13	51.26	51.38
Molded Package Width	E‡	0.530	0.535	0.540	13.46	13.59	13.72
Radius to Radius Width	E1	0.545	0.565	0.585	13.84	14.35	14.86
Overall Row Spacing	eB	0.630	0.610	0.670	16.00	15.49	17.02
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

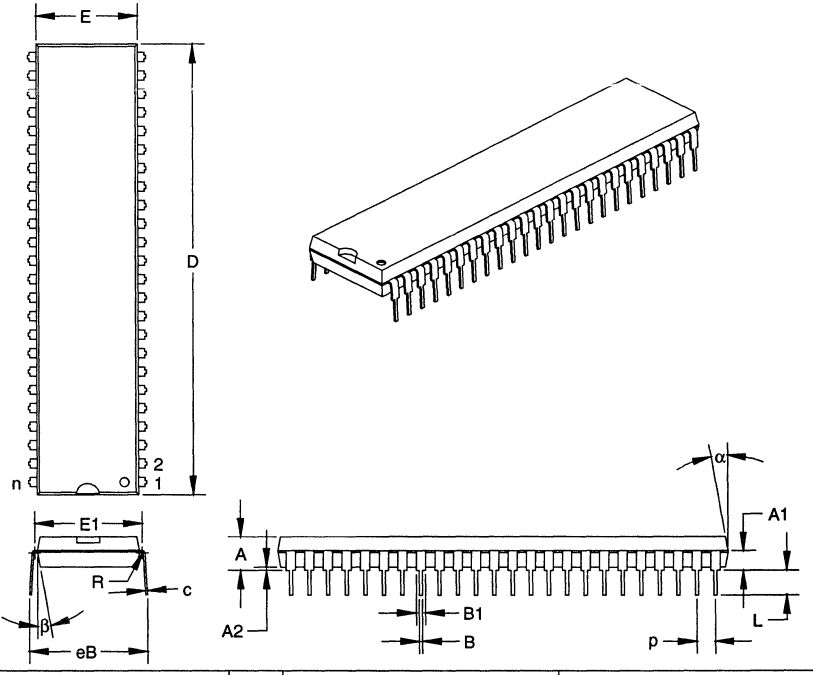
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-011 AC

Packaging Diagrams and Parameters

Package Type: K04-022 48-Lead Plastic Dual In-line (P) – 600 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		48			48	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1†	0.045	0.050	0.055	1.14	1.27	1.40
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.175	0.183	0.190	4.45	4.64	4.83
Top of Lead to Seating Plane	A1	0.088	0.108	0.128	2.22	2.73	3.24
Base to Seating Plane	A2	0.010	0.018	0.025	0.25	0.44	0.64
Tip to Seating Plane	L	0.125	0.134	0.142	3.18	3.39	3.61
Package Length	D‡	2.425	2.438	2.450	61.60	61.91	62.23
Molded Package Width	E‡	0.540	0.550	0.560	13.72	13.97	14.22
Radius to Radius Width	E1	0.570	0.583	0.595	14.48	14.80	15.11
Overall Row Spacing	eB	0.610	0.640	0.670	15.49	16.26	17.02
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

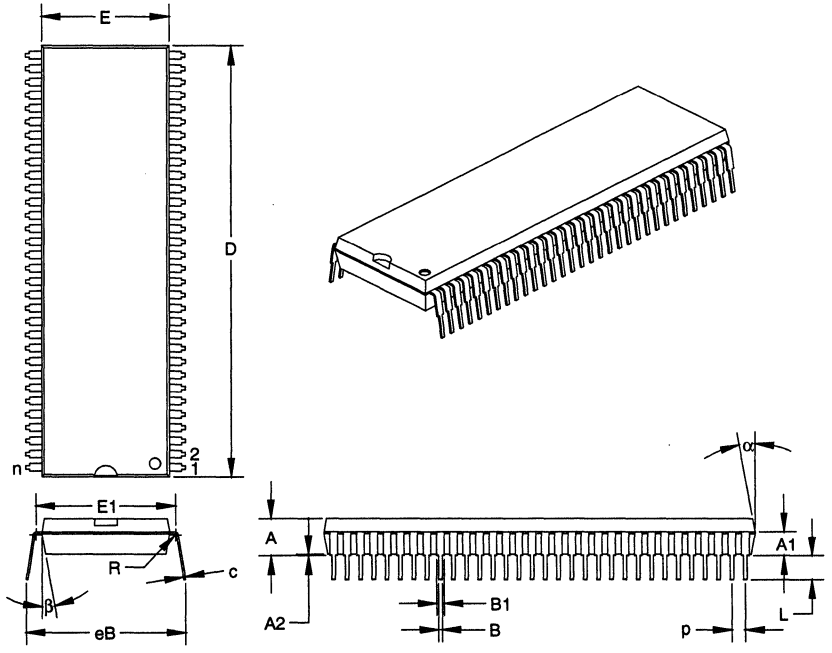
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-011 AD

Packaging Diagrams and Parameters

Package Type: K04-090 64-Lead Shrink Plastic Dual In-line (SP) – 750 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.750			19.05	
Number of Pins	n		64			64	
Pitch	p		0.070			1.78	
Lower Lead Width	B	0.015	0.019	0.022	0.38	0.47	0.56
Upper Lead Width	B1†	0.030	0.040	0.050	0.76	1.02	1.27
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.175	0.200	0.200	4.45	5.08	5.08
Top of Lead to Seating Plane	A1	0.110	0.130	0.150	2.79	3.30	3.81
Base to Seating Plane	A2	0.020	0.020	0.040	0.51	0.51	1.02
Tip to Seating Plane	L	0.120	0.128	0.135	3.05	3.24	3.43
Package Length	D‡	2.260	2.270	2.280	57.40	57.66	57.91
Molded Package Width	E‡	0.660	0.670	0.680	16.76	17.02	17.27
Radius to Radius Width	E1	0.720	0.733	0.745	18.29	18.61	18.92
Overall Row Spacing	eB	0.760	0.840	0.920	19.30	21.33	23.36
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

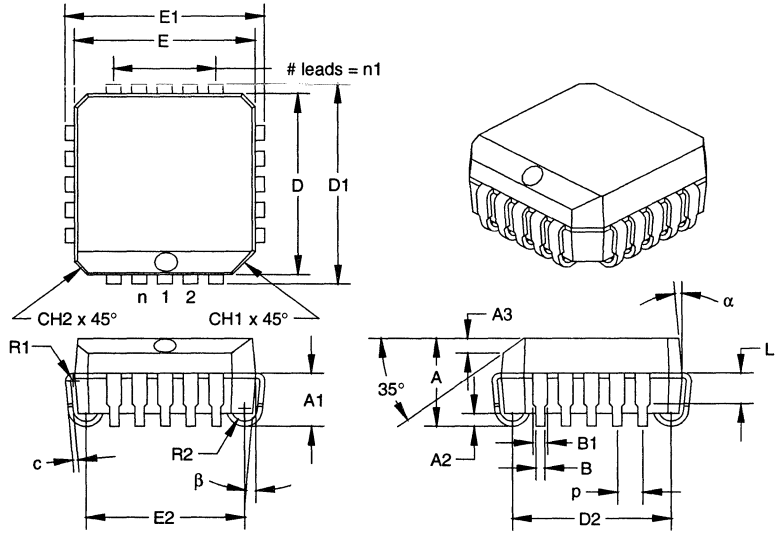
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-021 AA

Packaging Diagrams and Parameters

Package Type: K04-064 20-Lead Plastic Leaded Chip Carrier (L) – Square



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.165	0.173	0.180	4.19	4.38	4.57
Shoulder Height	A1	0.095	0.105	0.115	2.41	2.67	2.92
Standoff	A2	0.020	0.025	0.030	0.51	0.64	0.76
Side 1 Chamfer Dim.	A3	0.024	0.029	0.034	0.61	0.74	0.86
Corner Chamfer (1)	CH1	0.040	0.045	0.050	1.02	1.14	1.27
Corner Chamfer (other)	CH2	0.020	0.025	0.030	0.51	0.64	0.76
Overall Pack. Width	E1	0.385	0.390	0.395	9.78	9.91	10.03
Overall Pack. Length	D1	0.385	0.390	0.395	9.78	9.91	10.03
Molded Pack. Width	E‡	0.350	0.353	0.356	8.89	8.97	9.04
Molded Pack. Length	D‡	0.350	0.353	0.356	8.89	8.97	9.04
Footprint Width	E2	0.295	0.310	0.325	7.49	7.87	8.26
Footprint Length	D2	0.295	0.310	0.325	7.49	7.87	8.26
Pins along Width	n1		5			5	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1†	0.026	0.029	0.032	0.66	0.74	0.81
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Length	L	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Inside Radius	R1	0.003	0.005	0.010	0.08	0.13	0.25
J-Bend Inside Radius	R2	0.015	0.025	0.035	0.38	0.64	0.89
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

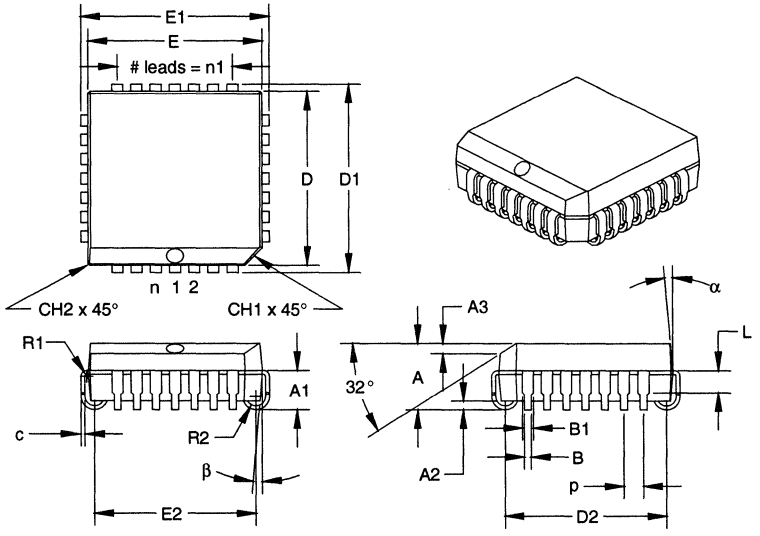
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-047 AA

Packaging Diagrams and Parameters

Package Type: K04-026 28-Lead Plastic Leaded Chip Carrier (L) – Square



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.165	0.173	0.180	4.19	4.38	4.57
Shoulder Height	A1	0.095	0.103	0.110	2.41	2.60	2.79
Standoff	A2	0.015	0.023	0.030	0.38	0.57	0.76
Side 1 Chamfer Dim.	A3	0.021	0.026	0.031	0.53	0.66	0.79
Corner Chamfer (1)	CH1	0.035	0.045	0.055	0.89	1.14	1.40
Corner Chamfer (other)	CH2	0.000	0.005	0.010	0.00	0.13	0.25
Overall Pack. Width	E1	0.485	0.490	0.495	12.32	12.45	12.57
Overall Pack. Length	D1	0.485	0.490	0.495	12.32	12.45	12.57
Molded Pack. Width	E‡	0.450	0.453	0.456	11.43	11.51	11.58
Molded Pack. Length	D‡	0.450	0.453	0.456	11.43	11.51	11.58
Footprint Width	E2	0.410	0.420	0.430	10.41	10.67	10.92
Footprint Length	D2	0.410	0.420	0.430	10.41	10.67	10.92
Pins along Width	n1		7			7	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1†	0.026	0.029	0.032	0.66	0.74	0.81
Lower Lead Width	B	0.015	0.018	0.021	0.38	0.46	0.53
Upper Lead Length	L	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Inside Radius	R1	0.003	0.005	0.010	0.08	0.13	0.25
J-Bend Inside Radius	R2	0.015	0.025	0.035	0.38	0.64	0.89
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

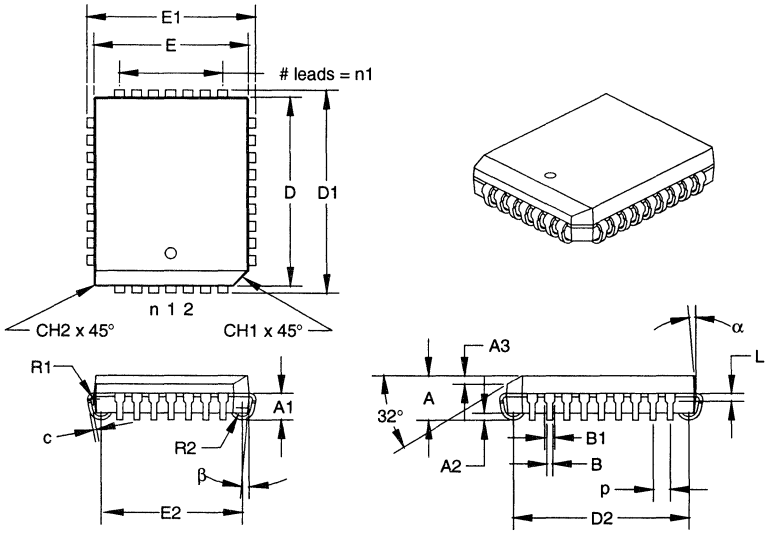
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-047 AB

Packaging Diagrams and Parameters

Package Type: K04-023 32-Lead Plastic Leaded Chip Carrier (L) – Rectangle



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		32			32	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.127	0.131	0.135	3.23	3.33	3.43
Shoulder Height	A1	0.060	0.078	0.095	1.52	1.97	2.41
Standoff	A2	0.015	0.020	0.025	0.38	0.51	0.64
Side 1 Chamfer Dim.	A3	0.021	0.026	0.031	0.53	0.66	0.79
Corner Chamfer (1)	CH1	0.035	0.045	0.055	0.89	1.14	1.40
Corner Chamfer (other)	CH2	0.000	0.005	0.010	0.00	0.13	0.25
Overall Pack. Width	E1	0.485	0.490	0.495	12.32	12.45	12.57
Overall Pack. Length	D1	0.585	0.590	0.595	14.86	14.99	15.11
Molded Pack. Width	E‡	0.447	0.450	0.453	11.35	11.43	11.51
Molded Pack. Length	D‡	0.547	0.550	0.553	13.89	13.97	14.05
Footprint Width	E2	0.380	0.410	0.440	9.65	10.41	11.18
Footprint Length	D2	0.480	0.510	0.540	12.19	12.95	13.72
Pins along Width	n1		7			7	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1†	0.026	0.029	0.032	0.66	0.74	0.81
Lower Lead Width	B	0.013	0.017	0.021	0.33	0.43	0.53
Upper Lead Length	L	0.010	0.020	0.030	0.25	0.51	0.76
Shoulder Inside Radius	R1	0.003	0.008	0.013	0.08	0.20	0.33
J-Bend Inside Radius	R2	0.020	0.025	0.030	0.51	0.64	0.76
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

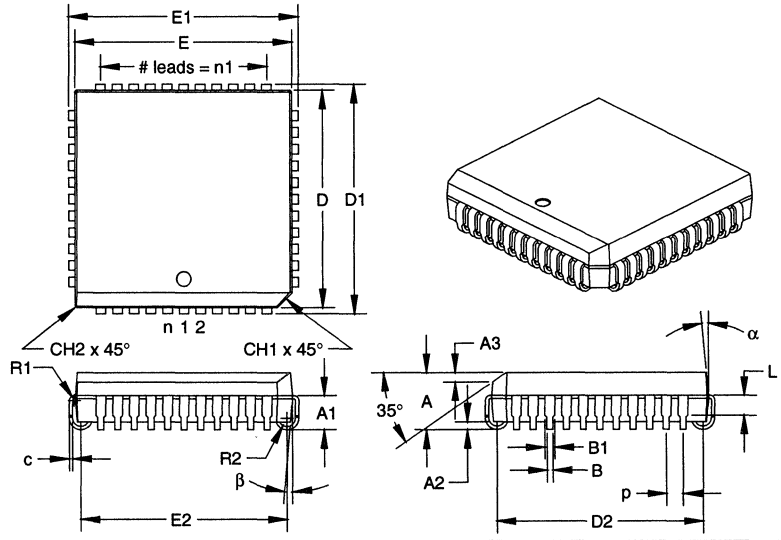
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-016 AE

Packaging Diagrams and Parameters

Package Type: K04-048 44-Lead Plastic Leaded Chip Carrier (L) – Square



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.165	0.173	0.180	4.19	4.38	4.57
Shoulder Height	A1	0.095	0.103	0.110	2.41	2.60	2.79
Standoff	A2	0.015	0.023	0.030	0.38	0.57	0.76
Side 1 Chamfer Dim.	A3	0.024	0.029	0.034	0.61	0.74	0.86
Corner Chamfer (1)	CH1	0.040	0.045	0.050	1.02	1.14	1.27
Corner Chamfer (other)	CH2	0.000	0.005	0.010	0.00	0.13	0.25
Overall Pack. Width	E1	0.685	0.690	0.695	17.40	17.53	17.65
Overall Pack. Length	D1	0.685	0.690	0.695	17.40	17.53	17.65
Molded Pack. Width	E‡	0.650	0.653	0.656	16.51	16.59	16.66
Molded Pack. Length	D‡	0.650	0.653	0.656	16.51	16.59	16.66
Footprint Width	E2	0.610	0.620	0.630	15.49	15.75	16.00
Footprint Length	D2	0.610	0.620	0.630	15.49	15.75	16.00
Pins along Width	n1		11			11	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1†	0.026	0.029	0.032	0.66	0.74	0.81
Lower Lead Width	B	0.015	0.018	0.021	0.38	0.46	0.53
Upper Lead Length	L	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Inside Radius	R1	0.003	0.005	0.010	0.08	0.13	0.25
J-Bend Inside Radius	R2	0.015	0.025	0.035	0.38	0.64	0.89
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

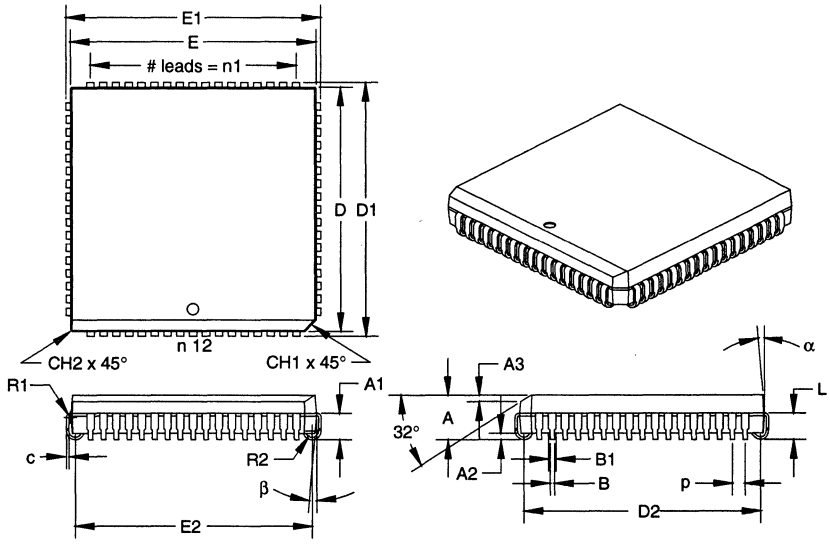
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-047 AC

Packaging Diagrams and Parameters

Package Type: K04-049 68-Lead Plastic Leaded Chip Carrier (L) – Square



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		68			68	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.165	0.175	0.185	4.19	4.45	4.70
Shoulder Height	A1	0.095	0.103	0.110	2.41	2.60	2.79
Standoff	A2	0.017	0.025	0.032	0.43	0.62	0.81
Side 1 Chamfer Dim.	A3	0.021	0.026	0.031	0.53	0.66	0.79
Corner Chamfer (1)	CH1	0.035	0.045	0.055	0.89	1.14	1.40
Corner Chamfer (other)	CH2	0.000	0.005	0.010	0.00	0.13	0.25
Overall Pack. Width	E1	0.985	0.990	0.995	25.02	25.15	25.27
Overall Pack. Length	D1	0.985	0.990	0.995	25.02	25.15	25.27
Molded Pack. Width	E‡	0.950	0.954	0.958	24.13	24.23	24.33
Molded Pack. Length	D‡	0.950	0.954	0.958	24.13	24.23	24.33
Footprint Width	E2	0.910	0.920	0.930	23.11	23.37	23.62
Footprint Length	D2	0.910	0.920	0.930	23.11	23.37	23.62
Pins along Width	n1		17			17	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1†	0.026	0.029	0.031	0.66	0.72	0.79
Lower Lead Width	B	0.015	0.018	0.021	0.38	0.46	0.53
Upper Lead Length	L	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Inside Radius	R1	0.003	0.005	0.010	0.08	0.13	0.25
J-Bend Inside Radius	R2	0.015	0.025	0.035	0.38	0.64	0.89
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

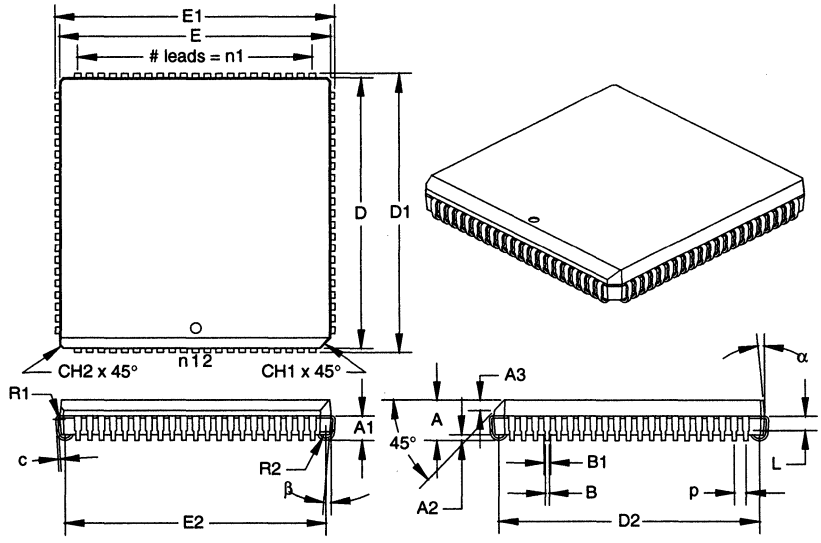
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-047 AE

Packaging Diagrams and Parameters

Package Type: K04-093 84-Lead Plastic Leaded Chip Carrier (L) – Square



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		84			84	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.165	0.173	0.180	4.19	4.38	4.57
Shoulder Height	A1	0.090	0.105	0.120	2.29	2.67	3.05
Standoff	A2	0.020	0.025	0.030	0.51	0.64	0.76
Side 1 Chamfer Dim.	A3	0.042	0.045	0.048	1.07	1.14	1.22
Corner Chamfer (1)	CH1	0.042	0.045	0.048	1.07	1.14	1.22
Corner Chamfer(other)	CH2	0.010	0.015	0.020	0.25	0.38	0.51
Overall Pack. Width	E1	1.185	1.190	1.195	30.10	30.23	30.35
Overall Pack. Length	D1	1.185	1.190	1.195	30.10	30.23	30.35
Molded Pack. Width	E‡	1.150	1.154	1.158	29.21	29.31	29.41
Molded Pack. Length	D‡	1.150	1.154	1.158	29.21	29.31	29.41
Footprint Width	E2	1.095	1.110	1.125	27.81	28.19	28.58
Footprint Length	D2	1.095	1.110	1.125	27.81	28.19	28.58
Pins along Width	n1		21			21	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1†	0.023	0.028	0.033	0.58	0.71	0.84
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46	0.58
Upper Lead Length	L	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Inside Radius	R1	0.003	0.005	0.010	0.08	0.13	0.25
J-Bend Inside Radius	R2	0.022	0.027	0.032	0.56	0.69	0.81
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

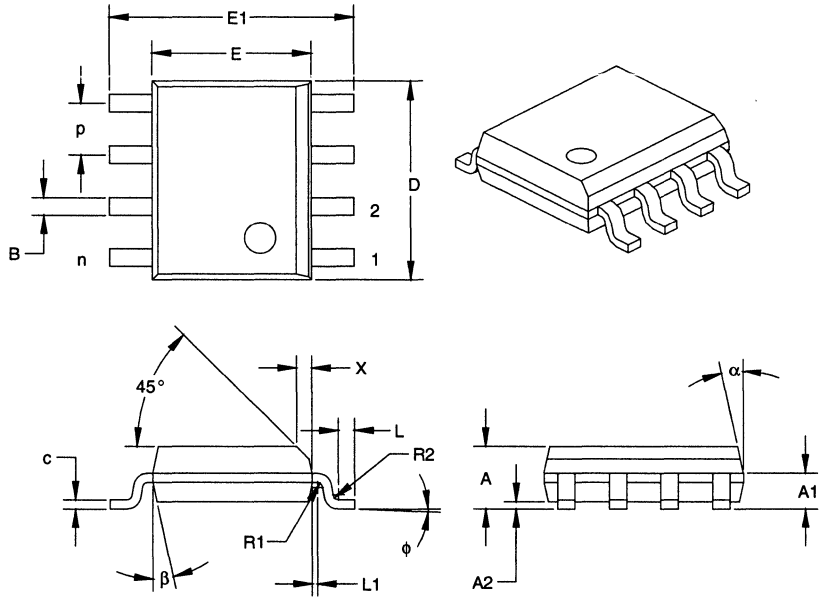
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-047 AF

Packaging Diagrams and Parameters

Package Type: K04-057 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.054	0.061	0.069	1.37	1.56	1.75
Shoulder Height	A1	0.027	0.035	0.044	0.69	0.90	1.11
Standoff	A2	0.004	0.007	0.010	0.10	0.18	0.25
Molded Package Length	D‡	0.189	0.193	0.196	4.80	4.89	4.98
Molded Package Width	E‡	0.150	0.154	0.157	3.81	3.90	3.99
Outside Dimension	E1	0.229	0.237	0.244	5.82	6.01	6.20
Chamfer Distance	X	0.010	0.015	0.020	0.25	0.38	0.51
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B†	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

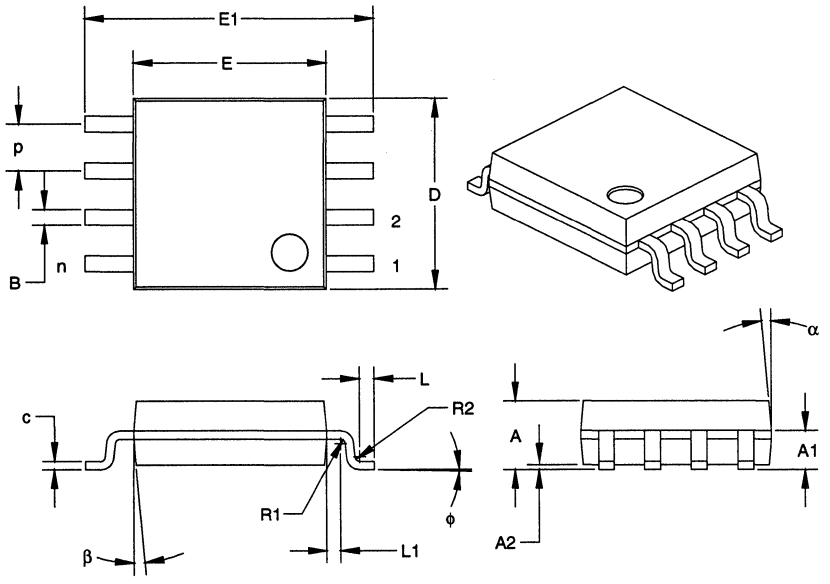
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-012 AA

Packaging Diagrams and Parameters

Package Type: K04-056 8-Lead Plastic Small Outline (SM) – Medium, 208 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		8			8	
Overall Pack. Height	A	0.070	0.074	0.079	1.78	1.89	2.00
Shoulder Height	A1	0.037	0.042	0.048	0.94	1.08	1.21
Standoff	A2	0.002	0.005	0.009	0.05	0.14	0.22
Molded Package Length	D‡	0.200	0.205	0.210	5.08	5.21	5.33
Molded Package Width	E‡	0.203	0.208	0.213	5.16	5.28	5.41
Outside Dimension	E1	0.300	0.313	0.325	7.62	7.94	8.26
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B†	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

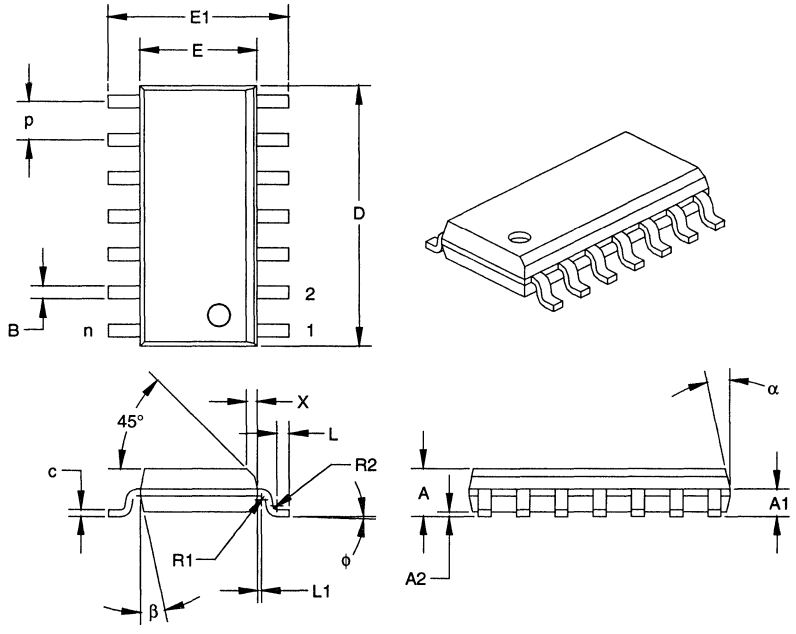
* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

Packaging Diagrams and Parameters

Package Type: K04-065 14-Lead Plastic Small Outline (SL) – Narrow, 150 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		14			14	
Overall Pack. Height	A	0.058	0.063	0.068	1.47	1.60	1.73
Shoulder Height	A1	0.027	0.036	0.044	0.69	0.90	1.12
Standoff	A2	0.004	0.006	0.008	0.10	0.15	0.20
Molded Package Length	D‡	0.338	0.341	0.344	8.59	8.66	8.74
Molded Package Width	E‡	0.150	0.153	0.156	3.81	3.89	3.96
Outside Dimension	E1	0.230	0.236	0.242	5.84	5.99	6.15
Chamfer Distance	X	0.010	0.014	0.018	0.25	0.36	0.46
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.009	0.010	0.19	0.22	0.25
Lower Lead Width	B†	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

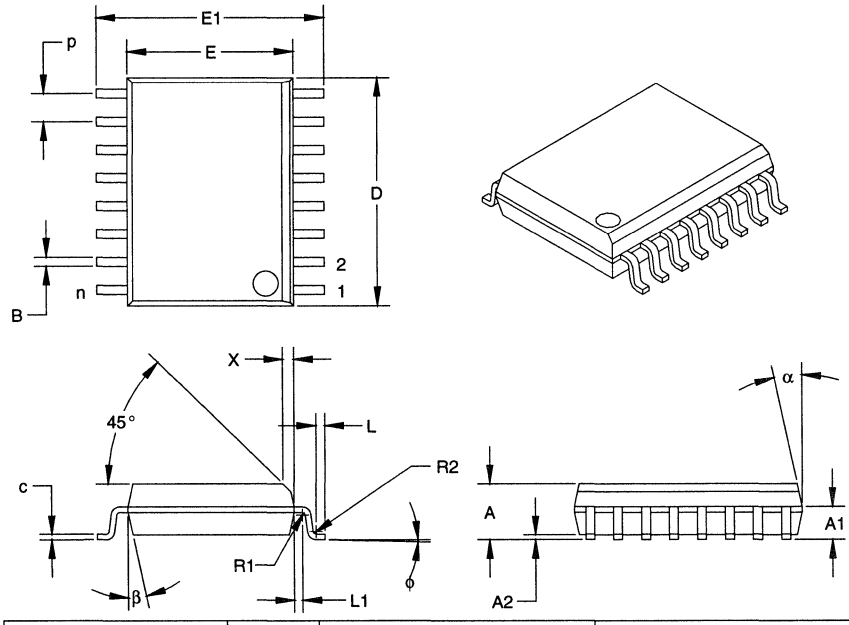
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-012 AB

Packaging Diagrams and Parameters

Package Type: K04-102 16-Lead Plastic Small Outline (SO) – Wide, 300 mil Body



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		16			16	
Overall Pack. Height	A	0.097	0.101	0.104	2.46	2.55	2.64
Shoulder Height	A1	0.050	0.060	0.070	1.27	1.52	1.78
Standoff	A2	0.005	0.009	0.012	0.13	0.22	0.30
Molded Package Length	D‡	0.402	0.407	0.412	10.21	10.34	10.46
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.400	0.405	0.410	10.16	10.29	10.41
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.010	0.013	0.23	0.25	0.32
Lower Lead Width	B†	0.014	0.016	0.019	0.36	0.41	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

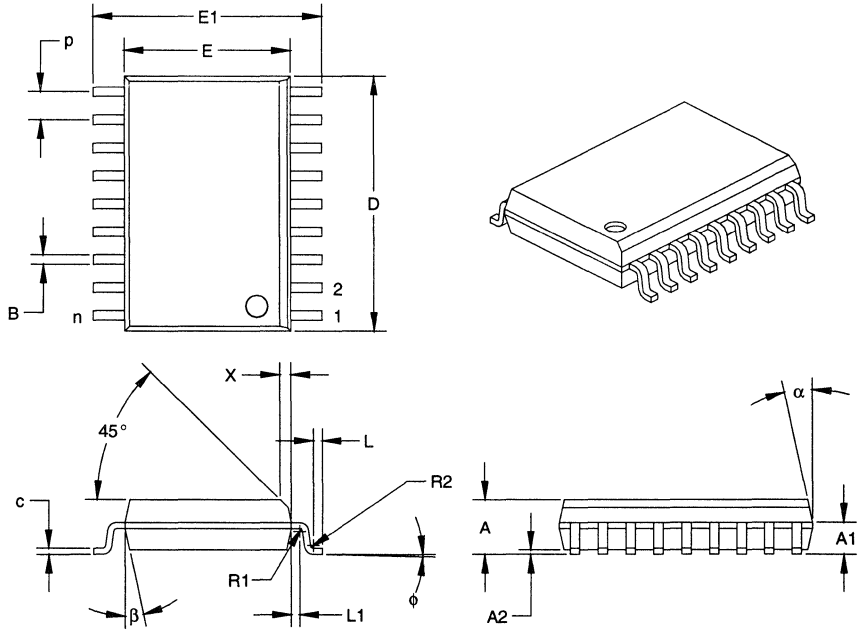
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-013 AA

Packaging Diagrams and Parameters

Package Type: K04-051 18-Lead Plastic Small Outline (SO) – Wide, 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		18			18	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D‡	0.450	0.456	0.462	11.43	11.58	11.73
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B†	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

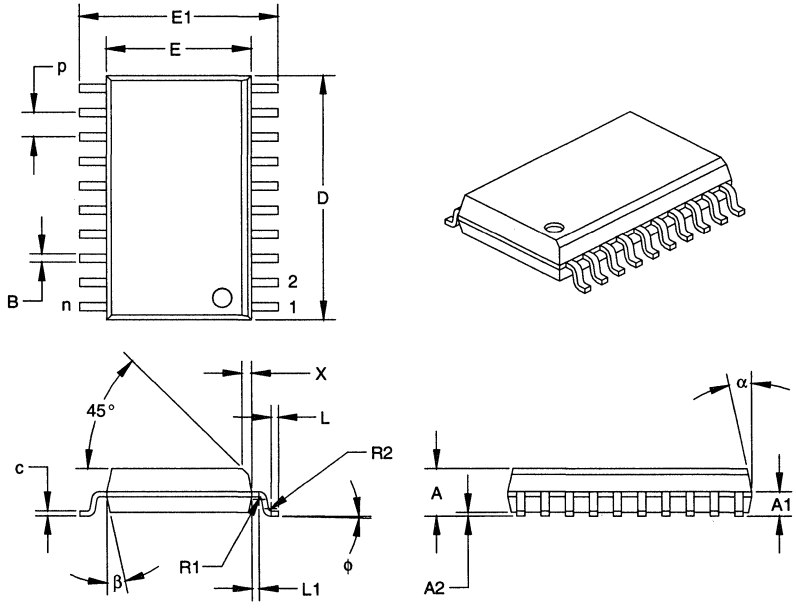
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-013 AB

Packaging Diagrams and Parameters

Package Type: K04-094 20-Lead Plastic Small Outline (SO) – Wide, 300 mil



Units		INCHES			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		20			20	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.041	0.051	0.061	1.04	1.30	1.55
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D‡	0.496	0.504	0.512	12.60	12.80	13.00
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B†	0.013	0.017	0.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

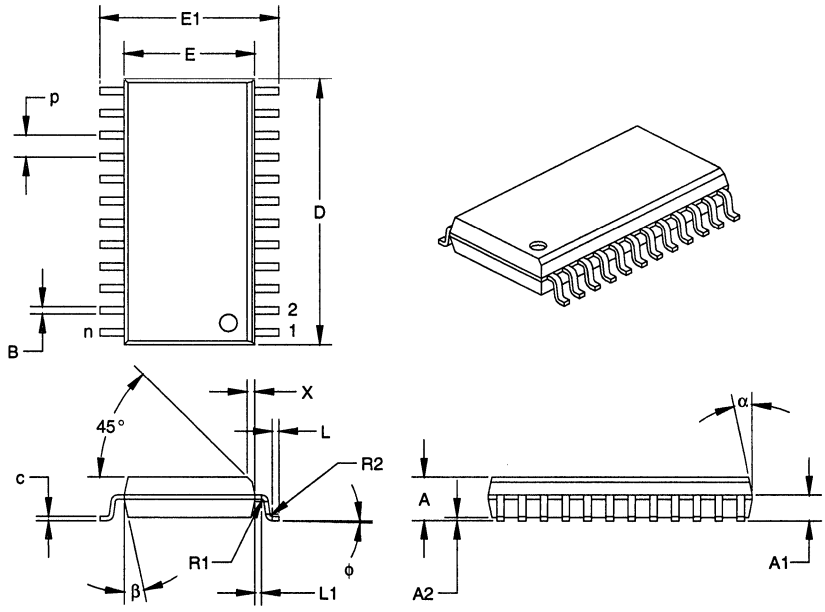
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-013 AC

Packaging Diagrams and Parameters

Package Type: K04-098 24-Lead Plastic Small Outline (SO) – Wide, 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		24			24	
Overall Pack. Height	A	0.095	0.100	0.105	2.41	2.54	2.67
Shoulder Height	A1	0.051	0.059	0.067	1.30	1.50	1.70
Standoff	A2	0.004	0.008	0.012	0.10	0.20	0.30
Molded Package Length	D‡	0.599	0.606	0.612	15.21	15.38	15.54
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.396	0.406	0.416	10.06	10.31	10.57
Chamfer Distance	X	0.010	0.018	0.025	0.25	0.44	0.64
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Lower Lead Width	B†	0.013	0.017	0.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

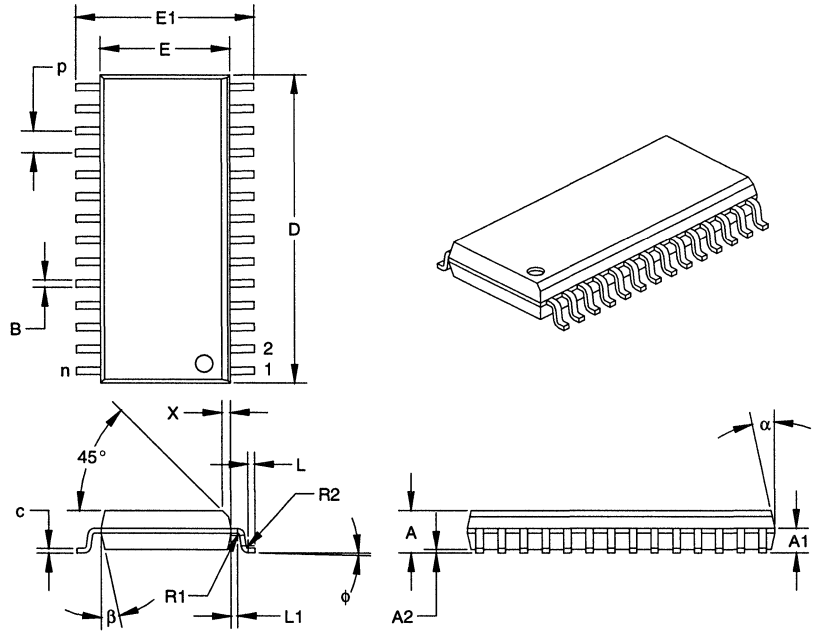
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-013 AD

Packaging Diagrams and Parameters

Package Type: K04-052 28-Lead Plastic Small Outline (SO) – Wide, 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		28			28	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D‡	0.700	0.706	0.712	17.78	17.93	18.08
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B†	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

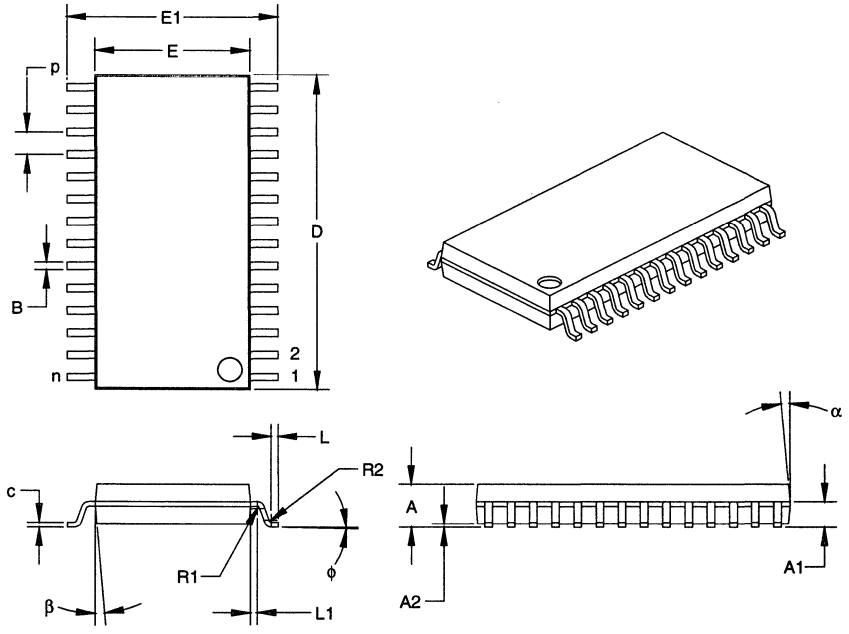
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-013 AE

Packaging Diagrams and Parameters

Package Type: K04-066 28-Lead Plastic Small Outline (SO) – Wide, 330 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		28			28	
Overall Pack. Height	A	0.090	0.097	0.104	2.29	2.46	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D‡	0.700	0.706	0.712	17.78	17.93	18.08
Molded Package Width	E‡	0.340	0.345	0.350	8.64	8.76	8.89
Outside Dimension	E1	0.463	0.470	0.477	11.76	11.94	12.12
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B†	0.014	0.017	0.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

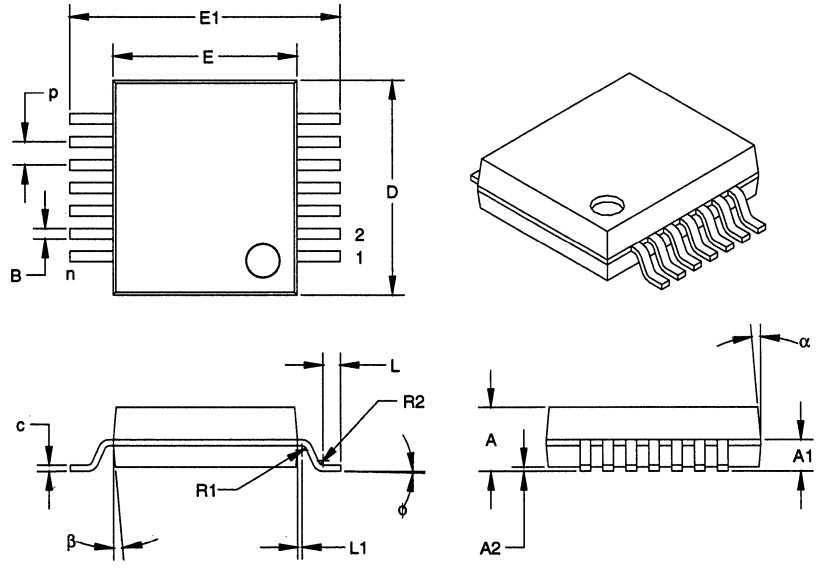
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-059 AC

Packaging Diagrams and Parameters

Package Type: K04-103 14-Lead Plastic Shrink Small Outline (SS) – 5.30 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		14			14	
Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D‡	0.239	0.244	0.249	6.07	6.20	6.33
Molded Package Width	E‡	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B†	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

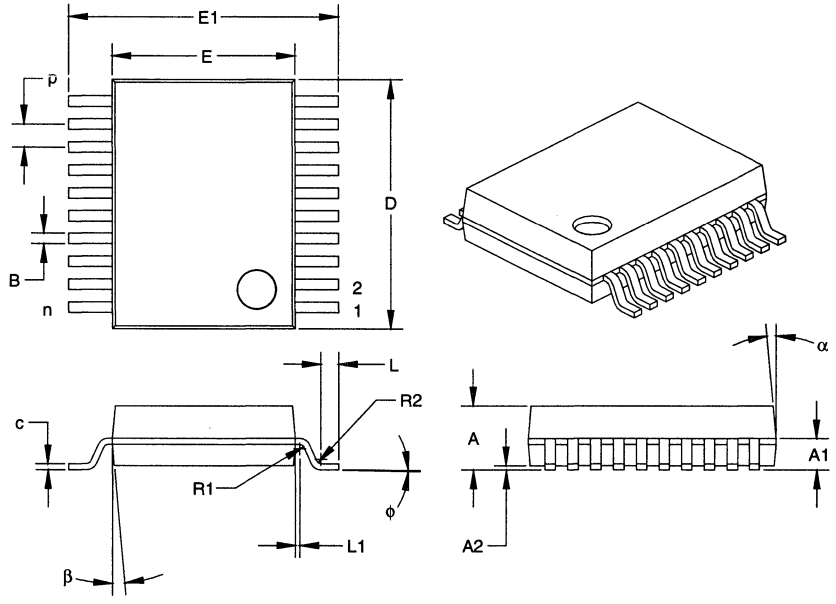
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-150 AB

Packaging Diagrams and Parameters

Package Type: K04-072 20-Lead Plastic Shrink Small Outine (SS) – 5.30 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		20			20	
Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D‡	0.278	0.283	0.289	7.07	7.20	7.33
Molded Package Width	E‡	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B†	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

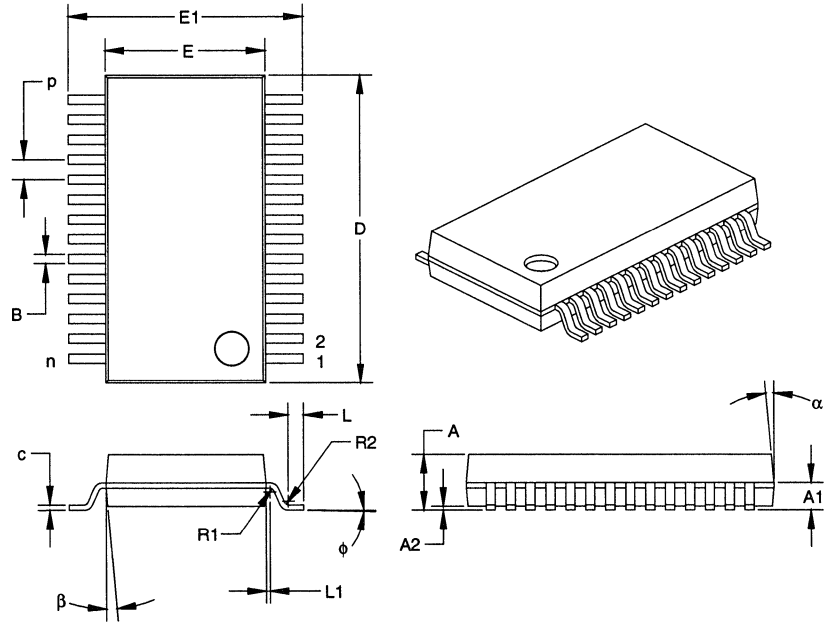
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-150 AE

Packaging Diagrams and Parameters

Package Type: K04-073 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		28			28	
Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D‡	0.396	0.402	0.407	10.07	10.20	10.33
Molded Package Width	E‡	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B†	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

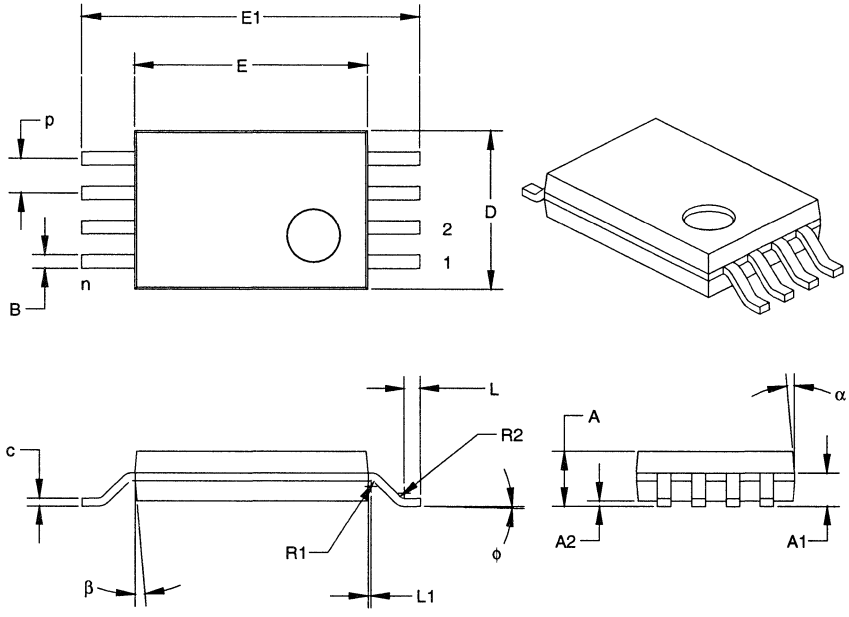
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-150 AH

Packaging Diagrams and Parameters

Package Type: K04-086 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		8			8	
Overall Package Height	A	0.039	0.041	0.043	1.00	1.05	1.10
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Molded Package Length	D‡	0.114	0.118	0.122	2.90	3.00	3.10
Molded Package Width	E‡	0.169	0.173	0.177	4.30	4.40	4.50
Outside Dimension	E1	0.246	0.251	0.256	6.25	6.38	6.50
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.007	0.010	0.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

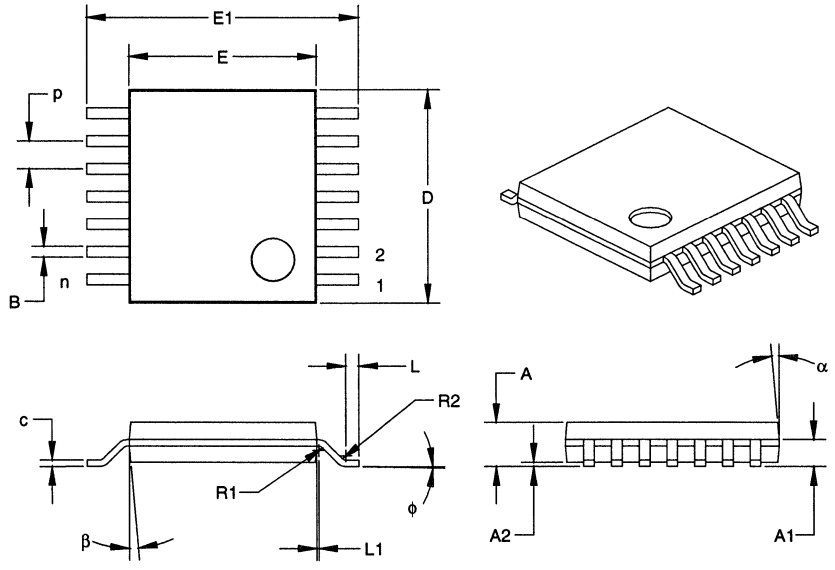
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-153 AA

Packaging Diagrams and Parameters

Package Type: K04-087 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		14			14	
Overall Package Height	A	0.039	0.041	0.043	1.00	1.05	1.10
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Molded Package Length	D‡	0.193	0.197	0.201	4.90	5.00	5.10
Molded Package Width	E‡	0.169	0.173	0.177	4.30	4.40	4.50
Outside Dimension	E1	0.246	0.251	0.256	6.25	6.38	6.50
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.007	0.010	0.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

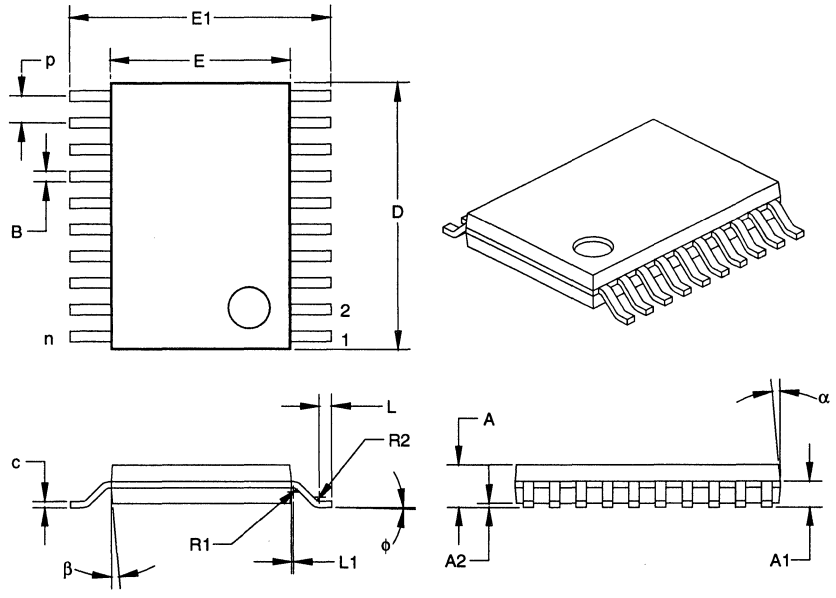
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-153 AB-1

Packaging Diagrams and Parameters

Package Type: K04-088 20-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		20			20	
Overall Package Height	A	0.039	0.041	0.043	1.00	1.05	1.10
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Molded Package Length	D‡	0.252	0.256	0.260	6.40	6.50	6.60
Molded Package Width	E‡	0.169	0.173	0.177	4.30	4.40	4.50
Outside Dimension	E1	0.246	0.251	0.256	6.25	6.38	6.50
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.007	0.010	0.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

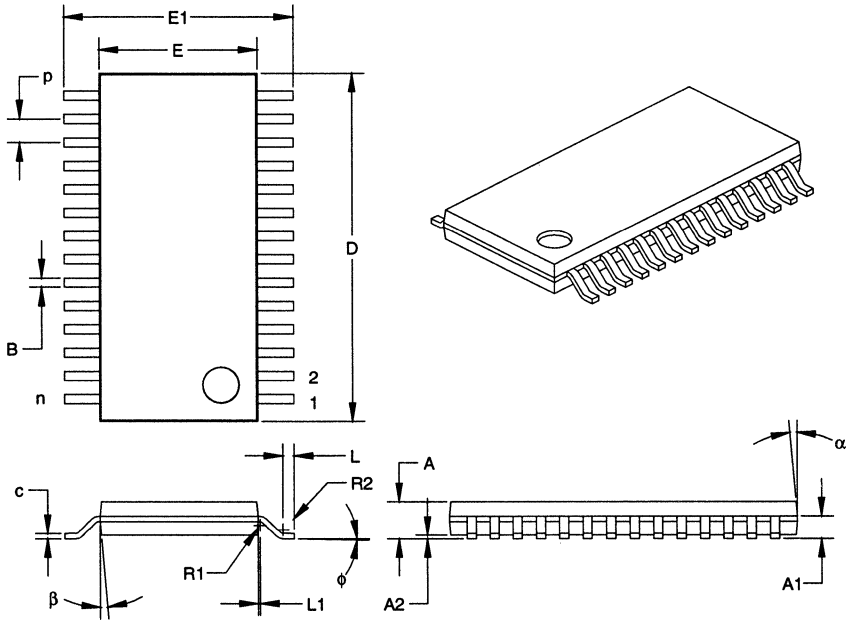
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-153 AC

Packaging Diagrams and Parameters

Package Type: K04-089 28-Lead Thin Shrink Small Outline (ST) – 4.4 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		28			28	
Overall Package Height	A	0.039	0.041	0.043	1.00	1.05	1.10
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Molded Package Length	D‡	0.378	0.382	0.386	9.60	9.70	9.80
Molded Package Width	E‡	0.169	0.173	0.177	4.30	4.40	4.50
Outside Dimension	E1	0.246	0.251	0.256	6.25	6.38	6.50
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.007	0.010	0.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

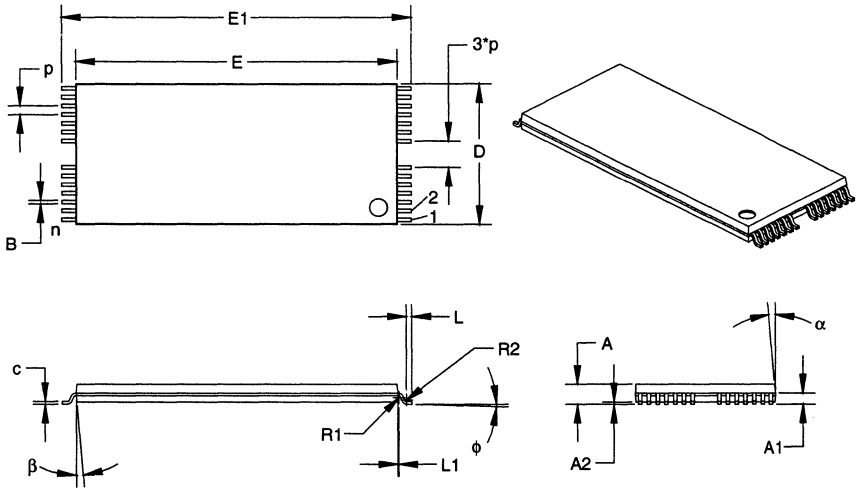
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MO-153 AE

Packaging Diagrams and Parameters

Package Type: K04-067 28-Lead Plastic Thin Small Outline (TS) – 8 x 20 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.020			0.50	
Number of Pins	n		28			28	
Overall Package Height	A	0.039	0.045	0.050	1.00	1.14	1.27
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.000	0.005	0.010	0.00	0.13	0.25
Molded Package Length	D‡	0.311	0.317	0.323	7.90	8.05	8.20
Molded Package Width	E‡	0.720	0.724	0.728	18.30	18.40	18.50
Outside Dimension	E1	0.780	0.787	0.795	19.80	20.00	20.20
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	ϕ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.004	0.006	0.008	0.10	0.15	0.20
Lower Lead Width	B†	0.006	0.008	0.010	0.15	0.20	0.25
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

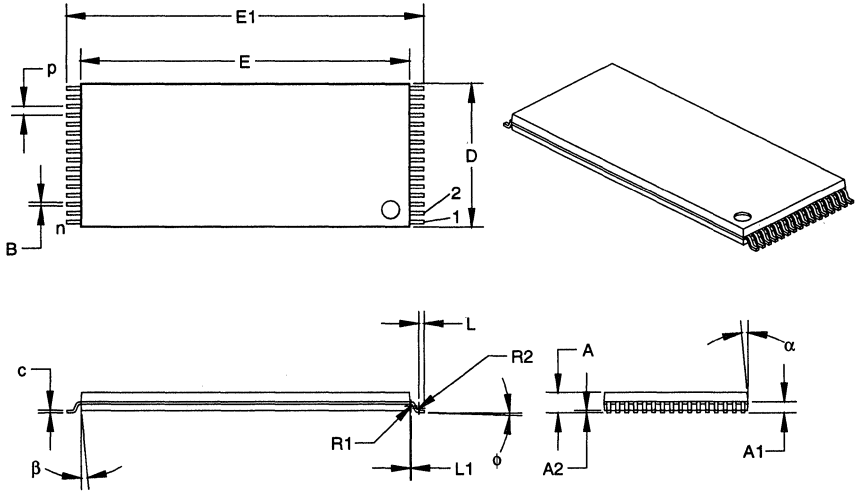
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

EIAJ equivalent: IC-74-2-3

Packaging Diagrams and Parameters

Package Type: K04-068 32-Lead Plastic Thin Small Outline (TS) – 8 x 20 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.020			0.50	
Number of Pins	n		32			32	
Overall Package Height	A	0.039	0.045	0.050	1.00	1.14	1.27
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.000	0.005	0.010	0.00	0.13	0.25
Molded Package Length	D‡	0.311	0.317	0.323	7.90	8.05	8.20
Molded Package Width	E‡	0.720	0.724	0.728	18.30	18.40	18.50
Outside Dimension	E1	0.780	0.787	0.795	19.80	20.00	20.20
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	φ	0	3	5	0	3	5
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.004	0.006	0.008	0.10	0.15	0.20
Lower Lead Width	B†	0.006	0.008	0.010	0.15	0.20	0.25
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

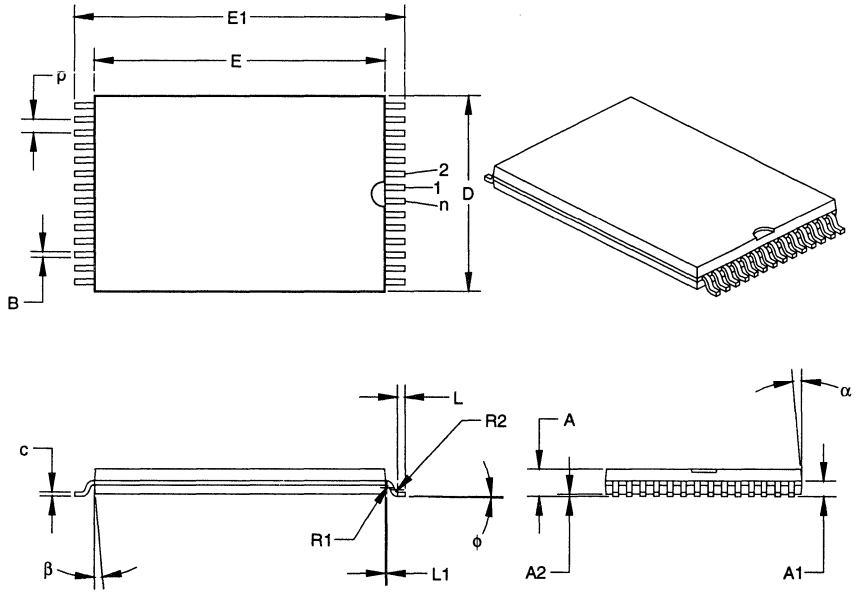
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

EIAJ equivalent: IC-74-2-3

Packaging Diagrams and Parameters

Package Type: K04-075 28-Lead Plastic Very Small Outline (VS) – 8 x 13.4 mm



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.022			0.55	
Number of Pins	n		28			28	
Overall Package Height	A	0.039	0.044	0.049	1.00	1.13	1.25
Shoulder Height	A1	0.020	0.025	0.030	0.51	0.64	0.76
Standoff	A2	0.000	0.004	0.008	0.00	0.10	0.20
Molded Package Length	D‡	0.311	0.315	0.319	7.90	8.00	8.10
Molded Package Width	E‡	0.461	0.465	0.469	11.70	11.80	11.90
Outside Dimension	E1	0.516	0.528	0.539	13.10	13.40	13.70
Shoulder Radius	R1	0.000	0.004	0.010	0.00	0.10	0.25
Gull Wing Radius	R2	0.000	0.004	0.010	0.00	0.10	0.25
Foot Length	L	0.007	0.012	0.017	0.18	0.30	0.43
Foot Angle	ϕ	0	3	5	0	3	5
Radius Centerline	L1	0.000	0.002	0.005	0.00	0.05	0.13
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B†	0.006	0.009	0.012	0.15	0.23	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	b	0	5	10	0	5	10

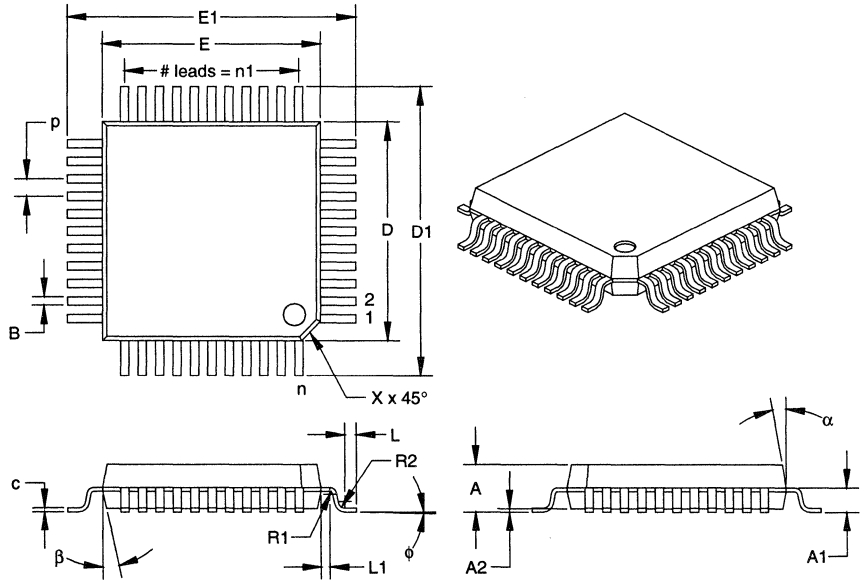
* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

Packaging Diagrams and Parameters

Package Type: K04-071 44-Lead Plastic Quad Flatpack (PQ)
10x10x2 mm Body, 1.6/0.15 mm Lead Form



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.031			0.80	
Number of Pins	n		44			44	
Pins along Width	n1		11			11	
Overall Pack. Height	A	0.079	0.086	0.093	2.00	2.18	2.35
Shoulder Height	A1	0.032	0.044	0.056	0.81	1.11	1.41
Standoff	A2	0.002	0.006	0.010	0.05	0.15	0.25
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.012	0.015	0.13	0.30	0.38
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	ϕ	0	3.5	7	0	3.5	7
Radius Centerline	L1	0.011	0.016	0.021	0.28	0.41	0.53
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.23
Lower Lead Width	B†	0.012	0.015	0.018	0.30	0.37	0.45
Outside Tip Length	D1	0.510	0.520	0.530	12.95	13.20	13.45
Outside Tip Width	E1	0.510	0.520	0.530	12.95	13.20	13.45
Molded Pack. Length	D‡	0.390	0.394	0.398	9.90	10.00	10.10
Molded Pack. Width	E‡	0.390	0.394	0.398	9.90	10.00	10.10
Pin 1 Corner Chamfer	X	0.025	0.035	0.045	0.635	0.89	1.143
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	12	15	5	12	15

* Controlling Parameter.

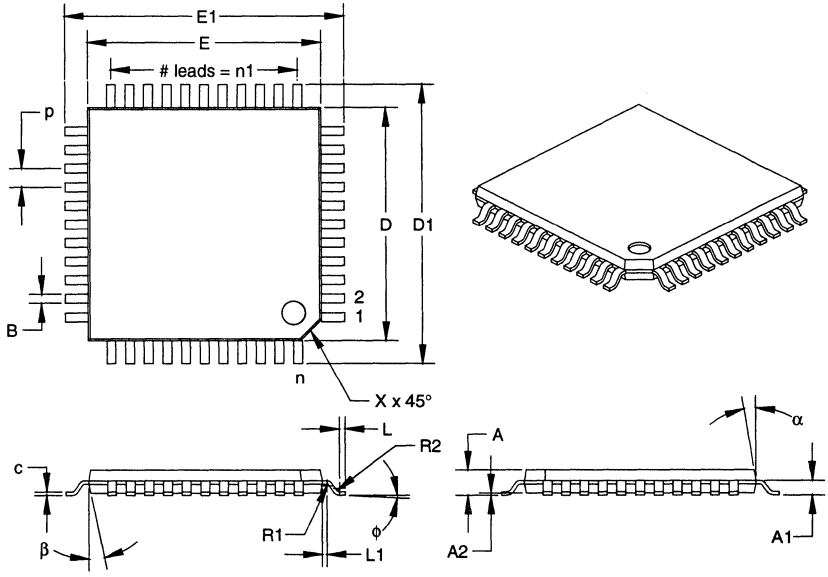
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-022 AB

Packaging Diagrams and Parameters

Package Type: **K04-076 44-Lead Plastic Thin Quad Flatpack (PT)**
10x10x1 mm Body, 1.0/0.1 mm Lead Form



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.031			0.80	
Number of Pins	n		44			44	
Pins along Width	n1		11			11	
Overall Pack. Height	A	0.039	0.043	0.047	1.00	1.10	1.20
Shoulder Height	A1	0.015	0.025	0.035	0.38	0.64	0.89
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Shoulder Radius	R1	0.003	0.003	0.010	0.08	0.08	0.25
Gull Wing Radius	R2	0.003	0.006	0.008	0.08	0.14	0.20
Foot Length	L	0.005	0.010	0.015	0.13	0.25	0.38
Foot Angle	φ	0	3.5	7	0	3.5	7
Radius Centerline	L1	0.003	0.008	0.013	0.08	0.20	0.33
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.012	0.015	0.018	0.30	0.38	0.45
Outside Tip Length	D1	0.463	0.472	0.482	11.75	12.00	12.25
Outside Tip Width	E1	0.463	0.472	0.482	11.75	12.00	12.25
Molded Pack. Length	D‡	0.390	0.394	0.398	9.90	10.00	10.10
Molded Pack. Width	E‡	0.390	0.394	0.398	9.90	10.00	10.10
Pin 1 Corner Chamfer	X	0.025	0.035	0.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	12	15	5	12	15

* Controlling Parameter.

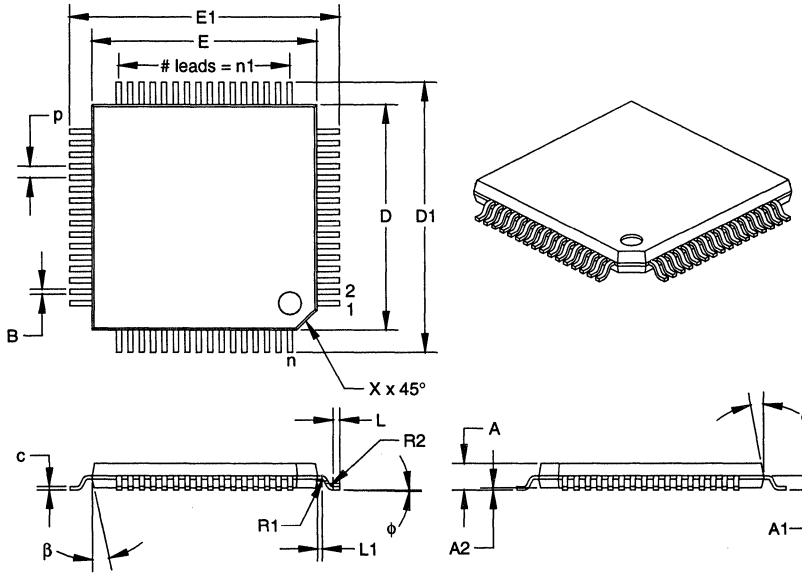
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-026 ACB

Packaging Diagrams and Parameters

Package Type: K04-085 64-Lead Plastic Thin Quad Flatpack (PT)
10x10x1 mm Body, 1.0/0.1 mm Lead Form



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.020			0.50	
Number of Pins	n		64			64	
Pins along Width	n1		16			16	
Overall Pack. Height	A	0.039	0.043	0.047	1.00	1.10	1.20
Shoulder Height	A1	0.015	0.025	0.035	0.38	0.64	0.89
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Shoulder Radius	R1	0.003	0.003	0.010	0.08	0.08	0.25
Gull Wing Radius	R2	0.003	0.006	0.008	0.08	0.14	0.20
Foot Length	L	0.005	0.012	0.015	0.13	0.30	0.38
Foot Angle	φ	0	3.5	7	0	3.5	7
Radius Centerline	L1	0.003	0.008	0.013	0.08	0.20	0.33
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.007	0.009	0.011	0.17	0.22	0.27
Outside Tip Length	D1	0.463	0.472	0.482	11.75	12.00	12.25
Outside Tip Width	E1	0.463	0.472	0.482	11.75	12.00	12.25
Molded Pack. Length	D‡	0.390	0.394	0.398	9.90	10.00	10.10
Molded Pack. Width	E‡	0.390	0.394	0.398	9.90	10.00	10.10
Pin 1 Corner Chamfer	X	0.025	0.035	0.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	12	15	5	12	15

* Controlling Parameter.

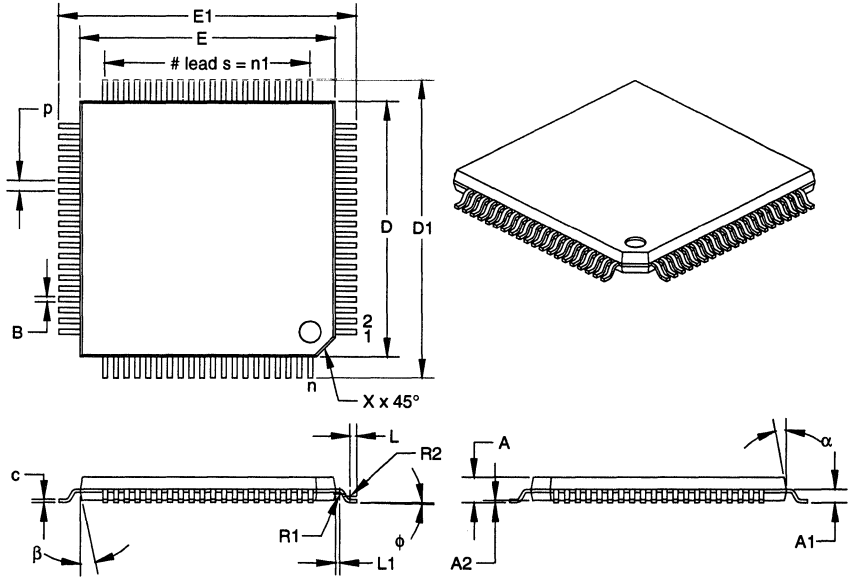
† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-026 ACD

Packaging Diagrams and Parameters

Package Type: K04-092 80-Lead Plastic Thin Quad Flatpack (PT)
12x12x1 mm Body, 1.0/0.1 mm Lead Form



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.020			0.50	
Number of Pins	n		80			80	
Pins along Width	n1		20			20	
Overall Pack. Height	A	0.039	0.043	0.047	1.00	1.10	1.20
Shoulder Height	A1	0.015	0.025	0.035	0.38	0.64	0.89
Standoff	A2	0.002	0.004	0.006	0.05	0.10	0.15
Shoulder Radius	R1	0.003	0.003	0.010	0.08	0.08	0.25
Gull Wing Radius	R2	0.003	0.006	0.008	0.08	0.14	0.20
Foot Length	L	0.005	0.012	0.015	0.13	0.30	0.38
Foot Angle	ϕ	0	3.5	7	0	3.5	7
Radius Centerline	L1	0.003	0.008	0.013	0.08	0.20	0.33
Lead Thickness	c	0.004	0.006	0.008	0.09	0.15	0.20
Lower Lead Width	B†	0.007	0.009	0.011	0.17	0.22	0.27
Outside Tip Length	D1	0.542	0.551	0.561	13.77	14.00	14.25
Outside Tip Width	E1	0.542	0.551	0.561	13.77	14.00	14.25
Molded Pack. Length	D‡	0.462	0.472	0.482	11.73	12.00	12.24
Molded Pack. Width	E‡	0.462	0.472	0.482	11.73	12.00	12.24
Pin 1 Corner Chamfer	X	0.025	0.035	0.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	12	15	5	12	15

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-026 ADD

Packaging Diagrams and Parameters

NOTES:

Product Tape and Reel Specifications

FIGURE 1: EMBOSSED CARRIER DIMENSIONS (8, 12,16, AND 24MM TAPE ONLY)

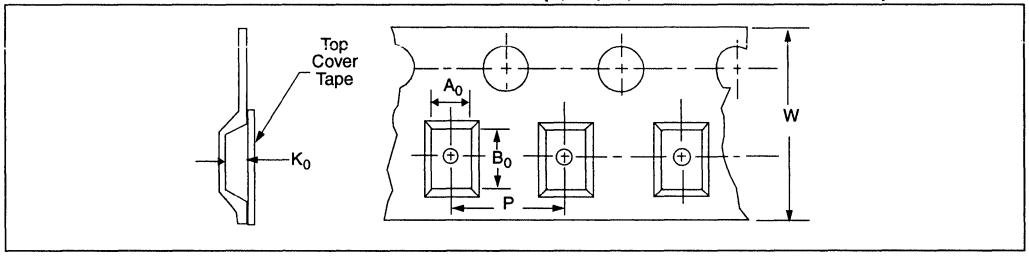
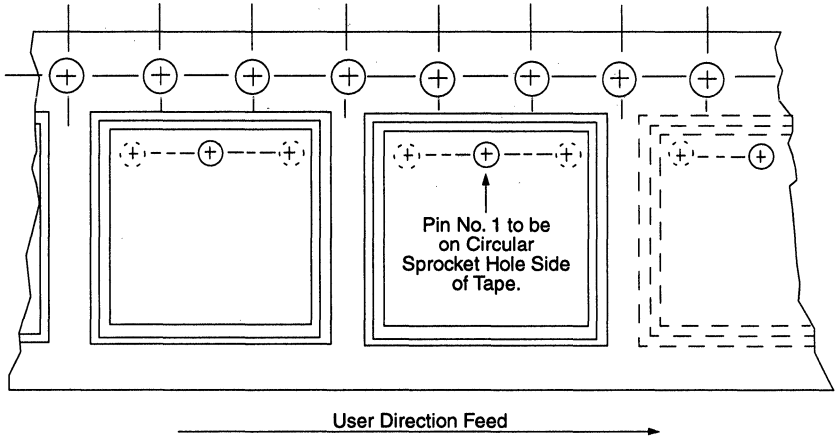


TABLE 2: CARRIER TAPE/CAVITY DIMENSIONS

Case Outline	Package Type		Carrier Dimensions		Cavity Dimensions			Output Quantity Units	Reel Diameter in mm
			W mm	P mm	A0 mm	B0 mm	K0 mm		
SN	SOIC .150"	8L	12	8	6.4	5.2	2.1	3300	330
SO	SOIC .300"	18L	24	12	10.9	13.3	3.0	1600	330
SO	SOIC .300"	20L	24	12	10.9	13.3	3.0	1600	330
SO	SOIC .300"	28L	24 24	12 12	10.9 11.1	18.3 18.5	3.0 3.0	1600 1600	330 330
L	PLCC	28L	24	16	13.0	13.0	4.9	750	330
L	PLCC	32L	24	16	13.1	15.5	3.9	900	330
L	PLCC	44L	32 32	24 24	18.0 18.0	18.0 18.0	4.9 5.0	500 500	330
SM	SOIC .208"	8L	16	12	8.3	5.7	2.2	2100	330
SL	SOIC .150"	14L	16	8	6.5	9.5	2.1	2600	330
TS	TSOP	28L/ 32L	32	16	8.6	20.6	2.1	1500	330
SS	SSOP	20L	16	12	8.2	7.6	3.0	1600	330
SS	SSOP	28L	24	12	8.4	10.9	2.4	2100	330
PQ	MQFP	44L	24	24	16.6	16.6	2.8	900	330
PT	TQFP	44L	24	24	16.6	16.6	2.1	1200	330
VS	VSOP	28L	24	12	8.7	13.9	2.1	2500	330

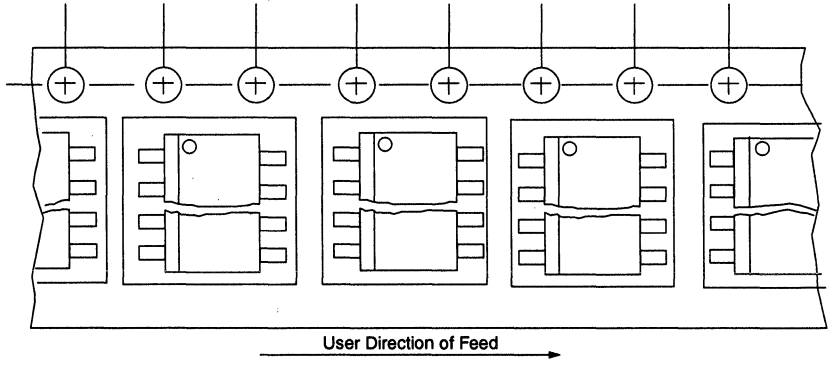
FIGURE 3: MECHANICAL POLARIZATION (PCC AND LCC DEVICES)



Note 1: Top view shown with cover tape removed.

2: Only single sprocket tape shown - polarization for double sprocket tape (32 mm and wider) is the same as shown.

FIGURE 4: MECHANICAL POLARIZATION (SOIC DEVICES)



Note 1: Top view shown with cover tape removed.

2: Only single sprocket tape shown – polarized for double sprocket tape (32 mm and wider) is the same as shown.

Overview of Microchip Die/Wafer Support

INTRODUCTION

Microchip Technology Inc. devices are available in wafer form and in die form. All products sold in die or wafers have been characterized and qualified according to the requirements of Microchip Technology Inc. Specifications SPI-41014, "Characterization and Qualification of Integrated Circuits," and QCI-39000, "Worldwide Quality Conformance Requirements."

PRODUCT INTEGRITY

Product supplied in die or wafer form are fully tested and characterized. Die or Wafers are inspected to Microchip Technology Inc. Specification, QCI-30014.

CAUTION

Some EEPROM devices use EPROM cells for device configuration. Exposure to ultra-violet light must be avoided. Exposure to ultra-violet light may cause the device to operate improperly.

Extreme care is urged in the handling and assembly of these products since they are susceptible to damage from electro-static discharge.

ORDERING INFORMATION

Die sales must be conducted by contacting your Microchip Sales Office.

To order or obtain information (on pricing or delivery) for a specific device, use one of the following part numbers:

Devices in Waffle Pack
DEVICE_NUMBER/S

Devices in Wafer form
DEVICE_NUMBER/W
DEVICE_NUMBER/WF

where DEVICE_NUMBER is the device that you require. The S specifies die in a waffle pack while a W specifies wafer sales, and WF specifies sawn wafer on frames.

ELECTRICAL SPECIFICATIONS

The functional and electrical specifications of Microchip devices in die form are identical to those of a packaged version. Please refer to individual data sheets for complete details.

QTP

Quick Turnaround Production (QTP) applies only to EPROM and EEPROM microcontrollers.

With QTP devices, the program memory array is only tested against the code provided. This method ensures that the device will operate correctly as programmed, but does not ensure that every program memory bit can be programmed to every state.

Note: Do not erase QTP devices and program them with a different code.

EPROM

EPROM devices are supplied as fully erased programmable parts that are UV erasable and re-programmable by the user (except for QTP and SQTP devices).

EEPROM

EEPROM devices may not be supplied in a fully erased state, but are re-programmable by the user (except for QTP and SQTP devices).

ROM

ROM devices are supplied as fully programmed parts (program memory only). These are not reprogrammable by the user.

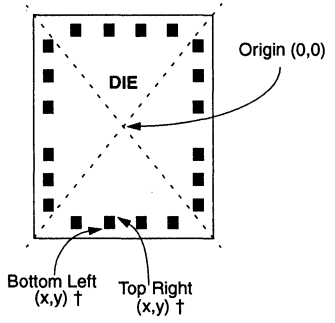
DIE MECHANICAL SPECIFICATIONS

Refer to the individual data sheet for these specifications.

BOND PAD COORDINATES

The die figures have associated bond pad coordinates. These coordinates assist in the attaching of the bond wire to the die. All the dimensions of these coordinates are in micrometers (μm) unless otherwise specified. The origin for the coordinates is the center of the die, as shown in Figure 1. Refer to the Microchip Die Specification sheet for openings and pitch.

FIGURE 1: DIE COORDINATE ORIGIN



† All dimensions in μm unless specified otherwise.

The die is capable of thermosonic gold or ultrasonic wire bonding. Die meet the minimum conditions of MIL-STD 883, Method 2011 on "Bond Strength (Destructive Bond Pull Test)". The Bond Pad metallization is silicon doped aluminum.

SUBSTRATE BONDING

Substrate bonding may be required on certain product families. For more information refer to the die specification sheet.

SHIPPING OPTIONS

DIE Form Shipping

Microchip product in die form can be shipped in waffle-pack. The waffle pack has sufficient cavity area to restrain the die, while maintaining their orientation. Lint free paper inserts are placed over the waffle packs, and each pack is secured with a plastic locking clip. Groups of waffle packs are assembled into sets for shipment. A label with lot number, quantity, and part number is attached.

These waffle packs are hermetically sealed in bags.

Wafer Form

Products may also be shipped in wafer form (see ordering information). Wafers are shipped in a wafer tub. The tub is padded with non-conductive foam. Lint free paper inserts are placed around each wafer. A label with lot number, quantity, and part number is attached.

Sawn Wafer on Frames

Products may also be shipped on wafer frames. Wafers are mounted on plastic frames and 100% sawn through. Sawn wafer on frames may be shipped in bulk (25 wafers per carrier) or in a single wafer in a carrier. A label with lot number, quantity, and part number is attached with each shipment.

Storage Procedures

Temperature and humidity greatly affect the storage life of die. It is recommended that the die be used as soon as possible after receipt.

Upon receipt, the sealed bags should be stored in a cool and dry environment (25°C and 25% relative humidity). In these conditions, sealed bags have a shelf life of 12 months. Temperatures or humidities greater than these will reduce the storage life.

Once a bag containing waffle packs has been opened, the devices should be assembled and encapsulated within 48 hours (assuming, 25°C and 25% humidity).

MICROCHIP

SECTION 12
WORLDWIDE SALES ADDRESS LISTINGS

Factory Representatives 12-1
Distributors 12-7
Factory Sales 12-21

Factory Representatives

AFRICA

Tempe Technologies Pty. Ltd.
62 Oude Kaap Estate
Dowerglen Edenvale
South Africa
TEL: 27-11-4520530
FAX: 27-11-4520543

CANADA

Alberta

Enerlec Sales Ltd.
#103, 155 Glendeer Circle SE
Calgary, Alberta T2H 2S8
Canada
TEL: 403 777-1550
FAX: 403 777-1553
Email: asutti@enerlec.com

British Columbia

Enerlec Sales Ltd.
#7 3671 Viking Way
Richmond BC V6V 1W1
Canada
TEL: 604 273-0882
FAX: 604 273-0884
Email: rayq@enerlec.com

Ontario

Pipe-Thompson
6 Bentworth Cresent
Nepean ON K2G 3X2
Canada
TEL: 613 596-1908
FAX: 613 596-2905
Email: pipethom@idirect.com

Pipe-Thompson
4 Robert Speck Parkway, Suite 1170
Mississauga ON L4Z 1S1
Canada
TEL: 905 281-8281
FAX: 905 281-8550
Email: pipethom@idirect.com

Quebec

Pipe-Thompson
150, Plante
Ste-Madeleine QC J0H 1S0
Canada
TEL: 514 795-3944
FAX: 514 795-6644
Email: pipethom@idirect.com

Pipe-Thompson
4285 Rue Acres
Pierrefonds QC H9H 2T9
Canada
TEL: 514 624-8760
FAX: 514 624-0337
Email: pipethom@idirect.com

EUROPE

Austria

Active Rep GmbH
Wiessenstr. 40
A-4600 Wels
Austria
TEL: 43-7242-572463
FAX: 43-7242-572464

Belgium

Active Rep GmbH
Vertrieb Nord
Obenitterstr 21
D-42719 Solingen
Germany
TEL: 49-212-230400
FAX: 49-212-23-04-023

Czechoslovakia

Active Rep GmbH
Wiessenstr. 40
A-4600 Wels
Austria
TEL: 43-7242-572463
FAX: 43-7242-572464

England

Arizona Technologies
Unit 21, Loughborough Technology Centre
Epinal Way
Leicestershire LE11 OQE
England
TEL: 44-1509-611277
FAX: 44-1509-611288

France

LeadREP
99 route de Versailles
91160 Champlan
France
TEL: 33-1-69-79-9350
FAX: 33-1-69-79-9359
Email: carole.nomblot@microchip.com

Germany

Active Rep GmbH
Vertrieb Nord
Obenitterstr 21
D-42719 Solingen
Germany
TEL: 49-212-230400
FAX: 49-212-23-04-023

Active Rep GmbH
Augsburgerstr. 43
D-82110 Germering
Germany
TEL: 49-89-89-42-96-60
FAX: 49-89-89-42-96-62

Active Rep GmbH
Vertrieb Nord
Emil Pleitner Gang 2
D-26135 Oldenburg
Germany
TEL: 49-441-2069986
FAX: 49-441-2069989

Active Rep GmbH
Schubertstrasse 35
D-75438 Knittlingen
Germany
TEL: 49-7043-9329-0
FAX: 49-7043-3-34-92

Hungary

Active Rep GmbH
Wiessenstr. 40
A-4600 Wels
Austria
TEL: 43-7242-572463
FAX: 43-7242-572464

EUROPE *(Continued)*

Ireland

Eltech Agencies Ltd.
7 - 10 Robert Scott House
Patrick's Quay
Co. Cork
Ireland
TEL: 353-21-509-366
FAX: 353-21-509-344

Netherlands

Active Rep GmbH
Vertrieb Nord
Obenitterstr 21
D-42719 Solingen
Germany
TEL: 49-212-230400
FAX: 49-212-23-04-023

Norway

Component-74 Eidsvold
P. O. Box 9
N-2070 Raholt
Norway
TEL: 47-63-956010
FAX: 47-63-956019

Scotland

Juniper Solutions
Enterprise House
Springkerse Business Park
Sterling FK7 7UF
Scotland
TEL: 44-1786-446220
FAX: 44-1786-446223

Slovakia

Active Rep GmbH
Wiessenstr. 40
A-4600 Wels
Austria
TEL: 43-7242-572463
FAX: 43-7242-572464

Spain

LeadREP
99 route de Versailles
91160 Champlan
France
TEL: 33-1-69-79-9350
FAX: 33-1-69-79-9359
Email: carole.nomblot@microchip.com

Sweden

Memec Scandinavia AB
Sehlstedsgatan 6
115 28 Stockholm
Sweden
TEL: 46-8-459-79-00
FAX: 46-8-459-79-99

Switzerland

Mero (Microchip Engineering & Rep. Organization)
Switzerland/Liechtenstein
Heuerweg 1
CH-5605 Dottikon
Switzerland
TEL: 41-56-610-15-01
FAX: 41-56-610-15-03

SOUTH AMERICA

South America (except Brazil)

Ibars Electronics Corp
10020 N.W. 6th CT
Pembroke Pines FL 33024
USA
Tel: 954 430-3740
Fax: 954 430-3763

Brazil

Artimar, Ltda.
Rua Marques De Itu
70 - 10 Andar
01223 São Paulo
Brazil
Tel: 55-11-231-0277
Fax: 55-11-255-0511

UNITED STATES

Alaska

Micro Sales
2122-112th Avenue N.E.
Bellevue WA 98004-2947
USA
TEL: 206 451-0568
FAX: 206 453-0092
Email: bob@microsales.com

Alabama

Concord Components
190 Lime Quarry Road, Suite 102
Madison AL 35758
USA
TEL: 205 772-8883
FAX: 205 772-8262
Email: ccrga@concord-rep.com

Arizona

Western High Tech
7025 East Greenway Parkway
Suite 550
Scottsdale AZ 85254
USA
TEL: 602 993-9700
FAX: 602 993-9707
Email: whigh@aol.com

California

Northern California
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
TEL: 408-436-7950
FAX: 408-436-7955

Southern California
Los Angeles Area
Unitec Sales Associates (CTI)
23461 South Pointe Drive, Suite 120
Laguna Hills CA 92653
USA
TEL: 714 699-6120
FAX: 714 699-6132
Email: hempel@unitecsales.com

San Diego Area
Eagle Tech. Sales
1900 Sunset Drive, Suite A
Escondido CA 92025
USA
TEL: 760 743-6550
FAX: 760 743-6585
Email: eagles1900@aol.com

Colorado

Colorado Springs
Western Region Mktg.
6328 Brightstar Drive
Colorado Springs CO 80910
USA
TEL: 303 548-8282
FAX: 303 548-0462
Email: garth@wrmktg.com

Denver
Western Region Mktg.
9176 Marshall Place
Westminster CO 80030
USA
TEL: 303 428-8088
FAX: 303 426-8585
Email: garth@wrmktg.com

Connecticut

Enfield
SJ New England
12 Gem Grove
Enfield CT 06082
USA
TEL: 860 749-1531
FAX: 860 Same as Phone
Email: sjneweng@aol.com

Naugatuck
SJ New England
15 Coventry Lane
Naugatuck CT 06770
USA
TEL: 203 723-4707
FAX: 203 723-1629
Email: sjneweng@aol.com

Branford
SJ New England
9 Tanglewood Drive
Branford CT 06405
USA
TEL: 203 488-7568
FAX: 203 488-8149
Email: sjneweng@aol.com

UNITED STATES *(Continued)*

Delaware

SJ Mid-Atlantic
131-D Gaither Drive
Mt. Laurel NJ 08054
USA
TEL: 609 866-1234
FAX: 609 866-8627
Email: sjmidatl@pipeline.com

District of Columbia

SJ Chesapeake
900 South Washington Street, Suite 307
Falls Church VA 22046
USA
TEL: 703 533-2233
FAX: 703 533-2236
Email: sjches@pipeline.com

Florida

Altamonte Springs
Electramark Fla., Inc.
401 Whooping Loop, Suite 1565
Altamonte Springs FL 32701
USA
TEL: 407 830-0844
FAX: 407 830-0847
Email: eletrmkfla@aol.com

Margate
Electramark Fla., Inc.
767 South State Road 7, Suite 22B
Margate FL 33068
USA
TEL: 954 974-9933
FAX: 954 974-6616
Email: eletrmkfla@aol.com

Tampa
Electramark Fla., Inc.
2910 West Waters Avenue
Tampa FL 33614
USA
TEL: 813 915-1177
FAX: 813 915-1188
Email: eletrmkfla@aol.com

Georgia

Concord Components
6825 Jimmy Carter Boulevard
Suite 1303
Norcross GA 30071
USA
TEL: 770 416-9597
FAX: 770 441-0790
Email: ccral@concord-rep.com

Idaho

Micro Sales
1905 NW 169th Place, Suite D
Beaverton OR 97006
USA
TEL: 503 645-2841
FAX: 503 645-3754
Email: mariley@teleport.com

Illinois

Northern
Janus, Inc.
650 East Devon Avenue, Suite 170
Itasca IL 60143
USA
TEL: 630 250-9650
FAX: 630 250-8761
Email: janusil@janusinc.com

Southern
Spectrum Sales
5494 Brown Rd, Suite 124
St Louis MO 63042
USA
TEL: 314 731-4477
FAX: 314 731-1332
Email: spectrumkc@aol.com

Indiana

Sellersburg
Electro Reps
60 Buck Blvd.
Sellersburg IN 47172
USA
TEL: 812 246-2342
FAX: 812 246-3286
Email: kathy.samuels@microchip.com

Fort Wayne
Electro Reps
125 Airport North Office Park
Fort Wayne IN 46825
USA
TEL: 219 489-8205
FAX: 219 489-8408
Email: kathy.samuels@microchip.com

Indianapolis
Electro Reps
7240 Shadeland Station, Suite 275
Indianapolis IN 46256-3928
USA
TEL: 317 842-7202
FAX: 317 841-0230
Email: kathy.samuels@microchip.com

Iowa

Spectrum Sales
708 J Avenue N.E., Suite 9
Cedar Rapids IA 52402
USA
TEL: 319 366-0576
FAX: 319 366-0635
Email: spectrumkc@aol.com

Kansas

Spectrum Sales
5382 West 95th Street
Prairie Village KS 66207
USA
TEL: 913 648-6811
FAX: 913 648-6823
Email: spectrumkc@aol.com

Kentucky

Northern
Millennium Technical Sales
7155 Post Road
Dublin OH 43016
USA
TEL: 614 793-9545
FAX: 614 793-0256
Email: janet.deluca@microchip.com

Southern
Electro Reps
7240 Shadeland Station, Suite 275
indianapolis IN 46256-3928
USA
TEL: 812 842-7202
FAX: 812 841-0230
Email: kathy.samuels@microchip.com

Maine

SJ New England
Corp. Place #3
267 Boston Road
North Billerica MA 01862
USA
TEL: 508 670-8899
FAX: 508 670-8711
Email: sjneweng@aol.com

Maryland

SJ Chesapeake
900 South Washington Street, Suite 307
Falls Church VA 22046
USA
TEL: 703 533-2233
FAX: 703 533-2236
Email: sjches@pipeline.com

Massachusetts

SJ New England
Corp. Place #3
267 Boston Road
North Billerica MA 01862
USA
TEL: 978 670-8899
FAX: 978 670-8711
Email: sjneweng@aol.com

Michigan

Miltimore Sales, Inc.
3680 44th Street, Suite 100
Kentwood MI 49512
USA
TEL: 616 554-9292
FAX: 616 554-9210
Email: rwiesing@miltimore.com

Miltimore Sales, Inc.
22765 Heslip Drive
Novi MI 48375-4130
USA
TEL: 248 349-0260
FAX: 248 349-0756
Email: rwiesing@miltimore.com

UNITED STATES *(Continued)*

Minnesota

Mel Foster Company
7611 Washington Ave. South
Edina MN 55439
USA
TEL: 612 941-9790
FAX: 612 944-0634
Email: mikes@melfoster.com

Mississippi

Concord Components
190 Lime Quarry Road, Suite 102
Madison AL 35758
USA
TEL: 205 772-8883
FAX: 205 772-8262
Email: ccrga@concord-rep.com

Missouri

Spectrum Sales
5494 Brown Rd, Suite 124
St Louis MO 63042
USA
TEL: 314 731-4477
FAX: 314 731-1332
Email: spectrumkc@aol.com

Montana

Western Region Mktg.
9176 Marshall Place
Westminster CO 80030
USA
TEL: 303 428-8088
FAX: 303 426-8585
Email: garth@wrmktg.com

Nebraska

Spectrum Sales
5382 West 95th Street
Prairie Village KS 66207
USA
TEL: 913 648-6811
FAX: 913 648-6823
Email: spectrumkc@aol.com

Western High Tech
7025 East Greenway Parkway, Suite 550
Scottsdale AZ 85254
USA
TEL: 602 993-9700
FAX: 602 993-9707
Email: whigh@aol.com

New Hampshire

SJ New England
Corp. Place #3
267 Boston Road
North Billerica MA 01862
USA
TEL: 508 670-8699
FAX: 508 670-8711
Email: sjneweng@aol.com

New Jersey

Northern
Parallax
734 Walt Whitman Road
Suite 209
Melville NY 11747
USA
TEL: 516 351-1000
FAX: 516 351-1606
Email: espobob@ix.netcom.com

Southern
SJ Mid-Atlantic
131-D Gaither Drive
Mt. Laurel NJ 08054
USA
TEL: 609 866-1234
FAX: 609 866-8627
Email: sjmidatl@pipeline.com

New York

Melville
Parallax
734 Walt Whitman Road, Suite 209
Melville NY 11747
USA
TEL: 516 351-1000
FAX: 516 351-1606
Email: espobob@ix.netcom.com

Rochester
Apex Associates
1210 Jefferson Road
Rochester NY 14623
USA
TEL: 716 272-7040
FAX: 716 272-7756
Email: apex1assoc@aol.com

North Carolina

ZA Tech
4070 Barret Drive
Raleigh NC 27619
USA
TEL: 919 782-8433
FAX: 919 782-8476
Email: webmaster@za-inc.com

Ohio

Millennium Technical Sales
4700 Sunray Road
Kettering OH 45429
USA
TEL: 937 435-8650
FAX: 937 435-8570
Email: richard.mamula@microchip.com

Millennium Technical Sales
29500 Aurora Road, Suite 13
Solon OH 44139
USA
TEL: 216 349-6600
FAX: 216 349-6700
Email: janet.deluca@microchip.com

Millennium Technical Sales
7155 Post Road
Dublin OH 43016
USA
TEL: 614 793-9545
FAX: 614 793-0256
Email: janet.deluca@microchip.com

Oregon

Micro Sales
1905 NW 169th Place, Suite D
Beaverton OR 97006
USA
TEL: 503 645-2841
FAX: 503 645-3754
Email: mariley@teleport.com

Pennsylvania

Eastern
SJ Mid-Atlantic
131-D Gaither Drive
Mt. Laurel NJ 08054
USA
TEL: 609 866-1234
FAX: 609 866-8627
Email: sjmidatl@pipeline.com

Western
Millennium Technical Sales
7155 Post Road
Dublin OH 43016
USA
TEL: 614 793-9545
FAX: 614 793-0256
Email: janet.deluca@microchip.com

Millennium Technical Sales
302 Bayberry Lane
Imperial PA 15126
USA
TEL: 412 695-7661
FAX: 412 695-7870
Email: richard.mamula@microchip.com

UNITED STATES *(Continued)*

Rhode Island

SJ New England
Corp. Place #3
267 Boston Road
North Billerica MA 01862
USA
TEL: 508 670-8899
FAX: 508 670-8711
Email: sjneweng@aol.com

South Dakota

Mel Foster Company
7611 Washington Ave. South
Edina MN 55439
USA
TEL: 612 941-9790
FAX: 612 944-0634
Email: mikes@melfoster.com

South Carolina

ZA Tech
4070 Barret Drive
Raleigh NC 27619
USA
TEL: 919 782-8433
FAX: 919 782-8476
Email: webmaster@za-inc.com

Tennessee

Western Tennessee
Concord Components
190 Lime Quarry Road, Suite 102
Madison AL 35758
USA
TEL: 205 772-8883
FAX: 205 772-8262
Email: ccrga@concord-rep.com

Eastern Tennessee
ZA Tech
4070 Barret Drive
Raleigh NC 27619
USA
TEL: 919 782-8433
FAX: 919 782-8476
Email: webmaster@za-inc.com

Utah

Western Region Mktg.
3575 South West Temple, #4
Salt Lake City UT 84115
USA
TEL: 801 268-9768
FAX: 801 268-9796
Email: garth@wrmktg.com

Vermont

SJ New England
Corp. Place #3
267 Boston Road
North Billerica MA 01862
USA
TEL: 508 670-8899
FAX: 508 670-8711
Email: sjneweng@aol.com

Virginia

SJ Chesapeake
900 South Washington Street, Suite 307
Falls Church VA 22046
USA
TEL: 703 533-2233
FAX: 703 533-2236
Email: sjches@pipeline.com

West Virginia

Western Region Mktg.
9176 Marshall Place
Westminster CO 80030
USA
TEL: 412 428-8088
FAX: 412 426-8585
Email: garth@wrmktg.com

Washington

Micro Sales
2122-112th Avenue N.E.
Bellevue WA 98004-2947
USA
TEL: 425 451-0568
FAX: 425 453-0092
Email: bob@microsales.com

Wisconsin

Eastern Wisconsin
Janus, Inc.
760 Milwaukee Street
Delafield WI 53018
USA
TEL: 414 646-5420
FAX: 414 646-5421
Email: prheingans@janusinc.com

Western Wisconsin
Mel Foster Company
7611 Washington Ave. South
Edina MN 55439
USA
TEL: 612 941-9790
FAX: 612 944-0634
Email: mikes@melfoster.com

Wyoming

Western Region Mktg.
9176 Marshall Place
Westminster CO 80030
TEL: 303 428-8088
FAX: 303 426-8585

Distributors

AFRICA

South Africa

Avnet Kopp Pty Ltd.
P. O. Box 3853
Rivonia 2128
South Africa
TEL: 27-11-444-2333
FAX: 27-11-444-1706

Azona Pty. Ltd.
P.O. Box 16767
Unit 2, Lifestyle Management Park
Lyttelton 0140
South Africa
TEL: 27-12-664-1910
FAX: 27-12-664-1393

Pace Electronic Components (Pty) Ltd.
Cnr. Vanacht & Gewel Streets
P.O. Box 701
Isando 1600, Transvaal
South Africa
TEL: 27-11-9741211/6
FAX: 27-11-9741271

ASIA/PACIFIC

Australia

Avnet Pacific
Suite 9, 24 Sandgate Road
Breakfast Creek QLD 4010
Australia
TEL: 617-3262-5200
FAX: 617-3262-6161
Email: bri@avnet.com.au

Avnet Pacific
69 Walters Drive
Osbourne Park WA 6017
Australia
TEL: 619-242-4266
FAX: 619-242-4350
Email: per@avnet.com.au

Avnet Pacific
8/27 College Road
Kent Town SA 5067
Australia
TEL: 618-8362-0944
FAX: 618-8362-0955
Email: adl@avnet.com.au

Avnet Pacific
Unit C, 6-8 Lyon Park Rd.
North Ryde NSW 2113
Australia
TEL: 612-9878-1299
FAX: 612-9878-1299
Email: syd@avnet.com.au

Avnet Pacific
1st Floor, 664 Mountain Highway
Bayswater, Melbourne
Victoria 3153
Australia
TEL: 61-3-9738-1599
FAX: 61-3-9738-1799
Email: mel@avnet.com.au

Zatek Australia Pty. Ltd.
9-10 Bastow Place
P. O. Box 613
Melbourne
Australia
TEL: 613-95749644
FAX: 613-95749661

Zatek Australia Pty. Ltd.
Level 4,5
Belmore Street
Sydney
Australia
TEL: 61-2-97-44-5711
FAX: 61-2-97-44-5527

China

Excelpoint Systems Ltd.
Rm. A1108
Yinhai Commercial Bldg.
Shanghai 200233
PRC
TEL: 86-21-6482-2280
FAX: 86-21-6482-4680

Excelpoint Systems Ltd.
Rm. 610, Mingmao Bldg.
Shuncheng Road
Chengdu 610015
PRC
TEL: 86-28-662-8872
FAX: 86-28-662-8872

Excelpoint Systems Ltd.
79 JIA, Fuxing Road
Haidian District
Beijing 100854
PRC
TEL: 86-10-6837-3894
FAX: 86-10-6838-5621

Goldenchip Elect. Tech Co. Ltd.
7 Floor, 275 Wusi Road
Fuzhou 350003
PRC
TEL: 86-591-771-1118
FAX: 86-591-771-4160

Goldenchip Research
Unit 12B, 12 Floor,
Hua Kai Fu Gui Monetary World
Fuzhou 350001
PRC
TEL: 86-591-7602833
FAX: 86-591-7602833

Infinitron/SI Logic Ltd.
Block B, 1/fl.
153 FuRongJiang Road
Shanghai 200335
PRC
TEL: 86-21-62330879
FAX: 86-21-62330878

Weikeng Ind. Co. Ltd.
Rm. 14B, Jing Ming Mansion,
No. 8 Zun Yi South Road
Shanghai 200335
PRC
TEL: 86-21-6219-8745
FAX: 86-21-6219-8745

Weikeng Ind. Co. Ltd.
Rm. 1201, Unit C
Hui Yuan International Apartment
Beijing 100101
PRC
TEL: 86-10-6492-3726
FAX: 86-10-6499-1424

Wuhan Liyuan Research
15 Zhuo Dao Quan Road
P.O. Box 70020
Wuhan 430070
PRC
TEL: 86-27-7493505
FAX: 86-27-7493493

ASIA/PACIFIC *(Continued)*

Hong Kong

Excelpoint Systems Ltd.
Rm. 1506, 15/F Telford House
16 Wang Hoi Road
Kowloon Bay
Hong Kong
TEL: 852-2503-2212
FAX: 852-2503-1558

Gold Tender Limited
A2, 10/F, Blk A, Tonic Ind. Centre
26 Kai Cheung Road
Kln.
Hong Kong
TEL: 852-27586985
FAX: 852-23181290

Infinitron Asia Ltd.
Room 802, 8F Kinox Centre
9 Hung To Rd,
Kowloon
Hong Kong
TEL: 852-2341-6611
FAX: 852-2950-0987

Guangzhou Qiangli Electric Co. Ltd.
No. 498 12F/A, Huanshi East Road
Boli Commercial Centre
Guangzhou, China 510600
TEL: 86-20-8760-7508
FAX: 86-20-8760-4626

Texny Glorytact (HK) Ltd.
26/F, Metroplaza, Tower II
223 Hing Fong Road
Kwai Chung, Hong Kong
TEL: 852-2765 0118
FAX: 852-2765 0557

Weikeng Ind. Co. Ltd.
1509, Chevalier Comm Centre
Wang Hoi Road
Kowloon
Hong Kong
TEL: 852-27999035
FAX: 852-27966968

India

Excelpoint Systems India
3116, 6th C Main
Indiranagar, Hal 2nd Stage
Bangalore 560008
India
TEL: 91-80-5294846
FAX: 91-80-5294847

Future Electronics India
#401, 402, A-Wing
5th Floor, Mittal Towers
Bangalore 560 001
India
TEL: 91-80-559-3102
FAX: 91-80-559-2995

Future Electronics India
#A-22, Lower Ground Floor
Green Park Main
New Dehli 110 016
India
TEL: 91-11-652-2072
FAX: 91-11-652-2247

Primetech Communications
No. 289, 5th Cross, 1st Stage,
1st Phase
Gokul, Bangalore 560 054
India
TEL: 91-80-3378553
FAX: 91-80-3472580

Japan

Dianichi Contronics Inc.
Koraku Bldg., 1-1-8 Koraku
Bunkyo-Ku
Tokyo 112-0004
Japan
TEL: 81-3-3818-8081
FAX: 81-3-3818-8088

Global Electronics Corp.
Nichibei Time 24 Bldg.
35 Tansu-Cho, Shinjuku-Ku
Tokyo 162-0833
Japan
TEL: 81-3-3260-1411
FAX: 81-3-3260-7100

Marubeni Solutions Corp.
26-20, Higashi 1-chome
Shibuya-ku
Tokyo 150-0011
Japan
TEL: 81-3-5778-8661
FAX: 81-3-5778-8669

Ryoden Trading Co.
3-15-15, Higashi Ikebukuro
Toshima-Ku
Tokyo 170-0014
Japan
TEL: 81-3-5396-6211
FAX: 81-3-5396-6443

Unidux, Inc.
5-1-21, Kyonan-cho
Musashino-shi
Tokyo 180-0023
Japan
TEL: 81-422-31-4111
FAX: 81-422-31-2050

Korea

Prochips Inc.
#681-12 Gojan-Dong
Namdong-Gu
Inohou City 150 073
Korea
TEL: 82-32-821-7100
FAX: 82-32-822-0321

Nasco Co., Ltd.
#345-30 Kasan-Dong
Keumcheon-Gu
Seoul
Korea
TEL: 82-2-868-4988
FAX: 82-2-868-4984

Plato Technology Co.
61-3, Life Officetel #918
Yoido-Dong
Seoul 150-010
Korea
TEL: 82-2-785-4748
FAX: 82-2-784-5879

Hanil System
#402-2, Yangjae-Dong
Seocho-Gu
Seoul 130-130
Korea
TEL: 82-2-579-3194
FAX: 82-2-579-1208

M & K Sang SA
Room 516, Dong-A Bldg.
14-2, Yoido-Dong
Seoul 150-010
Korea
TEL: 82-2-785-1127
FAX: 82-2-785-1129

Daewon System
7-201 Daelim Apt 64-20
Bupyung 1-dong
Bupyung Incheon
Korea
TEL: 82-32-503-4530
FAX: 82-32-523-3527

ASIA/PACIFIC *(Continued)*

Malaysia

Excelpoint Systems LTD
Penang Office
Level 5 Hotel Equatorial
Bayan Lepas Penang 11900
Malaysia
TEL: 604-641-3218
FAX: 604-642-8218

Excelpoint Systems LTD
KL Office
8th Floor Wisma Stephens
Kuala Lumpur 55200
Malaysia
TEL: 603-244-8929
FAX: 603-244-8926

Gates Engineering Pte Ltd.
Penang Office
1-3-11, Persiaran Bukit Jambul 1
Penang 11900
Malaysia
TEL: 604-646-2887
FAX: 604-646-2889

Singapore

Excelpoint Systems Ltd.
24 Kaki Bukit Crescent
Kaki Bukit TechPark 1 416255
Singapore
TEL: 65-741-8966
FAX: 65-741-8980

Gates Engineering Pte. Ltd.
1123 Serangoon Road
#03-01 UMW Building 328207
Singapore
TEL: 65-299-9937
FAX: 65-299-7636

Taiwan

Bright Systems Co., Ltd.
6F-2, # 160
Ming Chuan E. Rd., Sec. 5
Taipei
Taiwan, R.O.C.
TEL: 886-2-2791-5766
FAX: 886-2-2794-9070

GoldenTechnology Corp.
4F, # 221, Chung Yang Road
Nan Kang Dist.
Taipei
Taiwan, R.O.C.
TEL: 886-2-2652-2255
FAX: 886-2-2651-0589

Infortech Co., Ltd.
6F-2, # 436, Fu Hsing N. Road
Taipei
Taiwan, R.O.C.
TEL: 886-2-2509-2734
FAX: 886-2-2509-2736

Solomon Technology Corp.
7F, #2, Lane 47, Sec. 3
Nan Kang Road
Taipei
Taiwan, R.O.C.
TEL: 886-2-2788-8989
FAX: 886-2-2788-8029

Weikeng Ind. Co. Ltd.
2F, # 34, Sec.1
Huan Shan Road, Nei Hu
Taipei
Taiwan, R.O.C.
TEL: 886-2-26590202
FAX: 886-2-26580959

Wing Footed Enterprise Co., Ltd.
9F-4, 238,
Chin-Hua North Road
Taichung
Taiwan, R.O.C.
TEL: 886-4-230-5023
FAX: 886-4-238-6124

Thailand

Electronics Source Co., Ltd.
5 Banmoh Rd.
Wangburapapirom Pranakorn
Bangkok 10200
Thailand
TEL: 662-884-9210
FAX: 662-884-9213

Gates Engineering Pte Ltd
184 Forum Tower 25th Floor
Rachadapisek Road
Huay Kwang Bangkok 10320
Thailand
TEL: 662-645-3679/80
FAX: 662-645-3681

CANADA

Alberta

Future Electronics
2015 32nd Avenue N.E., Unit 1
Calgary AB T2E 6Z3
Canada
TEL: 250-5550
FAX: 291-7054
Web: http://www.future.ca/

Future Electronics
6029-103rd Street N.E.
Edmonton AB T6H 2H3
Canada
TEL: 438-5888
FAX: 436-1874
Web: http://www.future.ca/

British Columbia

Arrow Semiconductor
8555 Commerce Ct
Burnaby BC V5A 4N4
Canada
TEL: 421-2333
FAX: 421-5030
Web: http://www.arrowsemi.com/

Bell Industries
4185 Still Creek Drive, Suite B201
Burnaby BC V5C 6G9
Canada
TEL: 291-0044
FAX: 291-9939
Web: http://www.bellind.com/

Future Electronics
3689 East 1st Avenue, Suite 200
Vancouver BC V5M 1C2
Canada
TEL: 294-1166
FAX: 294-1206
Web: http://www.future.ca/

Pioneer-Standard Electronics
10711 Combie Road, Suite 170
Richmond BC V6E 2V3
Canada
TEL: 273-5575
FAX: 565-5575
Web: http://www.pios.com/

Manitoba

Future Electronics
106 King Edward
Winnipeg MB R3H 0N8
Canada
TEL: 944-1446
FAX: 783-8133
Web: http://www.future.ca/

CANADA *(Continued)*

Ontario

Arrow Semiconductor
36 Antares Drive, Unit 100
Nepean ON K2E 7W5
Canada
TEL: 905 226-6903
FAX: 905 722-2018
Web: http://www.arrowsemi.com/

Arrow Semiconductor
1093 Meyerside Dr., Unit 2
Mississauga ON L5T 1M4
Canada
TEL: 905 670-7769
FAX: 905 670-7781
Web: http://www.arrowsemi.com/

Bell Industries
2738 Thamesgate Drive
Mississauga ON L4T 1G5
Canada
TEL: 905 678-0958
FAX: 905 678-1213
Web: http://www.bellind.com/

Future Electronics
1102 Prince of Whales Drive, Suite 210
Ottawa ON K2C 3W7
Canada
TEL: 613 727-1800
FAX: 613 727-9819
Web: http://www.future.ca/

Future Electronics
5935 Airport Road, Suite 200
Mississauga ON L4V 1W5
Canada
TEL: 905 612-9200
FAX: 905 612-9185
Web: http://www.future.ca/

Pioneer-Standard Electronics
3415 American Drive
Mississauga ON L4V 1T4
Canada
TEL: 905 405-8300
FAX: 905 405-6423
Web: http://www.pios.com/

Pioneer-Standard Electronics
148 York Street, Suite 209
London ON N6A 1A9
Canada
TEL: 519 672-4666
FAX: 519 672-3528
Web: http://www.pios.com/

Pioneer-Standard Electronics
223 Colonnade Road, Suite 112
Nepean ON K2E 7K3
Canada
TEL: 613 226-8840
FAX: 613 226-6352
Web: http://www.pios.com/

Quebec

Arrow Semiconductor
1255 Transcanada Highway, Suite 100
Dorval, Quebec H9P 2V4
Canada
TEL: 514 421-7411
FAX: 514 421-7430
Web: http://www.arrowsemi.com/

Bell Industries
6600 Trans Canada Highway, Suite 145
Pointe Claire, Quebec H9R 4S2
Canada
TEL: 514 426-5900
FAX: 514 426-5836
Web: http://www.bellind.com/

Future Electronics Corp.
237 Hymus Boulevard
Pointe Claire, Quebec H9R 5C7
Canada
TEL: 514 694-7710
FAX: 514 695-3707
Web: http://www.future.ca/

Future Electronics/Branch
1000, Ave. St. Jean Baptiste
Suite 201
Quebec City, G2E 5G5
Canada
TEL: 418 877-6666
FAX: 418 877-6671
Web: http://www.future.com

Pioneer-Standard Electronics
2954 Blvd. Laurier, Suite 100
Ste-Foy, Quebec G1V 4T2
Canada
TEL: 418 654-1077
FAX: 418 654-2958
Web: http://www.pios.com/

Pioneer-Standard Electronics
520 McCaffrey Street
Ville St. Laurent, Quebec H4T 1N1
Canada
TEL: 514 737-9700
FAX: 514 737-5212
Web: http://www.pios.com/

Future Electronics
1000, St. Charles
Vaudreuil, Quebec J7V 8PS
TEL: 514 457-3513
FAX: 514 457-4847

EUROPE

Austria

Avnet EMG GmbH
Waidhausenstrasse 19
A-1140 Wien
Austria
TEL: 43-1911-28-47
FAX: 43-1911-38-53

Metronik Austria
Diefenbachgasse 35
A-1150 Wien
Austria
TEL: 43-1-8915252
FAX: 43-1-8915250
Email: pracko@met.memec.com

Belgium

Acal Betea
Lozenberg 4
B-1932 Zaventem
Belgium
TEL: 32-2-720-59-83
FAX: 32-2-725-10-14
Web: http://www.acal.be

Future Benelux
Trinstraat 3
4823AA Breda
Netherlands
TEL: 31-765-444-888
FAX: 31-765-444-880

SEI Belg.
Office Belgium
Limburg Stirum 243, B-2
B-1780 Wemmel
Belgium
TEL: 2-4560747
FAX: 2-4600271

Bulgaria

Comet Electronics
Head Office
54, Scobelev Blvd., 1
1606 Sofia
Bulgaria
TEL: 359-2-9515866
FAX: 359-2-9540384
Email: comet@sof.omega.bg

Czech Republic

GM Electronics Czech
Karlinske nam. 6,
186 00 Prague 8
Czech Republic
TEL: 420-2-2322606
FAX: 420-2-2321194
Email: gm@gme.cz

EUROPE *(Continued)*

Denmark

Arrow Denmark
Smedeholm 13A
DK-2740 Herlev
Denmark
TEL: 45-44-50-82-00
FAX: 45-44-50-82-03

Finland

Arrow Finland
Tyopajakatu 5
Box 25
FIN-00581 Helsinki
Finland
TEL: 358-9-47-6660
FAX: 358-9-47666356

Memec Finland Oy
Kauppakaarre 1
FIN 00700 Helsinki
Finland
TEL: 358-9-3508-880
FAX: 358-9-3508-8828
Web: http://www.mef.memec.com

France

Future France
Parc Technopolis LP 854
Les Ulis
Courtaboeuf 91974
France
TEL: 33-1-69-82-11-11
FAX: 33-1-69-82-11-00
Web: http://www.future.ca/

Mecodis
Parc d'Activites
3 Allee des Erables
Cedex
France
TEL: 33-1-43-99-44-00
FAX: 33-1-43-99-98-28

MULTIcomposants
12 rue du Lyon
Silic 585
94663 Rungis Cedex
France
TEL: 33-1-49-78-49-00
FAX: 33-1-49-78-06-99

Rutronik Dimacel Composants
63, Rue Jean Jaures
BP 116
95874 Bezons Cedex I
France
TEL: 33-1-34-23-70-00
FAX: 31-1-30-76-31-97
Email: gjamet@dimacel,com

Germany

Avnet EMG GmbH
Stahlgruberring 12
D-81829 Muenchen
Germany
TEL: 49-89-4-5110-142
FAX: 49-89-4-5110-210

Future Electronics Deutschland GmbH
Muenchner Strasse 18
D-85774 Unterfoehring
Germany
TEL: 49-89-95727-0
FAX: 49-89-95727-140
Web: http://www.future.ca/

Metronik GmbH
Leonhardsweg 2
D-82008 Unterhaching
Germany
TEL: 49-89-61108-0
FAX: 49-89-61108-110

Rutronik RSC-Halbleiter GmbH
Industriestrasse 2
D-75228 Ispringen/Pforzheim
Germany
TEL: 49-7231-8010
FAX: 49-721-82282

Semitron W. Roeck GmbH
Im Gut 1
D-79790 Kuessaberg
Germany
TEL: 49-7742-8001-0
FAX: 49-7742-6901

Greece

P. Caritato & Associates SA
Ilia Iliou 31
Athens 11743
Greece
TEL: 30-1-9020115
FAX: 30-1-9017024
Email: pca@caritato.ath.forthnet.gr

Hungary

Chipcad Electronics Distribution, Ltd.
Dolmany u. 12
Hungary
H-1131 Budapest
TEL: 361-270-7680
FAX: 361-270-7699
Email: info@chipcad.hu
Web: http://www.chipcad.hu

Future Electronics Ltd.
Burok Utca 34
H-1124 Budapest
Hungary
TEL: 36-122-40-510
FAX: 36-122-40-511

Ireland

Top Tech Solutions Ltd.
124 Orby Drive
Belfast BT5 6BB
Ireland
TEL: 44-1232-704985
FAX: 44-1232-792563

Israel

Elina Electronics Ltd.
14 Raoul Wallenberg St.
P.O. Box 13190
Tel Aviv 61131
Israel
TEL: 972-3-649-85-43
FAX: 972-3-649-87-45
Email: elina_e@netvision.net.il

Italy

Claitron Spa
Viale Fulvio Testi, 280
20126 Milano
Italy
TEL: 39-2-661491
FAX: 39-2-66105666

Future Electronics SRL
Vis Fosse Ardeatine, 4
20092 Cinisello Balsamo
Milano
Italy
TEL: 39-2-66-0961
FAX: 39-2-660-8126
Web: http://www.future.ca/

Intesi SPA
Viale Fulvio Testi, 280
20126 Milano
Italy
TEL: 39-2-661791
FAX: 39-2-6435825

Kevin SRL
Via Venezia Giulia, 10
20157 Milano
Italy
TEL: 39-2-33200914
FAX: 39-2-33200917

EUROPE *(Continued)*

Latvia

Ormix Ltd.
Kr. Barona 136
LV-1012
Riga
Latvia
TEL: 371-2292839
FAX: 371-2292823

Netherlands

Acal Auriema
Beatrix de Rijkweg 8
NL-5657 EG Eindhoven
Netherlands
TEL: 31-40-2-502-602
FAX: 31-40-2-510-255
Web: http://www.acal.be

Future Benelux
Trinstraat 3
4823AA Breda
Netherlands
TEL: 31-765-444-888
FAX: 31-765-444-880

SEI Benelux
SEI Building
Takkebijsters 2, NL-4817 BI Breda
P.O. Box 6824
NL-4802 HV Breda
Netherlands
TEL: 31-76-572-2333
FAX: 31-76-572-2395
Email: Sales@Sonetech.N

Norway

Berendsen Components AS
P.O. Box 9376 Gronlund
N-0135
Oslo
Norway
TEL: 47-22-088500
FAX: 47-22-088590

Poland

Future Electronics Poland
Ul. Panienska 9
03-704 Warsaw
Poland
TEL: 48-226-189-202
FAX: 48-226-188-050

Gamma Poland
ul. Sady Zoliborskie 13A
PL-01-772 Warsaw
Poland
TEL: 48-22-6638376
FAX: 48-22-6639887

Portugal

Digicontrole
Dpt Comercial
Av. Eng. Arantes e Oliveira 5-2 D
1900 LISBOA
Portugal
TEL: 351-1-840-57-30
FAX: 351-1-849-03-73
Email: digicontrole@mail.pt

Russia

Gamma SPb
P.O. Box 38
St. Petersburg 197348
Russia
TEL: 7-812-325-5115
FAX: 7-812-325-5114

Slovakia

GM Electronics
Budovatelska 27
821-08 Bratislava
Slovakia
TEL: 421-7-52-60-439
FAX: 421-7-52-60-120

Spain

Sagitron
Corazon de Maria 80/82
28002 Madrid
Spain
TEL: 34-1-416-92-61
FAX: 34-1-413-5848

Sweden

Memec Scandinavia AB
Sehlstedsgatan 6
115 28 Stockholm
Sweden
TEL: 46-8-459-79-00
FAX: 46-8-459-79-99

Switzerland

Avnet EMG GMBH
Boehnirainstr.
Postfach 1575
CH-8801 Thalwil
Switzerland
TEL: 41-1722-13-30
FAX: 41-1722-13-40

Rutronik AG
Brandschenkestr. 178
CH-8027 Zurich
Switzerland
TEL: 41-1-209-6030
FAX: 41-1-209-6035

Semitron W. Roeck & Co.
Promenadenstr.6
CH-5330 Zurzach
Switzerland
TEL: 41-56-269-60-40
FAX: 41-56-249-3569

Turkey

Inter Muehendislik
Ve Ticaret A.S. 1
Hasircibasi Caddesi No. 55
Istanbul
Turkey
TEL: 90-216-349-9400
FAX: 90-216--349-9431
Email: halimoz@ibm.net

United Kingdom

Arrow-Jermyn
St. Martins Business Centre
Cambridge Road
Bedford MK42 0LF
England
TEL: 44-1234-270027
FAX: 44-1234-791549

Electronic Services Distribution Ltd.
Edinburgh Way
Harlow
Essex CM20 2DF
England
TEL: 44-1279-441144
FAX: 44-1279-443417

Eurodis HB Electronics Ltd
Lever Street
Bolton
Lancashire BL3 6BJ
England
TEL: 44-1204-555000
FAX: 44-1204-384911

FEC
Sales, Marketing & Admin Center
Canal Road
West Yorkshire LS12 2TU
England
TEL: 44-1132-790101
FAX: 44-1132-633404

Future Electronics Ltd.
Future House
Poyle Road, Colnbrook
Berks SL3 0EZ
England
TEL: 44-1753-763000
FAX: 44-1753-689100
Web: http://www.future.ca/

Solid State Supplies Plc.
Unit 2
Eastlands Lane
Kent TN12 6BU
England
TEL: 44-1892-836836
FAX: 44-1892-837837

MEXICO

Guadalajara

Electronica Seta, S.A. de C.V.
Santa Mario No. 100
Col. Capalita
Zapopan, Jalisco CP45000
Mexico
TEL: 523-121-0338
FAX: 523-121-0338

Future Electronics de Mexico,
S.A. de C.V.
Chimalhuacan 3569
6o Piso, Suite 2, Ciudad Del Sol
Zapopan, Jalisco CP45050
Mexico
TEL: 523-122-0043
FAX: 523-122-1066
Web: http://www.future.ca/

La Loma

Electronica Seta, S.A. de C.V.
Galena 114, 2o. Piso
La Loma Tlalnepantla CP 54060
Mexico
TEL: 525-390-7713
FAX: 525-390-9468

SOUTH AMERICA

All Others Countries Except Brazil

Ibars Electronics Corp
10020 N.W. 6th CT
Pembroke Pines FL 33024
USA
TEL: 954 430-3740
FAX: 954 430-3763

Brazil

Future Electronics Brazil
R. Luzitana, 740 - cj103/104
Centro-Campinas
13015 - 121 - SP
Brazil
TEL: 55-19-235-1511
FAX: 55-19-236-9834
Email: futurebr@nutecnet.com.br
Web: http://www.future.ca/

Hitech El. Indl. Coml. Ltda.
Rua Branco de Moreas, 489
04718-010-Chac. Sto. Antonio
Sao Paulo SP
Brazil
TEL: 55-11-5188-4130
FAX: 55-11-5188-4191

UNITED STATES

Alabama

Arrow Semiconductor
4930-G Corporate Drive
Huntsville AL 35805
USA
TEL: 205 864-3300
FAX: 205 864-3349

Bell Industries
8215 Highway 20 W, Suite 140
Madison AL 35758
USA
TEL: 205 464-8646
FAX: 205 464-8655
Web: http://www.bellind.com/

Future Electronics
6767 Old Madison Place
Huntsville AL 35806
USA
TEL: 205 971-2010
FAX: 205 922-0004
Web: http://www.future.ca/

Pioneer-Standard Electronics
4835 University Square, Suite 5
Huntsville AL 35816
USA
TEL: 205 837-9300
FAX: 205 837-9358
Web: http://www.pios.com/

Arizona

Arrow Semiconductor
1406 West 14th Street, Suite 101
Tempe AZ 85281-6909
USA
TEL: 602 966-6600
FAX: 602 966-4826
Web: http://www.arrowsemi.com/

Bell Industries
7025 E. Greenway Parkway, Suite 500
Scottsdale AZ 85254
USA
TEL: 602 905-2355
FAX: 602 905-2356
Web: http://www.bellind.com/

Future Electronics
4636 E. University Drive, Suite 245
Tempe AZ 85034
USA
TEL: 602 968-7140
FAX: 602 965-0334
Web: http://www.future.ca/

Pioneer-Standard Electronics
4908 East McDowell Rd., Suite 103
Phoenix AZ 85008
USA
TEL: 602 231-6400
FAX: 602 231-8877
Web: http://www.pios.com/

UNITED STATES *(Continued)*

California

Northern California

Rocklin
Arrow Semiconductor
580 Menlo Drive, Suite 8
Rocklin CA 95765-3706
USA
TEL: 916 624-9744
FAX: 916 624-9750
Web: http://www.arrowsemi.com/

Roseville
Bell Industries
3001 Douglas Blvd., Suite 205
Roseville CA 95661
USA
TEL: 916 781-8070
FAX: 916 781-2954
Web: http://www.bellind.com/

Future Electronics
755 Sunrise Avenue, Suite 150
Roseville CA 95661
USA
TEL: 916 783-7877
FAX: 916 783-7988
Web: http://www.future.ca/

San Jose
Arrow Electronics
1350 McCandless Drive
Milpitas CA 95035
USA
TEL: 408 935-4619
FAX: 408 935-4688

Arrow Semiconductor
Malibu Canyon Business Park
26677 West Agoura Road
Calabasas CA 91302-1959
USA
TEL: 818 880-9686
FAX: 818 880-4687
Web: http://www.arrowsemi.com/

Arrow Semiconductor
1680 McCandless Drive
Building 3
Milpitas CA 95035-8000
USA
TEL: 408 453-1200
FAX: 408 441-4504
Web: http://www.arrowsemi.com/

Bell Industries
1161 N. Fairoaks Avenue
Sunnyvale CA 94089
USA
TEL: 408 734-8570
FAX: 408 734-8875
Web: http://www.bellind.com/

Future Electronics
2220 O'Toole Avenue
San Jose CA 95131
USA
TEL: 408 434-1122
FAX: 408 433-0822
Web: http://www.future.ca/

Pioneer-Standard Electronics
333 River Oaks Parkway
San Jose CA 95134
USA
TEL: 408 954-9100
FAX: 408 954-9113
Web: http://www.pios.com/

Southern California

Irvine
Arrow Semiconductor
6 Cronwell Street, Suite 100
Irvine CA 92618-1816
USA
TEL: 714 768-4444
FAX: 714 768-6456
Web: http://www.arrowsemi.com

Bell Industries
220 Technology Drive, #100
Irvine CA 92718
USA
TEL: 714 727-4500
FAX: 714 453-4610
Web: http://www.bellind.com/

Future Electronics
25B Technology Way, Suite 200
Irvine CA 92618
USA
TEL: 714 453-1515
FAX: 714 453-1226
Web: http://www.future.ca/

Pioneer-Standard Electronics
217 Technology Drive, #110
Irvine CA 92618
USA
TEL: 714 753-5090
FAX: 714 753-5074
Web: http://www.pios.com/

Los Angeles Area
Bell Industries
125 Auburn Court, Suite 110
Westlake Village CA 91362
USA
TEL: 805 373-5600
FAX: 805 496-7340
Web: http://www.bellind.com/

Bell Industries (Corporate Headquarters)
2201 East El Segundo Blvd, Suite 300
El Segundo CA 90245
USA
TEL: 805 563-2355
FAX: 805 563-2508
Web: http://www.bellind.com/

Los Angeles Area (continued)
Future Electronics
27489 West Agoura Road, Suite 300
Agoura Hills CA 91301
USA
TEL: 818 865-0040
FAX: 818 865-1340
Web: http://www.future.ca/

Pioneer-Standard Electronics
5126 Clareton Drive, Suite 100
Agoura Hills CA 91301
USA
TEL: 818 865-5800
FAX: 818 865-5814
Web: http://www.pios.com/

San Diego
Aegis Electronic Group, Inc
1015 Chestnut Avenue, Suite G2
Carlsbad CA 92008
USA
TEL: 619 729-2026
FAX: 619 729-9295

Arrow Semiconductor
9511 Ridghaven Ct
San Diego CA 92123-1688
USA
TEL: 619 565-4800
FAX: 619 279-0862
Web: http://www.arrowsemi.com/

Bell Industries
6835 Flanders Drive, Suite 300
San Diego CA 92121
USA
TEL: 619 457-7545
FAX: 619 457-9750
Web: http://www.bellind.com/

Future Electronics
6256 Greenwich Drive, Suite 200
San Diego CA 92122
USA
TEL: 619 625-2800 (800-649-5020)
FAX: 619 625-2810
Web: http://www.future.ca/

Pioneer-Standard Electronics
9449 Balboa Avenue, Suite 114
San Diego CA 92123
USA
TEL: 619 514-7700
FAX: 619 514-7799
Web: http://www.pios.com/

UNITED STATES *(Continued)*

Colorado

Arrow Semiconductor
373 Inverness Drive South
Englewood CO 80112-5816
USA
TEL: 303 799-0258
FAX: 303 799-0730
Web: http://www.arrowsemi.com/

Bell Industries
9351 Grant Street, Suite 460
Thornton CO 80229
USA
TEL: 303 280-1115
FAX: 303 280-0005
Web: http://www.bellind.com/

Future Electronics
12600 W. Colfax Avenue, Suite B110
Lakewood CO 80215
USA
TEL: 303 232-2008
FAX: 303 232-2009
Web: http://www.future.ca/

Pioneer-Standard Electronics
5600 Greenwood Plaza Blvd., Suite 201
Englewood CO 80111
USA
TEL: 303 773-8090
FAX: 303 773-8194
Web: http://www.pios.com/

Connecticut

Arrow Semiconductor
860 North Main Street Ext
Wallingford CT 06492-2419
USA
TEL: 203 265-7741
FAX: 203 265-7988
Web: http://www.arrowsemi.com/

Bell Industries
326 West Main Street
Milford CT 06460-0418
USA
TEL: 203 878-5538
FAX: 203 878-6970
Web: http://www.bellind.com/

Future Electronics
700 W. Johnson Avenue
Westgate Office Center
Chesire CT 06410
USA
TEL: 203 250-0083
FAX: 203 250-0081
Web: http://www.future.ca/

Pioneer-Standard Electronics
Two Trap Falls, #101
Shelton CT 06484
USA
TEL: 203 929-5600
FAX: 203 929-9791
Web: http://www.pios.com/

Florida

Altamonte Springs
Bell Industries
650 South Northlake Blvd., #400
Altamonte Springs FL 32701
USA
TEL: 407 339-0078
FAX: 407 339-0139
Web: http://www.bellind.com/

Future Electronics
237 S. Westmonte Drive, Suite 307
Altamonte Springs FL 32714
USA
TEL: 407 865-7900
FAX: 407 865-7660
Web: http://www.future.ca/

Pioneer-Standard Electronics
337 South-North Lake, Suite 1000
Altamonte Springs FL 32701
USA
TEL: 407 834-9090
FAX: 407 834-0865
Web: http://www.pios.com/

Deerfield Beach
Arrow Semiconductor
400 Fairway Drive, Suite 101-104A
Deerfield Beach FL 33441-1884
USA
TEL: 954 429-8200
FAX: 954 428-3991
Web: http://www.arrowsemi.com/

Future Electronics
1400 E. Newport Center Drive, Suite 200
Deerfield Beach FL 33442
USA
TEL: 954 426-4043
FAX: 954 426-3939
Web: http://www.future.ca/

Pioneer-Standard Electronics
674 S. Military Trail
Deerfield Beach FL 33442
USA
TEL: 954 428-8877
FAX: 954 481-2950
Web: http://www.pios.com/

Largo
Future Electronics
2200 Tall Pines Drive, Suite 108
Largo FL 33771
USA
TEL: 813 530-1222
FAX: 813 538-9598
Web: http://www.future.ca/

Lake Mary
Arrow Semiconductor
37 Skyline Drive, Suite 3101
Lake Mary FL 32746
USA
TEL: 407333-9300
FAX: 333-9320
Web: http://www.arrowsemi.com/

Georgia

Arrow Semiconductor
4250 East River Green Parkway, Suite E
Duluth GA 30096
USA
TEL: 770 497-1300
FAX: 770 476-1493
Web: http://www.arrowsemi.com/

Bell Industries
3000 Northwoods Parkway, Suite 115
Norcross GA 30071
USA
TEL: 770 446-9777
FAX: 770 446-1186
Web: http://www.bellind.com/

Future Electronics
3150 Holcomb Bridge Road, Suite 130
Norcross GA 30071
USA
TEL: 770 441-7676
FAX: 770 441-7580
Web: http://www.future.ca/

Pioneer-Standard Electronics
4250 C Rivergreen Pkwy.
Duluth GA 30136
USA
TEL: 770 623-1003
FAX: 770 623-0665
Web: http://www.pios.com/

Illinois

Arrow Semiconductor
1166 Springlake Drive
Itasca IL 60143-2062
USA
TEL: 847 250-0500
FAX: 847 250-0916
Web: http://www.arrowsemi.com/

Bell Industries
175 West Central Road
Schaumburg IL 60195
USA
TEL: 630 202-6400
FAX: 630 202-5849
Web: http://www.bellind.com/

Future Electronics
3100 W. Higgins Road, Suite 100
Hoffman Estates IL 60195
USA
TEL: 847 882-1255
FAX: 847 490-9290
Web: http://www.future.ca/

UNITED STATES *(Continued)*

Indiana

Fort Wayne
Pioneer-Standard Electronics
237 Airport N. Office Park
Fort Wayne IN 46825
USA
TEL: 219 489-0283
FAX: 219 489-6262
Web: http://www.pios.com/

Indianapolis
Arrow Semiconductor
7108 Lakeview Parkway West Drive
Indianapolis IN 46268-4104
USA
TEL: 317 299-2071
FAX: 317 299-2379
Web: http://www.arrowsemi.com/

Bell Industries
6982 Hilldale Court
Indianapolis IN 46250-2040
USA
TEL: 317 842-4244
FAX: 317 570-1344
Web: http://www.bellind.com/

Future Electronics
8425 Woodfield Crossing
Suite 175
Indianapolis IN 46240
USA
TEL: 317 469-0477
FAX: 317 469-0448
Web: http://www.future.ca/

Pioneer-Standard Electronics
9350 N. Priority Way W. Dr.
Indianapolis IN 46240
USA
TEL: 317 573-0880
FAX: 317 573-0979
Web: http://www.pios.com/

Kansas

Arrow Semiconductor
9801 Legler Road
Lenexa KS 66219-1286
USA
TEL: 913 541-9542
FAX: 913 752-2612
Web: http://www.arrowsemi.com/

Bell Industries
6400 Glenwood
Overland Park KS 66202-4021
USA
TEL: 913 236-8800
FAX: 913 384-6825
Web: http://www.bellind.com/

Future Electronics
10977 Granada Lane, Suite 210
Overland Park KS 66211
USA
TEL: 913 498-1531
FAX: 913 498-1786
Web: http://www.future.ca/

Maryland

Arrow Semiconductor
9800J Patuxent Woods Drive
Columbia MD 21046-1561
USA
TEL: 913 309-0686
FAX: 913 309-0699
Web: http://www.arrowsemi.com/

Bell Industries
6460 Dobbin Road
Columbia MD 21045-5813
USA
TEL: 913 730-6119
FAX: 913 730-8940
Web: http://www.bellind.com/

Future Electronics
6716 Alexander Bell Drive
Suite 101
Columbia MD 21046
USA
TEL: 913 290-0600
FAX: 913 290-0328
Web: http://www.future.ca/

Pioneer-Standard Electronics
9100 Gaither Rd.
Gaithersburg MD 20877
USA
TEL: 913 921-0660
FAX: 913 670-0304
Web: http://www.pios.com/

Massachusetts

Arrow Semiconductor
25 Upton Drive
Wilmington MA 01887-1073
USA
TEL: 508 658-0900
FAX: 508 694-1754
Web: http://www.arrowsemi.com/

Bell Industries
187 Ballardvale Street
Wilmington MA 01887-1046
USA
TEL: 508 657-5900
FAX: 508 658-7989
Web: http://www.bellind.com/

Bell Industries
100 Burrt Road, #G-01
Andover MA 01810
USA
TEL: 508 623-3200
FAX: 508 474-8902
Web: http://www.bellind.com/

Future Electronics
41 Main Street
Bolton MA 01740
USA
TEL: 978 779-3000
FAX: 978 779-3050
Web: http://www.future.ca/

Pioneer-Standard Electronics
44 Hartwell Avenue
Lexington MA 02173
USA
TEL: 508 861-9200
FAX: 508 863-1547
Web: http://www.pios.com/

Michigan

Grand Rapids
Future Electronics
4505 Broadmoor S.E.
Grand Rapids MI 49512
USA
TEL: 616 698-6800
FAX: 616 698-6821
Web: http://www.future.ca/

Pioneer-Standard Electronics
4467 Byron Ctr. Rd. SW
Grand Rapids MI 49509
USA
TEL: 616 534-3145
FAX: 616 534-3922
Web: http://www.pios.com/

Detroit
Arrow Semiconductor
44720 Helm Street
Plymouth MI 48170-6019
USA
TEL: 313 455-0850
FAX: 313 734-6656
Web: http://www.arrowsemi.com/

Future Electronics
35200 Schoolcraft Road, Suite 106
Livonia MI 48150
USA
TEL: 313 261-5270
FAX: 313 261-8175
Web: http://www.future.ca/

Pioneer-Standard Electronics
44190 Plymouth Oaks Drive
Plymouth MI 48170
USA
TEL: 313 416-2157
FAX: 313 416-2415
Web: http://www.pios.com/

UNITED STATES *(Continued)*

Minnesota

Bloomington
Bell Industries
9401 James Avenue South, #142
Bloomington MN 55431
USA
TEL: 612 888-7747
FAX: 612 888-7757
Web: http://www.bellind.com/

Eden Prarie
Arrow Semiconductor
7690 Golden Triangle Drive
Eden Prarie MN 55344-3732
USA
TEL: 612 944-5454
FAX: 612 944-3045
Web: http://www.arrowsemi.com/

Future Electronics
10025 Valley View Road, Suite 196
Eden Prairie MN 55344
USA
TEL: 612 944-2200
FAX: 612 944-2520
Web: http://www.future.ca/

Pioneer-Standard Electronics
7625 Golden Triangle
Eden Prairie MN 55344
USA
TEL: 612 944-3355
FAX: 612 944-3794
Web: http://www.pios.com/

Thief River Falls
Digi-Key Corporation
P.O. Box 677
701 Brooks Avenue South
Thief River Falls MN 56701
USA
TEL: 218 681-6674
FAX: 218 681-3380

Missouri

Future Electronics
12125 Woodcrest Executive Drive
Suite 220
St. Louis MO 63141
TEL: 314 469-6805
FAX: 314 469-7226

Pioneer-Standard Electronics
4227 Earth City Express Way
Earth City MO 63045
TEL: 800 344-5218
FAX: 314 209-3054

New Jersey

Northern
Arrow Semiconductor
26 Chapin Road, Unit 1112
Pine Brook NJ 07058-4416
USA
TEL: 201 227-7960
FAX: 201 227-9246
Web: http://www.arrowsemi.com/

Bell Industries
271 Route 46 West, Bldg. F202
Fairfield NJ 07004
USA
TEL: 201 227-6060
FAX: 201 227-2626
Web: http://www.bellind.com/

Future Electronics
1259 Route 46 East
Parsippany NJ 07054
USA
TEL: 201 299-0400
FAX: 201 299-1377
Web: http://www.future.ca/

Phase 1 Technology Corp.
295 Molnar Drive
Elmwood Park NJ 07407
USA
TEL: 201 791-2990
FAX: 201 791-2552

Pioneer-Standard Electronics
14A Madison Road
Fairfield NJ 07006
USA
TEL: 201 575-3510
FAX: 201 575-3454
Web: http://www.pios.com/

Southern
Arrow Semiconductor
4 East Stow Road, Unit 11
Marlton NJ 08053-3152
USA
TEL: 609 596-8000
FAX: 609 596-9632
Web: http://www.arrowsemi.com/

Bell Industries
158 Gaither Drive, Suite 110
Mt. Laurel NJ 08054
USA
TEL: 609 439-8860
FAX: 609 439-9009
Web: http://www.bellind.com/

Future Electronics
12 East Stow Road, Suite 200
Marlton NJ 08053
USA
TEL: 609 596-4080
FAX: 609 596-4266
Web: http://www.future.ca/

Phase 1 Technology Corp.
560 Fellowship Road, Suite 205
Mt. Laurel NJ 08054
USA
TEL: 609 234-3232
FAX: 609 234-5012

New York

Binghamton
Pioneer-Standard Electronics
1249 Front Street, Suite 201
Binghamton NY 13901
USA
TEL: 607 722-9300
FAX: 607 722-9562
Web: http://www.pios.com/

Long Island
Arrow Semiconductor
47 Mall Drive
Commack NY 11725-5717
USA
TEL: 516 864-6600
FAX: 516 493-2244
Web: http://www.arrowsemi.com/

Future Electronics
801 Motor Parkway
Hauppauge NY 11788
USA
TEL: 516 234-4000
FAX: 516 234-6183
Web: http://www.future.ca/

Phase 1 Technology Corp.
46 Jefryne Blvd.
Deer Park NY 11729
USA
TEL: 516 254-2600
FAX: 516 254-2693

Upstate New York
Arrow Semiconductor
3375 Brighton-Henrietta Townline Rd.
Rochester NY 14623-2898
USA
TEL: 716 427-0300
FAX: 716 427-0735
Web: http://www.arrowsemi.com/

Bell Industries
1170 Pittsford Victor Road
Pittsford NY 14534-3807
USA
TEL: 716 381-9700
FAX: 716 381-9495
Web: http://www.bellind.com/

Bell Industries
77 Schmitt Blvd.
Farmingdale NY 11735-1410
USA
TEL: 716 420-9800
FAX: 716 752-9870
Web: http://www.bellind.com/

UNITED STATES *(Continued)*

Upstate New York (continued)

Future Electronics
200 Salina Meadows Parkway
Suite 130
Syracuse NY 13212
USA
TEL: 315 451-2371
FAX: 315 451-7258
Web: http://www.future.ca/

Future Electronics
300 Linden Oaks
Rochester NY 14625
USA
TEL: 310 387-9550
FAX: 315 387-9563
Web: http://www.future.ca/

Pioneer-Standard Electronics
Meridian Plaza III
3125 Veterans Memorial Highway
Ronkonkoma NY 11779
USA
TEL: 716 738-1700
FAX: 716 738-1790
Web: http://www.pios.com/

Pioneer-Standard Electronics
1250 Pittsford/Victor Road
Building 200
Pittsford NY 14534
USA
TEL: 716 389-8200
FAX: 716 389-8240
Web: http://www.pios.com/

North Carolina

Arrow Semiconductor
5240 Greens Dairy Road
Raleigh NC 27616-4600
USA
TEL: 919 876-3132
FAX: 919 878-9517
Web: http://www.arrowsemi.com/

Bell Industries
3100 Smoketree Court
Raleigh NC 27604
USA
TEL: 919 874-0011
FAX: 919 874-0013
Web: http://www.bellind.com/

Future Electronics
8401 University Executive Park
Suite 108
Charlotte NC 28262
USA
TEL: 919 547-1107
FAX: 919 547-9650
Web: http://www.future.ca/

Future Electronics
5225 Capital Blvd.
1 North Commerce Center
Raleigh NC 27604
USA
TEL: 919 790-7111
FAX: 919 790-8782
Web: http://www.future.ca/

Pioneer-Standard Electronics, Inc.
5510 Six Forks Road
Raleigh NC 27609
USA
TEL: 919 845-5100
FAX: 919 845-5055
Web: http://www.pios.com

Ohio

Cleveland

Arrow Semiconductor
6573 East Cochran Road
Solon OH 44139-3916
USA
TEL: 216 248-3990
FAX: 216 248-1106
Web: http://www.arrowsemi.com/

Bell Industries
6155 Rockside Road
Cleveland OH 44131-2289
USA
TEL: 216 447-1520
FAX: 216 447-1761
Web: http://www.bellind.com/

Future Electronics
6009-E Landerhaven Drive
Mayfield Heights OH 44124
USA
TEL: 216 449-6996
FAX: 216 449-8987
Web: http://www.future.ca/

Pioneer-Standard Electronics
29125 Solon Road
Solon OH 44139
USA
TEL: 216 248-8710
FAX: 216 248-9166
Web: http://www.pios.com/

Pioneer-Standard Electronics
4800 East 131st Street
Cleveland OH 44105
USA
TEL: 216 498-6305
FAX: 216 587-3906
Web: http://www.pios.com/

Dayton

Arrow Semiconductor
8200 Washington Village Drive, Suite A
Centerville OH 45458-1877
USA
TEL: 513 435-5563
FAX: 513 435-2049
Web: http://www.arrowsemi.com/

Bell Industries
446 Windsor Park Drive
Dayton OH 45459
USA
TEL: 513 434-8231
FAX: 513 434-8103
Web: http://www.bellind.com/

Future Electronics
1430 Oak Court, Suite 203
Beavercreek OH 45430
USA
TEL: 513 426-0090
FAX: 513 426-8490
Web: http://www.future.ca/

Pioneer-Standard Electronics
8741 Gander Creek Drive
Miamisburg OH 45342
USA
TEL: 513 428-6900
FAX: 513 428-6995
Web: http://www.pios.com/

Worthington

Pioneer-Standard Electronics
100 Old Wilson Bridge, Suite 105
Worthington OH 43085
USA
TEL: 614 848-4854
FAX: 614 848-4889
Web: http://www.pios.com/

Oklahoma

Arrow Semiconductor
12111 East 51 St, Suite 101
Tulsa OK 74146-6005
USA
TEL: 918 252-7537
FAX: 918 254-0917
Web: http://www.arrowsemi.com/

Pioneer-Standard Electronics
9717 E. 42nd Street, Suite 105
Tulsa OK 74146
USA
TEL: 918 665-7480
FAX: 918 665-1891
Web: http://www.pios.com/

UNITED STATES *(Continued)*

Oregon

Arrow Semiconductor
9500 SW Nimbus Avenue, Building E
Beaverton OR 97008-7163
USA
TEL: 503 629-8090
FAX: 503 645-0611
Web: http://www.arrowsemi.com/

Bell Industries
8705 S.W. Nimbus, Suite 100
Beaverton OR 97008
USA
TEL: 503 644-3444
FAX: 503 520-1948
Web: http://www.bellind.com/

Future Electronics
7204 SW Durham Road, Suite 900
Portland OR 97224
USA
TEL: 503-603-0956
FAX: 503-645-1559
Web: http://www.future.ca/

Pioneer-Standard Electronics
5665 S.W. Meadows Rd.
Lake Oswego OR 97035
USA
TEL: 503 968-6565
FAX: 503 598-2555
Web: http://www.pios.com/

Pennsylvania

Philadelphia Area
Pioneer-Standard Electronics
500 Enterprise Road
Keith Valley Business Center
Horsham PA 19044
USA
TEL: 215 674-4000
FAX: 215 674-3107
Web: http://www.pios.com/

Pittsburgh
Arrow Semiconductor
3245 Old Frankstwon Road
Pittsburgh PA 15239-2909
USA
TEL: 412 327-1130
FAX: 412 327-4181
Web: http://www.arrowsemi.com/

Future Electronics
103 Bradford Road, Suite 100
Wexford PA 15090
USA
TEL: 412 935-1113
FAX: 412 935-1188
Web: http://www.future.ca/

Pioneer-Standard Electronics
259 Kappa Drive
Pittsburgh PA 15238
USA
TEL: 412 782-2300
FAX: 412 963-8255
Web: http://www.pios.com

Texas

Austin
Arrow Semiconductor
Braker Center III, Building M1
Austin TX 78758-4079
USA
TEL: 512 835-4180
FAX: 512 832-9875
Web: http://www.arrowsemi.com/

Bell Industries
11824 Jollyville Road, Suite 103
Austin TX 78759
USA
TEL: 512 331-9961
FAX: 512 331-1070
Web: http://www.bellind.com/

Future Electronics
6850 Austin Center Blvd., Suite 320
Austin TX 78731
USA
TEL: 512 502-0991
FAX: 512 502-0740
Web: http://www.future.ca/

Pioneer-Standard Electronics
1826-D Kramer Lane, Suite D
Austin TX 78758
USA
TEL: 512 835-4000
FAX: 512 835-9829
Web: http://www.pios.com/

Dallas
Arrow Semiconductor
3220 Commander Drive
Carrollton TX 75006-2585
USA
TEL: 972 380-6464
FAX: 972 248-7208
Web: http://www.arrowsemi.com/

Bell Industries
14110 Dallas Parkway
Dallas TX 75081
USA
TEL: 972 458-0047
FAX: 972 404-0267
Web: http://www.bellind.com/

Future Electronics
800 E. Campbell Road, Suite 130
Richardson TX 75081
USA
TEL: 972 437-2437
FAX: 972 669-2347
Web: http://www.future.ca/

Pioneer-Standard Electronics
13765 Beta Road
Dallas TX 75244
USA
TEL: 972 386-7300
FAX: 972 490-6419
Web: http://www.pios.com/

Houston
Arrow Semiconductor
Westgate Center, Building B
19416 Park Rowe
Houston TX 77084-4860
USA
TEL: 713 647-6868
FAX: 713 492-8722
Web: http://www.arrowsemi.com/

Bell Industries
12000 Richmond Avenue, Suite 310
Houston TX 77082
USA
TEL: 713 870-8101
FAX: 713 870-8122
Web: http://www.bellind.com/

Future Electronics
10333 Richmond Avenue, Suite 970
Houston TX 77042
USA
TEL: 713 785-1155
FAX: 713 785-4558
Web: http://www.future.ca/

Pioneer-Standard Electronics
10530 Rockley Road, Suite 100
Houston TX 77099
USA
TEL: 713 495-4700
FAX: 713 495-5642
Web: http://www.pios.com/

Utah

Arrow Semiconductor
2440 South 1070 West, Suite A
Salt Lake City UT 84119-1554
USA
TEL: 801 973-8555
FAX: 801 973-8909
Web: http://www.arrowsemi.com/

Bell Industries
310 East 4500 S, Suite 110
Murray UT 84107
USA
TEL: 801 261-2999
FAX: 801 261-0880
Web: http://www.bellind.com/

Future Electronics
3540 S. Highland Drive, #301
Salt Lake City UT 84106
USA
TEL: 801 467-4448
FAX: 801 467-3604
Web: http://www.future.ca/

UNITED STATES *(Continued)*

Washington

Arrow Semiconductor
3310 146th Place SE
Bldg B, Suite A
Bellevue WA 98007
USA
TEL: 206 643-9992
FAX: 206 643-9709
Web: http://www.arrowsemi.com/

Bell Industries
19119 Borth Creek Pkwy, Suite 102
Bothell WA 98011
USA
TEL: 206 486-2124
FAX: 206 487-1927
Web: http://www.bellind.com/

Future Electronics
19102 N. Creek Parkway, Suite 118
Bothell WA 98011
USA
TEL: 206 489-3400
FAX: 206 489-3411
Web: http://www.future.ca/

Pioneer-Standard Electronics
2800 156th Avenue S.E., Suite 100
Bellevue WA 98007
USA
TEL: 206 644-7500
FAX: 206 644-7300
Web: http://www.pios.com/

Wisconsin

Bell Industries
W. 226 N. 900 Eastmound
Waukesha WI 53186
Tel: 414 547-8879
Fax: 414 547-6547

Future Electronics
250 North Patrick Blvd., Suite 170
Brookfield WI 53045
Tel: 414 879-0244
Fax: 414 879-0250

Pioneer-Standard Electronics
120 Bishop's Way, Suite 163
Brookfield WI 53005
Tel: 414 784-3480
Fax: 414 784-8207

MICROCHIP

Factory Sales

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602-786-7200 Fax: 602-786-7277
Technical Support: 602 786-7627
Web: http://www.microchip.com

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508-480-9990 Fax: 508-480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972-991-7177 Fax: 972-991-8588

Dayton
Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714-263-1888 Fax: 714-263-1338

New York
Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 516-273-5305 Fax: 516-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong
Microchip Asia Pacific
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

India
Microchip Technology Inc.
India Liaison Office
No. 6, Legacy, Convent Road
Bangalore 560 025, India
Tel: 91-80-229-0061 Fax: 91-80-229-0062

Japan
Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa 222-0033 Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai
Microchip Technology
RM 406 Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hong Qiao District
Shanghai, PRC 200335
Tel: 86-21-6275-5700
Fax: 86 21-6275-5060

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C
Microchip Technology Taiwan
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-1189-21-5858 Fax: 44-1189-21-5835

France
Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Müchen, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-39-6899939 Fax: 39-39-6899883

4/3/98

MICROCHIP

Printed in the USA, 4/98

Microchip Technology Inc. • 2355 W. Chandler Blvd. • Chandler, Arizona USA • 602-786-7200 • FAX: 602-899-9210

Microchip Worldwide Sales and Distribution

Microchip Technology Inc. • 2355 West Chandler Blvd. • Chandler, Arizona 85224-6199
Tel: 602.786.7200 • Fax: 602.899.9210 • **See us on the Web:** www.microchip.com
Technical Support Hotline: 1.800.437.2767 U.S. & Canada; 602.786.7627 Worldwide