Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- External control provided for output polarity selection
- External control provided for selection of odd or even parity
- Two key roll-over operation
- N-key lockout
- Programmable coding with a single mask change
- Self-contained oscillator circuit
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

DESCRIPTION

The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION
40 LEAD DUAL IN LINE

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
</tr>
<tr>
<td>2</td>
<td>Frequency Control B</td>
</tr>
<tr>
<td>3</td>
<td>Frequency Control C</td>
</tr>
<tr>
<td>4</td>
<td>Shift Input</td>
</tr>
<tr>
<td>5</td>
<td>Control Input</td>
</tr>
<tr>
<td>6</td>
<td>Parity Invert Input</td>
</tr>
<tr>
<td>7</td>
<td>Parity Output</td>
</tr>
<tr>
<td>8</td>
<td>Data Output B8</td>
</tr>
<tr>
<td>9</td>
<td>Data Output B7</td>
</tr>
<tr>
<td>10</td>
<td>Data Output B6</td>
</tr>
<tr>
<td>11</td>
<td>Data Output B5</td>
</tr>
<tr>
<td>12</td>
<td>Data Output B4</td>
</tr>
<tr>
<td>13</td>
<td>Data Output B3</td>
</tr>
<tr>
<td>14</td>
<td>Data Output B2</td>
</tr>
<tr>
<td>15</td>
<td>Data Output B1</td>
</tr>
<tr>
<td>16</td>
<td>Strobe Output</td>
</tr>
<tr>
<td>17</td>
<td>VCC</td>
</tr>
<tr>
<td>18</td>
<td>VSS</td>
</tr>
<tr>
<td>19</td>
<td>Strobe Control Input</td>
</tr>
<tr>
<td>20</td>
<td>Data &amp; Strobe Invert Input</td>
</tr>
</tbody>
</table>

Top View

Frequency Control A X0
Frequency Control C X1
Shift Input X2
Control Input X3
Parity Invert Input X4
Parity Output X5
Data Output B8 X6
Data Output B7 X7
Data Output B6 X8
Data Output B5 X9
Data Output B4 X10
Data Output B3 X11
Data Output B2 X12
Data Output B1 X13
Strobe Output X14
VCC X15
VSS X16
Strobe Control Input X17
Data & Strobe Invert Input X18

Keyboard Matrix
Inputs
Outputs

BLOCK DIAGRAM
OPERATION

The AY-5-2376 contains (see Block Diagram) a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control inputs select one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and 9, the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

TIMING DIAGRAM

![Timing Diagram](image-url)

MINIMUM SWITCH CLOSURE = SWITCH BOUNCE + (88 X 1/f) + STROBE DELAY + STROBE WIDTH

MAXIMUM EXPECTED DETERMINED BY FREQUENCY OF OPERATION (EXTERNAL RC)

DETERMINED BY EXTERNAL RC MINIMUM TIME REQUIRED BY EXTERNAL CIRCUITRY
ELECTRICAL CHARACTERISTICS

Maximum Ratings

- **Vo1 and Voo** (with respect to Vee) -20V to 0.3V
- **Logic input voltages** (with respect to Vee) -20V to 0.3V
- **Storage Temperature** -65°C to +150°C
- **Operating Temperature Range** 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

- **Vcc** = +5 Volts ± 0.5 Volts,
- **Vgg** = -12 Volts ± 1.0 Volts, **Vgg** = GND.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clock Frequency</strong></td>
<td>f</td>
<td>10</td>
<td>50</td>
<td>100</td>
<td>KHz</td>
<td>See Block diagram footnote** for typical R - C values</td>
</tr>
</tbody>
</table>

**Data Input**

(Shift, Control, Parity invert, data & strobe invert).

- **Logic “0” Level**
  - **Vil**
  - **Vgg**
  - Typ: 0.8 V
- **Logic “1” Level**
  - **Vih**
  - **Vcc-1.5**
  - Typ: Vcc+0.3 V

| Shift & Control Input Current | IINSC | 15 | 36 | 60 | µA | Vcc=5V |
| Data, Parity Invert Input Current | INDP | 8 | 16 | 30 | µA | Vcc=0V |

**X Output (X0-X1)**

- **Logic “1” Output Current**
  - **IX1**
  - **80**
  - **150**
  - **400**
  - **μA**
  - **VOUT = Vcc**
  - **140**
  - **300**
  - **800**
  - **μA**
  - **VOUT = Vcc-1.3V**
  - **250**
  - **700**
  - **1500**
  - **μA**
  - **VOUT = Vcc-2.0V**
  - **500**
  - **1500**
  - **3000**
  - **μA**
  - **VOUT = Vcc-5V**
  - **140**
  - **300**
  - **800**
  - **μA**
  - **VOUT = Vcc-10V**

**Logic “0” Output Current**

- **IX0**
  - **13**
  - **27**
  - **65**
  - **μA**
  - **Vcc-1.3V**
  - **12**
  - **25**
  - **60**
  - **μA**
  - **Vcc-2.0V**
  - **5**
  - **10**
  - **40**
  - **μA**
  - **Vcc-5V**
  - **1**
  - **20**
  - **μA**
  - **Vcc-10V**

**Y Input (Y0-Y10)**

- **Trip Level**
  - **Vt**
  - **Vcc-5**
  - **Vcc-3**
  - **Vcc-2**
  - **V**
  - **Vcc**
  - **Y Input Going Positive**
  - **Hysteresis**
  - **ΔVt**
  - **.5**
  - **.9**
  - **1.4**
  - **V**
  - **Vcc**

**Selected Y Input Current**

- **IY5**
  - **30**
  - **60**
  - **160**
  - **μA**
  - **Vcc**
  - **IY26**
  - **54**
  - **130**
  - **μA**
  - **Vcc**

**Unselected Y Input Current**

- **IY15**
  - **15**
  - **30**
  - **80**
  - **μA**
  - **Vcc**

**Input Capacitance**

- **CIN**
  - **3**
  - **10**
  - **pF**
  - **at 0V**

**Switch Characteristics**

- **Minimum Switch Closure**
  - **-**
- **Contact Closure Resistance**
  - **Zcc**
  - **-**
  - **300**
  - **Ω**

**Strobe Delay**

- **Trip Level (Pin 19)**
  - **VSD**
  - **Vcc-4**
  - **Vcc-3**
  - **Vcc-2**
  - **V**
  - **See Note 1**

**Hysteresis**

- **VSD**
  - **.5**
  - **.9**
  - **1.4**
  - **V**
  - **With 680K to Vss**

**Data Output (B1-B6)**

- **Logic “0”**
  - **-**
  - **-**
  - **0.4**
  - **V**
  - **Iol = 1.6mA**

**Logic “1”**

- **-**
  - **Vcc-1**
  - **-**
  - **V**
  - **Iol = 100 µA**

**Power**

- **Icc**
  - **-**
  - **5**
  - **10**
  - **mA**
  - **Vcc = +5V**

- **Icc**
  - **-**
  - **5**
  - **10**
  - **mA**
  - **Vss = -12V**

**NOTE**

1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = eleven.

**Typical values at +25°C and nominal voltages.**
TYPICAL CHARACTERISTIC CURVES

STROBE DELAY C1

TYPICAL OUTPUT ON RESISTANCE (R_{ON}) VS. GATE BIAS VOLTAGE (V_{GS})

OSCILLATOR FREQUENCY VS. C2

TYPICAL POWER CONSUMPTION (mW) VS. TEMP (°C)

KEYBOARD INPUT
TO INTERNAL GATING

"Y" INPUT STAGE FROM KEYBOARD

"X" OUTPUT STAGE TO KEYBOARD

STATIC CHARGE PROTECTION DEVICE

"Y" INPUT STAGE FROM KEYBOARD

STATIC CHARGE PROTECTION DEVICE

"X" OUTPUT STAGE TO KEYBOARD
Illustrated using a Logic "O" on the Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6).

NOTE 1: This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

EXAMPLE

B1 B2 B3 B4 B5 B6 B7 B8 PARITY

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1" (SEE DATA B1—B8)
LOGIC "1" = +5V
LOGIC "0" = GND

(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION X0 — Y9 AND PROPER MODE SELECTION)

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

<table>
<thead>
<tr>
<th>DATA AND STROBE INVERT INPUT (PIN 20)</th>
<th>CODE ASSIGNMENT CHART</th>
<th>DATA OUTPUTS (B1-B8)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
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<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>

PARITY INVERT TRUTH TABLE

<table>
<thead>
<tr>
<th>PARITY INVERT INPUT (PIN 6)</th>
<th>CODE ASSIGNMENT CHART</th>
<th>PARITY OUTPUT (PIN 7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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<td>0</td>
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<tr>
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<tr>
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</tbody>
</table>

STROBE INVERT TRUTH TABLE

<table>
<thead>
<tr>
<th>DATA AND STROBE INVERT INPUT (PIN 20)</th>
<th>INTERNAL STROBE</th>
<th>STROBE OUTPUT (PIN 16)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>1</td>
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<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

MODE SELECTION

S C  =  N
S C  =  S
S C  =  C
S C  =  C